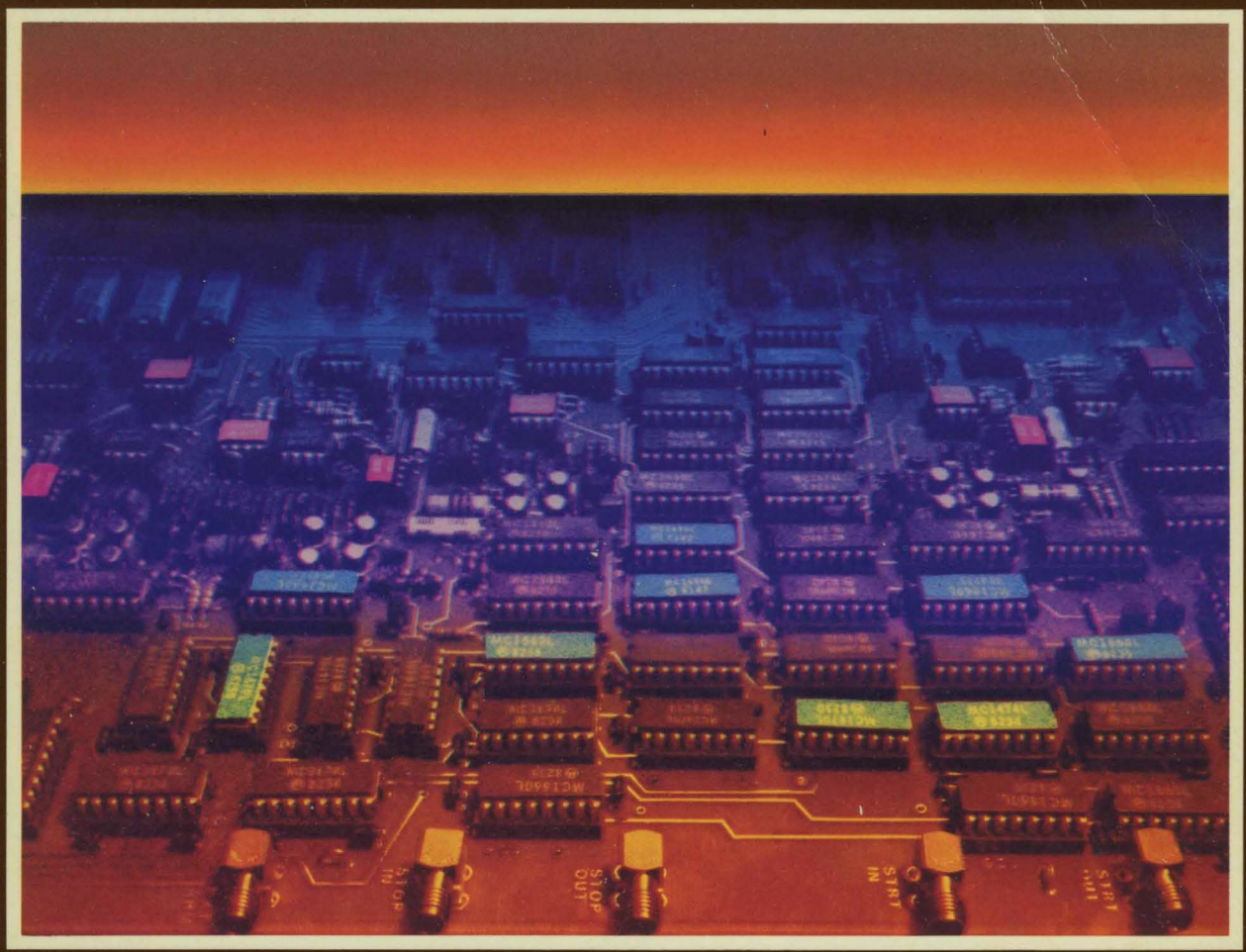
HB205R1

MOTOROLA INC.



MECL SYSTEM DESIGN HANDBOOK

MECL

SYSTEM DESIGN HANDBOOK

Fourth Edition

Compiled by the Computer Applications Engineering Department

Author

William R. Blood, Jr.

MOTOROLA *Semiconductor Products Inc.*

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this book has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

MECL, MECL I, MECL II, MECL III, MECL 10K/10KH, MTTL, MTTL III, Micro T, and MDTL are trademarks of Motorola Inc.

Fourth Edition
Second Printing

Printed in U.S.A.

PREFACE

In response to the demand for higher performance systems, engineers are looking at digital integrated circuit families which are faster than the popular TTL types. Motorola's Emitter Coupled Logic (MECL) circuits have the characteristics to meet the performance requirements for present and future systems. MECL 10K/10KH are ideal for computer and communications systems, while state-of-the-art instrumentation equipment uses MECL III and MECL 10KH.

As circuit speeds increase, wiring rules and system design techniques must be adjusted accordingly. Designing with MECL is no more difficult than designing high performance equipment with slower forms of logic. High performance system design for any form of logic, however, does require an understanding of the factors which affect system performance. In fact, many of the MECL features such as transmission line drive capability, complementary outputs, Wired-OR, and versatile logic functions can add as much to system performance as the short propagation delays and high toggle rates.

In the past, several articles and application notes have been written about MECL circuits and systems. However, there was a need for a book which would completely define MECL operation. This book has been written to give the designer the information to establish design rules for his own high performance systems.

The information in this book is based on equations derived from electronic theory, laboratory tests, and inputs from MECL users. All of the rules and tables are for conservative system design with MECL circuits. It is important to realize that the circuits can operate properly under conditions much more adverse than suggested in this book.

In addition to the technical contributors, Jon DeLaune, Jerry Prioste and Cary R. Champlin, the author would like to thank Lloyd Maul, Mike Lee, Reg Hamer, Don Murray, Mike Stowe and Tom Balph whose knowledge of MECL has added to the completeness and accuracy of this book. Finally, great appreciation is due to the many technicians, engineers, and managers who took their valuable time to read all or part of this book as it was developed.

Table of Contents

Introduction

What is MECL?

The term MECL identifies Motorola's emitter coupled logic. Emitter coupled logic is a non-saturating form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speed operation. "Emitter Coupled" refers to the manner in which the emitters of a differential amplifier within the integrated circuit are connected. The differential amplifier provides high impedance inputs and voltage gain within the circuit. Emitter follower outputs restore the logic levels and provide low output impedance for good line driving and high fanout capability.

History of MECL

Motorola has offered MECL circuits in five logic families: MECL I, MECL II, MECL III, MECL 10,000 (MECL 10K), and MECL 10H000 (MECL 10KH).

The MECL I family was the first digital monolithic integrated circuit line produced by Motorola. Introduced in 1962, MECL I was considerably beyond the state-of-the-art at that time. Several years passed before any other form of logic could equal the 8 ns gate propagation delays and 30 MHz toggle rates of MECL I. As a result of its reliability and performance, MECL I was designed into many advanced systems.

In 1977 MECL I was phased out of production. Features of the more advanced MECL III and 10K favor their being used in new designs. For example, MECL I required a separate bias driver package to be connected to each logic function. This means increased package count and extra circuit board wiring. Also the 10-pin packages used for MECL I limit the number of gates per package and the number of gate inputs. No provision was made for operation of MECL I with transmission lines, as they were unnecessary with the 8 ns rise and fall times.

In 1966 Motorola introduced the more advanced MECL II. The basic gate featured 4 ns propagation delays and flip-flop circuits that would toggle at over 70 MHz. MECL II immediately set a new standard for performance that has been equaled by non-ECL logic only with the introduction of Schottky TTL in 1970.

Motorola continued with the development of MECL II and flip-flop speeds were increased first to 120 MHz for the JK circuit, and then to 180 MHz for the type D flip-flop. To drive these high speed flip-flops, high speed line drivers were introduced with 2 ns propagation delays and 2 ns rise and fall times. With 2 ns edges, transmission lines could be used to preserve the waveforms and limit overshoot and

ringing on longer lines. Consequently, a part was designed to drive 50-ohm lines. Because of the significant speed increase of the line drivers and high speed flip-flops over the basic MECL II parts, these circuits are commonly called MECL II-1/2, although they are part of the MECL II family.

MECL II circuits have a temperature compensated bias driver internal to the circuits (except for the line receiver which requires no internal bias). The internal bias source simplifies circuit interconnections and tracks with both temperature and supply voltage to retain noise margin under varied operating conditions.

Complex functions became available in MECL II when trends shifted toward more complicated circuits. The family had adders, data selectors, multiplexers, decoders and a Nixie* tube decoder/driver. MECL II was discontinued in 1979 superseded by MECL III, MECL 10K and MECL 10KH.

Motorola's continuing development of ECL made possible an even faster logic family. As a result, MECL III was introduced in 1968. Its 1 ns gate propagation delays and greater than 500 MHz flip-flop toggle rates remain the industry leaders. The 1 ns rise and fall times require a transmission line environment for all but the smallest systems. For this reason, all circuit outputs are designed to drive transmission lines and all output logic levels are specified when driving 50-ohm loads. Because of MECL III's fast edge speeds, multi-layer boards are recommended above 200 MHz. For the first time with MECL, internal input pulldown resistors are included with the circuits to eliminate the need to tie unused inputs to V_{EE}. The Hi-Z 50 kΩ input resistors are used with transmission lines for most applications. MECL III's popularity is with high speed test and communications equipment.

Trends in large high speed systems showed the need for an easy to use logic family with 2 ns propagation delays. To fill this requirement, Motorola introduced the MECL 10K series in 1971. In order to make the circuits comparatively easy to use, edge speed was slowed to 3.5 ns (10%-90%) while the important propagation delay was held to 2.0 ns. The slow edge speed permits use of wire wrap and standard printed circuit lines. However, the circuits are specified to drive transmission lines for optimum performance.

Because of technological advances in processing as well as market demands for even higher performance devices, Motorola introduced its newest high-speed ECL family, MECL 10KH in 1981. This family provides propagation delays of 1 ns with edge speeds slowed to 1.8 ns (10-90%). These speeds, which are attained with no increase in power over MECL 10K, are due to both advanced circuit design techniques and Motorola's new oxide isolated process called MOSAIC (Motorola Oxide Self Alligned Implanted Circuits). This process allows smaller device geometries, improved f_Ts (greater bandwidth) and reduced paracitic capacitances.

To enhance existing systems, many of the MECL 10KH devices are pinout/functional duplications of the MECL 10K family. Also, MECL 10K/10KH are provided with logic levels that are completely compatible with MECL III and the MECL Macrocell Arrays to facilitate using all families in the same system. Another important feature of MECL10K/10KH is the significant power reduction over both MECL III and the older MECL II. Also, because of this low gate power and advanced circuit design techniques, the MECL 10KH family has many new functions not available by the other families. Although MECL 10K continues to be the most widely used ECL family in the industry, MECL 10KH is setting new standards in speed and power.

*T.M. – Burroughs Corp.

Why Use MECL?

Circuit speed is, of course an obvious reason for designing with MECL. MECL 10K/10KH offer shorter propagation delays and higher toggle rates than any non-ECL type of logic. Equally important to the circuit speed are the characteristics of MECL circuits which permit entire systems to operate at high speeds.

The ability of the faster MECL families to drive transmission lines becomes increasingly important in larger and faster systems. While a transmission line environment imposes some additional design rules and restrictions, the advantages of longer signal paths, better fanout, improved noise immunity, and faster operation, often more than compensate for the restrictions.

When using MECL 10K/10KH without transmission lines, the high input impedances permit the use of series-damping resistors to increase wiring lengths and to improve waveforms. Unlike non-ECL forms of logic, MECL circuits have constant power supply requirements, independent of operating frequency. This simplifies power supply design, since circuit speed need not be considered a variable. At fast circuit speeds MECL can offer a considerable power saving over the other types of logic.

In addition to faster operation, the line driving features of MECL circuits can be exploited to improve system performance. For one, the parts specified to drive transmission lines will drive coaxial cables over distances limited only by the bandwidth of the cable. In addition, the shielding in coaxial cable gives good isolation from external noise.

More economical than using coaxial cable, is the ability of the MECL circuits to differentially drive and receive signals on twisted pair lines. Using this technique, signals have been sent over twisted pair lines up to 1000 feet in length.

The complementary outputs and Wired-OR capabilities of MECL circuits result in faster system operation with reduced package count and a power saving. The complementary outputs are inherent in the circuit design and both outputs have equal propagation delay. This eliminates the timing problems associated with using an inverter to get a complement signal. The logic OR function is obtained by wiring circuit-outputs together. The propagation delay of the Wired-OR connection is much less than a gate function and can save power, as only one pulldown resistor or termination is required per Wired-OR.

Another advantage when designing with MECL is the low noise generated by the circuits. Unlike totem pole outputs, the emitter follower does not generate a large current spike when switching logic states, so the power lines stay comparatively noise free. The low current-switching in signal paths, relatively small voltage swing (typically 800 mV), and low output impedances, cut down crosstalk and noise.

Generated noise is also reduced by MECL's relatively slow rise and fall times. For each MECL family the edge speed is equal to or greater than the propagation delay. The low noise associated with MECL is especially important when the logic circuits are to be used in a system which contains low level analog or communications signals.

The flexibility of the MECL line receivers and Schmitt triggers to act as linear amplifiers leads to many functions that may be performed with standard MECL circuits. For example, in addition to amplifying low level signals to MECL levels, these MECL circuits can be used as crystal oscillators, zero crossing detectors, power buffers, Schmitt triggers, RF and video amplifiers, one-shot multivibrators, etc.

The Advantages of MECL

1. Highest speed IC logic available
2. Low cost
3. Low output impedance
4. High fanout capability
5. Constant supply current as a function of frequency or logic state
6. Very low noise generation
7. Complementary logic outputs save on package count
8. Low crosstalk between signal leads
9. All outputs are buffered
10. Outputs can be tied together giving the Implied-OR function
11. Common mode rejection of noise and supply variations is 1 V or greater for differential line receiving
12. Bias supplies are internal, allowing MECL use with a single power supply
13. Minimal degradation of parameters occurs with temperature variations
14. Large family of devices yields economical designs
15. Power dissipation can be reduced through use of Implied-OR and the "Series Gating" technique
16. Easy data transmission over long distances by using the balanced twisted pair technique with standard parts
17. Constant noise immunity versus temperature
18. Best speed-power product available
19. All positive logic functions are available
20. Adapts easily to MSI and LSI techniques

MECL Areas of Application

1. Instrumentation
2. High speed counters
3. Computers
4. Medical electronics
5. Military systems
6. Large real-time computers
7. Aerospace and communication satellite systems
8. Ground support system
9. High speed A/D conversion
10. Digital communication systems
11. Data transmission (twisted pair)

12. Frequency synthesizers
13. Phase array radar
14. High speed memories
15. Data delay lines

Purpose of This Book

Rules and guidelines for using the various MECL families comprise the subject matter of this book. Because of edge speed and bit rate capabilities, each family has differing system requirements. The family name will therefore be referenced for the examples and figures in the text, whenever applicable. The information in this book is meant to apply to MECL III and MECL 10K/10KH. The information about MECL 10K/10KH will also apply to the M10800 LSI processor family. This book aims at giving the reader an understanding of the MECL families, as well as the knowledge needed to confidently design with and use MECL.

Chapter 1 discusses the operation of MECL circuits and the characteristics of the various families. It also shows methods for internally connecting the basic gates to provide efficient complex functions. Of more importance to the user is Chapter 2 – a list of rules providing a condensed reference for *using* the various MECL families.

Chapters 3, 4, 5, and 6 elaborate on those rules giving a technical background for good system design and presenting test results showing MECL circuits in various modes of operation. Chapter 3 describes circuit-to-circuit interconnections on a card. Both open wire and transmission line techniques are covered. Chapter 4 expands the wiring techniques to show methods for card-to-card and panel-to-panel interconnections. Chapter 5 elaborates on power distribution, showing how voltage drops and power line noise affect noise immunity. Chapter 6 discusses thermal considerations. Attention is given to the problems of calculating chip temperature, removing heat from the system, and to the effect of thermal differences on noise immunity.

Chapter 7 provides background necessary for understanding transmission lines as they apply to MECL. Derivations of equations are shown, along with test results correlating with the theoretical analysis. This chapter should be especially useful when selecting a transmission line impedance and when determining the effect of fanout or stray capacitance on the line.

Chapter 8 contains application ideas for MECL circuits. Included are methods for interfacing various logic families with MECL, and numerous useful circuits designed with MECL for high performance.

Finally, a brief appendix illustrates some of the peripheral hardware and components of use in MECL Systems.

CHAPTER 1 MECL Families

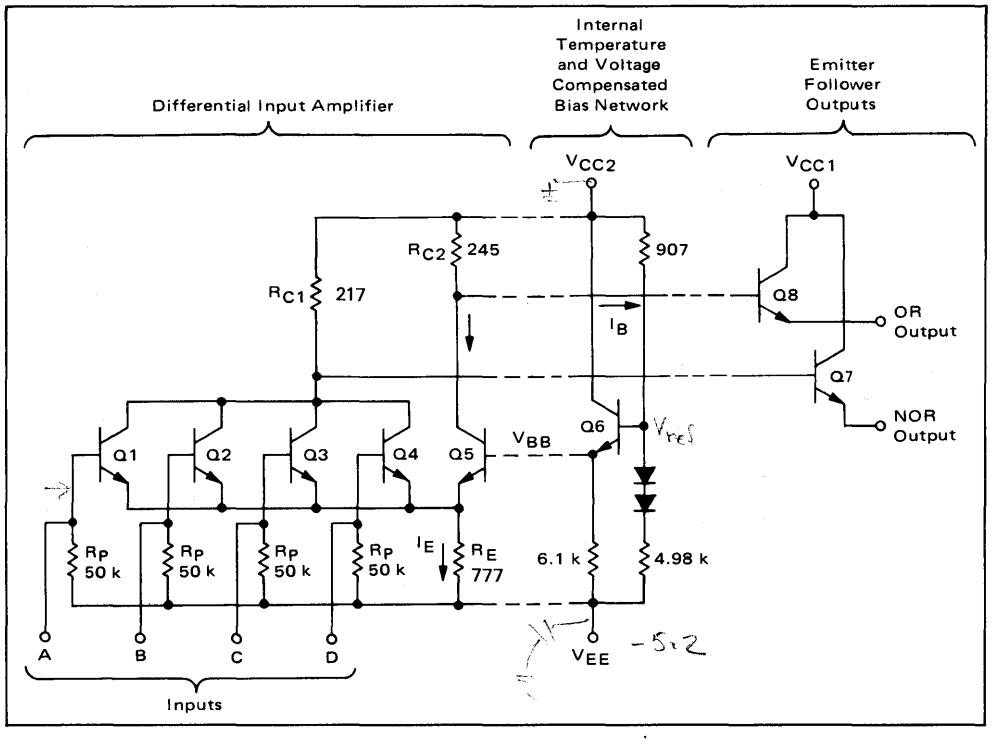
The Basic MECL Gate

An understanding of the basic circuits used in the construction of a logic family is important in order to successfully design and trouble-shoot a system which uses the family. This chapter describes MECL circuits, compares MECL families, and gives some suggested rules for using MECL circuits in system design.

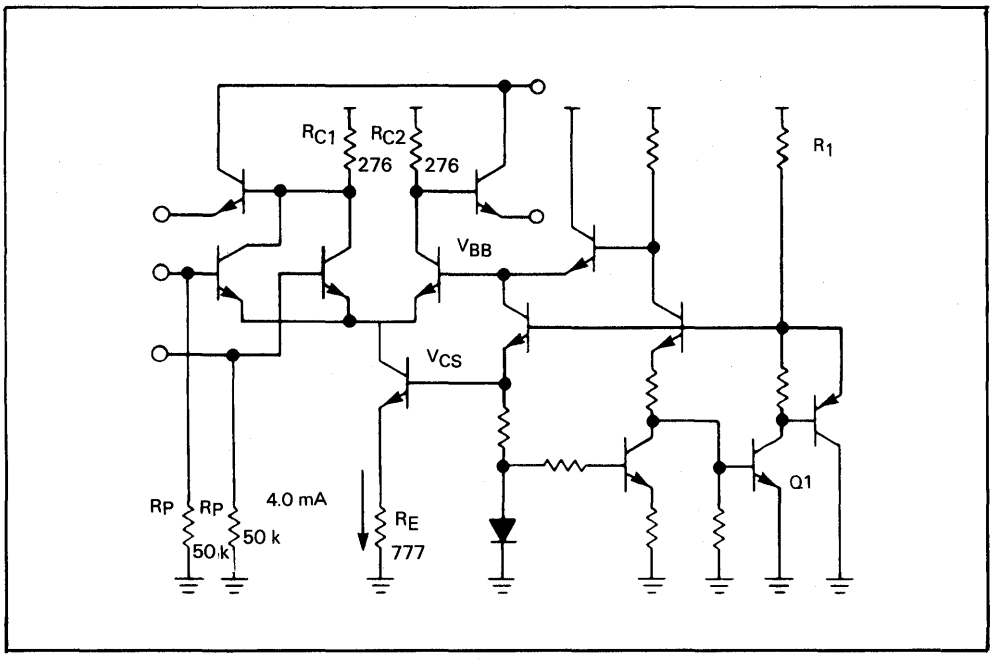
Figure 1-1a shows a typical MECL 10K gate, — the basic gate circuit for the MECL 10K family. The figure shows the separate functional circuits within the gate.

The differential amplifier section contains the current steering element that provides the actual logic gating of the circuit. It also provides the voltage gain necessary for a narrow linear threshold region.

1-1a: MECL 10K Basic Gate



1-1b: MECL 10KH Basic Gate



An internal temperature and voltage compensated bias driver supplies a reference voltage for the differential amplifier. The bias voltage, V_{BB}, is set at the midpoint of the signal logic swing. With the recommended - 5.2 volts supply voltage and 25° C ambient temperature, V_{BB} is - 1.29 volts dc for either MECL 10K/ 10KH or MECL III. The diodes in the voltage divider line, together with Q6, provide temperature compensation by maintaining a level consistent with the midpoint of the logic levels despite changing temperatures.

One additional feature of the bias supply is its ability to track supply voltage changes. Consequently MECL 10K gates, for example, are specified to operate from a - 5.2 volt ± 10% supply. In fact, they are capable of working over a much wider range (- 3.0 to - 8.0 volts) although ac performance would be degraded.

A typical MECL 10KH gate can be seen in Fig. 1-1b. This figure shows that both the bias regulator and the emitter resistor source of the MECL 10K gate has been replaced by a voltage regulator and a constant current source, respectively, in the MECL 10KH gate.

The new voltage regulator controls both variations in the output voltage as well as the AC characteristics of the devices. The constant current source allows the use of matched collector resistors which produces better matched delays, matched output tracking rates with temperature and less variation in the output voltage level with changes in the power supply. There is also a considerable improvement in noise margins over MECL 10K. MECL 10KH is specified to operate from a - 5.2 volt ± 5% power supply.

The emitter followers are output drivers. They provide level shifting from the differential amplifier to MECL output levels, and provide a low output impedance for driving transmission lines. MECL 10K/10KH and MECL III circuits use open emitter outputs. The reason is that since these circuits are designed for use with transmission lines, and since the line termination provides an output load, internal pulldown resistors would be a waste of power.

MECL 10K/10KH and MECL III circuit families, designed to drive transmission lines, have two V_{CC} power voltage inputs. V_{CC1} is used to supply current to the output drivers, while V_{CC2} supplies the remainder of the circuit. Separate V_{CC} lines are used to eliminate crosstalk between circuits in a package. More important, the use of two lines speeds up circuit performance by eliminating a voltage spike which otherwise would occur on the bias voltage, V_{BB}, caused by the relatively heavy currents associated with transmission lines. Each V_{CC} pin should be connected to the system ground by as short a path as possible (all V_{CC} pins are connected to the same system ground).

The input pulldown resistors shown in Figure 1-1a and b are characteristic of MECL 10K/10KH and MECL III. MECL 10K/10KH and MECL III use 50 k Ω resistors to drain off the input transistor leakage current. These resistors hold unused inputs at a fixed zero level, so unused inputs are left open.

MECL Logic Levels

The following calculations illustrate the current switching operation of a MECL 10K gate. Similar calculations may be performed for the other MECL families by substituting appropriate resistor values and voltage levels.

When all gate inputs are at a voltage, V_{in}, equal to a logic $\emptyset$ level, $|V_{IL}\ min| \geq V_{in} \geq V_{IL}\ max|$, the input transistors Q1 through Q4 in Figure 1-1a will not be conducting current, because the commn emitter point of these four transistors is at about -2.09 V: i.e., $V_{BB} + V_{BEQ5} \approx -1.29\ V + (-0.80\ V)$. This is not enough forward bias (base to emitter) on Q1 through Q4 for conduction. Thus, current flows through R_{C2}, Q5, and R_E. This current, $I_{E\emptyset}$, is:

$$I_{E\emptyset} = \frac{V_{EE} - (V_{BB} + V_{BE})}{R_E} \approx -4.0\ mA.$$

The voltage drop at the collector resistor. R_{C2}, may be calculated as:

$$V_{RC2} = I_{E\emptyset}R_{C2} + I_BR_{C2} \approx (-4.0\ mA) \bullet (245\ \Omega) = -0.98V.$$

The output transistor base current, I_B, is small compared to the switch current, so the second term above can be ignored.

The OR output is then obtained through an emitter-follower, Q8, which cuts the output level by one base-emitter drop, giving a voltage level:

$$V_{OL\ OR} = V_{RC2} + V_{BE},$$

where: V_{BE} = base to emitter drop on Q8, with logic zero current level (i.e., 6 mA thru Q8).

So:

$$V_{OL\ OR} \approx -0.98\ V + (-0.77\ V) \approx -1.75\ V,$$

typical at $T_A = 25°C$.

The base of the NOR output emitter-follower, Q7, is at about -0.05 V, yielding an output of -0.89 V typical, at an output device current level of 22.5 mA and $T_A = 25°C$. (These output voltage and current levels assume 50-ohm loads to a terminating voltage, V_{TT}, of -2.0 V).

If one or more of the gate inputs is switched to a voltage level, V_{in}, equal to a nominal logic 1 level, $|V_{IH\ min}| \geq |V_{in}| \geq |V_{IH\ max}|$, a current I_{E1} flows through R_{C1}, Q1-Q4, and R_E. This current is:

$$I_{E1} = \frac{V_{EE} - (V_{in} + V_{BE})}{R_E} \approx -4.51\ mA,$$

where: $V_{in} = -0.89\ V$

$V_{BE} = -0.80\ V$

The current flow through R_{C1} produces a voltage at the collector nodes of Q1 through Q4:

$$V_{RC1} \approx I_{E1}R_{C1} = (-4.51\ mA)\bullet(217\ \Omega) \approx -0.98\ V.$$

Finally, the output is obtained through an emitter follower, Q7, which drops the collector voltage level one base-emitter drop, so that:

$$V_{OL\ NOR} = V_{RC1} + V_{BE}\ (\text{output device at 6 mA})$$

$$\approx -0.98\ V + (-0.77\ V) = -1.75\ V,$$

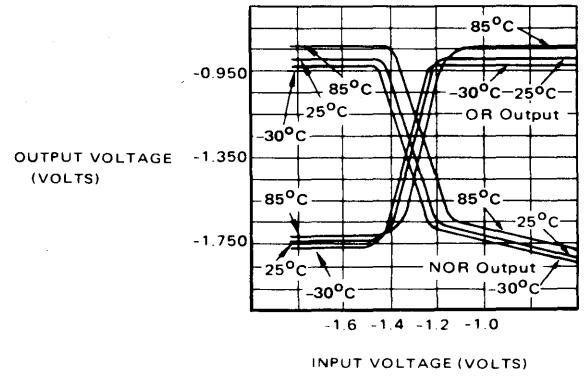
typical at $T_A = 25°C$.

The transfer curves in Figures 1-2(a) and (b) indicate the behavior of the MECL 10K gate while switching. Note from the data in Figure 1-3 and from the NOR transfer characteristic: for V_{in} increasing from $V_{IL\ min}$ to $V_{ILA\ max}$, the output remains at a high level. When V_{in} increases from $V_{ILA\ max}$ to $V_{IHA\ min}$, the NOR output will switch to a low level. Then, as the input continues more positive than $V_{IHA\ min}$, the output continues more negative with a slope of about -0.24. This is caused by the collector input node going more negative because of increasing collector current as V_{in} goes more positive.

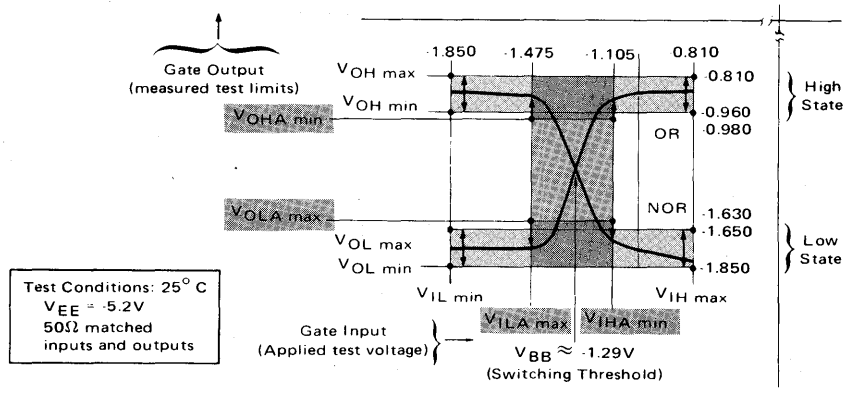
If the input continues in the positive direction, saturation will be reached at an input of about -0.4 volts. Beyond that point, the base-collector junction is forward biased to saturation and the collector voltage and output will go more positive with the increasing input level. Since the saturation point is well above $V_{OH\ max}$, operation in this mode will not occur in normal system operation. The OR output level depends on Q5's collector voltage (cf Fig. 1-1a). This output is unaffected by input levels except in the active transfer region.

Fig. 1-2 (c) and (d) demonstrates the switching behavior of MECL 10KH and Fig. 1-3 (c) lists the DC test parameters for 10KH. As can be seen in Fig 1-2 (d) the NOR output stays level after V_{in} reaches $V_{IH\ min}$ as opposed to MECL 10K which slopes downward.

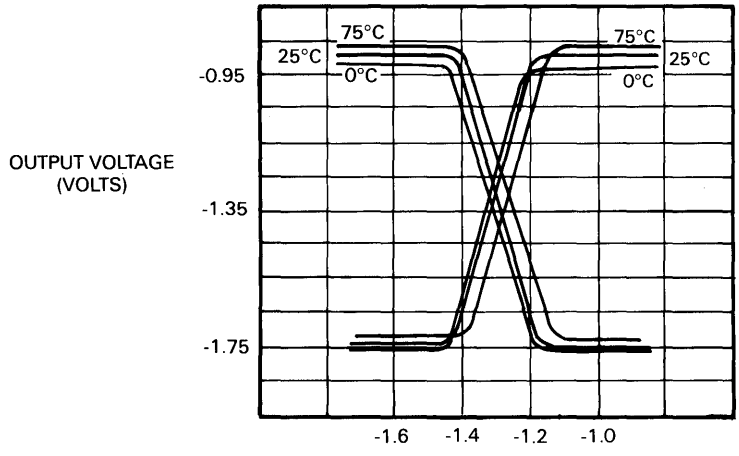
1-2; MECL 10K Transfer Characteristic and Specification Points



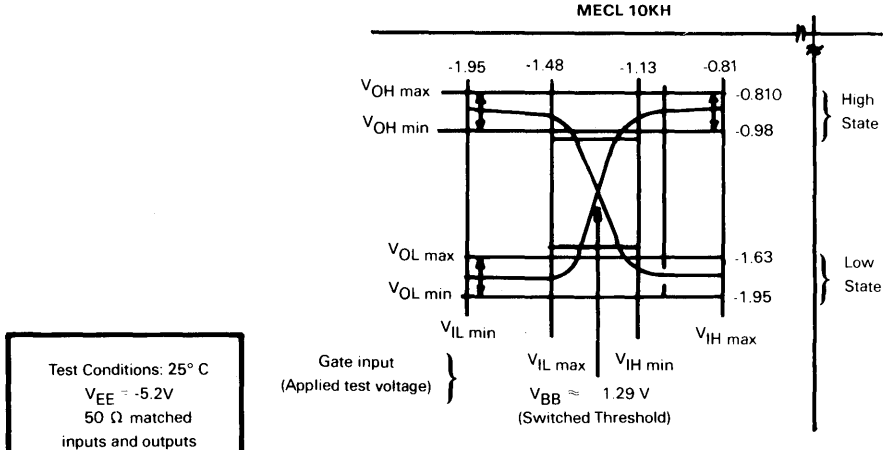
(a) TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE (MECL 10K)



(b) MECL TRANSFER CURVES (MECL 10K EXAMPLE) and SPECIFICATION TEST POINTS



(c) TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE (MECL 10KH)



(d) MECL 10KH TRANSFER CURVES and SPECIFICATION TEST POINTS.

1-3; MECL 10K/10KH and MECL III Specified Logic Levels and Thresholds

Forcing Function	Parameter	-55°C①	-30°C②	0°C②	25°C②	25°C①	75°C③	85°C②	125°C①	Unit
		MC10500 MC10600 MCM10500	MC10100 MC10200 MC10800	MCM10100	MC10100 MC10200 MC10800 MCM10100	MC10500 MC10600 MCM10500	MCM10100	MC10100 MC10200 MC10800	MC10500 MC10600 MCM10500	
V_{IHmax} =	V_{OHmax}	-0.880	-0.890	-0.840	-0.810	-0.780	-0.720	-0.700	-0.630	Vdc
	V_{OHmin}	-1.080	-1.060	-1.000	-0.960	-0.930	-0.900	-0.890	-0.825	
V_{IHAmin}	V_{OHAmin}	-1.100 -1.255#	-1.080 -1.205	-1.020 -1.145#	-0.980 -1.105	-0.950 -1.105	-0.920 -1.045	-0.910 -1.035	-0.845 -1.000	Vdc
V_{ILAmax}		-1.510	-1.500	-1.490	-1.475	-1.475	-1.450	-1.440	-1.400	Vdc
	V_{OLAmax}	-1.635	-1.655	-1.645	-1.630	-1.600	-1.605	-1.595	-1.525	
	V_{OLmax}	-1.655	-1.675	-1.665	-1.650	-1.620	-1.625	-1.615	-1.545	Vdc
V_{ILmin} =	V_{OLmin}④	-1.920	-1.890	-1.870	-1.850	-1.850	-1.830	-1.825	-1.820	
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.5	0.3	0.3	0.3	μA

NOTES: ①MC10500, MC10600, and MCM10500 series specified driving 100 Ω to -2.0 V.
②MC10100, MC10200, MC10800 and MCM10100 series specified driving 50 Ω to -2.0 V.
③Memories (MCM10100) specified 0-75°C for commercial temperature range, 50 Ω to -2.0 V. Military temperature range memories (MCM10500) specified per Note 1.
④Special circuits such as MC10123, and MC10800 family bus outputs have lower than normal V_{OLmin}. See individual data sheets for specific values.
#The MCM10149 specified V_{IHA} min @ -55°C to be -1.175 V and @ 0°C to be -1.130 V

Each MECL 10K series device as been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuits is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = -5.2V ± 0.010 V.

(a) MECL 10K DC TEST PARAMETERS

Forcing Function	Parameter	-30°C	25°C	85°C	Unit
V_{IHmax} =	V_{OHmax}	-0.875	-0.810	-0.700	Vdc
	V_{OHmin}	-1.045	-0.960	-0.890	
V_{IHAmin}	V_{OHAmin}	-1.065 -1.180	-0.980 -1.095	-0.910 -1.025	Vdc
V_{ILAmax}		-1.515	-1.485	-1.440	Vdc
	V_{OLAmax}	-1.630	-1.600	-1.555	
	V_{OLmax}	-1.650	-1.620	-1.575	Vdc
V_{ILmin} =	V_{OLmin}	-1.890	-1.850	-1.830	
V_{ILmin}	I_{INLmin}	0.5	0.5	0.3	μA

NOTE: All outputs loaded 50 Ω to -2.0 Vdc except MC1648 which has an internal output pulldown resistor.

(b) MECL III DC TEST PARAMETERS

ELECTRICAL CHARACTERISTICS

Each MECL III series device has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = -5.2 V ± 0.10 V.

1-3 (continued) (C) MECL 10KH DC TEST PARAMETERS

Forcing Function	Parameter	0°C	25°C	75°C	Unit
$V_{IH\ max}$	$V_{OH\ max}$ $V_{OH\ min}$	-0.84 -1.02	-.81 -.98	-.735 -.92	Vdc
$V_{IL\ min}$	$V_{OL\ max}$ $V_{OL\ min}$	-1.63 -1.95	-1.63 -1.95	-1.60 -1.95	Vdc
$V_{IL\ min}$	$I_{INL\ min}$	0.5	0.5	0.3	μA

Suffice it to say that while the manufacture of MECL circuits is not a primary concern of the user, nevertheless ease of manufacture does translate directly into end product cost. Although not as easy to build as some slower logic families because of smaller transistor geometries, MECL does have some features which facilitate processing. First, the voltage gain of the basic gate circuit (approximately 4.0 for MECL 10K) is essentially independent of transistor beta. So transistor beta can be allowed to vary from a low of about 70 in high speed MECL to a high in excess of 300, which permits easy processing limits. Second, the output voltage levels depend on diode drops for a high output, and diode drops and resistor ratios for a low output. Resistance ratios can be held to within ±5% even though absolute values vary by ± 20%. Again, this eases processing.

Third, since the transistors used do not saturate, the gold doping which is commonly required to decrease storage time is not required in MECL processing; therefore yields are better. Fourth, collector-emitter voltages are low, due to circuit design, again relaxing processing restrictions. Such advantages, together with Motorola's ability to control processing, permit high volume production of all MECL circuits. In effect, this means low-cost high performance circuits for the designer.

Noise Margin

MECL 10K and MECL III

Noise margin is a dc voltage specification which measures the immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worse case input logic level ($V_{IHA\ min}$ or $V_{ILA\ max}$) and the guaranteed worst case output ($V_{OHA\ min}$ or $V_{OLA\ max}$) for those inputs. Figure 1-3 lists the worst case limits for MECL 10K/10KH and MECL III.

High level noise margin is obtained by subtracting ($V_{IHA\ min}$) from ($V_{OHA\ min}$); similarly, low level noise margin is ($V_{ILA\ max}$) minus ($V_{OLA\ max}$). Worst-case noise margin is guaranteed to be at least 0.125 volts for MECL 10K and 0.115 volts for MECL III in dual in-line packages. Using typical output voltage levels for MECL circuits, noise margins are usually better than guaranteed — by about 75 millivolts.

MECL 10KH

The MECL 10KH family has only one set of output voltages (V_{OH} and V_{OL}) with minimum and maximum values specified. The minimum value of V_{OH} and the maximum value of V_{OL} of the MECL 10KH family is synonomous with the V_{OHA} and V_{OLA} specifications of the MECL 10K family.

The V_{OH} values for the MECL 10KH circuits are equal to or better than the MECL 10K levels at all temperatures. Input voltages ($V_{IH\ min}$ and $V_{IL\ max}$ for MECL 10KH,

which are synonomous with V_{IHA} and V_{ILA} of MECL 10K) are also improved. These improvements have resulted in a "1" level noise margin equal to the "0" level noise margin of 150 mV. The reduction in operating temperature range for MECL 10KH and the improvement in tracking rate allow for a lower V_{OL} level for MECL 10KH (-1950 m V instead of -1850 m V for MECL 10K). The change in this level does not affect system noise margins. Although some of the interface levels change with temperature, the changes in voltage levels are well within the tolerance ranges that would keep the families compatible. Fig. 1-4 lists some noise margins for V_{EE} supply variations.

Fig. 1-4 — NOISE MARGIN versus POWER-SUPPLY CONDITIONS

Parameter		V_{EE} -10% Typ	Min	V_{EE} -5% Typ	Min	V_{EE} Typ	Min	V_{EE} +5% Typ	Min
Noise Margin High	10KH	224	150	227	150	230	150	233	150
V_{NH} (mV)	10K	127	47	166	86	205	125	241	164
Noise Margin Low	10KH	264	150	267	150	270	150	273	150
V_{NL} (mV)	10K	223	103	249	129	275	155	301	181

*Temp 0 to 75° C

A second noise parameter of interest to the designer is obtained by cascading worst case gates and measuring the minimum "noise" input that will propagate through the gates. This measurement is more indicative of actual system operation than dc noise margin, and is often referred to as "noise immunity" or "ac noise immunity". Testing has shown that this "noise immunity" is typically at least 40 millivolts greater than the dc noise margin specified by voltage levels. However, ac noise immunity is rather difficult to measure. Consequently it is not specified on the data sheets.

In system design, the user is concerned with noise margin when devices at different temperatures and different power supply voltages interface with each other. Figure 1-3 tabulates the worst case change in logic levels as a function of temperature. Equally important is the change in output levels as a function of supply voltage (cf Figure 5-2). The logic 1 levels are relatively independent of power supply voltage, and the change in the output level is typically less than 0.05 of the V_{EE} change. The change in the $\emptyset$ level is a function of the resistor ratios in the current switch and is typically 0.25 of the V_{EE} change. These values illustrate the rejection of power supply variations that is characteristic of MECL. Detailed information on noise margin changes due to power supply and temperature variations is given in Chapters 5 and 6.

MECL 10KH and MECL 10K compatibility is demonstrated below. The method for determining compatiblity is to show acceptable noise margins for MECL 10KH, MECL 10K and mixed MECL 10K/MECL 10KH systems. The assumption is that the families are compatible if the noise margin for a mixed system is equal to or better than the same system using only MECL 10K series.

Using an all MECL 10K system as a reference, three possible logic mixes must be considered: MECL 10K driving MECL 10KH; MECL 10 KH driving MECL 10K; and MECL 10KH driving MECL 10KH. The system noise margin for the three configurations can now be calculated for the following cases (see fig. 1-5).

In Case 1, the system uses multiple power supplies, each independently voltage regulated to some percentage tolerance. Worst case is where one device is at the plus

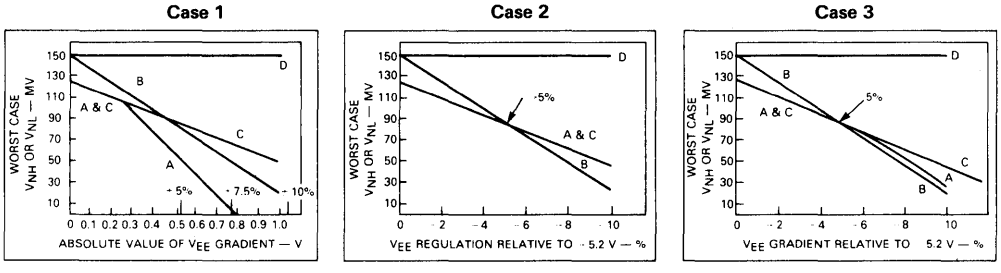
extreme and the other device is at the minus extreme of the supply tolerance.

In Case 2, a system operates on a single supply or several supplies slaved to a master supply. The entire system can drift, but all devices are at the same supply voltage.

In Case 3, a system has excessive supply drops throughout. Supply gradients are due to resistanc drops in V_{EE} bus.

The analysis indicates that the noise margins for a MECL 10K/10KH system equal or exceed the margins for an all 10K system for supply tolerance up to ±5%. The results of the analysis are shown in Fig. 1-5.

FIGURE 1.5 — NOISE MARGIN versus POWER-SUPPLY VARIATION



A. MECL 10K DRIVING MECL 10K B. MECL 10K DRIVING MECL 10KH C. MECL 10KH DRIVING MECL 10K D. MECL 10KH DRIVING MECL10KH

MECL Circuit Types

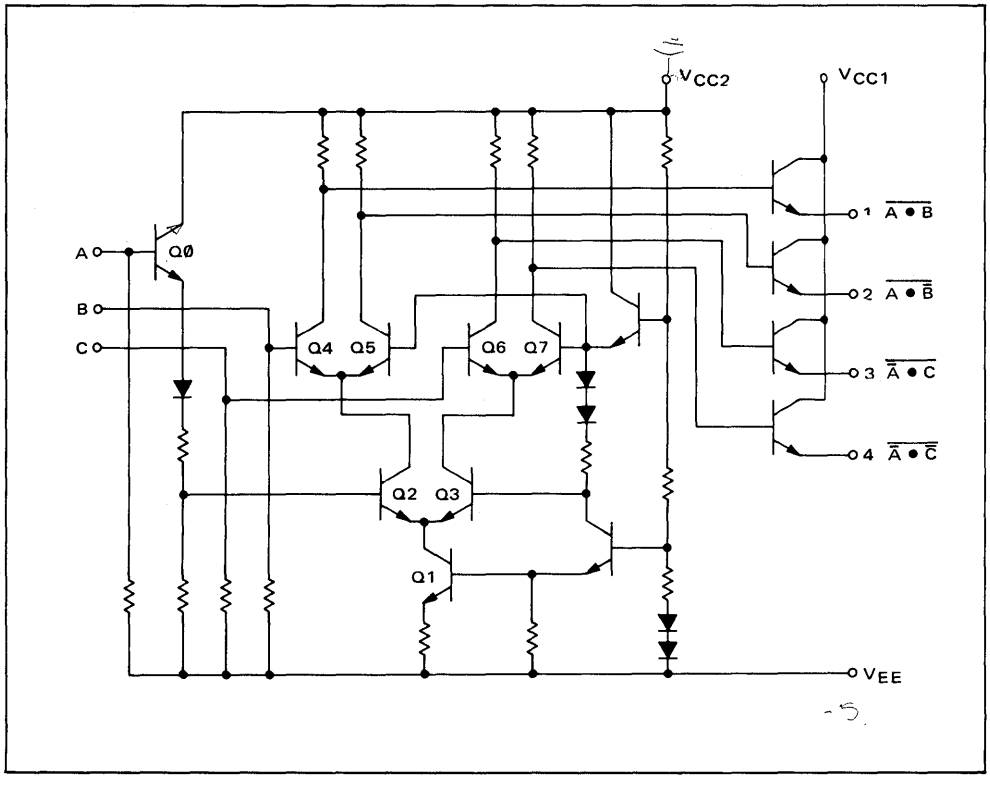
It is possible to connect the basic MECL differential amplifiers together within a circuit to increase logic flexibility, speed, and power efficiency. Two techniques, series gating and collector dotting, add the NAND and AND logic functions to the basic OR and NOR operation of the MECL gate with very little increase in propagation delay. A third technique, Wired-OR, gives the logic OR function by tying together two or more emitter-follower transistors. This is used internally in complex functions to save speed and power and, unlike collector dotting, may also be used externally by connecting logic outputs together.

Series gating is accomplished by connecting MECL differential amplifiers in a current-switch "tree", building up from a current source, Q1, as shown in Figure 1-6. The A input controls the switch, Q2/Q3 through the level shifter Q$\emptyset$ and the associated resistor diode network. The bias network is modified to provide the proper voltage level at Q3, a level which is lower than that on Q7 and Q5. The two upper switch pairs are controlled by inputs B and C. The overall circuit generates the four logic functions: $\overline{A \cdot B}$, $\overline{A \cdot \bar{B}}$, $\overline{\bar{A} \cdot C}$, and $\overline{\bar{A} \cdot \bar{C}}$. MECL circuits use up to three levels of series gating, permitting up to eight logic functions with one current source.

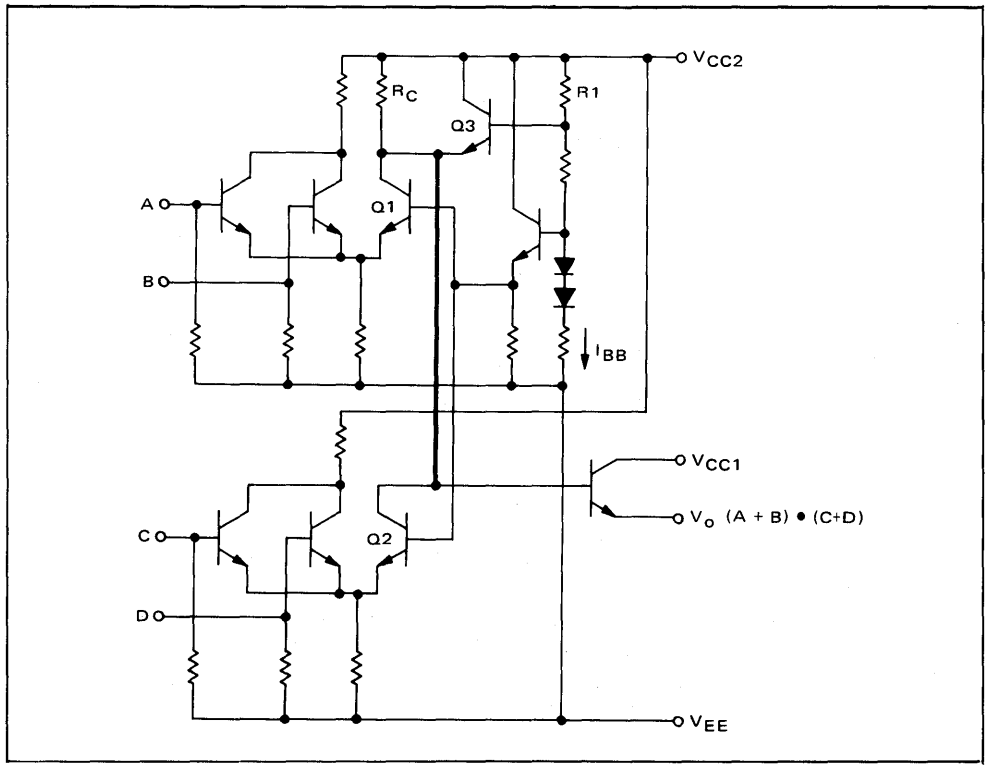
The propagation delay from an input, to a top current switch is approximately one gate delay. The propagation delay from an input to a lower level current switch is slightly longer because of the input level shifter Q$\emptyset$. Typically, the latter takes about 1.5 gate delays. More specific information is found on the data sheet for a particular part.

Series gating is an advantage in MECL logic since it provides the AND or NAND logic functions. Together with the OR/NOR function of the basic gate, MECL has the four basic logic functions needed for efficient logic design. Series gating is used internally in most MECL complex functions and flip flops.

1-6: Series Gating



1-7: Collector Dotting



Collector dotting is a second logic technique which is used in the MECL 10K/10KH series. With it, the logic AND function can be generated by interconnecting one collector node of separate differential current switches as shown in Figure 1-7. When connected this way the two 2-input OR gates give the logic function:

$$V_O = (A + B) \cdot (C + D)$$

Only one collector resistor (R_C) is used for the two transistors Q1 and Q2. The interconnection requires that at least one input to each gate be at a logic 1 level for the output to be at the logic 1 level. Since it is possible to have both Q1 and Q2 conducting at the same time (all inputs low), a clamp is used to limit the current in R_C and maintain the output ϕ logic level voltage. This clamp consists of R1 and Q3. They insure that the Q1/Q2 collector node never goes more negative than ($I_{BB}R_1 + V_{BEQ3}$). Propagation delays for all inputs to collector dotted circuits are equal and are typically about 20% greater than the basic gate delay.

To allow for temperature variations, the collector-dotted logic functions are designed to have the same V_{OL} as normal logic gates at $T_A = T$ max when only *one* gate has all of its inputs at a logic 0 level. Therefore, when *all* gates have all their inputs at a logic 0 level, V_{OL} will be slightly more negative than a normal gate. This does not limit device operation, but does give an increase in noise immunity for the logic 0 level.

The collector dot (OR-AND) logic function, series gating, and the Wired-OR characteristics of MECL combine to provide the means for designing very efficient and fast complex logic functions.

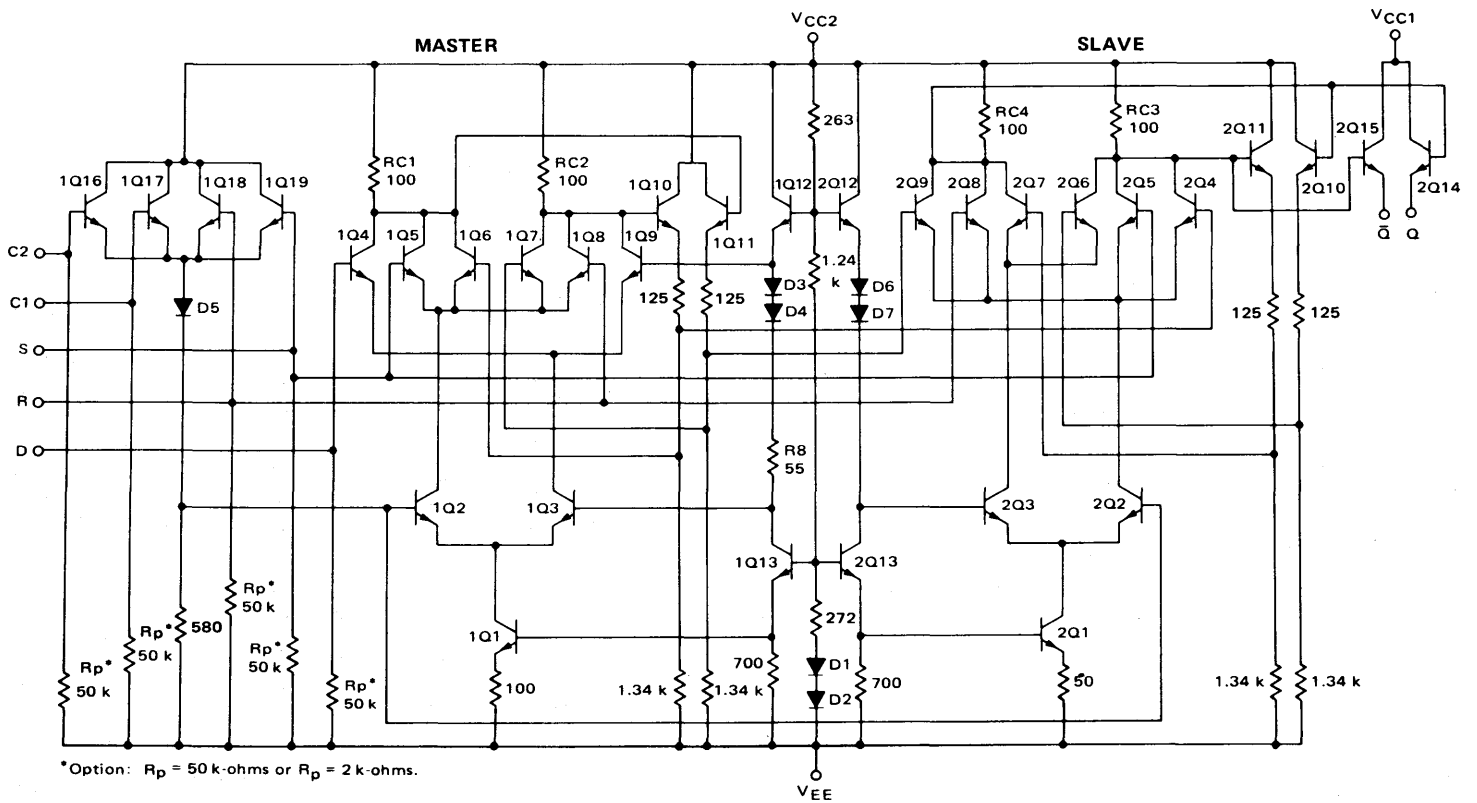
MECL Flip-Flops

In addition to the basic gate, the flip-flops in a logic line provide a necessary building block. All MECL 10K/10KH and MECL III flip-flops, use the direct coupled master-slave circuit as shown in Figure 1-8 for the MC1670. In each direct coupled circuit the master is updated while the clock is low, and data is transferred to the slave on the positive excursion of the clock. This type of circuit offers better noise protection than ac coupled circuits and is not susceptible to overshoot on the inputs. Also, the master-slave flip-flops do not have the rise time limitations of ac coupled circuits.

Operation Of Flip-Flop

In the circuit of Figure 1-8 assume that initially Q, C_1, C_2, R, S, and D are at ϕ levels and that $\overline{Q}$ is at the 1 level. Since the clocks and the R and S inputs are low, transistors 1Q3 and 2Q3 are conducting. In the slave section only transistors 2Q6 and 2Q7 are in series with 2Q3. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through 1Q3 and 1Q9.

Now assume that the D input goes high. The high-input signal on the base of 1Q4 causes it to conduct, and 1Q9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base of 1Q11 and therefore on the emitter of 1Q11. Since there is essentially no current flow through RC2, the base of transistor



1-8: MECL III Master-Slave Type D Flip-Flop (MC1670)

1Q10 is in a high state. This is reflected in the emitter of 1Q10, and in turn is transferred to the base of 1Q6. 1Q6 is biased for conduction but, since there is no current path, it does not conduct.

Now assume one of the clocks goes high. As the clock signal rises, transistor 1Q2 turns on and transistor 1Q3 turns off. This provides a current path for the common-emitter transistors 1Q5, 1Q6, 1Q7, and 1Q8. Since the bases of all these devices except 1Q6 are in the low state, current flow is through 1Q6. This maintains the base and emitter of 1Q11 low, and the base and emitter of 1Q10 high. The high state on 1Q10 is transferred to 2Q4 of the slave section.

As the clock continues to rise 2Q2 begins to turn on and 2Q3 to turn off. (Reference voltages in the master and slave units are slightly offset to insure prior clocking of the master section). With transistor 2Q2 conducting and the base of 2Q4 in a high state, the current path now includes 2Q2, 2Q4, and resistor RC3. The voltage drop across the resistor places a low-state voltage on the base of 2Q11, and therefore on the emitter, of 2Q11. The lack of current flow through RC4 causes a high-state input to the base of 2Q10. Finally these states are fed back to the latch transistors, 2Q6 and 2Q7 and appear on the Q and $\overline{Q}$ outputs.

As the clock voltage falls, transistor 2Q2 turns off and 2Q3 turns on. This provides a current path through the latch transistors, "locking in" the slave output.

In the master section, the falling clock voltage turns on transistor 1Q3 and turns off 1Q2. This enables the input transistor 1Q4 so that the master section will again track the D input.

A separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs 1Q2/1Q3 and 2Q2/2Q3. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors 2Q4 and 2Q9. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly likely if the D input changes at this time. The offsetting resistor, R8, also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

Both set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, 1Q2 begins to conduct because its base is now being driven through 1Q19 which is in turn connected to S. Transistor 1Q5 is now on, and the feedback devices 1Q6 and 1Q7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors 2Q2, 2Q5, 2Q6, and 2Q7.

MECL Family Comparison

A list of MECL circuit characteristics is tabulated in Figure 1-9. The various families are compared with respect to both features and performance. Because of the speed difference between the 10,100 series and 10,200 series, these products are given separate columns. The following paragraphs describe the MECL characteristics in the order of Figure 1-9. Differences between standard and military products are pointed out when significant.

1. . . Introduction year relates to the first year product was introduced. Several years are normally required to fill a product line and work continues to update MECL with new LSI, memories, and logic.

2. . . All MECL circuits incorporate internal V_{BB} bias drivers. The bias circuits are designed to operate over a wide range of temperatures, supply voltages, and circuit power

dissipation. All MECL parts have the same logic level and threshold voltages regardless of power dissipation. The M10800 and MECL 10KH families feature a voltage compensation network that holds logic levels constant with supply voltage.

3. . . MECL 10K/10KH and MECL III circuits feature open emitter outputs for easy interface to terminated transmission lines. The MC1648 VCO is an exception and can be used without an external resistor.

1-9: MECL Family Comparison

FEATURE	MECL 10KH	MECL 10,000 (10K)			MECL III
		10,100 10,500	10,200 10,600	10,800	
1. Year Introduced	1981	1971	1973	1976	1968
2. Bias Driver	V.C.*	10,000	10,000	V.C.*	10,000
3. Output Pulldown Resistors	No	No	No	No	No
4. Input Pulldown Resistors	Yes	Yes	Yes	Yes	Yes
5. Maximum Input D.C. Loading Current	265μA	265μA	410μA	350μA	350μA
6. Specified Ouput Current	≈22mA	≈22mA	≈22mA	≈22mA	≈22ma
7. Maximum Output Current	50mA	50mA	50mA	50mA	40mA
8. Transmission Line Drive	Yes	Yes	Yes	Yes	Yes
9. DC Loading Fanout	83	83	54	63	68
10. Input Capacitance	2.9 pf	2.9 pf	3.3 pf	-	3.3 pf
11. Output Impedance	7 ohm	7 ohm	7 ohm	7 ohm	5 ohm
12. Gate Progration Delay (typical)	1.0 ns	2 ns	1.5 ns	1-2.5 ns	1 ns
13. Gate Edge Speed (10 to 90%)	1.8 ns	3.5 ns	2.5 ns	3.5 ns	1 ns
14. Flip-Flop Toggle Speed (min)	250 MHz	125 MHz	200 MHz	N.A.	500 MHz
15. Gate Power	25 mW	25 mW	25 mW	2.3 mW	60 mW
16. Open Wire Length (Less than 100 mV undershoot)	3"	6"	3"	6"	1"
17. Wire-wrap Capability	Yes	Yes	Yes	Yes	No
18. Use of series damping Resistors	Yes	Yes	Yes	Yes	Yes
19. Separate V_{CC} Inputs	Yes	Yes	Yes	Yes	Yes
20. Speed-Power Product	25 pJ	50 pJ	37 pJ	4.6 pJ	60 pJ
21. Wire-or Capability	Yes	Yes	Yes	Yes	Yes
22. Full Military Temp. Range	TBD**	Yes	Yes	No	No
23. Flat Package	Special	Yes	Yes	No	Yes
24. Dual-In-Line Package	Yes	Yes	Yes	Quil	Yes

* Voltage compensated
** To be determined

4. . . All MECL single-ended inputs have internal (typical 50 kΩ) input pull down resistors. This simplifies wiring since unused inputs can be left floating and assume a solid logic Ø V_{OL} state. Differential devices such as line receivers and the MECL to TTL translator do not have input pull down resistors and should be connected as described on the individual data sheets.

5. . . Maximum input DC loading current is specified on individual circuit data sheets. The numbers here apply to a single input of a basic gate. If a package input goes to more than one point in a circuit, such as a gate strobe line would, additional current may be required.

Calculating the input current, I_{in}, for MECL 10K/10KH with a worst-case input resistor value of 30 kΩ (R_{in}) gives an input resistor current of:

$$I_{in} = \frac{V_R}{R_{in}} = 143\ \mu A$$

$$V_R = |V_{EE} - V_1| = 4.3\ V,$$

where: V_R = voltage drop across the input resistor, R_{in}, with a logic 1 input,

V_{EE} = -5.2 V supply voltage,

V_1 = -0.9 V (a typical logic 1 level).

The typical 50 kΩ value will use slightly less current, but either resistance value is very high compared to the output circuit impedance or the line impedance.

6-8. . . Output voltage levels are specified at currents representative of circuit operation. MECL 10K/10KH and MECL III are designed to drive 50 Ω transmission lines terminated to –2 Vdc (measured from V_{CC}). The current, I_{TT}, required by the line termination is:

$$I_{TT} = \frac{V_{TT} - V_1}{Z_o} = \frac{(-2.0 + 0.9)\ V}{50\ \Omega} = -22\ mA.$$

Consequently, the outputs are specified with 50 ohm loads. The 50 ohm load is a worst-case specification and does not require that system design be restricted to 50 Ω transmission lines. MECL 10K/10KH works well over a range of 50 to 120 ohm environments. Full military MECL 10,500 and and 10,600 series are limited to 100 ohm (11mA) loads.

The maximum permissible output currents of 50 mA for MECL 10K/10KH and 40 mA for MECL III insure a good safety margin over the specified currents.

9. . . The dc loading fanouts for MECL 10K/10KH and MECL III are computed by dividing the output current by the input current. However, both ac limitations and current needed in the transmission line termination can be expected to restrict the system fanout to a smaller number than the one computed.

10. . . Two techniques are used to measure circuit input capacitance. One method uses an impedance meter, such as the H.P. 4815A RF Vector Impedance Meter, to measure impedance and phase angle. The other technique uses a time domain reflectometer (TDR) to measure the effect of capacitance on the impedance

of a transmission line. (The mathematical relationships used to calculate input capacitance from TDR data are presented later in Chapter 7). Although small, the input capacitance will affect system rise time and transmission line propagation delay as a function of fanout at high MECL speeds.

11. . . DC output impedance can be calculated from measurements of the output voltage as a function of output current: $Z = \Delta V/\Delta I$. The gate output impedance must be much lower than the line characteristic impedance in order to provide full MECL signal levels when driving transmission lines. The output impedance (resistive load) is the parallel value of the output transistor and pull down resistor. It should be noted that capacitance charging rate during a negative transition is limited by current flow through the pull down circuit.

12-13. . . Gate propagation delay, edge speed, toggle rate, and power dissipation are standard data sheet information. Propagation delay (t_{pd}) is measured from the 50% amplitude point on the input signal to the 50% amplitude point on the output signal. Normally the edge speed given is measured between the 10 and the 90% amplitude points on the output signal. However, because of the amount of rounding on the upper 10% of the MECL 10K/10KH edges, these families are specified with 20 to 80% edge speeds for easier correlation. Nevertheless, 3.5 ns is a typical 10 to 90% figure for MECL 10K and 1.8 ns is a typical 10 to 90% figure for MECL 10KH.

14. . . Toggle speeds are minimum rates for the flip-flops in a family. For MECL III the 500 MHz shown is for the MC1690 D flip-flop. The family has divide by 4 prescalers which operate at 1 GHz.

15. . . Gate power for the MECL 10K/10KH and MECL III gates is specified with open emitter outputs, as is usual with most ECL product lines. The wide variety of output loads — both resistors used with transmission lines and pull down resistors — makes a power specification under load difficult to define. In a system, the output power is added to the gate power to find total power.

16-17. . . Open wire length and wire wrap usage are a function of edge speed and the propagation velocity of the wire. The distances shown are maxima, selected to give less than 100 mV undershoot at the receiving end of the line with a fanout of one. Additional information on line driving is found in Chapter 3. Wire wrap may be used with all families but MECL III. The 1 ns edges associated with MECL III cause too much reflection from the wire wrap connection to permit practical use. The open wire maximum line lengths still apply when using wire wraps, unless some form of resistor damping or line termination is used.

18. . . Damping resistors consist of small resistors (5 to 75 ohms) that are placed in series with a line at the output of the driving circuit to extend the permissible line length. The resistor provides a closer match between the line and the output impedance of the circuit than a direct connection. This match limits overshoot and ringing, and allows the use of line lengths somewhat greater than twice the non-damped lengths.

19. . . Separate V_{CC} inputs (V_{CC1}, V_{CC2}) are characteric of MECL 10K/10KH and MECL III. The separate V_{CC} pins are used to minimize any crosstalk between circuits in a package which might occur with the high switching currents when driving transmission lines. Separate V_{CC} lines do not affect using the parts and only require that two package

pins be connected to a single ground plane or ground bus. A few MECL 10K/10KH parts such as the MC10186 and the MC10H186A have only 1 V_{CC} pin because the function requires 14 I/O pins. These circuits keep V_{CC1} and V_{CC2} separate on the chip and use two bonding wires to the common V_{CC} package pin.

20. . . Speed-power product is a measure of a logic family's efficiency. Propagation delay (nanoseconds) is multipled by the gate power dissipation (milliwatts) to get a measure of efficiency in terms of energy (picojoules). It is interesting to note that gate efficiency has improved with each succeeding logic line introduced. The speed-power product is slightly inaccurate because power figures are used which do not include output loading (discussed previously). However, TTL speed-power products can be inaccurate also as they are generally computed for the circuits operating at a low rate. Such figures would be much worse for circuits operating near top switching rates. Gate power and speed-power for the M10800 family are calculated by dividing the number of equivalent gates in a logic function by the circuit power dissipation. The numbers are averages for the LSI circuits rather than any specific gate. Internal gates use less power than output gates with 50 line drive.

21 . . . Wired-OR is a technique used with all MECL circuits to obtain the logic OR function by connecting circuit outputs together. When several (more than 5) circuits are connected with Wired-OR outputs, it is possible to get a noise spike on the output if all gates are at a 1 output, and all gates but one are simultaneously changed to a logic $\emptyset$. The noise spike is due to the one gate suddenly having to source the output current previously supplied by the other circuits. The pulse width is normally less than the gate propagation delay and of insufficient amplitude to propagate in the system.

22-25. . . The remaining family features are self-explanatory. Packaging and temperature range for MECL 10K/10KH are based on initially introduced circuits. Other configurations are being investigated to meet future requirments.

CHAPTER 2 Using MECL

The design guidelines presented here are intended to assist the MECL user to apply MECL families in a system. The rules listed have been tried out in complete systems with good results. As rise times become less than 3 ns, special design rules must be followed. For rise times of 1.5 ns or shorter, designing with transmission lines is necessary.

MECL 10K/10KH and MECL III logic families are treated separately because of the differences in their capabilities and design techniques to be used. Reasons for the rules, methods for applying them, and test data are found in the following chapters under associated subjects. MECL 10K/10KH may be used with or without transmission lines and termination techniques. Rules for both design approaches are covered separately. Terminated transmission lines are recommended for large printed circuit boards and larger systems having several circuit boards.

1. MECL 10K/10KH without terminated lines

MECL 10K/10KH family of integrated circuits is designed to provide high circuit speed without putting a premium on special system layout techniques. This feature simplifies design with the emitter coupled logic family because most of the techniques used with high-speed TTL apply to MECL 10K/10KH .The ability of MECL 10K/10KH to interface with MECL III enables very high-speed systems to gain power economy, eased design rules, a large choice of logic functions, and lower system cost.

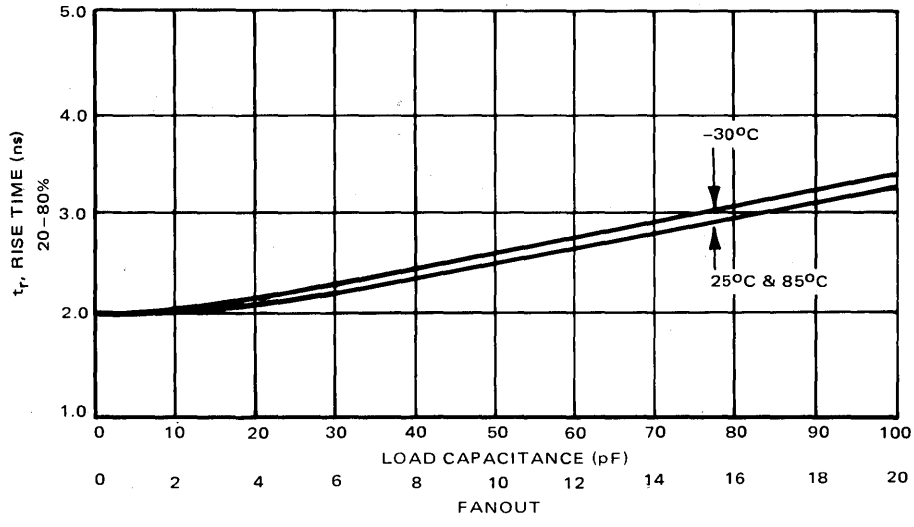
MECL 10K rise, fall and propagation delay times are typically each 2 ns. However, since rise and fall times are measured at 20-80% and are typically 3.5 ns 10-90%, transmission line techniques are not mandatory. The 10-90% rise and fall times of MECL 10KH are typically 1.8 ns, and are 1 ns 20-80%. Standard double-sized circuit boards and backplane wiring with ground planes are commonly used with MECL 10K/10KH.

Because of the wide variety of MECL 10K/10KH system sizes and interfaces, not all techniques will apply to every system. The designer should use these rules as guides, modifying them sensibly as required for a particular system.

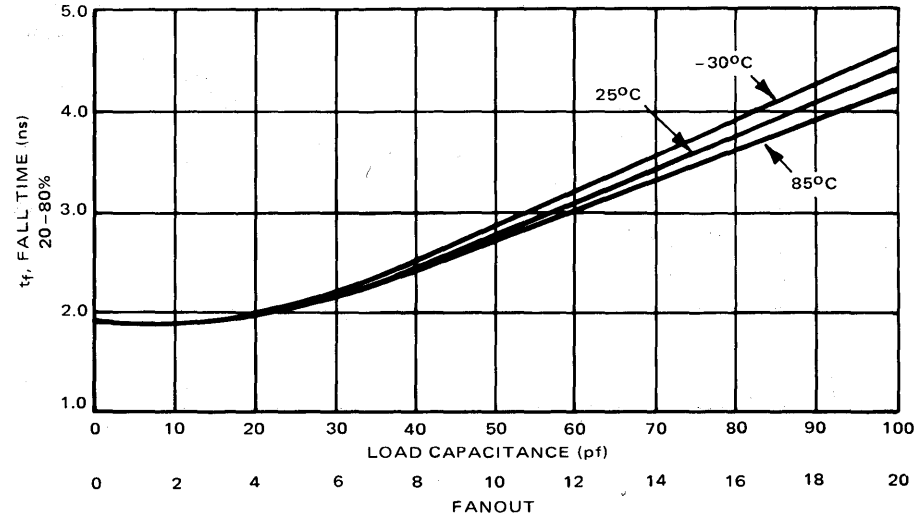
A. *Logic Design Considerations*

1. MECL rise, fall and propagation delay times are a function of fanout and capacitive loading. Figures 2-1 through 2-8 show the reduction in speeds with load placed near the output pin. Consequently when MECL 10K/10KH is operating near its upper speed limit, fanout should be restricted as indicated by the curves. Because of the emitter follower outputs, fall time and propagation delay to a ϕ level is more affected by capacitive loading than rise time and propagation delay to a 1 level (note that the curves in Figure 2-4 are steeper than those in Figure 2-3).

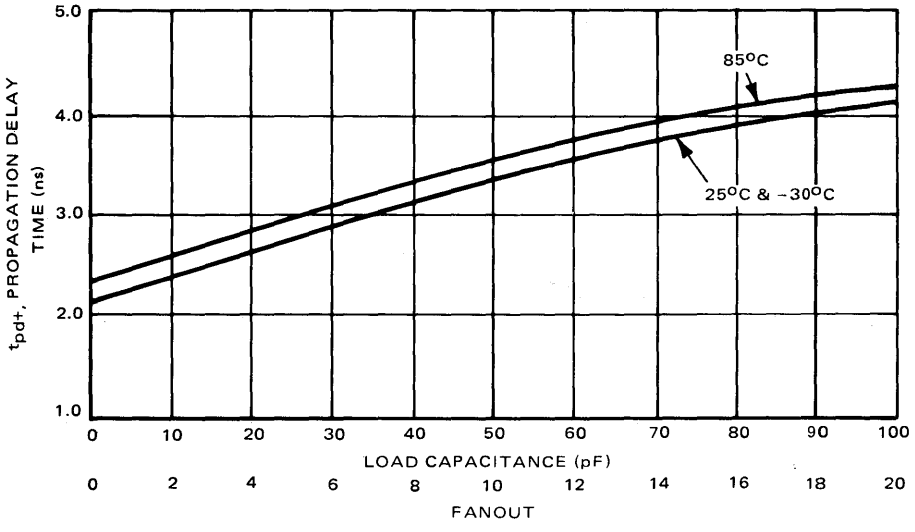
2-1: Rise Time versus Loading and Temperature (MECL 10K)
(50 ohm load)



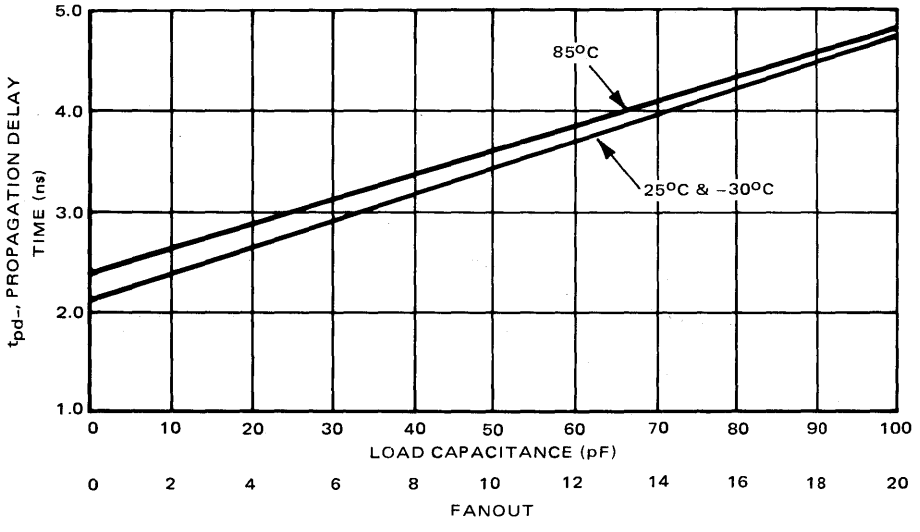
2-2: Rise Time versus Loading and Temperature (MECL 10K)
(50 ohm load)



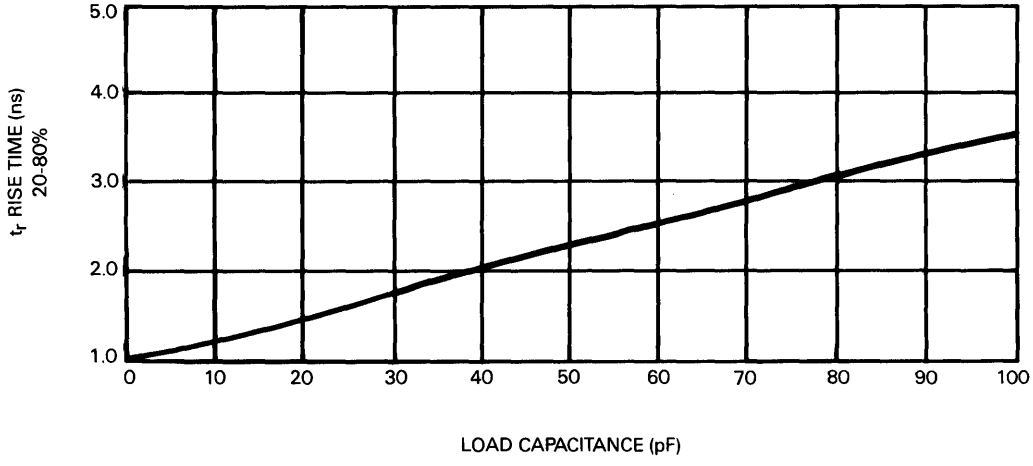
2-3: Propagation Delay, t_{pd+}, versus Loading (MECL 10K) and Temperature (50 ohm load)



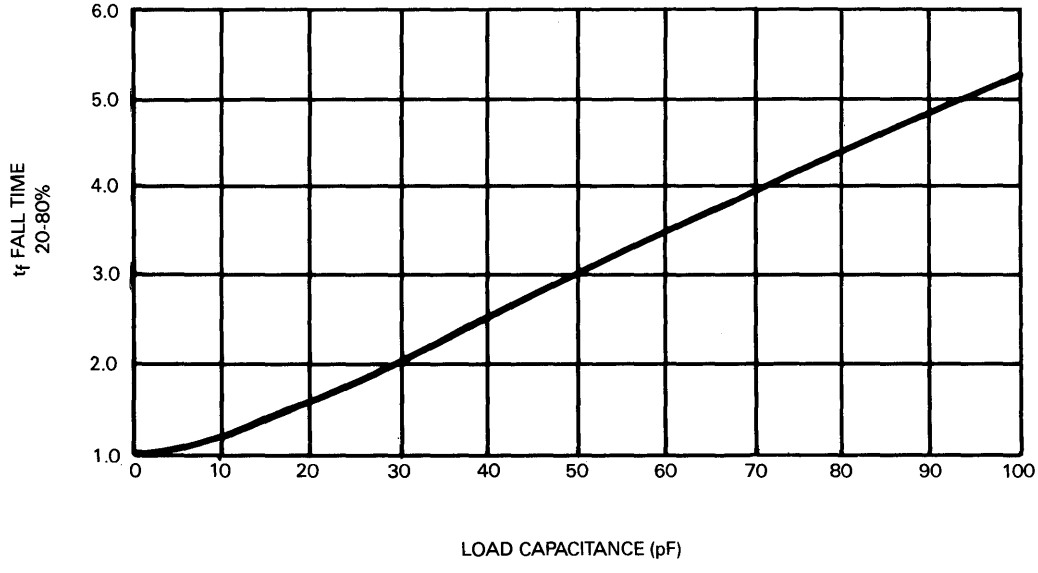
2-4: Propagation Delay, t_{pd-}, versus Loading (MECL 10K) and Temperature (50 ohm load)



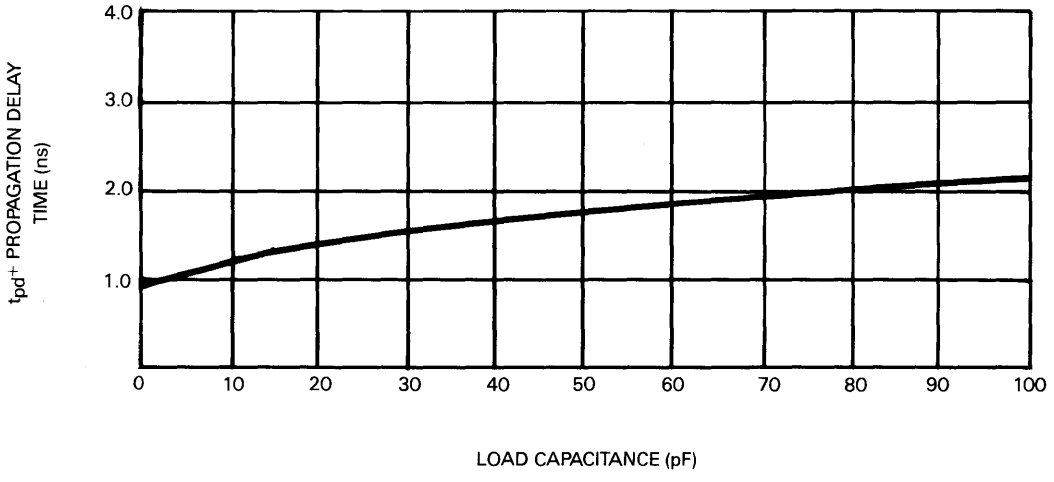
2-5: Rise Time versus Loading (MECL 10KH)
(50 ohm load)



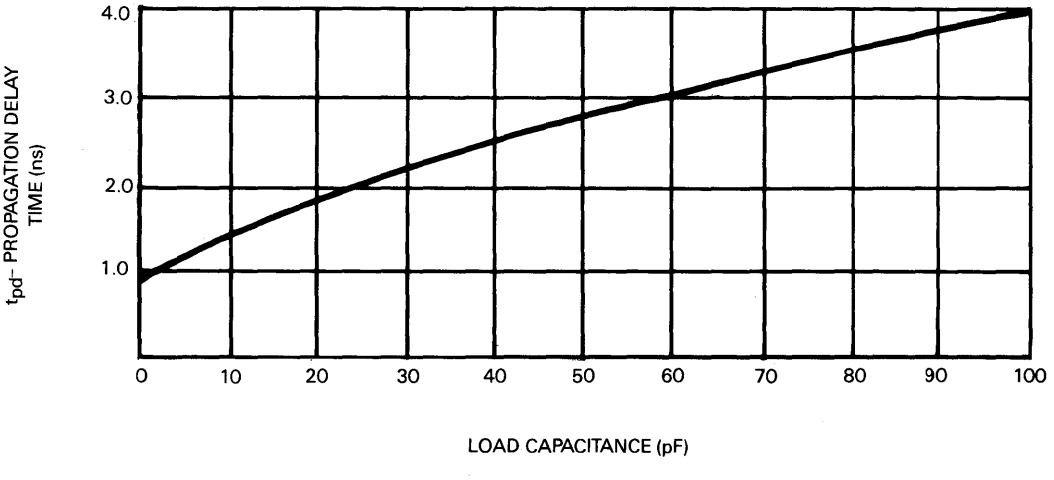
2-6: Fall Time versus Loading Capacitance (MECL 10KH)
(50 ohm load)



2-7: Propagation Delay, t_{pd+}, versus Loading (MECL 10KH) (50 ohm load)



2-8: Propagation Delay, t_{pd-}, versus Loading (MECL 10KH) (50 ohm load)



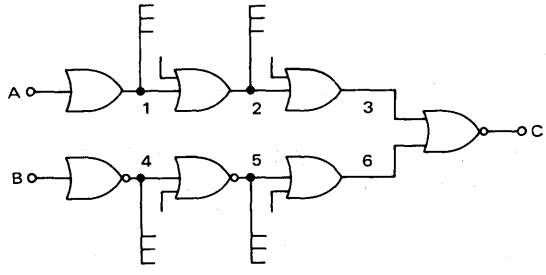
2. Fall-time and t_{pd-} may be improved by using a smaller load resistor between the output and −5.2 Vdc. A 240 Ω resistor will cut the delay caused by capacitive loading nearly in half. Load resistors less than 180 Ω should not be used because the heavy load may cause a reduction in noise immunity when the output is in the 1 state, due to increased output emitter-follower V_{BE} drop. Normally 510 Ω load resistors provide a good speed-power system design.

3. When driving flip-flops at high speed, clock driver circuits such as the MC10210, MC10211, MC10H210, MC10H211 or MECL III gates should be used. MECL III gates such as the MC1660 or MC1662 can provide the bandwidth necessary for clocking several flip-flops at once — as in a shift register or synchronous counter operating at high speed.

4. When driving a long string of flip-flops at speeds lower than 80 MHz (clock), two gates may be operated in parallel for additional drive. The MC10110 or MC10111 is useful in this application since its multiple OR or NOR outputs may be wired together.

5. The high operating speed of MECL and the effect of loading on propagation delay must be considered when parallel circuits converge at one point, as shown in Figure 2-9. Unequal delays along paths A and B can result in momentary outputs at point C, each lasting a time equal to the propagation delay difference between A and B. This can be compensated for by additional timing in the form of a strobe, or by adjusting the fanouts along A and B. If possible, unused gate inputs can be paralleled to simulate a larger fanout where required; otherwise a small capacitor can be substituted for the needed fanout (about 5 pF per gate input is recommended).

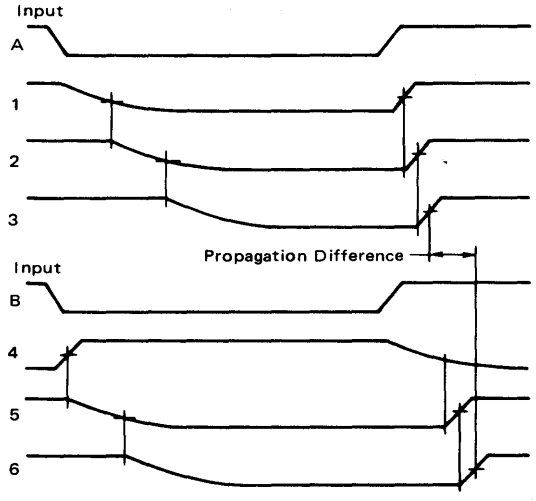
2-9: Parallel Signal Paths



Under heavy loading, propagation delay along path A will be less than along path B because of the use of OR outputs in A as opposed to the NOR outputs in B. This difference (Figure 2-10) is due to the effect of loading on the fall time, rather than being due to a timing difference between OR and NOR outputs. As a matter of fact, under light loading, propagation delays for both NOR and OR outputs are identical.

When designing clocks for high-speed flip-flops, these timing differences become increasingly important. For example, the MC10231 flip-flops can toggle on a 2.5 ns pulsewidth clock, consequently timing chain skewing in the order of 2.5 ns can cause false operation.

2-10: Propagation Differences



B. *System Layout Considerations*

1. System grounding and propagation delays in interconnecting leads are factors to be considered before laying out a system. Depending on the type of wire used, the wiring propagation time of a signal can greatly affect overall system speed. In normal backplane wiring it is realistic to expect a 2 ns per foot delay. Propagation delay is less in coaxial cable, but more for signal conductors in a multilayer circuit board.

2. System sections such as shift registers and synchronous counters should be on one card. Propagation delay between shift register clocks on separate boards can cause erroneous operation. Where timing is critical, equal length clock lines (to shift registers or other circuits on separate cards) should be run from a common clock to the card connectors. Such lines will also help limit overshoot and ringing (discussed further in section D. "Backplane Wiring").

3. The Wire-OR capability of MECL can be a powerful tool for reducing power, propagation delay, and package count. However, since the Wire-OR connection switches current when in operation (8 mA for a 510 ohm pulldown resistor), long interconnect lines can cause voltage transients due to signal line propagation delay. It is recommended that Wire-OR outputs be kept within a package or between nearby packages. Wire OR between circuit boards should be avoided except for bus lines where only one output goes high at a time. Large number Wire-OR ties can cause a loss of low-level noise margin because all outputs supply current to the pull-down resistor. A good rule is to limit the Wire-OR number to an average of 1 mA per output (6 outputs for 510 ohm pulldown, 8 for 390 ohms, 10 for 330 ohms, etc.).

4. Sections of a system where high fanout may be necessary (such as adders with lookahead carry) should be kept on one card. Signal path length should be reduced as fanout is increased to minimize both line delay and reflections.

C. *Circuit Board Layout Techniques*

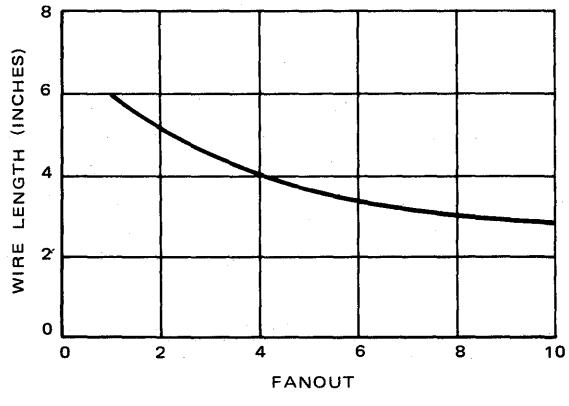
1. The size of a MECL system circuit board is not restricted by the logic family. System requirements should determine card size. Terminated transmission line techniques should be considered for circuit boards larger than 6 by 8 inches.

2. Standard double-sided circuit boards with a good ground distribution may be used with MECL 10K/10KH. A low impedance ground is necessary since any noise on the ground line may be coupled into signal lines. Also, any voltage drop across ground will subtract from the noise immunity of the MECL circuits. Grounding techniques are discussed at length in Chapter 5 "Power Distribution".

3. As with TTL, bypass capacitors between ground and −5.2V should be used with MECL. A 1.0 μF capacitor should be located on the board at the power supply inputs. Bypass capacitors, 0.01 to 0.1 μF, should be connected once every four or five packages. When breadboarding or using MECL 10K/10KH without a good ground plane, a 0.1 μF bypass capacitor should be used for every two packages. RF quality capacitors (low inductance) are recommended because of high-circuit speeds. Unlike TTL, MECL does not have large current spikes during switching. A 510 ohm pulldown resistor requires 8 mA for a logic 1 and 6 mA for a logic Ø or a delta of 2 mA switched current. The function of the bypass capacitors is to supply the small switching current of the pulldown resistor, circuit input capacitance, and circuit board stray capacitance, thus preventing spikes on the power leads.

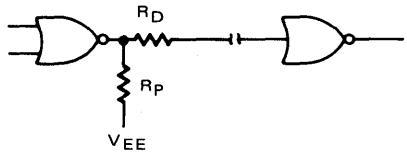
4. As with any high-speed system, signal lines should be kept as short as possible to minimize ringing and overshoot, as well as to simplify timing considerations arising from the propagation delay of a signal along a conductor. Ringing and overshoot are due to the intrinsic inductance and capacitance of the line itself, as well as lumped capacitance at the end of the line. Intrinsic inductance and capacitance are reduced by shortening the lines. A graph of recommended maximum line length as a function of fanout for MECL 10K is shown in Figure 2-11. Since increased fanout adds capacitance at the end of the line, the line should be shortened as shown by the following curve. Detailed unterminated signal line length information is found in Chapter 3, "Printed Circuit Board Connections".

2-11: Recommended Maximum Line Length versus Fanout (MECL 10K)



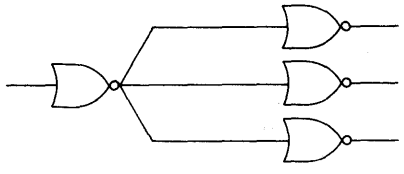
5. Longer line lengths are possible if a series damping resistor is used. The resistor is placed at the output of a gate, in series with the signal line as shown in Figure 2-12. The resistor value depends on the fanout and the required line length. Resistors under 150 ohms for a fanout of one, or under 30 ohms for fanouts greater than five, are normally used for damping. Values larger than these produce rise and fall time degradation and loss of noise immunity due to IR voltage drop in the resistor.

2-12: Damping Resistor



6. When driving large fanouts, line lengths can be increased by running parallel leads as shown in Figure 2-13. The distance between the parallel leads is not critical.

2-13: Parallel Signal Paths



This technique should be used for shift register clocks, counter resets, and other high fanout applications. Of course, for synchronous clock lines, clock skew delays should be matched. Series damping may also be used with parallel signal paths.

7. With MECL circuits, undershoot ringing on the logic 1 level is critical since it subtracts from noise immunity. For safe operating margins undershoot should be held to 100 mV or less.

D. *Backplane Wiring*

1. A ground screen is a good means for running a ground in the backplane wiring. A ground screen is made by connecting heavy bus wires to the connectors in a grid pattern before wiring the signal lines. The ground screen lines are wired both parallel to the connectors (tying to the connector pins), and perpendicular to the connectors (contacting multiple ground pins of each connector). This forms a grid network (cf Figure 5-6) of approximately 1 inch squares over which signal lines are then located.

2. Ferrite beads may be used in backplane wiring for longer signal runs. The recommended line lengths discussed for circuit cards also apply to backplane wiring.

A ferrite bead on a wire limits rise and fall time to about 7 ns by attenuating the high-frequency components of the signal. With a bead, lines up to three feet long can be driven without excessive overshoot.

3. Standard backplane wiring techniques may be used with smaller MECL 10K/10KH systems. Both wire-wrapped and soldered connections perform well. Point-to-point wiring is recommended instead of a laced harness, to lessen line length and reduce crosstalk.

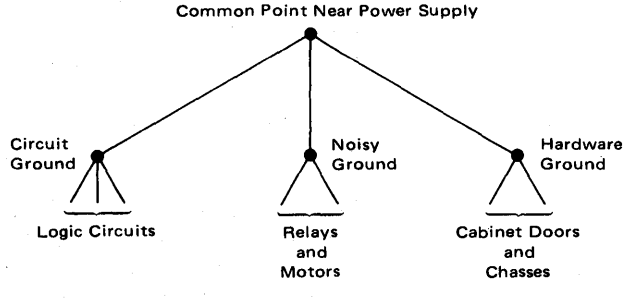
4. For longer signal paths (e.g. between panels or between cabinets) twisted pair lines are recommended. The twisted pair is connected to the OR and NOR outputs at the sending end and to an MC10115, MC10116, MC10H115 or MC10H116 line receiver at the receiving end. With this technique, long lines (hundreds of feet) have been driven with no system degradation other than propagation delay down the line.

E. *System Considerations*

1. A good system ground is required for best performance. All grounds should be connected to a common ground point – normally near the power supply. All logic circuits are connected to a circuit ground. All relays, solenoids, motors and other noise generating devices are wired to a separate ground network connected to the common ground point. Standard noise suppression techniques should be employed (i.e. diodes across relays, and capacitors across dc motor brushes).

All mechanical parts such as panels, chassis, and cabinet doors should be grounded with a third ground. A mounting frame is often used for this if good conduction can be made at points of contact. If some pieces of equipment in the system are left ungrounded they may carry transient voltages that will interfere with the rest of the system. The three separate ground systems connected to a common

2-14: Grounding System



point will eliminate noise on the signal ground (cf Figure 2-14). Heavy ground leads should be used on large systems to minimize any voltage drop along the ground line run.

2. Twisted pair lines and line receivers are normally used between sections of a system unless line lengths can be kept short. Twisted pair lines should always be used between sections operating at widely differing temperatures (>30°C), or between sections not connected with a solid ground network.

2. MECL 10K/10KH Design Rules

The MECL 10K/10KH family is a high-speed, economical logic family designed to fill the gap beneath the MECL III family and to meet the requirements for future high-performance systems. The family is designed to drive terminated transmission lines with impedances as low as 50 ohms and as low as 25 ohms in bus applications with the MC10123 and the new MC10H330, MC10H332 and the MC10H334. Also, increased circuit complexity is possible due to high component densities and very low-speed-power products. Finally, the relatively slow edge speeds of MECL 10K/10KH minimize wiring constraints on a logic system.

This section contains layout and design guidelines for power distribution, ground planes, terminations, line lengths, fanout loading, clock distribution, thermal considerations, and packaging, applicable to MECL 10K/10KH.

A. *General Considerations*

1. Standard double-sided plated-through-hole printed circuit boards may be used with the MECL 10K/10KH family. However multilayer boards will permit a higher component density for a given board area. As a result interconnect lengths are reduced, making the highest speed systems possible.

2. Backplane wire wrapping is also acceptable using commercially available boards. Rules and techniques will be discussed for interconnection lengths and terminations as a function of loading.

3. Coaxial cable, ribbon cable, or twisted pair line is normally required to interface between drawers and card racks in a large system. Microstrip lines are normally required for clock distribution with either series or parallel termination. Series damping resistors can be used to facilitate driving long, unterminated lines.

B. *Printed Circuit Card Layout Techniques*

1. For double-sided boards, a ground plane is recommended on one side of the card. This plane provides a stable ground reference for microstrip transmission lines on the other side of the board. Such transmission lines will have a characteristic impedance of less than 150 ohms. If a ground plane is not possible, a ground bus must be used as part of the layout on the board, to provide a low inductance V_{CC} line.

2. If possible, run the interconnections on one side of the board in the direction perpendicular to the interconnections on the other side of the board. (This works nicely for large boards holding 100 or more packages).

3. The ground plane or bus should be connected to 10% of the edge connector pins spaced equally apart. This reduces the ground impedance, in turn minimizing crosstalk – since multiple signals do not have to rely on a single ground return path.

4. The V_{CC1} and V_{CC2} package pins should be connected directly to the ground plane or bus, as close to the package as possible. Having the two V_{CC} pins and connecting the collectors of emitter follower outputs to only one V_{CC} pin is designed to minimize internal crosstalk.

5. The ground for high current devices – relays, lamps, core drivers, etc. – should be separate from the logic ground. These high current circuits should be connected to a separate ground bus on the card and in the backplane. The separated grounds should be connected at the system ground point.

6. Signal interconnection wires between circuits should be kept as short as possible.

C. *Power Supply Bypassing on Circuit Cards*

1. A 1.0 μF bypass capacitor is used on each board at the power supply inputs. Decouple every 4 to 5 packages with 0.01 μF to 0.1 μF RF quality capacitors (-5.2 Vdc to ground).

2. The power supply ground line noise should be limited to less than 50 mV peak-to-peak.

3. Maintain V_{EE} power supply voltage with less than 100 mV difference among all the logic cards to which signals must interconnect. (This will limit noise margin degradation to less than 30 mV).

4. Power supply regulation should be better than ± 10% for MECL 10K and MECL III and ± 5% for MECL 10KH.

D. *Backplane and Loading Considerations*

1. Wire wrapping techniques are acceptable in the backplane as long as the interconnection rules are followed.

2. A ground screen or ground plane is recommended in the backplane. This gives backplane wiring a characteristic impedance of approximately 140 ohms. (This may vary as much as ±50% depending on distance from the plane and the route taken). The capacitance of the wire over the ground screen is about 1 pF/in and the inductance is about 20 nH/in. Parallel terminating resistors, as described in Chapters 3 and 7, may be used to increase line lengths in the backplane.

3. 10% of the card edge connector pins should be connected to the ground plane or screen to reduce card-to-backplane ground impedance. The lowered ground impedance resulting from many pins paralleled to ground minimizes crosstalk since several signals do not have to rely on a single ground return path.

4. The optimum choice for backplane wiring (for maximum line impedance continuity) is the strip line motherboard technique. In such a case, board interconnections on the motherboard would follow the same rules as the strip line circuit card. Strip line techniques will be discussed in later sections (Chapter 3 and Chapter 7).

5. Series damping resistors can be used to series terminate the interconnect wires as follows:

a. Ten inches of open wire (with a 600 Ω output emitter pulldown resistor connecting to -5.2 volts) can be driven if a 50 ohm resistor is placed in series at the sending end. Up to eight loads may be driven using this configuration. Eighteen inches of line with up to 4 loads may be driven by using a 100 ohm series resistor. These resistor values will insure that any undershoot will be less than 100 mV.

b. Ten inches of open wire may be driven in series with 10 inches of printed circuit line (in either order) if a 100 ohm resistor is placed in series at the sending end. This arrangement can drive up to 4 loads.

6. Three inches of open wiring with a fanout of up to 4 gate loads will produce less than 100 mV undershoot. A ferrite bead placed in the line will increase the open wiring length to 15 inches.

7. A damping resistor or a combination of series/parallel terminations with microstrip lines is required when driving flip-flops whenever fanouts exceed 4 and whenever line lengths are greater than 3 inches.

8. Coaxial cable and twisted pair line are recommended when top speeds and rock-bottom noise pickup is a "must" for signal paths in a backplane. An alternate

approach, ample for nearly all requirements, is to use strip lines or microstrip lines in a backplane motherboard as in #4 above.

9. Recommended coaxial cables have characteristic impedances of 50-100 Ω, and time delays of 1.5 ns/ft.

10. Twisted-pair lines may be made of standard hookup wire (AWG 24-28), twisted about 30 turns per foot. Such twisted pair exhibits a characteristic impedance of about 110 ohms.

11. When driving coaxial cables, the printed circuit leads from the driver and receiver (going to the coax) should be kept as short as possible to reduce mismatch reflections, unless microstrip or strip line is used.

12. When driving 110 ohm twisted pair, the pair line should be terminated with a 110 ohm resistor across the differential input to a line receiver (MC10115, MC10116, MC10H115 or MC10H116). A 390 ohm pulldown resistor should be connected to each output of the gate driving the twisted pair.

13. Twenty feet of twisted line can be driven by a MECL 10K/10KH OR/NOR gate at a frequency of 100 MHz, when received by a line receiver.

14. Twisted pair line is recommended for interconnections whenever a temperature differential of more than 35 °C exists between sections in a system.

15. Twisted pair lines are recommended when high switching-current lines are in close proximity to the proposed signal route or when signals run between drawers or racks. If common mode noise is greater than 1.5 volts, then shielded twisted pair is recommended.

16. Inductance and overshoot are reduced if parallel lines are used to fanout to various loads on different circuit boards in the backplane (this also holds for interconnections on the circuit card). In this way, a parallel fanout of 4 will produce very little more overshoot than a fanout of one.

17. Twisted pair lines should be used to distribute clock signals to different logic boards and drawers in a system.

E. *System Distribution and Grounding*

1. High switching current lines for core drivers, relays, and motors should be separated physically from logic lines. (cf Chapter 4, discussion of crosstalk).

2. Avoid bundled parallel runs as much as possible. Signals in bundled cables produce crosstalk.

3. Signal distribution architecture should minimize wiring delays to permit the highest possible system clock speed. System clock speeds of greater than 40 MHz can be obtained in medium size computers.

4. The ground for the high switching current circuitry, should be separated from the logic ground. All separate grounds should, however, be tied together at one point – the system ground point. In that way, the ground buses will be at the same potential but current cannot be looped since they are connected at only one point.

5. The cabinet should be strapped to the system ground point to make it serve as an electrostatic shield.

6. If the system is in a high noise environment, connect the system ground point to earth ground with a heavy conductor.

7. All the equipment in a system should be grounded.

F. *Loading Rules for MECL 10K/10KH*

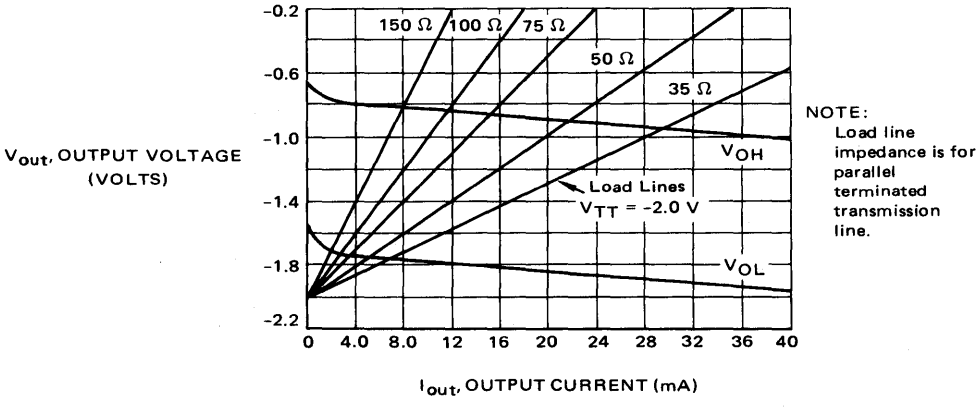
1. MECL 10K/10KH and MECL III are designed to directly interface with each other over the full range of ambient air temperatures and power supply tolerances.

2. MECL 10K/10KH and MECL III fanout rules are the same. Minimum output pulldown resistor loading is 50 ohms to -2 volts; 10 gate loads (in addition to the 50 Ω) will reduce noise margin by less than 20 mV. Maximum output pulldown resistor loading is 100 ohms to -2 volts. Larger resistors result in a loss of logic ∅ noise margin. See Figure 2-15 for typical output characteristics of MECL 10K/10KH as a function of output load current and the value of the output pulldown resistor.

3. It is recommended that output pulldown resistor values of from 270 Ω to 510Ω (connected to -5.2 V) be used when MECL 10K/10KH drives MECL 10K/10KH or MECL III. Under these conditions 25 MECL 10K/10KH gate loads or 20 MECL III gate loads may be driven.

4. MECL 10K/10KH fall time is primarily a function of the load capacitance and

2-15: Output Voltage Levels versus DC Loading



the emitter pulldown resistor. If the emitter pulldown is connected to -5.2 V, the fall time is given by:

$$t_f \approx (0.2\ RC + 2)\ ns,\ (10K)$$
$$t_f \approx (0.2\ RC + 1)\ ns,\ (10KH)$$

where R is the value of the emitter pulldown resistor (in kΩ) and C is the load capacitance (in pF). If the emitter pulldown is connected to -2 V, the fall time is given by:

$$t_f \approx (1.1\ RC + 2)\ ns,\ (10K)$$
$$t_f \approx (1.1\ RC + 1)\ ns,\ (10KH)$$

5. The propagation delay for the output to go negative is also a function of the load capacitance and the emitter pulldown resistor. If the emitter pulldown resistor is connected to -5.2 V, the propagation delay for the output to go negative is:

$$t_{pd-} \approx (0.1\ RC + 2)\ ns, (10K)$$
$$t_{pd-} \approx (0.1\ RC + 1)\ ns, (10KH).$$

If the emitter pulldown is connected to -2 V, the formula for the delay is:

$$t_{pd-} \approx (0.47\ RC + 2)\ ns. (10K)$$
$$t_{pd-} \approx (0.47\ RC + 1)\ ns, (10KH)$$

6. For computing the signal path delay with either a 50 Ω emitter pulldown to -2 volts, or 270 Ω to -5.2 V, propagation delay will increase by 0.1 ns per gate load (assuming 5 pF per gate load).

7. For all MECL 10K/10KH series devices, the various propagation delays listed in the data sheets have been measured with a 50 ohm emitter pulldown resistor connected to -2 volts. Thus, these propagation delays are longer than would occur for a lighter load condition. Consequently the propagation delays specified on the data sheet are used to determine *maximum* delay paths in a system. (Of course as discussed above, loading will increase the propagation delay and should be allowed for in delay calculations).

8. Emitter dotting is accomplished by tying two or more outputs together. This produces a logic OR function in positive logic. A logic AND function results if negative logic is assigned. For either the 50 Ω or the 270 Ω pulldown, the propagation delay will increase by 50 picoseconds per emitter dot. For loading purposes, each emitter dot may be considered as equivalent to 1/2 a gate load (more precisely, each emitter dot is equivalent to slightly less than 2 pF of capacitive loading).

9. The MECL 10K/10KH circuit propagation delay is unaffected by the intrinsic line capacitance of an unterminated line. However, overshoot at the receiving end could result in a slightly faster rise time.

10. The MECL 10K/10KH circuit propagation delay is unaffected by a transmission line properly terminated at the receiving end. Such lines appear as purely resistive loads.

11. High fanout at the end of a terminated transmission line longer than 1.7 ns does not increase the propagation delay of a MECL 10K circuit driving the line. Fanout loading increases the propagation delay of a signal on the line.

12. The delay in signal propagation along a printed circuit line must be taken into consideration. The basic delay of a signal on either a loaded (resistive loading) or unloaded printed circuit surface line over a ground plane is about 1.8 ns per foot or 0.15 ns/in for glass epoxy boards. The exact delay can be calculated using the formula: $t_{pd} = \sqrt{L_o C_o}$, where L_o and C_o are the intrinsic line inductance and capacitance.

13. The signal propagation delay down the line will increase by a factor of $\sqrt{1 + C_d/C_o}$. where C_o is the intrinsic line capacitance and C_d is the capacitance due to loading and stubs off the line:

$$t'_{pd} = t_{pd}\sqrt{1 + C_d/C_o}.$$

14. The increase in signal delay due to load capacitances should be calculated for the particular transmission line characteristics. Lines with low characteristic impedance are less affected because of their higher intrinsic capacitance per unit length.

15. The characteristic impedance of a transmission line is reduced due to load capacitances by the factor $\sqrt{1 + C_d/C_o}$. So, the formula for the modified characteristic impedance, Z'_o, of a transmission line is:

$$Z'_o = \frac{Z_o}{\sqrt{1 + C_d/C_o}},$$

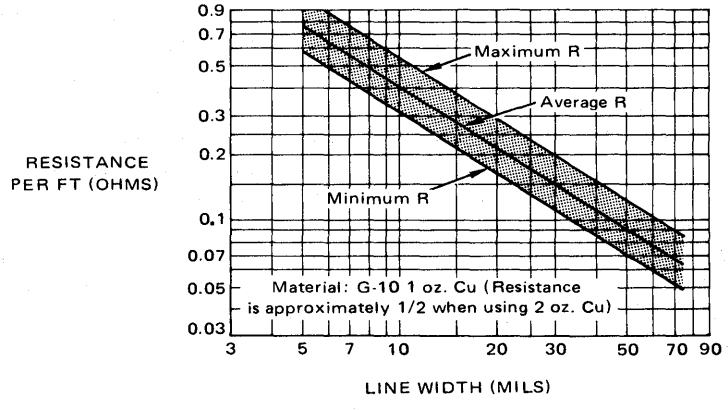
where Z_o is the original line impedance.

16. The maximum line length allowable on the circuit board can be calculated using the data in Figure 2-16 for printed circuit line resistance.

For lines terminated to -2 Vdc at the receiving end of the line, the signal voltage drop in the line is:

$$\Delta V_{Sig} = \left(\frac{2 - |V_{OH}|}{R_T}\right) \cdot (\text{line resistance}),$$

2-16: Resistance versus Line Width for Printed Circuit Lines



where V_{OH} is the logic 1 output voltage and R_T is the terminating resistor. Normally this signal voltage drop is small and need not be calculated. For example, 7 feet of 15-mil wide line will have less than 30 mV drop. The maximum length allowable will be that for which Δ V remains below about 100 mV.

17. The maximum stub length off terminated lines is 3 inches with a fanout of four gate loads on the stub, (for <100 mV undershoot). Whenever an open line (stub) is driven by a pulse, the resultant undershoot and ring are held to about 15% of the logic swing if the two way delay of the line is less than the rise time of the pulse. For these conditions the maximum unterminated line length may be calculated:

$$\ell_{max}\ (\text{in.}) = \frac{t_r}{2t'_{pd}},$$

where t_r is the rise time of the pulse. Here t'_{pd} is the propagation delay of 1 inch of line (cf #13 above).

18. Up to 3 parallel open lines can be driven by one gate, following the rules given above. Parallel fanout to loads is recommended when possible, since lead lengths longer than for a single line may then be used. However, a matched transmission line should be used for driving loads over lines longer than shown in Figure 3-13. Note that both stubs and terminated lines can be driven by one and the same gate.

19. If a ground plane is used, longer lines can be driven than if no ground plane is used; or else the value of a series damping resistor can be reduced. The best approach for determining the permissible values of resistance, length of line, and fanout is from the basic equations that are developed in Chapters 3 and 7.

3. MECL III Design Rules

The MECL III logic family is the widest bandwidth standard logic available. This family is designed to fill the high speed requirements of the communication, or instrumentation system designer. MECL III, like MECL 10K/10KH , is designed to drive terminated transmission lines.

Motorola has successfully met the device/package requirements for a 1 ns logic family. The ability to manufacture very fine geometry devices with reliable multilayer metallization results in very compact circuitry and makes LSI possible for MECL; and so, expansion with complex functions operating at higher data rates, lower power, and smaller size than any other form of logic, has become possible with MECL. This is a direct result of new processing technologies and the techniques available to the MECL circuit designer. These techniques include: series gating, collector dotting, and reducing internal logic swing.

The ability to process data with microelectronic structures at bit rates of over 200 million per second requires a thorough understanding of device circuit design, system interconnects, packaging, and thermal management. Specifically, the necessary compromises and possible trade-offs must be understood. A set of layout ground rules or guidelines will provide a first step toward this goal.

A. *Circuit Card Layout*

1. Leave maximum possible spacing among all parallel signal leads to reduce crosstalk. If two signal leads are run parallel at spacings of less than 150 mils, then a ground lead placed between the parallel wires will reduce crosstalk. Such a ground shield will reduce crosstalk from 12 to 7 mV for two 15-mil lines spaced 115 mils with a 35-mil ground shield centered between. If the ground shield is plated through to the ground plane every 1/2", the crosstalk will be reduced even further – to 3 mV.

2. The choice between two-layer and multilayer printed circuit board depends upon the maximum operating frequency and the circuit complexity. With clock rates above 250 MHz, the use of multilayer board is highly recommended. This is due to the possibility of ground loops caused by the use of ground plane areas as signal paths on double layer boards. One to three packages, as in a test fixture, may be used satisfactorily above 250 MHz with two-sided printed circuit board.

B. *Transmission Line (Microstrip Line)*

1. Avoid sharp bends in transmission lines, to prevent reflections from abrupt changes in the characteristic impedance of the line.

2. If two sided board is used, Figure 3-7 may be used to determine Z_O.

3. For MECL systems the physical width of microstrip lines used leads to characteristic impedances usually lying between 50 and 120 ohms. To achieve impedance values greater than 120 ohms, line widths have to be very narrow. This promotes two problems. One is that as dc series resistance goes up, signal level at the receiving end of the line is reduced. The second problem is that "etch-outs" or pin holes exist after etching narrow lines. As a result of various considerations, it happens that 68 ohms is a wise choice of impedance.

An impedance of 68 Ω yields the best trade-off between delay time and power consumption. A 50 Ω line would consume more power. A higher impedance would consume less power, but delay time would increase. As a matter of fact, three impedance levels can serve most applications: 50, 68, and 100 Ω. A 68 ohm stripline is a good choice for on-board uses, while 50 and 100 Ω are used for single ended or party line drive (respectively) off the board.

4. Line characteristic impedance, Z_O, is inversely proportional to the square root of the line capacitance. Therefore, known values of gate input capacitance can be used to modify Z_O, i.e.:

$$Z_o' = \frac{Z_o}{\sqrt{1 + C_d/C_o}} \quad \text{(ohms)},$$

where Z_o' is the new effective characteristic impedance, C_d is the sum of the capacitance due to loads distributed along the line (circuit inputs and stray capacitance), and C_o is the intrinsic line capacitance.

The effect of load capacitances on signal propagation delay time, t_{pd}, is:

$$t_{pd}' = \overbrace{Z_o C_o}^{t_{pd}} \sqrt{1 + \frac{C_d}{C_o}}.$$

If C_d and C_o are in pF, and Z_o in k ohms, t_{pd}' will be in ns.

These relationships show that load capacitances increase propagation delay and will decrease the characteristic impedance. Lines with low characteristic impedance are least affected due to their higher capacitance per unit length.

The one important advantage of transmission lines with proper termination is that stubs have little effect on line delay times. With a Z_o of 50 Ω, stubs must be limited to 1" or less to prevent excessive ringing.

C. *On-Card Clock Distribution Via Transmission Lines*

1. Use of the OR output for gates used as clock buffers is recommended in developing a clock chain or tree. A small clock skew may result from using both the OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers in a tree.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line. The effect of this arrangement is to cut the load capacitance per line in half.
4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.
5. It is always good practice to use a buffer when driving long lines off the card. One instance when a buffer is particularly desireable is when Q or $\overline{Q}$ outputs from a high frequency counter are also used within the feedback logic of the counter.

6. Parallel drive gates are used when high clocking repetition rates are required, and when driving high capacitance loads. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz of bandwidth can be gained with the two (or three) clock driver gates in parallel.

7. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid lumped loads at the end of lines greater than 3 inches long. A lumped load, if used, should consist of no more than four gate loads.

8. For Wired-OR (emitter dotting), two-way lines are required when connection distance is greater than 1 inch. A two-way 100 Ω transmission line is produced by terminating both ends with 100 Ω impedances. Single end termination may be used when all emitter connections are within 1 inch of each other.

D. *Off-Card Clock Distribution*

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines. At the far end of the twisted pair, an MC1692 differential line receiver is used. The line should be terminated. This may be done with approximately 110 ohms across the differential receiver input.

Alternatively, a 56-ohm resistor from each of the receiver inputs to -2 Vdc will provide both line termination and pulldown resistance for the MC1660 driver. This latter method not only provides high speed board-to-board clock distribution, but also yields noise margin advantages for the system. That is, the noise margin from board-to-board becomes independent of temperature differentials, due to the line receiver operating with differential inputs.

2. MECL III interfaces directly with MECL 10K/10KH. Use the wiring rules for whichever family drives the line.

E. *Testing MECL III*

1. Keep all unshielded lead lengths as short as possible, less than 1/4".

For dual-in-line packages use AMP 16-pin low profile sockets (or equivalent) which have no long paths from the device under test to the solder pads on the bottom of the socket.

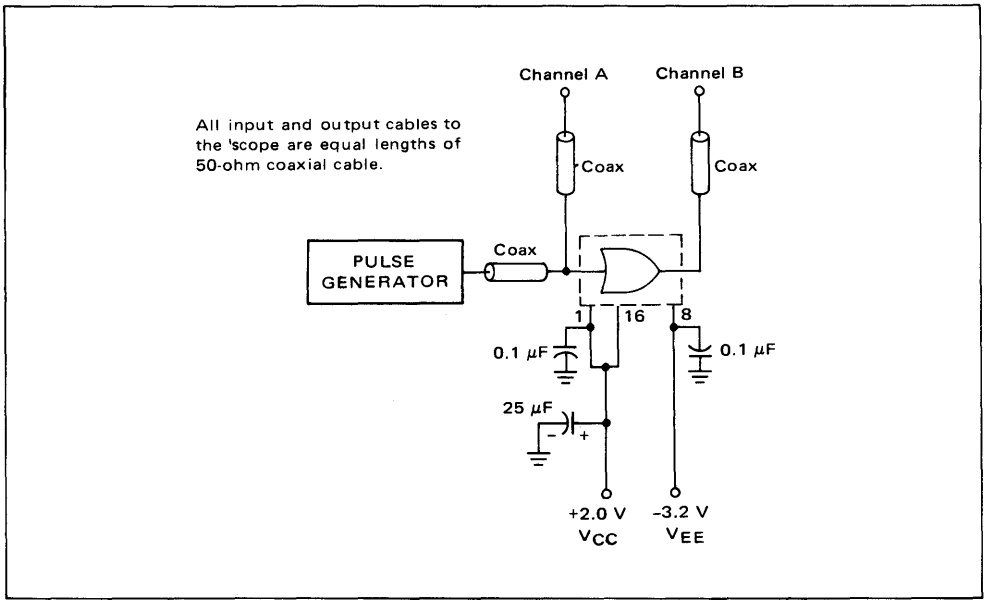
2. Use small RF quality parts: 1/8 W carbon composition resistors and 0.01 μF low inductance disc ceramic capacitors.

3. All input/output connections should be made with good quality miniature 50 Ω semi-ridge coax, and BNC, GR, or miniature coax fittings.

4. A solid ground plane should be used, with V_{CC} pins 1 and 14 or 16 connected directly to the +2.0 volt plane via the shortest possible path.

5. V_{CC} should be at +2.0 volts with V_{EE} at −3.2 volts. The gate under test should have its output connected to a 3S5/S2-50Ω sampling plug-in for a Tektronix 568 sampling system (or equivalent). The arrangement shown in Figure 2-17 is recommended by Motorola for measuring subnanosecond performance.

2-17: Recommended MECL Test Setup



CHAPTER 3 Printed Circuit Board Connections

Any signal path on a circuit board may be considered a form of transmission line. If the line propagation delay is short with respect to the rise time of the signal, any reflections are masked during the rise time and are not seen as overshoot or ringing. As a result, because of the high ratio of rise time to propagation delay time, signal lines for most MOS circuits may be several feet long without signal distortion. However, as edge speeds increase with faster forms of logic, the line lengths must be shorter in order to retain signal integrity.

Two techniques can be used to enable high speed circuits to operate over relatively long lines without serious waveshape deterioration. TTL uses an input clamp for fast negative edges. The energy of the overshoot is clamped at one diode drop below ground, and this reduces the amplitude of the following undershoot. The slower positive-going edges are allowed to overshoot, but are damped out by the relatively high output impedance (50 to 80 ohms) of the circuit in the logic 1 state. Also, greater noise immunity in the 1 state makes any undershoot less critical.

The disadvantages of the TTL technique show up at higher bit rates and faster edge speeds when fanouts along the line are used. Since the reflections are present in the lines, they will tend to combine at high bit rates to cause signal distortions and loss of noise immunity.

Consequently, MECL uses another approach for handling reflection problems: matching the impedance of the line. In this way, reflections are controlled and signal integrity is maintained.

This chapter discusses circuit interconnections as transmission lines, with the open line treated as an unterminated line. Although MECL III is the only family with a strict requirement for a transmission line environment, it is expected that most MECL 10K/10KH users will use matched impedance lines to improve interconnection distances and signal purity.

Circuit designers have a choice between transmission lines and conventional interconnect wiring when the distances between MECL devices are short, less than the lengths in Figure 1-9, #16 or when the rise times are greater than 3 ns. The design decision must be made after thorough analysis of the system requirements. Incorrect selection of conventional interconnect wiring could result in false system operation due to a high percentage of incident pulse reflections and subsequent lowering of the ac noise immunity.

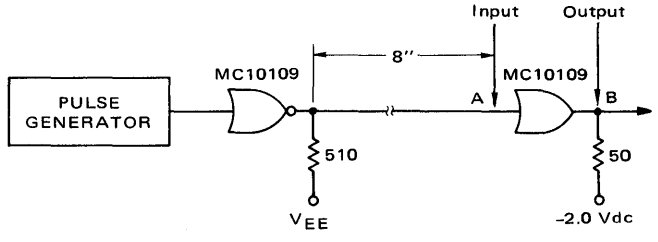
In many cases where MECL devices are used, transmission line techniques are advantageous. When using MECL devices with rise times less than 3 ns, transmission lines are highly recommended. The basic factors which will affect this decision are:

A. System rise time
B. Interconnect distance
C. Capacitive loading (fanout)
D. Resistive loading (line termination)
E. Percentage of undershoot and overshoot permissible (reduction in ac noise immunity).

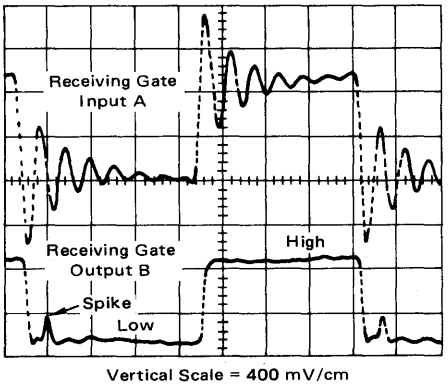
The result of analyses shows that transmission lines should be used if the percentages (E, above) exceed the acceptable design goal. A general rule of thumb that can be used is that undershoot should not exceed 10%, and overshoot should not exceed 35% of the logic swing. The 35% overshoot limit keeps the input out of saturation and the 10% undershoot is less than 100 mV loss of noise margin. Actually, most MECL circuits can tolerate up to 30% undershoot.

An example of a MECL 10K device driving an 8-inch open wire is shown in Figure 3-1. The oscilloscope traces, for the 8-inch open wire without a ground plane, taken at

3-1: Overshoot and Undershoot With an Open Wire Line



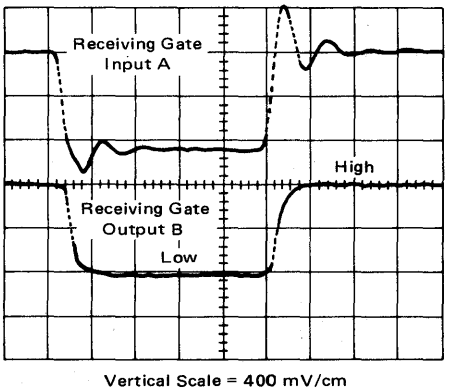
(a) Test Arrangement



Vertical Scale = 400 mV/cm
Horizontal Scale = 20 ns/cm

(b) Ground Plane Not Used

(c) Ground Plane Added



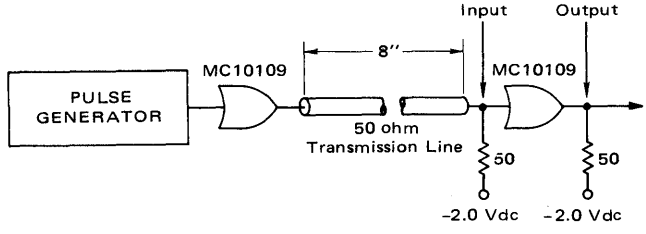
Vertical Scale = 400 mV/cm
Horizontal Scale = 10 ns/cm

points A and B are shown in Figure 3-1 (b). Trace A shows an overshoot condition of 60% and an undershoot of 40%. It can be seen how this undershoot condition affects trace B during the low level period of the signal — a small spike is produced.

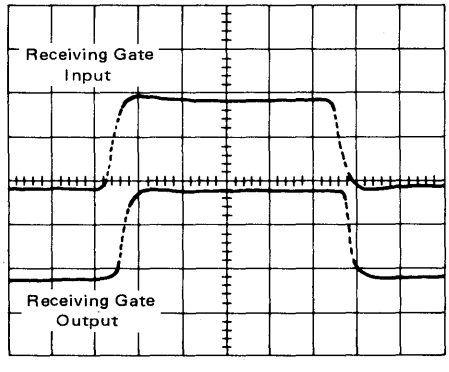
By way of contrast to the open wire circuit, a ground plane is added and the trace shown in Figure 3-1(c) is obtained. The addition of a plane reduces overshoot and undershoot to about 40% and 20% respectively.

Figure 3-2(a) shows an 8-inch transmission line correctly terminated. The scope traces in Figure 3-2(b) indicate the marked advantages of using transmission lines correctly terminated.

3-2: Matched Transmission Line Waveshapes



(a) Test Configuration



Vertical Scale = 400 mV/cm
Horizontal Scale = 10 ns/cm

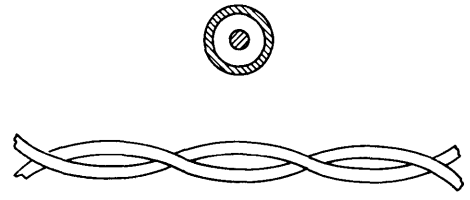
(b) Input and Output Waveforms

Transmission Line Geometries

Figures 3-3 through 3-6 show some of the types of transmission lines than can be used for interconnecting high speed logic systems. Details concerning each type are elaborated in the following paragraphs.

Coaxial Cable and Twisted Pair

Figure 3-3 shows a twisted pair line and the cross section of a coaxial cable transmission line. Some common types of coaxial cable have characteristic impedances of 50, 75, 93, or 125 ohms. Twisted pairs can be made from standard hook-up wire (AWG 24-28) twisted about 30 turns per foot. Such twisted pair has a characteristic impedance of about 110 ohms. Coaxial cable and twisted pair are recommended for long line lengths in the backplane.



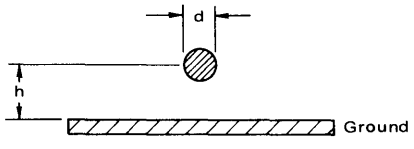
3-3: Coaxial Cable, Twisted Pair

Wire Over Ground

Figure 3-4 shows the cross section of a wire over a ground. The characteristic impedance of the wire is

$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4h}{d}\right),$$

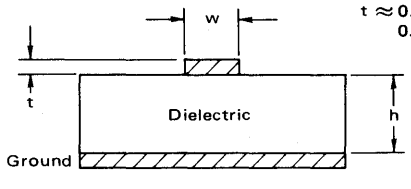
where e_r is the effective dielectric constant surrounding the wire. The wire over a ground plane is most useful for breadboard layout and for backplane wiring. The characteristic impedance of a wire over a ground plane in the backplane is about 120 ohms, although this may vary as much as ±40% depending on the distance from the plane, proximity of adjacent wires, and the configuration of the ground.



3-4: Wire Over Ground

Microstrip Lines

A microstrip line (Figure 3-5) is a strip conductor (signal line) separated from a ground plane by a dielectric. If the thickness, width of the line, and the distance



3-5: Microstrip

from the ground plane are controlled, the line will exhibit a predictable characteristic impedance that can be controlled to within ±5%.

The characteristic impedance, Z_o, of a microstrip line is:

$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right),$$

where:

e_r = relative dielectric constant of the board material (about 5 for G-10 fiber-glass epoxy boards),
w, h, t, = dimensions indicated in Figure 3-5.

The signal line is made by etching away the unwanted copper using photo resist techniques. The characteristic impedance of microstrip lines for various geometries is plotted in Figure 3-7. These values were calculated from the mathematical relation above and closely agree with experimental time domain reflectometer measurements. In fact, the equation proves to be very accurate for ratios of width to height between 0.1 and 3.0 and for dielectric constants between 1 and 15.

Figure 3-8 shows curves for the microstrip capacitance per foot as a function of line width and spacing.

The inductance per foot may be calculated using the formula:

$$L_o = Z_o^2 C_o,$$

where: Z_o = characteristic impedance,

C_o = capacitance/ft.

The propagation delay of the line may be calculated by:

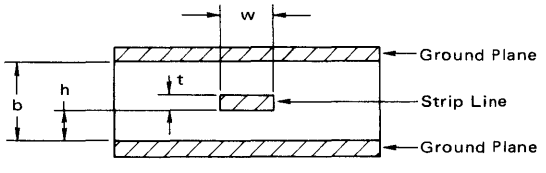
$$t_{pd} = 1.017 \sqrt{0.475\, e_r + 0.67} \quad \text{ns/ft}.$$

Note that the propagation delay of the line is dependent only on the dielectric constant and is not a function of line width or spacing. For G-10 fiber-glass epoxy boards ($e_r \cong 5.0$) the propagation delay of the microstrip line is calculated to be 1.77 ns/ft.

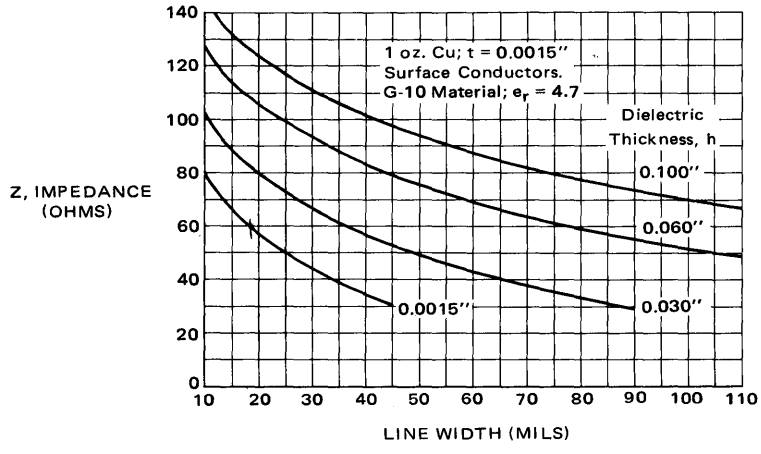
Strip Line

A strip line (Figure 3-6) consists of a copper ribbon centered in a dielectric medium between two conducting planes. If the thickness and width of the line, the

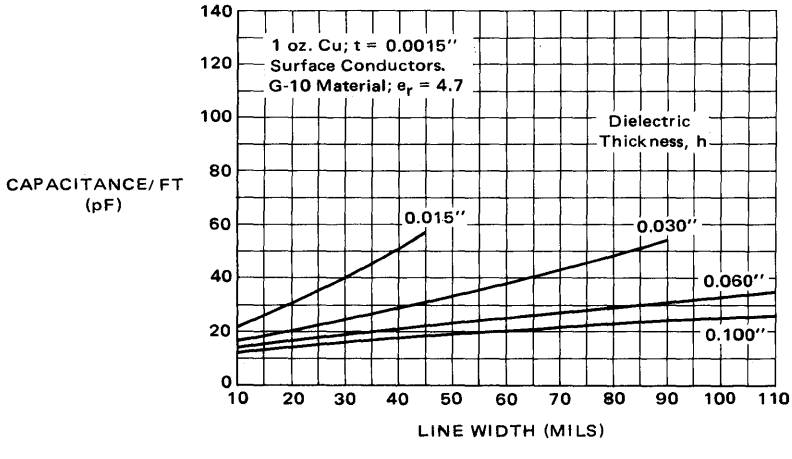
3-6: Stripline



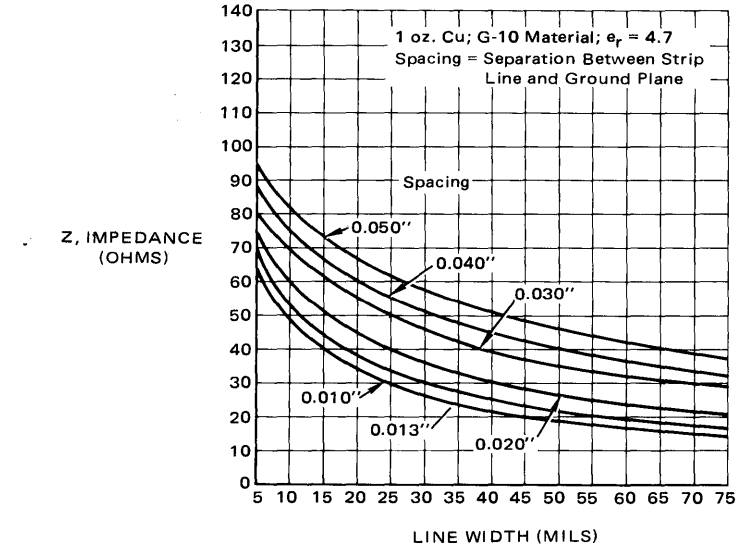
3-7: Impedance versus Line Width and Dielectric Thickness for Microstrip Lines



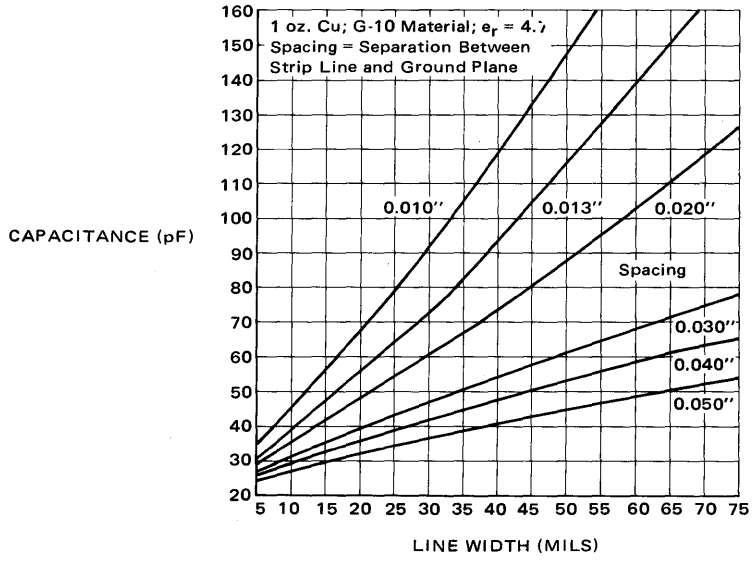
3-8: Capacitance versus Line Width and Dielectric Thickness for Microstrip Lines



3-9: Impedance versus Wire Width and Spacing for Strip Lines



3-10: Capacitance versus Line Width and Spacing for Strip Lines



dielectric constant of the medium, and the distance between the ground planes are all controlled, the line will exhibit a characteristic impedance that can be held constant within ±5%. The characteristic impedance of a strip line is theoretically:

$$Z_o = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4b}{0.67\,\pi w(0.8+\frac{t}{w})}\right).$$

This equation proves accurate enough for $w/(b-t)<0.35$ and $t/b<0.25$.

Figure 3-9 gives the actual characteristic impedance for various geometries of stripline. These values were measured with a time domain reflectometer. The measured results closely parallel those calculated from the above equation.

Figure 3-10 shows curves for the stripline capacitance per foot for various line widths and spacings. An LC meter was used to determine the capacitance.

The inductance per foot can be calculated using the relation $L_o = Z_o^2 C_o$, while the propagation delay of the line can be found from the relation:

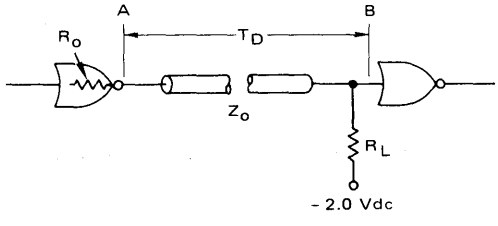
$$t_{pd} = 1.017\sqrt{e_r} \quad \text{ns/ft}.$$

For G-10 fiber-glass epoxy boards ($e_r \cong 5.0$), the propagation delay of the strip lines is 2.26 ns/ft. Again, the propagation delay is not a function of line width or spacing.

Basic Transmission Line Operation

The behavior of signals on a transmission line is important for understanding the methods used to terminate MECL lines. Figure 3-11 shows a line with typical

3-11: MECL Transmission Line



loads at both ends. For the purpose of discussion the line delay will be long with respect to the rise time so that reflections will appear at their full amplitude. The output voltage swing at point A is a function of the internal voltage swing, output impedance, and line impedance:

$$\Delta V_A = \Delta V_{INT}\left(\frac{Z_o}{R_o + Z_o}\right).$$

Since R_o is small compared to line impedance, the output swing is nearly the same as the input transition. The internal voltage swing is approximately 900 mV, giving a typical output swing greater than 800 mV.

This signal propagates down the line and is seen at point B time T_D later. The voltage reflection coefficient at the load end of the line, ρ_L, is a function of the line characteristic impedance and the load impedance:

$$\rho_L = \frac{R_L - Z_O}{R_L + Z_O}$$

Clearly, for the ideal case of $R_L = Z_O$, there is no reflection. More important, for any value of R_L close to Z_O the reflection is quite small. At time 2 T_D any reflection returns to point A and is again reflected, by the sending end reflection coefficient ρ_S:

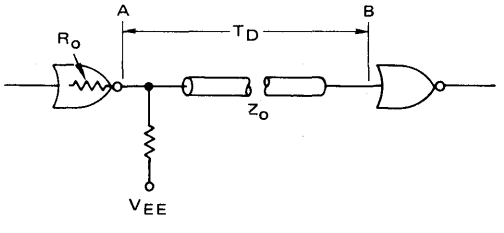
$$\rho_S = \frac{R_O - Z_O}{R_O + Z_O}$$

The reflection continues bouncing back and forth between the ends of the line, being successively reduced by the reflection coefficients and the resistance in the line.

Unterminated Lines

Figure 3-12 shows a specific transmission line variously known as an "open line," an "unterminated line" or a "stub." Behavior of this line is as follows. At time zero an initial, full MECL signal starts at point A. Time T_D later the signal reaches point B and is reflected by ρ_L discussed previously. Since the input impedance of the driven gate is very high with respect to Z_O, a large positive reflection occurs and signal overshoot results. At time 2 T_D the reflection is back at point A and is reflected by ρ_S. Because of the low value of R_O the reflection is in the negative direction (refer to equation for ρ_S), resulting in a signal at point B at time 3 T_D that is in the opposite direction to the initial signal. This signal at B at 3 T_D and its subsequent reflections produce the undershoot which subtracts from signal noise immunity. These reflections, successively smaller, cause the condition known as "ringing " as shown in Figure 3-1(b).

3-12: MECL Unterminated Transmission Line



If the lines are sufficiently short, the signal still will be rising at time T_D, and reflections are part of the rising edge. With longer lines, the rise of the signal will be completed before a time T_D, and reflections will appear as overshoot and

undershoot. For this reason, unterminated or undamped lines have maximum recommended lengths when used with MECL logic.

The undershoot caused by an unterminated line is held to about 15% of the logic swing if the two way delay of the line is less than the rise time of the pulse. The maximum open line length may be calculated by expressing this rule with the relation:

$$\ell_{max} \leqq \frac{t_r}{2t_{pd}} ,$$

where: t_r = rise time,

t_{pd} = propagation delay of the line per unit length.

(Use t'_{pd} when line is loaded, cf equation 11, Chapter 7).

It can be seen that the slower rise times of MECL 10K/10KH are compatible with open lines, but that line lengths are important for the faster MECL III. The other variable for line length, t_{pd}, is controlled by the type of line (velocity factor) and the loading on the line. Increased loading raises the propagation delay and accounts for the decreasing permissible line length with increasing fanout (cf Figure 2-7). The analysis of rate of propagation with line loading is covered in Chapter 7.

Suggested maximum open line lengths for MECL 10K/10KH and MECL III are tabulated in Figures 3-13, 3-14, and 3-15 for various fanouts and line impedances.

3-13. Maximum Open Line Length for MECL 10,100 (Gate Rise Time = 3.5 ns)

	Z_o (OHMS)	FANOUT = 1 (2.9 pF)	FANOUT = 2 (5.8 pF)	FANOUT = 4 (11.6 pF)	FANOUT = 8 (23.2 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	8.3	7.6	6.7	5.7
	68	7.0	6.2	5.0	4.0
	75	6.9	5.9	4.6	3.6
	82	6.6	5.7	4.2	3.3
	90	6.5	5.4	3.9	3.0
	100	6.3	5.1	3.6	2.6
STRIPLINE (Propagation Delay 0.188 ns/in.)	50	6.5	5.9	5.2	4.5
	68	5.6	4.9	3.9	3.2
	75	5.3	4.7	3.6	2.8
	82	5.2	4.4	3.3	2.6
	90	5.1	4.3	3.1	2.4
	100	4.9	4.0	2.8	2.1
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	6.6	5.4	3.8	2.8
	140	5.9	4.3	2.8	1.9
	180	5.2	3.6	2.1	1.3

3-14: Maximum Open Line Length for MECL 10,200, MECL 10H100, 10H210, 10H211 (Gate Rise Time ≈ 2 ns)

	Z_o (OHMS)	FANOUT = 1 (3.3 pF)	FANOUT = 2 (6.6 pF)	FANOUT = 4 (13.2 pF)	FANOUT = 8 (26.4 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX(IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	3.5	2.8	1.9	1.2
	68	3.2	2.3	1.5	0.8
	75	3.0	2.2	1.3	0.7
	82	2.9	2.0	1.2	0.6
	90	2.8	1.9	1.0	0.5
	100	2.6	1.8	0.9	0.4
STRIPLINE (Propagation Delay 0.188 ns/in.)	50	2.8	2.2	1.5	1.0
	68	2.5	1.9	1.2	0.6
	75	2.4	1.7	1.1	0.6
	82	2.3	1.6	0.9	0.5
	90	2.2	1.5	0.8	0.4
	100	2.0	1.4	0.7	0.3
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	2.8	1.8	0.9	0.4
	140	2.4	1.4	0.5	0.3
	180	2.0	1.0	0.3	0.1

3-15: Maximum Open Line Length for MECL III, MECL 10H209 (Gate Rise Time 1.1 ns)

	Z_o (OHMS)	FANOUT = 1 (3.3 pF)	FANOUT = 2 (6.6 pF)	FANOUT = 4 (13.2 pF)	FANOUT = 8 (26.4 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	1.6	1.1	0.7	0.6
	68	1.4	0.8	0.5	0.4
	75	1.3	0.8	0.4	0.3
	82	1.2	0.7	0.4	0.2
	90	1.1	0.6	0.3	0.2
	100	1.0	0.5	0.2	0.1
STRIPLINE (Propagation Delay 0.188 ns/in.)	50	1.2	0.8	0.6	0.5
	68	1.1	0.7	0.4	0.3
	75	1.0	0.6	0.3	0.2
	82	0.9	0.6	0.3	0.2
	90	0.9	0.5	0.2	0.1
	100	0.8	0.4	0.2	0.1
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	1.1	0.6	0.2	0.1
	140	0.8	0.3	0	0
	180	0.6	0.2	0	0

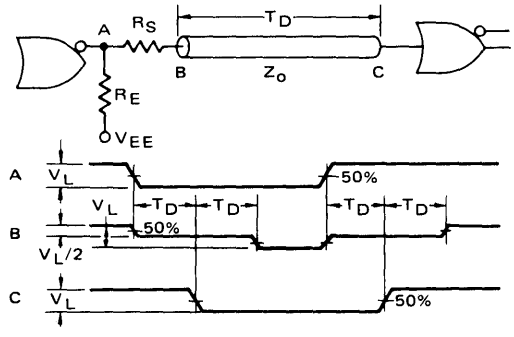
For these tables, line lengths are chosen to limit overshoot to 35% of logic swing and undershoot to 12%.

Series Damped and Series Terminated Lines

Overshoot and ringing on longer lines may be controlled by using series damping or series terminating techniques. Series damping is accomplished by inserting a small resistor (typically 10-75Ω) in series with the output of the gate as shown in Figure 3-16. This technique can be used with all MECL families and is associated with lines not defined by a controlled characteristic impedance, (e.g. backplane wiring, circuit boards without ground plane, and most wire wrapped connections).

The series termination is a specialized case of damping in which the resistor value plus the circuit output impedance is equal to the impedance of the transmission line. The waveforms in Figure 3-16 and the following description of operation are for series termination. A similar analysis may be done for any value of damping resistor and line impedance.

3-16: Driving a Series Terminated Line



The impedance looking back toward the driving gate at point B should be equal to the characteristic impedance of the transmission line. The dc output impedance is 5 ohms for a MECL III gate and 7 ohms for a MECL 10K/10KH gate. AC output impedance is only slightly higher than the dc impedance values. Therefore, if Z_0 is 75 ohms, then the value of R_S must be approximately 68 ohms.

At time = 0, the internal voltage in the circuit switches to the low state which represents a change of 0.9 volts (ΔV_{INT} = -0.9 V). The voltage change at point B can be expressed as:

$$\Delta V_B = \Delta V_{INT}\left(\frac{Z_0}{R_S + R_0 + Z_0}\right),$$

where R_0 is the output impedance of the MECL gate.

Since $R_S + R_0$ is made equal to Z_0 for a series terminated line, then the voltage change at B is 1/2 the voltage, ΔV_{INT}. It takes the propagation delay time

of the transmission line, T_D, for the waveform to reach point C, where the voltage doubles due to the near unity reflection coefficient at the end of the line. The reflected voltage, which is equal to the sending voltage, arrives at point B at a time, T_D, later. No more reflections occur if $R_S + R_O$ is equal to Z_O. Similar waveforms occur when the driving gate switches from the low to the high state.

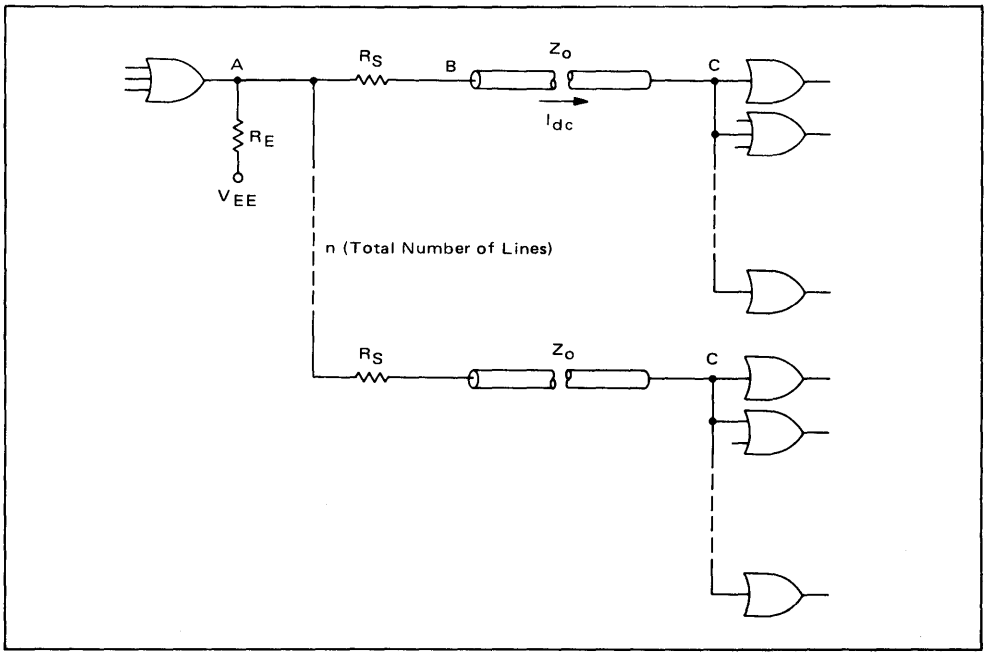
One of the advantages of using series terminated lines is that only the logic power supply is required. Another advantage is the lower overall power requirements. One power supply can also be used with parallel terminated lines described in the next section, but two resistors must be used for the total termination resistor, resulting in the need for considerably more power. In addition, when two power supplies are used with parallel terminated lines using one termination resistor, an extra voltage bus or plane is required to supply -2.0 volts to the termination resistors.

A disadvantage of series termination is that distributed loading along the line cannot be used, because of the half-voltage waveform travelling down the line (see Figure 3-16, waveform B). However there is no limit on the number of lumped loads that can be placed at the end of the series terminated line imposed by reflections at the receiving gate, since all the reflections will be absorbed at the source. Nevertheless, voltage drop across the series terminating resistor due to input current, limits loading to less than 10.

The distance permitted among the receiving gates at the end of the line can be found from Figures 3-13, 3-14, or 3-15. For example, if MECL III were used with 50 ohm microstrip lines, the maximum total separation of four gate loads at the end of a series terminated line is 0.7 inches (see Figure 3-15).

The disadvantages of slower propagation delay and using only lumped loading at the end of a series terminated line can be eliminated at the expense of more transmission lines, as in Figure 3-17. For parallel fanout, n transmission lines can be

3-17: Parallel Fanout Using Series Termination



used. The value chosen for R_S should be the same as discussed previously when n was equal to one.

To determine the value of the emitter pulldown resistor, R_E, the following procedure is recommended.

The value of R_E must be small enough to supply each transmission line with the necessary current. If R_E is made too large, the output transistor will turn off when switching from the high to the low voltage state. The maximum value for R_E can be derived by equating the voltage point at which the output transistor turns off with the midpoint of the logic swing:

$$\Delta V_B = \Delta V_{INT} \left(\frac{Z_o}{R_S + R_o + Z_o} \right),$$

where: ΔV_B = one half the logic swing = 400 mV,

ΔV_{INT} = V_{EE} - logic 1 level = (5.2 - 0.8) V = 4,400 mV, (since the output transistor is turned off, it does not affect the calculation),

R_S = series damping resistance,

R_o = R_E (because the output transistor is turned off).

So:

$$R_{E(max)} = 10 Z_o - R_S .$$

Finally, when n parallel lines are driven as in Figure 3-17:

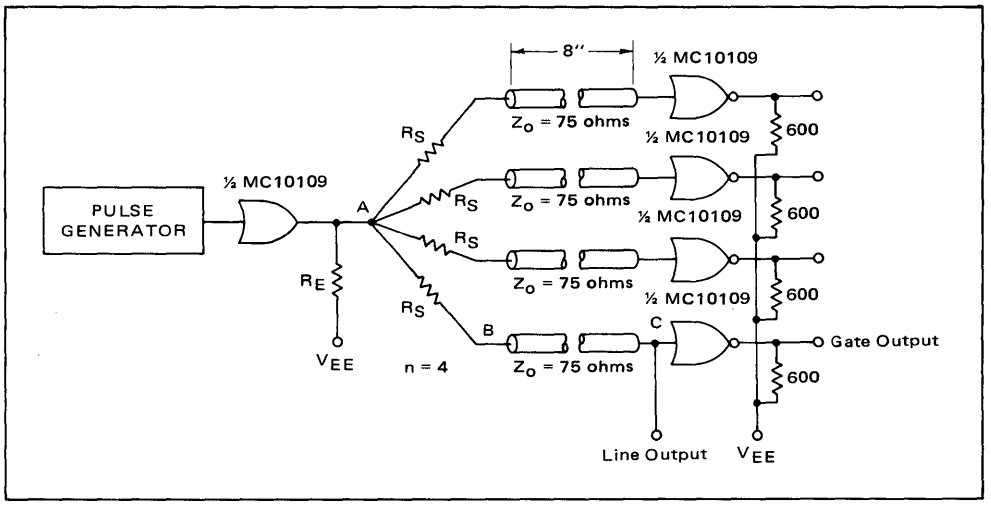
$$R_{E(max)} = \frac{10 Z_o - R_S}{n} .$$

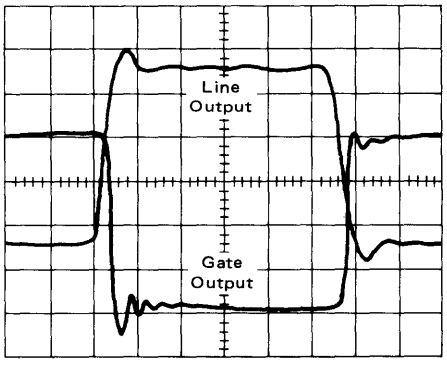
For n = 4, Z_o = 75 ohms, and R_S = 68 ohms, this relation gives R_E = 170 ohms.

Figure 3-18 shows a circuit using MC10109 logic gates. The driving lines have a width of 50 mils and a board thickness of 62 mils. This geometry corresponds to a line impedance of approximately 75 ohms. The length of each line is 8 inches, which produces a line propagation delay of 1.2 ns. The rise and fall times of the driving gate are about 2 ns each. Figure 3-19 shows the trace seen on a Tektronix 567 oscilloscope using the high impedance probe. The waveform of the line output when R_E = 180 ohms (close to the value calculated above) shows that the rise time and overshoot of the rising edge are equal to that of the falling edge. The small overshoot of about 50 mV is due to the line impedance being slightly larger than 75 ohms. This does not affect circuit operation in any way. The rise and fall time at the line output are each 3.3 ns.

Figure 3-20 shows the waveforms when R_E = 600 ohms. In this case the value of R_E is much larger than the 170 ohms value calculated. Consequently, the fall time of the waveform suffers since the output transistor turns off and R_E is unable to supply the proper line current. When the output transistor turns off, the output impedance of the gate becomes that of the pulldown resistor. Calculating the voltage

3-18: Series Termination Test Set-Up Using the MC10109 Gates

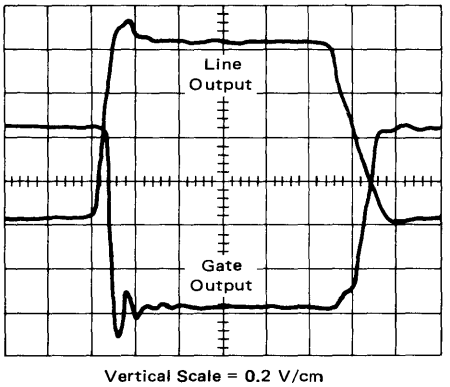




Vertical Scale = 0.2 V/cm
Horizontal Scale = 10 ns/cm

3-19: Waveforms from Test Set-Up of Figure 3-18
(R_E = 180 ohms, n = 4)

3-20: Waveforms from Test Set-Up of Figure 3-18
(R_E = 600 ohms, n = 4)



Vertical Scale = 0.2 V/cm
Horizontal Scale = 10 ns/cm

change at point B shows a ΔV of:

$$\Delta V_B = \Delta V_{INT} \left(\frac{\frac{Z_o}{n}}{R_E + \frac{R_S}{n} + \frac{Z_o}{n}} \right)$$

$$= (-4{,}400) \left(\frac{19}{600 + 17 + 19} \right)$$

$$\approx -130 \text{ mV},$$

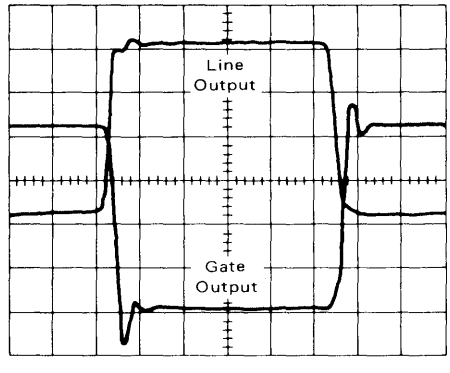
where ΔV_{INT} is the voltage drop in millivolts across the pulldown resistor when high, and n is the number of parallel series terminated lines.

When the waveform reaches the end of the line, the voltage will double to -260 millivolts and a reflection of -130 millivolts will be sent back toward the driving gate. Since the driving gate output is turned off, the reflection coefficient at the source is approximately 0.8. Therefore, after a time of twice the line delay, an additional -200 millivolts is received at the load. These reflections continue until the voltage at the end of the line reaches the logic $\emptyset$ state.

These steps in voltage can be seen in the falling edge of the line output waveform (Figure 3-20), in close agreement with the calculations. The fall time increases by approximately six times the line propagation delay, or 7.2 ns. If the transmission line had been longer, the voltage step duration would have increased correspondingly. Note that the gate output at the end of the line also has an increased rise time and propagation delay.

Figure 3-21 shows the waveforms from the test setup shown in Figure 3-18, when only one line is driven (n = 1) and with R_E = 600 ohms. Using the equation

3-21: Waveforms from Test Set-Up of Figure 3-18 with Only One Line Driven
(R_E = 600 ohm, n = 1)



Vertical Scale = 0.2 V/cm
Horizontal Scale = 10 ns/cm

for $R_{E(max)}$ gives a value of 680 ohms. Note that the rise and fall times are approximately equal (2 ns) meaning that the proper pulldown resistor was chosen. The rise and fall times at the line output are much faster in Figure 3-21 than in Figure 3-19, due to the lighter load at the gate output and reduced nodal capacitance at point A.

Analysis of series damping is very similar to that for a series terminated line. Differences are the line length and the value of the series damping resistor, R_S. For series damping this resistor value is normally smaller than the characteristic impedance of the line. Accordingly line lengths are permitted which are longer than the worst-case open line lengths ($R_S = 0$), as defined in Figures 3-13, 3-14, and 3-15. The same equations for voltage at point B and maximum R_E apply, as did for series terminated lines. In fact, series damping can be used to extend lines to any length, while limiting overshoot and undershoot to a predetermined amount. Figures 3-22 and 3-23 give minimum values of R_S for various line impedances for MECL 10K/10KH and MECL III. For these figures, overshoot was limited to 35% of signal swing and undershoot to 12%. The technique for calculating these R_S values is given in Chapter 7.

Here is an example of how Figure 3-22 and 3-23 can be used. Assume that a MECL III gate must drive a fanout of 2 (6.6 pF) at the end of 1 foot of line in the backplane. The characteristic impedance in the backplane is between 100 and 180

3-22: Minimum Values of R_S for Any Length of Line with Specified Limits of Overshoot and Undershoot, Using MECL 10K/10KH

Z_o (OHMS)	MIN R_S (OHMS) FOR R_o = 15	UNDERSHOOT %	OVERSHOOT %
50	9	12	34.6
68	18	12	34.6
75	21	12	34.6
82	25	12	34.6
90	29	12	34.6
100	34	12	34.6
120	43	12	34.6
140	53	12	34.6
160	63	12	34.6
180	72	12	34.6

3-23: Minimum Values of R_S for Any Length of Line with Specified Limits of Overshoot and Undershoot, Using MECL III

Z_o (OHMS)	MIN R_S (OHMS) FOR R_o = 6	UNDERSHOOT %	OVERSHOOT %
50	18	12	34.6
68	27	12	34.6
75	30	12	34.6
82	34	12	34.6
90	38	12	34.6
100	43	12	34.6
120	52	12	34.6
140	62	12	34.6
160	72	12	34.6
180	81	12	34.6

ohms. An open line should not be used because it exceeds the length given in Figure 3-15: 0.6 in. Another method therefore must be used – coax, twisted pair, or series damped line.

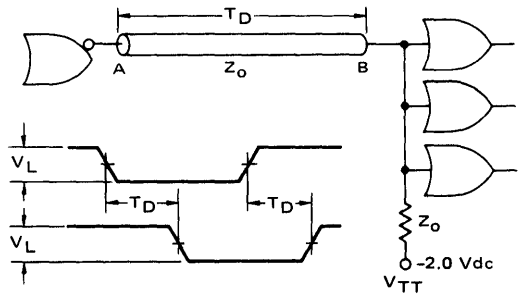
If series damping is used, then from Figure 3-23, a series damping resistor of 81 ohms or larger should be placed in the line at the driving end. The maximum value of the series damping resistor that should be used is 130 ohms for a fanout of 2, since there will be a dc level shift of 90 mV (maximum) caused by the series resistance in the line when the driving gate is in the high state. The 90 mV figure is based on the maximum input current, I_{inH}, of the MECL III gate being 350 μA. ($V = I \cdot R$, where $R = 130\Omega$, and $I = 2 \times 350\ \mu A$).

Both the maximum overshoot and undershoot that can occur are given in the tables. If the proper value of R_S (series damping resistor) is used, as given in the tables, there is no restriction on line length or capacitance at the end of the line for the specified undershoot and overshoot. Of course, ohmic line losses and line propagation delay effects must be considered in the design.

Parallel Terminated Lines

Parallel terminated lines (Figure 3-24) are used for fastest circuit performance and for driving distributed loads. MECL 10K/10KH and MECL III are specified to drive "50 ohm lines." This refers to a line, terminated at the receiving end through a resistor of the characteristic line impedance to -2 volts from the V_{CC} supply. With parallel terminated lines, the line termination supplies the output pulldown. Consequently no other pulldown resistor is required at the output of the driving gate.

3-24: Driving a Parallel Terminated Line



The operation of the parallel terminated line is comparatively simple. The signal swing at point A is:

$$\Delta V_A = \Delta V_{INT} \left(\frac{Z_o}{R_o + Z_o} \right)$$

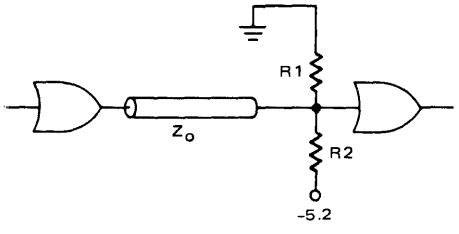
Since ΔV_{INT} is approximately 0.9 volts and the output impedance is low ($R_o \ll Z_o$), the signal swing at point B is typically greater than 800 millivolts. This signal propagates down the line, undistorted, in time T_D. Since the terminating resistor equals Z_o, there is no reflection and the sequence is ended.

An important feature of parallel termination is the undistorted waveform along the full length of the line. It should be noted that parallel termination can also be used with wire-wrap and backplane wiring where the characteristic impedance is not exactly defined. By approximating the characteristic impedance, the reflection coefficient ρ_L will be reasonably small, so overshoot and ringing will be held to within safe limits.

For large systems where total power is a consideration, the lines are normally terminated to a -2 Vdc supply. For power conservation, this is the most efficient manner of terminating MECL circuits. The drawback, of course, is the requirement of an additional supply voltage.

An alternate approach is to use two resistors in the way depicted in Figure 3-25. The Thevenin equivalent of these two resistors is one resistor equal to the

3-25: Parallel Termination with a Single Power Supply



THEVENIN EQUIVALENT RESISTORS FOR TERMINATION

Z_o (OHMS)	R1 (OHMS)	R2 (OHMS)
50	81	130
70	113	182
75	121	195
80	130	208
90	146	234
100	162	260
120	194	312
150	243	390

characteristic impedance of the line and terminated to -2 Vdc. R1 and R2 may be obtained as:

$$R_2 = 2.6\, Z_O$$

$$R_1 = \frac{R_2}{1.6}$$

Transmission Line Comparison

Since there are advantages to both series and parallel lines, the decision to use one or both methods in a system depends on the preference of the designer and on his system requirements. Figure 3-26 lists typical cases where terminations may be necessary, along with techniques which may be used.

Parallel terminated lines have the advantage when speed is the main factor. Loading a long line will not affect the propagation delay of the driving gate nor its edge speed, but loading does increase the propagation time of the signal down the line. It will be shown in Chapter 7 that the increase in delay time with loading is about twice as great for series damped lines as for parallel terminated lines. For short lines the capacitive load increases the propagation delay of the gate by slowing down the edges.

As mentioned previously, a big advantage of parallel termination is that the signal is undistorted along the full length of the line. When driving a large fanout, the loads may be distributed along the line with short stubs, instead of being lumped at the end of the line as is done with series termination. On the other hand, series

3-26: Types of Lines Recommended

SITUATION	PARALLEL TERMINATED LINE	SERIES TERMINATED LINE	OPEN LINE
1. Line lengths are shorter than specified (Fig. 3-13,-14,-15).	Yes	Yes	Yes
2. Driving gate drives 1 line, of length greater than specified (Fig. 3-13,-14,-15).	Yes	Yes	No
3. Driving gate drives 3 or more lines of lengths greater than specified (Fig. 3-13,-14,-15).	No	Yes	No
4. Gate loads must be distributed along a long transmission line.	Yes	No	No
5. Many gates are lumped at the end of long transmission line.	Yes	Yes	No
6. Only one power supply is to be used and the LOWEST power consumption is desired.	No	Yes	Yes
7. Two power supplies are used and the lowest power consumption is desired.	Yes	Yes	Yes
8. Backplane wire lengths are shorter than specified (Fig. 3-13,-14,-15).	Yes	Yes	Yes
9. Backplane wire lengths are longer than specified (Fig. 3-13,-14,-15) and a ground screen is used in backplane.	Yes (150 ohms)	Yes (100 ohms)	No
10. Backplane wire lengths are longer than specified (Fig. 3-13,-14,-15). (no ground screen is used).	Use Twisted Pairs, or Coax	No	No
11. Large temperature differentials exist between card bays or racks.	Use Twisted Pairs	No	No
12. Driving gate drives 3 or more lines in backplane longer than specified (Fig. 3-13,-14,-15).	No	Yes (100 ohms)	No
13. Wires are bundled closely together near noisy portion of system.	Use Coax or Twisted Pairs	Coax	No

termination has the ability to drive several parallel lines, as long as the drive current is compensated by the value of the output pulldown resistor. The MECL 10K/10KH and MECL III outputs will drive only one 50-ohm parallel terminated, or two 100-ohm parallel terminated lines. Exceptions to this rule include the MC10110/210, MC10111/211, MC10H210 and MC10H211 which have multiple gate outputs for driving three parallel 50 ohm lines, and the MC10123, MC10H330/332/334 which can drive 25 ohm lines.

Termination power is lowest for a parallel terminated line terminated to −2 Vdc. However, similar power savings may be realized by connecting the pulldown resistor for open wire or series terminated lines to −2 Vdc. Using a single power supply, the series termination and pulldown resistor uses less power than the two-resistor parallel termination. Typical power in the terminating resistors for 50 ohm lines for signals with 50% duty cycle is tabulated in Figure 3-27.

Additional information for calculating system power is contained in Chapter 5, "Power Distribution."

Crosstalk on circuit boards is normally not a problem with MECL, because the relationship of the signal line to the ground plane minimizes the energy coupled to adjacent lines. Even so, series terminated lines have less crosstalk than parallel terminated lines. The reason is that only one-half the logic swing is sent down the series terminated line. As a result the switched current is only one-half that of the larger, parallel terminated signal. This smaller signal energy results in less crosstalk.

3-27: Power Consumption for Various 50-Ohm-Line Terminations

TERMINATION SCHEME	RESISTOR ARRANGEMENT	RESISTOR POWER CONSUMPTION
Parallel	50 ohm to -2 Vdc	13 mW
Series	510 ohm to V_{EE}	30 mW
Parallel Combination	82 ohm to V_{CC}, and 130 ohm to V_{EE}	144 mW

Wirewrapped Cards

Wirewrapped cards can be used with MECL 10K/10KH. The fast edge speeds (1 ns) of MECL III exceed the capabilities of normal wirewrapped connections. Mismatch at the connections causes a reflection which distorts the fast signal, reducing noise immunity significantly or causing erroneous operation. The mismatch remains with MECL 10K/10KH but the distance between the wirewrap connection and the end of the line is well within the allowable stub-length distance, so the reflections cause no problem.

For lines longer than maximum allowable open line length for MECL 10K/10KH, either series or parallel termnation may be used. The parallel resistors are relatively high (typically 100 to 150 ohms) and are normally used only with MECL 10K/10KH because it can supply the output current required by the pulldown resistors. Of course series damping resistors may be used with wirewrapped lines for MECL 10K/10KH. Twisted pair lines may be used for longer distances across large wirewrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differently using a line receiver.

Twisted pair line driving is an important feature of MECL circuits and is discussed in more detail in the next chapter. The recommended wirewrapped circuit cards have a ground plane on one side and a voltage plane on the other, to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wirewrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize crosstalk between parallel paths in the signal lines. Point-to-point wire routing is recommended because crosstalk will be minimized and line lengths will be shortest.

Production area for MECL Integrated Circuits

CHAPTER 4 System Interconnections

Signal connections between logic cards, card panels, and cabinets are important for obtaining the maximum system performance possible with MECL circuits. To understand how ringing and crosstalk affect system operation, it is helpful to review guaranteed noise margins, discussed in Chapter 1.

Noise margin is defined as the difference between a worst case input logic level and the worst case threshold closest to that logic level. Guaranteed noise margin (N.M) for MECL 10K is:

$$NM_{1 \text{ level}} = V_{OHA \text{ min}} - V_{IHA \text{ min}}$$

$$= -0.980 \text{ V} - (-1.105 \text{ V}) = 125 \text{ mV};$$

$$NM_{\phi \text{ level}} = V_{ILA \text{ max}} - V_{OLA \text{ max}}$$

$$= -1.475 \text{ V} - (-1.630 \text{ V}) = 155 \text{ mV}.$$

The threshold levels associated with MECL 10K (V_{OHA}, V_{IHA}, V_{ILA} and V_{OLA}) are synonomous with V_{OHmin}, V_{IHmin}, V_{ILmax} and V_{OLmax} for MECL 10KH. The guaranteed noise margins (N.M.) for MECL 10KH are therefore:

$$NM_{1 \text{ level}} = V_{OH \text{ min}} - V_{IH \text{ min}}$$

$$= -0.980 \text{ V} - (-1.130 \text{ V})$$

$$= 150 \text{ mV}$$

$$NM_{\phi \text{ level}} = V_{IL \text{ max}} - V_{OL \text{ max}}$$

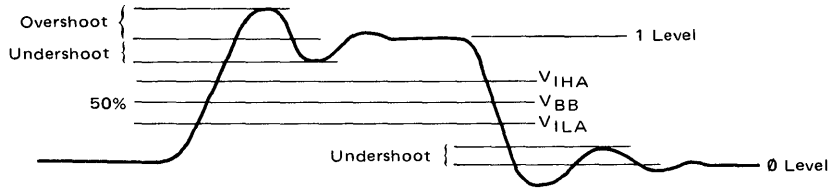
$$= -1.48 \text{ V} - (-1.63 \text{ V})$$

$$= 150 \text{ mV}$$

Thus, using the worst case design conditions, MECL 10K/10KH have 125 mV/150 mV respectively to guard against signal undershoot, and power or thermal disturbances. However, using *typical* logic levels of –0.900 volts and –1.750 volts, the circuit noise protection is typically greater than 200 mV for both the logic 1 and logic ϕ levels. Power and thermal design will be discussed in Chapters 5 and 6.

Good circuit interconnections should allow no more than 100 to 110 mV undershoot. The overshoot and undershoot waveform conventions are shown in Figure 4-1.

4-1: MECL Waveform Terminology



Both overshoot and undershoot are functions of many variables: line length, capacitive/inductive loading, rise time, and so on. Thus, in general, to maintain undershoot less than 110 mV requires one or more of the following:

- Reduction of system rise times;
- Reduction of interconnect line lengths;
- Use of matched, terminated transmission lines.

Reduction of rise time is easily accomplished by going to a slower MECL family, but this reduction in rise time may limit the use of the high bit rates and narrow pulse widths necessary for system performance goals. Interconnection line lengths are dictated by the system design and are routinely minimized as a matter of practice. Impedance matching of the interconnection lines remains then, the one variable which can be exploited for limiting the undershoot and ringing.

When using the faster varieties of MECL circuits, the type of card-to-card wiring in the system backplane area should be considered carefully. The initial decision is between two basic methods of board-to-board interconnect:

1. Controlled impedance, e.g., mother-daughter boards using microstrip lines, coax, ribbon flex, or twisted pair interconnects;
2. Uncontrolled impedance, e.g., open wire backplane wiring – with possible wide variations in characteristic impedance.

With MECL III, method 1 *must* be used. The entire system must be in a transmission line environment. While MECL 10K/10KH is designed to drive transmission lines, the slow edge speed allows it to operate with the more economical wire over a ground plane layout. Wire over a ground plane or ground screen often has a characteristic impedance between 100 and 150 ohms, and can be series damped or parallel terminated for extended open wire lengths in the backplane area. Both wirewrapped and soldered wire connections are suitable for connecting wires to card connectors in MECL 10K/10KH systems.

When designing system interconnections, four parameters must be taken into consideration:

- Propagation delay per unit length of line;
- Line attenuation;
- Crosstalk;
- Reflections due to mismatched impedance characteristics of the line, connectors, and line terminations.

Propagation delay of a line is important because unequal delays in parallel lines may cause timing errors. Also, for long lines the total delay time will often seriously affect system speed. Since the propagation delay of one foot of wire is

approximately equal to the propagation delay of a MECL 10K gate, line length must be minimized when total propagation time is important.

Attenuation is also a parameter of a line. It varies with frequency and is seen as an increase in impedance for an increase in frequency. The effects of attenuation first appear as a degradation in edge speed. This is followed by a loss of signal amplitude for high frequencies on long lines. A rounding of the waveform occurs, since the higher frequency components required to give sharp square waves are attenuated more than low frequency components. Within a backplane attentuation is seldom a problem, but it must be taken into consideration when interconnecting among panels or cabinets.

Crosstalk is the undesired coupling of a signal on one wire to a nearby wire. Since a coupled pulse in the direction of undershoot results in a reduction of noise immunity, precautions should be taken to limit crosstalk. A good ground system and shielding are the best methods for limiting crosstalk. Differential twisted pair line interconnections can avoid problems caused by crosstalk by virtue of the common mode rejection of the receivers used with such an arrangement. Crosstalk is discussed in more detail under the heading "Parallel Wire Cables" later in this Chapter.

Reflections due to mismatched lines in system interconnections cause the same loss of noise immunity as discussed in Chapter 3 for printed circuit boards. The ability to terminate a line effectively is primarily a function of how constant the impedance is over the length of the line. Because it has high uniformity, coaxial cable is easier to terminate than open wire. Yet in many cases, twisted pair cable or ribbon cable may be purchased with specifications on the impedance of the line.

Connectors

There are very few high frequency edge connectors that do not cause waveshape distortion when rise times are under 1 ns. The few that don't are of the "matched impedance" type in which the on-board strip transmission line flows right into and out of the connector, without encountering a mismatch. Unfortunately, this form of connector is usually expensive and is often difficult to design with.

The only forms of MECL logic which require the use of matched edge connectors are the MECL III family and the MC10H209. With rising edges of approximately 2 ns, the MECL 10K families may utilize conventional edge connectors. With them, very little mismatch occurs: typically < 20 mV.

Coaxial cable connectors that have near ideal characteristics over the bandwidths exhibited by MECL logic exist in a variety of types. The most popular are the BNC type and the subminiature SMA, SMB, or SMC types. The smaller miniature types offer direct microstrip to coaxial interconnects with low voltage standing wave ratio (VSWR), i.e. minimum reflection.

Coaxial Cable

Coaxial cable offers many advantages for distributing high frequency signals. The well defined and uniform characteristic impedance of the line permits easy matching. The ground shield on the cable minimizes crosstalk. Low attenuation at high frequencies makes good coaxial cable very desirable for handling the fast rise times associated with MECL signals.

The line bandwidths required for optimum MECL use are:

$$f = \frac{k}{t_r}, \qquad \text{where: } k = 0.37^*, \quad t_r = \text{rise time;}$$

so: $$f = \frac{0.37}{1 \times 10^{-9}} = 370 \text{ MHz for MECL III with a 50 } \Omega \text{ load}$$

and: $$f = \frac{0.37}{3.5 \times 10^{-9}} = 106 \text{ MHz for MECL 10K with a 50}\Omega \textit{ load}$$

and: $$f = \frac{0.37}{1.8 \times 10^{-9}} = 206 \text{ MHz for MECL 10KH with a 50}\,\Omega\text{load.}$$

At MECL frequencies, skin effect is a primary cause of attenuation. Dielectric losses are insignificant below 1 GHz for the common dielectric materials – polyethylene or teflon. Attenuation due to skin effect is proportional to the square root of frequency and so may be plotted conveniently on log-log paper. Figure 4-2 contains data for three cable types tested. Maximum cable lengths recommended with the various MECL logic families can be derived from these plots as the following example will show.

For maximum signal reductions of 100 mV in the 1 and Ø levels (i.e. a logic swing reduction from 800 mV p/p to 600 mV p/p) the permissible attenuation would be:

$$\text{Loss (dB)} = 20 \log\left(\frac{V_{in}}{V_o}\right) = 20 \log\left(\frac{0.8}{0.6}\right) = 2.5 \text{ dB.}$$

For MECL III with RG58/U the loss at 370 MHz is found to be 12 dB/100′ from Figure 4-2. Thus, with the 100 mV restriction:

$$\text{Max Length} = 100 \text{ ft.} \cdot \left(\frac{2.5 \text{ dB}}{12 \text{ dB}}\right) = 20.8 \text{ ft.}$$

Figure 4-3 shows curves giving maximum line length as a function of operating frequency for the same three cable types used for Figure 4-2. Each curve assumes 2.5 dB permissible loss. It should be noted that a high bandwidth line is necessary to preserve fast signal edges, regardless of the bit rate of the system.

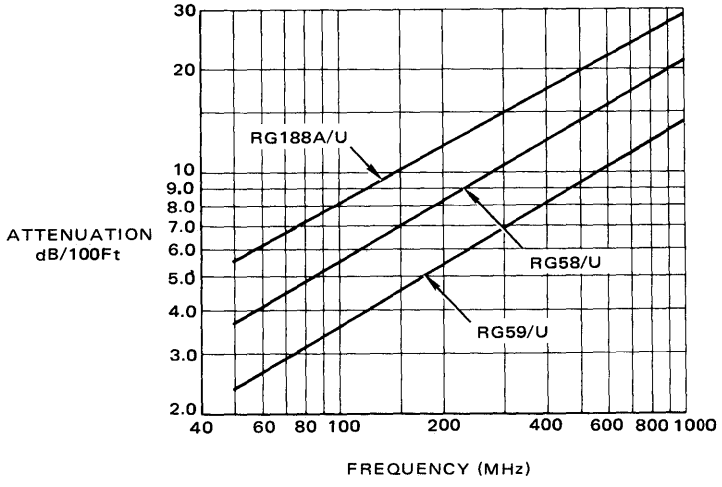
Figure 4-3 and the preceding calculations assume the coaxial line is properly terminated with a resistive load equal to the characteristic impedance of the line. The reactive component of the termination is of increasing importance at high frequencies. At such frequencies, reactive elements can change the terminating impedance, thus causing reflections on the line. In addition, the effective inductance or capacitance would distort the output waveform, causing additional reflection down the line.

Standard carbon resistors were carefully measured at high frequencies to determine their reactive components. Results are listed in Figure 4-4. The effective circuit is a resistor with an inductor in series. Carbon resistors display more inductive reactance as the resistor values become smaller, and display more capacitive reactance as the values get larger. However, 75 ohm resistors are normally close to being purely resistive.

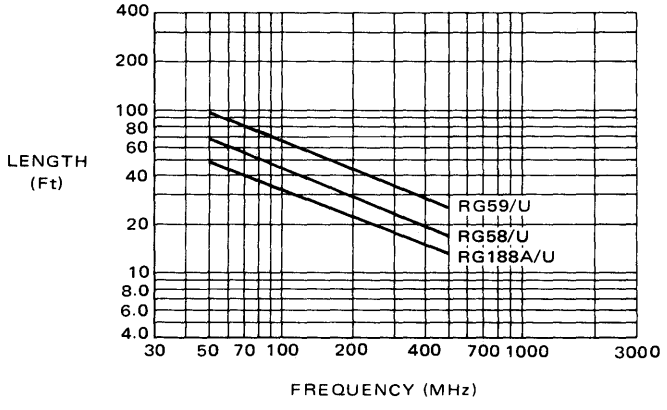
---

*O. Gene Gabbard, "High Speed Digital Logic for Satellite Communications." *Electro-Technology*, April 1969, p. 59.

4-2: Coaxial Cable Attenuation versus Frequency



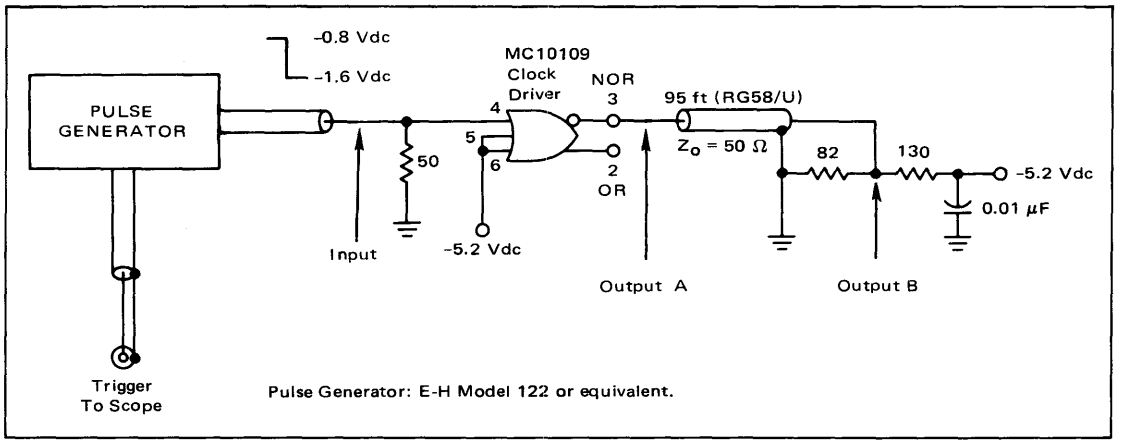
4-3: Coaxial Cable Length versus Operating Frequency: Constant 2.5 dB Loss Curves



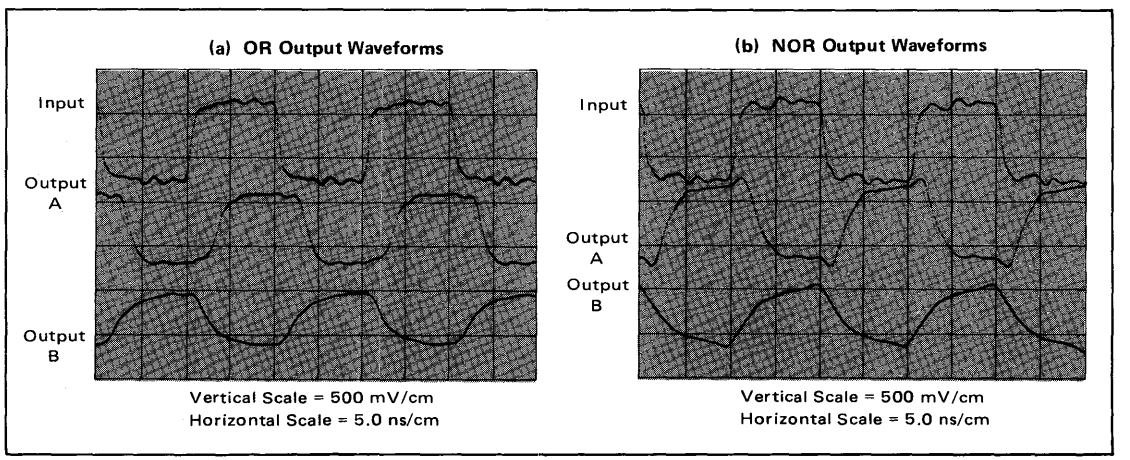
TEST CONDITION	Z = R + jX
1/2 W, 51 ohms, 500 MHz	Z = 51.8 + j15.5
1/2 W, 51 ohms, 300 MHz	Z = 51.4 + j5.6
1/4 W, 51 ohms, 500 MHz	Z = 48.8 + j6.1
1/4 W, 51 ohms, 300 MHz	Z = 49.4 + j0.29
1/8 W, 51 ohms, 500 MHz	Z = 51.5 + j6.7
1/8 W, 51 ohms, 300 MHz	Z = 51.7 + j1.6

4-4: Impedance Characteristics of Carbon Resistors Measured on a GR Admittance Bridge

4-5: Line Driver Test Circuit



4-6: Line Driver Test Circuit Input and Outputs, Observed Via High Impedance 'Scope Probes.



4-7: Typical Switching Times

(Test Circuit Figure 3-5, T_A = 25°C, f = 20 MHz)

Output A

TEST		TIME (ns)
OR		
t_{pd++}	(50% to 50%)	2.6
t_{pd--}	(50% to 50%)	2.7
t_r	(10% to 90%)	2.6
t_f	(90% to 10%)	2.0
NOR		
t_{pd+-}	(50% to 50%)	2.6
t_{pd-+}	(50% to 50%)	2.5
t_r	(10% to 90%)	2.4
t_f	(90% to 10%)	2.7

Output B

TEST		TIME (ns)
OR		
t_r	(10% to 80%)	3.8
	(10% to 90%)	5.4
t_f	(80% to 10%)	3.4
	(90% to 10%)	5.4
NOR		
t_r	(10% to 80%)	3.8
	(10% to 90%)	5.4
t_f	(80% to 10%)	3.7
	(90% to 10%)	5.7

The reflection at 300 MHz for a 50 ohm line using a 1/2-watt 51 ohm carbon resistor can be calculated:

$$\rho = \frac{Z_L - Z_o}{Z_L + Z_o},$$

where: Z_L = load impedance,

Z_o = line impedance;

so:
$$\rho = \frac{51.4 + j5.6 - 50}{51.4 + j5.6 + 50}.$$

Calculations yield:

$$\rho = 0.055 \ \angle 72.8° \ .$$

As a result, (0.055) • (800 mV logic swing) = 44 mV, is reflected back down the transmission line. Clearly, this is much less than the 300 mV maximum overshoot recommended for safe MECL usage. With a slow repetition rate in relation to the propagation delay of the line (time per pulse $>3T_D$) the reflection appears as a small overshoot at the receiving end of the line. In high frequency operation the reflection may subtract from the transmitted signal. The amount would depend on the exact length of the line and the propagation velocity of the line. Subtracting signals appear to reduce the signal on the line, as if either the signal were attenuated, or as if the driving gate were bandwidth limited.

Standard carbon 1/8 watt resistors have been found to have good high frequency characteristics when used with MECL III. Either 1/8 or 1/4 watt resistors work well with MECL 10K/10KH. When using precision wire wound or film resistors, care should be taken to determine the high frequency properties of these devices. Most wire wound and some film resistors become very inductive at high frequencies.

The fanout at the end of a coaxial line should also be limited at high frequencies because of reactive loading. At 300 MHz the fanout should be limited to four. The terminating resistor leads and circuit leads should be kept short. In many cases it is desirable to restrict long interconnecting cables to a fanout of one to minimize reflections and therefore to maintain a high degree of noise immunity.

The propagation velocity is very high in coaxial cable. Computing the propagation delay as:

$$t_{pd} = 1.017 \sqrt{e_r}$$

the delay for solid teflon and polyethylene insulated cables is 1.54 ns per foot (dielectric constant, $e_r \approx 2.3$). This compares with 2.2 ns per foot for stripline as calculated in Chapter 3. For maximum propagation velocity, coaxial cables with styrofoam or polystyrene beads in air dielectric may be used. However, many of these cables have high characteristic impedances and are slowed by capacitive loading. Nonetheless, coaxial cable definitely should be used when sending high repetition rate MECL signals over long lengths.

Illustrated in Figure 4-5 is a circuit used to test the performance of coaxial cable driven by an MC10109 gate. Figures 4-6 (a) and (b) show the waveforms of the circuit with 95 feet of RG58/U connecting cable. Output B in each figure clearly shows the waveform for a skin-effect limited line. Skin effect causes the waveform to rise sharply for the first 50% of the swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform rise time is 30 times greater than the 0 to 50% rise time when the cable is skin effect limited. The output amplitude of the cable is at least 200 mV p/p less than the input, as would be expected from Figure 4-3.

Figure 4-7 presents the test results for the circuit in Figure 4-5. Notice that the numerical data show that at the output of the line, the time from 10 to 80% is much less than 10 to 90% – because of the coaxial skin effect. When operating within the limits discussed previously in this chapter, MECL signals are transmitted over coaxial lines with minimum distortion.

Differential Twisted Pair Lines and Receivers

Twisted pair line, differentially driven into a MECL line receiver (Figure 4-8), provides maximum noise immunity. This is because any noise coupled into a twisted pair line generally appears equally on both wires (common mode). Because the receiver responds only to the differences in voltage between the lines, crosstalk noise is ignored, since it is picked up equally by each of the two lines of the pair. This holds true up to the common mode noise rejection limit of the receiver. Quad line receivers, such as the MC1692, have +1 and -1.8 volt common mode rejection limits before the receiver's output approaches MECL input threshold levels. The Common mode rejection lower limit can be improved to a -2.5 volt limit by using MECL 10K/10KH line receivers (e.g. MC10115, MC10116, MC10H115 or the MC10H116).

With devices such as these, the constant current source employed in the emitter node of the differential pair allows the increase in common mode rejection. This improvement is useful when signals are sent from circuits other than MECL. The MC1650 A/D Comparator is also used as a special purpose line receiver and offers ±2.5 volts common mode rejection. However the standard line receivers have more than adequate common mode noise rejection to handle any crosstalk between MECL signal lines. If higher voltage signal lines are run in parallel with MECL lines, shielded twisted pair lines may be used to reduce crosstalk further.

For low frequency operation, line length is limited by the dc resistance of the wire used and the voltage gain of the line receiver. In order to determine line length allowed it is first necessary to examine the required signal at the end of the line, and the amplification possible with the receiver. The typical differential voltage gain of the circuit (Figure 4-9) may be calculated. . .

Assume Q_2 and Q_3 are conducting. Then:

$$\text{gain} = g_m R_C .$$

R_C is known, and:

$$g_m = \frac{q\alpha I_E}{4KT},$$

where: $$I_E = \frac{V_{CS} - V_{BE}}{R_E} \cong 4.0 \text{ mA}$$

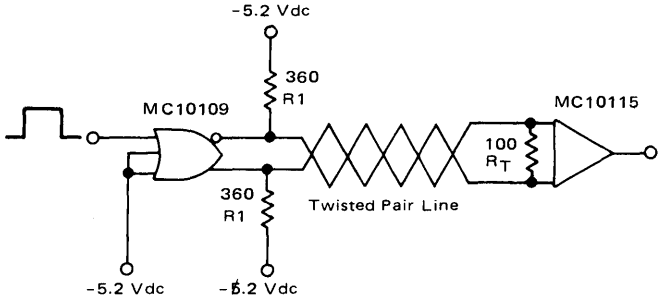
$$\alpha = \frac{\beta}{\beta + 1} \approx 1 \quad (\beta >> 1 \text{ for } Q_2),$$

K = Boltzmann constant = 1.38×10^{-23},

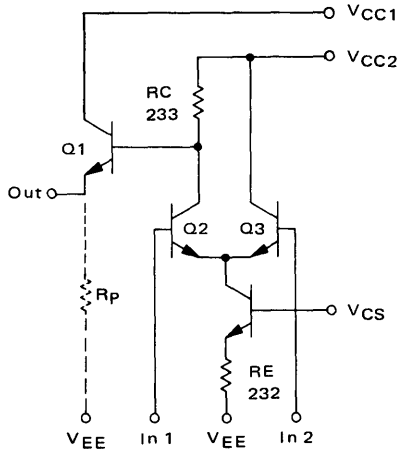
T = temperature degrees Kelvin $\approx$ 300,

and q = charge of electron = 1.602×10^{-19}.

4-8: Twisted-Pair Line Driver and Receiver



4-9: 1/4 MC10115 Schematic



Proceeding with the numerical calculations gives $g_m = 3.9 \cdot 10^{-2}$, and voltage gain = 9.0 V/V.

Allowing for 20% resistor tolerances, and temperature variations, the circuit gives a gain of at least 7 V/V. To obtain MECL level outputs, the minimum required imput signal is 800 mV÷7 = 114mV (differential). Referring to Fig. 4-8, the voltage drop across the input terminating resistor, R_T is,

$$V_T = \overbrace{(V_{EE} - 1 \text{ logic level})}^{\text{net voltage}} \bullet \overbrace{\left(\frac{R_T}{R_1 + R_T + R_{Line}}\right)}^{\text{fraction across } R_T},$$

when resistor ratios determine the low level output.

For large R_T or R_{Line} values, the lower driver output limits at about 800 mV below the high output. For calculating maximum line resistance, use the relation:

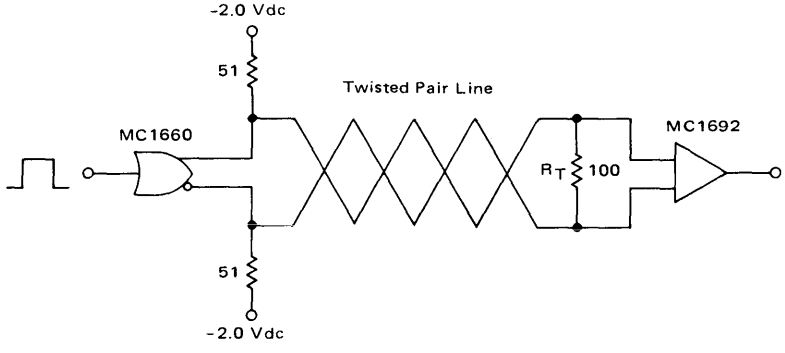
$$V_T = |V_{OH} - V_{OL}| \bullet \frac{R_T}{R_T + R_{Line}} .$$

Setting V_T = 150 mV minimum for conservative operation, the maximum line resistance is found to be 433 ohms. The resistance of #24 AWG wire averages 26 ohms per 1000 feet, giving a theoretical permissible length of over 1.5 miles of wire. Clearly, the ac attenuation of the line will be the realistic limiting factor.

4-10: Attenuation of 50 Ft Twisted Pair Line with MC10109 Line Driver

FREQUENCY (MHz)	MAX DIFFERENTIAL VOLTAGE AT R_T (mV)
25	600
50	475
75	350
100	240
125	175

4-11: MECL III Twisted Pair Line Driver and Receiver



4-12: Attenuation in a 50 Ft Twisted Pair Line with a MECL III Driver

FREQUENCY (MHz)	VOLTAGE AT R_T (mV)
50	380
75	340
100	320
125	280
150	250
175	180
200	160
225	150
250	140
275	120
300	100

4-13: Attenuation in a 10 Ft Twisted Pair Line with a MECL III Driver

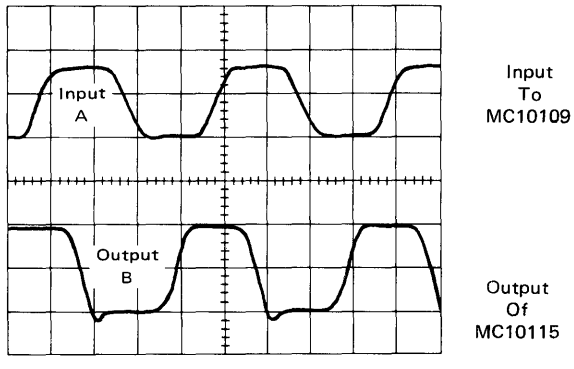
FREQUENCY (MHz)	VOLTAGE AT R_T (mV)
50	440
75	420
100	400
125	390
150	380
175	360
200	300
225	270
250	250
275	240
300	230

Figure 4-10 contains data for the attenuation of a 50 foot twisted pair line using the circuit of Figure 4-8. The voltage at R_T is the peak-to-peak voltage at either input. Driving and receiving the twisted pair line with the MECL III circuits as shown in Figure 4-11 yields the results in Figure 4-12. Comparison of the attenuation data in Figures 4-10 and 4-12 shows that the twisted pair line is bandwidth limited rather than limited by the MECL drivers. Reducing the line length to 10 feet of course results in less attenuation (cf Figure 4-13).

For very long lines the MECL 10K MC10115 line receiver will operate faster than the MECL III MC1692 receiver. The reason is that the voltage gain of the MC10115 is slightly higher than that of the MC1692. Driving a 1000 foot twisted pair line, the MC10115 would operate at 6.5 MHz with 600 mV output, while the MC1692 would be limited to 6.2 MHz for the same output.

Despite the gain difference, as lines become shorter ($<<$ 1000 ft.), the MC1692 will switch faster, since the MC10115 displays *bandwidth* limitations when used on short lines. Figure 4-14 shows the behavior of the circuit of Figure 4-8 when driving a 50-foot line at 50 MHz. The 2 ns rise and fall times of the receiver can be seen at the output of the MC10115 receiver. The same line driven by the MECL III circuit of Figure 4-11 yields the waveforms of Figure 4-15. The faster switching times of MECL III are shown on the output of the MC1692. For both circuits, the propagation down the line is 70 ns for 50 feet of line. At best, overall circuit performance is improved only from 74 to 72 ns by using the faster MECL III.

4-14: 50 Ft Twisted Pair Line with MECL 10K

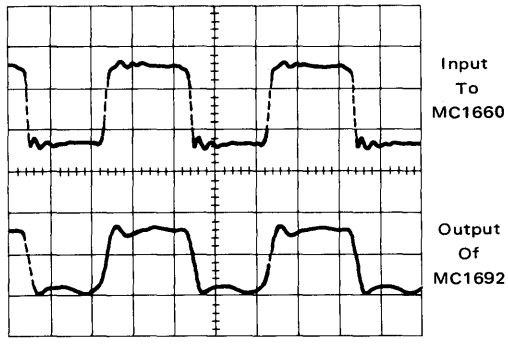


Horizontal Scale = 5 ns/div.
Vertical Scale = 500 mV/div.

However, The MECL III circuits do offer a big advantage over MECL 10K of high rate capabilities on lines shorter than 10 feet. The result of driving twisted pair lines at high speed is shown by the waveforms in Figure 4-16. The traces were obtained for the circuit of Figure 4-11 driving a 10-foot line at 350 MHz. Both the attenuation of the line and the bandwidth of the MC1692 limit the output signal to about 650 mV, which is indeed still a useful MECL signal.

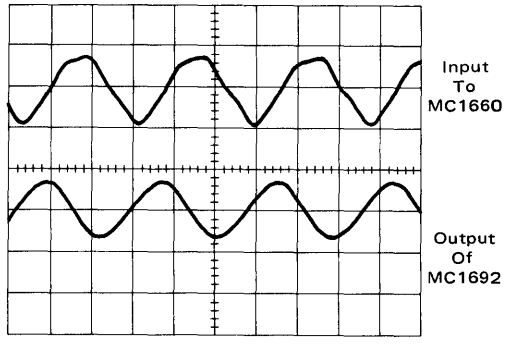
Party line operaton over a single twisted pair line with MECL receivers may be used for saving space, for reducing connections and wiring, as well as to benefit from the party line two-way scheme. Figure 4-17 shows a method for using MECL in a data bus circuit. All driving gates are operating in a Wired-OR configuration requiring that all drive gate outputs be held low when not sending data. (V_{BB} is

4-15: 50 Ft Twisted Pair Line at 50 MHz with MECL III



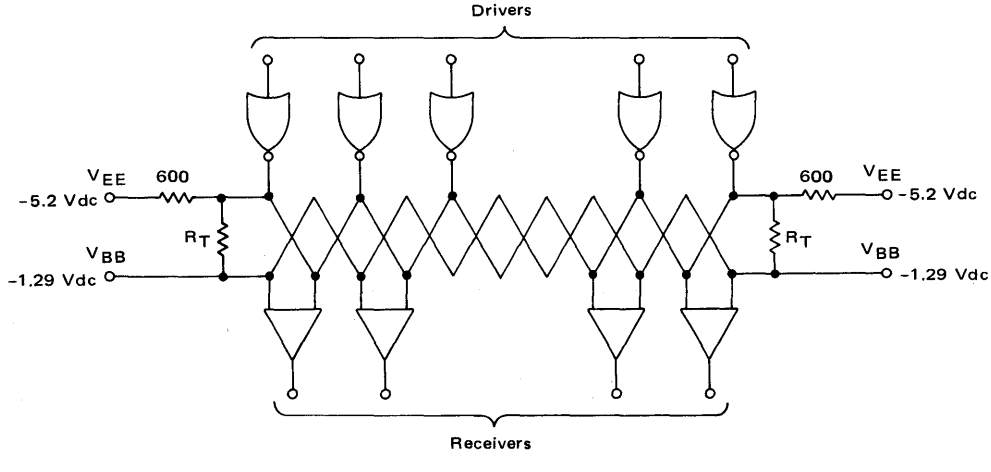
Horizontal Scale = 5.0 ns/cm (Both Traces)
Vertical Scale = 500 mV/cm (Both Traces)

4-16: 10 Ft Twisted Pair Line Operated at 350 MHz with MECL III



Horizontal Scale = 1.0 ns/cm (Both Traces)
Vertical Scale = 500 mV/cm (Both Traces)

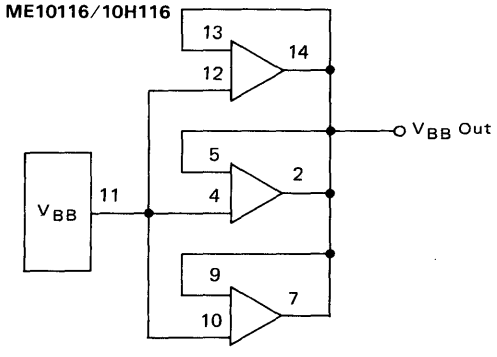
4-17: Party Line Operation with MECL Line Drivers and Receivers



available from the MC10114, MC10115/H115, MC10116/H116, and MC1692L and may be buffered as shown in Figure 4-18 to handle the necessary termination current).

All receivers operate in parallel. When driving long lines party-line style, it should be remembered that the receivers are operating single-ended. Consequently, the voltage gain is approximately one-half that for differential operation. Line attenuation must be computed accordingly. However, the advantages of crosstalk immunity deriving from common mode rejection of the differential line receiver remain. When stubbing off the data bus, the rules shown in Figures 3-13, 3-14, and 3-15 apply.

Twisted pair lines and line receivers offer several system advantages, when operating MECL circuits under adverse conditions. The following example is used to illustrate some of these advantages.



4-18: V_{BB} Generator

MECL 10K is specified to have a V_{OHA} min of -0.980 volts and a V_{IHA} min of -1.105 volts for a noise immunity of 125 mV, with both circuits at 25°C ambient temperature. However, if the driving gate is operating at 0°C, V_{OHA} min is reduced to -1.020 volts; if the driven gate is operating at 50°C the V_{IHA} min is increased to -1.075 volts; so the resultant noise immunity is reduced to 55 mV. To compound the worst case conditions, consider temperature and power supply changes also: if the driving gate is operated at a -5.46 volt supply (+5%) and 0°C temperature, the V_{OHA} min is -1.024 volts. With the driven gate operating at a -4.94 volt supply voltage (-5%) and 50°C temperature, V_{IHA} min is -1.037, giving a worst case noise immunity of 13 mV. Testing has shown that under these extreme conditions, worst case noise immunity in system usage is about 70 mV and circuits operating at typical levels have about 170 mV noise immunity.

The effect of temperature and power supply variations on noise margins is smaller for MECL 10KH than MECL 10K. At 25°C MECL 10KH is specified to have a V_{OH} min of —0.98 volts and a V_{IH} min of —1.13 volts for a noise immunity of 150 mV. If the driving gate operates at 0°C and the driven gate operates at 50°C, V_{OH} min is reduced to —1.02 volts and V_{IH} min is increased to —1.10 volts. The resulting noise margin is 80 mV. The effect of power supply variation is extremely small and can generally be ignored.

However, this somewhat unrealistic example does illustrate the reduction in noise immunity under very adverse conditions. Any noise or voltage drop on the system ground would add to the loss of noise immunity. Conditions similar to MECL 10K/10KH hold for MECL III with the voltages changed to reflect the change in input voltage due to the bias

point level, and the change in output voltage due to loading.

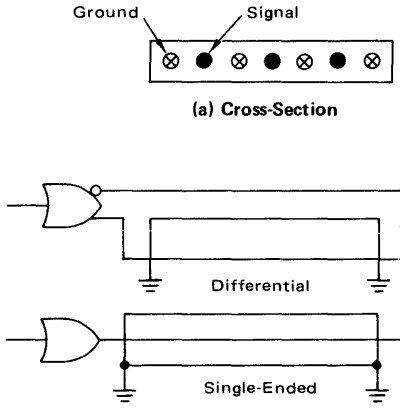
Line drivers operating differentially are not affected by the above conditions. The reduction of noise immunity to 13 mV (single-ended for MECL 10K) is seen by a line driver operated differentially, only as a small shift in the input levels – well within the acceptable limits of common mode operation. As a general rule, when operating MECL circuits at greatly differing temperatures or with differing supply voltage, or when the circuits are connected by a ground network with noise or voltage drop, the line driver should be used in the differential mode to retain maximum noise immunity.

Ribbon Cable

Ribbon cable is often used to interconnect MECL cards and panels. The advantages of ribbon cable include easy bonding to connectors because of the in-line arrangement of wires; and flexibility for use with hinged panels which swing open for servicing.

Two types of ribbon cable have been found to work well with the fast MECL circuits. One is the flat ribbon composed of several twisted pair lines. This twisted pair cable is operated differentially and should be received by one of the MECL line receivers. Single-ended operation is also possible by grounding one wire of the twisted pair. The conventional ribbon cable with side-by-side wires has a defined characteristic impedance only when every other wire is grounded as shown in Figure 4-19 (a). This cable may be driven either single-ended or differentially as shown in the examples in Figure 4-19 (b).

4-19: Ribbon Cable Interconnects



(a) Cross-Section

(b) Connections

Another type of multiconductor cable is called "triax." As its name suggests, this is a three-conductor cable with characteristics similar to coaxial cable. Triax has a flat cross section for flexibility, and may be used with all MECL families including MECL III. When using triax type cables, the manufacturer should be consulted for information about the impedance and attenuation characteristics of a specific cable type.

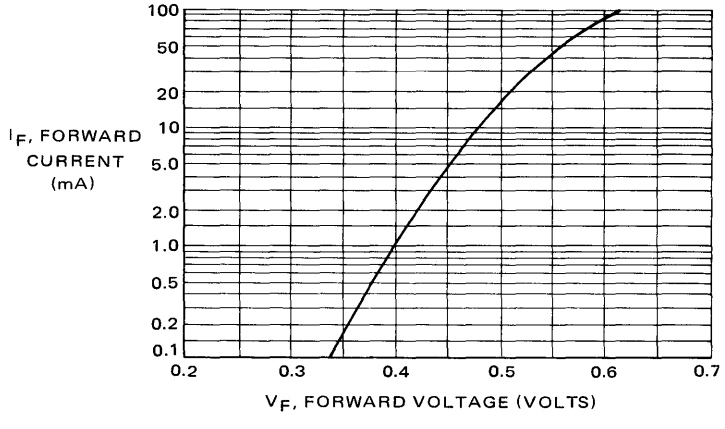
Schottky Diode Termination

Under certain board interface conditions, it may be advantageous to use a termination technique employing Schottky diodes. Several advantages are gained by the use of diode terminations:

- No matched impedance striplines are required;
- No line matching termination resistors are required;
- All signal overshoot is effectively clamped to the 1 or ∅ logic level;
- All external noise in excess of 1 or ∅ logic levels is clamped at the receiving gate or load;
- The total cost of layout, even though diodes are more expensive than resistors, may be less because no precise transmission line environment is necessary;
- If ringing is a problem on a drive line during system checkout, diode termination can be used to improve the waveform;
- Where line impedances are not well defined, as in breadboarding or prototype construction of systems using MECL, use of diode terminations is convenient and saves time.

The forward conduction characteristic of the Schottky barrier diode is used to match the line impedance of the signal path. For instance, if a 90 ohm line is used, the diode impedance equals 90 ohms at a forward voltage of 0.45 volts ($\frac{0.45\ V}{5\ mA}$ from Figure 4-20). Therefore, the line would be terminated with only a small overshoot. The variable conduction curve of the diode permits terminating line impedances from 150 Ω to 50 Ω.

4-20: Schottky Diode MBD101 Forward Transfer Characteristic



In use (cf Figure 4-21), one side of the parallel diode network is biased at the MECL threshold V_{BB} (–1.29 volts for MECL 10K/10KH and MECL III). The V_{BB} source can be either a separate supply or a gate that supplies the required sink and source current (cf

4-21: Diode Termination

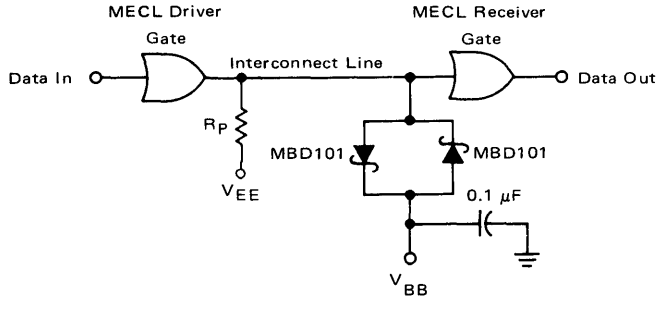


Figure 4-18). These current requirements can be determined from the graph in Figure 4-20 as follows:

$$V_{D1} \text{ (1 level diode drop)} = V_{BB} - \text{logic 1 level}$$

$$= -1.29 - (-0.90) = -0.39 \text{ V.}$$

From the graph in Figure 4-20, -0.39 V yields a diode current of approximately -1.0 mA (I_{BB1}), and:

$$V_{D\emptyset} \text{ (}\emptyset\text{ level diode drop)} = V_{BB} - \text{logic } \emptyset \text{ level}$$

$$= -1.29 - (-1.70) = 0.41 \text{ V,}$$

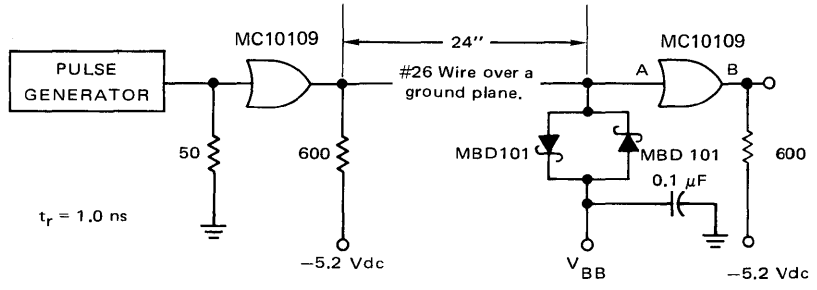
also indicating a current of 1.0 mA ($I_{BB\emptyset}$).

Thus at the receiving end of the line the power consumed would only be 0.4 mW. The driving device must have an emitter-follower pulldown resistor, R_P, to provide a current path to V_{EE} and to establish a well-defined output level.

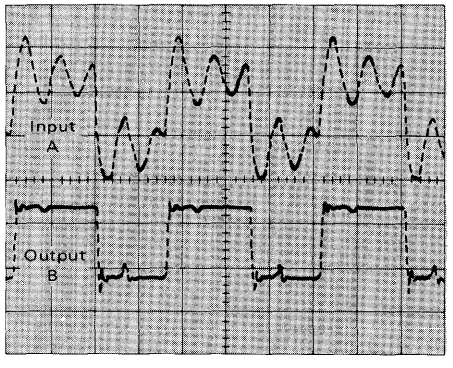
Consider a case when this resistor is 600 ohms, as for MECL 10K. The power consumed in this resistor would be about 25 mW. If the resistor were 100 ohms to a V_{TT} of -2.0 volts, then the power consumed would only be 7 mW average.

A disadvantage of the diode termination scheme is that as many as three voltages might be required: V_{EE} (−5.2 V), V_{TT} (−2.0 V), and V_{BB} (−1.3 V).

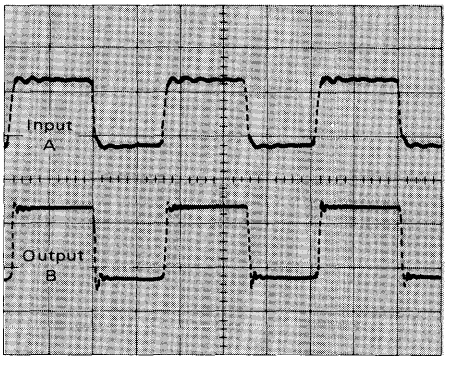
4-22: Circuit #1 — Reduction of Line Ringing by Use of Terminating Diodes



Without Diodes

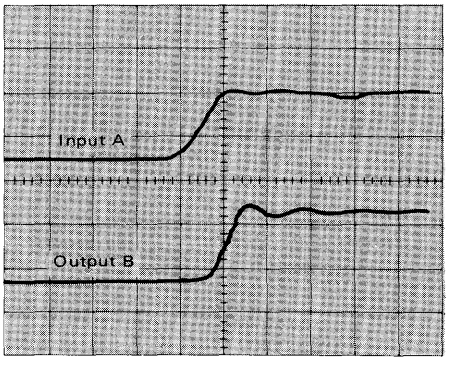


With Diodes

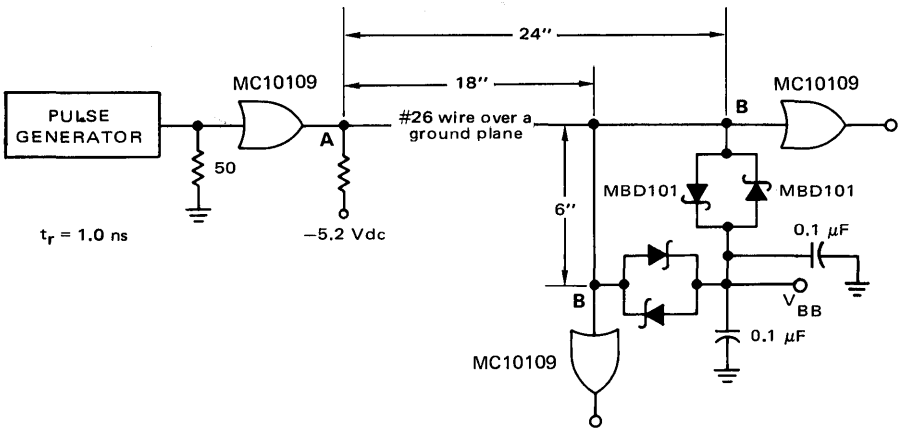


Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

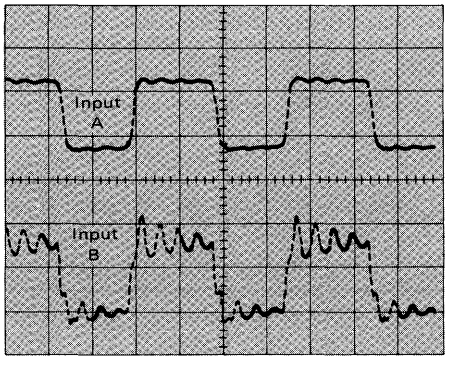
Circuit Rise Time with Diodes



4-23: Circuit #2 – Stub, off Diode Terminated Line

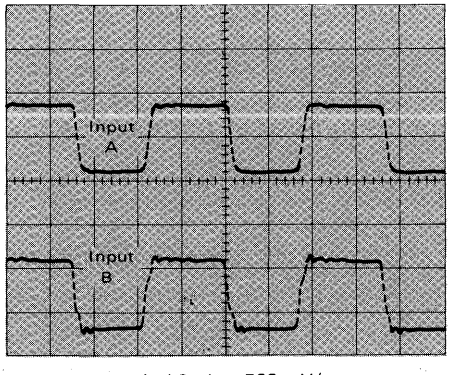


Without Diodes on Stub



Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

With Diodes on Stub



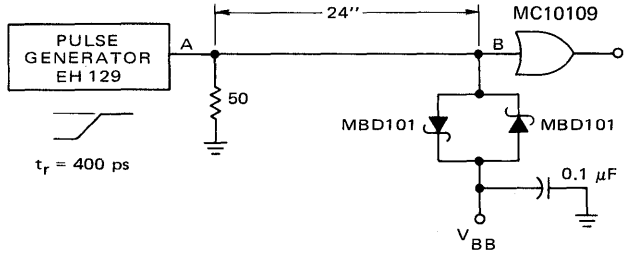
Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

Offsetting this are the elimination of the transmission line requirement, and the economical average termination power: (0.4 + 7.0) = 7.4 mW.

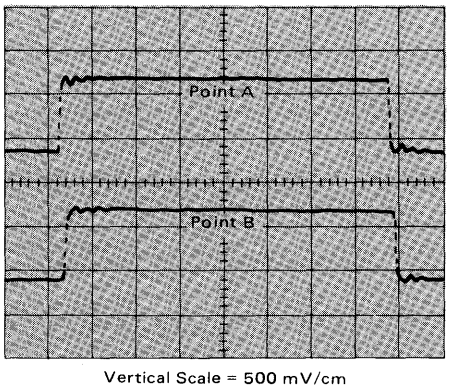
Figures 4-22 through 4-24 illustrate the performance of the Schottky diodes (MBD101) and show their unique ability to suppress severe ringing. Both circuit #1 (Figure 4-22) and circuit #2 (Figure 4-23) were evaluated with and without diode terminations. The 'scope traces show that ringing is reduced to less than 100 mV, while system rise time remains under 2.0 ns. Circuit #2 is a typical example of loads being stubbed off along a clock distribution line to provide clocking information to other parts of a system.

Even when dealing with subnanosecond risetimes (≈400 ps), Schottky diodes perform most satisfactorily – as shown by the waveforms derived from circuit #3 in Figure 4-24. The conclusion is that even for card-to-card or backplane interconnects, MECL III logic could be distributed with only a small amount of waveform degradation when diodes are used.

4-24: Circuit # 3 – Subnanosecond Performance of Diode Terminated Line

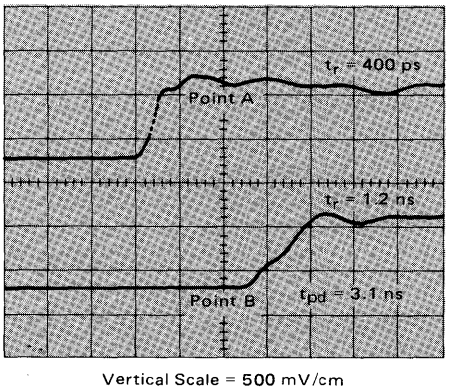


Line Input/Output Waveforms



Vertical Scale = 500 mV/cm
Horizontal Scale = 20 ns/cm

Waveform Rise Times

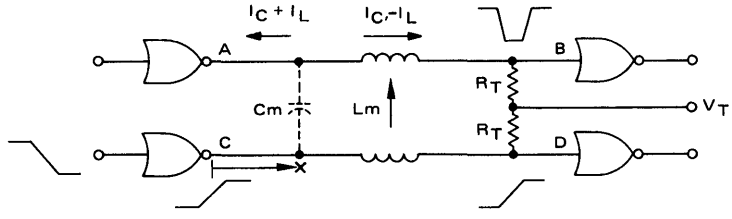


Vertical Scale = 500 mV/cm
Horizontal Scale = 1.0 ns/cm

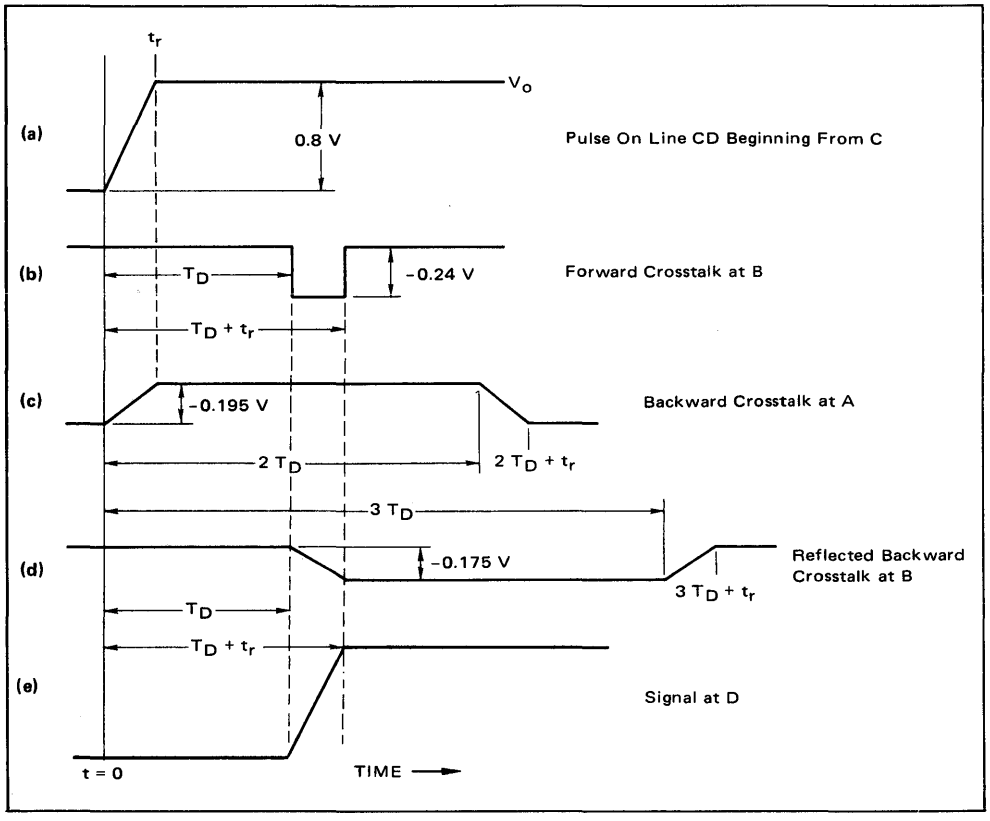
Parallel Wire Cables

Multiple conductor cables as purchased, or as constructed by lacing interconnection wires together, are not normally used with MECL because of crosstalk. Such crosstalk is due to capacitive and inductive coupling of signals among parallel lines as symbolized in Figure 4-25.

4-25: Crosstalk Coupling in Parallel Lines



4-26: Calculated Cross Talk



When a pulse propagating down line CD reaches any arbitrary point X, the signal is capacitively coupled into line AB. The coupled voltage on AB causes current (I_C) to flow from the point of coupling to both ends of the line.

Current in the direction of A is called "backward crosstalk" and that toward B is called "forward crosstalk." Coincident with capacitive coupling, the mutual inductance of the parallel lines also couples current (I_L) into line AB in the direction of backward crosstalk.

The total forward crosstalk is $I_C - I_L$ at point B. Since the parallel line coupling is primarily inductive, current flows from point B causing a negative pulse at that point (cf Figure 4-26). I_C and I_L are proportional in magnitude to the rate of change of the signal propagating from C (driving function). Coupling occurs only during the rise and fall times of the pulse as it propagates along CD.

Since the forward crosstalk propagates along AB at the same rate as the signal on CD, the result is a pulse at point B lasting for the duration of the rise time of the driving function. The amplitude of the resulting pulse is a function of the difference between inductive and capacitive coupling. Normally, the reflection of the backward crosstalk hides the small pulse at B.

Backward crosstalk current is $I_C + I_L$ and is a function of line length and velocity of propagation of the line. Backward crosstalk current starts at point A simultaneously with the signal at C. The coupling continues for the duration of the signal (T_D) on line CD; at time T_D the driving function is at point D, and also appears coupled to the other line at B. The backward crosstalk then requires another T_D to reach point A. Therefore the duration of backward crosstalk is:

$$T_B = 2\,T_D$$

The output impedance of the gate at point A (R_S) is low– typically 5 ohms compared with the line (Z_o = 75 to 150 ohms), so the backward crosstalk is reflected toward point B in proportion to the reflection coefficient.

Since the reflection coefficient for current, ρ_I, is:

$$\rho_I = \frac{Z_o - R_S}{Z_o + R_S},$$

if Z_0 = 100 ohms and R_S = 5 ohms, then:

$$\rho_I = +0.905\,.$$

The reflected backward crosstalk reaches point B at the same time the driven signal reaches point D, and is $2\,T_D$ in duration and about $0.9\,(I_C + I_L)$ in current amplitude. The positive reflection coefficient shows that the reflected current has the same polarity as the backward crosstalk. This reflection results in the pulse at point B (Figure 4-25) as shown in Figure 4-26d.

A similar analysis shows that if the gates at A and B were reversed so that the receiving gate and terminating resistor were at point A, the results would be similar. A positive crosstalk pulse would begin simultaneously with the driven signal at point C and have a duration of $2\,T_D$. The forward crosstalk would be reflected from the gate at point B and would not appear at point A until $2\,T_D$. This reflected signal is normally not seen as it occurs at the trailing edge of the backward crosstalk.

Calculating Crosstalk Amptitude

Crosstalk amplitude V (X,t) may be calculated with the following equation (cf reference 11, Chapter 7):

$$V(X,t) = K_f X \frac{d}{dt}\left[V_{in}(t - T_D\frac{X}{\ell})\right] + K_b\left[V_{in}(t - T_D\frac{X}{\ell}) - V_{in}(t - 2T_D + T_D\frac{X}{\ell})\right],$$

where:

K_f (forward crosstalk constant) $= -\frac{1}{2}\left(\frac{L_m}{Z_o} - C_m Z_o\right)$,

K_b (backward crosstalk constant) $= \frac{\ell}{4T_D}\left(\frac{L_m}{Z_o} + C_m Z_o\right)$,

L_m = mutual line inductance per unit length,
C_m = mutual line capacitance per unit length,
Z_o = characteristic line impedance,
ℓ = line length = 10 ft. for the following example,
X = arbitrary point along line,
t = arbitrary time,
T_D = total one-way line delay.

Also note that:

C_o = intrinsic line capacitance/unit length,
L_o = intrinsic line inductance/unit length.

Using the measured values $C_o \approx$ 1 pF/in, $L_o \approx$ 20 nH/in, $C_m \approx$ 0.446 pF/in, and $L_m \approx$ 10.3 nH/in for the cable under test, crosstalk can be calculated. The calculations can then be compared with test data on the cable.

First: $Z_o = \sqrt{\frac{L_o}{C_o}} = 141$ ohms,

and $t_{pd} = \sqrt{L_o C_o} = 0.14$ ns/in;

so: $T_D = 16.8$ ns.

Substituting values into the appropriate equations above gives:

$$K_f = -0.06 \text{ ns/ft},$$

and:

$$K_b = 0.244.$$

Forward Crosstalk Calculation

Proceeding now with the calculation of the forward crosstalk, V_f, in the line:

$$V_f(X,t) = K_f X \frac{d}{dt}\left[V_{in}\left(t - T_D\frac{X}{\ell}\right)\right],$$

where $V_{in}(t)$ may be represented by:

$$V_{in}(t) = \left(f_o(t) \cdot U(t)\right) - \left(f_o(t - t_r) \cdot U(t - t_r)\right).$$

Here U (t), the step function, has the values:

$$U(t) = 0, \text{ for all } t < 0,$$
$$U(t) = 1, \text{ for all } t \geqslant 0.$$

In this equation $f_o(t)$ describes the rising portion of the input pulse (Figure 4-26(a)), and since the pulse rises with a slope:

$$m \approx \frac{V_o}{t_r},$$

then the first term, $$f_o(t) = \frac{V_o}{T_r} \cdot t, \text{ for } t \geqslant 0,$$

$$= 0, \quad \text{for } t < 0.$$

The second term,

$$f_o(t - t_r) \cdot U(t - t_r) = \frac{V_o}{t_r}(t - t_r), \text{ for } t \geqslant t_r,$$

$$= 0, \text{ for } t < t_r.$$

Note that the second term of $V_{in}(t)$ is zero until $t = t_r$. The U function is being used to "turn on" the first term at $t = 0$, and bring in the second term only for $t \geqslant t_r$:

Note that after time t_r, the function $V_{in}(t)$ remains at a value V_o, for all values of t.

Substituting $V_{in}(t)$ into the equation for $V_f(X,t)$, substituting $\left(t - T_D\frac{X}{\ell}\right)$ for t in $V_{in}(t)$, and evaluating at the end of the line ($X = \ell$), gives:

$$V_f(\ell, t) = K_f \ell \left\{\frac{d}{dt}\left[f_o(t - T_D)\, U(t - T_D)\right] - \frac{d}{dt}\left[f_o(t - T_D - t_r)\, U(t - T_D - t_r)\right]\right\}$$

$$= K_f \ell \left[\frac{V_o}{t_r}\right] \cdot \left[U(t - T_D) - U\left(t - (T_D + t_r)\right)\right].$$

This gives a pulse at point B equal in duration to the driven line rise time, t_r, and starting at time T_D as shown in Figure 4-26(b). The amplitude of this pulse is, for a rise time t_r = 2 ns, at point B ($t = T_D$):

$$V_f(B) = \frac{K_f \ell V_o}{t_r} = \frac{(-0.06)(10)(0.8)}{2} = -0.24 \text{ volt.}$$

The backward crosstalk is calculated as follows:

$$V_b(X,t) = K_b \left[V_{in}\left(t - \frac{T_D X}{\ell}\right) - V_{in}\left(t - 2T_D + \frac{T_D X}{\ell}\right)\right].$$

For the same ramp function, $f_o(t) = \frac{V_o}{T_r} \cdot t$, as used with the forward crosstalk.

Taking X = 0 for point A:

$$V_b(0,t) = K_b \left[V_{in}(t) - V_{in}(t - 2T_D)\right],$$

$$V_b(t) = K_b \left(\frac{V_o}{t_r}\right)\left[tU(t) - (t - t_r)U(t - t_r) - \right.$$

$$(t - 2T_D)U(t - 2T_D) + (t - t_r - 2T_D)$$

$$\left. U(t - t_r - 2T_D)\right].$$

This gives a pulse at point A starting simultaneously with the driving signal at point C. The leading edge of the backward crosstalk pulse (Figure 4-26 (c)) is a ramp until time t_r. The pulse levels off until time 2 T_D then slopes to the starting point at time 2 T_D+ t_r. The amplitude of this pulse is:

$$V_b(A) = K_b V_o = 0.244(0.8) = 0.195 \text{ volt.}$$

These calculations assume the 10 foot line is terminated in its characteristic impedance at points D and B. However, since the gate output at point A of Figure 4-25 is a low impedance, only a small voltage pulse is seen at the MECL gate. As previously discussed, 90% of the backward crosstalk is reflected to point B. The amount of crosstalk at point B due to reflected backward crosstalk is calculated to be: (-0.9) (0.195) = -0.175 volts as shown in Figure 4-26(d).

Figure 4-27 lists measured crosstalk in a ten foot multiconductor cable for the test circuit of Figure 4-28. Using all wires in the cable for signal lines causes a prohibitive amount of crosstalk, as shown.

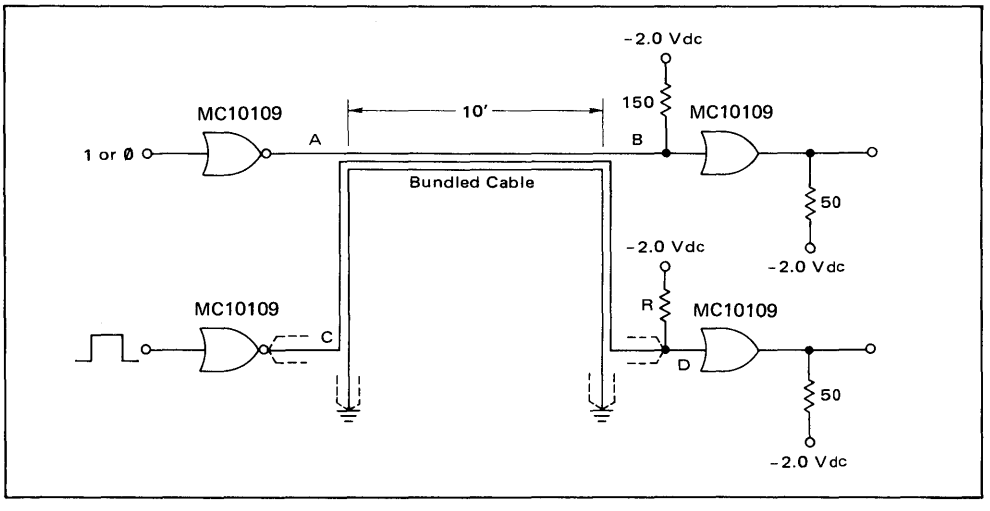
Several factors contribute to the discrepancy between calculated and measured crosstalk. The characteristic impedance of the line is comparatively undefined.

4-27: 10 Ft. Multiple Conductor Cable Crosstalk

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
① 1	240	150
2	360	75
3	420	50
1*	60	150
2**	80	75
3***	100	50

*With one wire in cable grounded at both ends
**With two wires in cable grounded at both ends
***With three wires in cable grounded at both ends
① Compare with theoretically calculated example.

4-28: Cross Talk Test Circuit



because there is not a solid ground reference for the cable. Thus, placement of the cable with respect to the system ground and other cables affects the characteristic impedance. In addition, capacitive and inductive coupling will vary along the cable due to the relative location of wires with respect to each other. The one other factor not allowed for in the calculations is attentuation in the line which damps out the higher frequency components of the signal, slowing the rise time of the signal as it propagates along the line.

The 150 ohm terminating resistor gives an approximate impedance match, to cut down overshoot and ringing. However, residual mismatch causes reflections to return along the line. Such reflections interfere with the signal by producing distortion at the receiving gate input, and so limiting high speed operation of the cable. Serious distortion occurs when the reflected signal coincides with a following signal, i.e. when the transmitted frequency equals:

$$\text{Frequency} = \frac{1}{2\,T_D}.$$

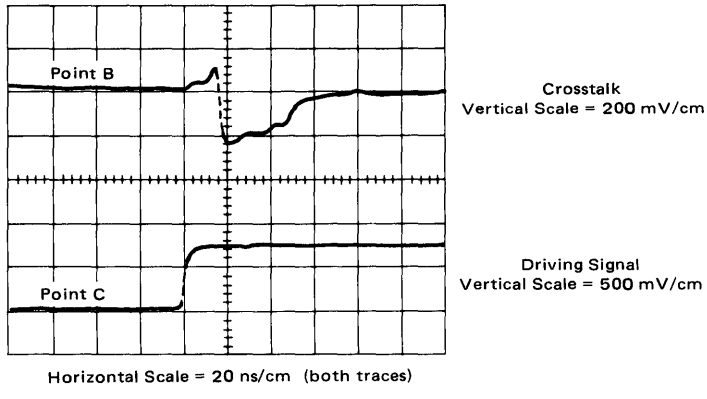
For the 10 foot line example just discussed:

$$f = \frac{1}{2\,(16.8)} = 29.8 \text{ MHz}.$$

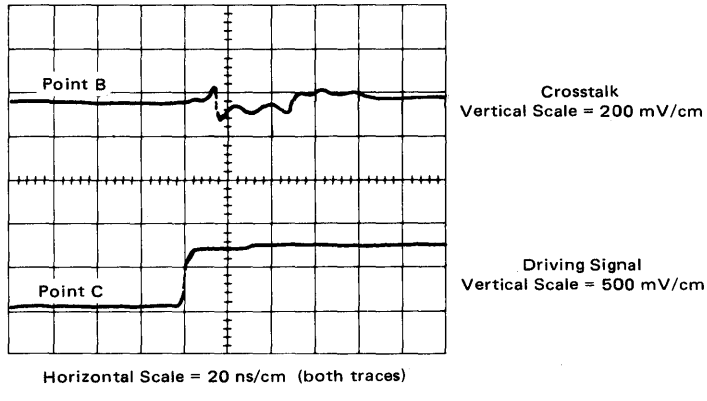
Test data coincides with the calculated performance to indicate that serious distortion occurs around 30 MHz in the 10 foot cable. The previously computed propagation speed of 1.68 ns/ft also closely agrees with the measured time of 1.65 ns/ft.

Crosstalk is reduced by supplying a ground reference in the cable. In a multiconductor cable this may be done by grounding approximately the same number of wires in the cable as there are signal lines. This measure reduces crosstalk by a factor of 4 (cf Figure 4-27). Figures 4-29 and 4-30 show the crosstalk in the circuit of Figure 4-28, and compare crosstalk of cables with and without one grounded wire in the cable.

4-29: Crosstalk in Multiconductor Cable with No Grounded Conductor



4-30: Crosstalk in Multiconductor Cable with One Grounded Conductor



The amplitude of crosstalk is independent of length for "long lines." Defining a long line as having a propagation delay greater than 1/2 the input rise time gives a "long line" length of 0.605 ft. for a 2 ns rise time waveshape:

$$\text{Long Line Length} \geq \frac{t_r}{2\,t_{pd}}$$

$$= \frac{2}{(1.65)\,(2)} = 0.605 \text{ ft. (for the cable just discussed).}$$

4-31: Test Results for an 18 Inch Multiple Conductor Cable: Crosstalk

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
1	240	150
2	350	75
3	400	50
1*	70	150
2**	80	75
3***	100	50

*With one wire in the cable grounded at both ends.
**With two wires in the cable grounded at both ends.
***With three wires in the cable grounded at both ends.

Test results (Figure 4-31) show that crosstalk for an 18 inch multiconductor cable is approximately equal to that for the 10 foot bundled cable shown in Figure 4-27. However, since reflections damp-out much faster because of the lesser propagation delay, the shorter cable is useful to 100 MHz.

Multiple conductor cables of this type (bundled) may be used successfully with MECL 10K/10KH if one-half the wires are grounded at both ends. However, the 100 mV of crosstalk present with the grounded lines significantly reduces noise immunity. The cable is also susceptible to external signals coupling to the entire cable. These cause additional noise on the line. Thus, this cable should be used only when cost or manufacturing techniques require it. Other cable types – coaxial, tri-axial, ribbon, or twisted pair – are recommended wherever possible.

Twisted Pair Cable, Driven Single-Ended

Cables formed of twisted pair lines have a more defined characteristic impedance than parallel wires. So, twisted pair can be terminated more accurately at the receiving end, reducing reflections. Further, the speed of operation of twisted pair is limited by attenuation rather than by any significant reflection interference. Test results show a 10 foot length of twisted pair cable may be used up to 70 MHz before attenuation reduces noise immunity by 100 mV. Propagation delay is the same as for parallel lines – 1.65 ns/ft.

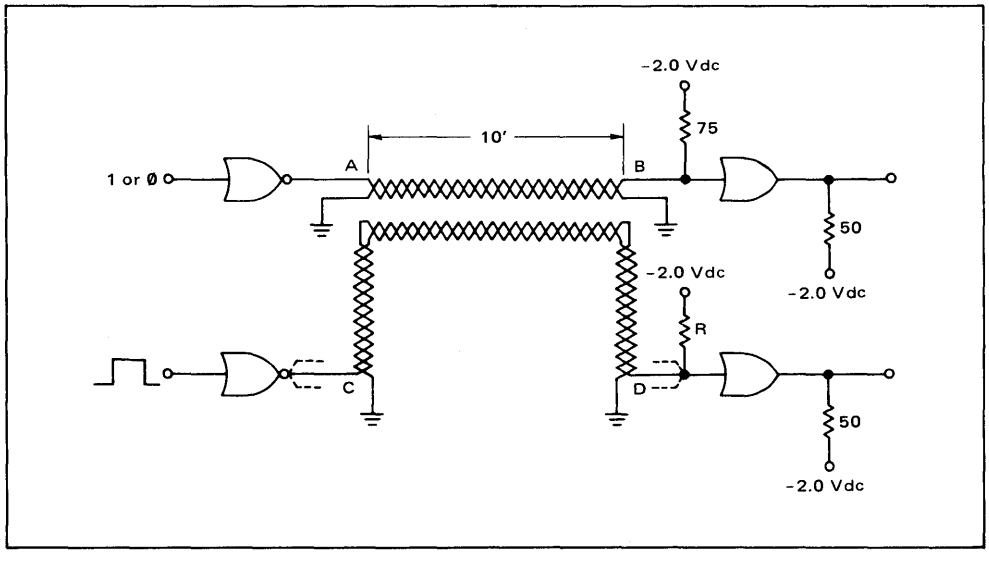
Crosstalk for the twisted pair cable is comparable to that for the parallel wire cable operated with half the leads grounded. This is because the higher switching current (due to lower Z_0 of twisted pair) offsets the better ground of the twisted pair. Crosstalk magnitude in a twisted pair cable is listed in Figure 4-32 for the test circuit of Figure 4-33. If shielded twisted pair cable is used, crosstalk is significantly reduced (compared to unshielded) as shown in Figure 4-34 and Figure 4-35. Both ends of the shield as well as the second wire of the pair were grounded in the test whose results are shown in Figure 4-34.

4-32: Crosstalk for 10 Ft Multiple Twisted Pair Cable

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
1	60	75
2	80	39
3	90	27

Differential operation of twisted pair line offers advantages over the standard multiconductor cable when sending higher frequency signals. When operated single-ended (as shown in Figure 4-33), twisted pair is still susceptible to noise external to the cable. Any noise coupled into the entire cable causes a direct reduction of noise immunity.

4-33: Twisted Pair Crosstalk Test Circuit

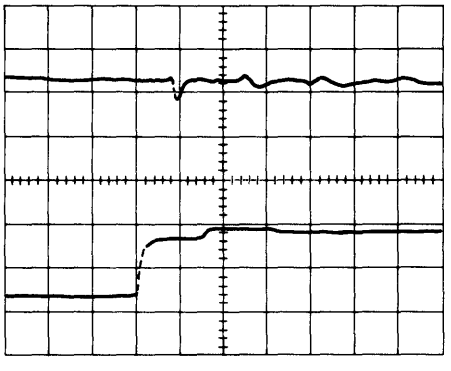


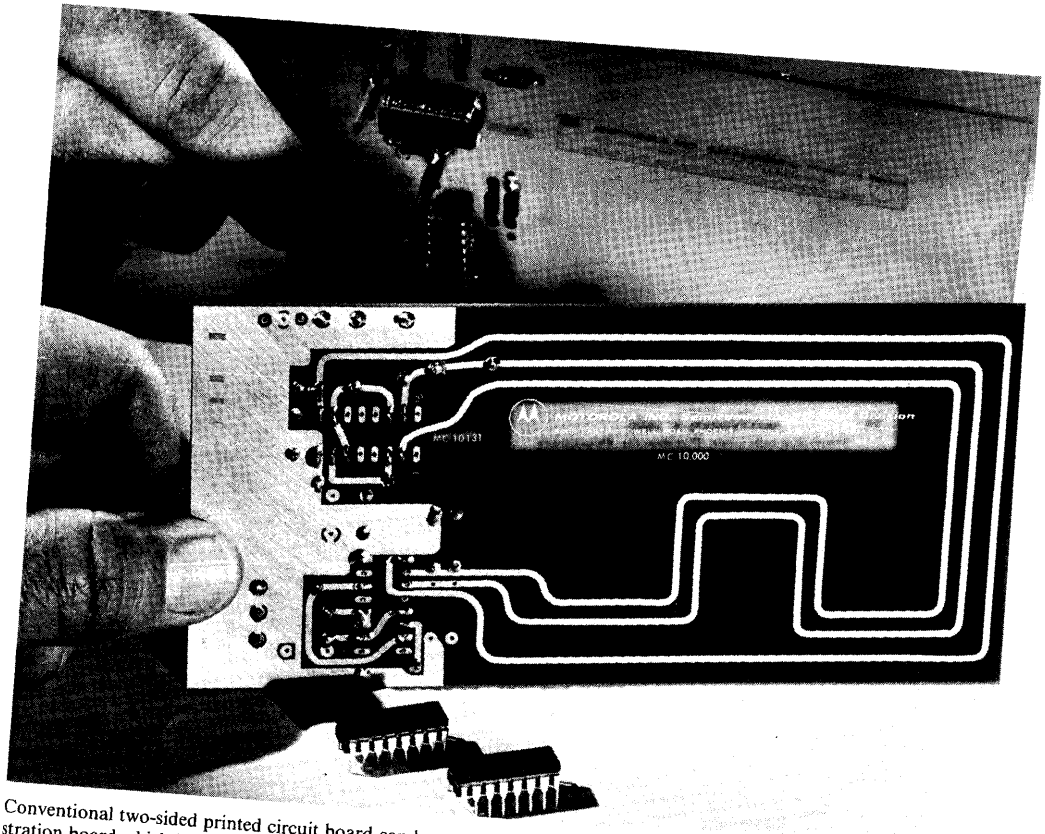
Since one-half the wires in a multiconductor cable should be grounded for low crosstalk (comparable to the twisted pair), cable density is the same for both – two wires per signal path. The use of shielded twisted pair significantly reduces crosstalk and should be used in applications where crosstalk could be a problem. Differential operation of twisted pair lines is *definitely preferred* over single-ended twisted pairs for sending MECL signals between sections of a system.

4-34: Crosstalk for 10 Ft Multiple Shielded Twisted Pair

CONDUCTORS AT C	CROSSTALK AT B (mV)	R (OHMS)
1	30	75
2	30	39
3	40	27

4-35: Crosstalk in a Multiconductor Shielded Twisted Pair Cable





Conventional two-sided printed circuit board can be used when designing with MECL 10K/10KH. Shown is a demonstration board which illustrates some of the capabilities of MECL 10K series parts.

The circuit consists of a ring oscillator and a divide by four counter, connected by a 12 inch microstrip line. Operating frequency is 83 MHz.

Together with an oscilloscope, the circuit illustrates propagation delay, edge speed, and synchronous flip-flop performance, as well as series, parallel and non-terminated line connections.

CHAPTER 5

Power Distribution

Power distribution is an important factor in system design. The loss of noise margin due to reduced power supply voltage or noise on the power supply lines means a reduction in the circuit tolerance to crosstalk and ringing as discussed in Chapters 3 and 4. Points to consider for overall system operation include total circuit and termination power, voltage drops on the power buses, and noise induced on the power distribution lines by the circuits and by external sources.

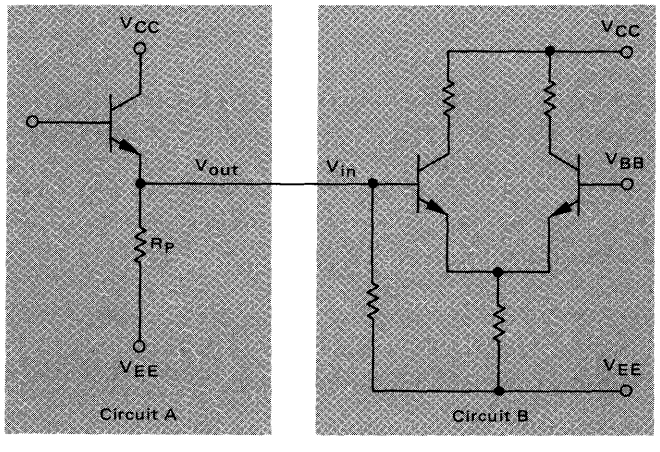
MECL circuits are designed to interface with each other over a wide power supply voltage range without loss of noise margin (other than that due to reduced signal swing at low voltage). However, if two circuits are at different supply voltages or on the same power supply with a voltage offset between circuits, there will be a predictable loss of noise margin.

Figure 5-1 illustrates supply points for two MECL circuits (A and B). The MECL circuits are most sensitive to voltage differences between V_{CC}s for the two circuits. Any voltage drop on this power bus causes a direct loss of noise immunity and should be avoided. Similarly, any noise on the V_{CC} line not common to both circuits may subtract from noise immunity. For this reason, V_{CC} is normally made to be the system ground – usually the most stable reference level in the system.

The main causes of V_{CC} offsets between circuits are:

- inadequate power buses to handle the current;
- separate supplies with common negative terminals operating at slightly different voltages (not recommended for system design);
- separate positive grounded supplies with inadequate interconnecting ground bus bars.

5-1: MECL Power Points



5-2: Changes in Output Levels and V_{BB} with V_{EE}

VOLTAGE	MECL 10KH	MECL 10K	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016	0.033
$\Delta V_{OL}/\Delta V_{EE}$	0.02	0.25	0.27
$\Delta V_{BB}/\Delta V_{EE}$	0.01	0.148	0.14

A more common problem is with circuits which have a good ground, but which operate with different V_{EE} voltages. The loss of noise margin can be calculated from the changes in V_{OH}, V_{OL}, and V_{BB} as functions of supply voltage. Figure 5-2 shows the change in these levels as a function of V_{EE} for the MECL families. The change in the logic 1 output level is very small compared to the change in logic $\emptyset$ as a function of V_{EE}. V_{BB} is designed to change at one-half the logic $\emptyset$ rate, to stay at the center of the logic swing.

The following example illustrates the loss of noise margin due to circuits operating at largely differing voltages. Worst case MECL 10K Series logic levels are used in the example.

If the driving gate is at -5.46 volts (+5% of nominal), the output levels are:

$$V_{OHA\ min} = (-0.980) - (0.016)(5.2)(0.05) = -0.984 \text{ volts},$$

$$V_{OLA\ max} = (-1.630) - (0.25)(5.2)(0.05) = -1.695 \text{ volts}.$$

If the receiving gate is at -4.94 volts (-5% of nominal), the input levels are:

$$V_{IHA\ min} = -1.105 + (0.15)(5.2)(0.05) = -1.066 \text{ volts},$$

$$V_{ILA\ max} = -1.475 + (0.15)(5.2)(0.05) = -1.436 \text{ volts}.$$

Worst case noise margin is therefore:

$$\text{Logic 1: } 1.066 - 0.984 = 0.082 \text{ volts},$$
$$\text{Logic } \emptyset\text{: } 1.695 - 1.436 = 0.259 \text{ volts}.$$

In this example, worst case noise margin in the logic 1 state was reduced from 125 mV to 82 mV by a 10% power supply difference. Although the logic $\emptyset$ noise margin here improved, it would in fact have been reduced if the receiving gate were at the +5% supply voltage. Since the example assumed worst case voltages, an additional 100 mV protection from noise could be expected in typical system use.

System Power Calculations

The total power required by MECL circuits consists of several parts: current switch, bias supply (V_{BB}), output emitter follower transistor, and terminating or pulldown resistor power. Since the output emitter follower power and resistor power are dependant on the method of termination for MECL 10K/10KH and MECL III, they are not included in the specified circuit power and must be added for total system power.

Gate power is calculated as the sum of the powers for each of the three sections illustrated for the basic MECL 10K gate (Figure 1-1a). The bias driver, which furnishes –1.29 volts to the base of Q5, dissipates about 5 mW/gate, as may be seen from the following:

$$I_{BB} = \frac{V_{EE} - V_{BB} - \text{diode drop (0.79 V)}}{R_{BQ6}} = -0.625 \text{ mA}$$

so: $P_{BB1} = I_{BB} \cdot V_{EE} = 3.24$ mW (shared by 2 gates);

and: $$I_{Q6} = \frac{V_{EE} - V_{BB}}{R_{EQ6}} = -0.64 \text{ mA},$$

$$P_{BB2} = I_{Q6} \cdot V_{EE} = 3.32 \text{ mW};$$

$$P_{TOTAL\ BIAS} = \frac{P_{BB1}}{2} + P_{BB2} = 4.94 \text{ mW},$$

per gate in a gate pair. For a single gate, the bias power is not shared, so the total power for a single gate would be 6.56 mW.

Current switch power can be calculated in a similar fashion:

$$I_{EQ5} = \frac{V_{EE} - V_{BB} - \text{diode drop (0.79 V)}}{R_E} = -3.99 \text{ mA};$$

$$P_{Q5} = I_{EQ5} \cdot V_{EE} = 20.8 \text{ mW}.$$

For one gate, the combined power dissipation would be: 20.8 mW + 6.6 mW = 27.4 mW. However, the actual power dissipation is less than this on a package basis, because the gates share a common bias driver, which is coupled through emitter followers for isolation. A quad gate, for example, has a typical per gate dissipation of 25 mW. Note that this power is constant over the full speed range of operation. Transistor base currents were omitted from the above calculations as they are beta dependent and have little effect on package power.

Typical input power may be computed when using a 50 kΩ input pulldown resistor. Input power for a logic 1 level (–0.9 volts) on the input is:

$$P_{in1} = \frac{(V_{EE} - \text{logic 1})^2}{R_P} = 0.37 \text{ mW}.$$

Input power for a logic ∅ (-1.7 volts) on the input is:

$$P_{in\emptyset} = \frac{(V_{EE} - \text{logic } \emptyset)^2}{R_P} = 0.25 \text{ mW}.$$

Totaling the input and gate power gives a typical 26.4 mW power per gate for a dual four-input gate, with two inputs high on each gate.

The total supply current for MECL 10KH was designed to be the same as MECL 10K thus producing the same power dissipation. For example the MC10H101 quad OR/NOR gate has the same current switch power dissipation of 20.8 mW per gate. Its bias driver dissipates 25 mW or 6.25 mW/gate for a total dissipation of 27.05 mW/gate.

Output power is a function of the load network. It is usually co nputed for circuits operating at a 50% duty cycle by calculating the 1 and ∅ level output powers and forming their average.

Figure 5-3 shows output transistor powers and load resistor powers for several of the popular terminations. This power must be added to gate power when determining system power. Unused outputs draw no power and may be ignored.

5-3: Typical Output Power

TERMINATING RESISTOR	P Q7 or Q8 (mW)	P RESISTOR (mW)	P TOTAL (mW)
150 ohms to -2.0 Vdc	5.0	4.3	9.3
100 ohms to -2.0 Vdc	7.5	6.5	14
75 ohms to -2.0 Vdc	10	8.7	18.7
50 ohms to -2.0 Vdc	15	13	28
2.0 k ohms to V_{EE}	2.5	7.7	10.2
1.0 k ohm to V_{EE}	4.9	15.4	20.3
680 ohms to V_{EE}	7.2	22.6	29.8
510 ohms to V_{EE}	9.7	30.2	39.9
270 ohms to V_{EE}	18.3	57.2	75.5
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140	165

Calculations for power required with an external 510 Ω output pulldown resistor are:

$$I_R \text{ (logic 1)} = \frac{V_{EE} - \text{logic 1 level}}{R_P \text{ (output)}} = -8.43 \text{ mA}.$$

So: $P_{Q7 \text{ or } Q8} = (I_R \text{ logic 1})(\text{logic 1 level}) = (-8.43)(-0.9) = 7.6 \text{ mW}$

(Q7 or Q8, depending upon which is connected to the 510 Ω output pulldown);

and: $P_{510 \text{ ohm}} = (I_R \text{ logic 1})(V_{EE} - \text{logic 1 level}) = 36.3 \text{ mW}.$

Similar calculations for a logic $\emptyset$ state give $P_{Q7 \text{ or } Q8} = 11.7$ mW and $P_{510 \text{ ohm}} = 24$ mW. Averaging $\emptyset$ and 1 level powers, gives:

$$P_{510\Omega} = 30.2 \text{ mW avg.};$$

$$P_{Q7 \text{ or } Q8} = 9.7 \text{ mW avg.}$$

Low impedance MECL III circuits require more input power because of their 2 kΩ input resistors. An average of 7.7 mW per used input must be added to the power for the rest of the circuit:

$$P_{in1} = \frac{(V_{EE} - \text{logic 1 level})^2}{R_{in}} = 9.3 \text{ mW};$$

$$P_{in\emptyset} = \frac{(V_{EE} - \text{logic } \emptyset \text{ level})^2}{R_{in}} = 6.1 \text{ mW}.$$

Power Supply Considerations

MECL 10K and MECL III are guaranteed functionally over a $\pm$ 10% power supply regulation. Circuit speeds are optimized at a V_{EE} of —5.2 V but other voltages may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. The loss of performance is negligible if supply voltage is held to a $\pm$ 5% range. MECL 10KH however, because of its internal voltage regulation is guaranteed both AC and DC over a 5% power supply regulation. Therefore, noise margins and performance specifications of MECL 10KH are unaffected by variations in V_{EE}.

MECL 10K/10KH, used without transmission lines, requires smaller switching current (less than 2.0 mA) because of output pull-down resistors (typically 510 Ω) and input current. Even so, worst case fluctuation in current requirements is less than 12 percent. In system use the fluctuation would normally be much less than 12% because of complementary outputs and the low probability of all circuits being in a logic 1 or 0 state at the same time.

Power supply requirements do become more important for MECL 10K/10KH and MECL III when they are used with transmission lines. In particular, a 50 ohm parallel terminated transmission line sinks 22 mA with a logic 1 output, and 6 mA with a logic $\emptyset$. The 16 mA differential between the two states can produce a significant power supply current fluctuation. Such an effect should be considered when specifying the power supply.

The current fluctuations are by no means insurmountable. Brief current changes are smoothed by bypass capacitors at the circuits. However longer current changes could cause noise on the supply lines unless a properly regulated supply is used. Fortunately, the presence of complementary outputs and the typical 50% distribution of output logic levels minimize current changes.

High frequency noise and ripple from the power supply should be avoided because they produce, in effect, differences in voltage levels among sections of a system, and lead to loss of noise margin. As a rule of thumb, noise can be considered "high frequency" whenever the mean wave length of the noise on the power lines is *not* several times greater than the length of the longest power line. It is recommended that for operation with MECL, high frequency supply noise be held to under 50 mV.

When multiple power supplies are used, the positive terminals should be connected together with a large bus and the output voltages maintained as equal as possible. It is desirable to keep the various supply levels within 50 mV of one another.

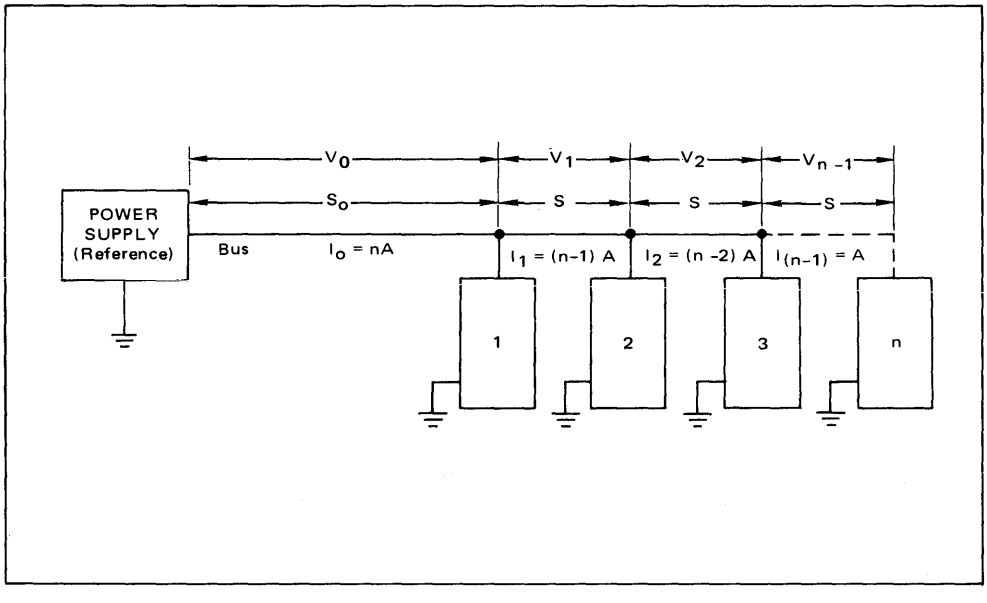
System Power Distribution

When designing the system power distribution network, primary areas of concern are:

1. Maintaining a low impedance ground – without voltage drops;
2. Limiting V_{EE} voltage drops;
3. Designing the supply lines to hinder external noise from coupling into the system.

The following method is used to calculate voltage drops along a voltage bus which has distributed loads (cf Figure 5-4).

5-4: Voltage Drops Along a Power Bus



Where:

S = average spacing of cards in inches,
r = resistance per inch of bus (ohms/in),
n = number of cards,
A = average card current load (amps),
and S_0 = distance from reference to first card (inches),

the voltage drop to the first card will be:

$$V_o = I \cdot R = (n \cdot A)(S_o \cdot r).$$

Between cards 1 and 2 the voltage drop is:

$$V_1 = (n - 1)A \cdot (S \cdot r).$$

Likewise:

$$V_2 = (n - 2)\,A \cdot (S \cdot r),$$
$$V_3 = \text{etc.}$$

So:
$$V'_n = n\,A\,S_o\,r + \sum_{1}^{n} V_n$$

$$= n\,A\,S_o\,r + A\,S\,r \sum_{1}^{n-1} n\,.$$

Example:

let $S_o = 5$ inches, $S = 1$ inch,
$r = 0.0004$ ohms/inch, $A = 500$ mA,
$n = 10$.

The voltage drop to package 10,

$$V'_{10} = 10^{-2} + 2 \times 10^{-4}\,(1 + 2 + 3 + 4 + 5 + 6 + 7 + 8 + 9)$$

$$= 19 \text{ mV}.$$

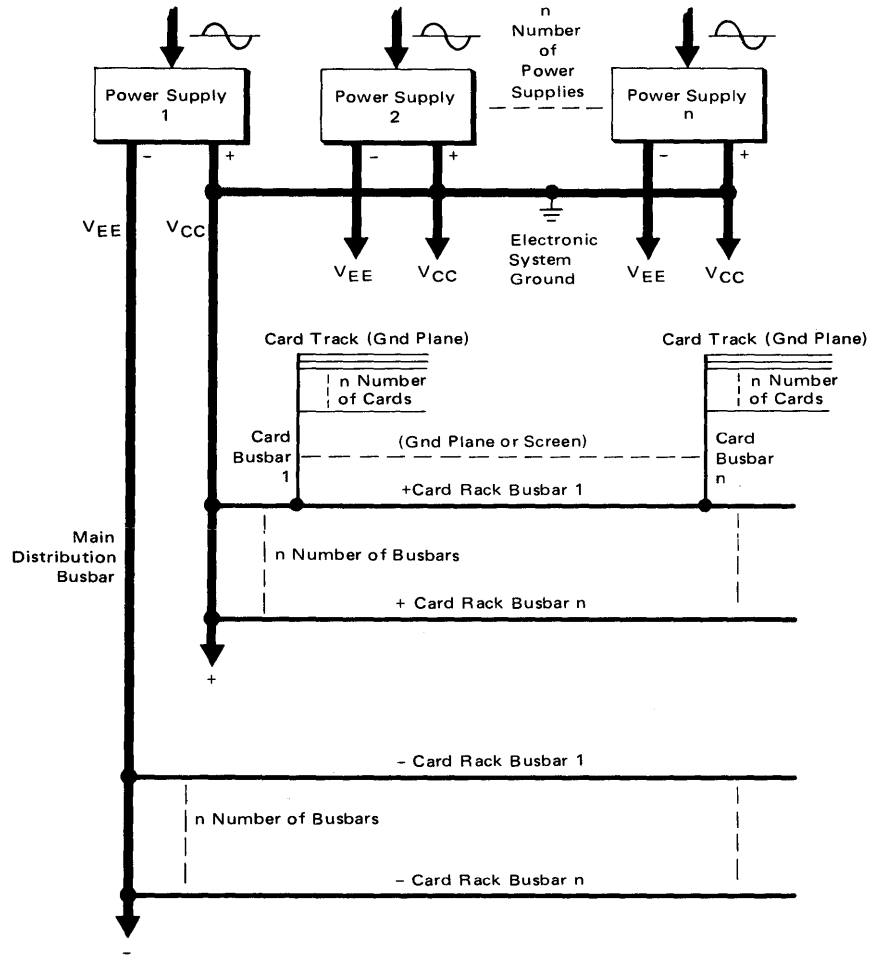
This type of calculation should be performed for all voltage distribution systems, and should also include edge connector voltage drops, etc. These calculations will indicate the results to be expected for a proposed distribution system, and the consequences of using a high resistance voltage bus are evident. The equation may be modified to accommodate other conditions – such as unequal spacing between cards or variations of loads among cards.

Laminated bus bars have advantages for power distribution to larger systems because they minimize the effects of induced noise. Noise is reduced by the high intrinsic capacitance of the laminated bus bars. Since each bus layer is separated by a dielectric, the bus bar appears overall as a very large capacitor. Bus bar design using a large width to thickness ratio ensures low self inductance. This type of power bus system is available with various options from many manufacturers.

For large systems, power distribution should avoid ground loops. Figure 5-5 shows power distribution to a typical large system. The flow of power from the supplies is via main bus bars directly to the ground plane or ground screen of individual card racks and cards. This method minimizes supply losses which would otherwise occur with power supplied through a series string of card racks.

In addition to preventing large voltage drops along the supply lines, the power distribution system must be designed to ward off external noise interference. All noisy and high power devices such as relays and motors should use a separate power supply and ground system. The ground systems are connected at the system ground point which is normally at the power supply. Relays and solenoids should be diode suppressed and motor brushes should be filtered. Other standard design practices should also be used to eliminate these sources of noise.

5-5: Power Supply System



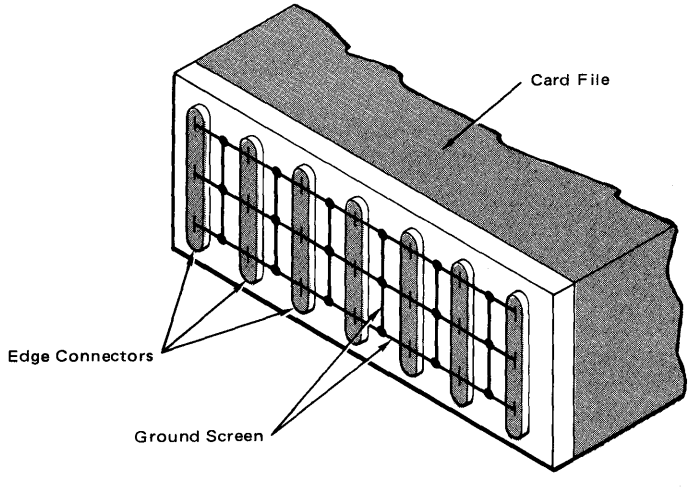
The mechanical sections of a system are commonly connected together with another ground. The frame connecting the panels to the chassis is used for this ground if good electrical conduction is made at points of mechanical contact. This hardware ground is also connected at the common ground point (cf Figure 2-10).

Backplane Power Distribution

For systems using MECL 10K/10KH circuits a common hard wired backplane is often used. The wires are either soldered or wire wrapped to connectors and are routed over a ground plane or ground screen. The ground plane is often formed by a large printed circuit board to which the connectors are mounted, or else, the ground plane is connected to the frame holding the card connectors. The metal is left on one side of the board and forms the ground plane for the backplane wiring. Alternatively, metal can be left on both sides of the board, to conduct both ground and V_{EE}. Ground plane circuit boards are commonly used over a metal ground plane as a means of isolating the MECL circuit ground system from the mechanical system component ground.

When a ground plane is not practical, a ground screen should be constructed on the backplane. A ground screen is made by connecting bus wires (wire size compatible with connector) to the edge connectors in a grid pattern prior to signal wiring, as shown in Figure 5-6. About every sixth pin on the card edge connectors is

5-6: Ground Screen Construction



used as a ground, providing connection points for the ground grid. This interconnection of ground points forms a grid network of approximately 1 inch squares over which the signal lines are wired. A characteristic impedance for a wire over ground screen of about 140 ohms can be expected, depending upon the exact routing and distance from the ground screen. The capacitance of this type line will be about 1 to 2 pF per inch, and series inductance will be about 20 nH per inch.

Point-to-point wiring is normally used instead of routing along channels, to shorten the interconnecting paths and minimize crosstalk which would occur among parallel signal paths. The system interconnecting methods of Chapter 4 are used in backplane wiring over a ground screen.

The faster edges of MECL III require a transmission line environment for connecting among circuit boards. One method is to use coaxial cable for interconnections, and matched impedance connectors on the boards. Care must be taken when stubbing off the cable using a connector "T", because of the short stub length allowed with MECL III. Normally this is avoided in favor of wiring with a single output per cable.

MECL III works very well with twisted pair lines if these lines are specified to have a constant, defined impedance. Differentially driven twisted pair lines with an MC1692 line receiver should always be used where there may be significant power supply voltage drops or noise on the ground system. The board connectors used with the twisted pair lines should be designed to minimize reflection from the interconnect point. Standard edge connectors with the terminating resistor and line receiver close to the point where the line meets the connector (within 1 inch) normally provide adequate termination points.

Although coaxial cable and twisted pair line do not require a ground plane in the backplane for impedance matching, the ground plane must be retained in both cases for a good circuit ground.

Multilayer backplane wiring (motherboard) is commonly used with MECL III. Striplines and microstrip line interconnects are designed in the circuit board, along with ground and V_{EE} voltage planes. Matched impedance connectors are available to permit interfacing between cards and the backplane motherboard without line discontinuity. This technique is normally used when a system design is sufficiently determined to minimize changes in the backplane wiring.

On - Card Power Distribution

Just as the backplane wiring, the method for distributing power on cards depends on the logic family used. Standard double sided circuit boards with a good ground may be used with MECL 10K/10KH because of relatively slow edge speeds and very low switching currents in the signal lines. A good ground is necessary to prevent voltage drops and noise from reducing circuit noise margin.

Here's an example of a circuit board which would work well with MECL 10K/10KH. The various techniques can be modified to fit specific system requirements.

The majority of interconnecting wires would be on one side of the board. A ground bus or modified ground plane with any remaining interconnections would be on the other side. The -5.2 Vdc line is not as critical as the V_{CC} line and may be routed as necessary. The ground buses would be made of wide circuit board paths on the card. The width should be kept as large as possible, with at least 0.15 inch of width for each 10 packages recommended. A modified ground plane is made by leaving the metal on one side of the board and etching only as necessary to run the interconnecting leads for devices on the other side. The layout should be planned so that such interconnecting paths will not cut off a section of the ground plane from the ground inputs or isolate a section so that it is connected only with a narrow metal strip to the rest of the ground plane.

For either method, circuit board grounding is simplified if several pins in the edge connector are used for ground. A standard 22 pin connector could have four or five evenly spaced pins on the connector allocated to ground.

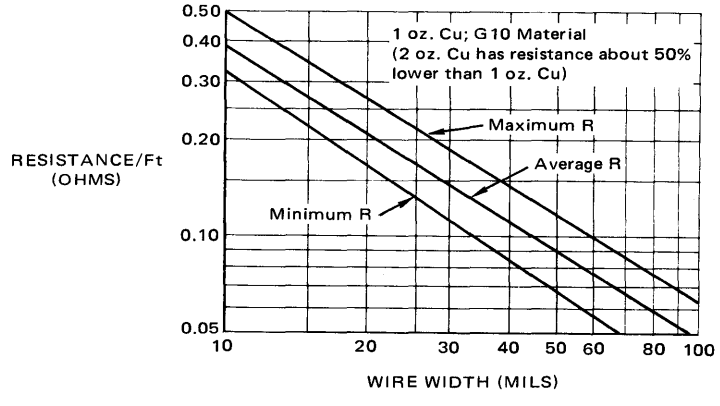
Power supply bypass capacitors are used on the circuit boards to handle the small current transients required by signal lines for charging stray capacitances. Bypass capacitors also lower the supply impedance on the card, reducing noise on the V_{EE} line. Typically a 1 to 10 μF capacitor is placed on the board at the power supply inputs, and a 0.1 to 0.01 μF RF type capacitor is connected between ground and -5.2 Vdc every four or five packages. RF type capacitors are recommended because of their low inductance. Because of their nearly constant current requirements, many MECL 10K/10KH systems are built without using bypass capacitors, and operate perfectly. However, the use of these capacitors will insure cleaner supply lines, especially at top circuit operating speeds.

MECL 10K/10KH systems use both standard double sided and multilayered circuit boards. However, when using MECL 10K/10KH, the ground plane described previously is recommended. Such a ground plane permits low impedance signal lines (over the ground plane) which may be terminated for optimum performance. Also, a ground plane gives the solid ground necessary for suppressing the current transients arising in parallel terminated lines and eliminates possible high frequency ground loops. Ideally, the ground plane would fully cover one side of the circuit board. However with MECL 10K/10KH, ground planes covering greater than 75 percent of the board surface area give good results.

The V_{CC1} and V_{CC2} pins of MECL 10K/10KH and MECL III packages should be connected directly to the ground plane as closely as possible to the package. V_{CC1} should equal V_{CC2} for best operation. If V_{CC1} drops below V_{CC2} by more than two tenths of a volt, the output devices could saturate and cause additional propagation delays.

When designing the V_{EE} line, care should be taken to prevent excessive voltage drop in the line. Figure 5-7 shows the bus resistance per foot for microstrip lines. This should be taken into consideration when designing large cards with high current requirements. Use of bypass capacitors with MECL 10K/10KH is strongly recommended to handle the current transients occurring when parallel terminated transmission lines are used. A 1.0 to 10 μF capacitor at the power supply inputs and 0.1 to 0.01 μF capacitors every four or five packages along the board give a low impedance supply.

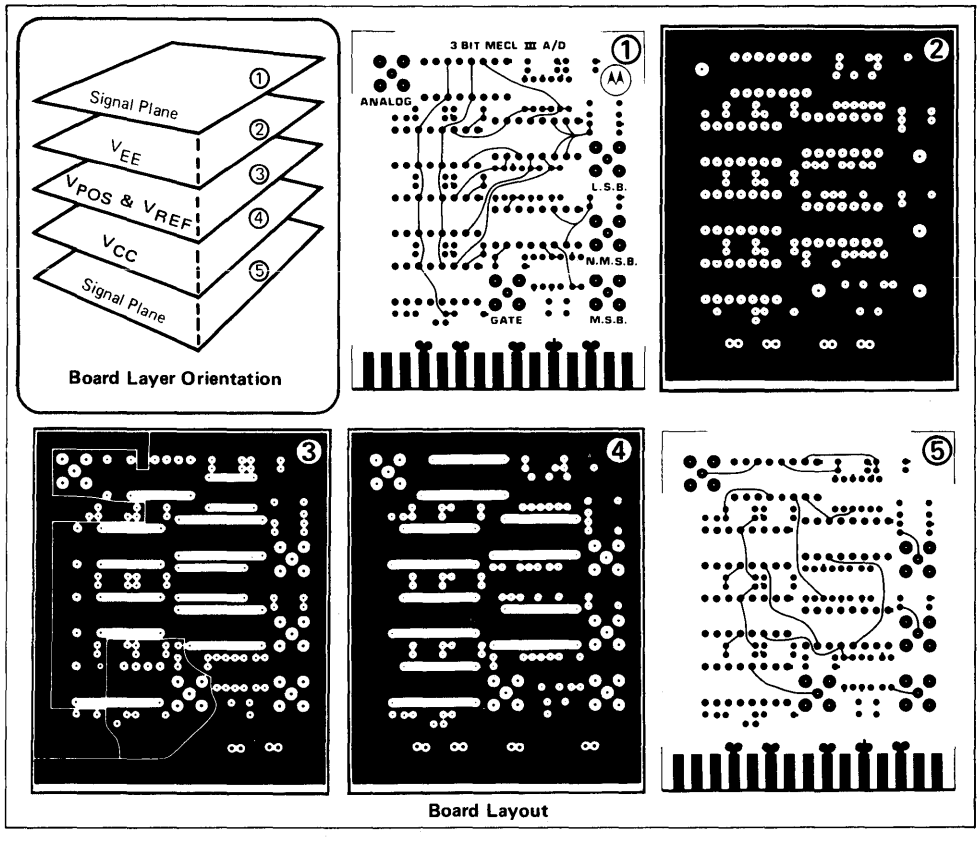
5-7: Bus. Resistance Per Foot for Microstrip Lines



Multilayer circuit boards are ordinarily used with MECL III. For small systems (with few packages) or small test circuits, a double sided board with a good ground plane may be used. With larger systems or systems operating above 200 MHz, multilayer boards are recommended for two reasons: to eliminate ground loops caused by the use of what would normally be ground plane areas as signal paths, and to provide uniform transmission line characteristics. Multilayer boards can be used for other advantages in MECL III systems – possible higher packing density and shorter interconnecting lines.

The layout of a typical small MECL III multilayer board is shown in Figure 5-8. When using multilayer boards, the correct use of ground and voltage planes leads to specific benefits and eliminates serious problems. For instance, when adjacent signal lines are switching, signal line crosstalk may occur. Crosstalk can be reduced by using a voltage plane to separate successive layers of signal lines. Ground lines, between parallel lines on a signal plane, connected to the ground plane via plated-through holes, give additional protection against noise coupling.

5-8: Typical MECL III Multilayer Board Layout



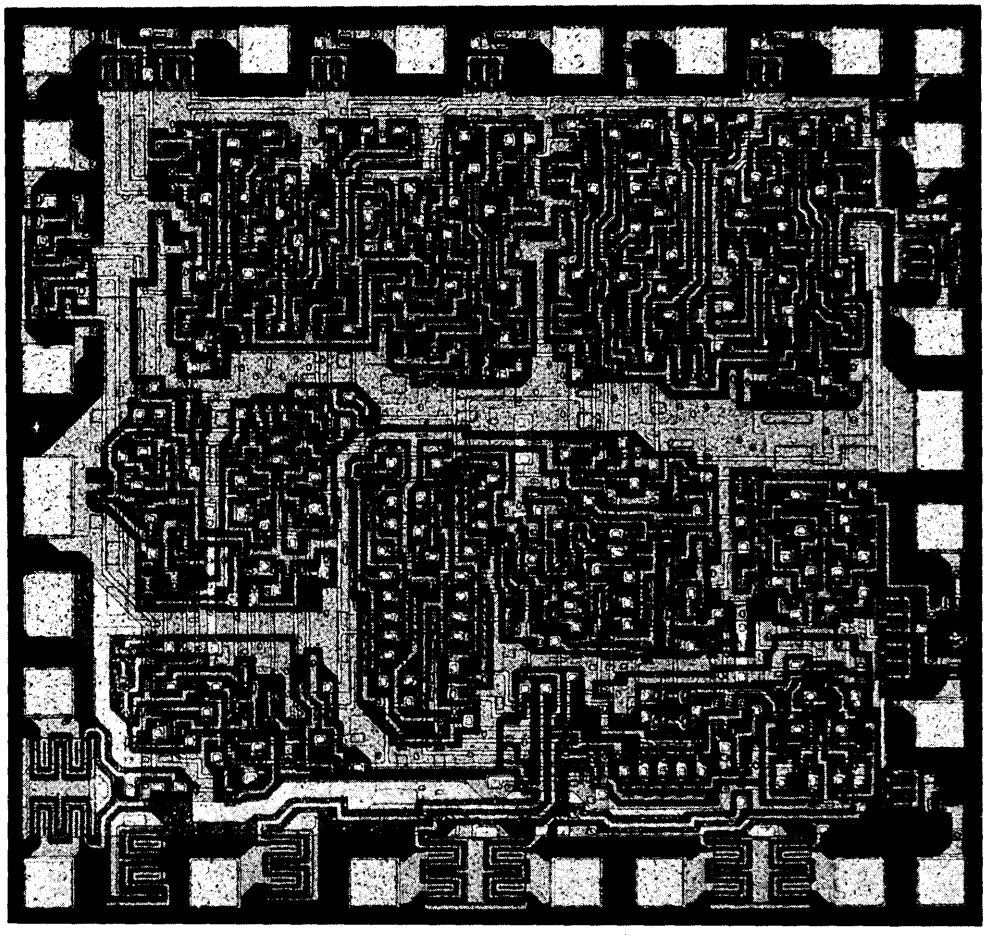
If two successive layers are used for signal interconnects, the use of an orthogonal system is suggested, i.e. interconnects running on one layer are perpendicular to those on the other. This will facilitate layout and reduce crosstalk problems. An associated ground plane can follow below to give ground reference to the two layers of signal lines. V_{EE} may be a separate plane or may be included with one of the signal planes.

The multilayer board ground planes provide a non-inductive, capacitive decoupling function. However, the thickness of the dielectric separating the voltage planes may be too great to provide sufficient inherent low frequency decoupling. In such a case, discrete capacitors are needed. These should be 0.1 to 0.01 μF in value, and are to be placed every three to five packages, to minimize voltage transients between the voltage planes (i.e. ground and V_{EE}).

V_{TT} Termination Voltage Distribution

The generation of a separate -2 Vdc termination voltage, common to all termination resistors, may be advantageous in many system designs. This is an alternate approach to the Thevenin equivalent resistor termination for each parallel termination, in which two resistors are needed.

The decision to use a separate -2 volt supply will depend on the system size. If it is feasible to provide a separate -2 volt supply, then lower termination component count per termination (one less resistor) and a power saving (up to a factor of 4) will be achieved. Since the V_{TT} supply is only used to sink current through the termination resistors, current regulation and ripple are not critical. A good rule to follow is to use the same design practices for V_{TT} as used for the negative supply, V_{EE}. However, if the system is small, cost may weigh against the use of a separate -2 volt supply. Also, the short circuit interconnects of many small systems use only a single pulldown resistor, and this reduces the need for a separate V_{TT} supply.



Complex MECL logic functions are exemplified by this microphotograph of the MC10181 Arithmetic/Logic Unit die. The array is a member of the MECL 10K logic family — whose low power gate is permitting a higher level of sophistication in the use of emitter coupled logic.

CHAPTER 6 Thermal Considerations

The electrical power dissipated in any integrated circuit forms a heat source in the package. This heat source increases the temperature of the circuit die relative to some reference point (normally 25°C ambient) in an amount which depends upon the net thermal resistance between the heat source and the reference point. Thermal resistance, θ, is the difference between the temperature of the junction and the temperature of the reference point, per unit power dissipation. Thermal resistance is the primary figure of merit for the power handling capability of any integrated circuit package. Thermal resistance from "junction to case", θ_{JC}, and/or the thermal resistance from "junction to ambient", θ_{JA}, are the thermal parameters most often specified for integrated circuit packages.

The junction temperature, T_J, for a given junction-to-ambient thermal resistance θ_{JA}, power dissipation P_D, and ambient temperature T_A, is given by:

$$T_J = P_D \theta_{JA} + T_A .$$

If a heat sink with thermal resistance θ_{SA} (sink to ambient) is used and the thermal resistance from junction to case, θ_{JC}, is given, then:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A,$$

where θ_{CS} is the thermal resistance from the integrated circuit package (case) to the heat sink. Due to the poor thermal conductivity of still air, the factor θ_{CS} may be significant if air voids exist. When using dual in-line MECL III packages that dissipate more than 750 mW, θ_{CS} should be reduced to a usable value by applying a good thermal paste between the package and the sink.

All integrated circuits, including the high speed MECL family members, have maximum allowable junction temperature limits. The MECL 10K/10KH family has T_J (max) = 165°C in ceramic and 140°C in plastic, the MECL III family has T_J(max) = 165°C in ceramic and 140°C in plastic except for the MC1666 thru MC1670 which have 145°C in ceramic. These limits are generally lower than for most other integrated circuits which may have a T_J (max) of between 175 and 200°C. With very high speed MECL circuits, stray die capacitances must be held to an absolute minimum. To do this, the on-chip interconnect metallization is made narrow. Here the current density and junction temperature become a significant concern to the integrated circuit device designer and require a lower junction temperature limit.

Thermal resistance usually is not specified for digital integrated circuits though maximum power dissipation is generally defined. The maximum ambient temperature rating has been the usual thermal limit of interest to the digital integrated circuit user. The system designer using MECL should be aware of the device junction

temperature, regardless of what his ambient temperature is. The lower the junction temperature of a device, the higher the reliability and consequently the life of the device; thus, system MTBF (mean time between failure) will be increased as junction temperatures are decreased.

MECL Integrated Circuit Heat Transfer

The electrical power dissipated in an integrated circuit is the heat source for thermal purposes. That is, the heat flow in watts equals the power dissipation in watts. The power-dissipating circuit elements are within a very narrow region on the top of the die (diffusion depths for MECL are shallow). The top of the die remains isothermal within a few degrees for MECL power dissipation levels.

The major means of heat transfer from the top of the die to the outside surfaces of the package is by conduction through solids. Heat transfer through bonding wires from the die to the lead frame is negligible.

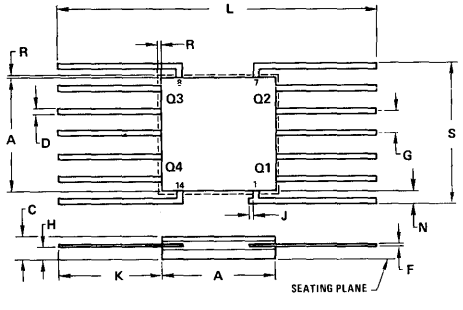
Once heat is transmitted to the package, its transfer to ambient depends upon the package mounting technique and its environment. If the integrated circuit package is installed in, or attached to a heat sink, then heat is transferred mainly by conduction to the heat sink, and then by convection and radiation from the heat sink to ambient.

In the 16-pin dual in-line ceramic package (see figure 6-1b), used for MECL 10K/10KH and MECL III, the heat flows from the top of the die, through the chip and

6-1: MECL Package Dimensions

MECL III integrated circuits are available in the 16-lead ceramic flat package, Case 607 (suffix F), and in the 16-lead dual in-line ceramic package, Case 620 (suffix L).

(a) **F SUFFIX**
CERAMIC PACKAGE
CASE 607-04

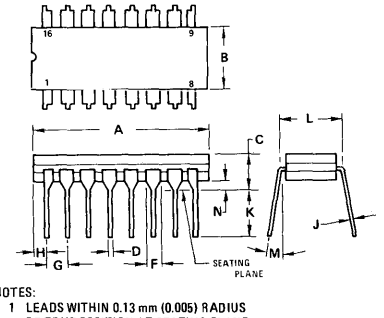


NOTE:
1. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.080
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

STYLE 1:
PIN
Q1: 1. COLLECTOR, 2. BASE, 3. EMITTER, 4. NOT CONNECTED
Q2: 5. EMITTER, 6. BASE, 7. COLLECTOR
Q3: 8. COLLECTOR, 9. BASE, 10. EMITTER, 11. NOT CONNECTED
Q4: 12. EMITTER, 13. BASE, 14. COLLECTOR

(b) **L SUFFIX**
CERAMIC PACKAGE
CASE 620-02



NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

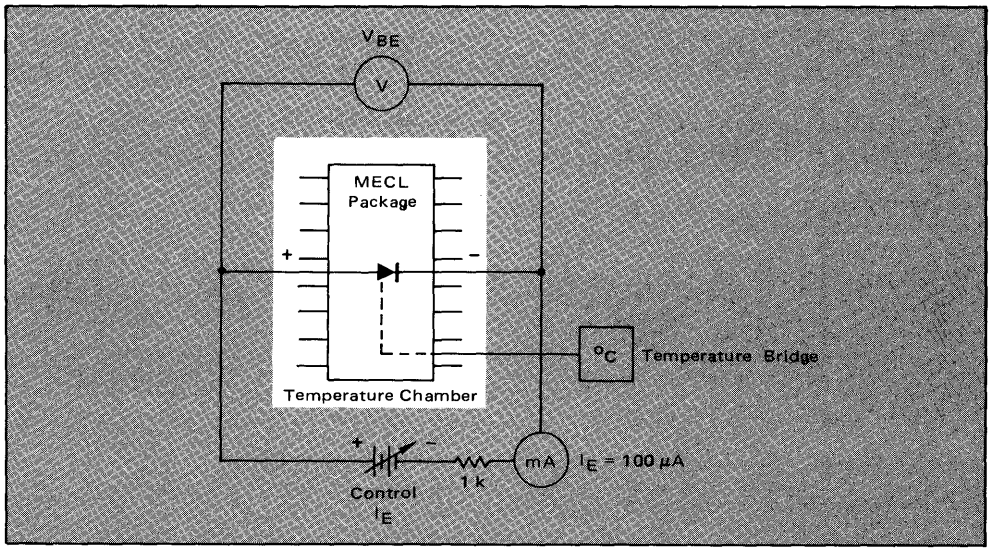
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

gold eutectic die bond, to the ceramic base. The optimum heat sink location would be in contact with the bottom of the package. Due to the poor thermal conductivity of glass, only a limited amount of heat is transferred from the ceramic base out through the lead frame.

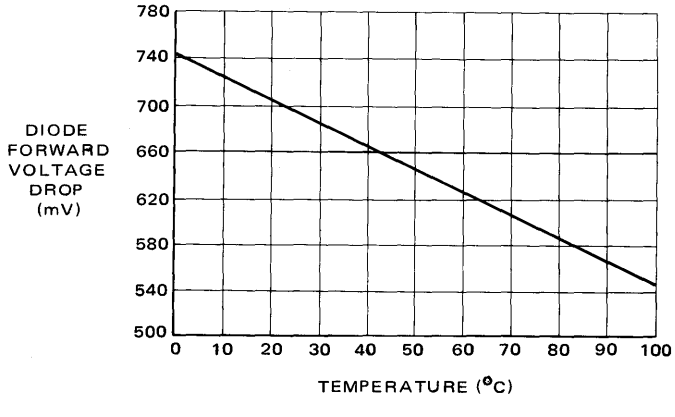
The difference between the temperature of the die and some reference point per unit power dissipation, yields the thermal resistance. The method used to measure the temperature of MECL devices is "internal temperature sensing" – by a special MECL integrated circuit. It employs an independent diode diffused on the chip. It is an easy method to use and calibrate, and has a voltage output that is very nearly a linear function of temperature.

The sensing diode within the MECL package is calibrated as a function of temperature by using the circuit shown in Figure 6-2. The forward V_{BE} drop of the

6-2: Diode Calibration Circuit

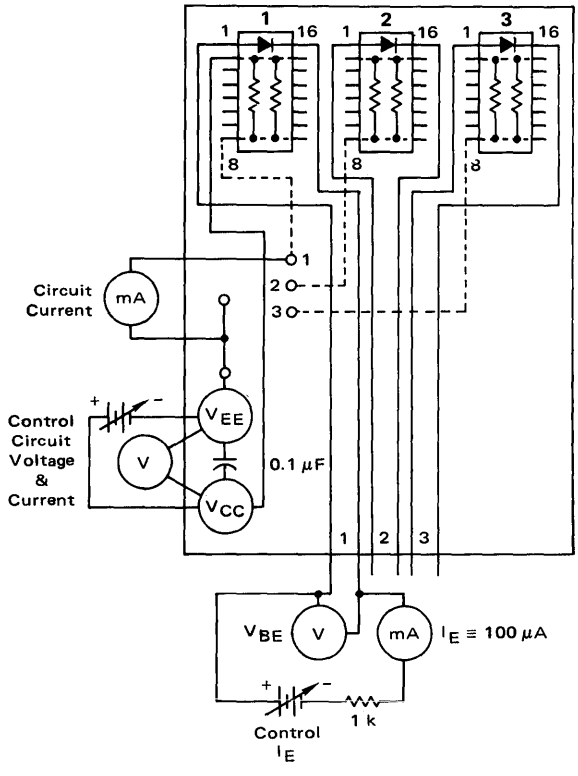


6-3: Typical Thermal Diode Calibration Curve



diode is recorded at stabilized oven temperatures between 0° and 100°C with the diode current held constant at 100 μA. A calibration curve is plotted as shown in Figure 6-3. This curve, along with the data recorded in the test setup of Figure 6-4,

6-4: Thermal Evaluation Test Circuit for 16-Pin Dual In-Line Ceramic Package



will produce data to plot T_J (°C), junction temperature, versus true power (watts). The slope of the curve is the thermal resistance, θ_J (°C/Watt), of the MECL case.

By recording the ambient temperature (T_A in °C) during the test, the thermal resistance from junction to ambient (θ_{JA} in °C/W) may be calculated as:

$$\theta_{JA} = T_{JA}/P_D \text{ (°C/W)},$$

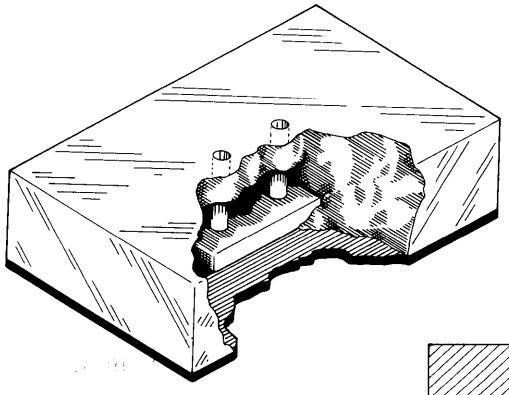
where:

$$T_{JA} = T_J - T_A \text{ (°C)}.$$

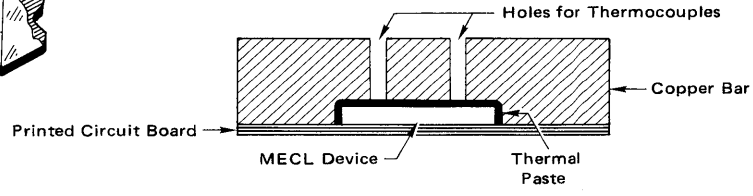
To obtain the thermal resistance from junction to case (θ_{JC}), an infinite heat sink must be provided. This can be approximated by using a copper bar 3-3/4" X

1-1/2" X 1/2" laid in thermal contact with the dual in-line 16-pin ceramic package. Copper-constantin thermocouples should be placed in holes in the sink next to the surface of the package. These thermocouples are used to measure the case temperature. Figure 6-5 shows a sample set-up for an infinite heat sink.

The thermal characteristics are listed in Figure 6-6. This information is based on package characteristics included in the figure.



6-5: Sample Infinite Heat Sink



6-6: Typical Thermal Characteristics for MECL Packages

THERMAL RESISTANCE VALUES FOR STANDARD MECL IC CERAMIC PACKAGES

THERMAL RESISTANCE IN STILL AIR										
Package Description							ϕ_{JA}		ϕ_{JC}	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	(°C/Watt) Avg.	Max	(°C/Watt) Avg.	Max
8	DIL	Epoxy	1/4" × 3/8"	Epoxy	2496	8100	102	133	50	80
8	DIL	Alumina	1/4" × 3/8"	Gold	2496	N/A	140	182	35	56
14	Flat	Alumina	1/4" × 1/4"	Gold	4096	N/A	165	215	28	45
14	DIL	Epoxy	1/4" × 3/4"	Epoxy	4096	6400	84	109	38	61
14	DIL	Alumina	1/4" × 3/4"	Gold	4096	N/A	100	130	25	40
16	Flat	Beo	1/4" × 3/8"	Gold	4096	N/A	88	114	13	21
16	Flat	Alumina	1/4" × 3/8"	Gold	4096	N/A	140	182	24	38
16	DIL	Epoxy	1/4" × 3/4"	Epoxy	4096	12100	70	91	34	54
16	DIL	Alumina	1/4" × 3/4"	Gold	4096	N/A	100	130	25	40
24	Flat	Beo	3/8" × 5/8"	Gold	8192	N/A	40	52	6	10
24	Flat	Alumina	3/8" × 5/8"	Gold	8192	N/A	64	83	11	18
24	DIL	Epoxy	1/2" × 1 1/4"	Epoxy	8192	22500	67	87	31	50
24	DIL	Alumina	1/2" × 1 1/4"	Gold	8192	N/A	50	65	10	16

NOTES:

(1) All plastic packages use copper lead frames — ceramic packages use alloy 42 frames

(2) Body style DIL is "Dual-In-Line"

(3) Beo body material is only used for military temperature range products

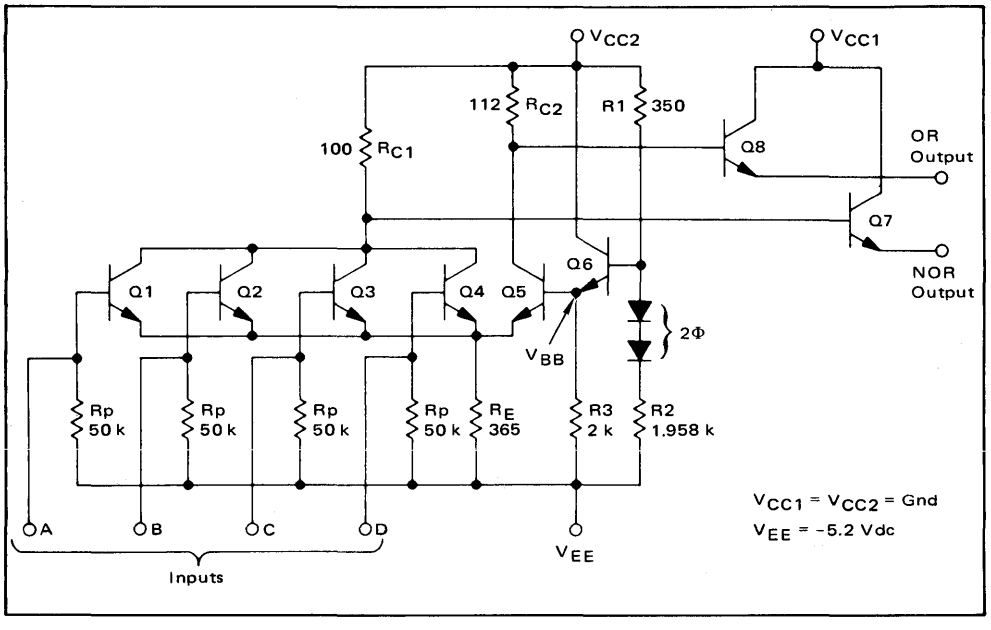
(4) Standard mounting methods:
a) Dual-in-Line in Socket or P/C board with no contact between bottom of pkg and socket or P/C board
b) Flat pack — Bottom of package in direct contact with non-metalized area of P/C board.

MECL DC Thermal Characteristics

To fully understand the thermal effects on the characteristics of MECL circuits, an explanation of the output level tracking and reference (V_{BB}) tracking will be presented. Some of the thermal equations offered are used mainly by a MECL integrated circuit designer, but are presented here to illustrate what parameters are changing and how they change as a function of temperature. Figure 6-7 shows the MECL III gate used for equation derivation. For all calculations, an ambient reference temperature of 25° C was chosen. The MECL circuit has the following basic parameters which influence dc performance: V_{BE}, beta, and resistor variations with temperature.

The threshold voltage level (V_{BB}) is most important and so an expression for V_{BB} as a function of V_{BE}, beta, and resistor values in the bias supply is derived first. Then, to analyze the temperature dependence of V_{BB}, a total derivative with respect to temperature is found in terms of dV_{BE}/dT, $d\beta/dT$, dR_1/dT, dR_2/dT, and dR_3/dT.

6-7: Basic High Input Impedance MECL III Gate



If loop equations are written for the bias supply, the expression obtained for V_{BB} is:

$$V_{BB} = \frac{R_1R_3\beta\,(V_{EE} - V_{BE} + 2\Phi) + R_1R_3\,(V_{EE} - V_{BE} + 2\Phi) - \beta\,(R_1R_3 + R_2R_3) +}{R_2R_3\beta V_{BE} - R_2R_3V_{BE} + R_1R_2V_{EE}} \quad (1)$$
$$R_1R_2 + R_2R_3 + R_1R_3$$

Differentiating with respect to temperature, T:

$$\frac{dV_{BB}}{dT} = \frac{\partial V_{BB}}{\partial R_1}\frac{dR_1}{dT} + \frac{\partial V_{BB}}{\partial R_2}\frac{dR_2}{dT} + \frac{\partial V_{BB}}{\partial V_{BE}}\frac{dV_{BE}}{dT} + \frac{\partial V_{BB}}{\partial R_3}\frac{dR_3}{dT} + \frac{\partial V_{BB}}{\partial \beta}\frac{d\beta}{dT} \tag{2}$$

Solving equation (1) for V_{BB} at 25°C using the parameters,

$R_1 = 0.35\ k\Omega$ $\quad V_{EE} = -5.2$ volts

$R_2 = 1.958\ k\Omega$ $\quad \beta = 100$

$R_3 = 3.0\ k\Omega$ $\quad V_{BE} = 0.745$ volts

$\Phi = 0.80$ volts (junction drop)

we obtain:

$$V_{BB} = -1.29 \text{ volts.} \tag{3}$$

The partial differential equations for reducing equation (2) will not be solved here due to their length. However a solution of (2) will show that the change of V_{BB} with temperature is:

$$dV_{BB}/dT = +1.11\ mV/°C\ . \tag{4}$$

This threshold tracking level will always insure that V_{BB} is centered between the V_{OH} and V_{OL} output logic levels. As a result, noise immunity can be guaranteed across the full operating temperature range.

Temperature variations in the two logic levels can be derived from the basic equations for the MECL gate. The logic 1 level equation is simply a relation of V_{OH} to the emitter-follower base-emitter voltage drop (V_{BE}) plus some further dependence upon emitter-follower base current through the current-switch collector resistor. It can be shown that the contribution by changes in β_{EF} and R_C to the 1 logic level output is about 100 μV/°C. These changes subtract from the nominal dV_{BE}/dT of -1.5 mV/°C.

The basic equation for the 1 logic level is:

$$V_{OH} = -V_{BE} - I_C R_C\ . \tag{5}$$

Differentiating with respect to temperature and inserting the values discussed:

$$\frac{dV_{OH}}{dT} = (-1)(-1.5\ mV/°C) - 0.1\ mV/°C \tag{6}$$

$$\frac{dV_{OH}}{dT} = +1.5\ mV/°C - 0.1\ mV/°C = +1.4\ mV/°C\ . \tag{7}$$

∅ Level Dependence on Temperature

The logic ∅ level can be calculated by developing the following equation from Figure 6-7:

$$V_{OL\,(OR)} = -\left[\frac{-\left(\frac{-V_{EE} - 2\Phi}{R_1 + R_2}\right)R_1 - V_{BE1} - V_{BE2} - V_{EE}}{R_E}\right] R_{C2} - V_{BE3}, \tag{8}$$

where:

$V_{EE} = -5.2$ volts,

$V_{BE1} = 0.745$ volts (bias driver transistor),

$V_{BE2} = 0.870$ volts (current switch transistor),

$V_{BE3} = 0.810$ volts (emitter-follower transistor),

$\Phi = 0.800$ volts (bias driver diode drop).

Substituting values yields:

$$V_{OL\,(OR)} = -1.745 \text{ volts.} \tag{9}$$

The logic zero level change with temperature can now be calculated from:

$$\frac{dV_{OL\,(OR)}}{dT} = \left\{\left[\frac{\left(2 - \frac{2R_1}{R_1 + R_2}\right)}{R_E}\right] R_{C2} - 1\right\} \frac{dV_{BE}}{dT}. \tag{10}$$

So,

$$\frac{dV_{OL\,(OR)}}{dT} = (0.514)(-1.5 \text{ mV/°C}) = 0.771 \text{ mV/°C}.$$

In normal operating temperature environments, the bias voltage shifts in such a way that it always remains halfway between the logic levels. Figure 6-9 shows the logic levels as a function of temperature for the MECL III gate.

The effects of temperature on MECL can be illustrated by a specific example. Assume that within a panel, one card is operating near the inlet airflow duct at 25°C, and another interconnected card (remote from the air inlet) is at 35°C. Thus a 10°C thermal differential exists within the system. The 25°C device has a typical V_{OH} of -0.900 volts and a V_{OL} of -1.700 volts. The 35°C device will have the following typical levels:

$$V_{OH}\,(35°C) = V_{OH}\,(25\,°C) + \frac{dV_{OH}}{dT}\,(\Delta T)$$

$$V_{OH}\,(35°C) = (-900\text{ mV}) + (1.4\text{ mV/°C})\,(10°C) = -0.886\text{ volts.}$$

$$V_{OL}\,(35°C) = V_{OL}\,(25\,°C) + \frac{dV_{OL}}{dT}\,(\Delta T)$$

$$V_{OL}\,(35°C) = (-1{,}700\text{ mV}) + (0.77\text{ mV/°C})\,(10°C) = -1.692\text{ volts.}$$

This shows that a shift of only 14 mV took place in the logic 1 level and about 8 mV in the logic 0 level. The overall loss in noise immunity (N.I.) would be even smaller than these figures – due to the positive threshold-shift. It is recommended that thermal gradients be limited to on-card differentials under 25°C. If differentials on a card get as great or greater than 25°C, then good thermal management has not been employed. However when a differential of 35°C or greater exists between panels or cabinets, another feature of MECL logic can be used to advantage: namely, the availability of complementary output devices and line receivers allows a differential mode of line driving and receiving which eliminates the loss of noise immunity between units that have large temperature differences. The differential transmission of signals on twisted pair is covered in detail in Chapter 4.

The change in threshold and output levels with respect to temperature for MECL 10K and MECL 10KH are shown in fig. 6-8.

6-8: Change in Levels due to Temperature

		Min	Typ	Max
$\Delta V_{OH}/\Delta T$ (mV/°C)	10KH	1.2	1.3	1.5
	10K	1.2	1.3	1.5
$\Delta V_{BB}/\Delta T$ (mV/°C)	10KH	0.8	1.0	1.2
	10K	0.8	1.0	1.2
$\Delta V_{OL}/\Delta T$ (mV/°C)	10KH	0	0.4	0.6
	10K	0.35	0.5	0.75
		0.75	1.0	1.55

The measure of safety, noise margin (N.M.), is defined as the worst case input threshold voltage (V_{IHA} (min) or V_{ILA} (max) for which the output is still within specified limits ($>V_{OLA}$ or $>V_{OHA}$), as was indicated in Chapter 1.

That is for MECL 10K and MECL III:

$$\text{N.M. (logic } \phi \text{ level)} = V_{ILA}\,(\text{max}) - V_{OLA}(\text{max})$$

$$\text{N.M. (logic 1 level)} = V_{OHA}\,(\text{min}) - V_{IHA}\,(\text{min.})$$

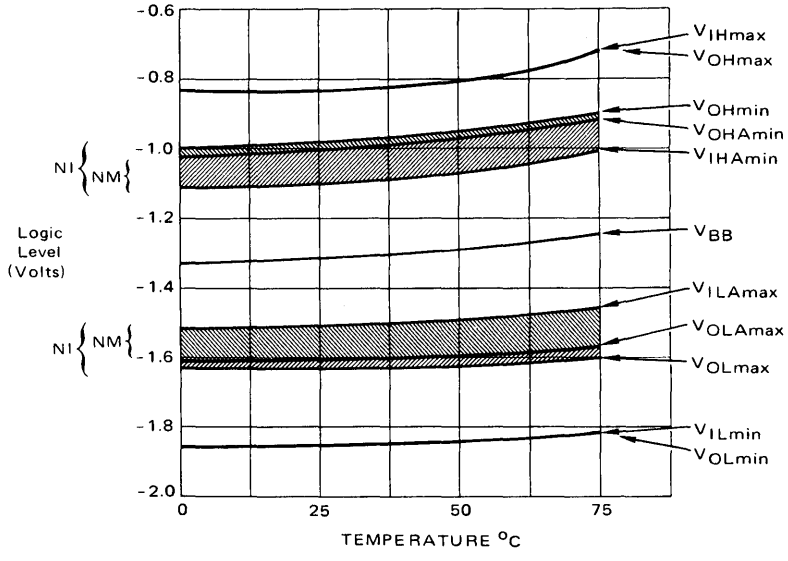
For MECL 10KH:

$$\text{N.M. (logic } \phi \text{ level)} = V_{IL}\,(\text{max}) - V_{OL}(\text{max})$$

$$\text{N.M. (logic 1 level)} = V_{OH}\,(\text{min}) - V_{IH}\,(\text{min.})$$

As can be seen from the data in Figure 6-10, a worst case noise margin of 115 mV is guaranteed for the dual in-line and flat ceramic package (both between -30 and 85° C with packages at the same ambient temperature, T_A). For MECL 10K, worst case noise margin is 125 mV and for MECL 10KH, worst case noise margin is 150 mV.

6-9: MECL III Logic levels versus Temperature



6-10: MECL III DC Test Parameters

Forcing Function	Parameter	-30°C	25°C	85°C	Unit
V_{IHmax} =	V_{OHmax}	-0.875	-0.810	-0.700	Vdc
	V_{OHmin}	-1.045	-0.960	-0.890	
	V_{OHAmin}	-1.065	-0.980	-0.910	Vdc
V_{IHAmin}		-1.180	-1.095	-1.025	
V_{ILAmax}		-1.515	-1.485	-1.440	Vdc
	V_{OLAmax}	-1.630	-1.600	-1.555	
	V_{OLmax}	-1.650	-1.620	-1.575	Vdc
V_{ILmin} =	V_{OLmin}	-1.890	-1.850	-1.830	
V_{ILmin}	I_{INLmin}	0.5	0.5	0.3	μA

NOTE: All outputs loaded 50 Ω to -2.0 Vdc except MC1648 which has an internal output pulldown resistor.

ELECTRICAL CHARACTERISTICS

Each MECL III series device has been designed to meet the dc specification shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = -5.2 V ± 0.10 V.

When calculating system noise immunity three factors must be taken into consideration. These are: loss of immunity due to temperature differentials (as above); power supply line losses, and power supply regulation (as shown in Chapter 5); and signal losses due to undershoot and ringing on signal lines (as described in Chapters 3 and 4). Proper attention must be given both to power distribution and to thermal factors for any system. The reason is that losses derived from these two areas directly subtract from the circuit's ability to withstand external noise, and to function properly despite signal deterioration due to mismatched lines.

Heat Dissipation Techniques

The majority of MECL users provide some form of air flow cooling in medium

and large size systems. For this reason MECL 10K/10KH and MECL III output levels are specified with air flow at 500 linear feet per minute (or greater) across the package. Many small systems and test circuits do not use forced air flow, but do use convective cooling with ambient temperature air, or some form of heat conduction – to avoid large thermal gradients.

As air passes over devices on a printed circuit board, it absorbs heat from each package. Thus the ambient temperature of the air will increase as it flows from inlet to outlet. The heat gradient from the first package to the last package is a function of the package density, air flow rate, and the individual package dissipations. The table in Figure 6-11 lists this gradient at various power levels for an air flow rate of 500 LFPM. These figures show the increase in junction temperature for each of the 16-pin DIPs as the inlet air passes over each device. Although Z-axis air flow information is given, the figures are similar for air flow 90° from this axis, in the plane of the PC board.

16-PIN DIP POWER DISSIPATION (mW)	T_J GRADIENT (°C/PACKAGE)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5" Air flow is 500 LFPM in the Z axis.

6-11: Junction Temperature Thermal Gradients

From the air flow curve of Figure 6-12, the 16-pin ceramic DIP has a θ JA of 50°C/W (MC10101L Quad OR/NOR, Loaded with 4 50 ohm loads to -2 Vdc, mounted on

6-12: Typical Thermal Resistance versus Air Flow

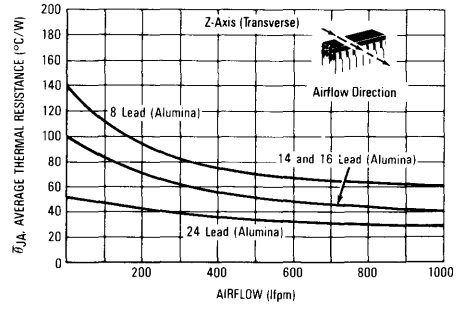


FIGURE 17A—AIRFLOW VERSUS THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PACKAGE)

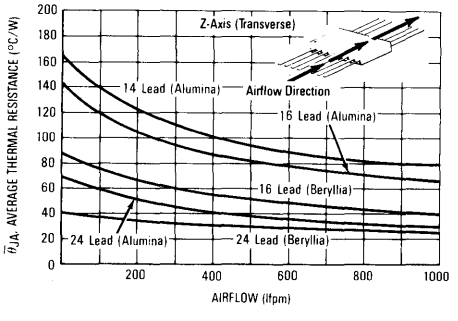


FIGURE 17B—AIRFLOW VERSUS THERMAL RESISTANCE (CERAMIC FLAT PACKAGE)

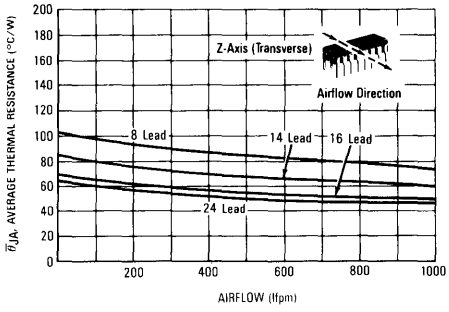


FIGURE 17C—AIRFLOW VERSUS THERMAL RESISTANCE (PLASTIC DUAL-IN-LINE PACKAGE)

printed circuit board with 500 LFPM air flow). This is a fairly standard air flow rate for cooling a moderate size system. In this case the first device in the 25°C air flow stream would have a junction temperature of:

$$T_J = \theta_{JA} P_D + T_A$$

$$T_J = (50°C/W)\,(0.195W) + 25°C = 34.8°\ C.$$

At an average power level of 200 mW/package, the heat gradient for junction temperature increase is 0.4°C per package. For example, the tenth package in an air flow path would have a junction temperature of 37.8°C.

The following is a typical thermal calculation for the amount of heat sinking to use with a dual in-line ceramic 16-pin MECL III counter circuit dissipating 900 mW. The maximum allowable junction temperature T_J, is 165°C and the operating ambient temperature, T_A, is 25°C. These calculations are based on still air.

$$\theta_{JA\ max} = \frac{T_{J\ max} - T_{A\ max}}{P_{D\ max}} = \frac{165°C - 25°C}{0.9\ watt} = 155.5°C/watt.$$

It is known that:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA},$$

where:

θ_{JC} = thermal resistance, junction to case,

θ_{CS} = thermal resistance, case to heat sink,

θ_{SA} = thermal resistance, sink to ambient;

therefore,

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS}).$$

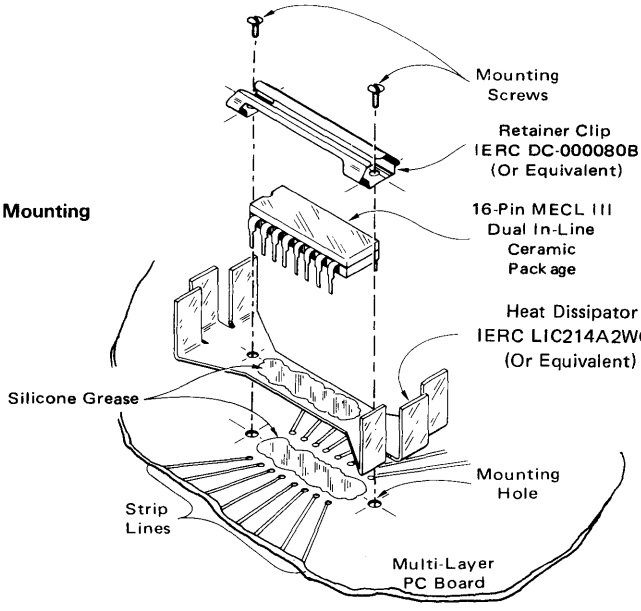
In still air, the thermal resistance, θ_{JC}, for the 16-pin DIL is 25°C/W. If thermal paste (Dow Corning 340, or equivalent) is used, the case to sink thermal resistance, θ_{CS}, would be 8°C/W. Thus the thermal resistance, θ_{SA}, can be calculated:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS}) = 155.5°C/W - (25°C/W + 8°C/W) = 122.5°C/W.$$

This is a worst allowable value. The heat sinking method actually chosen should have less thermal resistance than this, to insure the junction temperature (T_J) does not exceed 165°C.

The above calculations assume all package heat is dissipated through a heat sink. However, from Figure 6-12 it is seen that θ_{JA} for the package on a circuit board in still air is 100°C/W. Since this is below the 122.5°C/W previously calculated,

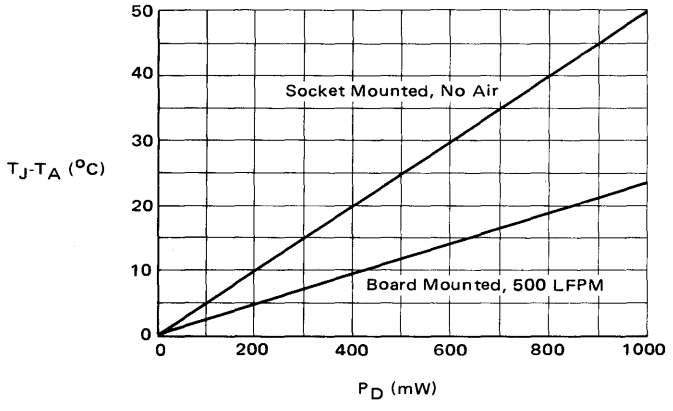
6-13: 16 Pin DIP Heat Sink Mounting



it is possible to use the MECL III counter in still air at 25°C and maintain the die temperatures within rated limits.

However, to allow for increased ambient temperatures and tight packaging, it is recommended that MECL III systems be designed *with* air flow, and that high dissipation MSI parts have additional heat sinking.

6-14: Thermal Curves for 16-Pin DIP Heat Sink IERC-LIC214A2WCB

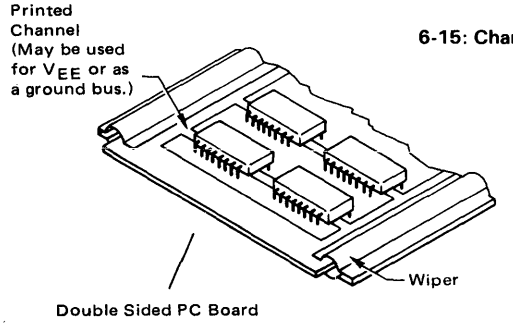


Mounting Techniques

Mounting techniques are particularly important with MECL III because of its higher package power dissipation. Some of the more complex MSI MECL III functions, such as the MC1678 decade counter, dissipate up to 900 mW and *do* require special cooling, MECL 10K/10KH dissipates much less package power, so standard mounting is normally more than adequate for most systems. For this reason, most of the mounting techniques discussed in this section apply primarily to MECL III.

A commercially available heat sink that was developed for use with the 16-pin dual in-line ceramic MECL III package is illustrated in Figure 6-13. This heat sink is small in size and will not affect lead interconnections. The overall package is very efficient in removing heat from the case as indicated by the graph in Figure 6-14. This type sink is recommended for the MC1678L decade counter complex function, or for that matter, any dual in-line package dissipating $\geqslant$ 750 mW. Another suitable heat sink is made by the Thermalloy Corporation.

Printed channeling is a useful technique for conducting heat away from the MECL DIP package when the device is soldered into a printed circuit board and thermal paste is used between the package and channel. As illustrated in Figure 6-15, this heat dissipation surface could also serve as a V_{EE} voltage distribution or ground bus. The channels should terminate into channel strips at each side or rear of a plug-in type printed circuit board. Then, by means of wipers that come into thermal contact with the edge channels, the heat can be removed from the circuit board into the cabinet or board slide-rack. This same technique can be used with the MECL flat package.



6-15: Channel/Wiper Heat Sinking

The importance of thermal management cannot be overemphasized. Proper design in this area can result in excellent system performance and increased reliability, especially in MECL III systems where higher power dissipation is encountered.

CHAPTER 7 Transmission Line Theory

Understanding the operation of transmission lines used in conjunction with high speed MECL circuits is necessary in order to be able to completely characterize system operation. While it is not expected that every system interconnection will be fully evaluated by a designer, the information in this chapter will be especially useful for setting up system design rules. This chapter describes transmission lines with respect to both line reflections and propagation delay times. Discussed will be the use of the Time Domain Reflectometer (TDR) for measuring transmission line characteristics.

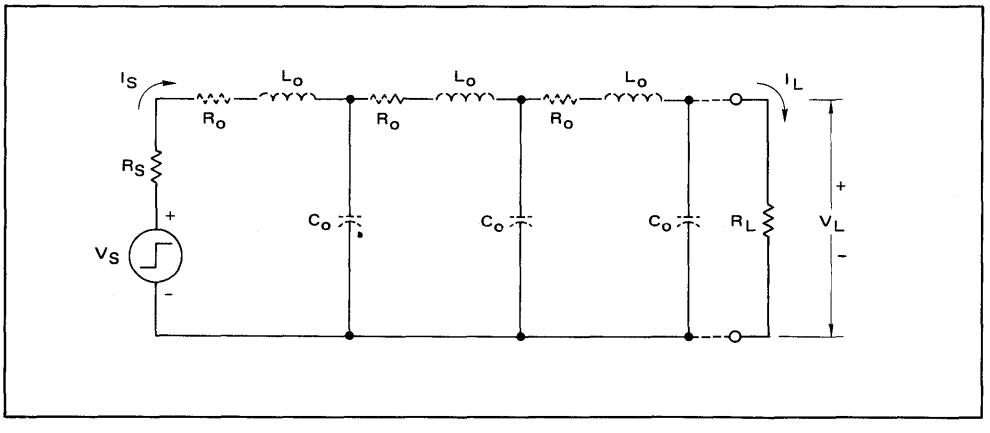
Transmission Line Design Information

A transmission line as used with high speed MECL is a signal path that exhibits a characteristic impedance. Coaxial cables and twisted pair lines have a defined characteristic impedance and are commonly referred to as transmission lines. Equally important, printed circuit fabrication of microstrip and striplines (as discussed in Chapter 3) results in closely-controlled transmission-line impedance.

The equations for voltage and current along a transmission line are fairly universal and may be found in reference 4. These equations show the voltage and current transmitted along a transmission line using the differential equations based on a point along the line.

Transmission lines may be approximated by the lumped constant representation shown in Figure 7-1. The effect of the resistance, R_O, of the line on the characteristic impedance, Z_O, is negligible, but it will cause some loss in voltage at the receiving end of long lines. The inductance and capacitance of the line in the presence of a ground plane are a function of the dielectric medium, the thickness and width of the line, and the spacing from the ground plane. The inductance and capacitance of the line can be measured using an LC meter.

7-1: Equivalent Circuit of a Transmission Line

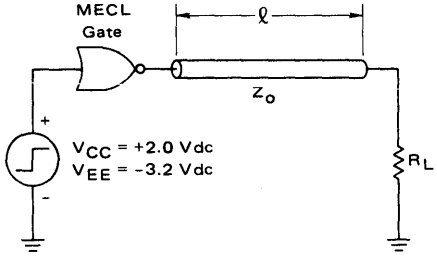


Microstrip and strip lines may be treated as operating in the transverse electro-magnetic (TEM) mode. Although microstrip propagation is not purely TEM because of non-uniform dielectrics, for all practical purposes it can be treated as TEM. The characteristic impedance of the line is $Z_O = \sqrt{L_O/C_O}$ and the propagation delay is $t_{pd} = \sqrt{L_O C_O} = Z_O C_O$. Reference 1 shows that for a homogeneous medium the propagation delay is also equal to $t_{pd} = \sqrt{\mu e} = \sqrt{\mu_O \mu_r e_O e_r}$, where μ is the permeability and e is the permittivity of the medium. In transmission lines, the relative permeability (μ_r) is unity, $\mu_O = 4\pi \times 10^{-7}$ Henry/meter, and $e_O = 8.85 \times 10^{-12}$ Farad/meter. Therefore, $t_{pd} = 1.017\sqrt{e_r}$ ns/ft, as was discussed earlier in Chapter 3 (e_r is the relative dielectric constant). For microstrip lines on glass epoxy boards $e_r = 3.0$, and for strip lines $e_r = 5.0$ (see reference 1).

From transmission line theory for a lossless line, it can be shown that a signal sent down a line of constant characteristic impedance will travel along the line without distortion. However, when the signal reaches the end of the line, a reflection will occur if the line is not properly terminated with the characteristic impedance of the line.

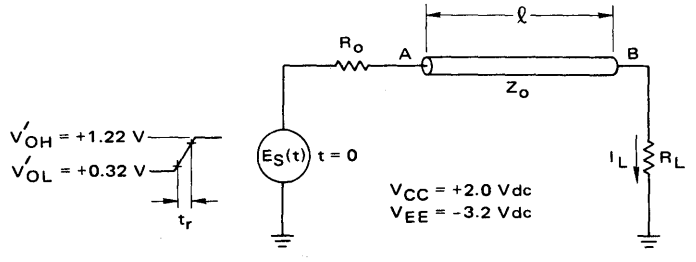
Figure 7-2 shows a MECL gate driving a transmission line terminated in a load resistor, R_L. A negative-going transition on the input to the gate will result in a positive-going transition at the NOR output. The MECL gate is essentially a VHF linear differential amplifier with a bandwidth of $0.37/t_r$ (MHz), where t_r is the rise time of the gate in nanoseconds. The effect of the capacitance of the transmission line will not decrease the bandwidth or affect the rise time at the MECL gate output. However, the signal at the end of a long transmission line may be attenuated due to band width limitations in the particular type of transmission line used. For the purposes of this discussion a long line is defined as a line having a propagation delay larger than the rise time of the driving circuit divided by two: $T_D > t_r/2$.

The circuit of Figure 7-2 can be redrawn as shown in Figure 7-3 to include the equivalent circuit of the MECL gate. The resistor, R_O, is the output source



7-2: MECL Gate Driving a Transmission Line

7-3: Equivalent MECL Gate Output, Driving a Transmission Line



impedance (for MECL 10K/10KH it is 7 ohms, and MECL III it is 5 ohms). According to theory, the rise time of the driving voltage source is not affected by the capacitance of the transmission line. Except for skin effect and dielectric losses, the signal will remain undistorted until it reaches the load. The equation representing the voltage waveform going down the line as a function of distance and time can be written as:

$$V_1(X, t) = V_A(t) \bullet U(t - Xt_{pd}), \text{ for } t < T_D \ , \tag{1}$$

where:

$$V_A(t) = E_S(t)\left(\frac{Z_o}{Z_o + R_o}\right),$$

V_A = voltage at point A,

X = the distance to an arbitrary point on the line,

ℓ = total line length,

t_{pd} = propagation delay of the line in ns/unit distance,

$T_D = \ell\, t_{pd}$,

$U(t)$ = a unit step function occurring at $t = 0$, and

$E_S(t)$ = the source voltage at the sending end of the line.

When the incident voltage V_1 reaches the end of the long line, a reflected voltage, V_1', will occur if $R_L \neq Z_o$. The reflection coefficient at the load, ρ_L, can be obtained by applying Ohm's Law.

The voltage at the load is $V_1 + V_1'$ which must be equal to $(I_1 + I_1')\, R_L$. But $I_1 = V_1/Z_o$, and $I_1' = -V_1'/Z_o$ (the minus sign is due to V_1' travelling toward the source). Therefore,

$$V_1 + V_1' = \left(\frac{V_1}{Z_o} - \frac{V_1'}{Z_o}\right) R_L \ . \tag{2}$$

By definition,

$$\rho_L = \frac{\text{reflected voltage}}{\text{incident voltage}} = \frac{V_1'}{V_1} \ .$$

Solving for V_1'/V_1 in equation 2, and substituting in the relation for ρ_L results in:

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o} \ . \tag{3}$$

Similarly, the reflection coefficient at the source is:

$$\rho_S = \frac{R_o - Z_o}{R_o + Z_o} \ . \tag{4}$$

By summing the incident voltage, V_1 (eq. 1), together with similar voltage contributions from the various orders of reflection (due to ρ_L and ρ_S), a general equation for total line voltage can be written, and used to develop practical design information:

$$V(X,t) = V_A(t)\Big[U\left(t - t_{pd}X\right) + \rho_L U\left(t - t_{pd}(2\ell - X)\right)$$

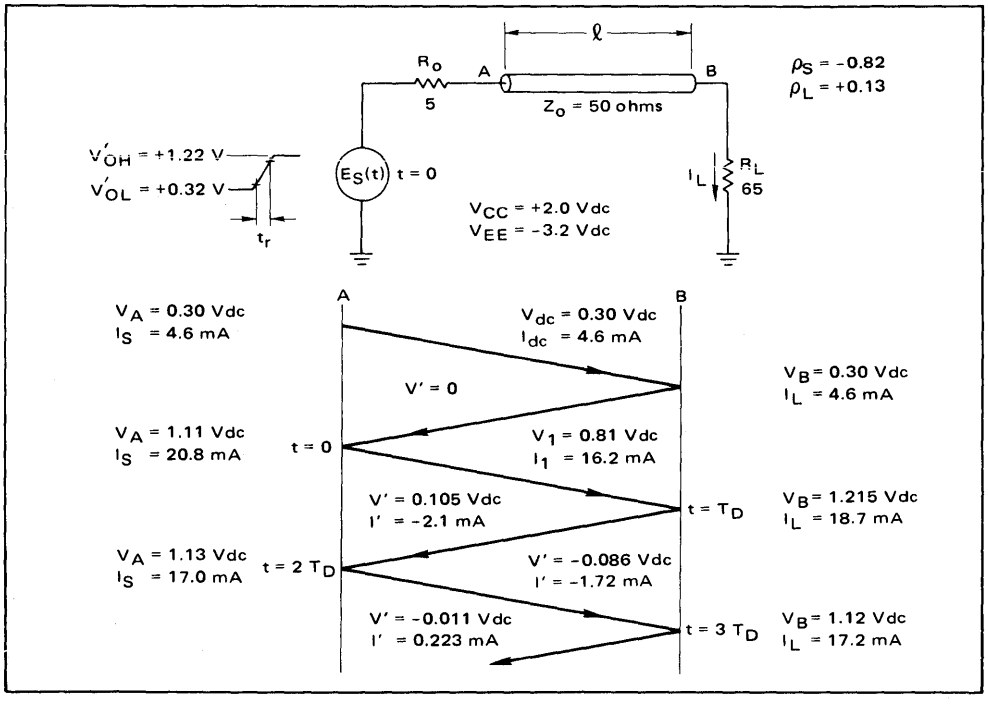
$$+ \rho_L\rho_S U\left(t - t_{pd}(2\ell + X)\right) + \rho_L{}^2\rho_S U\left(t - t_{pd}(4\ell - X)\right)$$

$$+ \rho_L{}^2\rho_S{}^2 U\left(t - t_{pd}(4\ell + X)\right) + \ldots\Big] + V_{dc} \qquad (5)$$

Note that as time progresses, the U step function brings successively higher order reflection coefficient terms into V (X, t). Successive terms may be positive or negative, depending on the resulting sign, and so damped ringing can occur. Equation 5 expresses the voltage at any point on the line, X, for any time, t. The equation can be used graphically with a lattice diagram (as explained in References 5 and 6), to find V (X, t).

Example 1. Figure 7-4 will be used to illustrate the lattice diagram method for

7-4: Lattice Diagram for a Typical Reflection Example



finding V (X, t) and the use of equation 5. The source impedance of the MECL III gate is 5 ohms, resulting in a reflection coefficient at the source of -0.82 for a line impedance of 50 ohms.

The load resistor is arbitrarily chosen to be 30 percent greater (65 ohms) than the characteristic impedance (50 ohms) so that reflections will occur. The resulting reflection coefficient at the load is $\rho_L = +0.13$. Two vertical lines are drawn to represent the input of the line, point A, and the output of the line, point B. A line is drawn from point A to point B before t = 0 to represent the steady state conditions. Note that for $V_{CC} = +2$ V and $V_{EE} = -3.2$ volts, the nominal logic levels are approximately logic $\emptyset = 0.3$ volts, and logic 1 = 1.14 volts. (These power supply conditions are used to permit convenient measurements when output resistors are returned directly to ground). For steady state conditions, the line looks like a short line with a resistance equal to R_{dc}. It can be assumed that R_{dc} is negligible for this example.

The voltage and current at points A and B are the same initially, as shown in the diagram. At t = 0, the voltage at the source switches from a logic $\emptyset$ to a logic 1 level. The voltage term, V_A (t), in equation 1 is:

$$V_A(t) = (V'_{OH} - V'_{OL}) \left(\frac{Z_o}{Z_o + R_o} \right) = V_1 = 0.81 \text{ volt},$$

where:

$$(V'_{OH} - V'_{OL}) = E_S(t) = \text{internal voltage swing in the circuit.}$$
$$= \Delta V_{INT}$$

Therefore, at time t = 0 a voltage waveform, $V_1 = 0.81$ volt, and a current, $I_1 = 16.2$ mA, travel down the line – as shown in the diagram by the line from t = 0 to t = T_D (T_D is the time it takes for the wavefront to travel down the length of line, ℓ). Next, a line is drawn from t = T_D to t = $2T_D$. Voltage and current values are indicated. Note that here the reflected current is negative, indicating the current is flowing back toward the source; the reflection coefficient for the current is a minus one times the reflection coefficient for the voltage.

To find the voltage at point B for t = T_D all the voltages arriving at and leaving from this point are summed. The same is done to determine the load current. The process continues until the voltage at the load approaches the new steady state condition – in the example, when t = $3T_D$. (The steady state logic 1 voltage is actually 1.13 volts).

This example indicates that for a case in which the load resistor is 30% higher than the characteristic impedance, 85 mV of overshoot and 10 mV of undershoot would occur. Generally, as far as noise immunity is concerned, only the undershoot need be considered. The typical noise immunity (or noise margin) for a MECL circuit is greater than 200 mV. Since the undershoot in this example was 10 mV, the typical noise immunity would exceed 190 mV. In actual system design, typically more than 100 mV of undershoot can be tolerated. Regarding overshoot, 300 mV can be tolerated, except in some early ac coupled flip-flops (MECL I and II). This restriction insures that saturation of the input transistor does not occur (if it did, the gate would slow down). If a 100 ohm load resistor were used in Figure 7-4, the resulting overshoot would be about 220 mV and the undershoot, about 80 mV. In effect then, if the load resistor is twice the characteristic impedance, the noise margin is typically 120 mV – which is more than acceptable for MECL circuits.

A slightly different situation can exist when the output of the MECL gate switches from a logic 1 to a logic ∅. The output of the MECL gate will turn off if the termination resistor, R_L, is somewhat larger than the characteristic impedance of the line. For the conditions in Figure 7-4, the output transistor of the MECL gate will turn off at t = 0 for the negative going transition, when $R_L > 70$ ohms.

An equation for the value of R_L at which the gate will turn off can be derived as follows. The maximum voltage change at point A, Figure 7-4, (due to turning off the output transistor) is the product of the dc current in the line and the characteristic impedance of the line:

$$\Delta V_A = I_{LINE}(Z_o) = \frac{V'_{OH}}{R_o + R_L}(Z_o).$$

The voltage at point A is also dependent on the internal resistance of the driving gate R_o and the internal logic swing:

$$\Delta V_A = \frac{Z_o}{R_o + Z_o}(\Delta V_{INT}).$$

Equating the two and solving for R_L:

$$R_L = \frac{V'_{OH}(R_o + Z_o)}{\Delta V_{INT}} - R_o. \tag{6}$$

Thus for the conditions given in Figure 7-4, the output transistor will turn off at t = 0 when $R_L = \frac{1.22(5 + 50)}{0.9} - 5 = 70\Omega$ is exceeded.

The case for which the MECL output turns off is not in itself a serious problem, although it makes a thorough analysis more difficult. Two reflection coefficients must be used at the sending end, and a piecewise approach used in determining the voltage reflections.

Example 2. The condition for a negative-going transition will now be analyzed (cf Figure 7-5.) The steady state high logic level current is:

$$I_{dc} = \frac{V'_{OH}}{R_o + R_L} = 11.6 \text{ mA}.$$

For the conditions shown in Figure 7-5, the use of equation 6 shows that the load resistor is indeed larger than required to turn off the output transistor during a negative transition.

To determine the voltage V_1 at t = 0, the following equation results from the application of Ohm's Law to the circuit:

$$V_1 = -\left(I_{dc} + \frac{V_A + 3.2 + V_1}{R_E}\right) Z_o. \tag{7}$$

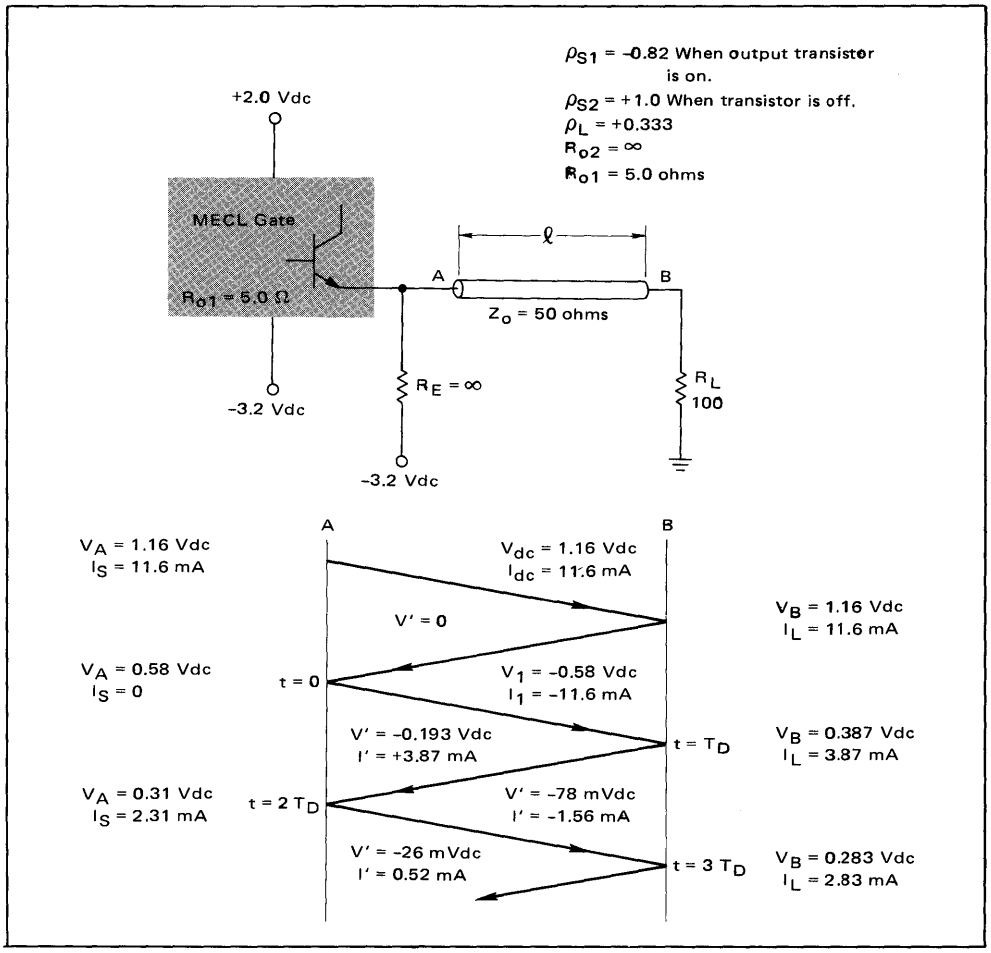
For the example shown, let $R_E = \infty$, then:

$$V_1 = -I_{dc}Z_o \cdot \tag{8}$$

Solving equation 8, $V_1 = -0.58$ volt. The implication of this result is that stubbing off the line with gate loads in a distributed fashion is not recommended, due to the reduced intital voltage swing. However, it would be acceptable to lump the loads at the end of the line (as will be shown).

Since the value of the load resistor is greater than the characteristic impedance, the voltage swing at the load resistor is greater than V_1 by the amount of $\rho_L V_1$ (in this example, 193 mV). When $t = T_D + T_1$, the voltage at B is equal to 0.387 volt; so 82 mV of undershoot occurs. Undershoot on the falling edge is defined as the amount of voltage step above the nominal logic $\emptyset$ level of 0.305 volt. Overshoot in the low logic state is defined as the amount of voltage change below the logic $\emptyset$ level.

7-5: Lattice Diagram for Negative-Going Voltage Transition



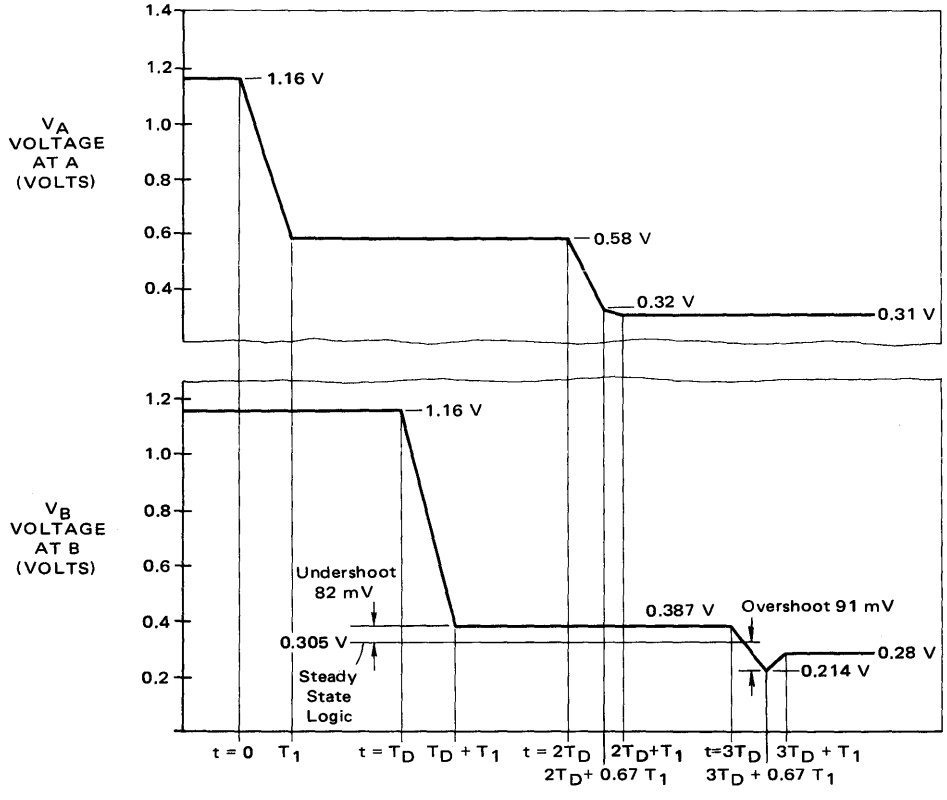
In Figure 7-6, the voltage waveforms at points A and B of this example are shown as a function of time. To be more realistic, the waveform in the figure is shown to be a negative-going ramp rather than an abrupt step function. The term, T_1, is the amount of time it takes for the waveform at A to switch to the level at which the output transistor turns off. The fall time of the signal would have been longer by an amount equal to $T_1' = \frac{(1.16 - 0.305)}{(1.16 - 0.58)} T_1$, if the termination resistor had been 70 ohms or less.

The reflected voltage waveform leaving point B at $t = T_D$ arrives at point A at $t = 2T_D$. The source impedance is very high initially ($\rho_S = +1.0$), with the output transistor being in the off condition until the voltage at A falls to 0.32 volt. Then, the source impedance changes to 5 ohms ($\rho_S = -0.82$). The following formula may be used to determine the point at which the transistor turns on:

$$\Delta V_{source} = V_1 + \rho_S V_1 = 2V_1 \quad \text{(valid prior to transistor conduction)}, \tag{9}$$

where V_1 is now the incident voltage approaching the source and ΔV_{source} is the change in voltage at the source necessary to turn the transistor on.

7-6: Voltage Waveforms for Points A and B in Example 2



In this example the actual voltage change for conduction to occur is: $\Delta V_{source} = 0.32 - 0.58 = -0.26$ volt. Therefore, the voltage waveform approaching the source (193 mV) can be broken into two signals, $V_{11} = -0.13$, and $V_{12} = -0.063$ volt. The reflected voltage due to V_{11} is $V'_{11} = -0.13$ volt, and for V_{12}, the reflected voltage is $V'_{12} = (-0.82)(-0.063) = +0.052$ volt. The two reflected voltages of opposite polarity at point A going toward point B are the reason for the increased overshoot of short duration at point B, when $t = 3T_D + \left(\frac{0.13}{0.193}\right) T_1$ (see Figure 7-6).

The steady state voltage reflection that occurs after $t = 2T_D + T_1$ is the sum of -0.13 volt and +0.052 volt, equal to -78 mV as shown in Figure 7-5. The steady state voltage reflection can be calculated using the relation:

$$V' = \rho_{S2}\Delta V_{source}\left(\frac{1 + \frac{Z_o}{R_{o2}}}{2}\right) + \rho_{S1}\left[V_1 - \Delta V_{source}\left(\frac{1 + \frac{Z_o}{R_{o2}}}{2}\right)\right]. \quad (10)$$

Equation 10 may be illustrated by solving for the steady state reflection voltage at $t = 2T_D + T_1$:

$$V' = (+1.0)(0.32 - 0.58)\left(\frac{1 + \frac{50}{\infty}}{2}\right) + (-0.82)\left[-0.193 - (0.32 - 0.58)\left(\frac{1 + \frac{50}{\infty}}{2}\right)\right] = 78 \text{ mV}.$$

From the analysis of Figure 7-5, it is concluded that the MECL gate can safely drive the transmission line ($Z_o = 50$ ohms) with a 100 Ω load resistor and with the gate loads lumped at the end of the line, since less than 100 mV of undershoot occurs. The remaining noise margin will be typically greater than 100 mV.

Signal Propagation Delay for Microstrip and Strip Lines with Distributed or Lumped Loads

The propagation delay, t_{pd}, has been shown in Chapter 3 to be 1.77 ns/ft for microstrip lines and 2.26 ns/ft for strip lines, when a glass epoxy dielectric is the surrounding medium. The propagation delay time of the line will increase with gate loading and the altered delay can be derived as follows. The unloaded propagation delay for a transmission line is $t_{pd} = \sqrt{L_o C_o}$. If a lumped load, C_d, is placed along the line, then the propagation delay will be modified to t'_{pd}:

$$t'_{pd} = \sqrt{L_o(C_o + C_d)} = \sqrt{L_o C_o}\sqrt{1 + \frac{C_d}{C_o}} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}}, \quad (11)$$

where L_o and C_o are the intrinsic line inductance and capacitance per unit length.

Therefore, the signal propagation down the line will increase by the factor of:

$$\sqrt{1 + \frac{C_d}{C_o}} .$$

A MECL gate input should be considered to have 5 pF of capacitance for ac loading considerations (includes stray capacitance). If 4 gate loads are placed on a 1 foot signal line, then the distributed capacitance, C_d, is equal to 20 pF/ft or 1.67 pF/in. As an example, assume that it is desired to find the propagation delay increase for a 50-ohm microstrip line on a glass epoxy board. From Figure 3-7 assume that the line width is chosen to be 25 mils; then the dielectric material should have a thickness of 15 mils to yield $Z_o = 50\Omega$. From Figure 3-8, the capacitance of the line is 35 pF/ft. Therefore, the modified propagation delay would be:

$$t'_{pd} = 1.77 \text{ ns/ft} \sqrt{1 + \frac{20}{35}} = 2.21 \text{ ns/ft} .$$

For a 50-ohm strip line on a glass epoxy board with a 15 mil spacing between the strip line and ground plane, a 12 mil width would be required (cf Figure 3-9). From Figure 3-10, the strip line would exhibit a capacitance of 41 pF/ft.

The modified propagation delay for such a strip line would be:

$$t'_{pd} = 2.26 \text{ ns/ft} \sqrt{1 + \frac{20}{41}} = 2.75 \text{ ns/ft} .$$

Notice that the propagation delay for the strip line and the microstrip line change by approximately the same factor when the separation between the line and ground plane, and the characteristic impedance are the same. However the line width of the strip line is less (by a factor of 2) than the microstrip line for the same characteristic impedance.

It should be noted that to obtain the minimum change and lowest propagation delay as a function of gate loading, the *lowest* characteristic impedance line should be used. This will result in the largest intrinsic line capacitance. With MECL 10K/10KH the lowest impedance that can be used is about 35 ohms ($V_{TT} = -2.0$ volts, $R_{TT} = 35$ ohms).

According to theory (Reference 1), whenever an open line (stub) is driven by a pulse, the resultant undershoot and ring are held to about 15 percent of the logic swing if the two way delay of the line is less than the rise time of the pulse. The maximum line length, ℓ_{max}, may be calculated using the equality:

$$\ell_{max} = \frac{t_r}{2t'_{pd}} \text{ (inches)} ,$$

where t_r is the rise time of the pulse in nanoseconds, and t'_{pd} is the modified propagation delay in nanoseconds/inch from equation 11.

A quadratic equation for maximum line length for G-10 fiber glass epoxy microstrip conductors may be written in terms of C_D C_o and t_r as:

$$\ell^2_{max} + \frac{C_D}{C_o}\ell_{max} - 11.1\ t_r^2 = 0, \text{ (for microstrip lines)}, \quad (12)$$

where C_D is total gate capacitance.

An equation for maximum open line length for a strip line (using G-10 fiber glass epoxy material) can be written in a similar fashion. The result is:

$$\ell^2_{max} + \frac{C_D}{C_o}\ell_{max} - 7.1\ t_r^2 = 0, \quad \text{(for strip lines)}. \quad (13)$$

Using the lattice diagram, it has been found that the rule of thumb used to derive equations 12 and 13 should be modified for an open line because the incident voltage doubles at the end of the line. This results in a faster rise time at the receiving end of an unloaded line than at the driving end. An approximate value of maximum open line length can be generated from equations 12 and 13 if the rise time that is substituted into the equations is multiplied by an adjustment factor, 0.75. This maintains an approximate overshoot and undershoot of less than 35% and 12% respectively.

To demonstrate how equations 12 and 13 may be used, the maximum open line length will be computed for a 50 ohm line with a fanout of one MECL 10K gate. Using the equation $t_{pd} = Z_o C_o$, the line capacitance, C_o, is found to be $C_o = 2.96$ pF/in for microstrip, and $C_o = 3.76$ pF/in for strip line. For a fanout of one, C_D is equal to 5 pF when the device is in a socket. The rise time for MECL 10K is 3.5 ns which means that a value of $t_r = 0.75 \times 3.5 = 2.6$ ns should be used in the equations. Solving equations 12 and 13, $\ell_{max} = 7.9$ inches for a 50 ohm microstrip line and $\ell_{max} = 6.2$ inches for a 50 ohm strip line.

Equations 12 and 13 can be very useful in finding the approximate maximum line length under various conditions. However if overshoot or undershoot differing from the above values is specified, equations 95 and 103 (derived later in this chapter) should be used for defining maximum line length. The exact voltage at the end of an open line with loading is also derived later in this chapter, and leads to equation 87. Using that equation, a computer program has been written in which the maximum line length is calculated when maximum overshoot and undershoot are specified. Figures 3-13, 3-14, and 3-15 show the results of the program. Note that the tables give the maximum line lengths for fanouts of 1, 2, 4, and 8 for various types of lines with a wide range of characteristic impedances.

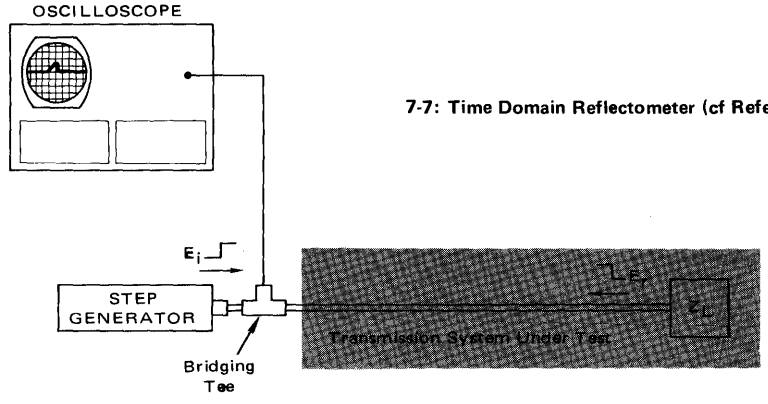
The maximum line lengths are also given for various characteristic impedances in the backplane. The characteristic impedance of the backplane should be between 100 and 180 ohms if a ground screen is used. For MECL 10K from Table 3-13, 5.9 inches of open backplane wiring can be driven for a fanout of one.

It should be remembered that these line lengths are based on 100 mV maximum undershoot, and are not absolute maximum lengths with which MECL circuits will operate. It is possible to use longer unterminated lines than shown – the tradeoff being an associated loss of noise immunity due to increased ringing.

From these calculations, it can be concluded that lower impedance lines result in longer line lengths before termination is required. The lower impedance lines are preferred over higher impedance lines because longer open lines are possible, and the propagation delay down the line is reduced. In addition, more stubbed-off gate loads can be driven with a terminated line due to its higher capacitance per unit length.

Microstrip Transmission Line Techniques, Evaluated Using TDR Measurements

The time domain reflectometer (TDR) employs a step generator and an oscilloscope in a system which might be described as "closed-loop radar" (cf Figure 7-7). In operation, a voltage step is propagated down the transmission line under investigation. Both the incident and reflected voltage waves are monitored on the oscilloscope at a particular point on the line.



7-7: Time Domain Reflectometer (cf Reference 7)

The incident voltage step, E_i, is a positive edge with an amplitude of 1 volt and a rise time of 30 ps. It is generated by a tunnel diode, which has a source impedance of 50 ohms (HP 1817A sampler, or equivalent). Also, the output edge has very little overshoot (less than ±5%).

This TDR technique reveals the characteristic impedance of the line under test. It shows both the position and the nature (resistive, inductive, or capacitive) of each discontinuity along the line, and signifies whether losses in a transmission system are series losses or shunt losses. All of this information is immediately available from the oscilloscope's display (cf Reference 7). An example of a microstrip line evaluated with TDR techniques is shown below.

TDR Example 1.

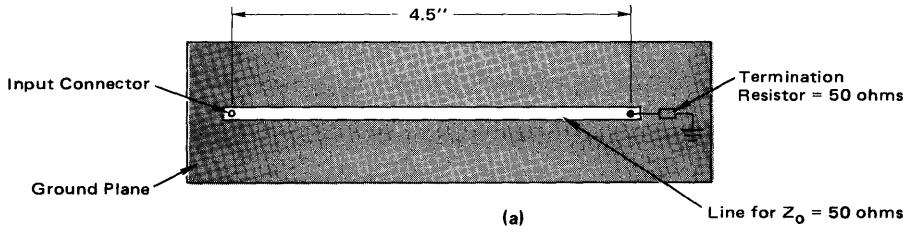
Board material:	Norplex Type G-10;
Dielectric thickness:	$h = 0.062$ inch;
Copper thickness:	$t = 0.0014$ inch;
Dielectric constant:	$e_r = 5.3$.

The formula for the characteristic impedance given in Chapter 3 was:

$$Z_o = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98\,h}{0.8\,w + t}\right). \qquad (14)$$

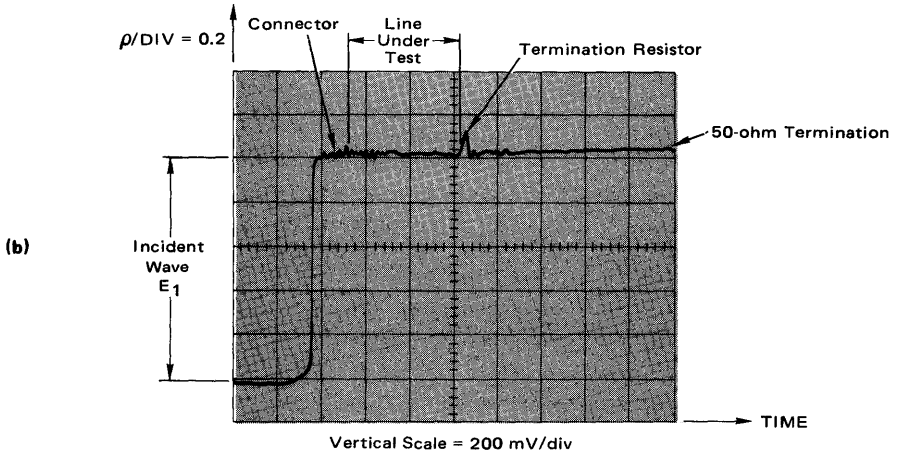
For a line width, $w = 0.1$ inch, the characteristic impedance of the line is calculated to be 51 ohms. A board was fabricated as shown in Figure 7-8(a) to the dimensions specified above. Figures 7-8(b) and 7-8(c) show the incident and reflected

7-8: TDR Determination of Line Characteristic Impedance



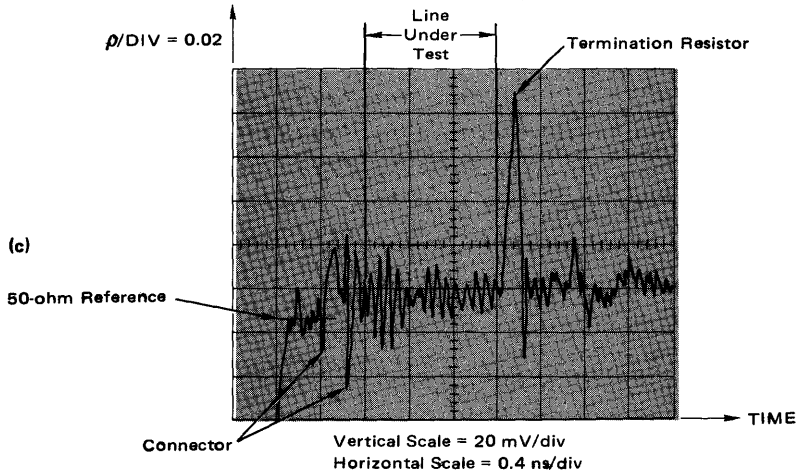
(a)

Vertical Scale = 500 mV/cm
Horizontal Scale = 2.0 ns/cm



(b)

Vertical Scale = 200 mV/div
Horizontal Scale = 0.6 ns/div



(c)

Vertical Scale = 20 mV/div
Horizontal Scale = 0.4 ns/div

waveforms observed with the TDR. The vertical scale is calibrated both in terms of the voltage and the reflection coefficient, ρ. Equation 3 can be rearranged to determine the characteristic impedance of the line:

$$Z_{line} = \left(\frac{1 + \rho}{1 - \rho}\right) \cdot Z_{reference} \quad , \tag{15}$$

where: Z_{line} = characteristic impedance of the line under test,

$Z_{reference}$ = impedance of the known line.

The 50 ohm reference point is shown in Figure 7-8(c). The mean level of the reflected waveform due to the line has a $\rho = +0.01$. Substituting values into equation 15 permits calculation of the line impedance:

$$Z_{line} = \left(\frac{1 + 0.01}{1 - 0.01}\right) \cdot 50 \text{ ohms} = 51 \text{ ohms} \quad ,$$

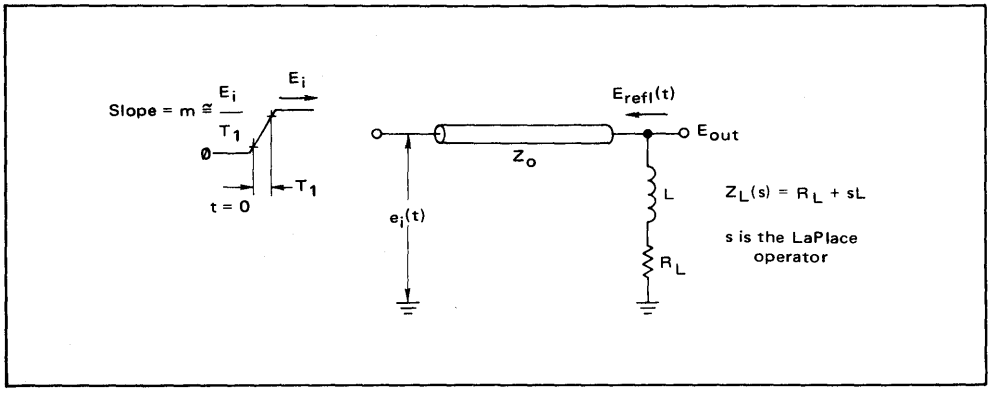
which agrees closely with the calculated value.

The reflected voltage due to the connector is ±40 mV. The line reflects a voltage of ±25 mV due to variations in the characteristic impedance of the line. The reflection of 88 mV shown for the termination resistor ($\rho = 0.088$) is due to the inductance of the resistor. It was calculated (by methods to be shown later) that the inductance of the resistor was less than 0.9 nH.

In these experiments, the input waveform comes from a tunnel diode generator which has a rise time of 28 ps. There is some attenuation of the signal noticeable as it reaches the termination resistor (t_r = 80 ps at the load). When driving the line with a MECL III gate with a rise time of 1 ns, the reflection due to the inductance of the resistor would be much less (about 10 mV).

TDR Example 2: An equation can be derived to determine the maximum reflection voltage due to the inductance of the resistor leads. The circuit shown in Figure 7-9 will be used in the derivation.

7-9: Circuit for Determining the Maximum Reflected Voltage Due to the Inductance of the Resistor Leads



Derivation: Maximum Reflection Voltage due to Resistor Inductance

The reflection coefficient at the load is:

$$\rho_L(s) = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{(R_L + sL) - Z_o}{(R_L + sL) + Z_o} = \frac{s + \dfrac{R_L - Z_o}{L}}{s + \dfrac{R_L + Z_o}{L}}, \qquad (16)$$

where s is the LaPlace operator for $j\omega$. The driving voltage will be represented as:

$$e_i(t) = mt\,U(t) - m(t - T_1)\,U(t - T_1), \qquad (17)$$

where U(t) is a step function occurring at t = 0. Taking the LaPlace transform of equation 17 gives:

$$E_i(s) = \frac{m}{s^2}\left(1 - e^{-T_1 s}\right). \qquad (18)$$

The reflected voltage at the load is then the product of the driving voltage and the reflection coefficient (both in the transformed plane):

$$E_{refl}(s) = E_i(s)\rho_L(s) = \frac{s + \dfrac{R_L - Z_o}{L}}{s^2\left(s + \dfrac{R_L + Z_o}{L}\right)} \cdot m\left(1 - e^{-T_1 s}\right). \qquad (19)$$

Taking the inverse LaPlace transform yields:

$$E_{refl}(t) = \left[\frac{2Z_oL}{(R_L + Z_o)^2} + \left(\frac{R_L - Z_o}{R_L + Z_o}\right)t - \left(\frac{2Z_oL}{(R_L + Z_o)^2}\right)e^{-\frac{(R_L + Z_o)t}{L}}\right] mU(t) -$$

$$\left[\frac{2Z_oL}{(R_L + Z_o)^2} + \left(\frac{R_L - Z_o}{R_L + Z_o}\right)(t - T_1) - \left(\frac{2Z_oL}{(R_L + Z_o)^2}\right)e^{-\frac{(R_L + Z_o)(t - T_1)}{L}}\right]$$

$$mU(t - T_1). \qquad (20)$$

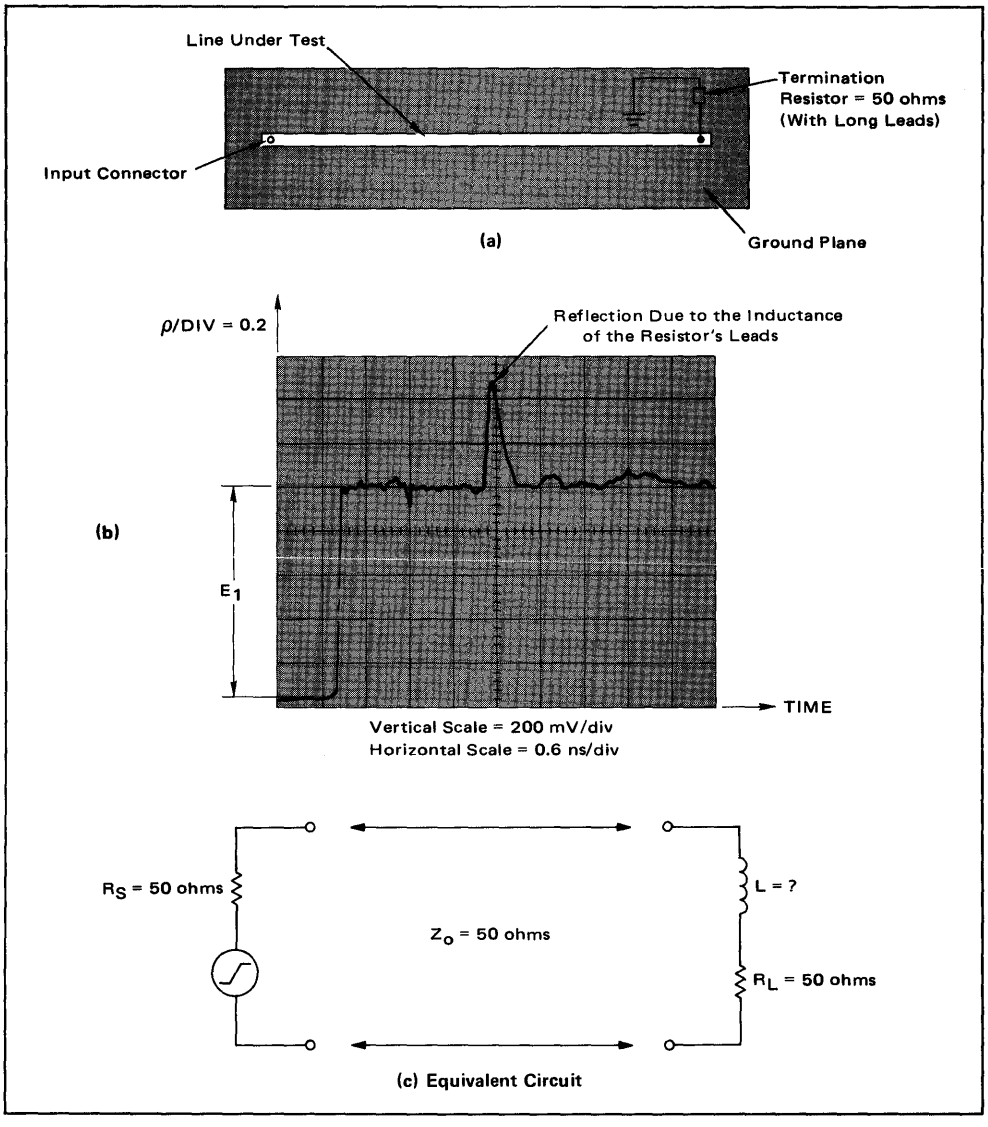
The maximum reflection voltage occurs at $t = T_1$. Then, for $R = Z_o$:

$$E_{refl}(t = T_1) = E_{refl\,max} = \frac{mL}{2Z_o}\left(1 - e^{-\frac{2Z_o}{L}T_1}\right). \qquad (21)$$

This equation relates the maximum reflected voltage, which can be measured by TDR, and the inductance, which can then be calculated for the circuit of Figure 7-9.

TDR Example 3. This example indicates how to measure the effect of resistor leads using the TDR. Figure 7-10(a) shows the construction of a microstrip board used for

7-10: Effects Due to Termination Resistor Leads



determining the effects of a resistor with 1" lead lengths. The reflected voltage determined from the TDR measurement is 480 mV (see Figure 7-10(b)). The rise time at the input to the line is 28 ps but it is lengthened to about 80 ps as the wavefront reaches the termination resistor.

The time, T_1, associated with the slope of the input voltage rise at the terminating resistor can be approximated as:

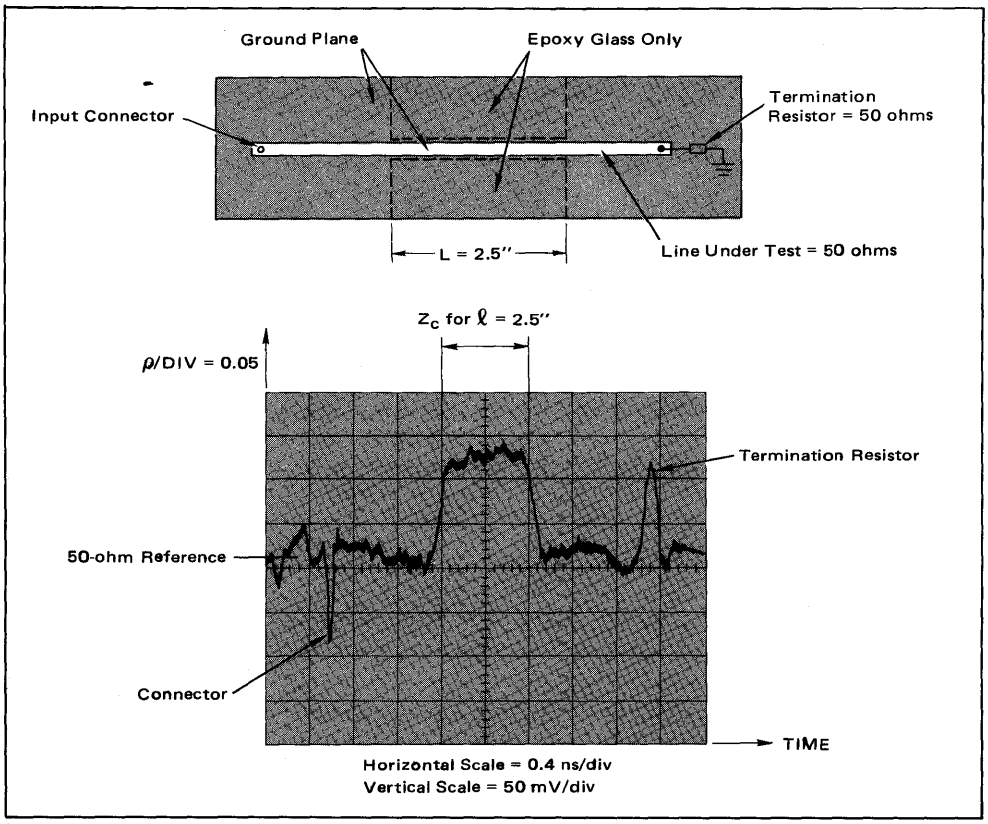
$$T_1 \approx \frac{t_r}{0.80} = 100 \text{ ps.} \tag{22}$$

The inductance can be computed by using equation 21, giving L = 6 nH. Additional information can be obtained from the decay of the reflection shown in Figure 7-10(b). The decay lasts about 0.3 ns, implying a time constant of about 0.3 ns/5 = 60 ps (using 5 time constants as a decay time). The calculated time constant for an inductance of 6 nH is: $L/2Z_o$ = 60 ps. The two results agree closely.

When driving the line with a MECL III gate – rise time = 1 ns – the reflection would be only 50 mV. Most carbon resistor types will have less than 10 nH of inductance. This inductance gives a reflection < 75 mV when the line is driven by a MECL III gate. Note that the reflection is positive, indicating that the noise immunity of a MECL gate connected at the load would be unchanged.

TDR Example 4. Experiments have also been performed to determine the effects of a ground plane on the characteristic impedance of microstrip lines. Figure 7-11

7-11: Effects of Ground Plane Discontinuities



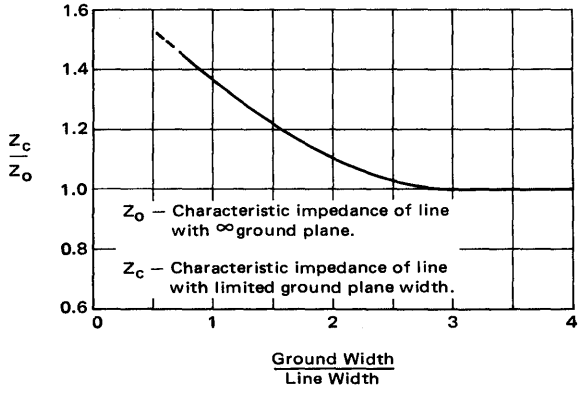
illustrates what happens when the ground plane width under the transmission line abruptly drops to the width of an active line. The TDR waveform shows that a 12% reflection occurs due to this discontinuity in the ground plane.

Using equation 15 the impedance of the 2-1/2 inch-long strip can be calculated as:

$$Z_{line} = \frac{1 + 0.12}{1 - 0.12} \cdot 50 = 68 \text{ ohms.}$$

Figure 7-12 shows a curve that approximates the change in the characteristic impedance of the line for various ratios of ground plane width to active line width. Note that when the ground width is greater than 3 times the line width, the characteristic impedance is constant according to equation 14.

7-12: Variation of Microstrip Impedance as a Function of Ground Width ÷ Line Width



A related experiment was performed to find the reflection due to a ground plane near the active line, but not directly under it. The test configuration and test results are shown in Figure 7-13. As indicated by the TDR measurement, the reflection is about 36%. Again using equation 15, the impedance of the 2-1/2 inch strip can be calculated:

$$Z_{line} = \frac{1 + 0.36}{1 - 0.36} \cdot 50 = 106 \text{ ohms.}$$

The reason for the reflection is the change in the characteristic impedance along the line resulting from the ground plane not being under part of the active line. In such a region, capacitance of the line to ground *decreases* while the inductance of the line *increases*, the net result being a higher characteristic impedance.

It must be remembered that the TDR input waveform has a rise time of 28 ps. Consequently, in a real logic circuit situation where, perhaps, a MECL III gate with a 1 ns rise time is driving the line, the reflection would actually be less than 27%, not 36% as in this example. This can be determined by scaling the value of ρ found with

the TDR waveshape in Figure 7-13(b), with a 1 ns rise time. When the length of the ground plane discontinuity is less than the distance travelled by the signal during its rise time, then the reflection coefficient can also be calculated as:

$$\rho' = \frac{2\ell\, t_{pd}}{t_r} \cdot \rho, \quad \text{for } \frac{2\ell\, t_{pd}}{t_r} < 1 \quad , \tag{23}$$

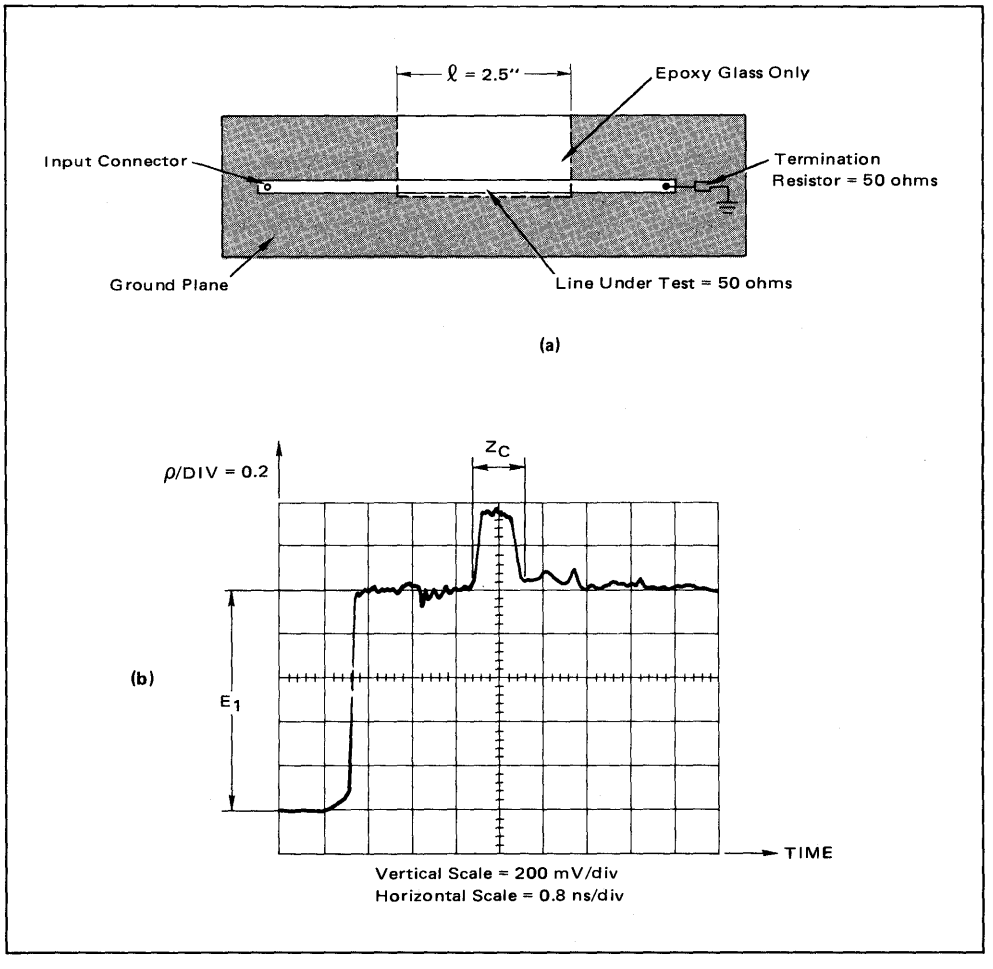
where: t_{pd} = the propagation delay time of the line in ns/in.

t_r = the rise time of the signal in ns,

ℓ = the length of the discontinuity in inches,

ρ = the reflection coefficient for $2\ell t_{pd}/t_r \geqslant 1$ (in this case the value found with the TDR waveshape with t_r = 28 ns).

7-13: Effects of Ground Plane Discontinuity



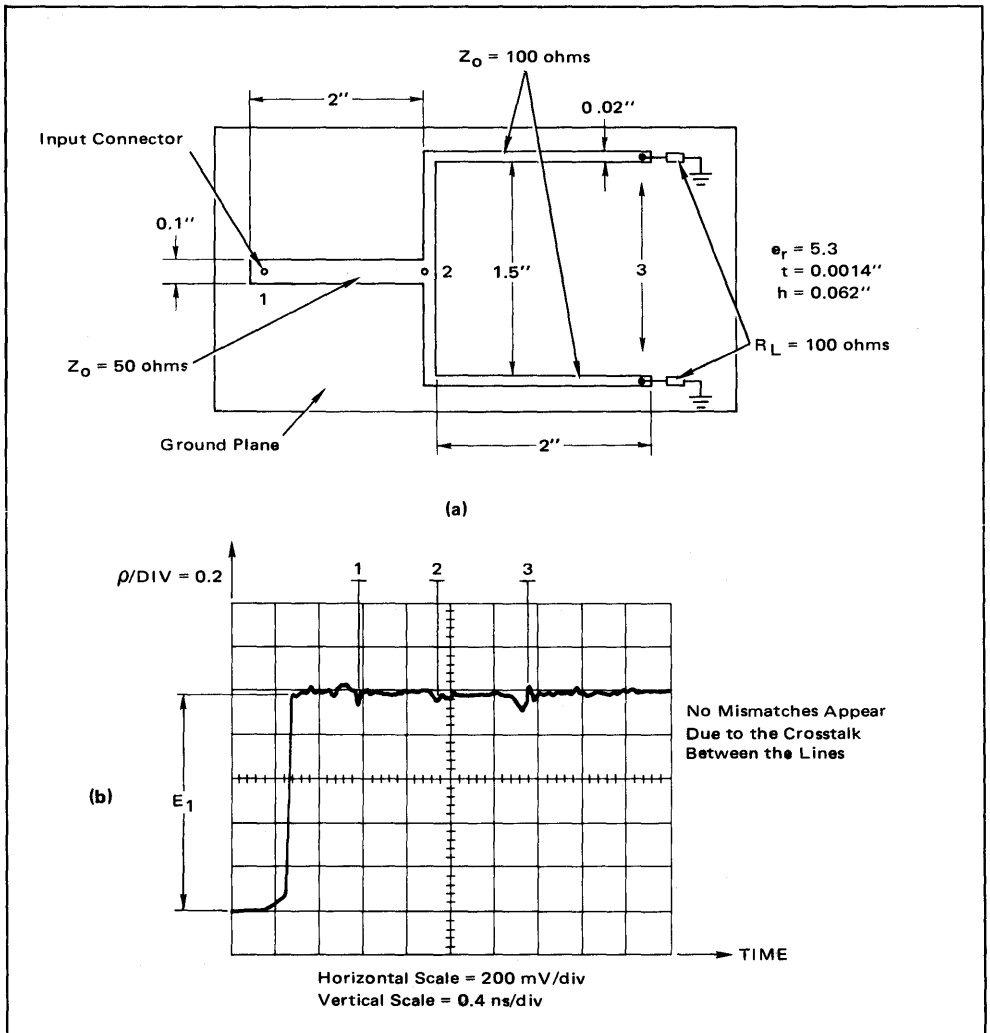
For a discontinuity in the ground plane of 2.5 inches length, a propagation delay of the line of 0.15 ns/in, and a MECL III gate with 1 ns rise time, the percent reflected voltage can be calculated. From Figure 7-13(b), ρ is found to be 0.36. Using equation 23,

$$\rho' = \frac{2(0.36)\,(2.5)\,(0.15)}{(1)} = 0.27 \quad .$$

Therefore, the reflection would be 27%. For a MECL 10K series gate, with a rise time of 3.5 ns, the reflection would only be 7.7%, and a MECL 10KH gate with a rise time of 1.8 ns, the reflection would be 15%.

TDR Example 5. Another measurement was performed, as shown in Figure 7-14, to observe the reflections due to the use of a hybrid divider. The construction of the

7-14: Hybrid Divider

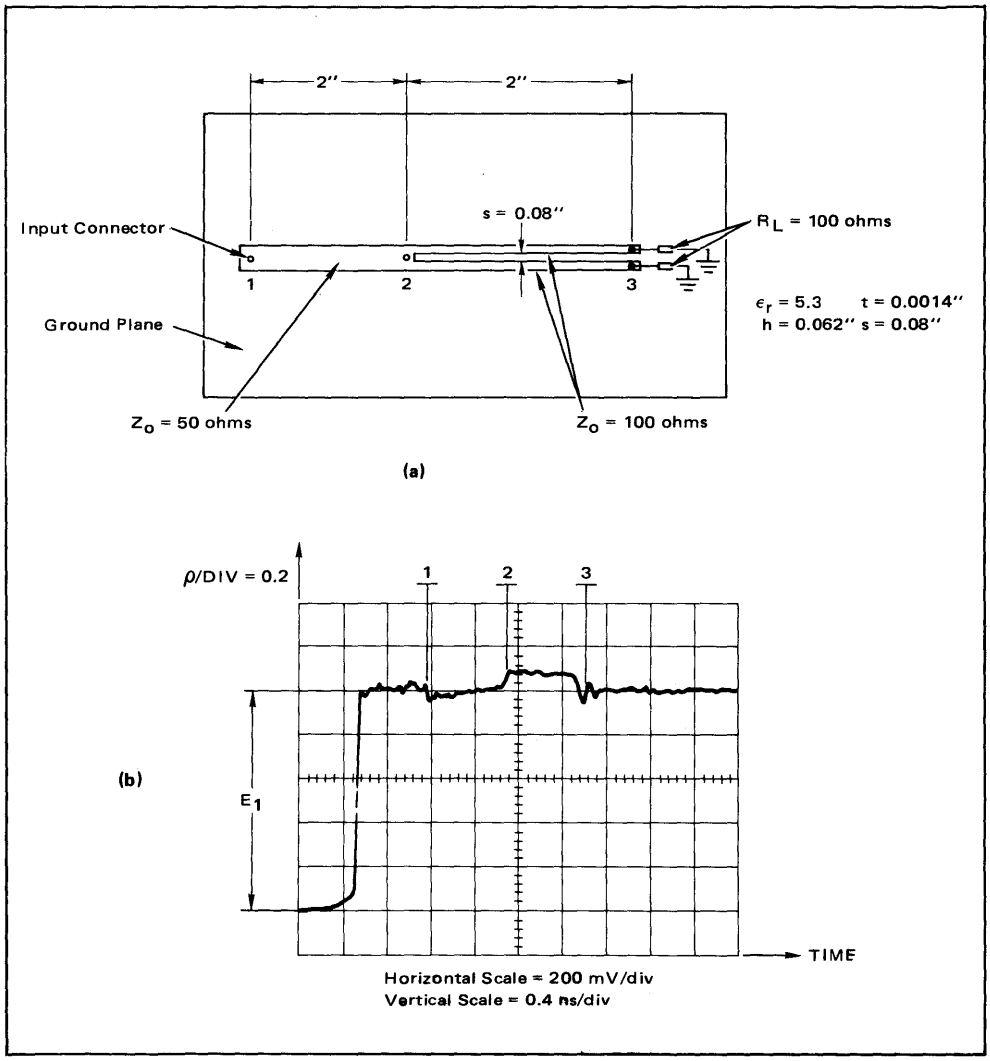


microstrip board used is shown in the figure. Note that the 50 ohm line branches out into two 100 ohm lines. A reflection of 4 percent is observed at point 2 where the junction occurs. Notice that the resistor exhibits a reflection of -8%, due to capacitance of the resistor.

Previously it was found that the 50 ohm resistor was inductive. Both results agree with Reference 8 in which it is stated that the lower values of resistors (<75 Ω) exhibit inductance, while the higher values behave capacitively. These effects are also shown in the data in Figure 4 of Chapter 4. Note that no mismatch appears due to crosstalk between the two 100 ohm branches, because of their wide separation.

Figure 7-15(b) shows the reflection due to the construction of Figure 7-15(a) where the two 100 ohm lines have been brought close together. The reflection at point 2 is now equal to 8% arising from the cross coupling of the two lines. Crosstalk is discussed in References 5, 9, 10, and 11.

7-15: Hybrid Divider With Crosstalk Problem



Even mode or odd mode characteristic impedance (Z_{oe} or Z_{oo}) can be considered to exist in a circuit with crosstalk. One, Z_{oe}, is due to the strips being at the same potential and carrying equal currents in the same direction. The other, Z_{oo}, is due to the strips being at equal but opposite potentials and carrying equal currents in opposite directions. The backward crosstalk voltage, V_B, on a passive line is given in Reference 10 as:

$$V_B = \left(\frac{Z_{oe} - Z_{oo}}{Z_{oe} + Z_{oo}} \right) E_1 \quad , \tag{24}$$

where E_1 is the signal propagating down the active line. Formulas are given in References 9 and 12 for calculating Z_{oe} and Z_{oo}. The backward crosstalk voltage shown in Figure 7-15(b) at point 2 is equal to 8% of the incident voltage E_1. Since both lines are active, the crosstalk due to one active line is 4% of E_1 for a spacing of 80 mils. Reference 5 should be consulted if information concerning crosstalk on microstrip lines is desired. There, curves are given from which the backward crosstalk can be predicted. (For example, Figure 10 in Reference 5 may be used to predict the backward crosstalk for Figure 7-15(a) as 11%).

Crosstalk is not ordinarily a problem when using MECL III on microstrip or strip line circuit boards, when line spacings are greater than 30 mils. Crosstalk theory is well described in Reference 11. In it, the mutual inductance and capacitance between two lines are used to determine the crosstalk coefficient. Crosstalk theory is presented in some detail in this handbook in Chapter 4, "System Interconnections". Forwárd crosstalk is normally much smaller than the backward crosstalk on microstrip lines – except for very long lines (>5 feet). Forward crosstalk does not exist at all on strip lines, since they are made with a homogeneous medium, so that the inductively and capacitively induced currents cancel (Reference 10).

The backward crosstalk coefficients for various types of microstrip lines on glass epoxy boards are shown in Figure 7-16 (cf also Reference 5). The backward crosstalk coefficient is equal to:

$$K_B = \frac{1}{4t_{pd}} \left(\frac{L_M}{Z_o} + C_M Z_o \right) \quad , \tag{25}$$

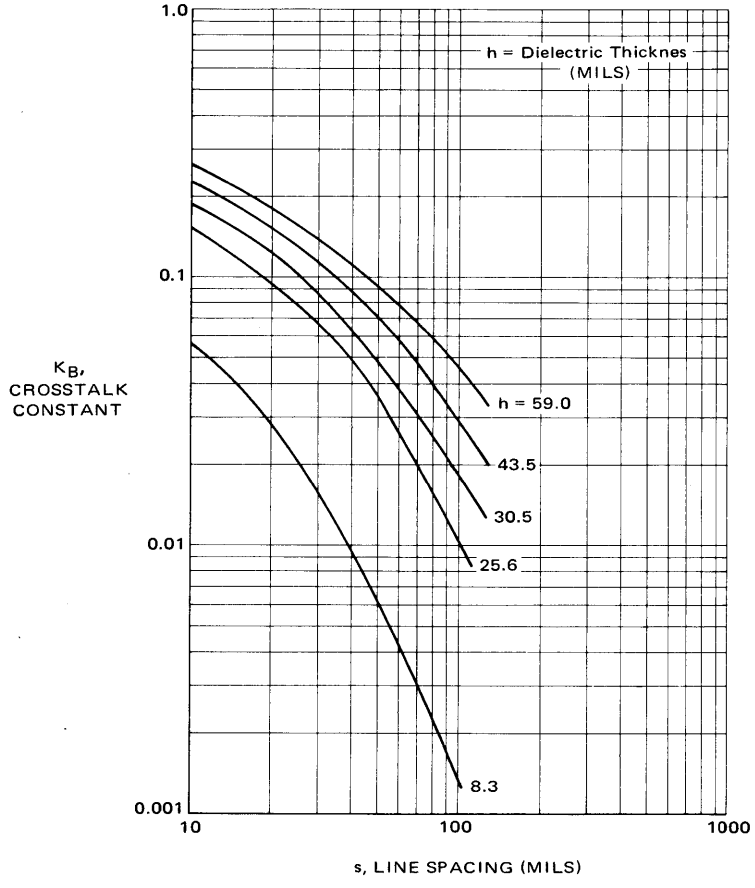
where: L_M = the inductive coupling,

C_M = the capacitive coupling,

t_{pd} = the propagation delay of the line per unit length.

TDR Example 6. The graph data in Figure 7-16 will be used to determine the percent of crosstalk coupling for the circuit of Figure 7-15. From the dimensions of the lines given in Figure 7-15(a), K_B is found to be 0.055 from the graph. This means that if one line (the active line) were driven with a signal, the other line (passive) would have a coupled signal of 5.5% of the amplitude on the active line, in a direction opposite to that of the driving signal. Since both 100 ohm lines are active

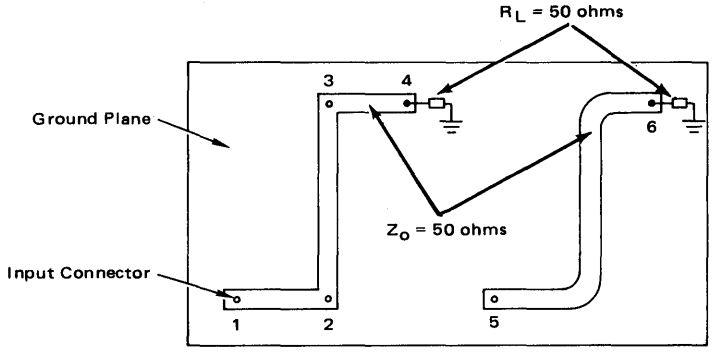
7-16: Backward Crosstalk Coefficient for Microstrip Lines on Glass Epoxy Boards (G-10 Material)



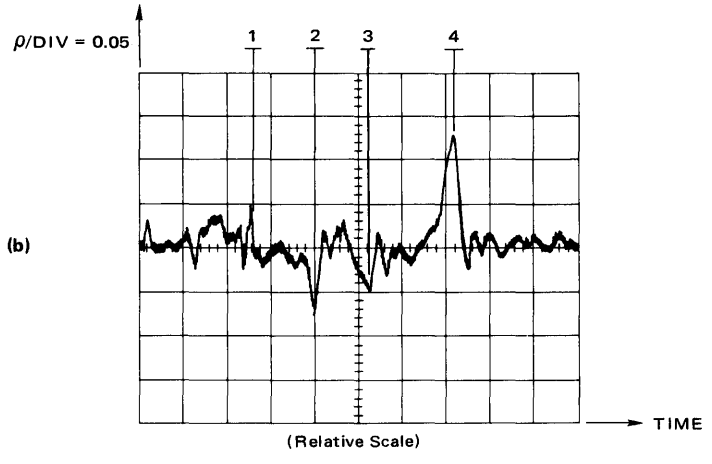
simultaneously, the reflection observed on the TDR is twice as much, or 11%. From Figure 7-15, the actual crosstalk can be seen to be about 8%.

In very high speed systems, the exact shape of a line can be important, if reflections are to be kept to a minimum. The arrangement shown in Figure 7-17(a) has been used to investigate the behavior of two different line shapes. For one line, corners are sharp. This permits the width of the line to be larger at corners than elsewhere. Figure 7-17(b) shows that a -7.5% reflection occurs at point 6 due to the lowered characteristic impedance at the corner. For the other line, the corners are rounded to produce a constant line width. Figure 7-17(c) shows that a constant line impedance exists for the second line. Note that an inductive reflection, as discussed before, does occur at the end of the line due to the inductance of the resistor. In conclusion, it is desirable to have smooth, rounded line edges and constant line widths when designing transmission lines for high speed systems. Resistor leads should be kept short to minimize termination inductance.

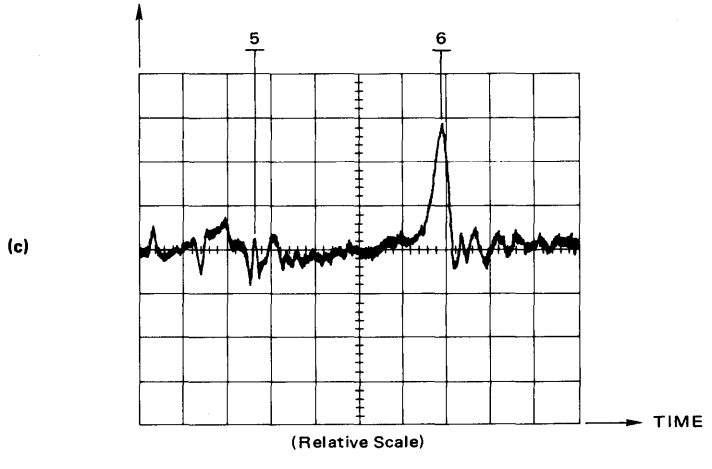
7-17: Reflections Caused by Signal-Line Shape Variations



(a)



(b)



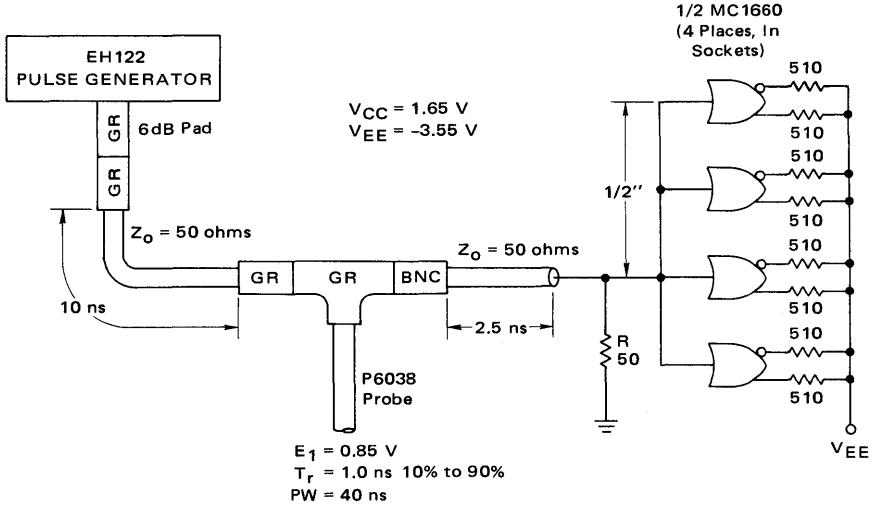
(c)

The Effect of Loading, on a Parallel Terminated Transmission Line

For designing high speed systems it is useful to understand the effects of loading a transmission line with MECL circuit inputs. Some tests were performed to determine the equivalent loading effects of a MECL gate load. The input impedance of the MECL gate is high and may be assumed to be purely capacitive as far as reflections are concerned.

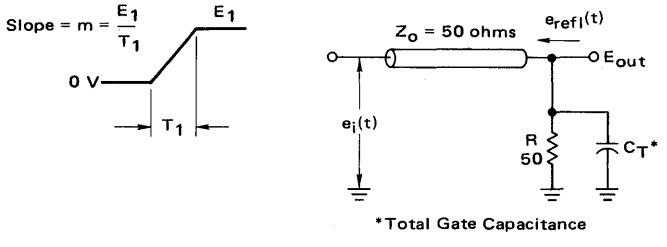
Accurate knowledge of gate input capacitance is necessary to develop accurate loading rules. A test setup, similar to that for a TDR, was used to determine the amount of reflection that occurred when driving four MECL III gates (MC1660L – cf Figure 7-18). The amount of reflection that occurred at the probe was found to

7-18: Test Setup for Measuring the Reflection From Four MECL III Gate Loads



be 275 mV, in a direction indicating it was due to a terminal capacitance, C_T. A formula may be derived so that the amount of this capacitance can be calculated. Figure 7-19 shows the equivalent circuit which will be used for the derivation of

7-19: Circuit for Driving the Maximum Reflected Voltage Due to the Capacitance of the Gate Inputs



such a formula.

The reflection coefficient at the load is:

$$\rho_L(s) = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{\dfrac{R}{sRC_T + 1} - Z_o}{\dfrac{R}{sRC_T + 1} + Z_o} = \frac{(R - Z_o) - sRZ_oC_T}{(R + Z_o) + sRZ_oC_T} \tag{26}$$

From equation 18, the LaPlace transform of the input voltage can be found to be:

$$E_i(s) = \frac{m}{s^2}\left(1 - e^{-T_1 s}\right). \tag{27}$$

The reflected voltage at the load, in LaPlace notation, is:

$$E_{refl}(s) = E_i(s)\rho_L(s) = \frac{-\left(s + \dfrac{Z_o - R}{RZ_oC_T}\right)}{s^2\left(s + \dfrac{Z_o + R}{RZ_oC_T}\right)}\, m\left(1 - e^{-T_1 s}\right). \tag{28}$$

Taking the inverse LaPlace transform yields:

$$e_{refl}(t) = -\left[\frac{2R^2Z_oC_T}{(Z_o + R)^2} + \left(\frac{Z_o - R}{Z_o + R}\right)t - \left(\frac{2R^2Z_oC_T}{(Z_o + R)^2}\right)e^{-\frac{(Z_o + R)}{RZ_oC_T}t}\right] mU(t) +$$

$$\left[\frac{2R^2Z_oC_T}{(Z_o + R)^2} + \left(\frac{Z_o - R}{Z_o + R}\right)(t - T_1) - \left(\frac{2R^2Z_oC_T}{(Z_o + R)^2}\right)e^{-\frac{(Z_o + R)}{RZ_oC_T}(t - T_1)}\right] mU(t - T_1). \tag{29}$$

The maximum reflection occurs at $t = T_1$. Then for $R = Z_o$, we obtain:

$$e_{refl}(t = T_1) = E_{refl\,max} = -\frac{m\,Z_oC_T}{2}\left(1 - e^{-\frac{2T_1}{Z_oC_T}}\right) \tag{30}$$

Equation 30 exhibits a relation between the maximum reflected voltage and the effective capacitance causing reflection, C_T, in the circuit of Figures 7-18 and 7-19. The reflected voltage was measured to be -275 mV and from equation 22, T_1 is found to be 1.25 ns. Thus the total capacitance, obtained from equation 30, is $C_T = 17.2$ pF. Since stray capacitance, C_S, is approximately 4.0 pF, the capacitance

due to the gate loads is the difference between C_T and C_S i.e., 13.2 pF, or 3.3 pF per gate input.

For comparison, an RF vector impedance meter was used to measure the input capacitance of a similar 4 gate setup at a frequency of 50 MHz. The total capacitance measured 20 pF. Since the stray capacitance for this configuration measured 6.5 pF, the capacitance due to the four gate loads is 13.5 pF, or 3.38 pF per gate input. It is felt that the two methods agreed well enough with each other to say that the equivalent load of a MECL III input is 3.3 pF.

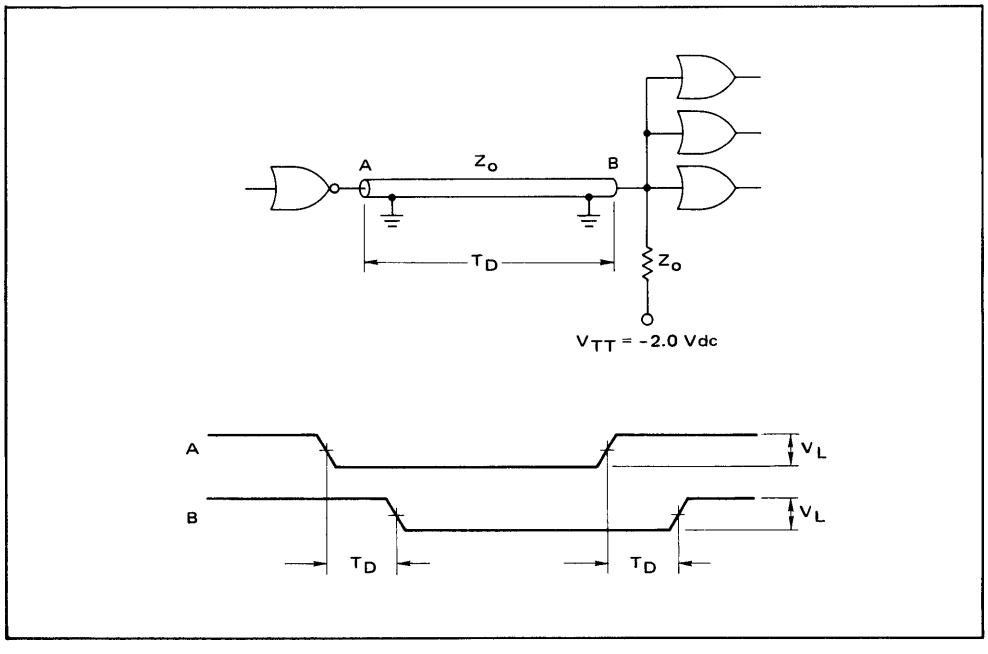
MECL 10K/10KH series elements were also tested. It was found that a MECL 10K/10KH gate input measured 2.9 pF using the RF vector impedance meter. Using the reflection method of Figure 7-18 and equation 30, the capacitance of a gate input was found to be 2.7 pF.

If printed circuit cards are used without sockets, 3.3 pF per MECL III gate input and 2.9 pF per MECL 10K/10KH gate input should be used. These values will be used in later calculations.

It was shown in equations 12 and 13 that the maximum length of an unterminated line (stub length) is a function of loading. Figures 3-13, 3-14, and 3-15 are a tabulation of some values of permissible lengths versus fanout and logic family. However, in most designs it becomes necessary to increase the line length beyond the distances specified in the table. It has been shown that for long lines, $2T_D$ (line) $> t_r$ (pulse), a termination resistor will reduce or eliminate reflections. In a practical situation, a MECL gate driving a transmission line must feed other gates along that line. So it is important to be able to determine the effects of individual gate loads on the line.

There are two ways of placing gates on a parallel terminated transmission line: one is called "distributed" loading, the other "lumped" loading. Figure 7-20 shows an example of a parallel terminated line with a lumped load at the end. The term T_D

7-20: Driving a Parallel Terminated Line



represents the delay of the line. Since a full logic swing is available all along the line, parallel termination permits distributed loading to be placed anywhere along the line.

The change in characteristic impedance of a line caused by gate loads being distributed along the line can be calculated. For a lossless line the characteristic impedance of a transmission line is:

$$Z_o = \sqrt{\frac{L_o}{C_o}} \quad , \tag{31}$$

where L_o is the intrinsic inductance of the line and C_o is the intrinsic capacitance of the line, both per unit length. The MECL gate has a high input impedance so that only the capacitive effect need be considered for ac conditions. The characteristic impedance of a transmission line altered by gate loading, Z'_o, is:

$$Z'_o = \sqrt{\frac{L_o}{C_o + C_d}} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \quad , \tag{32}$$

where Z_o is the original line impedance defined in equation 31 and C_d is the distributed gate capacitance. The propagation delay per unit length of a lossless transmission line is:

$$t_{pd} = \sqrt{L_o C_o} \quad . \tag{33}$$

Rearranging, and using equation 31 gives:

$$t_{pd} = \left(\sqrt{\frac{L_o}{C_o}}\right) C_o = Z_o C_o \quad . \tag{34}$$

Example. An application of the foregoing relationships and rules can be seen in the following design problem. Given: a 68 ohm microstrip line 8 inches long. It is desired to drive four MECL III gate loads spaced equally at 2" intervals along this line. These loads are, of course, "distributed" loads. The microstrip line is on a glass epoxy board which has a dielectric constant, e_r, of 5.0. It is necessary to determine a value for a parallel terminating resistor which will essentially eliminate reflections on the line.

First, the propagation delay of the microstrip line can be found using the relation from Chapter 3:

$$t_{pd} = 1.017 \sqrt{0.475\, e_r + 0.67} \text{ ns/ft} = 1.77 \text{ ns.ft} = 0.148 \text{ ns/in} \quad , \tag{35}$$

in this case. Using equation 34, the line capacitance, C_o is found to be:

$$C_o = \frac{0.148}{68} = 2.18 \text{ pF/in.}$$

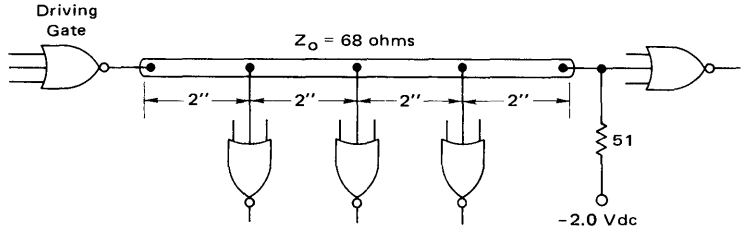
Four MECL III gate loads are equivalent to a load capacitance of 13.2 pF which is distributed along 8 inches of line. Therefore, C_d = 13.2 pF/8 in. = 1.65 pF/in. Substituting these values into equation 32 gives:

$$Z_o' = \frac{68}{\sqrt{1 + \frac{1.65}{2.18}}} = 51.5 \text{ ohms.}$$

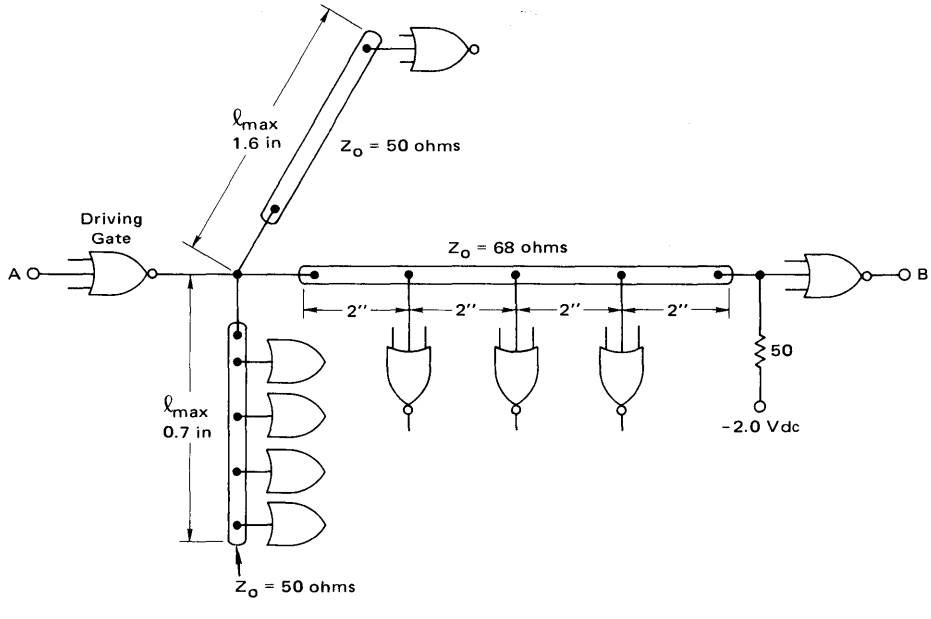
Thus, a 51 ohm termination resistor would be acceptable for terminating the 8 inch 68 ohm microstrip line with four distributed MECL III gates. The resulting circuit is shown in Figure 7-21.

The driving gate shown in Figure 7-21, besides driving the long transmission line, can also drive many lines (no limit) as long as the length of each stub does not exceed the limits of Figures 3-13, 3-14, or 3-15. For instance, if a 50 ohm microstrip line were used with MECL III to connect the driving gate to 1 gate load in one direction, and to four gate loads in another direction (in addition to the loads shown in Figure 7-21), then from Figure 3-15 the maximum permissible stub lengths are 1.6 and 0.7 inches, respectively (of Figure 7-22). It should be noted that the four

7-21: Example Illustrating Distributed Loading



7-22: MECL III Gate Driving a Long Transmission Line with Distributed Loads, and Short Stubs at the Driving Source



gates on the stub (ℓ_{max} = 0.7 inch) could be lumped at the end of that line, without the need for any other changes.

In order to determine the amount of reflection which can be tolerated on a line, the following development is presented. Reflection is, of course, caused by gate loading which produces a change in the impedance on a section of the transmission line. The equations to be developed use distributed line theory – an approximate method, but one which gives very accurate results, as verified in Reference 11.

The reflection coefficient given in equation 3 can be revised to take into account the reflection due to the altered characteristic impedance produced by loading:

$$\rho = \frac{Z_o' - Z_o}{Z_o' + Z_o} .$$

Substituting the expression for Z_o' given in equation 32 yields:

$$\rho = \frac{1 - \sqrt{1 + \frac{C_d}{C_o}}}{1 + \sqrt{1 + \frac{C_d}{C_o}}} . \tag{36}$$

From this equation, it is possible to find the maximum load capacitance that can be distributed or lumped on a length of transmission line. Further, the length of transmission line for distributing loads will be assumed to be the stub length defined in equations 12 and 13. This length of line will limit reflection discontinuities caused by differences between distributed and lumped loads. However a rule is needed which can be stated for a particular value of transmission line, to specify a limit for the number of gate loads distributed or lumped along an arbitrary length of line.

For a maximum reflection of 20% (ρ = -0.20) equation 36 may be solved for the ratio of C_d/C_o, giving:

$$\frac{C_d}{C_o} = 1.25 . \tag{37}$$

Since C_d is the distributed gate load capacitance per unit line length, it may be written that:

$$C_d = \frac{C_D}{\ell_{max}} , \tag{38}$$

where C_D is the total gate load capacitance. Substituting into equation 37 yields:

$$\frac{C_D}{C_o} = 1.25\, \ell_{max} . \tag{39}$$

For a 50 ohm microstrip transmission line, on a glass epoxy board, with MECL III gates, with C_o = 2.96 pF/in, and t_r = 1.1 ns, equation 12 may be used to find $\ell_{max} \approx 2.5$ inches. Then substituting into equation 39 and solving: C_D = 9.2 pF. This means that up to 9.2 pF can be distributed or lumped along any 2.5 inches of 50 ohm microstrip line using MECL III. Two MECL III gate loads can be used along any 1.8 inches of line for a carefully laid out board, or two MECL III gate loads and 2.6 pF of stray capacitance can be distributed or lumped along any 2.5 inches of line.

For a 50 ohm strip line on a glass epoxy board and using MECL III gates, with C_o = 3.77 pF/in and t_r = 1.1 ns, equations 13 and 39 may be used to find $\ell_{max} \approx 2.0$ inches. Then substituting into equation 39 and solving, C_D = 9.4 pF. This means that up to 9.4 pF can be distributed or lumped along any 2.0 inch portion of 50 ohm strip line when using MECL III gates. If 3.3 pF per gate input is used, then from equation 39 two gate loads can be lumped or distributed along any 1.4 inch portion of a 50 ohm strip line.

It is seen from these calculations that strip line has an advantage over microstrip: it can be used for driving more gate loads per unit length than microstrip, granting the same amount of reflection in each case. This is due to strip line having a larger capacitance per unit length. Figure 7-23 gives values for the maximum capacitance that can be lumped or distributed over any length (ℓ_{max}) of line for MECL III, MECL 10K/10KH and high speed MECL II.

As an example of how Figure 7-23 can be used, suppose 68 ohm microstrip lines are to be used with the MECL 10K series. From the Figure, 21 pF of capacitance of five gate loads can be lumped or distributed over any 7.7 inch portion of the line. The rise times shown in the figure are characteristic of the particular logic family and were used in the calculations to obtain the data.

7-23: Maximum Capacitance That Can Be Lumped or Distributed Over a Length of Terminated Transmission Line ℓ_{max}.

	CHARACTERISTIC IMPEDANCE OF TRANSMISSION LINE						
	STRIPLINE (e_r = 5.0)			MICROSTRIP (e_r = 5.0)			COAX (e_r = 2.2)
	50 Ω	68 Ω	90 Ω	50 Ω	68 Ω	90 Ω	50 Ω
MECL III							
C_{max} (pF)	9.4	6.9	5.2	9.2	6.8	5.1	9.4
ℓ_{max} (in)	2.0	2.0	2.0	2.5	2.5	2.5	3.0
t_r (ns) = 1.1							
MECL 10K							
C_{max} (pF)	29	21.5	16.2	28.6	21	15.9	29
ℓ_{max} (in)	6.2	6.2	6.2	7.7	7.7	7.7	9.3
t_r (ns) = 3.5							
MECL II½							
C_{max} (pF)	16.4	12.0	9.1	16.2	11.9	9.0	16.5
ℓ_{max} (in)	3.5	3.5	3.5	4.4	4.4	4.4	5.3
t_r (ns) = 2.0							
MECL 10KH							
C_{max} (pF)	15.1	11.0	8.4	14.8	10.9	8.2	15.0
ℓ_{max} (in)	3.2	3.2	3.2	4.0	4.0	4.0	4.8
t_r (ns) = .8							

Analysis: Series Terminated Lines Compared to Parallel Terminated Lines

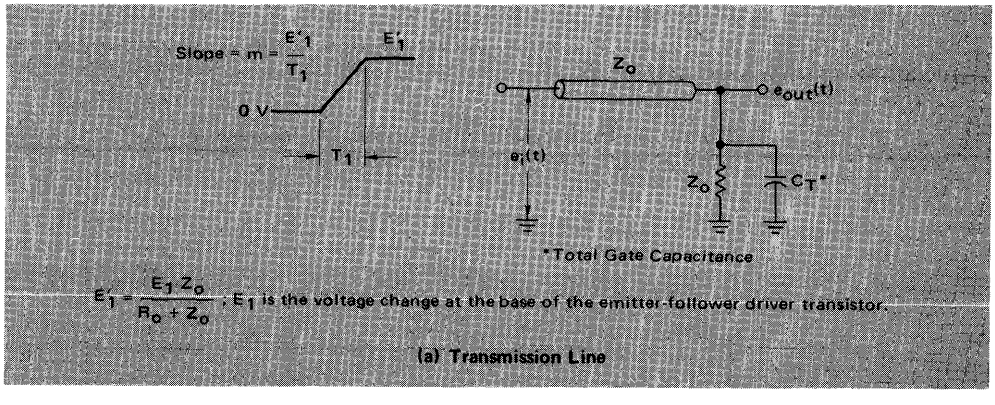
The propagation delay increase due to gate loading when a line is series terminated is about twice as large as for a comparable parallel terminated line. Equation 11 gives a fairly close approximation for the propagation delay of a parallel terminated line with loading. This equation was:

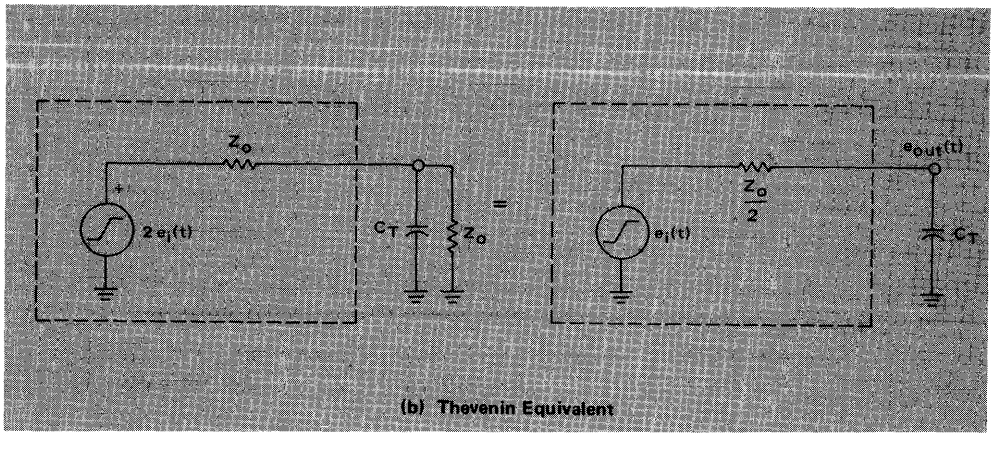
$$t'_{pd} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} \quad . \tag{11}$$

The output waveform at the end of a series terminated line or at the end of a parallel terminated line can be derived from an equivalent circuit using Thevenin's Theorem, assuming the line is long ($2T_D >> t_r$). Figure 7-24(a) shows a parallel terminated transmission line circuit, along with the waveform driving the line.

The equivalent open circuit voltage of the line is twice the input voltage and the Thevenin resistance is the impedance of the open line at the load looking toward the source. The Thevenin equivalent for a parallel terminated line is shown in Figure

7-24: Parallel Terminated Transmission Line, and its Thevenin Equivalent



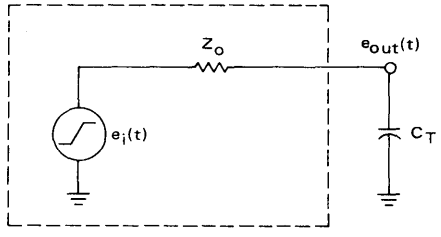


7-24(b). Figure 7-25 shows the Thevenin equivalent for a series terminated line. Note that the impedance (Z_O) of the series terminated line is twice as large as that for the parallel terminated line. A general equation can be derived for the output voltage assuming the impedance in the circuit to be R. Then a substitution for R will give the equations for both types of lines.

Writing the equation around either Thevenin equivalent loop:

$$e_i(t) = iR + \frac{1}{C_T} \int_o^t i\, dt \quad . \tag{40}$$

7-25: Thevenin Equivalent of Series Terminated Transmission Line



But also:

$$e_i(t) = mt\, U(t) - m(t - T_1)\, U(t - T_1) \quad . \tag{41}$$

Equating the equations and taking the LaPlace transform of both sides gives:

$$\frac{m}{s^2} - \frac{m}{s^2} e^{-T_1 s} = RI(s) + \frac{I(s)}{C_T s} = \left(R + \frac{1}{C_T s} \right) I(s) \quad . \tag{42}$$

But:

$$e_{out}(t) = \frac{1}{C_T} \int_o^t idt \quad \text{or} \quad E_{out}(s) = \frac{I(s)}{C_T s} \quad . \tag{43}$$

Therefore:

$$\frac{m}{s^2} - \frac{m}{s^2} e^{-T_1 s} = \left(R + \frac{1}{C_T s} \right) C_T s\, E_{out}(s) \quad . \tag{44}$$

Solving for $E_{out}(s)$:

$$E_{out}(s) = \frac{\frac{m}{s^2}\left(1 - e^{-T_1 s}\right)}{C_T s\left(R + \frac{1}{C_T s}\right)}, \tag{45}$$

which reduces to:

$$E_{out}(s) = \frac{\frac{m}{RC_T}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{RC_T}\right)} \quad . \tag{46}$$

Taking the inverse LaPlace transform yields:

$$e_{out}(t) = \left[mRC_T\left(e^{\frac{-t}{RC_T}} - 1\right) + mt\right] U(t) - \left[mRC_T\left(e^{\frac{-(t - T_1)}{RC_T}} - 1\right) + m(t - T_1)\right] U(t - T_1) \; . \tag{47}$$

Equation 47 defines the output voltage for a series terminated transmission line when $R = Z_o$; it defines the output voltage for a parallel terminated transmission line when $R = Z_o/2$.

From equation 47 the equation for the series terminated line can be written:

$$e_{out}(t) = \frac{E_1' Z_o C_T}{T_1}\left(e^{\frac{-t}{Z_o C_T}} - 1\right) + \frac{E_1'}{T_1}(t) \quad \text{for} \quad t \leq T_1 \; , \tag{48}$$

and:

$$e_{out}(t) = \frac{E_1'}{T_1} Z_o C_T \left(1 - e^{\frac{T_1}{Z_o C_T}}\right) e^{\frac{-t}{Z_o C_T}} + E_1' \quad \text{for} \quad t > T_1 \; , \tag{49}$$

where E'_1 is defined in Figure 7-24. The equations for the parallel terminated line can also be written:

$$e_{out}(t) = \frac{E'_1 Z_o C_T}{2T_1}\left(e^{\frac{-2t}{Z_o C_T}} - 1\right) + \frac{E'_1}{T_1}(t) \quad \text{for } t \leq T_1 \,. \tag{50}$$

and:

$$e_{out}(t) = \frac{E'_1 Z_o C_T}{2T_1}\left(1 - e^{\frac{2T_1}{Z_o C_T}}\right) e^{\frac{-2t}{Z_o C_T}} + E'_1 \quad \text{for } t > T_1 \,. \tag{51}$$

If the input voltage is assumed to be a step function, then the equation for the output voltage for a series terminated line can be written as:

$$e_{out}(t) = E'_1\left(1 - e^{\frac{-t}{Z_o C_T}}\right) \,, \tag{52}$$

and for a parallel terminated line:

$$e_{out}(t) = E'_1\left(1 - e^{\frac{-2t}{Z_o C_T}}\right) . \tag{53}$$

To derive the equation for the additional propagation delay due to gate loading at the end of the line, equations 52 and 53 will be used. A more exact equation can be derived using equations 48 through 51 but the analysis is more difficult due to the complexity of the equations. Letting $e_{out}(t) = 0.5\, E'_1$ and solving for t, we obtain a propagation delay time of:

$$t_{pd} = 0.7\, Z_o C_T \quad \text{for series termination,} \tag{54}$$

and:

$$t_{pd} = 0.35\, Z_o C_T \quad \text{for parallel termination.} \tag{55}$$

These additional line delays should be added to the existing physical line delay as expressed in equation 34 to obtain total system line delay. To derive the equation

for the output rise time, t_{ro}, knowing the input rise time, t_{ri}, equations 49 and 51 will be used. The output rise time is defined as the time it takes for the output voltage to travel from 10 to 90% of its final value. T_1 is defined as:

$$T_1 \approx 1.2\, t_{ri} \ . \tag{56}$$

Substituting into Equation 49, rearranging, and taking the natural log of both sides, the output rise time at the end of the transmission line is obtained:

$$t_{ro} = Z_o C_T \ln \left[\frac{Z_o C_T}{0.18\, t_{ri}} \left(\frac{1.2 t_{ri}}{e^{Z_o C_T}} - 1 \right) \right], \quad \text{for series termination.} \tag{57}$$

Doing the same thing with equation 51:

$$t_{ro} = \frac{Z_o C_T}{2} \ln \left[\frac{Z_o C_T}{0.36\, t_{ri}} \left(\frac{2.4 t_{ri}}{e^{Z_o C_T}} - 1 \right) \right], \quad \text{for parallel termination.} \tag{58}$$

Equations 56 and 57 may also be used to solve for the output fall time by substituting the input fall time, t_{fi}, in place of t_{ri}.

Example. An example will be shown to illustrate the use of equations 54 through 58 using MECL 10K gates. Figure 7-26(a) and (b) shows comparable setups for series and parallel termination. The load gates at point B were placed in sockets. The total capacitance at point B is C_T = 20 pF which takes into account the gate capacitances, socket capacitances, as well as interconnect and stray capacitances. The propagation delay due to the transmission line from A to B is 1.75 ns. The rise and fall times at point A, due to the MECL 10K driving gate, are t_{ri} = 3.5 ns, and t_{fi} = 2.8 ns. From equation 54, the propagation delay increase due to the series termination is: (0.7) (50 ohms) (20 pF) = 0.7 ns. From equation 55, the propagation delay due to the parallel terminations is half as much, 0.35 ns. Therefore, the total propagation delay from point A to B is 2.45 ns for series termination, and 2.1 ns for parallel termination.

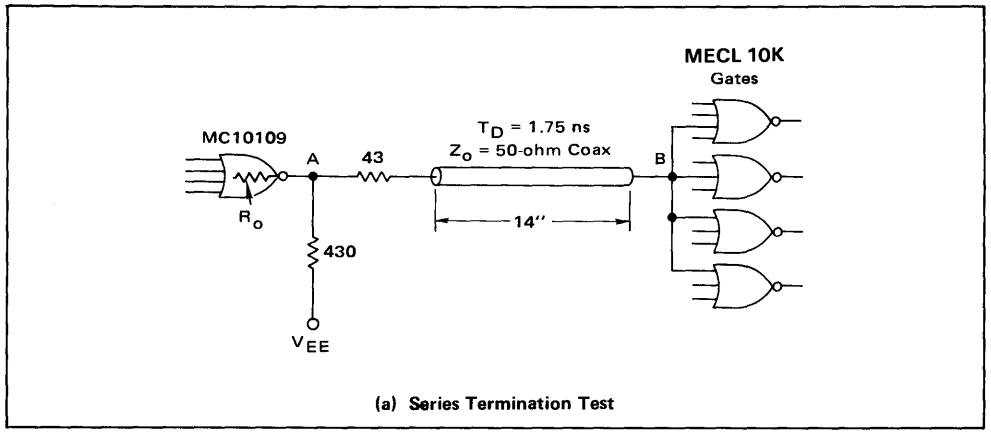
The rise and fall times at point B can be calculated from equations 56, 57, and 58. The mathematical 10 to 90% rise time at point B is 4.65 ns for series termination, versus 4.1 ns for parallel termination. The fall time at point B is 4 ns for series termination versus 3.35 ns for parallel termination. Measured test results agreed closely with the calculated values.

Equation 11 could have been used to calculate the propagation delay from A to B for the parallel termination arrangement. Solving for t'_{pd}:

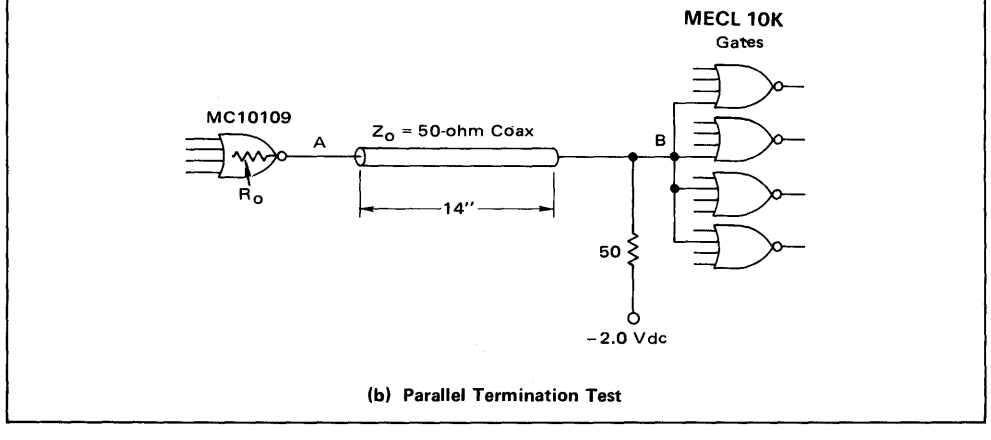
$$t'_{pd} = 1.75 \text{ ns} \sqrt{1 + \frac{20 \text{ pF}}{35 \text{ pF}}} = 2.2 \text{ ns} \ ,$$

which is very close to the value of 2.1 ns that was calculated using equation 54.

7-26: Test Setups for Comparison of Propagation Delays from A to B, and the Rise and Fall Times at B



(a) Series Termination Test



(b) Parallel Termination Test

Since the propagation delay increase is twice as much for a series terminated line as for a parallel terminated line, an equation similar to equation 11 can be derived. The propagation delay of a series terminated line can be written as:

$$t'_{pd} = t_{pd}\left[2\left(\sqrt{1+\frac{C_T}{C_o}}-1\right)+1\right], \qquad (59)$$

where t'_{pd} is the modified propagation delay of the line, t_{pd} is the original propagation delay of the line, C_T is the total capacitance at the end of the line, and C_o is the intrinsic capacitance of the transmission line.

The effective characteristic impedance of a transmission line decreases with capacitance at the end of the series terminated line, but only half as much as for a parallel terminated line (cf equation 32). The characteristic impedance due to

loading of a series terminated transmission line can be written:

$$Z_o' = \frac{2 Z_o}{\sqrt{1 + \frac{C_T}{C_o} + 1}} = R_S + R_o \qquad (60)$$

This means that the series terminating resistor should be changed in the proportion indicated by equation 60 when the capacitance at the end of the line exceeds the value of capacitance given in Table 7-23. Equation 60 has been verified in the laboratory as valid for heavy loading conditions. If the resistor, R_S, is not altered according to equation 60, increased propagation delays will result from underdamping.

Furthermore, if the amount of loading at the end of a series terminated line is more than that shown in Table 7-23, then the emitter pulldown resistor, R_E, should be lower than the value given in equation 61 for the maximum pulldown resistor value (Chapter 3). The maximum value of R_E as stated in Chapter 3 is:

$$R_{E(max)} = \frac{10 Z_o - R_S}{n} . \qquad (61)$$

The reason that the pulldown resistor should be lowered is that the reflection returning to the source contains a short positive component associated with the slower fall rate of the negative-going signal (due to capacitance loading). Thus, the output transistor will turn off due to this momentary positive reflection if a value given by equation 61 is used. The value of R_E should be chosen so that the output transistor of the driving gate is furnishing enough current to supply the maximum reflection without switching off. The maximum reflection on a series terminated line, due to capacitance, is +0.4 volts. Therefore, the value of R_E should be reduced enough so that the output transistor will be able to supply an additional current of $0.4/Z_o$. A modified emitter pulldown resistor equation can be written as:

$$R'_{E(max)} = \frac{3.6}{\frac{3.6}{R_{E\,max}} + \frac{0.4}{Z_o}} , \qquad (62)$$

where $R_{E\,(max)}$ is defined in equation 61.

There is no limit (due to reflections) on the amount of gate loading that can be placed at the end of a series terminated line, as long as equation 60 is used to determine the proper series terminating resistor. All reflections will be terminated at the driving end if the proper value of R_E is chosen with equation 61 or 62. This is true even though the amount of reflection is twice as much for a series terminated line as it is for a parallel terminated one.

The maximum loading for a parallel terminated transmission line is defined in Figure 7-23. There is no limit to the amount of distributed loading that can be placed on the line, as long as equation 32 is used to choose the terminating resistor. In actual practice, there seems to be no limit to the amount of lumped loading that is placed at the end of a parallel terminated line as long as the terminating resistor is chosen this way. This is true as long as there are no other gates stubbed off the line.

For reference purposes, the equations for the reflection that is sent back to the driving source, with lumped loading at the end of either a series terminated line or a parallel terminated line, can be derived from equations 48 and 50 as follows:

$$\text{percent of maximum reflection} = \frac{e_{out}(t) - E'_1}{E'_1} \qquad \text{at } t = T_1 \quad . \quad (63)$$

Therefore, the maximum reflection due to lumped loading at the end of a series terminated line is:

$$\text{percent of maximum reflection} = \frac{Z_o C_T}{T_1} \left(e^{-\frac{T_1}{Z_o C_T}} - 1 \right) , \quad (64)$$

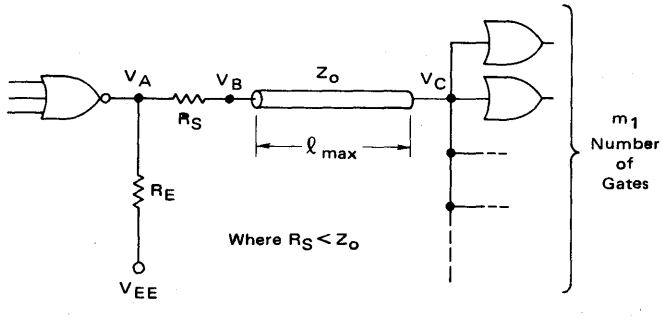
and for lumped loading at the end of a parallel terminated line:

$$\text{percent of maximum reflection} = \frac{Z_o C_T}{2T_1} \left(e^{\frac{-2T_1}{Z_o C_T}} - 1 \right) . \quad (65)$$

Analysis of Series Damping Terminations

A series damped line is very similar to a series terminated line with the exceptions being the line length and the value of the series damping resistor, R_S. The resistor is normally much smaller than the characteristic impedance of the line, Z_o. If $R_S = 0$, then an open line exists for which the maximum length is defined in Figures 3-13, 3-14, or 3-15. If a small value resistor, R_S, is placed in the line, a longer line length is possible. An example of series damping is shown in Figure 7-27

7-27: Series Damping Termination



where the voltage change at point B is defined in Chapter 3 as,

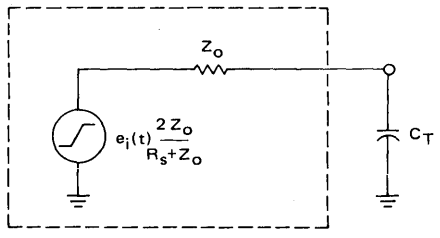
$$\Delta V_B = \Delta V_{INT} \cdot \frac{Z_o}{R_S + R_o + Z_o} \quad . \tag{66}$$

Series damping is primarily used where the characteristic impedance varies – as in backplane wiring when line lengths must be longer than those specified in Figures 3-13 through 3-15. A disadvantage of series damping is that distributed loading cannot be used. A propagation delay slightly slower than for parallel termination also results. Parallel fanout can be used as shown in Figure 3-18.

Figures 3-22, and 3-23, described in Chapter 3, show the minimum values for R_S for any line length, corresponding to specified limits of undershoot and overshoot. These figures were generated by a computer program based on the equations and calculations presented in the following pages. These calculations show how the output voltage from series-damped transmission lines may be derived.

The Thevenin equivalent circuit for a series damped transmission line is shown in Figure 7-28. Note that the circuit is similar to the equivalent circuit for a series terminated line except for the amplitude of the voltage waveform.

7-28: Thevenin Equivalent of a Series Damped Transmission Line



$$\text{Slope} = m = \frac{E'_i}{T_1}$$

$$\text{Where } E'_i = \frac{2Z_oE_1}{R_o+R_s+Z_o}$$

C_T = Total Load Capacitance

The equations for the output voltage from a series terminated line were derived previously (equations 48 and 49). Since the amplitude has been modified by the factor $(2Z_o/R_o + R_S + Z_o)$, a simple substitution will define the output voltage at the load. The output voltage for a series damped line can be written as:

$$e_{out}(t) = \frac{2Z_oE_1}{R_o + R_S + Z_o}\left[\frac{Z_oC_T}{T_1}\left(e^{\frac{-t}{Z_oC_T}} - 1\right) + \frac{t}{T_1}\right]$$

$$\text{for } t \leq T_1 \ , \tag{67}$$

and:

$$e_{out}(t) = \frac{2\,Z_o E_1}{R_o + R_S + Z_o}\left[\frac{Z_o C_T}{T_1}\left(1 - e^{\frac{T_1}{Z_o C_T}}\right)e^{\frac{-t}{Z_o C_T}} + 1\right]$$

$$\text{for } t > T_1 \ , \tag{68}$$

where E_1 is the voltage change at the base of the output emitter follower in the driving gate.

If the input voltage is assumed to be a step function, the equation for the output voltage from a series damped line becomes:

$$e_{out}(t) = \frac{2Z_o E_1}{R_o + R_S + Z_o}\left(1 - e^{\frac{-t}{Z_o C_T}}\right). \tag{69}$$

The additional propagation delay due to gate loading can be found by using equation 69, letting $e_{out}(t) = 0.5\,E_1$, and then solving for t. The increase in the line propagation delay which results, is:

$$t_{pd} = -\,Z_o C_T \ln\left(\frac{3Z_o - R_S - R_o}{4Z_o}\right). \tag{70}$$

The exact reflected voltage will now be derived by a method similar to that used previously in deriving equation 19. The reflection coefficient at the load is:

$$\rho_L(s) = \frac{\frac{1}{sC_T} - Z_o}{\frac{1}{sC_T} + Z_o} = \frac{1 - sC_T Z_o}{1 + sC_T Z_o} = \frac{-\left(s - \frac{1}{Z_o C_T}\right)}{s + \frac{1}{Z_o C_T}} \ . \tag{71}$$

The input voltage at point B in Figure 7-27 is:

$$e_i(t) = mtU(t) - m(t - T_1)\,U(t - T_1) \ , \tag{72}$$

where:

$$m = \frac{Z_o E_1}{(R_o + R_S + Z_o)\,T_1} = \text{slope} \ .$$

Here R_o is the output impedance of the driving gate; R_S is the series damping resistor; Z_o is the characteristic impedance of the transmission line; E_1 is the voltage change at the base of the output emitter follower of the gate at point A in Figure 7-27; and $T_1 = 1.2\, t_r$ where t_r is the 10 to 90% rise time of the voltage at point A.

Taking the LaPlace transform of equation 72 gives:

$$E_i(s) = \frac{m}{s^2}\left(1 - e^{-T_1 s}\right) . \tag{73}$$

The first reflected voltage waveform at the load at time T_D (point C in Figure 7-27) due to the input voltage is (in LaPlace notation):

$$E_{refl\ 1}(s) = E_i(s)\,\rho_L(s) = \frac{-\left(s - \frac{1}{Z_o C_T}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)}\, m\left(1 - e^{-T_1 s}\right) . \tag{74}$$

The second reflected voltage waveform at the load occurs a time $2T_D$ later and can be written as:

$$E_{refl\ 2}(s) = E_{refl\ 1}(s)\,\rho_S\,\rho_L(s) = \frac{\left(s - \frac{1}{Z_o C_T}\right)^2 \rho_S}{s^2\left(s + \frac{1}{Z_o C_T}\right)^2}\, m\left(1 - e^{-T_1 s}\right) , \tag{75}$$

where:

$$\rho_S = \frac{R_o + R_S - Z_o}{R_o + R_S + Z_o} . \tag{76}$$

The third reflected voltage waveform at the load is:

$$E_{refl\ 3}(s) = E_{refl\ 1}(s)\,\rho_S{}^2\,\rho_L{}^2(s) = \frac{-\left(s - \frac{1}{Z_o C_T}\right)^3 \rho_S{}^2\, m\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)^3} . \tag{77}$$

So the n^{th} reflected voltage waveform at the load is:

$$E_{refl\,(n)}(s) = E_{refl\,1}\,\rho_S^{n-1}\,\rho_L^{n-1}(s)$$

$$= \frac{(-1)^n \left(s - \frac{1}{Z_o C_T}\right)^n \rho_S^{n-1}\, m \left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)^n} \quad . \qquad (78)$$

The output voltage at the end of the line can be derived by using equations 73 through 78. The output voltage, E_{o1}, due to the input voltage waveform and the first reflection is:

$$E_{o1}(s) = E_i(s) + E_{refl\,1}(s) = E_i(s)\left(1 + \rho_L(s)\right)$$

$$= \frac{\frac{2m}{Z_o C_T}\left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)} \quad , \qquad (79)$$

It should be noted that equations 79 and 46 are equal (though they were derived differently), when $R = Z_o$. At first glance it may appear that equation 79 is twice the value of equation 46, but the apparent discrepancy is resolved by noting that m has been defined differently for each equation.

The output voltage, E_{o2}, due to the first reflected voltage waveform returning from the driving source will be:

$$E_{o2}(s) = \rho_S E_{refl\,1}(s) + E_{refl\,2}(s) = E_i(s)\,\rho_S\,\rho_L(s)\left(1 + \rho_L(s)\right)$$

$$= \frac{\frac{-2m}{Z_o C_T}\rho_S \left(s - \frac{1}{Z_o C_T}\right)\left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)^2} \cdot U(t - 2T_D) \quad . \qquad (80)$$

Similarly, the output voltage, E_{o3}, due to the second reflected voltage waveform returning from the driving source is:

$$E_{o3}(s) = E_i(s)\,\rho_S^2\,\rho_L^2(s)\left(1 + \rho_L(s)\right),$$

or:

$$E_{o3}(s) = \frac{\frac{2m}{Z_o C_T}\rho_S^2 \left(s - \frac{1}{Z_o C_T}\right)^2 \left(1 - e^{-T_1 s}\right)}{s^2 \left(s + \frac{1}{Z_o C_T}\right)^3} \cdot U\left(t - 4T_D\right) . \qquad (81)$$

Finally, the n^{th} output voltage waveform will be:

$$E_{on}(s) = E_i(s)\,\rho_S^{n-1}\,\rho_L^{n-1}(s)\left(1 + \rho_L(s)\right)$$

$$= \frac{(-1)^{n-1}\left(\frac{2m}{Z_o C_T}\right)\rho_S^{n-1}\left(s - \frac{1}{Z_o C_T}\right)^{n-1}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)^n} \cdot$$

$$U\left(t - 2(n-1)\,T_D\right); \qquad (82)$$

therefore, the general equation for the output voltage at the end of the line (point C in Figure 7-27) can be formulated as a summation of the individual reflected voltage components:

$$E_{out}(s) = E_{o1}(s) + E_{o2}(s) + E_{o3}(s) + \ldots + E_{on}(s) + \ldots$$

$$= \sum_{n=1}^{\infty} \left[\frac{(-1)^{n-1}\left(\frac{2m}{Z_o C_T}\right)\rho_S^{n-1}\left(s - \frac{1}{Z_o C_T}\right)^{n-1}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_o C_T}\right)^n} \cdot \right.$$

$$\left. U\left(t - 2(n-1)\,T_D\right) \right] . \qquad (83)$$

The inverse LaPlace transforms for equations 79, 80, and 81 can be found in standard tables. The inverses can be written to take into account the time delays the following way.

The inverse LaPlace transform of equation 79 is:

$$e_{o1}(t) = \mathcal{L}^{-1}\left[\frac{\frac{2m}{Z_oC_T}\left(1 - e^{-T_1 s}\right)}{s^2\left(s + \frac{1}{Z_oC_T}\right)}\right]$$

$$= 2mZ_oC_T\left(e^{\frac{-t}{Z_oC_T}} + \frac{t}{Z_oC_T} - 1\right) \cdot U(t)$$

$$- 2mZ_oC_T\left(e^{\frac{-(t - T_1)}{Z_oC_T}} + \frac{t - T_1}{Z_oC_T} - 1\right) \cdot U(t - T_1). \qquad (84)$$

Likewise, the inverse transform of equation 80 becomes:

$$e_{o2}(t) = 2m\rho_S Z_oC_T\left[\left(-3 + \frac{t - 2T_D}{Z_oC_T}\right) + \left(3 + \frac{2(t - 2T_D)}{Z_oC_T}\right)\cdot e^{-\left(\frac{t - 2T_D}{Z_oC_T}\right)}\right] \cdot U(t - 2T_D) - 2m\rho_S Z_oC_T \cdot$$

$$\left[\left(-3 + \frac{t - 2T_D - T_1}{Z_oC_T}\right) + \left(3 + \frac{2(t - 2T_D - T_1)}{Z_oC_T}\right)\cdot e^{-\left(\frac{t - 2T_D - T_1}{Z_oC_T}\right)}\right] \cdot U(t - 2T_D - T_1) \; . \qquad (85)$$

Finally, the inverse transform of equation 81 produces:

$$e_{o3}(t) = 2m\rho_S^2 Z_o C_T \left[-5 + \frac{t - 4T_D}{Z_o C_T} + \left(5 + \frac{4(t - 4T_D)}{Z_o C_T} + \frac{2(t - 4T_D)^2}{(Z_o C_T)^2} \right) \cdot e^{\frac{-(t - 4T_D)}{Z_o C_T}} \right] \cdot U(t - 4T_D) -$$

$$2m\rho_S^2 Z_o C_T \left[-5 + \frac{t - 4T_D - T_1}{Z_o C_T} + \left(5 + \frac{4(t - 4T_D - T_1)}{Z_o C_T} + \frac{2(t - 4T_D - T_1)^2}{(Z_o C_T)^2} \right) \cdot e^{\frac{-(t - 4T_D - T_1)}{Z_o C_T}} \right] \cdot U(t - 4T_D - T_1) \quad . \quad (86)$$

A general form equation can be established for $e_{o\,(n)}(t)$ as an extension of the preceeding equations. Such a general equation can then be used to obtain a general relationship for $e_{out}(t)$ derived from equation 83.

However, for our purposes, the output voltage needs to be defined only for a period of time long enough to determine the maximum amount of overshoot and undershoot. The following can be written for the first three reflections (a sufficient time interval):

$$e_{out}(t) = \sum_{n=1}^{3} \left\{ 2m\rho_S^{n-1} Z_o C_T \left[\left(\frac{t - 2T_D(n-1)}{Z_o C_T} - (2n-1) \right) \cdot \left(1 - e^{\frac{t - 2T_D(n-1)}{Z_o C_T}} \right) + \left((n-1) e^{\frac{-\left(t - 2T_D(n-1)\right)}{Z_o C_T}} \right) \cdot \left(\frac{2\left(t - 2T_D(n-1)\right)}{Z_o C_T} + (n-2)\left(\frac{t - 2T_D(n-1)}{Z_o C_T} \right)^2 \right) \right] \cdot U\left(t - 2(n-1)T_D\right) \right\}$$

$$-\sum_{n=1}^{3}\left\{2m\rho_S^{n-1}\,Z_oC_T\left[\left(\frac{t-2T_D(n-1)-T_1}{Z_oC_T}-(2n-1)\right)\cdot\left(1-e^{-\frac{\left(t-2T_D(n-1)-T_1\right)}{Z_oC_T}}\right)+\left((n-1)\,e^{-\frac{\left(t-2T_D(n-1)-T_1\right)}{Z_oC_T}}\right)\cdot\left(\frac{2\left(t-2T_D(n-1)-T_1\right)}{Z_oC_T}+(n-2)\left(\frac{t-2T_D(n-1)-T_1}{Z_oC_T}\right)^2\right)\right]\cdot U\left(t-2(n-1)T_D-T_1\right)\right\}\,,\quad \text{for } t<6T_D\,, \tag{87}$$

where:

$$m=\frac{Z_oE_1}{(R_o+R_S+Z_o)\,T_1}\,,$$

$$T_1=1.2\,t_r\,,$$

and t_r is the 10 to 90% rise time of the voltage at point A in Figure 7-27. Figs. 3-13 through 3-15 are generated with a computer program using an extension of equation 87 in which the first 7 reflections were considered.

An extension of equation 87 was used in generating Tables 3-22 and 3-23 and may also be used to determine maximum line length for specified undershoot and overshoot, instead of using equations 12 and 13. This derivation follows.

For $C_T = 0$ and $t < 6T_D$, equation 87 reduces to:

$$e_{out}(t)=2\,mt\,U(t)-2m\,(t-T_1)\,U\,(t-T_1)+2m\rho_S\cdot(t-2T_D)\,U\,(t-2T_D)-2m\rho_S\,(t-2T_D-T_1)\,U\,(t-2T_D-T_1)+2m\rho_S^2\,(t-4T_D)\,U\,(t-4T_D)-2m\rho_S^2\,(t-4T_D-T_1)\cdot U\,(t-4T_D-T_1)\,. \tag{88}$$

This equation can also be derived by starting from equation 5.

Using a lattice diagram, it is found that the maximum overshoot occurs at $t = T_1$. Substituting $t = T_1$ into equation 88 gives:

$$E_{max} = 2m \left[T_1 + \rho_S (T_1 - 2T_D) \right] , \qquad (89)$$

$$\text{for } 2T_D < T_1 < 4T_D ;$$

and:

$$E_{max} = 2mT_1 ,$$

$$\text{for } T_1 \leq 2T_D . \qquad (90)$$

In both cases,

$$m = \frac{Z_o E_1}{(R_o + Z_o + R_s)T_1} ,$$

$$T_1 = 1.2t_r ,$$

$$T_D = t_{pd} \cdot \ell ,$$

and

t_{pd} = line delay in nanoseconds/inch,

ℓ = line length in inches.

By definition,

$$E_{max} = E_1 \frac{(100 + O.S.)}{100} , \qquad (91)$$

where E_1 is the voltage change at the output of the driving gate, and O.S. is the percent overshoot based on logic swing level. Thus by substituting into equation 89, the percent overshoot can be obtained:

$$\%O.S. = \left[-1 + \frac{2\,Z_o}{Z_o + R_S + R_o}\ (1 + \rho_S) - \frac{4\rho_S t_{pd} \ell Z_o}{1.2\,t_r (Z_o + R_S + R_o)}\right] \cdot 100\ , \tag{92}$$

$$\text{for } 2t_{pd} < T_1 < 4t_{pd}\ .$$

Equation 92 gives the overshoot (as a percentage of the logic swing) that occurs for a particular length of line, assuming zero capacitance at the end of the line. If the two way propagation delay of the line is equal to or greater than T_1, then this particular length of line is:

$$\ell \geq \frac{1.2\,t_r}{2t_{pd}}\ . \tag{93}$$

If equation 93 is satisfied, then the overshoot reaches a maximum value which can be solved for by using equation 90:

$$\%O.S._{max} = 100\left(\frac{2\,Z_o}{Z_o + R_S + R_o} - 1\right)\ . \tag{94}$$

If the length of line is less than that specified in equation 93, the line length can be found from equation 92, given the permissible overshoot for a given design:

$$\ell = \left[\frac{2\,Z_o}{R_o + Z_o + R_S} \cdot (1 + \rho_S) - \frac{(100 + O.S.)}{100}\right] \cdot \left(\frac{(R_o + Z_o + R_S)\,1.2\,t_r}{4\,Z_o \rho_S\, t_{pd}}\right)\ . \tag{95}$$

In this relation , it is necessary that:

$$\ell < \frac{1.2\,t_r}{2t_{pd}}\ .$$

Maximum Line Lengths

The maximum permissible line length with capacitance loading can be approximated in a manner similar to that used to establish a maximum open line length in a previous section:

$$\frac{\ell}{\ell_{max}} = \frac{t_{pd}\sqrt{1 + \frac{C_T}{C_o \ell_{max}}}}{t_{pd}} \quad . \tag{96}$$

Solving for ℓ_{max}:

$$\ell_{max} = \frac{-\frac{C_T}{C_o} + \sqrt{\left(\frac{C_T}{C_o}\right)^2 + 4\ell^2}}{2} \quad , \tag{97}$$

where C_T is the total lumped capacitance in pF, C_o is the intrinsic line capacitance in pF/in, and ℓ is the length of line in inches defined in equation 95.

Using a lattice diagram, it has been found that the maximum undershoot occurs when $t = 2T_D + T_1$. Substituting this information into equation 88 produces the relation:

$$E_{min} = 2m\left((2T_D + T_1) - 2T_D + \rho_S T_1 + \rho_S^2 (T_1 - 2T_D)\right) \quad , \tag{98}$$

for:

$$2T_D < T_1 < 4T_D \quad ,$$

$$E_{min} = 2m\,(1 + \rho_S)\,T_1 \quad , \tag{99}$$

$$T_1 \leq 2t_{pd} \quad .$$

By definition,

$$E_{min} = E_1 \frac{(100 - U.S.)}{100} \quad , \tag{100}$$

where U.S. is the percent undershoot. Equation 98 can be used to form a useful

relationship, which expresses the undershoot in terms of circuit parameters:

$$\%U.S. = \left(1 - \frac{2Z_o}{Z_o + R_S + R_o}\left(1 + \rho_S + \rho_S^2\right) + \frac{4\rho_S^2\, t_{pd}\, \ell\, Z_o}{1.2\, t_r\,(Z_o + R_S + R_o)}\right) \cdot 100 \qquad (101)$$

for:

$$2T_D < T_1 < 4T_D$$

and:

$$\ell < \frac{1.2\, t_r}{2\, t_{pd}} .$$

Thus equation 101 gives the undershoot as a percentage of the logic swing – for a particular length of line.

If equation 93 is satisfied, then the undershoot reaches a maximum value which can be found from equation 99 to be:

$$\%U.S._{max} = 100\left(1 - \frac{2\,Z_o}{Z_o + R_S + R_o} \cdot (1 + \rho_S)\right) . \qquad (102)$$

On the other hand, if the length of line is less than specified in equation 93, the line length can be found from equation 101 once the permissible undershoot has been specified. Solving:

$$\ell = \left(\frac{2\,Z_o}{Z_o + R_S + R_o}(1 + \rho_S + \rho_S^2) - \frac{(100 - U.S.)}{100}\right) \cdot \frac{(Z_o + R_S + R_o)\ 1.2\, t_r}{4\, Z_o \rho_S^2\, t_{pd}} , \qquad (103)$$

for:

$$\ell < \frac{1.2\, t_r}{2t_{pd}} .$$

Equations 95 and 97 can be used to find the maximum open line length (instead of equations 12 and 13) when the maximum percentage overshoot has been specified. Equations 97 and 103 can be used when the maximum undershoot is specified. Of course, a more exact value for the maximum permissible line length is found when a computer program is used to generate the values using an extension of equation 87. This was done to generate Figures 3-13, 3-14, and 3-15. The first seven reflections (n = 7) were used to accurately define the open line length required to limit overshoot and undershoot for a wide range of load capacitances. Equations 94 and 102 were used to generate the values given in Figures 3-22 and 3-23 using a computer program.

REFERENCES

1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines", IEEE Transactions on Electronic Computers, Vol. EC-16, No. 2, April 1967, pp. 185-193.
2. Cohn, S. B., "Characteristic Impedance of the Shielded Strip Transmission Line", Transactions IRE, Vol. MTT-2, July 1954, pp. 52-57.
3. Springfield, W. K., "Designing Transmission Lines into Multilayer Circuit Boards", Electronics, November 1, 1965, pp. 90-96.
4. Skilling, H. H., "Electric Transmission Lines", New York, McGraw-Hill, 1951.
5. DeFalco, J. A., "Reflections and Crosstalk in Logic Circuit Interconnections", IEEE Spectrum, July 1970, pp. 44-50.
6. Millman, J., and Taub, H., "Pulse, Digital and Switching Waveforms", New York, McGraw-Hill, 1965, pp. 83-106.
7. "Time Domain Reflectometry", Hewlett-Packard Application Note 62, 1964.
8. Botos, Bob, "Nanosecond Pulse Handling Techniques in I/C Interconnections", Motorola Application Note AN-270.
9. Schwarzmann, A., "Microstrip Plus Equations Adds Up to Fast Designs", Electronics, October 2, 1967, pp. 109-112.
10. Catt, I., "Crosstalk (Noise) in Digital Systems", IEEE Transactions on Electronic Computers, Vol. EC-16, No. 6, December 1967, pp. 743-763.
11. Feller, A., H. R. Kaupp, J. J. Digiacoma, "Crosstalk and Reflections in High-Speed Digital Systems", Proceedings, Fall Joint Computer Conference, 1965, pp. 511-525.
12. Cohn, S. B., "Shielded Coupled-Strip Transmission Line", IRE Transactions-Microwave Theory and Techniques, October 1955, pp. 29-38.
13. Gabbard, O. G., "High-Speed Digital Logic for Satellite Communications", Electro-Technology, April 1969, pp. 59-65.
14. Henschen, I. E. and E. M. Reyner II, "Adapting PC Connectors for Impedance Matching", Proceedings, NEPCON, 1970.

CHAPTER 8

MECL Applications

INTERCONNECTION TECHNIQUES FOR MOTOROLA'S MECL 10K/10KH SERIES EMITTER COUPLED LOGIC

INTRODUCTION

As the digital integrated circuit market has become more mature, the need for very high speed logic elements has grown. Future machine designs demand a logic family with high clock rate capability, short propagation delays, and a minimum of layout constraints. From this need, the MECL 10K/10KH families of emitter-coupled logic have evolved — designed to be the most usable very high speed logic families available.

The 2.0 nanosecond gate propagation delay of MECL 10K and 1.0 ns gate propagation delay of MECL10KH gives the families a speed range between the older MECL II and MECL III families. Additional characteristics, such as low power dissipation (25mW per gate function), and slow rise and fall times have eased the difficulties encountered in trying to balance system speed versus ease of design.

A MECL 10K system has the capability for clock rates in excess of 100 MHz, and MECL 10KH has clock rates in excess of 200 MHz. To permit such high speed operation, gate propagation delays must necessarily be short. However, to simplify wiring techniques and to minimize the use of transmission lines, rise and fall times have been kept to slower values.

The 1 nanosecond rise time of MECL III demands a transmission line environment. On the other hand, MECL 10K/10KH have been designed to approach the higher speed rates of MECL III, but with simpler wiring requirements.

The operational behavior of a MECL III gate with a rise time of 1 nanosecond (10%-90%) is shown in figure 1 for comparison. Figure 1a shows the difference in rise times when either gate is driving only a pulldown resistor. Figure 1b shows the same outputs driving an 8 inch signal line to a gate input. The MECL III gate shows severe ringing. This necessitates the use of a transmission line. The effect of the slower rise time of the MECL 10K gate is obvious in that ringing is not as severe. Herein, lies an advantage for the system designer using MECL 10K — that is, he may realize a very high speed system using only a minimum of transmission lines.

When driving long lines or large fanouts at maximum frequency, transmission lines are needed. MECL 10K/10KH has the capability to drive such lines. Also, the families are specified to be completely compatible with MECL III in the 16-pin dual-in-line packages. As a result, MECL 10K/10KH can be used to obtain maximum versatility with low power and ease of layout design.

The following discussion is intended to give the system designer insight into these problem areas: The use of non-transmission line interconnections; the characteristics of transmission lines which affect MECL interconnections; and the techniques used for transmission lines. Other considerations to be made for system interconnections are also discussed, such as noise margins, clock driving, wire wrapping, and party line techniques.

SIGNAL LINE CONSIDERATIONS

The purpose of an interconnection line in any digital system is to transmit information from one point of the system to another. When information on a signal line changes, a finite amount of time is necessary for the information to travel from the sending end to the receiving end of the line. As the circuit speed becomes faster and clock rates increase, the dynamic behavior of the interconnection line becomes increasingly important. The rise and fall times of the logic elements, loading effects, delay times of the signal paths, and the various other transient characteristics, all affect reliable operation of the system. The effects of these factors and the advantages of the dynamic characteristics of MECL 10K/10KH are perhaps best shown by briefly investigating the transmission line qualities of a signal path.

In figure 2a is shown a simple interconnection circuit. A MECL 10K/10KH gate is shown driving a line length ℓ, to another gate with a pulldown resistor, R_L. If the loading effect of the receiving gate is disregarded for the moment (input impedance is very large with respect to R_L), the same line could be modeled as shown in figure 2b.

The driving gate is modeled as a voltage source with output impedance, R_O. The signal line will exhibit an impedance to a transient signal which is called its characteristic impedance, Z_O. If the line is not a regular transmission line, Z_O will vary somewhat. However, for this example let us assume Z_O is constant.

When the output of the driving gate changes state, the voltage at point A is a function of the internal voltage swing, V_{INT}, output impedance, and line impedance:

$$V_{A(t)} = V_{INT(t)}\left(\frac{Z_O}{R_O + Z_O}\right).$$

For MECL 10K/10KH, R_O is small with respect to the line impedance, so the output swing is nearly the same as the input transition – typically 800 mV. The signal will prop-

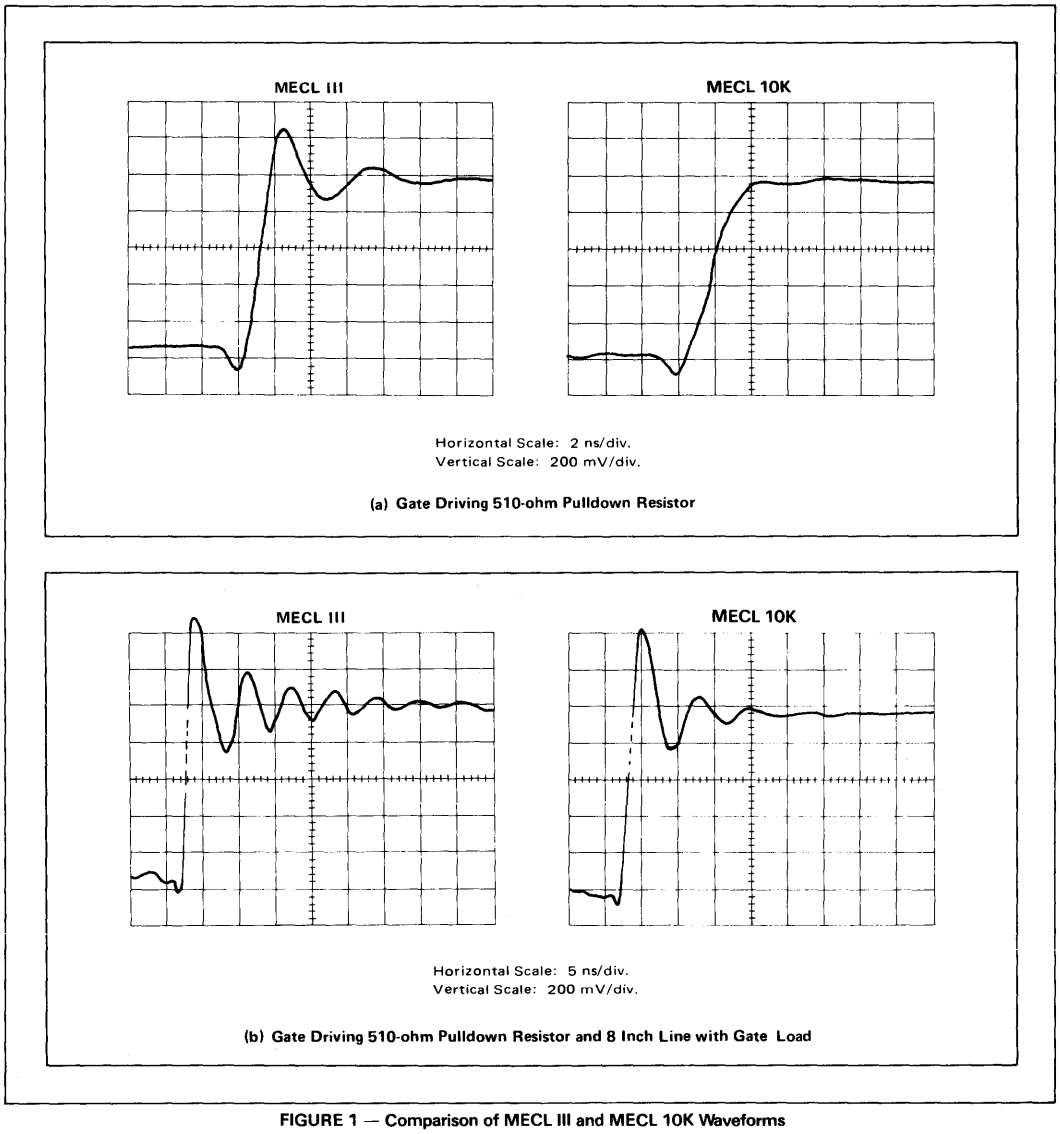


FIGURE 1 — Comparison of MECL III and MECL 10K Waveforms

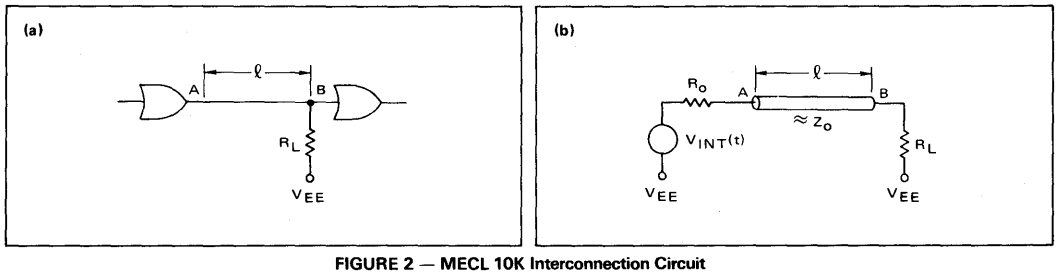


FIGURE 2 — MECL 10K Interconnection Circuit

agate down the line and be seen at point B time T_D later. The signal, when reaching the end of the line (point B), may be reflected and returned toward the sending end of the line. The reflected voltage is:

$$V_A' = \rho_L V_A,$$

where ρ_L is the reflection coefficient,

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o}.$$

In the special case where $R_L = Z_o$, then $\rho_L = 0$ and the reflected voltage is zero. In this situation the load resistor exactly matches the characteristic impedance of the line, so no reflection occurs.

When reflection does occur, it returns to point A at time 2 T_D, where T_D is the one-way line propagation delay. The sending end will again reflect this voltage with a reflection coefficient, ρ_S, given by:

$$\rho_S = \frac{R_o - Z_o}{R_o + Z_o}.$$

The reflected signal will continue to bounce back and forth between the ends of the signal line, gradually diminished in amplitude by reflection coefficients and the resistance in the line.

Now consider a second line in which the load resistor has been moved to the sending end of the line (figure 3a). This model is altered from the first only in that the load resistor is seen at the driver output. When the output of the driving gate changes state, the output swing, V_A, will be typically 800 mV.

The signal reaching point B will be reflected (as discussed). The coefficient, ρ_L, becomes worst case (≈ 1) because the input impedance of the receiving gate is high. In such a case the reflection will be large. As the reflection returns to point A at time 2 T_D, the reflection coefficient, ρ_S, comes into play. Its value will be very close to the previous case:

$$\rho_S = \frac{\frac{R_o R_L}{R_o + R_L} - Z_o}{\frac{R_o R_L}{R_o + R_L} + Z_o} \approx \frac{R_o - Z_o}{R_o + Z_o},$$

since R_o is small compared to R_L.

The reflections, as before, continue to bounce back and forth on the line getting successively smaller in amplitude. The result is that ringing appears on the signal line (figure 3c).

Rise time effects may be understood by considering the delay time of the line. If the line length ℓ is sufficiently short, the first reflections are seen at the sending end of the line while the driver is still changing state. The reflections are hidden by the rising edge of the pulse, and ringing is reduced. Therefore, the slow rise time of MECL 10K/10KH permits longer line lengths to be used before trouble with ringing is encountered.

This second signal line example is called an open line or an unterminated line. To limit undershoot to about 12 percent of the logic swing, the maximum open line length permitted would be:

$$L_{max} = \frac{t_r}{2t_{pd}},$$

where: t_r = Rise time of driving gate (ns) (20% - 80%)
t_{pd} = Propagation delay per unit line length (ns/in).

The above expression may also be used to show the effect of loading on an interconnection. t_{pd} is dependent on the rate of signal propagation on the line; the rate is controlled by the type of line and the loading on the line. MECL inputs are high impedance and capacitive in net reactance (3 to 5 pF per input). Increased loading slows the rate of propagation of the line and decreases allowable open line length. That is, as fan-out increases, the maximum open line length decreases for acceptable undershoot.

To understand how ringing and undershoot affect system operation, it is helpful to define guaranteed noise mar-

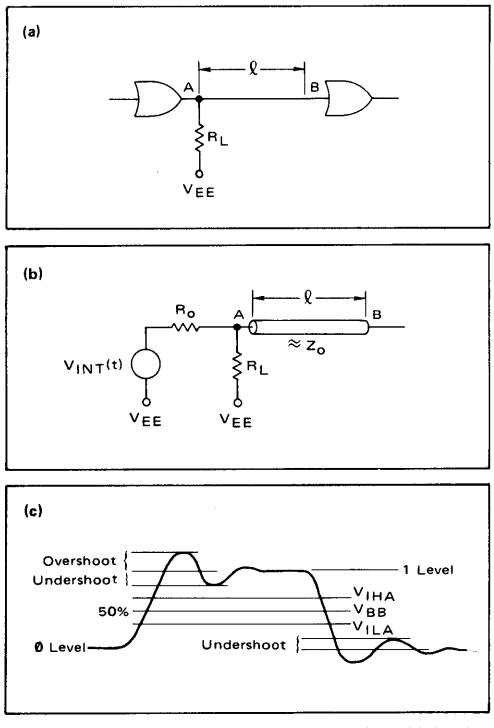


FIGURE 3 — MECL 10K/10KH Interconnection with Load Resistor at Sending End of Line

gins. Noise margin is defined as the difference between a worst case input logic level (V_{OHAmin} or V_{OLAmax}) and the worst case threshold (V_{IHAmin} or V_{ILAmax}) for the corresponding logic level. Guaranteed noise margins (N.M.) for MECL 10K at 25°C are:

$$\text{Logic 1 N.M.} = V_{OHAmin} - V_{IHAmin} = -0.980 - (-1.105) = 125 \text{ mV};$$

$$\text{Logic } \emptyset \text{ N.M.} = V_{ILAmax} - V_{OLAmax} = -1.475 - (-1.630) = 155 \text{ mV}.$$

However, using typical logic levels of -0.900 volts and -1.700 volts, the nominal voltage margins are greater than 200 mV for both logic levels. Noise margin for MECL 10KH is 150 mV for both logic 1 and 0 N.M.

For system design, worst case conditions should be considered. If so, a 125 mV noise margin becomes the design limit for MECL 10K. This voltage margin protects against signal undershoot, power supply variations, and system noise. Good circuit interconnections should limit maximum undershoot to less than 100 to 110 mV to provide a design safety margin.

Other factors – such as line impedance and placement of loads on the line – also affect ringing of signals. A long and elaborate discussion would be necessary to describe all of the varying effects, and the description here is only intended to give a brief idea of the many factors involved. When line lengths and fanout go beyond limits (which will be defined), techniques such as twisted pair lines and terminated lines may be used.

PRINTED CIRCUIT BOARD INTERCONNECTS

Layout rules needed for designing with MECL 10K/ 10KH depend mainly on the design goals of the system user. MECL 10K/ 10KH may be used in layouts ranging from single layer printed circuit (PC) board with wired interconnects, to the most elaborate multilayer board with a complete transmission line environment. Optimization of system layout will include considerations of the system size, desired performance, and cost.

Use of a ground plane is a suggested procedure whenever possible. A ground plane is beneficial for maintaining a noise free voltage plane for the V_{CC} supply, and for maintaining constant characteristic impedance whenever transmission lines become necessary. A ground plane may be established by using single sided board with wired interconnects, or by using double or multilayer PC board.

WITHOUT GROUND PLANE

In small systems where the number of interconnects and the package density are high, it is difficult to reserve a large ground plane area without the use of multilayer board, a costly approach. However, MECL 10K/ 10KH may still be used with good system performance if certain guidelines are followed:

(1) V_{CC} should be bussed to the V_{CC} pins of each package. Bus lines should be as wide as possible with a width of 0.1 inch minimum per row of packages. If an edge connector is used, V_{CC} should be pinned out to several connector pins.

(2) V_{EE} should also be bussed, if possible, to pin 8 of each package (pin 12 of the 24 pin package). When V_{EE} is brought onto the board via an edge connector, the V_{EE} line should be in close proximity to a V_{CC} pin for easy bypassing.

(3) Each device should be bypassed between the V_{CC} and the V_{EE} pins with a low inductance 0.01 μF capacitor.

(4) Logic interconnecting lines should be kept to minimum length. A maximum line length of 6 inches is suggested; ringing will begin to get too severe with longer line lengths. For line lengths greater than 6 inches, signal lines with series damping resistors are necessary (similar to those shown in figure 13).

(5) For high fanout (8 or greater) and high speed clock distribution, twisted pair lines or coaxial cable should be used. Both of these techniques are described in detail later.

Figure 4 shows a double-sided PC board in which the above rules are illustrated. Several MECL 10K devices are used with MTTL in a high speed counter, in which the MECL and MTTL are operated by a common voltage supply. Notice that V_{EE} and V_{CC} are both bussed to the package and that bus lines are as

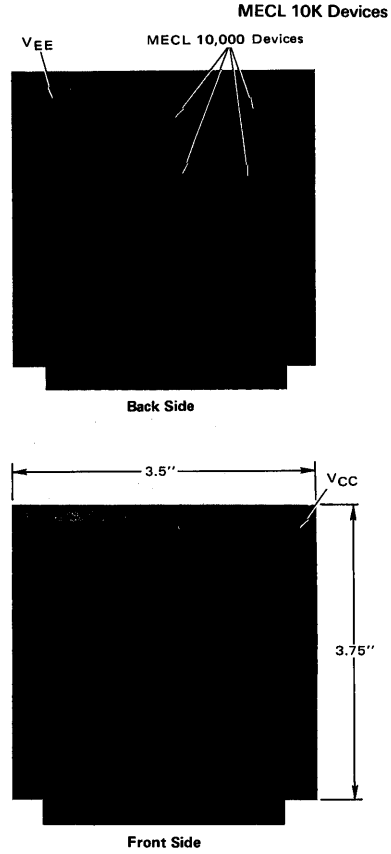


FIGURE 4 — Printed Circuit Board for MECL 10K System Without Ground Plane

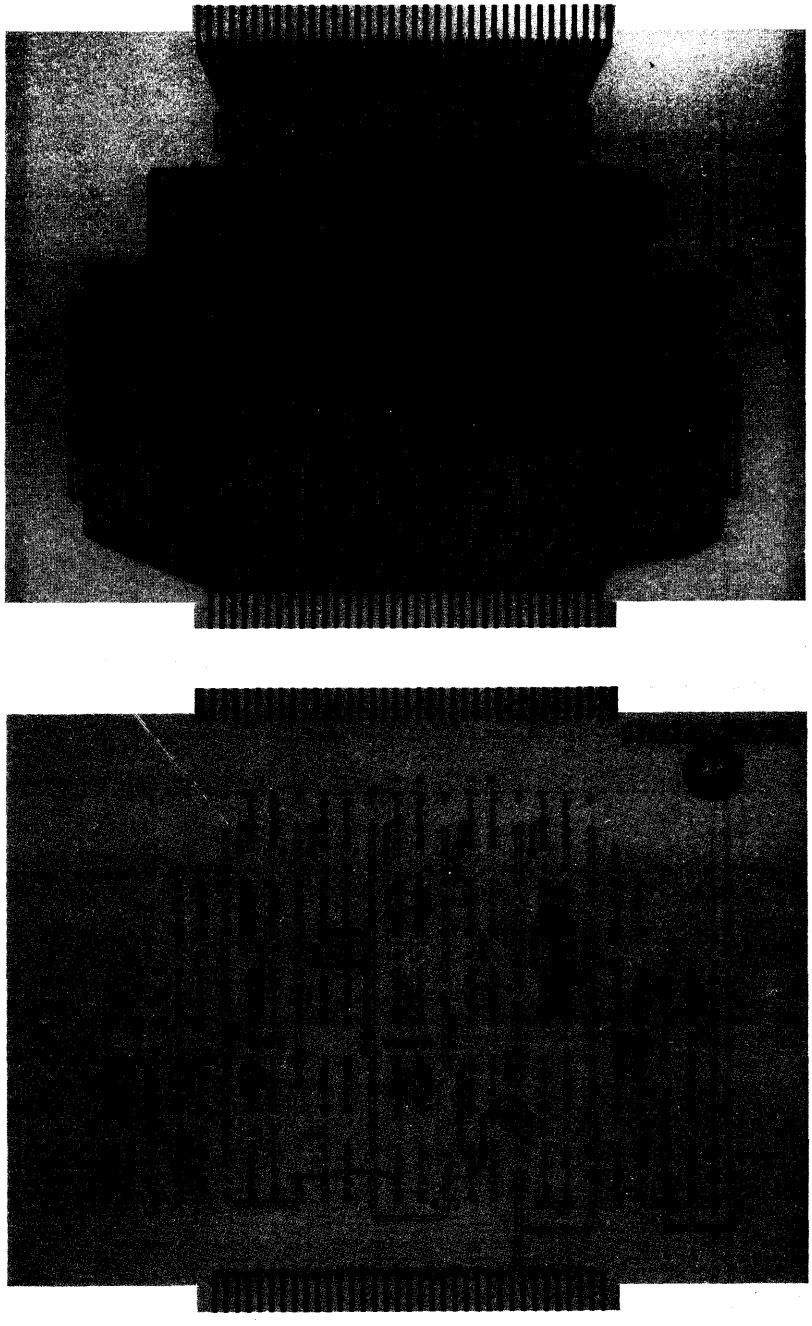


FIGURE 5 – MECL 10,000 PC Board With Ground Plane

wide as conveniently possible. Two 0.1 μF capacitors are used for low frequency bypassing on the board. Each MECL 10K device is bypassed with a 0.01 μF capacitor, and additional bypassing is scattered through the MTTL circuitry. Note that signal lines are short and no transmission lines are used.

WITH GROUND PLANE

A ground plane allows best performance for a MECL 10K/10KH system. The ground plane serves two purposes. First, it provides a constant characteristic impedance (Z_O) to signal interconnections; secondly, it provides a low inductance path for ground currents on the V_{CC} supply. As with systems which have no ground plane, certain design guidelines are recommended as follows:

(1) The ground plane (V_{CC}) need not cover 100% of the board surface. Approximately 30 to 40% of the ground area may be removed for signal interconnections, as illustrated in figure 5. When using edge connectors, the ground plane should be pinned out to about every seventh connector pin.

(2) The V_{EE} supply should be bussed if possible, to pin 8 of each package. Bus line width at any point should be a minimum of 0.1 inch. Where possible, the V_{EE} supply should be extended to a plane under the signal lines etched on the ground plane side of a two-sided circuit board. If V_{EE} is a plane under these lines, they will exhibit a constant characteristic impedance. This technique is also shown in figure 5.

(3) Bypassing need not be as extensive as on a board without a ground plane. Provide a low inductance 0.01 μF capacitor every two to six packages, depending upon how extensive the ground plane is. As a rule if the ground plane covers less than 50% of the board area, then bypass every two packages. On two-sided systems or multilayer systems where 100% ground plane is present, only one capacitor for every four to six packages is needed.

(4) In practice, the majority of board interconnects are shorter than six inches, with fanouts four or less. As discussed, the rise and fall times of MECL 10K allow these lines to be treated as unterminated transmission lines requiring only a pull-down resistor. Normally, a 510-ohm resistor to V_{EE} is used. (Detailed limits for interconnections are provided as a function of line impedance and fanout in the following section). MECL 10KH allows 3 inches to be treated as an unterminated line.

(5) For high fanout and high speed clock distribution, terminated transmission lines or twisted pair lines should be used. These techniques are discussed in the following sections.

TRANSMISSION LINE GEOMETRIES

With a ground plane present, three types of transmission line geometries are feasible: wire over ground; microstrip line; and strip line. The following sections summarize the characteristics of each type of line.

(1) Wire over ground – The cross section of a wire over a ground is shown in figure 6a. The characteristic impedance of the wire is:

$$Z_O = \frac{60}{\sqrt{e_r}} \ln\left(\frac{4h}{d}\right),$$

where e_r is the effective dielectric constant surrounding the wire. The wire over ground plane is useful for breadboard layouts (as with single-sided board) and for backplane wiring. The characteristic impedance of a wire over ground plane will be about 120 ohms with variance depending on the wire size, type of insulation, and distance from the ground plane..

(2) Microstrip lines – A microstrip line (figure 6b) is a strip conductor separated from a ground plane by a dielectric medium. Two-sided and most multilayer boards use this type of transmission line. If the thickness, width, and height of the line above the ground plane are controlled, the line will exhibit a characteristic impedance of:

$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8\,w + t}\right),$$

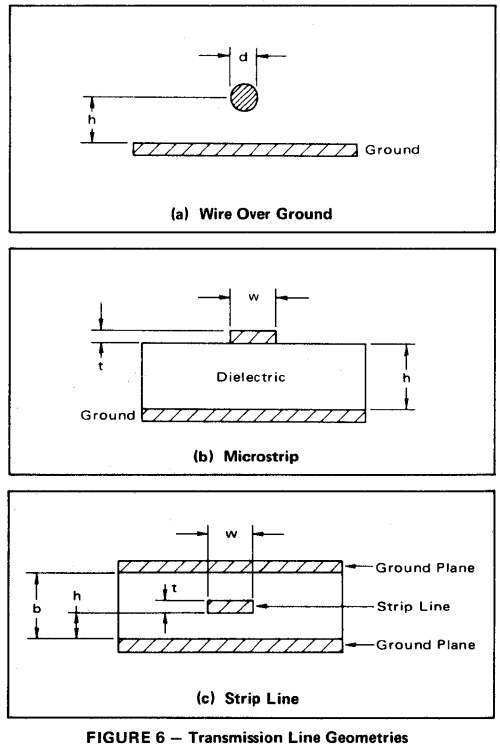


FIGURE 6 – Transmission Line Geometries

Here e_r is the dielectric constant of the board. For standard G-10 fiberglass epoxy boards the dielectric constant is about 5.0.

The signal line is obtained by etching unwanted copper from the board using photo resist techniques. A characteristic impedance can easily be controlled to within 10 percent.

As mentioned above, board thickness and dielectric constant affect line impedance. Figure 7 gives a table of values for characteristic impedance versus line width for 0.031" and 0.062" G-10 board with one ounce copper (widths for two ounce copper are nominally 1 to 2 mils narrower).

The propagation delay of microstrip line may be calculated by:

$$t_d = 1.017 \sqrt{0.475\, e_r + 0.67} \text{ ns/ft.}$$

Note that the propagation delay of the line depends only on the dielectric constant and is not a function of line width or spacing. For G-10 fiberglass epoxy boards (e_r = 5.0) the propagation delay of the microstrip line is calculated to be 1.77 ns/ft.

FIGURE 7 – Microstrip Characteristic Impedance versus Line Width for One Ounce G-10 Fiberglass Epoxy Board

Z_o (OHMS)	LINE WIDTH (MILS) (Dimension w of Figure 6b)	
	0.062" BOARD	0.031" BOARD
50	103	47
55	89	41
60	77	35
65	66	30
70	57	26
75	49	22
80	42	19
85	36	16
90	31	14
95	27	11
100	23	10

(3) Strip Line – A strip line (figure 6c) is a copper ribbon centered in a dielectric medium between two conducting planes. This type of line is used in mutlilayer boards and is not seen in most systems. Multilayer boards are justified when operating MECL 10K/10KH at top circuit speed, and when high density packaging is a system requirement. Since most designers need not concern themselves with strip lines, little is presented here about them.

UNTERMINATED LINE LIMITS

As previously mentioned, a MECL signal line may be considered as an unterminated transmission line. Rise time, characteristic impedance of the line, and loading affect the maximum interconnection length for unterminated lines. Figure 8 shows a tabulation of suggested maximum open line lengths for various fanouts and line impedances.

The tabulated values were calculated for limiting overshoot to 35% of the logic swing, or undershoot to 12% (whichever was the limiting factor under specified conditions). Severe overshoot can slow down clock rates, and severe undershoot can result in reduced noise immunity. The transmission line model of figure 3 was used in calculations.

As an example of how the table of line limits may be used, consider a system layout using 0.062" board (G-10 fiberglass epoxy). Assume that signal interconnection widths may be from 25 to 40 mils wide. If a ground plane is used on one side of the system PC board, all system interconnects would show a corresponding characteristic impedance. The wide line (40 mils) is preferable since Z_o would be 82 ohms which is lower than that for a 25 mil line ($Z_o \approx 97$ ohms) and the lower impedance allows a longer maximum length line. The lower impedance line with a fanout of 4 would then have a suggested maximum length of about 4.2 inches. On normal system-sized PC boards (5"x7"), the majority of signal line interconnections will be less than 4 inches in length if the system layout is well planned.

FIGURE 8 — Maximum Unterminated Line Length for MECL 10K to Maintain Less Than 12% Undershoot

	Z_o (OHMS)	FANOUT = 1 (2.9 pF)	FANOUT = 2 (5.8 pF)	FANOUT = 4 (11.6 pF)	FANOUT = 8 (23.2 pF)
		ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)	ℓ MAX (IN)
MICROSTRIP (Propagation Delay 0.148 ns/in.)	50	8.3	7.5	6.7	5.7
	68	7.0	6.2	5.0	4.0
	75	6.9	5.9	4.6	3.6
	82	6.6	5.7	4.2	3.3
	90	6.5	5.4	3.9	3.0
	100	6.3	5.1	3.6	2.6
BACKPLANE (Propagation Delay 0.140 ns/in.)	100	6.6	5.4	3.8	2.8
	140	5.9	4.3	2.8	1.9
	180	5.2	3.6	2.1	1.3

An interconnection with the pulldown resistor at the sending end of the line is the worst case situation for an unterminated line. If unterminated interconnection lengths are extended beyond the suggested limits, overshoot and undershoot are increased. The lengths given are calculated so that undershoot never exceeds the guaranteed noise margins, although typically noise margins are much greater than specified.

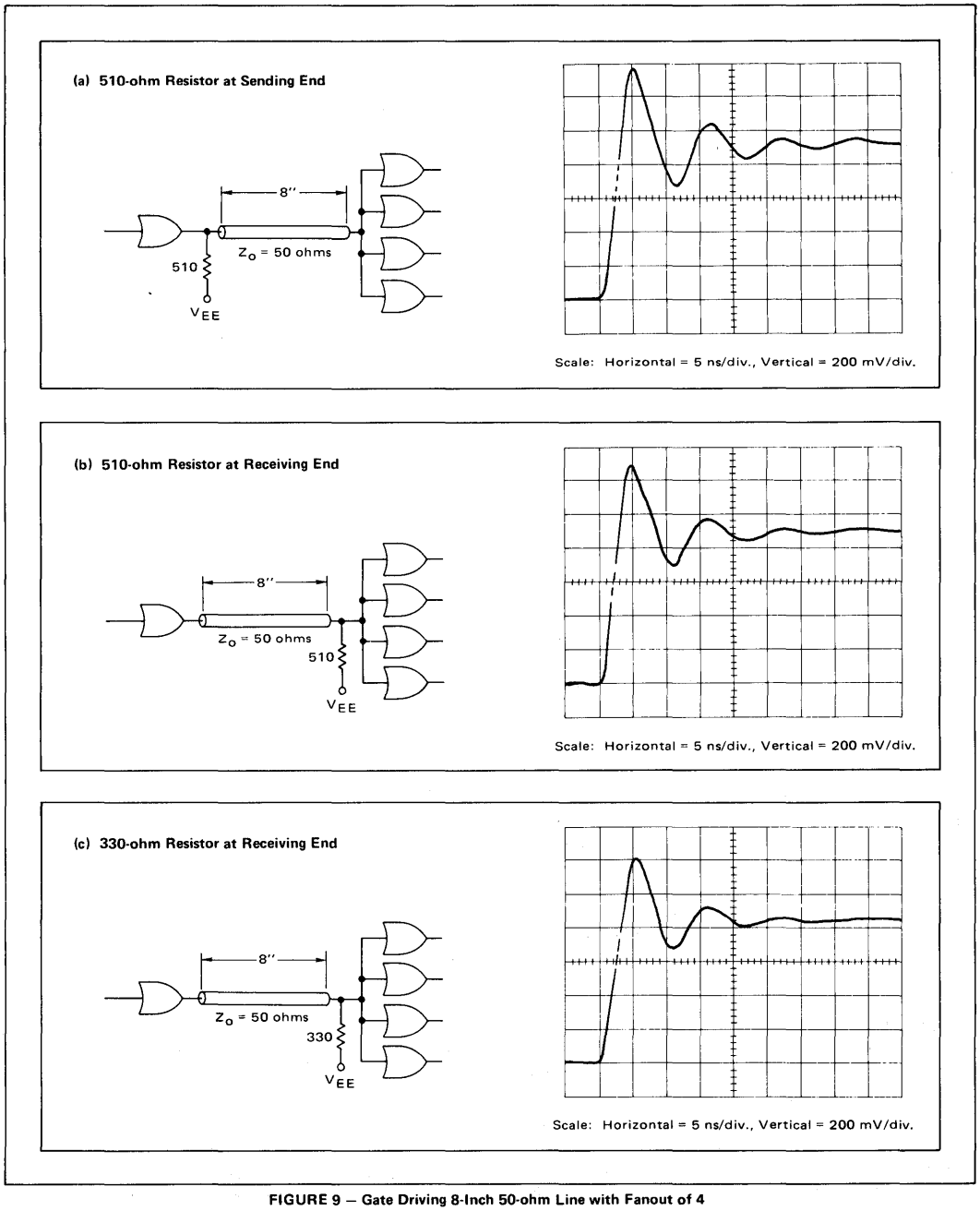


FIGURE 9 – Gate Driving 8-Inch 50-ohm Line with Fanout of 4

Overshoot and undershoot may also be reduced by locating the pulldown resistor at the receiving end of the line. If the pulldown resistor is moved to the receiving end, the reflection coefficient (ρ_L) is reduced. This reduces ringing.

Figure 9 shows the signal at the receiving end of an 8-inch 50-ohm line with a fanout of 4. In figure 9a, a 510-ohm pulldown is at the sending end of the line. Figure 9b has a 510-ohm pulldown at the receiving end, while figure 9c has a 330-ohm pulldown at the receiving end. The overshoot and undershoot are successively reduced in the latter two cases.

For worst case, the reflection coefficient is approximately equal to one ($\rho_L \approx 1$). For the best case shown, using a 330-ohm pulldown, $\rho_L = (330 - 50)/330 + 50) = 0.74$, which represents an improvement of about 25%. In comparing the waveforms, notice that overshoot is reduced by roughly the same percentage (9c versus 9a).

The tabulated values of figure 8 are not necessarily absolute limits for unterminated lines. Longer unterminated lines may be used if the pulldown resistor is moved to the receiving end of the line, or if increased overshoot and undershoot are acceptable.

TRANSMISSION LINE TERMINATION TECHNIQUES

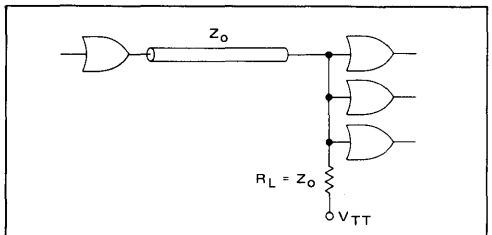
Proper transmission line termination prevents reflections on the line, so ringing does not occur. As a result, interconnection lengths are only limited by attenuation, bandwidth, etc. MECL transmission line interconnections utilize several techniques.

(1) Parallel Termination – A transmission line will have a reflection coefficient, (ρ_L), of zero when driving a load impedance equal to its characteristic impedance. MECL 10K/10KH can source current for driving a 50-ohm characteristic impedance line with the line terminated by 50 ohms to -2 volts. The termination voltage (V_{TT} = -2 volts) is necessary since 50 ohms loaded to V_{EE} would use excessive current. Figure 10 illustrates parallel termination.

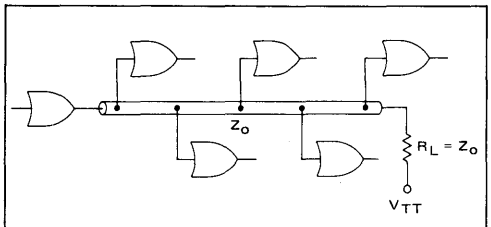
Gate inputs may be distributed along the transmission line (10b), and do not have to be lumped at the end of the line (10a). The gate inputs appear as high impedance stubs to the transmission line and should be as short as possible. While inputs may appear anywhere along the line, the terminating resistor should be at the end of the line. As fanout with this configuration increases, the edge of the waveform slows down, since the signal drives an increasing amount of capacitance. The waveform is undistorted along the full length of the line.

For large systems where total power is a consideration, all lines should be parallel terminated to a -2 volt supply. This is the most power-efficient manner for terminating MECL circuits. The drawback is of course, the requirement for an additional power supply.

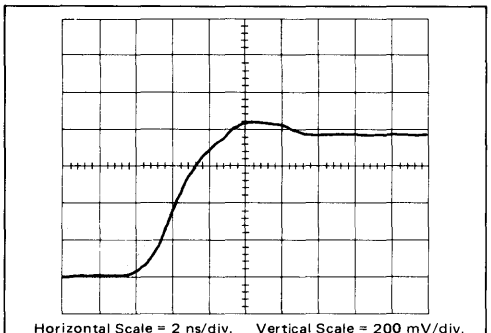
An alternate approach is to use two resistors – as shown in figure 11. The Thevenin equivalent of the resistor network is a resistor equal to the characteristic impedance of the line, terminated to -2 Vdc. R1 and R2 may be calcu-



(a) Parallel Terminated Line with Lumped Fanout

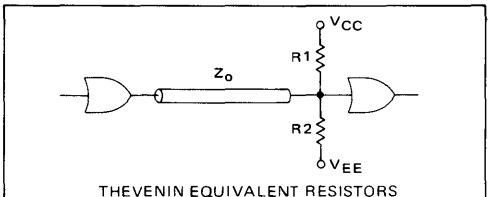


(b) Parallel Terminated Line with Distributed Fanout



(c) Waveform at Receiving End of Line

FIGURE 10 – Parallel Termination



THEVENIN EQUIVALENT RESISTORS FOR TERMINATION

Z_o (OHMS)	R1 (OHMS)	R2 (OHMS)
50	81	130
70	113	182
75	121	195
80	130	208
90	146	234
100	162	260
120	194	312
150	243	390

FIGURE 11 – Parallel Termination Using a Thevenin Equivalent Resistor Network

lated as follows:

$$R2 = 2.6\ Z_O;$$

$$R1 = \frac{R2}{1.6}.$$

(2) Series damping and series termination -- A series terminated line eliminates reflections at the sending end of the line. Series termination is accomplished by inserting a resistor in series with the output of the gate as shown in figure 12. The resistor value plus the circuit output impedance is made equal to the impedance of the transmission line.

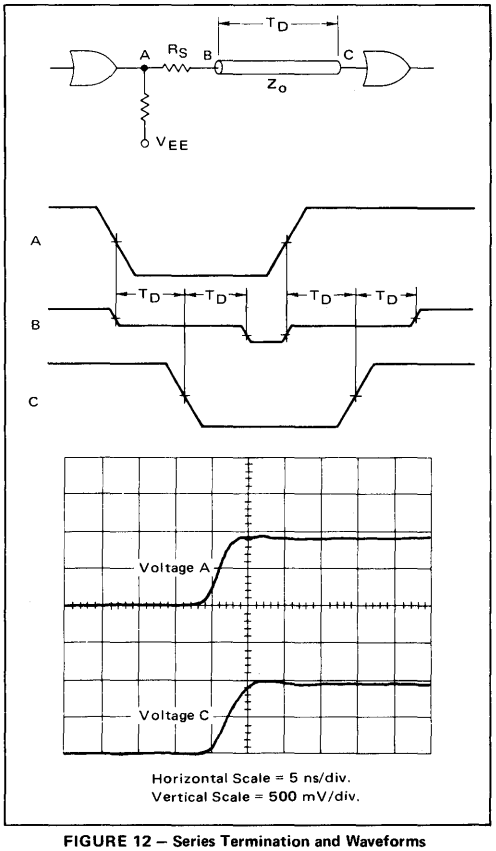


FIGURE 12 – Series Termination and Waveforms

The dc output impedance is 7 ohms for a MECL 10K/10KH gate. Therefore, the value of R_S should be equal to Z_o minus 7 ohms.

At time t = 0, the internal voltage switches to the low-state which represents a change of 0.8 to 0.9 volts (ΔV_{INT} = -0.8 to -0.9 volts). The voltage change at point B can be expressed as:

$$\Delta V_B = \Delta V_{INT} \frac{Z_o}{R_S + R_o + Z_o},$$

where R_o is the output impedance of the gate.

Since $R_S + R_o$ is made equal to Z_o, the voltage change at B is 1/2 the voltage, ΔV_{INT}. It takes the propagation delay time of the transmission line, T_D, for the waveform to reach point C, where the voltage doubles due to the unity reflection coefficient at the end of the line. The reflected voltage, which is equal to the sending voltage, arrives back at point B at time 2 T_D. No more reflections occur if $R_S + R_o$ is equal to Z_o. Similar waveforms occur when the driving gate switches to the high state.

An advantage of using series terminated lines is that only one power supply is required. The Thevenin equivalent parallel termination technique also uses only one supply, but requires more overall power. A disadvantage of series termination is that distributed loading along the line cannot be used because of the half-voltage waveform traveling down this line (see figure 12, waveform B). A number of lumped loads may be placed at the end of the terminated line as far as reflection at the receiving end is concerned, since a full initial signal transition is observed at this point and all subsequent reflections will be absorbed at the source.

The disadvantage of using only lumped loading at the end of a series terminated line can be eliminated at the expense of more lines (figure 13). As shown, there are n transmission lines for parallel fanout. The value of R_S should be the same as discussed previously for the emitter pulldown resistor, in which case n was equal to one.

The value of R_E, will be determined by the number of lines in the following way. R_E must be small enough to supply each transmission line with the proper voltage level. If R_E is too large, the output transistor will turn off when switching from the high to the low voltage state. The maximum value of R_E is given by:

$$R_{E(max)} = \frac{10\ Z_o - R_S}{N}.$$

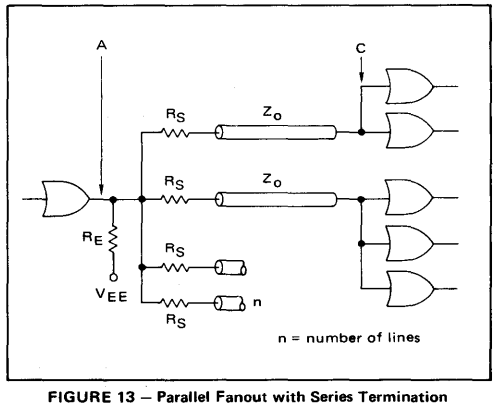


FIGURE 13 – Parallel Fanout with Series Termination

Figure 14a shows the gate output fall time (voltage A) and the fall time at the end of the line (voltage C) when N = 1, Z_O = 50 ohms, R_E = 1 k ohms, R_S = 43 ohms, and fanout = 3. The "steps" in the fall time waveform are due to the output device turning off because R_E is too large. Figure 14b shows the fall time when R_E = 290 ohms ($R_E < R_{E(max)}$).

The fanout at the end of a series terminated line is limited by the value of the series resistor, R_S. In the high state a voltage drop occurs across the series resistor:

$$V_S = (\text{fanout}) \times (\text{input current}) \times R_S .$$

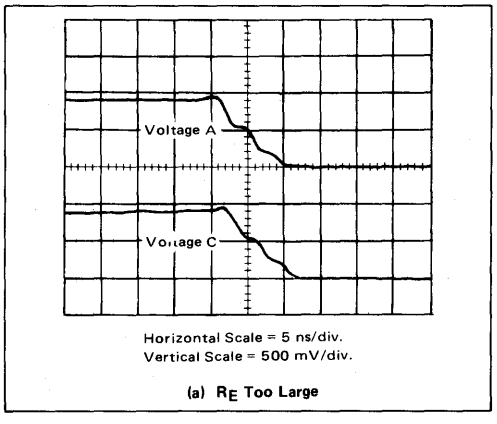
The input current to a MECL 10K gate is typically about 160 μA. If the fanout were 4 and R_S were 43 ohms for a 50 ohm line, V_S would equal about 28 mV. Noise margin would typically be cut by that amount. As fanout or the value of R_S increases, V_S increases and results in lower noise margins.

Series damping may also be used to reduce overshoot and ringing. Series damping is similar to series termination in that a small series resistor is used to reduce ringing rather than to completely terminate ringing. The resistor is smaller than the characteristic impedance of the line and it may be used to increase line length for the worst case open line (that is, R_S = 0) as shown in figure 8.

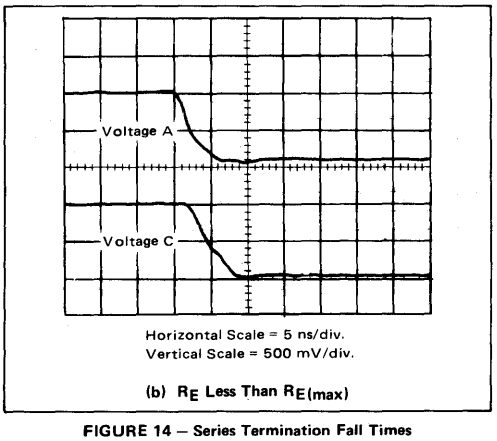
Series damping may also be used for greatly extended line lengths while remaining within calculated limits of overshoot and undershoot. Figure 15 gives minimum values of R_S needed for various line impedances to limit overshoot to 35% of signal swing, or undershoot to 12%. Using these values of minimum R_S, very long lines may be used.

FIGURE 15 — Minumum Values of R_S for Any Length Line, for Less Than 35% Overshoot or 12% Undershoot for MECL 10K/10KH

Z_o (OHMS)	MIN R_S (OHMS)
50	9
68	18
75	21
82	25
90	29
100	34
120	43
140	53
160	63

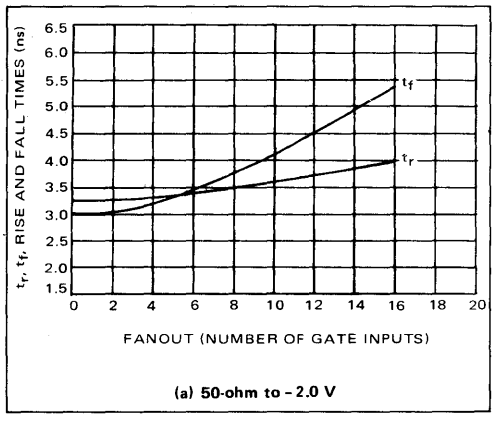


(a) R_E Too Large

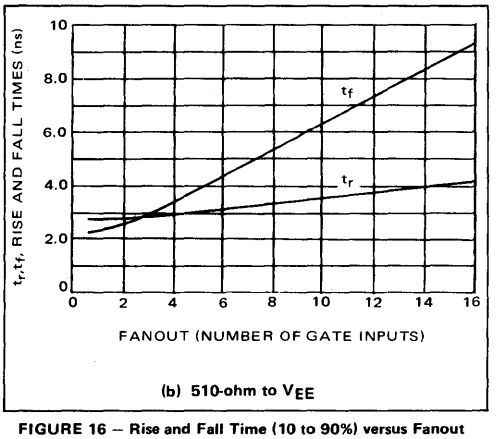


(b) R_E Less Than $R_{E(max)}$

FIGURE 14 — Series Termination Fall Times



(a) 50-ohm to -2.0 V



(b) 510-ohm to V_{EE}

FIGURE 16 — Rise and Fall Time (10 to 90%) versus Fanout

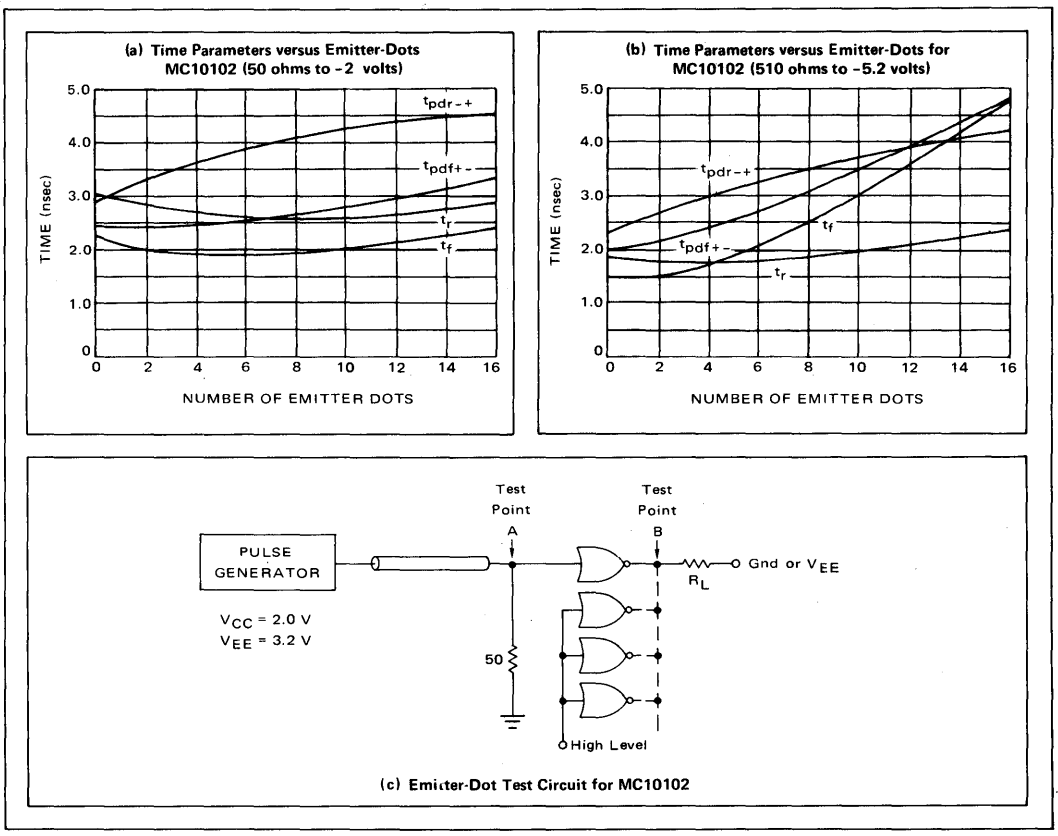


FIGURE 17

OTHER CONSIDERATIONS

Additional factors other than line length and transmission line terminations must be considered in system design. Some of these are discussed here:

(1) Fanout — The dc fanout capability of MECL 10K/10KH is very high since its high impedance inputs require little current (typically 160 μA). System speed requirements will ordinarily be the limiting factor for ac fanout. Capacitance increases with fanout and can cause rise and fall times to slow down.

Figure 16 shows the rise and fall times of an MC 10K gate as a function of fanout, both for 50 and 510 terminations. As fanout increases, load capacitance (both device and interconnection capacitance) increases, resulting in longer rise and fall times.

Larger fanout will normally result in longer interconnecting lines with their longer line delays, so ringing can become excessive. Under these conditions, use of properly terminated lines will result in best performance. A low impedance (50 Ω) parallel terminated line has a shorter propagation delay than a series damped or series terminated line with equivalent fanout. However, multiple series terminated lines driven from a single gate output (figure 13), with lower fanout per line, will show shorter delay times than a single parallel terminated line with an equivalent total fanout. Multiple series terminated or damped lines also show greater flexibility in line routing than a single parallel terminated line. The choice between the two schemes will depend on the fanout number and physical layout of the system.

(2) Wired-OR – The outputs of several gates may be tied together to perform the Wired-OR or emitter dot function. One resistor is normally used to pulldown the outputs.

Figure 17 graphs typical rise and fall times and propagation delays versus the number of emitter dots for both 50 Ω to - 2 volts termination and 510 ohms to V_{EE} termination. Rise and fall times are not greatly affected by emitter dotting, with the exception of fall times with the 510 Ω loading. The reason for this is that the discharge path for load capacitance has a longer time constant with the 510 Ω resistor. The most significant effect of Wired-ORing is increased propagation delays. As for ac fanout, desired system speed is the basic limiting factor for the emitter dot.

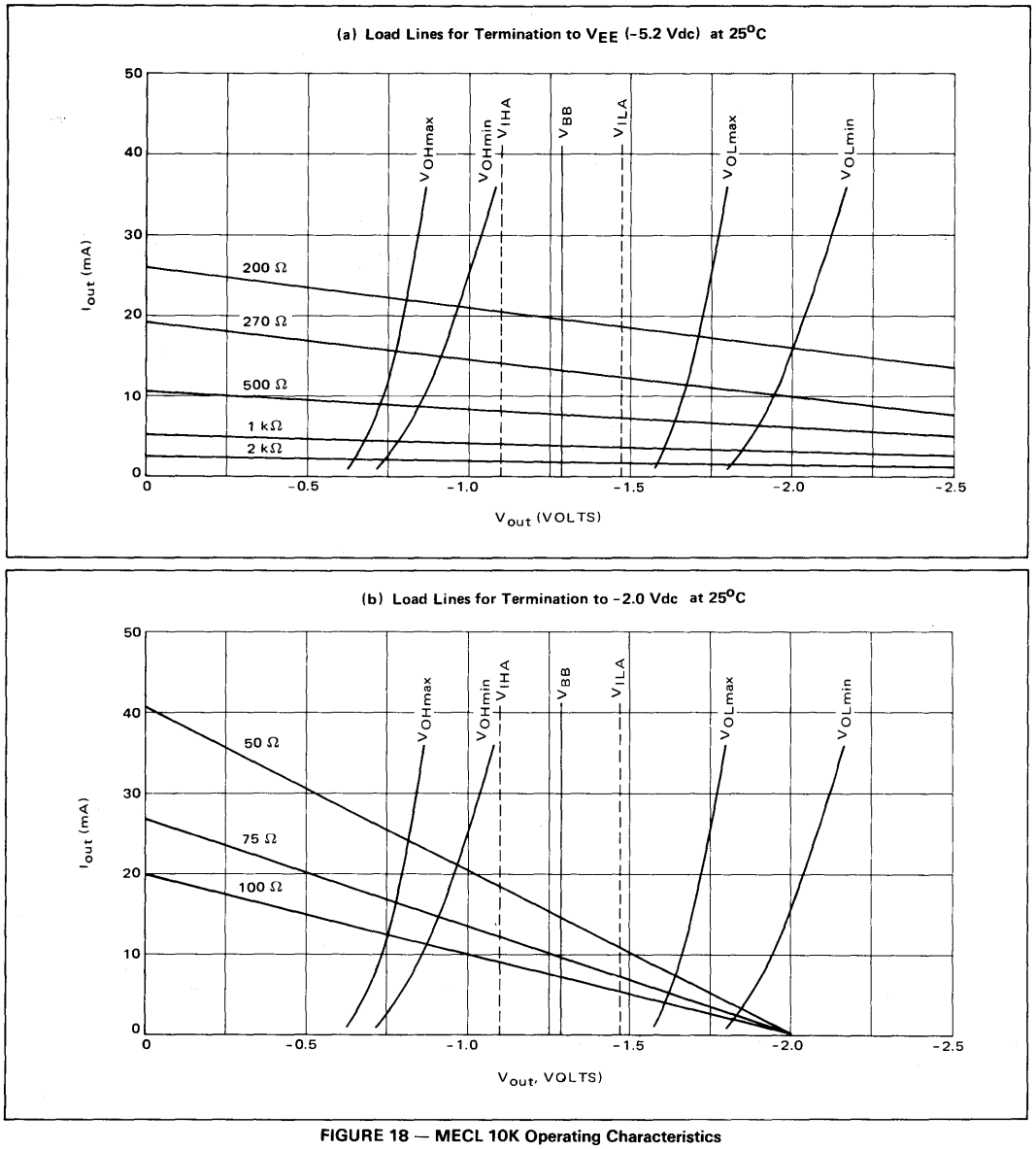


FIGURE 18 — MECL 10K Operating Characteristics

A second limiting factor in the case of the emitter dot is a dc level shift as the number of dots increase. The wired emitter-followers share current through the pulldown resistor and each additional wired output causes the current in every output to decrease. The logic levels shift upward as device current decreases. As the $\emptyset$ level shifts upward, noise margin may be lost. Figure 18 shows loading curves for a typical MECL 10K output and illustrates the shift in logic levels with output current. The $\emptyset$ level shift and resulting reduction of noise margin may be a greater limiting factor than ac considerations, depending on system requirements.

When using Wire-OR, interconnections should be held to minimum lengths for unterminated lines and parallel terminated lines. For larger numbers of distributed emitter-dots and longer interconnections, a doubly terminated line called a "data bus" may be used. Figure 19 shows an example of a 100-ohm data bus system. The dc loading

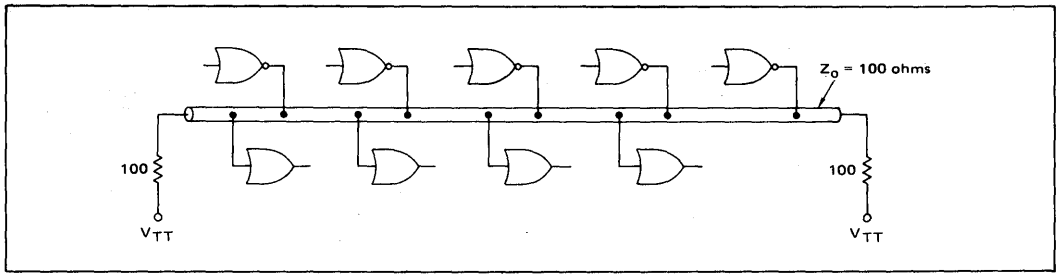


FIGURE 19 – 100-ohm Data Bus Line

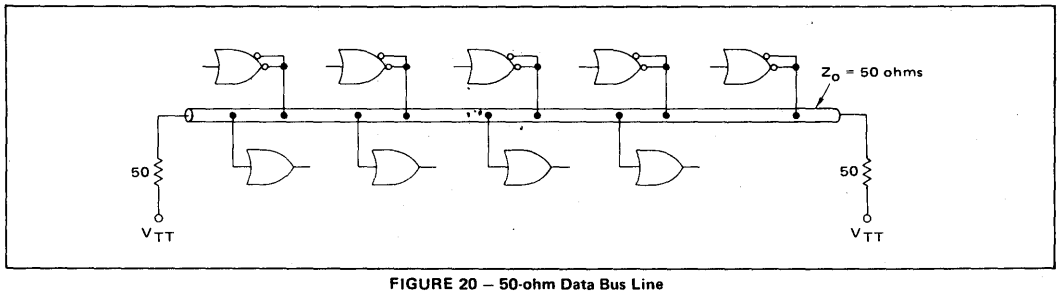


FIGURE 20 – 50-ohm Data Bus Line

on the line is 50 Ω as the 100 Ω terminating resistors are in parallel. However, for a transient waveform driven from any point on the line, the waveform travels to either end of the line and is properly terminated, so reflections are eliminated.

A lower impedance system is better for driving the high capacitive loading of a bus system. A 50 Ω system similar to the 100 Ω system is shown in figure 20. Notice that the drivers for the 50 Ω line must have two outputs in parallel to drive the 25 Ω dc load of the paralleled 50 Ω terminating resistors. The MC10110/or MC10111 multiple output gates may be used conveniently in this application.

When considering system timing, it must be noted that a long bus will add delay time to a data path. The worst case length on the bus, plus the effects of capacitive loading, should be considered for delay time. More will be said on bussing in the following section on board-to-board interconnections.

(3) Clock distribution – Clock lines usually handle the highest frequency in a system. For large fanout, a distribution tree should be used for maximum frequencies (figure 21). A good rule of thumb is to limit fanout to 4 per line and use as low an impedance line as possible. Parallel terminated lines or series damped lines (as in figure 13) may be used. A parallel terminated 50 Ω line with a fanout of 4 will drive a clock line to a frequency of about 110 to 120 MHz.

For higher clock frequencies, series terminated lines with fanout limited to 1 or 2 may be used; line lengths should be kept short and of equal length. A MECL III gate with faster edges will provide highest clock frequency capability.

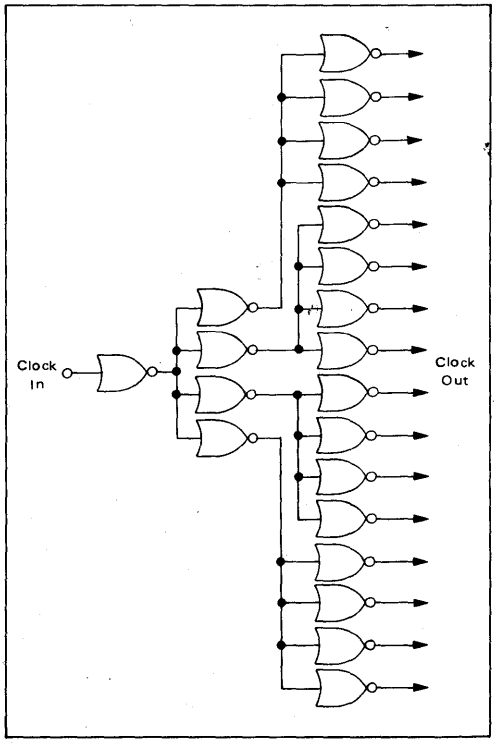


FIGURE 21 – Distribution Tree for a Clock Line with Large Fanout

BOARD-TO-BOARD INTERCONNECTS

Signal connections among logic cards, card panels, and cabinets are important for maintaining the best possible system performance. Ringing and crosstalk can appear when line lengths are long, or when characteristic impedance varies due to lack of a good ground. Ringing and crosstalk, along with power supply variations and system noise, can seriously affect system operation. To be within system noise margins (as previously mentioned, 125 mV worst case for MECL 10K), maximum undershoot should be less than 100 to 110 mV.

The most practical means for limiting undershoot to less than 100 mV is either to limit line lengths, or else to use matched terminated transmission lines. Line lengths in board-to-board applications are necessarily long; therefore, some kind of terminated line should be used. The edge speeds of MECL 10K/ 10KH permit a choice among several methods for producing nominally constant impedance interconnections. Coaxial cable, mother-daughter boards, striplines, and wire over ground may be used.

When designing system interconnections, four parameters must be taken into consideration.

(a) propagation delay per unit length of line;
(b) attenuation of the line;
(c) crosstalk between lines;
(d) reflections due to mismatched impedance between the line and the line termination.

Propagation delay of the line is significant because unequal delays in parallel lines cause timing errors. Moreover, on long lines the total delay time will seriously affect system speed. Since the propagation delay of one foot of wire is approximately equal to the propagation delay of a MECL 10K Series gate, line lengths must be minimized when a total system propagation time is of concern.

Attenuation is a characteristic of the line which increases for high frequency signals, due to higher impedance in the line. Attenuation first appears as a degradation in edge speed, then as a loss of signal amplitude for high frequencies on long lines. Within a backplane attenuation seldom is a problem, but it must be allowed for when interconnecting panels or cabinets.

Crosstalk is the coupling of a signal from one cable to a nearby cable. A coupled pulse in the direction of undershoot gives a reduction of noise immunity and should be avoided. A good ground system together with shielding is the best method for limiting crosstalk. Differential twisted pair line connections avoid problems of crosstalk by virtue of the common mode rejection of line receivers.

Reflections due to mismatched lines also cause loss of noise immunity. Successful termination of a line depends on how constant the impedance is maintained along the line. Coaxial cable is easier to terminate than open wire because of its constant impedance. In many cases twisted pair cable and ribbon cable may be purchased with specifications on the impedance of the line.

Conventional edge connectors may be utilized to get on and off PC boards with little mismatch in line impedances. Coaxial cable connectors which have excellent characteristics across the bandwidth exhibited by MECL 10K/ 10KH exist in a variety of types. The most popular types are BNC, and subminiature types such as SMA, SMB, or SMC.

SINGLE-ENDED LINES

Single ended lines are interconnections such as coaxial cable or other single path transmission line as opposed to a twisted pair of lines over which a differential signal is sent. To maintain some kind of constant impedance, a ground must be present. A ground plane may not be present for board-to-board interconnects, and so a ground must be run together with the signal line.

Types of single ended lines are discussed in the following paragraphs.

(1) Coaxial Cable – The well defined characteristic impedance of coaxial cable permits easy matching of the line, and the ground shield internal to the cable minimizes crosstalk between lines. In addition, low attenuation at high frequencies allows the cable to transmit the rise times associated with MECL signals.

Bandwidth and attenuation are the limiting factors in using coaxial cable. The bandwidth required for MECL 10K is:

$$f \approx \frac{0.37}{\text{rise time}};$$

$$\approx \frac{0.37}{3 \times 10^{-9}};$$

$\approx$ 125 MHz bandwidth for 50 Ω load.

Attenuation is due mainly to skin effect in the cable. The loss in signal amplitude due to attenuation will limit the maximum usable length of line. For a maximum signal reduction of 100 mV from the logic 1 and $\emptyset$ levels (800 mV p/p to 600 mV p/p) the permissible attenuation is 2.5 dB:

$$\text{dB} = 20 \log \left(\frac{V_{in}}{V_{out}} \right) = 20 \log \left(\frac{0.8}{0.6} \right) = 2.5 \text{ dB}.$$

The maximum line length which will produce no more than 2.5 dB attenuation will be:

$$\text{max length} = 100 \text{ ft.} \left(\frac{2.5 \text{ dB}}{\text{Atten.}} \right),$$

where Atten. is the cable attenuation in dB/100 ft. at the operating frequency.

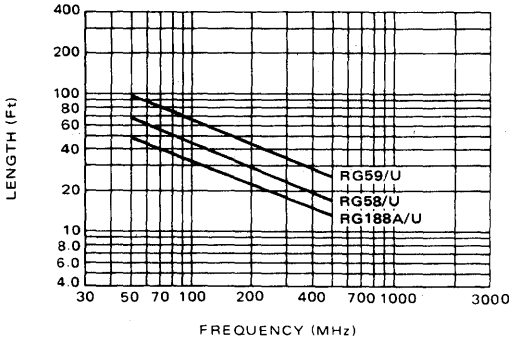


FIGURE 22 – Coaxial Cable Length versus Operating Frequency: Constant 2.5 dB Loss Curves

Figure 22 shows curves for maximum line lengths versus operating frequencies for a 2.5 dB loss. Data for three cable types are plotted. A high bandwidth line is necessary to preserve fast signal edges regardless of the bit rate of a system.

In figure 22 it is assumed that the coaxial line is properly terminated with a resistive load equal to the characteristic impedance of the line. Standard carbon 1/8 or 1/4 watt resistors work well for all line terminations. However when using precision wire-wound or film resistors, care should be taken to determine the high frequency properties of these devices since they may become highly inductive at high frequencies, and thus be unusable.

Coaxial cable should be used for sending single-ended signals over long lines. The constant impedance and low attenuation of such cable allows transmission of signals with minimum distortion.

(2) Parallel Wire Cable – Multiple conductor cable as purchased, or as constructed by lacing interconnecting wires together, is not normally used with MECL or other high speed logic types because of crosstalk. Such crosstalk is due to the capacitive and inductive coupling of signals between parallel lines. Such cable is also susceptible to external signals coupling to the entire cable. Multiple conductor, single-ended cable is not recommended for use with MECL unless individual shields on each wire are employed.

(3) Ribbon Cable – Systems requiring large numbers of board-to-board interconnections may take advantage of multiconductor ribbon cable (figure 23). Ribbon cable is easily wired to connectors because of its in-line wire arrangement. Its flexibility permits easy routing and board removal. The side-by-side arrangement of signal lines produces a defined characteristic impedance because of the presence of alternate ground wires.

Commercial ribbon cable is available with a wide variety of characteristic impedances, and the manufacturer should be consulted for information on such cable parameters as attenuation, characteristic impedance, and number of conductors.

With ribbon as with coaxial cable, the maximum permissible attenuation is 2.5 dB. Attenuation per foot is generally higher for ribbon cable than for coaxial cable. Consequently maximum line lengths for ribbon are limited by operating frequency.

(4) Point-to-point Wiring – A system made up of several logic cards may be assembled using edge connectors to form a card file. Point-to-point wiring via the board connectors may then be used for system interconnections.

A ground plane is often formed by a large printed circuit board to which the card connectors are mounted. The ground plane may be connected to the frame holding the card connectors. Metal is left on one side of the PC board to form the backplane system ground, or metal may be left on both sides of the board to supply power to the system logic cards. These card file systems are commercially available from a number of manufacturers.

When a solid ground plane is not practical, a ground screen should be constructed on the backplane. A ground screen may be made by connecting bus wires (wire size compatible with connector) to the edge connectors in a grid pattern, prior to signal wiring (figure 24). About every sixth pin on the card edge connectors is used as a ground, providing connection points for the ground grid. This interconnection of ground points forms a grid network of approximately 1 inch squares over which the signal lines are wired. A characteristic impedance of about 140 ohms can be expected for a wire over ground screen, depending upon the exact routing and distance from the screen.

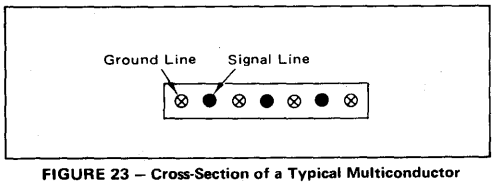


FIGURE 23 – Cross-Section of a Typical Multiconductor Ribbon Cable

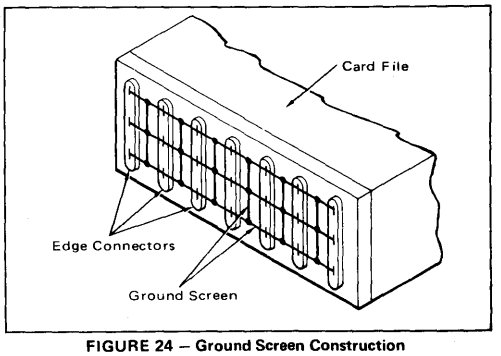


FIGURE 24 – Ground Screen Construction

To provide maximum signal purity, a motherboard composed of multilayer or two layer board may be used to mount the card connectors. Striplines or microstrip lines are designed on the circuit board, along with ground and voltage planes. Connectors are available to interface between cards and the motherboard with little line discontinuity. The motherboard technique is normally used when the system design is sufficienty determined that changes in the backplane wiring will be few.

When using point-to-point wiring with a ground plane or screen, soldered connections or wire wrap techniques may be used. In general one good terminating technique is to parallel terminate with approximately 100 to 120 Ω to - 2 volts. The resistor will be near the characteristic impedance of the line and so minimize ringing. Series damping or termination may be used, following the rules presented previously. An unterminated line with a fanout of 4 may be up to 15 inches long when a ferrite bead is placed at the sending end of the line.

For high speed lines, such those for clock distribution, coaxial cable and twisted pair lines should be used between cards. Maximum signal integrity of clock signals should be maintained for best system performance.

DIFFERENTIAL TWISTED PAIR LINES

Twisted pair lines, differentially driven into a line receiver (figure 25), provide maximum noise immunity. Any noise coupled into a twisted pair line appears equally on both wires (common mode). Because the receiver senses only the differential voltage between the lines, crosstalk noise has no detrimental effect on the signal up to the common mode rejection limit of the receiver. The line receivers MC10115, MC10116, MC10H115 and MC10H116 have a common mode rejection limit of 1 volt to a positive-going common mode signal, and 2.5 volts to a negative-going common mode signal.

The partial schematic of an MC10115 line receiver is shown in figure 26. Each receiver is a differential amplifier whose output level is dependent on the input voltage differential. If the inputs, IN1 and IN2, are at the same voltage, the output will be at the mid point of a MECL 10K/10KH logic swing; that is, at -1.3 V = V_{BB} (note that a pulldown resistor on the output is necessary). The output voltage will go more positive as input IN2 goes more positive than input IN1; that is when the differential voltage from IN2 to IN1 is plus to minus. The inverse is also true. The output goes more negative than V_{BB} when the polarity of the differential voltage from IN2 to IN1 is minus to plus (cf figure 26b).

The output voltage change of the receiver is equal to the input voltage differential times the voltage gain of the amplifier. To have a full MECL swing, the output must swing ±400 mV about V_{BB}. Therefore, with the voltage gain of the differential amplifier typically 6 V/V, the minimum input differential must be approximately: 0.4 V/6 = 67 mV (either plus to minus or minus to plus.)

For system design, other factors affect the minimum differential input voltage. Decreasing voltage gain with increasing frequency (figure 27), offset voltage of the am-

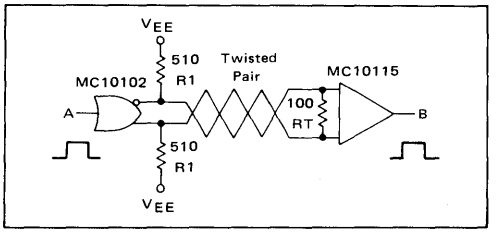


FIGURE 25 – Twisted Pair Line Driver and Receiver

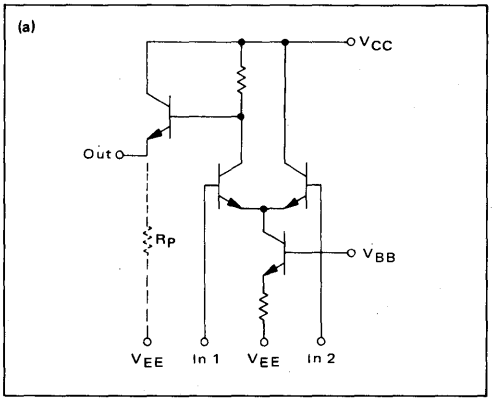


FIGURE 26 – 1/4 MC10115 Circuit Schematic

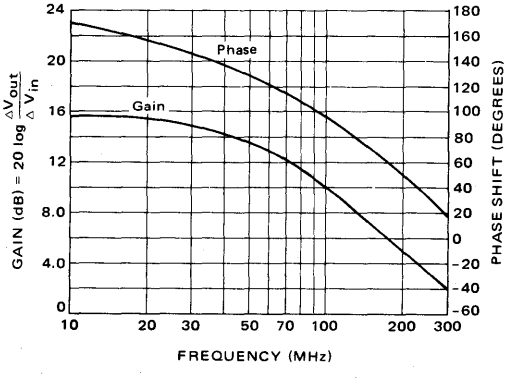


FIGURE 27 – Typical Gain and Phase Characteristics for MC10115 Line Receiver

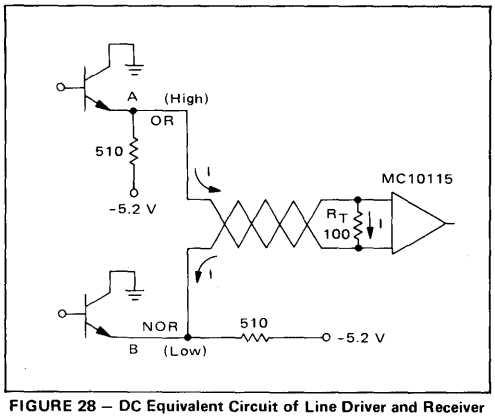


FIGURE 28 – DC Equivalent Circuit of Line Driver and Receiver

plifier, noise, and other system parameters demand a larger input differential voltage. A minimum differential input voltage of 150 mV at maximum frequency is recommended for system design.

Except at slow bit rates, attenuation will be the limiting factor for twisted-pair line length. The dc equivalent of the twisted pair line of figure 25 is shown in figure 28. Ignoring the dc resistance in the line, the voltage across the terminating resistor is:

$$V_{RT} = \frac{(5.2\ V - 0.9\ V)\ (100\ \Omega)}{510\ \Omega + 100\ \Omega},$$

$$= 0.705\ V.$$

Note that if V_{RT} becomes as large as 800 mV and begins to go below a logic ∅ level of - 1.7 V, the NOR output will clamp the voltage at node B.

The voltage across the terminating resistor decreases as frequency increases due to attenuation in the line. Figure 29 tabulates the maximum differential voltage appearing across the termination resistor, versus frequency for a 50 ft. line as shown in figure 25. Maximum line length will be determined by operating frequency.

A different termination method for a twisted pair line is shown in figure 30. The pulldown resistors terminate the line. As a result, full output levels are presented to the receiver. Attenuation data for this line is shown in figure 31. Waveforms for input and output signals for both termination methods are pictured in figure 32.

FIGURE 29 – Attenuation of 50 Ft. of Twisted Pair Line with MC10102 and MC10115

FREQUENCY (MHz)	MAX DIFFERENTIAL VOLTAGE AT R_T (mV)
25	520
50	420
75	325
100	235
125	165

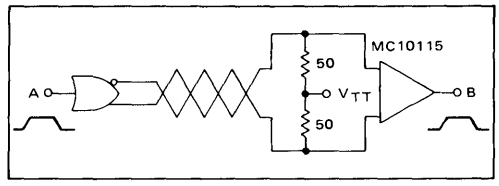
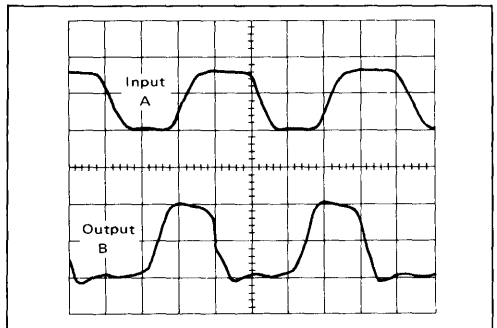


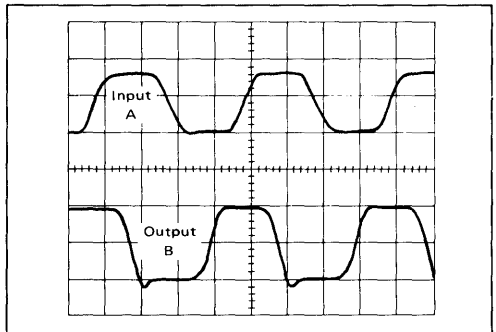
FIGURE 30 – Twisted Pair Line with Pulldown Resistors As Equivalent Termination Resistor

FIGURE 31 – Attenuation of 50 Ft. of Twsited Pair Line Driven By an MC10102 with 50-ohm Pulldowns

FREQUENCY (MHz)	MAX DIFFERENTIAL VOLTAGE AT R_T (mV)
25	600
50	475
75	350
100	240
125	175



(a) 510-ohm Pulldowns (cf Figure 25)



(b) 50-ohm Pulldowns (cf Figure 30)

FIGURE 32 – Waveforms for 50 Feet of Twisted Pair Lines at 50 MHz

A variety of cable types can be used with differential twisted pair lines:

(1) Bundled twisted pair cable – Cable with several bundled twisted pairs is commercially available. When running MECL signals in parallel with higher voltage analog or logic signals, shielded twisted pair lines should be used. Shielded twisted pair lines have foil shield on each twisted pair that may be tied to the system ground.

(2) Ribbon cable – Ribbon composed of several twisted pairs is one type of ribbon cable available. Conventional side-by-side cable (figure 23) may also be used with differentially driven signal lines (figure 33). With every other wire grounded, the signal lines will have a constant characteristic impedance.

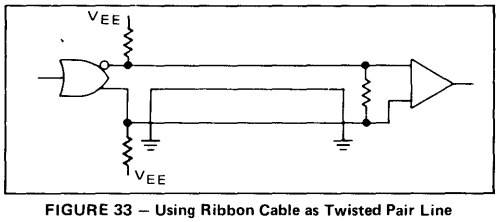


FIGURE 33 – Using Ribbon Cable as Twisted Pair Line

Differential twisted pair lines offer several advantages under adverse conditions compared to single ended lines. For example, power supply and temperature variations might occur between panels or between cabinets of a system. Corresponding shifts in logic levels within the system will subtract from noise margins when driving single ended lines between these points in the system. However, differential lines are unaffected by variation in logic levels, since the receiver detects only the differential voltage between the driver outputs, rather than detecting absolute logic levels.

With single ended lines, noise generated on the signal line by crosstalk and inductive coupling directly reduces noise immunity. Noise is coupled equally onto both wires of a twisted pair line, so the differential voltage is unaffected. As a result, the receiver will not detect noise as long as it is within the common mode range of the receivers.

DATA BUSSING AND PARTY LINE TECHNIQUES

Data bussing usually requires large fanout, long lines, and several driving points. A MECL 10K/10KH bus or "party line" may be made by emitter-dotting gates together, with the restriction that only one driver is allowed to go high at one time.

Figures 19 and 20 illustrate data bus lines which may be extended for board-to-board use. The characteristic impedance of board-to-board interconnections will generally be from 100 to 150 ohms so the termination resistors must be adjusted accordingly.

Another scheme for bussing is the twisted-pair party line of figure 34. The driving gates are emitter-dotted. It is required that all their outputs be held low when not sending data. (V_{BB} is available from the MC10115/H115 and MC10116/H116, and may be buffered as shown in figure 35 to handle the necessary termination current).

In both bussing schemes the driving lines are operating single ended. However, the twisted pair bus retains the advantage of the common mode rejection of the line receivers. As previously mentioned, the limiting factors for emitter-dotting also apply to the party lines shown.

WIREWRAPPING TECHNIQUES

The versatility of MECL 10K/10KH allows the use of this logic family with wirewrapping techniques. Wirewrapping is popular for breadboarding large system prototypes and for interconnecting system logic boards. The ability to change system interconnections easily has made wirewrap extremely usable for breadboarding new system designs.

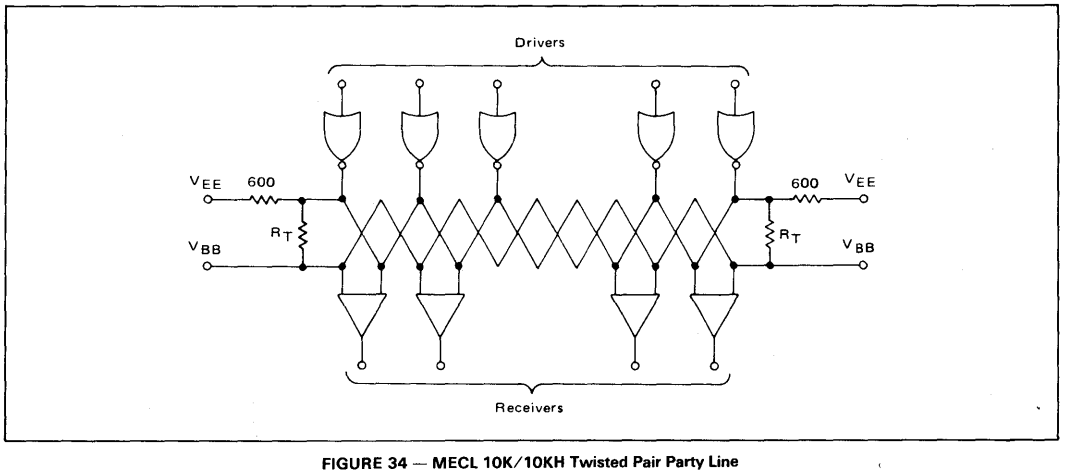


FIGURE 34 – MECL 10K/10KH Twisted Pair Party Line

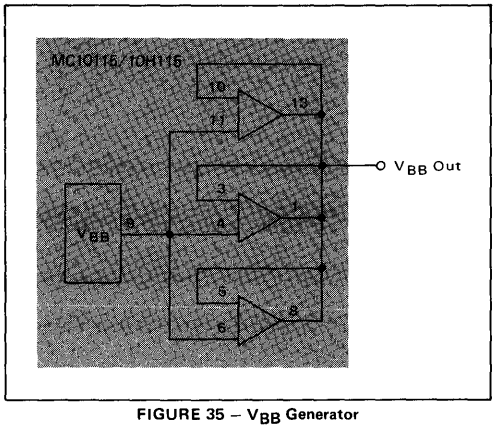


FIGURE 35 – V_{BB} Generator

MECL 10K/10KH systems may be wirewrapped using high density dual-in-line packaging boards. In addition, wirewrapping may be used for board-to-board interconnections when the logic boards are mounted in a card file in edge connectors. Some general guidelines for use of MECL 10K/10KH with wirewrap follow:

SYSTEM PROTOTYPING — Several types of wirewrap boards for dual-in-line packages are commercially available. For MECL 10K/10KH systems, a board should be used that has voltage planes on both sides of the board and low-profile device mounting. Device mounting via pins set in the boards is the most satisfactory method.

The V_{CC} pins of the device mounting should be soldered to the V_{CC} voltage plane (the voltage plane on the device side of the board is the best choice.) When the V_{CC} pins are wirewrapped to the V_{CC} voltage source, a ferrite bead on a wire between the V_{CC1} and the V_{CC2} pins of the same package will help avoid high frequency noise and will prevent possible oscillation. Long leads from the ground plane to the V_{CC} pins help induce oscillation and noise, due to their added inductance. V_{EE} pins may be wirewrapped to the V_{EE} voltage plane with no detrimental effects. Bypassing on the board should be provided in a manner similar to that mentioned for a two-sided PC board with a ground plane.

Wiring rules for wirewrapped interconnections are similar to those for a wire over ground. If a voltage plane is present, the characteristic impedance of a wirewrap interconnection is 100 to 150 ohms. Parallel termination, series damping, and unterminated lines may all be used, and the unterminated line lengths of figure 8 (backplane) also apply to wirewrap. However, in prototyping and breadboarding these lengths may be extended if low bit rates are present or if greater ringing is acceptable. When doing prototype breadboarding, the designer is often concerned with the "workability" of the design, as opposed to operation with best noise margins and signal waveforms.

With wirewrap, the pulldown resistors may be provided by commercial resistor networks in a dual-in-line package or via adaptor plugs. Many manufacturers are marketing resistor networks in a variety of values suitable for MECL 10K/10KH terminations. Resistor networks with good high frequency characteristics should be used. Networks composed of discrete resistor chips mounted in a package, or thick-film cermet resistors with a minimum of interconnect metal within the package, provide the best high frequency characteristics. Wirewrap equipment manufacturers have made dual-in-line adaptor plugs available, to allow discrete components to be mounted for use on the wirewrap board (cf figure 36).

An example of a wirewrap system is shown in figure 37. A 4 x 4 bit multiplier (figure 38) was constructed using MECL 10K. The delay line oscillator has a frequency of 30 MHz and the total multiplication cycle time is about 175 ns. The multiplier uses an add-shift algorithm.

The clock distribution for this system used a parallel terminated wirewrap line (Thevenin equivalent). Twisted pair lines may also be used for clock distribution, and are helpful for higher clock rates. With wirewrap, maximum clock rates are in the neighborhood of 100 MHz, when using twisted pairs.

To get signals on and off the board, commercially available multiconductor ribbon cable was utilized. Commercial cable adaptors, which plug into the wirewrap board, are available. Alternate lines are grounded to minimize crosstalk and generate a characteristic impedance for the signal lines.

BACKPLANE WIREWRAP A card file composed of several logic cards may use wirewrap for board-to-board interconnection. The same rules as discussed in the section, SINGLE-ENDED LINES #4 for board-to-board interconnects, apply to wirewrap. A ground plane or ground screen is recommended; termination techniques and line lengths should follow the rules previously presented.

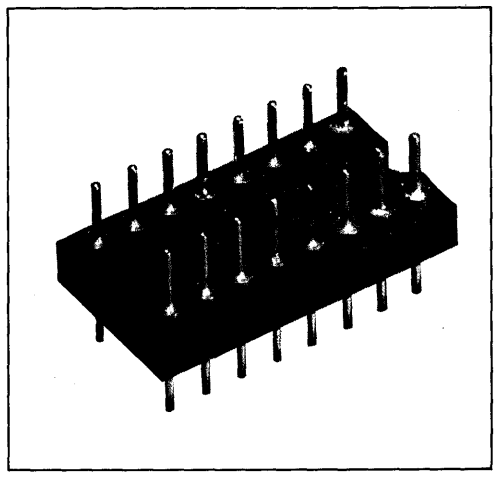


FIGURE 36 – Dual-in-line Adaptor Plug for Mounting Discrete Components.

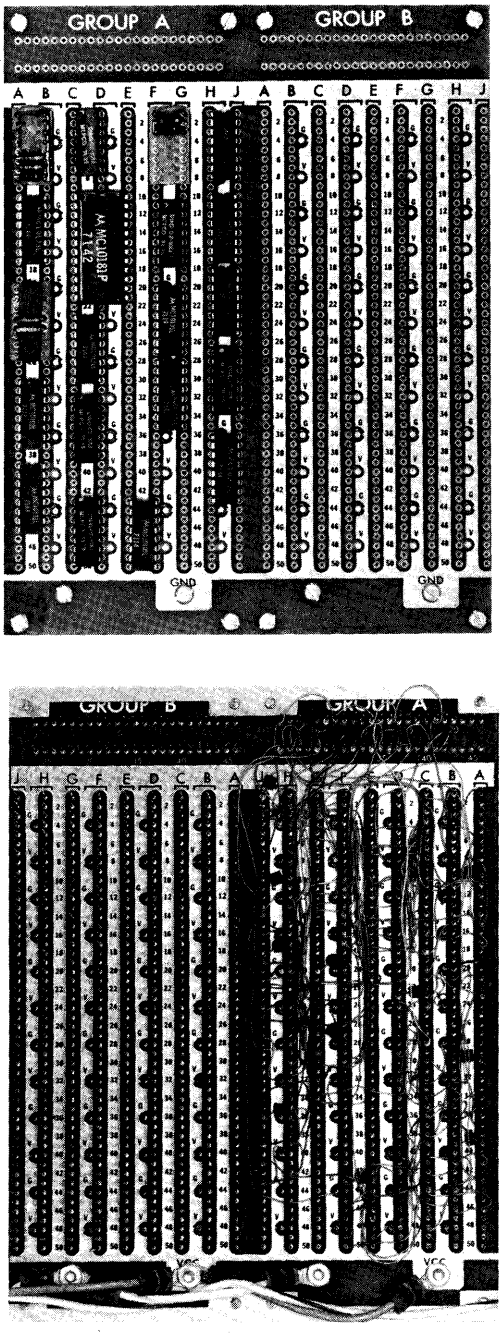


FIGURE 37 — 4 x 4 Bit Multiplier Prototype Showing Wirewrap with MECL 10K Logic

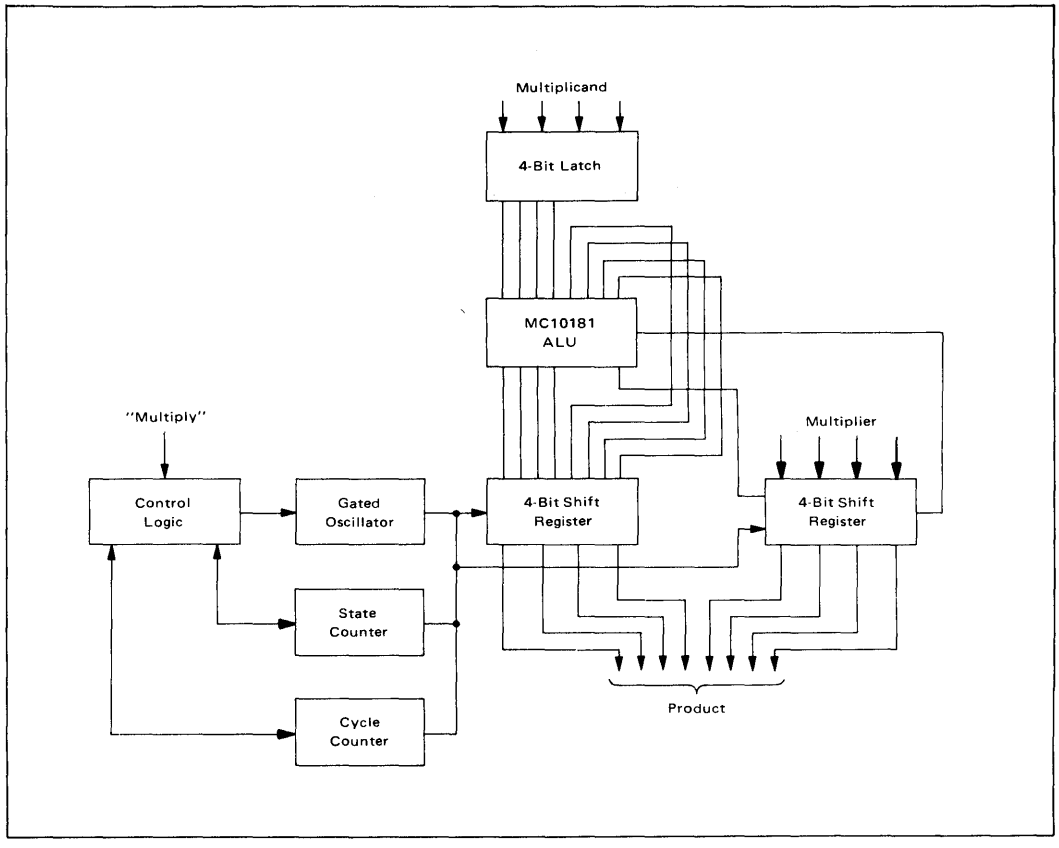


FIGURE 38 — 4 x 4 Bit MECL 10K Multiplier

CONCLUSION

This application note has been written to present information which a designer may use to construct a reliable, high performance MECL 10K system. Much of the transmission line theory that explains the effects of high speed signals on interconnects has not been presented here because the application note is directed toward usage rules rather than a detailed theoretical discussion.

AC NOISE IMMUNITY OF MECL 10K INTEGRATED CIRCUITS

INTRODUCTION

For reliable system operation it is necessary to keep noise in a system below the noise tolerance levels of the logic circuits. Motorola specifies worst case dc noise margins for all MECL circuits on the component data sheets. High level noise margin for MECL 10K is defined as the difference between V_{OHA} min and V_{IHA} min which is 125 mV. Low level noise margin, defined as the difference between V_{ILA} max and V_{OLA} max, is 155 mV. These numbers may be used for worst case design when calculating steady state conditions such as power supply losses through the system. While designing for worst case the designer may also wish to use dc noise margins when considering transient conditions such as crosstalk and ringing, however these noise margin values may be unnecessarily restrictive. The MECL circuits have a response time to transient conditions which may be used to ease the design rules for this type of noise. The response characteristics of MECL 10K circuits to transient noise is the topic of this application note.

Because of the large number of circuit types in the MECL product line this note will not characterize all parts. Worst case AC noise immunity is not specified because of final test considerations. Therefore, the following test results should be considered typical rather than worst case. Anyone interested in determining this type of information for other MECL parts is encouraged to build similar test fixtures and perform noise immunity tests on these parts.

TEST CIRCUITS

Transient noise can enter a MECL circuit at one or more of four different points. These are: at the input to a circuit; on V_{CC}, which is normally ground; on V_{EE}, which is normally -5.2 Vdc; and on the termination voltage, V_{TT}, which is normally -2.0 Vdc. The response of the MECL circuit to noise depends on where the noise enters. For this reason separate tests are used to measure the response of a circuit to induced noise.

A test circuit for measuring noise immunity to a transient signal on an input line is shown in Figure 1. As is characteristic of MECL testing, the text fixture puts +2.0 V on V_{CC} and -3.2 V on V_{EE}, to permit terminating the MECL outputs to ground through a 50 Ω 'scope probe. This has proven to be the most accurate method for testing MECL 10K and MECL III because possible problems with high impedance scope probes are eliminated.

Both V_{CC} and V_{EE} are capacitor bypassed to ground to eliminate noise at these points. If the oscilloscope's 50-ohm input will handle the HIGH logic level (about +1.1 volts) accurately, the MECL circuit outputs may be connected directly to the oscilloscope inputs. If not, 2:1 attenuation resistors and 100-ohm pulldown resistors may be used as shown in the figure.

The input of the test circuit is arranged to utilize an accurate bias, provided by a power supply, to set the input logic levels. The pulse generator is terminated by a 51-ohm resistor and is capacitor-coupled to the input pin, to induce a noise pulse. An inductor, made of four turns of wire wound around a ferrite bead, isolates the noise from the input-bias source.

A 450-ohm resistor is used in series with the 50-ohm 'scope input to isolate the input from the 'scope. This results in a 10:1 amplitude attenuation, but still gives an accurate picture of the input noise.

The response of MECL circuits to noise on the V_{CC} line is tested in a manner similar to that for input noise. A test circuit for V_{CC} noise is shown in Figure 2. A power supply is again connected to the circuit input to set the HIGH and LOW logic levels. The pulse insertion network is connected to V_{CC} pins 1 and 16. Since good MECL design practice is to tie both V_{CC} pins to a common ground, tests were not conducted for signals inserted on only one V_{CC} pin.

A slightly more complicated test circuit, Figure 3, was used to measure response to noise on V_{EE}. A PNP transistor is connected as an emitter-follower to provide a low-impedance V_{EE} path. The high speed pulse generator is capacitor-coupled into the base of the transistor. Because of the large signals required on V_{EE} to affect the circuit outputs, the emitter-follower transistor is used to allow better termination of the pulse generator than with the generator driving the V_{EE} pin. V_{EE} noise amplitude is approximately equal to the maximum pulse output of the pulse generator used. A very high speed MM4049 transistor or equivalent should be used to retain the fast pulse edge speed.

V_{TT} noise tests were made with the circuit shown in Figure 4. Power supplies are connected to V_{CC}, V_{EE}, and the circuit input. Bypass capacitors are used to keep noise from these points. The output of the test circuit is arranged to insert noise on V_{TT}. For this test, the 51-ohm termination resistors are connected to ground through an inductor. The induced pulse is capacitor-coupled to the V_{TT} point.

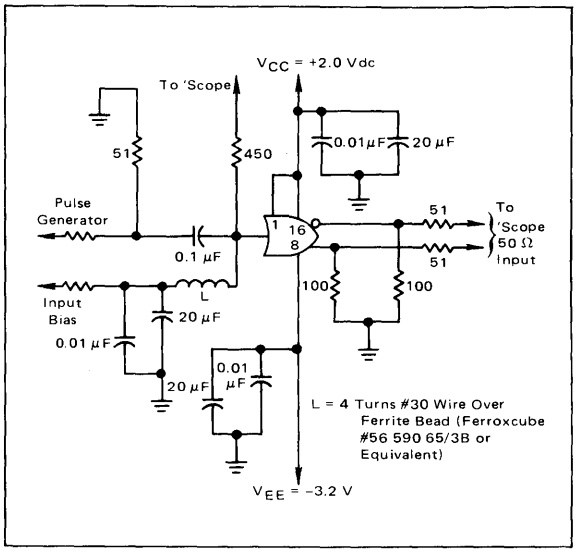


FIGURE 1 – INPUT NOISE TEST CIRCUIT

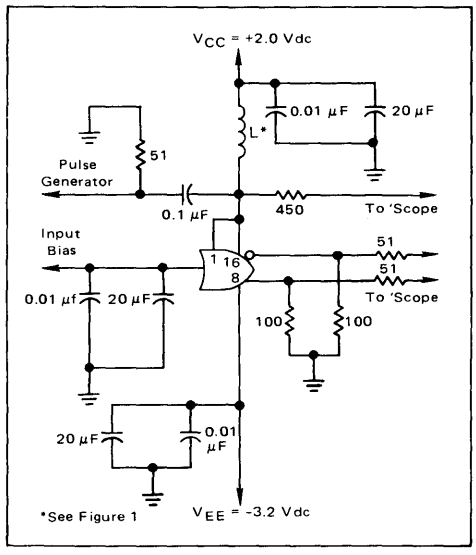


FIGURE 2 – V_{CC} NOISE TEST CIRCUIT

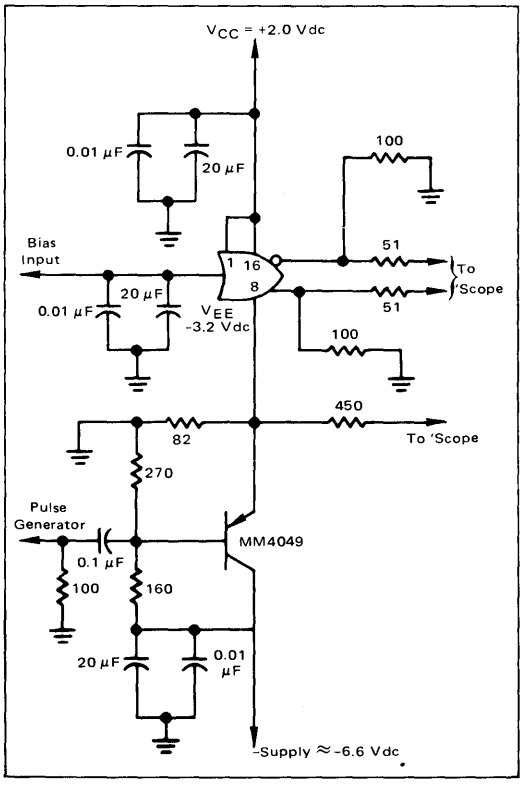


FIGURE 3 – V_{EE} NOISE TEST CIRCUIT

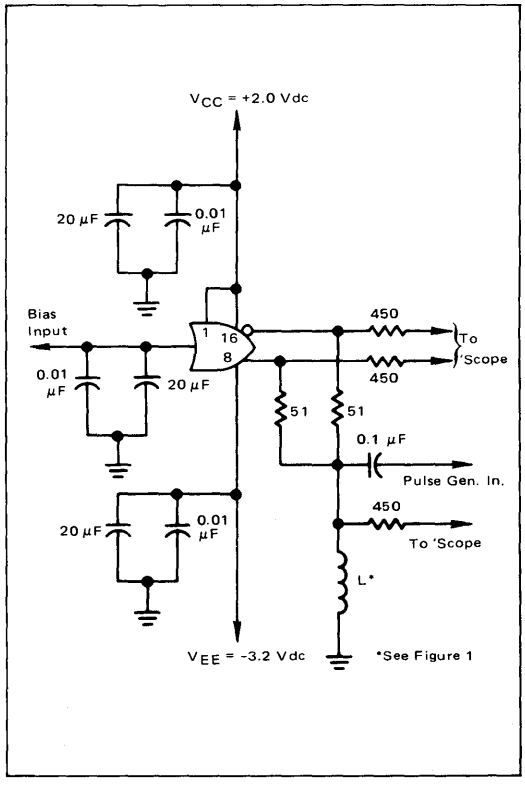


FIGURE 4 – V_{TT} NOISE TEST CIRCUIT

Circuit outputs are isolated from the 50-ohm oscilliscope inputs by 450-ohm attenuation resistors. These resistors prevent the MECL circuit from driving both the 51-ohm resistors to V_{TT}, and the 50-ohm 'scope input.

TEST CONDITIONS

The test limits chosen to determine noise immunity of typical MECL 10K parts are based on the specified voltages shown on component data sheets. The circuit output was allowed to move to the input threshold points before the noise amplitude was considered a maximum. The HIGH logic level was allowed to drop to V_{IHA}, 0.895 volts, and the LOW level to rise to V_{ILA}, 0.525 volts, (voltage given for V_{CC} at +2.0 V).

These two points were chosen because the outputs of a circuit with these input levels are defined by the threshold voltages on data sheets. Output test limits should be determined by the tester when evaluating parts for specific test information.

The input bias points were set at normal test voltages. These are +1.11 V for a HIGH logic level and +0.31 V for a LOW level. With these inputs, the outputs of the circuits under test averaged the following levels: V_{OH} "OR" = 1.100 V; V_{OH} "NOR" = 1.099 V; V_{OL} 'OR" = 0.290 V, and V_{OL} "NOR" = 0.265 V.

Using the limits described above the following transitions were allowed on the outputs before maximum noise was reached: ΔV_{OH} "OR" = 0.205 V; ΔV_{OH} "NOR" = 0.204 V; ΔV_{OL} "OR" = 0.235 V; and ΔV_{OL} "NOR" = 0.260 V. This technique for reading output transition amplitudes is used because it is more convenient than reading DC values on an oscilloscope.

The tests are conducted by setting the power supplies and circuit inputs into the quiescent conditions. A pulse width is selected. Then the amplitude of the pulse generator is increased until the output reaches the predetermined limit. The pulse width is then changed and the test repeated.

To generate the narrow pulses used in the tests, a very high speed pulse generator (EH 129 or equivalent) was used. This generator is capable of 500 MHz operation and has pulse edges of about 0.5 ns rise time. This represents worst-case noise conditions, because this edge speed is much faster than would be expected in a MECL system.

TEST RESULTS

Typical noise immunity for a MECL 10K gate is shown in Figure 5. A pulse is applied to the circuit input and the pulse amplitude and width are measured to determine the tolerance limits previously defined. The average is shown by the solid line which levels at about 370 mV for a 6 ns pulse width. The curve is relatively flat to about 3 ns, then rises sharply as the circuit becomes bandwidth limited.

Test results have shown that there is some deviation from the single line shown, due to variations in V_{BB} from the exact center voltage of 0.71 V. When this happens there will be two curves as shown by the dotted lines in Figure 5. V_{OH} OR and V_{OL} NOR would follow one curve, and V_{OL} OR and V_{OH} NOR the other. For example, if V_{BB} were 30 mV low, V_{OH} OR and V_{OL} NOR would follow the upper dotted curve.

This behavior can be explained by the MECL transfer curves shown in Figure 6. The heavy vertical lines show the nominal input test levels. The outputs must move to the heavy horizontal lines. Under conditions (greater than about 6 ns pulse width), the circuit follows the transfer curve. A low level input has to move from +0.31 volts to about +0.67 volts before the output noise limit is reached. Similarly, a high input has to move from 1.11 volts to about +0.74 volts before the maximum output change is reached. This gives about 370 mV noise margin, as shown in Figure 5. If V_{BB} is slightly to one side of the 0.71 V nominal value, the transfer curves shift slightly

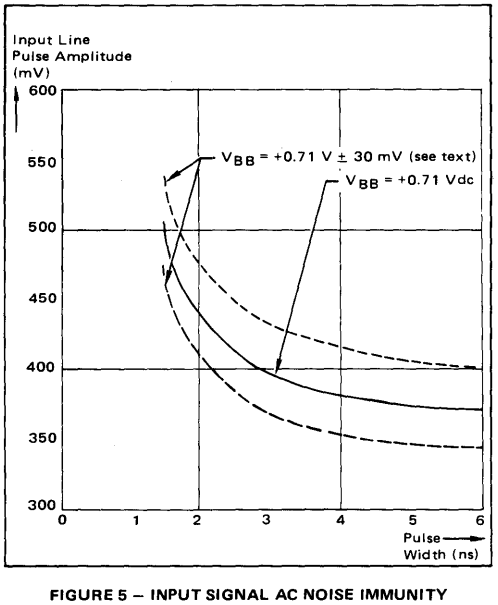


FIGURE 5 – INPUT SIGNAL AC NOISE IMMUNITY

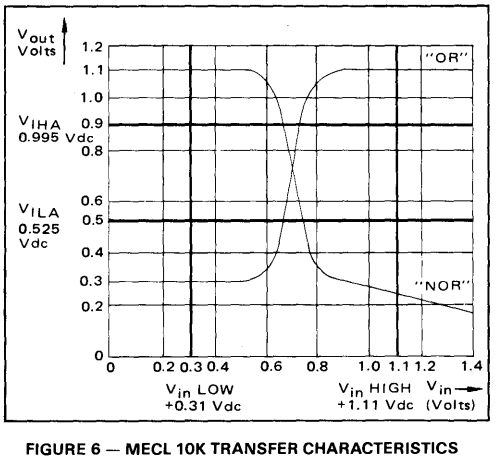


FIGURE 6 — MECL 10K TRANSFER CHARACTERISTICS

to the left or right. This causes the dotted curves of Figure 5.

Noise immunity to transients on the V_{CC} supply line is shown by the curves in Figure 7. The tests are made by applying a negative pulse to V_{CC} when the tested outputs are at a HIGH logic level, and a positive pulse when at a LOW level output. The circuits are most susceptible to negative noise spikes on V_{CC} affecting the HIGH logic levels.

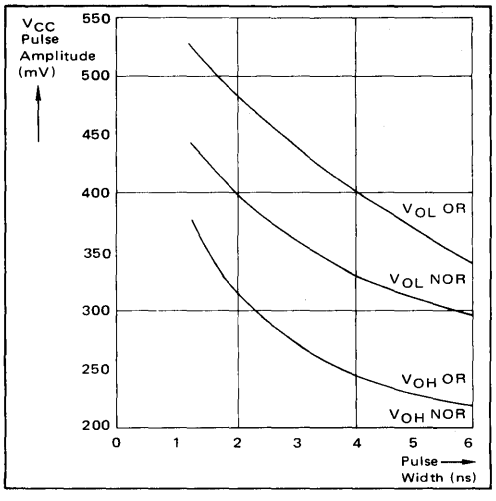


FIGURE 7 – V_{CC} ac NOISE IMMUNITY

For wide pulses there is a one-to-one loss of noise margin with pulse amplitude. At 6 ns, there is about 215 mV of noise immunity. This compares with the 204 mV maximum output transient allowed by the previously defined test limits. For narrower pulses the response time is shown in the figure.

The noise immunity to positive-going pulses is greater than for the negative-going transient in a MECL gate. This can best be explained by the gate schematic shown in Figure 8. A positive going pulse on the V_{CC} lines increase the total voltage across the circuit. With the output at a low logic level, the change in output level to V_{CC} is due to the ratio of R_C to R_E, and to the voltage drop across the switch transistor. In a MECL gate the LOW output will follow V_{CC} at about a 3 to 4 amplitude ratio, i.e., V_{CC} noise is attenuated about 25%. As a result, the degree of coupling of noise on V_{CC} to the outputs is dependent on the output logic level rather than on the direction of the noise signal. However, since HIGH level noise margin is only reduced by a negative signal on V_{CC}, the circuit is more vulnerable to negative going transients than positive ones.

The V_{CC} noise margin is approximately the same for the HIGH level OR and NOR outputs. However, the OR and NOR noise immunities differ when the outputs are at a LOW logic level. This is again explained by the gate schematic of Figure 8. With both inputs LOW, Q1 and Q2 are turned off and Q3 is conducting. With a positive pulse on V_{CC}, V_{BB} goes more positive, insuring that Q1 and Q2 remain off. There is no tendency for the gate to change logic states.

However, when one or both of the inputs are HIGH, the current path is through the Q1/Q2 pair, giving a LOW level on the NOR output. In this case, when V_{BB} rises due to a positive spike on V_{CC}, the difference between V_{BB} and the input signals is reduced. If the noise spike is sufficiently large, Q3 will start conducting some of the

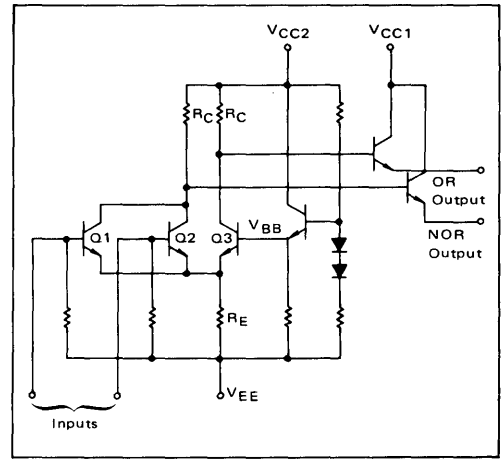


FIGURE 8 – MECL GATE SCHEMATIC

switch current. This in turn causes the NOR output to go more positive. For a positive pulse on V_{CC}, the V_{BB} bias voltage will track the signal with about 85% amplitude.

Another reason for less noise immunity on the NOR output is due to the collector resistors, R_C. The collector resistor connected to the NOR output transistor has a smaller value than the resistor connected to the OR output driver (220 ohms, compared to 245 ohms, typical). This makes the noise attenuation less for the NOR output by the difference in the R_C to R_E ratios.

The noise immunity to transients on the V_{EE} supply line is shown in Figure 9. The tests are performed by applying a pulse on the V_{EE} line, using the circuit shown in Figure 3. The pulse polarity is chosen so that there is a positive pulse on V_{EE} when the output is LOW, and a negative pulse with a HIGH output. The amount of noise immunity in the MECL circuit is dependent on whether the OR or NOR output is tested, and the logic state of the output.

The rate MECL outputs track with V_{EE} depends on the output logic level. The HIGH logic state changes at a rate of about 1.6% that of V_{EE}, making it relatively immune to V_{EE} changes. The LOW logic level is more affected by V_{EE} fluctuations, changing at a rate about 25% that of V_{EE}.

V_{BB} changes at about 15% of V_{EE}. This is not sufficient to shift the transfer curves enough to affect output levels. However, because of the very fast rise and fall times (0.5 ns) of the pulse generator used in these tests,

there is some capacitive coupling between V_{EE} and V_{BB}.

Referring to the schematic in Figure 8 it can be observed that the noise coupling into V_{BB} is seen primarily on the NOR output. Coupling on V_{BB} is toward the input logic level when measuring NOR output noise immunity, and away from the input level when testing to OR outputs.

Example: when testing the NOR output with inputs LOW, the output is HIGH and a negative pulse is applied to V_{EE}. This negative pulse couples into V_{BB} and causes it to move toward the LOW level inputs. If the V_{EE} noise is sufficiently large, both halves of the logic switch will start conducting and the output will move toward the opposite logic state. This gate switching will also be seen on the OR output, but since the V_{EE} pulse is opposite in polarity to the OR output movement, coupling of V_{EE} to the output offsets the effects of V_{BB} transients. Normally, about 2 volts of noise immunity exists for the OR output in this test condition.

From Figure 9 it may be seen that the OR outputs have more noise immunity than the NOR outputs (as would be expected from the V_{BB} coupling). HIGH logic levels are more immune than LOW levels due to the voltage tracking ratio of the output logic levels with V_{EE}.

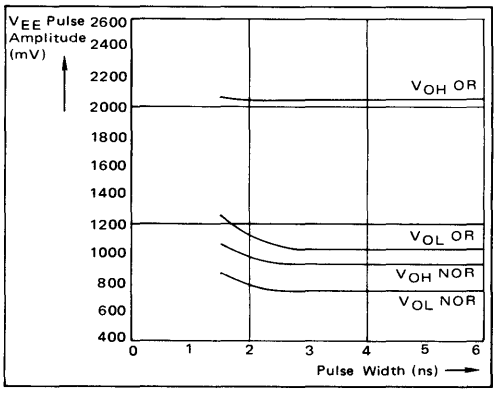


FIGURE 9 – V_{EE} ac NOISE IMMUNITY

The LOW level NOR output is most affected by V_{EE} noise. This is due to a combination of V_{OL} tracking and V_{BB} coupling. However, the noise immunity to this worst case condition remains greater than 700 mV. The greatest immunity occurs on the HIGH level OR output and is greater than 2 volts. In general, the MECL circuits are more immune to noise on V_{EE} than on any other point in the system.

The noise immunity of MECL circuits to noise on the V_{TT} termination voltage is dependent on the output impedance of the MECL gate and on the response time of the MECL circuit. The test circuit in Figure 4 shows that the pulse generator signal is connected to the outputs through 50-ohm termination resistors. Since the resistors have a better bandwidth than the pulse signal, there is no noise immunity change as a function of pulse width. Full amplitude output transitions are present down to the measuring limit of about 1.5 ns.

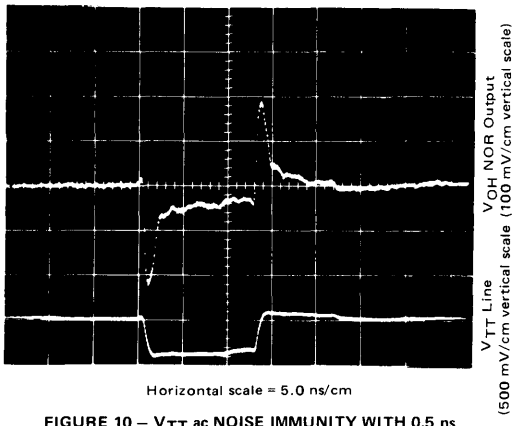


FIGURE 10 – V_{TT} ac NOISE IMMUNITY WITH 0.5 ns NOISE EDGE SPEED

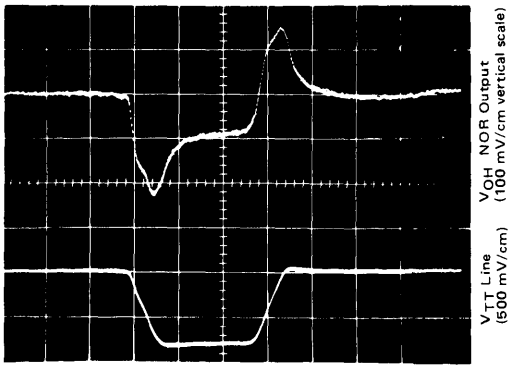
Figure 10 shows waveforms associated with V_{TT} noise immunity measurements. The upper trace shows the noise pulse coupling through the circuit output and the MECL gate recovering from the pulse and then restoring the logic level. The response time of the MECL 10K output circuit is about 2 ns.

The lower oscilloscope trace shows the pulse generator noise on the V_{TT} line. About 400 mV is required to cause a 204 mV transient on the output. The ratio of noise amplitude on the V_{TT} line to the noise on the output is dependent on the output impedance of the MECL circuit. As a result, the noise immunity to fast pulse edges is independent of the OR or NOR output tested and of the polarity of the noise pulse. For all outputs, about 400 mV of V_{TT} noise with 0.5 ns rise and fall times is required before the test limits are reached.

Since the V_{TT} noise immunity is dependent on the MECL circuit response time, the 0.5 ns pulse rise times are a worst case test condition. By increasing the pulse rise and fall times for the noise on V_{TT}, the MECL circuits become more immune to V_{TT} noise. With the outputs at a HIGH logic level and a negative pulse with 2 ns edges on V_{TT}, the MECL circuits have about 800 mV noise immunity, as shown in Figure 11. Because of the emitter-follower outputs of MECL circuits, the noise immunity for a LOW level output is limited by the output transistors turning off and the outputs following the V_{TT} voltage level. For example, with V_{TT} at ground in the test circuit, and a low level noise margin output test limit of 0.525 volts, the maximum tolerable positive pulse amplitude on V_{TT} is 525 mV.

CONCLUSION

The MECL circuits are most susceptible to noise on the V_{CC} supply line. For this reason, MECL design rules commonly suggest operating MECL circuits with a positive ground on V_{CC} and -5.2 volts on V_{EE}. By having a low impedance system ground, noise on the V_{CC} line between two circuits can be controlled and minimized.



Horizontal Scale = 5.0 ns/cm

FIGURE 11 – V_{TT} ac NOISE IMMUNITY WITH 2 ns NOISE EDGE SPEED

In some cases it is desirable to operate MECL circuits with ground and +5 volt supplies. MECL circuits operate very well in this mode when care has been taken to keep noise on the +5 volt supply line to a minimum. The MECL circuits are most immune to noise on the V_{EE} supply line. With standard capacitor bypassing techniques, noise on the V_{EE} line is controlled to safe system levels.

The amount of noise present in a digital system is dependent on many factors – such as power supplies and system environment. A primary source of noise is crosstalk, which is proportional to signal speed and signal amplitude. The 800 mV logic swing and relatively slow rise and fall times of MECL 10K along with its ability to operate in a transmission line environment, serve to reduce crosstalk in a MECL system.

One factor contributing to power supply noise is the amount of current "spiking" inherent in a logic family. MECL circuits have emitter-follower outputs and differential-amplifier switches. Consequently MECL generates very little noise. In fact, the high ratio of noise immunity to internally generated noise in MECL, is a feature leading to reliable system operation.

TESTING MECL 10K/10KH INTEGRATED LOGIC CIRCUITS

INTRODUCTION

The use of high speed logic circuits can be very beneficial to the system manufacturer. High speed logic offers a better performance/cost ratio than slower logic types, and thus an advantage in the competitive marketplace for digital equipment. Because of the high performance offered by logics such as MECL 10K/10KH, it may be necessary for the user to adjust his test procedures to get good test correlation between his measurements and Motorola's device specifications. Initially, correlation is important in the laboratory evaluation performed by a potential circuit user. If data sheet performance can not be verified, it is difficult to design with or use the parts.

After a decision to purchase components has been made, the important test is "incoming inspection." This testing is often performed under conditions differing from data sheet specified operation. It is possible to modify incoming inspection test limits to compensate for temperature stabilization or air flow and still insure that parts meet data sheet specifications. Motorola uses such a technique in high speed final testing of the MECL 10K/10KH and MECL III circuits.

Circuit performance must also be tested under *system* operating conditions during system checkout and rework. This testing need not be as thorough as component evaluation, but it must not interfere with overall system operation. The tester should be aware of the effects of system loading on circuit performance and possible inaccuracies deriving from normal system checkout test equipment operating at MECL 10K/10KH circuit speeds.

This application note describes methods for testing MECL 10K/10KH circuits to obtain results which correlate with the data sheet specifications. Test fixtures will be described and examples of expected results from typical MECL 10K/10KH circuits will be given. The parameters tested, and deviations of these parameters from guaranteed values when circuits are tested in other than the data-sheet-specified environment, will also be discussed.

Factors Involved in Testing

With circuit speeds of 2 ns for 10K and 1 ns for 10KH, some of the methods used for testing and evaluating such circuits must be modified from techniques used with lower speed circuits. To determine circuit performance accurately it is necessary to minimize distortion from outside sources. The technique used with MECL 10K/10KH and MECL III circuits is to keep the complete test system in a controlled 50-ohm transmission-line environment.

The 50-ohm transmission line system provides several benefits. By terminating all interconnection lines, signal reflections are eliminated. This results in waveforms undistorted by overshoot or ringing.

With transmission line interconnections, the propagation delays of signal paths are easily controlled and matched. As an example of how critical this can be, it should be noted that at MECL 10K circuit speeds, signal lines mismatched by 1.5 inches of length can cause a 10% error in test results.

An additional advantage of the 50-ohm system is its capability to drive 50-ohm test equipment inputs directly (oscilloscopes, frequency counters, etc.). Generally, 50-ohm inputs are more accurate and consistent than high input impedance probes. Probe calibration is very critical when evaluating circuits to within 100 ps accuracies.

Other factors influencing test results include temperature and air flow. MECL 10K/10KH circuits are specified at 25°C ambient air temperature, with 500 linear feet per minute air flow (to simulate normal system operating conditions). The logic outputs are defined after the circuit temperature has stabilized under the above conditions. Because of a possible different ambient environment temperature during testing, MECL input and output logic levels may differ from specified values by predictable, small amounts due to a differing circuit temperature. For example, testing in still air would result in a higher junction temperature, which would affect dc test results slightly. In many cases this small change in parameter values can be ignored, because the parts have a sufficient guardband to remain within specification limits. In other cases the logic test levels should be altered to compensate for circuit temperature. Methods for calculating junction temperature and modified test logic levels will be shown in the section on high speed testing later in this note.

A MECL 10K/10KH Test Fixture

Figure 1 shows the schematics for typical MECL 10K/10KH test fixtures. A pulse generator capable of generating pulses with MECL 10K/10KH edge speeds is connected directly to the logic circuit input. The generator line then continues to the 50-ohm 'scope where it is properly terminated by the 'scope in its characteristic 50-ohm impedance. The junction point at the gate input is kept as short as possible (normally under 1/2 inch) to

minimize any impedance discontinuities arising at this point. All interconnecting cables are 50-ohm coaxial cable. RG188AU or equivalent coax is commonly used because of its flexibility and thinness.

The output of the MECL circuit is connected to the other 50-ohm 'scope input with a similar 50-ohm cable. The cable from the circuit input to the 'scope, and the cable from the circuit output to the 'scope, are equal in length to eliminate propagation delay skew due to differing signal propagation delay times in the cables. Cable length from the pulse generator to gate input is not critical. Long cable lengths should be avoided because of bandwidth limitations which would arise from their excessive length. Up to 5-foot cable lengths can be used with MECL 10K circuits without problems.

An important feature of the test fixture is the use of 50-ohm terminated lines for all signal interconnections. Proper matched-impedance termination minimizes reading distortions which might be caused by signal reflections or crosstalk. The 50-ohm drive capability of the MECL 10K/10KH families and the fact that circuits are specified with 50-ohm loads are factors which aid in testing and evaluaiton of the parts. By eliminating high impedance probes, testing accuracy and repeatability of results becomes very good.

MECL 10K/10KH outputs are specified when driving 50-ohm loads to -2 Vdc (measured from ground). However, the scope input is itself a 50-ohm impedance to ground. For this reason, the normal -5.2 volt power supply for MECL (under normal conditions) is offset by 2,0 Vdc in the test fixture as shown in Figure 1a. V_{CC} is connected to +2.0 Vdc and V_{EE} to -3.2 Vdc. This permits terminating all signals in the system to ground.

The full military temperature range parts in the MECL 10K product line (MC10500 and MC10600) are specified for

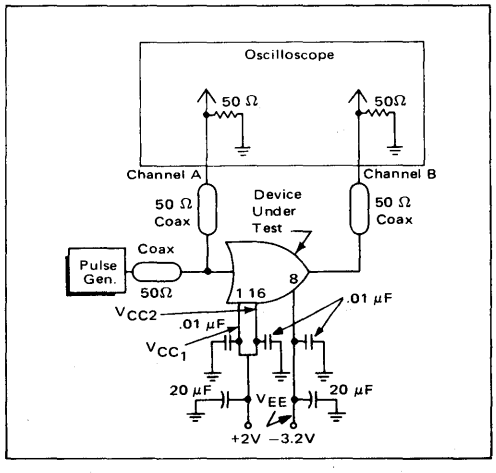


FIGURE 1A — MECL 10K/10KH Test Fixture Schematic

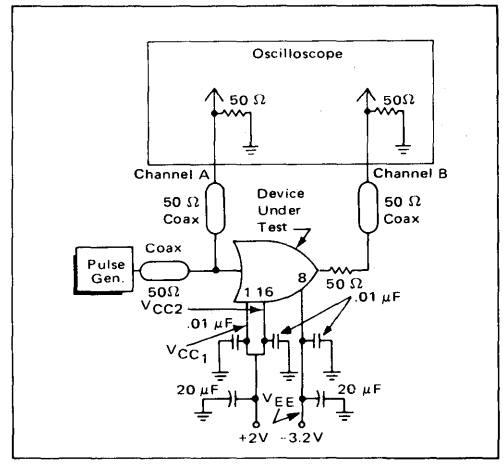


FIGURE 1B — Test Fixture Schematic for MC10,500 & 10,600 Series Parts

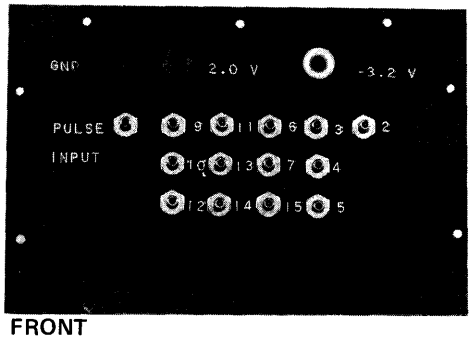
driving 100-ohm (minimum) loads. To test these parts, the test fixture is modified as shown in Figure 1b, by the addition of a 50-ohm series resistor on the gate output. This arrangement still allows use of the oscilloscope 50-ohm input, but does cause a 2-to-1 amplitude reduction which must be taken into consideration when interpreting 'scope readings.

Capacitor bypassing at IC sockets is used on both power supply lines to eliminate the possibility of voltage noise spikes. Such noise can be caused by the voltage source at the circuit responding to current fluctuations during circuit switching. The current fluctuations arise from unequal output current requirements between the logic levels, rather than from noise generated by switching in the basic MECL gate circuit. Supply voltage spikes could distort ac test information. They can be removed by heavy capacitor bypassing as shown in Figure 1. The 0.01 μF capacitors should be an RF (low inductance) type.

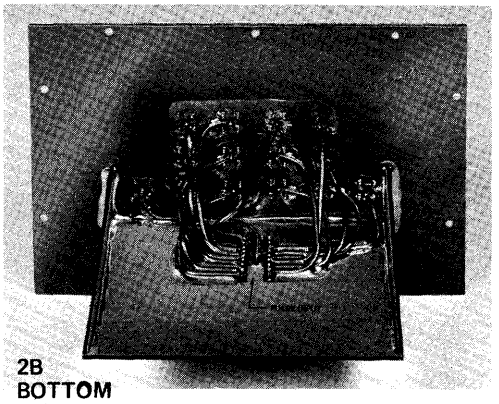
A MECL 10K test fixture for component evaluation is shown in Figure 2. The front view shows the miniature coaxial cable connectors for each circuit signal lead. The connectors are wired directly to the IC pins with semi-rigid 50-ohm coaxial cable*. These cables are matched in length for equal propagation delay. Outputs are easily observed by connecting a cable between the pin connector and the 'scope input. For best test results, unused circuit outputs should be terminated with 50-ohm loads at the connector.

The output from the pulse generator is connected to the pulse input connector of the test fixture. This signal is routed to a terminal near the circuit pins via semi-rigid coax cable (cf Figure 2B). A jumper runs to the desired IC input pin with a short wire. The jumper is soldered in as necessary to drive different input pins. A coaxial cable

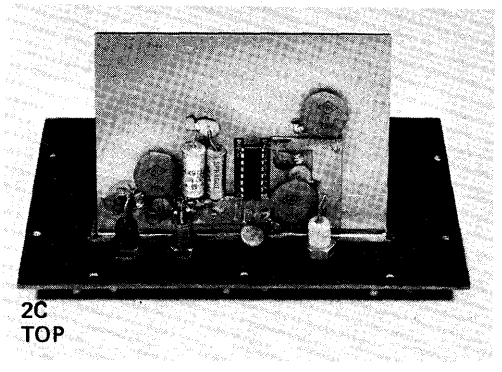
*e.g., Precision Tube Co., "Coaxitube" AA50085, or equivalent.



FRONT



2B
BOTTOM



2C
TOP

FIGURE 2 — Views of MECL 10K Test Fixture

from the IC input pin connector on the front panel of the test jig, to the 'scope input, provides for observing the input pulse and terminating the pulse generator.

The three power supply inputs are: ground; +2.0 Vdc; and -3.2 Vdc. The inputs are routed through standard banana plugs, for easy connection to power supplies. The ground input is connected to a reference voltage plane and to all coaxial cable or connector shields. The +2 Vdc input is bussed to pins 1 and 16 with a wide bus wire, or the metal of a circuit board. Both pins 1 and 16* are connected to the +2 Vdc bus close to the package. This line is well bypassed to ground. The V_{EE} line is similarly connected to pin 8 with a heavy bus and bypass capacitors.

The MECl 10K/10KH circuits should be plugged into a low-profile integrated circuit socket. An alternate approach is to remove the pins from a low-profile socket and connect these pins to the circuit board material from which the test set is built. (This approach has been found to be more appropriate when heavy use of the test fixture is expected.) The size of the test fixture is made compatible with the oven used for thermal testing.

This type of test fixture is easily constructed and is very good for low-volume laboratory evaluations. The fixture is acceptable for testing any 16-pin MECL 10K/10KH circuit, and the results will be very precise. The limitation of this type of test set comes in the handling of parts, and test equipment controls for large volume testing. For large volume testing an automated system is preferable.

Test Parameters

Circuit tests are usually performed to confirm data sheet specifications. These tests are of two general types: dc testing, and ac testing. DC testing measures logic levels or noise margins, circuit current, and input currents. AC testing measures propagation delays, edge speeds, and flip-flop toggle rates. It should be noted that MECL 10K/10KH dc parameters are specified with a grounded V_{CC}, -2 Vdc termination, and -5.2 Vdc on V_{EE} (as the parts are normally used in a system).

Nominal AC parameters are specified with the test fixture at +2.0 Vdc on V_{CC}, ground termination, and -3.2 Vdc on V_{EE} as discussed earlier. Other circuit parameters not included in the data sheets, but often measured, include: input capacitance, input impedance, and output impedance. The difficulty of performing these tests with

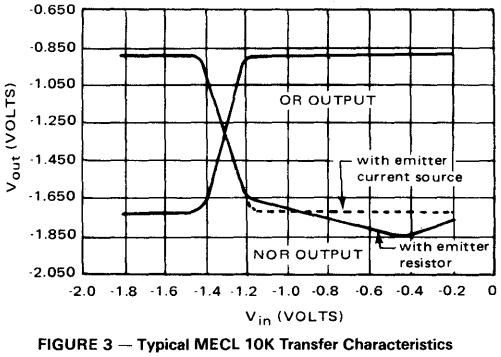


FIGURE 3 — Typical MECL 10K Transfer Characteristics

The solid curve shows the transfer behavior for the basic MECL 10K OR/NOR gate. The dotted section of the curve describes the transfer function for parts such as the MC10107, and most MSI circuits. These have a constant current source in the emitter node of the internal switch.

*On a few devices only one of these pins is used for V_{CC}. Consult specific part data sheets.

high-speed final test equipment makes specifying these parameters impractical for standard parts.

MECL circuit transfer characteristics are often plotted during device qualification. Plotting transfer characteristics is accomplished by putting a variable input voltage on the circuit input and measuring the output voltage. Figure 3 shows the typical transfer characteristics for MECL 10K logic functions. The test fixture previously described in this note may be used for transfer characteristic measurement by connecting a power supply to the input pin through the coaxial connector and loading all output pins with 50-ohm loads. The output of a selected load is then connected to a voltmeter. Loads other than 50-ohms may be used to evaluate circuit performance, but the data sheet values are specified with 50-ohm loads*. The 50-ohm load specification is a worst case test condition. With lighter loads, the MECL circuits will have a larger logic swing. Since the circuit will be operating in the linear transfer region during these measurements, a small capacitor (0.1 μF) on the output of the MECL circuit will eliminate any possible oscillation which could cause distorted readings.

DC transfer curves for circuits with internal feedback (such as the MECL master-slave flip-flops) cannot be measured. However, threshold points can be determined by measuring the input voltage at which switching occurs. This is commonly done by putting a ramp signal on the circuit input and observing the point at which the circuit switches with an oscilloscope.

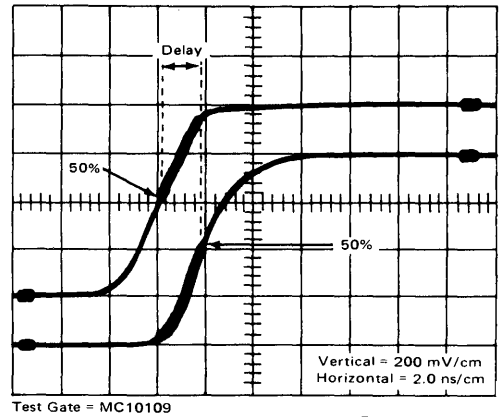
Noise margin is a measure of the protection against adverse operating conditions built into MECL. Noise margin is specified as the voltage difference between the specified input thresholds ($V_{IHA\ min}$ or $V_{ILA\ max}$ for 10K, $V_{IH\ min}$ and $V_{IL\ max}$ for 10KH) and the guaranteed output thresholds ($V_{OHA\ min}$ or $V_{OLA\ max}$ for 10K. $V_{OH\ min}$ and $V_{OL\ max}$ for 10KH). As shown on the device data sheet the noise margin is 125 mV for a HIGH output logic level and 155 mV min for a LOW output logic level for MECL 10K and 150 mV for both high and low for MECL 10KH.

The noise margin values are found by calculating the difference between V_{IHA} and V_{OHA}, and between V_{ILA} and V_{OLA}, respectively. Further information may be found in reference 1 or 2. By setting the threshold voltages by means of a power supply, and using the same test fixture employed to measure the transfer characteristics, the output levels can be measured and noise margins calculated.

Propagation delays are measured by connecting a test circuit as shown in Figure 1. For all MECL circuits propagation delay is measured from the 50% amplitude point on the input signal to the 50% point on the output signal. Input signal levels for ac testing MECL 10K are specified in the data sheets as +1.11 Vdc for a HIGH level, and +0.31 Vdc for a LOW level. The input signal rise and fall times are set at 2.0 ns with a 20% to 80% measurement for MECL 10K. This puts the 50% point at +0.71 volt, equal to the MECL 10,000 internal bias voltage V_{BB} when V_{CC} is at +2.0 volts.

*excepting military temperature range parts.

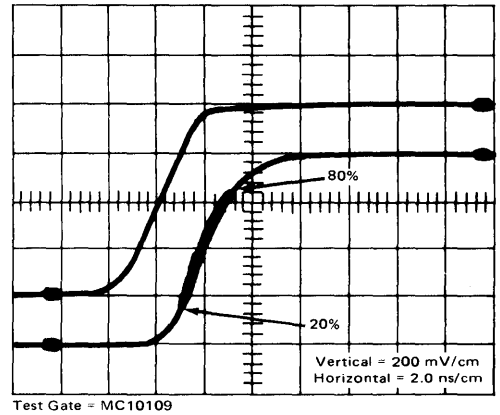
If a sampling oscilloscope with a digital readout is used, the test circuit waveforms for an OR gate function will look like Figure 4. The intensified zone on the waveform



Test Gate = MC10109

FIGURE 4 — MECL 10K Propagation Delay

shows the time interval of measurement — about 2 ns for the MECL 10K device under test. When a digital readout is not used, the delay time is determined from the scope traces by visual methods.



Test Gate = MC10109

FIGURE 5 — MECL 10K Rise Time

Rise-time and fall-time testing is identical to propagation delay measuring except that the output waveform is measured for slope. With MECL 10K/10KH the output is specified from the 20% to the 80% points. The other MECL families are specified between 10% and 90%. Because of the designed-in rounding of the upper 20% of a MECL 10K/10KH waveshape, the 10% to 90% waveform is difficult to measure accurately. However, the 20% to 80% time is representative of the slope during the active transfer region of the MECL circuit input.

A typical rise-time test waveform for a MECL 10K circuit is shown in Figure 5. The intensified trace is shown for a 20% to 80% test and is approximately 2 ns. The 10% to 90% rise time would be about 3.2 ns. The 20% to 80% rise time of MECL 10KH is approximately 1 ns with a 10% to 90% rise time of 1.8 ns.

Flip-flop toggle rates are measured by connecting a high speed pulse generator to the clock input. It may be necessary to decrease the pulst generator signal edge from the standard 2 ns (20% to 80%) when measuring toggle rates above 125 MHz in order to retain MECL amplitudes. When measuring toggle rates for the type D flip-flops, the Q output is connected to the D input. The J and K inputs of the J-K master-slave flip-flop are either left open or are connected to the LOW logic level (V_{OL}).

The upper frequency limit of MECL 10K/10KH flip-flops is commonly due to the output LOW level failing to remain at specified voltages, rather than to a failure to toggle. Figure 6 shows a MC10131 dual "D" flip-flop operating at 150 MHz. The device still has a MECL signal swing at its output. However at about 160 MHz, the LOW level output would rise out of specified limits for the part under test.

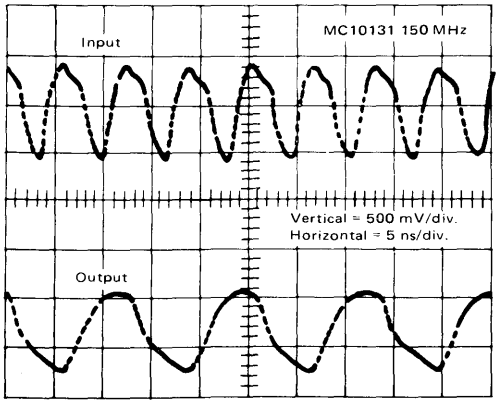


FIGURE 6 – MC10131 Toggle Rate Test

DC Considerations

Power supply current drain is specified at the V_{EE} negative supply pin of the IC package. By measuring I_E, the current out of this node, the device can be specified independently of output loading. Because of the wide variety of possible output loads for MECL 10K/10KH circuits in system operation, it is impossible to specify power for every possible loading situation. The power supply current drain defines power requirements for the logic current switches and bias drivers in the package. When calculating system power it is necessary to add power due to input current drain and output loading, to the specified power for the package based on $P_D = I_E \times V_{EE}$.

Input current requirements for a MECL 10K/10KH part depend on the use of the input. The basic specification of 265 μA (maximum) applies for a fan-in of one gate load. The input current for a HIGH logic level is divided between the internal input pulldown resistor and the current switch input of a MECL circuit. Since only one pulldown resistor is required for a multiple fan-in pin, input current is not directly proportional to the number of current switches being driven in the package. For example, a four-gate strobe input in the MC10101 is specified at a maximum of 550 μA, a value only slightly more than two single gate inputs.

Input current requirements for a LOW level logic signal is less than for the HIGH level. The signal must still drive the internal input pulldown resistor, but the MECL switch input current consists of only a small amount of reverse leakage current when the input transistor is off.

Other circuit parameters often tested but not specified on the data sheets include output impedance and input capacitance. The dc output impedance is measured by changing the loading of the MECL output and observing the change in output voltage. The change in output voltage divided by the change in output current gives an output impedance of about 7 ohms for a typical MECL 10K/10KH circuit.

Input capacitance is more difficult to measure and normally requires a time domain reflectometer, a stripline reflectometer setup, or a current probe transformer (e.g., Tektronix CT-1, or equivalent). Testing has shown the typical input capacitance for MECL 10K/10KH gate circuits to be about 2.9 pF. The details needed for testing input capacitance may be found in Chapter 7 of the MECL System Design Handbook, referenced at the end of this note.

High Speed Testing

High speed testing techniques are normally used when a large volume of parts must be checked. High speed testing usually involves a machine which automatically checks a part for all the tested parameters without manually setting controls for each test. To take advantage of the speed of such machines it is normally undesirable to provide air flow or to wait for the circuit under test to temperature stabilize*. Considering that the test will be performed with the chip temperature near 25°C, it may be necessary to compensate the test parameters so the circuit will be within the specifications at stabilized operating conditions. Each MECL 10K circuit is designed to have the same input and output logic levels at the specified ambient of 25°C and 500 linear feet per minute air flow, regardless of power levels within the package. Therefore, the amount of compensation for high speed testing will depend on the power dissipation of the circuit.

Junction temperature T_J (under normal system operation) may be calculated:

$$T_J = P_D \theta_{JA} + T_A,$$

where θ_{JA} is the thermal resistance of the package (junction to ambient) about 50° C/W with 500 linear feet per minute air flow, and T_A is the ambient temperature. From the above equation, the junction temperature for a 200 mW part will be 35°C for a 25°C ambient temperature. This results in a stabilized junction temperature 10°C above the high speed test temperature for the 200 mW part.

*In about 10-15 sec., the device will have reached 80% of equilibrium. A 5-minute delay prior to making measurements, is more than adequate to insure full stabilization.

For MECL 10K parts, the change in the HIGH logic level, V_{OH}, is about 1.4 mV/°C and the change in the LOW logic level, V_{OL}, is about 0.5 mW/°C. Using the above 200 mW part, the 10°C lower junction temperature would shift V_{OH} 14 mV more negative and V_{OL} 5 mV more negative.

The input signal requirements are controlled by the temperature tracking of the respective output levels. V_{IH} levels will be shifted by the V_{OH} factor of 1.4 mV/°C and the V_{IL} level will be shifted by the V_{OL} factor of 0.5 mV/°C. When calculating the power to determine thermal shifting, it is also necessary to include the power dissipated by the output devices, e.g. $[P_{output} = (\text{No. of outputs}) \times (I_D \times V_D)]$.

It can be seen that these small changes in output levels would not keep the majority of parts from meeting specified performance if the test parameters are not altered. There is sufficient noise margin built into the circuits, plus a safety factor between Motorola final test specifications and the limits specified on MECL 10K/ 10KH data sheets, to overcome most test environment differences. However, some of the more complex MSI functions can dissipate around 600 mW. If these parts are tested without allowing the circuits to temperature stabilize, the logic levels may be sufficiently different to offset incoming test yields. In such a case, test level compensation should be considered.

Test Equipment

The main factor when selecting test equipment to work with MECL circuits is the high frequency capability of the test units. Pulse generators must have 50-ohm output drive. In addition, edge speed and offset must be MECL compatible. The 50-ohm drive is characteristic of virtually all high speed pulse generators. It is necessary to drive coaxial cables or other 50-ohm lines at high speed without signal distortion due to improperly terminated lines.

When testing MECL 10K/ 10KH, a pulse generator should be set to 2.0 ns 20% to 80% edge speeds. The offset and amplitude should be adjustable to MECL logic levels. When driving a test fixture with a +2.0 Vdc supply on V_{CC}, the logic levels are +1.11 volts and +0.31 volt. It is also desirable to have the pulse generator capable of interfacing with MECL 10K/ 10KH operating with grounded V_{CC}. In this mode of operation the logic levels are typically -0.89 volt and -1.69 volts.

The selection of an oscilloscope depends on where the 'scope is to be used. The requirements are different for component evaluation and for system checkout. A good sampling scope is normally needed for device qualification because of the accuracy requirements entailed when measuring 100 picosecond increments. However, 500 MHz real time 'scope will give good results. All of these 'scope can be purchased with 50-ohm inputs which are compatible with MECL 10K/ 10KH test fixtures.

When performing system checkout, a real time 'scope of at least 150 MHz bandwidth is normally adequate. While edge speed will be degraded by this bandwidth, and while some overshoot and ringing may be attenuated, the speed is sufficient to determine that the circuits are operating properly. Using oscilloscopes with less than 100 MHz bandwidth is not recommended because such 'scope will seriously degrade the presentation of the MECL signals and may not see signals which affect operation of the MECL circuits.

It is also possible (and usually desirable) to use high impedance probes during system checkout. However, the ground reference should be connected to the probe tip and kept near to the point under test. Having a separate ground wire from the 'scope to the system (in place of a probe ground) will cause distorted readings because of the length of the ground run in relation to signal speed.

Other types of laboratory equipment, such as power supplies and voltmeters, have no special performance requirements imposed on them when used for MECL testing. The ac response time of the power supply is not especially critical because of the large amount of capacitor bypassing used on a MECL test fixture. DC voltmeters are normally used to measure output logic levels during dc testing, because of their higher accuracy than an oscilloscope.

Conclusion

Testing MECL 10K/ 10KH circuits requires special techniques to insure accurate results. However, if these techniques are practiced, testing high speed integrated circuits is no more difficult than testing lower speed parts. The use of a transmission line system greatly improves the accuracy and consistency of high speed digital testing. By using test techniques consistent with Motorola's component evaluation and final test, the circuit user can obtain test results which correlate well with Motorola's data sheet and other test information.

INTERFACING WITH MECL 10K/10KH INTEGRATED CIRCUITS

INTRODUCTION

The MECL 10K/10KH series are high speed logic families designed for applications where system performance is important. Emitter coupled logic is used to obtain the required circuit speed and provide the circuit features necessary to optimize high speed system design. All MECL 10K/10KH circuits interface directly with each other. In addition, MECL 10K/10KH circuits are completely compatible with the very fast MECL III circuits, permitting a designer to mix all families in the same system for best performance.

MECL 10K/10KH circuits normally operate with ground on V_{CC} and a negative 5.2 Vdc power supply on V_{EE}. While MECL may be used with ground on V_{EE} and +5 Vdc on V_{CC}, the negative supply operation has noise immunity advantages and is recommended for larger systems. Also, emitter coupled logic operates with a relatively small 800 mV logic swing. With the -5.2 volt power supply the normal MECL 10K/10KH high logic level is about -0.9 volt and the low logic level about -1.7 volts. For these reasons MECL 10K/10KH and MECL III are not directly compatible with the common slower speed logic types such as TTL, DTL, and MOS. Translators must be used when interfacing these logic types with MECL.

In many designs it is necessary to interface with signals which are not digital logical levels. These may be low amplitude input signals which must be amplified before they can be used and low frequency signals which require shaping. The linear characteristics of the MECL line receivers allow these circuits to be used as amplifiers or Schmitt triggers.

Another important interface requirement is driving optic displays. The MECL 10K/10KH outputs are directly compatible with light emitting diode requirements. MECL circuits are also available for driving other types of displays.

INTERFACING WITH TTL

The most common interface requirement for MECL is with TTL logic levels. This occurs when a MECL system must interface with an existing TTL system or when both MECL and TTL are used in the same system design. The interface requirements between MECL and TTL depend on how the circuits are being used.

The normal MECL/TTL interface occurs when MECL is powered with a -5.2 volt power supply and TTL with +5 volts. The use of a common ground and separate power supplies helps isolate TTL generated noise from the MECL supply lines. The MECL/TTL translator circuits, MC10124, MC10125, MC10H124 and MC10H125 shown in Figure 1 provide this interface.

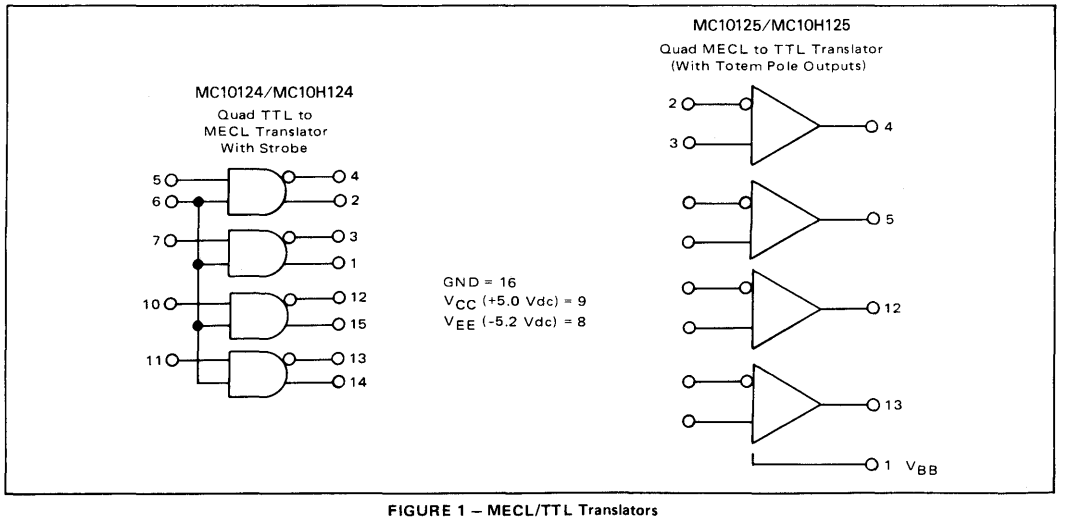


FIGURE 1 – MECL/TTL Translators

The MC10124 is a quad TTL to MECL translator, with a common TTL strobe input and complementary MECL outputs. The propagation delay through the circuit is typically 5 ns and the top operating frequency is normally greater than 85 MHz. If maximum operating frequency tests are made with the 5.5 ns input rise and fall times specified on the component data sheets, operating speed is limited to 70 MHz because of input restrictions. With faster rise and fall times on the inputs, circuit speed increases until the output fails to reach specified limits at about 85 MHz.

The MC10H124 is the MECL 10KH version of the MC10124. The propagation delay is typically 1.5 ns as opposed to the 5 ns typical for the MC10124.

Motorola also offers a variation of the MC10H124, the MC10H424. It is also a TTL-to-ECL translator and has the same pinouts as the MC10H124 but it has an ECL strobe instead of TTL.

The MC10125 is a quad MECL to TTL translator with differential amplifier inputs and Schottky clamped transistor "totem pole" TTL outputs. Propagation delay time for the circuit is a function of fan-out loading as shown by the curves in Figure 2. As with the MC10124, maximum operating frequency is limited by the output failing to reach specified output levels above 85 MHz.

The MC01H125 is the MECL 10KH version of the MC10125. The propagation delay is typically 2.5 ns with a fanout of 5 as opposed to 5.5 ns for the MECL 10K part.

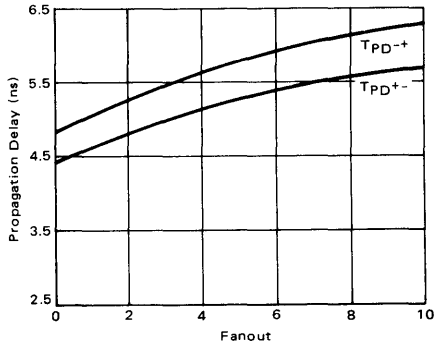


FIGURE 2 – Propagation versus Fanout for the MC10125

A feature of the MC10124/MC10125 pair is the ability to operate over long distances with a twisted pair line. Figure 3 shows the flexibility of using these parts with twisted pair lines as any combination of MECL and TTL inputs and outputs can be interfaced with MECL signal levels on the interconnecting lines.

The complementary outputs of a MECL gate or the MC10124 translator and the differential inputs of a MECL line receiver or the MC10125 translator are used with a twisted pair line to send signals over long distances. Since the line receiver looks at the voltage difference between the two input signals and not the absolute value, the circuit has good noise rejection capability. A noise pulse coupling into the twisted pair line appears equally on both of the line receiver inputs and is rejected as common mode noise. The differential operation is also advantageous when two sections of a system are not connected with a solid ground or power line. The power supply offset appears as common mode signal to the receiver and is rejected within the limits of the receiver. The MECL to TTL translator typically rejects common mode signals greater than plus or minus 2.5 volts before the output fails to remain within specified limits.

When high speed signals are transmitted on long lines, termination techniques should be used to minimize reflections and waveform distortion. These reflections cause ringing on the signal line which if severe enough will effect system noise immunity. The designer should consider using termination resistors when the two way propagation time of the line is greater than the rise time of the signal on the line for best system performance. Figure 3 shows the use of a parallel termination resistor, R_T, at the receiving end of the line. The value of R_T should match the line impedance which is about 110 ohms for common twisted pair lines.

A common application for the MECL translators is high speed line drivers and receivers in an all TTL system. The TTL system sees only the translator TTL inputs and outputs, but takes advantage of MECL line driving capabilities to send signals from one point to another in the system. The gain of the MC10125 is typically greater than 15 volts per volt making the circuit a useful input device for interfacing to TTL logic levels.

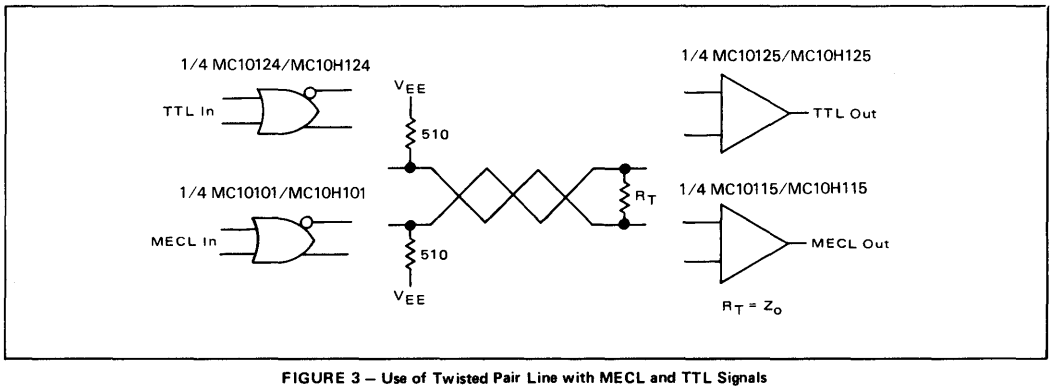


FIGURE 3 – Use of Twisted Pair Line with MECL and TTL Signals

Some designs are restricted to using only one power supply thus the MC10124 and MC10125 cannot be used. Therefore Motorola developed the MC10H350 single supply ECL to TTL translator. The device was designed to operate from a single power supply of either +5.0 V or -5.2V. The MC10H350 incorporates ECL differential inputs and Schottky 3-state outputs. The 3-state outputs produce a high impedance output when the output enable ($\overline{OE}$) is brought high.

INTERFACING WITH TTL BUSSES

In many system designs it is necessary to tie several pieces of equipment together with input/output bus lines. These lines are time shared with the various sections of the total system, requiring that only one line driver be active at a time. Three state TTL is commonly used in

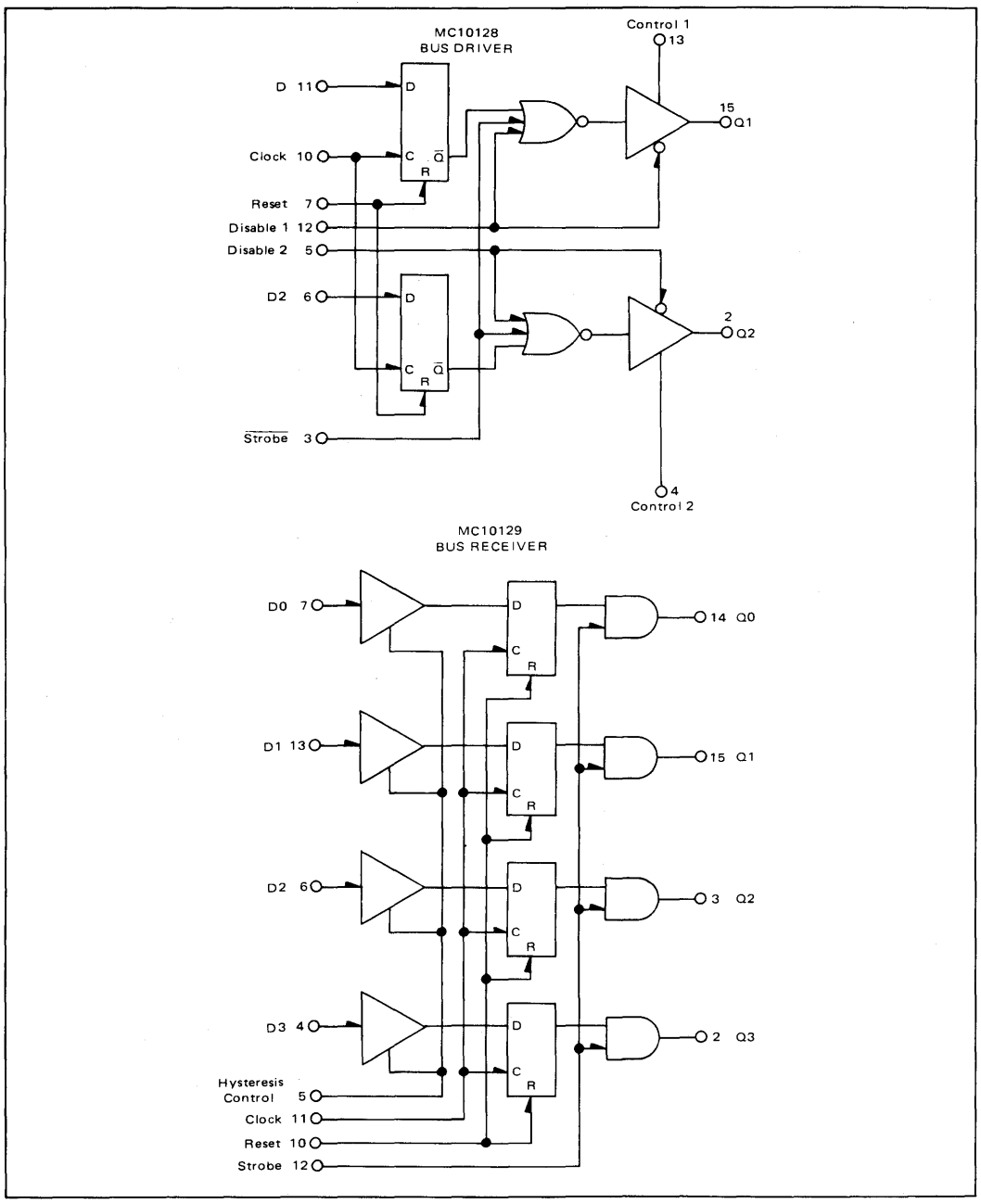


FIGURE 4 – MECL to IBM or TTL Interface Circuits

these applications because of the ability to disconnect the driver from the line. When disabled, the driver does not appear as a heavy load to the active driver or as a low impedance discontinuity to the bus line. The MC10128 Bus Driver and MC10129 Bus Receiver shown in Figure 4 are designed to interface a high speed MECL system into a TTL compatible bus line.

The MC10128 is a dual bus driver with MECL inputs. Internal latches are provided to free the data inputs while waiting for the information to be used. When the clock input is held at a low logic level or left unconnected data passes through the latch. Disabled inputs are provided for each bus driver to control the three state output. A high MECL logic level on a disable line causes the driver output to go to a high impedance state overriding the strobe, but the clock and data inputs can still be used with the latch.

Leakage current into a disabled output is important when interfacing with TTL three state drivers since the TTL circuits are commonly rated at 2 mA and 2.4 volts for a high level output. The curve in Figure 5 shows typical leakage current of the MC10128 bus driver with the output disabled. This current should be considered when figuring loading on a TTL driver. The MECL part is rated for 50 mA at 2.5 volts, therefore loading is not a problem for the MC10128 driving disabled outputs.

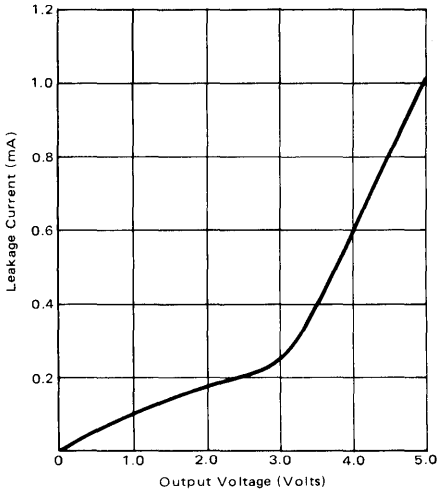


FIGURE 5 – Output Current into a Disabled MC10128 Bus Driver

The MC10128 bus drivers have control inputs which control the mode of circuit operation. When a control input is left open the bus driver operates in a TTL compatible bus system. With a grounded control input the bus driver outputs are compatible with IBM System 360 I/O bus requirements. IBM compatibility will be discussed in a following section.

The MC10129 quad bus receiver accepts TTL or IBM bus logic levels and translates to MECL outputs. Internal latches are provided to free the bus lines while waiting for the data to be used. The circuit features a hysteresis control input which changes the threshold points for circuit switching as shown in Figure 6. In normal operation the hysteresis input is connected to V_{EE} giving guaranteed input threshold points of 2.0 volts for a high logic level, and 0.8 volt for a low level with TTL inputs (1.7 volts and 0.7 volt with IBM bus inputs). Figure 6a shows the transfer characteristics when the hysteresis feature is not used.

In a high noise environment hysteresis is added to the circuit by connecting the hysteresis control input to ground. In the hysteresis mode high level threshold points are specified at 2.6 and 1.9 volts. The circuit is guaranteed to recognize a high level input below 2.6 volts, but the input may drop to 1.9 volts and remain a guaranteed high level. The low level threshold points are 1.0 volts and 1.7 volts. Typical transfer characteristics and specified MC10129 threshold points in the hysteresis mode are shown in Figure 6b. The hysteresis is the input difference between the rising and falling output edges and is nearly 700 mV in the figure.

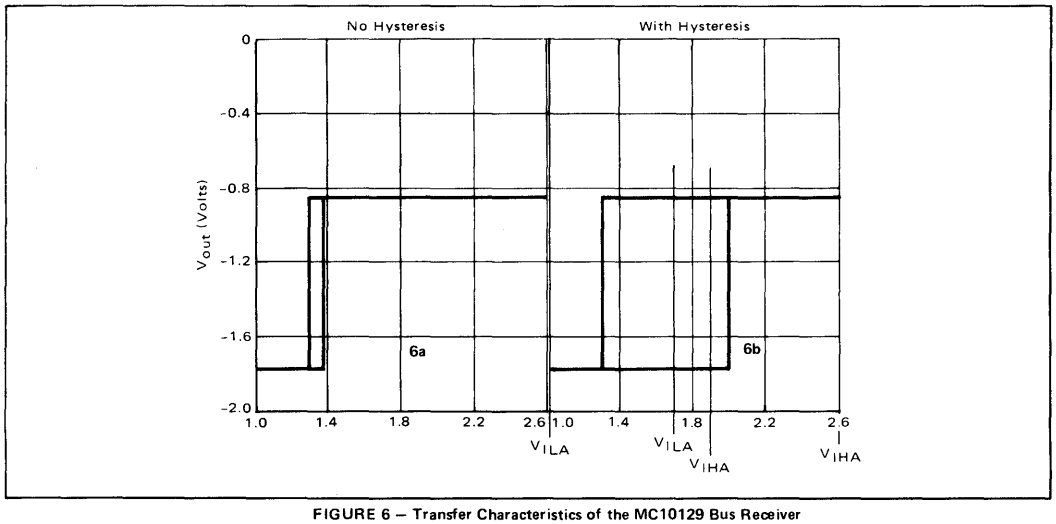


FIGURE 6 – Transfer Characteristics of the MC10129 Bus Receiver

Figure 7 illustrates a bus line using both TTL and MECL bus driver and receiver citcuits. Any standard pull up or termination resistor network presently used on the TTL bus will be compatible with the MC10128. Thus with the MC10128 and MC10129 it is possible to directly interface a high performance MECL system into many existing minicomputer I/O bus lines.

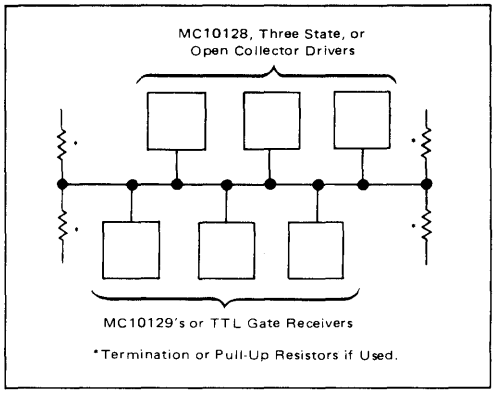


FIGURE 7 – MECL/TTL Bus Line

The MECL bus driver and receiver circuits can also be used to build bus lines in an all MECL system as shown in Figure 8. The MC10128 bus driver is specified driving 50 ohms to ground or 25 ohms to +1.5 Vdc. A 100 ohm bus would be terminated by a 100 ohm resistor to ground at each end, or a 50 Ω bus by 50 ohm resistors to +1.5 Vdc at each end. An alternate to the +1.5 V supply is a resistor equivalent of 68 Ω to ground and 160 Ω to +5 Vdc. The terminated bus allows high speed data transfer because it is not necessary to allow time for reflections on the line to settle out. Normally a TTL output is not able to drive a bus terminated as shown in Figure 8.

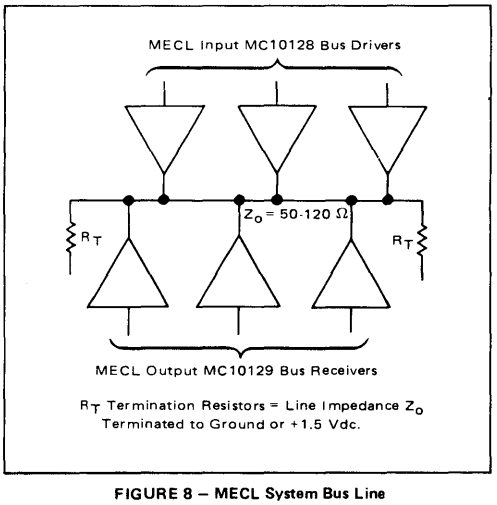


FIGURE 8 – MECL System Bus Line

INTERFACING WITH TTL ON A COMMON POWER SUPPLY

In many system designs where a small number of MECL circuits are used, it is desirable to operate both MECL and TTL on a +5 Vdc power supply. MECL works very well in this mode if care is taken to isolate the TTL generated noise from the MECL +5 volt supply line. Translators for interfacing TTL and MECL in this mode are built with discrete components since integrated circuit translators do not operate on a single +5 volt supply.

The TTL to MECL translator shown in Figure 9a consists of three resistors in series to attenuate TTL outputs to MECL input requirements. The translation is very fast, normally under 1 ns, depending on wiring delays and stray capacitance.

Two techniques for interfacing MECL to TTL are illustrated in Figures 9b and 9c. The circuit in Figure 9b takes advantage of MECL complementary outputs to drive a differential amplifier made from two PNP transistors. Speed of this translator is in excess of 100 MHz when driving one TTL load. The circuit in Figure 9c uses only one PNP transistor to perform the translation, but is slower than the differential approach. Typical translation delay time is less than 10 ns when driving one high speed TTL load. Both of the MECL to TTL translator designs use a pulldown resistor to ground to sink the low level TTL input current. For this reason fanout is normally limited to one TTL device unless resistor values are changed.

INTERFACING WITH IBM BUS LEVELS

High speed MECL systems, such as add-on memories or disk storage controllers, are often required to interface with IBM compatible input/output bus logic levels. The MC10128 Bus Driver and MC10129 Bus Receiver, Figure 4, are designed to meet IBM System 360 and System 370 I/O interface requirements. These circuits, described in an earlier section, interface directly with MECL 10K/10KH and MECL III logic levels.

In the IBM mode of operation the MC10128 driver meets the following guaranteed specifications: The low level output will not exceed +0.15 volt or go below -0.5 volt while sourcing 240 μA current. The high level output will not be below 3.11 volts with an output load of 53.9 mA or exceed 5.85 volts with an output load of 30 μA. The circuits are tested against damage from an output shorted to ground and are specified for a maximum short circuit output current of 320 mA.

Testing has shown that the MC10128 bus driver also meets the following IBM interface requirements. A 7 volt output is the maximum permitted with a supply over-voltage on the driver. This specification is met because +8 Vdc (maximum recommended MECL overvoltage) typically results in an output level less than +5.5 volts at the specified load of 123 mA. Testing has also shown that the loss of either or both power supplies on the bus driver will not cause a fault condition on the bus. Maximum load current occurs with a positive supply shorted to ground

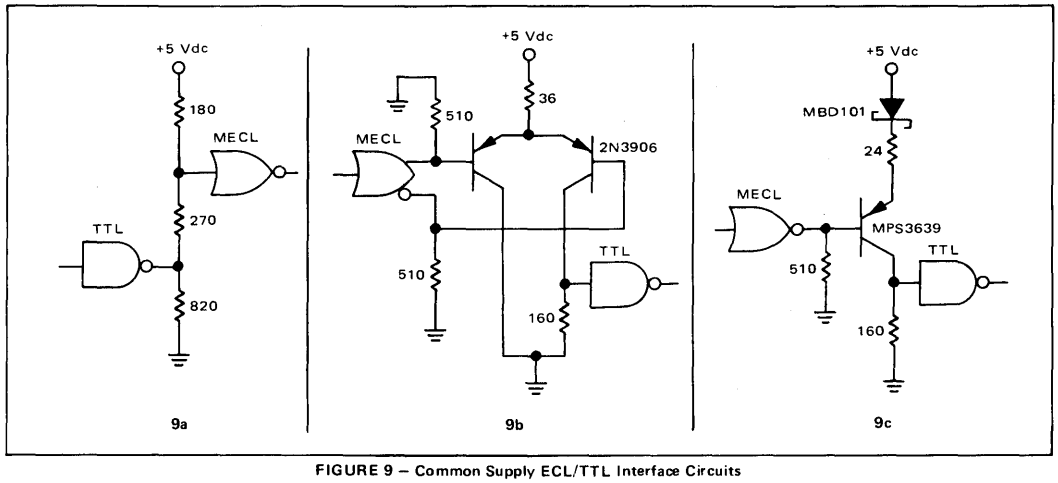


FIGURE 9 – Common Supply ECL/TTL Interface Circuits

and this is typically less than 4 mA with +6 volts on the bus line or less than 1 mA with 5 volts or less on the bus.

The MC10129 bus receiver is designed to translate IBM compatible bus lines to MECL logic levels. The high and low input logic level threshold points are specified at +1.7 volts and +0.7 volt to give IBM specified noise margins. The input current requirements for the MC10129 are well below IBM maximum specifications. At a high input level of 3.11 volts the MC10129 input current is less than 95 μA and the low level input current at 0.15 volt is not below -1.0 μA. This compares with 420 μA and -240 μA for the IBM specifications.

Testing has shown compatibility with most other IBM specification requirements. The circuit will withstand 7 volts on the bus input with power applied, although input current may be as high as 30 mA with a 7 volt input. The MC10129 has no problem meeting the -0.15 volt on the input either power up or power down. IBM's requirement of 6 volts on the receiver input with no power on the MC10129 is not met if the V_{CC} line on the receiver is shorted to ground. With the positive supply open, the 6 volt requirement is met, but input current can exceed 25 mA. This specification may be met by using a series resistor of 510 to 1000 ohms between the bus line and the receiver input. This limits current into the line receiver during a power down condition. Another IBM specification not directly met is the input impedance requirement of greater than 4 k ohms and less than 20 k ohms. Typical input impedance of the MC10129 is approximately 50 k ohms with a high level of 3.11 volts on the bus. If this interface requirement is necessary, a 20 k ohm resistor between the MC10129 input and ground provides an input impedance within specified limits.

The MC10128 and MC10129 bus drivers and receivers give the MECL system designer the capability to interface with the input/output requirements of many system types. In addition these parts can be used for bus lines interconnecting sections of large MECL systems.

INTERFACING WITH ECL OPERATING AT NON-MECL POWER SUPPLY VOLTAGES

MECL circuits are sometimes required to interface with ECL systems operating at power supply voltages that differ from the standard MECL ground and -5.2 volts. These circuits commonly use ground for a bias reference voltage, resulting in a logic swing centered around ground. This signal can be converted to and from MECL 10K/10KH logic levels with MECL line receivers and proper use of available power supplies.

MECL signals can be shifted more positive as shown in Figure 10a. The first line receiver stage generates complimentary signals and is unnecessary when MECL complimentary signals are available at the input. The second line receiver is powered by the MECL -5.2 volts on V_{EE} and the +1.3 volts on V_{CC} from other ECL circuits. The complimentary outputs from the first stage present a differential signal to the second stage within the common mode range of the circuit. The line receiver doing the translating operates at a total supply voltage of 6.5 volts, which is no problem for a low power line receiver circuit such as the MC10116/MC10H116.

The circuit in Figure 10b may be used to translate down to MECL input requirements. A line receiver connected to +1.3 volts and -5.2 volts is used to generate complementary outputs and amplify the signal prior to using a voltage divider to the second stage. Due to the differential operation of the MC10116 line receiver, the +1.3 volt supply is not critical and any value between +1.0 and +1.5 volts is acceptable. With the power on the circuit elevated to 6.5 volts, typical output swing is greater than 900 mV. The resistor divider network shifts the signals to MECL levels as required by the second line receiver stage. This stage, operating at normal MECL power supply levels, delivers normal MECL output signals. The use of differential signals is recommended in the voltage dropping network as this eliminates the need for critical

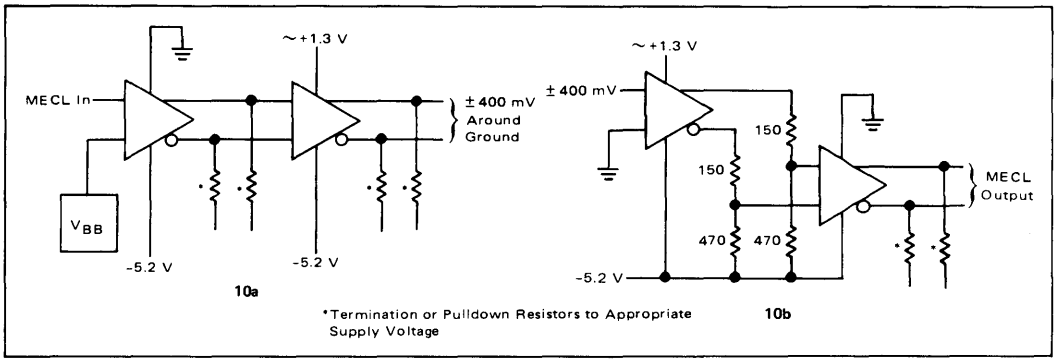


FIGURE 10 – Interfacing with Non-MECL Compatible ECL Using MC10116's

resistor values, and eases thermal or power supply tolerance design restrictions. The two stage interface circuit total delay is typically 5 ns including wiring and the resistor dividers. (The MC10116 has a typical propagation delay of 2 ns per stage.)

Another circuit that can be used to translate a signal swing around ground to MECL logic levels is the MC1650. This MECL III part is a high speed dual A/D comparator which is ideal for this interface, but designers should consider the cost and capability of the MC1650 against system requirements to determine the best interface circuit.

MECL/MOS INTERFACE CIRCUITS

The MECL/MOS interface varies with the type of MOS and the MOS power supply voltages. For P-channel MOS circuits operating between ground and a negative voltage, the circuits shown in Figure 11 may be used. The diode in the MECL to PMOS translator biases the PNP transistor off and on with MECL logic levels, as the transistor amplifies the MECL logic swing to the large P-channel MOS requirements.

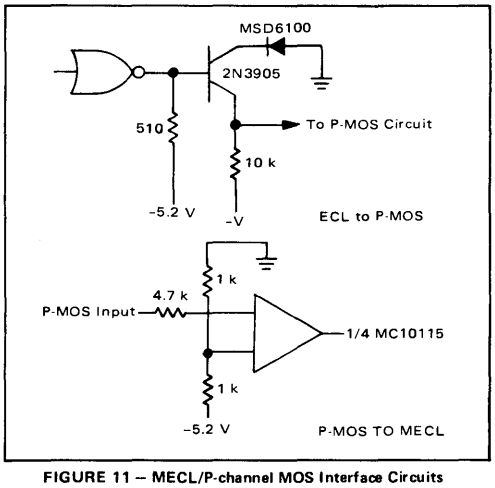


FIGURE 11 – MECL/P-channel MOS Interface Circuits

The MOS to MECL interface circuit in Figure 11 uses a line receiver to perform the translation. The line receiver offers advantages over a basic MECL gate since the reference voltage can be made more negative with the resistor divider, and the receiver input is a lighter load for a P-MOS output due to the absence of internal pulldown resistors. The 4.7 k resistor is used to limit input current when the MECL input clamps at about -6 volts in the negative direction.

Modern N-channel circuits are commonly TTL compatible, and CMOS at +5 volts operates with TTL logic levels. The MECL/TTL translators (MC10124 and MC10125) or the MECL bus circuits (MC10128 and MC10129) described earlier perform these interface requirements. The MC10129 bus receiver is especially useful as a MOS to MECL translator because the low input current requirements of the MC10129 (typically 60 μA at 3 volts) does not load the MOS circuits as would a normal TTL circuit input.

This availability of interface circuits allows the designer to take advantage of both MECL performance, and the low power and high circuit density of MOS for the slower sections of a system.

LOW LEVEL SIGNALS TO MECL

The differential amplifier operation of MECL line receivers permits these circuits to amplify low level signals to MECL logic levels. The circuit in Figure 12 is a typical amplifier design which uses the MC10116 line receiver to receive signals as low as 50 mV and give good MECL outputs. This design features two 100 ohm resistors in parallel for a 50 ohm input impedance to AC signals. The resistor values can be adjusted to terminate other wire impedances. Capacitor coupling is recommended for operation with signals that do not swing around a center point equal to the V_{BB} reference voltage.

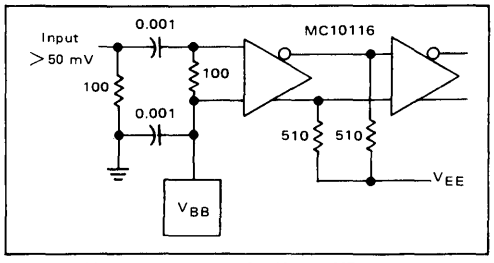


FIGURE 12 – Low Level Amplifier Using a MECL Line Receiver

The maximum bandwidth of the amplifier depends on the MECL line receiver part type as shown in the circuit gain versus operating frequency curves in Figure 13. The lowest frequency part that meets system requirements should be selected to lower component cost and ease of design rules. For example, the MC1692 should be limited to two cascaded stages and short interconnection lines to insure circuit stability. Also, the MC1692 is more stable in the stud "S" package than the dual in-line "L" package when used as an amplifier. Cascading three or more stages is possible with the slower MC10116 or MC10115 line receiver circuits.

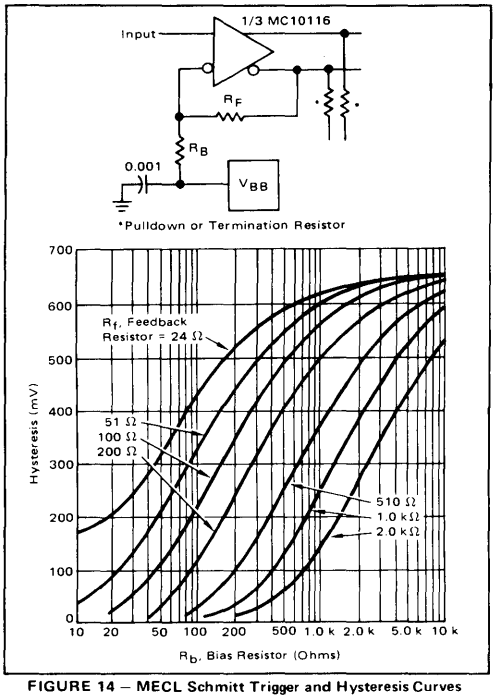


FIGURE 14 – MECL Schmitt Trigger and Hysteresis Curves

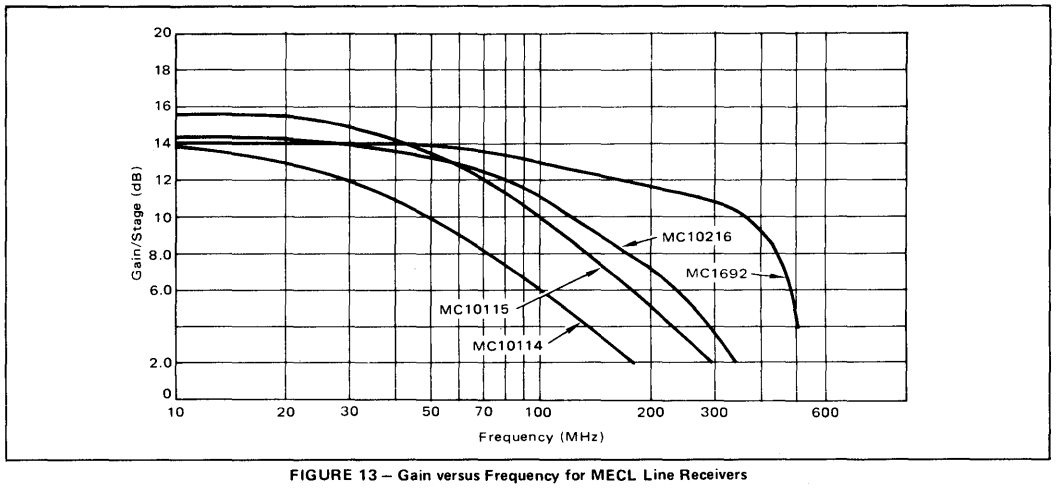


FIGURE 13 – Gain versus Frequency for MECL Line Receivers

MECL line receiver circuits can also be connected as Schmitt triggers to shape low frequency signals to MECL rise and fall times. An MC10116 connected as a Schmitt trigger is illustrated in Figure 14. The table in the figure shows the amount of hysteresis as a function of the feedback resistors. For low frequency signals below 1 kHz at least 150 mV of hysteresis should be used to insure the circuit does not momentarily oscillate during the output transition.

When connecting a line receiver as a Schmitt trigger it is important that the feedback resistors be connected to an inverting output from the input signal. If this is not followed, the performance of the input signal will be degraded because of negative, instead of positive, feedback. When the Schmitt trigger must also handle higher frequencies it is necessary to restrict the values of the feedback resistors. Above 50 MHz the resistors should be limited to 200 ohms or less, so stray capacitance does not

slow the feedback path causing serious phase shift between the two inputs of the line receiver. Use of a Schmitt trigger is discouraged at high frequencies because feedback phase shift makes bandwidth less than that of a straight line receiver amplifier. However, the combination of a MECL amplifier, Figure 12, followed by a MECL Schmitt trigger, Figure 14, gives a versatile buffer circuit for many input requirements within the frequency limits of the Schmitt trigger.

The MC1650 A/D comparator, Figure 15, also provides a good interface between low level signals and MECL. This circuit features 3 μA input current, 20 mV built in hysteresis, 5 mV offset voltage, and an internal latch. The MC1650 interfaces with a wide range of signal types since this part has a plus or minus 2.5 volt common mode range.

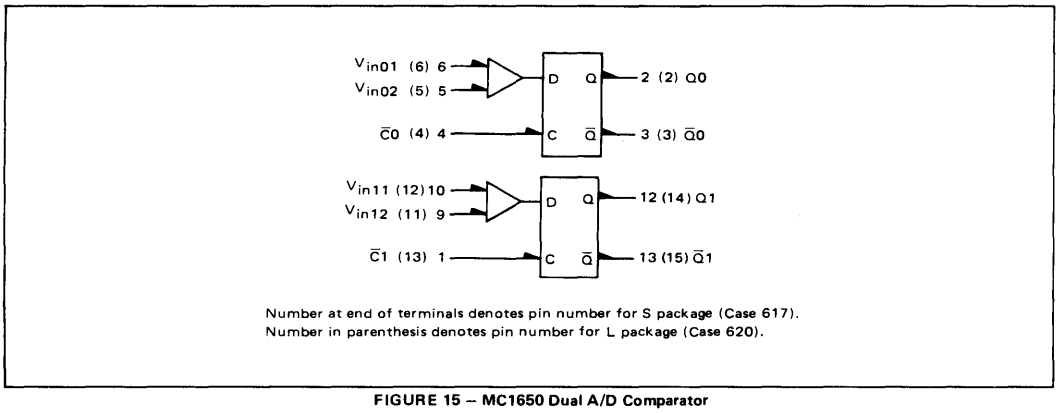


FIGURE 15 – MC1650 Dual A/D Comparator

INTERFACING WITH LIGHT EMITTING DIODES

Light emitting diodes are used with MECL 10K/10KH and MECL III for both data display and troubleshooting. When monitoring a MECL output for troubleshooting, the diode is connected between the output and V_{CC} as shown in Figure 16. With a typical MECL low output level of -1.7 volts, and a LED forward conduction of 1.6 volts, the diode lights. The high MECL level (typically -0.9 volts) is insufficient forward voltage for the diode to conduct.

The use of standard MECL circuits to drive LEDs is normally limited to system testing or low volume designs because the circuit is not guaranteed worst case. (Worst case MECL low level is -1.65 volts, and worst case diode forward voltage is 1.8 volts at 20 mA for a MLED 600.)

When LEDs are driven from MECL for data display, the MC10123 bus driver should be used. This circuit has a guaranteed low logic level output of -2.03 to -2.10 volts and a worst case high level of -0.960 volt. These levels are compatible with standard LED worst case requirements.

Generally, it is not advisable to drive another MECL circuit from an output driving a LED. The diode capacitance, typically 150 pF, slows the MECL rise and fall times which can cause timing problems, and the diode forward voltage may be small enough to clamp a MECL low level output above ECL input requirements.

MECL 10K/10KH and MECL III circuits are specified driving 50 ohm loads to -2.0 Vdc, which represents a typical output current of 22 mA for a high output. Designing with this limit, resistors as low as 200 ohms to -5.2 volts can be used in series with the LED. When the MECL circuit is in the low logic state, a 1.6 volt drop across the LED gives a diode current of 18 mA. Larger resistor values are used when less diode current is desired.

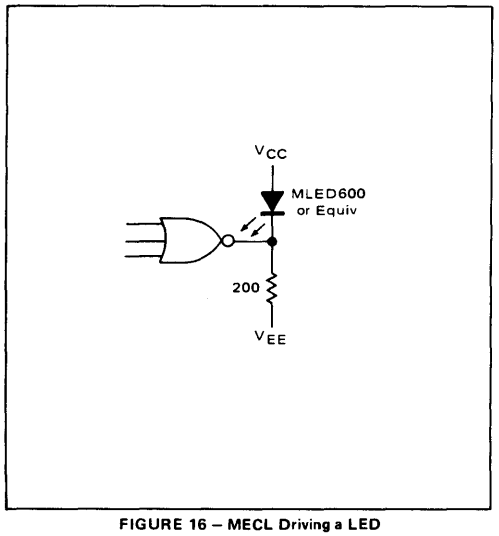


FIGURE 16 – MECL Driving a LED

BUSSING WITH MECL 10K/10KH INTEGRATED CIRCUITS

INTRODUCTION

A bus line is designed to interconnect several points in a system with a common data path. Normally drivers and receivers are located at each end of the line, so data can flow in either direction. Additional drivers and receivers often connect to the bus at various points along the line, requiring that the driver be capable of sending a signal in both directions. For this reason, a high speed bus driver must operate into a load equal to one-half the line characteristic impedance. Only one driver on a bus can send data at any given time. If more than one MECL driver were simultaneously transmitting, any output at a high logic state would predominate causing a loss of data.

System busses utilize either a single ended or differential operating mode. A differential bus requires two wires per signal path and the receiver looks at the voltage difference between the two lines. The differential line has noise immunity advantages for longer bus runs, but this approach is speed limited when compared to a single-ended bus. A differential system requires special drivers and receivers which are usually slower than high speed logic circuits. Also, present approaches to differential bus driving switch only one line of the differential pair when initializing a data transfer. This results in a crosstalk condition between the two lines which may limit maximum speed.

The single-ended bus uses one wire for each data path, minimizing wire and interconnection requirements. The signal voltages on a single-ended bus are referenced to some common voltage, usually ground, so standard high speed MECL circuits function as both drivers and receivers. With the use of high speed circuits as drivers, performance is largely determined by the transmission line characteristics of the bus. This application note discusses the transmission line parameters which should be considered in the design of a high speed MECL single-ended bus. Some of these parameters include termination, capacitive loading, stub lengths, and timing considerations.

HIGH SPEED SINGLE-ENDED BUSSES

High speed single-ended busses commonly have a high fanout density and use MECL circuits as drivers and receivers. Fanout on a MECL bus is not limited by dc loading considerations, however, circuit input and output capacitance will slow ac performance. Input capacitance of a MECL gate is about 3 pF and output capacitance about 2 pF. With packages soldered in and stray capacitance considered, distributed capacitance averages about 5 pF per circuit connection.

Performance tests were made on a typical MECL bus line as illustrated in Figure 1. This line is a 75-ohm microstrip built on a 0.062 inch double sided G-10 epoxy circuit board. Nine drivers and nine receivers are distributed along the 32-inch line at 4-inch intervals.

A 50-ohm termination resistor is used at each end of the line to minimize reflections. Fanout along a signal line lowers the effective characteristic impedance by the equation:

$$Z_o' = \frac{Z_o}{\sqrt{1 + \frac{C_D}{C_o \ell}}}$$

where

Z_o, the unloaded line impedance = 75-ohms

C_D, the total distributed capacitance = 5 pF per fanout

C_o, the line intrinsic capacitance per unit length = 24 pF per foot for the 75-ohm microstrip line.

ℓ = length of line in inches.

Calculating the characteristic impedance of the bus line in Figure 1 gives:

$$Z_o' = \frac{75}{\sqrt{1 + \frac{90}{24\,(2.67)}}} = 48 \text{ ohms}$$

The two 50-ohm resistors in parallel are a 25-ohm load which is beyond the specified 50-ohm drive of a standard MECL output. For this reason, MC10111 triple output gates are used as bus drivers. These gates have three outputs, each capable of 50-ohm loads. Paralleling two outputs gives the required 25-ohm drive.

Propagation delay time of the bus is a function of the line type, length, and load. Unloaded microstrip line has a propagation delay of 1.77 ns per foot for G-10 circuit board material with a dielectric constant of 5.0. This gives an unloaded propagation delay time of (32 in ÷ 12 in/ft) X 1.77 ns/ft or 4.72 ns for the 32-inch bus line. The unloaded bus model measured 4.92 ns propagation time. The slight increase from calculated time is due to added capacitance from the short stubs and differences in the dielectric constant between the test board and the calculated 1.77 ns per foot.

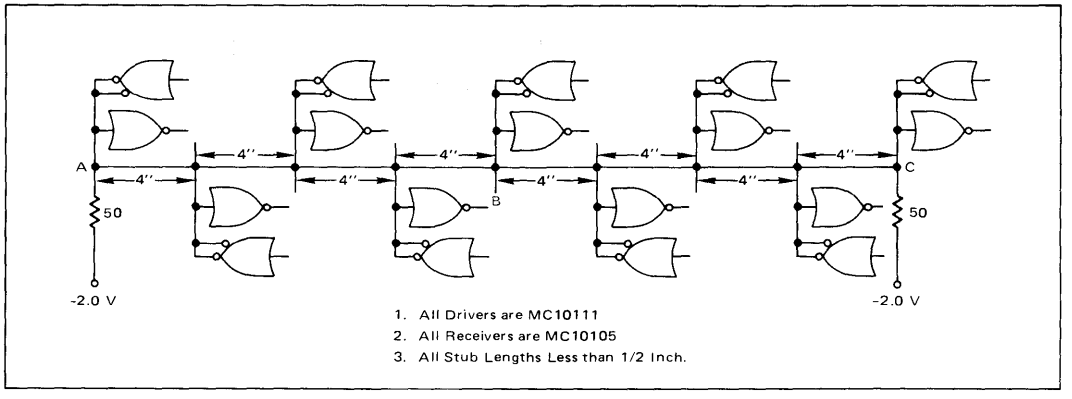


FIGURE 1 – MECL Bus Test Fixture

Propagation delay time of a loaded line may be calculated from the following equation:

$$t_{pd'} = t_{pd}\sqrt{1 + \frac{C_D}{C_{0\ell}}}$$

where t_{pd} is the unloaded line propagation delay. The bus line in Figure 1 loaded only with receiving gates has a calculated delay of:

$$t_{pd'} = 4.92\sqrt{1 + \frac{45}{24\,(2.67)}} = 6.42 \text{ ns}$$

This compares with 6.62 ns for the tested bus line.

When the bus line is loaded with both drivers and receivers, the increased distributed capacitance slows the calculated propagation delay to 7.62 ns. Test waveforms for the bus line in Figure 1 are shown in Figure 2. Propagation delay for a high or low transition is 7.7 ns and agrees with the calculated time. However, the low to high delay is increased to 9.7 ns because of a step in the rising edge of the waveform. This rising edge step is due to the output impedance characteristics of a MECL circuit. When the bus line is at a low logic level, all driver outputs are sourcing current to the termination resistors. These MECL outputs appear as low (7 to 10 ohm) impedances along the line. A rising signal traveling down the bus sees these low impedance outputs and reflects back to the sending point causing the rising edge step. After the signal rises to a level where the nondriving emitter followers are no longer sourcing current, these outputs become high impedances and reflections no longer occur. The transition from high to low is no problem because only the active driver is sourcing current and the other circuits appear as high impedances along the line.

In the preceding example, it was shown that fanout on a bus will lower the characteristic impedance of the line. This should be taken into consideration when determining termination resistor values. A low impedance line is less affected by loading than a higher impedance line. However, since a bus line is terminated at both ends, the driver output current capability must be considered as a limit to minimum line impedance.

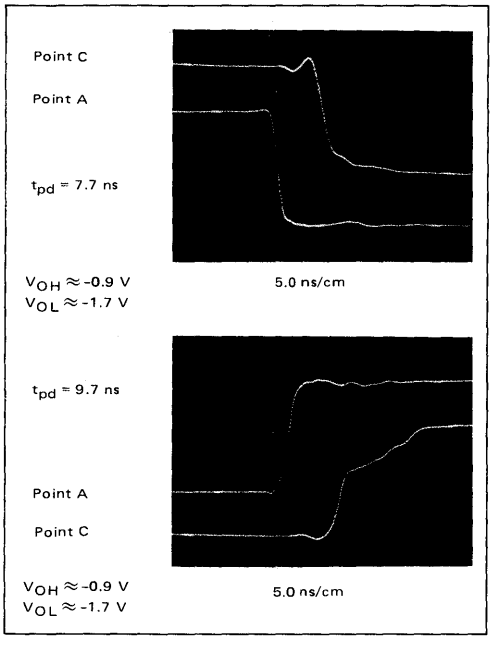


FIGURE 2 – Bus Waveforms With MC10111 Drivers

Standard MECL 10K circuits are specified driving a 50-ohm load. This equates to a 100-ohm bus line terminated at each end. Therefore, when these circuits are used as drivers, fanout density must be limited or the line will be over-terminated (actual line impedance less than 100 ohms) and reflections will occur. For short bus lengths, typically less than 12 inches, this is acceptable as reflections die out within a few nanoseconds.

Propagation delay increase with fanout must also be considered when figuring bus line performance. Propagation delay is least affected by low impedance lines. Therefore, it is usually desirable to design long bus runs with the lowest impedance line that is compatible with the driver circuits.

For short bus lines the advantage of driving the bus from any MECL circuit and not having special drivers overcomes any delay caused by high impedance lines. With longer busses, the designer has the choice of using a high impedance line with standard circuits or increasing performance by going to a properly terminated lower impedance line. Lower impedance lines require paralleling MECL circuits for increased drive or going to special circuits within the family which have better than 50-ohm drive. The recommended minimum bus line impedance is 34 ohms (17-ohm resistive load) which could be driven by MC10110 or MC10111 circuits having all three outputs wired together. The 50-ohms as in Figure 1 is a more conservative limit.

Ideally, the loading on a bus line should be evenly distributed along the line. With this type loading, the impedance is constant along the line and reflections are minimized. It is realized that in system design this is not always possible and care should be taken to avoid lumping too much capacitance at one point on a long line. For example, if lump loading is held to less than 21 pF in a 7.7-inch length of 68-ohm microstrip line, reflections will be less than 20% along the line. Additional information on lump loading is available in Chapter 7, page 145. If the loading is evenly distributed on the line, there is no practical limit to fanout density other than minimum line impedance for the driver.

The low impedance outputs of standard MECL circuits cause an impedance discontinuity on the line, and limit rising edge performance of high speed busses. If the bus lines are less than 18 inches, the reflection-caused step in the rising edge is largely hidden in the relatively slow MECL 10K rise time and performance degradation is minimal. However, for longer lines, this step in the rising edge will cause a slowing of data transfer which should be considered in the design of a high speed bus system.

THE MC10123 FOR HIGH SPEED BUSSES

When using standard MECL 10K/10KH circuits as drivers, low impedance discontinuities on the bus line caused a step in the waveform and limit the maximum performance of long bus lines. If the unused outputs could be made to have a high impedance in both the high and low logic states, bus performance would be improved. Since MECL busses are normally terminated with resistors to -2.0 volts, a MECL low logic level below -2.0 volts would turn off the emitter follower output.

The MC10123 is designed with a low logic level specified between -2.03 and -2.10 volts. Therefore, when the bus is at a low level, the line is at the -2.0 termination voltage and all drivers have a high output impedance. A rising edge sees no reflections, so rise time is improved. The primary difference in using the MC10123 as a bus driver is the bus logic levels of -2.0 and -0.9 volts instead of the normal MECL levels of -1.7 and -0.9 volts. Although not necessary or even recommended, the termination voltage could be raised to -1.7 volts and the MC10123 driven bus would have normal MECL levels with no reflections. A second feature of the MC10123 is the 25-ohm drive capability. Busses as low as 50 ohms can be terminated at each end without having to use multiple output driver circuits.

The MC10123 Bus Drivers were substituted for the MC10111's in Figure 1. The results of the MC10123 bus are in the Figure 3 waveforms. When compared with Figure 2, the step in the rising edge is missing with the associated improvement in propagation delay to 7.9 ns.

The oscilloscope photograph of the negative going edge in Figure 3 shows some ringing due to reflections at the driving end of the bus. This is because the driver goes below the termination voltage and becomes a high impedance load. Therefore, any small reflections are not clamped by the low impedance output as was the case in Figure 2. This ringing is not a problem and causes no loss of noise margin because the low level output voltage of the MC10123 bus in Figure 3 is 300 mV more negative than the normal MECL output.

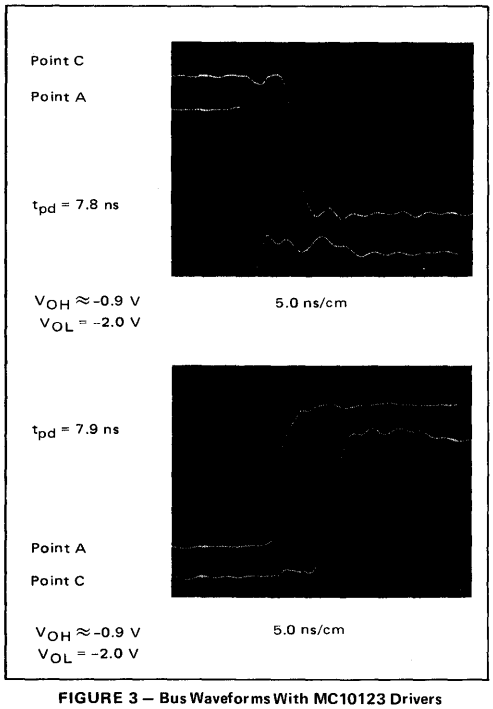


FIGURE 3 – Bus Waveforms With MC10123 Drivers

The advantages of a bus using MC10123 drivers become more apparent when signals along the bus are examined. Figure 4 shows the waveforms for the bus in Figure 1 driven at point A and the oscilloscope monitoring point B. The large step in the rising edge of the MC10111 driven bus is completely eliminated in the MC10123 bus.

The MC10123 bus driver is recommended where maximum performance is required over long line lengths and high fanout. This part minimizes reflections on the bus

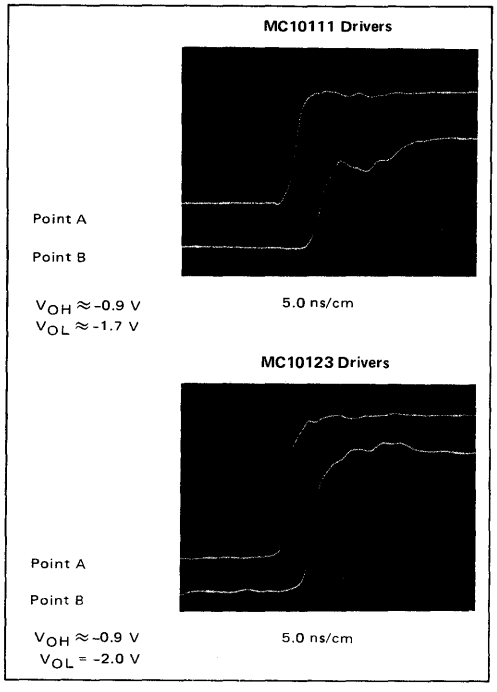


FIGURE 4 – Bus Waveforms at Midpoint

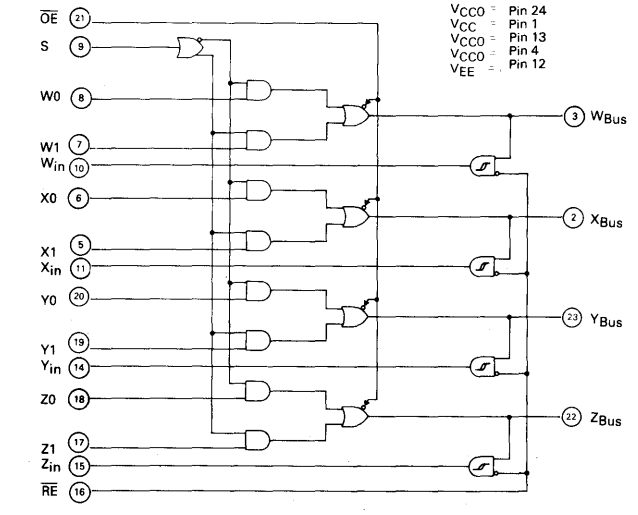
line and noticeably improves propagation delay time. However, when maximum speed is not required or lines are kept short, using standard MECL circuits as bus drivers should not be disregarded as this minimizes part count and still gives good system speed.

There is no absolute limit to the length of MECL bus lines. Lines of 25 feet and longer are possible if good transmission lines are used to restrict external noise coupling. The delays of these long lines will be significant and should be considered when calculating overall system performance.

The MC10H330 SERIES OF 25 Ω TRANSCEIVERS

The MC10H330 series consists of three 25 ohm bus transceiver parts. These devices drive and receive on a 25 ohm line as well as provide useful logic functions. The MC10H330 (Figure 5) is a quad bus driver/receiver with 2-to-1 output multiplexers. The MC10H332 (Figure 6) is a dual bus driver/receiver with 4-to-1 output multiplexers. The MC10H334 (Figure 7) is a quad bus driver/receiver with transmit and receiver latches.

This series of parts have receivers with 200 mV of hysteresis on their bus inputs to insure proper operation with a noisy bus. The outputs of these transceivers when low, appear as a high impedance to the bus and thus eliminate discontinuities in the characteristic impedance of the bus.



MULTIPLEXER TRUTH TABLE

$\overline{OE}$	S	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}
H	X	-2.0 V	-2.0 V	-2.0 V	-2.0 V
L	L	W0	X0	Y0	Z0
L	H	W1	X1	Y1	Z1

X — Don't care

RECEIVER TRUTH TABLE

$\overline{RE}$	W_{in}	X_{in}	Y_{in}	Z_{in}
H	L	L	L	L
L	W_{Bus}	X_{Bus}	Y_{Bus}	Z_{Bus}

FIGURE 5 — LOGIC DIAGRAM (MC10H330)

MULTIPLEXER TRUTH TABLE

$\overline{OE}$	S1	S0	X_{Bus}	Y_{Bus}
H	X	X	-2.0 V	-2.0 V
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

X — Don't care

RECEIVER TRUTH TABLE

$\overline{RE}$	X_{in}	Y_{in}
H	L	L
L	X_{Bus}	Y_{Bus}

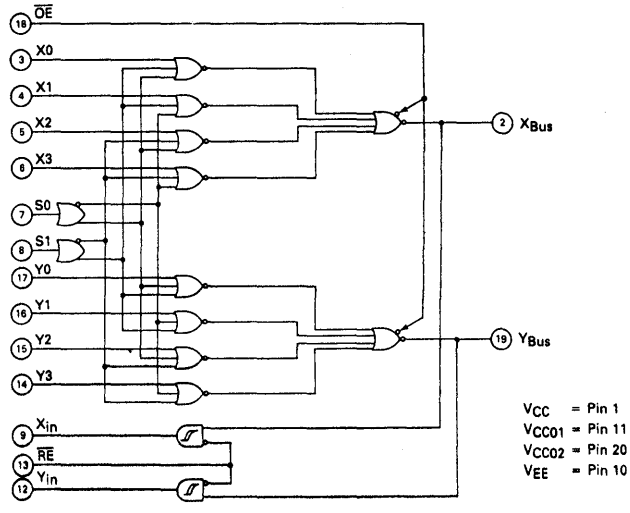
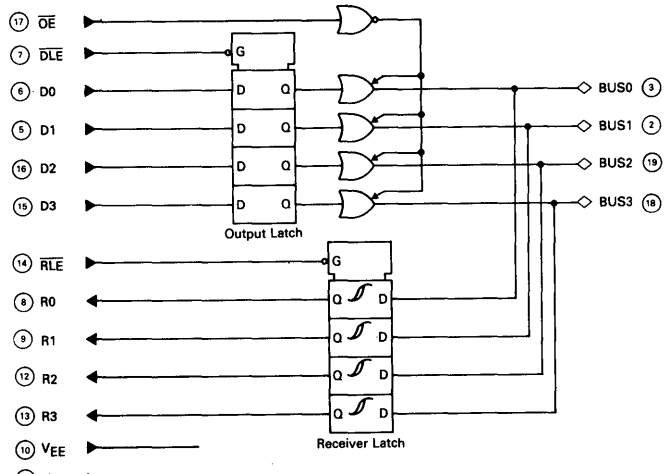


FIGURE 6 — LOGIC DIAGRAM (MC10H332)



DRIVER TRUTH TABLE

D	$\overline{DLE}$	$\overline{OE}$	Bus_{n+1}
X	X	H	-2.0 V
D	L	L	D
X	H	L	Bus_n

X — Don't care

RECEIVER TRUTH TABLE

Bus	$\overline{RLE}$	R_{n+1}
Bus	L	Bus
X	H	R_n

X — Don't care

FIGURE 7 — LOGIC DIAGRAM (MC10H334)

STUBBING OFF A MECL BUS

Stubs on a MECL bus should be designed for minimum length. A stub on a bus appears as an impedance discontinuity to a signal on the line, causing a series of reflections. The signal reaching the stub point splits, sending reduced amplitude signals down both the line and the stub. The longer the stub, the greater the time for the reflections to settle out and the signal to reach final amplitude. The primary effect of these reflections is a rounding of the signal edge, resulting in increased propagation delay and decreased bandwidth. By keeping stub lengths short, the reflections are hidden in the signal rise or fall time and high speed performance is maintained.

Reflections and waveforms at points along a bus can be analyzed with a lattice diagram. A lattice diagram shows the amount of signal reflected at discontinuities on a line, allowing waveforms to be calculated. Reflection coefficients are used to determine the amplitude of each reflection. Additional details on lattice diagrams can be found in Chapter 7, (Ref. 1).

Figure 8 shows a bus being driven from one end (point A), a stub on the bus (points B and C) and a terminated end at point D. The reflection coefficients are calculated from the formula:

$$\rho = \frac{Z1 - Z2}{Z1 + Z2}$$

Where Z1 is the line impedance before the discontinuity and Z2 the characteristic impedance after the discontinuity as seen from the driving source. Figure 8 also shows the reflection coefficients at key points on the bus for a 75-ohm line. A high logic level output impedance of 10 ohms for the MC10123 driver is used in the output high calculations and a very high output impedance is used for the low logic level reflection coefficient. The line will be analyzed for both conditions.

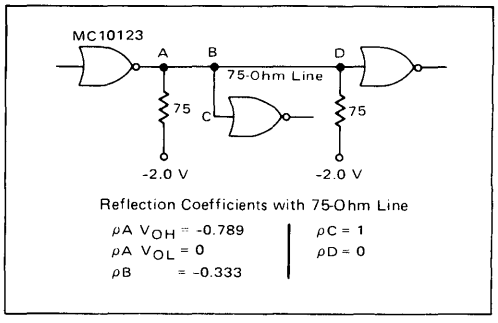


FIGURE 8 — Reflection Coefficients for a Stub on a MECL Bus Line

Figure 9 is the lattice diagram for the bus in Figure 8. Points A, B, C, and D are the four vertical lines. Time is determined by the vertical scale as a function of line and stub propagation delays. This particular lattice diagram was drawn with the stub length B to C much shorter than line A to B to allow the B to C reflections to settle out before the reflections from B to A returned.

Following the lattice diagram, at time 0 a signal leaves point A with an amplitude normalized to 1.0. After propagation delay time A to B, the signal reaches point B. Here the signal sees a discontinuity with a reflection coefficient equal to -0.333. A signal of -0.333 returns down the line from B to A and the difference between the initial signal (1.0) and the reflected signal (-0.333) of +0.667 travels down both lines B to C and B to D. The voltage at point B is also equal to 0.667 of the initial signal. After propagation delay time BC, the signal reaches point C, sees a reflection coefficient of 1.0 and reflects back to B. This returning reflection at B sees a reflection coefficient of -0.333 and reflects back to point C with an amplitude of (0.667) x (-0.333) or -0.222. The difference between 0.667 and -0.222 travels down line B to A and B to D. These reflections between B and C continue, each getting smaller until they die out.

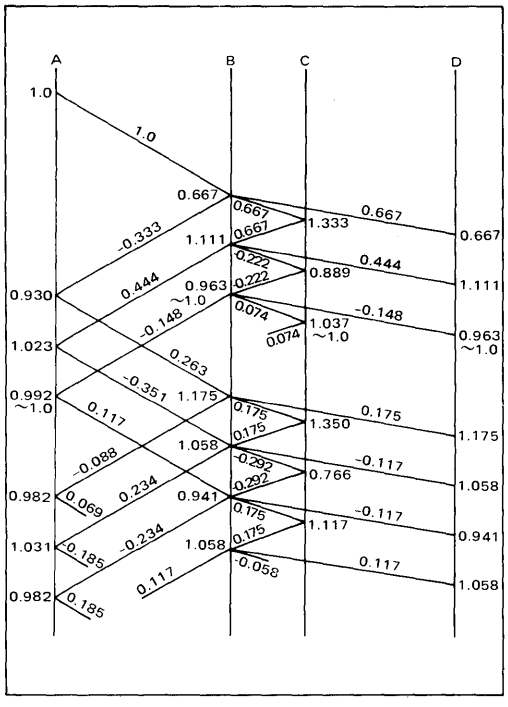


FIGURE 9 — Lattice Diagram for End-Driven Line with Stub

If the driver at point A has a low output level, the line is properly terminated at 75-ohms, no reflections occur and the sequence is terminated. However, if the driver is in a high state, the reflected signal from B to A sees the 75-ohm termination resistor and the MECL output impedance or a reflection coefficient of -0.789. This results in a reflected signal going from A to B delayed in time from the initial signal by twice the A to B propagation delay. This signal, smaller in amplitude than the original signal, causes another series of B to C reflections.

Point D need not be considered from a signal reflection standpoint since this point is always properly terminated. The waveshape at point D is the same as point B delayed in time by one B to D propagation delay.

Plotting the waveforms at A, B, and C, as shown in Figure 10, illustrates the results of reflections on the line. The initial signal ends up with a big step at two-thirds amplitude that results in a greatly increased 10-90% rise time. The increase in rise time would occur at each succeeding stub along the line. Also, a reflected pulse from point A results in a negative pulse along the line that can cause a loss of noise immunity.

A test fixture was constructed with a 12-foot, 75-ohm line between points A and B, a 2-foot stub B to C, and a 4-foot length for B to D. To get a fast signal edge, the line was driven by a pulse generator with 1.0 ns edge speed. **The photograph in Figure 11 shows the waveforms at points A, B, and C, and has a very good correlation with the lattice diagram calculations.**

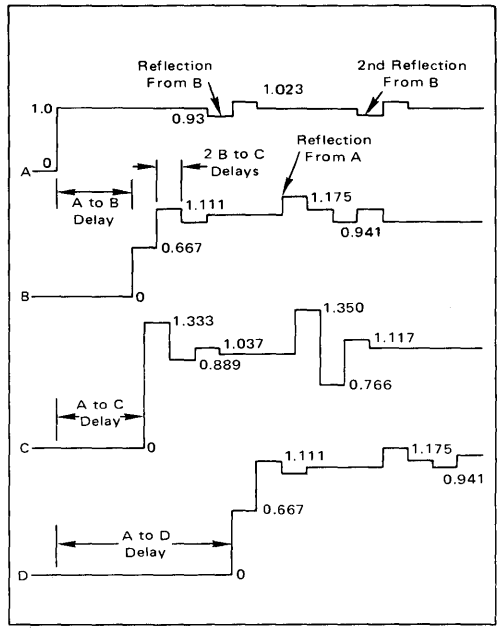


FIGURE 10 — Waveforms of Figure 6 Lattice Diagram

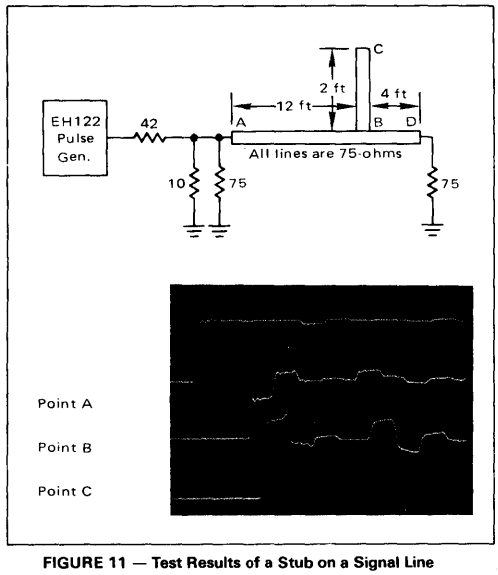


FIGURE 11 — Test Results of a Stub on a Signal Line

In addition to driving a bus from one end as in the previous example, it is necessary to drive from points along the line. This type of bus and the associated lattice diagram are shown in Figure 12. Waveforms at points on the line, Figure 13, point out the slowing of edge speed caused by reflections between points B and C. Unlike the previous example, reflections from the line ends need not be considered since both ends are properly terminated.

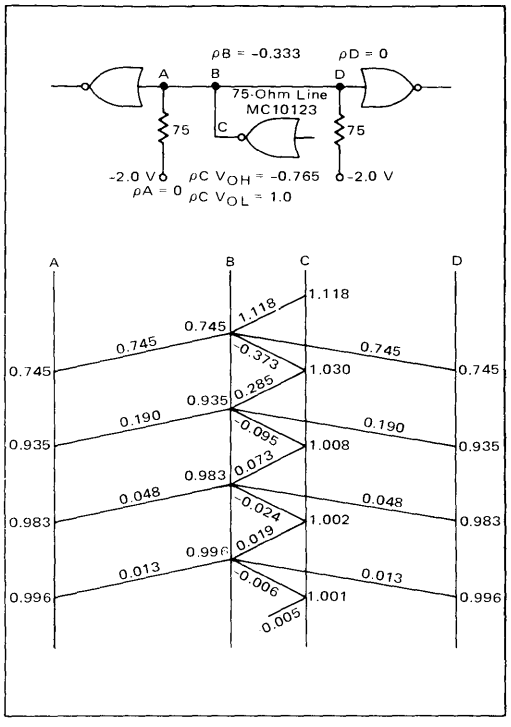


FIGURE 12 — Lattice Diagram for Center-Driven MECL Bus

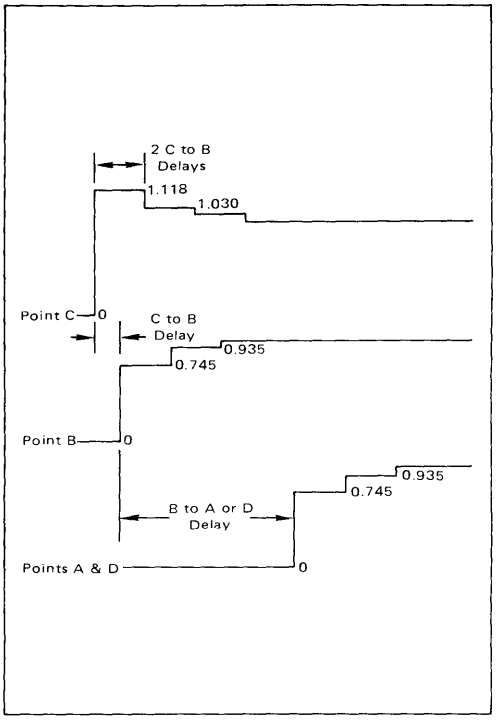


FIGURE 13 — Waveforms of Figure 9 Lattice Diagram

Notice also the initial signal at point C is 1.118. This value was calculated to give a final bus voltage normalized to 1.0. The driving circuit sees a final load of 37.5 ohms and an initial load of only the 75-ohm stub. An output impedance of 10 ohms gives an overshoot of 11.8% at point B which drops to a final value of 1.0 as the reflections die out.

This section using lattice diagrams appears to show that stubs cause a serious loss of edge speed when used in a high speed system. However, this will be true only if the stubs are long with respect to the signal edge speed. If stubs are sufficiently short, the reflections decay very rapidly. For example, a 1-inch stub on microstrip board has a one way propagation delay time of 0.148 ns. This means 5 two-way delay times, normally enough for reflections to settle out, occur within 1.5 ns or about one-half a MECL 10K 10 to 90% rise time. The waveforms in Figure 3 are for a bus with 14 short stubs. Although there are some minor reflections, the signals will work very well in a MECL system.

There is no strict limit to stub lengths which can be used in a MECL system. If time permits reflections to settle out, long stubs (greater than 6 inches) can be used. However, when top speed is required, stubs will have to be kept shorter. If the bus is restricted to one circuit board, stub lengths can be kept to one-half inch and not be noticed. When the bus is constructed in a system backplane and must fanout to several cards, bus stubs should be restricted to 1.5 to 2 inches. This is sufficient to get through the card connector and to a MECL package near the connector. For these bus runs, it is usually better to have the bus driver and receiver near the edge connector or use buffer gates in place of running long stubs on the circuit board.

CONCLUSION

Although only a few examples have been presented, the techniques described in this application note can be used with a wide variety of bus lengths and fanout densities. The importance of operating in a transmission line environment has been demonstrated by the good correlation between calculations and test results. Using proper termination practices and considering the effects of reflections on a bus line can lead to higher performance and error free operation from a high speed MECL system.

IC CRYSTAL CONTROLLED OSCILLATORS

INTRODUCTION

If a circuit is to produce sustained oscillation, it must contain an amplifier with a feedback network capable of 360° phase shift from output to input. For the circuits discussed in this application note, the amplification is achieved with MECL 10K gates or line receivers. The use of a MECL gate as an amplifier may be explained with the aid of the basic MECL 10K circuit schematic shown in Figure 1. The circuit consists of inputs, amplifier, bias and outputs. As the input makes small excursions around V_{BB} the OR output will amplify this signal, while the NOR output will amplify and invert the signal. Thus, the MECL 10K gate may be treated as an amplifier or an inverting amplifier, depending on which output is under consideration.

In accordance with MECL 10K design rules all unused single-ended inputs may be left unconnected. Differential input devices such as the MC10115 or MC10116 do not have internal input pulldown resistors and cannot be left floating. If a differential receiver stage of either device type is unused, one input of the receiver should be tied to the V_{BB} pin provided, and the other input to V_{EE}. Also, since the circuits presented are intended for high frequency use, good layout procedures should be used, keeping leads as short as possible.

For the feedback network, a quartz crystal is used in the series resonant mode of oscillation, providing a low impedance path from output to input when operating at or near resonance. An electrical equivalent circuit of a quartz crystal is shown in Figure 2. L, R, and C_s represent the piezoelectric characteristics of the quartz crystal, while C_o represents the static capacitance between leads.

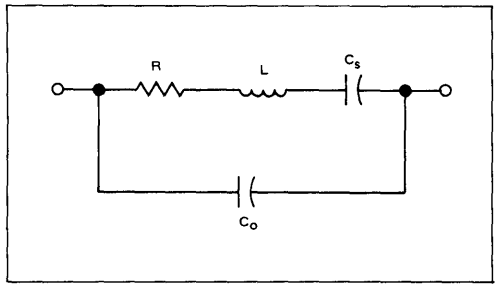


FIGURE 2 – Equivalent Circuit of a Quartz Crystal

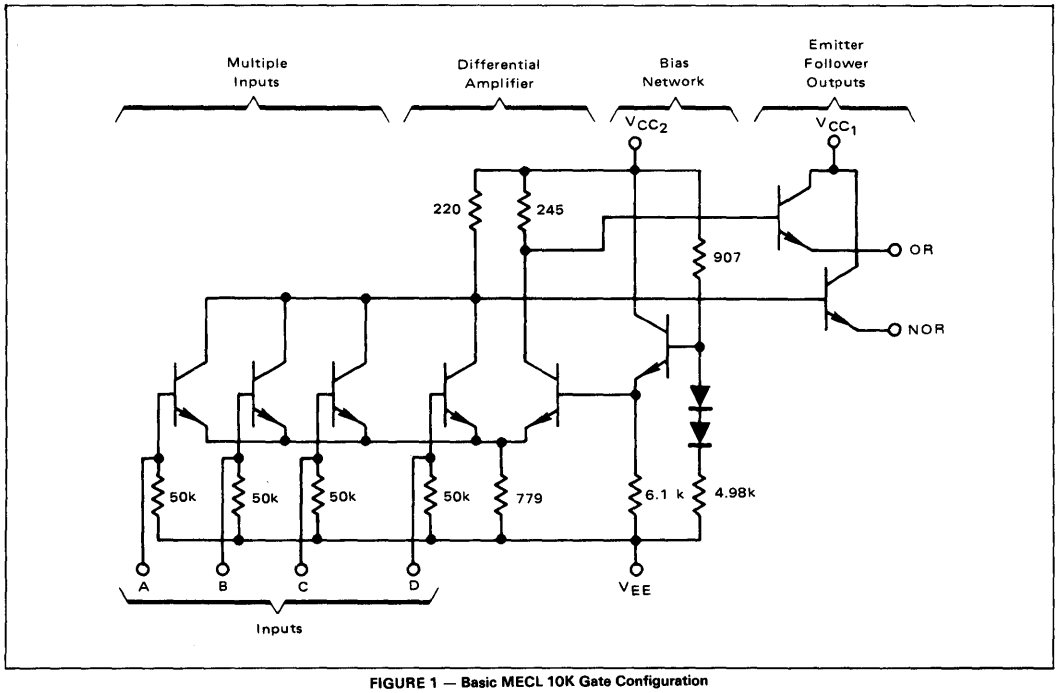


FIGURE 1 — Basic MECL 10K Gate Configuration

An inspection of the equivalent circuit reveals that two modes of resonance are possible; the series resonant frequency of L and C_S, and the parallel resonant, or antiresonant frequency of L and C_O. As mentioned earlier, the mode of operation to be employed here is the series resonant mode. With the crystal operating in this manner, the reactances of L and C_S effectively cancel each other and the resulting feedback path then consists of the resistance R, shunted by C_O.

Due to processing limitations during manufacture, the maximum resonant frequency of most quartz crystals is approximately 20 MHz. For frequencies above 20 MHz, crystals are used which will oscillate at a harmonic, or "overtone" of their fundamental frequency. When the desired oscillator frequency requires that an overtone crystal be used, additional precautions must be taken in the design of the circuit to insure that it will oscillate only at the desired frequency. This is because an overtone crystal will operate at harmonics other than the one intended, as well as the fundamental frequency.

The use of MECL 10K circuits in crystal oscillators has several advantages over conventional circuitry. When a second gate is used as a buffer for the oscillator, there is minimum frequency change with output loading. Also, the high input impedance and 0.8 volt logic swing prevent the possibility of overdriving the crystal. In addition, circuits presented in this note are frequency insensitive to ±20% power supply variations, and the frequency versus temperature characteristics closely follow the crystal characteristics.

AN OVERTONE CRYSTAL OSCILLATOR

Figure 3 illustrates a circuit employing an adjustable resonant tank circuit which insures operation at the desired crystal overtone. C_1 and L_1 form the resonant tank circuit, which with the values specified has a resonant frequency adjustable from approximately 50 MHz to 100 MHz. Overtone operation is accomplished by adjusting the tank circuit frequency at or near the desired frequency. The tank circuit exhibits a low impedance shunt to off-frequency oscillations and a high impedance to the desired frequency, allowing feedback from the output. Operation in this manner guarantees that the oscillator will always start at the correct overtone.

The reference voltage for the differential amplifier (mentioned in the discussion of the basic MECL gate) is supplied internally by the MC10116 and has a nominal value of -1.3 volts when V_{CC} = ground and V_{EE} = -5.2 volts (recommended MECL voltages). For the oscillator to function properly, the non-feedback input of the differential amplifier must be biased near V_{BB} or -1.3 volts. This is accomplished by L_1 which is connected to a V_{BB} source.

The V_{BB} source can be obtained from V_{BB} output on MC10114, MC10115, or MC10116 line receivers. Alternately, a V_{BB} source can be generated with a MECL gate by connecting the NOR output to an input; the circuit is then biased in the center of the logic swing or at V_{BB}. A 0.001 μF capacitor insures the V_{BB} generator does not oscillate. R_p is an output pulldown resistor required with all MECL 10k outputs.

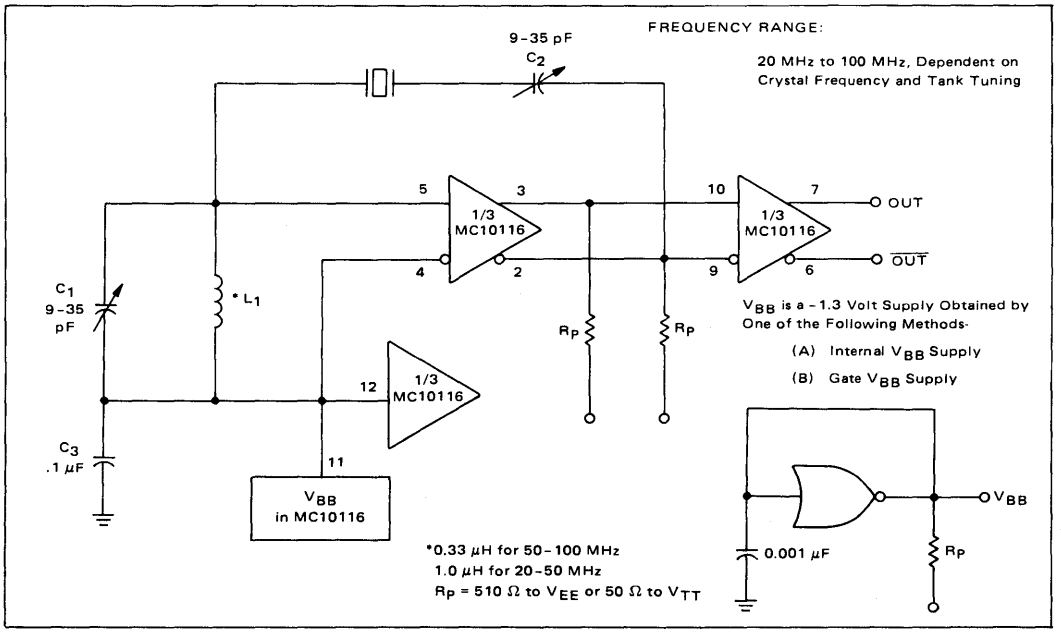


FIGURE 3 – MECL Overtone Crystal Oscillator

Capacitor C_2 adjusts the overtone frequency feedback phase shift. This insures operation on the intended overtone frequency. The second receiver serves the dual purpose of a buffer and wave shaper. The output of the first receiver, which is approximately a sine wave, is fed into the second receiver, which shapes it into a square wave with rise and fall times of approximately 2 ns. It should be noted that both the square wave and its complement are simultaneously available at the second circuit due to the OR/NOR configuration of MECL gates.

Although the circuit shown in Figure 3 is usable in the 50 MHz to 100 MHz range, it is restricted to these frequencies only by the specified values of L_1 and C_1. The operating frequency range can be moved in either direction by changing the value of L_1 and/or C_1. For example, if the value of L_1 is changed to 1 μH, and C_1 remains unchanged, the usable frequency range will now cover, approximately, 27 MHz to 50 MHz as predicted from the formula

$$f \approx \frac{1}{2\pi\sqrt{L_1C_1}}.$$

A FUNDAMENTAL FREQUENCY CRYSTAL OSCILLATOR

For frequencies below 20 MHz, a fundamental frequency crystal can be used and the resonant tank is no longer required. Also, at this lower frequency range the typical MECL 10,000 propagation delay of 2 ns becomes small compared to the period of oscillation, the typical MECL 10K propagation delay of 2 ns becomes small compared to the period of oscillation, and it becomes necessary to use a non-inverting output. A schematic of a circuit which works well at the lower frequencies is shown in Figure 4. Since the non-inverting output is used, the MC10116 oscillator section functions simply as an amplifier. The 1.0 k resistor biases the line receiver near V_{BB} and the 0.1 μF capacitor is a filter capacitor for the V_{BB} supply. V_{BB} is available as an output on the MECL line receiver circuits. The capacitor, in series with the crystal, provides for minor frequency adjustments.

The second section of the MC10116 is connected as a Schmitt trigger circuit. This insures good MECL edges from a rather slow, less than 20 MHz, input signal. The third stage of the MC10116 is used as a buffer and to give complementary outputs from the crystal oscillator circuit.

The circuit in Figure 4 has a maximum operating frequency of approximately 20 MHz and a minimum frequency of approximately 1 MHz. Also, as mentioned earlier, it is intended for use with a crystal which operates in the fundamental mode of oscillation.

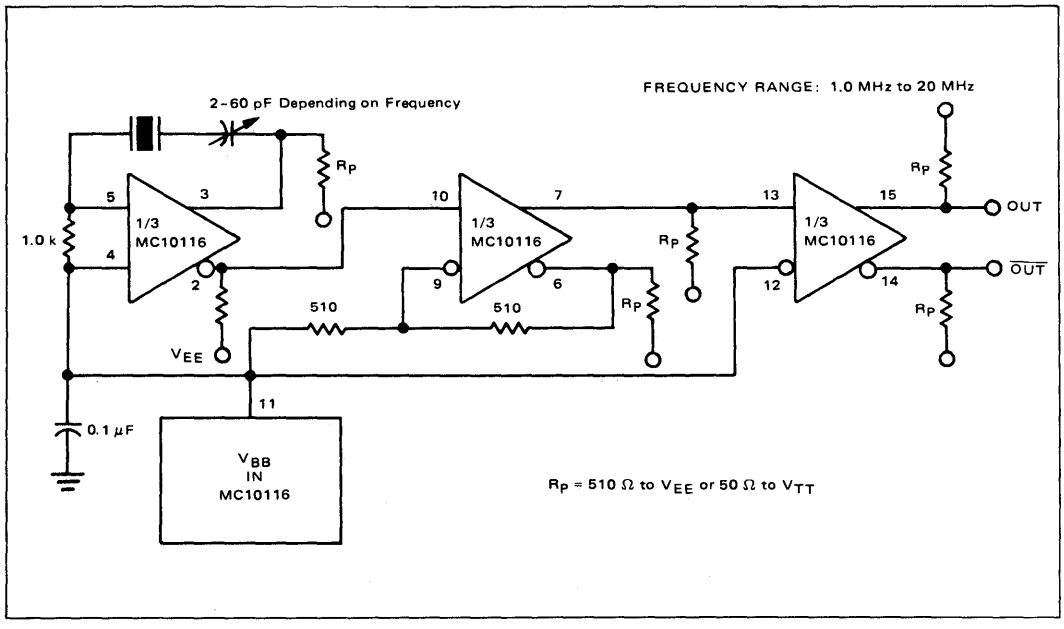


FIGURE 4 – MECL Fundamental Crystal Oscillator

HIGH FREQUENCY CRYSTAL OSCILLATORS

The high speed performance of MECL III often requires a stable oscillator in the 200 to 300 MHz range. Standard crystals are normally limited to less than 150 MHz because of the high order of harmonics required at these frequencies. A higher speed oscillator is possible by combining a MECL 10K crystal oscillator with a MECL III frequency doubler as shown in Figure 5.

One section of the MC10101 is connected as a 100 MHz crystal oscillator with the crystal in series with the feedback loop. The LC tank circuit tunes the 100 MHz harmonic of the crystal and may be used to calibrate the circuit to the exact frequency. A second section of the MC10101 buffers the crystal oscillator and gives complementary 100 MHz signals.

The frequency doubler consists of two MC10101 gates as phase shifters and two MC1662 NOR gates. For a 50% duty cycle at the output, the delay to the true and complement 100 MHz signals should be 90°. This may be built precisely with 2.5 ns delay lines for the 200 MHz output or approximated by the two MC10101 gates as shown in Figure 5. The gates are easier to incorporate and cause only a slight skew in output signal duty cycle. The MC1662 gates combine the 4-phase 100 MHz signals as shown in Figure 6. The outputs of the MC1662's are wire-OR connected to give the 200 MHz signal. MECL III gates are used because of the bandwidth required for 200 MHz signals.

One of the remaining MC1662 gates is used as a V_{BB} bias generator for the oscillator. By connecting the NOR output to the input, the circuit stays in the center of the logic swing or at V_{BB}. A 0.001 μF capacitor insures the V_{BB} circuit does not oscillate.

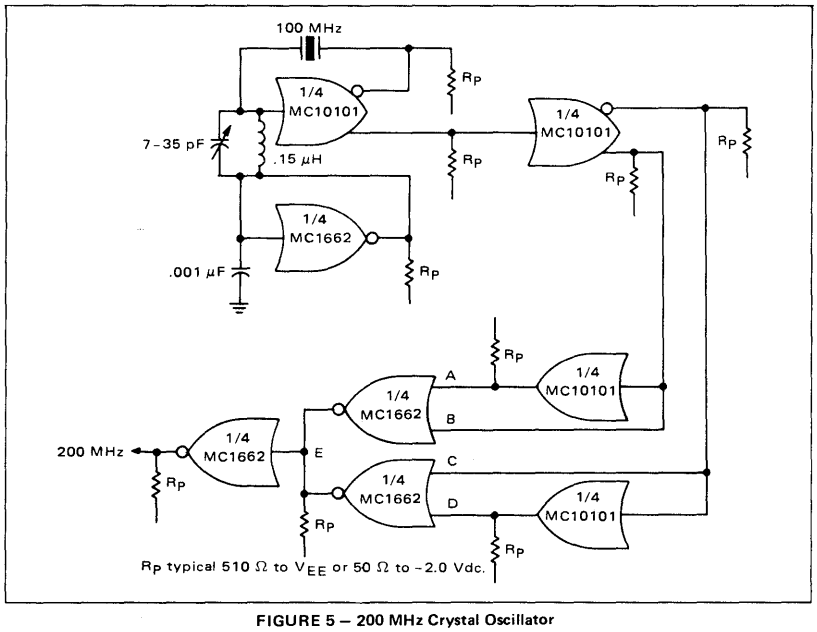


FIGURE 5 – 200 MHz Crystal Oscillator

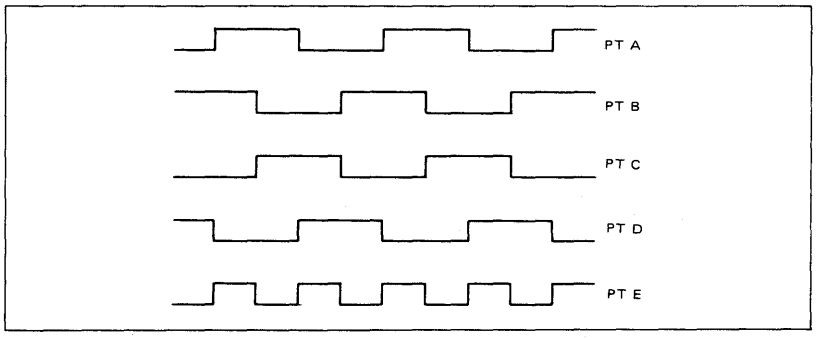


FIGURE 6 – Frequency Doubler Waveforms

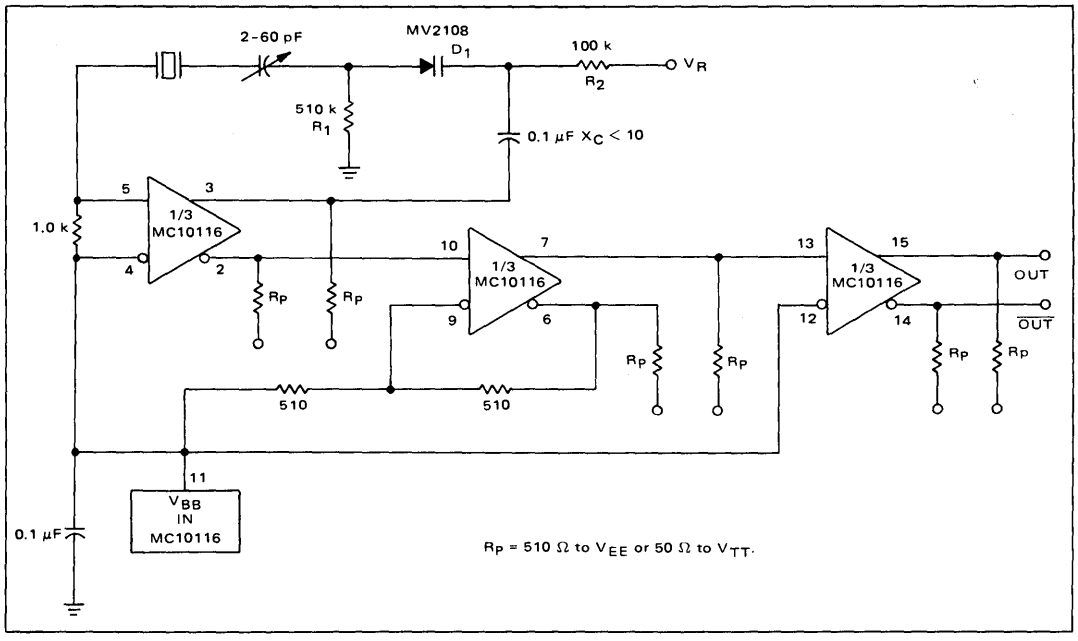


FIGURE 7 –MECL Voltage Controlled Crystal Oscillator

VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

The voltage controlled crystal oscillator, Figure 7, is a variation of the fixed frequency circuit in Figure 4. A voltage-variable capacitance tuning diode is placed in series with the crystal feedback path. Changing the voltage on V_R varies the tuning diode capacitance and tunes the oscillator. The 510 k resistor, R_1, establishes a reference voltage for V_R (ground is used in this example). A 100 k resistor, R_2, isolates the tuning voltage from the feedback loop and a 0.1 μF capacitor, C_2, provides ac coupling to the tuning diode.

The circuit operates over a tuning range of 0 to 25 volts. It is possible to change the tuning range from 0 to -25 volts by reversing the tuning diode D_1. Center frequency is set with the 2–60 pf trimmer capacitor. Deviation on either side of center is a function of the crystal frequency. Table 1 shows measured deviation in parts per million for several tested crystals.

The high speed crystal oscillators in this application note are useful in advanced instrumentation, frequency synthesizer, and processor systems.

TABLE 1
Crystal Frequency Deviation

NOMINAL FREQUENCY	DEVIATION	
MHz	+PPM	-PPM
1.0000	57.0	48.0
1.8432	95.5	80.3
10.000	197.4	202.8
15.000	325.4	322.9

PROGRAMMABLE COUNTERS USING THE MC10136 AND MC10137 MECL 10K UNIVERSAL COUNTERS

INTRODUCTION

Phase-locked loop and frequency synthesis applications often require programmable counters with high frequency capability. As the family of MECL 10K MSI functions has grown to include two new universal counters the MC10136 and MC10137, programmable counters may now be designed with an operating frequency capability in excess of 100 megahertz. This performance is about 4 times that possible with standard 7400 Series TTL MSI in the same application.

The preset and count (up or down) features of these two synchronous counters are utilized to design counting systems with variable divide moduli. To exploit maximum frequency capabilities of the MC10136 and MC10137, pulse "gobbling"* techniques (see below) are also used in the system design.

COUNTER OPERATION

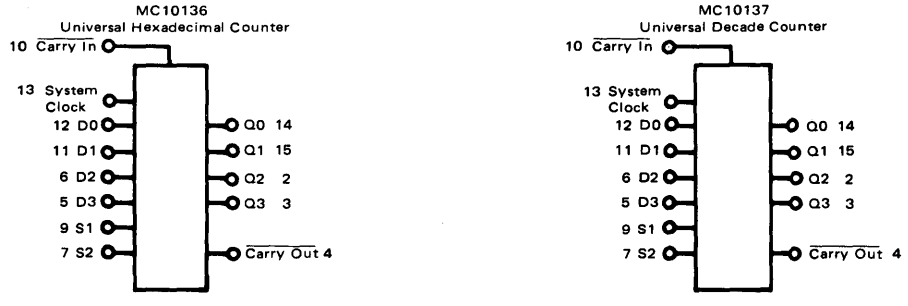
The MC10136 and MC10137 are both fully sunchronous counters. The MC10136 is a hexadecimal (0 thru 15 binary) counter, and the MC10137 is a BCD decade counter. Operation of both counters is similar; that is, three control lines (S1, S2, $\overline{C}_{in}$) determine the operational mode of the counter. Lines S1 and S2 control one of four operations: preset (program); increment (count up); decrement (count down); or hold (stop count). Figure 1 shows the logic configurations for each counter and the function select table applicable to both counters.

In the preset mode a clock pulse is necessary to load the counter. When the S1 and S2 select lines are both in the LOW state, the information present on the data inputs (D0, D1, D2, D3) will be entered into the counter on the positive transition of the clock.

The system clock is defined as positive going, and the counters change state only on the rising edge of the clock signal. Due to the master-slave construction of the flip-flops, any other data or control input may change at any time other than during the positive transition of the clock (observing proper set-up and hold times).

The $\overline{C}_{in}$ line overrides the clock when the counter is in either the increment mode or the decrement mode of operation. This input allows several devices to be cascaded into a fully synchronous multistage counter.

*Pulse "gobbling": A technique by which an external flip-flop is used to "hold" a pulse, thus acting as an auxiliary counter.



FUNCTION SELECT TABLE

S1	S2	OPERATING MODE
0	0	Preset (Program)
0	1	Increment (Count up)
1	0	Decrement (Count Down)
1	1	Hold (Stop Count)

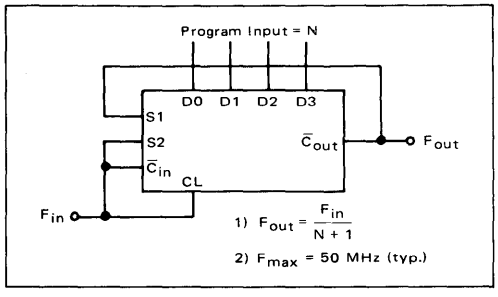
FIGURE 1 — MECL 10K Universal Counter Logic Diagrams and Function Select Table.

The $\overline{C}_{out}$ output goes LOW on the terminal state of the counter, whether in the increment mode or the decrement mode of operation. With both counters, the $\overline{C}_{out}$ output goes LOW on the zero state when operating in the count-down mode. The count-up mode causes the $\overline{C}_{out}$ to go LOW at the count of 15 for the MC10136, and at the count of 9 for the MC10137.

$\overline{C}_{out}$ is obtained by ORing $\overline{C}_{in}$ with the outputs of the counter. In this manner the carry is rippled through the counter for multistage applications.

PROGRAMMABLE COUNTERS USING NO EXTERNAL GATING

Both the MC10136 and MC10137 may be used in a programmable counter without external gating. Figure 2 illustrates a technique in which $\overline{C}_{out}$ is used to control the counter's operational mode.



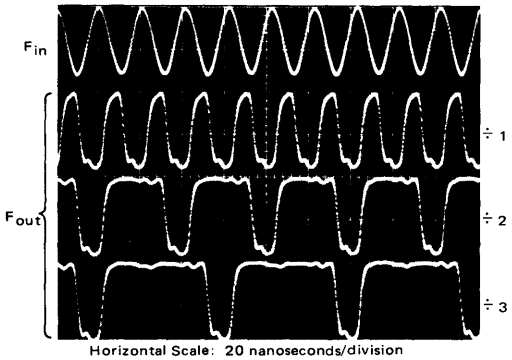


FIGURE 2 – Programmable Counter Using no External Gating. Divide Modulus M = N + 1.

The counter is normally in the decrement mode and counts down from the number N preset into the device. On reaching the "zero" state the $\overline{C}_{out}$ goes LOW and allows the next clock pulse to reload the number N into the counter. The divide modulus M then is equal to N+1.

The clock signal is tied common to the $\overline{C}_{in}$ and S2 control lines to prevent a latch-up state when reloading the counter. In the program mode $\overline{C}_{out}$ is forced LOW and $\overline{C}_{in}$ is disabled. $\overline{C}_{out}$, fed back to the S1 line, would latch up the counter unless the clock is tied to the other control lines.

As noted previously, the range in divide modulus will determine the choice between the MC10136 or the MC10137. For the MC10136, M may vary from 1 to 16; for the MC10137, M may vary from 1 to 10. Maximum toggle frequency in both cases is over 50 MHz, Figure 2 shows typical waveforms at 50 MHz.

If a larger divide modulus is required, two or more devices may be used in a larger counter – at a sacrifice in maximum operating frequency. Figure 3 shows a two-stage configuration with maximum frequency typically 35 MHz. The divide modulus is extended to 256 with the MC10136 and to 100 with the MC10137.

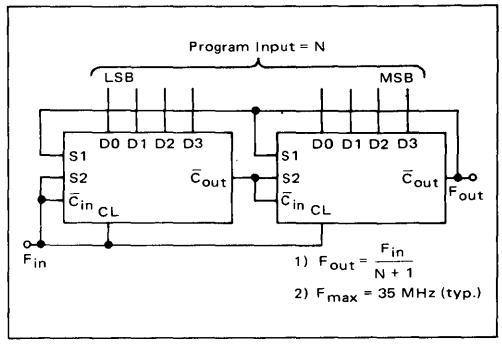


FIGURE 3 – Two-Stage Programmable Counter. Divide Modulus M is 256 Maximum with MC10136.

HIGHER FREQUENCY COUNTERS

Other techniques may be used to produce higher frequency programmable counters. External decoding and pulse "gobbling" allow higher performance at the cost of an increased package count.

One of the above improvements is used in the counter of Figure 4. A gate is used to externally decode the preset condition for the counter. This can decrease delay time by 2 to 3 nanoseconds. Using a MECL 10K gate, maximum operating frequency is typically 75 MHz.

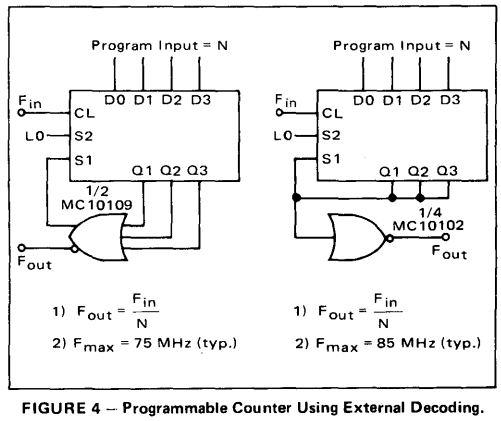
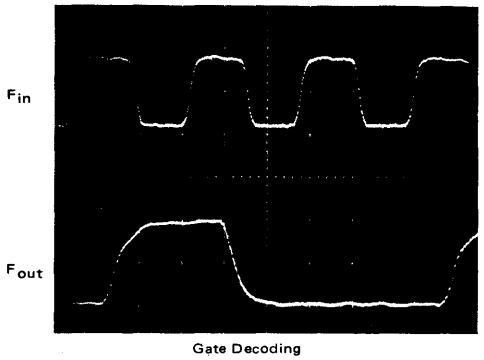


FIGURE 4 – Programmable Counter Using External Decoding. Either a Gate or a Wired-OR May be Used.

The divide modulus for this counter is equal to the program input N, (M = N). The preset condition is decoded one clock pulse before the zero state of the counter. In this manner the clock pulse necessary for preset is included in the programmed input number N. For the MC10136, M may vary from 2 to 15, and from 2 to 9 for the MC10137.

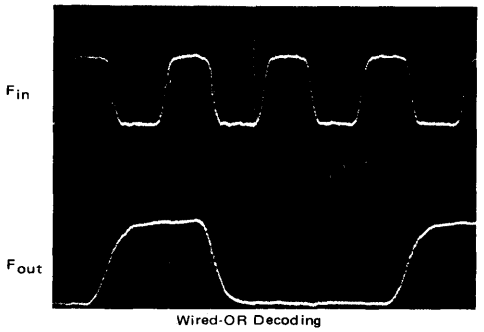
A wired-OR may be used in place of the OR gate. Maximum operating frequency can be extended to 85 MHz with this technqiue. A gate should still be used, however, to buffer the signal out (F_{out}).

In Figure 5, F_{out} and F_{in} waveshapes are shown for both circuit configurations. Notice that the frequency of the Wired-OR is displayed at 85 MHz, as opposed to the 75 MHz shown for the gate version. Both are dividing by a modulus of 3.



Gate Decoding

Horizontal Scale: 5 nanoseconds/division
Vertical Scale: 500 millivolts/division



Wired-OR Decoding

Horizontal Scale: 5 nanoseconds/division
Vertical Scale: 500 millivolts/division

FIGURE 5 – Waveforms for Programmable Counters Using External Decoding.

A second higher frequency technique incorporates pulse "gobbling" (Figure 6). In addition to externally decoding the preset condition, a flip-flop is used to "gobble" a pulse and provide an even shorter preset delay time than the external decoding version.

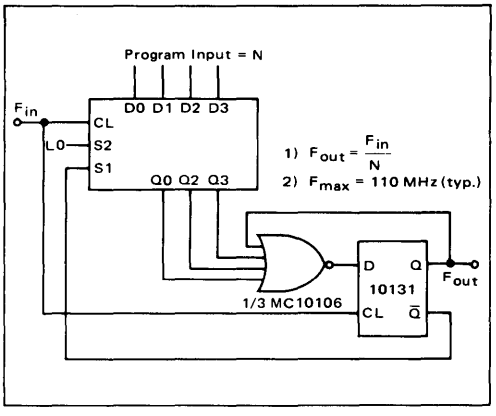


FIGURE 6 – Programmable Counter Using External Decoding and Pulse Gobbling. Divide Modulus M = N.

The pulse diagram in Figure 7 shows the sequence of signals for this counter. The S1 line is HIGH during the count phase of operation. On reaching the count of 2, the D input line to the flip-flop is forced HIGH. On the next clock pulse the HIGH state is clocked into the flip-flop, causing the S1 line and the D input line both to go LOW. The succeeding clock pulse presets the counter and loads a LOW back into the flip-flop, causing the S1 line to return to a HIGH state. The counter is then ready to proceed in the decrement count mode. In the diagram the number 8 was loaded into the counter.

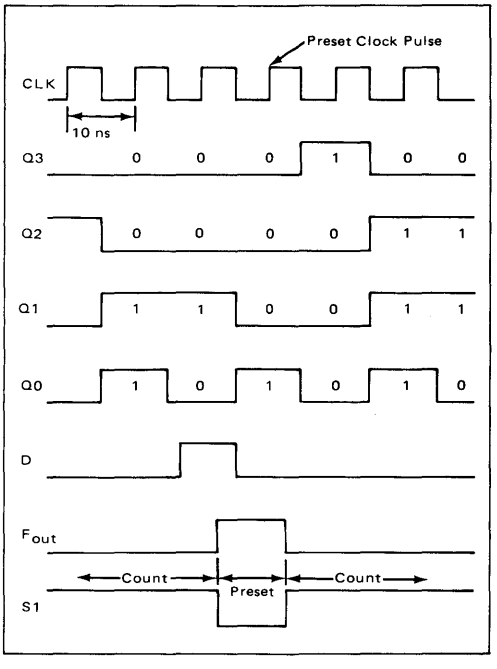
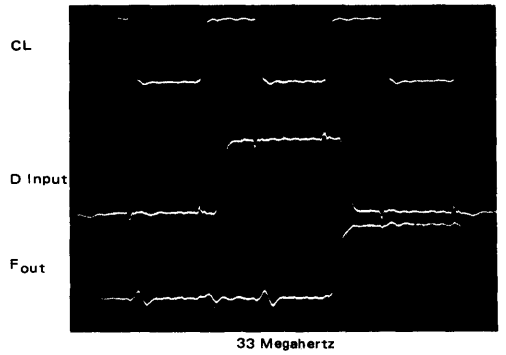


FIGURE 7 – Pulse Diagram for Pulse Gobbling Technique

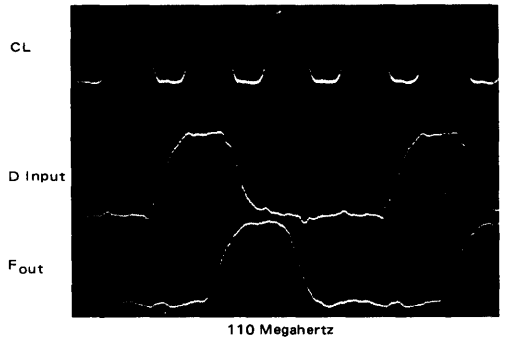
The advantage of this technique is that the decode delay and set-up time for presetting the counter do not have to occur within one clock period. These two times occur within separate clock periods. Again this allows a higher frequency of operation. Maximum frequency is typically about 110 MHz.

Examples of some of the actual waveforms idealized in the pulse diagram are presented in Figure 8. The F_{in} (or CL), the D input to the flip-flop, and F_{out} are shown. The sequence is as discussed in the previous paragraphs, although the divide modulus is 3. Two frequencies – 33 MHz and 110 MHz – are shown.

The divide modulus M is similar to the preceding design, that is, M equals the program input N. For larger moduli counters, two counters may be cascaded using the pulse gobbling technique (Figure 9). The divide modulus may be extended to 255 with two MC10136's. The maximum frequency is about 80 MHz for such a configuration.



33 Megahertz
Horizontal Scale: 10 nanoseconds division
Vertical Scale: 500 millivolts division



110 Megahertz
Horizontal Scale: 5 nanoseconds/division
Vertical Scale: 500 millivolts/division

FIGURE 8 – Waveforms for Programmable Counter Using Pulse Gobbling

CONCLUSION

In the preceding designs, either universal counter may be used. The choice of either the MC10136 or the MC10137 will normally be based upon the range in divide modulus desired. In all cases the program input N is binary coded (hexadecimal or BCD). The number preset or loaded into the counter is the initial state from which decrement starts.

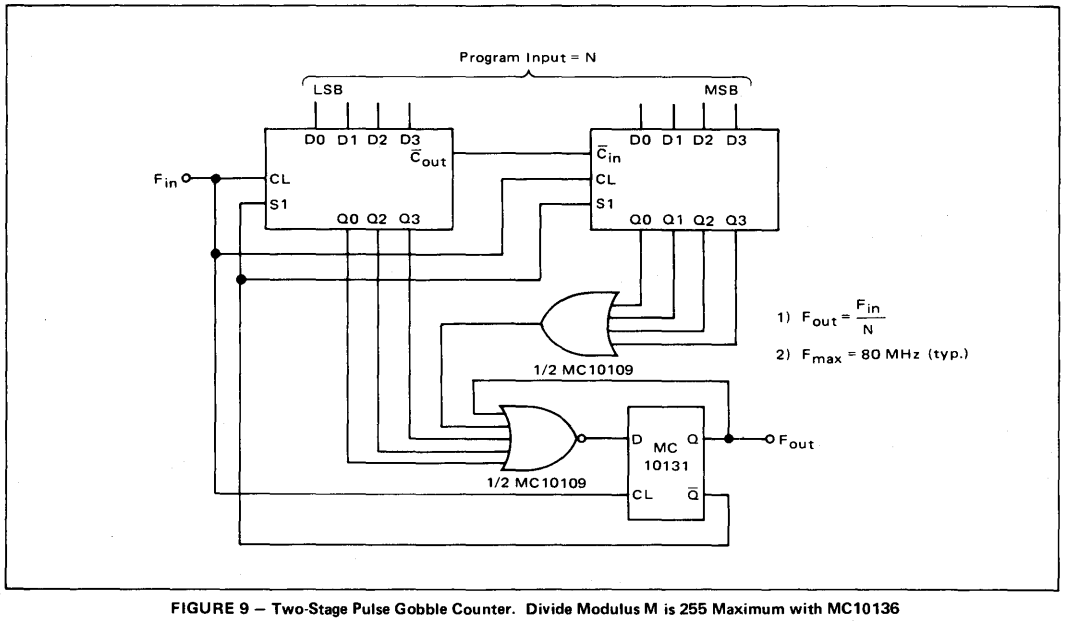


FIGURE 9 – Two-Stage Pulse Gobble Counter. Divide Modulus M is 255 Maximum with MC10136

M10800 MECL LSI CIRCUITS ARE DESIGNED FOR HIGH-PERFORMANCE MICROPROGRAMMED PROCESSORS

The M10800 family is a set of high-speed LSI circuits that combine an advanced bit-slice architecture with MECL circuit technology for overall system performance. This application note describes each family part type, then illustrates how the circuits can be interconnected in typical microprogrammed processor examples.

The evolution of high-speed bipolar LSI has progressed toward building blocks which can be interconnected into high-speed processor systems. Unlike the slower speed MOS technologies which have evolved into sophisticated microprocessors and interface circuits, high-speed bipolar circuits give the designer control over a processor's bus structure, word size, and instruction set. This flexibility is important for both performance and cost reasons.

As performance requirements increase, a processor's instruction set and bus structure should be optimized for each application. A processor designed for a high-speed disk controller makes a poor minicomputer or signal processor. In other systems it is important to capitalize on existing software for economic reasons. The flexibility to meet both performance and software requirements is inherent in microprogrammed bipolar LSI systems.

The normal advantages of LSI complexity components are obvious to a digital system designer. These include lower cost, reduced design time, fewer circuit boards and interconnections, smaller system size, reduced power dissipation, etc. However, with high performance circuitry, especially at ECL speeds, LSI becomes important for performance reasons. In larger systems built with MSI and SSI complexity circuits, the time wasted in signal interconnect lines can equal the propagation delays of logic elements. By going to faster logic, a point of diminishing returns is reached where system speed does not improve in proportion to cost due to fixed wiring delays. LSI solves this problem because the system is physically smaller and the number of wiring interconnections is reduced.

The requirement for flexible bipolar LSI led to the introduction of bit slice families in both TTL and ECL technologies. Bit slice circuits are based on taking a microprogrammed processor and dividing it into major sections such as ALU, microprogram control, I/O interface, etc. Each section is further "sliced" into circuits, commonly 4 bits wide, which meets bipolar design limits for die size, power dissipation, and yield.

The M10800 family is today's highest speed standard product LSI family. These circuits combine an advanced bit slice architecture with ECL circuit technology for overall system performance. Processor applications including disk controllers, 32-bit and larger computers, special-purpose signal processors, and high-speed test systems can now take advantage of LSI by selecting and programming the required M10800 circuits.

THE M10800 FAMILY

The M10800 family is a set of circuits which can be interconnected into a high-speed microprogrammed processor system. The present family (see Table 1) includes the basic ALU, microprogram control, timing, and I/O interface functions, plus special-purpose LSI and bus interface circuits. Designed around the bit slice concept, each part type is expandable with parallel circuits to meet system size requirements and each part contains data ports for easy interconnection with other LSI circuits.

Technology developments required to implement the family are based on new circuit design techniques rather than an IC process breakthrough. A major circuit design advancement is the develop-

ment of -2-volt internal MECL logic. Multiplexers, registers, and other commonly used logic elements operate directly from a -2-volt power supply to minimize power dissipation while maintaining logic speed. Other logic functions such as adders can be built more efficiently with series gated MECL structures operated from the conventional MECL -5.2-volt supply. These circuit developments allow the M10800 family to be manufactured on a previously developed LSI process already in production for the high volume MCM10146 1K MECL RAM.

The MC10800 4-Bit ALU Slice initialized the development of standard product MECL LSI. This circuit performs the logic, arithmetic, and shift functions required to execute various machine

TABLE 1

The M10800 family is a series of LSI and bus interface circuits. The parts combine with each other and with fast MECL memories to form a high-speed bipolar LSI processor.

MC10800	—	4-Bit ALU Slice
MC10801	—	Microprogram Control Function
MC10802	—	Timing Function
MC10803	—	Memory Interface Function
MC10804/5	—	MECL/TTL Bidirectional Transceivers
MC10806	—	Dual Access Stack
MC10807	—	5-Bit Bus Transceiver
MC10808	—	Programmable Multi-Bit Shifter

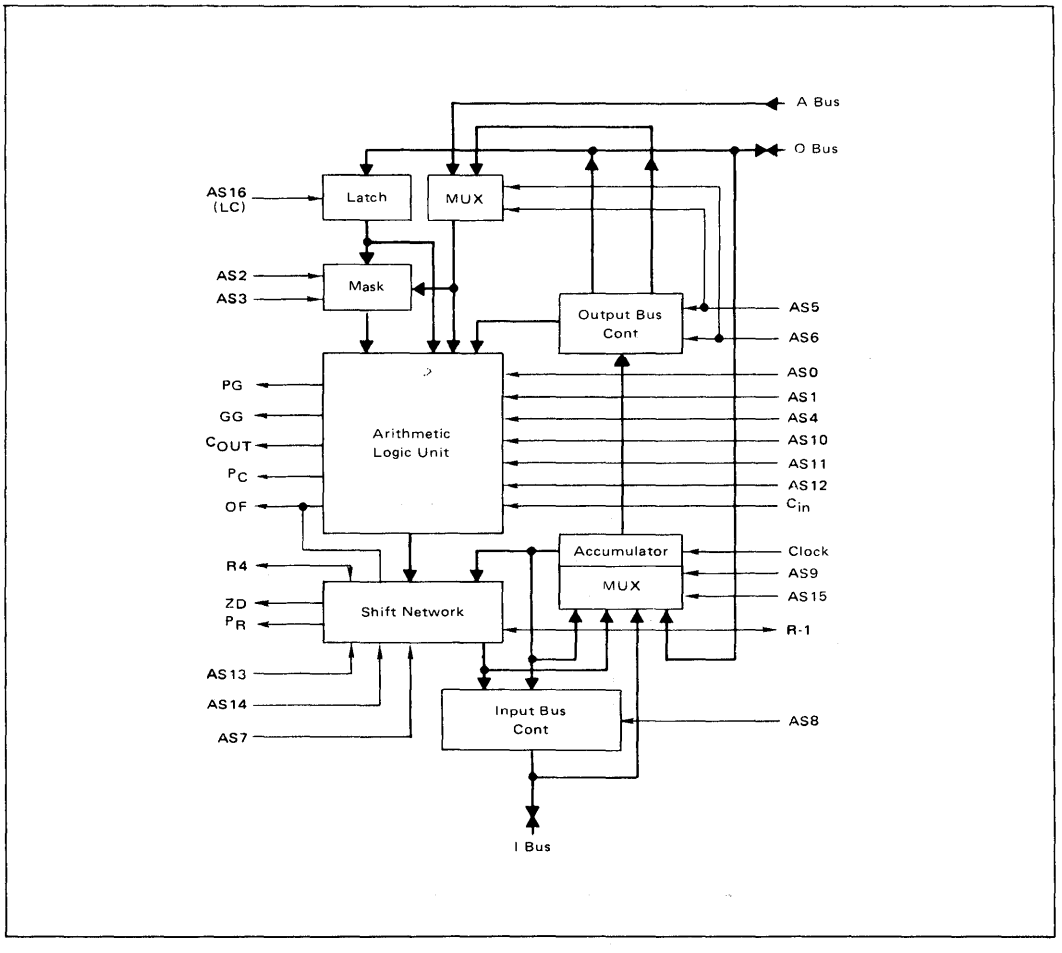


FIGURE 1 — MC10800 4-Bit Slice Block Diagram
The MC10800 4-Bit ALU Slice Block Diagram shows the 3-bus structure with bidirectional buses. A special feature is the ability to handle both binary and BCD data formats.

instructions. Being the first part built with the new -2-volt circuits, logic complexity was held to a conservative 350 equivalent gates. Chip size using standard MECL design rules and double layer metal is less than 15,000 square mils.

The MC10800 is built around three data ports as shown in Figure 1; bidirectional O Bus and I Bus ports, and an input-only A Bus. Seventeen select lines control all circuit functions and determine the source and destination for ALU data. A full set of condition code outputs including output parity is available for branch testing.

Special system-oriented features of the circuit include an ALU that performs binary and BCD arithmetic with equal ease and speed and a shift network that signals overflow when arithmetic shift left results in a sign bit change. The ability to do direct BCD arithmetic is becoming important for some business computers, process controllers, and test systems where human interface is normally in a BCD format.

The MC10801 Microprogram Control Function provides microprogram sequencing control without restricting memory size or organization. High yields on the MC10800 paved the way for a more complex part. The MC10801 has 550 equivalent gates in a 25,000 square mil chip (approximately 1.7 times the MC10800 chip area).

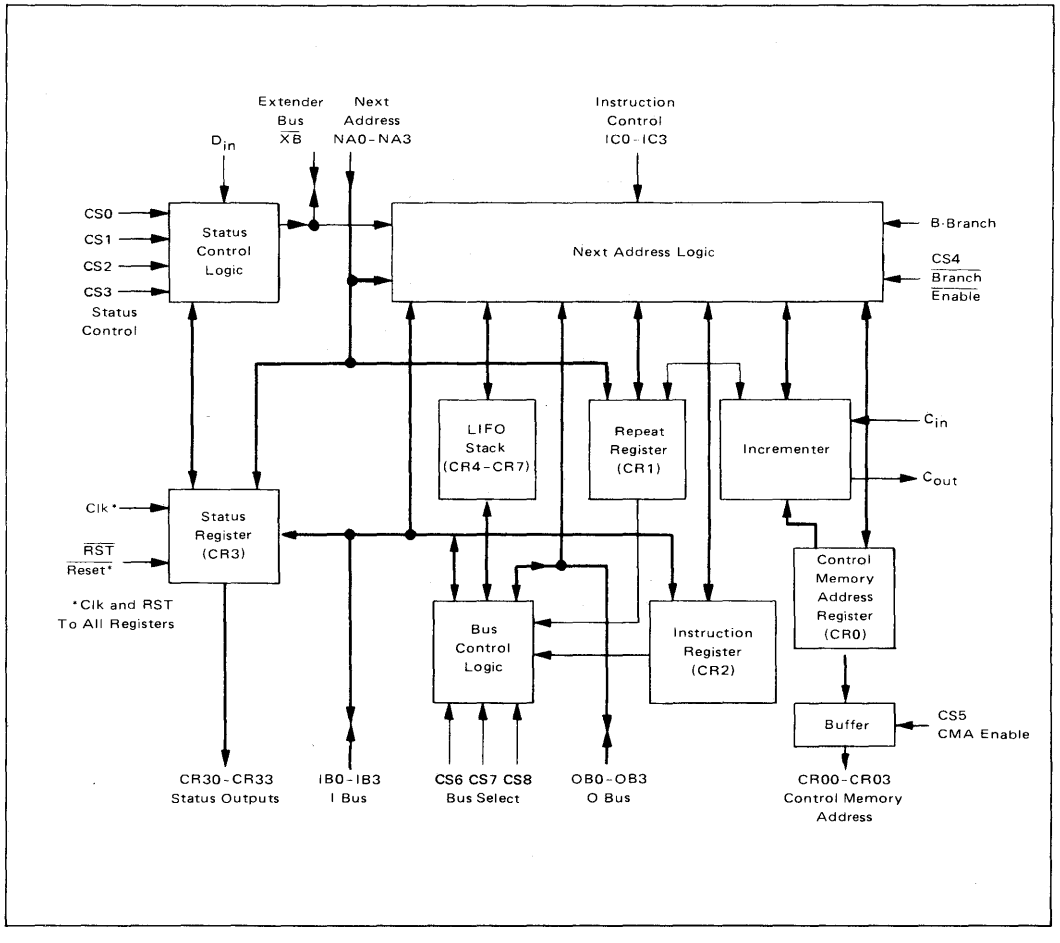


FIGURE 2 — MC10801 Microprogram Control Function Block Diagram

The MC10801 Microprogram Control Function generates the microprogram address and provides the logic for complete sequence control. Five address buses interface the microprogram memory to other LSI parts and to external test points.

The MC10801, also a 4-bit slice part, is organized as shown in Figure 2. Register CR0 holds the microprogram memory address, while the remaining blocks provide logic for sequencing through microprogram. Register CR1 is normally used as a cycle counter for repeat operations, but can also provide a return destination for some microprogram interrupts. CR2 is set up for holding a machine instruction starting address or an interrupt vector.

Status Register CR3 is unique to the MC10801. This register interfaces microprogram control to external test points. For example, it is possible to load individual CR3 bits with status information, then test these bits for conditional microprogram jumps. It is also possible to set or clear CR3 bits under microprogram control to signal processor status. An alternate use for CR3 is the page address in a word/page organized microprogram. CR0 then holds only the microprogram word address.

Registers CR4 through CR7 are connected as a 4-word LIFO stack for nesting subroutines within microprogram. Operation of the LIFO is completely automatic with logic built into the MC10801. If needed, the LIFO can be extended or tested for full stack through the I bus or O Bus ports. Two branch inputs, B and $\overline{XB}$, supply status for conditional microprogram jumps.

The whole part is tied together with 16 instructions built into the Next Address Logic. These instructions, shown in Table 2, control the source for each new microprogram word address and are designed to save both microprogram memory size and microprogram development time. For example, an 8-bit shift in the ALU could be accomplished with two microprogram words — an RSR to load the repeat number (8) into CR1 and an RPI to perform the 8 shifts. System development time is saved by having a set of 16 microprogram sequencing instructions defined and built into the LSI circuit.

TABLE 2

A set of 16 microprogram flow instructions provide a means for sequencing through program. Having these instructions built into the MC10801 simplifies system design and microprogramming.

INC	—	Increment
JMP	—	Jump to NA Inputs
JIB	—	Jump to I Bus
JIN	—	Jump to I Bus and Load CR2
JPI	—	Jump to Primary Instruction (CR2)
JEP	—	Jump to External Port (O Bus)
JL2	—	Jump to NA Inputs and Load CR2
JLA	—	Jump to NA Inputs and Load Address into CR1
JSR	—	Jump to Subroutine
RTN	—	Return from Subroutine
RSR	—	Repeat Subroutine (Load CR1 from NA Inputs)
RPI	—	Repeat Instruction
BRC	—	Branch to NA Inputs on Condition; Otherwise Increment
BSR	—	Branch to Subroutine on Condition; Otherwise Increment
ROC	—	Return from Subroutine on Condition; Otherwise Jump to NA Inputs
BRM	—	Branch and Modify Address with Branch Inputs (Multiway Branch)

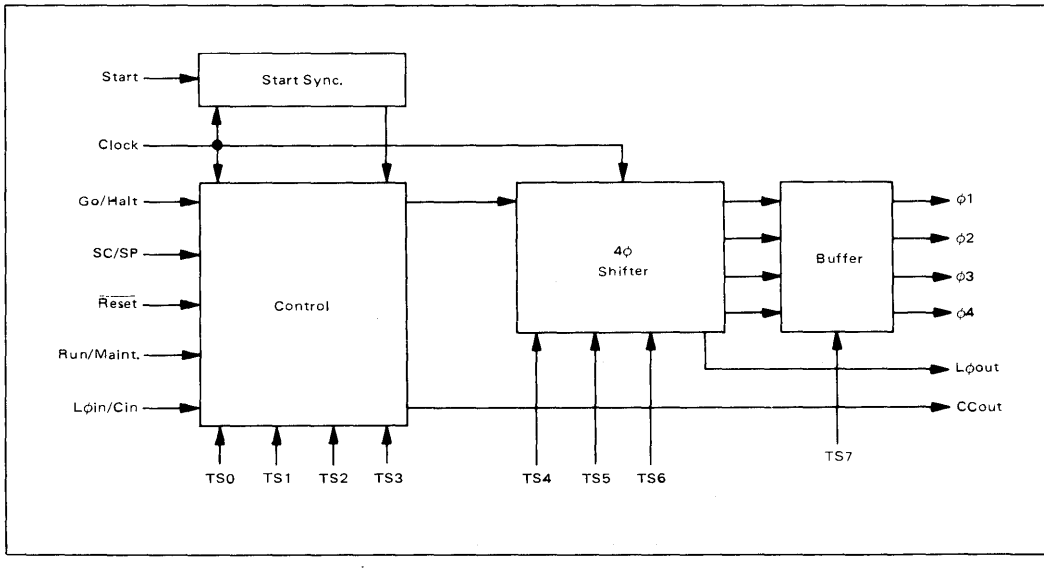


FIGURE 3 — MC10802 Timing Function Block Diagram
The MC10802 Timing Function solves a number of problems common to processor design. These include system start, stop, and clock control for diagnostics. A Start Synchronizer simplifies interface to front panel switches.

The MC10802 Timing Function is unique to the M10800 family. Clock control, often a complex part of processor design, can now be implemented with one LSI circuit. The MC10802 as diagrammed in Figure 3 contains the logic to generate clock phases, simplify system start and stop, and provide some diagnostic capability.

A clock input, normally from a crystal oscillator, is divided into individual clock phases by the 4 ϕ shifter block. The number of clock phases is programmable to two, three, or four phases as required for a particular system. Go/Halt, Run/Maintenance, and Start inputs control system start/stop operations. Single Cycle/Single Phase helps with diagnostics by advancing the system one clock phase or one complete cycle for each start signal input. Interface to the Start input is simplified by a synchronizer network built into the part. Although not as complex as the MC10800 or MC10801, the MC10802 follows the bit slice concept of LSI circuits for major system functions.

The MC10803 Memory Interface Function interfaces the high-speed processor to slower memory and peripherals. Designed for maximum speed, the circuit operates in parallel with other M10800 LSI parts and is able to simultaneously route data and do memory or peripheral addressing. Compared to the MC10801, the MC10803 has 600 equivalent gates in a 21,000 square mil chip. The slightly higher gate count in a smaller area is primarily due to a less complex MC10803 metal pattern.

Also organized as a 4-bit slice, MC10803s are connected in parallel to meet system data and address requirements. Referring to Figure 4, the circuit has Data and Address ports for interfacing to peripheral equipment and the I Bus and O Bus which connect directly to other M10800 parts. A fifth port, the Pointer (P) inputs to the ALU, can be used as a source of address modifiers or constants for memory addressing.

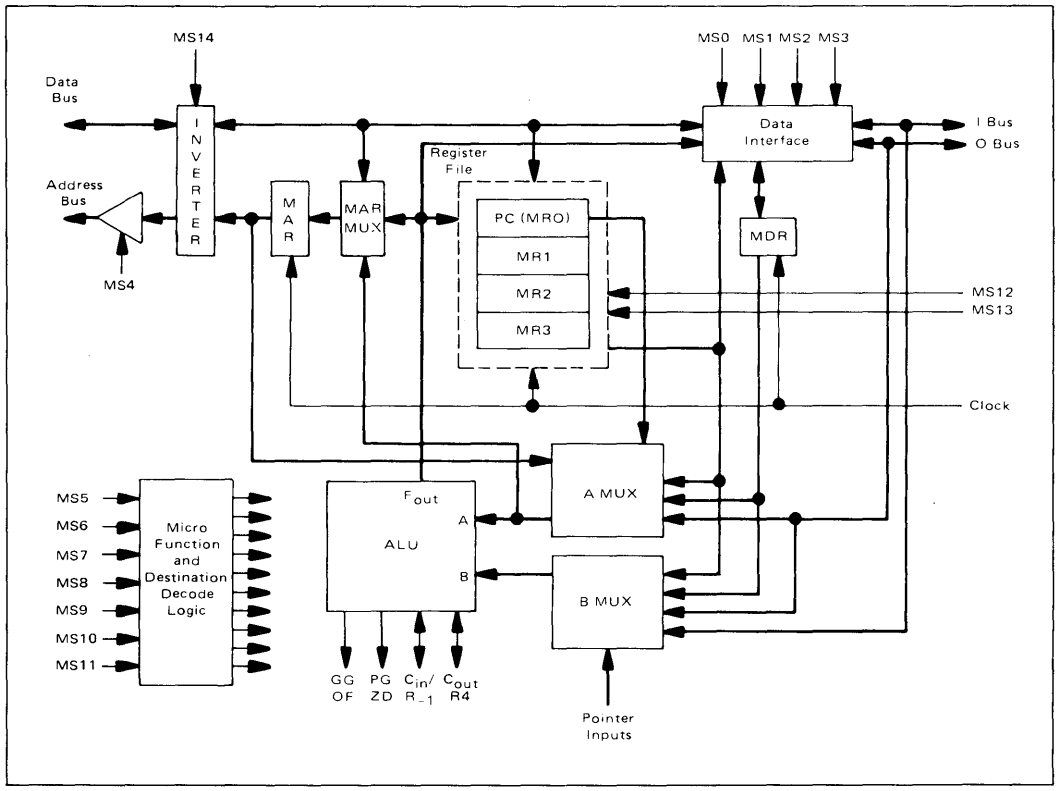


FIGURE 4 — MC10803 Memory Interface Function Block Diagram

The MC10803 Memory Interface Function interfaces to peripheral equipment through Data and Address buses. Separate select lines provide for parallel data transfer and address generation within one microprogram cycle. As with other M10800 family parts, the MC10803 is expandable to meet system size requirements.

A Memory Address Register (MAR) holds the memory address and a Memory Data Register (MDR) buffers incoming or outgoing data. A separate four-word Register File stores information commonly required for memory addressing. Possible uses include program counter, index register, stack pointer, and page addresses.

Select lines to a Data Interface control 17 different data transfer operations between buses and registers. Additional select lines control the ALU function, data source, and destination through Microfunction and Destination Decode Logic. The ALU, normally used for memory addressing, performs seven basic functions (add, subtract, OR, AND, exclusive OR, shift left, and shift right) on a wide range of data sources.

The MC10803 is not limited to memory interfacing operations. A peripheral controller, for example, normally transfers and formats data, requiring little arithmetic capability. These systems can use the MC10803 for both I/O and ALU, reducing parts count and still maintaining system speed.

THE PARTS TIE TOGETHER IN A SYSTEM

Bus ports on the MC10800, MC10801, and MC10803 directly interconnect with each other when building a processor system. Although structures vary with different applications, the 16-bit processor (Figure 5) will illustrate several key system features. This combination of LSI circuits and bus structure could be used for a general-purpose minicomputer or signal processor.

The MC10801 Microprogram Control Function supplies an address to microprogram memory, selecting one microprogram word. Each microprogram word is divided into groups of bits called fields and each field, represented by the wide arrows in Figure 5, independently controls a system section. Since all fields are present at the same time, the various system sections can operate simultaneously for best system speed.

A system function performed by all the fields in one microprogram word is called a microinstruction. Several microinstructions may be required for one

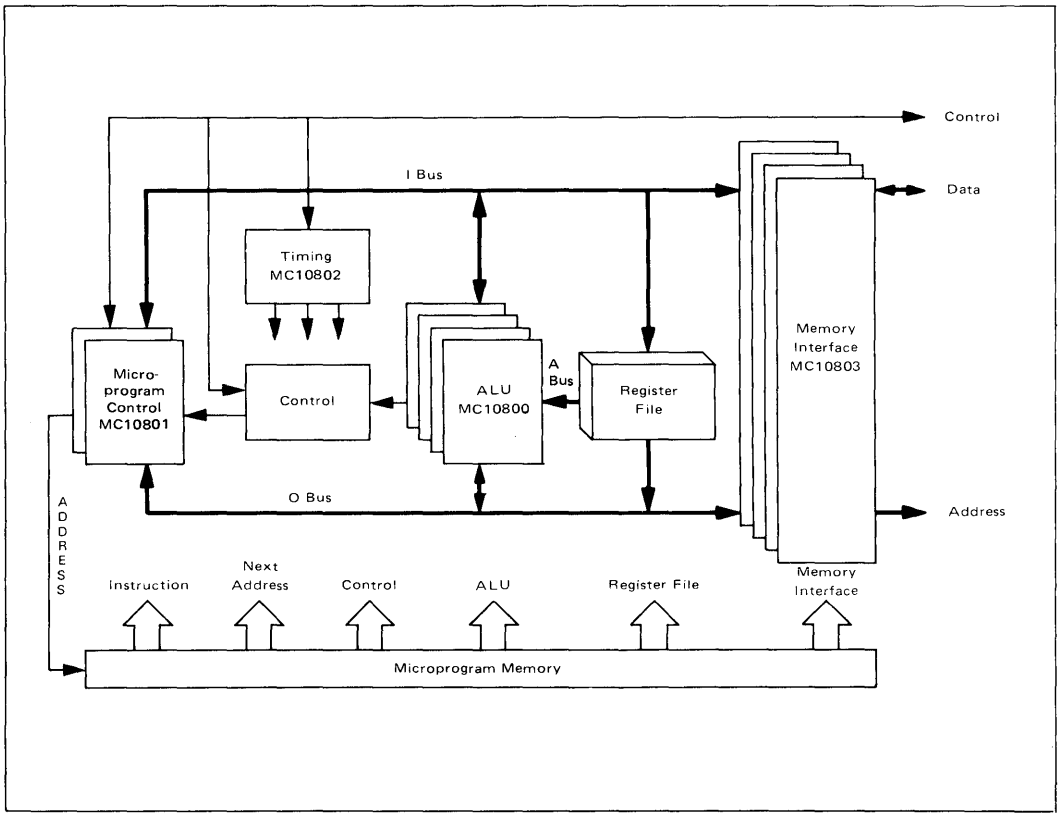


FIGURE 5
M10800 family circuits bus together into a high-speed processor system. This design uses 11 LSI parts plus MECL 10,000 MSI and memories for a 16-bit minicomputer or signal processor.

machine instruction. System performance, therefore, is determined by the number of microinstructions in a system instruction and the speed of each microinstruction. Microinstruction cycle time for a 16-bit M10800 family based system would be around 100 ns.

Figure 5's system operation can be explained by the relationship of microprogram fields to the LSI blocks. Two fields controlling the MC10801 generate each new microprogram address. An Instruction field selects one of the 16 program flow instructions given in Table 2. Once selected, all logic needed to execute the instruction is contained in the MC10801. However, some instructions require additional information. For example, a JMP — Jump to Next Address or JSR — Jump to Subroutine require a jump destination which is supplied by the Next Address microprogram field. An important feature of the MC10801 is the ability to route Next Address data through the O Bus port for ALU or Memory Interface constants, bit mask patterns, and offsets when the field is not required for microprogram flow.

Branch control is a third field associated with microprogram addressing. Most programs have to make a large number of flow decisions either from ALU condition codes such as zero detect, overflow, sign bit, etc., or from external test points. These status signals are multiplexed into the MC10801 branch inputs through control logic under command of the control field. Branch instructions built into the MC10801 include BRC — Branch on Condition, BSR — Branch to Subroutine, and BRM — Branch and Modify.

The MC10800 performs arithmetic, logic, and shift operations on data within the ALU, Register File, and/or Memory Interface. The bus structure in Figure 5 also allows the ALU to generate microprogram addresses through the I Bus, if required. The ALU as shown will operate in either binary or BCD data formats as controlled by the ALU microprogram field.

Unlike most other bipolar LSI families, M10800 leaves Register File as a separate block. This allows register file expansion to any size or organization. More important is the ability of the ALU and Memory Interface circuits to share Register File without tieing up each other. Possible circuits for the Register File block include MCM10145 16 x 4 RAMs and the MC10806 Dual Address Stack.

The MC10803 interfaces to peripheral equipment through Data and Address ports. I/O information can be routed directly to or from the required internal processor circuits via the I Bus and O Bus. The MC10803's ability to transfer data and generate memory addresses independent of ALU operation is an architectural strength of the M10800 family. When not used for I/O, the MC10803 internal ALU can be connected in parallel with the main ALU for double precision arithmetic.

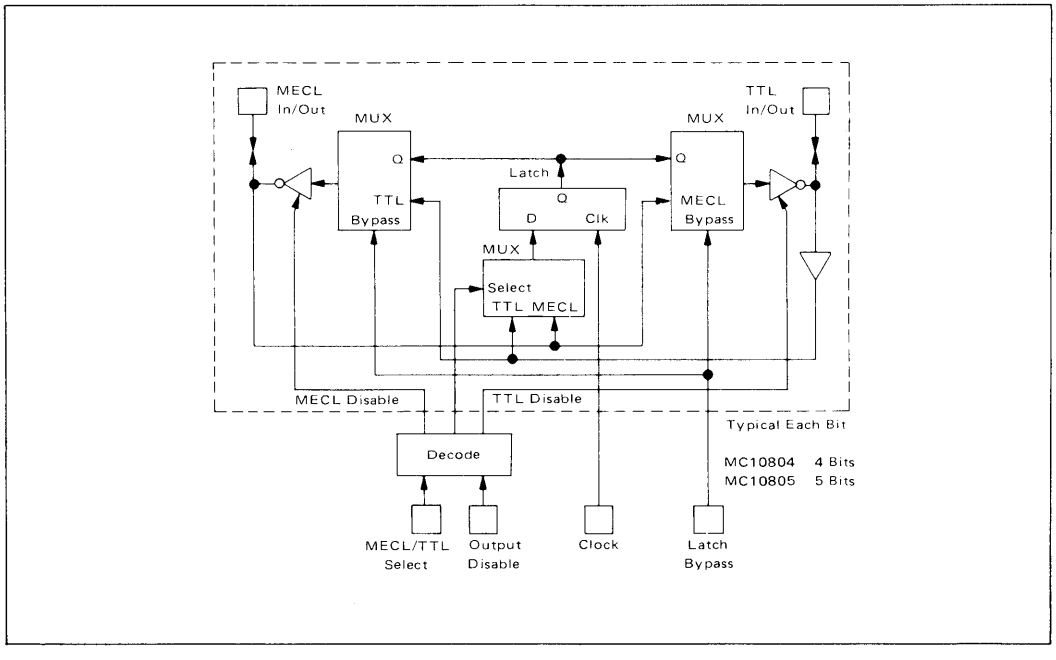


FIGURE 6 — MC10804/MC10805 Block Diagram
The MC10804/5 MECL/TTL Bidirectional Transceivers simplify the interface to TTL peripherals. An internal latch can be used to compensate for a MECL bus which may be much faster than the TTL side.

MORE M10800 FAMILY CIRCUITS

The preceding circuit descriptions covered the main components required for processor design. However, bus interface parts and special-purpose LSI circuits are needed to solve additional system problems. The MC10804 through MC10808 fall into these categories.

The MC10804 and MC10805 are bidirectional ECL/TTL bus transceivers. Many high-speed ECL processors interface to existing TTL compatible peripherals. MECL 10,000 translators such as the MC10124 and MC10125 handle this interface on address and control lines. Now the MC10804/5 completes the interface with translation on bidirectional data buses.

The MC10804 is a 4-bit part in a 16-pin package and the MC10805 is 5 bits in a 20-pin package. The combination of 4 and 5 bits permit efficient translation of 9-bit data bytes. Figure 6 shows the logic configuration of one bit in either part type.

A MECL/TTL select line controls the direction of data through the circuit. This combines with an Output Disable to force the TTL side to a three-state mode and MECL to a busable VOL. An internal latch holds data in either direction. The Latch Bypass input routes data around the latch for faster translation time or to transfer data while holding information in the latch. The MC10805 is also designed to drive a heavy capacitive load, allowing the circuit to interface directly with MOS main memory for good speed and minimum part count.

The MC10807 5-Bit Transceiver followed as a result of inputs to do a MECL circuit with MC10805 functionality, but without TTL translators. This circuit as shown in Figure 7 is identical to the MC10805, but has MECL signals on both ports. The buffered bidirectional MECL driver/receivers allow complex MECL bus networks to maintain a full transmission line environment.

The MC10806 Dual Access Stack represents a significant jump in standard product MECL LSI. Although equivalent gate count does not directly equate on a memory type part, circuit complexity can be judged by the large 35,500 square mil chip area. Knowledge gained during M10800 family development has allowed circuit complexities to increase such that the MC10806 is almost 2.4 times larger than the MC10800.

The MC10806 is primarily intended as a data buffer between a high-speed MECL processor and slower peripherals. However, a versatile dual read/write bus structure also allows the circuit to function in a LIFO or FIFO stack, or in an M10800 system register file. The MC10806 has two bidirectional data buses, A Data Bus and B Data Bus, each having access to a 32 × 9 memory as shown in Figure 8. Output register latches in series with both data buses give the circuit a master-slave appearance where the memory cells are master stages and the latches are slaves.

A and B Address inputs each select a memory word for the corresponding A and B Data Buses.

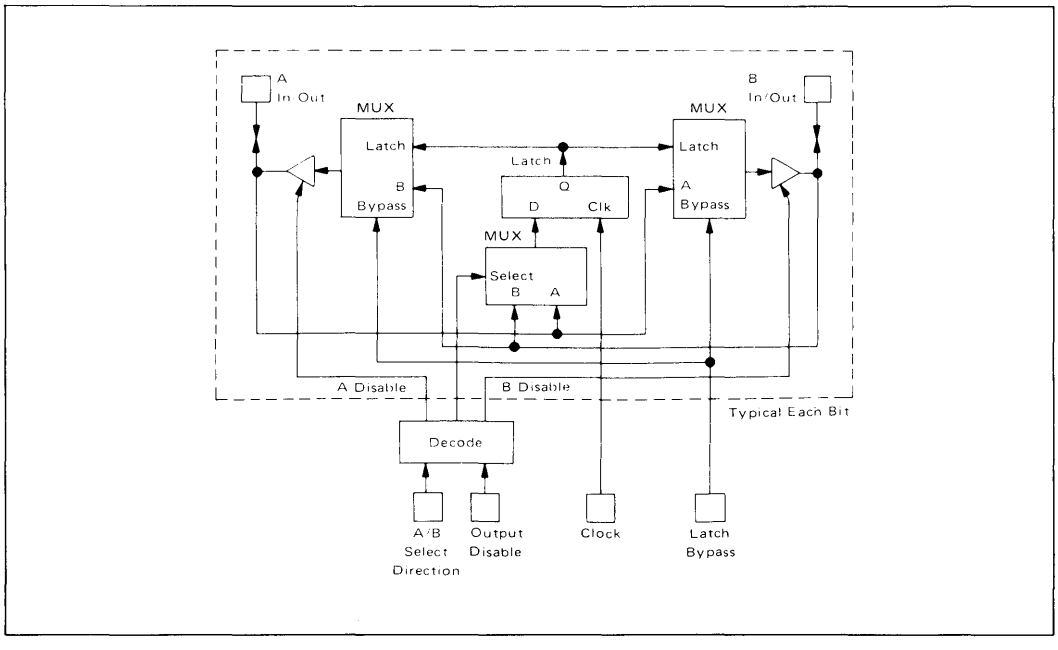


FIGURE 7 — MC10807 Block Diagram
The MC10807 5-Bit Transceiver sends MECL bus signals in both directions. A transceiver in one part reduces fanout and package count over separate driver and receiver circuits.

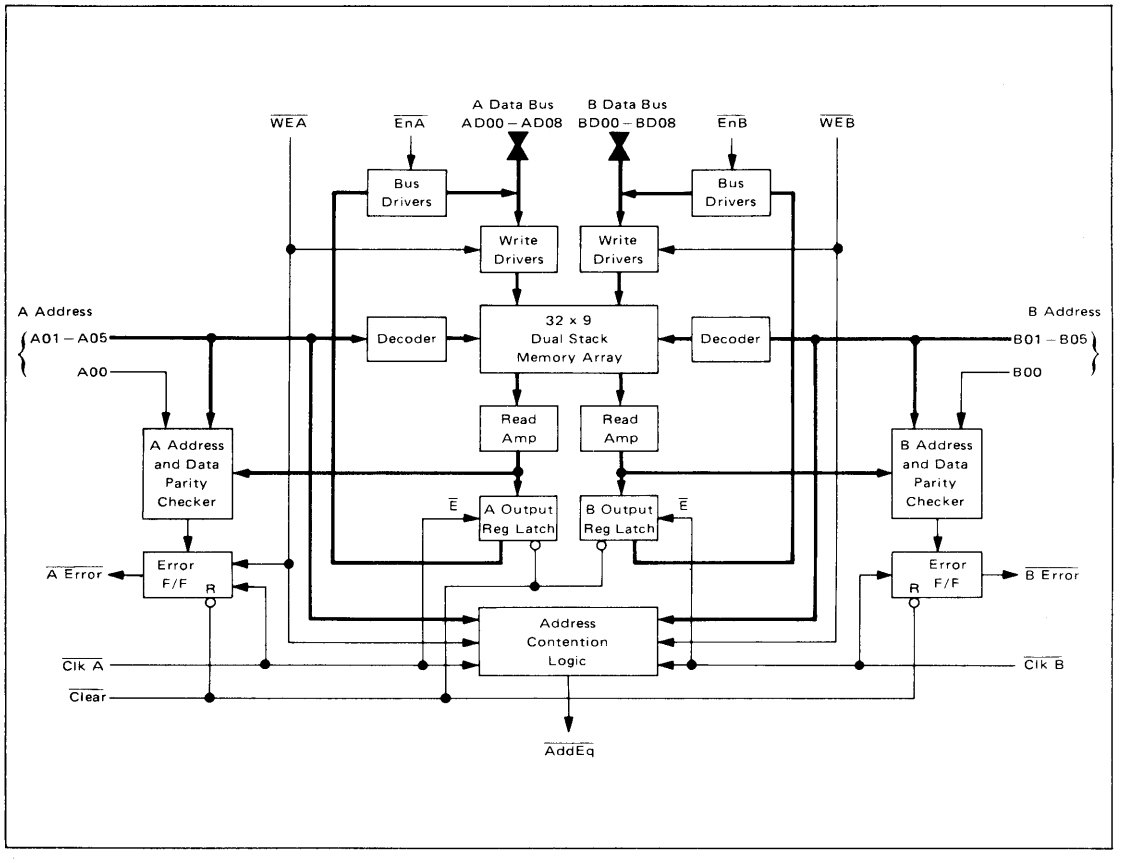


FIGURE 8 — MC10806 Dual Access Stack Block Diagram

The MC10806 Dual Access Stack is a 32 x 9 memory array with two independent read/write data and address ports. The dual port structure combines with optional internal parity checking to solve many buffer memory design problems.

Separate clocks, write enables, and data enables control read/write operations for each side. Parity checking is automatic on the 9-bit data word and optional on the address inputs. When parity is used, write is prohibited on any address with incorrect parity. Parity can be bypassed for systems not requiring this feature.

The flexibility of being able to write from both data ports can lead to priority problems. For example, writing different data on the A and B Data Buses into the same word address causes loss of one or both data words. Within the MC10806, Address Contention Logic looks at write enables and addresses to detect and signal address conflicts.

The MC10808 Programmable Multi-Bit Shifter is another example of using standard LSI to solve a system problem. ALU circuits shift data only one or two bits per microinstruction. This becomes time-consuming when data must be shifted many places for formatting, bit testing, or normalizing floating point numbers. The MC10808 shifts data any number of bits in one 10 ns pass.

Each circuit is a 16-bit shifter organized as shown in Figure 9. The algorithm used combines with the MECL wired-OR for unlimited expansion — 4 parts for a 32-bit shifter, 16 parts for a 64-bit shifter, etc. Circuit expansion is in a horizontal manner so only one part delay is required regardless of shifter size.

The number of bits shifted is programmed on Scale Factor inputs. Shift Type inputs select one of eight possible shift patterns or output controls as shown in Table 3. SRC and SLC permit programming the scale factor as a two's complement number, controlling both direction and distance. A Sign Bit input controls sign bit polarity and allows the circuit to operate in either positive or negative logic formats.

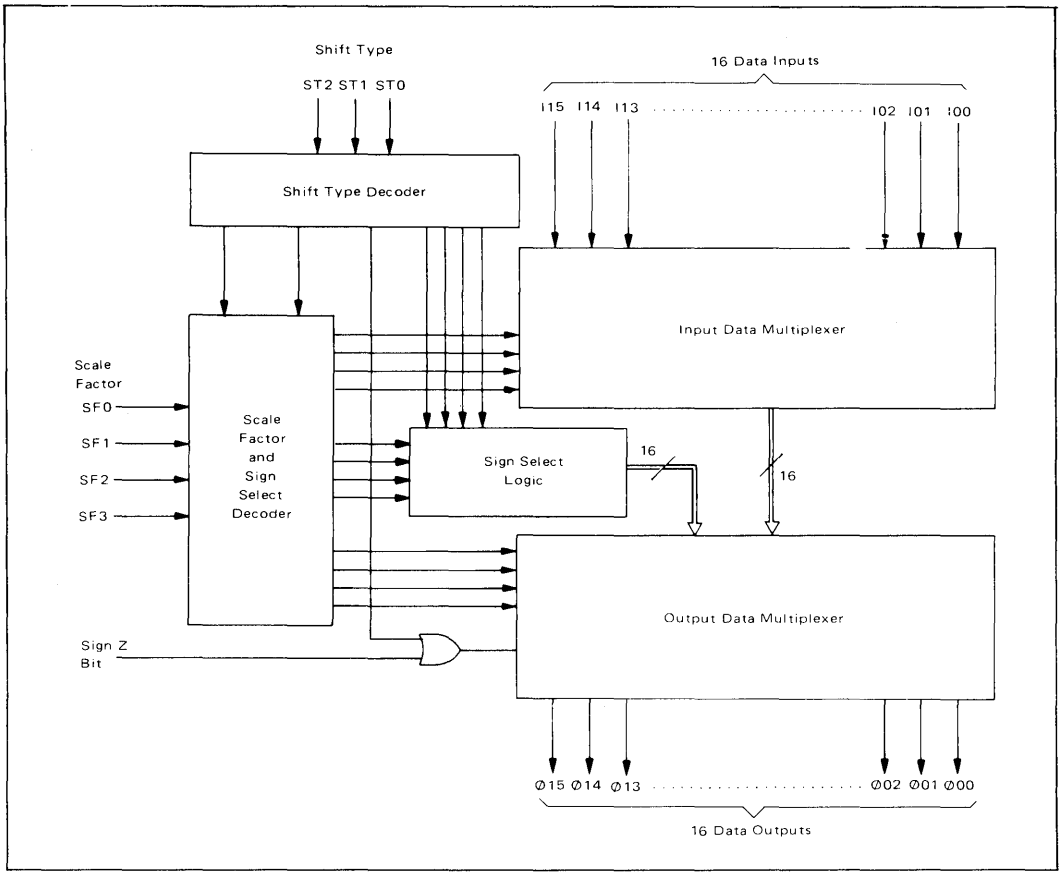


FIGURE 9 — MC10808 Functional Block Diagram
The MC10808 Programmable Multi-Bit Shifter shifts 16 input bits 0 to 15 places left, right, or rotate. The circuit is fully expandable to larger word sizes without loss of speed.

TABLE 3

The MC10808 has an instruction set of eight shift and output commands. Both linear and rotate shifts are covered with sign polarity control on linear shifts.

ALS	—	Arithmetic Shift Left
ARS	—	Arithmetic Shift Right
RLT	—	Rotate Left
RRT	—	Rotate Right
SRC	—	Shift Right — 2's Complement
SLC	—	Shift Left — 2's Complement
ODA	—	Output Disable
SBO	—	Sign Bit at All Outputs

A HIGHER PERFORMANCE M10800 FAMILY PROCESSOR

With additional M10800 functions, the Figure 5 processor can be redrawn into a higher performance system as shown in Figure 10. Translators at interface points give the processor TTL-compatible I/O. An MC10806 data buffer holds 32 data words allowing the TTL bus to be slower than the MECL system microinstruction cycle time. The MC10806 dual bus structure easily adapts to the bidirectional data bus so both incoming and outgoing data can be stored.

Data Bus following the MC10806 buffer is routed directly to Microprogram Control. Compared to Figure 5 this bus structure saves instruction execution time since a starting address need not go through Memory Interface, but the ALU no longer has a direct path to Microprogram Control.

The system also uses an MC10806 for Register File. The first half of a microinstruction reads

Register File via the O Bus, then the second microinstruction half routes ALU results to Memory Interface or back to Register File with the I Bus. O Bus latch internal to the MC10800 4-bit ALU Slice holds the O Bus input during the second microinstruction half to eliminate race conditions within the ALU. The other Register File port routes data through the Shifter to ALU A Bus, to Memory Interface, or to Microprogram Control.

The MC 10808 Shifter is placed in front of the ALU for single pass shift and test. Data shifting through the part only takes about 10 ns so this series arrangement has little effect on microinstruction cycle time. The same microprogram ALU field can control both the MC10808 and MC10800 for a very powerful ALU function set.

A Pipeline Register is placed between microprogram memory and the data handling LSI circuits to reduce microinstruction cycle time. This register permits parallel operation between Microprogram Control and the rest of the processor. While the ALU, Register File, and Memory Interface are executing one microinstruction, the MC10801 is generating a new microprogram memory address. Pipelining is optional in an M10800 family system and the MC10801 interfaces directly to microprogram in either case.

A final feature of the Figure 10 system is the use of Branch, ALU, and Interface decoding logic. These blocks allow a relatively wide Pipeline Register feeding a large number of LSI control inputs to be driven from a narrow microprogram word. For example, a 6-bit microprogram field can select 1 of 64 ALU instructions. However, the ALU logic may require 12 to 20 control inputs. This fanout is performed in decode logic commonly built with fast MCM10139 PROMs. In addition to reducing microprogram size for cost reasons, decoding logic allows microprogram fields to be structured for easier programming. The decoding logic does not slow system performance since it is possible to go from clock to MC10801 address out through microprogram RAM or PROM and decoding logic to Pipeline Register within one microinstruction cycle time.

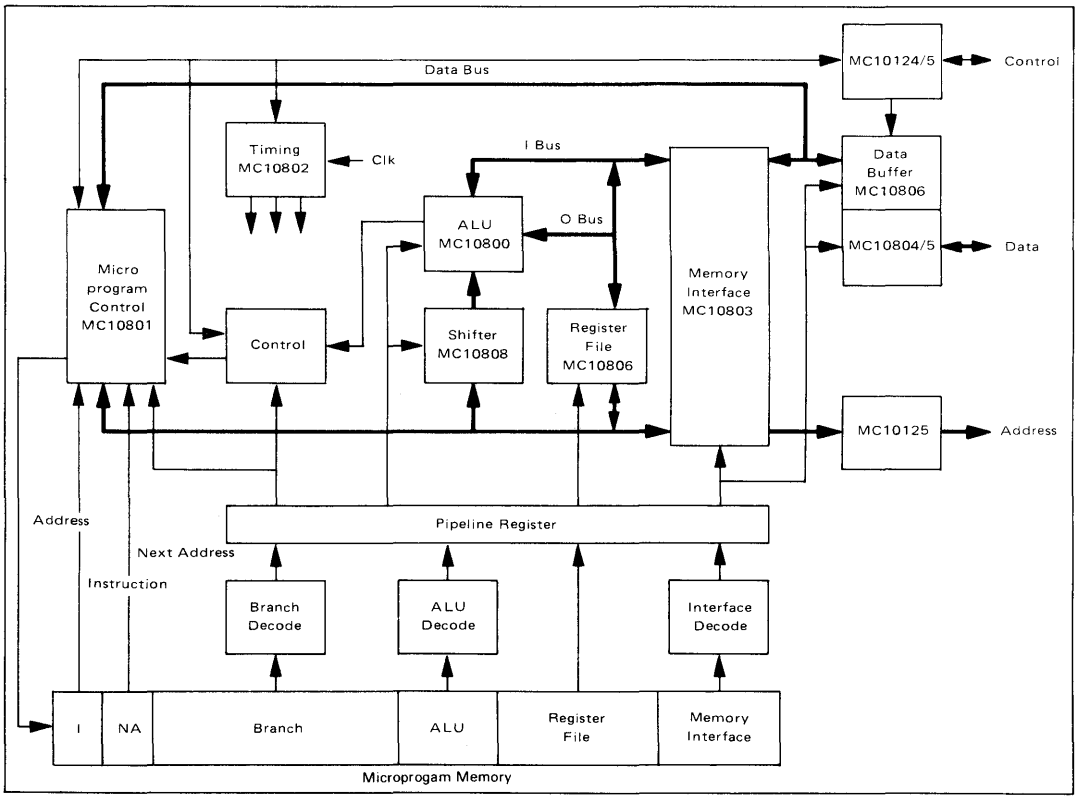


FIGURE 10 — Higher Performance M10800 Processor
This M10800 family based processor design has the MC10808 in series with the MC10800 for greater arithmetic power and the MC10806 with TTL translators for a more flexible I/O interface. Other features include a pipeline register to reduce microinstruction cycle time and microprogram field decoding to reduce microprogram word length.

HIGH RESOLUTION WAVEFORMS RESULT WHEN A VERY HIGH SPEED D/A CONVERTER GETS DRIVEN BY A MICROPROGRAMMED ECL PROCESSOR

Many high-speed digital systems must eventually supply an analog output. This is especially true of test equipment and communications systems doing digital filtering or signal processing. D/A converters are readily available for systems operating at microprocessor performance levels, but engineers requiring the performance of higher speed bipolar TTL or ECL based processors face an expensive or complex transfer to analog signals.

The MC10318, see Figure 1, sets a new standard for high-performance D/A conversion. The part accepts an 8-bit ECL 10K compatible binary data word input and generates current source analog outputs accurate to ±½LSB. A 10 ns combined conversion and settling time outperforms the fastest digital processor systems.

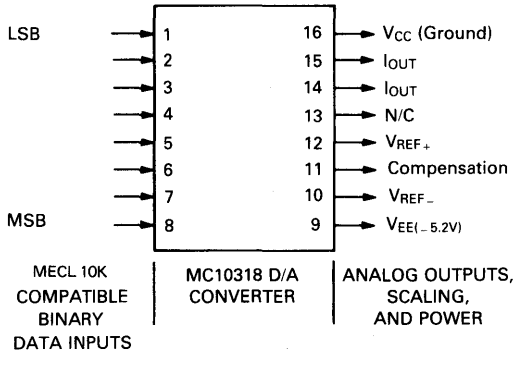


FIGURE 1
The MC10318 converts 8-bits of binary data to true and complement analog current source outputs. A fast 10ns conversion time results from innovative circuit design and high-speed ECL processing.

This article describes the MC10318 D/A converter, then connects it to a microprogrammed processor built with the M10800 LSI bit slice family. Waveform examples show the MC10318 performance characteristics and the flexibility inherent in a processor controlled analog output.

A NEW HIGH-SPEED D/A CONVERTER

Circuit speed is the result of emitter coupled differential amplifiers, a high-speed current summing conversion technique, and ECL (emitter coupled logic) integrated circuit processing technology. Figure 2 provides additional information on current summing as used with the MC10318, ECL 10K compatible signals on the 8 inputs (MSB-LSB) have a logic "1" of -0.9 volts referenced from ground and a logic "0" of −1.7 volts. The input signals are measured against an internally generated V_{BB} source of about −1.3 volts.

Collector outputs of the input differential amplifiers are buffered and translated downward to current summing differential amplifiers. Precision constant current sources in the respective current summing amplifiers are weighted according to bit value with MSB having 128 times more current than LSB. Reference inputs to the constant current sources are used for calibration and to establish full-scale current levels. Full-scale current is approximately 15.9 times the reference input current. (3.1 mA for a full-scale 50 mA output.)

Getting further into the circuit, logic "1" levels on all data inputs cause the associated Q1 transistors to conduct, cutting off Q2. This in turn causes Q4 to conduct cutting off Q3. Maximum output current is pulled from I_{out} while $\overline{I_{out}}$ is essentially floating. Logic "0" on all data inputs reverses the process, pulling maximum

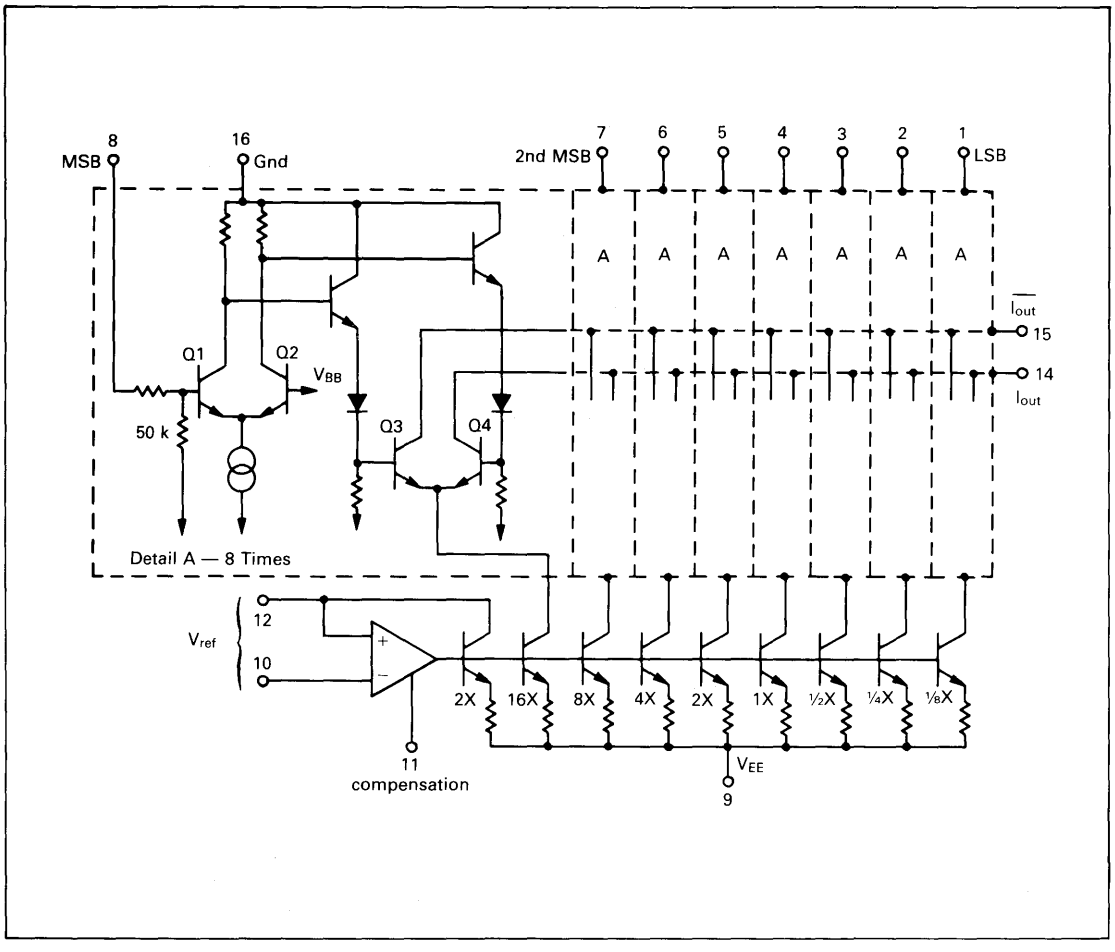


FIGURE 2
Each bit moving upward from LSB controls twice the output current of the preceding bit. The 8-bit binary word pattern selects one of 256 current values between zero and I max for either analog output.

output current from $\overline{I_{out}}$. A combination of logic "1" and logic "0" inputs splits the current between both outputs proportional to bit weight. The total of both outputs is always equal to maximum output current. Constant current sources in the input differential amplifiers and current summing amplifiers give the circuit a constant power level, independent of input and output signals, for minimum noise generation and fast settling times.

CONNECT IT TO A MICROPROGRAMMED PROCESSOR

The microprogrammed processor used to drive the D/A converter is diagrammed in Figure 3. Microprogram memory addressing, in a word/page format, is handled by the MC10801 Microprogram Control Function. Feedback from microprogram instructs the MC10801 how to sequence through program. Common instructions include Increment, Direct Jump, Conditional Jump, Jump to Subroutine, etc.

Next Address (NA) inputs normally supply jump destinations for microprogram memory flow patterns. More important to the problem of generating analog waveforms is the MC10801's ability to transfer the NA information to the ALU and Data outputs. This allows lookup tables to be placed in microprogram for maximum speed when generating random wave patterns.

ALU and I/O operations are handled by MC10803 Memory Interface circuits. Advantages of the MC10803 are a strong I/O interface at the expense of some arithmetic power. Four internal MC10803 accumulators and a 16 word register file store ALU operands, addresses, and data constants. A pipeline register built from

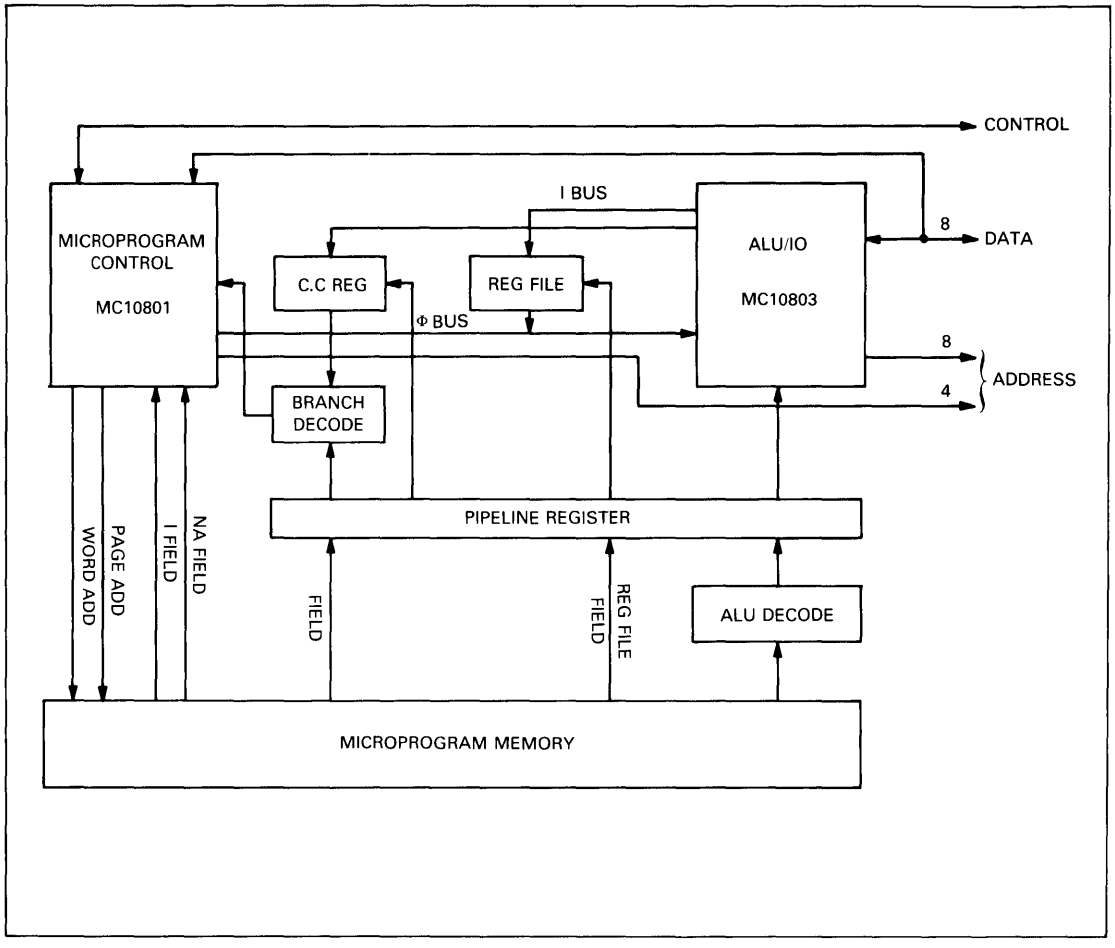


FIGURE 3
PROCESSOR BLOCK DIAGRAM

MC10176 hex flip flops holds microprogram information so the MC10801 can generate a new microprogram address in parallel with the MC10803 executing a microinstruction. The overlap of addressing and execution permits a fast 100 ns worst case microinstruction cycle time.

Detailed information on microprogrammed processor design is outside the scope of this article and not directly relevant to the D/A converter interface. The processor's main feature is its ability to update the MC10318 every 100 ns either from a lookup table or with simple ALU calculations. A 100 ns data input is 30 to 60 times faster than a MOS microprocessor doing the same job.

Address, Data, and Control lines from the processor easily interface to the D/A as shown in Figure 4. Address decode selects the converter as an output peripheral. A proper address enables the system clock which transfers data bus information to an 8-bit holding register. Outputs from the holding register go directly to the MC10318 which converts the binary information to an analog current level. Holding register outputs remain constant unless the proper address is present.

The MC10318 adapts to a wide range of output voltage levels between -1.3 and $+2.5$ volts, and output currents up to 51 mA. A 200 ohm resistor to $+5$ volts and 50 ohm resistor to ground on each output in Figure 4 give an analog output voltage range of $+1$ to -1 volt with a full-scale output current of 50 mA. Accuracy is maintained by the MC1503U, a temperature compensated/voltage regulated 2.5 volt source, on the reference input. Setting the 500 ohm potentiometer provides final full-scale calibration for the 50 mA output level. A special feature of the 50 ohm to ground output resistor is the ability to substitute a properly terminated 50 ohm coaxial cable and transmit the analog output a reasonable distance without special buffers or drivers.

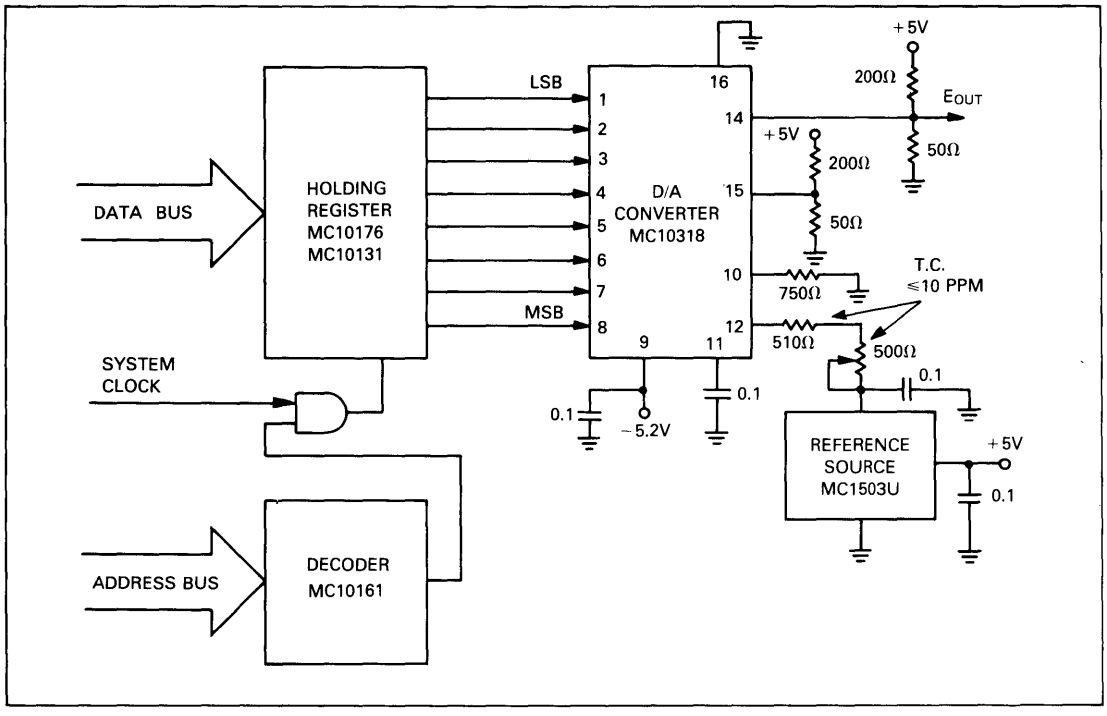


FIGURE 4

The MC10318 interfaces to the ECL processor I/O with minimum buffering and decoding logic. D/A interface to TTL signals requires adding MC10124 translators

THE PROCESSOR ALLOWS UNLIMITED WAVEFORMS

A lookup table in microprogram memory is the most direct way to use the processor. Any waveform mapped on the Figure 5 grid can be duplicated at the analog output. 8-bits give the converter 256 distinct voltage levels (00-FF_H) from −1.0 volt to +1.0 volt. The horizontal grid in 100 ns increments is the top processor cycle time. Since the processor is built with static bipolar circuits, system clock can be varied from DC to 10 MHz for additional output frequency control.

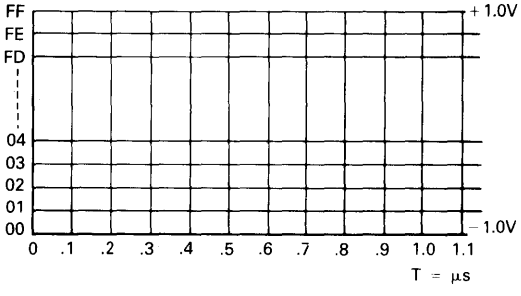


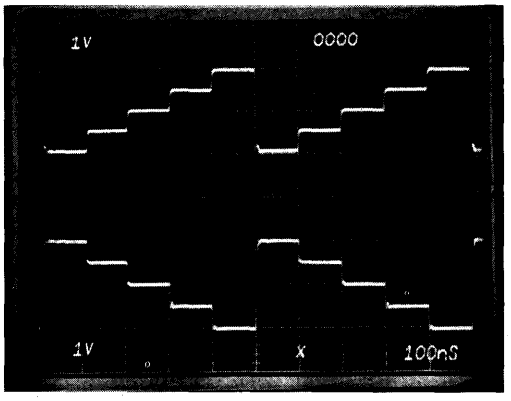
FIGURE 5

The processor generated analog output can follow any waveshape drawn on the 256 line by 100 ns grid. Programming the proper 00-FF_H code selects one of 256 distinct voltage levels.

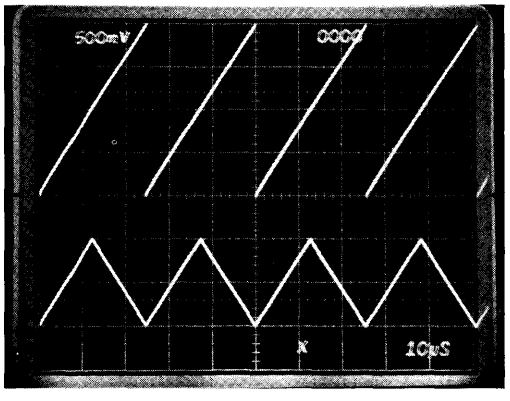
The first example, Figure 6A, shows the true (upper trace) and complement (lower trace) analog outputs from a simple five-level stairstep program. Using a lookup table for voltage levels, the program as shown below requires 6 microprogram words each equating to a 100 ns microinstruction command. The WORD column is a relative microprogram word address, FLOW describes the program sequence pattern (increment and direct jump in this example), and FUNCTION is the actual microinstruction assignment. Program flow keeps the processor in a continuous loop between words 2 through 6.

WORD	FLOW	FUNCTION
1	INC	Set D/A Address
2	INC	00_H to Data (-1.000 V_{out})
3	INC	40_H to Data (-0.498 V_{out})
4	INC	80_H to Data ($+0.004$ V_{out})
5	INC	BF_H to Data ($+0.498$ V_{out})
6	JMP 2	FF_H to Data ($+1.000$ V_{out})

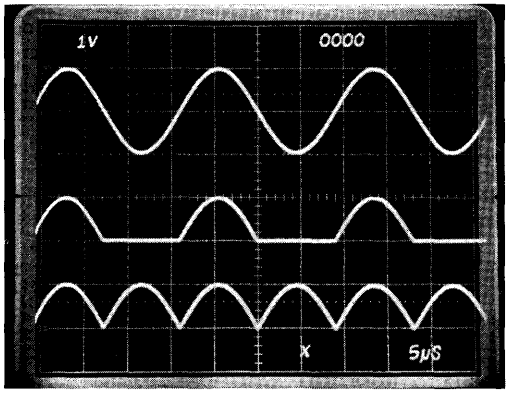
Figure 6A also illustrates the very fast MC10318 conversion time and edge speeds. Changes in the analog output are a small percent of the 100 ns per division oscilloscope trace.



6A



6B



6C

FIGURE 6
Various analog signal patterns illustrate processor microprogramming techniques.

The processor ALU can calculate simple patterns to reduce program space otherwise required for a lookup table. Figure 6B shows two ramp patterns based on incrementing or decrementing the data bus every microinstruction. Upper trace is a 256 step ramp requiring 25.6 µs per cycle. Microprogram is as follows:

WORD	FLOW	FUNCTION
1	INC	Set D/A Address
2	JMP 2	Increment Data Bus

The lower Figure 6B waveform uses more processor features to control end limits and the number of repetitive steps in a cycle. Word 2 in the program below establishes the signal starting point at hexidecimal 40(−0.498 volts). In addition to incrementing the Data Bus, word 3 sets a program cycle counter internal to the MC10801 for 126 repeats. Word 4 is a repeat command which increments the Data Bus 126 times then automatically moves on to word 5. Words 5 and 6 are similar to 3 and 4 except the Data Bus is decremented. Repeat count is one less at 125 to compensate for the extra microinstruction at word 2.

WORD	FLOW	FUNCTION
1	INC	Set D/A Address
2	INC	40_H to Data Bus
3	INC, CC = 126	Increment Data Bus
4	Repeat/INC	Increment Data Bus
5	INC, CC = 125	Decrement Data Bus
6	Repeat/JMP 2	Decrement Data Bus

Performance advantages of microprogrammed bipolar LSI processors over MOS microprocessors become more apparent when the program must keep track of program cycle counts as in the preceding example. The processor executes MC10801 repeat instructions in parallel with MC10803 increment or decrement commands, maintaining a 100 ns D/A update interval. MOS microprocessors handle the cycle count in series with output results and would be 60 to 120 times slower than the ECL processor used here.

The third example, Figure 6C, illustrates three waveforms generated with lookup table subroutines. One subroutine, SINPOS, starts at the mid point (0 volts) and generates the first 180° of a sine wave in 3 degree increments. SINNEG, a second subroutine, provided the second sine wave half. The following program uses the subroutines to generate a sine wave, half-wave rectified signal, and full-wave rectified output. With a little care the program can be written to supply proper output data every microinstruction, even while jumping to and from subroutines.

WORD	FLOW	FUNCTION
1	INC	Set D/A Address
2	JSR SINPOS	80_H to Data Bus
3	JSR SINNEG	80_H to Data Bus
4	JMP 2	79_H to Data Bus
5	INC	Set D/A Address
6	JSR SINPOS	80_H to Data Bus
7	INC, CC = 58	80_H to Data Bus
8	REPEAT/JMP 6	80_H to Data Bus
9	INC	Set D/A Address
10	JSR SINPOS + 1	86_H to Data Bus
11	JMP 10	80_H to Data Bus

Figure 7 further demonstrates programming flexibility by combining some of the Figure 6 programs into a unique output pulse pattern. More important, the Figure 6 and 7 examples illustrate a capability that can be used by design engineers in signal processors, test equipment and research projects to generate unlimited signal patterns. Although lower-speed microprocessors and D/A converters preform similar functions, the quantum performance jump offered by the MC10318 D/A and M10800 ECL LSI processor family opens up new application areas for digitally generated analog signals.

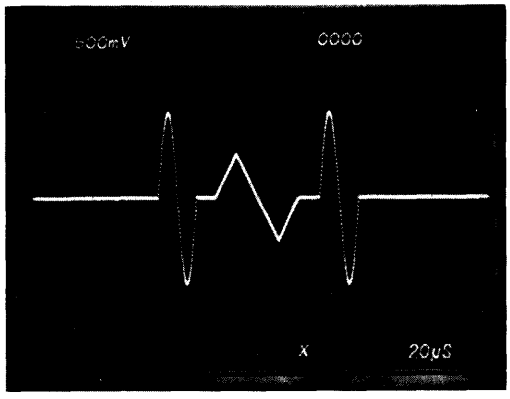


FIGURE 7
The flexibility of processor generated analog signals becomes more apparent when different programs are combined into a unique pulse pattern.

ARRAY-BASED LOGIC BOOSTS SYSTEM PERFORMANCE

Using ECL arrays to build standard logic blocks increases gate speeds by more than a factor of four and offers 100 times the density of standard 10K ECL logic.

by Cary R. Champlin and Jerry E. Prioste

In any IC technology, LSI exhibits many advantages. In 10K ECL, speed and logic density are particularly important benefits. A family of standard ICs derived from the MCA I macrocell array, for example, gives the ECL designer greater than a fourfold increase in speed, and two orders of magnitude reduction in package count.

The MC109XX high speed family consists of an LSI multiplier, two types of ALUs, a program sequencer, and an error detection/correction unit. Each of these parts has logic densities of approximately 1200 equivalent gates and typical gate delay times of 800 ps. In comparison, an IC in 10K ECL typically has a logic density of 12 gates and gate delay times of 3.5 ns.

A common problem for high speed applications is the optimal filtering of digital signals. Optimal filtering occurs when filter characteristics are adjusted in accordance with the optimization of some signal parameter. An example of a third-order adaptive digital filter is shown in Fig 1. Two distinct areas of computation are required. In the digital filtering area, four multiplications and four additions are computed for each raw input signal sample in what is termed a "weighted-moving-average."

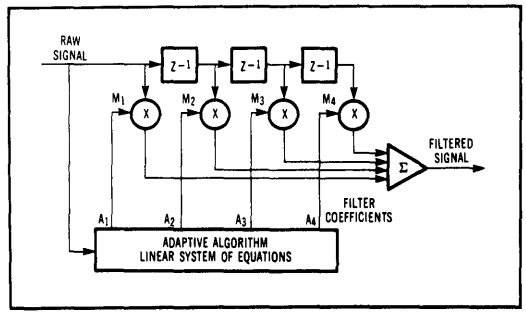


Fig 1 In this adaptive digital filter, the adaptiveness of the coefficients to the signal guarantees convergence to an optimal response with respect to a desired system parameter. When implemented in hardware, this application is intensive in arithmetic and addressing.

In the second area of computation, the adaptive algorithm solves a linear system of equations to obtain new filter coefficients. When solving a linear system of equations, variables and coefficients are organized naturally in vectors. Similarly, filter samples can be represented using vector notation. Note that in the actual implementation of the filter, the signal samples must be delayed (ie, stored) by an amount of time equal to the computation time of the adaptive algorithm. This will match—with respect to time—the filter coefficients and the signal samples.

Cary R. Champlin is a senior electrical engineer in the Aerospace Data Section at Motorola's Government Electronics Group, 8201 East McDowell Rd, Scottsdale, AZ 85282. Mr. Champlin has a BSEE from the University of Wyoming and an MSE from Arizona State University.

Jerry E. Prioste is a systems engineer in Motorola's Bipolar LSI and Memory Products Div, 2200 West Broadway, Mesa, AZ 85202. He holds a BSEE from New Mexico State University and an MSE from Arizona State University.

Reprinted with Permission
COMPUTER DESIGN/May 1984

Traditionally, arithmetic intensive applications, such as the optimal filtering problem, require unique fixed-hardware implementations. This creates problems for the designer when the adaptive algorithm or the order of filter is modified. The alternate approach, provided the technology is sufficiently fast, is to implement the design with a computer architecture based on a linear algebra enhanced instruction set. The MC109XX family modularizes this architectural approach into three basic sections: arithmetic, memory-I/O, and control-interface.

Accelerating operations

Data is configured as a 32-bit floating point number, using an 8-bit exponent and a 24-bit mantissa format. This allows enough dynamic range for a large class of applications without compromising computational throughput. As shown in Fig 2, this also allows a specialized arithmetic module architecture based on four fundamental computations: multiply, multiply-accumulate, add/subtract, and add/subtract-accumulate.

Using an 8-bit exponent and a 24-bit mantissa format allows dynamic range for a large class of applications.

The algorithm for floating point multiplication begins by multiplying the two 24-bit mantissa fields using nine MC10901 8 x 8-bit expandable multipliers. The MC10901 is a parallel, combinatorial array based on the Dadda reduction and a fast lookahead-carry addition scheme. This method results in a maximum 8 x 8-bit multiplication time of 24.3 ns. Two mode controls (C1 and C2) are used to set the multiplier for 2's complement, unsigned magnitude, or mixed-mode operands. Through the use of C1 and C2 and the two 8-bit additive operand inputs, larger arrays are easily constructed with the MC10901.

For two left-justified operands, their product is either normalized or has 1 bit of sign extension. Examination of the top 2 product bits will detect the position of the active MSB. The MC10808 16-bit barrel shifter accomplishes the necessary shifting; two MC10808s are needed to shift a 24-bit number.

The other part of the floating point multiply algorithm is exponent processing, which requires a two-step sequence. After the exponents of the two operands are summed, the result is decremented if the MSB detect indicates sign extension in the product. The MC10902 high speed ALU is used as the exponent processor for the multiplier and the floating point add/subtract unit. OV1 is the overflow for binary arithmetic operations, while OV2 is the overflow for shift left operations. The MC10902 uses an internal 8-bit register as an accumulator or for pipeline system structures.

Floating point addition/subtraction, although more involved, is equally efficient when designed with LSI ECL. For both computations, the first step is to equalize the exponents of the two operands to align the binary point. The exponent differential is calculated and a corresponding downshift applied to one of the operand mantissas. The sign bit of the

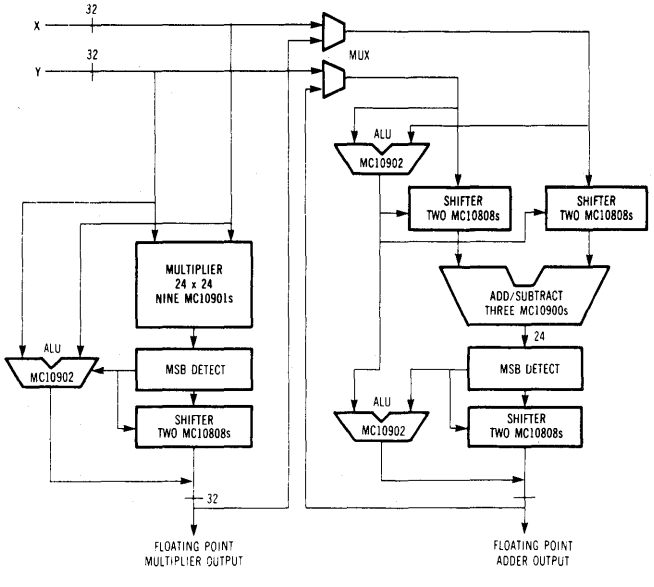


Fig 2 The 32-bit floating point arithmetic module relies heavily on LSI ECL devices. Four fundamental operations support real and complex arithmetic: multiply, multiply-accumulate, add/subtract, and add/subtract-accumulate.

Reprinted with Permission
COMPUTER DESIGN/May 1984

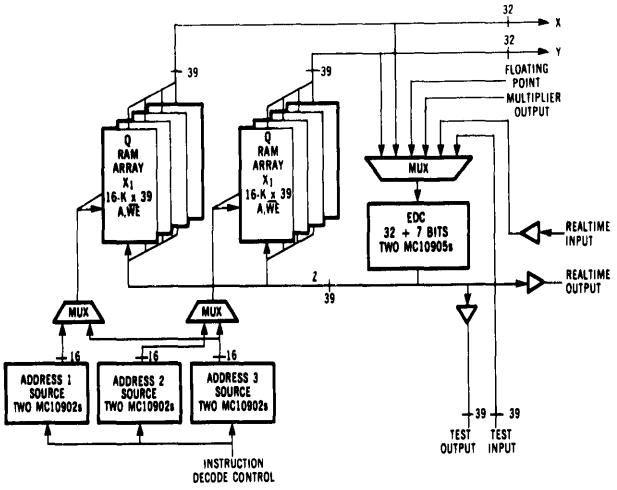


Fig 3 The MC10902 is efficient in operand address generation and arithmetic sections. To access a vector, the unit computes a sequence of locations from initial base address, displacement, index, and step-size values. The MC10905 error detection and correction (EDC) improves data validity and enhances testing diagnostics, yet only increases the pipeline by one cycle.

exponent differential selects which operand is downshifted and which exponent is used next. Two suboperations occur in the second stage. The larger exponent is gated to the second exponent ALU and the two 24-bit operands are added/subtracted.

Three MC10900 8-bit ALUs form the mantissa adder and I/O latching supports the pipelined architecture of the arithmetic module. The MC10900 generates a sum with a maximum delay of 17 ns. Using three devices and ripple carry yields a 24-bit sum in under 32 ns. Although not implemented in this application, the MC10900 maintains full parity generation and verification internally.

The third stage consists of detecting the position of the active MSB in the summation. An upshift in the range of -1 to 25 is possible at this point. Caused by an arithmetic overflow, the -1 upshift corresponds to a single-bit downshift. Total computation pipeline time for either of the two floating point calculations is 80 ns or four clock cycles. However, data is pipelined at two clock cycle intervals.

Considering memory and I/O

The continuous processing characteristic of the arithmetic module carries over to the memory architecture of Fig 3. Four interrelated sections comprise this module: dual RAM array, address generation, error detection and correction (EDC), and I/O multiplexing. Data flow during execution of a typical instruction depends on the timely interaction of these sections. First, sequences of addresses are generated from two source address ALUs and then time multiplexed to the dual RAM array during the read cycles. X and Y vector source data is routed to the arithmetic module and monitored by the EDC on a time-multiplexed basis. A flag is set upon the detection of an error. The floating point result is generated four clock cycles later and 7 check bits are appended. Finally, a sequence of addresses, generated from the destination address ALU, is applied to the dual RAM array during the write cycles. The dual RAM array is architecturally suited for three-part address, high speed vector access requirements. A dual-read/single-write memory organization nicely matches the imbalance of multiple read operations.

The continuous processing characteristic of the arithmetic module carries over to memory architecture.

Vector stack addressing is used for each operand. A 16-bit, 2's complement displacement is added to the base address, and each subsequent location is determined by the addition of a 16-bit, 2's complement step-size value. The selection of real or complex data affects addressing. To multiply complex numbers, four read multiplications and two additions or subtractions are necessary. This requires the source addressing to repeat each complex number in a specific sequence. The MC10902 ALU handles address computations (Fig 4). The internal register and the input data latches hold the current values for base, displacement, and step-size parameters. Register values load from the bit fields of the instruction decode control logic.

If applications require detailed interpretation of output data, as in image analysis, then some form of error control is warranted. The MC10905 16-bit EDC is based on a modified Hamming code that allows full single-bit correction and double-bit detection of errors. Bit-slice operation is expandable to 96-bit words. The MC10905's separate input and output buses, data latches, check bits, and

Reprinted with Permission
COMPUTER DESIGN/May 1984

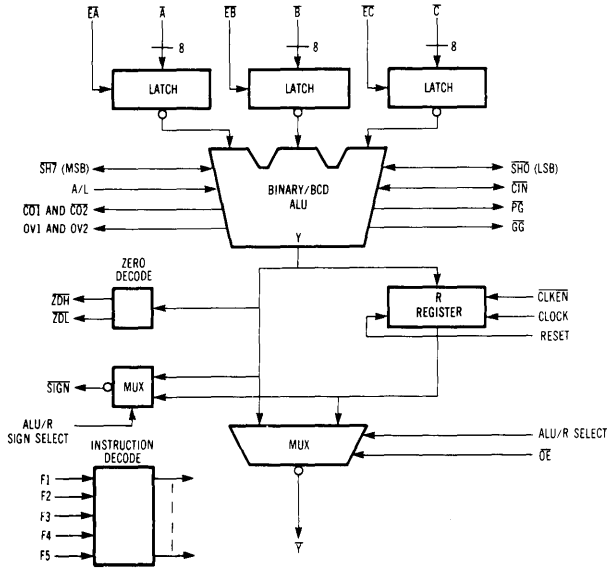


Fig 4 The high speed MC10902 ALU operates on three 8-bit data inputs with an instruction set of 32 functions. Maximum time for addition is 18 ns. Internal zero detection and separate sign bit outputs support direct application of status-bit operations.

error flags allow full support of high speed systems. For 32-bit data, two MC10905 EDCs are required, and 7 check bits are generated. Four modes of operation are possible: read and check, read and correct, generate, and diagnostic. Each of these modes is used in the 32-bit application. A read and check mode is used on the X and Y data as it is accessed for calculations. The read and correct mode is used for external data outputs. The generate mode is applied to floating point results and external data inputs. And, of course, the test lines allow the diagnostic mode to be exercised.

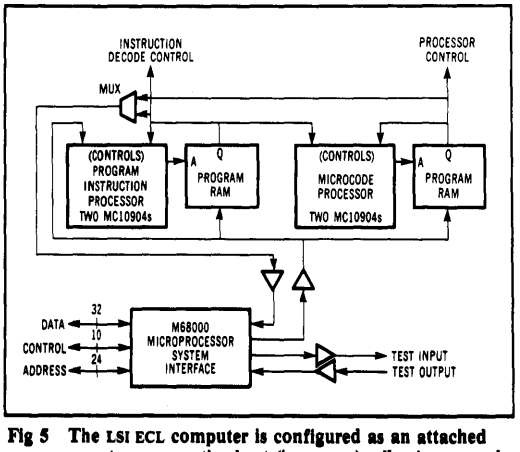


Fig 5 The LSI ECL computer is configured as an attached coprocessor to an executive host (ie, M68000), allowing several to be controlled. The MC10904 is used as the program sequencer for the instructions and the microcode control.

The input as well as output of data to the processor take two forms. The difference between the forms is in the method of handshaking. The test I/O method is non-real time, asynchronous and controlled externally by a host computer. This I/O method is used for performance simulations and its placement simplifies testing. Simple testing allows an I/O check via the EDC, an exercising of the dual RAM, and a thorough testing of the arithmetic functions. Each word of data is transferred when the assertion of an I/O request line is returned with an acknowledge signal. The second method of data transfer is in real time and controlled by sync pulses indicating the beginnings of data batches. Minimal handshake and execution overhead characterizes this method, but the external digital environment must transfer data at an identical high rate.

User access

The module that ties the high speed data processing power of the arithmetic and memory modules to a user accessible environment is the control-interface module. To the host system, the LSI ECL computer appears as an attached coprocessor. Shown in Fig 5, the module consists primarily of three subsections: program processor, microcode processor, and system interface.

Reprinted with Permission
COMPUTER DESIGN/May 1984

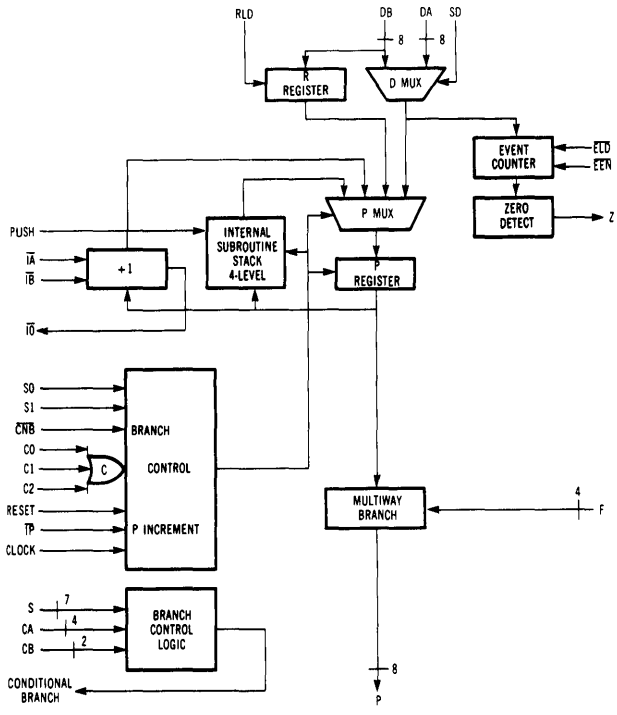


Fig 6 The MC10904 microcode sequencer controls program execution by generating an 8-bit address. The branch control logic allows a complete conditional branching capability, and the use of the "F" lines allows case branching.

The microcode processor executes a sequence of microcode controls in response to an instruction, much like a subroutine is executed in response to a main program call statement. Microcode is repeated for vector operations based on the value of a vector-length register and a simple conditional branch microcode instruction located at the end of each sequence. The MC10904 microcode sequencer slice of Fig 6 is versatile enough to house complete conditional branching and event counting operations internally. Six branch condition inputs combine into 14 logic patterns, minimizing the need for external branch control logic. An internal 8-bit event counter can repeat specific instructions or sequences.

In the program processor subsection, the MC10904 performs as a program counter register. The MC10904 supports several modern programming conventions. Two direct data inputs, DA and DB, provide jump, conditional branch, and subroutine cell destinations. An internal four-level subroutine stack eliminates the need for external logic to handle limited-stack applications. "F" control lines gate the bottom four program addresses to enable up to 16-way case branching. Controlling the $\overline{IA}$ and $\overline{IB}$ increment enable signals allows diagnostic testing of individual instructions.

The system interface attaches the high speed processor to an executive controller for non-realtime computing, program/microcode downloading, and diagnostic testing. The interface is simple, consisting of ECL/TTL translators, data latches, and address decode logic. It appears to the host system as a block of memory locations.

The system-oriented MC109XX IC family offers an alternate approach to the traditional hardwired method of implementing high speed computing applications. Using LSI ECL in system design has the advantages of shortened propagation delay times, increased logic densities, reduced power consumption, and consistent logic structures. New circuits are being identified and developed to expand the family. Exponent processors, address computation units, and activity detection units are some of the proposed candidates for MCA I implementation. Additionally, with the MCA II ECL array introduction, another family of computer-oriented ICs is being developed. With subnanosecond speed and LSI logic density, the MC109XX, and future array-based products, many opportunities exist for ECL logic design.

Reprinted with Permission
COMPUTER DESIGN/May 1984

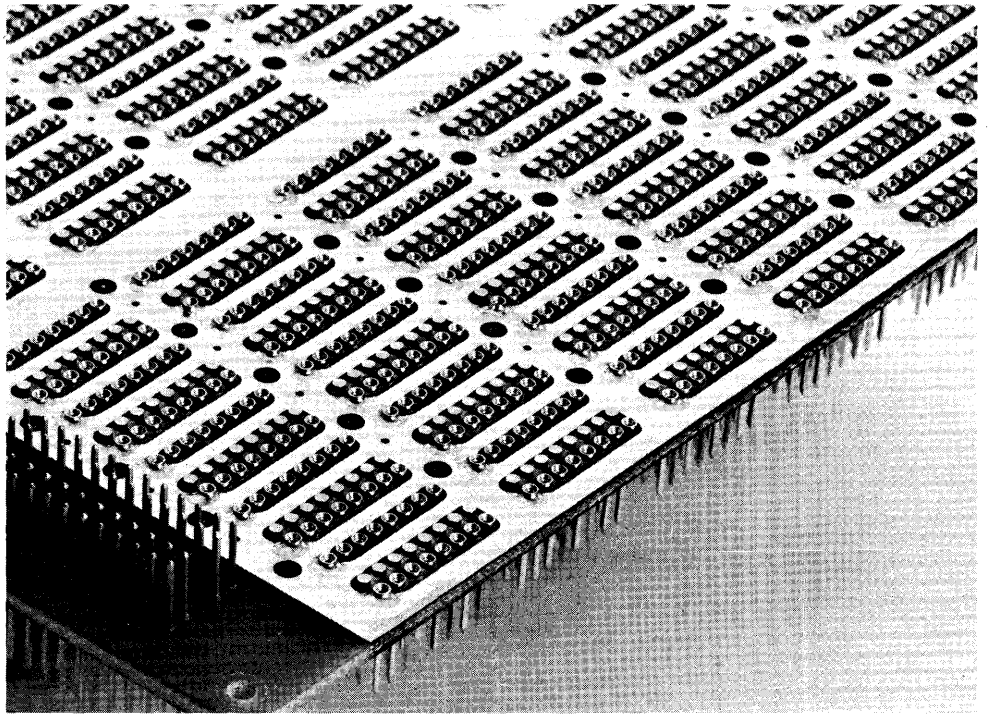
Appendix I

A successful and cost-effective logic system design is brought about by careful attention to hardware and other components, as well as by the use of the proper logic type. Some manufacturers have been developing peripheral components specifically for MECL users. Other hardware and components have appeared on the market and are proving useful in MECL systems. A few examples will be given here. No endorsement of a particular product is intended; rather, any specific components mentioned are by way of example only.

Wirewrap Boards

As mentioned in Chapter 3, wirewrap cards can be used with MECL 10K/10KH. At least one manufacturer (Augat Inc.) is offering boards designed specifically for use with MECL 10K/10KH (see Fig. A-1). Boards of this type have 3 planes: one for V_{CC}, one for

A-1: One type of wirewrap board designed for MECL 10K/10KH applications requiring high density packaging. V_{CC} plane is seen here on same side as IC package locations. V_{TT} and V_{EE} planes are on other side. Resistor tie-ins are made on the wirewrap side of the panel (bottom) to any of 4 V_{TT} pins or 4 isolated pins provided in the row between IC package pins.



V_{EE}, and one for V_{TT}. Provisions are included on the board for bypass capacitors, terminating or damping resistors, and flat-cable interface connections. Characteristic impedance of a wirewrapped line on such panels is typically 100 to 140 ohms.

Thermal Fins

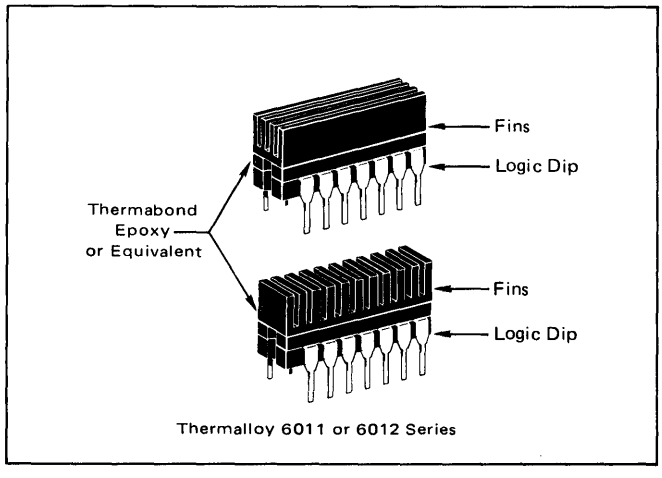
Heat sinking hardware for MECL III devices is discussed in Chapter 6. In addition, it should be pointed out that for some MECL III dual in-line packaged logic functions, finned heat dissipators, attached with thermal epoxy, may be useful. Figure A-2 shows one such approach (offered by Thermalloy Co.)

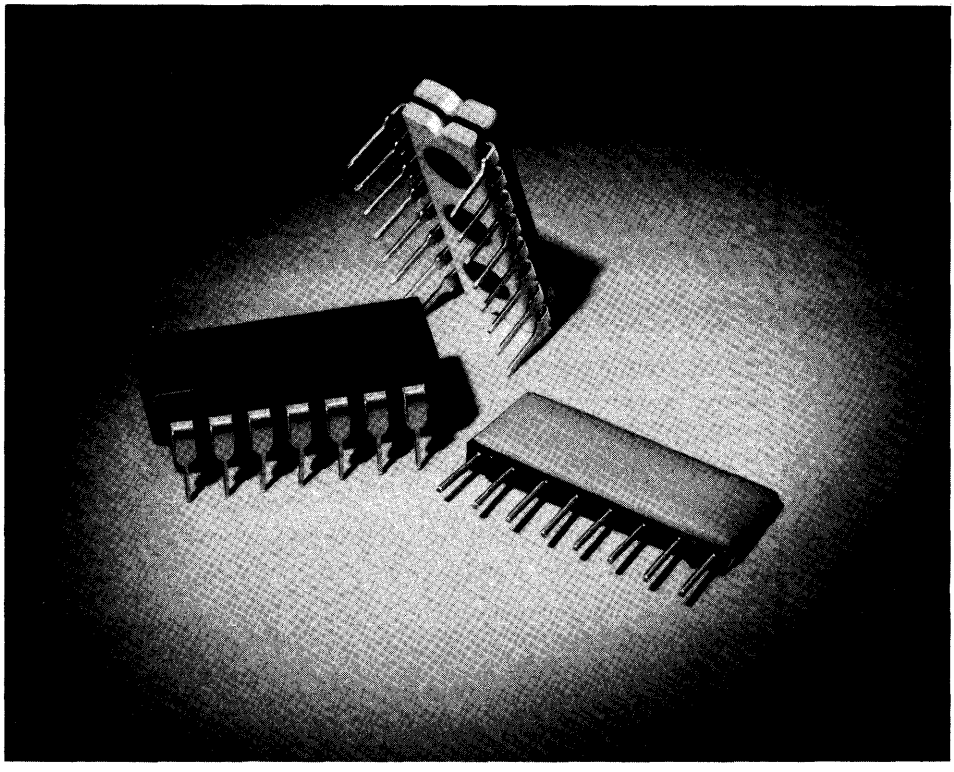
Resistor Arrays

Multiple resistors and resistor arrays are now offered by several manufacturers in dual in-line packages or in single in-line packages (see Figure A-3). Either package style may be obtained with pin count, size, and spacings to mate with IC sockets. A variety of resistor values, tolerances, and power ratings are offered.

Such resistor arrays can prove useful in MECL 10K/10KH logic systems for uses such as series damping, gate output pulldowns, and in-line terminating with either a single resistor or a Thevenin equivalent pair.

A-2: Heat Fins useful with some MECL III logic functions.





A-3: Resistor arrays in single or dual in-line packages are available from several manufactures. Such arrays can serve a variety of uses in system interconnections.

Index of Tabulated Data

Index

8107-10 PRINTED IN USA 4-86 IMPERIAL LITHO C39197 20,000