DL136
REV 2

MOTOROLA

TELECOMMUNICATIONS DEVICE DATA

MOTOROLA TELECOMMUNICATIONS DEVICE DATA

Q3/89
DL136
REV 2

MOTOROLA

TELECOMMUNICATIONS DEVICE DATA

Prepared by
Technical Information Center

Motorola is a major supplier of semiconductors to telecommunications equipment manufacturers worldwide. This book includes complete specifications for a wide variety of devices designed for this market. Selection guides are included to simplify the task of choosing appropriate devices for a system. Applications information, handling and design guidelines, and reliability and quality overviews provide additional support for the user of these circuits.

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ALPHANUMERIC INDEX

This index includes all Motorola devices characterized in this book. Other devices also used in telecommunication applications, but associated with specific product families, appear in the following documents. A number of these devices are specifically referenced in the Selection Guides in Section 1 of this book.

Document No.	Title
DL118/D	Optoelectronics Device Data
DL122/D	MECL Device Data
DL125/D	Rectifiers and Zener Diodes Data
DL126/D	Small-Signal Transistors, FETs and Diodes
DL128/D	Linear and Interface ICs
DL130/D	NMOS/CMOS Special Functions Data
DL139/D	Microprocessor, Microcontroller and Peripheral Data
FR68K/D	M68000 Family Reference
MC . . .	Data Sheets
DSP . . .	Data Sheets

MECL is a trademark of Motorola, Inc.

Selection Guides 1

SELECTION GUIDE

This selection guide includes all Motorola devices characterized in this book. A number of devices that appear in the following documents are added to provide a wider overview of available products.

Document No.	Title
DL118/D	Optoelectronics Device Data
DL122/D	MECL Device Data
DL125/D	Rectifiers and Zener Diodes Data
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MC . . .	Data Sheets
DSP . . .	Data Sheets

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Device Number	Function	Page Number
RF MODEMS		
MC1374	TV Modulator Circuit	DL128/D
MC1496	Balance Modulator/Demodulator	DL128/D
MC1648	Voltage-Controlled Oscillator	DL122/D
MC3356	Wideband FSK Receiver	2-21
MC3357	Low Power FM IF	2-27
MC3359	High Gain Low Power FM IF	2-31
MC3361	Low Voltage Narrow Band FM IF	2-37
MC3362	Low Power Dual Conversion FM Receiver	2-44
MC12000 Series	Prescalers	DL122/D
MC13010	TV Parallel Sound IF and AFT	DL128/D
MC13055	Wideband FSK Receiver	2-133
MC14489	Multi-Character LED Display/Lamp Driver	MC14489/D
MC145026, 7, 8	Programmable Encoder/Decoders	DL130/D
MC145030	Remote Control Encoder/Decoder	MC145030/D
MC145151-2 Series	PLL Frequency Synthesizers	MC145151-2/D
DISCRETE DEVICES		
MFOD1100	Pin Photo Diode for Fiber Optic Systems	DL118/D
MFOE1200	High Power AlGaAs LED Fiber Optic Emitter	DL118/D
MJE270	NPN Power Transistor	2-679
MJE271	PNP Power Transistor	2-679
MPSA42/43	NPN 300 V/200 V TO-92 Transistor	DL126/D
MPS6717	NPN 1 Watt Amplifier Transistor	2-681
1N6274	MO-sorb Zener Overvoltage Suppressor	DL125/D
4N25	Optocoupler	DL118/D
4N35/36/37	Optoisolator	2-682
MPU/MCU		
M6800 Family	Microprocessors	DL139/D
M6801 Family	Microcontrollers	DL139/D
M6804/M68HC04 Family	Microcontrollers	DL139/D
M6805/M68HC05 Family	Microcontrollers	DL139/D
M6809 Family	Microcontrollers	DL139/D
M68HC11 Family	Microcontrollers	DL139/D
M68000 Family	Microprocessors	FR68K/D
SIGNAL PROCESSING		
DSP56001	56-Bit General Purpose Digital Signal Processor	DSP56001/D
DSP56200	Cascadable-Adaptive Finite-Impulse-Response (CAFIR) Digital-Filter Chip	DSP56200/D

Data Sheets 2

MC1488

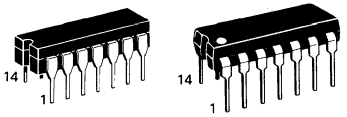
QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

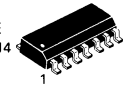
QUAD MDTL LINE DRIVER
RS-232C
SILICON MONOLITHIC INTEGRATED CIRCUIT



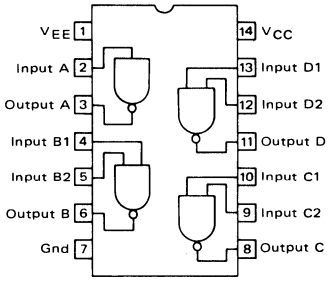
L SUFFIX
CERAMIC PACKAGE
CASE 632-08

P SUFFIX
PLASTIC PACKAGE
CASE 646-06

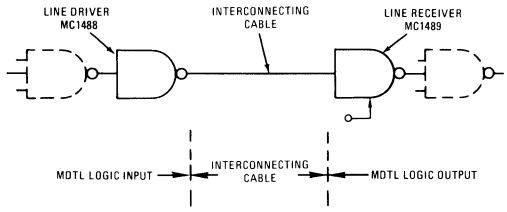
D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
(SO-14)



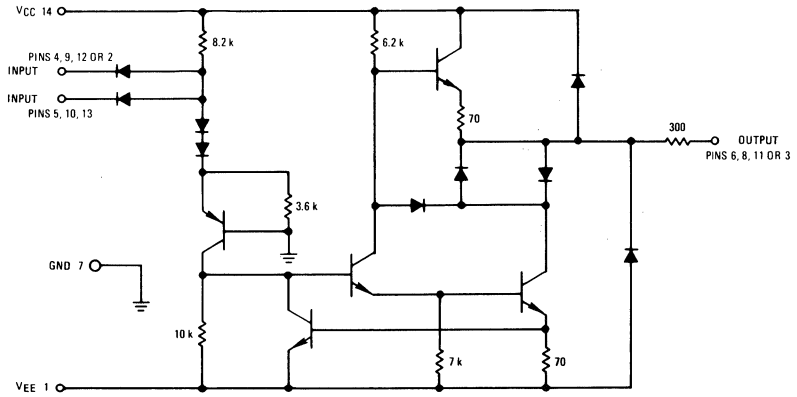
PIN CONNECTIONS



TYPICAL APPLICATION



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



MDTL and MTTL are trademarks of Motorola Inc.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = 0 to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (V_{IL} = 0)	1	I_{IL}	—	1.0	1.6	mA
Input Current — High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	—	—	10	μA
Output Voltage — High Logic State (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OH}	 +6.0 +9.0	 +7.0 +10.5	 — —	Vdc
Output Voltage — Low Logic State (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OL}	 −6.0 −9.0	 −7.0 −10.5	 — —	Vdc
Positive Output Short-Circuit Current (1)	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current (1)	3	I_{OS-}	−6.0	−10	−12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\|V_O\|$ = ±2.0 V)	4	r_o	300	—	—	Ohms
Positive Supply Current (R_l = ∞) (V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)	5	I_{CC}	 — — — — — —	 +15 +4.5 +19 +5.5 — —	 +20 +6.0 +25 +7.0 +34 +12	mA
Negative Supply Current (R_L = ∞) (V_{IH} = 1.9 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −12 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −12 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −15 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −15 Vdc)	5	I_{EE}	 — — — — — —	 −13 — −18 — — —	 −17 −500 −23 −500 −34 −2.5	mA μA mA μA mA mA
Power Consumption (V_{CC} = 9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{CC} = 12 Vdc, V_{EE} = −12 Vdc)		P_C	 — —	 — —	 333 576	mW

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = +25°C.)

Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PLH}	—	275	350	ns
Fall Time	(z_l = 3.0 k and 15 pF)	6	t_{THL}	—	45	75	ns
Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PHL}	—	110	175	ns
Rise Time	(z_l = 3.0 k and 15 pF)	6	t_{TLH}	—	55	100	ns

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

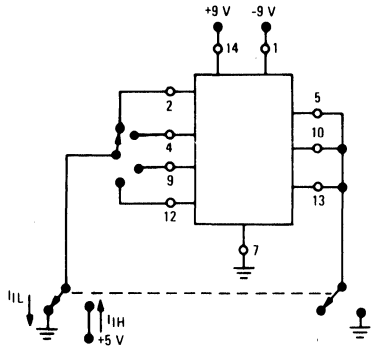


FIGURE 2 – OUTPUT VOLTAGE

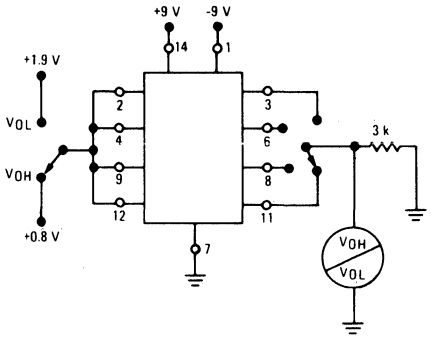


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

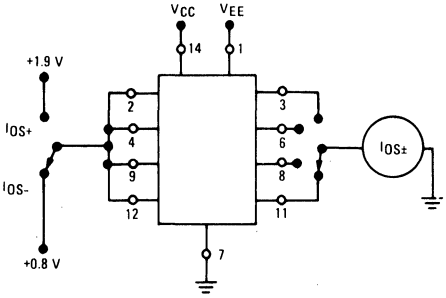


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

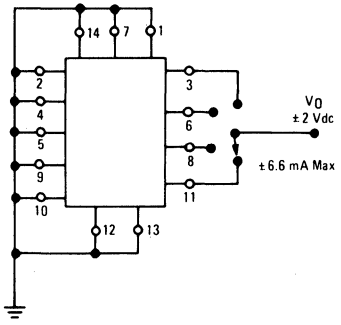


FIGURE 5 – POWER-SUPPLY CURRENTS

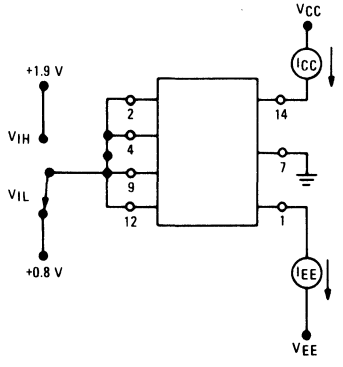
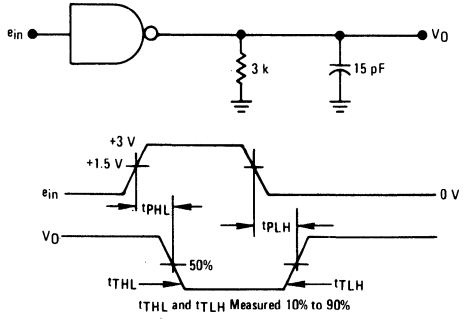


FIGURE 6 – SWITCHING RESPONSE



2

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 — TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

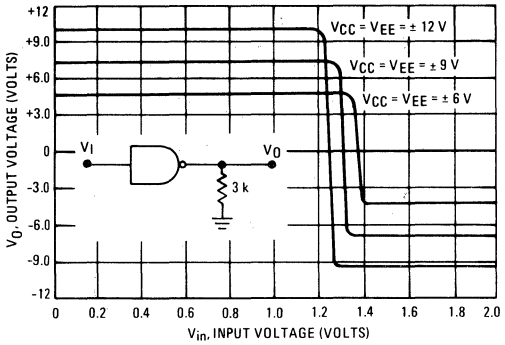


FIGURE 8 — SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

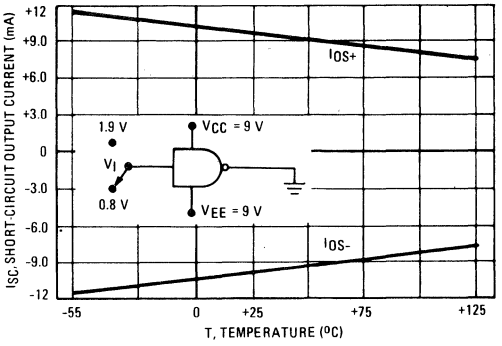


FIGURE 9 — OUTPUT SLEW RATE versus LOAD CAPACITANCE

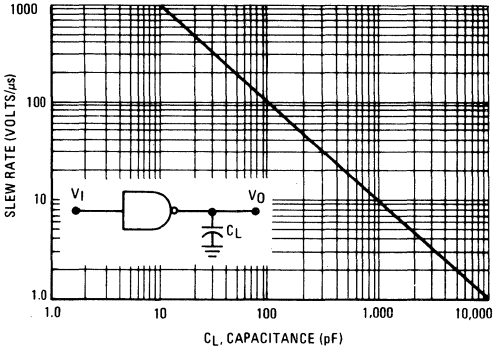


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

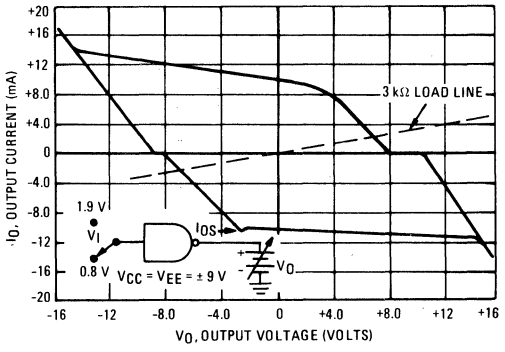
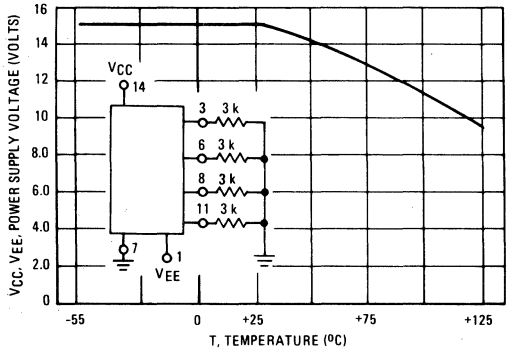


FIGURE 11 — MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



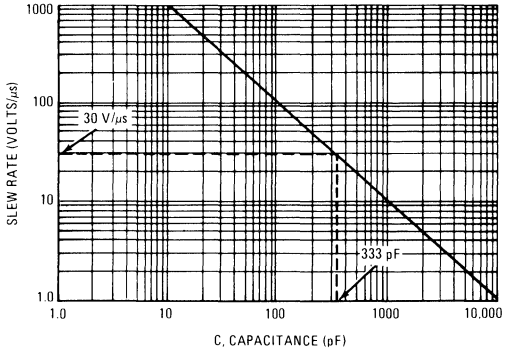
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too

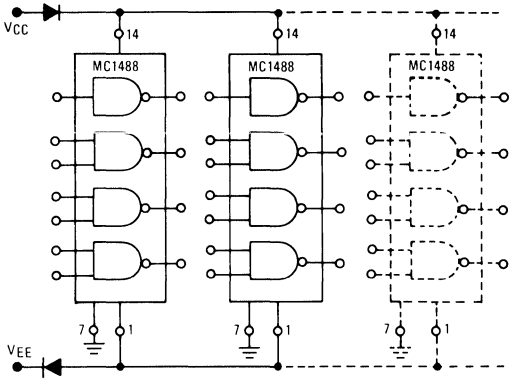
FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

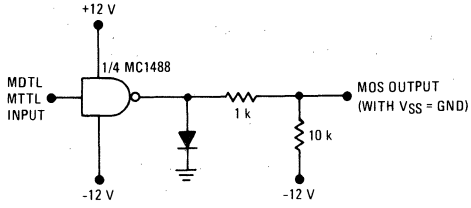
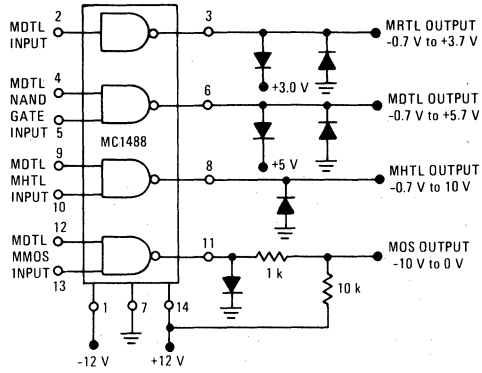


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



MC1489
MC1489A

2

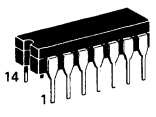
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

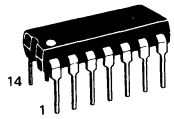
- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  a) Logic Threshold Shifting
  b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS RS-232C

SILICON MONOLITHIC INTEGRATED CIRCUIT

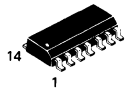


L SUFFIX
CERAMIC PACKAGE
CASE 632-08

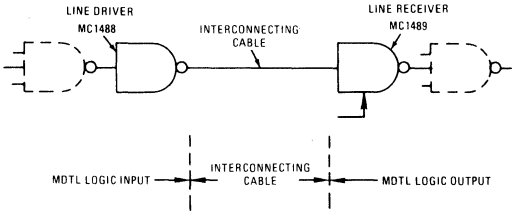


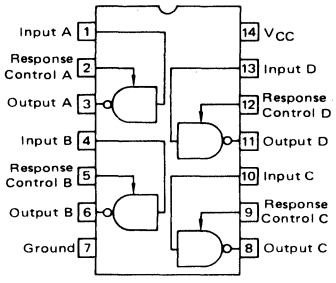
P SUFFIX
PLASTIC PACKAGE
CASE 646-06

D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
(SO-14)

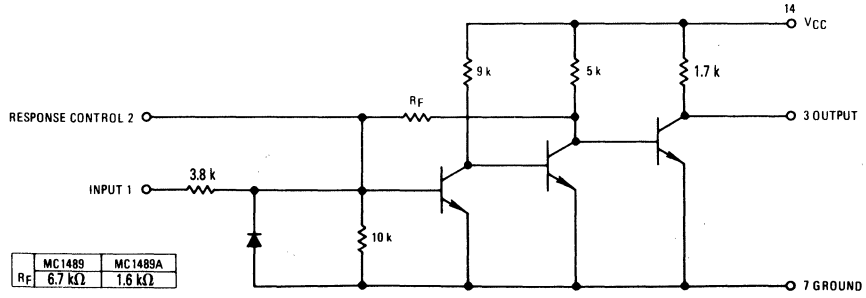


TYPICAL APPLICATION





EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
RF	6.7 kΩ	1.6 kΩ

MDTL and MTTL are trademarks of Motorola Inc.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta JA$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±10%, T_A = 0 to +75°C unless otherwise noted)

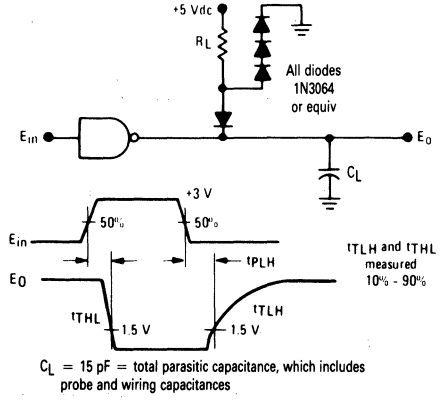
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	I_{IH}	3.6 0.43	— —	8.3 —	mA
Negative Input Current	(V_{IL} = −25 Vdc) (V_{IL} = −3.0 Vdc)	I_{IL}	−3.6 −0.43	— —	−8.3 —	mA
Input Turn-On Threshold Voltage (T_A = +25°C, V_{OL} ≤ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = −0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = −0.5 mA) (Input Open Circuit, I_L = −0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current		I_{OS}	—	−3.0	−4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = +5.0 Vdc)		I_{CC}	—	16	26	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ±1%, T_A = +25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	—	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	—	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	—	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	—	10	20	ns

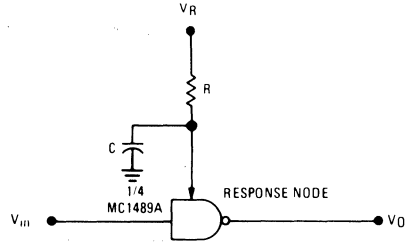
TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE



C_L = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

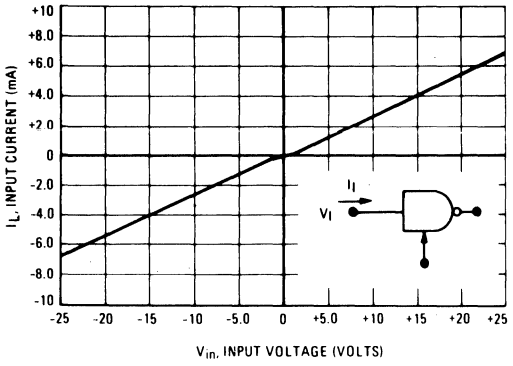


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

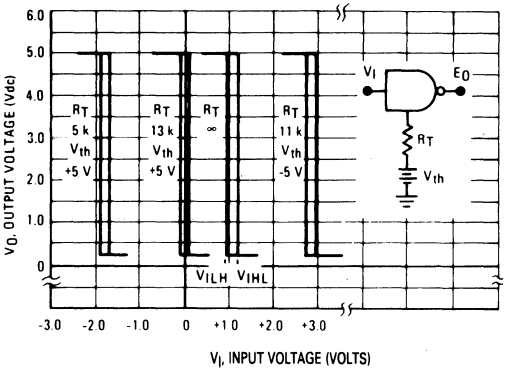


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

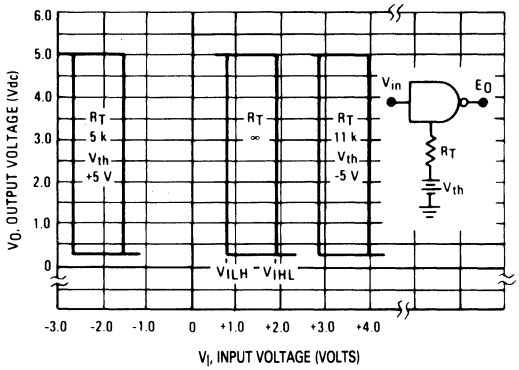


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

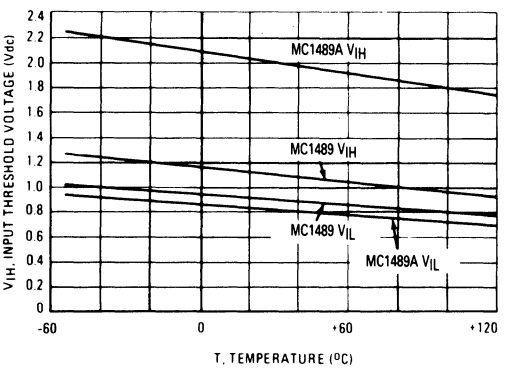
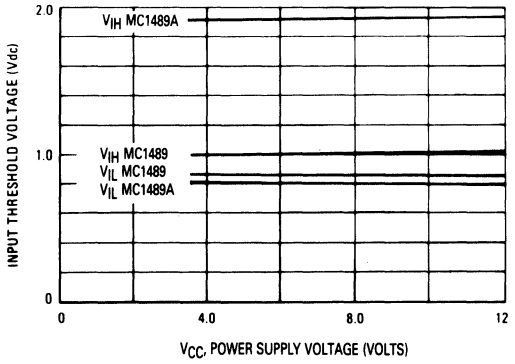


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

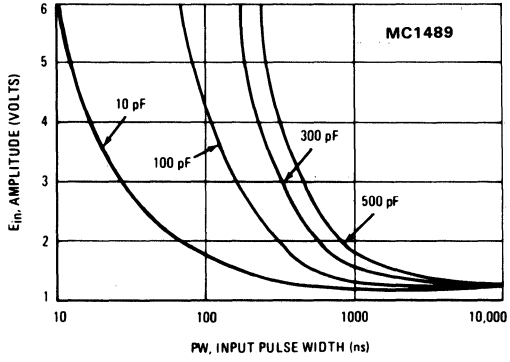
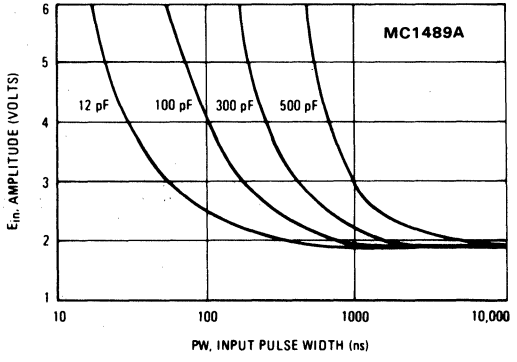


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

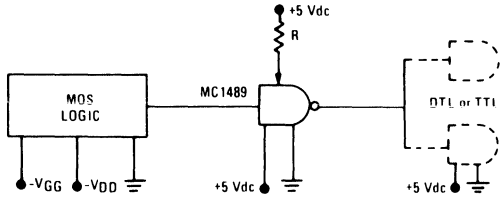
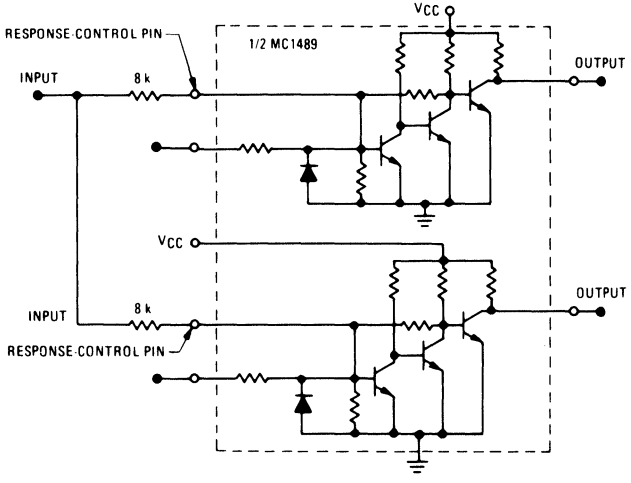


FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



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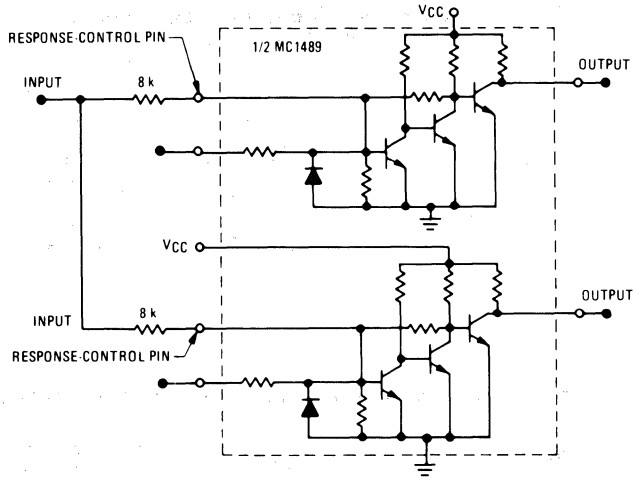
APPLICATIONS INFORMATION (continued)

FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



MC2831A

LOW POWER FM TRANSMITTER SYSTEM

The MC2831A is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a Microphone Amplifier, Pilot Tone Oscillator, Voltage Controlled Oscillator and Battery Monitor.

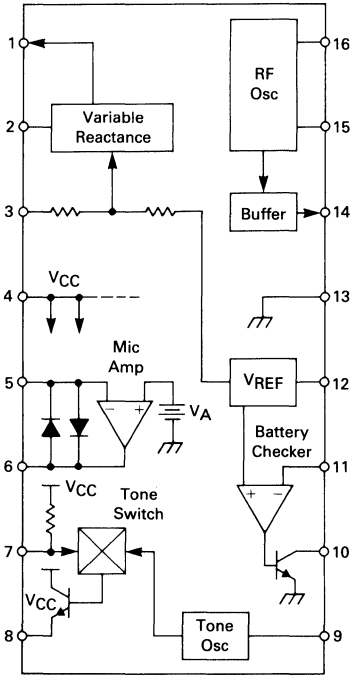
- Wide Range of Operating Supply Voltage (3.0 V–8.0 V)
- Low Drain Current (4.0 mA Typ Full Operation at V_{CC} = 4.0 V)
- Battery Checker (290 μA Typ at V_{CC} = 4.0 V)
- Low Number of External Parts Required

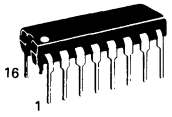
LOW POWER FM TRANSMITTER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

2

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

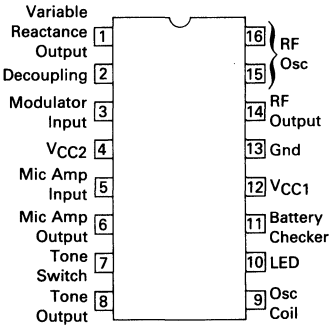




P SUFFIX
PLASTIC PACKAGE
CASE 648-08

D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

PIN ASSIGNMENTS



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 12	V_{CC}	10	Vdc
Operating Supply Voltage Range	4, 12	V_{CC}	3.0 to 8.0	Vdc
Battery Checker Output Sink Current	10	I_{LED}	25	mA
Junction Temperature	—	T_J	+150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +75	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC1} = 4.0 Vdc, V_{CC2} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Drain Current	I_{CC1}	12	150	290	420	μA
Drain Current	I_{CC2}	4	2.2	3.6	6.5	mA
BATTERY CHECKER						
Threshold Voltage (LED Off → On)	V_{TB}	11	1.0	1.2	1.4	Vdc
Output Saturation Voltage (Pin 11 = 0 V, Pin 10 Sink Current = 5.0 mA)	V_{OSAT}	10	—	0.15	0.5	Vdc
MIC AMPLIFIER						
Voltage Gain, Closed Loop (V_{in} = 1.0 mV_{rms}, f_{in} = 1.0 kHz)	—	5, 6	27	30	33	dB
Output dc Voltage	—	6	1.1	1.4	1.7	Vdc
Output Swing (V_{in} = 30 mV_{rms}, f_{in} = 1.0 kHz)	—	6	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_O = 31 mV_{rms}, f_{in} = 1.0 kHz)	THD	6	—	0.7	—	%
PILOT TONE OSCILLATOR (250 Ω LOADING)						
Output AF Voltage (f_O = 5.0 kHz)	—	8	—	50	—	mV_{rms}
Output dc Voltage	—	8	—	1.4	—	Vdc
Total Harmonic Distortion (f_O = 5.0 kHz, V_{AF} = 150 mV_{rms})	—	8	—	1.8	5.0	%
Tone Switch Threshold	—	7	1.1	1.4	1.7	Vdc
FM MODULATOR (120 Ω LOADING)						
Output RF Voltage (f_O = 16.6 MHz)	VRFO	14	—	40	—	mV_{rms}
Output dc Voltage	—	14	—	1.3	—	Vdc
Modulation Sensitivity (Note 1) (V_{in} = 1.0 V ± 0.2 V)	—	3, 14	6.0	10	18	Hz/mVdc
Maximum Deviation (Note 1) (V_{in} = 0 V to +2.0 V)	—	3, 14	±2.5	±5.0	±12.5	kHz
RF Frequency Range	—	14	—	—	60	MHz

Note 1. Modulation sensitivity and maximum deviation are measured at 49.815 MHz, which is the third harmonic of the crystal frequency.

FIGURE 2 — TEST CIRCUIT

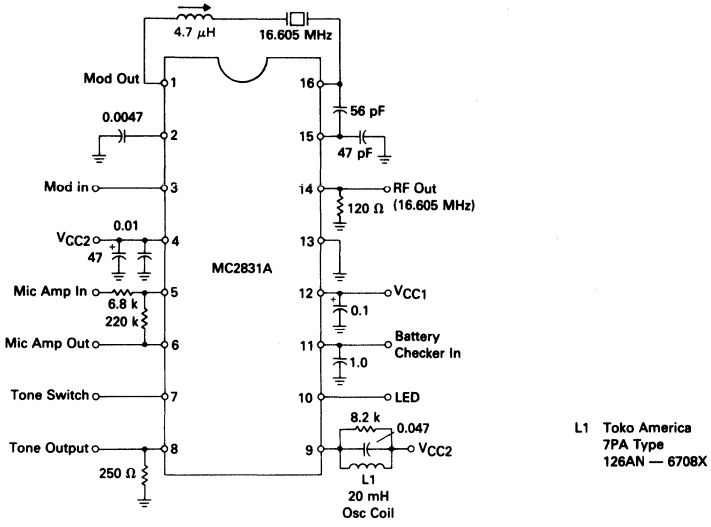
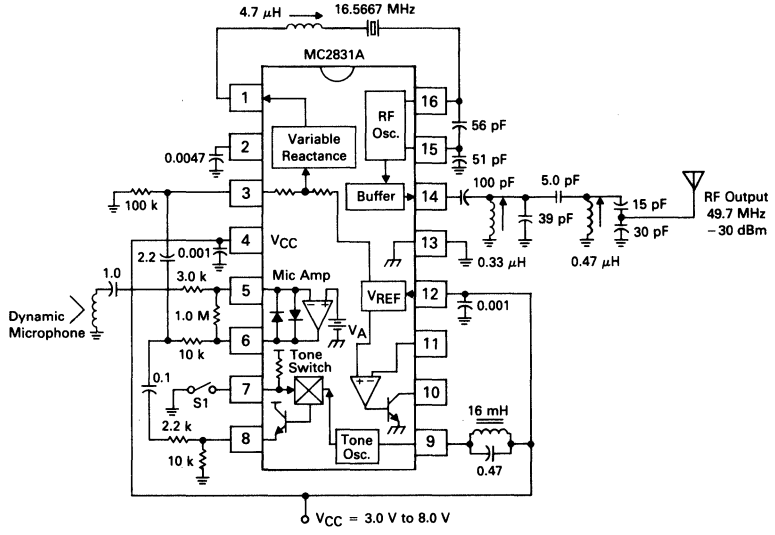


FIGURE 3 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES:

S1 is a normally closed push button type switch.

The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which generates useful harmonics to 60 MHz.

The network on the output at Pin 14 provides output tuning and impedance matching to 50 Ω at 49.7 MHz. Harmonics are suppressed by more than 25 dB.

Battery checker circuit (Pins 10, 11) is not used in this application.

All capacitors in microfarads, inductors in Henries and resistors in Ohms, unless otherwise specified.

MC2833

Product Preview

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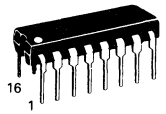
LOW POWER FM TRANSMITTER SYSTEM

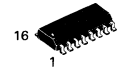
MC2833 is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- −30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On-Chip Transistor Amplifiers

LOW POWER FM TRANSMITTER SYSTEM

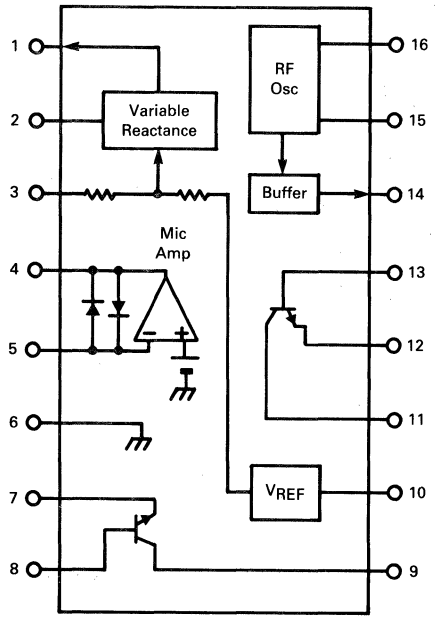


P SUFFIX
PLASTIC PACKAGE
CASE 648-08

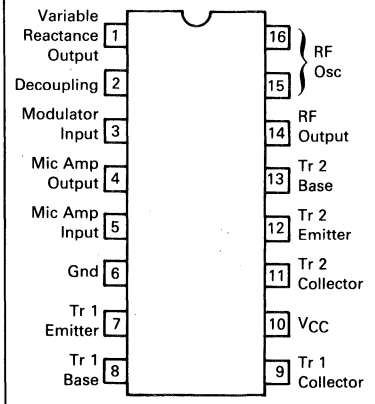


D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3.0 14	7.0 —	10 —	15 —	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3.0 14	3.0 —	5.0 —	10 —	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_v	4.0 5.0	27 —	30 —	33 —	dB
Output DC Voltage (No input signal)	V_{out} dc	4.0	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p-p	4.0	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4.0	—	0.15	2.0	%

AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	—	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	—	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	—	70	—	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	—	6.2	—	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	—	—	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	—	—

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	—	500	—	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	—	2.0	—	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	—	3.3	—	pF

2

FIGURE 1 — TEST CIRCUIT

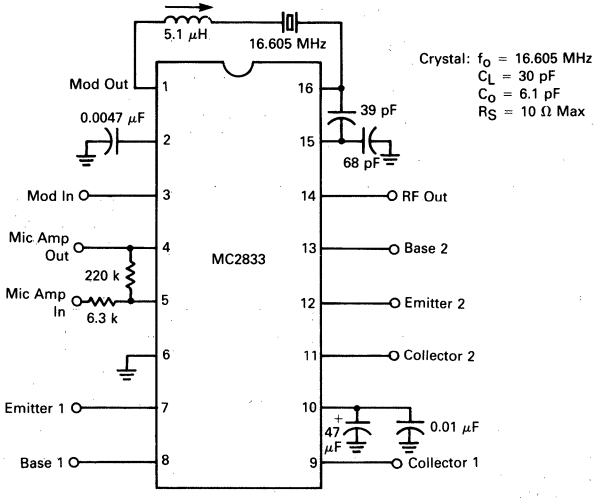
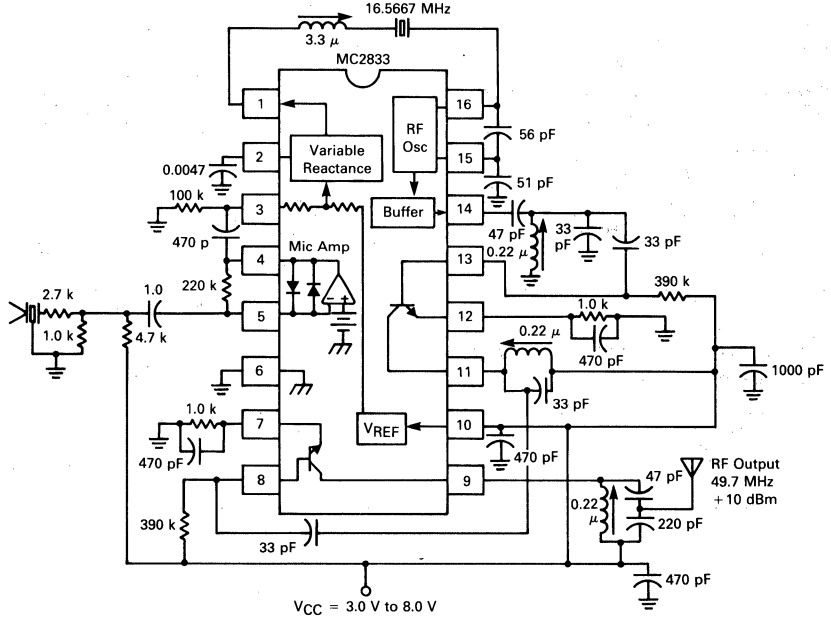


FIGURE 2 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES: The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which is being used as a frequency tripler in this application.
The networks in the output stages provide frequency selectivity and impedance matching at 49.7 MHz.
The RF output is +10 dBm (10 mW into 50 Ω load) at 49.7 MHz, with all harmonics reduced by more than 50 dB.
All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.
0.22 μH inductors are Toko B199SN-T1048Z
3.3 μH inductor is Toko B199KN-T1055Z

MC3356

Advance Information

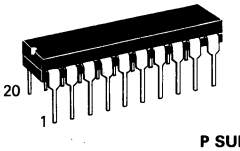
WIDEBAND FSK RECEIVER

. . . includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly versatile, full-function device, yet few external parts are required

WIDEBAND FSK RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

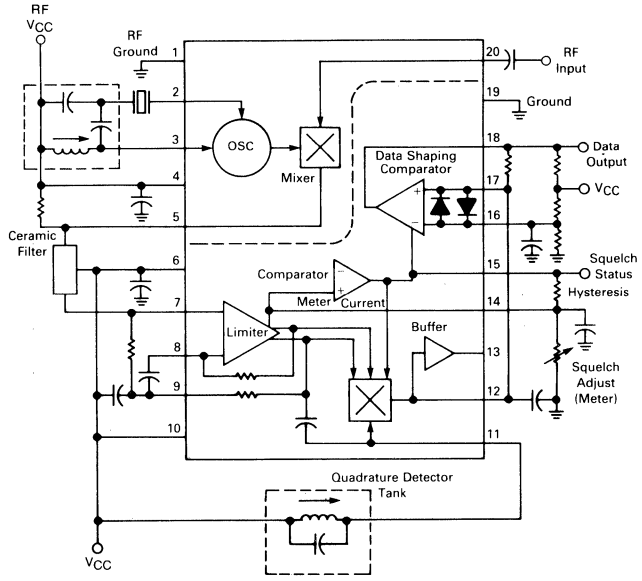
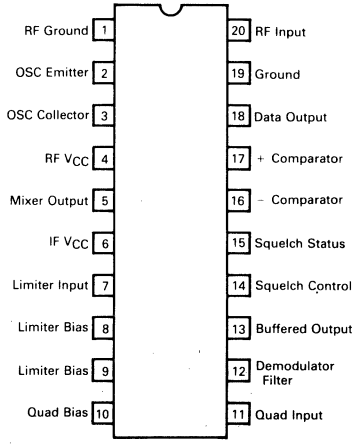


FIGURE 2 — PIN CONNECTIONS



This is advance information on a new introduction and specifications are subject to change without notice.

2

MAXIMUM RATINGS

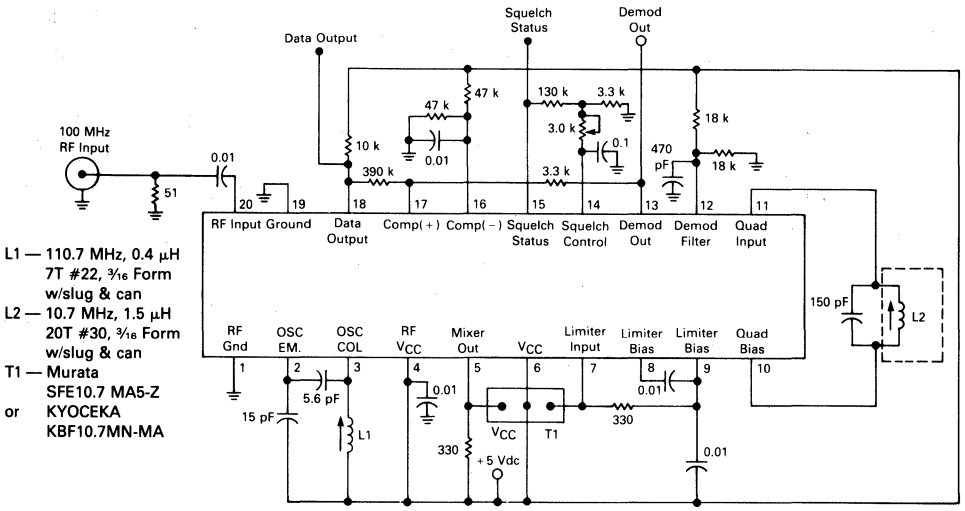
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating R.F. Supply Voltage Range (Pin 4)	R.F. V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 3, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	—	20	25	mAdc
Input for −3 dB limiting	—	30	—	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	—	60	—	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	—	2.0	3.0	
Mixer Input Resistance, 100 MHz	—	260	—	Ω
Mixer Input Capacitance, 100 MHz	—	5.0	—	pF
Mixer/Oscillator Frequency Range (Note 1)	—	—	200	MHz
IF/Quadrature Detector Frequency Range (Note 1)	0.2	—	50	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	—	50	—	dB
Demodulator Output, Pin 13	—	0.5	—	Vrms
Meter Drive	—	7.0	—	μA/dB
Squelch Threshold	—	0.8	—	Vdc

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

FIGURE 3 — TEST CIRCUIT



L1 — 110.7 MHz, 0.4 μH
7T #22, 3/16 Form
w/slug & can
L2 — 10.7 MHz, 1.5 μH
20T #30, 3/16 Form
w/slug & can
T1 — Murata
SFE10.7 MA5-Z
or KYOCEKA
KBF10.7MN-MA

FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

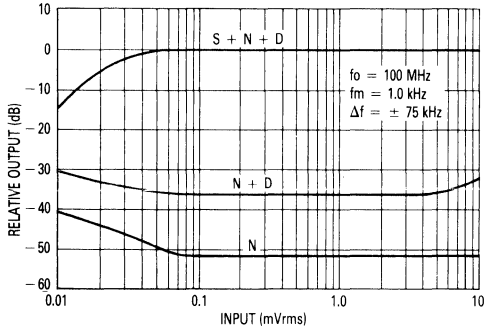
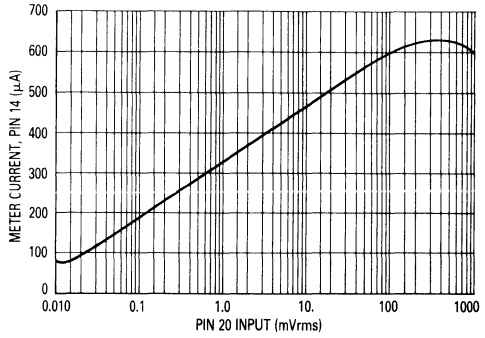


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



2

General Description

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 400 MHz. A mixer/oscillator voltage gain of 2 up to approximately 200 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but nonlinearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The −3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

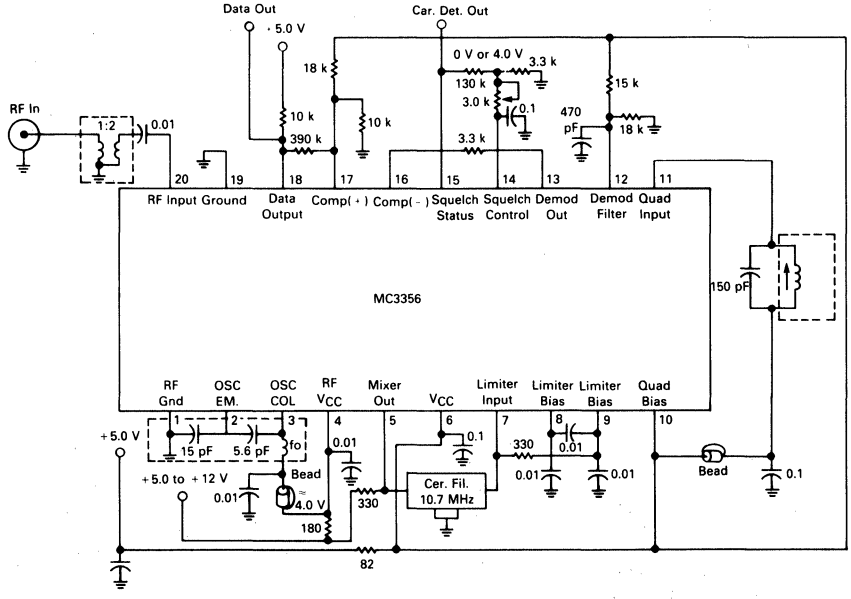
The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+)input of Data Shaper as shown in figures 1 and 3.)

2

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER



Application Notes

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

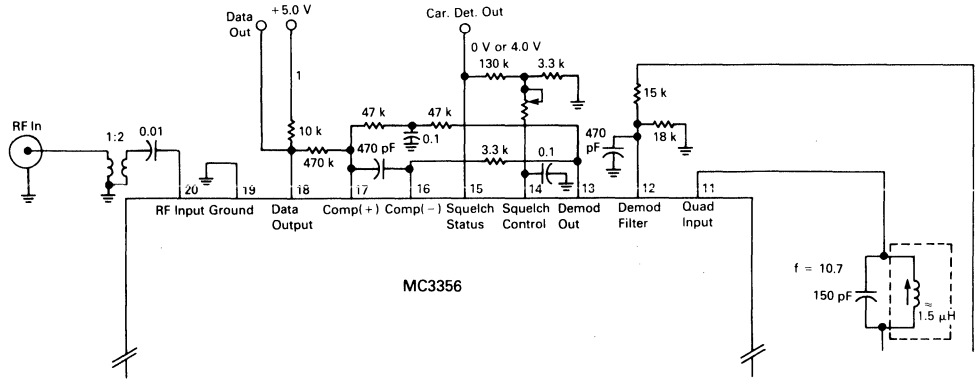
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has separate V_{CC}'s and grounds for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of figures 1 and 3 have RF, oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a *separate* path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER



APPLICATION NOTES, continued

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

2

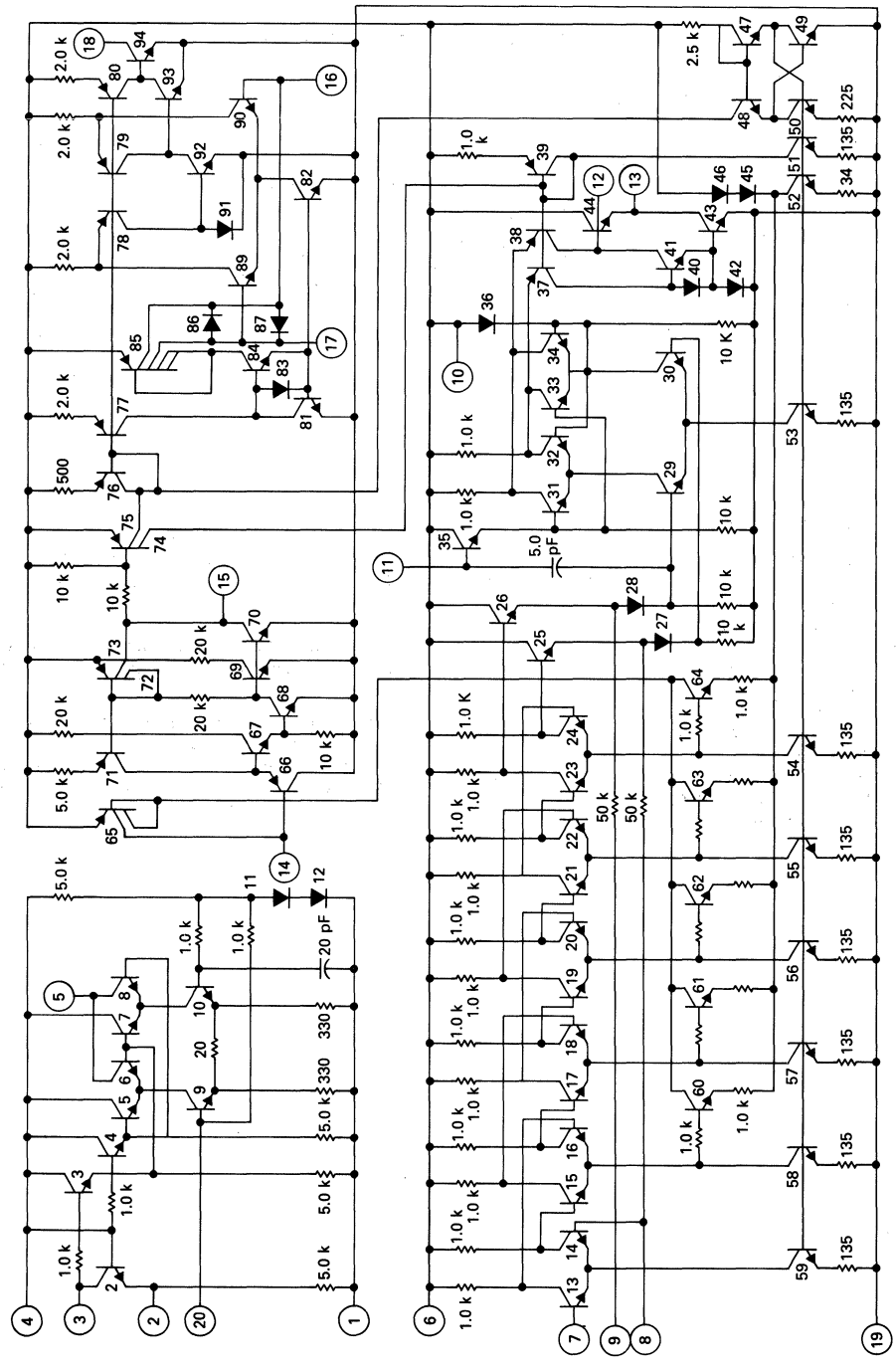


FIGURE 8 — INTERNAL SCHEMATIC

MC3357

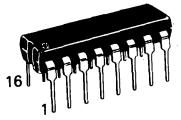
LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required

LOW POWER FM IF

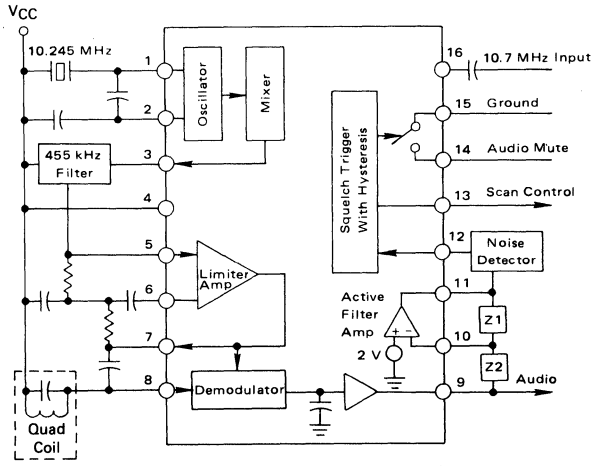
SILICON MONOLITHIC INTEGRATED CIRCUIT



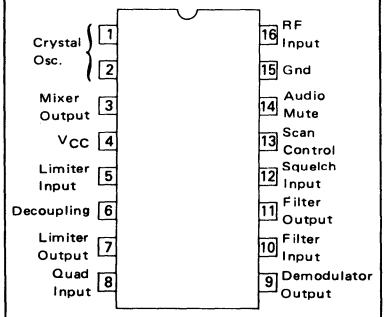
P SUFFIX
PLASTIC PACKAGE
CASE 648-08

D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



2

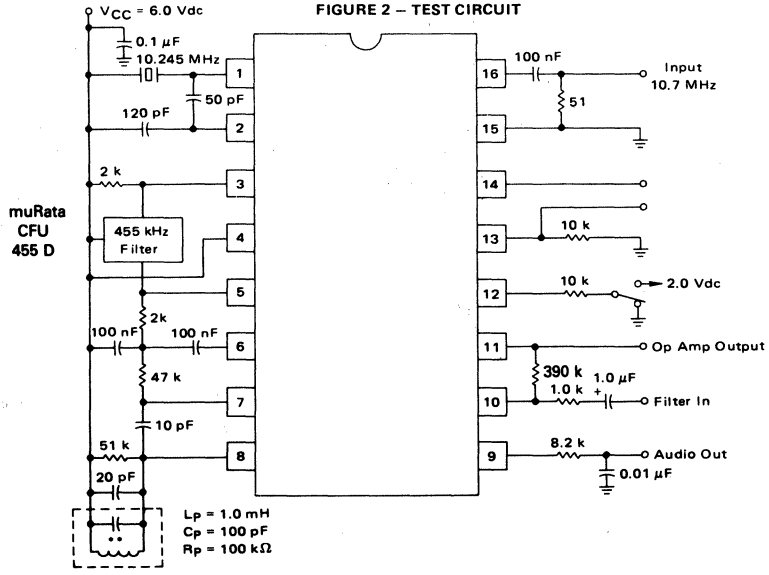
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp-p
Input Voltage (V_{CC} ≥ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	-30 to +70	°C
Storage Temperature Range	–	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4				mA
Squelch Off		–	2.0	–	
Squelch On		–	3.0	5.0	
Input Limiting Voltage (–3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

FIGURE 2 – TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

2

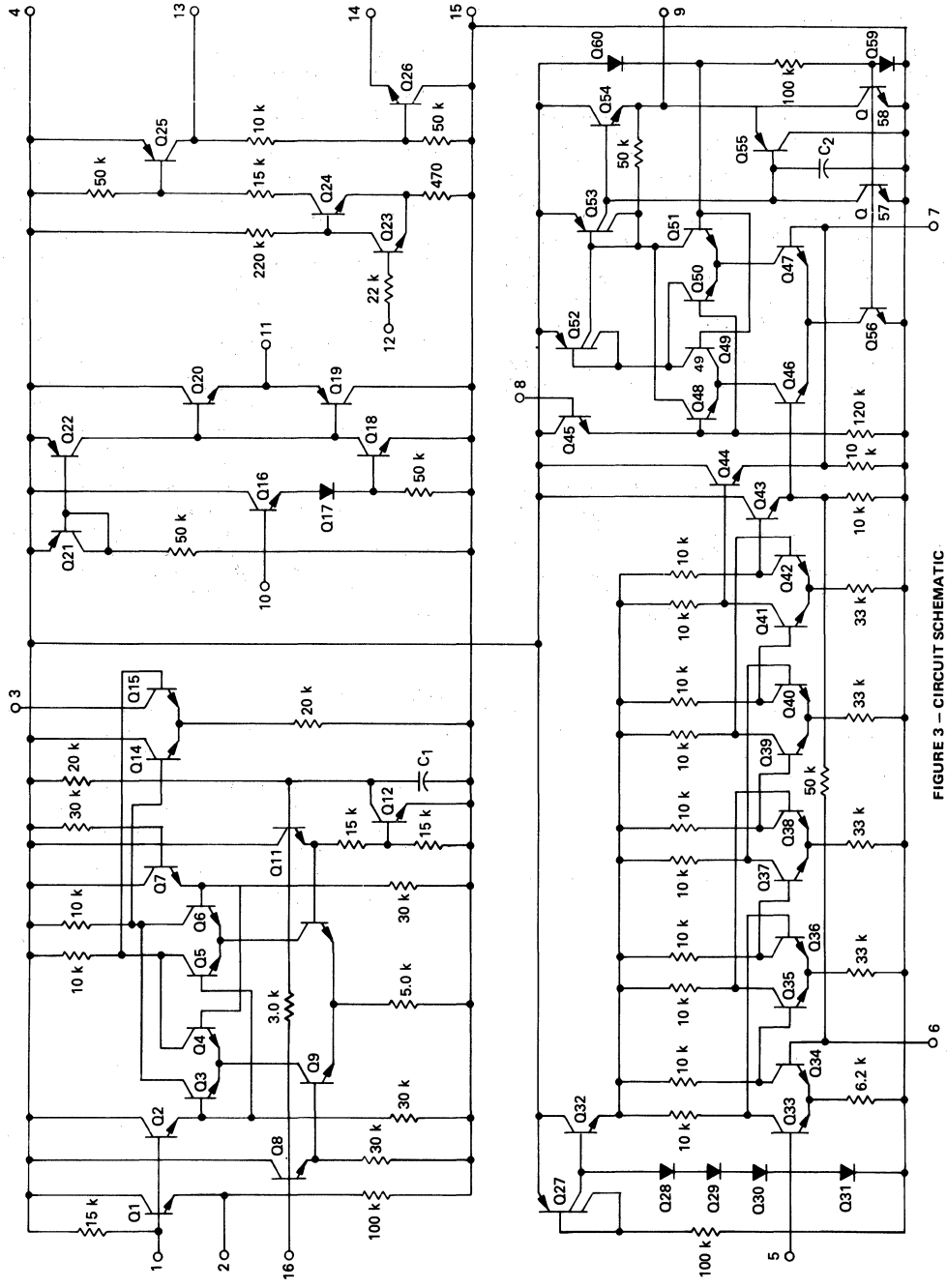


FIGURE 3 – CIRCUIT SCHEMATIC

MC3359

HIGH GAIN LOW POWER FM IF

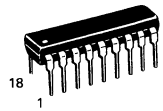
SILICON MONOLITHIC INTEGRATED CIRCUIT

2

LOW POWER NARROWBAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts.

- Low Drain Current: 3.6 mA (Typ) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV (Typ)
- Low Number of External Parts Required



P SUFFIX
PLASTIC PACKAGE
CASE 707-02

DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03

FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER

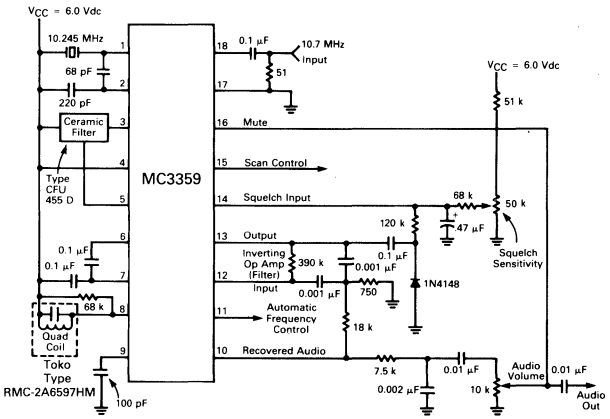
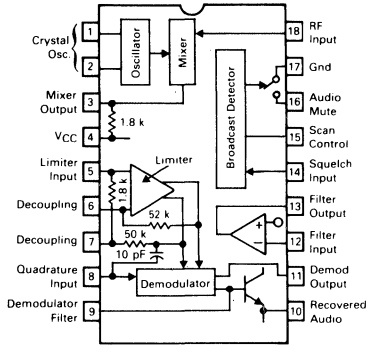
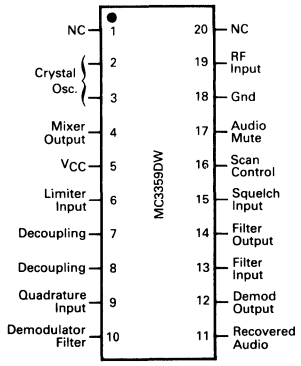


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



CASE 707-02



CASE 751D-03

2

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 9	Vdc
Input Voltage (V_{CC} ≥ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	−0.7 to 12	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off Squelch On	— —	3.6 5.4	6.0 7.0	mA
Input for 20 dB Quieting		—	8.0	—	μVrms
Input for −3.0 dB Limiting		—	2.0	—	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		—	46	—	
Mixer Third Order Intercept, 50 Ω Input		—	−1.0	—	dBm
Mixer Input Resistance		—	3.6	—	kΩ
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	—	mVrms
Detector Center Frequency Slope, Pin 10		—	0.3	—	V/kHz
AFC Center Slope, Pin 11, Unloaded		—	12	—	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	—	dB
Squelch Threshold, Through 10K to Pin 14		—	0.62	—	Vdc
Scan Control Current, Pin 15	Pin 14 — High — Low	— 2.0	0.01 2.4	1.0 —	μA mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 — High — Low	—	5.0 1.5	10 —	Ω MΩ

FIGURE 3 — TEST CIRCUIT

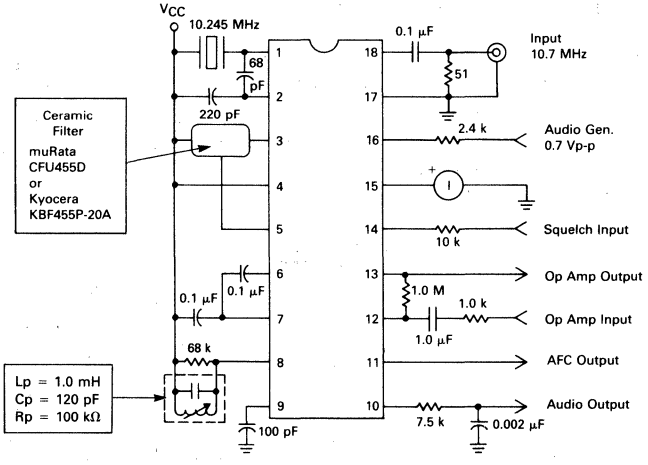


FIGURE 4 — MIXER VOLTAGE GAIN

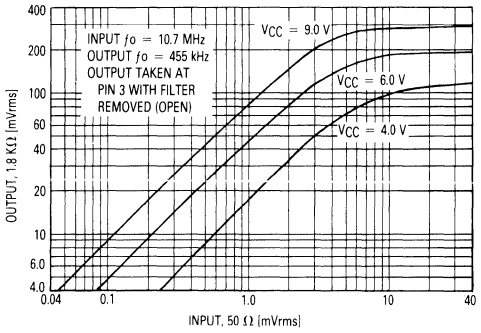


FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE

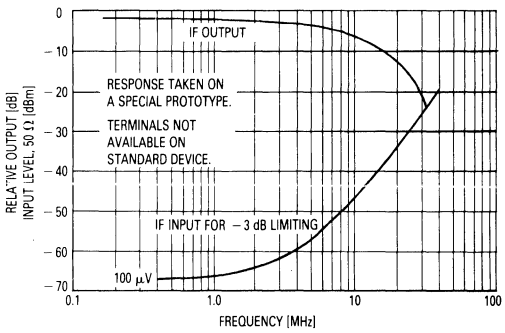


FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE

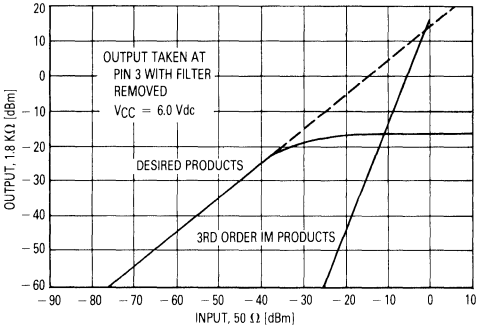


FIGURE 7 — DETECTOR AND AFC RESPONSES

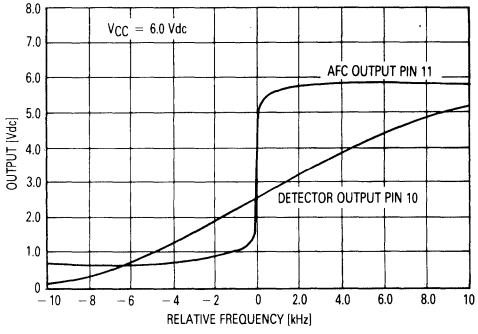


FIGURE 8 — RELATIVE MIXER GAIN

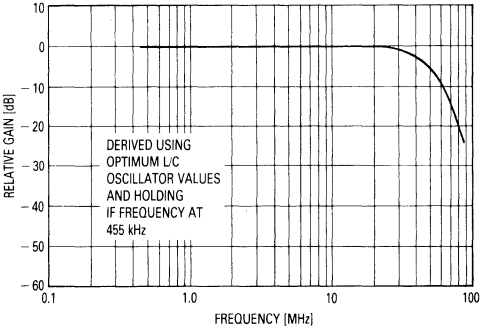


FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION

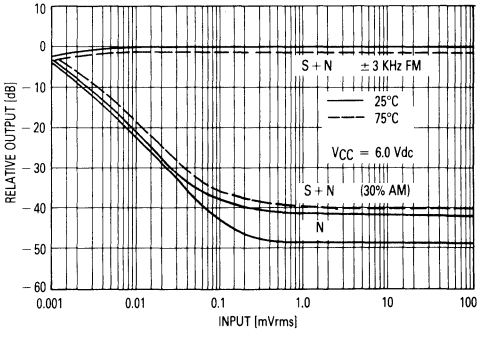


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FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

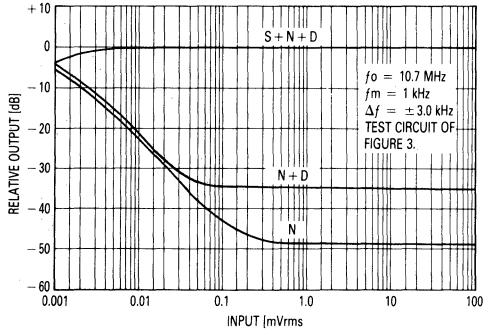


FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE

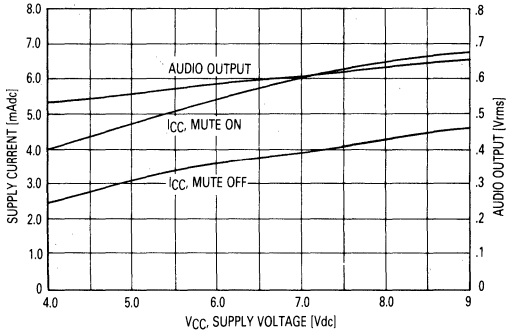


FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY

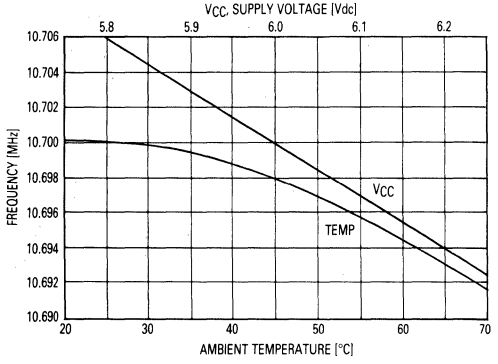


FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE

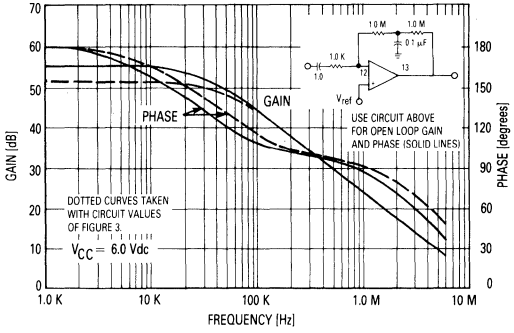


FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES

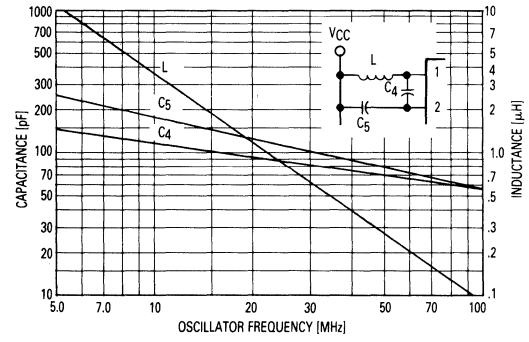
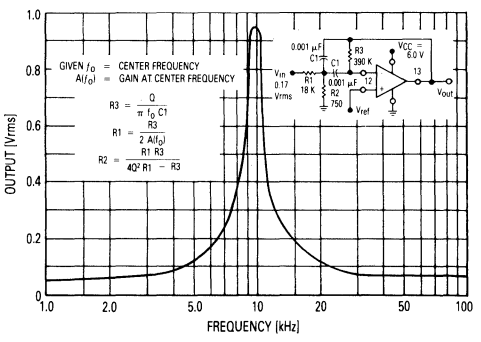


FIGURE 15 — THE OP AMP AS A BANDPASS FILTER



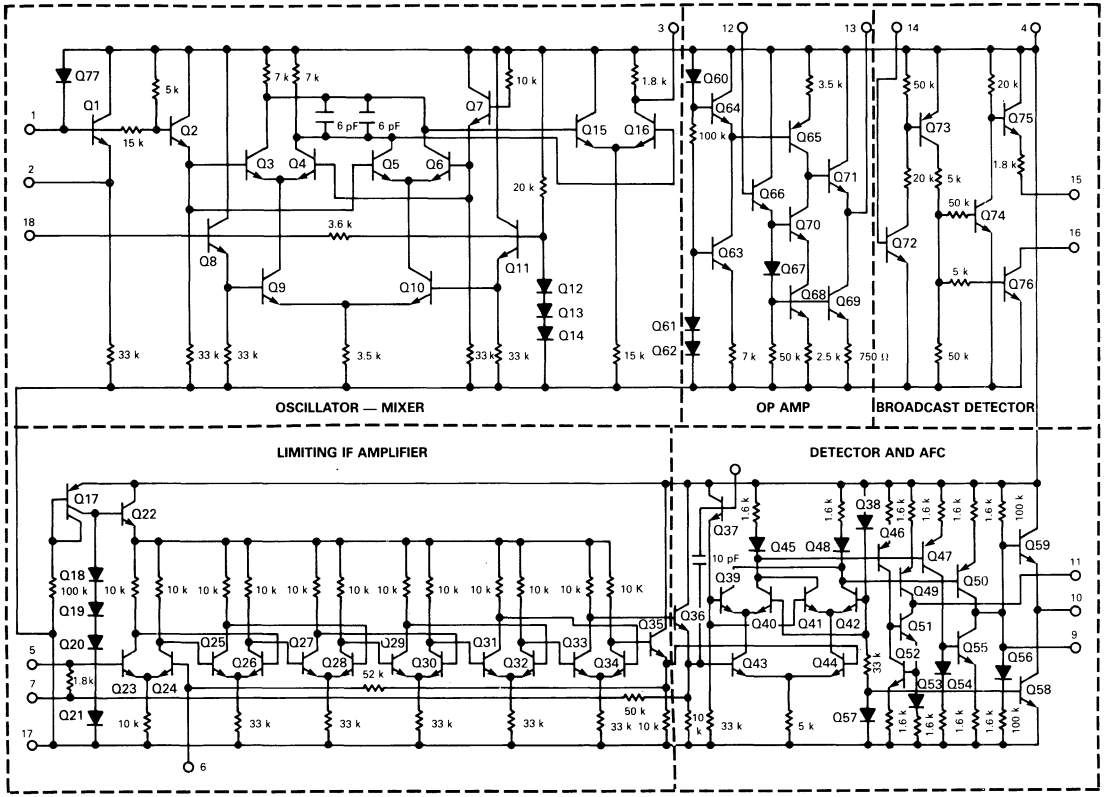


FIGURE 16 — CIRCUIT SCHEMATIC

2

CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximatley 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de-emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch-trigger circuit such that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open-circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high-impedance ground-reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MC3361

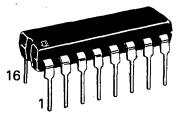
LOW POWER NARROW BAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3361 is designed for use in FM dual conversion communications equipment.

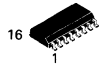
- Operates From 2.0 V to 8.0 V Supply
- Low Drain Current 4.2 mA Typ @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV Typ
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

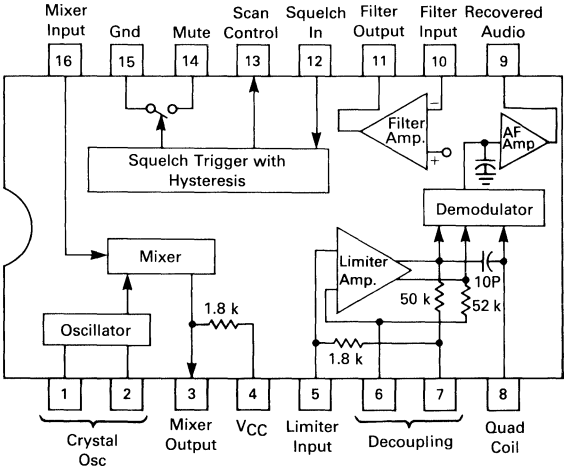


P SUFFIX
PLASTIC PACKAGE
CASE 648-08

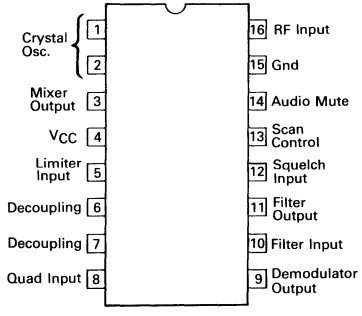


D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
SO-16

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



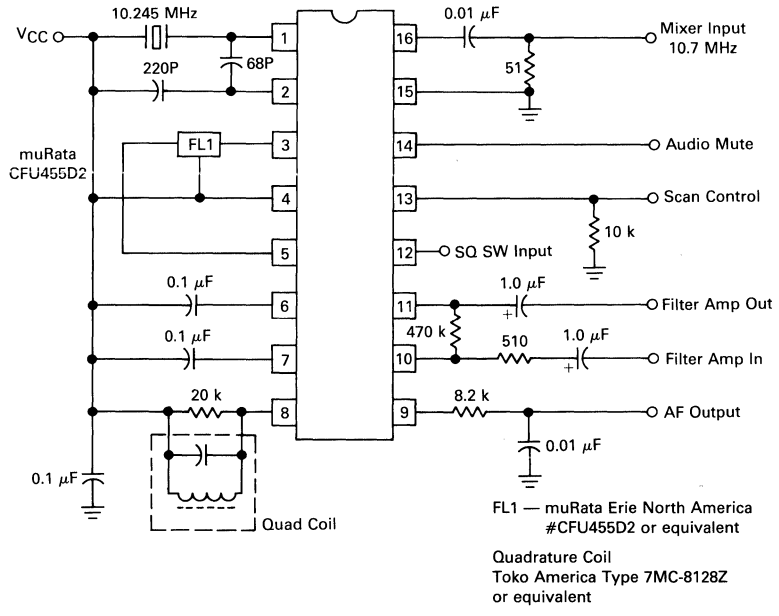
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage ($V_{CC} \geq$ 4.0 Volts)	16	V_{16}	1.0	Vrms
Mute Function	14	V_{14}	−0.5 to +5.0	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No signal)	4				mA
Squelch Off		—	4.2	7.0	
Squelch On		—	5.2	9.0	
Recovered Audio Output Voltage (V_{in} = 10 mVrms)	9	100	150	270	mVrms
Input Limiting Voltage (−3.0 dB Limiting)	16	—	2.0	6.0	μV
Total Harmonic Distortion	9	—	0.8	—	%
Recovered Output Voltage (No Input Signal)	9	60	150	—	mVrms
Drop Voltage AF Gain Loss	9	−8.0	−0.5	—	dB
Detector Output Impedance	—	—	450	—	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mVrms)	—	40	49	—	dB
Filter Output Voltage	11	—	1.7	—	Vdc
Mute Function Low	14	—	10	50	Ω
Mute Function High	14	1.0	10	—	MΩ
Scan Function Low (Mute Off) (V_{12} = 1.0 Vdc)	13	—	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	3.0	3.5	—	Vdc
Trigger Hysteresis	—	—	45	100	mV
Mixer Conversion Gain	3	—	28	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

FIGURE 2 — TEST CIRCUIT



FL1 — muRata Erie North America #CFU455D2 or equivalent

Quadrature Coil
Toko America Type 7MC-8128Z
or equivalent

FIGURE 3 — AUDIO OUTPUT, DISTORTION

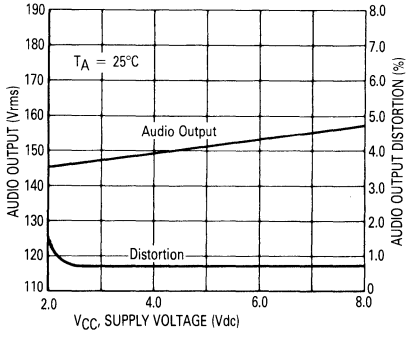


FIGURE 4 — AUDIO OUTPUT, DISTORTION

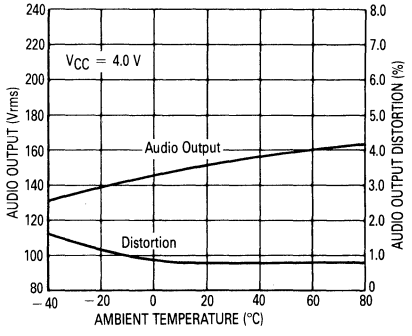


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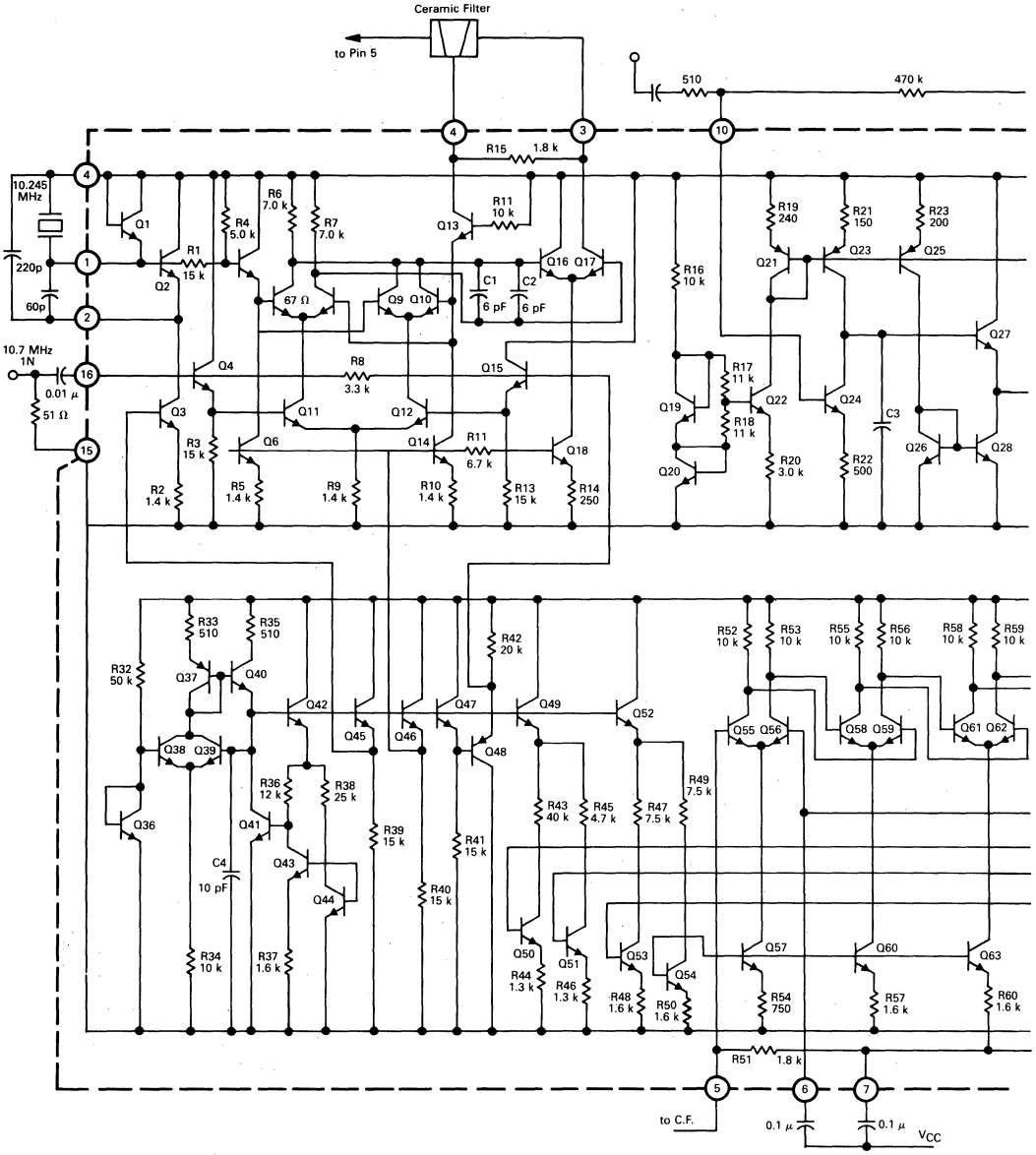
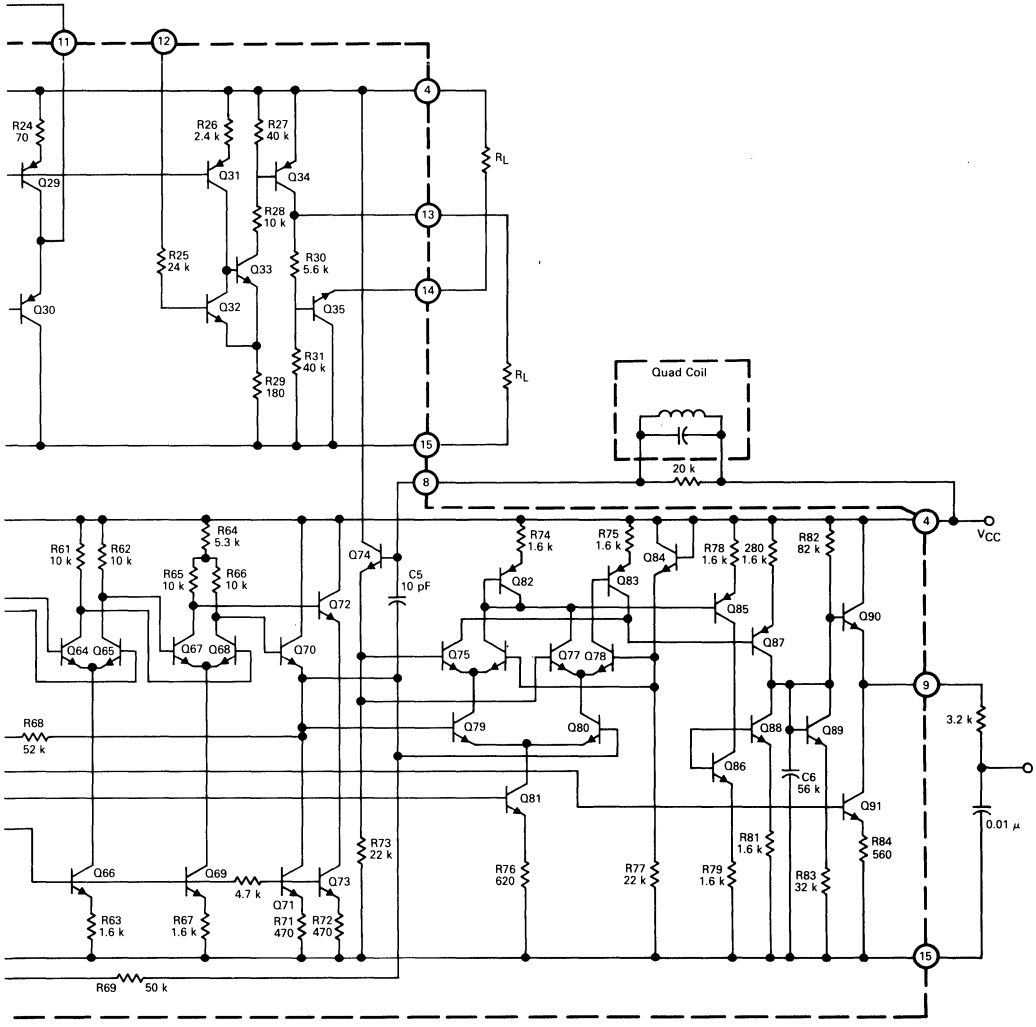
FIGURE 5 — LOW VOLTAGE LOW POWER
NARROW BAND FM IF

CIRCUIT SCHEMATIC




11
12
4
13
14
15
8
9
R24 70
R26 2.4 k
R27 40 k
R28 10 k
R25 24 k
R30 5.6 k
R29 180
R31 40 k
Q29
Q30
Q31
Q32
Q33
Q34
Q35
RL
RL
Quad Coil
20 k
VCC
R61 10 k
R62 10 k
R64 5.3 k
R65 10 k
R66 10 k
Q64 Q65
Q67 Q68
Q70
Q72
Q74
C5 10 pF
R74 1.6 k
R75 1.6 k
Q82
Q83
Q84
R78 1.6 k
280 1.6 k
R82 82 k
Q85
Q87
Q90
Q75
Q77 Q78
Q79
Q80
Q88
Q89
Q86
C6 56 k
Q81
Q91
R68 52 k
3.2 k
0.01 μ
R73 22 k
R76 620
R77 22 k
R81 1.6 k
R79 1.6 k
R83 32 k
R84 560
Q66
Q69
4.7 k
Q71
Q73
R63 1.6 k
R67 1.6 k
R71 470
R72 470
R69 50 k

2

FIGURE 6 — INPUT LIMITING VOLTAGE

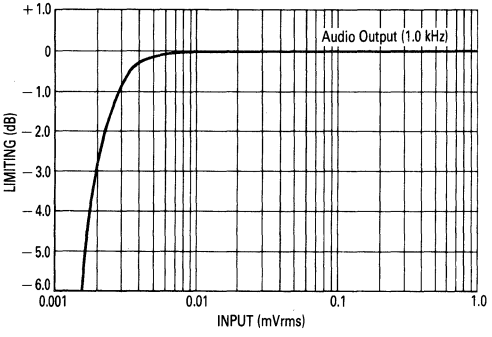


FIGURE 7 — OVERALL GAIN, NOISE, AND A.M. REJECTION

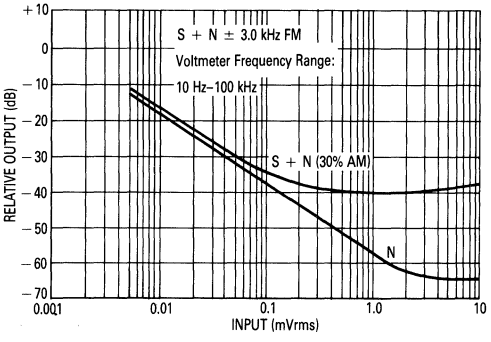


FIGURE 8 — FILTER AMP RESPONSE

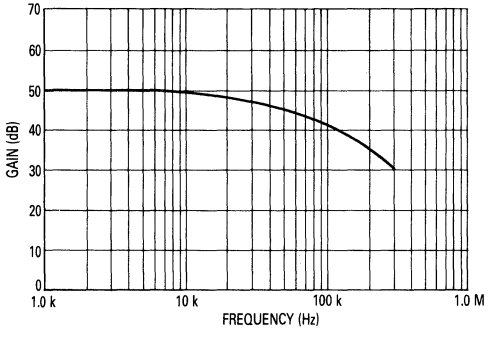


FIGURE 9 — FILTER AMP GAIN

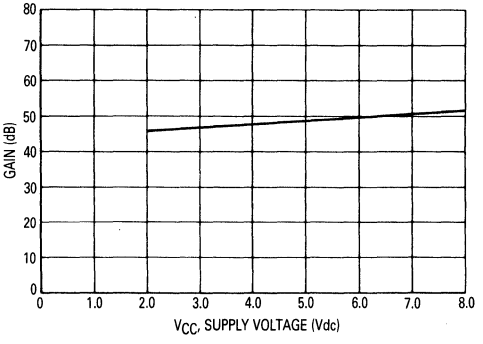


FIGURE 10 — SUPPLY CURRENT

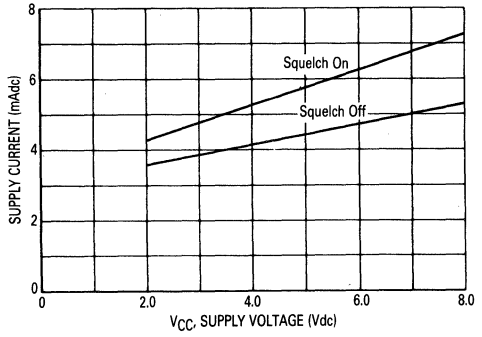
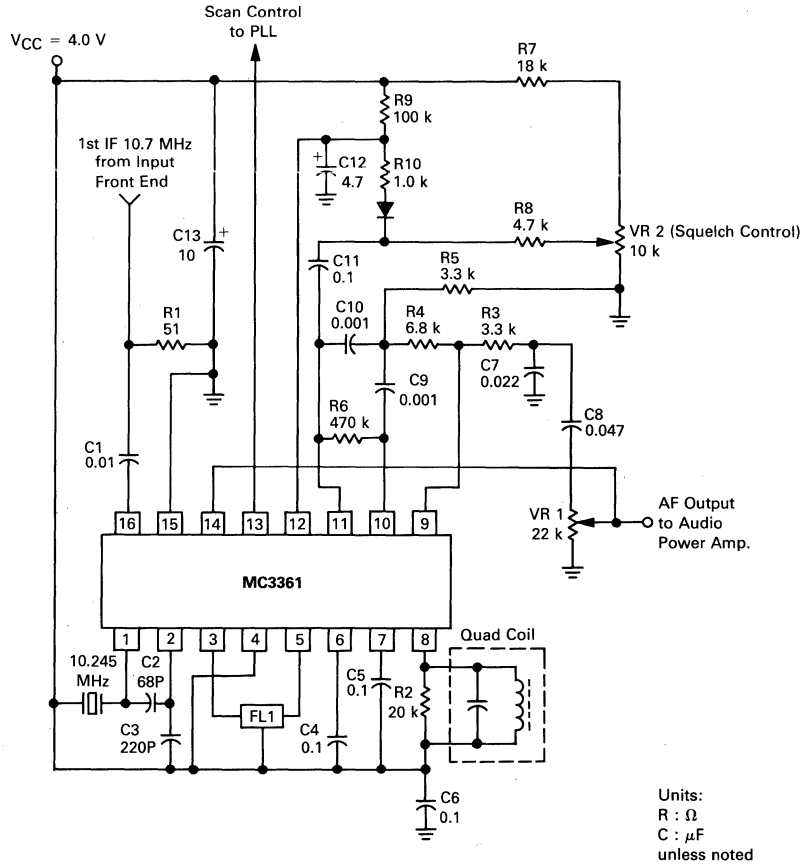


FIGURE 11 — TYPICAL APPLICATION



FL1 muRata Erie North America
Type CFU455D2 or
equivalent

Quadrature Coil
Toko America
Type 7MC-8128Z
or equivalent

MC3362

Advance Information

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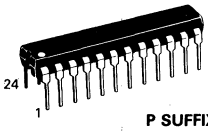
LOW POWER NARROWBAND FM RECEIVER

. . . includes dual FM conversion with oscillators, mixers, quadrature detector, and meter drive/carrier detect circuitry. The MC3362 also has buffered first and second local oscillator outputs and a comparator circuit for FSK detection.

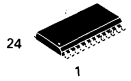
- Wide Input Bandwidth:
  - — 200 MHz using Internal Local Oscillator
  - — 450 MHz using External Local Oscillator
- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 7.0 Vdc
- Low Drain Current (3.6 mA (Typ) @ V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: Input 0.7 μV (Typ) for 12 dB SINAD
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology

LOW-POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724-03



DW SUFFIX
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CASE 751E-03
SO-24

FIGURE 1 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

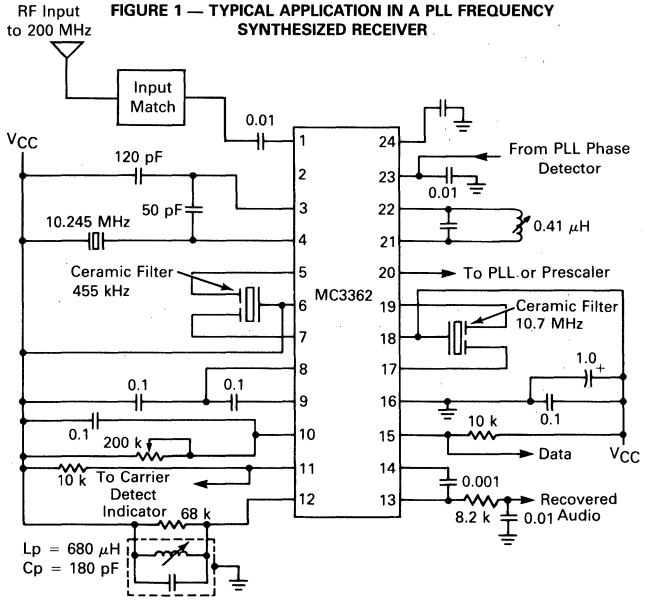
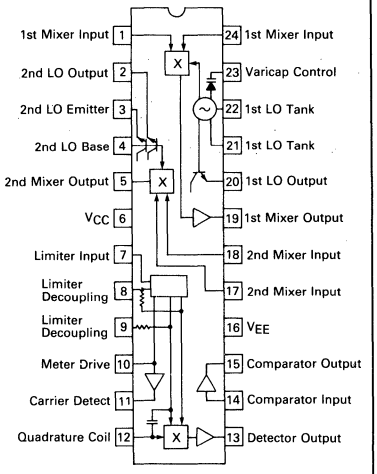


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice. MOSAIC is a trademark of Motorola.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	6	$V_{CC(max)}$	8.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V_{CC}	2.0 to 7.0	Vdc
Input Voltage ($V_{CC} \geq$ 5.0 Vdc)	1, 24	V_{1-24}	1.0	Vrms
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 3 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low — See Figure 5)	6	—	4.5	7.0	mA
Input for −3.0 dB Limiting	—	—	0.7	2.0	μVrms
Recovered Audio (RF signal level = 10 mV)	13	—	350	—	mVrms
Noise Output (RF signal level = 0 mV)	13	—	250	—	mVrms
Carrier Detect Threshold (below V_{CC})	10	—	0.64	—	Vdc
Meter Drive Slope	10	—	100	—	nA/dB
Input for 20 dB (S+N)/N (See Figure 7)	—	—	0.7	—	μVrms
First Mixer 3rd Order Intercept (Input)	—	—	−22	—	dBm
First Mixer Input Resistance (Rp)	—	—	690	—	Ω
First Mixer Input Capacitance (Cp)	—	—	7.2	—	pF
First Mixer Conversion Voltage Gain	—	—	18	—	dB
Second Mixer Conversion Voltage Gain	—	—	21	—	dB
Detector Output Resistance	13	—	1.4	—	kΩ

FIGURE 3 — TEST CIRCUIT

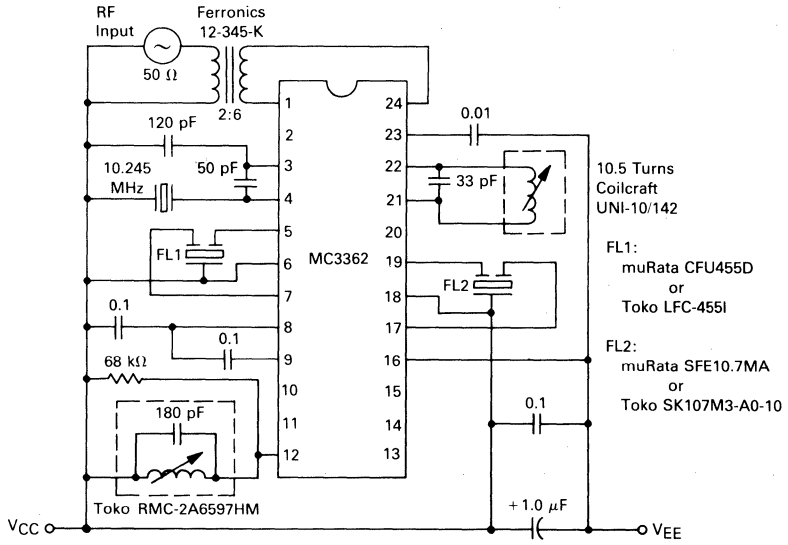


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FIGURE 4 — I_{METER} versus INPUT

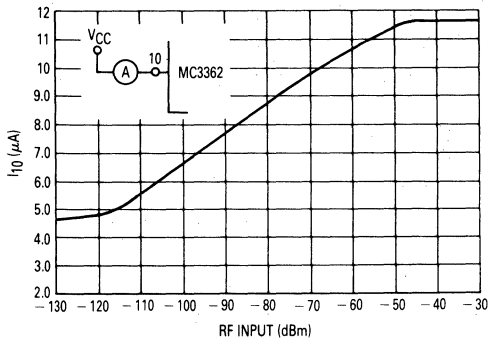


FIGURE 5 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

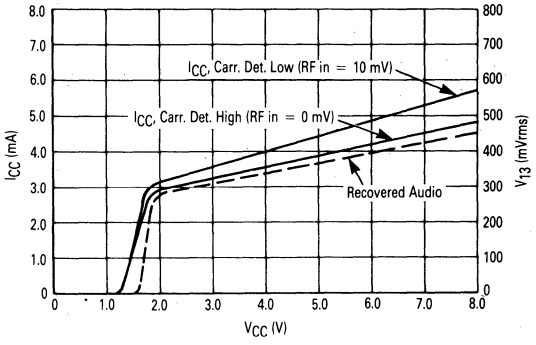


FIGURE 6 — SIGNAL LEVELS

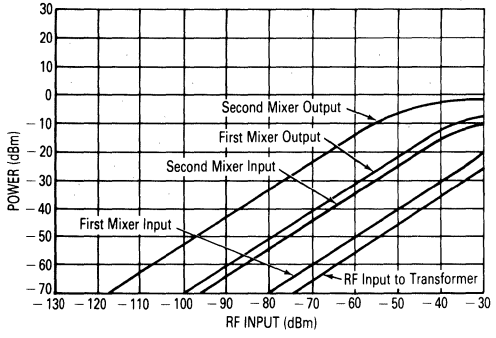


FIGURE 7 — S+N, N, AMR versus INPUT

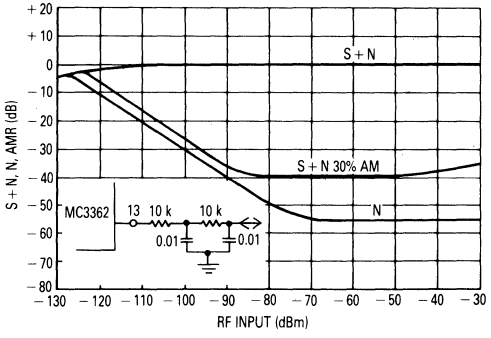


FIGURE 8 — 1ST MIXER 3RD ORDER INTERMODULATION

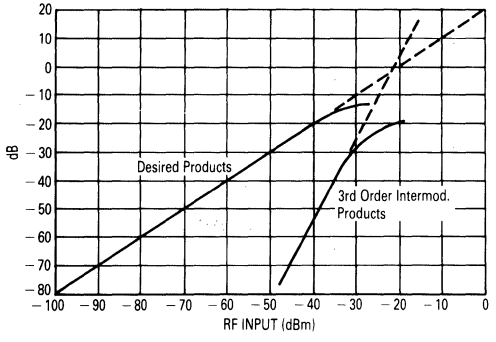
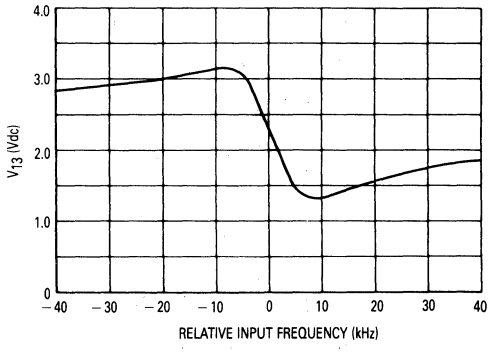


FIGURE 9 — DETECTOR OUTPUT versus FREQUENCY



CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator can be run using a free-running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S+N)/N is 0.7 μV using the two-pole post-detection filter pictured.

*If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}.

The 455 kHz IF is typically filtered using a ceramic bandpass filter then fed into the limiter input pin. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC}. A 68 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the circuit of Figure 1. Hysteresis is available by connecting a high-valued resistor from Pin 15 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} \simeq 0.64\ \text{Vdc} / I_{10}$$

Hysteresis is available by connecting a high-valued resistor R_H between Pins 10 and 11. The formula is:

$$\text{Hyst.} = V_{CC}/(R_H \times 10^{-7})\ \text{dB}$$

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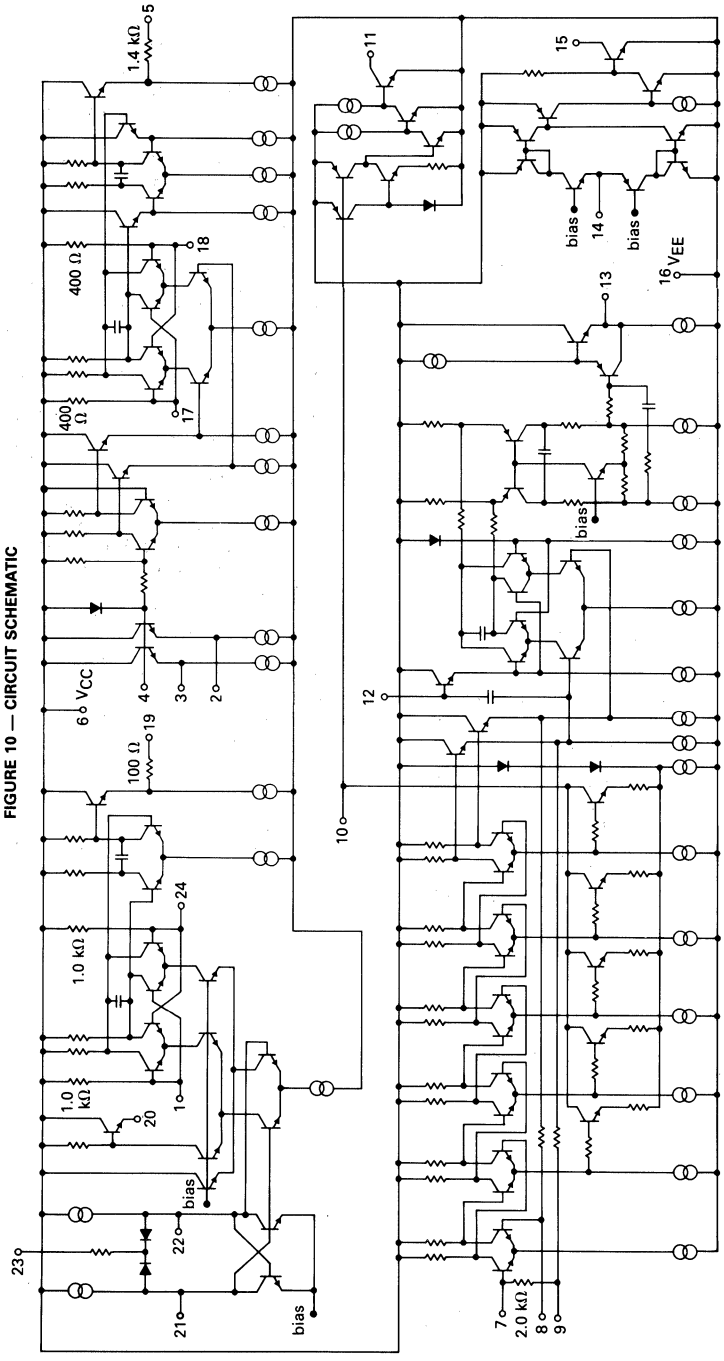


FIGURE 10 — CIRCUIT SCHEMATIC

MC3363

Advance Information

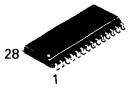
LOW POWER DUAL CONVERSION FM RECEIVER

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth — 200 MHz Using Internal Local Oscillator
  — 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: V_{CC} = 2.0 V to 7.0 V
- Low Drain Current: I_{CC} = 3.6 mA (Typ) at V_{CC} = 3.0 V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input 0.3 μV (Typ) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology
- See AN980 For Additional Design Information

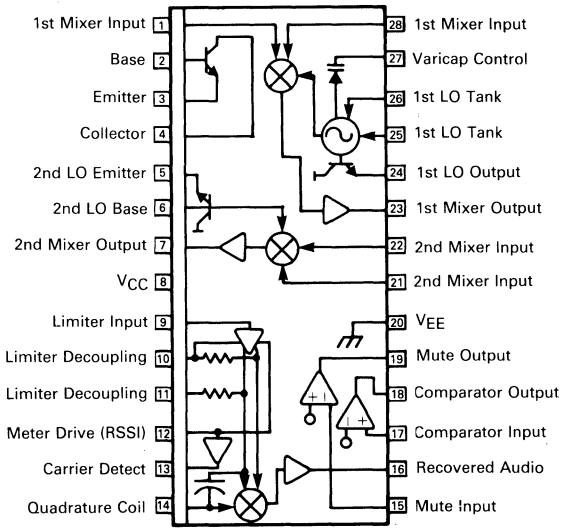
LOW POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-03
SO-28

FIGURE 1 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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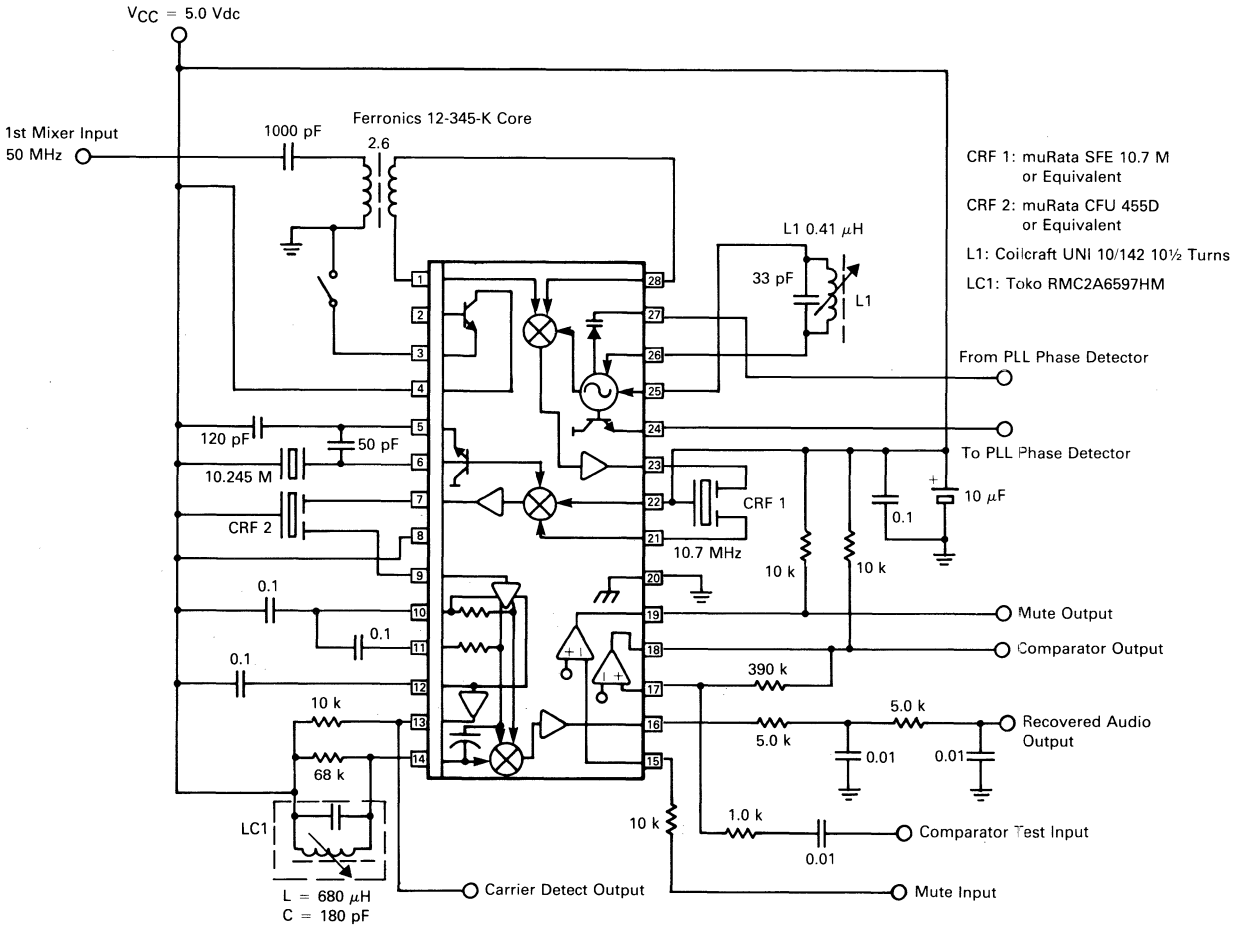
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	8.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 7.0	Vdc
Input Voltage (V_{CC} = 5.0 Vdc)	1, 28	V_{1-28}	1.0	Vrms
Mute Output Voltage	19	V_{19}	−0.7 to 8.0	Vpk
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = ±3.0 kHz, T_A = 25°C, Mod 1.0 kHz, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (Carrier Detect Low)	8	—	4.5	8.0	mA
−3.0 dB Limiting Sensitivity (RF Amplifier Not Used)	—	—	0.7	2.0	μVrms
20 dB S/N Sensitivity (RF Amplifier Not Used)	—	—	1.0	—	μVrms
1st Mixer Input Resistance (Parallel — Rp)	1, 28	—	690	—	Ohm
1st Mixer Input Capacitance (Parallel — Cp)	1, 28	—	7.2	—	pF
1st Mixer Conversion Voltage Gain (A_{vc1}, Open Circuit)	—	—	18	—	dB
2nd Mixer Conversion Voltage Gain (A_{vc2}, Open Circuit)	—	—	21	—	dB
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	—	10	—	μVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	—	100	—	μVrms
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mAdc
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	—	mVrms
Noise Output Level (RF Signal = 0 mV)	16	—	70	—	mVrms
THD of Recovered Audio (RF Signal = 1.0 mV)	16	—	2%	—	%
Detector Output Impedance	16	—	400	—	Ohm
Data (Comparator) Output Voltage — High — Low	18 18	— 0.1	— 0.1	V_{CC} —	Vdc Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance — High — Low	19 19	— —	10 25	— —	Mohm Ohm

FIGURE 2 — TEST CIRCUIT



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CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer's transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to V_{CC}.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to V_{CC}. A 68 kOhm shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kOhm are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a preset level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and V_{CC}. Values between 80–130 kOhms are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

$$\text{Hyst} = V_{CC}/(\text{Rh} \times 10^{-7})\ \text{dB}$$

The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similar to that used with the MC3357/MC3359/MC3361 FM I.F.'s. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of <0.3 μV for 12 dB SINAD.

FIGURE 3 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

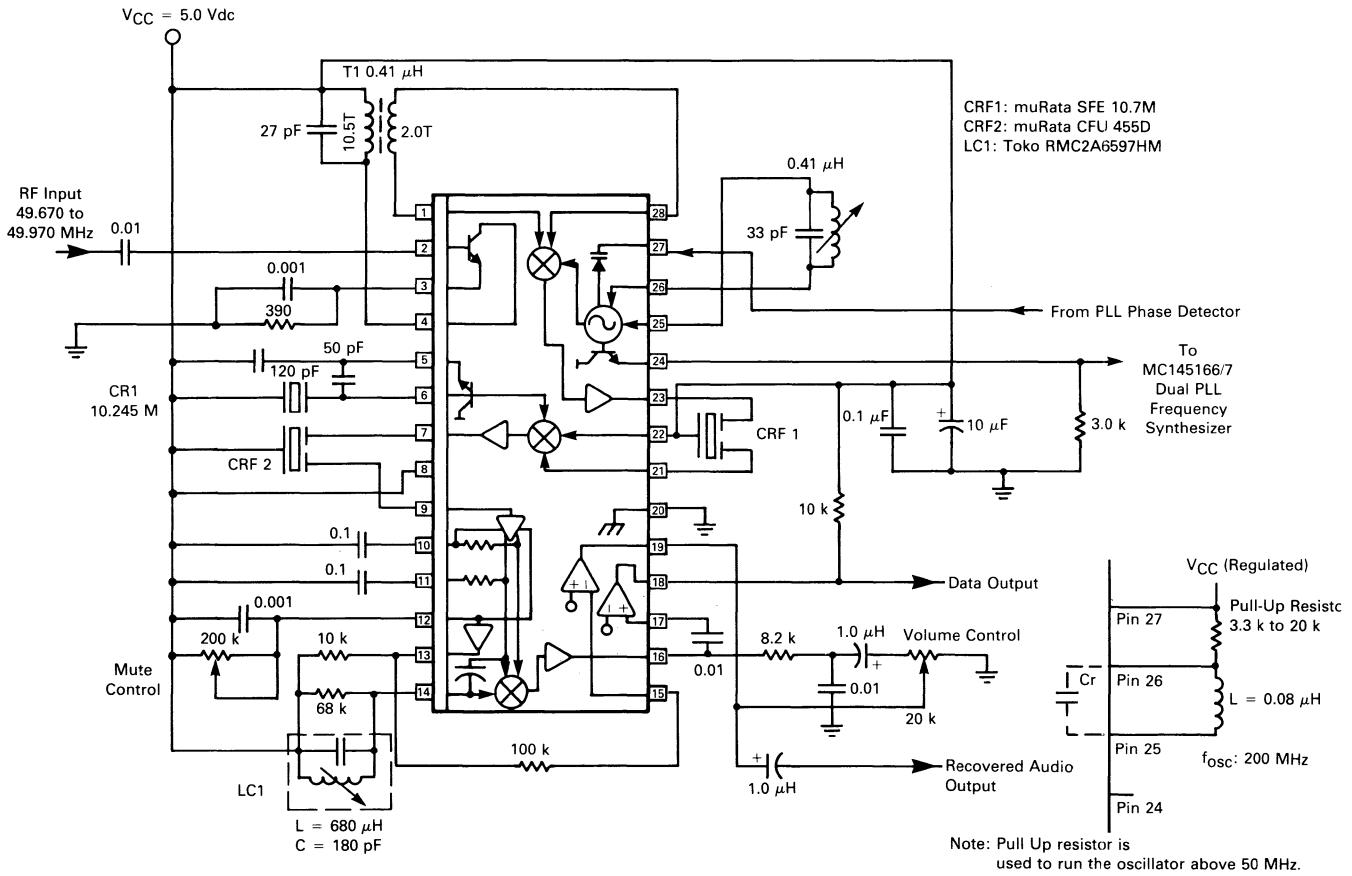
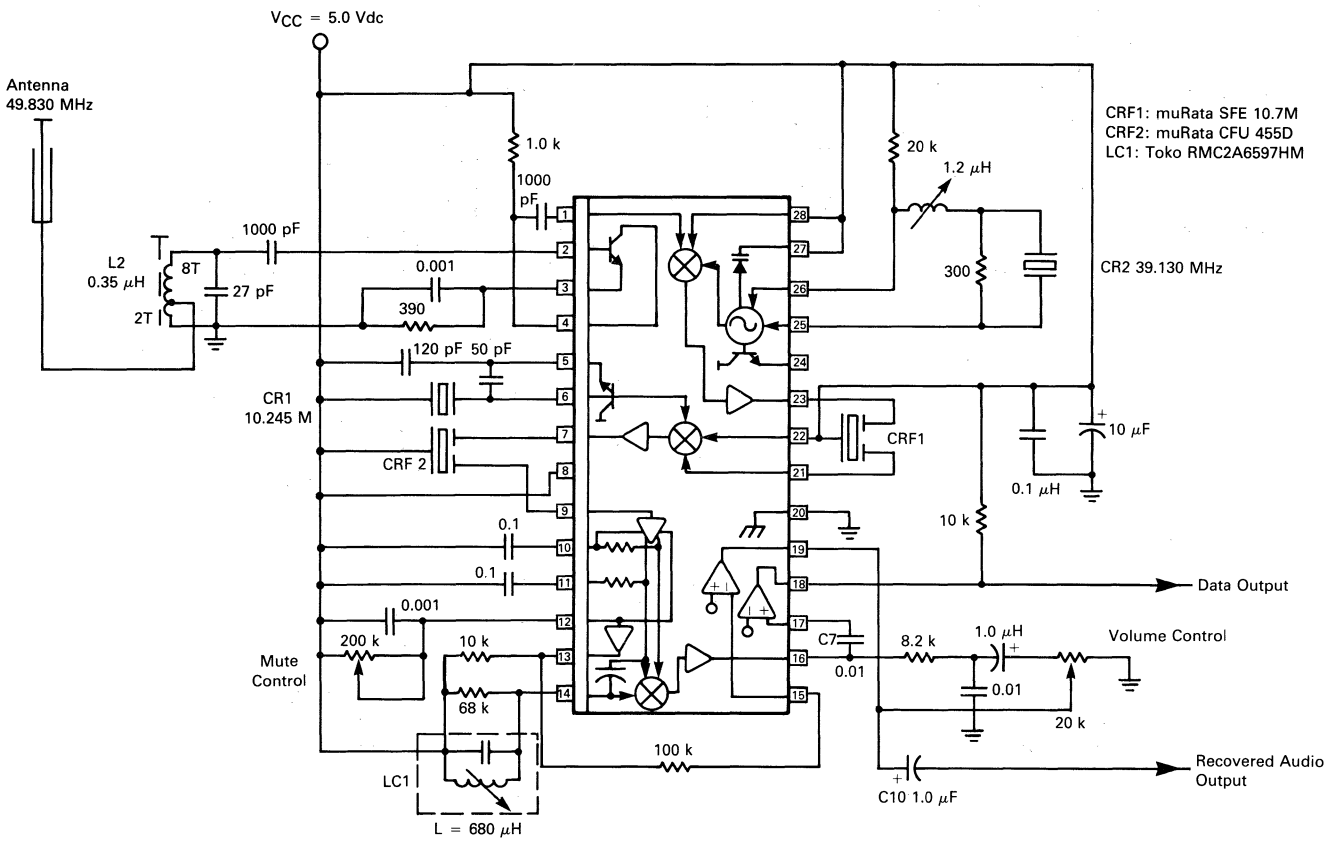


FIGURE 4 — SINGLE CHANNEL CRYSTAL CONTROLLED FM RECEIVER



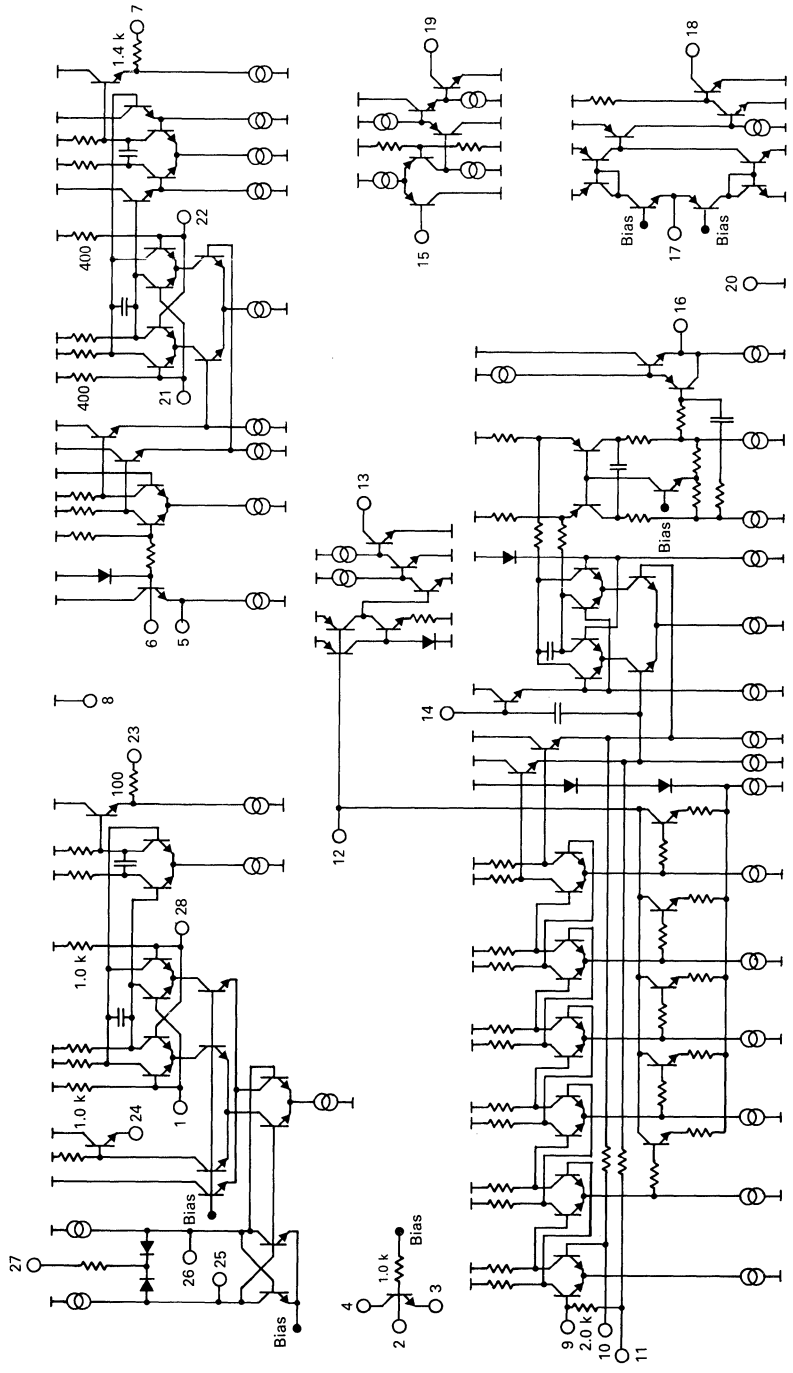


FIGURE 5 — CIRCUIT SCHEMATIC

MC3367

Product Preview

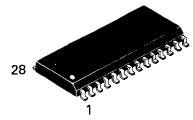
LOW VOLTAGE FM NARROWBAND RECEIVER

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3367 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3367 also includes an on-board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down "sleep mode," two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception.

- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: Input Limiting Voltage (−3.0 dB) = 0.2 μVrms
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer with Nominal Gain A_V = 4.0
- Data Buffer with Nominal Gain A_V = 3.2
- Comparator with > 25 kHz (50 kbaud) Capability
- Standard 28-Lead Surface Mount (SOIC) Package

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-03
SO-28

PIN CONNECTIONS

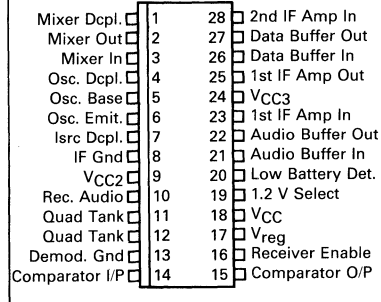
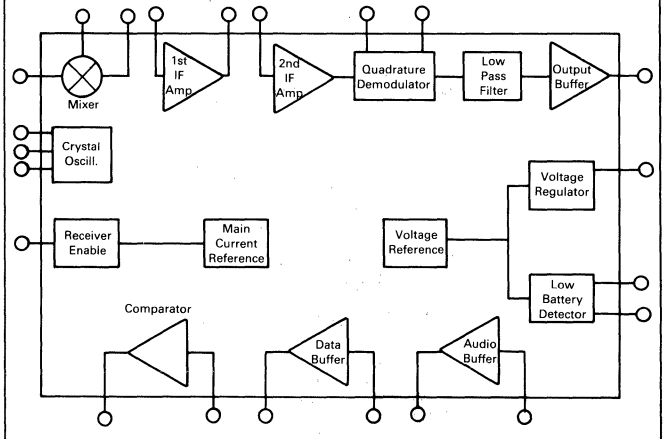


FIGURE 1 — BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to Pin 12; T_A = 25°C)

Parameter	Pin	Value	Units
Supply Voltage	18	5.0	Vdc
RF Input Signal	3	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	14	1.0	Vrms
Junction Temperature	—	150	°C
Storage Temperature	—	−65 to +150	°C

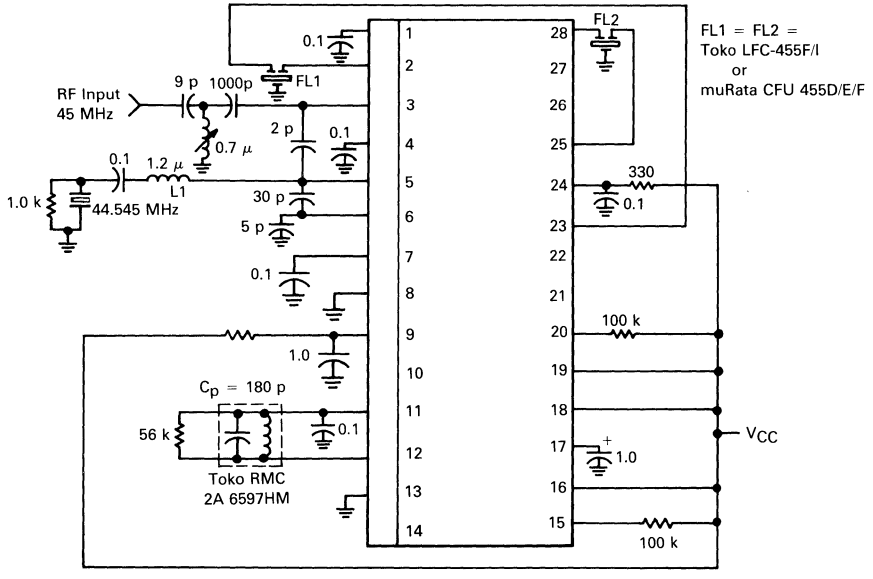
Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Units
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	16	0 or V_{CC}	Vdc
1.2 V Select Voltage	19	V_{CC}	Vdc
RF Input Signal	3	0.001 to 100	mVrms
RF Input Frequency	3	0 to 75	MHz
Intermediate Frequency (IF)	—	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	14	10 to 300	mVrms
Ambient Temperature	—	0 to 70	°C

FIGURE 2 — TEST CIRCUIT

(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)



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ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 45 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
OVERALL MC3367 PERFORMANCE					
Drain Current — Pin 15 = V_{CC}	—	—	1.4	3.0	mA
— Pin 15 = 0 Vdc	—	—	0.5	—	μA
Recovered Audio (RF Input = 10 mV)	10	—	13	—	mVrms
Noise Output (RF Input = 0 mV)	10	—	4.5	—	mVrms
Input for −3.0 dB Limiting	3	—	0.2	—	μVrms
MIXER					
Mixer Input Resistance (Rp)	3	—	3.0	—	kΩ
Mixer Input Capacitance (Cp)	3	—	9.0	—	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	—	—	25	—	dB
AUDIO BUFFER					
Voltage Gain	—	—	4.0	—	V/V
Input Resistance	21	—	125	—	kΩ
Maximum Input for Undistorted Output	21	—	70	—	mVrms
Maximum Output Swing	22	—	800	—	mVpp
Output Resistance	22	—	680	—	Ω
DATA BUFFER					
Voltage Gain	—	—	3.2	—	V/V
Input Resistance	26	—	8.0	—	MΩ
Maximum Input for Undistorted Output	26	—	70	—	mVrms
Maximum Output Swing	27	—	600	—	mVpp
Output Resistance	27	—	1.5	—	kΩ
COMPARATOR					
Minimum Input for Triggering	14	—	7.0	—	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	14	—	25	—	kHZ
Rise Time (10–90%; R_L = 100 kΩ)	15	—	5.0	—	μs
Fall Time (90–10%; R_L = 100 kΩ)	15	—	0.4	—	μs
LOW BATTERY DETECTOR					
Low Battery Trip Point	18	—	1.09	—	Vdc
Low Battery Output — V_{CC} = 0.9 V	20	—	0.2	—	Vdc
— V_{CC} = 1.3 V	20	—	V_{CC}	—	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 6)	17	—	0.95	—	Vdc
Source Capability	17	—	—	3.0	mA

FIGURE 3 — RECOVERED AUDIO versus SUPPLY

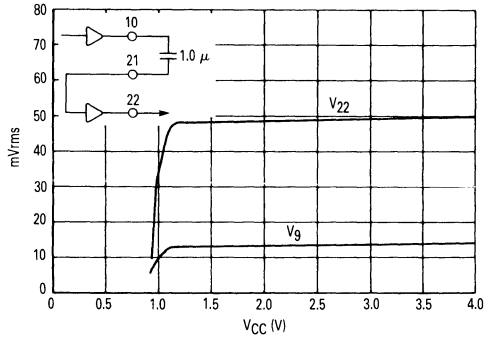


FIGURE 4 — DRAIN versus SUPPLY

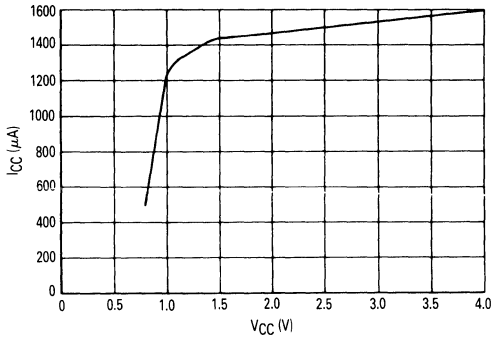


FIGURE 5 — S+N, N versus INPUT

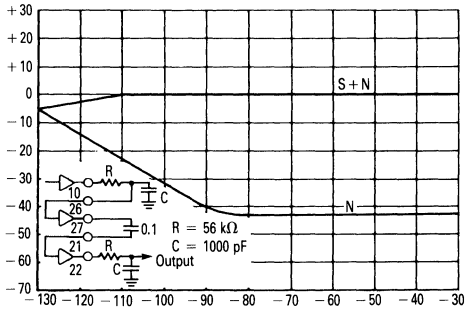
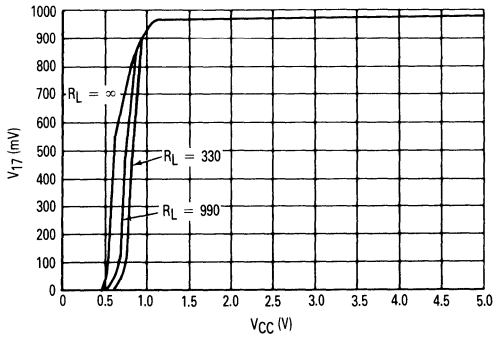


FIGURE 6 — V_{REG} versus SUPPLY



CIRCUIT DESCRIPTION

The MC3367 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts the RF or IF frequency to 455 kHz. This signal is then filtered by a 455 ceramic filter and applied to the first intermediate frequency (IF) amplifier input. This amplifier amplifies the 455 kHz IF before it is filtered by a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Audio is recovered by a conventional quadrature detector.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3367 is an FM utility receiver to be used for voice and/or narrowband data reception, especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

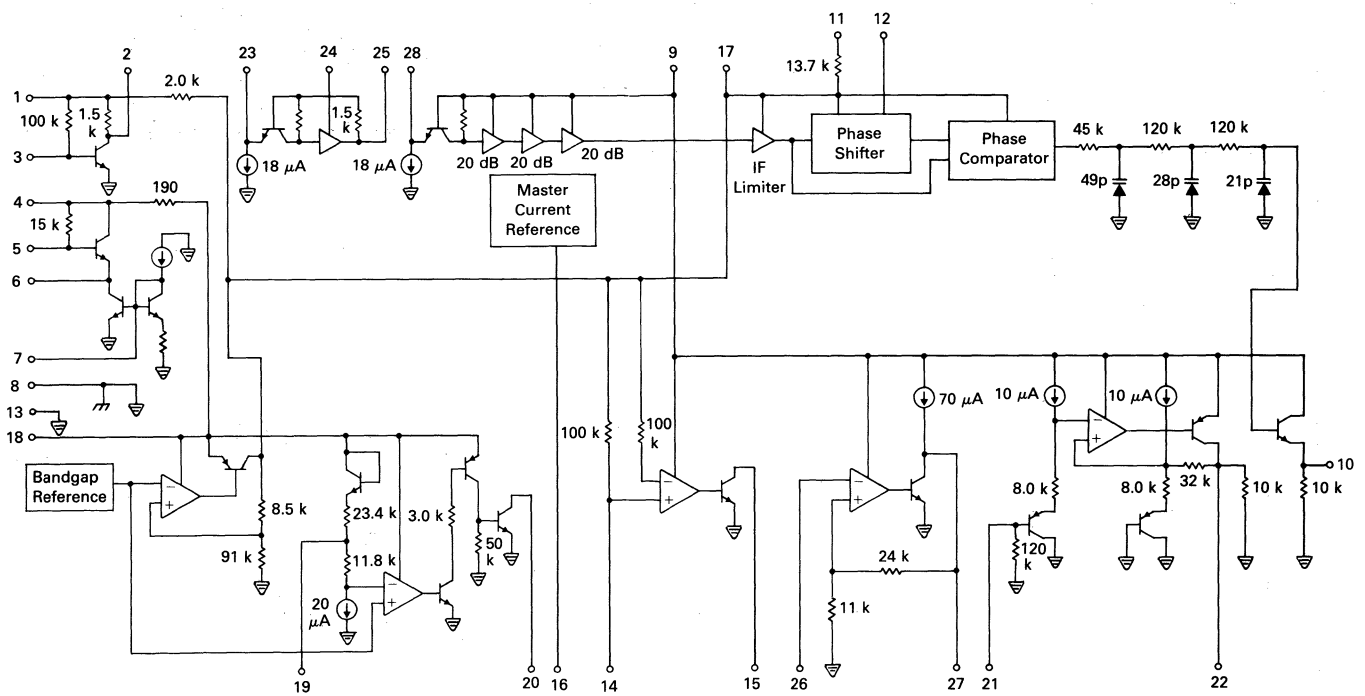
The MC3367 can be used as a high performance FM IF for use in low power dual conversion receivers. Because of the MC3367's extremely good sensitivity (0.6 μV for 20 dB (S+N)/N, see Figure 5), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference.

The oscillator is a Colpitts type which can be run as an LC oscillator or under crystal control. The crystal in Figure 2 is a 3rd overtone series mode type, and the 1.2 μH coil (L1) and 1.0 kΩ resistor are needed to ensure proper operation. For fundamental mode crystals, the inductor L1 can be omitted.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 2. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally as with the MC3359 and the MC3361.

FIGURE 7 — CIRCUIT SCHEMATIC



A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 11) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor shown in Figure 2 determines the peak separation (and thus the detector bandwidth) of the detector. Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a non-inverting amplifier with a nominal voltage gain of 3.2 V/V. This buffer needs its dc bias (approx. 250 mV) provided externally or else debiasing will occur. A single-pole RC filter as shown in Figure 5 connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post-detection filtering. The buffer can also be used as an active filter.

The audio buffer is a non-inverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self-biasing so its input should be ac coupled. The two buffers, when used as active filters, can be used together to allow simultaneous audio and very low-speed data reception. Another possible configuration is to receive audio only and include a noise-triggered squelch.

The comparator is a non-inverting type with an open collector output. Typically the pull-up resistor used between Pin 15 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. This circuit is self-biasing, so its input should be ac coupled.

The regulator is a 0.95 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3367.

All three V_{CC}'s on the MC3367 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 2. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3367 supply voltage drops below 1.1 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3367 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 16 is a receiver enable, which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

MC3417, MC3517
MC3418, MC3518

Specifications and Applications Information

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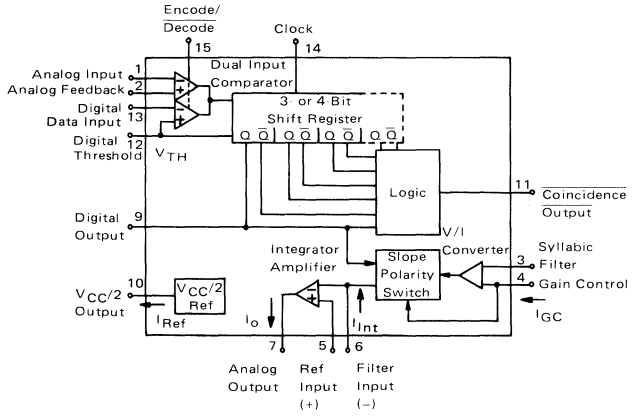
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

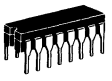
- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

CVSD BLOCK DIAGRAM

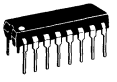


CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT



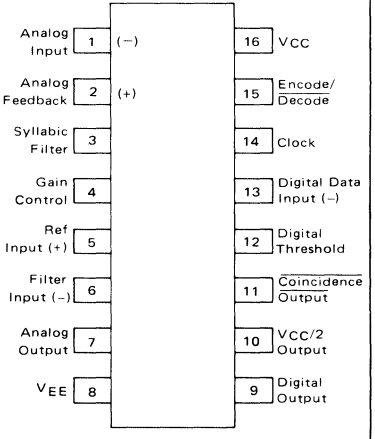
L SUFFIX
CERAMIC PACKAGE
CASE 620-10



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

DW SUFFIX
PLASTIC PACKAGE
CASE 751G-01
SO-16L

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Temperature Range
MC3417L	Ceramic DIP	0°C to +70°C
MC3418DW	Plastic SOIC	0°C to +70°C
MC3418L	Ceramic DIP	0°C to +70°C
MC3418P	Plastic DIP	0°C to +70°C
MC3517L	Ceramic DIP	−55°C to +125°C
MC3518L	Ceramic DIP	−55°C to +125°C

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to +70°C for MC3417/18, T_A = −55°C to +125°C for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (@ Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V, All except MC3418P,DW)		—	3.7	5.0	—	3.7	5.0	
(V_{CC} = 5.0 V, MC3418P,DW)		—	—	—	—	3.7	5.5	
(V_{CC} = 15 V, All except MC3418P,DW)		—	6.0	10	—	6.0	10	
(V_{CC} = 15 V, MC3418P,DW)		—	—	—	—	6.0	11	
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	—	3.0	0.002	—	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	—	V_{CC} − 1.3	1.3	—	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA)	V_O	1.3	—	V_{CC} − 1.3	1.3	—	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							μA
Analog Input (I1)		—	0.5	1.5	—	0.25	1.0	
Analog Feedback (I2)		—	0.5	1.5	—	0.25	1.0	
Syllabic Filter Input (I3)		—	0.06	0.5	—	0.06	0.3	
Reference Input (I5)		—	−0.06	−0.5	—	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							μA
Analog Input/Analog Feedback |I1 − I2| — Figure 3		—	0.15	0.6	—	0.05	0.4	
Integrator Amplifier |I5 − I6| — Figure 4		—	0.02	0.2	—	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	—	2.0	6.0	—	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	—	0.1	0.3	—	
Integrator Amplifier, 0 to ±5.0 mA Load		1.0	10	—	1.0	10	—	
Propagation Delay Times (Note 1)								μs
Clock Trigger to Digital Output	t_{PLH}	—	1.0	2.5	—	1.0	2.5	
(C_L = 25 pF to Gnd)	t_{PHL}	—	0.8	2.5	—	0.8	2.5	
Clock Trigger to Coincidence Output	t_{PLH}	—	1.0	3.0	—	1.0	3.0	
(C_L = 25 pF to Gnd) (R_L = 4.0 kΩ to V_{CC})	t_{PHL}	—	0.8	2.0	—	0.8	2.0	
Coincidence Output Voltage — Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	—	0.12	0.25	—	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State (V_{OH} = 15 V, 0°C ≤ T_A ≤ 70°C)	$I_{OH(Con)}$	—	0.01	0.5	—	0.01	0.5	μA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	—	$V_{CC}-2.0$	+1.2	—	$V_{CC}-2.0$	Vdc
Digital Threshold Input Current ($1.2\ V \leq V_{th} \leq V_{CC} - 2.0\ V$)	$I_{I(th)}$							μA
(V_{IL} applied to Pins 13, 14 and 15)		—	—	5.0	—	—	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		—	−10	−50	—	−10	−50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	—	—	±5.0	—	—	mA
$V_{CC}/2$ Generator Maximum Output Current (Source only)	I_{Ref}	+10	—	—	+10	—	—	mA
$V_{CC}/2$ Generator Output Impedance (0 to +10 mA)	z_{Ref}	—	3.0	6.0	—	3.0	6.0	Ω
$V_{CC}/2$ Generator Tolerance ($4.75\ V \leq V_{CC} \leq 16.5\ V$)	ϵ_r	—	—	±3.5	—	—	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	—	$V_{th}-0.4$	Gnd	—	$V_{th}-0.4$	
High Logic State	V_{IH}	$V_{th}+0.4$	—	18	$V_{th}+0.4$	—	18	
Dynamic Total Loop Offset Voltage (Note 2) — Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12 μA, V_{CC} = 12 V								
T_A = 25°C (All except 3418P,DW)		—	—	—	—	±0.5	±1.5	
(MC3418P,DW)		—	—	—	—	±0.5	±3.0	
$0°C \leq T_A \leq +70°C$ (MC3417/18L)		—	—	—	—	±0.75	±2.3	
(MC3418P,DW)		—	—	—	—	±0.75	±3.8	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	—	—	—	±1.5	±4.0	
I_{GC} = 33 μA, V_{CC} = 12 V								
T_A = 25°C		—	±2.5	±5.0	—	—	—	
$0°C \leq T_A \leq +70°C$ (MC3417/18)		—	±3.0	±7.5	—	—	—	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	±4.5	±10	—	—	—	
I_{GC} = 12 μA, V_{CC} = 5.0 V								
T_A = 25°C (All except MC3418P,DW)		—	—	—	—	±1.0	±2.0	
(MC3418P,DW)		—	—	—	—	±1.0	±3.5	
$0°C \leq T_A \leq +70°C$ (MC3417/18L)		—	—	—	—	±1.3	±2.8	
(MC3418P,DW)		—	—	—	—	±1.3	±4.3	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	—	—	—	±2.5	±5.0	
I_{GC} = 33 μA, V_{CC} = 5.0 V								
T_A = 25°C		—	±4.0	±6.0	—	—	—	
$0°C \leq T_A \leq +70°C$ (MC3417/18)		—	±4.5	±8.0	—	—	—	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	±5.5	±10	—	—	—	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{OH} = −0.35 mA)	V_{OH}	$V_{CC}-1.0$	$V_{CC}-0.2$	—	$V_{CC}-1.0$	$V_{CC}-0.2$	—	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	—	V_{CC}	+3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int}\rvert$							
(I_{GC} = 12 μA)		8.0	10	12	8.0	10	12	μA
(I_{GC} = 1.5 mA) (All except 3418P,DW)		1.45	1.5	1.55	1.45	1.5	1.55	mA
(MC3418P,DW)		—	—	—	1.42	1.5	1.58	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$							mV
(All except MC3418P,DW)		—	±100	±250	—	±100	±250	
(MC3418P,DW)		—	—	—	—	±100	±280	
Input Current — High Logic State (V_{IH} = 18 V)	I_{IH}							μA
Digital Data Input		—	—	+5.0	—	—	+5.0	
Clock Input		—	—	+5.0	—	—	+5.0	
Encode/$\overline{\text{Decode}}$ Input		—	—	+5.0	—	—	+5.0	
Input Current — Low Logic State (V_{IL} = 0 V)	I_{IL}							μA
Digital Data Input		—	—	−10	—	—	−10	
Clock Input		—	—	−360	—	—	−360	
Encode/$\overline{\text{Decode}}$ Input		—	—	−36	—	—	−36	
Clock Input, V_{IL} = 0.4 V		—	—	−72	—	—	−72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16 kHz. For the MC3418/MC3518, the clock frequency is 32 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the noninverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ on Pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6.0 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V – I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should always be between 8.0 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6.0 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and non-inverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6.0 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor.

2

If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3.0 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4.0 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 — Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 — V_{CC}

The power supply range is from 4.75 to 16.5 volts between Pin V_{CC} and V_{EE}.

FIGURE 1 — POWER SUPPLY CURRENT

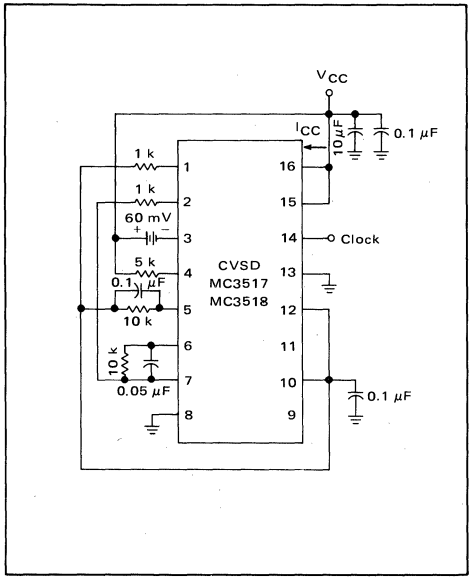
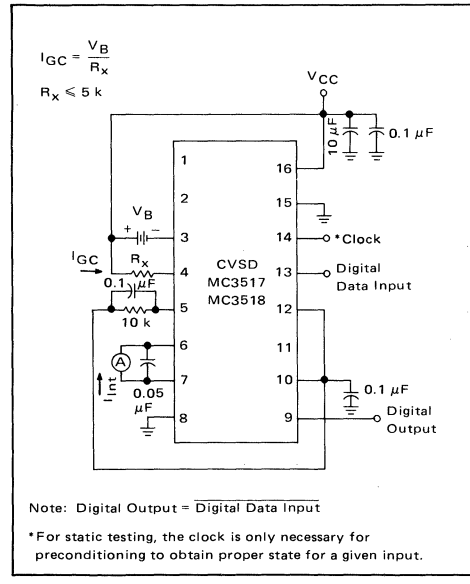


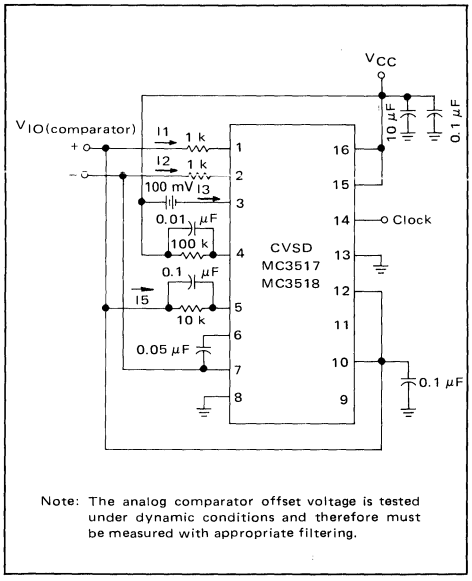
FIGURE 2 – I_{GCR}, GAIN CONTROL RANGE and I_{Int} – INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

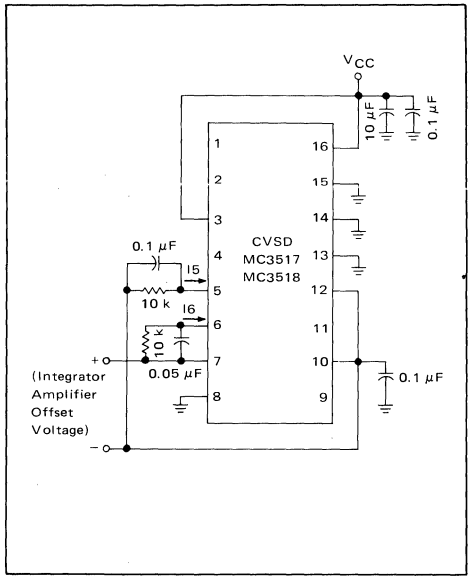
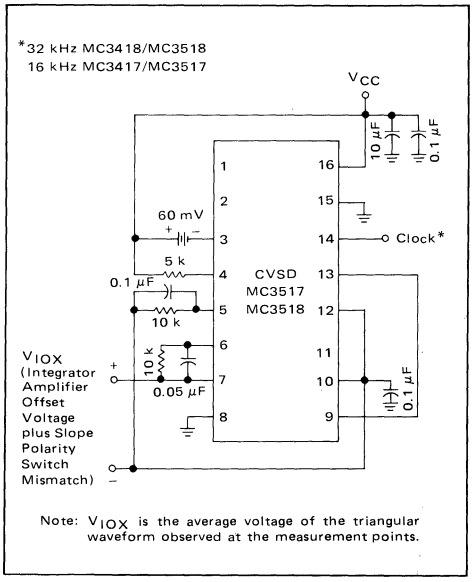
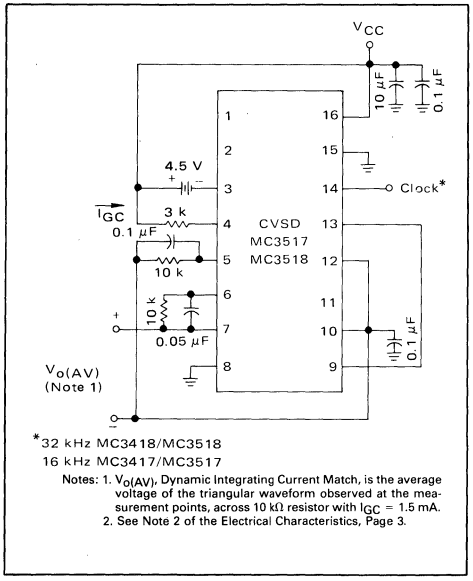


FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH



*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, Page 3.

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TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

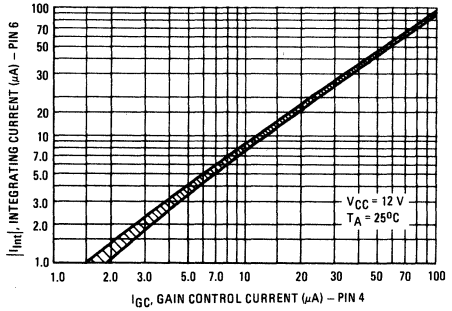

FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

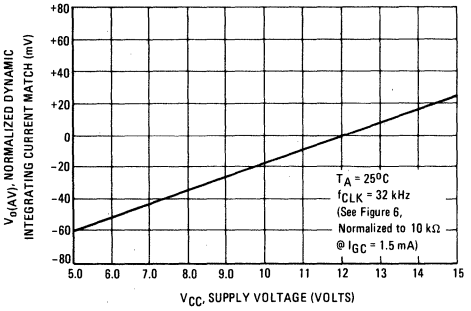

FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

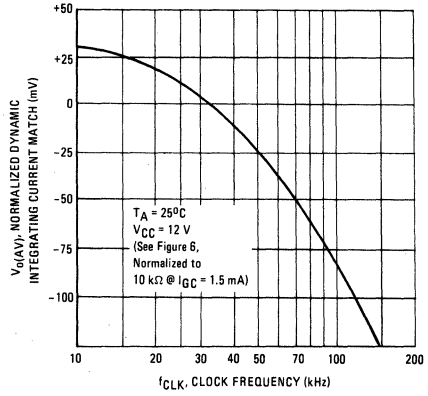

FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

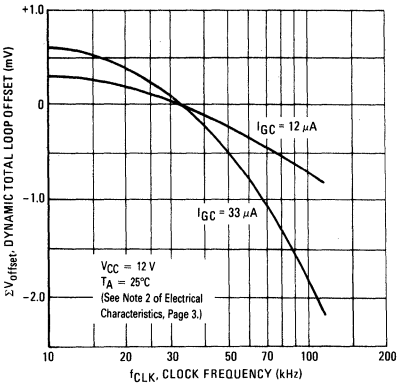

FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER

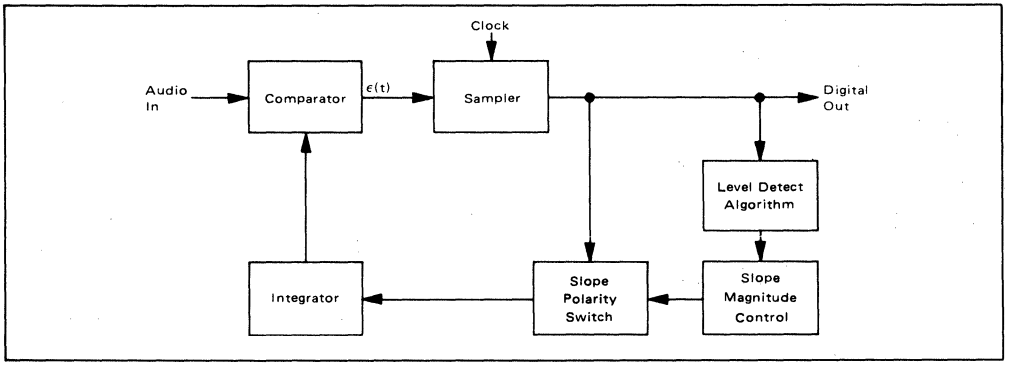

FIGURE 12 – CVSD WAVEFORMS

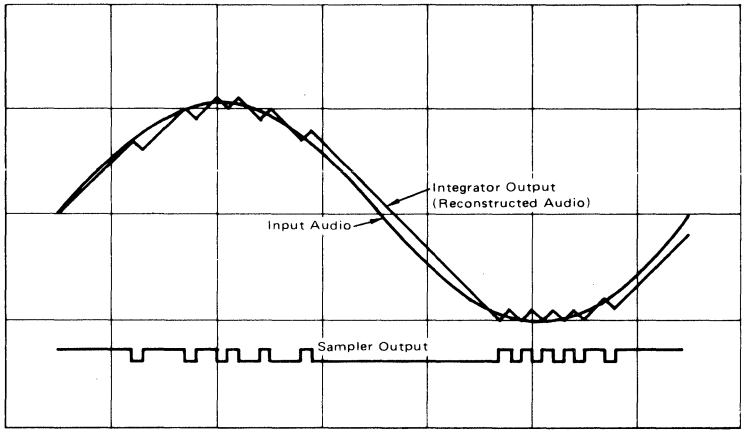

FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

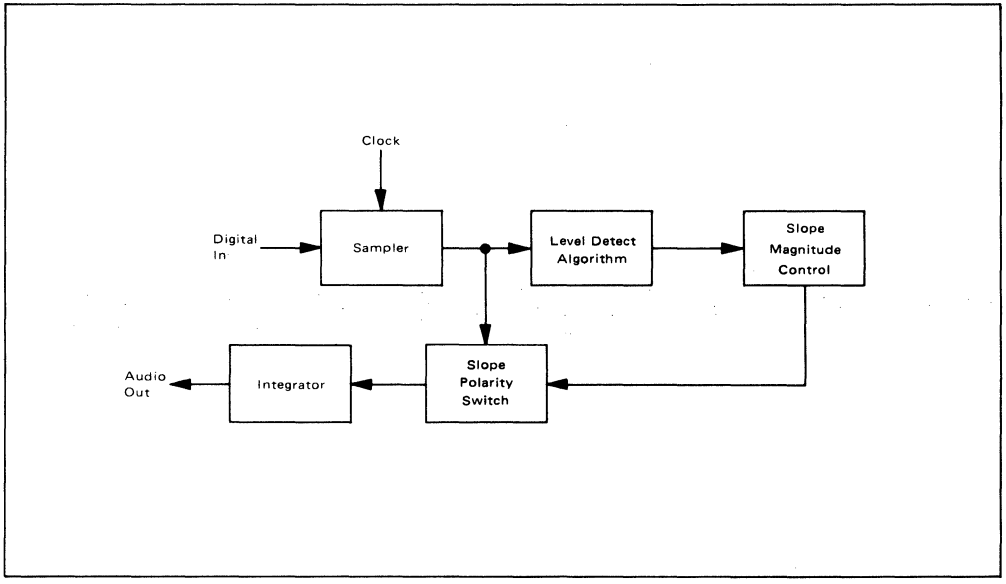

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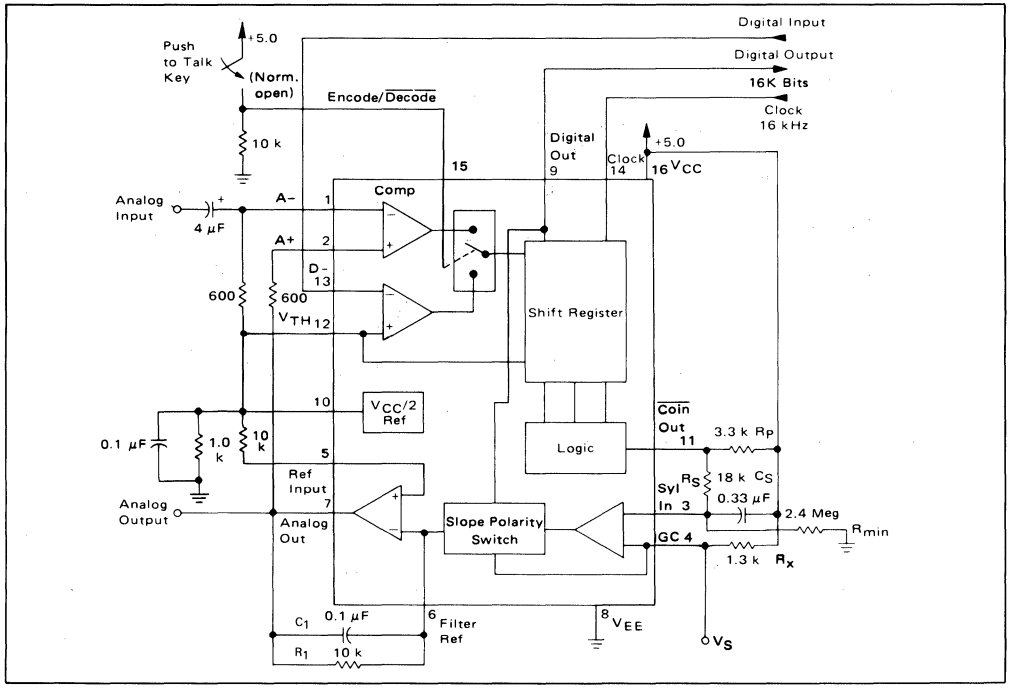
FIGURE 14 – 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

CIRCUIT DESCRIPTION (continued)

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application, and they are as follows:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

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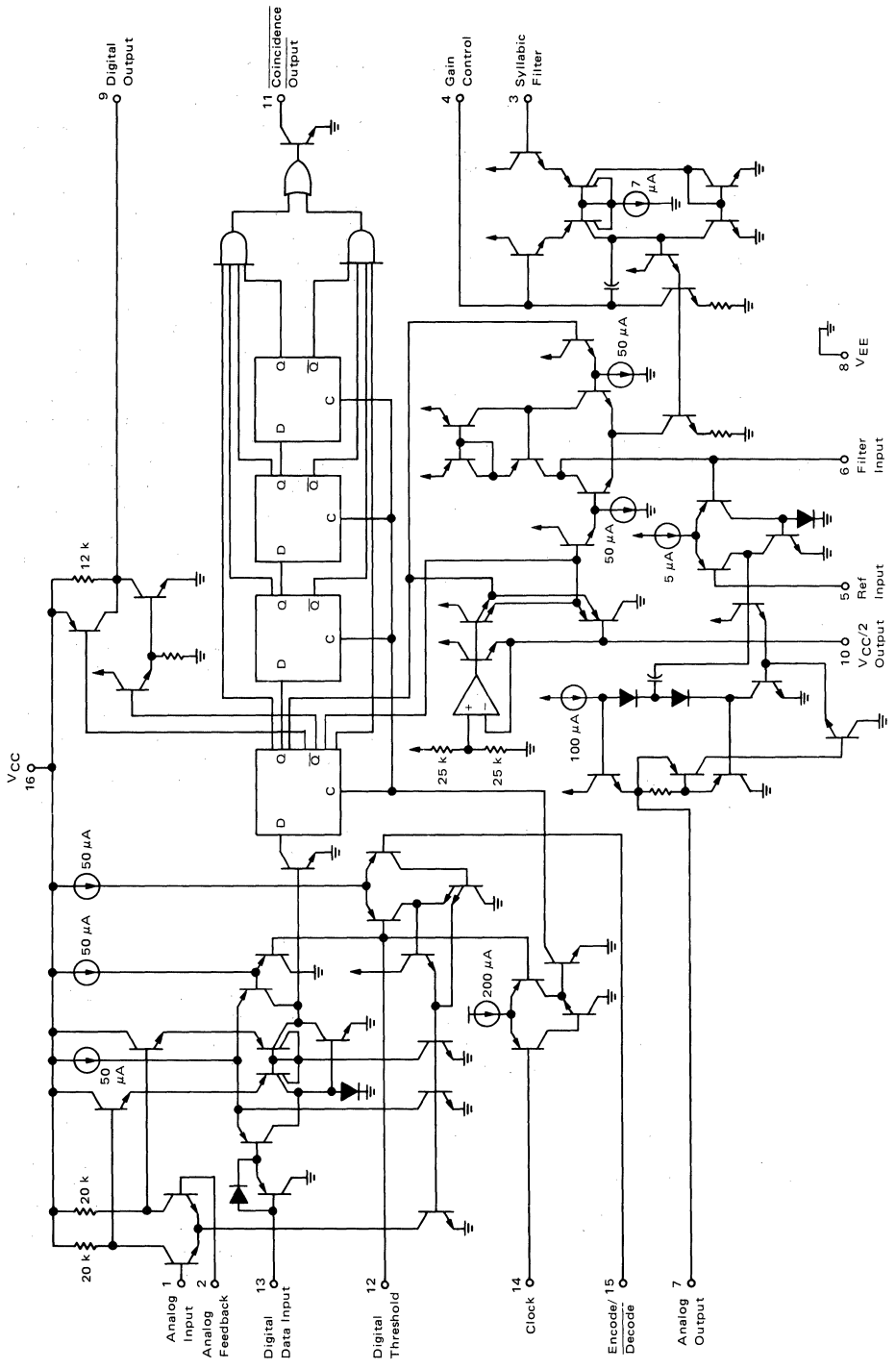
CVSD CIRCUIT SCHEMATIC



CVSD DESIGN CONSIDERATIONS (continued)

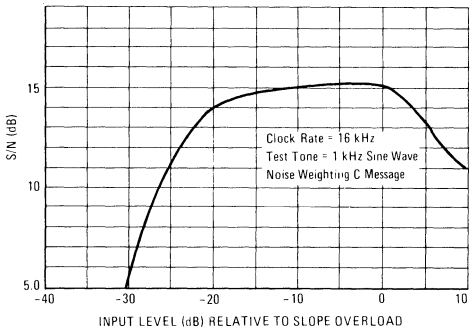
Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1–7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R_1 = 10\ k\Omega,\ C_1 = 0.1\ \mu F$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R_1} + \left(C_1 \times \frac{dV_o}{dt}\right)$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across R_1 when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

CVSD DESIGN CONSIDERATIONS (continued)

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R_1} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\,\mu F \;\; 20\text{ mV}}{62.5\,\mu s} = 33\,\mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_X.

$$I_i R_X = V_S min;\ \text{for } 33\,\mu A,\ V_S min = 41.6\text{ mV}$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_S min \qquad R_{min} \simeq 2.4\ M\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

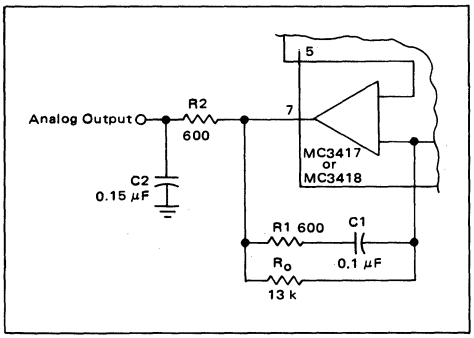
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

INCREASING CVSD PERFORMANCE (continued)

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

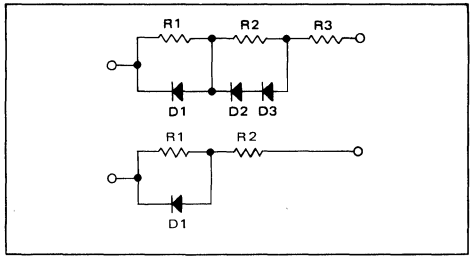
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

TELEPHONE CARRIER QUALITY CODEC USING MC3418 (continued)

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of Pin 11 is 6.0 volts. The operating companding ratio is analoged by the voltage between Pins 10 and 4 by means of the virtual short across Pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2 - 0.7$). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6.0 V).

The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to Pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at Pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at Pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on Pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2 and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily

FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER

(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)

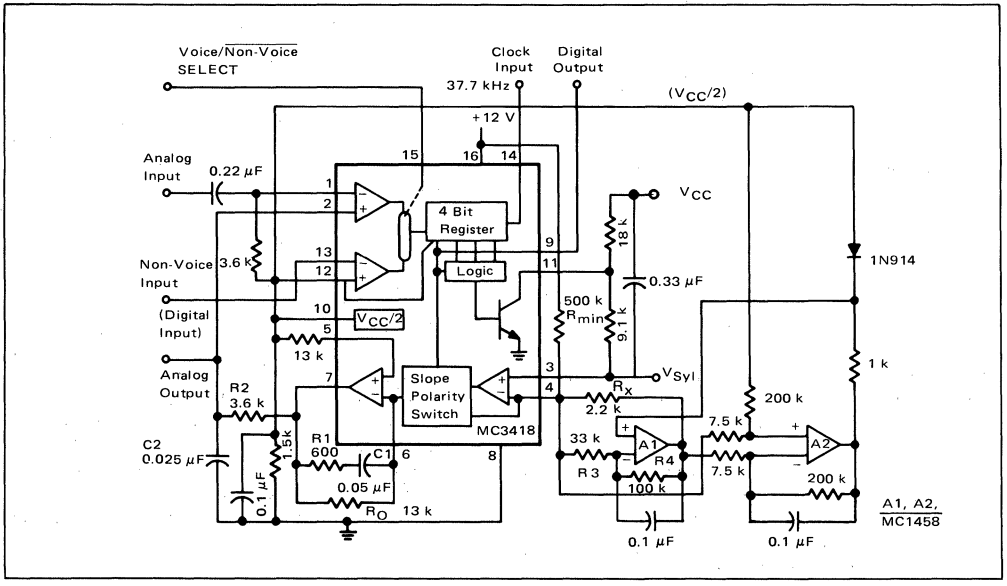
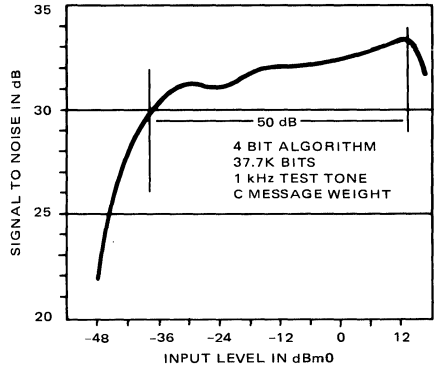
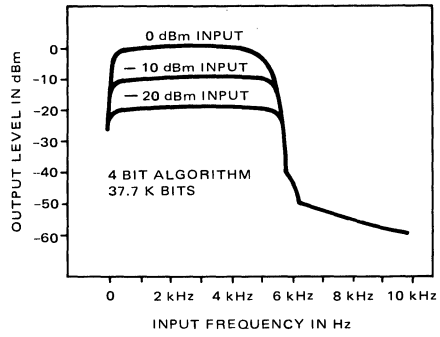


FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE
(Showing the improvement realized with the circuit in Figure 18.)

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



repeated.

With no input signal, the companding ratio at Pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to –24 under the control of A1. At –24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

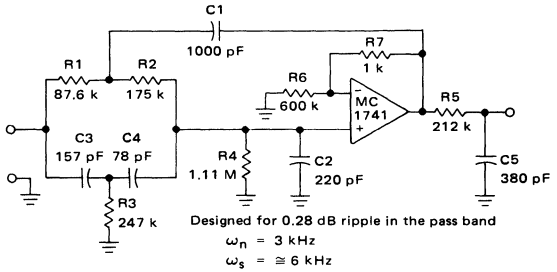
The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

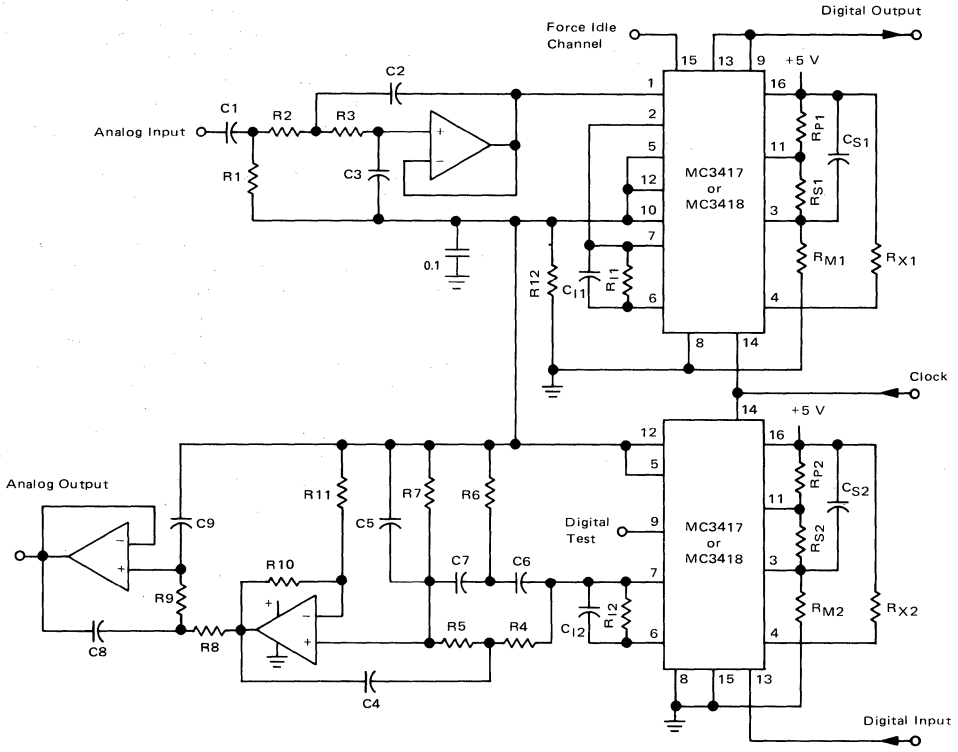
FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT



Designed for 0.28 dB ripple in the pass band
ω_n = 3 kHz
ω_s = ≅ 6 kHz
AdB at ω_s and above 29.5 dB

2

FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ
R_{M1}, R_{M2} –5 MΩ (MC3417)
Minimum step size = 20 mV
R_{M1}, R_{M2} – 15 MΩ (MC3418)
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0.05 μF
C_{I1}, C_{I2} – 0.05 μF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 kΩ
R11 – 72 kΩ

C1 – 3.3 μF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

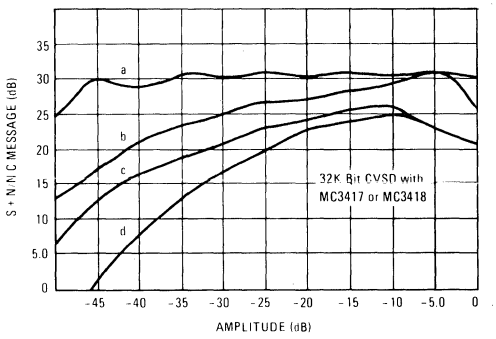
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

FIGURE 22 – COMPARATIVE CODEC PERFORMANCE – SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a — Complex companding and double integration (Figure 18 — MC3418)
Curve b — Double integration (Figure 14 using Figure 16 — MC3418)
Curve c — Single integration (Figure 14 — MC3418) with 6.0 mV step size
Curve d — Single integration (Figure 14 — MC3417) with 25 mV step size

MC3419-1L

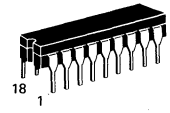
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT

TELEPHONE LINE-FEED CIRCUIT

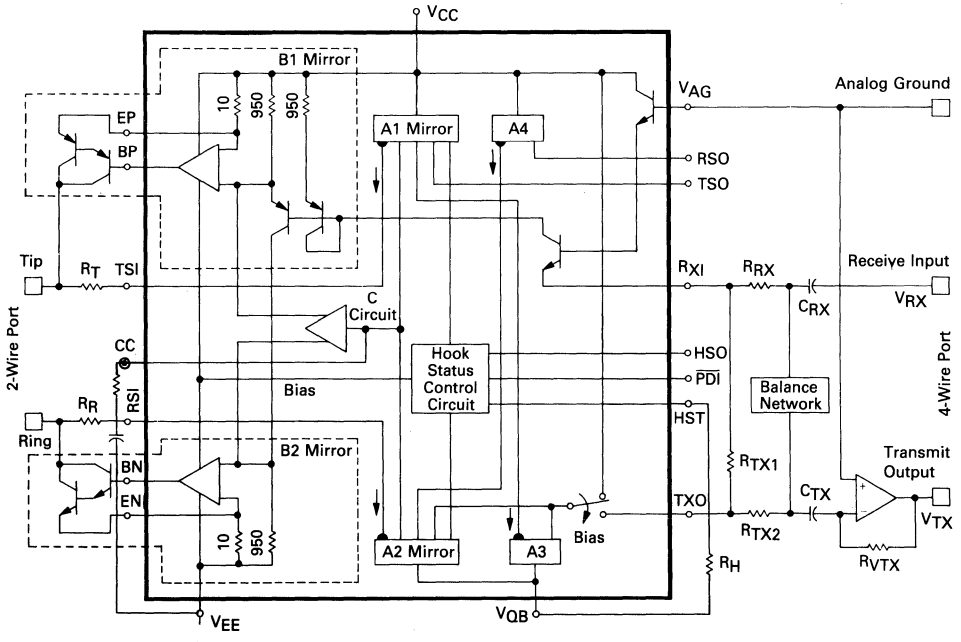
. . . designed as the heart of a circuit to provide BORSHT functions for telephone service in Central Office, PABX, and Subscriber Carrier equipment. This circuit provides dc power for the telephone (Battery), Overvoltage protection, Supervision features such as hook status and dial pulsing, two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input (Hybrid), and facilitates ringing insertion, Ring trip detection and Testing.

- Totally Upward Compatible with the MC3419
- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads for Auxiliary Functions such as: Ground Key, Ring Trip, Message Waiting Lamp, etc.
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Powerdown Input
- Ground Fault Protection
- Operates from Single −20 V to −56 V Power Source
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.



L SUFFIX
CERAMIC PACKAGE
CASE 726-04

FUNCTIONAL BLOCK DIAGRAM



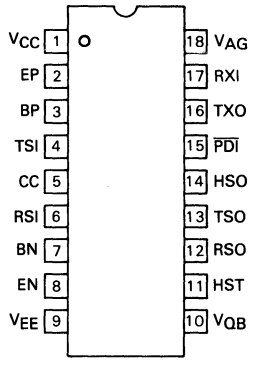
MAXIMUM RATINGS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Voltage	V_{EE} V_{QB}	−60 V_{EE} −1.0 V	Vdc
Powerdown Input Voltage Range	$V_{\overline{PDI}}$	+15 to −15	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	10 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage Compliance Range	V_{RSO}, V_{TSO}	−2.0 to −20	Vdc
Hook Status Output	V_{HSO}	+15 to −20	Vdc
Loop Resistance	R_L	0 to 2500	Ω

PIN CONNECTIONS



TRANSMISSION CHARACTERISTICS (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transmit and Receive Gain Variation (Insertion Loss) (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_L, V_L/V_{RX}	−0.3	0	+0.3	dB
Transhybrid Rejection (Input — 1.0 kHz @ 0 dBm) Fixed (1%) Resistor Balance Network Trimmed Balance Network All Types	1	V_{TX}/V_{RX}	 −23 —	 −35 −55	 — —	dB
Level Linearity (−48 to +3.0 dBm, referenced to 0 dBm @ 1.0 kHz) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Frequency Response (200–3400 Hz referenced to 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Total Distortion @ 1.0 kHz, 0 dBm (C-Message Filtered)	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB

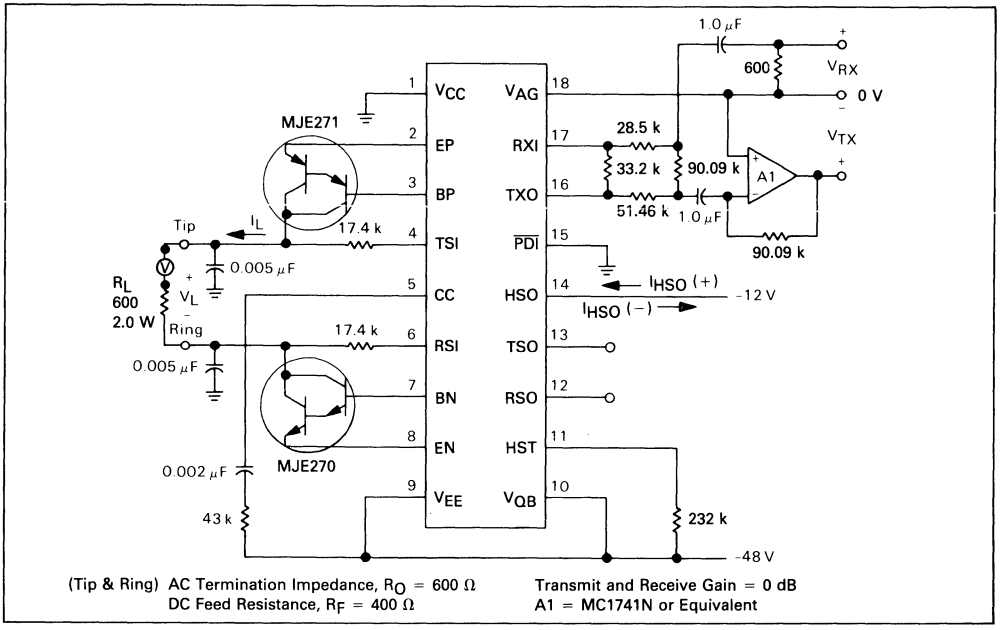
TRANSMISSION CHARACTERISTICS (continued) (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Idle Channel Noise (V_{RX} = 0 V)	1	V_{TX}, V_L	—	3.0	10	dBrnC
Return Loss (referenced to 600 ohms) @ 1.0 kHz, 0 dBm	1	$20 \log \left\lvert \frac{R_0-600}{R_0+600} \right\rvert$	30	—	—	dB
Longitudinal Induction (60 Hz) (I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnC
Longitudinal Balance (200–3000 Hz)	2	V_{TX}/V_{LON}, V_L/V_{LON}	−45	—	—	dB

ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = V_{EE}, V_{AG} = 0 V, R_L = 600 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Propagation Delay	1	T_P, V_{RX} to V_L V_{RX} to I_{TX}	— —	750 1.2	— —	ns μs
Supply Current — On-Hook (V_{EE} = V_{QB} = 56 V, R_L > 100 MΩ)	3	I_{VCC}	—	40	200	μA
On-Hook Power Dissipation (R_L > 100 MΩ)	3	P_D	—	1.0	—	mW
Power Supply Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{ee}	−40	—	—	dB
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{qb}	—	−6.0	—	dB
Sense Current Tip Ring	4	 I_{TSO}/I_{TSI} I_{RSO}/I_{RSI}	 0.15 0.15	 0.17 0.17	 0.19 0.19	mA/mA
Fault Currents Tip to V_{CC} Ring to V_{CC} Tip to Ring Tip and Ring to V_{CC}	1	 I_{Tip} I_{Ring} I_{Loop} I_{Tip} and I_{Ring}	 — — — —	 0 2.5 120 2.5	 — — — —	mA
Analog Ground Current	1	I_{VAG}	—	0.1	2.0	μA
Powerdown Logic Levels		$I_{\overline{PDI}}$ V_{IH} V_{IL}	— −1.2 —	−1.0 — —	−10 — −4.0	μA Vdc Vdc
Hook Status Output Current (R_L < 2.5 kΩ, V_{HSO} = +0.4 Vdc) V_{HSO} = −0.4 Vdc) (R_L > 10 kΩ, V_{HSO} = +12 Vdc) V_{HSO} = −12 Vdc)	1	I_{HSO}	 +1.0 −0.4 — —	 +3.0 −1.5 0 0	 — — +50 −2.0	 mA mA μA μA

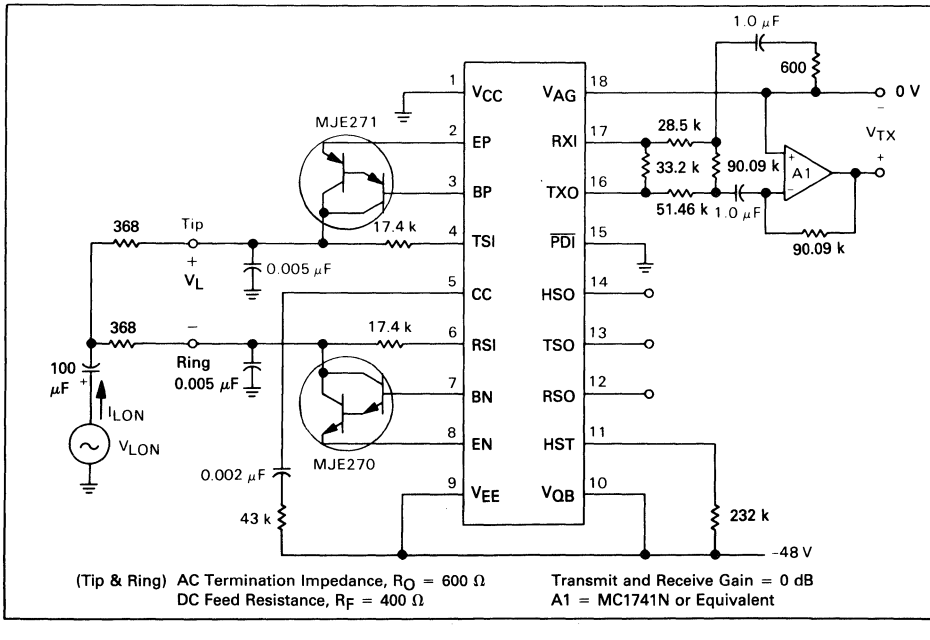
FIGURE 1 — AC TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT

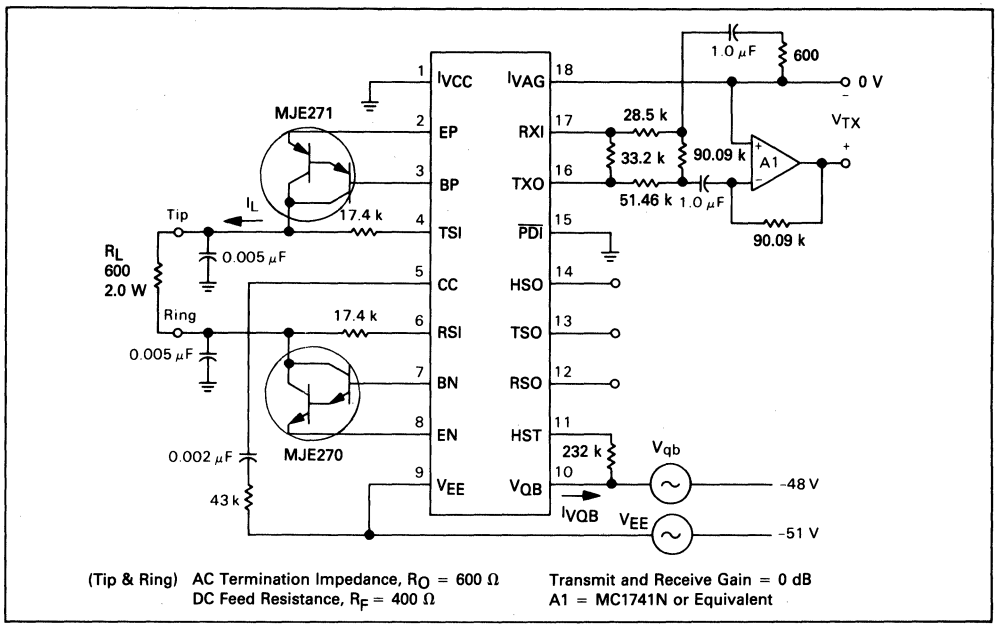


(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

2

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

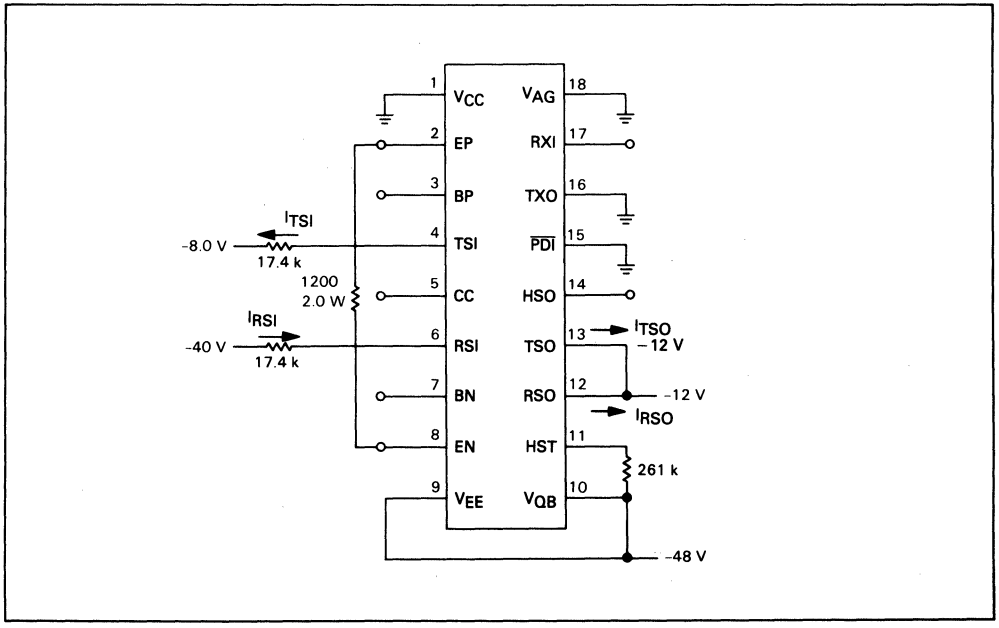


FIGURE 5 — QUIET BATTERY CURRENT I_{VQB} versus LOOP CURRENT I_L

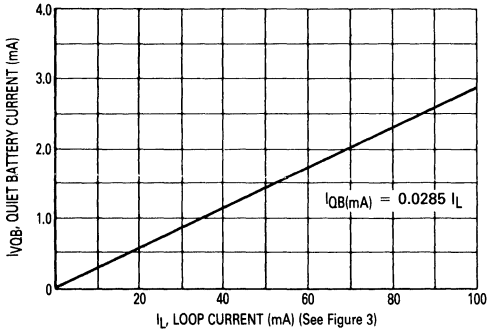
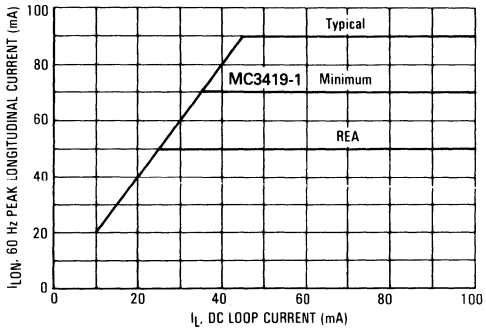


FIGURE 6 — LONGITUDINAL CAPACITY



PIN DESCRIPTIONS

Pin	Name	Function
1	V_{CC}	The positive supply voltage. This point is ground in typical applications.
2, 8	EP & EN	Loop current sensing inputs. These are connected to the emitters of the PNP and NPN Darlington transistors. They are tied through 10 Ω resistors to V_{CC} and V_{EE}, respectively. The maximum continuous current through these inputs is 240 mA.
3, 7	BP & BN	Base drive outputs. These pins drive the bases of the PNP and NPN transistors and are able to sink or source, respectively, up to 5.0 mA.
4, 6	TSI & RSI	Tip and Ring voltage Sensing Inputs. They are low impedance inputs (approximately 600 Ω each i.e., 400 Ω + 3 diodes) that translate the voltages on Tip and Ring to a current through resistors R_T and R_R. TSI is referenced to V_{CC} and RSI is referenced to V_{QB}. These pins have 6.0 V zener diodes (to their respective reference) for protection against overvoltage line surges.
5	CC	Compensation Capacitor pin. This pin is used to stabilize the longitudinal or common mode circuitry.
9	V_{EE}	Negative supply voltage. This pin ties to the chip substrate. Its operating voltage range is −20 V to −56 V. It can withstand −60 V without damage and can sustain a voltage surge to −75 V for less than 4.0 ms without significant degradation of performance. Most of the loop current and bias currents flow through this pin.
10	V_{QB}	Quiet Battery Voltage reference. This is the voltage reference for the RSI pin. Its voltage must not go more negative than V_{EE}. The current through this pin, while powered up, is proportional to the loop current, allowing it to be used for loop current limiting. The voltage on this pin, less 4 volts, is the "effective battery feed voltage for the 2-wire lines even though most of the power comes from the V_{EE} supply.
11	HST	Hook Status Threshold programming resistor input. R_H determines the value of loop resistance at which on-hook and off-hook status is switched.
12	RSO	Ring Sense current Output. This output reflects the voltage status of the Ring terminal for voltages more positive than V_{QB}. The current is sourced from this output, it is one-sixth I_{RSI}, its voltage range is 0 to −20 V and its saturation voltage is approximately −2.0 V.
13	TSO	Tip Sense current Output. This output reflects the voltage status of the Tip terminal for voltages more negative than V_{CC}. The current is sourced from this output, it is one-sixth I_{TSI}, its voltage range is 0 V to −20 V and its saturation voltage is approximately −2.0 V.
14	HSO/$\overline{\text{HSO}}$	Hook Status Output. This is a digital output that reflects the condition of the loop resistance. If loop resistance is less than a predetermined value established by R_H, usually $R_L < 2.5$ kΩ, the HSO pin will be active, i.e., with positive voltage logic (a resistor tied from a +5.0 V or +12 V supply to HSO), this pin will sink current to V_{CC} ($V_{HSO} \cong 0$ V); with negative voltage logic (a resistor tied from a −12 V supply to HSO), this pin will source current from V_{CC} ($V_{HSO} \cong 0$ V). If loop resistance is greater than a predetermined value again established by the same resistor R_H, usually $R_L > 10$ kΩ, the HSO pin is inactive, i.e., V_{HSO} = logic supply voltage.
15	$\overline{\text{PDI}}$	Powerdown Input pin. This pin is used to deny service to the subscriber. A logic level "O" ($V_{IL} <$ −4.0 V) powers down the MC3419-1 except for HSO, TSO and RSO. The voltage range of this high impedance input pin is ±15 V.
16	TXO	Transmit current Output. This output sinks current to V_{QB} and is proportional to $I_{TSI} + I_{RSI}$ by a ratio of K1 where: K1 = 0.51. Its saturation voltage is V_{QB} + 2.5 V typ. (+3.5 V over the temperature range). This pin is only active during the off-hook power-up condition.
17	RXI	Receive Input. This input sums ac currents from TXO and the receive voltage input (V_{RX}) and sources all the dc current to TXO. It has a low input impedance (15 Ω) typically biased 4.5 V below the V_{AG} pin voltage during off-hook power-up conditions. During powerdown conditions, the voltages on RXI and TXO can drift up to V_{AG}.
18	V_{AG}	Analog Ground Voltage reference input. The input impedance of this pin is much greater than 1.0 MΩ. It should be ac coupled to system ground and could be direct coupled if system ground is between 0 V and −12 V. AC coupling requires 300 kΩ to V_{CC} and 0.1 μF to system ground. If V_{CC} and system ground are common, tie V_{AG} directly to V_{CC}. If dc loop currents are allowed to go higher than 60 mA, V_{AG} should be biased from −2.5 V to −12 V to avoid problems at high ambient temperatures.

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram on page 1, line sensing resistors (R_R and R_T) at the TSI and RSI pins convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. An output of A1 is mirrored by A3 and summed together with an output of A2 at the TXO terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TXO output.

All the dc current at the TXO output is fed back through the RXI terminals to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a unity gain output of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TXO output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less, but proportional to the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TXO output were returned to the B1 input along with the dc current. Instead, the MC3419-1 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp (external to the MC3419-1) and a feedback resistor which produces the transmit output voltage (V_{TX}) at the 4-wire interface. Transmission gain is programmed by the op amp feedback resistor (R_{VTX}).

Reception gain is realized by converting the ac coupled receive input voltage (V_{RX}) to a current through an external resistor (R_{RX}) at the low impedance RXI terminal. This current is summed at RXI with the dc and ac feedback current from the A-Circuit mirrors and drives the B1 mirror input. The B-Circuit mirror outputs drive the 2-wire port with balanced ac current proportional to the receive input voltage. Reception gain is programmed by the R_{RX} resistor.

Since receive input signals are transmitted through the MC3419-1 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419-1 by two methods. The first is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit mirrors and summed together at TXO, the total current at TXO remains unchanged. Therefore, the ac currents due to the common-mode signal are cancelled before reaching the transmit output.

The second longitudinal suppression method is more dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals.

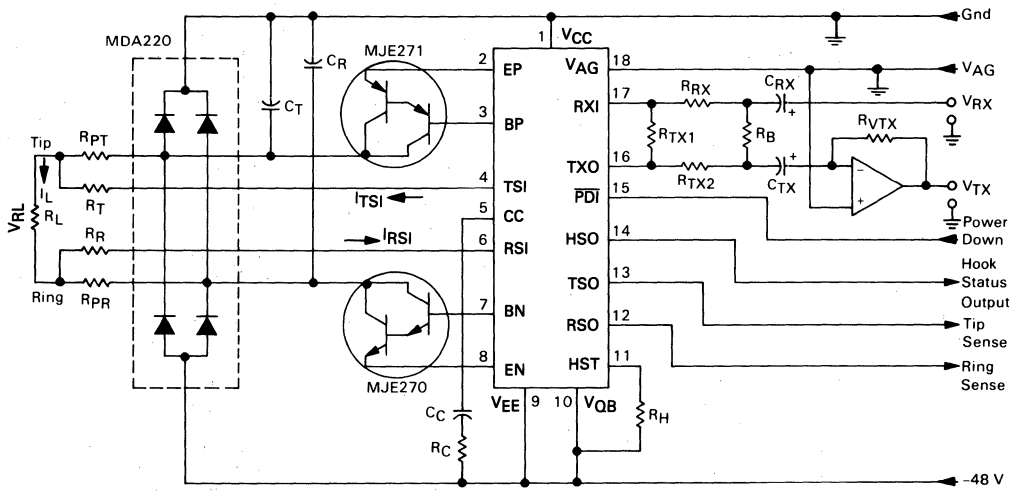
A common-mode suppression circuit detects common-mode inputs and drives the loop with balanced currents to reduce the input amplitude. Subtracting currents from outputs of the A1 and A2 mirrors produces a signal current at the CC terminal in response to the common-mode voltage at Tip and Ring. A transconductance amplifier (C-Circuit) generates a current proportional to the CC terminal voltage which is summed with the current from the RXI terminal at the inputs of current mirrors B1 and B2. The weighting and polarity of the summing networks produce common-mode B1 and B2 mirror output currents at the 2-wire port. The common-mode input impedance is inversely proportional to the gain of the longitudinal suppression circuit. R_C and C_C compensate the common-mode feedback loop. At 60 Hz with typical component values, the 2-wire common-mode impedance is less than 5 Ω.

The longitudinal suppression circuit output currents are generated by modulating dc current fed to the loop by the B1 and B2 current mirrors. This configuration avoids the increased power dissipation attributed to current mode loop drive because dc and longitudinal currents are not cumulatively sourced to the loop. However, driving common-mode currents through the B-circuit current mirrors in this manner limits the longitudinal suppression capability. The suppression circuit is unable to reverse 2-wire current polarities to maintain a low-impedance termination when longitudinal currents exceed the dc loop current. At low dc loop currents, the common-mode signal capability, known as longitudinal capacity, is limited by the loop current (Figure 6). At high-loop currents, longitudinal capacity is limited by the maximum voltage swing of the CC terminal and is therefore independent of dc loop current.

*A current mirror is a circuit which behaves as a current controlled current source. It has a single low-impedance input terminal with respect to a reference point and one or more high impedance outputs.

2

FIGURE 7 — BASIC SLIC CIRCUIT



The hook status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419-1. To activate the bias currents, the control circuit compares the current through the sense resistors, R_R and R_T, and the load resistance R_L with the current through the hook status threshold programming resistor, R_H, by using outputs from both A1 and A2 mirrors. The A1 mirror output sources current to the R_H resistor. (This reduces all internal currents to near zero during the on-hook state in order to eliminate unnecessary power consumption.) If this current is large enough the voltage on the HST pin will trip an internal comparator, then another circuit compares the current from the A1 output with that of an A2 output. These currents must match within ±15%. If so, HSO will be activated and the bias circuits will turn on provided the voltage on $\overline{PDI}$ is greater than −1.2 V. The HSO pin can have either a pull-up resistor or a pull-down resistor and when activated it will switch to V_{CC} (0 volts).

Once the MC3419-1 is powered up, a circuit with a gain of 20 feeds current to the R_H resistor in order to keep the bias circuitry active. (The sense resistors are paralleled with the Darlington transistors which reduces the sense input currents.) Should the sense input currents drop below one-twentieth of the required power-up current, the bias currents will be removed, forcing a power-down condition.

Current mode analog signal processing is critically dependent on voltage to current conversion at the 2-wire and 4-wire inputs. Precise, low-noise voltage sensing through resistors R_T, R_R and R_{RX} requires quiet, low impedance terminations at terminals TSI, RSI and RXI respectively. For 2-wire signals, terminal V_{QB} isolates the loop-sensing resistors and current mirrors from noise at the high-current V_{EE} terminal. External filtering from V_{CC} to V_{QB} ("quiet battery" terminal) ensures loop voltages are sensed without interference from system supply noise. V_{EE} noise rejection at audio frequencies is typically 60 dB or greater.

Receive input terminal RXI is referenced to the V_{AG} terminal which references the 4-wire input to the "analog ground" of the 4-wire signal source, thus isolating the input from power ground voltage transients. This isolation offers 70 dB of noise rejection at audio frequencies.

SYSTEM EQUATIONS

K1 — The current gain from I_{TSI} + I_{RSI} to TXO only during an off-hook power-up condition. K1 = 0.51 ± 1%.

K2 — The current gain from RXI to the collectors of the off-chip Darlington transistors only during an off-hook power-up condition. K2 = 95 ± 1%.

For simplicity, the following equations do not use K1 or K2. Instead the actual numerical value is used, for instance (1 + [2]K1K2) = 1 + 1.02 x 95 = 97.9 is approximately 98.

R_L — Loop resistance. This is a load resistance from Tip to Ring and can be either ac or dc depending on context.

LOOP CURRENT REGULATIONS

FIGURE 8(a)

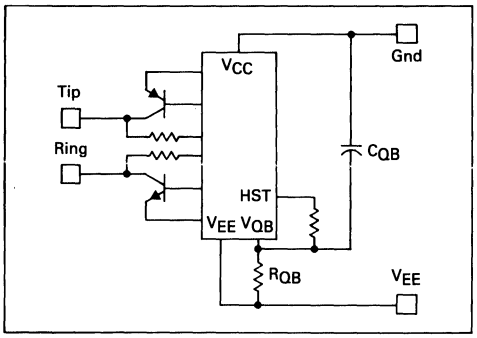


FIGURE 9(a)

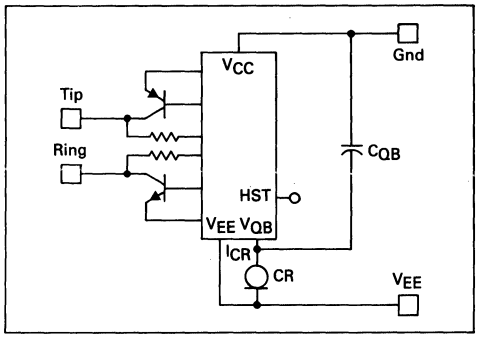


FIGURE 8(b)

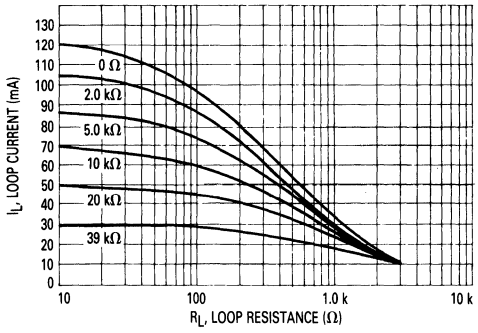
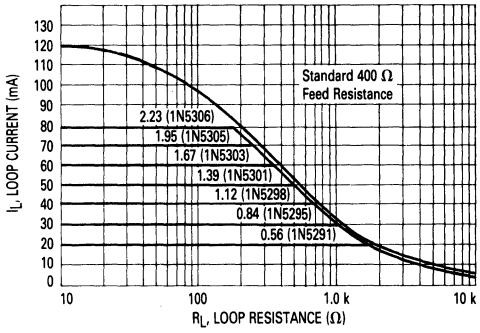


FIGURE 9(b)



SYSTEM EQUATIONS (continued)

Z_L — Loop impedance. This is used only to connote a complex impedance loading on Tip and Ring.

I_L — Loop current. The dc current flow through R_L.

R_F — Dc feed resistance. The synthesized resistance from which battery (V_{CC} and V_{EE}) current is fed to R_L. The battery feed resistance is balanced differential feed. See Figure 7. (This assumes $V_{QB} = V_{EE}$.) The first order equation is:

$$R_F = \frac{R_R + R_T + 1200\ \Omega}{98} \quad (1)$$

Because of the diode voltage drops on TSI and RSI, the actual dc feed resistance is higher. The second order equation is:

$$R_F = \frac{|V_{QB}|(98\ R_L + R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} - R_L \quad (2)$$

ignoring the effects of R_L

$$R_F = \frac{|V_{QB}|(R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} \quad (3)$$

So:

$$R_R = R_T = \frac{49R_F\ (|V_{QB}| - 4.0\ V)}{|V_{QB}|} - 600 \quad (4)$$

The minimum value for R_R and R_T is 5.0 kΩ.

The first order value of R_F can not be greater than the desired value of the termination impedance (usually 600 Ω or 900 Ω). To achieve dc feed resistances that are greater, a resistor can be placed between V_{QB} and V_{EE} along with a filter capacitor C_{QB} which restores the desired termination impedance and filters power supply noise. A diode should also be placed between V_{QB} and V_{EE} to prevent damage in case a catastrophic power supply failure occurs.

2

I_{VQB} — This is the current that is sourced from the V_{QB} pin and is proportional to the currents into and out of RSI and TSI. When the SLIC is in the off-hook power-up mode, I_{VQB} is also proportional to I_L.

$$I_{VQB} = 2.15\, I_{RSI} + 0.7\, I_{TSI} \quad (5)$$

$$I_{VQB} = 0.029\, I_L \quad (6)$$

R_{FQ} — Dc feed resistance. The synthesized resistance from which battery current is fed to R_L, see Figure 8. (This assumes V_{QB} is tied to V_{EE} through a resistor R_{QB}.) R_{QB} synthesizes additional dc feed resistance to the R_F value previously stated.

When using R_{QB}, the dc feed is effectively balance fed from V_{CC} and V_{QB} instead of V_{EE}. The sense resistors (R_R and R_T) should be selected to make R_F (first order) less than the termination impedance.

$$R_{FQ} = \frac{|V_{EE}|(98R_L + R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} - R_L \quad (7)$$

Ignoring R_L, this simplifies to:

$$R_{FQ} = \frac{|V_{EE}|(R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} \quad (8)$$

Therefore:

$$R_{QB} = \frac{98R_{FQ}(|V_{EE}| - 4.0\ V) - |V_{EE}|(R_R + R_T + 1200\ \Omega)}{2.85|V_{EE}|} \quad (9)$$

C_{QB} — Power supply noise filter capacitor.

$$C_{QB} = \frac{2.85\ R_{QB} + R_R + R_T + 1200\ \Omega}{2\pi f\ R_{QB}\ (R_R + R_T + 1200\ \Omega)} \quad (10)$$

Figure 9B shows R_{QB} replaced with a current regulating device such as Motorola's 1N5283 family.

I_{CRQB} — The current that is sourced to a current regulating device from the V_{QB} pin. When this current reaches the regulated value, the voltage differential between V_{EE} and V_{QB} increases causing the effective battery voltage to decrease which limits I_L to a maximum value as determined below:

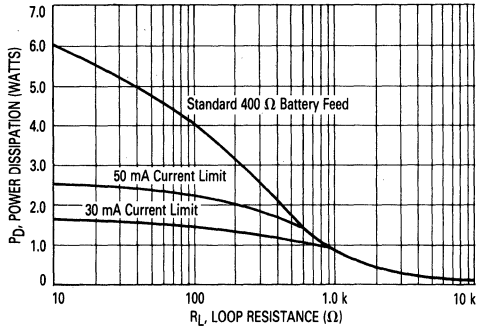
$$I_L = 34.5\, I_{CRQB} \quad (11)$$

The graph, Figure 9B, shows loop current versus loop resistance using several values of I_{CRQB}. The closest current regulating diode part number to that value is also shown. A typical value for C_{QB} in this case is 10 μF, 60 Vdc.

Figure 10 shows how power can be conserved on the shorter loop lengths by utilizing current limiting techniques.

Overvoltage protection on the 2-wire port is achieved with the MDA220 diode bridge and the protection resistors R_{PR} and R_{PT}. Whenever the voltage on the 2-wire port exceeds the power supply rails (V_{CC} and V_{EE}), the MDA220 diodes will forward bias and "clamp" to the rail voltage. The current is limited by the protection resistors. These resistors should be as large in value as possible. However, if they are too large, they will interfere with the performance of the SLIC under worst case conditions.

FIGURE 10 — TOTAL SLIC POWER DISSIPATION versus LOOP RESISTANCE



$$R_{PT} < R_T/196 - 15 \quad (12)$$

Using the voltage of V_{QB} when I_L is at its minimum off-hook value (Typ. 20 mA):

$$R_{PR} < R_R/196 + 25|V_{EE} - V_{QB}| - 15 \quad (13)$$

The tolerance of these resistors is not critical due to placement inside a closed loop. Positive temperature co-efficient resistors (PTC) may be considered here. Consult resistor manufacturers for component selections that will meet the surge current and peak voltage requirements.

Because the MC3419-1 is a broadband device it requires compensation components to keep its circuits stable.

C_R & C_T — Compensates the longitudinal gain of the A and the B circuit mirrors. Their values range from 2000 pF to 5000 pF.

R_C & C_C — Compensates the longitudinal "C" circuitry. Their values can be ratioed according to:

$$R_C \times C_C = R_T \times C_T. \quad (14)$$

Two off-chip power Darlington transistors are used with the MC3419-1. These transistors reduce any temperature gradiant problems with the precision matched devices on-chip and they alleviate thermal stress conditions that could occur for every on-hook and off-hook transition. The power dissipation in these devices is:

$$P_{QT} = I_L{}^2(R_T/98 - R_{PT} - 4) + (2.0\ V)I_L \quad (15)$$

$$P_{QR} = I_L\,[|V_{EE}| - 2 - I_L(R_T/98 + R_L + R_{PR} + 16)] \quad (16)$$

where $I_L = |V_{EE}|/R_{FQ}$ or $I_L(max)$ in current limited designs.

SYSTEM EQUATIONS (continued)

R_H — The resistor that determines the hook status threshold values of R_L. R_H is selected from a graph of the following two equations:

Off-hook threshold

$$R_H = 6(R_L + R_R + R_T) \quad (17)$$

On-hook threshold

$$R_H = 27.25\,[R_L + 0.01(R_R + R_T)] \quad (18)$$

FIGURE 11 — HOOK STATUS DETECTION

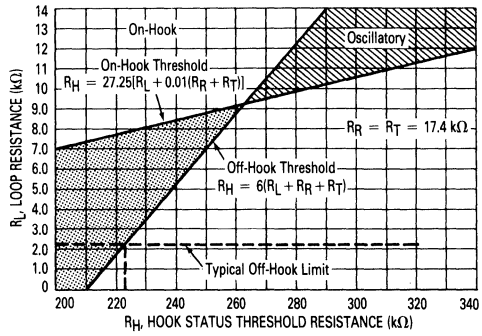


Figure 11 shows such a graph using 17.4 kΩ as the values for R_R and R_T. Note the oscillatory condition to the right of the crossing point. Selection of R_H in this region is usually not a problem since the majority of telephone lines do not fall into this resistance range. R_H always ties to V_{QB} and HST and will give reliable hook status information regardless of power supply voltages and $\overline{PDI}$.

R_O — Termination impedance of the 2-wire port. This impedance is greater than the dc feed resistance R_F because of a current splitting network in the feedback loop, R_{TX1} and R_{TX2}.

K3 — A constant, formed by R_{TX1} and R_{TX2}, between 0 and 1, which determines the ratio of the first order value of R_F to R_O.

$$R_O = \frac{R_R + R_T + 1200\ \Omega}{1 + 97K3} \quad (19)$$

So:

$$K3 = \frac{R_R + R_T + 1200\ \Omega - R_O}{97R_O} \quad (20)$$

and

$$K3 = \frac{R_{TX2} + Z_{in}}{R_{TX1} + R_{TX2} + Z_{in}} \quad (21)$$

Z_{in} — The input impedance of the current to voltage converter op amp. This impedance is usually negligible, it can be used to sway the selection of a 1% component value.

$$Z_{in} = \frac{(R_R + R_T + 1200\ \Omega)\,G_{TX}}{1020\,(1 - K3)} = \frac{R_{VTX}}{1000} \quad (22)$$

R_{TX1} — Feeds most of the TXO dc current to the RXI pin. To keep TXO from saturation the maximum value of R_{TX1} is as follows:

$$R_{TX1} < \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{QB}|min - |V_{AG}|max - 6.5\ V)}{|V_{QB}|min - 5.4\ V} \quad (23)$$

Where:

$$|V_{QB}|min = \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{EE}|min - 4)}{(R_R + R_T + 1200\ \Omega + 2.8\ R_{QB})} \quad (24)$$

or If a current regulator diode is used:

$$R_{TX1} < \frac{0.01\ I_L(max)\,(R_R + R_T + 600\ \Omega) - |V_{AG}|max - 3.9\ V}{0.01\ I_L(max)} \quad (25)$$

It is beneficial to make R_{TX1} as large as possible. Typical values range from 15 k to 24 kΩ.

$$R_{TX2} = \frac{K3\,R_{TX1}}{1 - K3} - Z_{in} \quad (26)$$

$$C_{TX} = \frac{R_R + R_T + 1200\ \Omega}{7R_{TX2}} \quad \text{The result is in } \mu F. \quad (27)$$

G_{TX} — The voltage gain from the 2-wire port to V_{TX} which is adjustable by R_{VTX}.

$$G_{TX} = \frac{1.02\,(1 - K3)\,R_{VTX}}{R_R + R_T + 1200\ \Omega} \quad (28)$$

$$R_{VTX} = \frac{G_{TX}(R_R + R_T + 1200\ \Omega)}{1.02\,(1 - K3)} \quad (29)$$

G_{RX} — The voltage gain from the V_{RX} input to the 2-wire port which is adjustable by R_{RX}.

$$G_{RX} = \frac{-95\,R_L\,(R_R + R_T + 1200\ \Omega)}{R_{RX}\,[(R_R + R_T + 1200\ \Omega) + R_L(1 + 97K3)]} \quad (30)$$

$$G_{RX} = \frac{-95\,R_L\,R_O}{R_{RX}(R_L + R_O)} \quad (31)$$

$$R_{RX} = \frac{95\,R_L\,R_O}{G_{RX}(R_L + R_O)} \quad (32)$$

$$C_{RX} > \frac{R_{RX} + R_B}{2\pi\,f\,R_{RX}R_B} \quad (33)$$

Where f is the minimum passband frequency, usually 200 Hz.

Transhybrid Rejection — The voltage gain from V_{RX} to V_{TX}. It is expressed in dB, the number should be negative and the larger the value the better. Transhybrid rejection is achieved by summing a current from the V_{RX} input (R_B) with the TXO current that flows to the current to voltage converter. R_B balances a resistive load, R_L.

$$R_B = \frac{R_{RX}(1 + 97K3)\,(R_O + R_L)}{97R_L\,(1 - K3)} \quad (34)$$

2

FIGURE 12 — BALANCE NETWORK FOR CAPACITIVE LINES

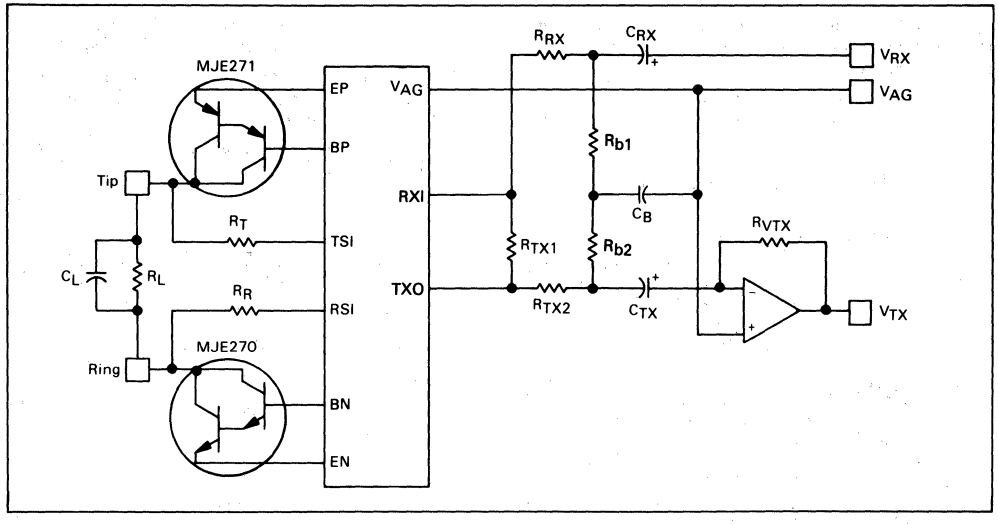
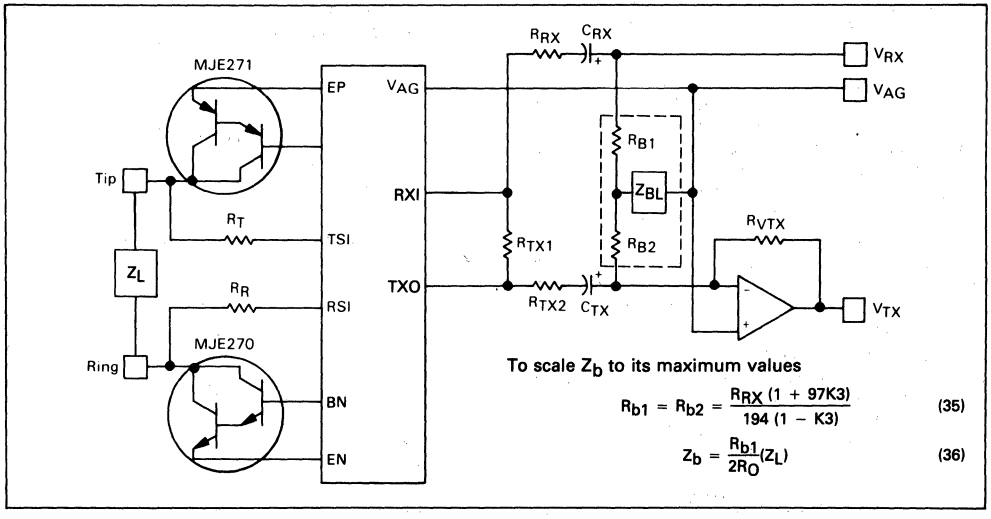


FIGURE 13 — BALANCE NETWORK FOR COMPLEX LOAD IMPEDANCES



To scale Z_b to its maximum values

$$R_{b1} = R_{b2} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} \quad (35)$$

$$Z_b = \frac{R_{b1}}{2R_O}(Z_L) \quad (36)$$

When the 2-wire port has a parallel R and C load, then (see Figure 12):

$$R_{b1} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_L(1 - K3)} \quad (37)$$

$$R_{b2} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_O(1 - K3)} \quad (38)$$

$$C_b = \frac{R_L C_L}{R_{b2}} \quad (39)$$

When it is desirable to balance complex load impedances using component values that are equal to the load values (see Figure 13) then:

$$R_{b1} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} + \sqrt{\left[\frac{R_{RX}(1 + 97K3)}{194(1 - K3)}\right]^2 - \frac{R_O R_{RX}(1 + 97K3)}{97(1 - K3)}} \quad (40)$$

$$R_{b2} = \frac{R_{RX}(1 + 97K3)}{97(1 - K3)} - R_{b1} \quad (41)$$

$$Z_b = Z_L \quad (42)$$

R_{b1} and R_{b2} values are interchangeable.

SYSTEM EQUATIONS (continued)

The Tip and Ring Sense Output currents are proportional to the currents out of and into TSI and RSI, respectively.

$$I_{TSO} = \frac{I_{TSI}}{6} \quad (43)$$

$$I_{RSO} = \frac{I_{RSI}}{6} \quad (44)$$

$$I_{TSO} = \frac{|V_{Tip} - V_{CC}| - 2.0\ V}{6\ (R_T + 600\ \Omega)} \text{ for } V_{Tip} < V_{CC} \quad (45)$$

$$I_{RSO} = \frac{|V_{Ring} - V_{QB}| - 2.0\ V}{6(R_R + 600\ \Omega)} \text{ for } V_{Ring} > V_{QB} \quad (46)$$

Digital interfacing to the MC3419-1 $\overline{PDI}$ pin and the HSO pin is shown in Figures 14a, 14b and 14c. If the $\overline{PDI}$ pin is not used it should be terminated to V_{CC} and if HSO is not used, it can be left open.

Figure 15 is an application circuit showing solid state ringing insertion using an MOC3030 zero-crossing detector optocoupled triac to replace the conventional electromechanical relay. This device inserts the ringing signal on a zero voltage crossing which eliminates noise in adjacent cable pairs and removes the signal on a zero current crossing which eliminates inductive voltage spikes that commonly destroy relay contacts. The ringing generator provides a continuous 40 V to 120 V RMS signal from 15 to 66 Hz superimposed upon −48 Vdc. Ringing cadencing is inserted with the Ring Enable Input. The 2N6558 and MPSA42 replace the MJE270 for systems that use ringing generator voltages greater than 70 V_{RMS}. The MDA220 diode bridge is replaced with a series 1N4007 on the Tip lead and a shunting 1N4004 to V_{EE} and to allow ringing voltage

FIGURE 14 — INTERFACE-TO-DIGITAL LOGIC

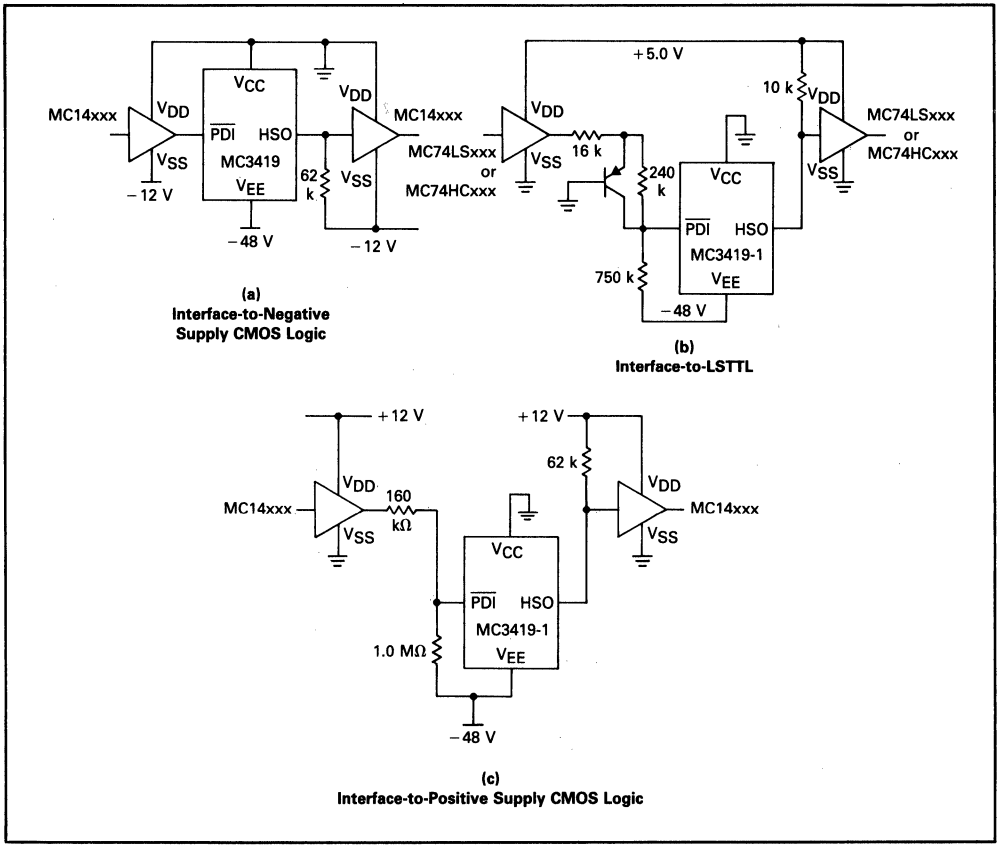
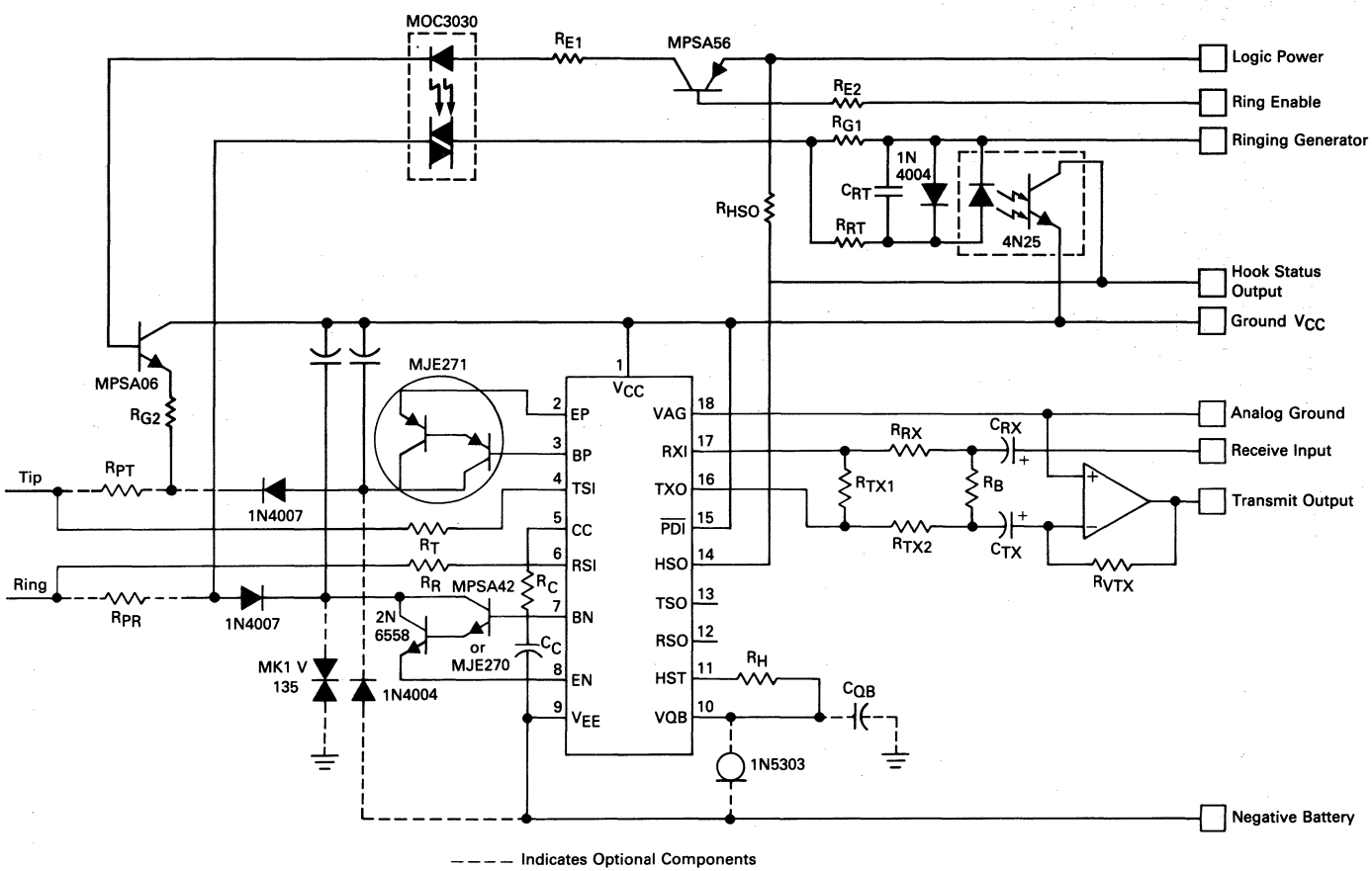


FIGURE 15 — PBX LINE CIRCUIT



SYSTEM EQUATIONS (continued)

on the Ring lead to exceed the power supply voltages, a 1N4007 and an MK1V-135 (Sidac) are used for protection. The forward voltage drop across the 1N4007, during normal operation, will not affect the parametric characteristics of the MC3419-1 since it is "inside" a feedback circuit. If the MJE270 is used, the MK1V-135 should be replaced with a lower voltage Sidac or MOSorb transient suppressor.

An optocoupled transistor circuit is used for ring trip detection on long lines. It samples only the ac and dc ringing signal current and uses a simple one pole filter to eliminate the low level ac signal. Under worst case conditions this circuit will ring trip in 1½ to 4 cycles. In systems serving only short loops (<700 Ω), if R_{G1} and R_{G2} are 620 Ω or greater, the optotransistor circuit is not needed, the Hook Status Output will perform ring trip on a Zero Crossing. The Ring Enable input and the Hook Status Output interface with standard CMOS and TTL logic.

The op amp in this circuit is an integral part of the following codecs, filters or combos:

MC3417/8 — MC145414
MC14404/6/7 — MC14413/4
MC14401/2/3/5

2

LONG LINES OFF-PREMISE LINES

Specifications

R_F	— 200 Ω	R_O	— 600 Ω	Off-Hook	— <2500 Ω
I_L(max)	— 60 mA	R_X Gain	— 0 dB 200–3400 Hz	On-Hook	— >10 kΩ
R_L(max)	— 1900 Ω	T_X Gain	— 0 dB 200–3400 Hz	Protection	— 1000 V
				Ringer Equivalent	— 5

V_{Logic}	—	+5.0 V	
V_{EE}	—	−42 to −56 Volts	
$V_{Ringing}$	—	(40 V to 120 V_{RMS}) + V_{EE}	

Parts List

MPSA56	R_R	—	9.09 k	1%	Matched
2N3905	R_T	—	9.09 k	1%	if desired
2N6558	R_{PT}	—	47 Ω	5%	
MPSA42	R_{PR}	—	75 Ω	5%	
MJE271	R_{G1}	—	620 Ω	5%	
1N4007	R_{G2}	—	100 Ω	5%	
MK1V135	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
1N4007	R_{RT}	—	20 k	5%	
1N5303	R_C	—	24 k	5%	
1N4004	R_H	—	127 k	1–3%	
MC3419-1	R_{HSO}	—	10 k	5%	

MOC3030	R_{TX1}	—	12.1 k	1%	
4N25	R_{TS2}	—	5.76 k	1%	
	R_{RX}	—	28.7 k	1%	
	R_B	—	28.0 k	1%	
	R_{VTX}	—	28.6 k	1%	
	C_T		0.004 μF		
	C_R	—	0.004 μF		
	C_C	—	0.001 μF		
	C_{RX}	—	1.0 μF/20 V		
	C_{TX}	—	2.0 μF/40 V		
	C_{RT}	—	20 μF/5.0 V		
	C_{QB}	—	10 μF/60 V		

SHORT LINES ON-PREMISE LINES

Specifications

R_F	—	500 Ω	
R_L(max)	—	700 Ω	
Ring Trip	—	<50 ms	
Ringer Equivalent	—	2.5	
R_O	—	600 Ω	

R_X Gain	—	−5.0 dB	
T_X Gain	—	0 dB	
V_{Logic}	—	+5.0 Volts	
V_{EE}	—	−20 to −56 Volts	
$V_{Ringing}$	—	(40 V to 70 V_{RMS}) + V_{EE}	

Parts List

MJE271	R_R	—	19.6 k	1%	
MJE270	R_T	—	19.6 k	1%	
MPSA56	R_{G1}	—	620 Ω	5%	
2N3905	R_{G2}	—	620 Ω	5%	
1N4007	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	

MOC3030				R_{HSO}	—	10 k	5%
				R_{TX1}	—	19.6 k	1%
C_T	—	0.004 μF		R_{TX2}	—	42.2 k	1%
C_R	—	0.004 μF		R_{RX}	—	69.8 k	1%
C_C	—	0.004 μF		R_B	—	301 k	1%
C_{RX}	—	0.1 μF		R_{VTX}	—	127 k	1%
C_{TX}	—	0.5 μF		R_C	—	56 k	5%

MC6172

(Formerly MC6862)

2

2400 bps DIGITAL MODULATOR

The MC6172 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The modulator provides the necessary modulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6172 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

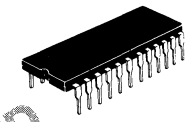
N-channel silicon-gate technology permits the MC6172 to operate using a single voltage supply and be fully TTL compatible.

The modulator is compatible with the MC6173 demodulator to provide medium-speed data communications capability.

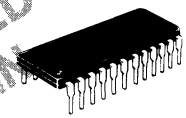
- Clear-to-Send Delay Options
- 511-Bit CCITT Test Pattern
- Terminal Interfaces are TTL Compatible
- Compatible Functions for 201B/C Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation
- Answer-Back Tone
- The MC6173 Is the Companion Demodulator
- Application Note Available — AN-870

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps MODULATOR



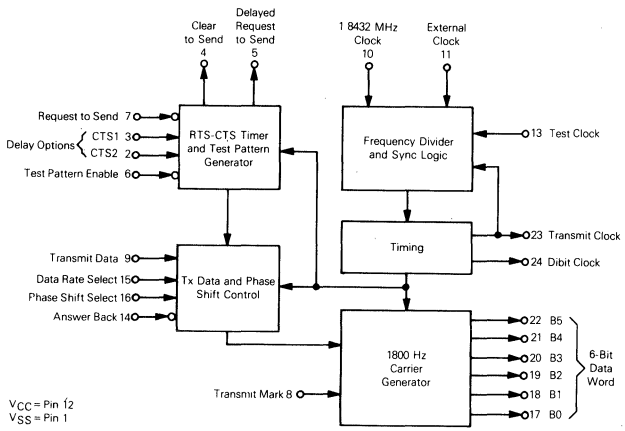
L SUFFIX
CERDIP PACKAGE
CASE 623



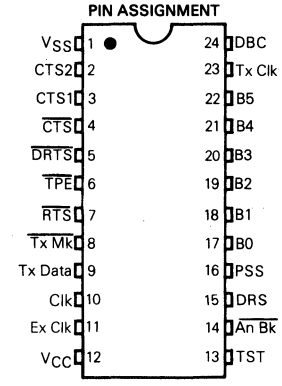
P SUFFIX
PLASTIC PACKAGE
CASE 709

NOT RECOMMENDED FOR NEW DESIGN

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	T_L to T_H 0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Package Cerdip Package	θ_{JA}	 120 65	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

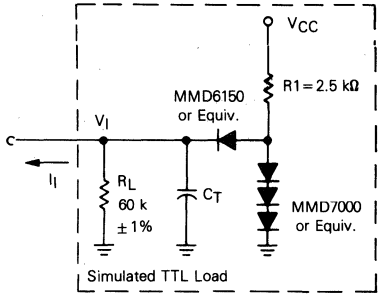
DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ±0.25 Vdc, V_{SS} = 0, $T_A = T_L$ to T_H, all outputs loaded as shown in Figure 1 unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	V
Input Current ($V_{in} = V_{SS}$) CTS1, CTS2, PSS, DRS, $\overline{An\ Bk}$, and $\overline{Tx\ MK}$ $\overline{RTS}$ and $\overline{TPE}$	I_{in}	– –	– –	−0.2 −1.6	mA
Input Leakage Current (V_{in} = 5.25 V, $V_{CC} = V_{SS}$)	I_{IL}	–	–	2.5	μA
Output High Voltage (I_{OH} = −0.04 mA, Load A) (I_{OH} = 0.0 mA, Load B)	 V_{OH1} V_{OH2}	 V_{SS} + 2.4 V_{CC} − 0.5 V	 – –	 V_{CC} V_{CC}	V
Output Low Voltage (I_{OL} = 1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (Measured at $T_A = T_L$) (All inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL outputs open)	P_{int}	–	210	315	mW
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% points)	t_r, t_f	–	–	1.0*	μs
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r, t_f	–	–	40	ns
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Tx Data Setup Time (Figure 2)	t_{su}	35	–	–	μs
Tx Data Hold Time (Figure 2)	t_h	35	–	–	μs
Output Transition Times	t_r, t_f	–	–	5.0	μs

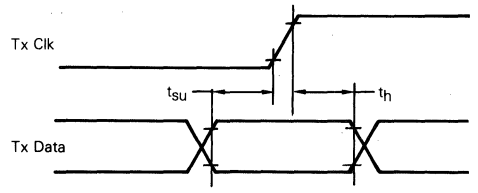
*Maximum Input Transition Times are ≤0.1 × Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 1 — OUTPUT TEST LOAD



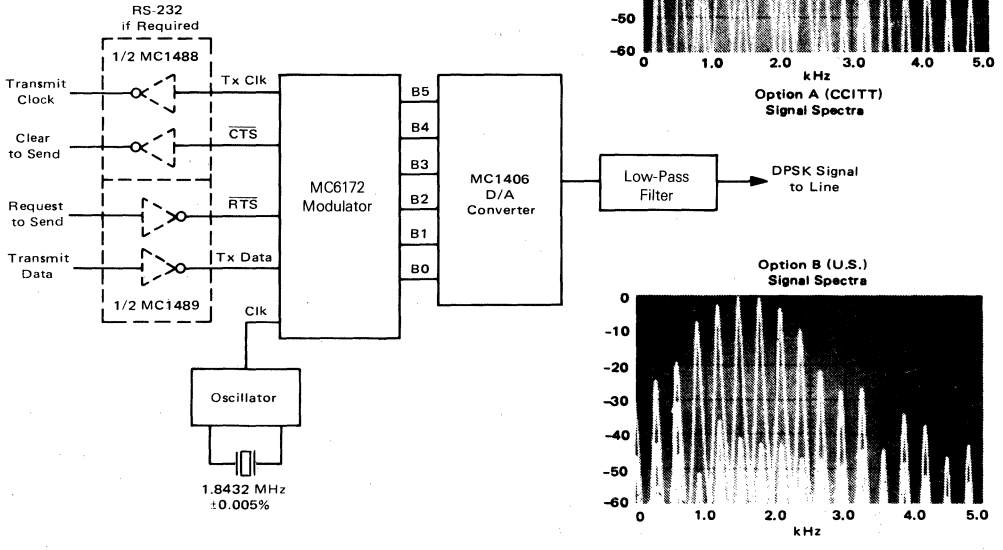
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 2 — TRANSMIT DATA SETUP AND HOLD TIME



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 3 — 2400 bps MODULATOR INTERFACE

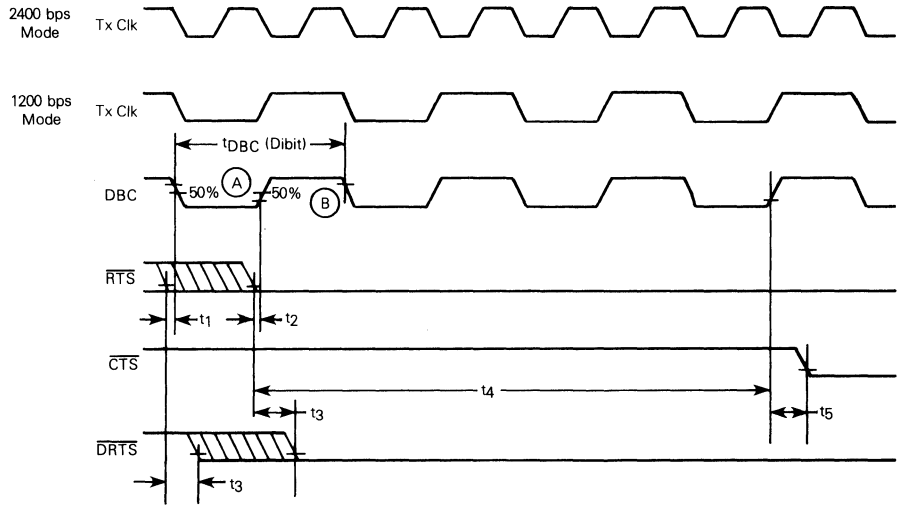


DELAY TIMINGS (See Figures 4 and 5)

Characteristic	Symbol	Min	Typ	Max	Unit
$\overline{RTS}$ to DBC Delay	t_1	–	–	8	μs
DBC to $\overline{RTS}$ Delay	t_2	45	–	–	μs
$\overline{RTS}$-$\overline{DRTS}$ Delay	t_3	–	–	35	μs
$\overline{RTS}$-$\overline{CTS}$ Delay					
CTS1=0, CTS2=1	t_4*	0	–	35	μs
CTS1=1, CTS2=0		8.55	–	9.35	ms
CTS1=1, CTS2=1		24.9	–	26.4	ms
CTS1=0, CTS2=0		147.0	–	154.0	ms
$\overline{CTS}$-DBC Delay					
CTS1=1, CTS2=0	t_5	–	–	35	μs
CTS1=1, CTS2=1		–	–	35	
CTS1=0, CTS2=0		–	–	35	
$\overline{RTS}$ to $\overline{CTS}$ Low	t_6	–	–	1.60	ms
$\overline{RTS}$ Min Delay	t_7	–	–	1.67	ms
DBC to $\overline{DRTS}$ Delay	t_8	–	–	35	μs
DBC Cycle Time	t_{DBC}	833.28	833.33	833.37	μs

*The reference frequency tolerance is not included.

FIGURE 4 — $\overline{RTS}$-$\overline{CTS}$ AND $\overline{RTS}$-$\overline{DRTS}$ DELAYS



$\overline{RTS}$-$\overline{CTS}$ delay options are selected by the CTS1 and CTS2 inputs, and are stated as time delay interval t_4. An $\overline{RTS}$ input signal synchronized about point A will synchronize $\overline{CTS}$ with the positive transition of DBC (Dibit Clock). Delay t_4 is measured with respect to the negative transition of $\overline{RTS}$.

$\overline{RTS}$ signals synchronized with the positive transition of DBC (point B), will result in the same $\overline{CTS}$ delay (t_4). For this case the negative transition of $\overline{CTS}$ is synchronized with the negative transition of DBC with delay t_4 measured with respect to the negative transition of $\overline{RTS}$.

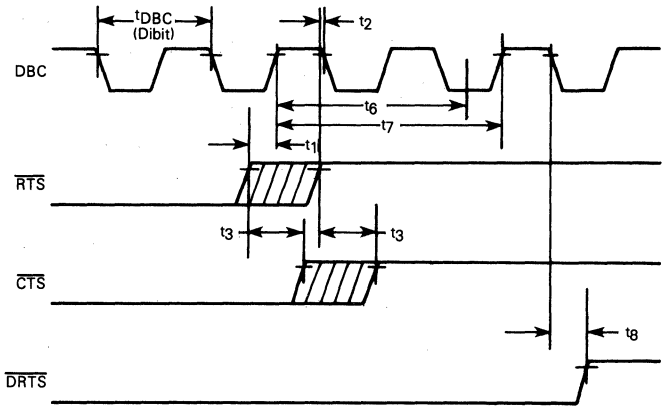
$\overline{DRTS}$ will go low within t_3 of the negative transition of $\overline{RTS}$. With the exception of the no-delay option, $\overline{CTS}$ will go low within t_5 of the positive transition of DBC, following the t_4 delay selected. This applies when $\overline{RTS}$ is synchronized to Point A as shown.

If $\overline{RTS}$ goes high and remains high ≥ 20 μs within time interval t_4, a reset of the internal $\overline{RTS}$-$\overline{CTS}$ timer function will occur. If $\overline{RTS}$ goes high for less than 20 μs, the circuit may or may not respond to this momentary loss of the $\overline{RTS}$ signal.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

2

FIGURE 5 — LOSS OF $\overline{RTS}$ TO $\overline{DRTS}$ DELAY



A positive transition of $\overline{RTS}$ after $\overline{CTS}$ has become active can result in different functional characteristics of the $\overline{CTS}$ and $\overline{DRTS}$ output signals, depending on the time duration that $\overline{RTS}$ remains inactive.

Under all conditions, $\overline{CTS}$ will go high within t_3 following a positive transition of $\overline{RTS}$. If $\overline{RTS}$ goes high in the shaded region shown (i.e., synchronized to the positive transition of DBC) and remains high beyond the time interval defined as t_7, then $\overline{DRTS}$ will go high within t_8 of the next negative transition of DBC. If $\overline{RTS}$ were to go low after t_7, the $\overline{RTS}$-$\overline{CTS}$ delay times given in Figure 4 will result.

If $\overline{RTS}$ goes high in the shaded region shown, and then returns low within time interval t_6, the negative transition of $\overline{CTS}$ will follow within 35 μs, and $\overline{DRTS}$ will remain in the active or low state. Under these conditions, the normal $\overline{RTS}$-$\overline{CTS}$ delay times are not encountered when $\overline{RTS}$ is reactivated. If $\overline{RTS}$ goes low for less than 20 μs, the circuit may or may not respond

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

DEVICE OPERATION

GENERAL

Figure 3 shows the modulator and its intra-connections. The data to be transmitted is presented in synchronous serial format to the modulator for conversion to DPSK signals used in transmission. The modulator output is digital; therefore, a D/A converter and a filter transform the signal to an analog form.

The control functions provide four different Clear-to-Send delay options. An Answer-Back tone is available for automatic answering applications. The modulator has a built-in 511-bit pseudorandom pattern generator for use in system diagnostic tests.

INPUT/OUTPUT FUNCTIONS

Request to Send ($\overline{RTS}$)

The $\overline{RTS}$ signal from the data terminal controls transmission from the modulator. A low level on $\overline{RTS}$ activates the modulator data output. A constant mark, for synchronization, is sent during the $\overline{RTS}$ to $\overline{CTS}$ delay interval. Termination of the transmission is accomplished by taking $\overline{RTS}$ high (see Figures 4 and 5).

Delayed Request to Send ($\overline{DRTS}$)

This output can be used to control transmission as specified by the Transmit Mark control input. $\overline{DRTS}$ follows the negative transition of $\overline{RTS}$, and goes negative within t_3 of the negative transition of $\overline{RTS}$ (Figure 4). The delay from a positive transition of $\overline{RTS}$ to a positive transition of $\overline{DRTS}$ is shown in Figure 5. The $\overline{DRTS}$ delay allows data within the modulator to be transmitted before transmission is inhibited.

Clear to Send ($\overline{CTS}$)

$\overline{CTS}$ follows $\overline{RTS}$ to both the logic 0 and logic 1 levels. The delay from a negative transition of $\overline{RTS}$ to a negative $\overline{CTS}$ transition is selectable by external strapping of CTS1 and CTS2. The delay from a positive transition of $\overline{RTS}$ to a positive $\overline{CTS}$ transition is less than t_4.

$\overline{CTS}$ will go low within t_5 after the positive transition of the Dibit Clock (see Figure 4) except when the non-delay option is selected. For the no-delay option, $\overline{CTS}$ follows $\overline{RTS}$ within t_5.

$\overline{RTS}$-$\overline{CTS}$ Delay Options (CTS1, CTS2)

The $\overline{RTS}$-$\overline{CTS}$ delays are selectable according to the following strapping options

$\overline{RTS}$-$\overline{CTS}$ Delay	CTS1	CTS2
0.0 + 0.035 ms, −0.0 ms	0	1
8.55 to 9.35 ms	1	0
24.90 to 26.4 ms	1	1
147.0 to 154.0 ms	0	0

Transmit Mark (Tx Mk)

The Transmit Mark control allows the system designer to select whether the Delayed Request to Send activitates and deactivates the transmission on the modulator chip or off the chip in the output amplifier.

When Tx Mk is high, transmission is controlled on the modulator chip, and occurs from the chip only when $\overline{DRTS}$ or Answer Back is in the logic 0 state (see Figure 6).

When Tx Mk is low, transmission is controlled off the modulator chip. In this mode, the modulator chip transmits marks at all times except when data or an Answer-Back tone is being transmitted (see Figure 6).

Test Pattern Enable ($\overline{TPE}$)

A 511-bit test pattern generator is contained on the modulator chip. This pattern is in accord with CCITT specification V52.

The 511-bit test pattern is activated by applying a logic 0 to $\overline{TPE}$. A mark (logic 1) condition on the Transmit Data input with $\overline{TPE}$ activated (logic 0) causes the test pattern to appear at the data output. A space (logic 0) condition on Tx Data with $\overline{TPE}$ activated causes the test pattern data to appear inverted at the data output.

Although the Motorola 2400 bps modulator contains a CCITT 511 test pattern generator it does not incorporate the 511 data randomizer or scrambler.

Random data applied to Tx Data with TPE activated causes the test pattern data to be scrambled (exclusive NORed) with the data, and the result appears at the data output.

The MC6173 demodulator does contain a built-in data descrambler, which is enabled by $\overline{TPE}$ input going active. To scramble data using the modulator, the circuit in Figure 7 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern. Then the data is delayed by a full data bit before being transmitted by the modem. This assures a proper Transmit Data/Transmit Clock phase relationship.

If the data scrambler is to be an optional feature, then the transmit data multiplexer would also have to be built. This is selected by the Test Pattern Enable signal or any other signal that is found suitable.

The scrambling of data in the data comm environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that with respect to the modem carrier, there is always random data on the line with little chance for a long string of ones or zeros to exist. This is particularly important if an adaptive equalizer is being incorporated at the demodulator. The adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is exclusive ORed with data.

The test pattern generator can be enabled only when $\overline{CTS}$ and $\overline{RTS}$ are logic 0. If $\overline{TPE}$ is activated outside this time interval, the previously stated $\overline{RTS}$-$\overline{CTS}$ and $\overline{RTS}$-$\overline{DRTS}$ delays, shown in Figures 4 and 5, are not valid.

Data-Rate Select (DRS)

The modulator can transmit at either 2400 bps or 1200 bps. Both data rates utilize an 1800 Hz carrier signal and employ phase shifting at 1200 Hz. The 2400 bps rate is obtained by encoding two bits of data into each phase shift. The 2400 Hz rate is selected by applying a logic 1 to the Data-Rate Select lead. The 1200 Hz rate is selected by applying a logic 0 to DRS.

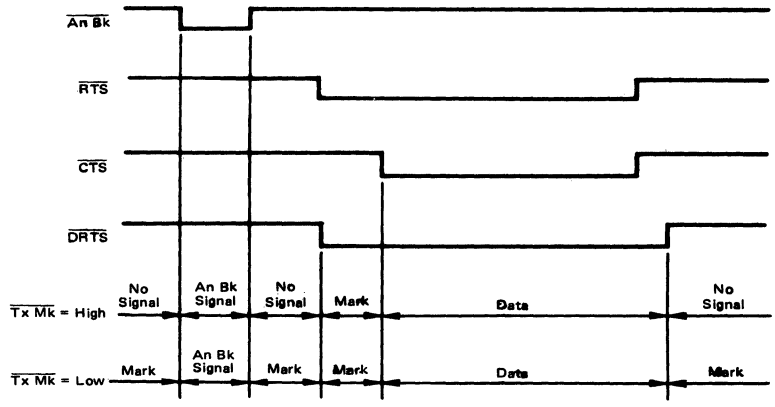
Phase-Shift Select (PSS)

Option A (CCITT) or Option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A*	PSS = 1 Option B
00	0°	+45°
01	+90°	+135°
11	+180°	+225°
10	+270°	+315°

*See example Figure 8.

FIGURE 6 — TRANSMIT MARK CONTROL



2

FIGURE 7 — MODULATOR CCITT 511 DATA SCRAMBLER

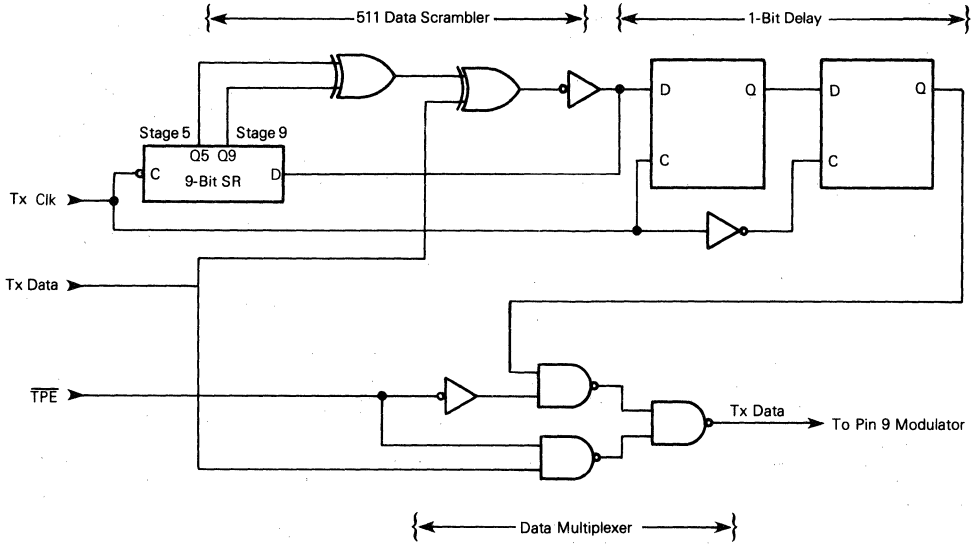
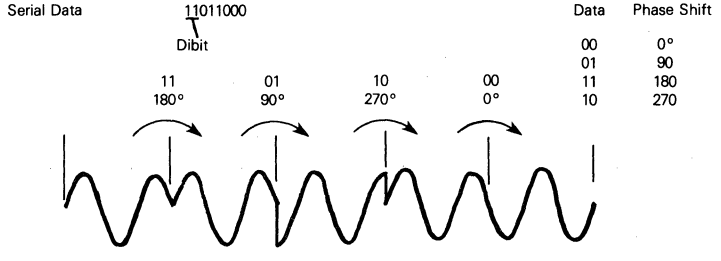


FIGURE 8 — EXAMPLE-CARRIER PHASE SHIFTS FOR OPTION A



For 1200 bps operation, Option C (CCITT) or Option D (U.S.) phase shift can be selected:

Data	PSS = 0 Option C	PSS = 1 Option D
0	+90°	+45°
1	+270°	+225°

Option C is selected by applying a logic 0 to the Phase Shift Select lead when the Data Rate Select lead is strapped for 1200 bps operation (logic 0). Option D is selected by applying a logic 1 to PSS with DRS at logic 0. The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

Transmit Data (Tx Data)

Transmit Data is the serial binary information presented for DPSK modulation. A high level represents a mark. For timing, see Transmit Clock (Figure 4).

Transmit Clock (Tx Clk)

A 2400/1200 Hz Transmit Clock output is provided for the communication terminal. The Transmit Data signal is sampled on the positive transition of Transmit Clock. The Transmit Data to Transmit Clock setup and hold time requirements are shown in the Electrical Characteristics Table and in Figure 2.

Dibit Clock (DBC)

A 1200 Hz Dibit Clock identifies the modulation timing. This signal goes negative less than 100 μs prior to the start of dibit modulation.

External Clock (Ex Clk)

A 2400/1200 Hz clock signal applied to the External Clock lead causes Transmit Clock to be synchronized with Ex Clk. This input must have an accuracy within ±0.005%.

When no transitions occur on this input, the internal clock provides the 2400/1200 Hz transmit timing signal. Fast synchronization of Tx Clk to Ex Clk is not provided on the chip. *When Ex Clk is not used, it should be tied to either the logic 0 or logic 1 state.*

1.8432 MHz (Clk)

This input must be a square wave with rise and fall times of less than 40 ns and a 50 ±20% duty cycle. The clock accuracy must be written ±0.005%.

Answer Back ($\overline{\text{An Bk}}$)

A logic 0 level applied to Answer Back causes a 2025 Hz carrier to be generated on the modulator chip instead of a phase shifted 1800 Hz carrier. A logic 1 level applied to $\overline{\text{An Bk}}$ enables the modulator to generate the normal phase shifted 1800 Hz carrier signal, as shown in Figure 6. The time delay from a transition on $\overline{\text{An Bk}}$ to the appropriate signal at the modulator chip output is less than 2 ms.

Activation of $\overline{\text{An Bk}}$ (a logic 0) will disable all other operation modes including the $\overline{\text{Tx Mk}}$ function, and will reset $\overline{\text{CTS}}$ to an inactive state along with the $\overline{\text{RTX}}$-$\overline{\text{CTS}}$ internal timer. $\overline{\text{An Bk}}$ should therefore be activated only before initiating $\overline{\text{RTS}}$ or after loss of the $\overline{\text{DRTS}}$ output signal. The combination of a logic 0 on $\overline{\text{An Bk}}$ with a logic 0 on $\overline{\text{TPE}}$ is not used in normal system operation, and hence is used as a reset input during device test.

Digital Output (B0-B5)

These outputs are designed to interface with a 6-bit digital-to-analog converter. The resultant signal out of the D/A is the differential phase shift keyed signal quantized at a 14.4 kHz rate. A low-pass filter can then be used to smooth the data transitions. B0 is the least-significant bit, and the positive level the active state.

Test Clock (TST)

A test signal input is provided to decrease test time of the chip. *In normal operation this input must be strapped low.*

MC6173

2

2400 bps DIGITAL DEMODULATOR

The MC6173 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

The demodulator provides the necessary demodulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6173 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

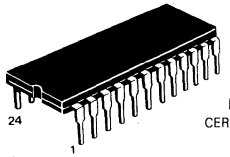
N-channel silicon gate technology permits the MC6173 to operate using a single voltage supply and be fully TTL compatible.

The demodulator is compatible with the M6800 microcomputer family, and provides medium-speed data communications capability.

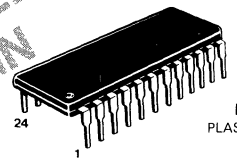
- Compatible with MC6172 Modulator
- 511-Bit CCITT V.52 Test Pattern
- Terminal Interfaces Are TTL Compatible
- Compatible Functions for 201B/C and V.26 Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation

MOS
(N-CHANNEL, SILICON-GATE)

2400 bps DEMODULATOR



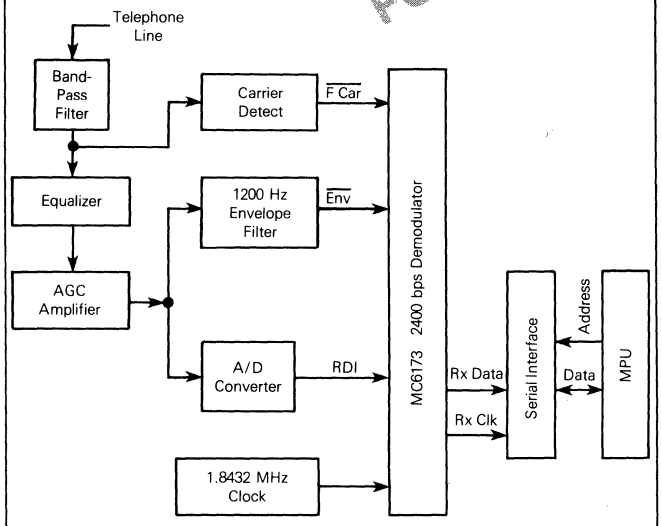
L SUFFIX
CERDIP PACKAGE
CASE 623



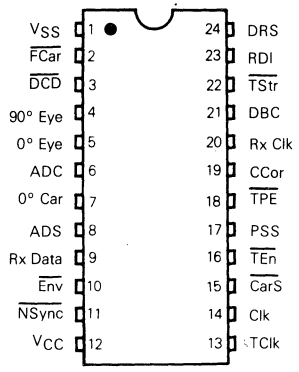
P SUFFIX
PLASTIC PACKAGE
CASE 709

NOT RECOMMENDED FOR NEW DESIGN

FIGURE 1 — TYPICAL APPLICATIONS



PIN ASSIGNMENT



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{SS}).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 ±0.25 Vdc, V_{SS} = 0, $T_A = T_L$ to T_H all outputs loaded as shown in Figure 3 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS}+0.8	V
Input Current ($V_{in} = V_{IL}$) Pins 3, 11, 13, 15, 16, 17, 18, 22, 24	I_{IL}	–	–	−0.2	mA
Input Leakage Current (V_{in} = 5.25 Vdc, $V_{CC} = V_{SS}$) Pins 2, 10, 14, 23	I_{in}	–	–	2.5	μA
Output High Voltage (I_{OH} = −0.04 mA, Load A) (I_{OH} = 0.0 mA, Load B)	V_{OH1} V_{OH2}	V_{SS}+2.4 V_{CC}−0.5 V	– –	V_{CC} V_{CC}	V
Output Low Voltage (I_{OL} = 1.6 mA, Load A)	V_{OL}	V_{SS}	–	V_{SS}+0.4	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Internal Power Dissipation (measured at $T_A = T_L$) (All Inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL Outputs Open)	P_{Int}	–		630	mW
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r t_f	– –	– –	40 40	ns
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% Points)	t_r, t_f	–	–	1.0*	μs
Output Transition Times (From 10% to 90% Points)	t_r, t_f	–	–	5.0	μs
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Data Setup Time	t_{DS}	770	–	–	ns
Rx Data Setup Time	t_{su}	35	–	–	μs
Data Hold Time	$t_{h(D)}$	0	–	–	ns
Rx Data Hold Time	t_h	35	–	–	μs
Data-Clamp Delay Time Option 1 Option 2 Option 3 Option 4	 t_{DCD1} t_{DCD2} t_{DCD3} t_{DCD4}	 5.7 4.135 20.795 104.135	 6 4.17 20.83 104.17	 6.3 4.205 20.865 104.205	 ns ms ms ms
A/D Clock to A/D Strobe Delay Time	t_{ADCD}	1.06	–	1.11	μs
Envelope-to-Dibit Clock Delay Time	t_{ED}	140	–	220	μs
Clock Frequency, ±0.005%	f_{Clk}	–	1.8432	–	MHz
A/D Clock Cycle Time (f_{Clk}/4)	t_{cyc}	–	2.17	–	μs
A/D Clock Pulse Width	$t_{w(ADC)}$	940	1000	1040	ns
A/D Strobe Pulse Width	$t_{w(ADS)}$	–	10.85	–	ns
New Sync Input Pulse Width	$t_{w(NSync)}$	0.84	–	–	ms

*Maximum input transition times are ≤ 0.1X pulse width or the specified maximum of 1.0 μs, whichever is smaller.

2

FIGURE 2 — DEMODULATOR BLOCK DIAGRAM

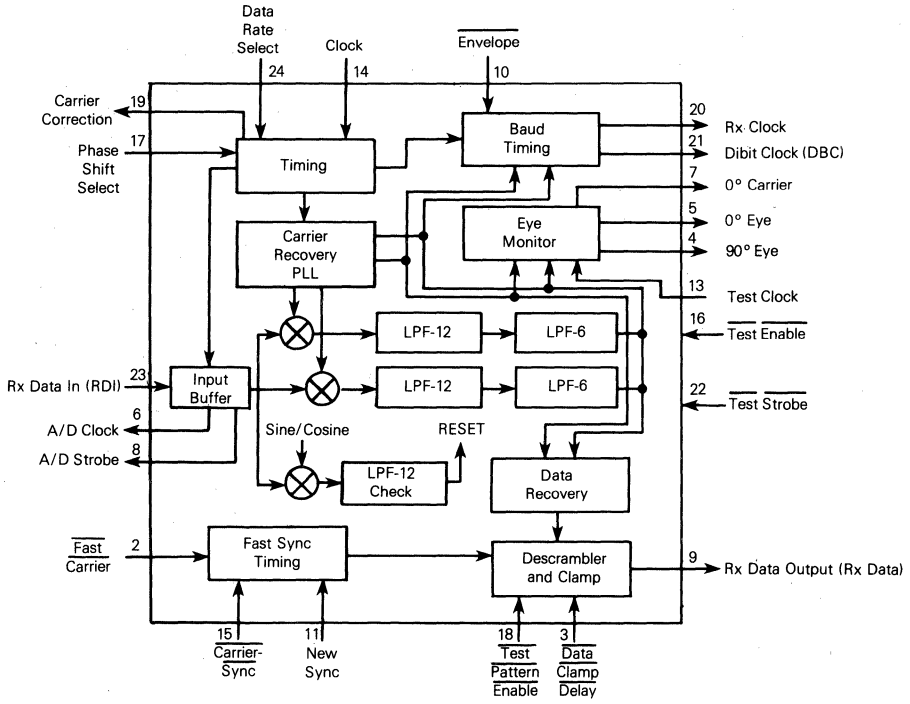
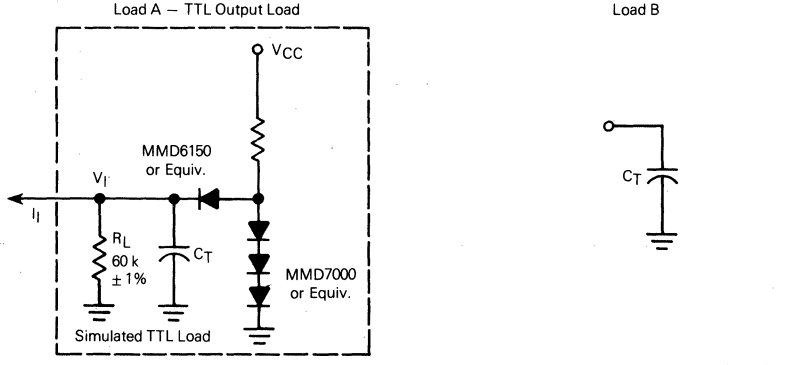


FIGURE 3 — OUTPUT TEST LOADS



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances

GENERAL DESCRIPTION

The MC6173 Phase-Shift Key (PSK) Demodulator serves as an integral part of a system to recover synchronous data from an 1800 Hz PSK modulated carrier. Data rates of 1200 and 2400 bits-per-second are available. In the case of 1200 bps operation, the MC6173 detects phase shifts of 0 to 180 degrees to represent digital "0s" and "1s". When 2400 bps operations is desired, the MC6173 detects phase shifts of 0, 90, 180, and 270 (option A) or 45, 135, 225, and 315 (option B) degrees to represent two bits of data called dibits. These phase shifts decode to 00, 01, 10, and 11, respectively. In either data rate, the 1800 Hz carrier is modulated at a 1200 rate.

Figure 1 shows the MC6173 demodulator in a typical application. The band-pass filter, equalizer, analog-to-digital (A/D) converter, 1200 Hz envelope filter, AGC amplifier, and 1800 Hz carrier detector are external to the MC6173. The band-pass filter passes roughly 300 Hz to 3000 Hz eliminating noise, 60 Hz and 120 Hz pickup, and harmonics of 1800 Hz. The output of this filter is fed to the equalizer which adjusts phase versus amplitude such that a constant amplitude is maintained regardless of phase and is fed into the carrier detect circuit. The AGC amplifier provides a constant level signal regardless of the input level from the equalizer. The output of the AGC amplifier drives two basic sections of external circuitry, i.e., the A/D converter, and 1200 Hz envelope filter.

The A/D converter samples each 1200 Hz cycle or dibit 12 times. After each sample, digital data is clocked serially to the MC6173 receiver data input (RDI). The MC6173 generates the sampling clock for AD Strobe (ADS) and the serial clock (ADC) from the 1.8432 MHz internal oscillator.

The 1200 Hz envelope filter recovers the 1200 Hz component of the equalizer output during fast training and generates a 1200 Hz square wave. This square wave is connected to the envelope ($\overline{Env}$) input and is used for internal timing.

The carrier detect circuit is used to signal the fast carrier ($\overline{FCar}$) input that a carrier is present. Immediately after $\overline{FCar}$ has received a negative transition, the internal phase-lock loop temporarily widens its band width so that it can quickly adjust the internal timing of the MC6173 with respect to the 1200 Hz $\overline{Env}$ input (this is called fast Sync or fast training). The timing adjustments are made so that each dibit can be sampled at the most advantageous places.

The internal circuitry digests the dibit samples and produces the digital data (Rx Data) along with the receive data clock (Rx Clk). These two signals are used to drive a serial-to-parallel interface such as an MC6852 Synchronous Serial Interface Adapter.

PIN DESCRIPTION

FAST CARRIER ($\overline{FCar}$), Pin 2 — A negative transition on this input will force a period of approximately 8.3 ms of fast training for both baud and carrier timing.* Fast Sync or fast training allows for large corrections to be made in the internal timing of the demodulator. After the fast training period, the timing should be reasonably well adjusted. Small adjustments are made automatically to maintain proper phase relationships internally after the fast-train period.

The $\overline{FCar}$ input, which normally comes from the carrier threshold detect circuits, must remain at a low level during the entire period of baud and carrier synchronization.

A positive level on the $\overline{FCar}$ input will disable the baud and carrier correction circuitry. Baud and carrier timing are then direct derivatives of the 1.8432 MHz clock as illustrated in Figure 4.

The first positive edge of the envelope ($\overline{Env}$) input will be totally asynchronous to the demodulator. This will be $\pm$ ½ cycle of the 2400 clock ($\pm$ 208 μs). The nine following positive edges will introduce added tolerance equal to nine times the offset of $\overline{Env}$ from the absolute 1200 Hz (as defined by the 1.8432 MHz $\pm$0.005% clock). Thus . . .

$$\text{Max Fast Train Time} = 4.17\ \text{ms} + 9\ f_{\overline{Env}} + 0.21\ \text{ms}$$
$$= 4.38\ \text{ms} + 9/f_{\overline{Env}}$$
$$\text{Min Fast Train Time} = 4.17\ \text{ms} - 0.21\ \text{ms} + 9/f_{\overline{Env}}$$
$$= 3.96\ \text{ms} + 9/f_{\overline{Env}}$$

DATA-CLAMP DELAY ($\overline{DCD}$), Pin 3 — Data-clamp delay enables the selection of one of four delays during which Rx Data is held to a logic-high condition. This delay is measured from the negative edge of $\overline{FCar}$. The four options are available at one pin through the use of the internal multiplexing in the demodulator. Options 3 and 4 are available by demultiplexing the dibit clock as demonstrated in Figure 5. The available delay options are listed in Table 1, these times will be approximate due to their direct relationship to the $\overline{Env}$ input during the first 8.3 ms. Also, these times are further dependent upon carrier offset. The delays given in Table 1 assume no carrier offset and that $\overline{Env}$ is synchronous with the Tx Clk. Figure 4 is illustrative of the timing and sequencing of this circuit.

A scheme for programming the data-clamp delay is illustrated in Figure 5. The $\overline{DCD}$ input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock options 3 and 4 are produced at the same input pin.

ENVELOPE ($\overline{Env}$), Pin 10 — The envelope input comes from the 1200 Hz envelope detection circuitry. Envelope detection will normally consist of a 1200 Hz filter and a voltage comparator to generate an approximate limited square wave. This is normally derived from a constant mark signal sent by the modulator for Sync acquisition purposes.

Each positive edge that is input to $\overline{Env}$ will reset both baud timing and the dibit clock to a logic "0". The optimum timing of the positive transition at the $\overline{Env}$ input will be t_{ED} prior to the falling edge of the dibit clock. Timing is illustrated in Figure 6.

$\overline{Env}$ will be effective in the training of baud timing and dibit clock only if $\overline{FCar}$ is in the active low state.

Minimum positive pulse width at the $\overline{Env}$ is $\geq$2.17 μs.

NEW-SYNC ($\overline{NSync}$), Pin 11 — This input port is normally controlled by the business machine. If $\overline{FCar}$ is at an active low, then an active low pulse in excess of 0.84 ms on the $\overline{NSync}$ lead will put the demodulator into the fast-Sync

*The postive transition of the 1200 Hz signal, present at the $\overline{Env}$ input, provides a divide-by-20 counter with every other clock. This will cause approximately 8.3 ms of fast training to the incoming signal at the demodulator.

2

FIGURE 4 — DEMODULATOR SYNC TIMING DIAGRAM

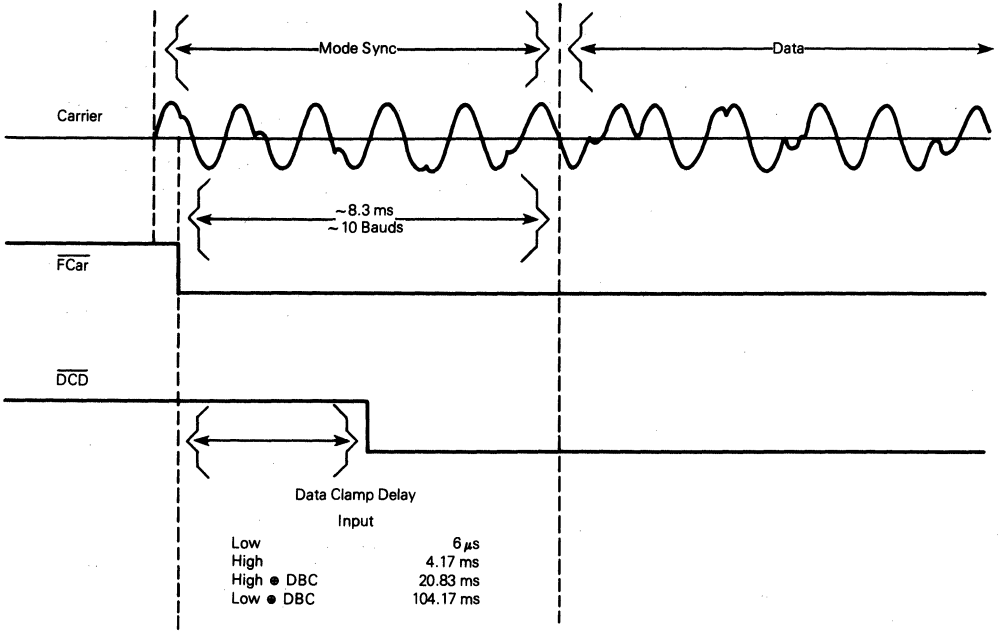


TABLE 1 — DATA-CLAMP DELAY OPTIONS

Option	A	C	$\overline{DCD}$	Data-Clamp Delay
1	1	0	0	6 μs
2	0	0	1	4.17 ms ± 35 μs
3	1	DBC	DBC	20.83 ms ± 35 μs
4	0	DBC	$\overline{DBC}$	104.17 ms ± 35 μs

FIGURE 5 — DATA-CLAMP DELAY DEMULTIPLEXER

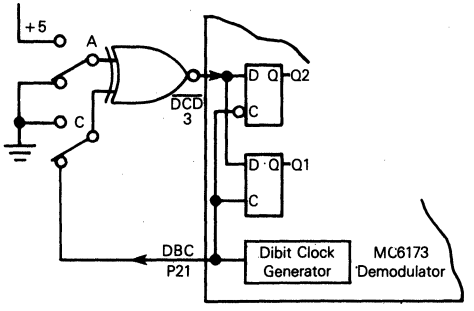
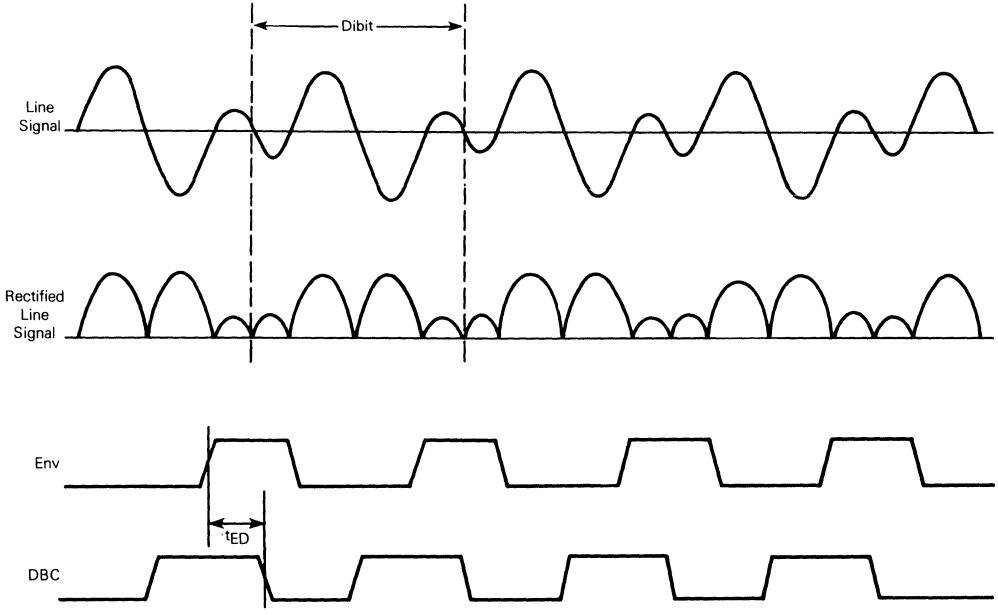


FIGURE 6 — ENVELOPE CLOCK TIMING DIAGRAM



or fast-train mode (these terms are synonymous).

Activation of $\overline{\text{NSync}}$ allows large corrections to be made to both baud and carrier timing similar to initial activation of the $\overline{\text{FCar}}$ lead. These corrections will be applied for approximately 8.3 ms. The receiver must complete the 8.3 ms period of fast Sync before another $\overline{\text{NSync}}$ is recognized.

$\overline{\text{CARRIER-SYNC}}$ ($\overline{\text{CarS}}$), Pin 15 — When $\overline{\text{CarS}}$ is taken to an active low, baud timing will be taken from the $\overline{\text{Env}}$ input. In addition, the slow carrier correction will be doubled in the 2400 baud mode as defined by the data-rate select (DRS) and phase-shift select (PSS) inputs. (This is not the same as the fast training that is incorporated when $\overline{\text{FCar}}$ or $\overline{\text{NSync}}$ are active, which is a changing of the bandwidth of the internal phase-lock loop [PLL]). This widening of the PLL band width will allow a faster search and lock on the 1800 Hz carrier. This Carrier-Sync mode will remain active as long as $\overline{\text{CarS}}$ is held in the active state. The normal application of this option would be to extend the training or Sync time under the mark input data condition that exceeds 8.3 ms.

If $\overline{\text{FCar}}$ is at a logic "1" inactive state, this input is ignored by the demodulator.

A/D CLOCK (ADC), Pin 6 — This output will allow, in a serial format, the six A/D data bits plus sign information to be synchronously clocked into the demodulator. (See Figure 8.)

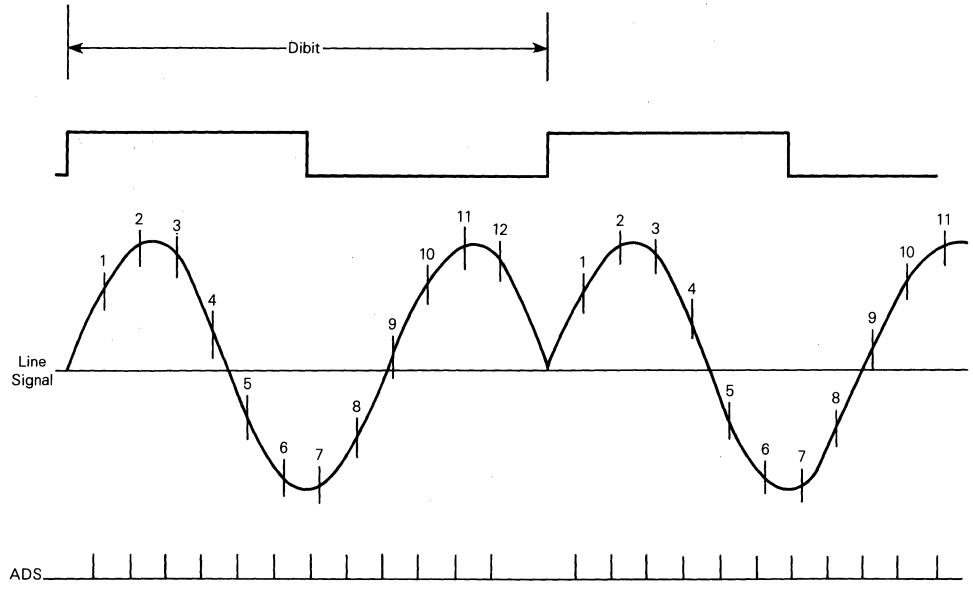
There are nine 1 μs positive pulses occuring at a 460 kHz rate. The first pulse, along with ADS, is used to begin the A/D conversion sequence. The next seven positive edges strobe data serially from the A/D converter to the demodulator input (RDI) enabling the demodulator to properly decode the A/D data.

This signal is also used to clock 0 and 90 degree eye data out of the demodulator. This is described in the Eye Pattern section. When $\overline{\text{TEn}}$ is low, ADC monitors check accumulator output (see $\overline{\text{TEn}}$).

A/D STROBE (ADS), Pin 8 — A positive going, approximately 11 μs, pulse is used as an enable signal for a sample and hold circuit prior to the A/D converter. The negative edge of this pulse is used to start the conversion process. Pulse rate of this signal is 14.4 kHz which allows each dibit to be sampled 12 times. (See Figure 7.) When $\overline{\text{TEn}}$ is low, ADS monitors zero crossings (see $\overline{\text{TEn}}$).

RECEIVER DATA INPUT (RDI), Pin 23 — The digital decode of the line signal magnitude, as sampled by the A/D, is input to the demodulator at this port. The data format is scaled binary. This sign bit occurs on the second A/D clock, followed by six magnitude bits which begin with the most-significant bit as shown in Figure 8. The data is strobed syn-

FIGURE 7 — ANALOG TO DIGITAL SAMPLE SCHEME



chronously with the positive edges of the ADC.

A logic one in the sign bit slot will represent a positive value. The magnitude of the six data bits increases from 000000 to 111111 with all ones always representing the most-positive value as illustrated below:

Sign	MSB					LSB	Value
1	1	1	1	1	1	1	+63
1	0	0	0	0	0	0	0
0	1	1	1	1	1	1	−0
0	0	0	0	0	0	0	−63

RECEIVE DATA OUTPUT (Rx Data), Pin 9 — This pin is the demodulator output for mark and space serial data. Data is synchronous with the receiver clock output with the positive going edge of the receiver clock occurring in the center of the data bit. A mark is represented by a logic high ("1") level except for the conditions described under PSS and $\overline{TPE}$.

The Rx Data output is inhibited in a logic-high level when $\overline{FCar}$ is in the inactive high state. The delay from the positive edge of $\overline{FCar}$ to the inhibiting of data is 2 μs.

RECEIVE CLOCK (Rx Clk), Pin 20 — The receive clock output provides the 2400 Hz ±0.005% timing signal to the business machine for sampling the demodulated received data marks and spaces (Rx Data). Receive clock is present at the demodulator chip output at all times; is not clamped to an inactive state when the carrier detected is not presented on $\overline{FCar}$; nor is Rx Clk clamped by any other combination of inputs to the demodulator.

Timing corrections to the receive clock, that are generated internally, are made following $\overline{FCar}$ going active. As described in $\overline{FCar}$, if $\overline{CarS}$ is held active the receive clock is continuously updated from dibit Sync.

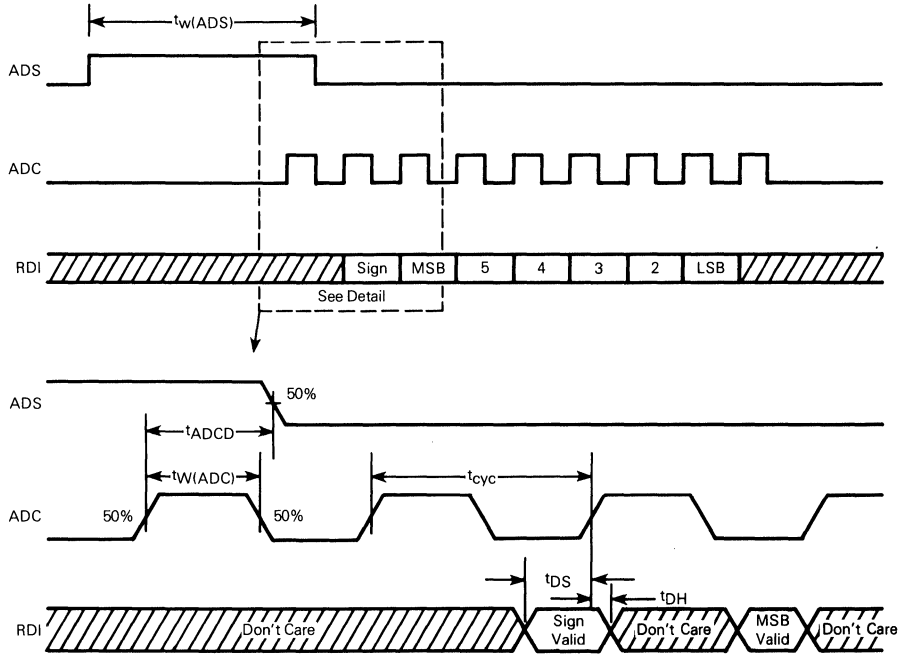
The positive transition of the Receive Clock, which occurs in the middle of the data bit, should be used to strobe data from the demodulator, under normal operating conditions. When $\overline{TPE}$ scrambler/descrambler is being incorporated, then the negative edge of the Rx Clk will occur in the center of the data bit.

Receive Clock will be 2400 bps or 1200 bps depending on the logic input at the DRS input. The Rx Clk edges described above apply to either 2400 bps or 1200 bps data rates.

Under $\overline{TPE}$ active, the Dibit relation to Rx Clk does not change. See Figure 9 for relative timing of Rx Clk, DBC and Rx Data.

Figure 10 depicts the requirements at the demodulator if the data scrambler is being incorporated. The exclusive Nor gating of $\overline{TPE}$ and Rx Clk would then maintain proper phasing of Rx Clk as it goes to the RS-232 driver. This circuit would be required since the positive edge of Receive Clock is a Data Communications Standard.

FIGURE 8 — ANALOG-TO-DIGITAL TIMING DIAGRAM



DATA RATE SELECT (DRS), Pin 24 — The following levels are valid for either phase-shift select:

Logic high equals 2400 bps,
Logic low equals 1200 bps.

PHASE-SHIFT SELECT (PSS), Pin 17 — Option A (CCITT) or option B (U.S.) phase shift can be selected for 2400 bps operation. The input data format and phase shift relationship for these two options are as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
00	0	+45
01	+90	+135
11	+180	+225
10	+270	+315

For 1200 bps operation, option A (CCITT) or option B (U.S.) phase shift can be selected as follows:

Data	PSS = 0 Option A (Degrees)	PSS = 1 Option B (Degrees)
0	+90	+45
1	+270	+225

The phase shifts shown are the difference in phase between the signal at the end of one dibit period and the new signal at the beginning of the next dibit.

If the logic level inputs to PSS are EXORed with DBC (dibit clock) or $\overline{DBC}$, then the test-pattern enable option may be selected and produce the compliment of normal data at Rx Data as explained in the $\overline{TPE}$ description. (See Figure 11.)

$\overline{TEST\text{-}PATTERN\ ENABLE}$ ($\overline{TPE}$), Pin 18 — Incorporated in the demodulator is the 511-bit test pattern shift register that is in accord with CCITT specification V52. This is the pattern that is generated by feedback from the 5th and 9th stages of a 9-bit shift register.

When the $\overline{TPE}$ input is allowed to be pulled up internally, there is normal data flow through the receiver. When the $\overline{TPE}$ input is pulled low, the incoming data is passed through this self-synchronous decoder which will produce the inverse of the 511-bit CCITT V52 pattern.

$\overline{TPE}$ works in coordination with PSS. If PSS is directly pulled high or low to represent option A or option B, then the presence of the 511-test pattern at the (RDI) input and $\overline{TPE}$ active will result in logic "1" condition at Rx Data output. If the DBC option is being utilized at the PSS input and $\overline{TPE}$ is active while the 511-bit test pattern is being received, the receiver data output will equal a logic "0". These options (Figure 11) are summarized in Table 2.

2

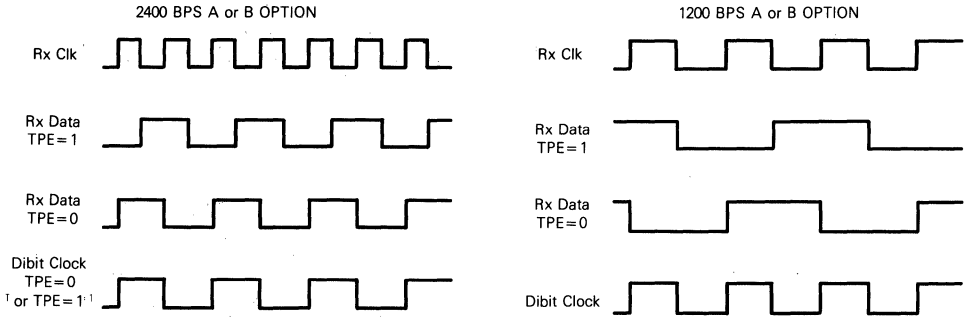
This assumes the modulator is sending the 511-bit test pattern with Rx Data being either a constant mark (logic "1") or space (logic "0"). If a logic "0" is received in options 1 or 2 or a logic "1" is received in options 3 or 4, then a transmission error has occurred. The number of errors-per-unit time is a measure of the transmission line quality.

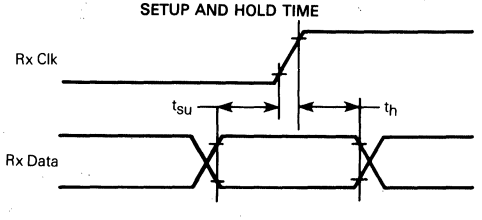
A feature of the above type of pattern detector is that it will be self-synchronizing. It should be pointed out that there will be at least two error counts each time an error is detected.

If the $\overline{TPE}$ input is in the active state, it is important to note that the Rx Clk phase changes. The necessary circuit to regain proper phase is shown in Figure 10.

A scheme for programming the phase-shift select is illustrated in Figure 11. The PSS input may either be a constant high or low level which will produce options 1 and 2. If the input "A" is exclusive ORed with the dibit clock, options 3 and 4 are produced at the same input pin.

FIGURE 9 — CLOCK TIMING DIAGRAM





Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 10 — DEMODULATOR DATA SCRAMBLER RECEIVE CLOCK PHASE CORRECTION REQUIREMENTS

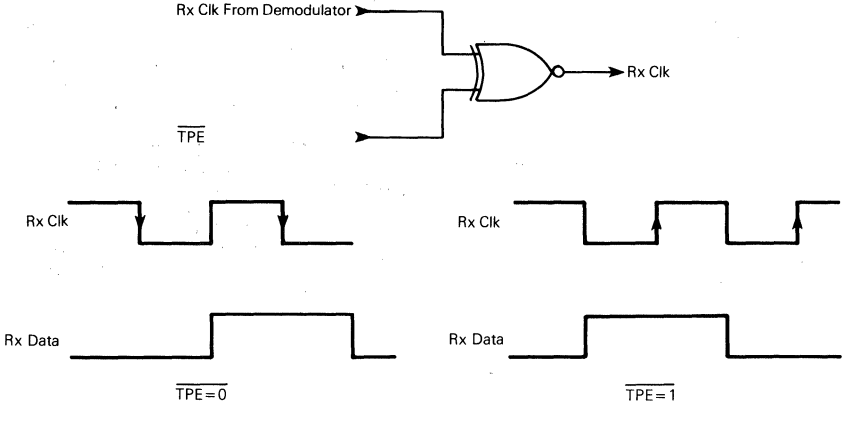


FIGURE 11 — PHASE-SHIFT SELECT DEMULTIPLEXER FOR TEST PATTERN ENABLE

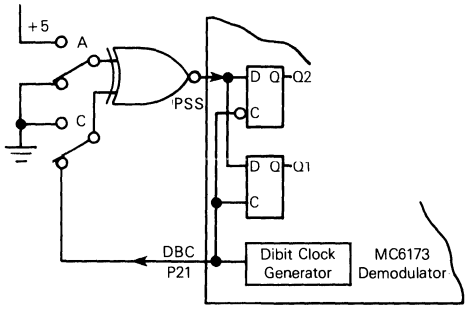


TABLE 2 — TEST PATTERN ENABLE OPTIONS

Option	$\overline{TPE}$	A	C	Phase Option	PSS	Output State
1	0	1	0	A	0	Rx Data Output = 1
2	0	0	0	B	1	Rx Data Output = 1
3	0	1	DBC	A	DBC	Rx Data Output = 0
4	0	0	DBC	B	$\overline{DBC}$	Rx Data Output = 0

CLOCK (Clk), Pin 14 — A 1.8432 MHz signal input ±0.005% is required at this port. The clock requirements are the same as the modulator clock specifications. See Figure 12 for a suggested clock circuit.

The receive clock is generated by dividing down the 1.8432 MHz. Since receive clock accuracy must be at least ±0.005%, the clock source must be of the same accuracy.

TEST-CLOCK (TClk), Pin 13 — This input is used for production testing of the demodulator device. In normal operation this pin should be left open which will enable the internal pullup resistor.

Pin 5	0 Degree Eye
Pin 4	90 Degree Eye
Pin 7	0 Degree Carrier
Pin 19	Carrier Correction

These test outputs are explained in the test enable ($\overline{TEN}$) description below.

$\overline{TEST}$ $\overline{ENABLE}$ ($\overline{TEn}$), Pin 16; 0° Eye, Pin 5; 90° Eye, Pin 4; 0° Car, Pin 7; CCor, Pin 19 — These pins allow the monitoring of ten internal points within the demodulator. A low level on $\overline{TEn}$ is normally associated with testing of the demodulator such as in a production test environment or incoming testing. Activation of $\overline{TEn}$ affects internal timing.

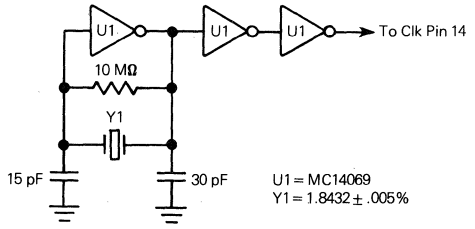
TABLE 3 — INTERNAL MONITORS

Output	$\overline{TEn}$	Function
ADS (Pin 8)	H	See Description Under ADS (Pin 8)
	L	Monitors Zero Crossings
ADC (Pin 6)	H	See Description Under ADC (Pin 6)
	L	Monitors Check Accumulator Output
0 Degree Eye (Pin 5)	H	Monitors 0 Degree Eye 2s Complement Information from 6 Tap Filter
	L	Monitors 0 Degree Eye 2s Complement Information from 12 Tap Filter
90 Degree Eye (Pin 4)	H	Monitors 90 Degree Eye 2s Complement Information from 12 Tap Filter
0°Car (Pin 7)	H	Monitors 0 Degree Carrier
	L	Monitors Check Accumulator Compare Errors
CCor (Pin 19)	H	Monitors Carrier Correction Enable
	L	Monitors Carrier Correction Direction

DIBIT CLOCK (DBC), Pin 21 — This output is a 1200 Hz clock which is derived from incoming data envelope and provides a dibit reference. This signal is representative of "data derived timing." When studying the quality of the demodulated signal, through the use of eye patterns, this output is necessary for proper synchronization of the oscilloscope.

$\overline{TEST}$ $\overline{STROBE}$ ($\overline{TStr}$), Pin 22 — This input is used to facilitate testing of the demodulator during the manufacturing process. It should be left unconnected which will result in

FIGURE 12 — OSCILLATOR CONFIGURATION



the internal pullup resistor causing the high level on this pin.

V_{SS} Pin 1 = The most negative supply, typically ground.

V_{CC} Pin 12 = The most positive supply, typically 5 volts.

DATA SCRAMBLER

The scrambling of data in the data communication environment is not done in an attempt to encrypt information in the normal sense of the word. Rather, the purpose of the scrambling of data is to guarantee that, with respect to the modem carrier, there is always random data on the line with little chance for a long string of "1s" or "0s" to exist. This is particularly important if an adaptive equalizer is being incorporated in the modem as the adaptive equalizer will require reasonably evenly distributed data to optimize its statistical response to the incoming signal. The normally used code is the CCITT 511 sequence which is EXORed with data.

The Motorola 2400 bps modulator contains a CCITT 511-bit test-pattern generator. It does not, however, incorporate the 511 data randomizer or scrambler. To scramble data using the MC6172 modulator, the circuit in Figure 10 must precede the Tx Data input of the modulator. Tx Data is added to the scrambler output pattern; then, the data is delayed by a full data bit before being transmitted by the modem. This assures a proper transmit-data/transmit-clock phase relationship. If the data scrambler is to be an optional feature, then the transmit-data multiplexer would also have to be built. This is selected by the test-pattern enable signal or any other signal that is found suitable.

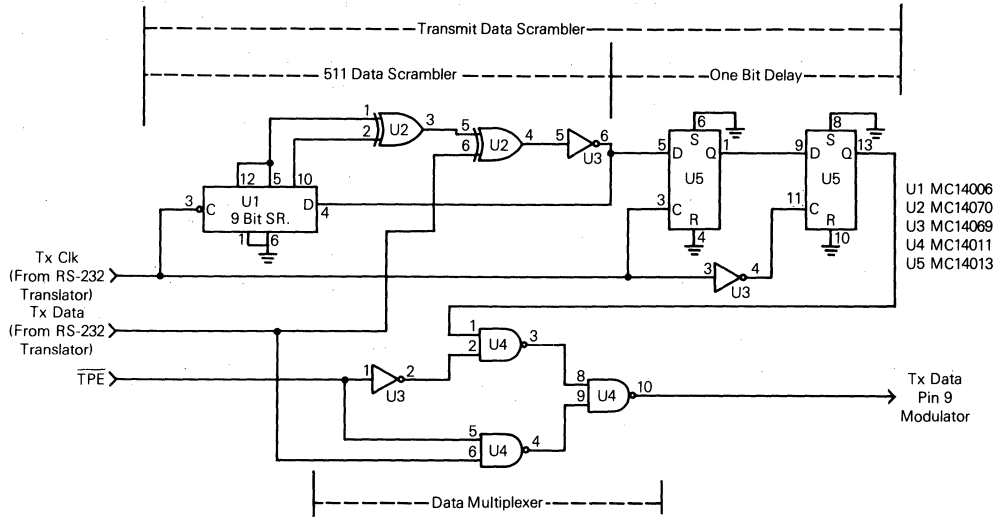
The demodulator does contain a built-in data descrambler which is enabled by the $\overline{TPE}$ input going active. The receive phasing, with respect to data, changes when $\overline{TPE}$ goes active. The exclusive NOR gating of $\overline{TPE}$ and Rx Clk, as shown in Figure 10 will maintain proper phase of Rx Clk. This circuit is required since the clocking of data on a positive edge is a data communications standard.

EYE PATTERN

When performing an evaluation of an 2400 bps modem, one common point of comparison is the quality of the eye patterns produced by the demodulator. The eye pattern may also be used as an indicator of the incoming signal with respect to level and line perturbations. Eye patterns are for test and evaluation only and are not used in the demodulation of the incoming signal.

Timing information in the Motorola 2400 bps demodulator is derived directly from the demodulated data signal. This is referred to as data derived timing. The advantage of data

FIGURE 13 — MODULATOR CCITT 511 DATA SCRAMBLER

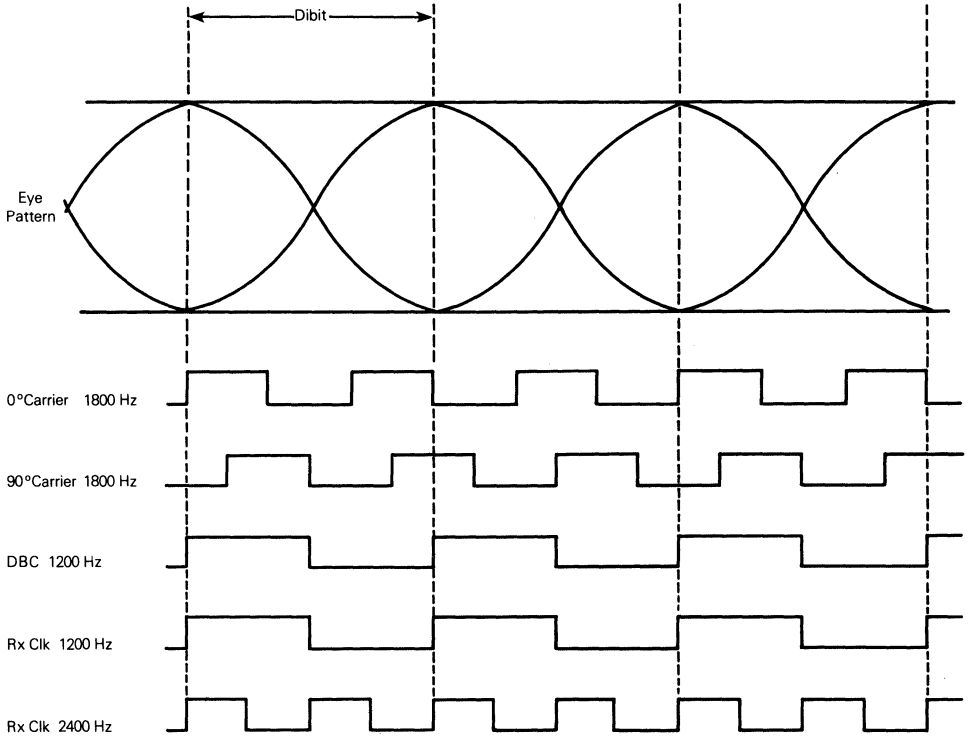


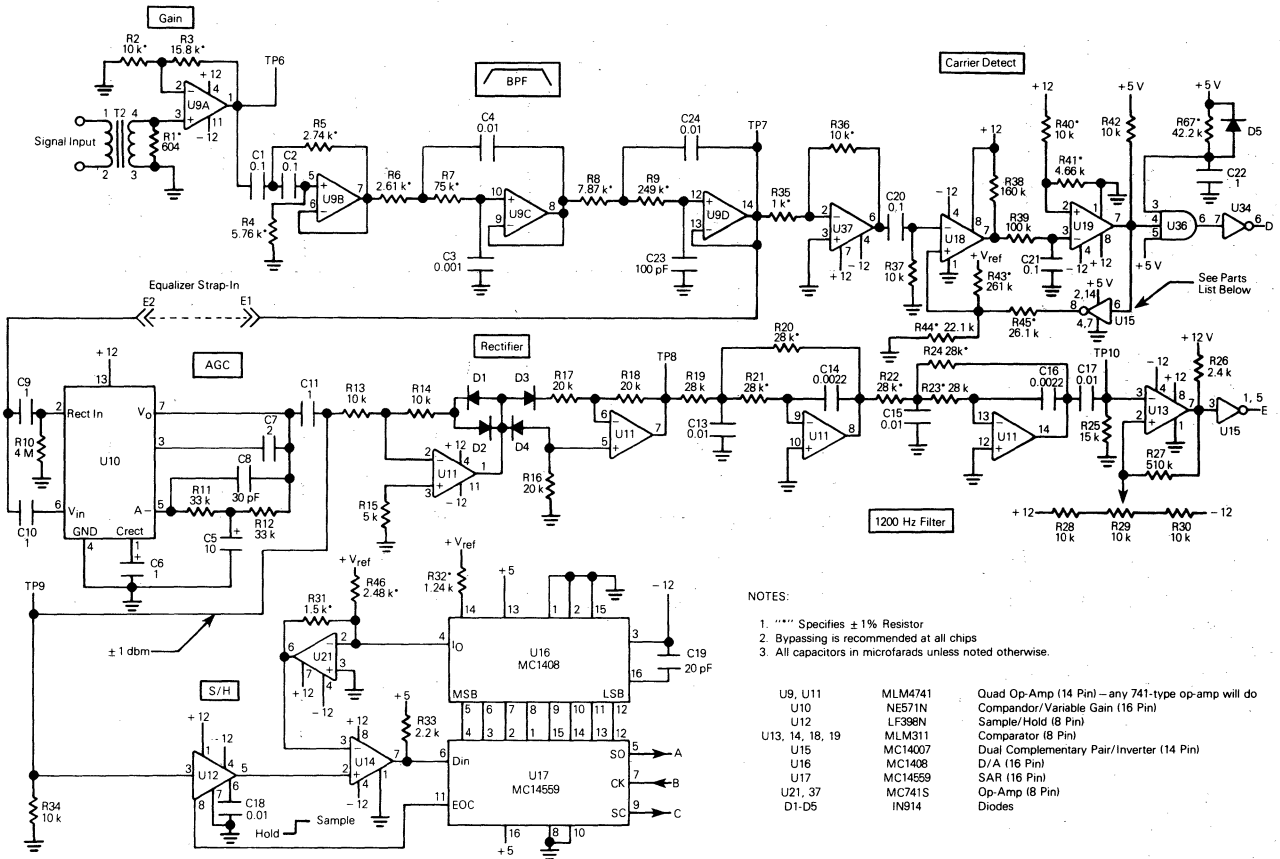
derived time is that it allows data to be sampled at optimum times. The demodulated signals, in differential phase-shift keying, take the form of "eye patterns" as shown in Figure 14. The demodulator, in optimizing its performance for minimum error rates, strobes data at the point of maximum eye opening. The demodulator constantly examines the eye opening to assure that the data sample is being taken at exactly the optimum point. As a result of constantly adjusting timing control, correct sampling is maintained. This technique provides improvements in reception that are significant, especially in a poor communications media environment.

The circuit in Figure 16 is required to observe the eye patterns. This circuit was built using Motorola CMOS devices. The 0 and 90 degree eye data is strobed from pins 4 and 5, respectively, into the shift register by the A/D clock. The A/D strobe then latches the data sample into the "D" type storage devices. The output of the storage devices taken across the scaled resistors will then represent the appropriate value of the sample taken. To properly observe the actual eye patterns, it is necessary to Sync on dibit clock while observing the 0 to 90 degree eye data. Overlaying the two patterns produces a two-level digital-eye pattern from which the quality of the incoming signal may be judged.

Figures 15 thru 17 show a typical receive/demodulator and transmit/modulator circuit, respectively. The transmit filter illustrated in Figure 17 limits the bandwidth of the signal to those frequencies allowed on a telephone line. The receive filter and equalizer in Figure 15 clean up and normalize the incoming signal for the A/D network, 1200 Hz envelope detector, and 1800 Hz carrier detector.

FIGURE 14 — EYE PATTERN





NOTES:

1. "*" Specifies ± 1% Resistor
2. Bypassing is recommended at all chips
3. All capacitors in microfarads unless noted otherwise.

U9, U11	MLM4741	Quad Op-Amp (14 Pin) – any 741-type op-amp will do
U10	NE571N	Compandor/Variable Gain (16 Pin)
U12	LF398N	Sample/Hold (8 Pin)
U13, 14, 18, 19	MLM311	Comparator (8 Pin)
U15	MC14007	Dual Complementary Pair/Inverter (14 Pin)
U16	MC1408	D/A (16 Pin)
U17	MC14559	SAR (16 Pin)
U21, 37	MC741S	Op-Amp (8 Pin)
D1-D5	IN914	Diodes

FIGURE 15 — 2400 BPS DPSK DEMODULATOR SYSTEM

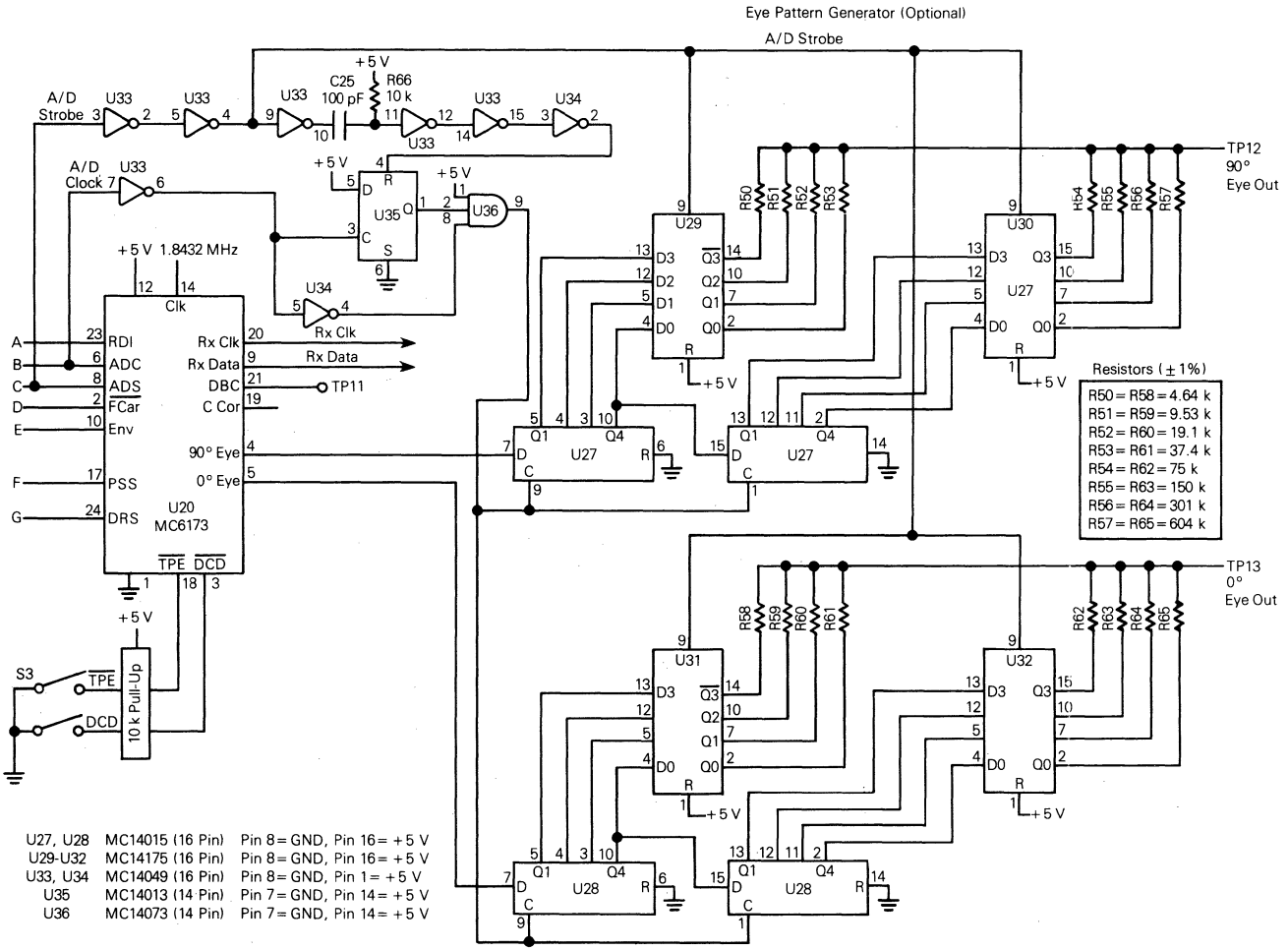
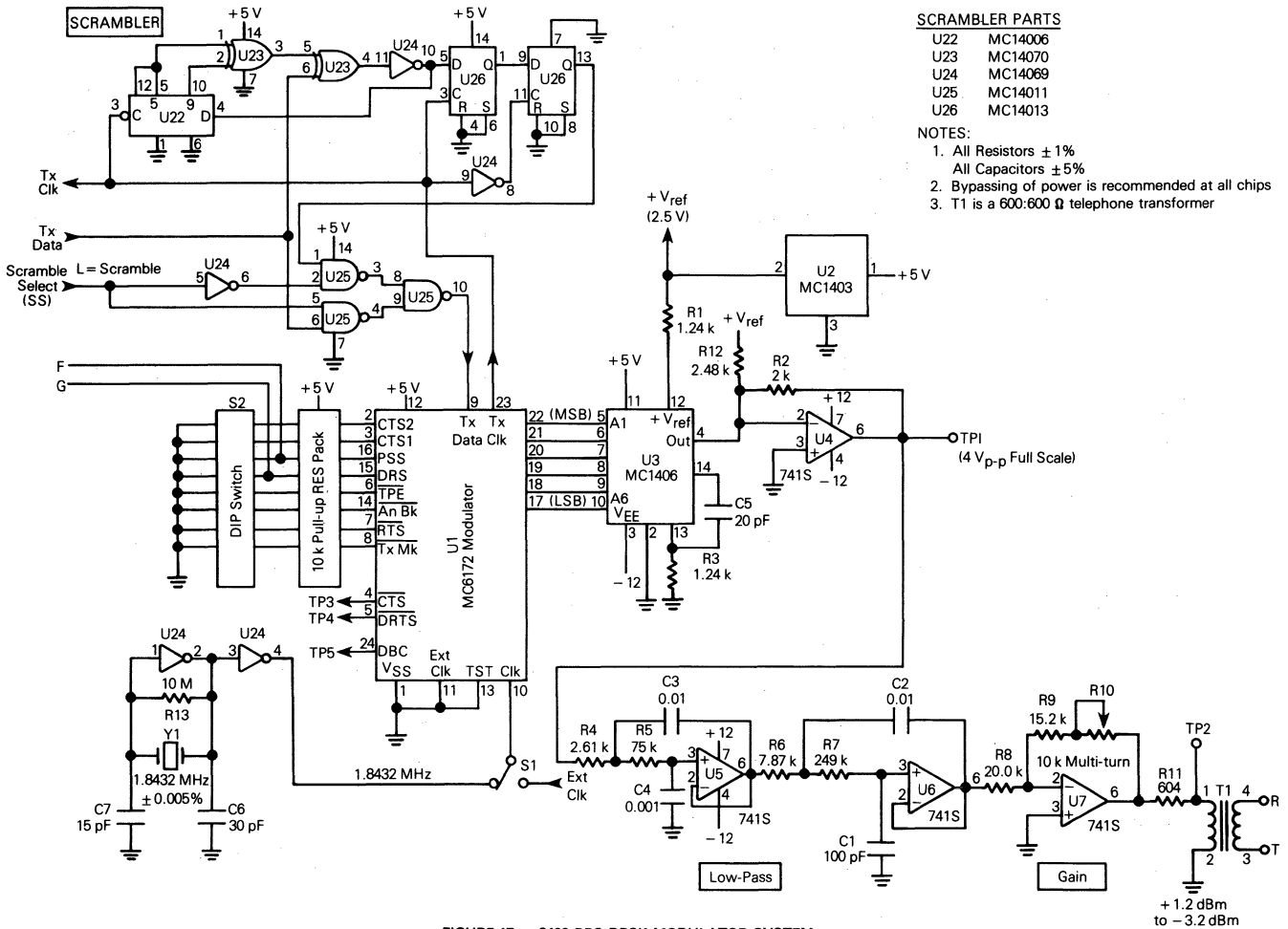


FIGURE 16 — 2400 BPS DPSK DEMODULATOR SYSTEM



SCRAMBLER PARTS

U22	MC14006
U23	MC14070
U24	MC14069
U25	MC14011
U26	MC14013

NOTES:
1. All Resistors ±1%
   All Capacitors ±5%
2. Bypassing of power is recommended at all chips
3. T1 is a 600:600 Ω telephone transformer

FIGURE 17 — 2400 BPS DPSK MODULATOR SYSTEM

MC6860

MOS

(N-CHANNEL, SILICON-GATE)

0-600 bps
DIGITAL MODEM

2

0-600 bps DIGITAL MODEM

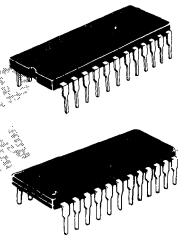
The MC6860 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) at bit rates up to 600 bps. The MC6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon-gate technology permits the MC6860 to operate using a single-voltage supply and be fully TTL compatible.

The modem is compatible with the M6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter to provide low-speed data communications capability.

- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect
- Compatible Functions for 100 Series Data Sets
- Compatible Functions for 1001A/B Data Couplers

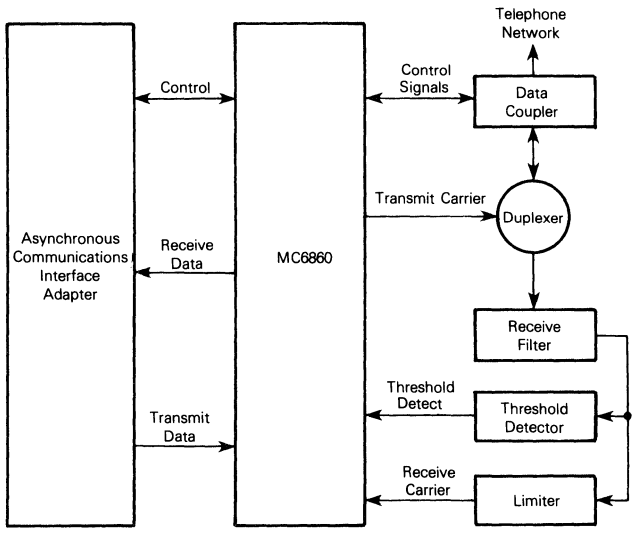


L SUFFIX
CERAMIC PACKAGE
CASE 623

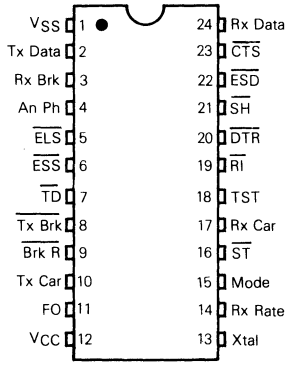
P SUFFIX
PLASTIC PACKAGE
CASE 709

NOT RECOMMENDED FOR NEW DESIGN

FIGURE 1 — TYPICAL MC6860 SYSTEM CONFIGURATION



PIN ASSIGNMENT



2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic	θ_{JA}	 65 120	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv i_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS

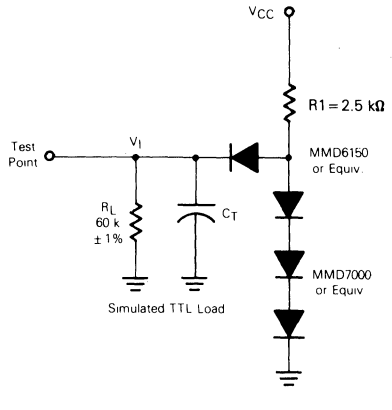
(V_{CC} = 5.0 ±5% Vdc, all voltages referenced to V_{SS} = 0, $T_A = T_L$ to T_H, all outputs loaded as shown in Figure 2 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, All Inputs Except Crystal	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, All Inputs Except Crystal	V_{IL}	V_{SS}	–	0.80	V
Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = 50 ± 5%)	V_{in}	1.5	–	2.0	V_{p-p}
Input Current ($V_{in} = V_{SS}$) All Inputs Except Rx Car, Tx Data, $\overline{TD}$, $\overline{TST}$, $\overline{RI}$, $\overline{SH}$ / $\overline{RI}$, $\overline{SH}$ Inputs	I_{in}	– –	– –	–0.2 –1.6	mA
Input Leakage Current (V_{in} = 7.0 V, $V_{CC} = V_{SS}$, T_A = 25°C)	I_{IL}	–	–	1.0	μA
Output High Voltage, All Outputs Except An Ph and Tx Car (I_{OH1} = –0.04 mA, Load A)	V_{OH1}	2.4	–	V_{CC}	V
Output Low Voltage, All Outputs Except An Ph and Tx Car (I_{OL1} = 1.6 mA, Load A)	V_{OL1}	V_{SS}	–	0.40	V
Output High Current, An Ph (V_{OH2} = 0.8 V, Load B)	I_{OH2}	0.30	–	–	mA
Output Low Voltage, An Ph (I_{OL2} = 0, Load B)	V_{OL2}	V_{SS}	–	0.30	V
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Output Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{out}	–	10	–	pF
Transmit Carrier Output Voltage (Load C)	V_{CO}	0.20	0.35	0.50	V(RMS)
Transmit Carrier Output 2nd Harmonic (Load C)	V_{2H}	–25	–32	–	dB
Input Transition Times, All Inputs Except Crystal (Operating in the Crystal Input Mode; from 10% to 90% Points)	t_r t_f	– –	– –	1.0* 1.0*	μs
Input Transition Times, Crystal Input (Operating in External Input Reference Mode)	t_r t_f	– –	– –	30 30	ns
Output Transition Times, All Outputs Except Tx Car (From 10% to 90% Points)	t_r t_f	– –	– –	5.0 5.0	μs
Internal Power Dissipation (All Inputs at V_{SS} and All Outputs Open) (Measured at $T_A = T_L$)	P_{INT}	–	–	340	mW

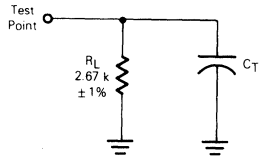
*Maximum Input Transition Times are ≤ 0.1 × Pulse Width or the specified maximum of 1.0 μs, whichever is smaller.

FIGURE 2 — OUTPUT TEST LOADS

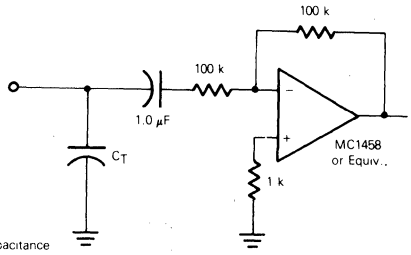
Load A — TTL Output Load for Receive Break, Digital Carrier, Mode, Clear-to-Send, and Receive Data Outputs



Load B — Answer Phone Load



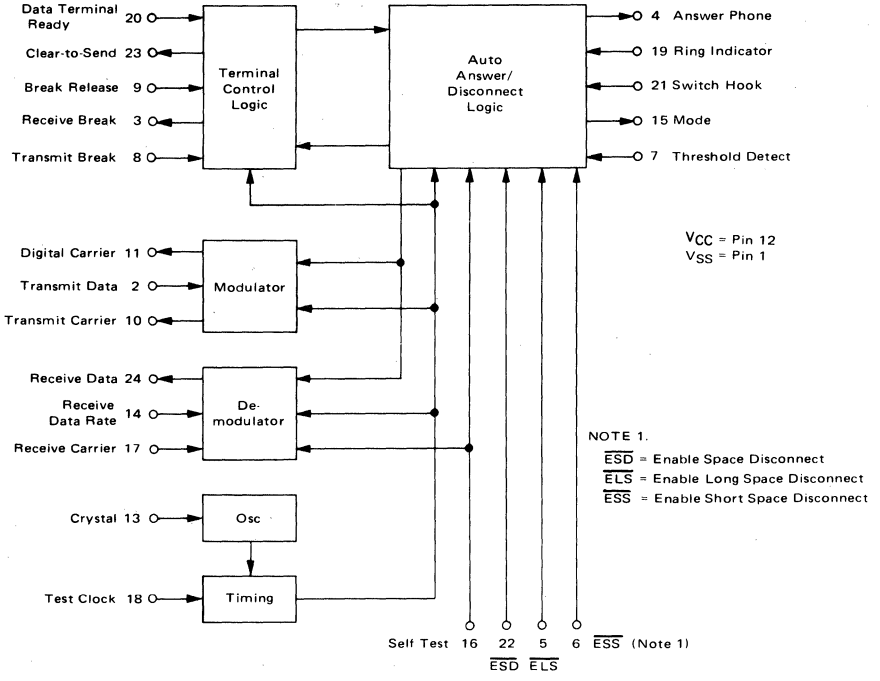
Load C — Transmit Carrier Load



CT = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitance

2

FIGURE 3 — BLOCK DIAGRAM



DEVICE OPERATION*

GENERAL

Figure 1 shows the modem and its interconnections. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission on the telephone line (refer to Figure 3). The modulator output is buffered before driving the line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

The Supervisory Control provides the necessary commands and responses for handshaking with the remote modem, along with the interface signals to the data coupler and communication terminal. If the modem is a built-in unit, all input-output (I/O) logic need not be RS-232 compatible. The use of MC1488 and MC1489A line drivers and receivers will provide a RS-232 interface conforming to the EIA specification.

ANSWER MODE

Automatic answering is first initiated by a receipt of a Ring Indicator ($\overline{RI}$) signal. This can be either a low level for at least 51 ms as would come from a CBS data coupler, or at least 20 cycles of a 20-47 Hz ringing singal (low level ≥ 50% of the duty cycle) as would come from a CBT data coupler. The presence of the Ring Indicator signal places the modem in the Answer Mode; if the Data Terminal Ready line is low, indicating the communication terminal is ready to send or receive data, the Answer Phone output goes high. This output is designed to drive a transistor switch which will activate

*See Tables 1 and 2 for delay time tolerances.

the Off Hook (OH) and Data Transmission (DA) relays in the data coupler. Upon answering the phone the 2225-Hz Transmit Carrier is turned on.

The originate modem at the other end detects this 2225-Hz signal and after a 450 ms delay (used to disable any echo suppressors in the telephone network) transmits a 1270-Hz signal which the local answering modem detects, provided the amplitude and frequency requirements are met. The amplitude threshold is set external to the modem chip. If the signal level is sufficient the $\overline{TD}$ input should be low for 20 μs at least once every 32 ms. The absence of a threshold indication for a period greater than 51 ms denotes the loss of Receive Carrier and the modem begins hang-up procedures. Hang-up will occur 17 s after $\overline{RI}$ has been released provided the handshaking routine is not re-established. The frequeny tolerance during handshaking is $\pm$ 100 Hz from the Mark frequency.

After the 1270-Hz signal has been received for 150 ms, the Receive Data is unclamped from a Mark condition and data can be received. The Clear-to-Send output goes low 450 ms after the receipt of carrier and data presented to the answer modem is transmitted. Refer to Figure 4.

AUTOMATIC DISCONNECT

Upon receipt of a space of 150 ms or greater duration, the modem clamps the Receive Break high. This condition exists until a Break Release command is issued at the receiving station. Upon receipt of a 0.3 s space, with Enable Short Space Disconnect at the most negative voltage (low), the modem automatically hangs up. If Enable Long Space Disconnect is low, the modem requires 1.5 s of continuous space to hang up. Refer to Figure 5.

ORIGINATE MODE

Upon receipt of a Switch Hook ($\overline{SH}$) command the modem function is placed in the Originate Mode. If the Data Terminal Ready input is enabled (low) the modem will provide a logic high output at Answer Phone. The modem is now ready to receive the 2225-Hz signal from the remote answering modem. It will continue to look for this signal until 17 s after $\overline{SH}$ has been released. Disconnect occurs if the handshaking routine is not established.

Upon receiving 2225 $\pm$ 100 Hz for 150 ms at an acceptable amplitude, the receive Data output is unclamped from a Mark condition and data reception can be accomplished. 450 ms after receiving a 2225-Hz signal, a 1270-Hz signal is transmitted to the remote modem. 750 ms after receiving the 2225-Hz signal, the Clear-to-Send output is taken low and data can now be transmitted as well as received. Refer to Figure 6.

INITIATE DISCONNECT

In order to command the remote modem to automatically hang up, a disconnect signal is sent by the local modem. This is accomplished by pulsing the normally low Data Terminal Ready into a high state for greater than 34 ms. The local modem then sends a 3 s continuous space and hangs up provided the Enable Space Disconnect is low. If the remote modem hangs up before 3 s, loss of Threshold Detect will cause loss of Clear-to-Send, which marks the line in Answer Mode and turns the carrier off in the Originate Mode.

If $\overline{ESD}$ is high the modem will transmit data until hang-up occurs 3 s later. Receive Break is clamped 150 ms following the Data Terminal Ready interrupt. Refer to Figure 7.

INPUT/OUTPUT FUNCTIONS

Figure 8 shows the I/O interface for the low speed modem. The following is a description of each individual signal:

Receiver Carrier (Rx Car)

The Receive Carrier is the FSK input to the demodulator. The local Transmit Carrier must be balanced or filtered out and the remaining signal hard limited. The conditioned receive carrier is measured by the MC6860. Any half-cycle period greater than or equal to 429 $\pm$ 1.0 μs for the low band or 235 $\pm$ 1.0 μs for the high band is detected as a space. Resultant peak phase jitter is as follows:

Data Rate Bits per Second	Answer Mode ϕ_J (Peak %)	Originate Mode ϕ_J (Peak %)
300	7.0	3.7
200	4.7	2.5
150	3.5	1.8
110	2.6	1.4

Ring Indicator ($\overline{RI}$)

The modem function will recognize the receipt of a call from the CBT data coupler if at least 20 cycles of the 20-47 Hz ringing singal (low level $\geq$50% of the duty cycle) are present. The CBS data coupler $\overline{RI}$ signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS data coupler is recognized if the $\overline{RI}$ signal is present for at least 51 ms. This input is held high except during ringing. An $\overline{RI}$ signal automatically places the modem function in the Answer Mode.

Switch Hook ($\overline{SH}$)

$\overline{SH}$ interfaces directly with the CBT data coupler and via the EIA RS-232 level conversion for the CBS data coupler. An $\overline{SH}$ signal automatically places the modem function in the Originate Mode.

$\overline{SH}$ is low during origination of a call. The modem will automatically hang up 17 s after releasing $\overline{SH}$ if the handshaking routine has not been accomplished.

Threshold Detect ($\overline{TD}$)

This input is derived from an external threshold detector. If the signal level is sufficient, the $\overline{TD}$ input must be low for 20 μs at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid.

If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently.

Loss of threshold for 51 ms or longer results in a loss of Clear-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.

2

TIMING DIAGRAMS

FIGURE 4 — ANSWER MODE

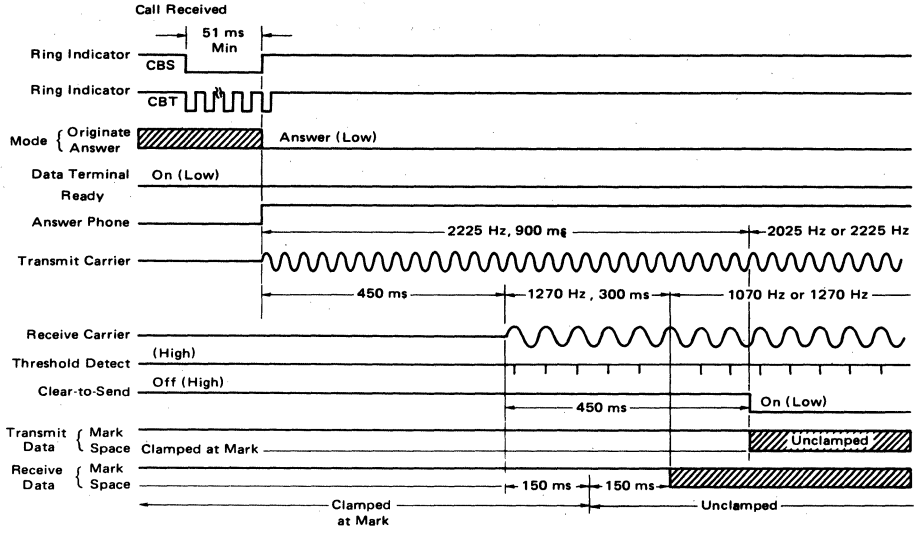


FIGURE 5 — AUTOMATIC DISCONNECT — LONG OR SHORT SPACE

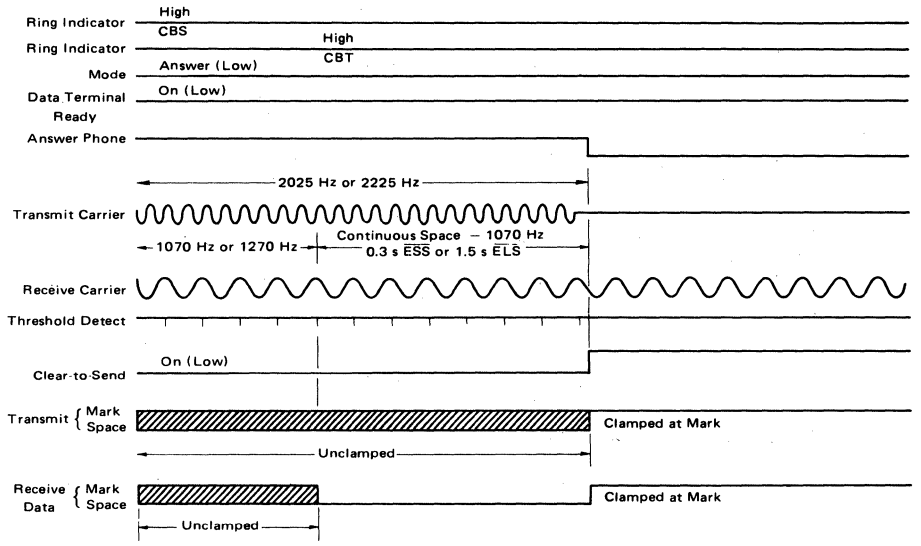


FIGURE 6 — ORIGINATE MODE

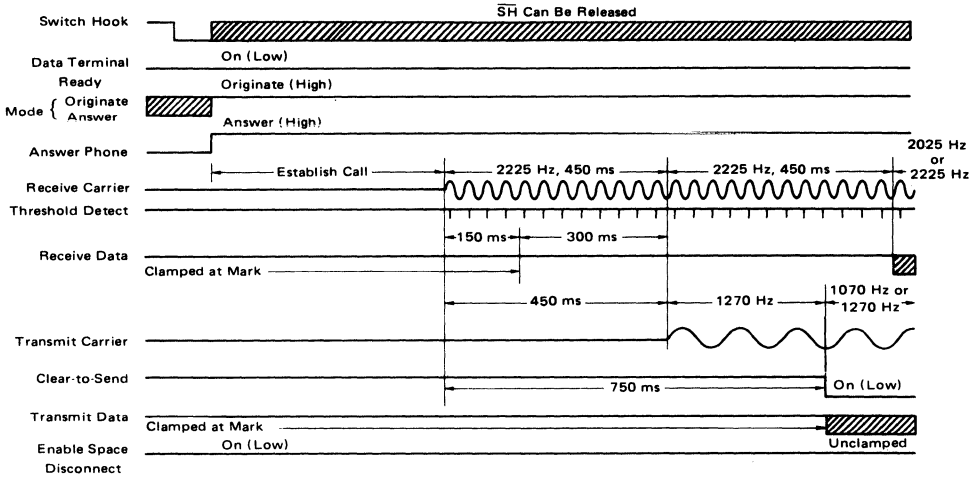
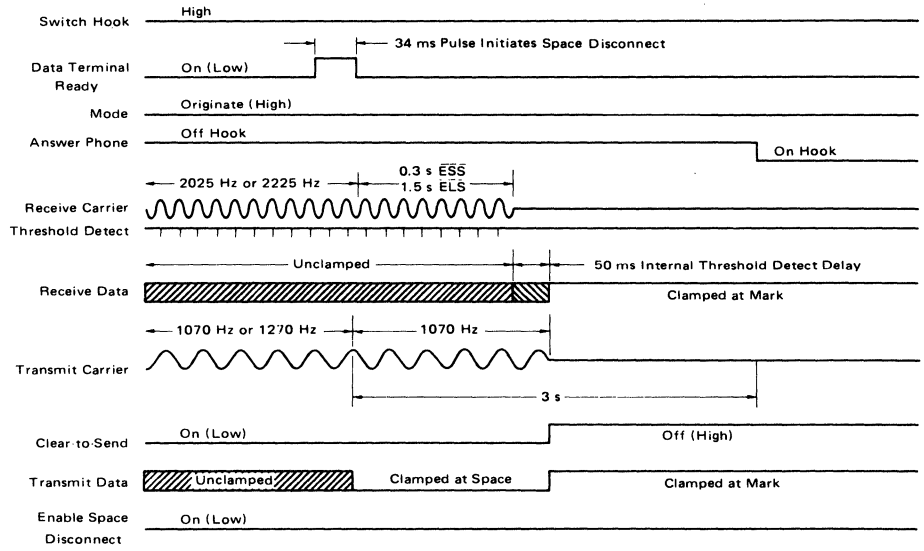


FIGURE 7 — INITIATE DISCONNECT



2

Receive Data Rate (Rx Rate)

The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.

Transmit Data (Tx Data)

Transmit Data is the binary information presented to the modem function for modulation with FSK techniques. A high level represents a Mark.

Data Terminal Ready ($\overline{DTR}$)

The Data Terminal Ready signal must be low before the modem function will be enabled. To initiate a disconnect, $\overline{DTR}$ is held high for 34 ms minimum. A disconnect will occur 3 s later.

Break Release ($\overline{Brk\ R}$)

After receiving a 150 ms space signal, the clamped high condition of the Receive Break output can be removed by holding Break Release low for at least 20 μs.

Transmit Break ($\overline{Tx\ Brk}$)

The Break command is used to signal the remote modem to stop sending data.

A Transmit Break (low) greater than 34 ms forces the modem to send a continuous space signal for 233 ms. Transmit Break must be initiated only after $\overline{CTS}$ has been established. This is a negative edge sense input. Prior to initiating $\overline{Tx\ Brk}$, this input must be held high for a minimum of 34 ms.

Enabled Space Disconnect ($\overline{ESD}$)

When $\overline{ESD}$ is strapped low and $\overline{DTR}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If $\overline{ESD}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.

Enable Short Space Disconnect ($\overline{ESS}$)

$\overline{ESS}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. *$\overline{ESS}$ and $\overline{ELS}$ must not be simultaneously strapped low.*

Enable Long Space Disconnect ($\overline{ELS}$)

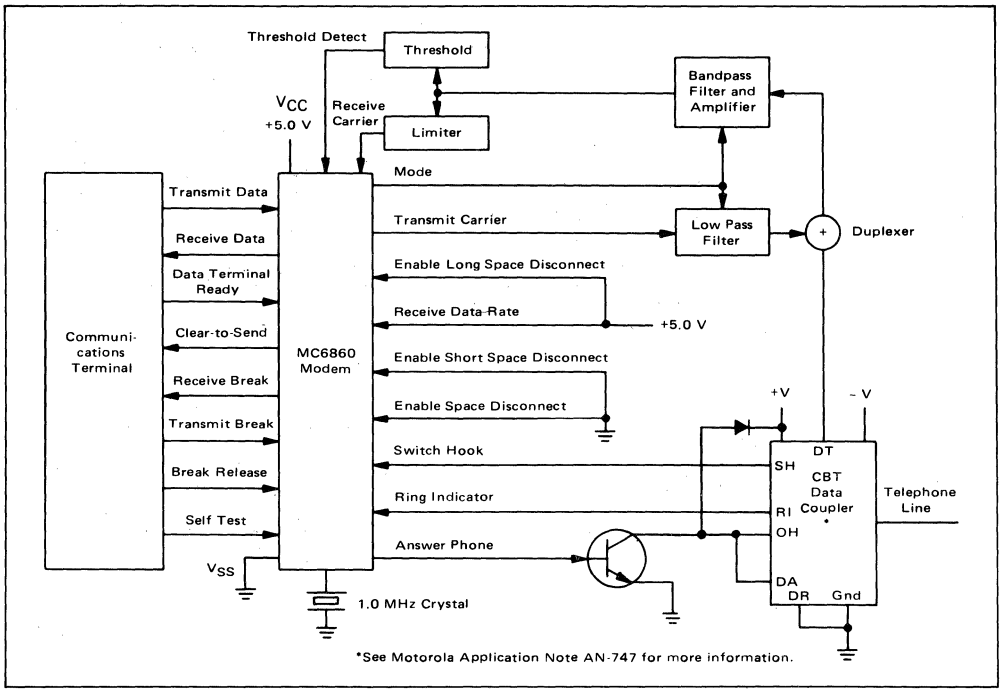
$\overline{ELS}$ is a strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.

Crystal (Xtal)

A 1.0 MHz crystal with the following parameters is required to utilize the on-chip oscillator. A 1.0-MHz square wave can also be fed into this input to satisfy the clock requirement.

Mode:	Parallel
Frequency:	1.0 MHz ±0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0-70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

FIGURE 8 — I/O INTERFACE CONNECTIONS FOR MC6860 (ORIGINATE/ANSWER MODEM)



When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be ≤9 pF at the crystal input. Reliable crystal oscillator start-up requires that the V_{CC} power-on transition time be >15 milliseconds.

Test Clock (TST)

A test signal input is provided to decrease the test time of the chip. In normal operation this input *must be strapped low.*

Self Test ($\overline{ST}$)

When a low voltage level is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishement, which occurred during the initial handshake, is not lost during self test. The Mode Control ouput changes state during Self Test, permitting the receive filters to pass the local Transmit Carrier.

$\overline{ST}$	$\overline{SH}$	$\overline{RI}$	Mode
H	⊓⊔*	H	H
H	H	L	L
L	⊓⊔*	H	L
L	H	L	H

*Note maximum $\overline{SH}$ low time in Table 1.

Answer Phone (An Ph)

Upon receipt of Ring Indicator or Switch Hook signal and Data Terminal Ready, the Answer Phone output goes high [$(\overline{SH}+\overline{RI})\cdot\overline{DTR}$]. This signal drives the base of a transistor which activates the Off Hook, and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.

Mode

The Mode output indicates the Answer (low) or Originate (high) status of the modem. This output changes state when a Self Test command is applied.

Clear-To-Send ($\overline{CTS}$)

A low on the $\overline{CTS}$ output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.

Receive Data (Rx Data)

The Receive Data output is the data resulting from demodulating the Receive Carrier. A Mark is a high level.

Receive Break (Rx Brk)

Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-to-Send is established.

Digital Carrier (FO)

A test signal output is provided to decrease the chip test time. The signal is a square wave at the transmit frequency.

Transmit Carrier (Tx Car)

The Transmit Carrier is a digitally-synthesized sine wave (Figure 9) derived from the 1.0 MHz crystal reference. The frequency characteristics are as follows:

Mode	Data	Transmit Frequency	Tolerance*
Originate	Mark	1270 Hz	−0.15 Hz
Originate	Space	1070 Hz	0.90 Hz
Answer	Mark	2225 Hz	−0.31 Hz
Answer	Space	2025 Hz	−0.71 Hz

*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0 μs following a data bit change with no more than 2.0 μs phase discontinuity. The typical output level is 0.35 V (RMS) into 100 k ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (see Figure 10).

POWER-ON RESET

Power-on reset is provided on-chip to insure that when power is first applied the Answer Phone output is in the low (inactive) state. This holds the modem in the inactive or idle mode until a $\overline{SH}$ or $\overline{RI}$ signal has been applied. Once power has been applied, a momentary loss of power at a later time may not be of sufficient time to guarantee a chip reset through the power-on reset circuit.

To insure initial power-on reset action, the external parasitic capacitance on $\overline{RI}$ and $\overline{SH}$ should be <30 pF. Capacitance values >30 pF may require the use of an external pullup resistor to V_{CC} on these inputs in addition to the pullup devices already provided on chip.

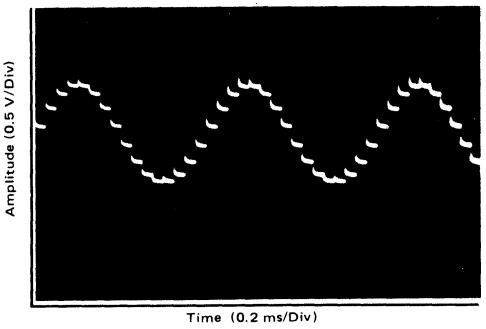


FIGURE 9 — TRANSMIT CARRIER SINE WAVE

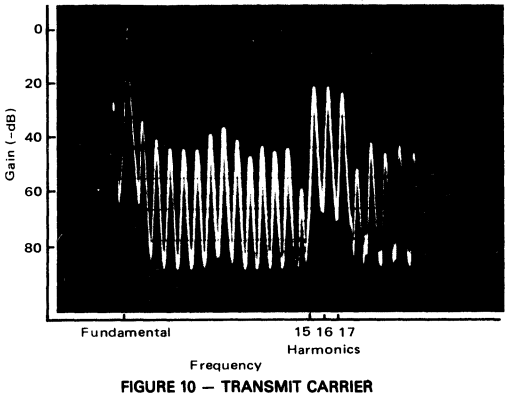


FIGURE 10 — TRANSMIT CARRIER FREQUENCY SPECTRUM

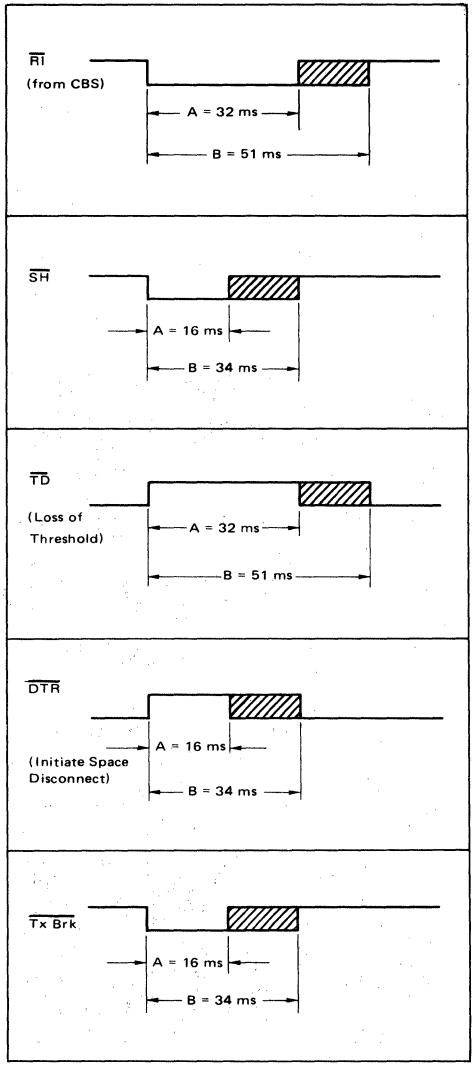
2

TABLE 1 – ASYNCHRONOUS INPUT PULSE WIDTH AND OUTPUT DELAY VARIATIONS
(Time delays specified do not include the 1-MHz reference tolerance.)

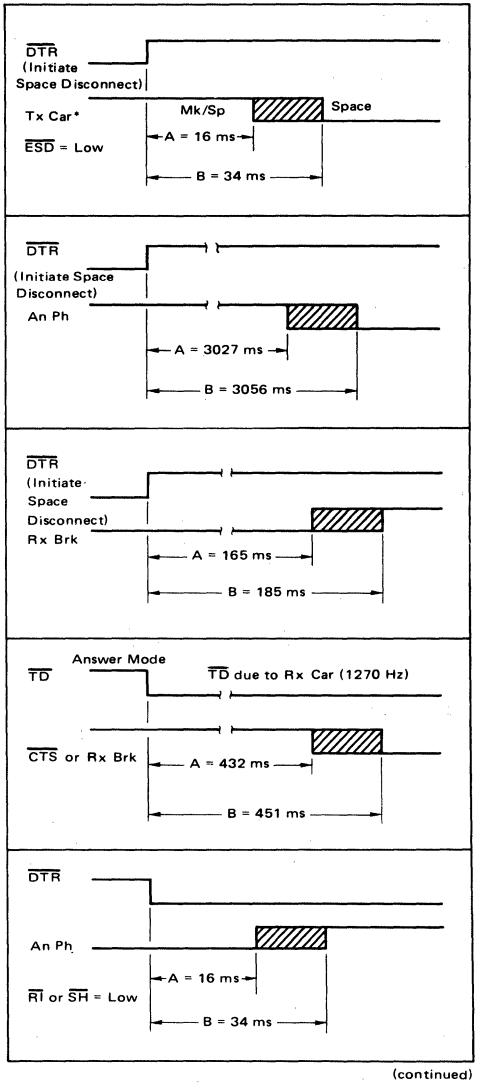
Due to the asynchronous nature of the input signals with respect to the circuit internal clock, a delay variation or input pulse width requirement will exist. Time delay A is the maximum time for which no response will occur. Time delay B is the minimum time required to guarantee an input response. Input signal widths in the cross-hatched region (i.e., greater than A but less than B) may or may not be recognized as valid.

For output delays, time A is the minimum delay before an output will respond. Time B is the maximum delay for an output to respond. Output signal response may or may not occur in the cross-hatched region (i.e., greater than A but less than B).

INPUT PULSES



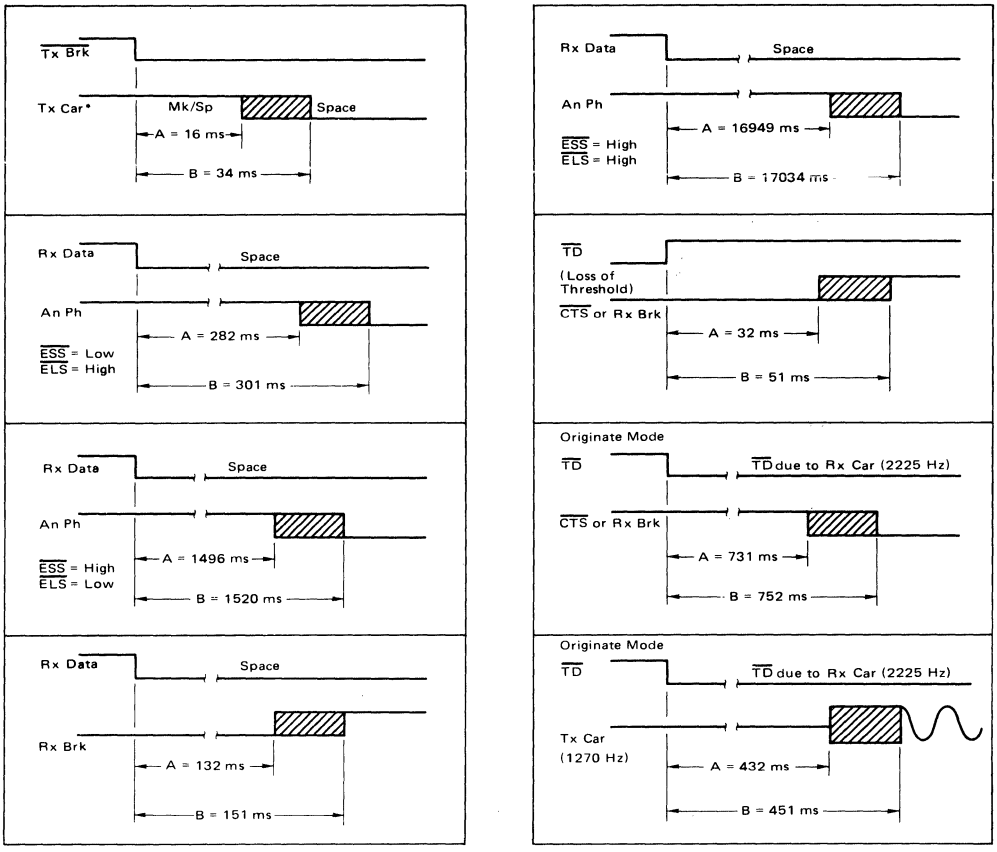
OUTPUT DELAYS



*Digital Representation.

(continued)

TABLE 1 – OUTPUT DELAY VARIATIONS (continued)



*Digital Representation

TABLE 2 – TRANSMIT BREAK AND DISCONNECT DELAYS

Function Description	Min	Max	Unit
Tx Brk (Space Duration)	232	235	ms
Space Disconnect (Space Duration) (DTR = High, ESD and TD = Low)	3010	3023	ms
Loss of Carrier Disconnect (Measured from positive edge of CTS to negative edge of An Ph, with RI, SH, and TD = High)	16965	17034	ms
Override Disconnect (Measured from positive edge of RI or SH to negative edge of An Ph, with TD = High)	16916	17101	ms

FIGURE 11 — FLOW DIAGRAM

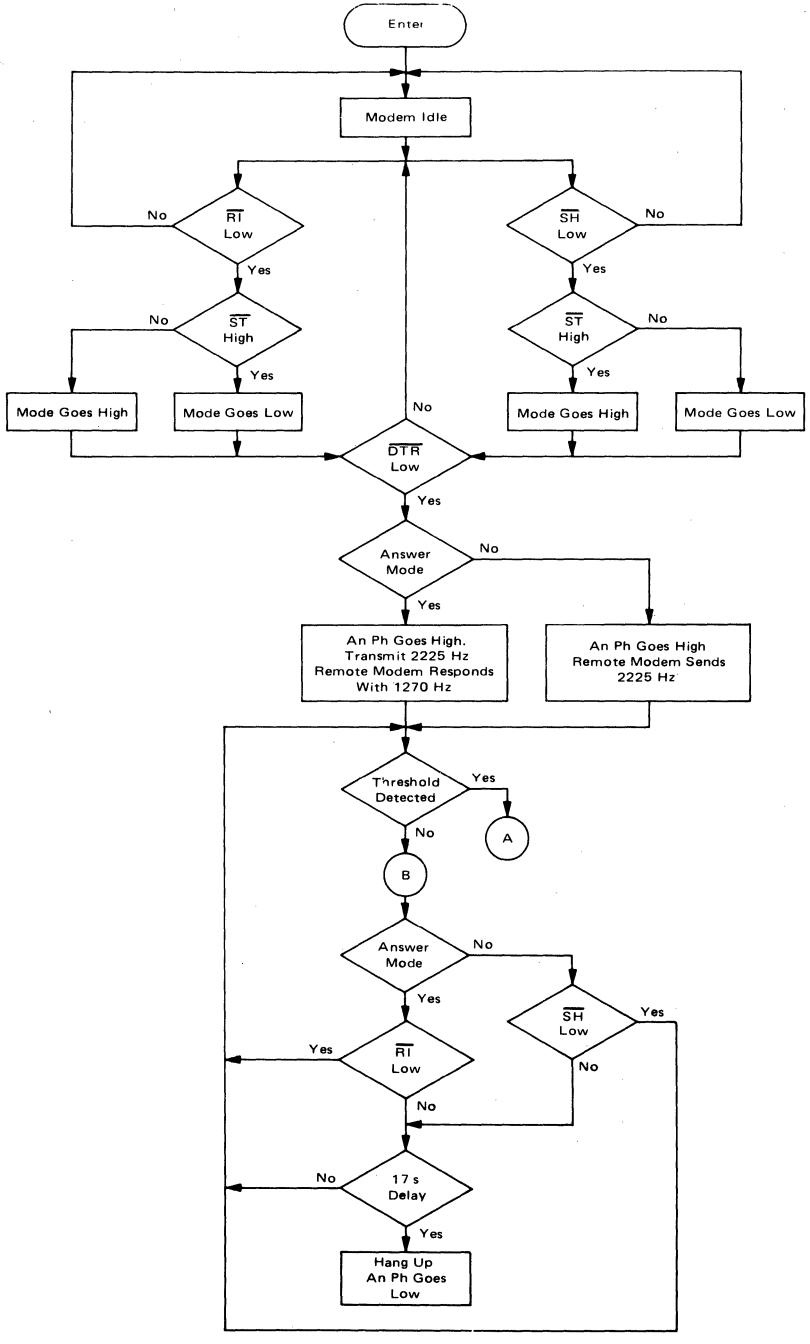
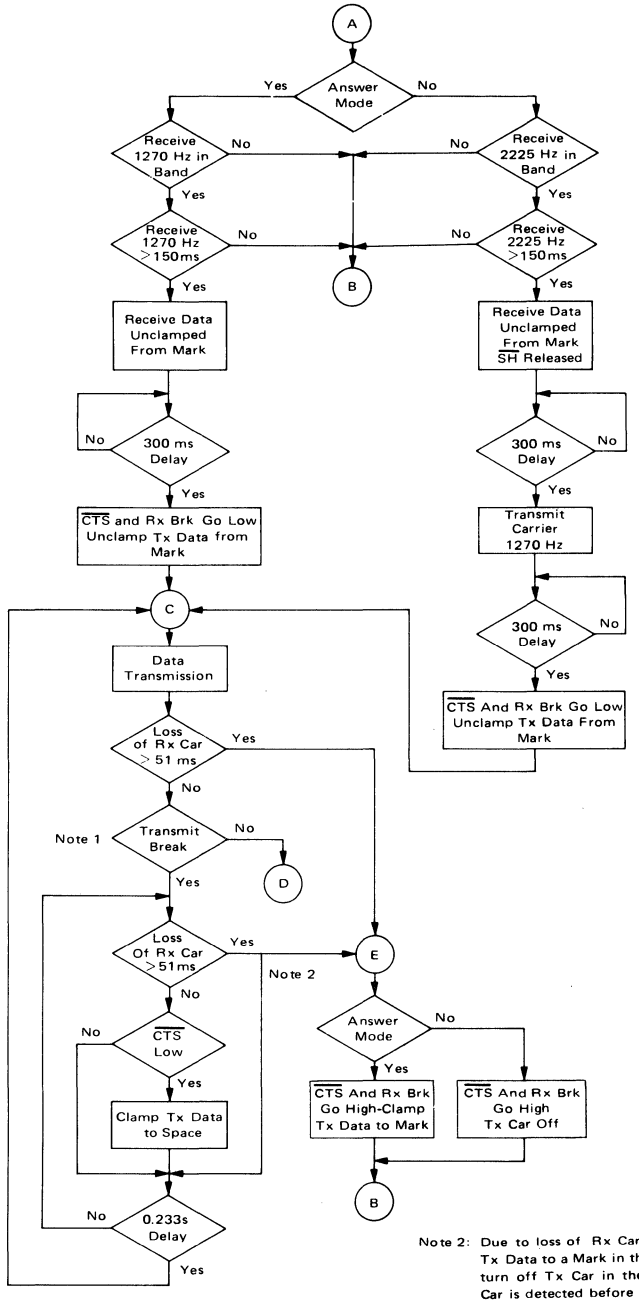


FIGURE 11 — FLOW DIAGRAM (CONTINUED)

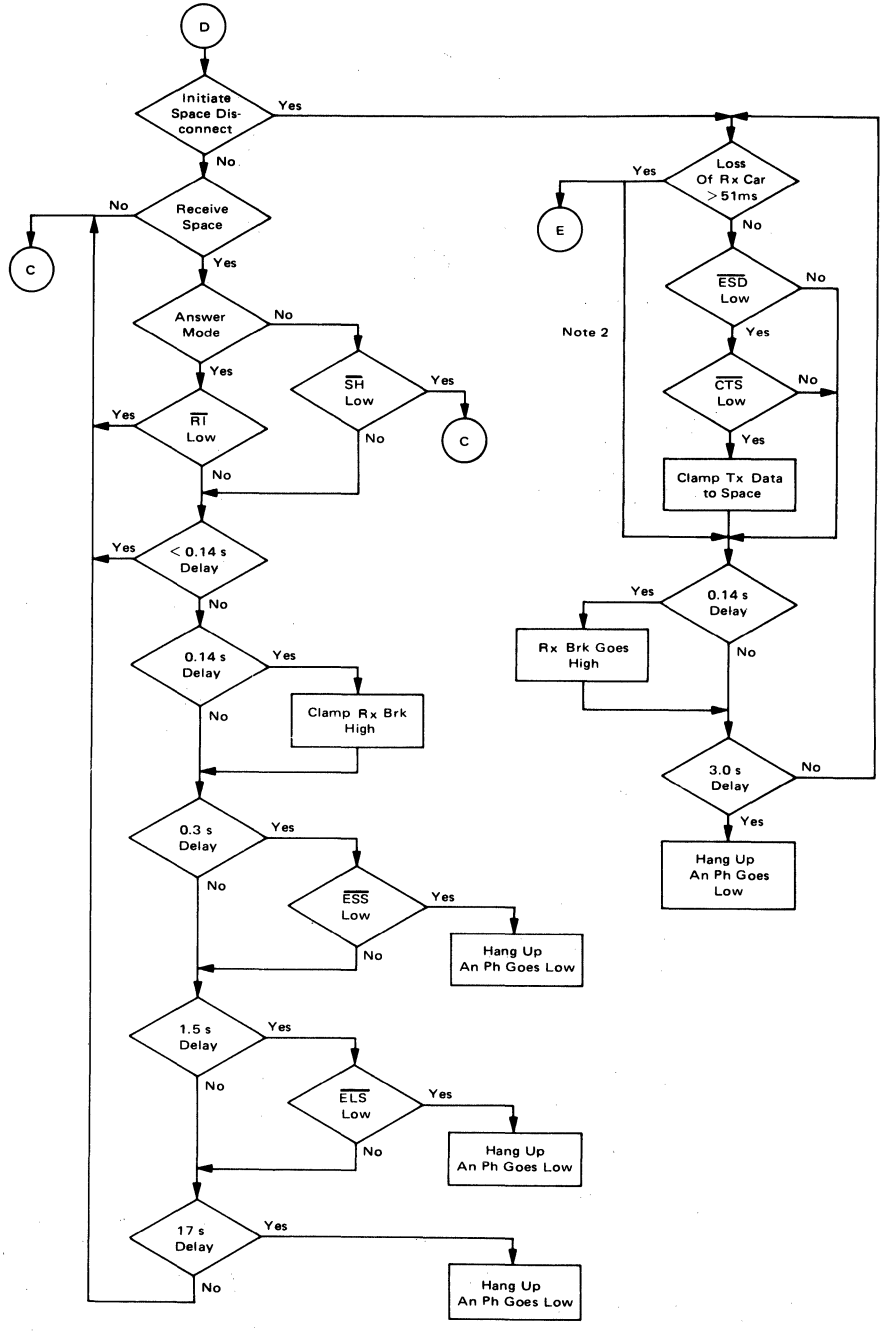


Note 1: Transmit Break, Initiate Space Disconnect, and Receive Space are mutually exclusive events.

Note 2: Due to loss of Rx Car, the modem will clamp Tx Data to a Mark in the Answer Mode and will turn off Tx Car in the Originate Mode. If Rx Car is detected before completion of Tx Brk or Initiate Space Disconnect, normal operation of Tx Brk or Initiate Space Disconnect will continue until completion of their respective time delays.

2

FIGURE 11 — FLOW DIAGRAM (CONCLUDED)



MC13055

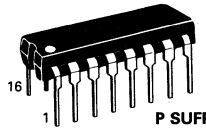
WIDEBAND FSK RECEIVER

The MC13055 is intended for RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The excellent signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

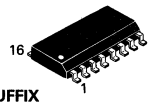
- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

WIDEBAND FSK RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

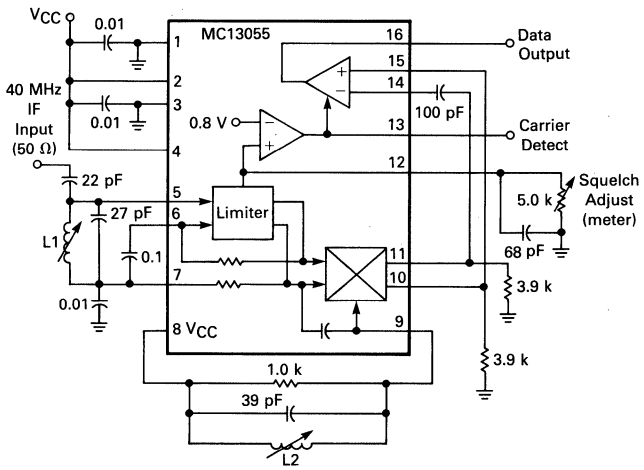


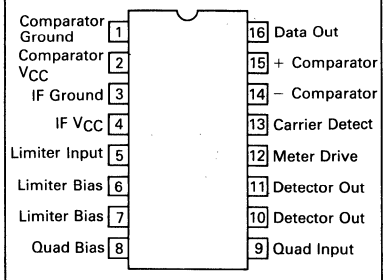
P SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
PLASTIC PACKAGE
CASE 751B-03
(SO-16)

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM





2

MAXIMUM RATINGS

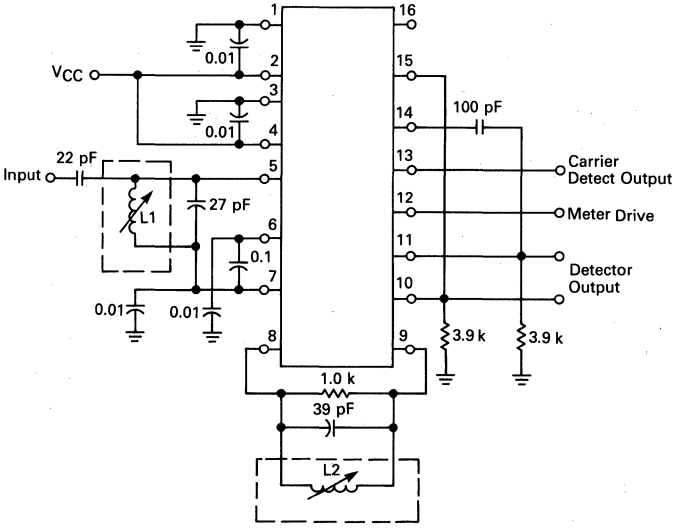
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, Test circuit of Figure 2)

Characteristics		Measure	Min	Typ	Max	Unit
Total Drain Current		I2 + I4	—	20	25	mA
Data Comparator Pull-Down Current		I16	—	10	—	mA
Meter Drive Slope versus Input		I12	—	7.5	—	μA/dB
Carrier Detect Pull-Down Current		I13	—	1.3	—	mA
Carrier Detect Pull-Up Current		I13	—	500	—	μA
Carrier Detect Threshold Voltage		V12	700	800	900	mV
DC Output Current		I10, I11	—	430	—	μA
Recovered Signal		V10 − V11	—	350	—	mVrms
Sensitivity for 20 dB S+N/N, BW = 5.0 MHz		VIN	—	20	—	μVrms
S+N/N at V_{in} = 50 μV		V10 − V11	—	30	—	dB
Input Impedance @ 40 MHz	R_{in} C_{in}	Pin 5, Ground	— —	4.2 4.5	— —	kΩ pF
Quadrature Coil Loading	R_{in} C_{in}	Pin 9 to 8	— —	7.6 5.2	— —	kΩ pF

FIGURE 2 — TEST CIRCUIT



Coils — Shielded
Coilcraft UNI-10/142
L1 Gray 8-1/2 Turns, nominal 300 μH
L2 Black 10-1/2 Turns, nominal 380 μH

or
TOKO Series E526HNA
L1 Part No. 100301
L2 Part No. 100079

All curves taken with test conditions of ELECTRICAL CHARACTERISTICS, unless otherwise noted

FIGURE 3 — OVERALL GAIN, NOISE, AM REJECTION

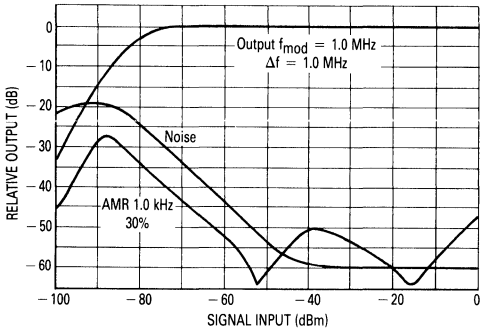


FIGURE 4 — METER CURRENT versus SIGNAL

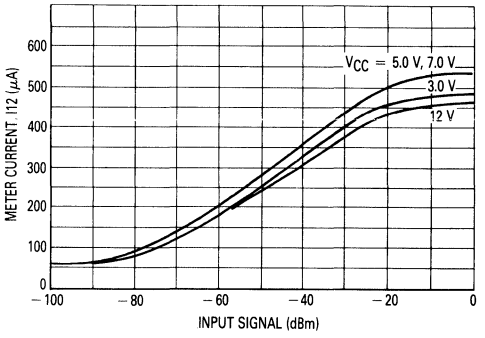


FIGURE 5 — UNTUNED INPUT: LIMITING SENSITIVITY versus FREQUENCY

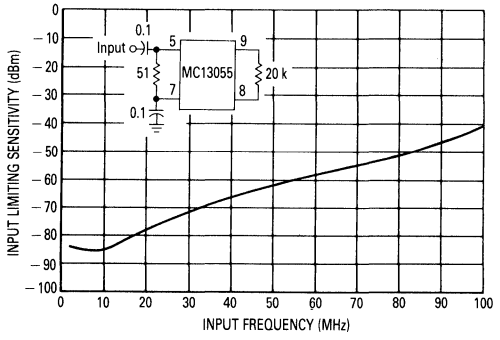


FIGURE 6 — UNTUNED INPUT: METER CURRENT versus FREQUENCY

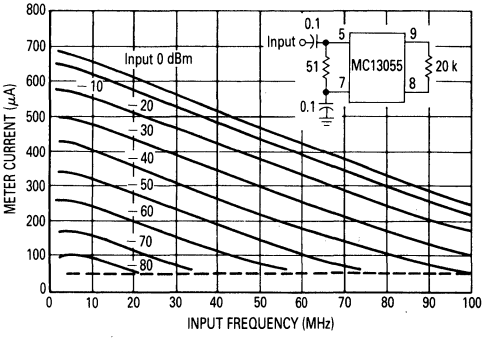


FIGURE 7 — LIMITING SENSITIVITY AND DETUNING versus SUPPLY

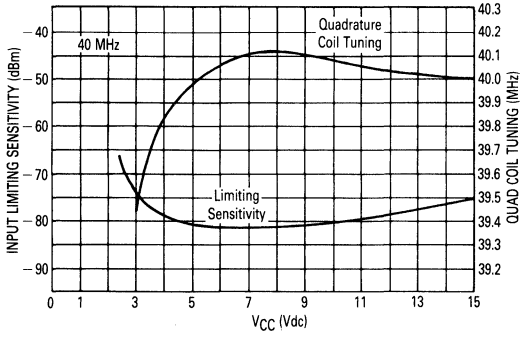
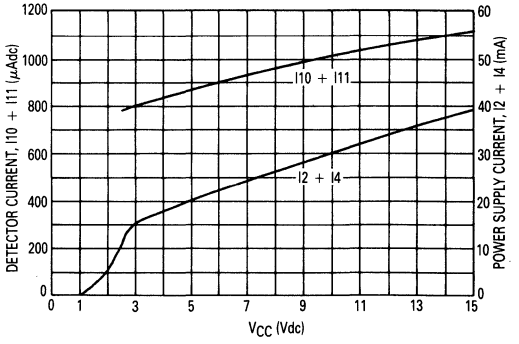


FIGURE 8 — DETECTOR CURRENT AND POWER SUPPLY CURRENT versus SUPPLY VOLTAGE



2

FIGURE 9 — RECOVERED AUDIO versus TEMPERATURE

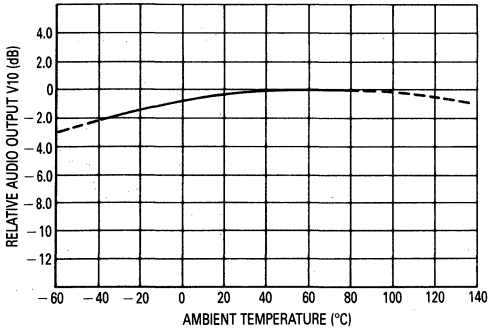


FIGURE 10 — CARRIER DETECT THRESHOLD versus TEMPERATURE

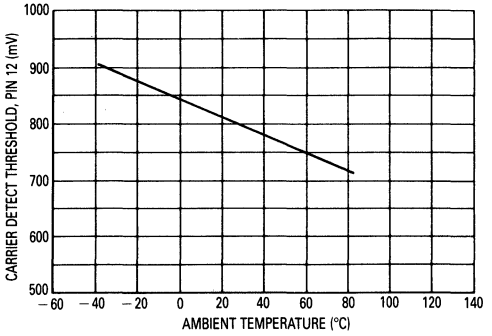


FIGURE 11 — METER CURRENT versus TEMPERATURE

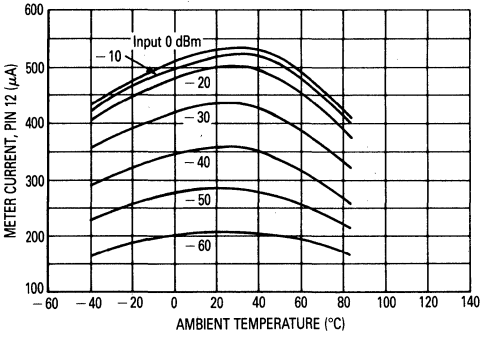
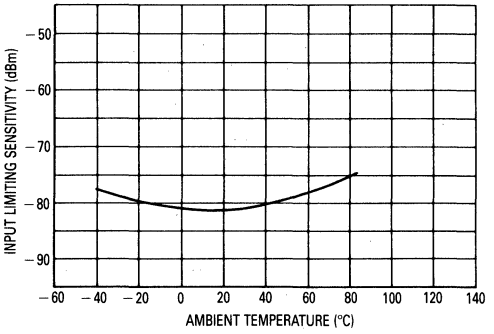


FIGURE 12 — INPUT LIMITING versus TEMPERATURE



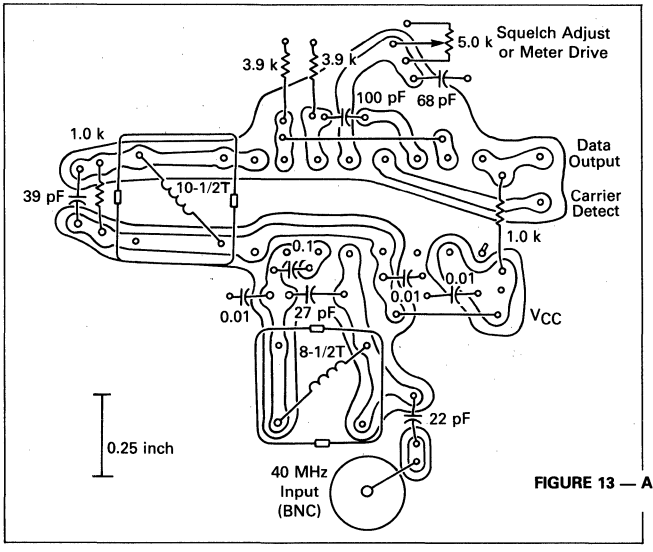


FIGURE 13 — APPLICATION PRINTED CIRCUIT BOARD (Bottom View)

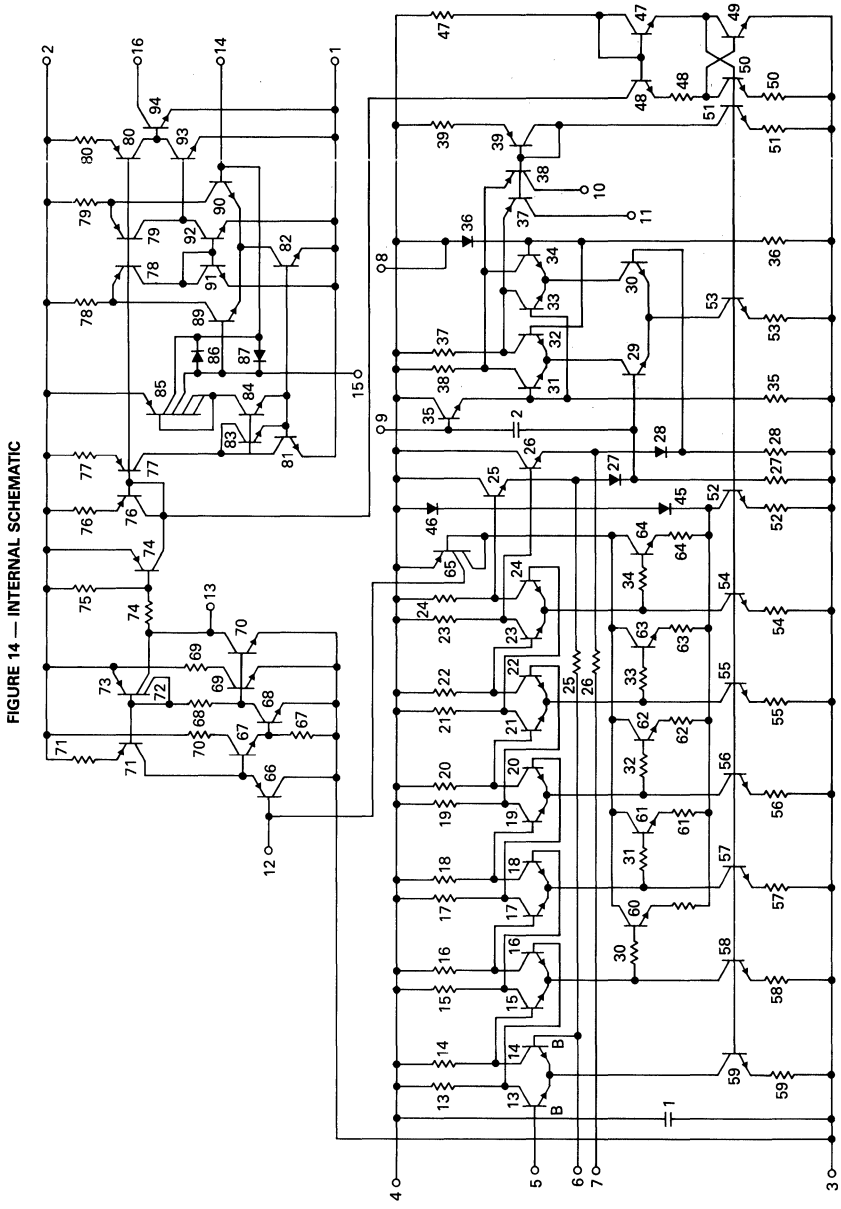


FIGURE 14 — INTERNAL SCHEMATIC

2

GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open-collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms. (See Figure 4.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor R from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be translated into an equal amount of hysteresis by Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or non-inverted form.

MC14400
MC14401
MC14402
MC14403
MC14405

2

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

CODEC-FILTER
PCM MONO-CIRCUIT

CODEC-FILTER PCM-MONO-CIRCUIT

The MC14400, MC14401, MC14402, MC14403, and MC14405 are all per channel codec-filter PCM mono-circuits. These devices perform the voice digitizing and recovery, as well as the band limiting and signal restoration necessary in PCM systems. The MC14400 and MC14403 are general purpose devices that are offered in a 16-pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on-chip precision voltage reference. The MC14401 is the same device, but offered in an 18-pin package. In addition, it offers the user the capability of selecting from three peak overload voltages (2.5, 3.15 and 3.78 V). The MC14405 is a synchronous device in a 16-pin package intended for instrument use. The MC14402 is the full feature device which presents all of the options available on the chip. This device is packaged in a 22-pin DIP and 28-pin chip carrier package, and contains all the features of the MC14400 and MC14401 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

The devices were designed to be upward compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of TSACs (MC14416/MC14417/MC14418) as well as the MC3419 SLIC.

The PCM codec-filter mono-circuits utilize CMOS due to its reliable low-power performance and proven capability for complex analog/ digital LSI functions.

MC14400

- 16-Pin Package
- On-Chip Precision Voltage Reference (3.15 V)
- Power Dissipation — 45 mW at 2.048 MHz at 10 V
  0.1 mW Powered Down at 10 V
- Compatibility with Various Supply Configurations: ±5, ±6, +10, +12 Volts (5%)
- Pin Selectable TTL and CMOS Digital Levels
- Automatic Prescale Divide of Any One of 5 Clock Frequencies (128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz) to Generate the Internal Sequencing Clock
- Pin Selection of Both A-LAW/Mu-LAW Companding and D3/D4 or CCITT Digital Formats
- Output Drive Capability for 600 and 900 Ohm Loads of +12 dBm
- Synchronous and Asynchronous Operation
- On-Chip Attendent Interrupt Conferencing
- Transmit Bandpass and Receive Low-Pass Filters on Chip

MC14401 — All of the Above Plus:

- 18-Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15 and 3.78 Volts)
- Access to the "Minus" Input of the Tx Input Op Amp

MC14402 — All of the Above Plus:

- 22-Pin Package
- Variable Data Clocks (64 kHz to 3.088 MHz)
- Access to Transmit Input Amplifier
- An External Precision Reference May Be Used
- External Gain Adjust for Complex SLIC Configurations

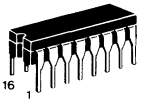
MC14403

- 16-Pin Package
- Same Device as MC14400 with Access to Transmit Input Amplifier with Single Ended Receive Output
- MSI Tied Internally to TDE

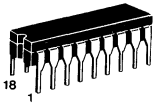
MC14405

- 16-Pin Package
- Same Device as MC14403 with Common 64 kHz to 3.088 MHz Data Clocks

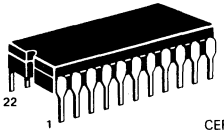
USE MC1400 SERIES FOR NEW DESIGN



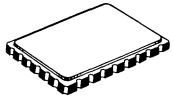
MC14400/03/05
L SUFFIX
CERAMIC PACKAGE
CASE 620



MC14401
L SUFFIX
CERAMIC PACKAGE
CASE 726



MC14402
L SUFFIX
CERAMIC PACKAGE
CASE 736



MC14402
Z SUFFIX
28-PIN CHIP CARRIER
CASE 763

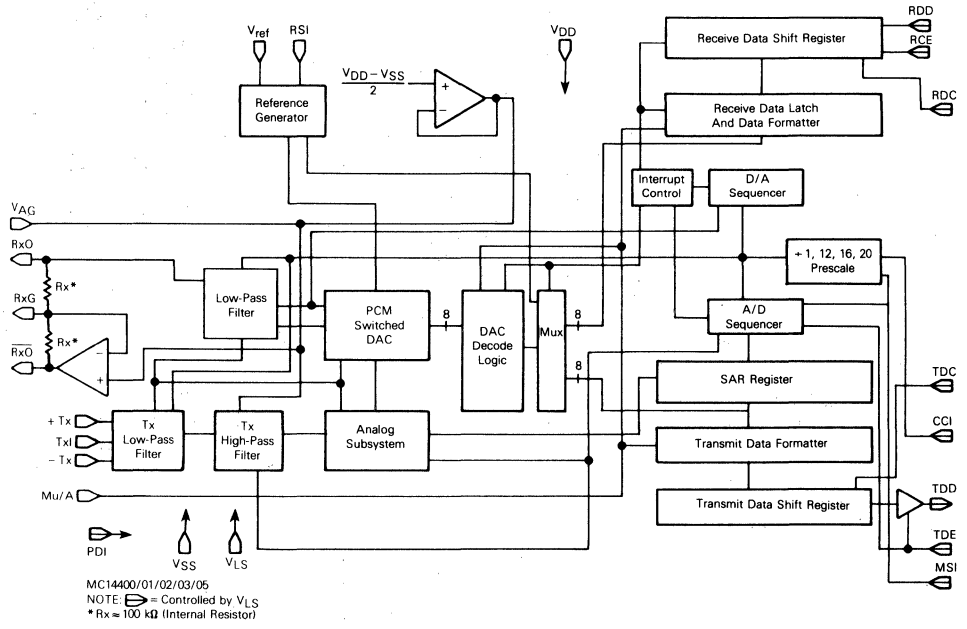
ORDERING INFORMATION

MC14XXXXX

- 1 CCITT (G7.12)
- 2 D3/D4 (PUB 43801)
- L Ceramic Package
- Z Leadless Ceramic Package

2

PCM MONO-CIRCUIT BLOCK DIAGRAM



DEVICE DESCRIPTIONS

There are five distinct versions of the Motorola PCM mono-circuit.

MC14400

The MC14400 PCM mono-circuit is a PCM codec-filter intended for standard word interleaved synchronous or asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty) 1.536, 1.544, 2.048 or 2.56 MHz. (For other data clock frequencies see MC14402 or MC14405.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the + 3 dBm0 level of the PCM mono-circuit. All other functions are described in the pin description.

MC14401

The MC14401 PCM mono-circuit offers the same features and is for the same application as the MC14400, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 Vp, 3.15 Vp or 3.78 Vp. The – Tx pin allows for external transmit gain adjust and simplifies interface to the MC3419 SLIC. Otherwise, it is identical to MC14400.

MC14402

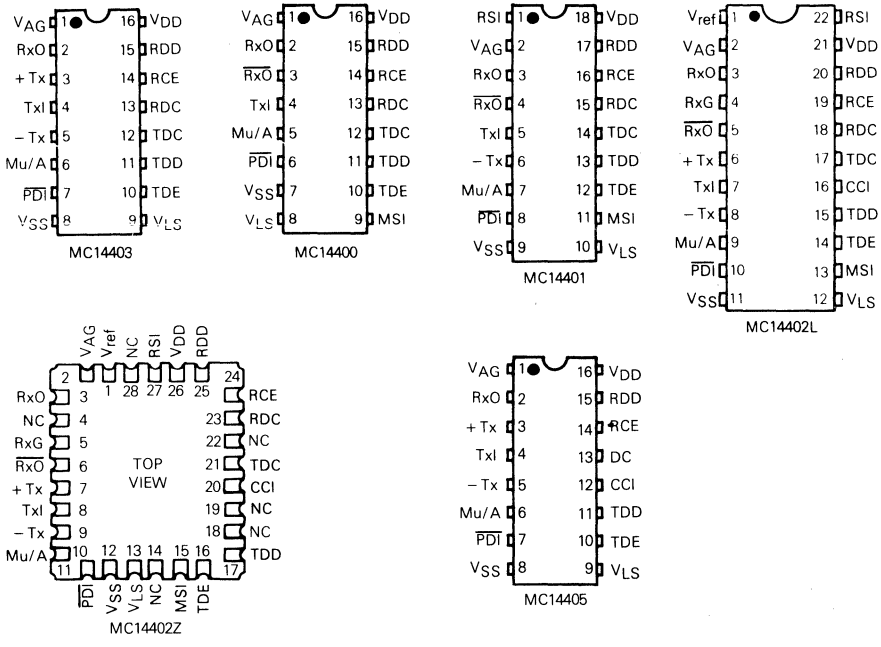
The MC14402 PCM mono-circuit is the full featured 22-pin device. It is intended for use in applications requiring maximum flexibility. The MC14402 contains all the features of the MC14400 and MC14401. The MC14402 is intended for bit interleaved or word interleaved operation with data clock frequencies which are non standard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input and the data clock inputs can be any frequency between 64 kHz and 3.088 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference and RxG and + Tx provide maximum flexibility for analog interface.

MC14403

The MC14403 PCM mono-circuit is intended for standard word interleaved asynchronous or synchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty) 1.536, 1.544, 2.048 or 2.56 MHz. (For other data clock frequencies see MC14402 or MC14405.) The internal reference is set of 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the + 3 dBm0 level of the PCM mono-circuit. The + Tx and – Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC14405

The MC14405 PCM mono-circuit is intended for word interleaved synchronous applications. The MC14405 has all the features of the MC14403 but internally connects TDC and RDC (see pin description) to the DC pin. One of five standard frequencies (listed above) should be applied to CCI and the DC input can be any frequency between 64 kHz and 3.088 MHz.



MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{CC} to V_{SS}	6	10 to 12	13	V
Power Dissipation CMOS Mode 10 V TTL Mode 10 V	V_{DD} to V_{SS}	– –	45 75	70 110	mW
Power Down Dissipation 10 V	V_{DD} to V_{SS}	–	0.1	1.0	mW
Frame Rate Transmit and Receive	MSI	7.5	8.0	8.5	kHz
Data Rate MC14400, MC14401, and MC14403 (Must Use One of These Frequencies) ±2%	TDC, RDC	– – – – –	128 1536 1544 2048 2560	– – – – –	kHz
Data Rate MC14402, MC14405		64	–	3088	kHz
Full Scale Output and Input Levels MC14400, MC14403, MC14405	RxO, TxI	–	3.15	–	Vp
MC14401 and MC14402, $V_{ref} = V_{SS}$ RSI = V_{DD}	RxO, TxI	–	3.78	–	Vp
RSI = V_{SS}	RxO, TxI	–	3.15	–	Vp
RSI = V_{AG}	RxO, TxI	–	2.50	–	Vp

2

DIGITAL LEVELS (T_A = 0 to 70°C)

Parameter		Symbol	V_{DD} to V_{SS}	Min	Typ	Max	Unit
CMOS Mode							
TDE, RCE, RDD, $\overline{PDI}$, RDC, TDC, DC, CCI, MSI	"0"	–	12	–	5.25	3.6	V
	"1"	–	12	8.4	6.75	–	
TTL Mode							
TDE, RCE, RDD, $\overline{PDI}$, RDC, TDC, DC, CCI, MSI	"0"	–	10	–	V_{LS} + 1.0	V_{LS} + 0.8	V
	"1"	–	10	V_{LS} + 2.0	V_{LS} + 1.8	–	
TDD Output Current							
(TTL Mode)	V_{OH} = 2.4 V	I_{OH}	10	150	–	–	μA
	V_{OL} = 0.8 V	I_{OL}	–	1.6	–	–	ma

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, 0 dBm0 = +6 dBm@600 Ω, V_{LS} = V_{AG} = 0, T_A = 0 to 70°C, TDC = RDC; TDE = RCE = 8 kHz)

Characteristic	E to E		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz)	−0.3	+0.3	−0.3	+0.3	−0.3	+0.3	dB
Gain vs Level Tone (Relative to −10 dBm0, 1.02 kHz)							
+3 to −40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
−40 to −50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
−55 dBm0	−1.6	+1.6	−1.0	+1.0	−0.8	+0.8	
Gain vs Level – Pseudo Noise (A-Law Only, MC144XXL1 Only) (Relative to −10 dBm0)							
−10 to −55 dBm0	−0.45	+0.45	–	–	–	–	dB
−60 dBm0	−0.90	+0.90	–	–	–	–	
Total Distortion – 1.02 kHz Tone (C Message)							
0 to −30 dBm0	35	–	35	–	36	–	dB
−40 dBm0	29	–	29	–	30	–	
−45 dBm0	24	–	24	–	25	–	
Total Distortion with Noise (A-Law Only, MC144XXL1 Only)							
−3 dBm0	27.5	–	–	–	–	–	dB
−6 to −27 dBm0	35	–	–	–	–	–	
−34 dBm0	33.1	–	–	–	–	–	
−40 dBm0	28.5	–	–	–	–	–	
−55 dBm0	13.5	–	–	–	–	–	
Idle Noise							
(Mu Law, C Message)	–	18	–	18	–	13	dBrnCo
(A Law, Psophometric – MC144XXL1 Only)	–	−68	–	−68	–	−75	dBmOp
Frequency Response (Relative to −10 dBm0, 1.02 kHz)							
15 to 60 Hz	–	−23	–	−23	–	0.15	dBm0
300 to 3000 Hz	−0.30	+0.30	−0.15	+0.15	−0.15	+0.15	
3400 Hz	−1.6	0	−0.8	0	−0.8	0	
4000 Hz	–	−28	–	−14	–	−14	
4600 Hz	–	−60	–	−32	–	−30	
Inband Spurious (1.02 kHz@0 dBm0)							
300 to 3400 Hz	–	−43	–	−43	–	−43	dBm0
Out-of-Band Spurious (0 to 12 kHz in, @0 dBm0)							
0 to 3400 Hz	–	−30	–	−30	–	–	dBm0
3400 to 4600 Hz	–	−28	–	–	–	–	
4600 Hz to 12 kHz	–	−30	–	–	–	–	
Idle Noise Selective							
@ 8 kHz with V_{AG} = TxI Measure at RxO, 30 Hz Bandwidth	–	−50	–	–	–	–	dBm0
Group Delay Difference							
0 dBm0, TDC, RDC = 2.048 MHz							
500 to 600 Hz	–	80	–	–	–	–	μsec
600 to 1000 Hz	–	60	–	–	–	–	
1000 to 2600 Hz	–	140	–	–	–	–	
2600 to 2800 Hz	–	80	–	–	–	–	
Go to Return Crosstalk @0 dBm0							
TxI to TDD @ RxO RDD to RxO @ TDD	–	–	–	−65	–	−65	dBm0
Absolute Group Delay @ 1.02 kHz							
TDC = RDC = 2.048 MHz	–	460	–	–	–	–	μs

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = (10-12 V) ±5%, 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	−Tx, +Tx, (TxI for MC14400)	I_{in}		±0.01	±30	nA
AC Input Impedance (1 kHz)	TxI (for MC14400) to V_{AG}	Z_{in}	100	200	–	kΩ
AC Input Impedance (1 kHz)	−Tx, +Tx to V_{AG}	Z_{in}	1.5	5.0	–	MΩ
Input Common Mode Voltage Range V_{DD} = 10.0 V	−Tx, +Tx	V_{ICR}	+1.5	–	+8.0	V
Output Voltage Range						
RL = 20 k to V_{AG}	RxO, $\overline{RxO}$	V_{OR} to V_{AG}	−4.0	–	+4.0	V
RL = 600 to V_{AG}	Each		−3.2	–	+3.2	
RL = 900 to V_{AG}	Output		−3.9	–	+3.9	
Output Current RxO, $\overline{RxO}$	$V_{OH} = V_{DD}$ 0.8		−5.0	–	–	mA
	V_{OL} = 0.8	–	+5.0	–	–	
Power Supply Rejection Ratio	RxO to V_{AG}	PSRR	30	40	–	dB
V_{DD} = 12 V ±0.05 V peak @ 1 kHz	$\overline{RxO}$ to V_{AG}		30	40	–	
Shared External Reference	V_{ref} to V_{AG}		2.0	–	3.8	V
V_{ref} Input Current		I_{in}	–	0.3	–	mA
V_{AG} Output Current	Source	I_{VAG}		200		μA
	Sink	I_{VAG}		8.0		mA

MODE CONTROL LOGIC (V_{SS} = 0 V, 0 to 70°C)

Characteristics		V_{DD} Vdc	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode		10	0	–	6.0	V
		12	0	–	8.0	
V_{LS} Voltage for CMOS Mode		10	9.5	–	–	V
		12	11.5	–	–	
Mu/A Select Voltage						
Mu-Law Mode		10	9.5	–	–	V
		12	11.5	–	–	
Sign Magnitude Mode		10	4.0	–	6.0	
		12	5.0	–	7.0	
A-Law Mode		10	–	–	0.5	
		12	–	–	0.5	
Reference Select Voltage	3.78 V Mode	10	9.5	–	–	V
		12	11.5	–	–	
	2.5 V Mode	10	4.0	–	6.0	V
		12	5.0	–	7.0	
	3.15 V Mode	10	–	–	0.5	V
		12	–	–	0.5	
V_{ref} Mode Voltage	External Reference Mode	10	4.0	–	–	V
		12	5.0	–	–	
	Internal Reference Mode	10	–	–	0.5	
		12	–	–	0.5	
Analog Test Mode Selection Frequency, MSI = CCI		10	–	128	–	kHz
See Pin Description; Test Modes		12	–	128	–	

2

SWITCHING CHARACTERISTICS (V_{DD} = (10 to 12 V), T_A = 0 to 70°C, C_L = 50 pF CMOS or TTL Mode)

Characteristic				Symbol	Min	Typ	Max	Unit
Output Rise Time Output Fall Time			TDD	t_{TLH} t_{THL}	–	30	80	ns
Input Rise Time Input Fall Time			DC, TDE, CCI, RCE, RDC, TDC, MSI	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width			DC, TDE Low, CCI, RCE, RDC, TDC, MSI	t_{WH}	100	–	–	ns
Clock Pulse Frequency			DC, TDC, RDC	f_{CL}	64	–	3088	kHz
Clock Pulse Frequency (MSI = 8 kHz) This Pin Will Accept One of These 5 Discrete Clock Frequencies and Compensate to Produce Internal Sequencing.			CCI 1 2 3 4 5	f_{CL1} f_{CL2} f_{CL3} f_{CL4} f_{CL5}	– – – – –	128 1536 1544 2048 2560	– – – – –	kHz
Propagation Delay Time	TTL		TDE to TDD Low Impedance	t_{P1}	85	130	180	ns
	CMOS		TDE to TDD Low Impedance	t_{P1}	50	100	160	
	TTL		TDE to TDD High Impedance	t_{P2}	–	50	75	
	CMOS		TDE to TDD High Impedance	t_{P2}	–	20	40	
	TTL		TDC* to TDD	t_{P3}	–	120	180	
	CMOS		TDC* to TDD	t_{P3}	–	80	160	
TDE Rising Edge to TDC Falling Edge Setup Time				t_{su1} t_{su2}	20 100	– –	– –	ns ns
RCE Rising Edge to RDC Falling Edge Setup Time				t_{su3} t_{su4}	20 100	– –	– –	ns ns
MSI Rising Edge to CCI Falling Edge Setup Time				t_{su6} t_{su7}	20 100	– –	– –	ns ns
RDD Valid to RDC Falling Edge Setup Time				t_{su5}	60	40	–	ns
RDD Hold Time from RDC Falling Edge				t_h	100	60	–	ns

*For the sign bit, t_{P3} is measured from TDE or TDC, whichever is last.

PIN DESCRIPTION

DIGITAL

V_{LS} selects CMOS or TTL compatibility for all digital I/Os. $V_{LS} = V_{DD}$; all I/O is CMOS, (V_{DD} to V_{SS} swing). $V_{LS} < V_{DD} - 4$ volts; all I/O is TTL with switchpoint 1.4 V above V_{LS}. The pins controlled by V_{LS} are inputs MSI, CCI, TDC, RDC, TDE, RCE, RDD, $\overline{PDI}$ and output TDD. In TTL applications V_{LS} is Digital GND.

MSI is a continuous 8 kHz (for sampling rate) signal which is used as a time base for internally selecting a prescale divider for CCI input. MSI should be tied to the frame sync or system sync signal, but has no relation to transmit or receive data timing, except as described under TDE. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied to TDE in MC14403/05.)

CCI input is designed to accept five discrete clock frequencies. These are 128 kHz 40 to 60% duty cycle, 1.536 MHz, 1.544 MHz, 2.048 MHz or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The four clocks in the MHz frequency range have only minimum pulse width duty cycle requirements. In the asynchronous applications, CCI should be derived from transmit timing. (CCI is tied to TDC in MC14400/01/03).

TDC is the transmit data bit rate input. It can be any frequency from 64 kHz to 3.088 MHz, and is often tied in common to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and leading edges produce successive data bits at TDD. In asynchronous applications, TDE should be derived from this clock. (TDC and RDC are tied together in MC14405 and are called DC.)

TDE serves two functions for the transmit data timing. It establishes the transmit sync in conjunction with MSI. If the leading edges of TDE occur at 8 kHz and both MSI and TDE are derived from TDC, then the MSI relationship is transparent and TDE is simply transmit sync. The leading edge of TDE produces the sign bit at TDD during the current TDC period. The TDC shifts out the remaining bits at the TDC rate. The TDD pin is active as long as TDE is high. If there is more than one TDE leading edge per frame, then the first TDE after MSI is the Tx sync. Thus, TDE may be taken low to three state TDD after the first leading edge. The additional TDE high periods before the next MSI merely un-three-states TDD. This can be used for bit interleaved systems. In asynchronous applications, TDE is derived from TDC.

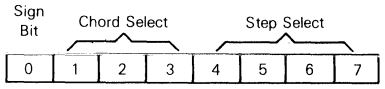
TDD is the digital data output. It operates in sync with TDC and TDE. It is a three-state output. TDC, TDE, and TDD independently control transmit data timing. The data format (Mu-Law, A-Law or sign magnitude) is controlled by Mu/A. This output may be made high-speed CMOS compatible using a pullup resistor.

RDC is the receive data clock and works in conjunction with RCE and RDD to produce all receive data timing. These three signals must be synchronous, but can be asynchronous with all other digital pins. RDC provides the receive register clock. The RDC clock may be any frequency from 64 kHz to 3.088 MHz.

RCE – The rising edge of RCE should identify the sign bit of a receive word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In the asynchronous mode and with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive words may be decoded each transmit frame to allow on chip conferencing.

RDD is the digital data input. It operates synchronously with RDC and RCE. The data format is determined by the Mu/A pin.

Code	Sign/ Magnitude	Mu-Law	A-Law (CCITT)
+ full scale	1111 1111	1000 0000	1010 1010
+ zero	1000 0000	1111 1111	1101 0101
− zero	0000 0000	0111 1111	0101 0101
− full scale	0111 1111	0000 0010	0010 1010



Note: Starting from sign magnitude, to change format:
To Mu-Law −
MSB is unchanged (sign)
invert remaining seven bits
if code is 0000 0000, change to 0000 0010 (for zero code suppression)
To A-Law −
MSB is unchanged (sign)
invert odd numbered bits
ignore zero code suppression

Mu/A Select − This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu255 Companding D3 Data Format with Zero Code Supress

Mu/A = V_{AG}; Mu255 Companding with Sign Magnitude Data Format

Mu/A = V_{SS}; A-law Companding with CCITT Data Format Bit Inversions

$\overline{PDI}$ − The power down input disables the bias circuitry and gates off all clock inputs. This puts the TxI, RxO, $\overline{RxO}$, and T_{DD} outputs into a high impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI} = V_{LS}$ or V_{SS}. The circuit operates normally with $\overline{PDI} = V_{DD}$ or with a logic high as defined by connection at V_{LS}. T_{DD} will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DC − In the MC14405, TDC and RDC are internally connected to this pin.

ANALOG

V_{AG} Analog Ground

Each version of the PCM mono-circuit produces its own analog ground internally. The DC voltage is approximately $(V_{DD} - V_{SS})/2$. All analog functions within the device use this as a reference point for signal processing. In symetric dual supply systems (±5, ±6, etc.), V_{AG} may externally be tied to the system analog ground supply. The V_{AG} output will sink more than 8 mA of current, but can source only 200 μA. When RxO or $\overline{RxO}$ are output drives for 600 or 900 loads tied to V_{AG}, a pullup resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground.

V_{ref} Positive Voltage Reference Input (MC14402 Only)

The V_{ref} pin provides for the supply of an external voltage reference or for the selection of an internal reference within the PCM mono-circuit. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected. In each case, the overload or full scale gains of the codec are selected by the reference select pin (RSI). Both the internal and external references are inverted within the PCM mono-circuit for negative input voltage such that only one reference is required.

External Mode − In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 volt reference like the MC1403 is connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref}s and V_{AG}s from different PCM mono-circuits. In special applications, the reference voltage may be between 2 and 4 volts. However, the gain selection logic associated with RSI must be considered to arrive at the desired PCM mono-circuit gain.

Internal Mode − In the internal reference mode ($V_{ref} = V_{SS}$), an internal reference supplies the reference voltage for the PCM mono-circuit.

RSI Reference Select Input (MC14401/02 Only)

The RSI input allows the selection of three different overload or full scale voltages independent of the internal or external reference mode. The selection of maximum signed level is made by connecting RSI to V_{DD}, V_{AG} or V_{SS}. The various modes of operation are summarized in the table below. The internal reference is designed to give internal gains equal to those obtained with an external 2.5 volt reference.

RxO and $\overline{RxO}$ Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak-to-peak signal described with the reference. If a 2.5 V reference is used with RSI tied to V_{AG} and a +3 dBm0 sine wave is decoded, the RxO output will be a 5 V peak-to-peak signal. $\overline{RxO}$ will also have a signal output of 5 V peak-to-peak. External loads may be connected from RxO to $\overline{RxO}$ for a 6 dB push-pull signal gain or from either RxO or $\overline{RxO}$ to V_{AG}. With RSI tied to V_{SS}, each output will drive 600 Ω to +9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to +9 dBm.

ADDITIONAL PIN DESCRIPTIONS

RxG Receive Output Gain Adjust (MC14402 Only)

If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{RxO}$. Thus the push-pull gain to a load from RxO to $\overline{RxO}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{RxO}$ (RG), the gain of $\overline{RxO}$ can be set differently from −1. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{RxO}$ gain is equal to minus RG/RI(VRxO). The purpose of RxG is to allow external receive gain adjustment. The circuit for RxG and $\overline{RxO}$ is shown in the block diagram.

+Tx Positive Tx Amplifier Input (MC14402/03/05 Only)
−Tx Negative Tx Amplifier Input (MC14401/02/03/05 Only)

The TxI pin is the input to the transmit bandpass filter. If +Tx or −Tx are available, then there is an internal amplifier preceding the filter whose pins are +Tx, −Tx and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 k. If +Tx is not available, it is internally tied to V_{AG}. If −Tx and +Tx are not available, the TxI is a unity gain high impedance input.

2

TxI Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC14401/02/03/05. The input impedance is greater than 100 k to V_{AG} in the MC14400. The TxI input has an internal gain of 1.0, such that a +3 dBm0 signal at TxI corresponds to the peak-to-peak swing of RxO described above. For ±2.5 V shared references and RSI = V_{AG}, the +3 dBm0 input should be 5.0 volt peak-to-peak.

Power Supplies

V_{DD} – Most Positive Supply. V_{DD} is typically 10 to 12 volts.

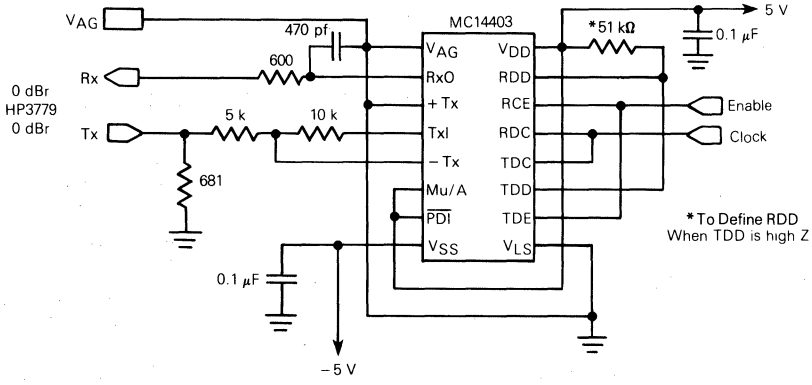
V_{SS} – Most Negative Supply. This is the most negative supply pin.

For single-supply systems, these are the only power pins. V_{LS} will be tied to V_{SS} or V_{DD} and V_{AG} is an output. In dual-supply systems, V_{LS} may be digital ground and V_{AG} may be analog ground.

Testing Considerations (MC14400/01/02 Only)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the codec (the output of the Tx filter) is available on the PDI pin. This input is a DC auto zeroed access to the A/D side of the codec. If monitored with a high-impedance buffer, the output of the Tx low-pass filter can also be measured at the PDI pin. This test mode allows independent evaluation of the transmit low-pass filter and A/D side of the codec. The receive channel of the mono-circuit is tested with the codec and filter together.

TEST CIRCUIT



OPTIONS AVAILABLE BY PIN SELECTION

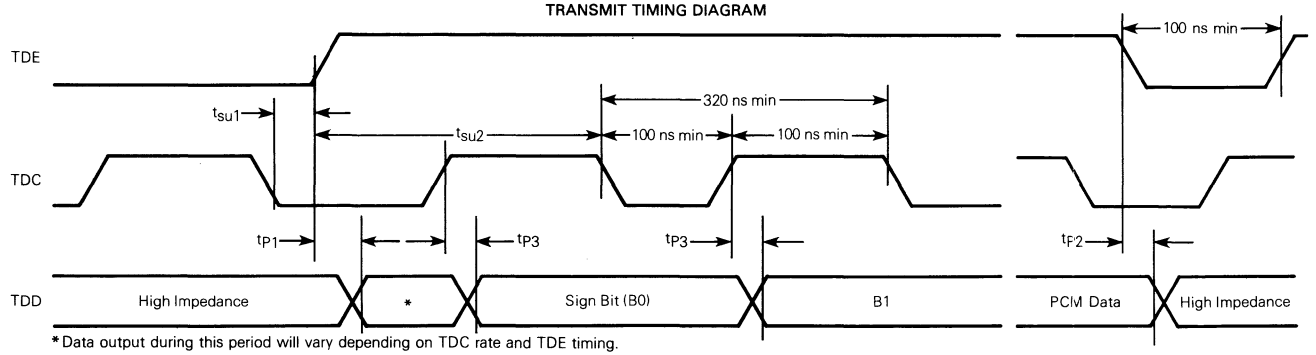
RSI* Pin Level	V_{ref}* Pin Level	Peak-to-Peak Overload Voltage (TxI, RxO)
V_{DD}	V_{SS}	7.56 V_{PP}
V_{DD}	$V_{AG}+V_{EXT}$	(3.02 × V_{EXT}) V_{PP}
V_{AG}	V_{SS}	5 V_{PP}
V_{AG}	V_{AG} + V_{EXT}	(2 × V_{EXT}) V_{PP}
V_{SS}	V_{SS}	6.3 V_{PP}
V_{SS}	V_{AG} + V_{EXT}	(2.52 × V_{EXT}) V_{PP}

*On MC14400/03/05, RSI and V_{ref} tied internally to V_{SS}.
On MC14401, V_{ref} tied internally to V_{SS}.

SUMMARY OF OPERATION CONDITIONS USER PROGRAMMED THROUGH PINS V_{DD}, V_{AG}, AND V_{SS}

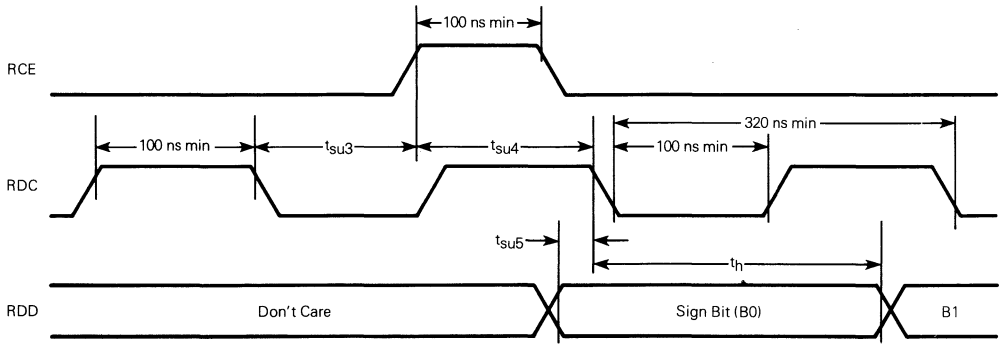
Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu-Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu-Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A-Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up

TRANSMIT TIMING DIAGRAM

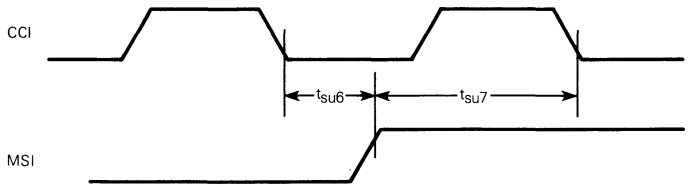


*Data output during this period will vary depending on TDC rate and TDE timing.

RECEIVE TIMING DIAGRAM



CCI/MSI TIMING DIAGRAM



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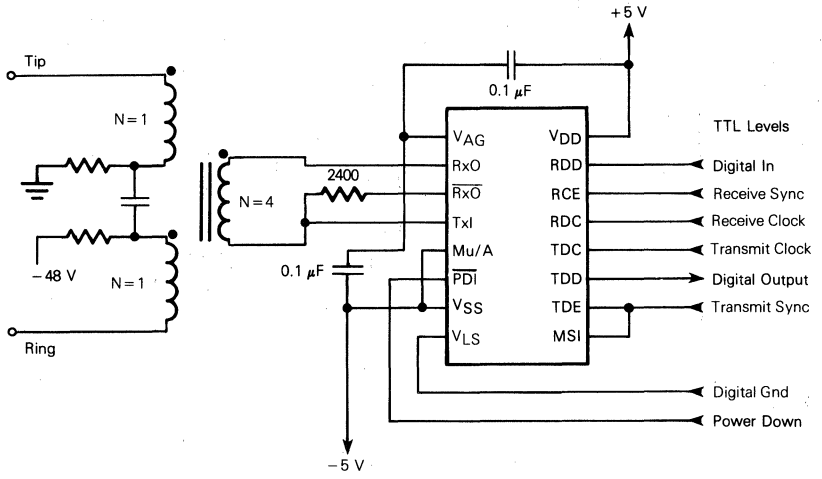
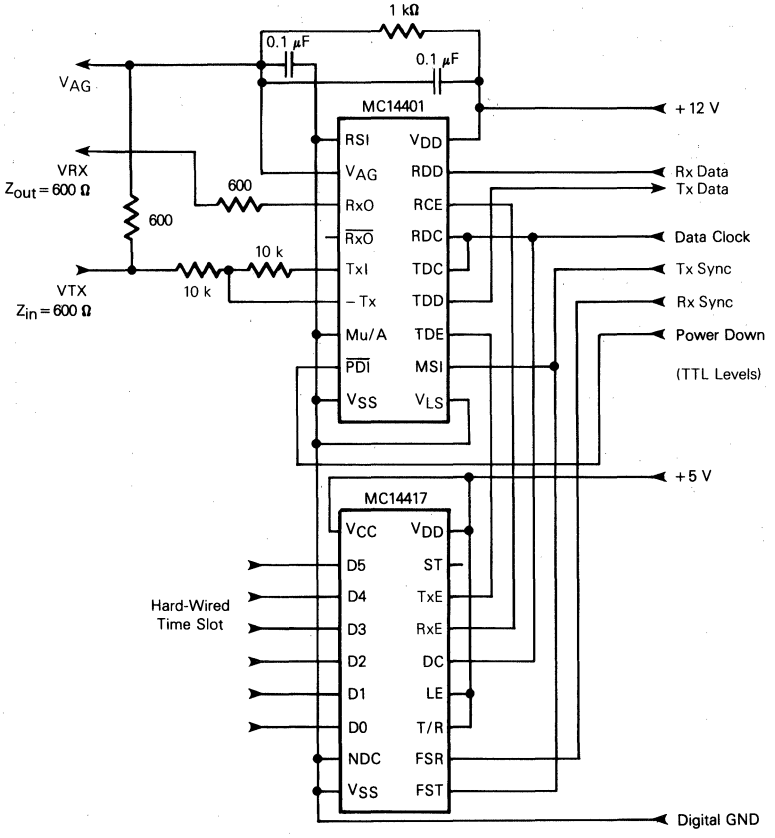
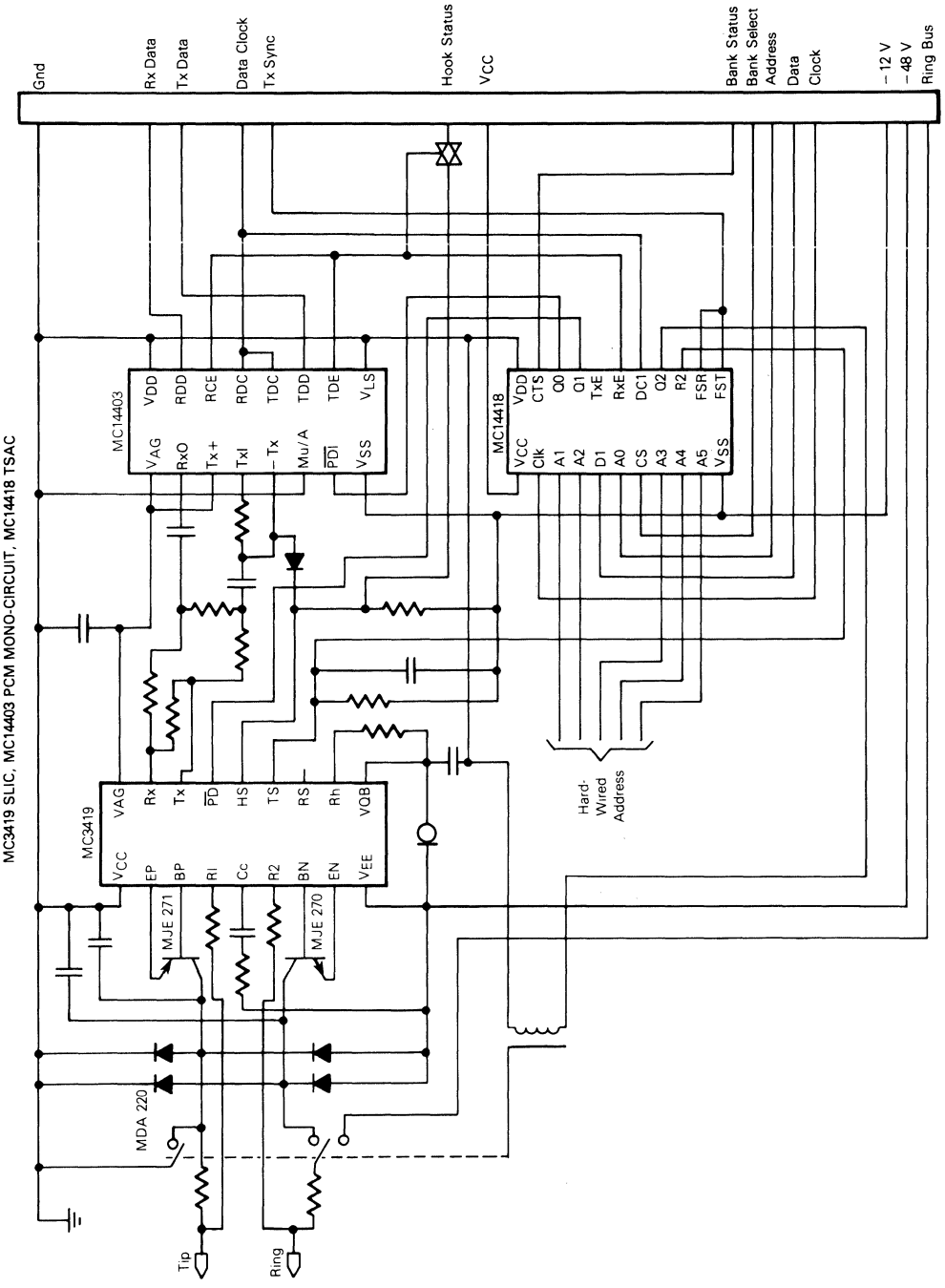
THE BASIC VOICE CHANNEL USING THE MC14400 PCM CODEC/FILTER MONO-CIRCUIT



MC14401 PCM MONO-CIRCUIT WITH MC14417 TSAC

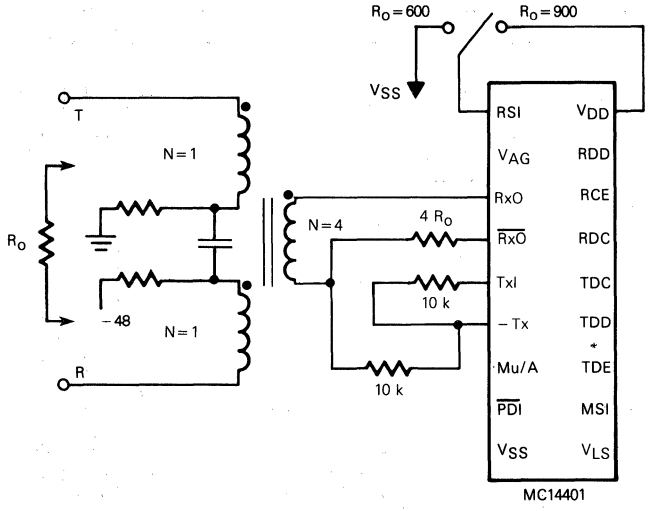


A COMPLETE SINGLE PARTY CHANNEL UNIT USING
MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC

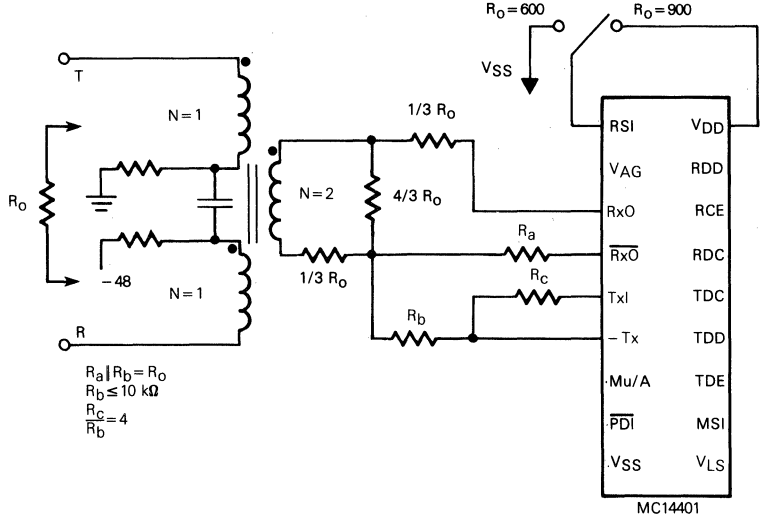


2

HYBRID INTERFACES TO MC14401 PCM CODEC FILTER MONO-CIRCUIT

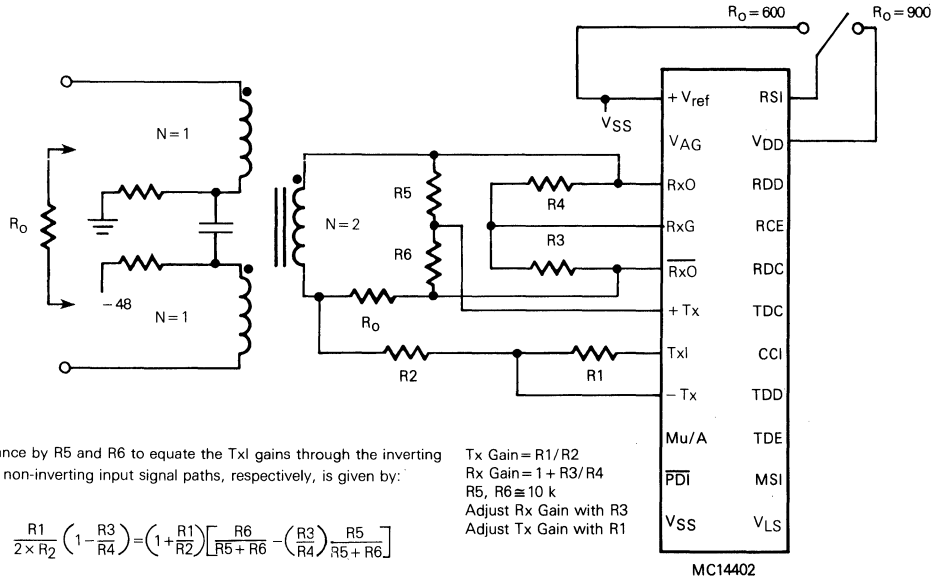


Simplified Transformer Hybrid Using MC14401



"T" Padded Transformer Hybrid Using MC14401

HYBRID INTERFACES TO THE MC14402 PCM CODEC/FILTER MONO-CIRCUIT

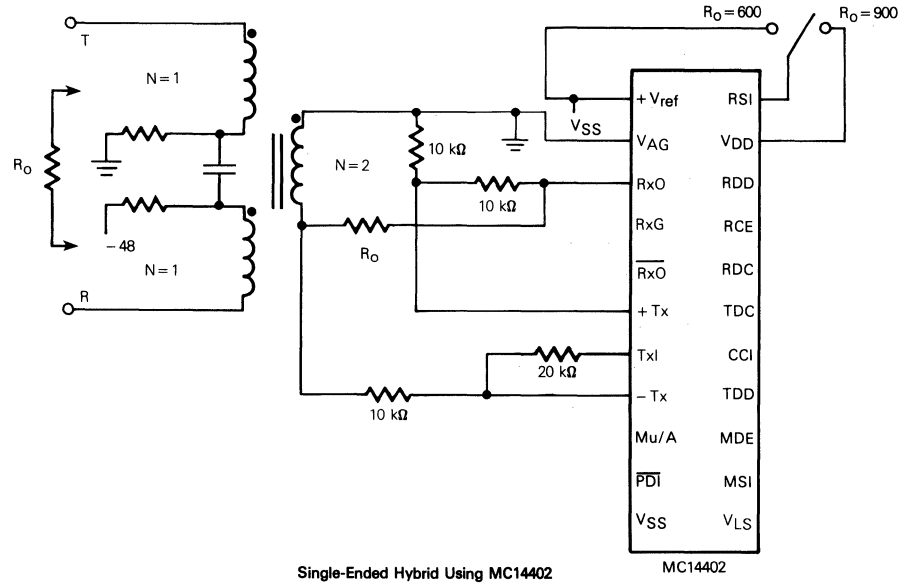


Balance by R5 and R6 to equate the Txl gains through the inverting and non-inverting input signal paths, respectively, is given by:

$$\frac{R1}{2 \times R_2}\left(1-\frac{R3}{R4}\right)=\left(1+\frac{R1}{R2}\right)\left[\frac{R6}{R5+R6}-\left(\frac{R3}{R4}\right)\frac{R5}{R5+R6}\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≅ 10 k
Adjust Rx Gain with R3
Adjust Tx Gain with R1

Universal Transformer Hybrid Using MC14402



Single-Ended Hybrid Using MC14402

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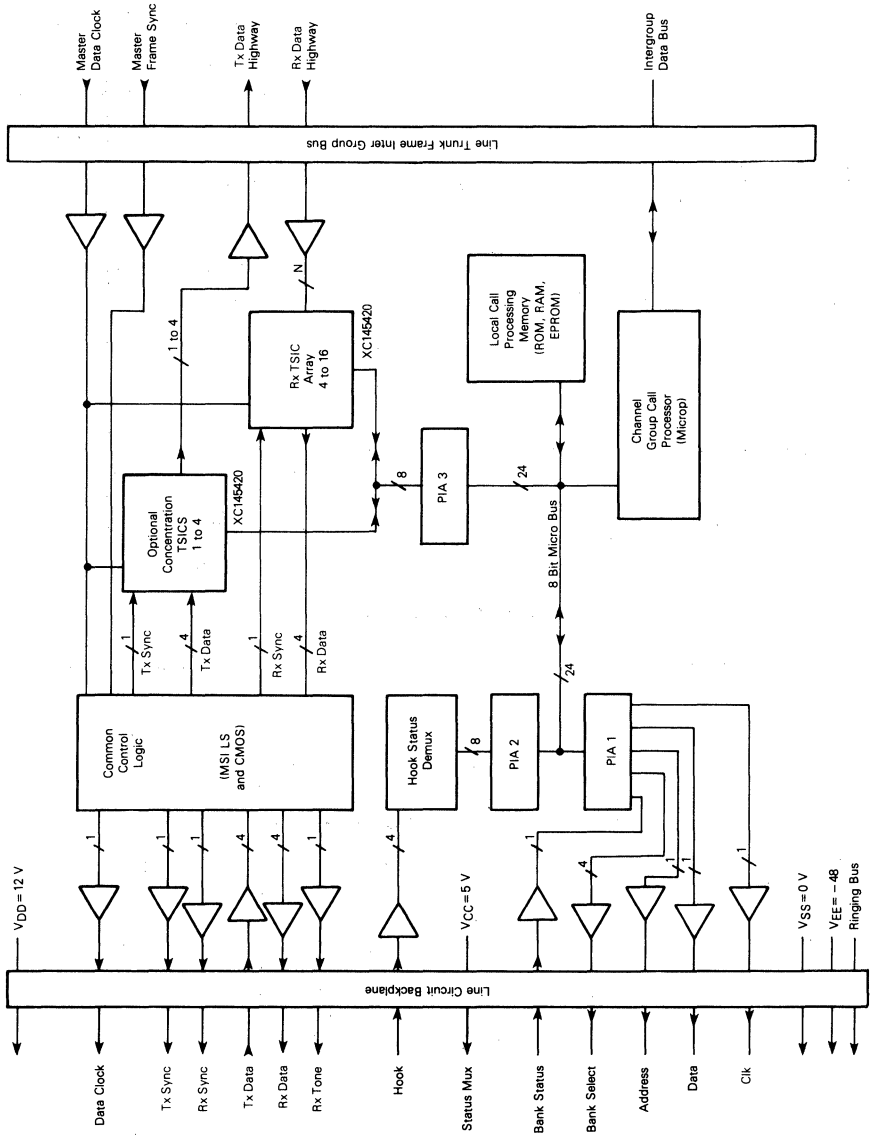
128 CHANNEL GROUP COMMON CONTROL
IN A TYPICAL SWITCHING SYSTEM



NOTE: See single party line drawing for line card details.

MC14408
MC14409

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

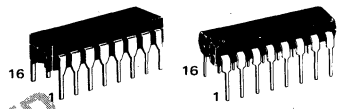
BINARY TO PHONE PULSE CONVERTER SUBSYSTEM

The MC14408 and the MC14409 are devices designed to convert a four bit binary input code to a number of serial output pulses corresponding to the value of the input code.

The devices can be used in telephone pulse dialing applications when combined with their companion device, the MC14419 (2-of-8 keypad-to-binary code converter). The devices have been partitioned to allow convenient addition of RAM memory and controls for repertoire dialing applications.

The MC14408 and MC14409 perform identical functions with the exception of the signal output at the DRO (Dial Rotating Output). In the MC14408, DRO remains high during continuous outpulsing of all digits and in the MC14409 DRO is low between each digit pulse burst.

- On-Chip Oscillator
- Diode Protection on All Inputs
- Dialing of Numbers Up to 16 Digits Long
- Memory Storage (FIFO) and Re-Dialing (single pin) of Last Telephone Number
- Hold Interrupt Control for Additional Interdigit Delays (such as a Wait for Intermediate Dial Tones)
- Selectable Dialing Rate (10 pps or 20 pps)
- Selectable Interdigit Time (300 or 800 ms @ 10 pps; 150 or 400 ms @ 20 pps)
- Selectable Make-Break Ratio (61% or 67%)
- Buffered Outputs Compatible with Discrete Transistor Driver Interface, One Low-power Schottky TTL Load or Two Low-power TTL Loads Over the Rated Temperature Range.
- Low Power Dissipation – I_{DD} (operating with oscillator) = 470 μA typ @ V_{DD} = 5.0 Vdc, f_{Osc} = 16 kHz, C_L = 50 pF

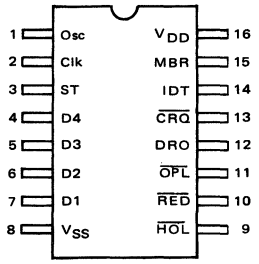


L SUFFIX
CERAMIC PACKAGE
CASE 620

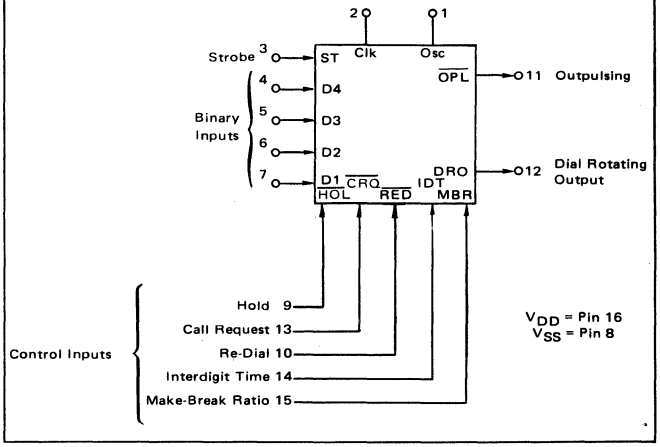
P SUFFIX
PLASTIC PACKAGE
CASE 648

NOT RECOMMENDED FOR NEW DESIGN

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Noise Immunity										
($\Delta V_{out} \leq$ 0.5 Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
($\Delta V_{out} \leq$ 0.5 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.80	-1.7	–	-0.60	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.20	–	-0.16	-0.36	–	-0.12	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
Input Current	I_{in}	6.0	–	0.3	–	±0.00001	±0.30	–	1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	12	–	5.0	12	–	12	pF
Operating Supply Current	I_{DD}	3	–	250	–	160	200	–	200	μAdc
f_{cl} = 16 kHz (operating		5	–	700	–	470	550	–	550	
with Osc)		6	–	1250	–	740	1000	–	1000	

FIGURE 1
TIMING DIAGRAM — DATA AND STROBE INPUTS

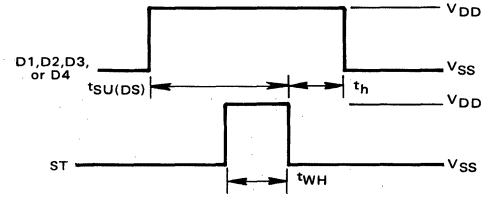
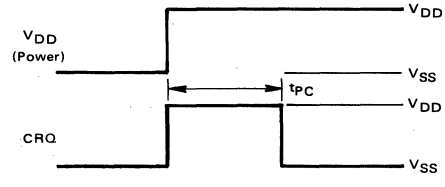


FIGURE 2
TIMING DIAGRAM — CALL REQUEST



If power is turned off after each call, CRQ must stay high after power is applied (for a duration of t_{PC}) to ensure no spurious outpulsing. For this use the redial function is invalid.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time** t_{TLH} = (3.0 ns/pF) C_L + 30 ns	t_{TLH}	5.0	–	180	400	ns
Output Fall Time** t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	ns
Power Up to Call Request Pause	t_{PC}	3 to 6	48/f_{cl}*	–	–	ms
Call Request to First Strobe Pulse	t_{CS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe to Strobe Separation Time	t_{SS}	3 to 6	48/f_{cl}*	–	–	ms
Strobe Pulse Width	t_{WH}	3 to 6	1.0	–	–	μs
Strobe to Data Hold Time	t_h	3 to 5	–	150	400	ns
Clock Frequency***	f_{cl}	3 to 6	12.5	16	100	kHz
Percent Break to Make Ratio	%MB	3 to 6				%
(MBR = 0)			–	61	–	
(MBR = 1)			–	67	–	
Outpulsing Rate (f_{OPL} = *f_{cl}/1.6)	f_{OPL}	3 to 6				pps
f_{cl} = 16 kHz			–	10	–	
f_{cl} = 32 kHz			–	20	–	
Interdigit Time	t_{ID}	3 to 6				ms
t_{ID} = (5 x IDT + 3)/f_{OPL}						
IDT = 0						
f_{OPL} = 10 pps			–	300	–	
f_{OPL} = 20 pps			–	150	–	
IDT = 1						
f_{OPL} = 10 pps			–	800	–	
f_{OPL} = 20 pps			–	400	–	
Strobe to Output Time	t_{SOI}	3 to 6				ms
Initial Outpulsing Stream						
IDT = 0						
f_{OPL} = 10 pps			300	–	400	
f_{OPL} = 20 pps			150	–	200	
IDT = 1						
f_{OPL} = 10 pps			800	–	900	
f_{OPL} = 20 pps			400	–	450	
Continued Outpulsing Stream	t_{SOC}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Hold to Outpulse Time	t_{HOL}	3 to 6				ms
IDT = 0 or 1						
f_{OPL} = 10 pps			100	–	200	
f_{OPL} = 20 pps			50	–	100	
Dial Rotating Overlap Time .	t_{DRO}	3 to 6				ms
f_{OPL} = 10 pps			–	100	–	
f_{OPL} = 20 pps			–	50	–	
Data to Strobe Setup Time (f_{cl} = 16 kHz)	$t_{SU(DS)}$	3 to 6	1.5	–	–	μs
Re-dial Pulse Width (f_{cl} = 16 kHz)	–	3 to 6	–	200	–	ns

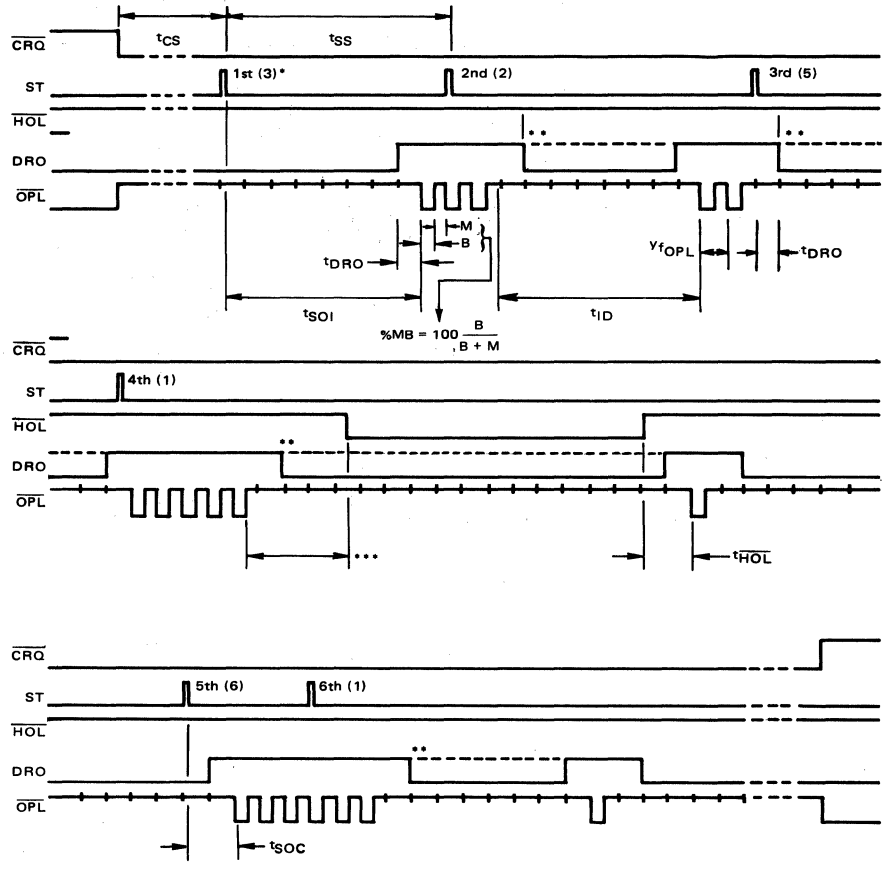
*f_{cl} in kHz

**The formula given is for the typical characteristics only.

*** Minimum clock pulse width = 1.0 μs.

2

FIGURE 3
PHONE DIALER SYSTEM TIMING DIAGRAM



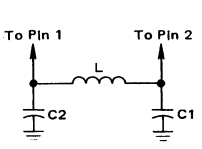
Notes:

(*)1st, 2nd, 3rd, etc., denotes Strobe pulse sequence — i.e., which digit in the phone number is being dialed. The number in parentheses denotes the numerical value of the digit being dialed. The examples define the various voltage — level and timing requirements, not a complete phone number.

(**)For the MC14408 the DRO signal will remain high provided digits remain in the memory, or a digit for continuing outpulsing is strobed in before the anticipated falling edge of the most significant digit in the memory. (i.e., [200 % MB] ms after the most significant outpulsing edge). The time from Strobe to DRO can be 0 to 100 ms.

(***)For the HOL signal to hold a next digit (e.g. the 4th, etc.,) the HOL falling edge must not appear after [t_{ID}-%MB + 100] ms the last outpulsing edge of the previous digit.

FIGURE 4
COMPONENT SELECTION FOR OSCILLATOR/CLOCK FREQUENCY



$f_{cl} = \frac{7.118}{\sqrt{LC}}$ where f_{cl} in kHz, L in mH, C = C1 = C2 in μF

$\%f_{cl} = -0.5\,[\%C + \%L] \pm 3.0$ where $\%f_{cl}$, %C, %L are the frequency capacitor, and inductor tolerances in percent. The ±3.0% accounts for supply voltage and ambient temperature variations.

EXAMPLE

L	%L	C=C1=C2	%C	f_{cl}	$\%f_{cl}$	OUTPULSING RATE $f_{OPL} = f_{cl}/1.6$
5.0 mH	±5.0	0.04 μF	±5.0	≈16 kHz	±8.0	≈10 pps
5.0 mH	±5.0	0.01 μF	±5.0	≈32 kHz	±8.0	≈20 pps

FIGURE 5
TRUTH TABLE

INPUTS							OUTPUTS	
$\overline{CRQ}$	D4 D3 D2 D1	ST	$\overline{RED}$	$\overline{HOL}$	IDT	MBR	$\overline{OPL}$	DRO †
1	X X X X	X	X	X	X	X	0	0
0	X X X X	0	1	1	X	X	1 (Steady State)	0 (Steady State)
0	X X X X (nth Digit)	⊓	1	1	X	X	Number of pulses (LF) of nth digit = binary combination of D4, D3, D2, D1. *	1 During outpulsing 0 Otherwise
0	X X X X	0	⊓	1	X	X	Digits of number in memory re-sent.	1 During outpulsing 0 Otherwise
0	X X X X	X	1	0	X	X	1 { After conclusion of digit being outpulsed.	0 { After conclusion of digit being outpulsed
X	X X X X	X	X	X	0 1	X	300 ms Interdigit time 800 ms Interdigit time } f_{cl} = 16 kHz	
X	X X X X	X	X	X	X	0 1	61% (≈1.6:1) Make-Break Ratio 67% (≈2:1) Make-Break Ratio	

X = Don't Care

* With the exception of 0000 which will give 10 pulses.

† Refer to timing diagram Figure 3.

FIGURE 6
MEMORY CLEAR

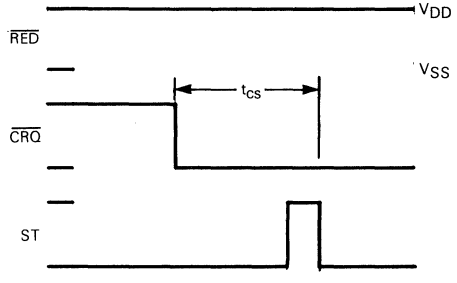
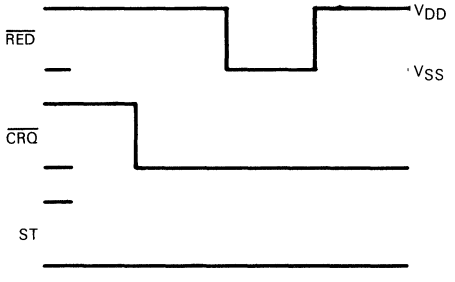


FIGURE 7
REDIAL SEQUENCE



2

DEVICE OPERATION

OSCILLATOR (Osc, Pin 1)

This pin is an input to the internal oscillator and feedback connection for the L-C π-network. An external clock signal, if desired can be applied to Osc.

CLOCK (Clk, Pin 2)

This pin is an output from the internal oscillator and feedback connection for the L-C π-network and provides the system clock for the MC14419 bounce eliminator circuitry.

STROBE INPUT (ST, Pin 3)

This Strobe input, when high (ST = V_{DD}), signifies that the data at the D1, D2, D3, and D4 inputs is valid, and enters the 4-bit number into the internal FIFO (First-In, First-Out) memory for subsequent outpulsing. The first strobe pulse after a call is requested (CRQ = low) clears the memory of any previous number and enters the first digit of the new number. Successive strobe pulses will store up to a maximum of 16 digits in the internal FIFO memory, which ignores all digits entered in excess of that amount until a new call is requested.

DATA INPUTS (D4, D3, D2, D1, Pins 4, 5, 6, 7)

These pins are the Data inputs to the internal memory. A binary coded digit number entered will result in an equivalent number of pulses at the $\overline{OPL}$ (outpulsing) output, except for the code 0000, which will outpulse 10 pulses.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 8)

This pin is the negative power supply connection. Normally this pin is system ground.

HOLD ($\overline{HOL}$, Pin 9)

When taken low ($\overline{HOL}$ = V_{SS}), the Hold input disables the outpulsing at the completion of the digit being outpulsed. When taken high, outpulsing resumes. This feature can be used in multi-dial-tone phone systems to provide longer interdigit pauses when necessary.

RE-DIAL ($\overline{RED}$, Pin 10)

The Re-Dial input, when taken low ($\overline{RED} = V_{SS}$) automatically outpulses the digits entered into memory after the last time a call was requested. (See Redial Sequence Diagram Figure 6.)

OUTPULSING ($\overline{OPL}$, Pin 11)

The Outpulsing output sends out bursts of pulses equivalent to the digits of the telephone number stored in the memory. The duty cycle and interdigit time of the digit pulse bursts are controlled, respectively by the MBR (Pin 15) and IDT (Pin 14).

DIAL ROTATING OUTPUT (DRO, Pin 12)

The Dial Rotating (also known as "Off Normal") Output provides a signal which indicates that digit pulse bursts are being sent. In the MC14409, DRO goes high (V_{DD}) at the beginning of the first digit pulse burst and goes low (V_{SS}) between succeeding consecutive digit pulse bursts. In the MC14408, however, DRO goes high at the beginning of the first digit pulse burst and remains high until the last digit pulse burst of the telephone number has been sent (see Timing Diagram, Figure 3).

CALL REQUEST ($\overline{CRQ}$, Pin 13)

The Call Request input when taken low ($\overline{CRQ} = V_{SS}$) resets internal counters and prepares the internal logic to either accept new digit inputs to be dialed, or to re-dial (see RED, Pin 10) the digits stored in the memory. The Relationship Between Memory Clear and Redial is shown in Figure 7.

INTERDIGIT TIME (IDT, Pin 14)

The Interdigit Timing input determines the length of time between consecutive digit pulse bursts. See the Interdigit Time (t_{ID}) in the switching characteristics for the length of time.

MAKE-BREAK RATIO (MBR, Pin 15)

The Make-to-Break Ratio input controls the duty cycle of the digit pulse bursts at the $\overline{OPL}$ output. For MBR = V_{DD}, duty cycle = 67% low, 33% high; and for MBR = V_{SS}, duty cycle = 61% low, 39% high.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

This pin is the package positive power supply pin.

FIGURE 8 — KEYPAD TO PULSE DIALER FLOW DIAGRAM

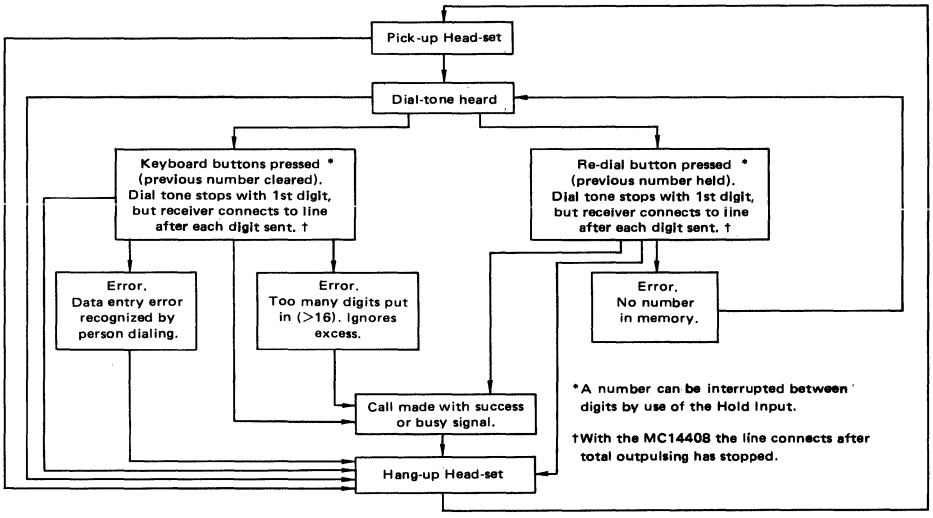


FIGURE 9 — PHONE DIALER SYSTEM

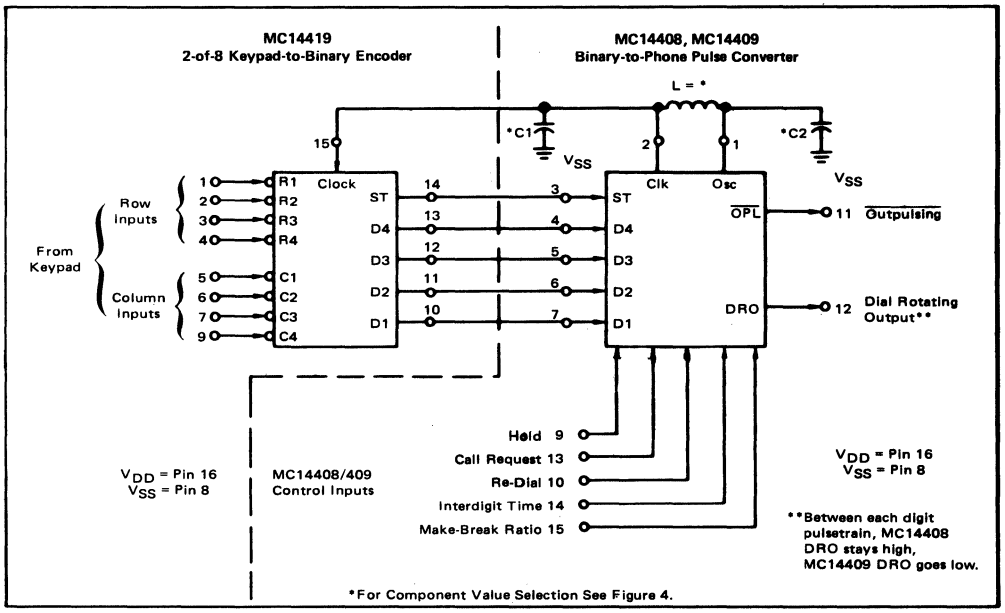


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FIGURE 10 — STANDARD K-500 TELEPHONE

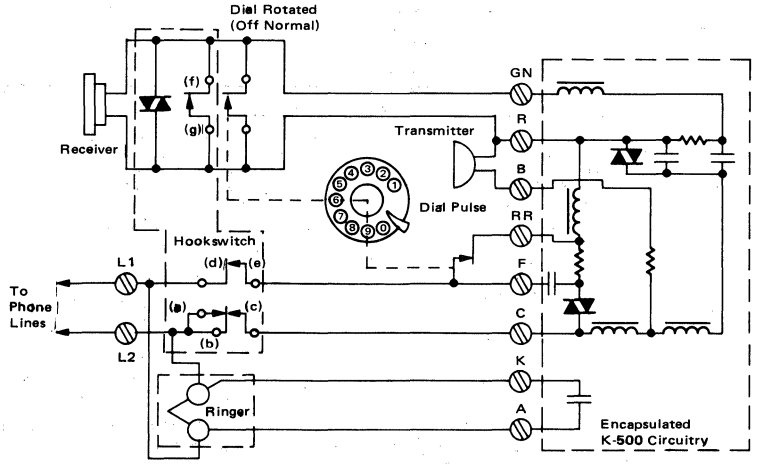
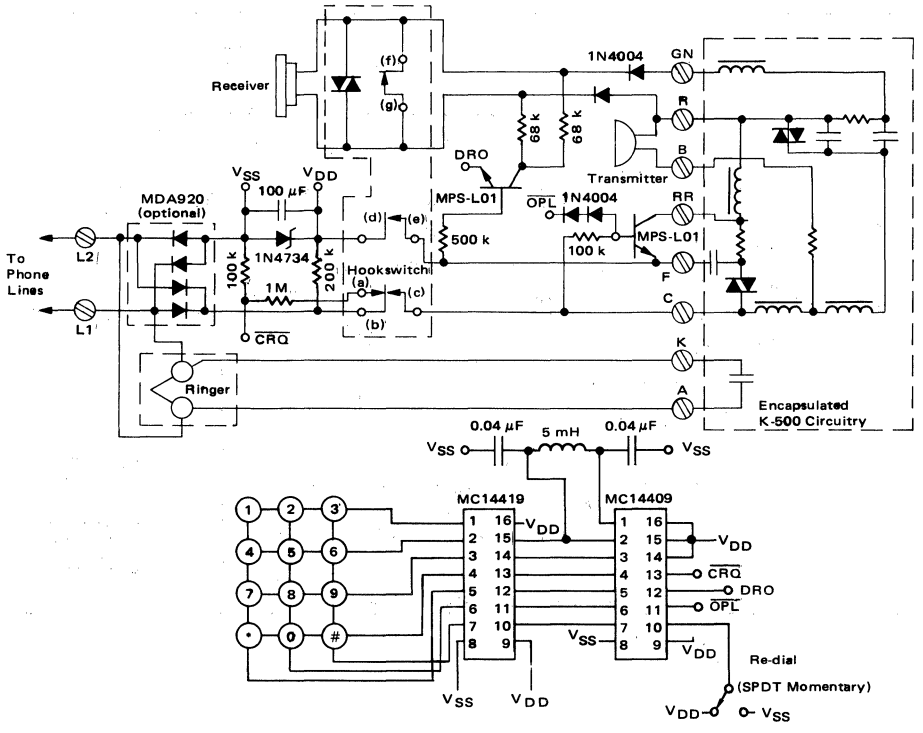


FIGURE 11 — MODIFIED K-500 TELEPHONE



MC14410

CMOS LSI

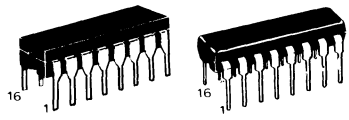
(LOW-POWER COMPLEMENTARY MOS)

2-OF-8 TONE ENCODER

2-OF-8 TONE ENCODER

The MC14410 2-of-8 tone encoder is constructed with complementary MOS enhancement mode devices. It is designed to accept digital inputs in a 2-of-8 code format and to digitally synthesize the high and low band sine waves specified by telephone tone dialing systems. The inputs are normally originated from a 4 x 4 matrix keypad, which generates 4 row and 4 column input signals in a 2-of-8 code format (1 row and 1 column are simultaneously connected to V_{SS}). The master clocking for the MC14410 is achieved from a crystal controlled oscillator which is included on the chip. Internal clocks, which operate the logic, are enabled only by one or more row and column signals being activated simultaneously. The two sine wave outputs have NPN bipolar structures on the same substrate which allows for low output impedance and large source currents. Applications of this device include telephone tone dialing, radio and mobile telephones, process control, point-of-sale terminals, and credit card verification terminals.

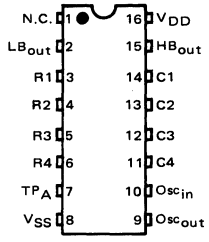
- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Supply Voltage Range = 4.4 Vdc to 6.0 Vdc
- On-Chip Oscillator (Crystal or External Clock Source may be applied to Pin 10)
- On-Chip Pull-Up Resistors on Row and Column Inputs
- Designed with Multiple Key Lockout (Eliminates Need for Mechanical Lockout in Keypad)
- Two Sine Wave Generators On-Chip
- Frequency Accuracy ±0.2%
- Low Harmonic Distortion
- Single Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times



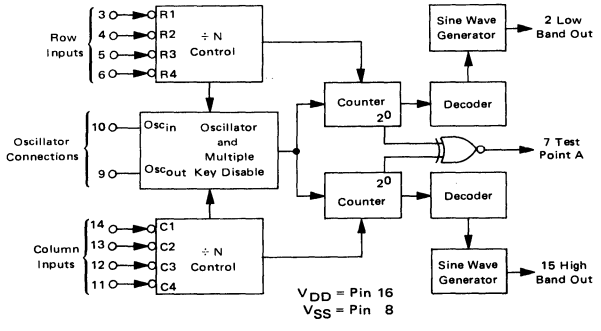
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a peak sinewave voltage.

2

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.0	Vdc
Input Voltage, All Inputs	V_{in}	V_{SS} -0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.4	6.0	4.4	5.0	6.0	4.4	6.0	Vdc
Output Voltage "0" Level Pins 7 and 9	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage (V_O = 4.5 or 0.5 Vdc) "0" Level	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}									mAdc
Pin 7		5.0	-0.05	–	-0.05	-0.4	–	-0.04	–	
Pin 9			-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}									mAdc
Pin 7		5.0	0.05	–	0.05	0.20	–	0.04	–	
Pin 9			0.23	–	0.20	0.78	–	0.16	–	
Input Pull-Up Resistor Source Current (V_{in} = 0 Vdc) Pins 3-6, 11-14	I_{IL}	6.0	–	140	–	30	100	–	80	μAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Current	I_Q									mAdc
		4.4	–	0.48	–	0.2	0.4	–	0.33	
		6.0	–	1.3	–	0.55	1.1	–	0.9	
Total Supply Current (Dynamic plus Quiescent)	I_T									mAdc
(R_L = 15 kΩ, f = 1 MHz)		4.4	–	1.7	–	0.7	1.4	–	1.15	
		6.0	–	3.5	–	1.45	2.9	–	2.4	
Low Band Output Voltage Swing Pin 2 Only (R_L = 100 k)	V_{Lpp}									mVpp
		4.4	400	600	500	600	700	550	750	
		6.0	800	1000	900	1000	1100	950	1150	
High Band Output Voltage Swing Pin 15 Only (R_L = 100 k)	V_{Hpp}									mVpp
		4.4	600	900	700	850	1000	800	1100	
		6.0	1000	1400	1100	1350	1500	1200	1600	
Low Band–High Band Voltage Differential	ΔV	5.0	–	–	–	2.5	–	–	–	dB
Low Band–High Band Pin 2,15 Output Impedance AC only	z_o	–	–	–	–	80	–	–	–	Ω
Low Band–High Band Pin 2,15 2nd thru 14th Harmonics (R_L = 15 kΩ)	V_{2H}-V_{14H}	4.4 to 6.0	–	-20	–	-30	-25	–	-25	dB
Maximum Clock Pulse Frequency	f_{cl}	4.4	–	–	–	1.0	–	1.1	–	MHz
Turn-on Time (Power on to oscillation)	t_{on}	5.0	–	–	–	8.0	–	–	–	ms

TABLE 1 – FUNCTIONAL TRUTH TABLE

ACTIVE LOW INPUTS		OUTPUTS	
Activated Row Lines	Activated Column Lines	Low Band Pin 2	High Band Pin 15
None	X**	dc level	dc level
X**	None	dc level	dc level
One	One	f_L*	f_H*
Two or more	One	dc level	f_H*
One	Two or more	f_L*	dc level
Two or more	Two or more	dc level	dc level

*See Table 2
**X = Don't care

TABLE 2 – OUTPUT FREQUENCY TABLE

Input Line Activated (low)	Frequency Generated**	
	f_L (Hz)	f_H (Hz)
R1	697	–
R2	770	–
R3	852	–
R4	941	–
C1	–	1209
C2	–	1336
C3	–	1477
C4	–	1633

**All frequencies are accurate to ±0.2% (crystal tolerance not included).

FIGURE 1 – TYPICAL SINE WAVE OUTPUT
(Pins 2 or 15, No External Filtering)

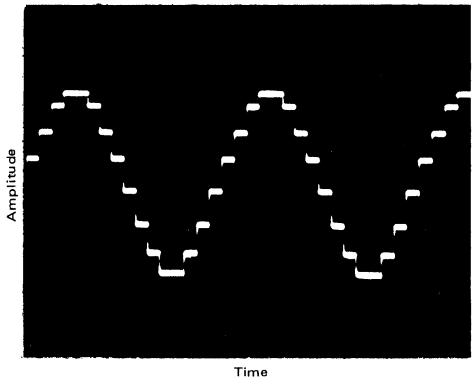


FIGURE 2 – TYPICAL FREQUENCY SPECTRUM
(Pins 2 or 15, No External Filtering)

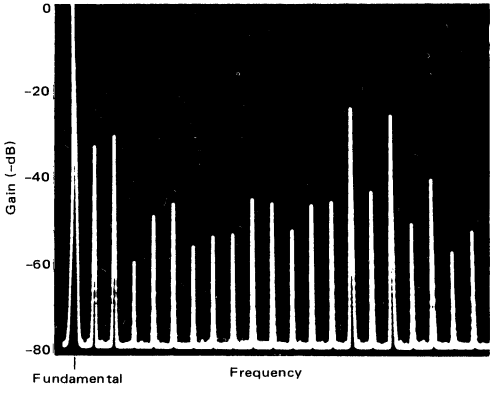


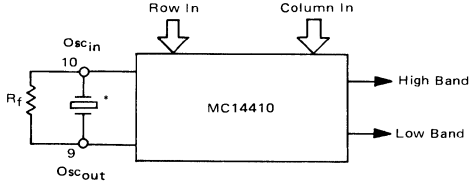
FIGURE 3 – TYPICAL CRYSTAL CIRCUIT

R_f = 15 MΩ ± 10%

CRYSTAL SPECIFICATION

Crystal Mode	Parallel
Frequency	1 MHz ± 0.1%
R_S	540Ω typ
C_0	7.0 pF typ
Temperature Range	-40°C to +85°C
Test Level	1 mW
Test Set	TS–330/TSM or Equivalent

*Recommended Crystals: CTS KNIGHT



2

FIGURE 4 – TYPICAL TELEPHONE INTERFACE APPLICATION

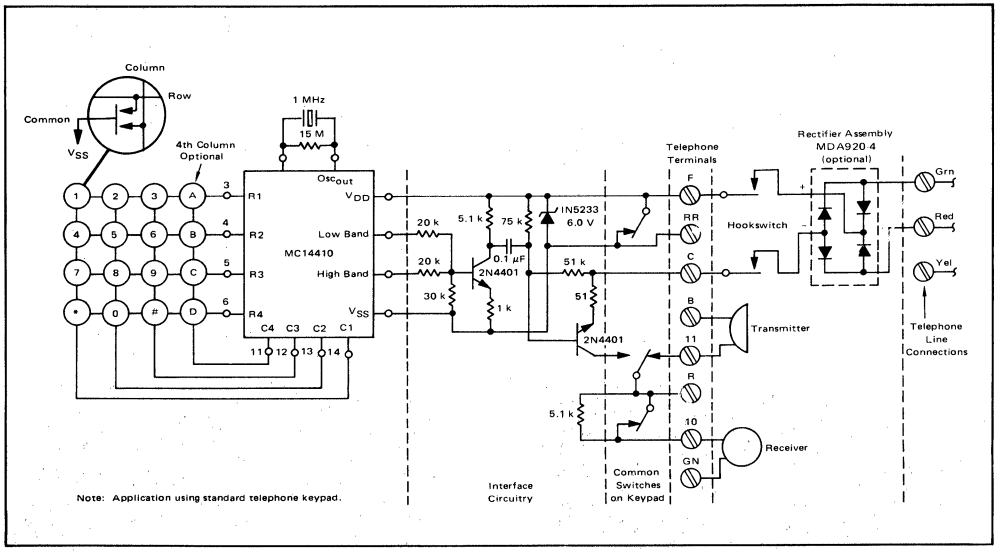


FIGURE 5 – LOW LEVEL OUTPUT TONE GENERATOR APPLICATION

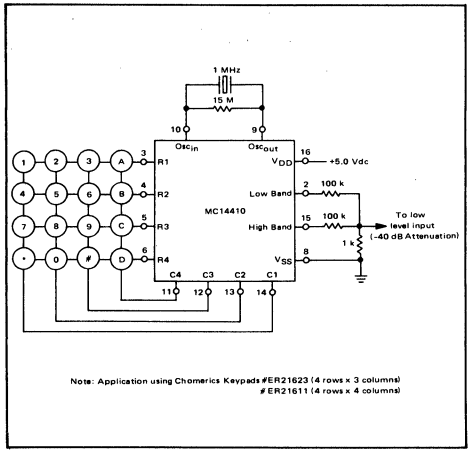
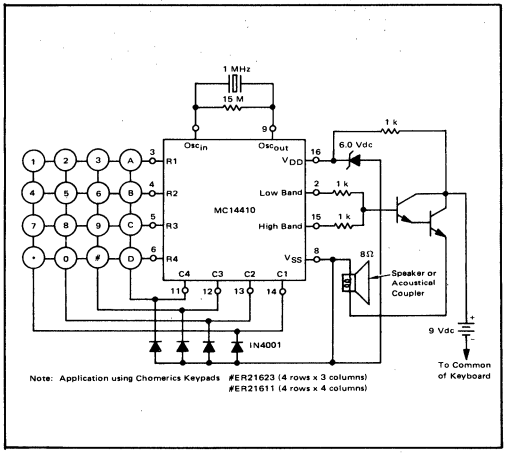


FIGURE 6 – BATTERY POWERED OPERATION (Driving Audio Speaker)



MC14411

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR

2

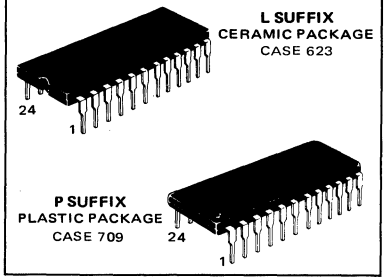
BIT RATE GENERATOR

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

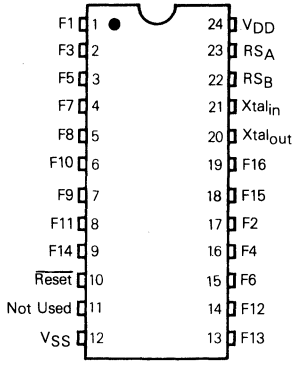
A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- Sixteen Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 21
- Internal Pullup Resistor on Reset Input



PIN ASSIGNMENT

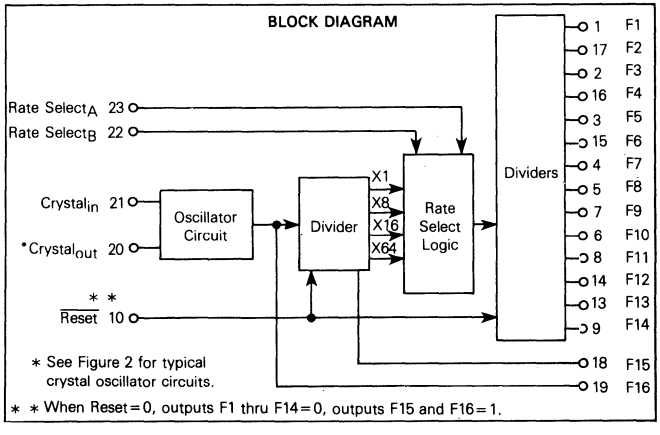


V_{DD} = Pin 24
V_{SS} = Pin 12

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits.

* * When Reset = 0, outputs F1 thru F14 = 0, outputs F15 and F16 = 1.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	V
Input Voltage (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
Output Drive Current (V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mA
Input Current Pins 21, 22, 23	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pin 10		5.0	–	–	−1.5	–	−7.5	–	–	μA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	$P_D = (7.5\ mW/MHz)\ f + P_Q$							mW
Output Rise Time** $t_r = (3.0\ ns/pF)\ C_L + 25\ ns$	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** $t_f = (1.5\ ns/pF)\ C_L + 47\ ns$	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	1.85	–	–	1.85	–	1.85	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L) = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}{}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1 — OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz) X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

*F16 is buffered oscillator output.

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS

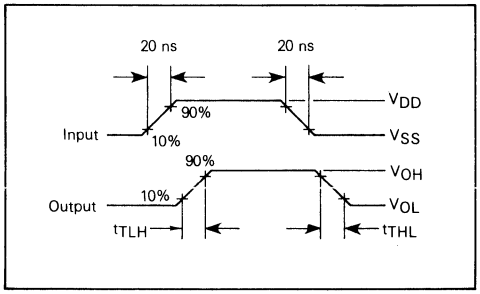
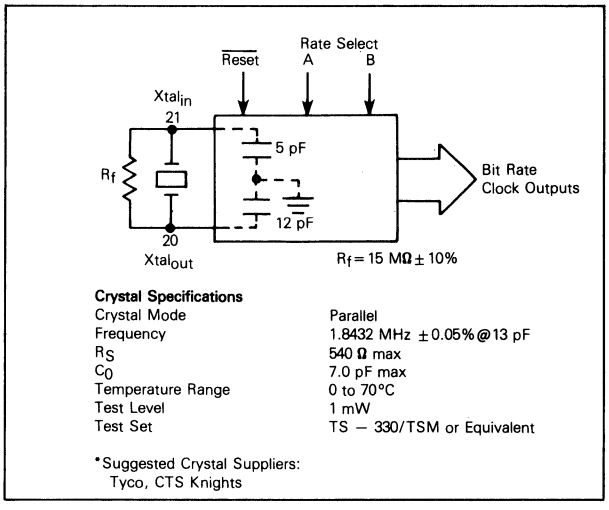


FIGURE 2 — TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

Crystal Mode	Parallel
Frequency	1.8432 MHz ±0.05%@13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS — 330/TSM or Equivalent

*Suggested Crystal Suppliers:
Tyco, CTS Knights

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc., or others.

MC14412

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

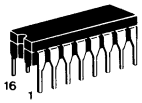
UNIVERSAL LOW SPEED
(0-600 bps)
MODEM

2

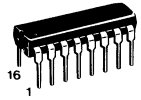
UNIVERSAL LOW SPEED MODEM (0-600 bps)

The MC14412 contains a complete FSK (Frequency-Shift Keying) modulator and demodulator compatible with both foreign (C.C.I.T.T. standards) and U.S.A. low speed (0 to 600 (bps) communication networks.

- On-Chip Crystal Oscillator with External Crystal
- Echo Suppressor Disable Tone Generator
- Originate and Answer Modes
- Simplex, Half-Duplex, and Full-Duplex Operation
- On-Chip Sine Wave Generator
- Modem Self Test Mode
- Single Supply:
  V_{DD} = 4.75 to 15 Vdc MC14412FP, MC14412 FL
  V_{DD} = 4.75 to 6.0 Vdc MC14412VP, MC14412VL
- Selectable Data Rates: 0-300, 0-600 bps
- Post Detection Filter
- TTL or CMOS Compatible Inputs and Outputs



L SUFFIX
CERAMIC PACKAGE
CASE 620



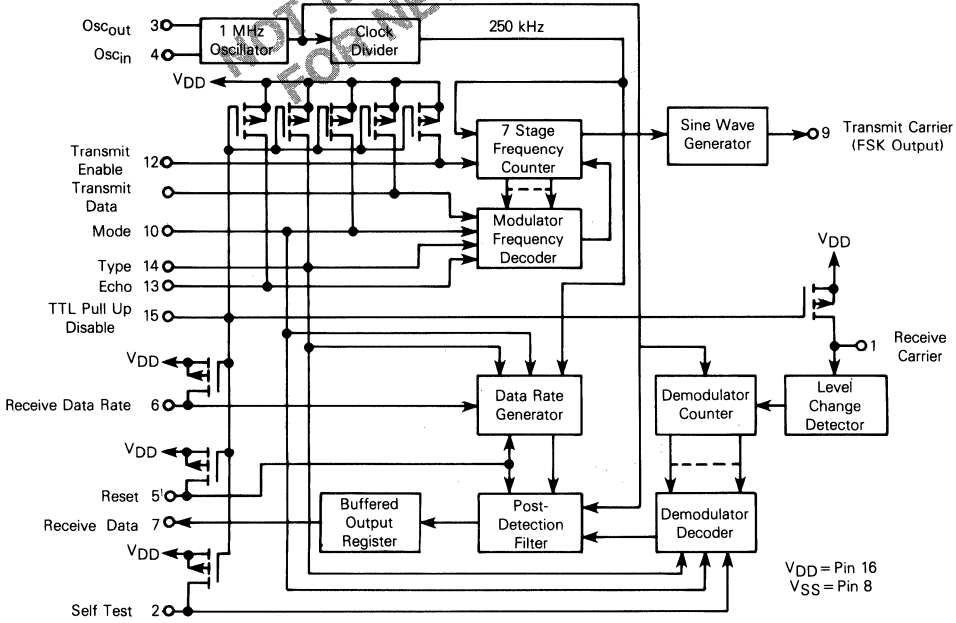
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC144XX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- F 4.75 to 15 Vdc
- V 4.75 to 6.0 Vdc

NOT RECOMMENDED FOR NEW DESIGN

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}** Vdc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage Pin 7 Only "0" Level $V_{in}=V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in}=0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage* "0" Level										
($V_O=4.5$ or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
($V_O=9.0$ or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
($V_O=13.5$ or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level										
Pin 15		5 to 15	$V_{DD}-0.75$	–	$V_{DD}-0.8$	$V_{DD}-2$	–	$V_{DD}-0.85$	–	
($V_O=0.5$ or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
($V_O=1.0$ or 9.0 V)	V_{IH}	10	7.0	–	7.0	5.50	–	7.0	–	V
($V_O=1.5$ or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current Pin 7 Only										
($V_{OH}=2.5$)	I_{OH}	5	−0.62	–	−0.5	−1.5	–	−0.35	–	mA
($V_{OH}=9.5$)		10	−0.62	–	−0.5	−1.0	–	−0.35	–	
($V_{OH}=13.5$)		15	−1.8	–	−1.5	−3.6	–	−1.1	–	
($V_{OL}=0.4$)		4.75	2.3	–	2.0	4.0	–	1.6	–	
($V_{OL}=0.5$)	I_{OL}	10	5.3	–	4.5	10	–	3.6	–	mA
($V_{OL}=1.5$)		15	15	–	13	35	–	10	–	
Input Current (Pin 15 = V_{DD})	I_{in}	–	–	–	–	±0.00001	±0.1	–	–	μA
Input Pull-Up Resistor Source Current (Pin 15 = V_{SS}, $V_{in}=2.4$ Vdc) Pins 1, 2, 5, 6, 10, 11 12, 13, 14	I_P	5	285	–	250	460	–	205	–	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	–	–	–	pF
Total Supply Current (Pin 15 = V_{DD})	I_T	5	–	4.5	–	1.1	4.0	–	3.5	mA
		10	–	13	–	4.0	12	–	11	
		15	–	27	–	8.0	25	–	23	
Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	ACC	5 to 15	–	–	–	0.5	–	–	–	%
Transmit Carrier Output 2nd Harmonic	V_{2H}	5	–	–	−20	−25	–	–	–	dB
		15	–	–	−25	−32	–	–	–	
Transmit Carrier Output Voltage ($R_L=100$ kΩ) (Pin 9)	V_{out}	5	–	–	0.2	0.30	–	–	–	V_{RMS}
		10	–	–	0.5	0.85	–	–	–	
		15	–	–	1.0	1.5	–	–	–	
Maximum Receive Carrier Rise and Fall Times (Pin 1)	t_r, t_f	5	–	15	–	–	15	–	15	μs
		10	–	5.0	–	–	5.0	–	5.0	
		15	–	4.0	–	–	4.0	–	4.0	
Maximum Oscillator Frequency	f_{max}	5	–	–	1.2	5	–	–	–	MHz
Minimum Clock Pulse Width	t_w	5	–	–	–	50	350	–	–	ns

*DC Noise Immunity (V_{IL}, V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the circuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to MC14412VP devices.

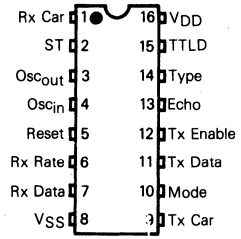
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltages MC14412FP, FL MC14412VP, VL	V_{DD}	−0.5 to 15 −0.5 to 6.0	V
Input Voltages, All Inputs	V_{in}	V_{DD}+0.5 to V_{SS}−0.5	V
DC Current Drain per Pin (except Pin 8, 7)	I	10	mA
DC Current Drain (Pin 8, 7)	I	35	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



DEVICE OPERATION

GENERAL

Figure 1 shows the modem in a system application. The data to be transmitted is presented in serial format to the modulator for conversion to FSK signals for transmission over the telephone network. The modulator output is buffered/amplified before driving the 600 ohm telephone line.

The FSK signal from the remote modem is received via the telephone line and filtered to remove extraneous signals such as the local Transmit Carrier. This filtering can be either a bandpass which passes only the desired band of frequencies or a notch which rejects the known interfering signal. The desired signal is then limited to preserve the axis crossings and fed to the demodulator where the data is recovered from the received FSK carrier.

INPUT/OUTPUT FUNCTIONS

Figure 2 shows the I/O interface for the MC14412 low-speed modem. The following is a description of each individual signal.

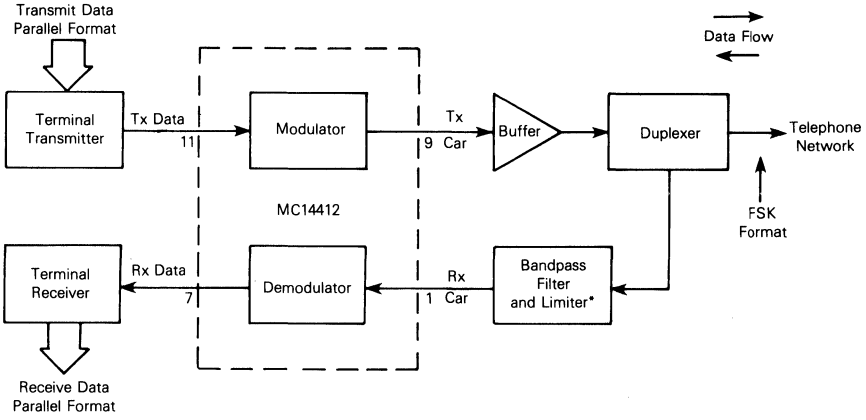
TYPE (Pin 14)

The Type input selects either the U.S. or C.C.I.T.T. operational frequencies for both transmitting and receiving data. When the Type input="1", the U.S. standard is selected and when the Type input="0", the C.C.I.T.T. standard is selected.

TRANSMIT DATA (Tx Data, Pin 11)

Transmit Data is the binary information input. Data entered for transmission is modulated using FSK techniques. When operating in the U.S. standard (Type="1") a logic "1" input level represents a Mark or when operating in the CCITT standard (Type="0") a logic "1" input level represents a Mark.

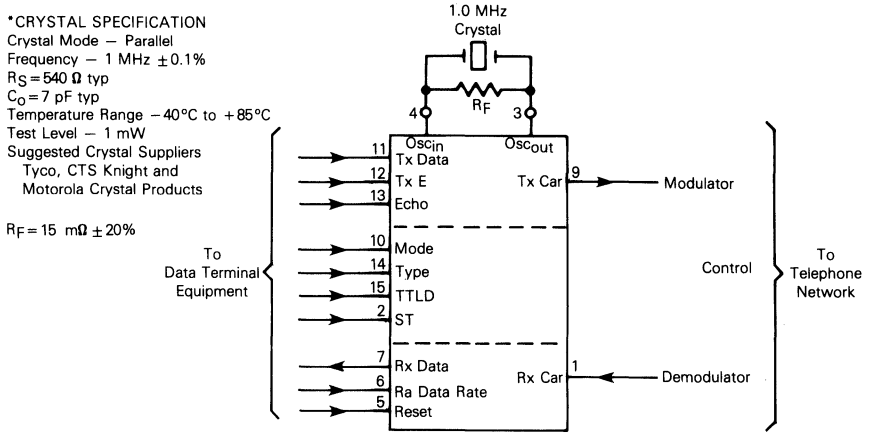
FIGURE 1 — TYPICAL LOW-SPEED MODEM APPLICATION



Since the modulator and demodulator sections of the MC14412 are functionally equivalent to those of the MC6860, additional application information can be obtained from the following Motorola publications:

AN-731 Low-speed Modem Fundamentals
AN-747 Low-speed Modem System Design Using the MC6860
EB-49 Application Performance of the MC6860 MODEM.

FIGURE 2 — MC14412 INPUT/OUTPUT SIGNALS



2

TRANSMIT CARRIER (Tx Car, Pin 9)

The Transmit Carrier is a digital-synthesized sine wave derived from a 1.0 MHz oscillator reference. The Tx CAR has an AC output impedance of 5 kΩ typical. The frequency characteristics are as follows:

United States Standard
Type = "1"
Echo = "0"

Mode		Tx Data		Tx Car
Originate	"1"	Mark	"1"	1270 Hz
Originate	"1"	Space	"0"	1070 Hz
Answer	"0"	Mark	"1"	2225 Hz
Answer	"0"	Space	"0"	2025 Hz

C.C.I.T.T. Standard
Type = "0"
Echo = "0"

Mode		Tx Data		Tx Car
Channel	"1"	Mark	"1"	980 Hz
No. 1	"1"	Space	"0"	1180 Hz
Channel	"0"	Mark	"1"	1650 Hz
No. 2	"0"	Space	"0"	1850 Hz

Echo Suppressor Disable Tone
Type = "0"
Echo = "1"

Mode	Tx Data	Tx Car
Chan. No. 2 "0"	"1"	2100 Hz

TRANSMIT ENABLE (Tx Enable, Pin 12)

The Transmit Carrier output is enabled when the Tx Enable input = "1". No output tone can be transmitted when Tx Enable = "0".

MODE (Pin 10)

The Mode input selects the pair of transmitting and receive frequencies used during modulation and demodulation. When Mode = "1", the U.S. originate mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 1 (Type input = "0"). When mode = "0", the U.S. answer mode is selected (Type input = "1") or the C.C.I.T.T. Channel No. 2 (Type input = "0").

ECHO (Pin 13)

When the Echo input = "1" (Type = "0", Mode = "0", Tx Data = "1") the modulator will transmit a 2100 Hz tone for disabling line echo suppressors. During normal data transmission, this input should be low = "0".

RECEIVE DATA (Rx Data, Pin 7)

The Receive Data output is the digital data resulting from demodulating the Receive Carrier.

RECEIVE CARRIER (Rx Car, Pin 1)

The Receive Carrier is the FSK input to the demodulator. This input must have either a CMOS or TTL compatible logic level input (see TTL pull-up disable) at a duty cycle of 50% ±2%, that is a square wave resulting from a signal limiter.

RECEIVE DATA RATE (Rx Rate, Pin 6)

The demodulator has been optimized for signal to noise performance at 300, and 600 bps.

Data Rate	Rx Rate
0-300 bps	"1"
0-600 bps	"0"

SELF TEST (ST, Pin 2)

When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

RESET (Pin 5)

This input is provided to decrease the test time of the chip. In normal operation, this input may be used to disable the demodulator (Reset = "1") – otherwise it should be tied low = "0". The reset pin does not reset Rx data pin 7.

CRYSTAL (Osc_{in}, Osc_{out}, Pin 4, Pin 3, respectively)

A 1.0 MHz crystal is required to utilize the on chip oscillator. A 1.0 MHz square wave clock can also be applied to the Osc_{in} input to satisfy the clock requirement (see Figure 2).

When utilizing the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be <9 pF at the crystal input (pin 4). Pin 3 is capable of driving only one CMOS input.

TTL PULL-UP DISABLE (TTLD, Pin 15)

To improve TTL interface compatibility, all of the inputs to the MODEM have controllable P-Channel devices which act as pull-up resistors when TTLD input is low ("0"). When the input is taken high ("1") the pull-up is disabled, thus reducing power dissipation when interfacing with CMOS. Pin 15 should be taken high ("1") with V_{DD} greater than 6 volts.

FIGURE 3 — M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

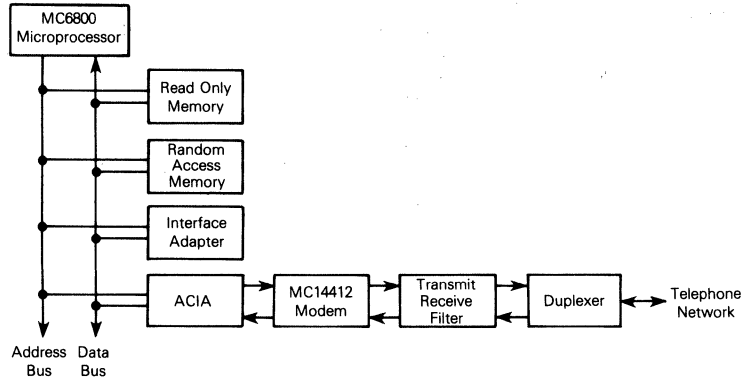


FIGURE 4 — TRANSMIT CARRIER SINEWAVE

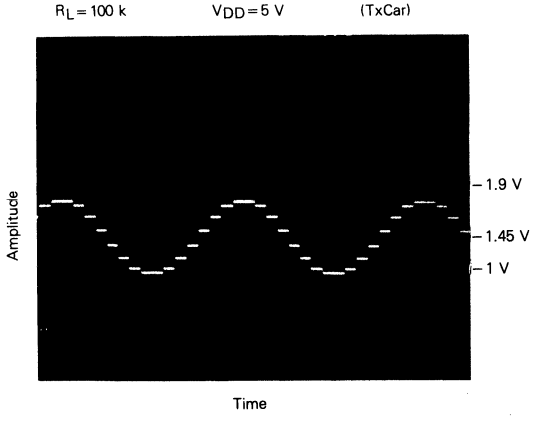
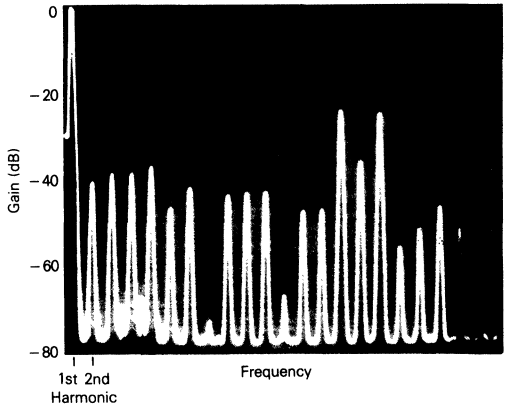


FIGURE 5 — TYPICAL TRANSMIT CARRIER FREQUENCY SPECTRUM



MC14413-1
MC14413-2
MC14414-1
MC14414-2

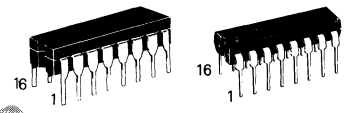
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)
PULSE CODE MODULATION
SAMPLED DATA FILTERS

PULSE CODE MODULATION SAMPLED DATA FILTERS

The MC14413-1, -2 and MC14414-1, -2 are sampled data, switched capacitor filter ICs intended to provide the band limiting and signal restoration filtering necessary in PCM Codec voice digitization systems. Both ICs are capable of operating from either a single or split power supply and can be powered-down when not in use. Included on both chips are two totally uncommitted op amps for use elsewhere in the systems as I to V converters, gain adjust buffers, etc.

- Transmit Band-pass and Receive Low-pass (MC14413-1, -2)
- Transmit and Receive Low-pass (MC14414-1, -2)
- D3/D4 Specifications (MC14414-2/13-2)
- CCITT Specification (MC14414-1/13-1)
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- Single Supply Capability when Used with MC14404/6/7 Codecs
- ±5 to ±8 Volt Power Supply Ranges
- Receive Filter Compatible with 15% to 100% Duty Cycle PAM Inputs with Sinx/x Correction
- No Precision Components Required (MC14413-1, -2)
- TTL Compatible Inputs Using V_{LS} Pin
- Two Operational Amplifiers Available to Reduce System Component Count

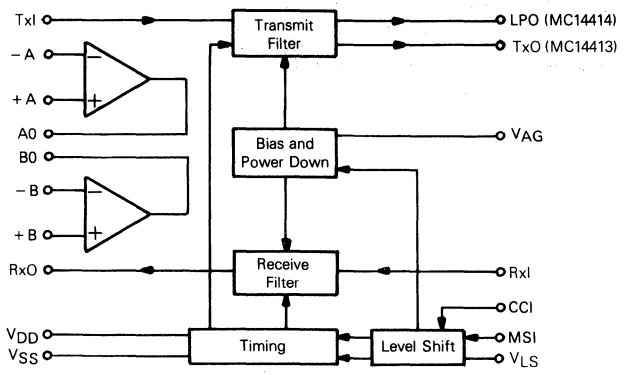


L SUFFIX
CERAMIC PACKAGE
CASE 620

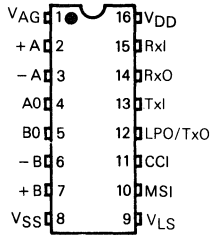
P SUFFIX
PLASTIC PACKAGE
CASE 648

NOT RECOMMENDED FOR NEW DESIGN

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Convert Clock Frequency	CCI	50	128	400	kHz
Master Sync Frequency	MSI	–	8	32	kHz

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD}	0°C		25°C			85°C		Unit
			Vdc	Min	Max	Min	Typ	Max	Min	Max	
Operating Current		I_{DD}	12	–	5.0	–	2.0	4.3	–	5.0	mA
Power-Down Current (PDI = V_{SS})		I_{PD}	12	–	50	–	10	40	–	50	μA
Input Capacitance		C_{in}	12	–	–	–	5.0	7.5	–	–	pF
MODE CONTROL LOGIC LEVELS											
V_{LS} Power-Down Mode		V_{IH}	12 15	11.5 14.5	– –	11 14	11 13	– –	11.5 14.5	– –	V
V_{LS} TTL Mode		–	12 15	2 2	9.0 11.0	2.0 2.0	– –	9 12.0	2 2	9.0 11.0	V
V_{LS} CMOS Mode		V_{IL}	12 15	– –	0.8 0.8	– –	– –	0.8 0.8	– –	0.8 0.8	V
V_{AG} Power-Down Mode		V_{IH}	12 15	11.5 14.5	– –	11.5 14.5	10.5 13.5	– –	11.5 14.5	– –	V
V_{AG} Analog-Ground Mode		V_{IL}	12 15	– –	9.0 12.0	– –	– –	9.0 12.0	– –	9.0 12.0	V
CMOS LOGIC LEVELS ($V_{LS} = V_{SS}$)											
Input Current CCI		I_{in}	12	–	±1.0	–	±0.00001	±0.3	–	±1.0	μA
Input Current MSI (Internal Pulldown Resistors)	"1" Level "0" Level	I_{in}	12 12	– –	200 −1.0	– –	50 −0.00001	100 −0.3	– –	200 −1.0	μA
Input Voltage CCI, MSI	"0" Level	V_{IL}	12 15	– –	– –	– –	5.25 6.75	3.60 4.0	– –	– –	V
	"1" Level	V_{IH}	12 15	– –	– –	9.0 11.5	6.75 8.25	– –	– –	– –	V
TTL LOGIC LEVELS (V_{LS} = 6 V, V_{SS} = 0 V)											
Input Current CCI		I_{in}	12	–	±1.0	–	±0.00001	±0.3	–	±1.0	μA
Input Current MSI (Internal Pulldown Resistor)	"1" Level "0" Level	I_{in}	12 12	– –	200 −1.0	– –	30 −0.00001	– −0.3	– –	200 −1.0	μA
Input Voltage CCI, MSI	"0" Level "1" Level	V_{IL} V_{IH}	12 12	– –	– –	– V_{LS}+2.0	– –	V_{LS}+0.8 –	– –	– –	V

2

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	0°C		25°C			85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Input Current	V_{AG}	I_{in}	–	±30	–	–	±10	–	±30	μA
Input Current	RxI, TxI	I_{in}	–	–	–	±0.00001	±1.0	–	±1.0	μA
AC Input Impedance (1 kHz)	RxI, TxI	Z_{in}	1.0	–	1.0	2.0	–	1.0	–	MΩ
Input Common Mode Voltage Range	TxI, RxI	V_{ICR}	–	–	1.5	–	10.5	–	–	V
Output Voltage Range	TxO, LPO, RxO	V_{OR}								V
(R_L = 20 kΩ to V_{AG})			1.5	10.5	1.5	–	10.5	1.5	10.5	
(R_L = 600 Ω to V_{AG})			2.0	9.3	2.0	–	9.3	2.0	9.3	
(R_L = 900 Ω to V_{AG})			1.5	10.5	1.5	–	10.5	1.5	10.5	
Small Signal Output Impedance (1 kHz)	TxO (MC14413)	Z_o	–	–	–	50	–	–	–	Ω
	LPO (MC14414)		–	–	–	50	–	–	–	
	RxO		–	–	–	50	–	–	–	
Output Current										mA
(V_O = 11 V)	TxO, LPO, RxO	I_{OH}	−5	–	−5	−6.0	–	−5	–	
(V_O = 1 V)	TxO, LPO, RxO	I_{OL}	5	–	5	7	–	5	–	

OP AMP PERFORMANCE ($V_{DD} - V_{SS}$ = 12 V)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Input Offset Voltage		–	±80	–	–	±70	–	±80	mV
Open Loop Gain	Z_L = 600 Ω + 200 pF to V_{AG}	–	–	–	45	–	–	–	dB
Input Bias Current		–	–	–	±0.1	–	–	–	μA
Output Voltage Range									V
(R_L = 20 kΩ to V_{AG})		–	–	1.5	–	10.5	–	–	
(R_L = 600 Ω to V_{AG})		–	–	2.0	–	9.3	–	–	
(R_L = 900 Ω to V_{AG})		–	–	1.5	–	10.5	–	–	
Output Current	V_{OH} 10.5	–	5.1	–	7.0	–	–	5.1	mA
	V_{OL} 0.5	–	−5.1	–	−7.0	–	–	−5.1	
Output Noise		–	0	–	−3	–	–	0	dBrnc0
Slew Rate		–	–	–	2	–	–	–	V/μs

RECEIVE FILTER SPECIFICATIONS

($V_{DD} - V_{SS}$ = 12 V, CCI = 128 kHz, MSI = 8 kHz, includes sinx/x correction, V_{in} = −10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Gain (1020 Hz)		−0.3	0.30	–	±0.2	–	−0.30	0.30	dB
Pass-band Ripple (50 Hz to 3000 Hz)	Relative to 1.02 kHz@0 dBm0	−0.15	+0.15	–	±0.08	–	−0.15	+0.15	dB
Out of Band Rejection Relative to 1.02 kHz@0 dBm0	MC14414/13-1	–	−0.9	–	−0.5	−0.9	–	−0.9	dB
3400 Hz	MC14414/13-2	–	−1.5	–	−0.8	−1.5	–	−1.5	
4000 Hz-4600 Hz		−14	–	−14.2	−15.5	–	−14	–	
4600 Hz-64 kHz		−28	–	−30	−33	–	−28	–	
Output Noise (RXI = V_{AG})	ref to 900 Ω	–	–	–	8	12	–	–	dBrnc0
Dynamic Range		–	–	81	83	–	–	–	dB
Absolute Delay Difference									μs
1150 to 2300 kHz Delay		–	22	–	12	22	–	22	
1000 to 2500 kHz Delay		–	35	–	25	35	–	35	
800 to 2700 kHz Delay		–	41	–	31	41	–	41	
Crosstalk 0 dBm@3 kHz		–	–	–	76	–	–	–	dB
Power Supply Rejection Ratio V_{DD} = 12 V + 0.1 Vrms@1 kHz		–	–	–	40	–	–	–	dB

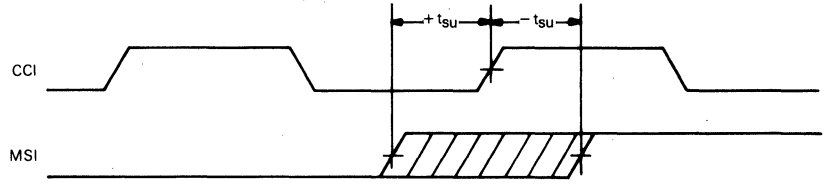
TRANSMIT FILTER SPECIFICATIONS ($V_{DD} - V_{SS} = 12$ V, CC = 128 kHz, MSI = 8 kHz, $V_{in} = -10$ dBm0, full scale = +3 dBm0, 7 Vp-p)

Characteristic		0°C		25°C			85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Gain (1020 Hz)	MC14413-1, -2	−0.3	+0.3	–	±0.2	–	−0.3	+0.3	dB
	MC14414-1, -2	−0.25	0.25	–	±0.15	–	−0.25	0.25	
Pass-band Ripple (300 Hz to 3000 Hz)	Relative to 1.02 kHz@0 dBm0	−0.15	0.15	–	±0.08	–	−0.15	0.15	dB
Rejection									dB
50 Hz (Relative to 1.02 kHz)	MC14413-1, -2 Only	−24	–	−26	−28	–	−24	–	
60 Hz	MC14413-1, -2 Only	−22	–	−22.7	−25	–	−22	–	
180 Hz			−0.8	–	−0.3	–	–	−0.8	
3400 Hz	MC14414-1/13-1	–	−0.8	–	−0.5	−0.8	–	−0.8	
	MC14414-2/13-2	–	−1.5	–	−0.6	−1.5	–	−1.5	
4000 Hz-4600 Hz		−14	–	−14	−15.5	–	−14	–	
4600 Hz-64 kHz		−32	–	−32	−33	–	−32	–	
Output Noise (300 Hz-3400 Hz)	MC14413-1, -2	–	15	–	10	15	–	15	dBrnc0
	MC14414-1, -2	–	12	–	7	10	–	12	
Dynamic Range (7 V p-p Max)	MC14413-1, -2	–	–	78	84	–	–	–	dB
	MC14414-1, -2	–	–	81	87	–	–	–	
Absolute Delay Difference									μs
1150 to 2300 kHz Delay		–	22	–	12	22	–	22	
1000 to 2500 kHz Delay		–	35	–	25	35	–	35	
800 to 2700 kHz Delay		–	41	–	31	41	–	41	
Crosstalk	0 dBm@3 kHz RXO, TXO	–	–	–	76	–	–	–	dB
Power Supply Rejection Ratio	V_{DD} = 12 V + 0.1 V_{RMS}@1 kHz	–	–	–	40	–	–	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ V)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	CCI, MSI	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width	CCI, MXI	t_{WH}	200	–	–	ns
Clock Pulse Frequency	CCI	f_{CL}	50	–	500	kHz
CCI Duty Cycle		–	40	–	60	%
Setup Time MSI Rising Edge to CCI Rising Edge (CCI = 128 kHz)*		t_{su}	−3.0	–	+3.0	μs

*Specifications assume use of 50% duty cycle for clocks.



2

FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)

This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outpus are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A

Noninverting input of op-amp A.

Pin 3 — −A

Inverting input of op-amp A.

Pin 4 — A0

Output of uncommitted op-amp A.

Pin 5 — B0

Output of uncommitted op-amp B.

Pin 6 — −B

Inverting input of op-amp B.

Pin 7 — +B

Non-inverting input of op-amp B.

Pin 8 — V_{SS}

This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)

The voltage on this pin determines the logic compatibility for the CCI and MSI inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If V_{LS} is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at CCI and MSI will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 — MSI (Master Sync Input)

This pin should receive a low-to-high transition concurrent with each new PAM sample received at the receive filter input, ADI. A new transmit filter output sample will be presented 8 CCI clocks after this.

Pin 11 — CCI (Convert Clock Input)

Normally, a 128 kHz clock signal should be applied to this pin to operate both filters at fo = 3100 Hz. For other break frequencies use the following equation: fo = 0.02422 f clock.

Pin 12 — TxO (Transmit Band-pass Output — MC14413-1, -2)

This is the output of the transmit band-pass filter. It is 100% duty cycle PAM at 8 kHz.

Pin 12 — LPO (Transmit Low-pass Output — MC14414-1, -2)

This is the output of the transmit low-pass filter. It is 100% duty cycle PAM at CCI frequency, normally 128 kHz.

Pin 13 — TxI (Transmit Input)

This is the transmit-filter input.

Pin 14 — RxO (Receive Output)

This pin is the output of the receive filter. It is 100% duty cycle PAM at the same frequency as the CCI pin, normally 128 kHz.

Pin 15 — RxI (Receive Input)

This is the receive filter input. It will accept 15% to 100% duty cycle PAM at 8 kHz.

Pin 16 — V_{DD}

Nominally 12 volts.

NOTE: Both V_{AG} and V_{LS} are high-impedance inputs.

PCM FILTER DESCRIPTION

Transmit Filter Description

The transmit filter in both the MC14413-1, -2 and MC14414-1, -2 consists of a 5-pole elliptic low-pass section operating at a sampling rate of 128 kHz. This filter provides the band limiting necessary to prevent aliasing of the input signal in the codec. Since the transmit filter itself samples at a 128 kHz rate, its input (TxI) signal should be band limited to 124 kHz. If energy above 124 kHz could be present, a single-pole RC pre-filter should precede the transmit filter.

In addition to the low-pass section, the transmit filter of the MC14413-1, -2 incorporates a 3 pole Chebychev high-pass filter to provide 50/60 Hz and 15 Hz rejection. Although the MC14414-1, -2 does not include this filter, it can be externally realized using one of the on-board uncommitted op amps as an active filter. This is shown in Figures 10 and 11.

Both the MC14413-1, -2 and MC14414-1, -2 can be used in cascade to produce a sharper rolloff. This is especially useful in testing the MC14413-1, -2 since the 8 kHz PAM from the Tx filter will be sampled and sinx/x corrected by applying the Tx output to the RxI input and observing RxO.

Receive Filter Description

The receive filter sections of the MC14413-1, -2 and MC14414-1, -2 are identical and are 5-pole elliptic low-pass filters operating at a sampling rate of 128 kHz. These filters are used to smooth the PAM output of the PCM Codec. They are similar to the transmit low-pass sections with the exception that they include a 1/8 duty cycle 8 kHz pre-sampler on their inputs (RxI).

This circuitry resamples the codec's PAM output and thereby effecively eliminates the sinx/x distortion normally associated with 15% to 100% 8 kHz PAM pulse trains and eliminates the need to predistort the receive filter's pass-band characteristic.

In normal use as a codec's receive filter, MSI will be an 8 kHz signal. With the MC14407 codec family, the filter MSI is the same as the codec MSI. With other codecs, the MSI signal is receive sync.

The MC14414 may also be used in analog applications by disabling the sinx/x correction. If MSI and CCI are tied together, the receive filter has the same frequency response as the transmit filter and a gain of 18 dB.

Timing And Synchronization

Timing and synchronization of the MC14413-1, -2 and MC14414-1, -2 are provided by the CCI and MSI inputs. A 128 kHz signal should be applied to CCI. An 8 kHz signal, whose low-to-high transition coincides with a new output sample from the PCM codec, should be applied to MSI. The rising edges of theCCI and MSI signals should be skewed no more than 3.0 μs for proper operation.

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, V_{LS}.

Power Down

Both the MC14413-1, -2 and MC14414-1, -2 may be powered down in either of two ways: by bringing V_{AG} to within 0.5 V of V_{DD} or by bringing V_{LS} to within 0.5 V of V_{DD}.

If used on a single supply with the MC14406/7 PCM Codec, the filter IC will power down automatically when the codec does, since the codec raises its V_{AG} pin to V_{DD} in power down. When used in a split supply configuration, the circuit shown in Figure 7 may be utilized.

FIGURE 1 — RECEIVE FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14413-1, -2/MC14414-1, -2, SINX/X CORRECTION INCLUDED)

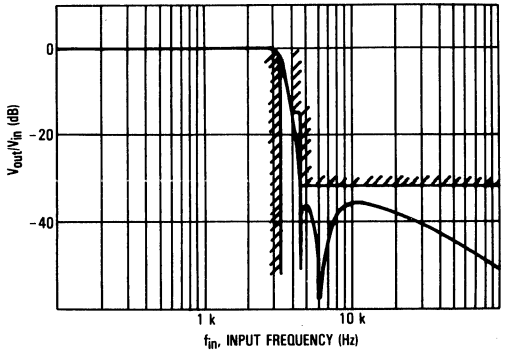


FIGURE 2 — RECEIVE FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14413-1, -2/MC14414-1, -2)

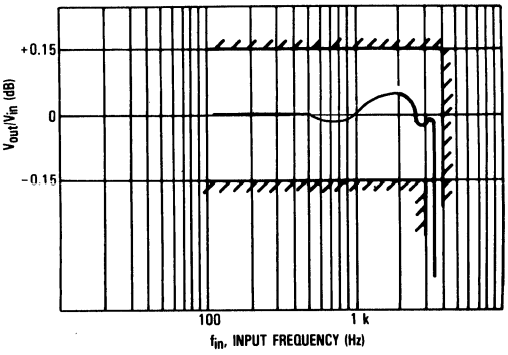


FIGURE 3 — TRANSMIT FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14413-1, -2 AND MC14414-1, -2 USING FIGURES 10 AND 11)

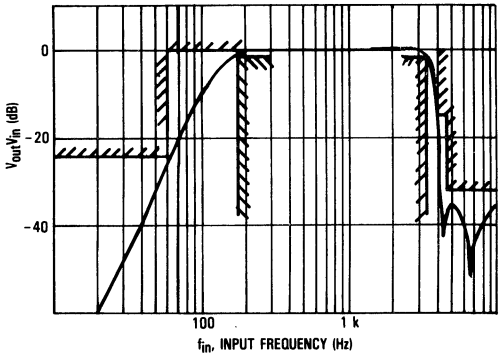


FIGURE 4 — TRANSMIT FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14413-1, -2 AND MC14414-1, -2 USING FIGURES 10 AND 11)

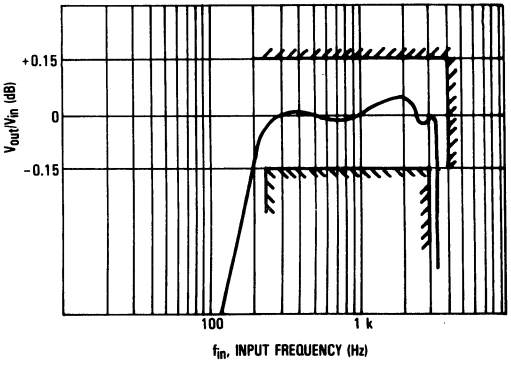


FIGURE 5 — TRANSMIT FILTER TYPICAL AND GUARANTEED PASS-BAND PERFORMANCE (MC14414-1, -2)

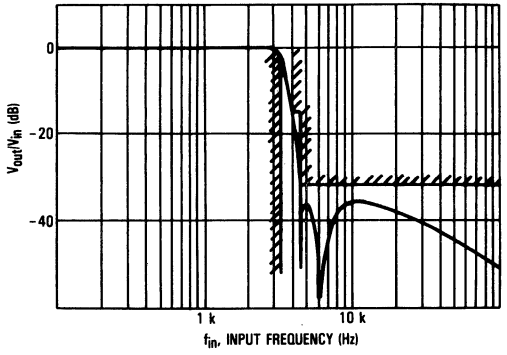


FIGURE 6 — TRANSMIT FILTER TYPICAL AND GUARANTEED PERFORMANCE (MC14414-1, -2)

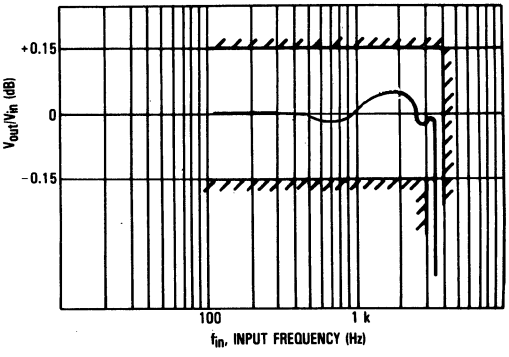


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FIGURE 7 — TYPICAL CIRCUIT CONFIGURATION
USING THE MC14407 CODEC AND MC14413-1, -2 FILTER
(SPLIT SUPPLY)

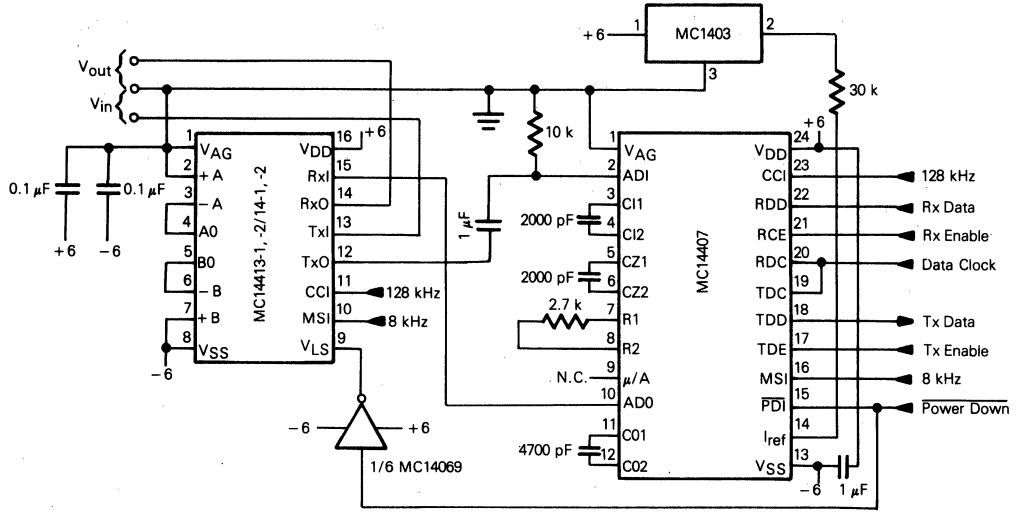
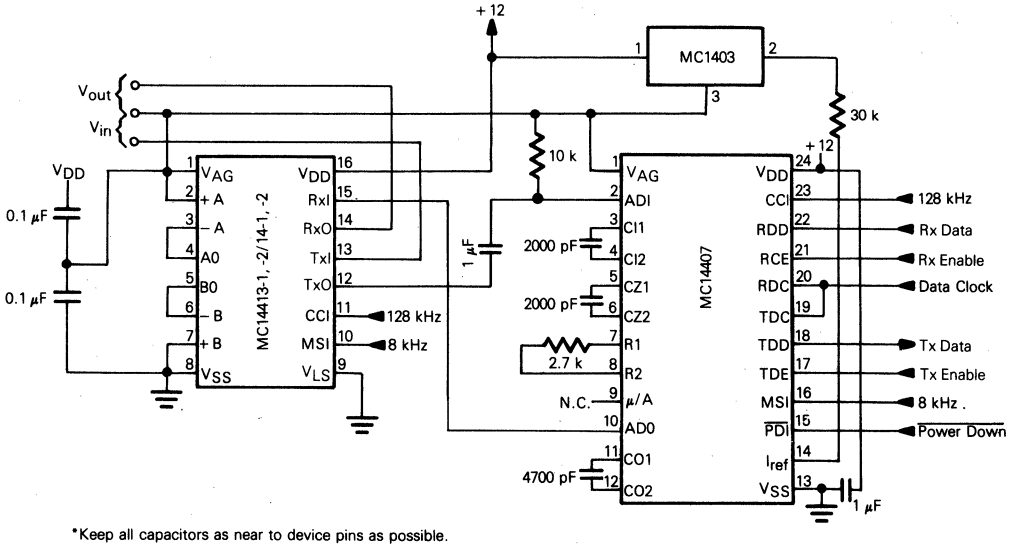
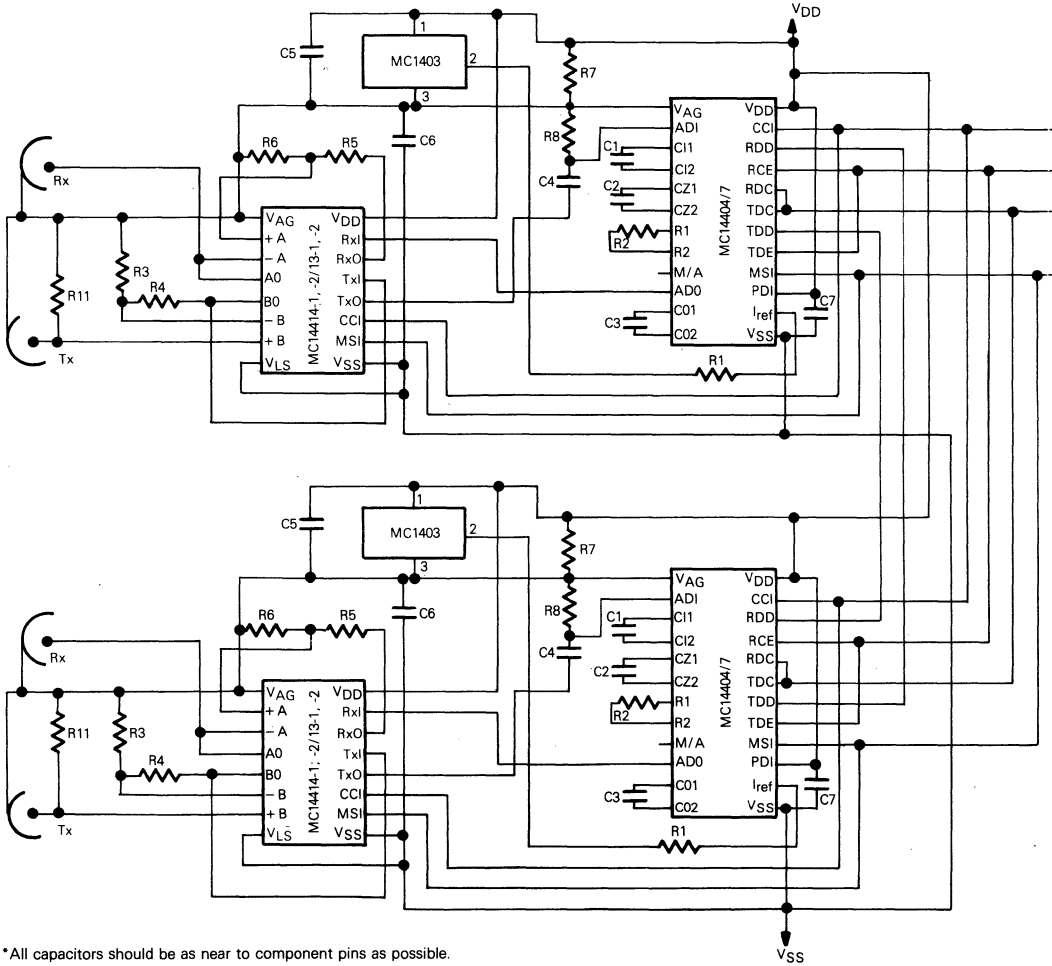


FIGURE 8 — TYPICAL CIRCUIT CONFIGURATION
USING THE MC14407 CODEC AND MC14413-1, -2 FILTER
(SINGLE SUPPLY)



*Keep all capacitors as near to device pins as possible.

FIGURE 9 — MOTOROLA CODEC FILTER EVALUATION BOARD



C1, C2*	2000 pF	20%
C3*	4700 pF	20%
C5, C6*	0.1 μF	20%
C7, C4*	1 μF	20%
R1	30 k	1%
R2	2.7 k	1%
R3	237 k	1%
R4	169 k	1%
R5	20 k	1%
R6	33 k	1%
R7	4.7 k	10%
R8,	10 k	10%
R11	900	1%

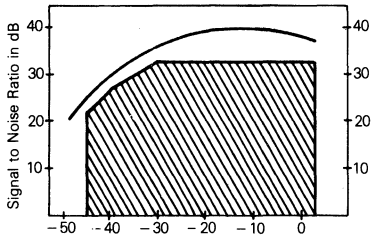
*All capacitors should be as near to component pins as possible.
*In noisy environments, R3-R6 should be 10 kΩ or less to minimize pickup.

2

TYPICAL END-TO-END CHANNEL PERFORMANCE FOR MOTOROLA
MC14413-1, -2/14-1, -2-MC14404/7 CODEC AND FILTER

MC14407/13-2
SPECIFICATION BELL PUB 43801

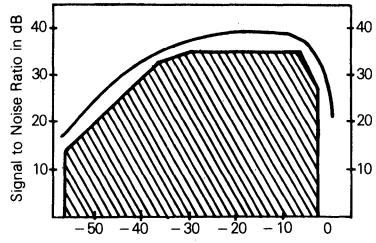
QUANTIZING DISTORTION
SINUSOIDAL INPUT
C MESSAGE WEIGHTED



Input Level (dBm) Referenced to 0 dBm0 @ 1.02 kHz

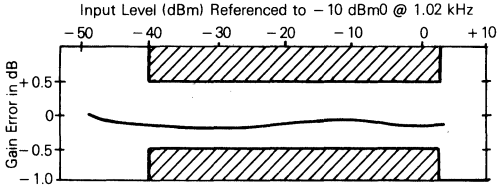
MC14404/13-1
SPECIFICATION CCITT G7.12

QUANTIZING DISTORTION
PSEUDO RANDOM NOISE
3 kHz FLAT WEIGHTING

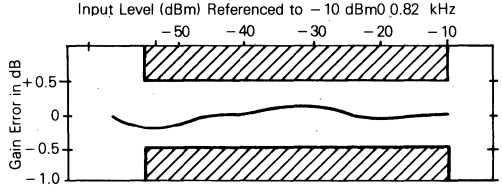


Input Level (dBm) Referenced to 0 dBm0 @ 0.82 kHz

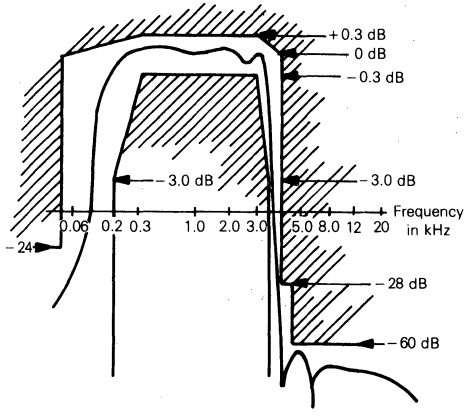
SINUSOIDAL GAIN TRACKING



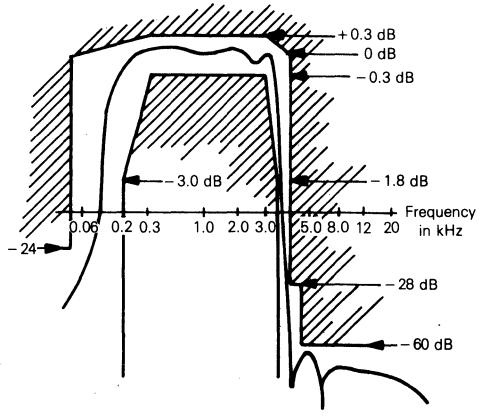
PSEUDO-RANDOM NOISE GAIN TRACKING



GAIN vs FREQUENCY, SINUSOIDAL



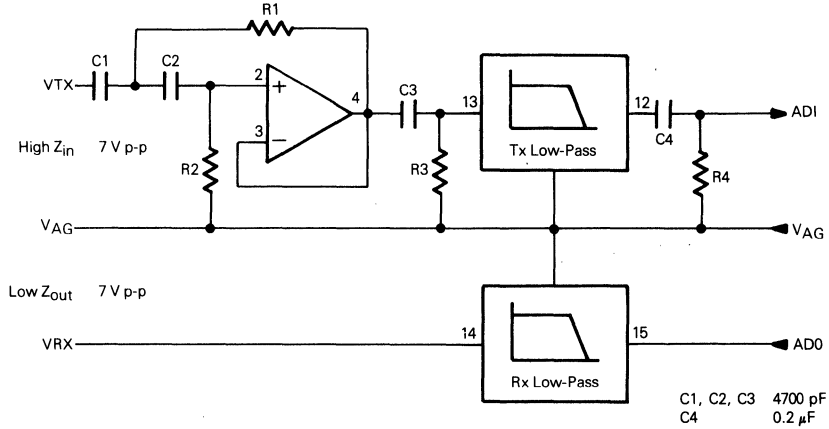
GAIN vs FREQUENCY, SINUSOIDAL



TYPICAL END-TO-END PERFORMANCE OF MOTOROLA CODEC AND FILTER
(All measurements made using HP3779B PCM Test Set)

Specification	Typical Performance of MC14407/4 Codec and MC14413 Filter	Bell System D4 Voice Frequency Requirements PUB 43801	CCITT G7.12 Voice Frequency Requirements
Channel Saturation	+3 dBm0	+3 dBm0	+3 dBm0
Gain Tracking with 1 kHz Tone			
+3 to −40 dBm0	±0.2 dB	≤ ±0.5 dB	≤ ±0.5 dB
−40 to −50 dBm0	±0.3 dB	≤ ±1.0 dB	≤ ±1.0 dB
−55 dBm0	±0.5 dB	≤ ±3.0 dB	≤ ±3.0 dB
Quantizing Distortion @ 1 kHz			
+3 to −30 dBm0	37 dB	≥33 dB	>33 dB
−35 dBm0	34 dB	≥30 dB	≥30 dB
−40 dBm0	31 dB	≥27 dB	≥27 dB
−45 dBm0	25 dB	≥22 dB	≥22 dB
Idle Channel Noise with VTX = V_{AG}	16 dBrnc0	≤23 dBrnc0	≤ −65 dBm0P
Quiet Code Noise (all 1's at decoder (RDD) input)	10 dBrnc0	≤15 dBrnc0	≤ −75 dBm0P
Selective Response @ Multiplex of 8 kHz	−60 dBm0	See Frequency Response	≤ −50 dBm0
Frequency Response @ 0 dBm0 Input			
50 Hz Gain Relative to 1.02 kHz	−28 dB	−	≤ −24 dB
60 Hz Gain or 0.820 kHz	−24 dB	≤ −20 dB	−
200 to 300 Hz Ripple	±0.20 dB	≤ ±0.3 dB	≤ ±0.5 dB
3400 Hz Gain	−1.0 dB	≥ −3.0 dB	≥ −1.8 dB
4000 Hz Gain	−32 dB	≤ −28 dB	≤ −28 dB
≥4600 Hz Gain	< −62 dB	≤ −60 dB	≤ −60 dB
Single Frequency Spurious Response			
In Band with Input 1 kHz @ 0 dBm	≤ −44 dB	≤ −40 dB	≤ −40 dB
Out of Band with Input 0 to 12 kHz @ 0 dBm	≤ −32.5 dB	≤ −28 dB	≤ −25 dB
Differential Delay Distortion			
1150 to 2300	58 μs	≤60 μs	
1000 to 2500	72 μs	≤100 μs	
900 to 2700	91 μs	≤200 μs	

FIGURE 10 — FILTER SCHEMATIC FOR MC14414-1, -2 WITH 60 Hz REJECT FILTER



C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% + 80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

*In noisy environments, R1-R4 should be 10 kΩ or less to minimize pickup.

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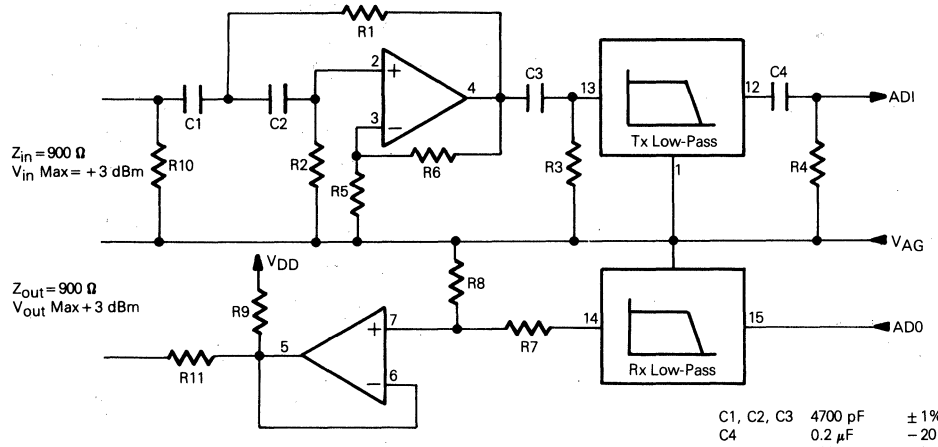
FIGURE 11 — FILTER SCHEMATIC FOR MC14414-1, -2 WITH 60 Hz REJECTION AND 900 TERMINATION



C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% +80%
R1	236 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%
R5	200 kΩ ¼ W	1%
R6	169 kΩ ¼ W	1%
R7	24 kΩ ¼ W	1%
R8	33 kΩ ¼ W	1%
R9	1.8 kΩ ¼ W	10%
R10	900 Ω ¼ W	1%
R11	900 Ω ¼ W	1%

*In noisy environments, R1-R8 should be 10 kΩ or less.

FIGURE 12 — TYPICAL 2-WIRE PORT INTERFACE USING MC14413

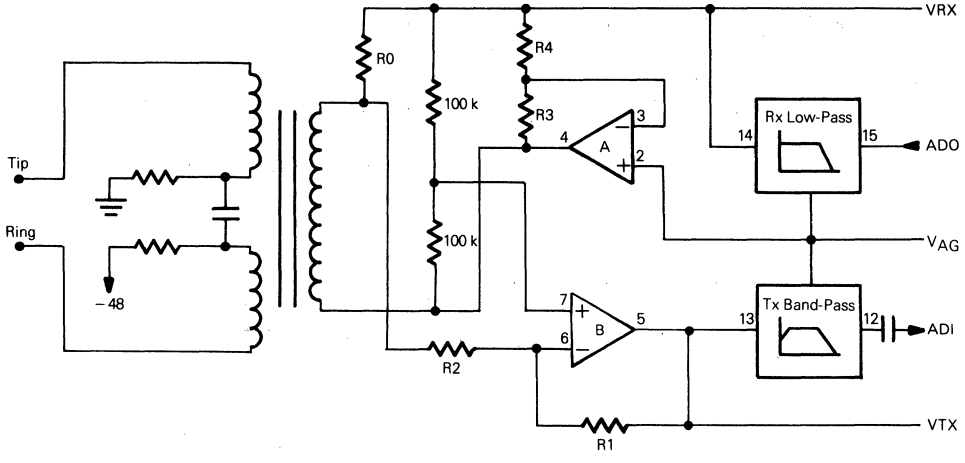
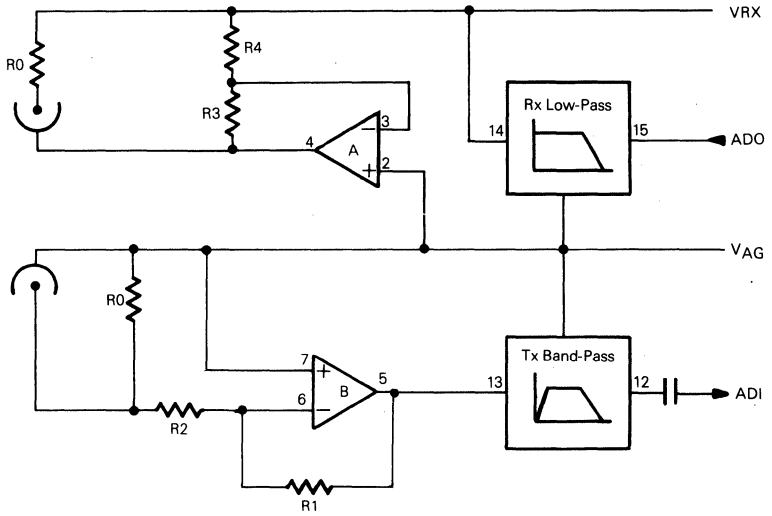


FIGURE 13 — TYPICAL 4-WIRE PORT INTERFACE USING MC14413



Full Scale Voltage at TxO (LPO) RxI	Port Impedance (RO)	Relative Level	R1	R2	R3	R4
5 V p-p	600	4.16 dBr	161 k	100 k	23.9 k	100 k
	900	2.4 dBr	198 k	150 k	51.8 k	100 k
6.2 V p-p, +9 dBm	600	6.00 dBr	100 k	100 k	Short	Open
	900	4.26 dBr	245 k	150 k	18.5	100 k
7.6 V p-p, +9 dBm	900	6.00 dBr	150 k	150 k	Short	Open

Interface to 2-wire or 4-wire ports using the MC14413-1,-2/14-1, -2 is shown in Figures 12 and 13, respectively. The table above shows some voltages typically used with the filter and the appropriate resistor values for cases in which the codec/filter OTLP is less than or equal to the 0 dBm level. If the codec/filter overload voltage is greater than required for 0 dBm levels in the load, the RxO output can be voltage divided by two resistors and the extra op amp used as a voltage follower.

FIGURE 14 — GENERATOR FOR 128 kHz IN SYSTEM USING 2.048 MHz CLOCK

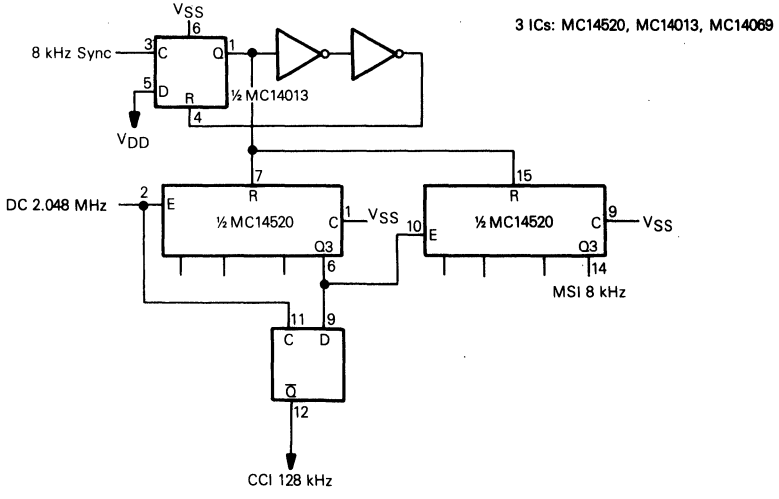


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FIGURE 15 — 128 kHz FREQUENCY SYNTHESIZER USING 8 kHz INPUT

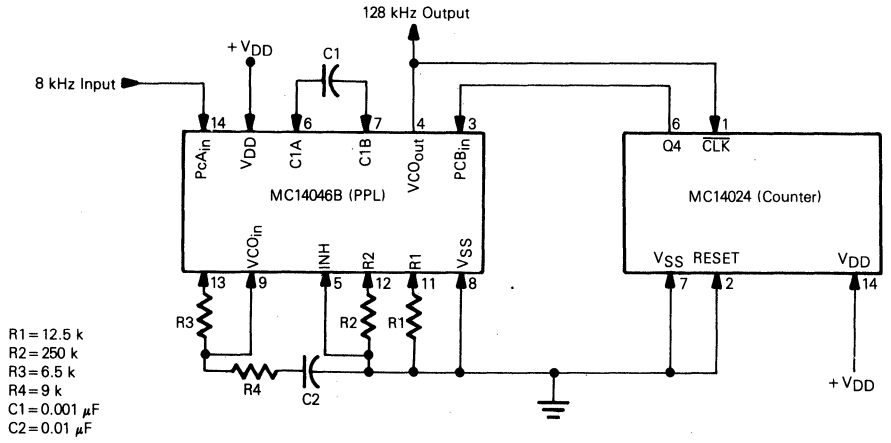


FIGURE 16 — GENERATION OF 128 kHz IN SYSTEM USING 1.544 MHz CLOCK

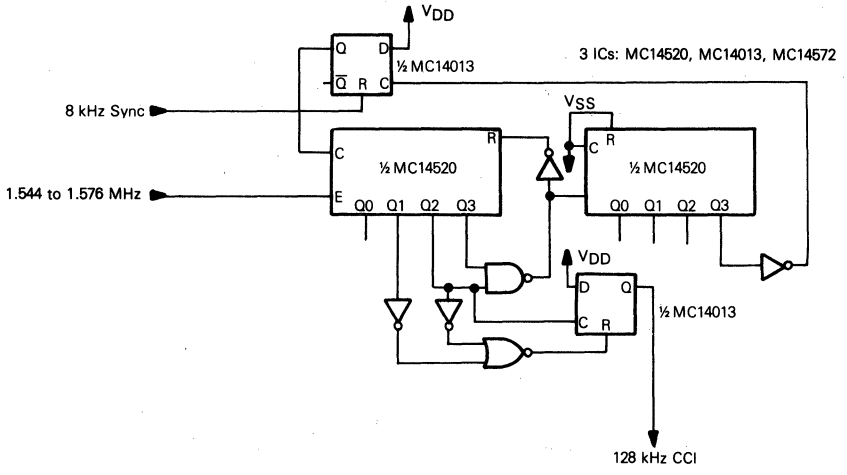
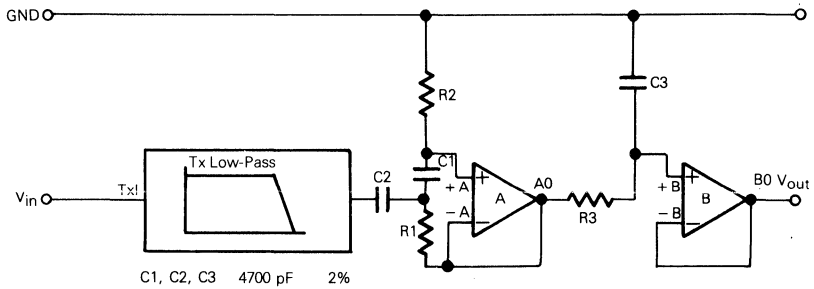


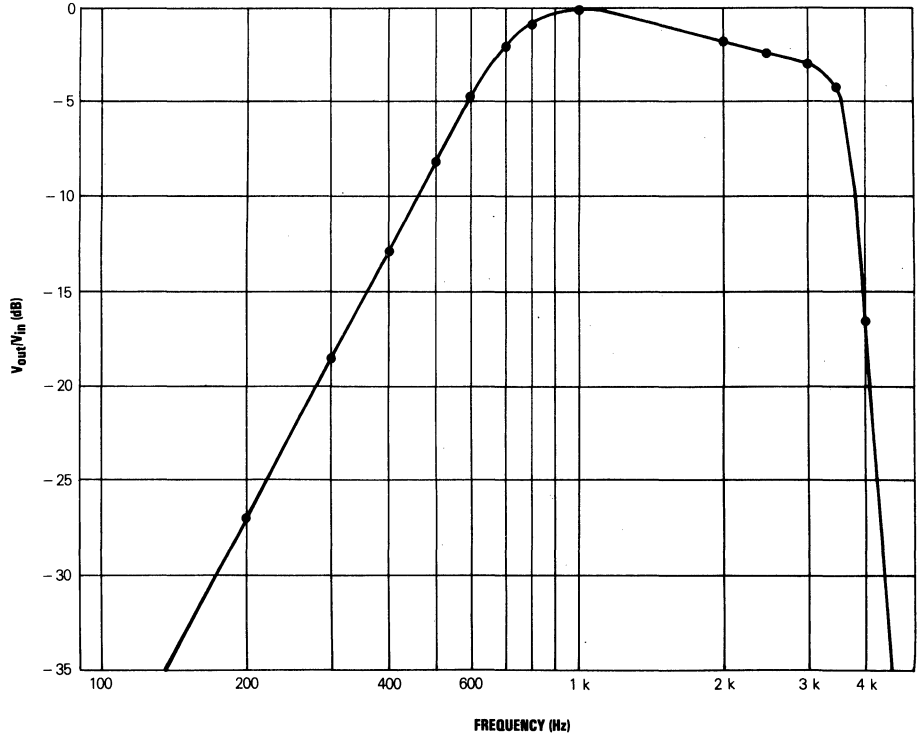
FIGURE 17 — TELEPHONY C-MESSAGE FILTER USING MC14414-1, -2 FILTER



C1, C2, C3	4700 pF	2%
R1	19.6 k	1%
R2	97.6 k	1%
R3	8.25 k	1%

V_{AG}, V_{LS} connected to GND
MSI, CCI connected to 134 kHz TTL clock
0.1 μF, V_{DD} to V_{AG} and V_{SS} to V_{AG}
Rx Filter can also be used and will provide 18 dB of input gain
V_{DD} = +5 V, V_{SS} = −5 V

NOTE: Op Amps A and B are the free op amps on the MC14414-1, -2 filter.



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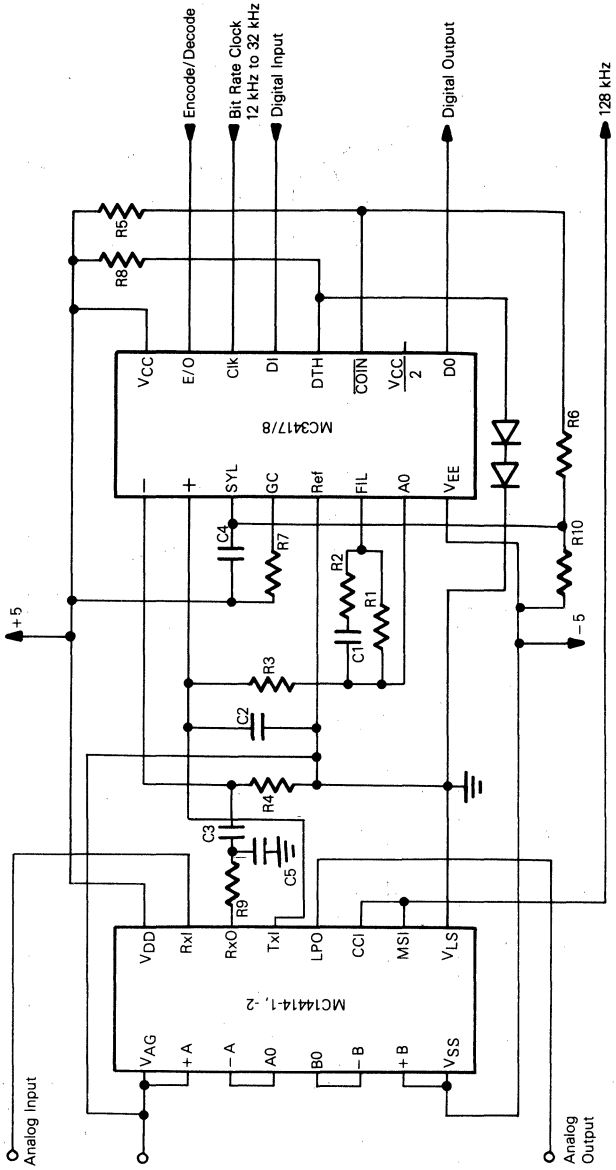


FIGURE 18 — DELTAMOD VOICE DIGITIZER USING MC3417 AND MC14414-1, -2

MC14416
MC14418

MOS LSI

(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER
CIRCUITS

2

PER CHANNEL, ADDRESSABLE TIME SLOT ASSIGNER CIRCUITS (TSACs)

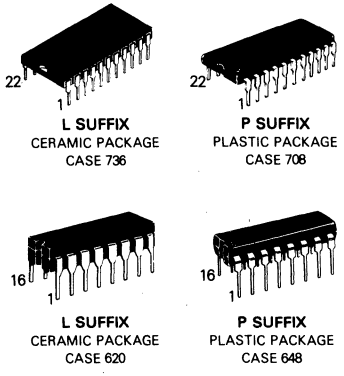
The MC14416 and MC14418 are per channel devices that allow variable codec time slot assignment to be programmed through a serial microprocessor port (0-63 time slots): Both devices have independent transmit and receive frame syncs and enables. They also include chip select and clear to send signals which simplify system design.

The MC14418 provides the additional addressing capability which allows a parallel bus back plane in the channel group. In addition, the MC14418 provides control bits which can be used for the power down, ring enable and ring trip functions on a line circuit.

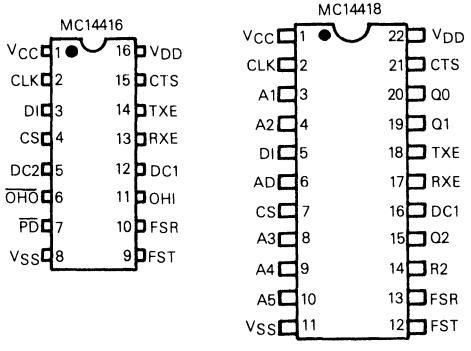
The MC14416 provides the ability to multiplex off hook signals for a bank of TSACs.

Both devices are fabricated using the CMOS technology for reliable low power performance. The MC14418 is the full featured device produced in a 22-pin package. The MC14416 without the addressing capability is offered in a 16-pin package.

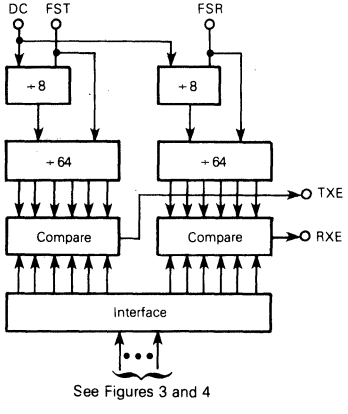
- Low Power
- 5-Volt Interface on Microprocessor Port
- 5-16 Volt Output Logic Levels
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- For Use With Up to 2.56 MHz Clocks
- Provides Power Down Control for Line Circuits
- Compatible with MC14400/01/02/03/05 and MK5116 Codecs
- Provides the Ring Enable and Ring Trip Functions (MC14418)
- Allows Use of a Parallel Backplane for Line Circuits Due to the Hard Wired Address Feature (MC14418)
- Off-Hook Multiplex Control (MC14416)
- CMOS Metal Gate for High Reliability



PIN ASSIGNMENTS



BLOCK DIAGRAM



See Figures 3 and 4

2

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	Vdc
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	 V_{in1} V_{in2}	 −0.5 to V_{DD} +0.5 −0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

Characteristic		Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage	$V_{SS} = 0$ V	V_{DD}	–	4.5	12	16	V
DC Supply Voltage	$V_{SS} = 0$ V	V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$ (V_{OL} = 0.4 V) (V_{OL} = 1.0 V)		I_{OL}	5 12	0.51 2.0	– 4.0	– –	mAdc
(V_{OH} = 4.6 V) (V_{OH} = 1.0 V)		I_{OH}	5 12	−0.20 −2.0	– −4.0	– –	mAdc
Output Current CTS, OHO (V_{OL} = 0.8 V) (V_{OL} = 0.8 V) (V_{OL} = 1.5 V)		I_{OL}	5 12 12	3.0 6.6 12.0	5.5 11.5 20.0	– – –	mAdc
(V_{OH} = 0.8 V) (V_{OH} = 2.0 V) (V_{OH} = 0.8 V) (V_{OH} = 2.0 V) (V_{OH} = 10.5 V)		I_{OH}	5 5 12 12 12	−8 −6 −40 −35 −15	−20 −18 −100 −90 −30	−40 −40 −200 −200 −60	μAdc
Input Voltage (CMOS) FST, FSR, R2, DC1, DC2, A1, A2	"0" Level	V_{IL}	5 12	– –	– –	1.0 2.4	Vdc
A3, A4, A5, OHI	"1" Level	V_{IH}	5 12	4.0 9.6	– –	– –	Vdc
Input Current OHI (Active Pull Down)		I_{inH}	5 12	+1.5 +10	+4.0 +25	+15 +100	μAdc
Input Voltage (TTL) CLK, CS, AD, DI	"0" Level	V_{IL}	5 12	– –	– –	0.8 0.8	Vdc
V_{CC} = 5 V	"1" Level	V_{IH}	5 12	2.00 2.00	– –	– –	Vdc
Input Current		I_{in}	15	–	$\pm 10^{-5}$	±0.1	μAdc
Input Capacitance		C_{in}	–	–	5	7.5	pF
Total Supply Current (Outputs Unloaded) V_{DD} = 12 V V_{DD} = 5 V	DC1 at 2.048 MHz	I_T	12 5	– –	3 2	6 4	mAdc
Total Supply Current (Power Down) MC14418 Only After CTS = V_{DD} CLK, CS, AD, DI Inputs ≤ 0.6 V		I_{PD}	–	–	–	0.1	mAdc

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$, unless otherwise noted)

Characteristic	Symbol	Fig.	V_{DD}	Min	Typ	Max	Unit
Output Rise Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_r	–	5 12	– –	100 50	200 100	ns
Output Fall Time TXE, RXE, Q0, Q1, Q2, $\overline{P_D}$	t_f	–	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time	t_{SFS}	1	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	1	5 12	200 100	– –	– –	ns
Propagation Delay – DC to TXE, RXE (Note 1) $C_L = 20$ pF	t_{PLHE}, t_{PHLE}	1	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	–	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width (at $f_{DC(MAX)}$)	t_{PWDC}	1	5 12	200 140	244 192	293 260	ns
Clock Frequency	f_{CLK}	–	5 12	00 00	– –	0.3 0.3	MHz
Clock Pulse Width (at $f_{CLK(MAX)}$)	t_{PWC}	2	5 12	0.5 0.5	– –	– –	μs
Address and Data Setup Time	t_{su}	2	5 12	300 300	– –	– –	ns
Address and Data Hold Time	t_h	2	5 12	200 200	– –	– –	ns
Propagation Delay – DC1 to CTS	t_{PCL}	2	5 12	– –	– –	250 150	ns
DC1 or FST to CTS 10K Pullup or Equivalent	t_{PCH}	2	5 12	– –	– –	300 200	ns
Propagation Delay – DC to PD	t_{PQ}	2	5 12	– –	– –	300 200	ns
DC to Q0-Q2	t_{PQ}	2	5 12	– –	– –	300 200	ns
Propagation Delay – R to Q2	t_P	2	5 12	– –	100 50	200 100	ns
Chip Select Setup Time Leading CS to Falling CLK	t_{SCS}	2	5 12	1 1	–	–	μs
Chip Select Hold Time Falling CTS to Falling CS	t_{HCS}	2	5 12	10 10	– –	– –	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 – TIMING DIAGRAMS

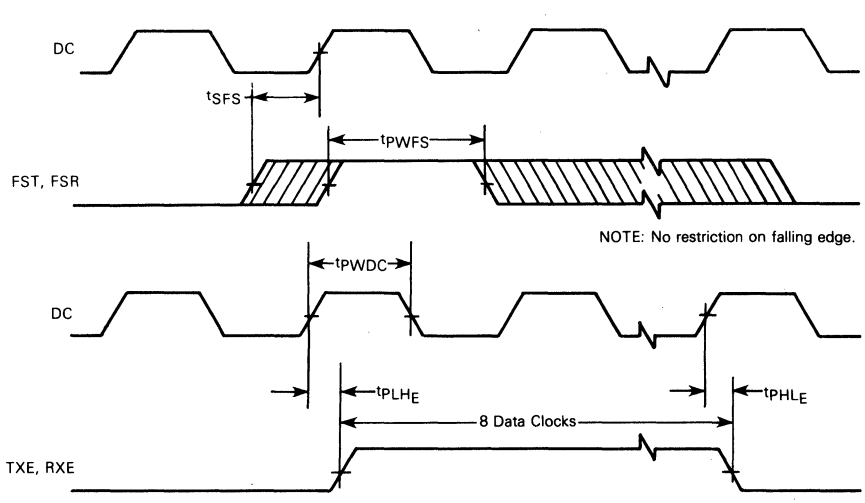
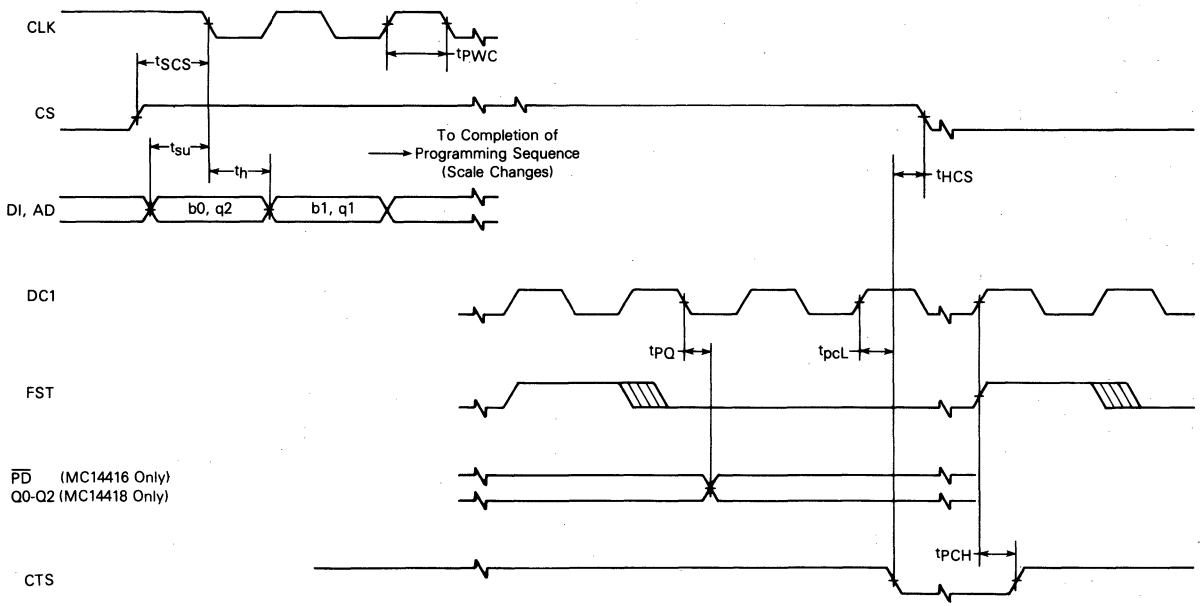
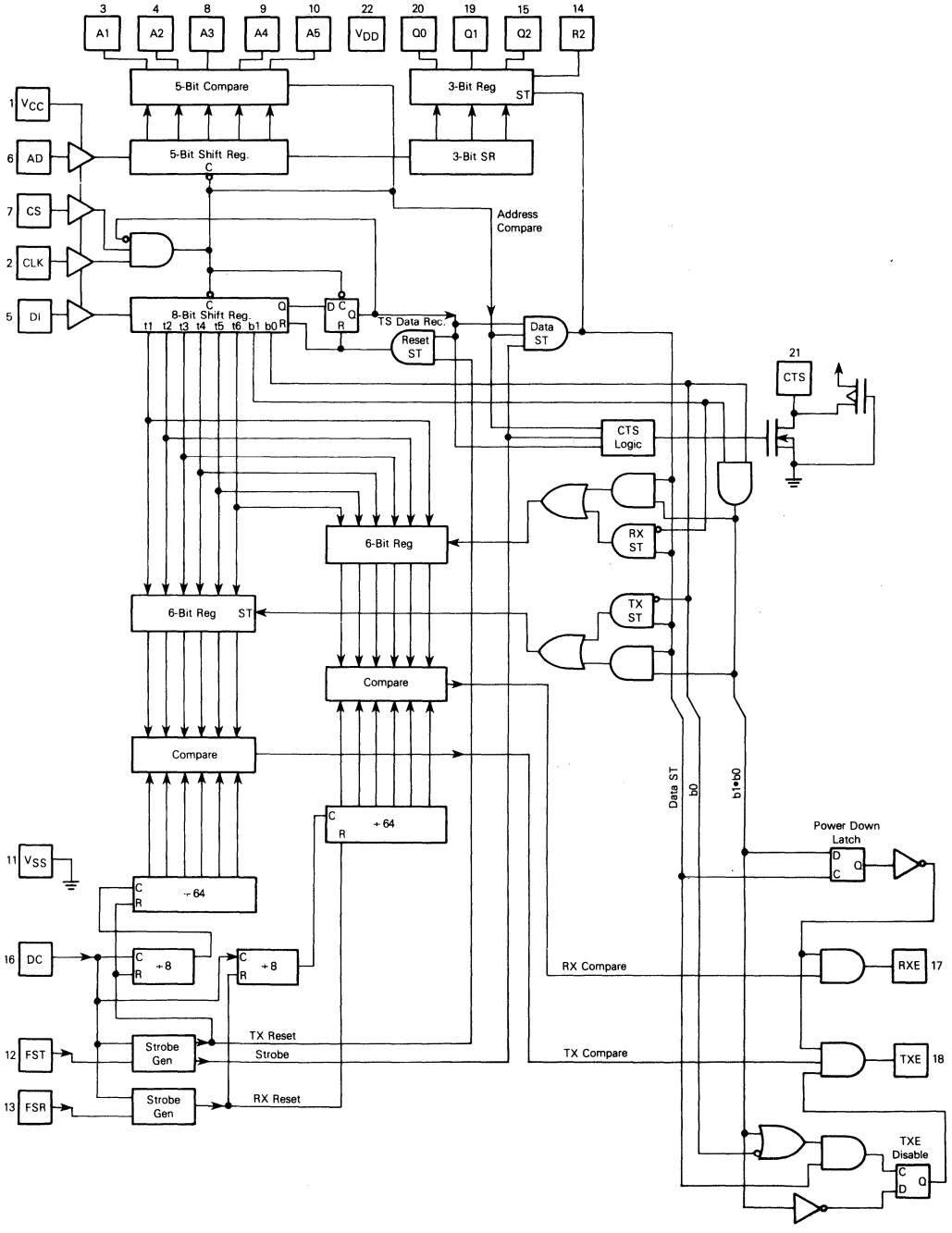


FIGURE 2 — PROPAGATION DELAYS FOR PROCESSOR INTERFACE PINS



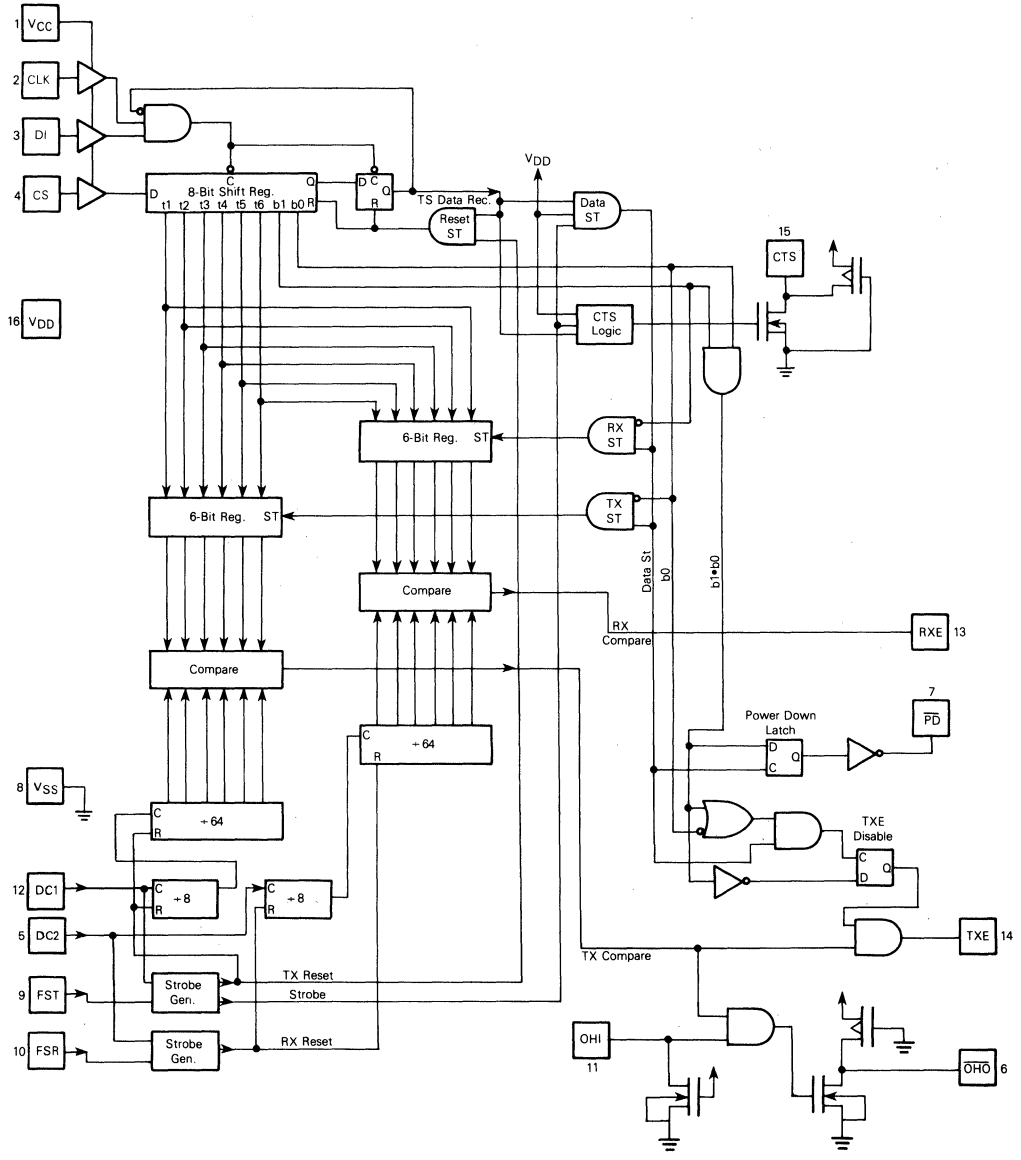
NOTE: t_{PCH} is measured from the rising edge of the latter of FST or DC1.

FIGURE 3 — MC14418 22 PIN



2

FIGURE 4 — MC14416 16 PIN



GENERAL DEVICE DESCRIPTION

The MC14416 and MC14418 TSACs are microprocessor peripherals intended to be used to control and supervise per channel codec subscriber channel units. The TSACs consist of three basic functions.

The Serially Programmable Microprocessor Port consists of V_{CC}, CLK, DI, CS and CTS for the MC14416 and further includes AD and A1 through A5 for the MC14418. This port allows the call processing microprocessor to access load data into each TSAC. See the applications section for a detailed description of the microprocessor port. Figure 5 defines the data word bit assignments.

The Supervision Controls consist of Q0, Q1, Q2, R2 on the MC14418 and OHI, $\overline{OHO}$ and $\overline{PD}$ on the MC14416. These functions provide data path for the supervision and control of user selected requirements in the subscriber channel unit. Figure 3 shows some typical uses of these bits.

The Time Slot Computation section of the chip derives separate transmit and receive time slot outputs (TXE and RXE) for the controlled codec from the bit rate clock and sync pins DC1, DC2, FST and FSR, respectively. The computed time slot is then derived from the information received through the microprocessor port.

PIN DESCRIPTIONS

V_{CC} (Positive Supply for Microprocessor Port) — If this is a 5-volt supply, AD, DI, CS and CLK are TTL compatible CMOS inputs. V_{CC} may be any voltage from 4.5 V to V_{DD} allowing either TTL or CMOS compatibility.

CS (Chip Select Input) — For the MC14418, the pin is used to select a bank of TSACs.

For the MC14416, the CS is used to select that individual TSAC. All CSs are normally held low. To PROGRAM A SPECIFIC TSAC, CS must go high prior to the first falling edge of CLK. CS must stay high until the selected CTS goes low to guarantee a valid access.

CS is synchronous with DI, AD and CLK. CS can be asynchronous with DC1, DC2, FST or FSR. (This pin is normally intended to be set by a microprocessor.)

CLK (Microprocessor Clock Input) — Serial data is entered through the AD and DI pins under the control of CLK. The data is entered on the trailing edge of CLK. CLK is synchronous with CS, AD and DI and can be asynchronous with the TSAC's data clocks (DC1 or DC2).

DI (Serial Time Slot Data and Mode Input) — 8-bit words are clocked into the device through DI under the control of CLK after CS is brought high. The first 2 bits of DI control the various programming modes while the last 6 bits are time slot data. (See Figure 5 for the format of the DI word.)

AD (Serial Address and Control Bits Input — MC14418 only) — 8-bit words are clocked into the device through AD under the control of CLK after CS is brought high. AD words are loaded in parallel with the DI words. The first 3 bits of AD program the control bits Q0, Q1, and Q2 while the last 5 bits are compared with the hardware address on A1 through A5 to identify a specific TSAC in a bank. (See Figure 5 for the format of the AD words.)

A1-A5 (Codec Address Inputs — MC14418 only) — These five pins provide a unique identity for each TSAC. The TSAC address pins are either hardwired on the PC board or in the channel bank backplane. The processor loads the 5-bit address data into AD, and each MC14418 in the selected bank compares this data to the hardwired address set by its A1-A5 to determine if the time slot data loaded into DI is intended for that TSAC. By this process, only one of 32 TSACs in a bank will accept the transmitted time slot data. A1-A5 are CMOS inputs, logical "1" = V_{DD} and logical "0" = V_{SS}.

Q0, Q1, Q2 (Status Bit Outputs — MC14418 Only) — These three bits are programmed by the first 3 bits of the 8-bit word which is loaded into AD. The bits are used for the basic control functions of a line circuit. See the applications section (ref. Figure 11) for an example of how these status bits are used. In this example, Q1 selects to receive data streams, Q0 is used for the power down control, and Q2 is used for the ring enable. These are CMOS outputs.

R2 (Reset Input for Q2) — The R2 input provides a direct reset of the Q2 output. When R2 is taken high, Q2 is set to "0" independent of all other TSAC functions. See the applications section (ref Figure 11) for an example of how this reset bit is used, i.e., the ring trip signal is used to reset Q2 which is the ring enable. This combination of R2 and Q2 allows a simple solution to the ring trip function.

CTS (Clear to Send Output) — This output provides a simple diagnostic capability for the processor TSAC combination. The selected TSAC outputs the CTS signal after it has accepted data. This output goes low three data clock cycles after the next FST, and returns high on the subsequent FST. For the MC14418, only the TSAC which accepts transmitted data will respond with CTS low. All other TSACs in the bank will leave CTS high. The CTS output is an open drain transistor with a weak internal pullup. Normally a bank of CTS outputs are wire ORed together to provide a single diagnostic bus, which can be used to verify that transmitted data was properly acknowledged by some TSAC in the bank.

CTS may also be used to strobe additional supervision data into a selected channel unit, due to its dependence upon the address selection logic of the MC14418.

DC1, DC2 (Data Clock Input) — The data clock input establishes the bit rate of the TSAC and its associated codec. It is intended to be between 1.536 and 2.56 MHz and is the same as the codec's bit rate clock. Both TSACs divide these inputs by eight to derive the time slot rate. For the MC14418, DC1 provides the data rate clock for both transmit and receive time slot computation. The MC14416 derives transmit timing from DC1 and receive timing from DC2. They are CMOS compatible inputs.

FST, FSR (Frame Sync Transmit and Frame Sync Receive Inputs) — These inputs are leading-edge sensitive synchronization pulses for establishing the position of time slot zero in the transmit and receive frames, respectively.

The rising edge of DC (1 or 2) associated with the rising edge of FST or FSR identifies the sign bit period of time slot zero. See Figures 6 and 7 for detailed timing. In the MC14418, both zero time slots are derived from DC1 but may be different by an integral number of bits. In the MC14416, FST and DC1 derive the transmit time slot zero, while FSR and DC2 derive the receive time slot zero independently. DC1 and DC2 can be asynchronous. FSR and FST are CMOS inputs.

2

TXE, RXE (Transmit Enable and Receive Enable Outputs) – These are the outputs of the time slot computation circuitry. Each output is high for eight data clocks; i.e., an integral number of time slots after the rising edge of FST and FSR for TXE and RXE, respectively. The binary number entered in the last 6 bits of the DI input indicates the number of eight data clock intervals (time slots) between FST or FSR and the eight data clock time slot, when TXE or RXE will be high. These are CMOS B series outputs which will drive one TTL LS input when V_{DD} is five volts. See Figure 6 and Figure 7 for detailed timing and numbering.

TABLE 1 – BASIC OPERATION OF MC14418

Input Conditions				Action to Outputs After Next FST						
TS Data Received	Address Compare	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	RXE Disabled	Data Reg. (Q0-Q2) Load	Time Slot Counters Running
No	X	X	X	1	No	No	No Change	No Change	No	No Change
Yes	No	X	X	1	No	No	No Change	No Change	No	No Change
Yes	Yes	0	0	0	Yes	Yes	No	No	Yes	Yes
Yes	Yes	0	1	0	Yes	No	No	No	Yes	Yes
Yes	Yes	1	0	0	No	Yes	No Change	No	Yes	Yes
Yes	Yes	1	1	0	X	Yes	Yes	Yes	Yes	No

TABLE 2 – BASIC OPERATION OF MC14416

Input Conditions					Action to Outputs After Next FST			
TX Data Received	CS	b0	b1	CTS	TX Reg. Load	RX Reg. Load	TXE Disabled	$\overline{PD}$ Output
No	X	X	X	1	No	No	No Change	No Change
Yes	0	X	X	1	No	No	No Change	No Change
Yes	1	0	0	0	Yes	Yes	No	1
Yes	1	0	1	0	Yes	No	No	1
Yes	1	1	0	0	No	Yes	No Change	1
Yes	1	1	1	0	No	No	Yes	0

Note 1: The $\overline{OHO}$ output remains operational when TXE is disabled.

FIGURE 5 – FORMAT FOR DI AND AD WORDS

MC14418	DI Word Input								AD Word Input							
	First Bit Sent								First Bit Sent							
Results of Bit Pattern	Mode		Time Slot Data						Status Bits			Address Data				
	b0	b1	t6	t5	t4	t3	t2	t1	q2	q1	q0	a5	a4	a3	a2	a1
Assign TSAC 16 to the first time slot (TSO) for both receive and transmit and set its status bit to 011	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
Assign TSAC 1 to time slot 8 for receive only and set status bits to 011	1	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1
Assign TSAC 8 to time slot 2 for transmit only and set status bits to 011	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0	0
Program TSAC 4 to idle (no time slot outputs) and set status bits to 011	1	1	X	X	X	X	X	X	0	1	1	0	0	1	0	0
Codec 1 is powered down (80=0)	X	X	X	X	X	X	X	X	0	1	0	0	0	0	0	1
Line circuit associated with codec 2 is programmed to ring the line (See Fig. 13)	X	X	X	X	X	X	X	X	1	1	1	0	0	0	1	0

MC14416

Assign the selected TSAC to the first time slot (TSO) for both receive and transmit and set $\overline{PD}=1$	0	0	0	0	0	0	0	0
Assign the selected TSAC to time slot 8 for receive only and set $\overline{PD}=1$	1	0	0	0	1	0	0	0
Assign the selected TSAC to time slot 2 for transmit only and set $\overline{PD}=1$	0	1	0	0	0	0	1	0
Power down the selected TSAC, i.e., $\overline{PD}$ to "0"	1	1	X	X	X	X	X	X

*See Figures 12 and 13 for the hardware implementations using MC14418 and MC14416.

FIGURE 6 — DATA MULTIPLEX TIMING FOR 2.048 MHz

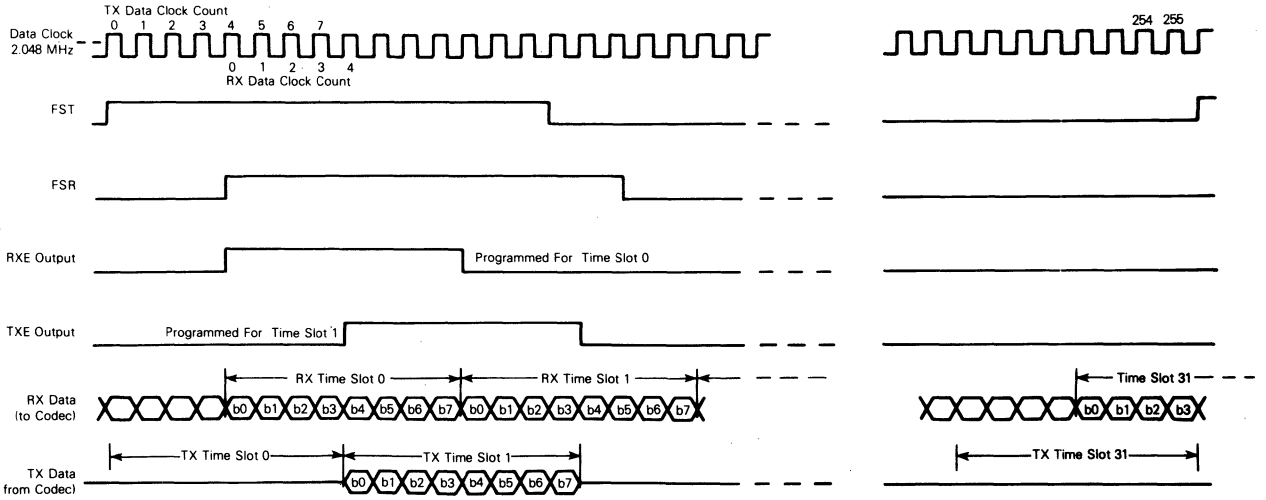
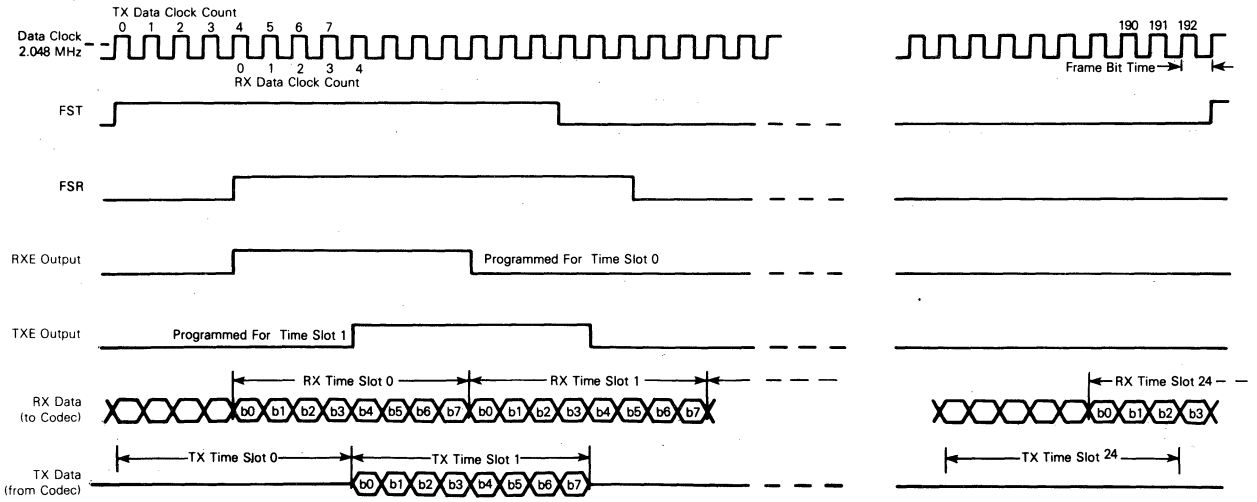


FIGURE 7 — DATA MULTIPLEX TIMING FOR 1.544 MHz



$\overline{PD}$ (Power Down Output — MC14416 Only) — The $\overline{PD}$ output is normally high. It is set high whenever b0 or b1 is a zero and the TSAC is programmed. If b0 and b1 are both one, then PD will be set low. This output is intended to be used to power down other circuitry in the channel unit when the channel unit is idle. This is a CMOS B series output which will drive one TTL LS load when V_{DD} is five volts.

OHI (Off Hook Input — MC14416 Only) — The OHI is a CMOS input with an internal pull-down resistor. A DC level at this pin will appear at the OHO output during the programmed TXE time slot.

$\overline{OHO}$ (Off Hook Output Inverted — MC14416 Only) — During the programmed transmit time slot, the data at OHI appears inverted at $\overline{OHO}$; otherwise $\overline{OHO}$ will be pulled high passively. The $\overline{OHO}$ output is an open drain N-channel transistor with a weak pull-up to V_{DD}. A number of these outputs can be wire ORed together to form a hook status bus consisting of a serial stream of hook information from a bank of channels. When the MC14416 powers down its codec, the TXE output is disabled; but the $\overline{OHO}$ output continues to multiplex out OHI and transmit time slot information during the previously entered transmit time slot.

V_{SS} — This is the most negative supply pin and digital ground for the package.

V_{DD} — This is the most positive supply. V_{DD} is typically 12 V with an operation range of 5 to 16 volts. All logic outputs swing the full supply voltage.

APPLICATIONS

The following section is intended to facilitate device understanding through several application examples. Included are Data Multiplex Timing Diagrams, a description of the TSAC Microprocessor port, a sample program, two circuit configurations using Motorola's devices, a systems drawing and two suggested clock circuits for obtaining codec data and control clocks.

In Figures 6 and 7 are shown Data Multiplex Timing Diagrams for 2.048 MHz and 1.544 MHz data clocks. The major points to be seen from these examples are:

1) Receive and transmit programming for the MC14418 are bit synchronous and word asynchronous. The MC14416 can be completely asynchronous.
2) The rising edges of FST and FSR initiate the programming frame for transmit and receive channels, respectively, and identify transmit and receive time slot "0," respectively.
3) Time slots identify eight data clock words. In this example: the transmit time slot is programmed as time slot "1." Therefore, bits 8 through 15 after FST are time slot "1."
4) For the 1.544 MHz clock, the framing bit is at the very end of the frame.

TSAC Microprocessor Port (MC14418 and MC14416) — The MC14418 provides four pins with 5-volt microprocessor input characteristics. These are AD, CS, CLK, and DI. The input supply for these inputs is V_{CC}. The CTS output is an open drain device with a weak pull up to V_{DD}. Typically, these five pins are bused in parallel to 24 or 32 TSACs per processor port. If desired, AD, CLK, DI, and CTS may be bused to greater than 32 TSACs by using the CS input as a group select. A microprocessor port of eight bits can thus control four groups of 32 TSACs with no additional decoding, as shown in Figure 8.

In order to program any given codec to a transmit or receive time slot, the processor simply exercises the corresponding 8-bit port.

Beginning with CS1 to CS4 low, all TSACs in the bank have their data registers in the Ready for Data Mode. The microprocessor takes the appropriate CS high and clocks in two bits of data into the 32 selected TSACs through DI and AD using CLK. The microprocessor presents data on the leading edge of CLK and the TSACs clock in data on the trailing edge of CLK. After eight CLK pulses (high, then low) the 32 selected TSACs will have two new 8-bit words; one in the data register through DI and one in the address register through AD. The unique TSAC, whose last 5 bits of the address register match its hardwired address on A1 through A5, acknowledges the new data. After the next FST, the selected TSAC will pull CTS low. This event notifies the processor that its transmission has been recognized. If CTS occurs at any other time, the processor can recognize the fault condition and restart the transmission using the reset function of the TSAC chip select. The uniquely selected TSAC will load its new program data into the appropriate TIME SLOT register on the next leading edge of FST. The bank of 32 TSACs will internally reset to the Ready for Data Mode when the transmission is completed, after the next FST. The TSAC, which was uniquely selected, and which has CTS low, will clear CTS to the pulled-up condition with the next FST. The processor may now program a new time slot immediately, with or without returning the selected CS low. Time Slot data can thus be sent at the rate of once every 256 μsec. for 8 kHz sampling (FST). The processor need not operate in an interrupt mode even though the TSAC's DC and CLK are asynchronous.

The processor port of the MC14416 works similarly to the MC14418, but will accept data if CS is high, and does not compare a hardwired address to the address word.

Figure 11 shows the typical signal timing for programming the microprocessor port.

To demonstrate the programming of the TSAC, consider the following configuration. A microprocessor is used to control four groups of thirty-two TSACs through an eight-bit PIA port. Four of the PIA lines are used for group select lines. The other four lines are dedicated to CLK, DI, AD, and CTS. The TSACs are programmed by serially loading bits into the DI and AD leads. Data bits are latched on the falling edge of CLK. The PIA port is connected as shown in Figure 9. The flow chart in Figure 10 and the following program illustrate one method of TSAC programming.

Before running the following program, the address, time slot, and group number must be entered in appropriate locations. During execution, CS (group select), AD, and DI words are arranged for serial presentation to the TSACs. The bits are presented with CLK high and are latched in with the falling edge of CLK. After eight passes through the loop, the TSAC is programmed, and CTS falls on the third data clock pulse after the next FST. The program waits for CTS to go high again before removing CS to prevent aborting the TSAC's programming. This program allows a maximum rate of programming equal to one TSAC per two frames.

2

FIGURE 8 — TYPICAL 8-BIT PORT

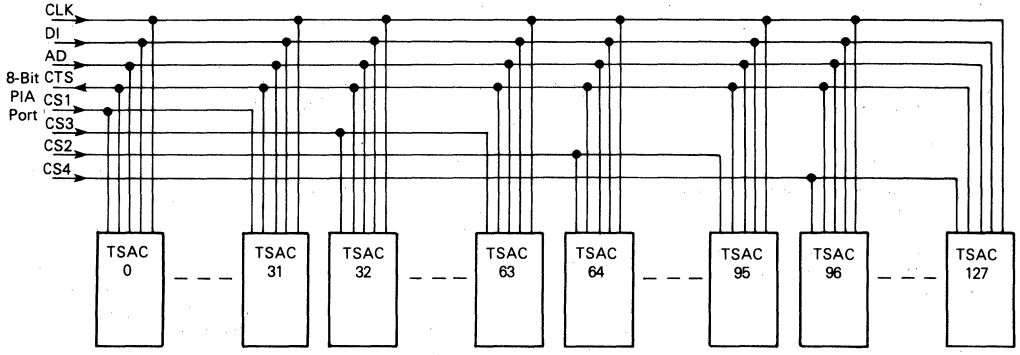


FIGURE 9 — PIA PORT ASSIGNMENT

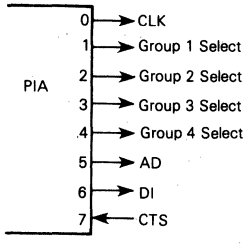
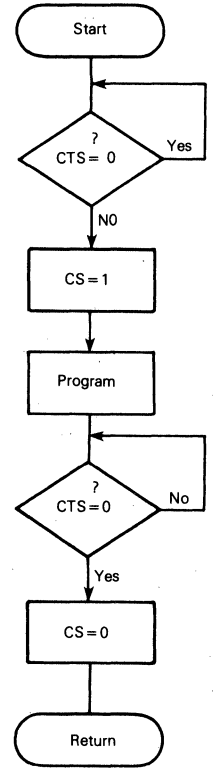


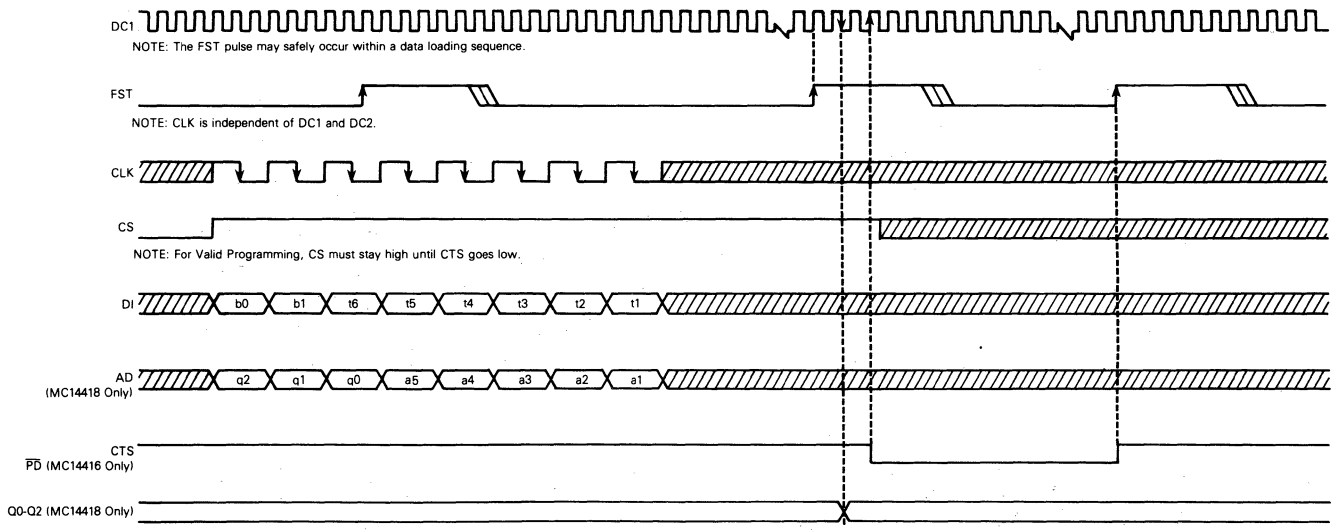
FIGURE 10 — TSAC PROGRAMMING FLOW CHART



Instructions for use:
Load in AD word (Q2, Q1, Q0, A5, A4, A3, A2, A1)
DI word (b0, b1, t6, t5, t4, t3, t2, t1)
group word
Start routine.

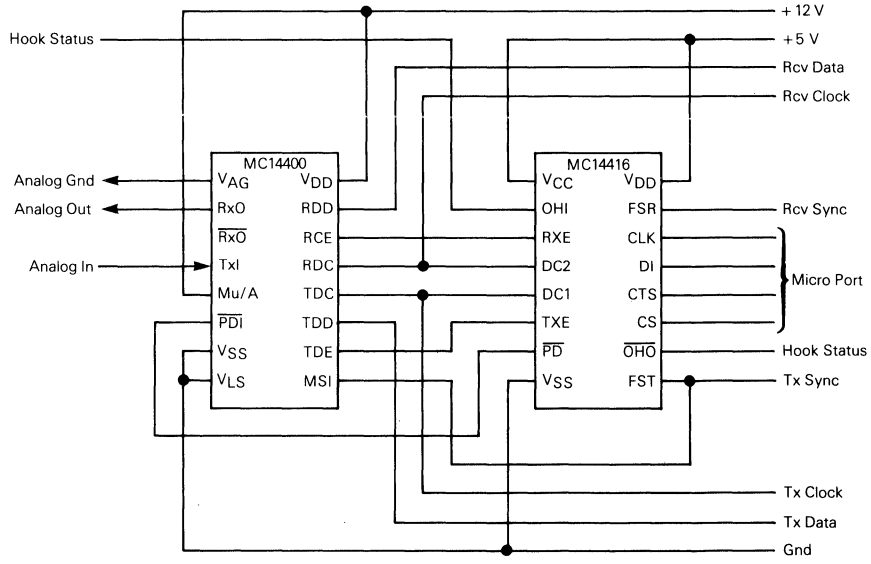
```
        LDAA GROUP      STORE GROUP # IN ACCA
        DECA            CHECK IF EQ. TO ONE
        BNE ONE         IF NOT GO TO NEXT TEST
        LDAB #03        EQUALS ONE
        STAB SELECT     LOAD PROPER SELECT BITS IN SELECT WORD
        BRA START       JUMP TO NEXT PART
ONE     DECA            IS GROUP EQ. TO TWO?
        BNE TWO         IF NOT GO TO NEXT TEST
        LDAB #05        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
TWO     DECA            CHECK IF EQ. TO THREE
        BNE THREE       IF NOT IS EQ. TO FOUR
        LDAB #09        LOAD PROPER SELECT BITS IN SELECT WORD
        STAB SELECT
        BRA START       JUMP TO NEXT PART
THREE   LDAB #11        LOAD GROUP SELECT BITS FOR GROUP FOUR
        STAB SELECT
START   LDAA #00        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAA #7F        INITIALIZE PIA
        STAA DDRB       INITIALIZE PIA
        LDAA #04        INITIALIZE PIA
        STAA CONTRLB    INITIALIZE PIA
        LDAB #80        TEST FOR CTS HIGH
WAIT    BITB PIAOUT     WAIT FOR CTS HIGH
        BEQ WAIT
        LDAA #01        NOW CTS IS HIGH, SET CLK HI AND LEAVE CS LOW
        STAA PIAOUT
        LDAA #08        INITIALIZE LAP COUNTER
        STAA COUNTER
        LDX 00          MOVE AD AND DI INPUTS
        STX 02          TO SHIFT LOCATIONS
        LDAA SELECT     BRING CS HIGH
        STAA PIAOUT
LOOP    LDAA SELECT     START BIT STUFFING
        ROL 0002        CHECK AD WORD
        BCC 02          CHECK AD WORD
        ORAA 20         CHECK AD WORD
        ROL 0003        CHECK DI WORD
        BCC 02          CHECK DI WORD
        ORAA 40         CHECK DI WORD
        STAA PIAOUT     WRITE BITS TO TSAC
        DECA            WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        NOP             WRITE FALLING EDGE OF CLK
        STAA PIAOUT     WRITE FALLING EDGE OF CLK
        DEC COUNTER     DECREMENT LAP COUNTER
        BNE LOOP        TEST FOR LOOP COMPLETION
        LDAB #80        TEST AND WAIT FOR CTS LOW
ISITLO  BITB PIAOUT     TEST AND WAIT FOR CTS LOW
        BNE ISITLO      TEST AND WAIT FOR CTS LOW
        CLR PIAOUT      REMOVE CS (GROUP SELECT)
        RTS             RETURN FROM SUBROUTINE
```

FIGURE 11 — MICROPROCESSOR PORT TIMING



NOTE: For the MC14416, the CTS line is pulled low by the device selected by the CS pin.
For the MC14418, the CTS line is pulled low by the device whose address matches the data loaded in through the AD pin.

FIGURE 12 — TYPICAL CIRCUIT CONFIGURATION USING MC14416
IN CONJUNCTION WITH MC14400



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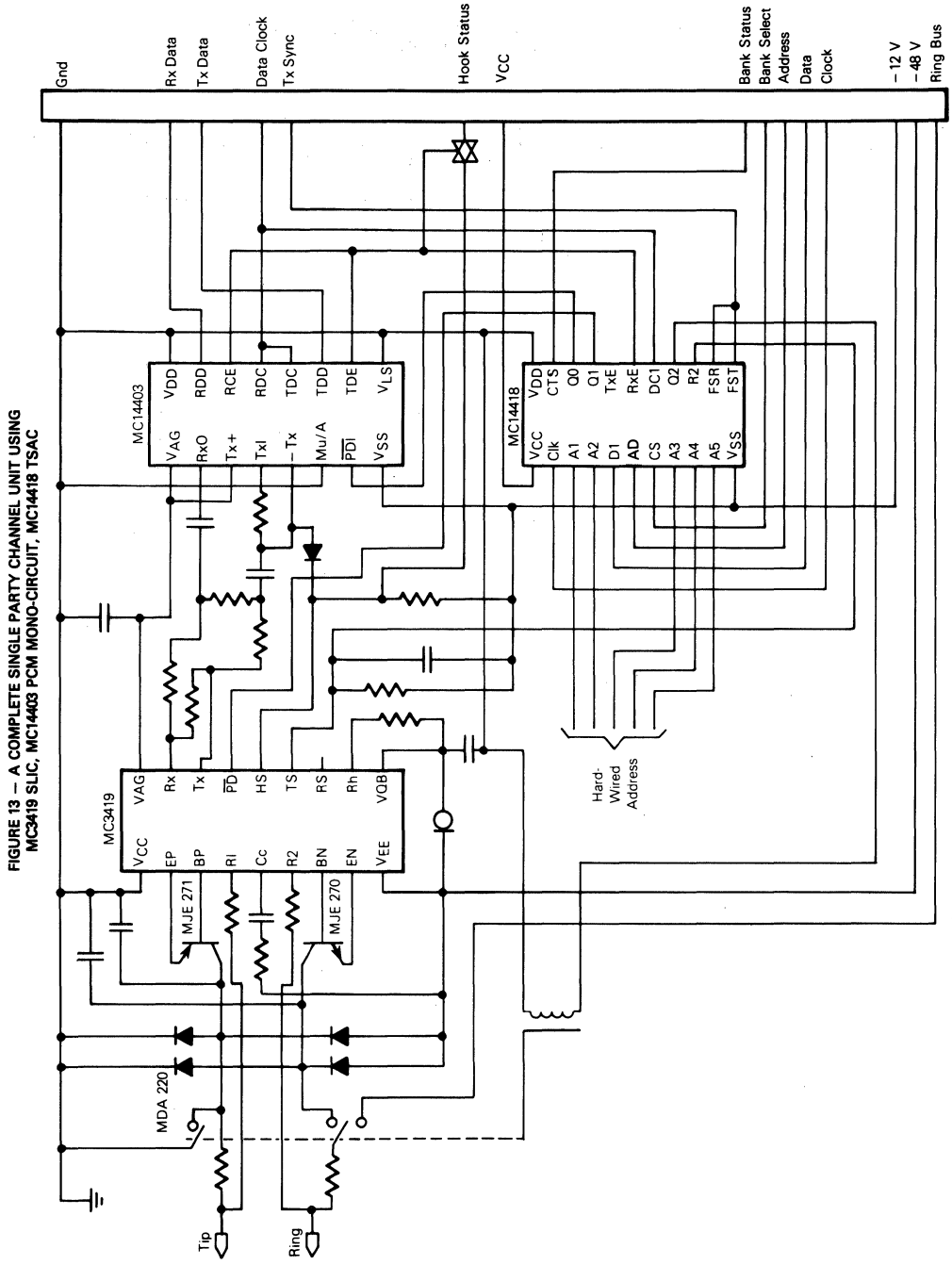
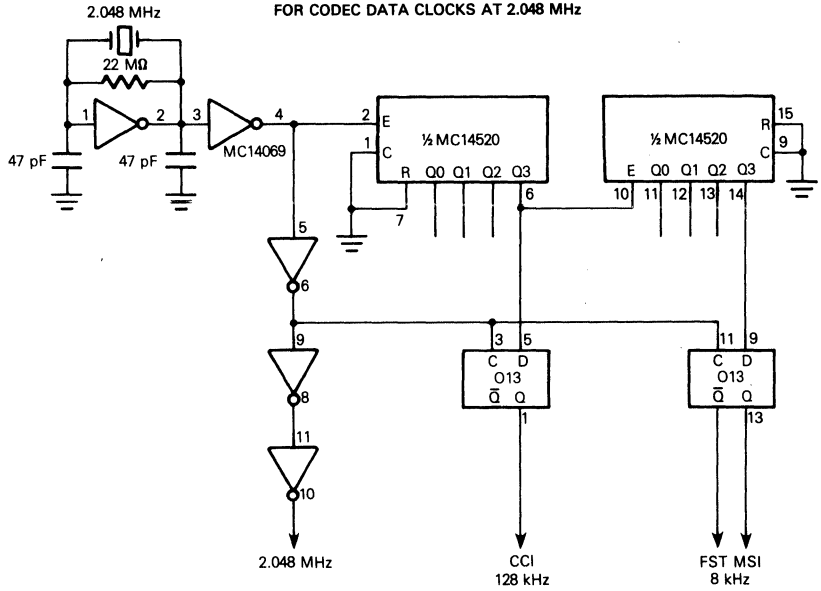
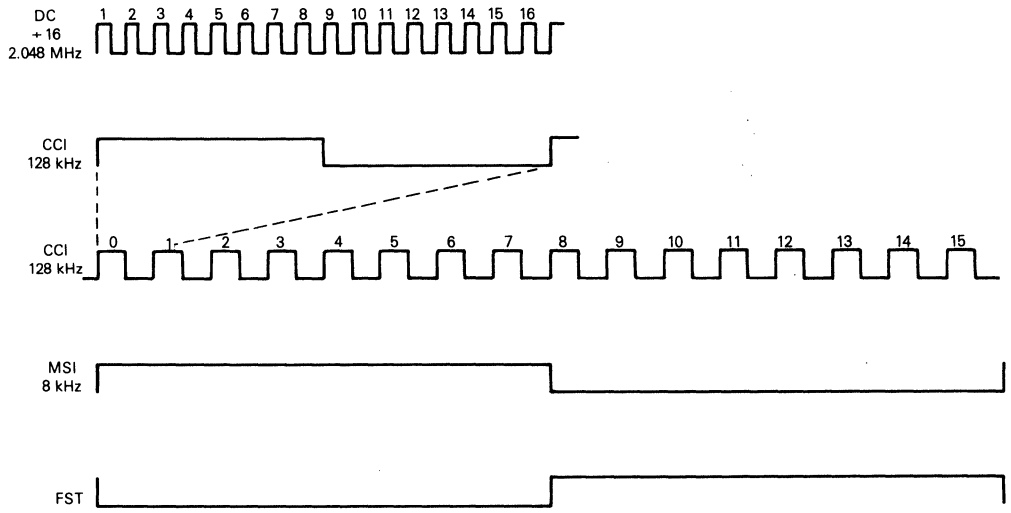


FIGURE 13 – A COMPLETE SINGLE PARTY CHANNEL UNIT USING MC3419 SLIC, MC14403 PCM MONO-CIRCUIT, MC14418 TSAC

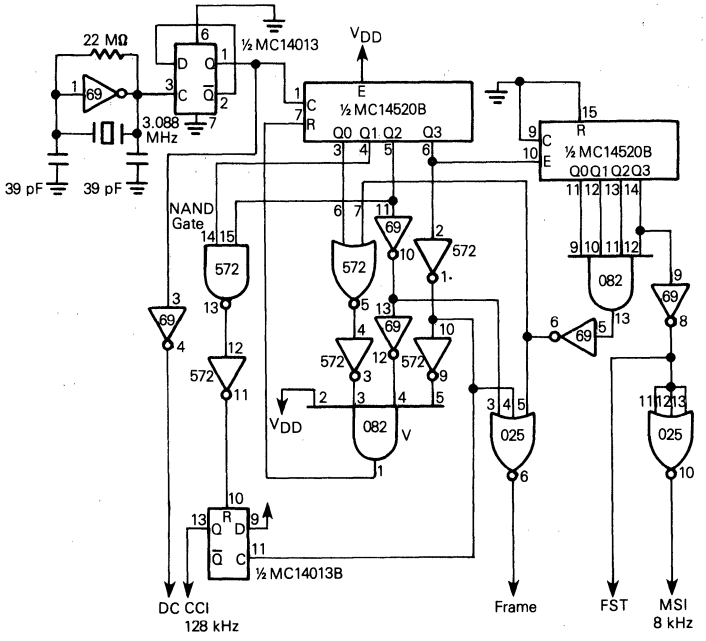
FIGURE 14 – CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 2.048 MHz

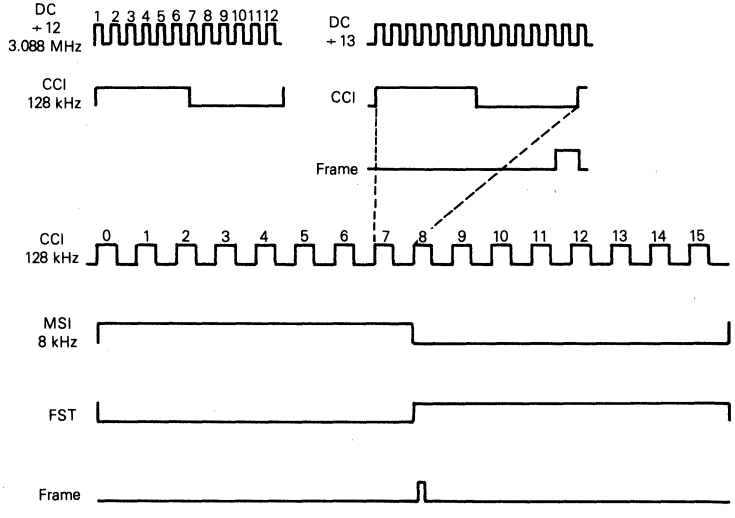




2

FIGURE 15 — CLOCK CIRCUIT AND TIMING
FOR CODEC DATA CLOCKS AT 1.544 MHz





MC14417

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

TSAC
TIME SLOT ASSIGNER
CIRCUIT

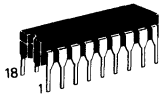
2

BASIC TIME SLOT ASSIGNER CIRCUIT (TSAC)

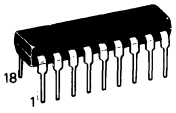
The MC14417 is a per channel Time Slot Assigner Circuit (TSAC) that produces 8-bit receive and transmit time slots for a PCM Codec. The pins D0 to D5 are the time slot data inputs which can be either hard-wired on the printed circuit board for fixed time slot assignment, or externally programmed through the use of these pins and the latch enable function. The receive and transmit frame syncs and enables are independent. In addition, a T/R (TXE/RXE swap) input is provided which allows a simplified switching mechanism for a small systems architecture (i.e., key systems).

The MC14417 can operate from a single 5-volt supply for TTL levels or up to 16-volts for CMOS levels. The MC14417 is fabricated using the CMOS technology for reliable low-power performance.

- TTL and CMOS Level Compatibility
- 5 to 16 Volt Operation
- Low Operating Power Consumption
- For Use With Up to 2.56 MHz Clocks
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- Compatible with MC14400/01/02/03/05 PCM Mono-Circuits
- Allows Swapping of Transmit Enable (TXE) and Receive Enable (RXE) Signals
- CMOS Metal Gate for High Reliability



L SUFFIX
CERAMIC PACKAGE
CASE 726

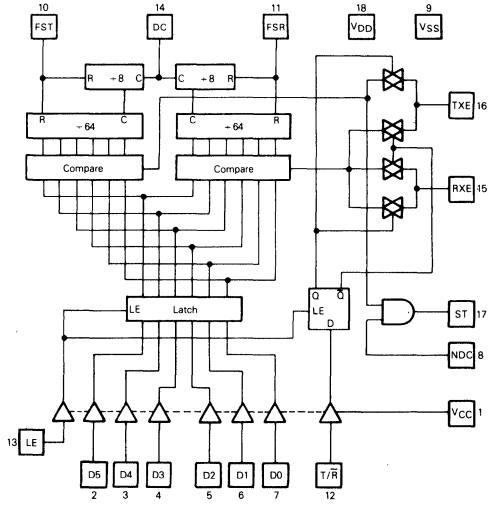


P SUFFIX
PLASTIC PACKAGE
CASE 707

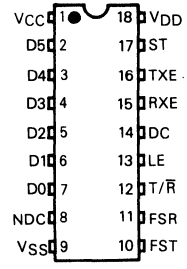
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Level Shift Voltage	V_{CC}	−0.5 to V_{DD}	V
Input Voltage Inputs Referenced to V_{DD} to V_{CC}	 V_{in1} V_{in2}	 −0.5 to V_{DD}+0.5 −0.5 to V_{DD}+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +165	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

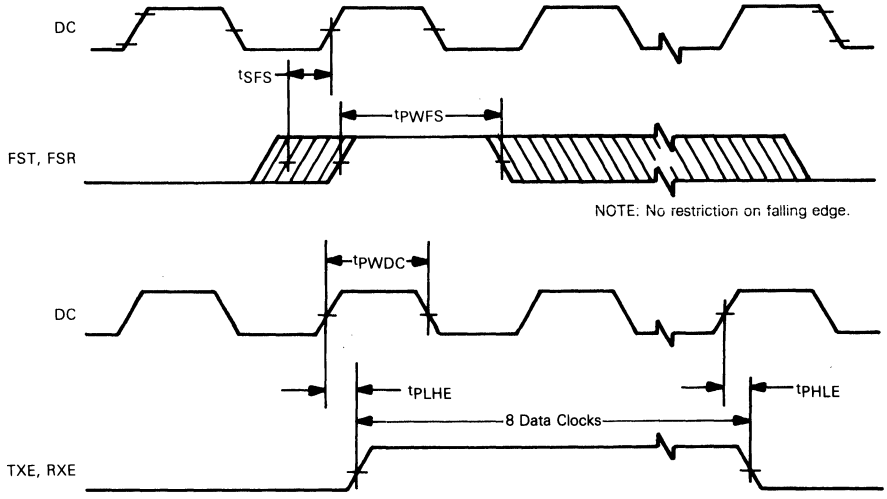
Characteristic		Symbol	V_{DD}	Min	Typ	Max	Unit
DC Supply Voltage, V_{SS} = 0 V		V_{DD}	–	4.5	12	16	V
DC Supply Voltage, V_{SS} = 0 V		V_{CC}	–	4.5	5	V_{DD}	V
Output Current TXE, RXE, ST (V_{OL} = 0.4 V) (V_{OL} = 1.0 V)		I_{OL}	 5 12	 0.51 2.0	 – 4.0	 – –	mA
 (V_{OH} = 4.6 V) (V_{OH} = 11.0 V)		I_{OH}	 5 12	 −0.2 −2.0	 – −4.0	 – –	mA
Input Voltage (CMOS) FST, FSR, DC1, DC2, NDC	"0"	V_{IL}	5 12	– –	– –	1.0 2.4	V
	"1"	V_{IH}	5 12	4.0 9.6	– –	– –	V
Input Voltage (TTL) D0-D5, LE, T/$\overline{R}$, V_{CC} = 5 V	"0"	V_{IL}	5 12 16	– – –	– – –	0.8 0.8 0.7	V
	"1"	V_{IH}	5 12	2.0 2.0	– –	– –	V
Total Supply Current (Outputs Unloaded) DC1 at 2.048 MHz		I_T	5 12	– –	1.5 2.5	– –	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, Unless Otherwise Noted)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time, TXE, RXE, ST	t_r	5 12	– –	100 50	200 100	ns
Output Fall Time, TXE, RXE, ST	t_f	5 12	– –	100 50	200 100	ns
Frame Sync Setup Time (See Figure 1)	t_{SFS}	5 12	−150 −75	– –	+150 +75	ns
Frame Sync Pulse Width	t_{PWFS}	5 12	200 100	– –	– –	ns
Propagation Delay (Note 1) DC1 to TXE, DC2 to RXE, C_L = 20 pF	t_{PHLE}, t_{PLHE}	5 12	– –	130 80	180 125	ns
Data Clock Frequency	f_{DC}	5 12	– –	– –	2.048 2.6	MHz
Data Clock Pulse Width at f_{DC} (Max)	t_{PWDC}	5 12	200 140	244 192	293 260	ns
LE Pulse Width	t_{PWLE}	5 12	1 1	– –	– –	μs
NDC to ST Propagation Delay		5 12	– –	– –	120 80	ns
FST to ST Propagation Delay		5 12	– –	– –	200 130	ns

NOTE 1: For time slot 0, t_{PHLE} and t_{PLHE} are measured from the leading edge of DC or FST (FSR), whichever occurs last.

FIGURE 1 — TIMING DIAGRAMS



PIN DESCRIPTIONS

V_{CC} (Positive Supply) — The V_{CC} power supply controls the inputs LE, D0-D5 and T/$\overline{R}$. It can be supplied by any voltage from 4.5 to V_{DD}. In typical usage, V_{CC} is 5 volts for TTL or microprocessor compatibility of the control inputs to the TSAC while V_{DD} and V_{SS} are connected to the Codec supplies.

D5-D0 (Parallel Time Slot Data Inputs) — The six inputs to the input-storage latch are the time-slot data. D0 is the least-significant bit while D5 is the most-significant. The binary word at this input represents the number of 8 bit time slots from FST and FSR where TXE and RXE will occur, respectively. These can be 5-volt input compatible with TTL and are internally level shifted to the V_{DD} supply.

LE (Latch Enable Input with Internal Pull-Up) — This input allows the data D0 through D5 and T/$\overline{R}$ bits to be latched in the input-storage latch. If LE is held high, then the inputs to the latch are combinational and directly applied to the compare circuits. When LE is pulled low, the input values applied at D0 through D5 and T/$\overline{R}$ are latched and held in the storage latch.

T/$\overline{R}$ (TXE/RXE Swap Input with Internal Pull-Up) — This input allows the TXE and RXE inputs to be swapped. When T/$\overline{R}$ is a one, the TXE output is derived from FST and RXE from FSR. If T/$\overline{R}$ is a zero, the derivation is reversed. If FST and FSR are eight data clocks apart, then two TSAC channels programmed to the same D0 through D5 and different T/$\overline{R}$ bits will create a completed conversation. This feature is intended for use in simplifying small-key systems.

DC (Data Clock Input) — The data clock input establishes the bit rate for the TSAC. This is typically 1.544 or 2.048 MHz but can be any frequency up to 2.56 MHz. The data clock is divide-by-8 for both transmit- and receive-time slots. The data clock input is a CMOS compatible input between V_{DD} and V_{SS}.

FST (Frame Sync Transmit Input) — This input identifies the beginning of the zero-transmit time slot by resetting the divide-by-8 and divide-by-64 counters. FST is a CMOS compatible input between V_{DD} and V_{SS}. The TXE output will begin and end on one 8-bit word boundary which is synchronized with the FST input. The FST signal should be aligned with the leading edge of data clock and is typically 8 kHz.

FSR (Frame Sync Receive Input) — The FSR input provides the same functions for the RXE output as FST did for TXE. The FSR and FST inputs can be any number of data clocks different, or can be the same.

TXE, RXE (Transmit-Enable and Receive-Enable Outputs) — These outputs are used to control the transmitting and receiving of data words to and from Codecs. Each output swings from V_{DD} to V_{SS} and is eight data clocks long. TXE and RXE go high at the beginning of the programmed time slot and low at the end. TXE is derived from FST and RXE is derived from FSR, provided the T/$\overline{R}$ bit is high.

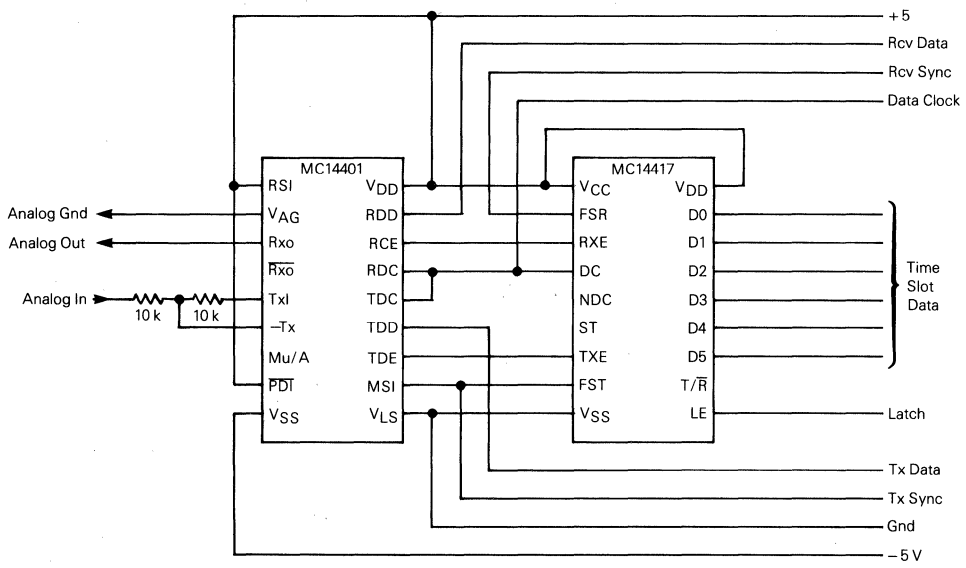
ST (Strobe Output) — The strobe output is provided to allow simplified input data storage or off-hook multiplexing control. ST is the logical AND of an enable signal (NDC) and the TXE time slot period. Thus, ST can only be high during a programmed TXE time slot. Since no other TSAC in a bank can have the same TXE programming, the ST output on any TSAC can be used to uniquely identify that TSAC by a pulse input on NDC. In many applications ST is used to control the LE input.

NDC (New Data Clock Input with Internal Pull-Up) — This input can be used in conjunction with ST to strobe data into a TSAC bank. NDC can be used to enable the strobe output.

V_{DD}, V_{SS} — The TSAC will operate from any single supply from 4.5 to 16 volts. The TSAC can be used in a 5-volt-only system by making both V_{CC} and V_{DD} 5 volts.

2

FIGURE 2 — MOTOROLA MONO-CIRCUIT/TSAC COMBINATIONS



The MC14417 TSAC offers simple flexible time slot assignment for the PCM mono-circuit. Assignments are wired or latched into the data port. The MC14401 offers supply flexibility of ±5, ±6, +12, or +10 V with 18 pin packages and TTL compatibility.

MC14419

2-OF-8 KEYPAD-TO-BINARY ENCODER

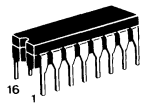
The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 × 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

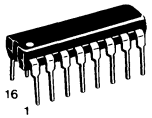
- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0-9 Produce a Strobe Pulse
- One Key Rollover Feature

CMOS
(LOW-POWER COMPLEMENTARY MOS)

2-OF-8 KEYPAD-TO-BINARY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620



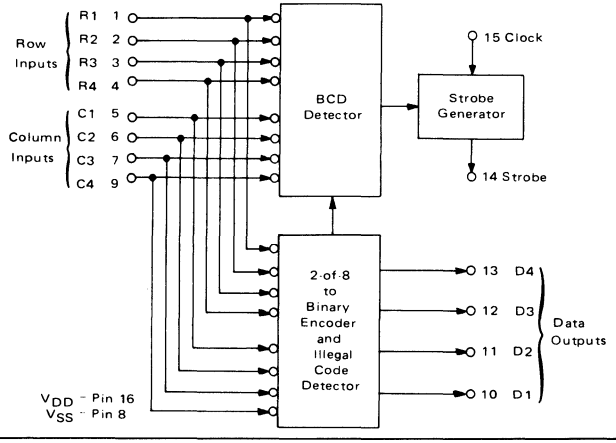
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

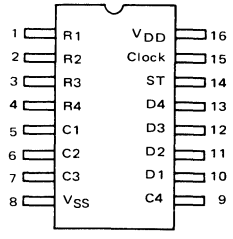
MC14XXX_

Suffix	Denotes
L	= Ceramic
P	= Plastic

BLOCK DIAGRAM



PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

2

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage Operating Range	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
Noise Immunity ($\Delta V_{out} \leq 0.8$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Leakage Current ($V_{in} = V_{DD}$)	I_{IH}	5.0	–	–	–	10	–	–	–	pAdc
Pullup Resistor Source Current (Row and Column Inputs) ($V_{in} = V_{SS}$)	I_{IL}	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance ($V_{in} = V_{SS}$)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Standby Supply Current (f_{clock} = 16 kHz, No Keys Depressed)	I_{DDS}	3.0	–	3.0	–	1.0	3.0	–	6.0	μAdc
		5.0	–	15	–	5.0	15	–	30	
		6.0	–	60	–	20	60	–	120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	I_{DDS}	5.0	I_{DDS} = 0.09 μA/kHz + 3.0 μA							μAdc

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	t_r,t_f	5.0	–	300	–	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	–	1000	–	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	4.0	16	80	kHz

FIGURE 1 – SWITCHING TIME WAVEFORMS

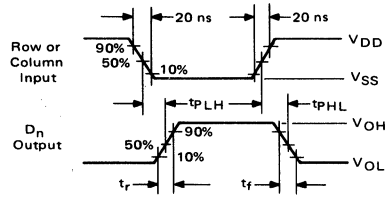
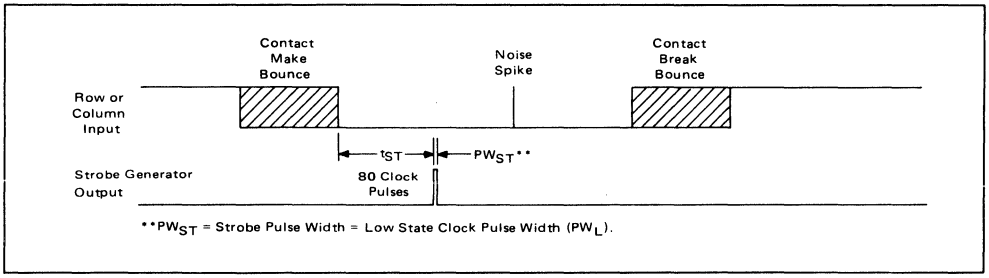


FIGURE 2 – TYPICAL STROBE PULSE DELAY TIMES

PRF Clock Frequency kHz	t_{ST}* Strobe Pulse Delay Time ms
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*t_{ST} = (1/PRF) • 80, with PRF in kHz, t_{ST} in ms.

FIGURE 3 – STROBE GENERATOR TIMING DIAGRAM



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

TRUTH TABLE

	Inputs								Outputs				
	Row				Column								
Key**	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	⎍
2	1	1	1	0	1	1	0	1	0	0	1	0	⎍
3	1	1	1	0	1	0	1	1	0	0	1	1	⎍
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	⎍
5	1	1	0	1	1	1	0	1	0	1	0	1	⎍
6	1	1	0	1	1	0	1	1	0	1	1	0	⎍
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	1	1	0	0	1	1	1	⎍
8	1	0	1	1	1	1	0	1	1	0	0	0	⎍
9	1	0	1	1	1	0	1	1	1	0	0	1	⎍
C	1	0	1	1	0	1	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	⎍
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 4 for keypad designation.

2

FIGURE 4 – TYPICAL KEYPAD INTERFACE APPLICATION

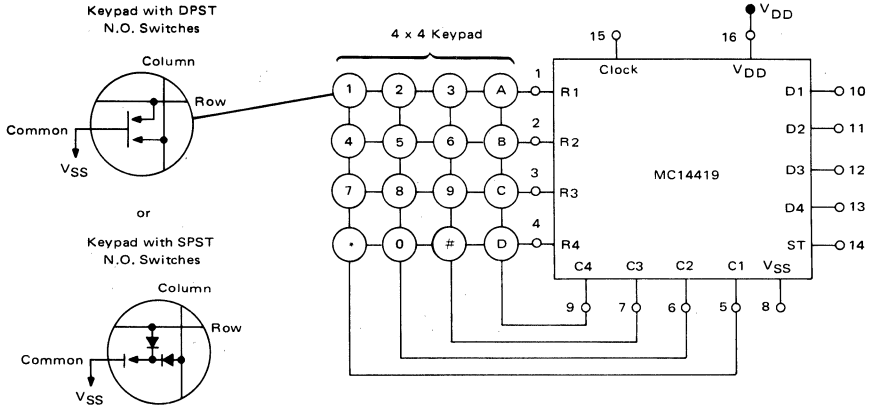
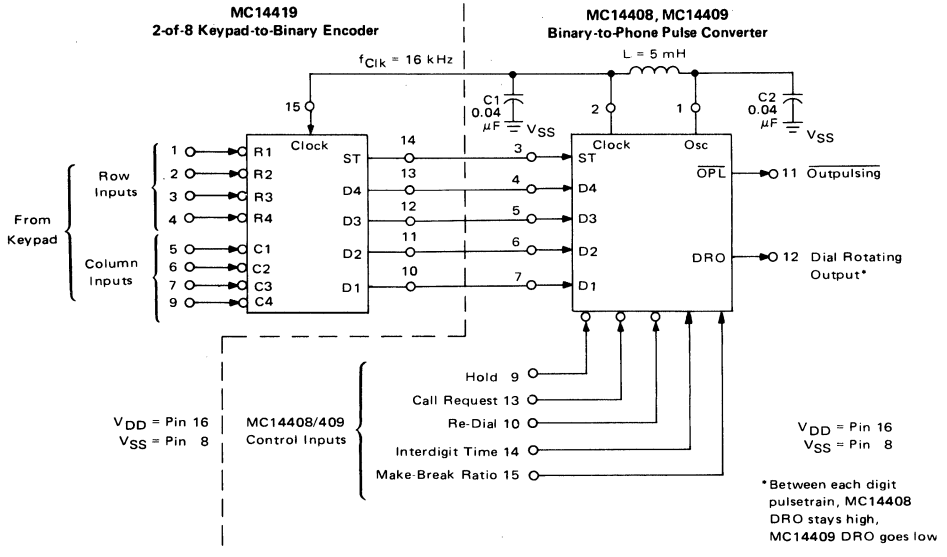


FIGURE 5 – PHONE DIALER SYSTEM



MC33120

Product Preview

SUBSCRIBER LOOP INTERFACE CIRCUIT

The MC33120 is designed to provide the interface between the 4-wire side of a central office, or PBX, and the 2-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, hookswitch detection, adjustable transmit, receive and transhybrid gains, ground key and single/double fault indication. Additionally, the MC33120 provides a minimum of 58 dB of longitudinal balance.

The transmit and receive signals are referenced to analog ground (VAG), easing the interface to codecs, filters, etc. The two Status outputs (Hook Status and Faults) and the Power Down Input are TTL and CMOS compatible. The Power Down Input permits local control of the circuit.

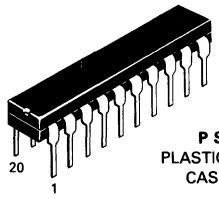
Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC33120 will be available in both a 20-pin DIP and a 20-pin surface mount (SOIC) package.

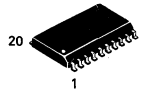
- 58 dB Longitudinal Balance (Minimum)
- Transmit, Receive, and Transhybrid Gains Externally Adjustable
- Proper Hook Switch Detection with 30 kΩ Leakage
- Single and Double Fault Indication
- Critical Sense Resistors Included Internally
- Standard Power Supplies: −48 to −22 Volts, and +5.0 Volts, ±10%
- Internal Drivers for External Pass Transistors
- Power Down Input
- Available in 20-Pin DIP and 20-Pin SOIC Plastic Packages
- Operating Ambient Temperature: −40 to +85°C

SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

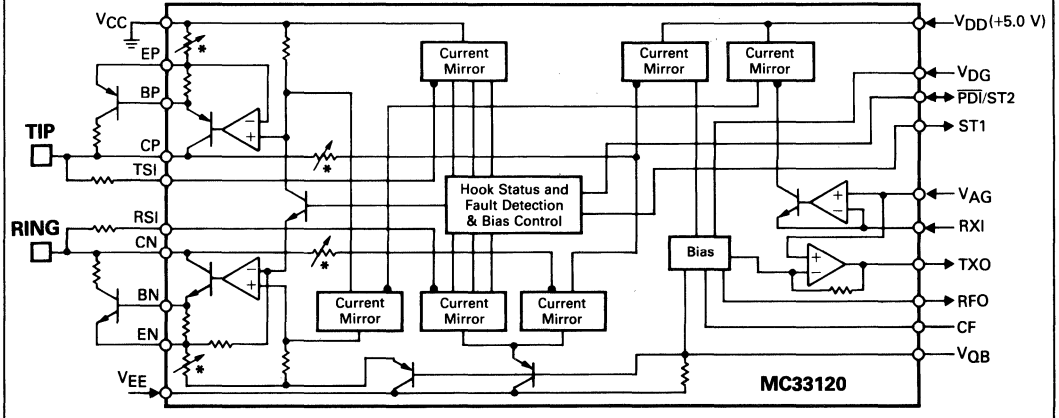
THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03



*Indicates Trimmed Resistor

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

2

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
V_{EE} Supply Voltage (w/respect to V_{CC})	−60	Vdc
V_{DD} Supply Voltage (w/respect to V_{DG})	−0.5, +7.0	Vdc
Input Voltage at $\overline{PDI}$ (w/respect to V_{DG})	−0.5, +7.0	Vdc
Voltage at Pins 1–5, 16–20	V_{CC} to V_{EE}	Vdc
Junction Temperature	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
V_{EE} Supply Voltage (w/respect to V_{CC})	V_{EE}	−58	−48	−22	Vdc
V_{DD} Supply Voltage (w/respect to V_{DG})	V_{DD}	+4.5	+5.0	+5.5	Vdc
V_{AG} Voltage (w/respect to V_{CC})	V_{AG}	−2.0	0	+2.0	Vdc
V_{DG} Voltage (w/respect to V_{CC})	—	−2.0	—	+7.0	Vdc
V_{DD} Voltage (w/respect to V_{EE})	—	—	—	63.5	Vdc
V_{DD} Voltage (w/respect to V_{CC} and V_{AG})	—	+3.5	—	—	Vdc
PDI Input Voltage	V_{PDI}	0	—	V_{DD}	Vdc
$\overline{PDI}$ Input Sink Current (PDI ≤ 0.8 V)	I_{PDI}	0	—	1.0	mA
Tx, Rx Signal Level	—	−48	—	+3.0	dBm
Loop Resistance (V_{EE} = −48 V, I_L = 20 mA)	R_L	0	—	1900	Ω
Ambient Temperature	T_A	−40	—	+85	°C

All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = −48 V, V_{DD} = +5.0 V, unless noted, See Figure 1, V_{AG} = V_{DG} = V_{CC})

Parameter	Min	Typ	Max	Units
On-Hook Supply Current (R_L > 10 MΩ) I_{EE} @ V_{EE} = −56 Volts I_{DD} @ V_{DD} = +5.5 Volts	 — —	 −1.0 2.5	 — —	mA
Off-Hook Supply Current (Includes loop current, R_L = 0) I_{EE} @ V_{EE} = −56 Volts I_{DD} @ V_{DD} = +5.5 Volts	 — —	 −46 10	 — —	mA
Loop Resistance On-Hook Threshold	—	6.3	—	kΩ
Loop Resistance Off-Hook Threshold	—	2.7	—	kΩ
Off-Hook Loop Current Limit (RRF = 6200 Ω, R_L = 0)	—	34	—	mA
$\overline{PDI}$ Input Voltage (Power Down Control) — High — Low	2.0 —	— —	— 0.8	Vdc
ST2 Output Voltage — High (I = −100 μA) — Low (I = 1.0 mA)	2.4 —	— —	— 0.4	Vdc
ST1 Output Voltage — High (I = −100 μA) — Low (I = 1.0 mA)	2.4 —	— —	— 0.4	Vdc
$\overline{PDI}$ Input Current (@ 3.0 Volts, R_L = 600 Ω)	—	−100	—	μA
V_{AG} Input Current	—	1.0	—	μA
TXO Offset Voltage (w/respect to V_{AG})	−150	0	+150	mV
TXO Output Current	—	±500	—	μA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = −48 V, V_{DD} = +5.0 V, f = 1.0 kHz, see Figure 1, V_{AG} = V_{DG} = V_{CC})

Parameter	Min	Typ	Max	Units
Transmit Voltage Gain (Pins 4, 17 to Pin 11)	—	0.33	—	V/V
Receive Current Gain (I_{EP}/I_{RXI})	—	102	—	mA/mA
Tx & Rx Gain Variations versus Frequency (3.4 kHz versus 1.0 kHz)	−0.1	0	+0.1	dB
Tx & Rx Gain Variations versus Signal Level (−48 dBm to +3.0 dBm)	−0.1	0	+0.1	dB
2-Wire Longitudinal Impedance (Tip to Ground, Ring to Ground) (R_S = 6.8 k)	—	144	—	Ω
Power Supply Rejection Ratio (V_{TXO}/V_{EE}, C_{QB} = 10 μF)	40	—	—	dB
Power Supply Rejection Ratio (V_{TXO}/V_{DD}, C_{QB} = 10 μF)	40	—	—	dB

SYSTEM SPECIFICATIONS (T_A = 25°C, V_{EE} = −48 V, V_{DD} = +5.0 V, f = 1.0 kHz, see Figure 2, V_{AG} = V_{DG} = V_{CC})

Parameter	Min	Typ	Max	Units
Off Hook Loop Current Limit (R_{RF} = 6200 Ω, R_L = 0)	—	34	—	mA
DC Feed Resistance (R_{RF} = 6200 Ω, R_L >1000 Ω)	—	335	—	Ω
2-Wire Return Loss	30	—	—	dB
Transhybrid Rejection (V_{TX}/V_{RX})	—	−35	—	dB
Transmit Voltage Gain (V_{TX}/V_L)	—	0	—	dB
Receive Voltage Gain (V_L/V_{RX})	—	0	—	dB
2-Wire Longitudinal Balance @ 300 Hz (V_{TIP} − V_{RING}/V_{LONG}) @ 1.0 kHz @ 3000 Hz	−58 −58 −53	−64 −64 −60	— — —	dB
4-Wire Longitudinal Balance @ 300 Hz (V_{TXS}/V_{LONG}) @ 1.0 kHz @ 3000 Hz	−58 −58 −53	−64 −64 −60	— — —	dB
Idle Channel Noise @ TXO (w/C-message Filter)	—	2.0	—	dBrnC
Idle Channel Noise @ Tip/Ring (w/C-message Filter)	—	0	—	dBrnC

PIN DESCRIPTION

Symbol	Pin No.	Description
V_{CC}	20	Connect to system ground. Carries all loop current and some bias current.
V_{DD}	15	Connect to +5.0 volt, ±10% supply.
V_{EE}	1	Connect to negative supply (−58 to −22 volts, typically −48 volts).
CP, BP, EP	17–19	Connect to external PNP transistor which passes loop current to TIP.
TSI, RSI	16, 5	Sense inputs. Connect to external sense resistors to TIP and RING.
EN, BN, CN	2–4	Connect to external NPN transistor which passes loop current from RING.
V_{DG}	14	Ground pin for the digital section (normally connected to V_{CC}).
$\overline{PDI}$/ST2	12	A Power Down Input, AND a Status output. Used with ST1 to indicate hook status and single/double faults. TTL/CMOS compatible.
ST1	13	Status Output. Used with ST2 to indicate hook status and single/double faults. TTL/CMOS compatible.
V_{AG}	9	System AC signal ground (normally connected to V_{CC}).
RXI	10	Receive signal current input. Return loss network connects between here and TXO.
TXO	11	Transmit voltage signal output (to a Codec/filter).
RFO	8	Connect to external resistor to set the current limit value.
CF	7	Connect to external capacitor to filter AC from the DC feed circuit.
V_{QB}	6	Quiet Battery. Filtering this pin will reduce power supply noise at the speech paths.

2

FIGURE 1 — TEST CIRCUIT

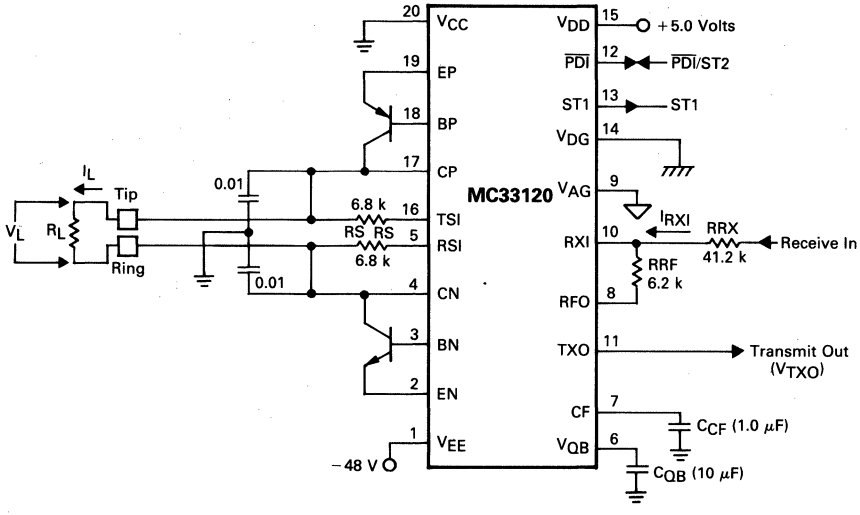
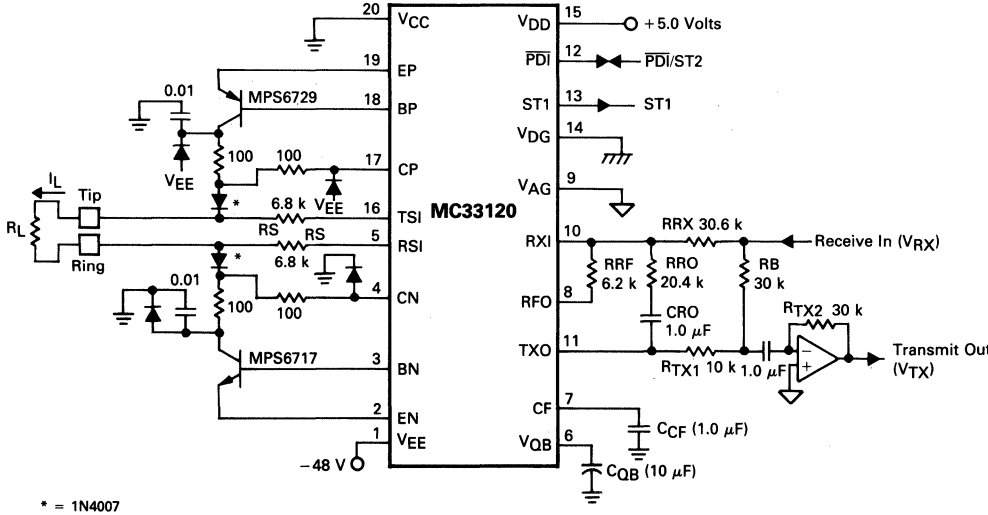
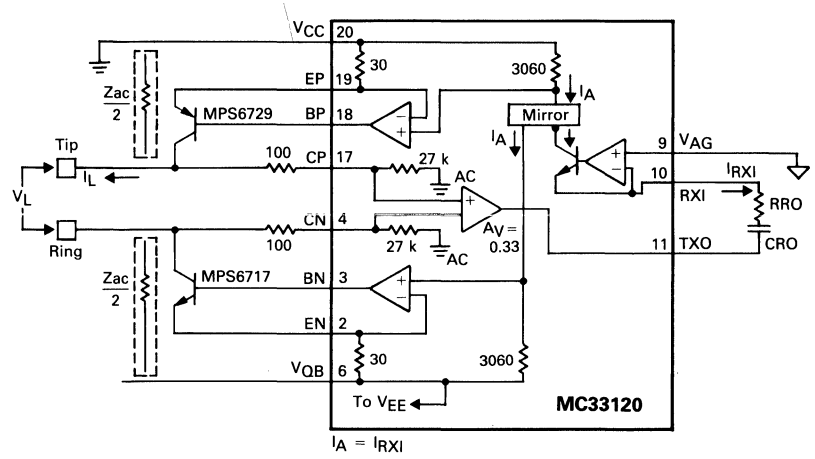


FIGURE 2 — APPLICATION CIRCUIT



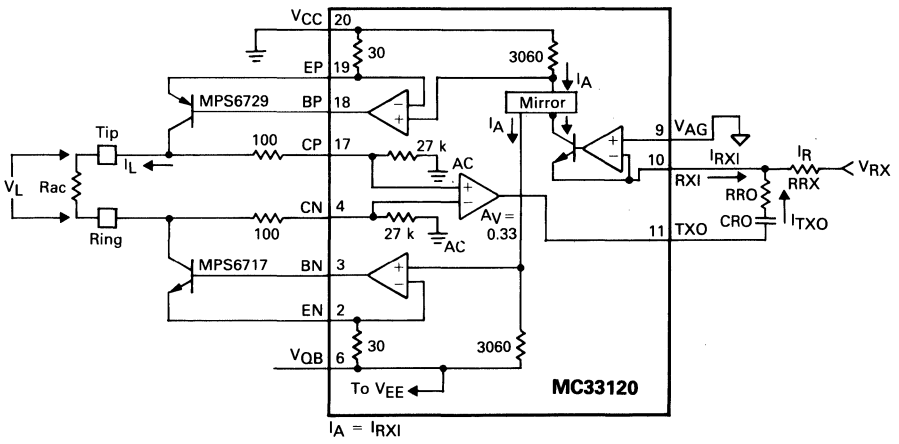
* = 1N4007
Component values shown for a 600 Ω system.

FIGURE 3 — AC TERMINATING IMPEDANCE AND SOURCE IMPEDANCE (Zac)



Note: ⏚ AC represents an AC virtual ground, not an actual ground connection.
The circuit creates a synthesized impedance (Zac/2) from Tip to V_{CC}, and from Ring to V_{QB} as follows:
— An incoming signal (V_L) produces a differential voltage at CP and CN, which produces a signal of $V_L/3$ at TXO.
— The signal at TXO creates a current I_{RXI} through RRO (pin 10 is a virtual ground).
— I_{RXI} is gained up by a factor of 102 to produce the I_L to Tip & Ring.
— Zac (defined as V_L/I_L) is therefore determined by RRO, and is equal to *RRO/34* (first order).
— For 600 Ω systems, RRO = 20.4 kΩ; for 900 Ω systems, RRO = 30.6 kΩ.
— For more precise determination of Zac, consider the following:
1) The effects of CRO in determining I_{RXI} (Zac increases as the frequency is decreased).
2) The RS resistors at pins 5 & 16 (not shown above, see Figure 2) which are in parallel with the Zac/2 resistors shown above;
3) The voltage divider effect of the 100 Ω and 27 kΩ resistors.

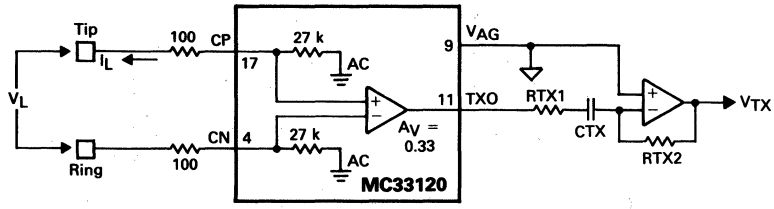
FIGURE 4 — RECEIVE GAIN (G_{RX})



Receive Gain (voltage gain from V_{RX} to V_L) is calculated as follows:
— RXI (pin 10) is a virtual ground, Rac is the AC impedance of the load (typically 600 Ω or 900 Ω).
— $I_L = 102 \times I_{RXI} = 102 \times (I_R - I_{TXO})$
— $I_R = V_{RX}/RRX$, and
— $I_{TXO} = V_{TXO}/RRO = \dfrac{V_L}{3 \times RRO}$
— $\therefore \dfrac{V_L}{V_{RX}} = G_{RX} = \dfrac{102 \times Rac}{RRX\left(1 + \dfrac{34\ Rac}{RRO}\right)}$ (first order)
— Since Zac = RRO/34 (see Figure 3) $G_{RX} = \dfrac{102 \times Rac}{RRX\left(1 + \dfrac{Rac}{Zac}\right)}$
— To obtain G_{RX} = 0 dB, set RRX = 51 Rac (for the case where Rac = Zac).
∴ RRX = 30.6 kΩ for 600 Ω systems, 45.9 kΩ for 900 Ω systems.
— The AC source impedance to Tip and Ring of the above circuit is Zac.
— For more precise determination of the receive gain, consider the following:
1) The effect of CRO in determining I_{TXO} (G_{RX} increases as frequency is decreased).
2) The RS resistors at pins 5 & 16 (not shown above, see Figure 2) each of which are in parallel with half of the Zac term.
3) The voltage divider effect of the 100 Ω and 27 kΩ resistors.

2

FIGURE 5 — TRANSMIT GAIN (G_{TX})



Transmit Gain (voltage gain from V_L to V_{TX}) is calculated as follows:

— $\frac{V_{TX}}{V_L} = G_{TX} = \frac{RTX2}{R_{TX1} \times 3}$ (first order)

— For 0 dB gain, make R_{TX2} = 3 RTX1

— TXO (pin 11) can source and sink 500 μA.

— CTX can be used to set low frequency roll-off.

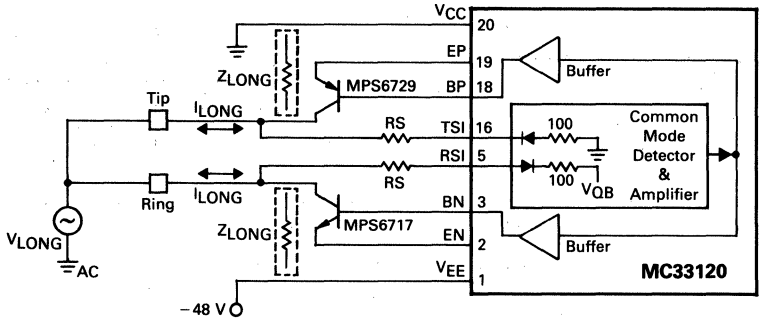
— The op amp may be part of a codec/filter.

— The terminating impedance to the source voltage (V_L) is Zac (see Figure 3).

— For a more precise determination of the transmit gain, consider the following:

1) The effects of CTX on the gain of the op amp (G_{TX} will increase as frequency is increased).
2) The voltage divider effect of the 100 Ω and 27 kΩ resistors.

FIGURE 6 — LONGITUDINAL IMPEDANCE (Z_{CM})



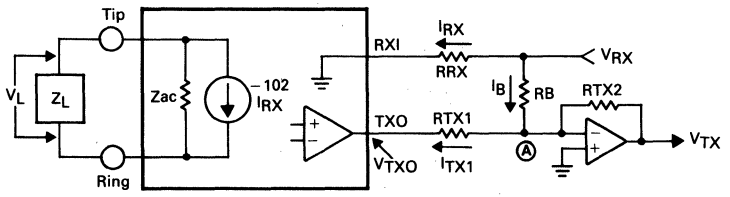
— The longitudinal impedance, defined as V_{LONG}/I_{LONG}, is determined by R_S according to: $Z_{LONG} = \frac{R_S}{47}$

— For R_S = 6.8 kΩ, Z_{LONG} = 144 Ω.

FIGURE 7 — CALCULATION OF THE BALANCE NETWORK (RB) FOR PROPER TRANSHYBRID LOSS

METHOD A

— The appropriate part of the circuit is modeled as follows:



Given:

— Z_L is the AC load impedance. Zac was previously calculated (see Figure 3).

— $I_{RX} = V_{RX}/RRX$; $I_B = V_{RX}/RB$

— $V_{TXO} = V_L/3$; $I_{TX1} = V_{TXO}/RTX1 = V_L/(3 \times RTX1)$

— $I_{TX1} = \frac{102\ I_{RX} \times Zac \times Z_L}{[Zac + Z_L] \times 3 \times RTX1} = \frac{102 \times V_{RX} \times Zac \times Z_L}{RRX \times [Zac + Z_L] \times 3 \times RTX1}$

— Good transhybrid loss requires that $I_B = I_{TX1}$ in both magnitude and phase at node Ⓐ.

For the case where Z_L is purely resistive the above equations reduce to:

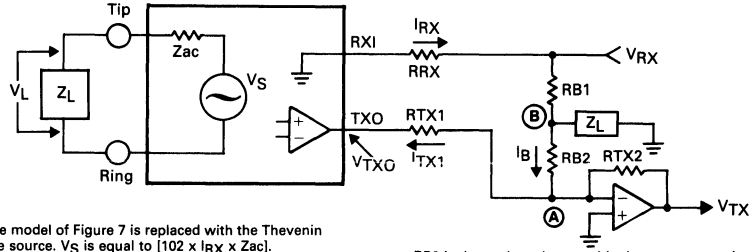
$$RB = \frac{RRX \times RTX1}{34 \times [Zac//Z_L]}$$

— Since Z_L is rarely purely resistive, a phase shift results between V_{RX} and V_{TXO}, which requires that RB be a complex network which creates a comparable phase shift for I_B. The following method is a fairly direct and simple way to design a balance network, but requires more external components than Method B.

FIGURE 8 — CALCULATION OF THE BALANCE NETWORK (RB) FOR PROPER TRANSHYBRID LOSS — Continued

METHOD A

— First, the Model in Figure 7 is changed to:



— The current source model of Figure 7 is replaced with the Thevenin equivalent voltage source. V_S is equal to [102 x I_{RX} x Zac].
— RB is replaced with two series resistors (RB1 and RB2), and a network (Z_L) which is identical in configuration and component values to the load Z_L.
— RB1 is set equal to Zac (calculated in Figure 3). This creates a phase shift at node (B) equal to the phase shift at V_L (with respect to V_{RX}), and consequently at V_{TXO}.
— RB2 is then selected to provide the proper magnitude for I_B, and is calculated from:

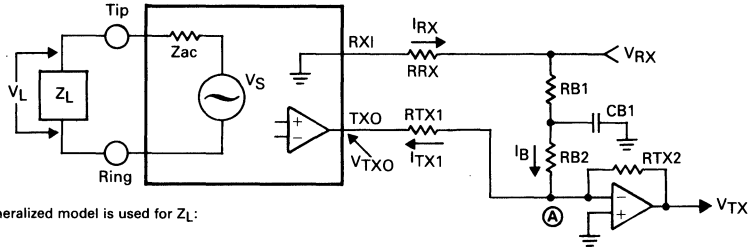
$$RB2 = \frac{RRX \times RTX1}{34 \times Zac}$$

— If Zac had been intentionally made complex, RB1 and RB2 must also be complex.

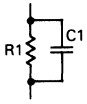
FIGURE 9 — CALCULATION OF THE BALANCE NETWORK (RB) FOR PROPER TRANSHYBRID LOSS

METHOD B (EXAMPLE A)

— The following model is used:



— The following generalized model is used for Z_L:



$$Z_L = \frac{R1 - j\,(\omega\ C1\ R1^2)}{[1 + (\omega\ C1\ R1)^2]}$$

— At this point, it is beneficial to calculate the magnitude for Z_L, and the phase angle (θ_L) with respect to V_{RX}, at a frequency of interest (usually 1.0 kHz), and use these calculated values in subsequent equations.

$$Z_L\ (mag) = \frac{\sqrt{\left[R1\right]^2 + \left[(\omega\ C1\ R1^2)\right]^2}}{[1 + (\omega\ C1\ R1)^2]}$$

— The phase angle across Z_L with respect to V_{RX} is created by Z_L's reactive component in conjunction with Zac. The phase angle is calculated by:

$$\theta_L = \left[\text{Tan}^{-1}\ \omega\ C1\ R1\right] - \left[\text{Tan}^{-1}\ \frac{(\omega\ C1\ R1^2)}{Zac\ [1 + (\omega\ C1\ R1)^2] + R1}\right]$$

— In the RB network (RB1, RB2, CB1), I_B is equal to:

$$I_B = \frac{V_{RX}}{(RB1 + RB2) + j\,(\omega\ CB1\ RB1\ RB2)}$$

— As shown in Method A, I_{TX1} is equal to:

$$I_{TX1} = \frac{V_{RX} \times 34 \times Z_L \times Zac}{RTX1 \times RRX \times (Zac + Z_L)}$$

— Good transhybrid loss requires that $I_B = I_{TX1}$ in both magnitude and phase at node (A).
(Note: The values of θ_L and Z_L (mag) calculate above, and the value of ω used in those calculations must be used in the remaining equations):

$$I_B\ (mag) = \frac{V_{RX}}{\sqrt{(RB1 + RB2)^2 + (\omega\ CB1\ RB1\ RB2)^2}}$$

$$I_B\ (phase) = \theta_B = \text{Tan}^{-1}\ \frac{(\omega\ CB1\ RB1\ RB2)}{(RB1 + RB2)} = \theta_L$$

$$\text{Therefore } \sqrt{(RB1 + RB2)^2 + (\omega\ CB1\ RB1\ RB2)^2} = \frac{RTX1 \times RRX \times (Zac + Z_L)}{34 \times Z_L \times Zac}$$

— To facilitate the remaining equations, the condition (C1 x R1) = (CB1 x RB2) is arbitrarily set.
— Combining the above equations yields:

$$RB1 = \left(\frac{RTX1 \times RRX \times (Zac + Z_L)}{34 \times Z_L \times Zac \times (\omega\ C1\ R1)}\right)\left(\frac{\text{Tan}\ \theta_L}{\sqrt{1 + \text{Tan}^2\theta_L}}\right)$$

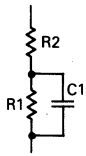
$$RB2 = \left(\frac{\omega\ C1\ R1\ RB1}{\text{Tan}\ \theta_L}\right) - RB1$$

$$CB1 = \frac{C1 \times R1}{RB2}$$

FIGURE 10 — CALCULATION OF THE BALANCE NETWORK (RB) FOR PROPER TRANSHYBRID LOSS

METHOD B (EXAMPLE B):

— For the case where the load Z_L has the following form:



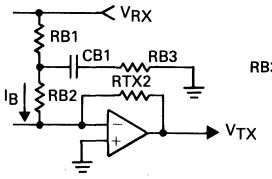
$$Z_L = \frac{R1 + R2\,[1 + (\omega\,C1\,R1)^2] - j\,(\omega\,C1\,R1^2)}{[1 + (\omega\,C1\,R1)^2]}$$

— The following equations are used to calculate Z_L (mag) and θ_L.

$$Z_L\,(mag) = \frac{\sqrt{\left[R1 + R2\,[1+(\omega\,C1\,R1)^2]\right]^2 + \left[(\omega\,C1\,R1^2)\right]^2}}{[1 + (\omega\,C1\,R1)^2]}$$

$$\theta_L = \left[\text{Tan}^{-1}\frac{(\omega\,C1\,R1^2)}{R1 + R2[1+(\omega\,C1\,R1)^2]}\right] - \left[\text{Tan}^{-1}\frac{(\omega\,C1\,R1^2)}{R1 + [R2 + Zac][1 + (\omega\,C1\,R1)^2]}\right]$$

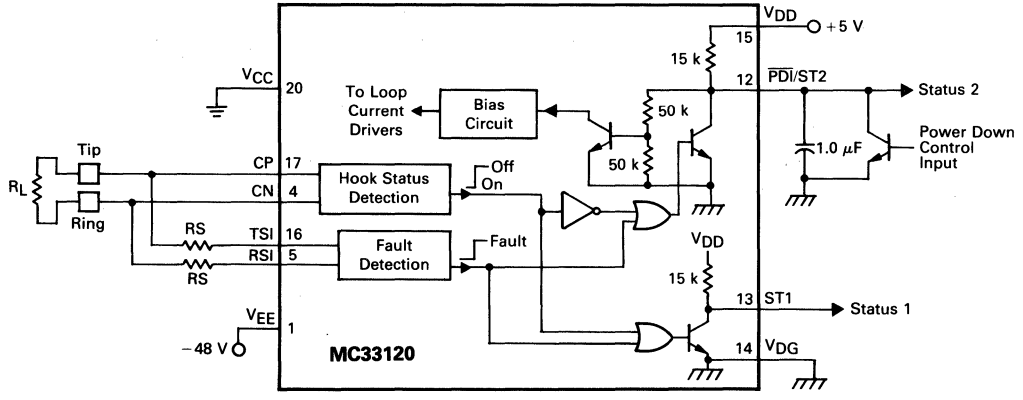
— The same equations shown in Example A for RB1, RB2, and CB1 can be used to calculate those component values. This will generally yield good results at the frequency used in the above calculations, but will degrade at other frequencies. To obtain more consistent performance in this case, a resistor (RB3) must be added in series with CB1. This adds a zero to I_B's frequency response, thereby matching Z_L's frequency response.



$$RB3 = \frac{C1 \times R1 \times R2}{CB1 \times (R1 + R2)}$$

— The four components calculated above will yield good results for transhybrid loss. However, some minor adjustments to the component values can generally improve the loss by several dB. Generally, adjustments for maximum loss should be made in the following sequence: RB2, and then CB1 at the prime frequency or interest, and then RB3 at other frequencies.

FIGURE 11 — LOGIC INTERFACE (HOOK STATUS, FAULT INDICATIONS, POWER DOWN CONTROL)



TRUTH TABLE:

Hook Status	Fault Detection	Outputs ST1	Outputs ST2	Circuit Condition
On Hook	No Fault	Hi	Lo	Internally powered down
Off Hook	No Fault	Lo	Hi	Powered up
On Hook	Fault	Lo	Lo	Internally powered down
Off Hook	Fault	Lo	Lo	Internally powered down

— On-hook and off-hook conditions are determined by the thresholds listed in the specifications.
— The condition where ST1 = ST2 = Hi may occur momentarily during the transition from off-hook to on-hook.
— The capacitor at ST2 prevents incorrect transitions during excessive longitudinal signals
— Pin 12 ($\overline{PDI}$/ST2) is both an input and output. As an output, it is used in conjunction with ST1 to indicate Hook status and faults. As an input, it may be taken low with a transistor (as shown) or an open-collector output to deny loop current to the subscriber. ST1 will still indicate hook status.
— Resistors RRF (see Figure 12) and RS (see Figure 6) affect the hook status thresholds as follows:

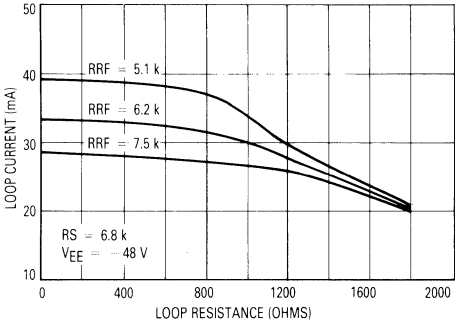
RRF	Off-On Hook Threshold
5.1 k	6.5 kΩ
6.2 k	7.7 kΩ
7.5 k	9.0 kΩ

R_S	On-Off Hook Threshold
5.1 k	4.1 kΩ
6.8 k	5.0 kΩ
10 k	6.8 kΩ

NOTE: RS does not significantly affect the Off-On Hook threshold, nor does RRF significantly affect the On-Off Hook threshold.

— Fault conditions are nominally defined as (RS = 6.8 k):
1) On-hook
   a) <3.0 kΩ between Ring and V_{CC} (no hysteresis);
   b) <4.5 kΩ between Tip and V_{EE} (no hysteresis);
   c) Both a) and b) simultaneously.
   d) Tip to V_{CC} and/or Ring to V_{EE} are not detected as faults while the MC33120 is on-hook.
2) Off-hook (R_L = 600 Ω):
   a) <60 Ω between Tip and V_{CC} (resets at ≈2.0 kΩ);
   b) <400 Ω btween Tip and V_{EE} (resets at ≈4.7 kΩ);
   c) <160 Ω between Ring and V_{EE} (resets at ≈4.7 kΩ);
   d) <150 Ω between Ring and V_{CC} (resets at ≈2.3 kΩ).

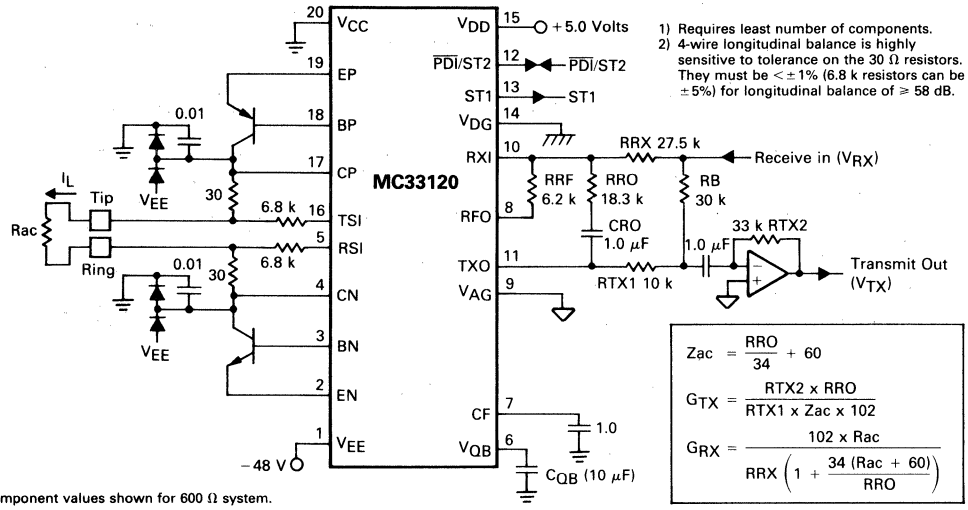
FIGURE 12 — BATTERY FEED AND CURRENT LIMIT



NOTES:
— Per the graph, varying RRF varies both the battery feed resistance and the maximum loop current.
— Between 1000 Ω and 1800 Ω loop resistance, battery feed resistance is:
  — ≈290 Ω for RRF = 5.1 k;
  — ≈335 Ω for RRF = 6.2 k;
  — ≈400 Ω for RRF = 7.5 k.
— Varying RS from 5.0 kΩ to 10 kΩ will change the maximum loop current by ≈4.0%. Varying RS has a negligible effect at 1800 Ω loop resistance.

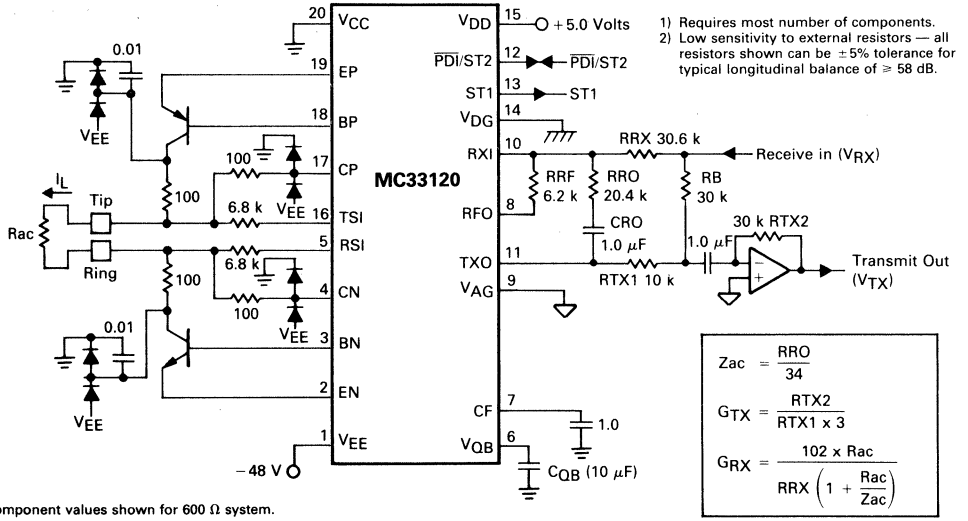
2

FIGURE 13 — ALTERNATE 2-WIRE FAULT PROTECTION CONFIGURATION



Component values shown for 600 Ω system.

FIGURE 14 — ALTERNATE 2-WIRE FAULT PROTECTION CONFIGURATION



Component values shown for 600 Ω system.

MC34010

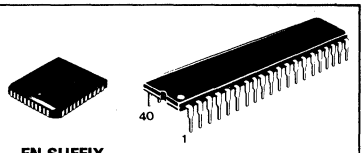
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- Microprocessor Interface Port for Automatic Dialing Features

ELECTRONIC TELEPHONE CIRCUIT

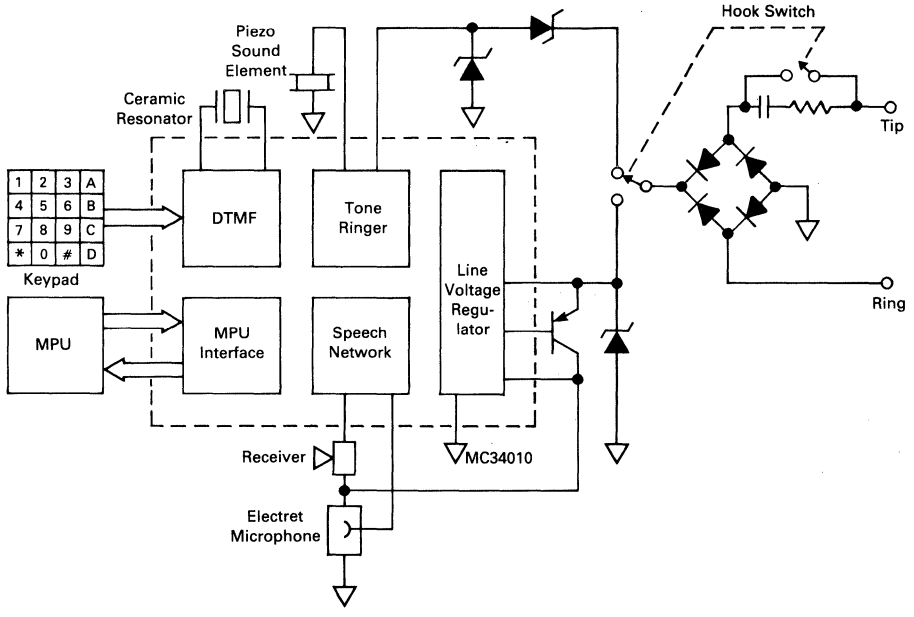
BIPOLAR LINEAR/I^2L



FN SUFFIX
44-PIN
PLCC
CASE 777-02

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

FIGURE 1 — ELEMENTS OF THE ELECTRONIC TELEPHONE



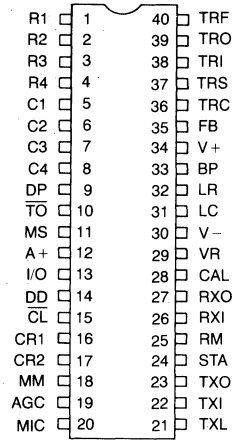
This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+20, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+	+122, −1.0	V
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



GENERAL CIRCUIT DESCRIPTION

Introduction

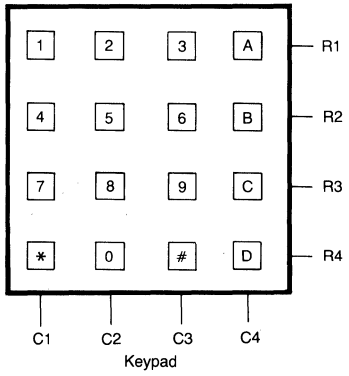
The MC34010 Electronic Telephone Circuit (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1). The MC34010 also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34010 in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

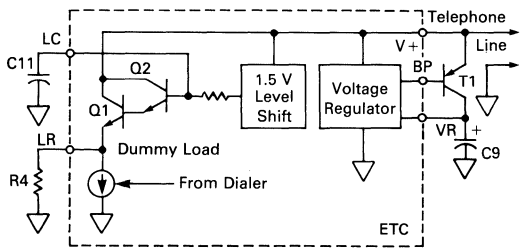
The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the

FIGURE 2 — MPU INTERFACE CODES



Key	Row	Column	Code (B3–B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

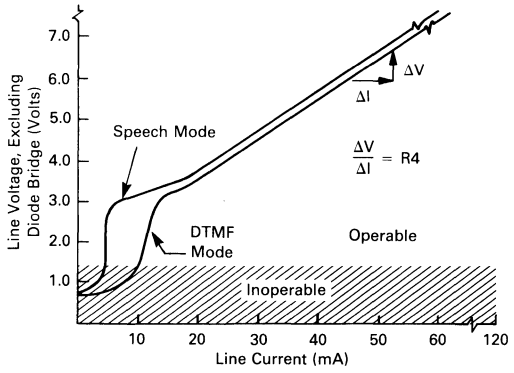
FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM



GENERAL CIRCUIT DESCRIPTION (continued)

speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34010 telephone.

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



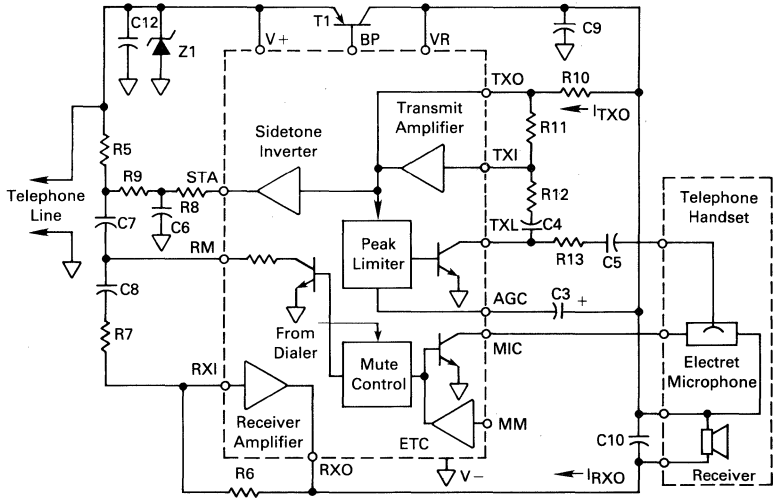
Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

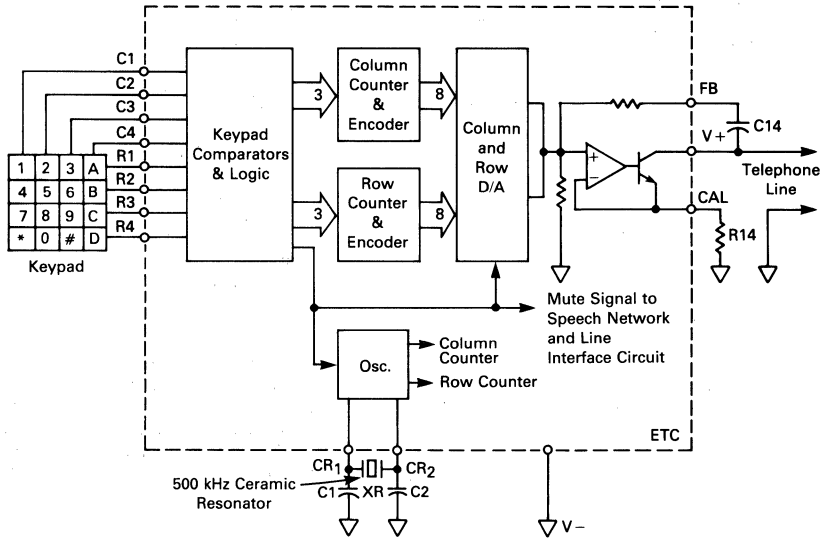
Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM



Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

Microprocessor Interface

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 2). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the microprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a Logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logic "0" to enable the DTMF generator. Figures 9 and 10 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is

depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to the microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

See Figure 45 for a typical interconnection to an MC6821 PIA (Peripheral Interface Adapter). Connection to a port on any other class of microprocessor will be similar.

FIGURE 7 — TONE RINGER BLOCK DIAGRAM

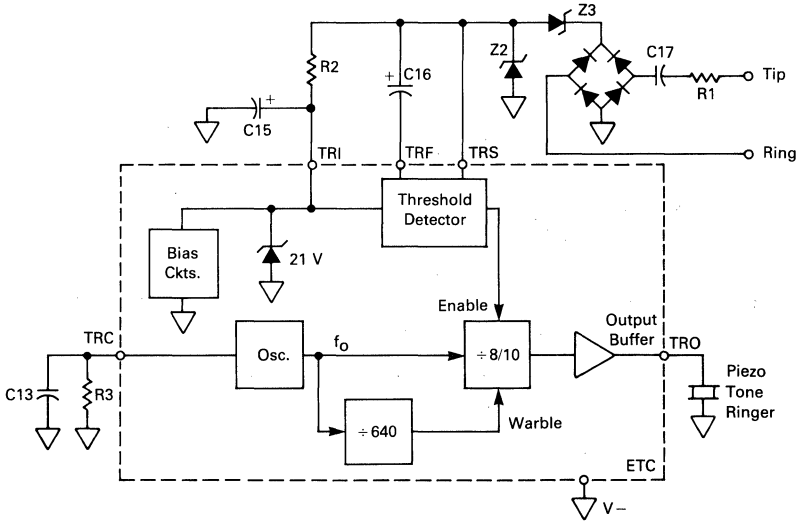


FIGURE 8 — MICROPROCESSOR INTERFACE BLOCK DIAGRAM

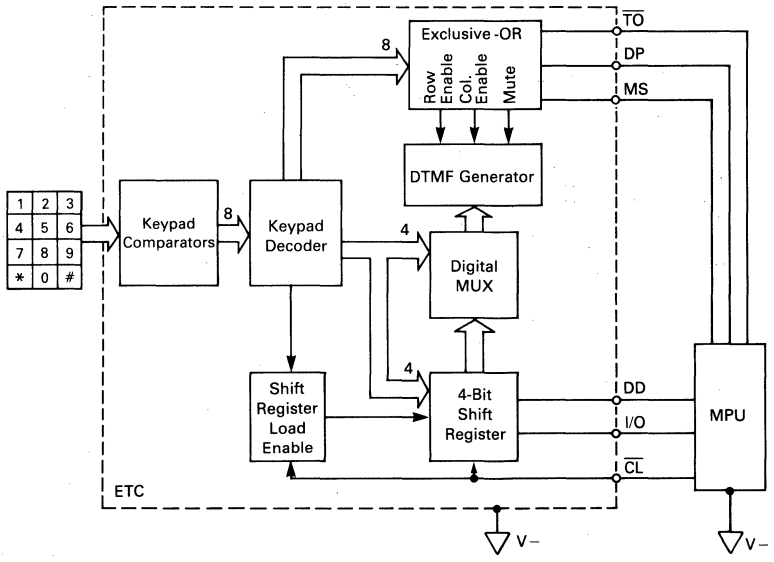


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FIGURE 9 — OUTPUT DATA CYCLE

NOTE: $\overline{TO}$ may be low (Tone generator enabled) if desired.

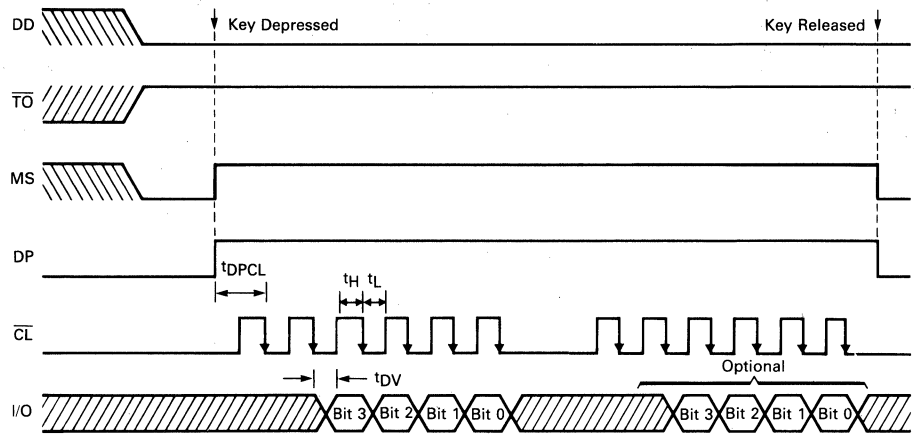


FIGURE 10 — INPUT DATA CYCLE

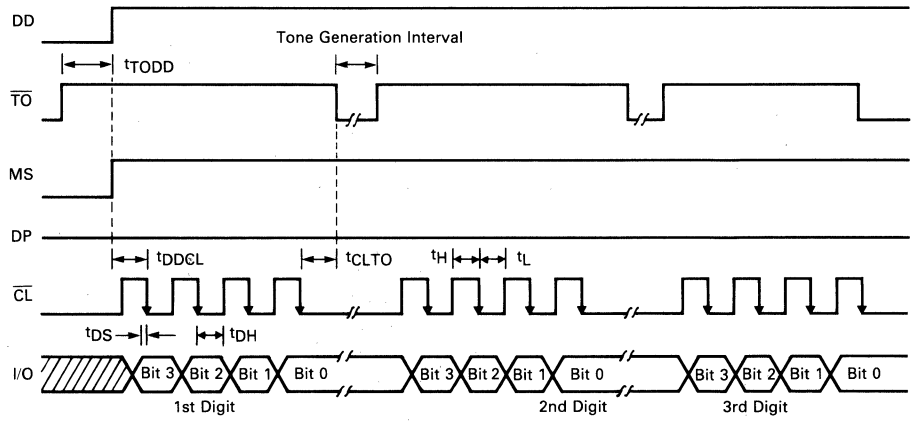


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15	—	—	μs	Figs. 9,10
t_L	Clock Low Time	15	—	—	μs	Figs. 9,10
t_r, t_f	Clock Rise, Fall Time	—	—	2.0	μs	
t_{DV}	Clock Transition to Data Valid	—	—	10	μs	Fig. 9
t_{DPCL}	Time from DP High to $\overline{CL}$ Low	20	—	—	μs	Fig. 9
t_{DDCL}	Time from DD High to $\overline{CL}$ Low	20	—	—	μs	Fig. 10
t_{DS}	Data Setup Time	10	—	—	μs	Fig. 10
t_{DH}	Data Hold Time	10	—	—	μs	Fig. 10
t_{CLTO}	Time from $\overline{CL}$ Low to $\overline{TO}$ Low	10	—	—	μs	Fig. 10
t_{TODD}	Time from $\overline{TO}$ High to DD High	20	—	—	μs	Fig. 10

PIN DESCRIPTION

(See Figure 45 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈0.5 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<250 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>250 mV and <1.0 volt).
11	9	DP	Depressed Pushbutton (Output) — Normally low; A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
12	10	$\overline{TO}$	$\overline{Tone\ Output}$ (Input) — When a Logic "1," disables the DTMF generator. Keypad is not disabled.
13	11	MS	Mute/Single Tone (Output) — A Logic "1" indicates the tone generator is enabled. A Logic "0" indicates tone generator is disabled.
14	12	A+	MPU Power Supply (Input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except Tone Ringer) in the absence of voltage at V+.
15	13	I/O	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD = Logic "0."
16	14	DD	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1," I/O is an input to the DTMF generator. As a Logic "0," I/O outputs keypad entries to the microprocessor.
17	15	$\overline{CL}$	$\overline{Clock}$ (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20 kHz.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
22	20	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.

(continued)

PIN DESCRIPTION (continued)

PIN (PLCC)	PIN (DIP)	Designation	Function
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path through the MIC terminal is disabled.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, f_O = (R3C13 + 8.0 μs)$^{-1}$.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	4.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	4.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	280	380	500	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.39 V_{ROC}	Vdc

MICROPROCESSOR INTERFACE

Voltage Regulator Output A+ Regulator	29	$V_{R/A+}$	0.95	1.1	1.3	V
A+ Input Current Off-Hook	28a	I_A(off)	300	500	700	μA
A+ Input Current On-Hook	28b	I_A(on)	4.0	6.0	9.0	mA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	30	R_{in}	50	100	150	kΩ
Input Current (I/O)	31	I_{in}	—	80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IH}	2.0	—	A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IL}	—	—	0.8	V
Output High Voltage (MS, DP, I/O)	32	V_{OH}	2.4	4.0	—	V
Output Low Voltage (MS, DP, I/O)	33	V_{OL}	—	0.1	0.4	V

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.5	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.5	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.8	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

2

ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.46	0.53	0.62	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	250	nA
TXO Terminal Positive Swing	22c	$V_{TXO(+)}$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO(-)}$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.41	0.45	0.55	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.46	0.62	0.62	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO(+)}$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO(-)}$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL(OFF)}$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL(ON)}$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM(OFF)}$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM(ON)}$	410	570	770	Ω

DTMF GENERATOR

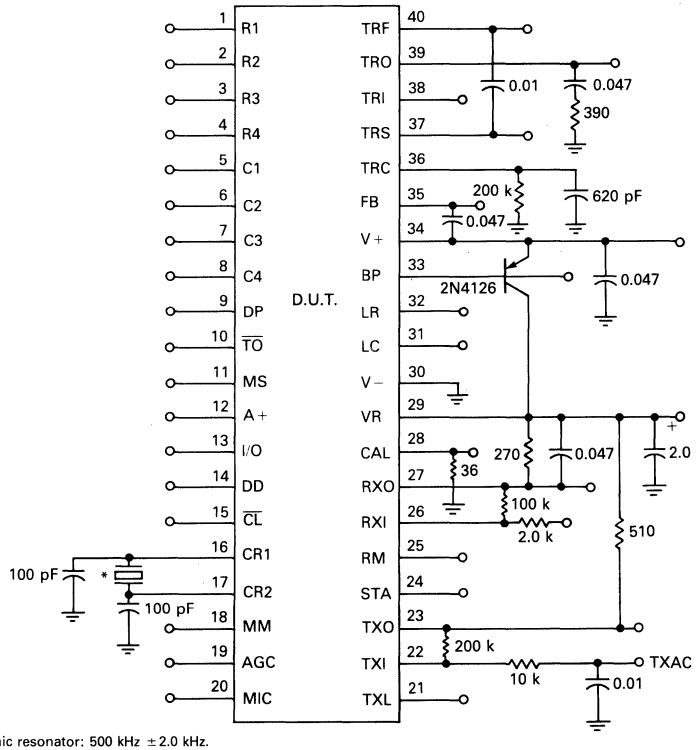
Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.34	0.39	0.50	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.43	0.48	0.62	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current		I_{TRS}				
V_{TRS} = 24 volts	15a		70	120	170	μA
V_{TRS} = 30 volts	15b		0.4	0.8	1.5	mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

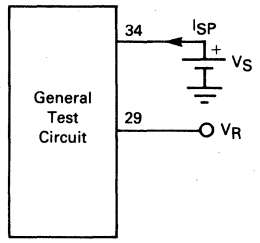
FIGURE 11 — GENERAL TEST CIRCUIT



Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin outs shown are for the 40 pin DIP.

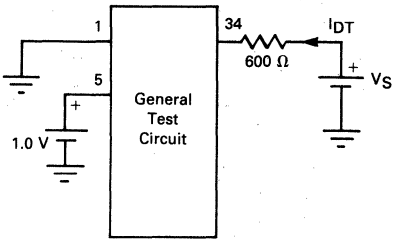
2

FIGURE 12 — TEST ONE



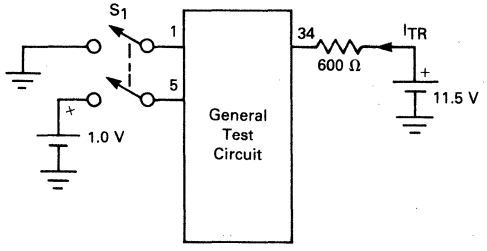
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 13 — TEST TWO



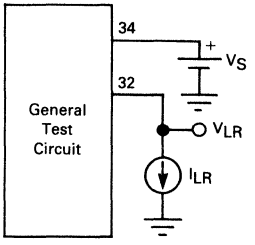
a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = I_{DT}\Big|_{26\ V} - I_{DT}\Big|_{11.5\ V}$

FIGURE 14 — TEST THREE



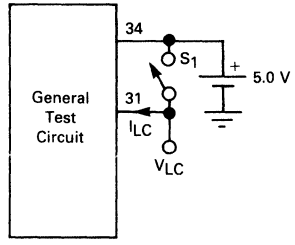
With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:
$\Delta I_{TR} = I_{TR}\Big|_{S_1\ Closed} - I_{TR}\Big|_{S_1\ Open}$

FIGURE 15 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

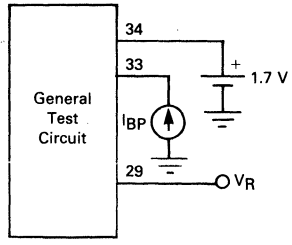
FIGURE 16 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

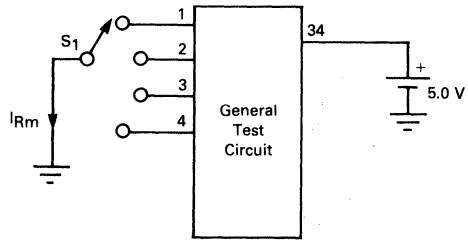
FIGURE 17 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = V_R\Big|_{0.0\ \mu A} - V_R\Big|_{150\ \mu A}$$

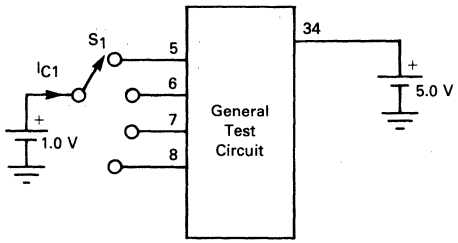
FIGURE 18 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

FIGURE 19 — TEST EIGHT

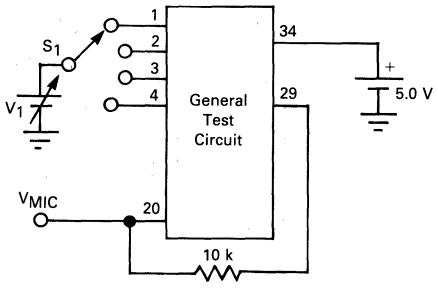


Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

2

FIGURE 20 — TEST NINE

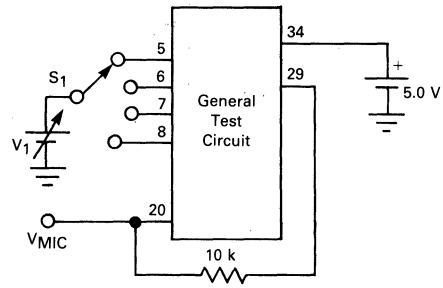


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 21 — TEST TEN

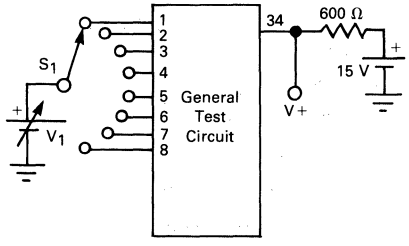


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.39 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 22 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

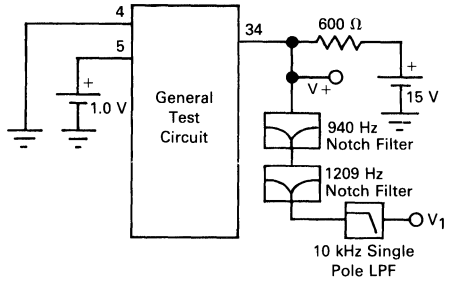
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 23 — TEST TWELVE

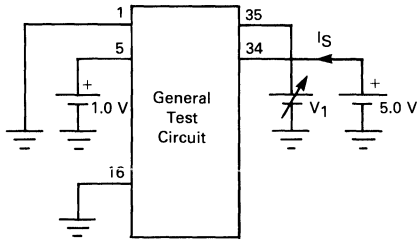


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 24 — TEST THIRTEEN

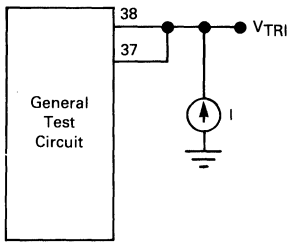


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

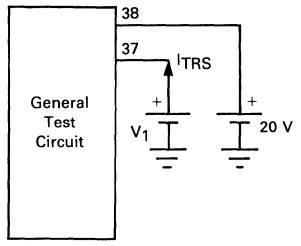
$$R_O = 1.0\ V \div \left[|I_S|_{2.8\ V} - |I_S|_{1.8\ V} \right]$$

FIGURE 25 — TEST FOURTEEN



Set I = 1.0 mA and measure V_{TRI}.

FIGURE 26 — TEST FIFTEEN

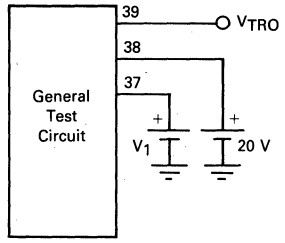


a. Measure I_{TRS} with V_1 = 24 V.

b. Measure I_{TRS} with V_1 = 30 V.

2

FIGURE 27 — TEST SIXTEEN



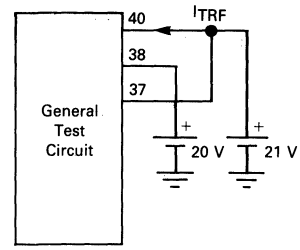
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20\ V$

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

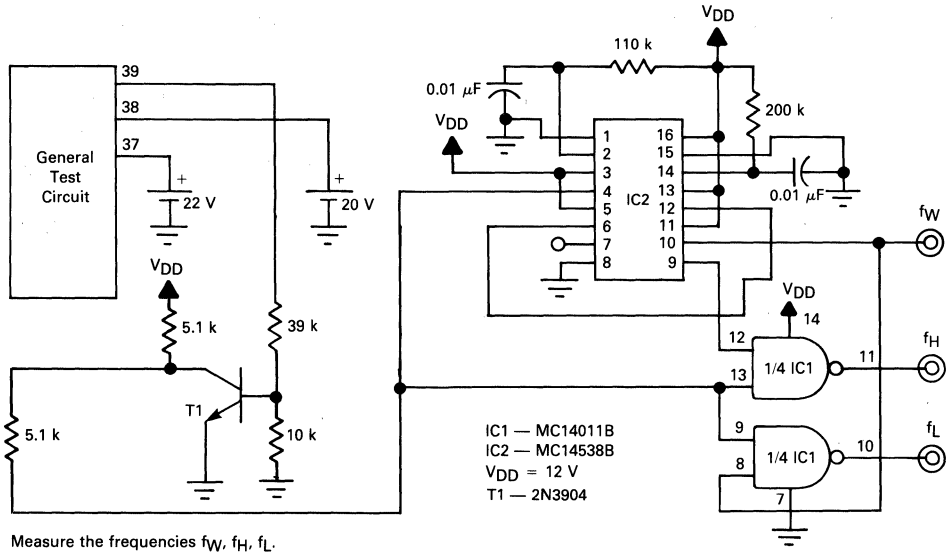
$$\Delta V_{TRF} = V_1\Big|_{\substack{\text{Test}\\16a}} - V_1\Big|_{\substack{\text{Test}\\16b}}$$

FIGURE 28 — TEST SEVENTEEN



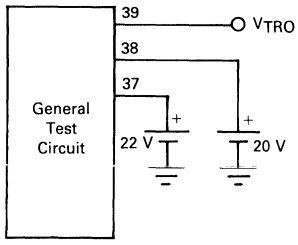
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 29 — TEST EIGHTEEN



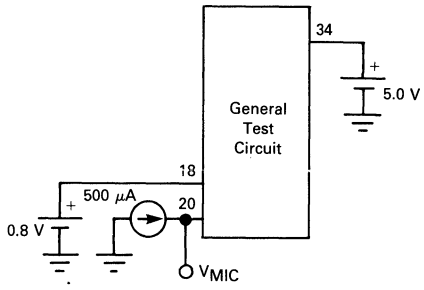
Measure the frequencies f_W, f_H, f_L.

FIGURE 30 — TEST NINETEEN



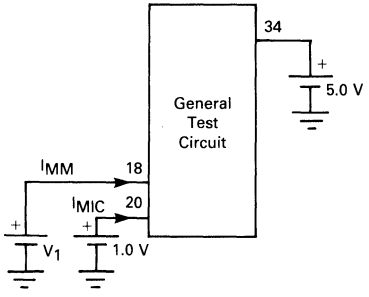
Measure V_{TRO} peak-to-peak voltage swing.
Using V_{TRI} from Test 14 Calculate:
$V_{o(p\text{-}p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 31 — TEST TWENTY



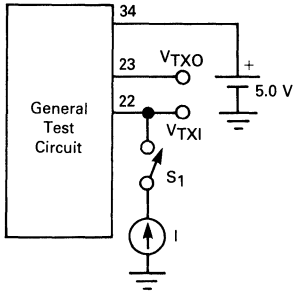
Measure V_{MIC}

FIGURE 32 — TEST TWENTY-ONE



a. Set V_1 = 2.0 V and measure I_{MIC}.
b. Set V_1 = 5.0 V and measure I_{MM}. Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

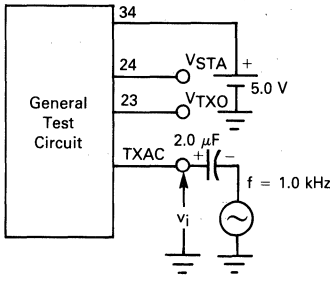
FIGURE 33 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$
c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.
d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

2

FIGURE 34 — TEST TWENTY-THREE



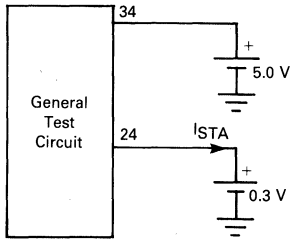
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

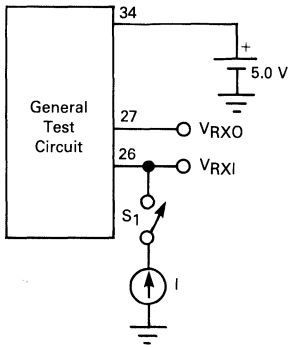
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 35 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 36 — TEST TWENTY-FIVE



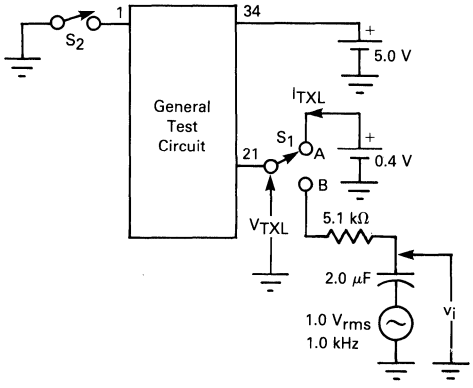
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 37 — TEST TWENTY-SIX

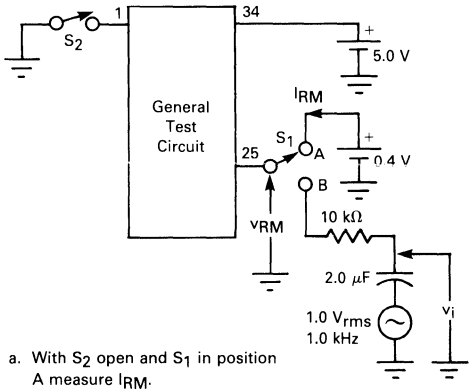


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

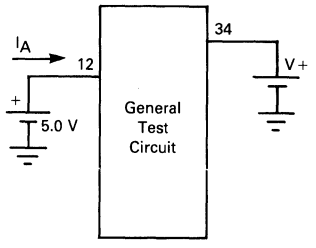
FIGURE 38 — TEST TWENTY-SEVEN



a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

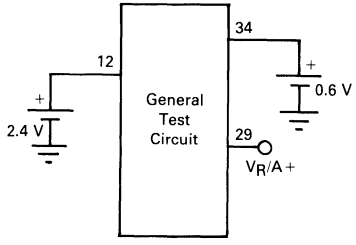
b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:
$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

FIGURE 39 — TEST TWENTY-EIGHT



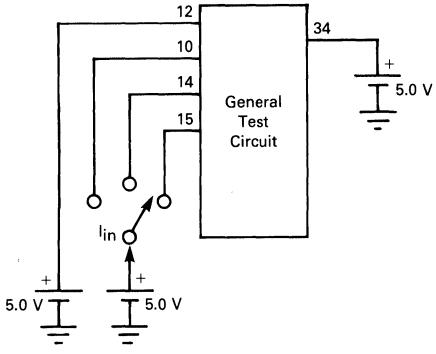
a. Set V+ = 1.4 V. Measure $I_A(OFF)$
b. Set V+ = 0.6 V. Measure $I_A(ON)$

FIGURE 40 — TEST TWENTY-NINE



Measure $V_R/A+$

FIGURE 41 — TEST THIRTY



Measure I_{in} at each of three inputs. For each, calculate:
$R_{in} = 5.0\ V/I_{in}$

2

FIGURE 42 — TEST THIRTY-ONE

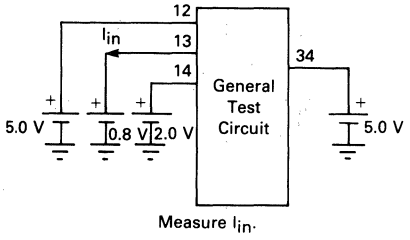
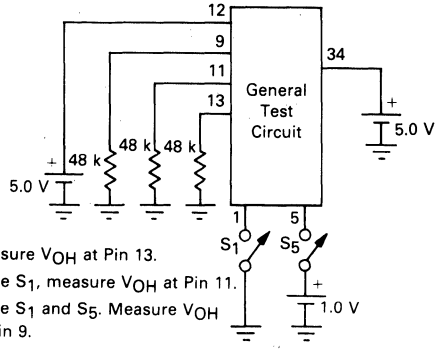
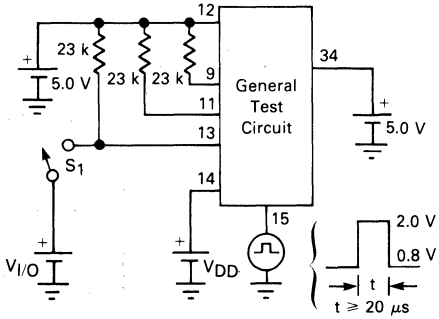


FIGURE 43 — TEST THIRTY-TWO



a. Measure V_{OH} at Pin 13.
b. Close S_1, measure V_{OH} at Pin 11.
c. Close S_1 and S_5. Measure V_{OH} at Pin 9.

FIGURE 44 — TEST THIRTY-THREE



a. Set V_{DD} to 0.8 V Measure V_{OL} voltages at Pins 9 and 11.
b. Close S_1. Force $V_{I/O}$ to 0.8 V and V_{DD} to 2.0 V. Apply 4 clock pulses to Pin 15. Open S_1 and decrease V_{DD} to 0.8 V. Measure V_{OL} at Pin 13.

APPLICATIONS INFORMATION

Figure 45 specifies a typical application circuit for the MC34010. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration in Figure 45 is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be ≤ 1.0 μF to satisfy 5.0 Hz impedance specifications.

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_O) of a relaxation oscillator. Typically $f_O = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_O/10$ and $f_O/8$. The warble rate is $f_O/640$. The tone ringer will operate with f_O from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Hook-Switch Click Suppression

When the telephone is switched to the off-hook condition C3 charges from 0 volts to a 300 mV bias voltage. During this time interval, receiver clicks are suppressed by a low impedance at the RM terminal. If this click suppression mechanism is desired during a rapid succession of hook switch transitions, then C3 must be quickly discharged when the telephone is on-hook, R16 and S3 provide a rapid discharge path for C3 to reset the click suppression timer. R16 is selected to limit the discharge current in S3 to prevent damage to switch contacts.

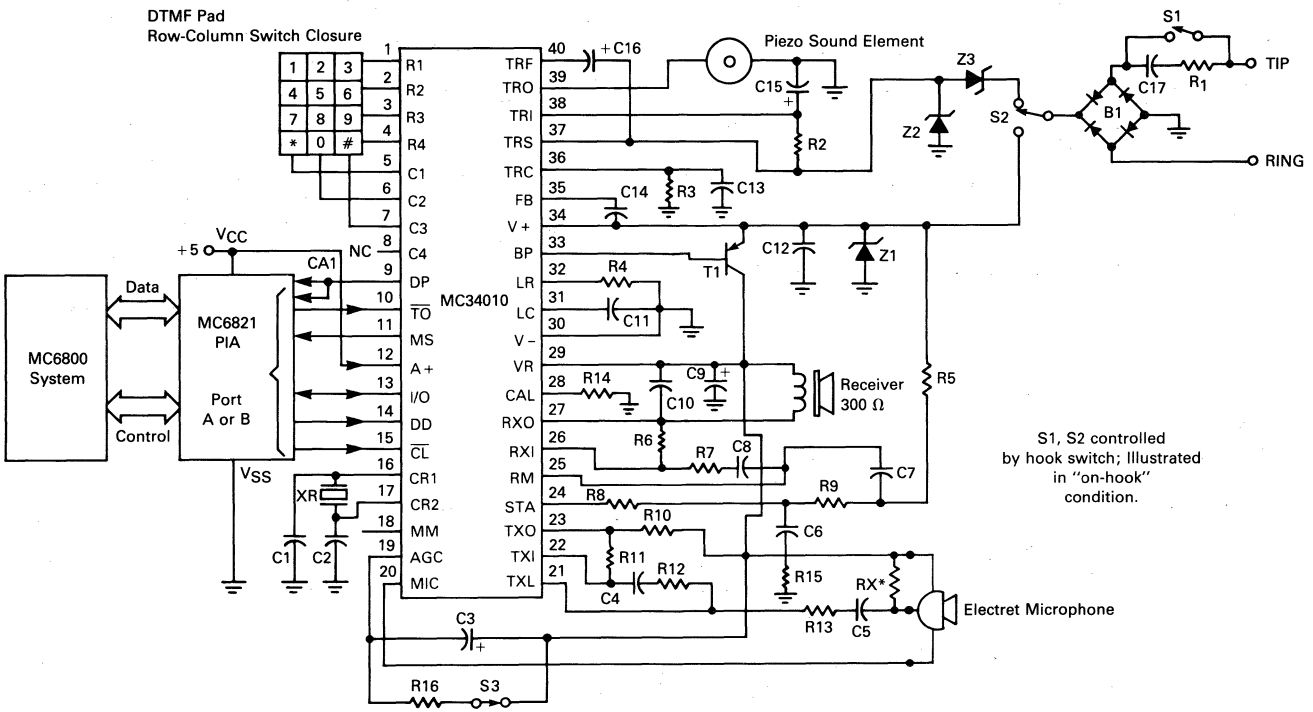
Microprocessor Interface

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Figure 47. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The MC34010A clock speed requirement is slow enough (typically 20 kHz) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a Logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at Pin 12 (A+) may be disconnected to conserve power. Normally the speech circuitry is powered by the voltage supplied at the V+ terminal (Pin 34) from the telephone lines. During this time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook," and V+ falls below 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a microprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook."

FIGURE 45 — ELECTRONIC TELEPHONE APPLICATION CIRCUIT



EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 45)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R16	100	Hook switch click suppression current limit resistor (optional): limits current when S3 discharges C3 after switching to the on-hook condition.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

2

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

Motorola Inc. does not endorse or warrant the suppliers referenced.

MC34011A

Advance Information

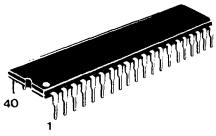
ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- Equalization Provided to Compensate for Long/Short Line Performance

ELECTRONIC TELEPHONE CIRCUIT

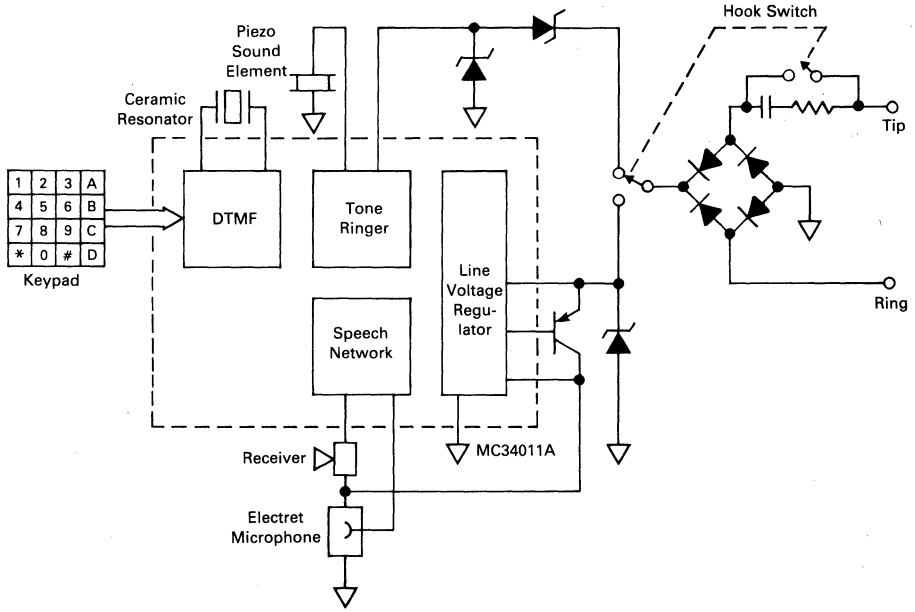
BIPOLAR LINEAR/I^2L

FN SUFFIX
44-PIN
PLCC
CASE 777-02



P SUFFIX
PLASTIC PACKAGE
CASE 711-03

FIGURE 1 — ELEMENTS OF THE ELECTRONIC TELEPHONE



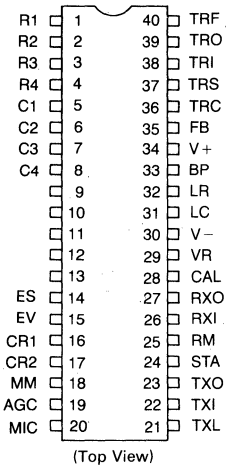
This document contains information on a new product. Specifications and information herein are subject to change without notice.

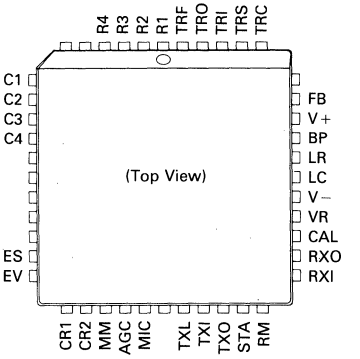
2

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+18, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

FIGURE 2 — PIN CONNECTIONS





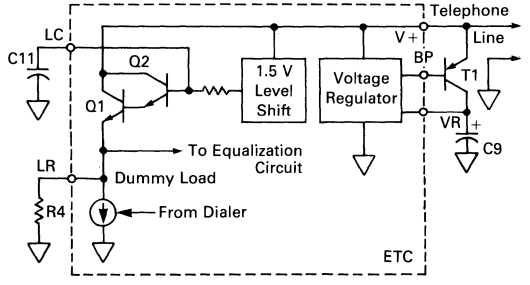
GENERAL CIRCUIT DESCRIPTION

Introduction

The MC34011A Electronic Telephone Circuit (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1).

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34011A in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM

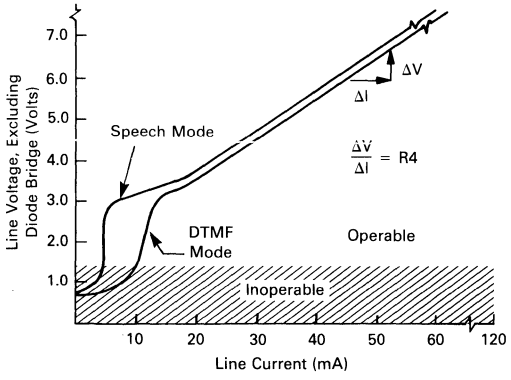


Line Voltage Regulator

The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34011A telephone.

GENERAL CIRCUIT DESCRIPTION (continued)

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

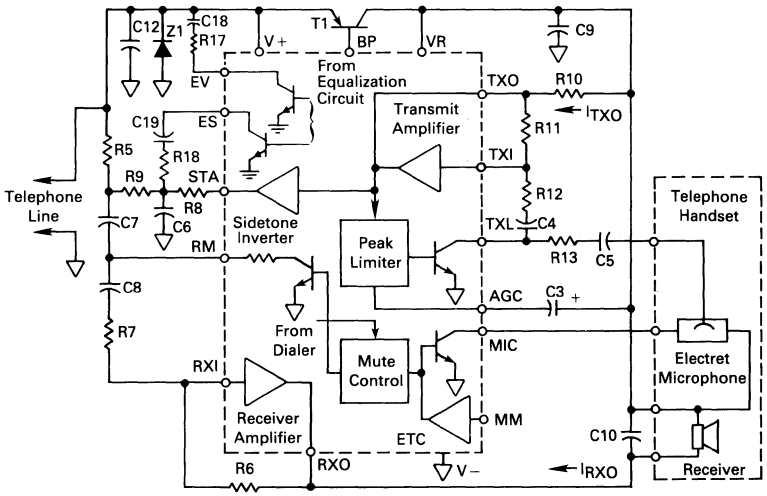
Equalization Circuit

The equalization circuit varies the transmit, receive and sidetone gains with loop current to compensate for losses in long lines. The LR terminal voltage varies directly as the dc loop current. The equalization circuit senses this voltage and switches in external resistors between V+ and V− and across capacitor C6 (Figure 5) when the loop current exceeds a threshold level. The speech network operates with full transmit, receive and sidetone gains for long loops. On short loops the LR voltage exceeds the threshold and these gains are reduced. The threshold detection circuit has a dc hysteresis to prevent distortion of speech signals when the telephone is operated at the threshold current. The equalization is disabled (gains at full value) during dialing.

DTMF Dialer

Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



2

The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM

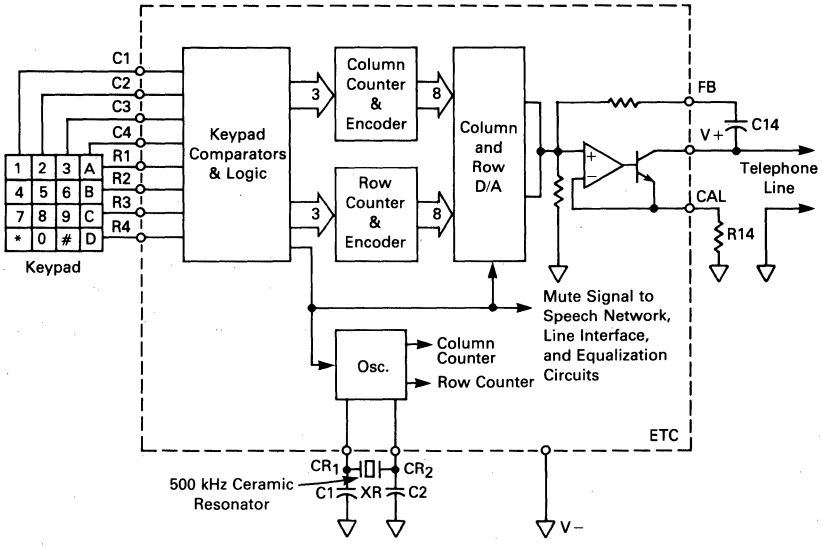


FIGURE 7 — TONE RINGER BLOCK DIAGRAM

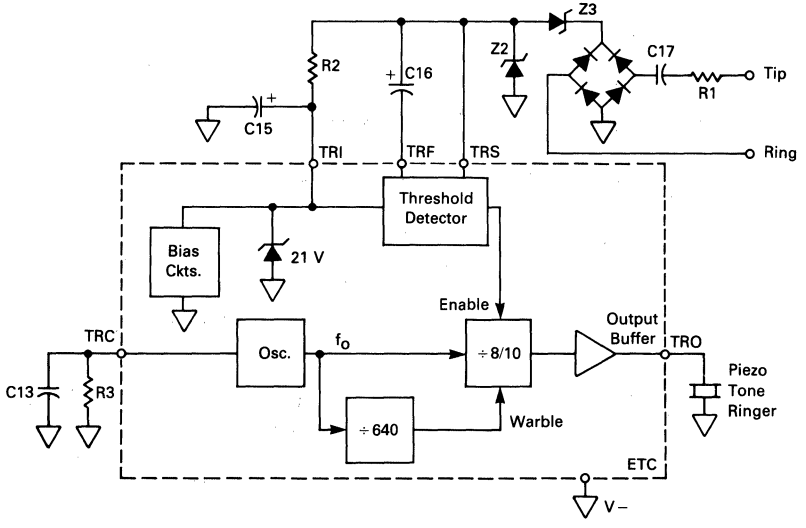


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

2

PIN DESCRIPTION

(See Figure 38 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>600 mV and <3.0 volt).
5, 6 11–15, 23,39	9–13	NC	No connection
16	14	ES	Sidetone Equalization terminal connects an external resistor between the junction of R8, R9 and V−. At loop currents greater than the equalization threshold this resistor is switched in to reduce the sidetone level. The resistor is switched out during dialing.
17	15	EV	Voice Equalization terminal connects an external resistor between V+ and V−, for loop length equalization. At loop currents greater than the equalization threshold this resistor is switched in to reduce the transmit and receive gains. The resistor is switched out during dialing.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path and the transmit amplifier output are disabled.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
22	20	MIC	Microphone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.

(continued)

PIN DESCRIPTION (continued)

PIN (PLCC)	PIN (DIP)	Designation	Function
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\ \mu s)^{-1}$.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	5.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	5.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	950	1100	1200	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.30 V_{ROC}	Vdc

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.0	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.4	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.6	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

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ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.48	0.53	0.68	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	400	nA
TXO Terminal Positive Swing	22c	$V_{TXO(+)}$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO(-)}$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.40	0.45	0.54	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.48	0.52	0.68	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO(+)}$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO(-)}$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL(OFF)}$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL(ON)}$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM(OFF)}$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM(ON)}$	410	570	770	Ω

DTMF GENERATOR

Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.38	0.45	0.55	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.48	0.55	0.67	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

EQUALIZATION CONTROL

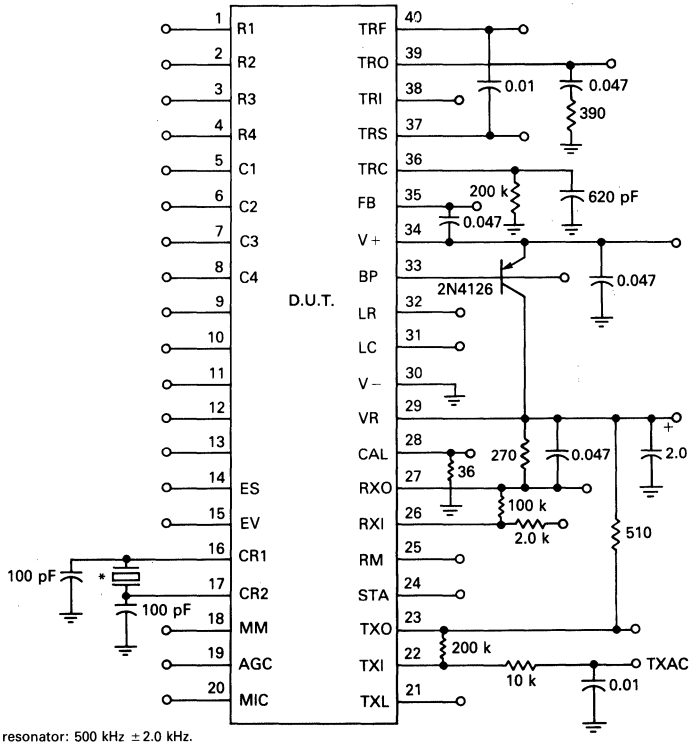
ES Terminal OFF Resistance	34a	$R_{ES(OFF)}$	100	200	325	kΩ
Equalization Threshold Voltage	34b	V_E	1.4	1.6	2.0	Vdc
Equalization Threshold Hysteresis	34c	ΔV_E	75	200	300	mVdc
EV Terminal OFF Resistance	35a	$R_{EV(OFF)}$	100	200	325	kΩ
EV Terminal ON Resistance	35b	$R_{EV(ON)}$	—	20	50	Ω

ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current		I_{TRS}				
V_{TRS} = 24 volts	15a		70	120	170	μA
V_{TRS} = 30 volts	15b		0.4	0.8	1.5	mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

FIGURE 8 — GENERAL TEST CIRCUIT



Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin numbers in this Figure and in Test Circuits are for the DIP package.

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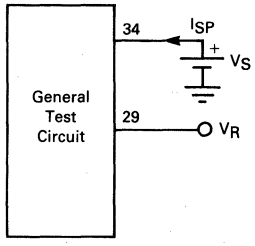
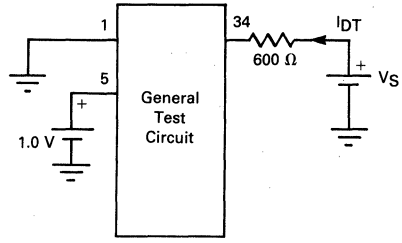
FIGURE 9 — TEST ONE



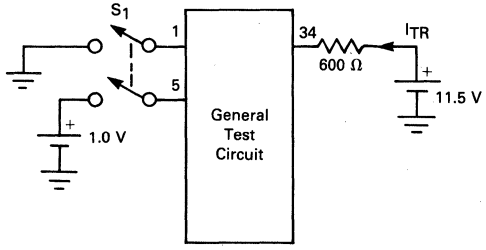
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 10 — TEST TWO



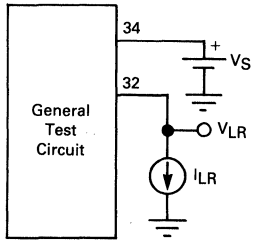
a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = |I_{DT}|_{26\ V} - |I_{DT}|_{11.5\ V}$

FIGURE 11 — TEST THREE



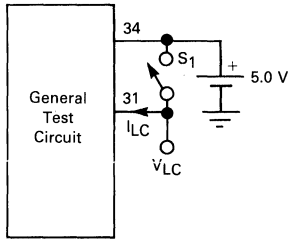
With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:
$\Delta I_{TR} = |I_{TR}|_{S_1\ Closed} - |I_{TR}|_{S_1\ Open}$

FIGURE 12 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

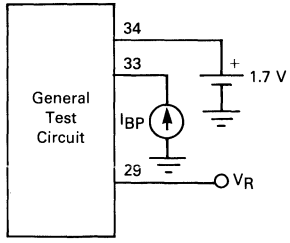
FIGURE 13 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

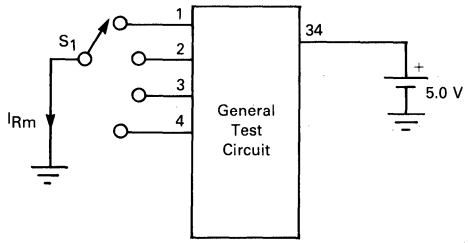
FIGURE 14 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = |V_R|_{0.0\ \mu A} - |V_R|_{150\ \mu A}$$

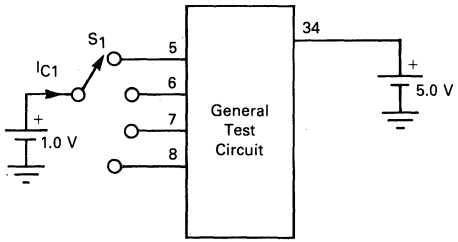
FIGURE 15 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

FIGURE 16 — TEST EIGHT

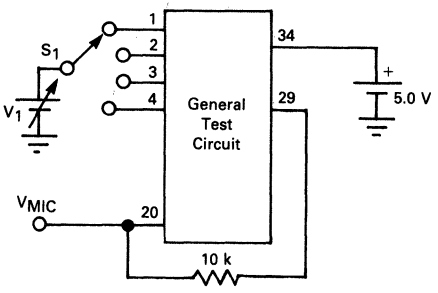


Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

2

FIGURE 17 — TEST NINE

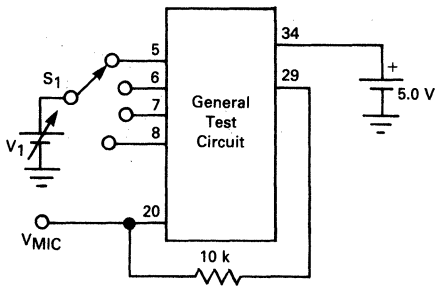


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 18 — TEST TEN

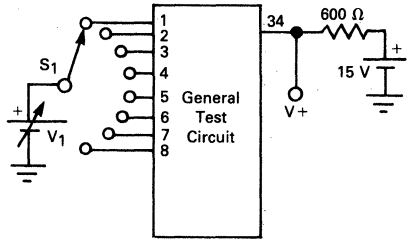


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.30 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 19 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

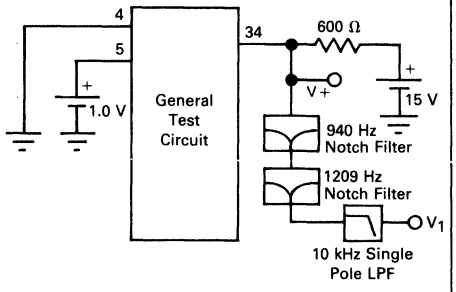
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 20 — TEST TWELVE

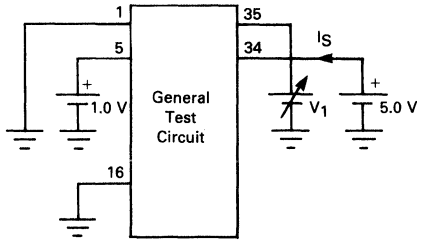


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 21 — TEST THIRTEEN

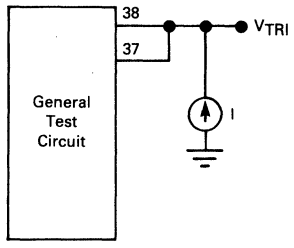


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

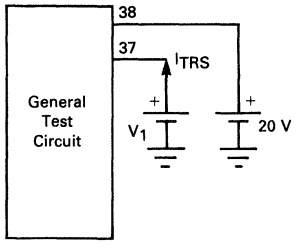
$$R_O = 1.0\ \text{V} \div \left[I_S\Big|_{2.8\ \text{V}} - I_S\Big|_{1.8\ \text{V}} \right]$$

FIGURE 22 — TEST FOURTEEN



Set I = 1.0 mA and measure V_{TRI}.

FIGURE 23 — TEST FIFTEEN

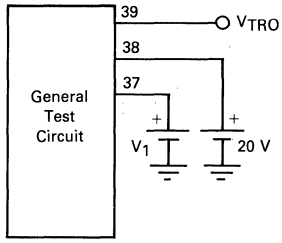


a. Measure I_{TRS} with V_1 = 24 V.

b. Measure I_{TRS} with V_1 = 30 V.

2

FIGURE 24 — TEST SIXTEEN



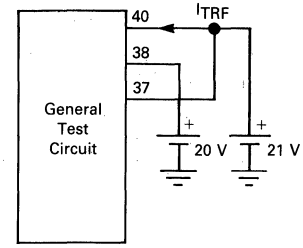
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20\ V$

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

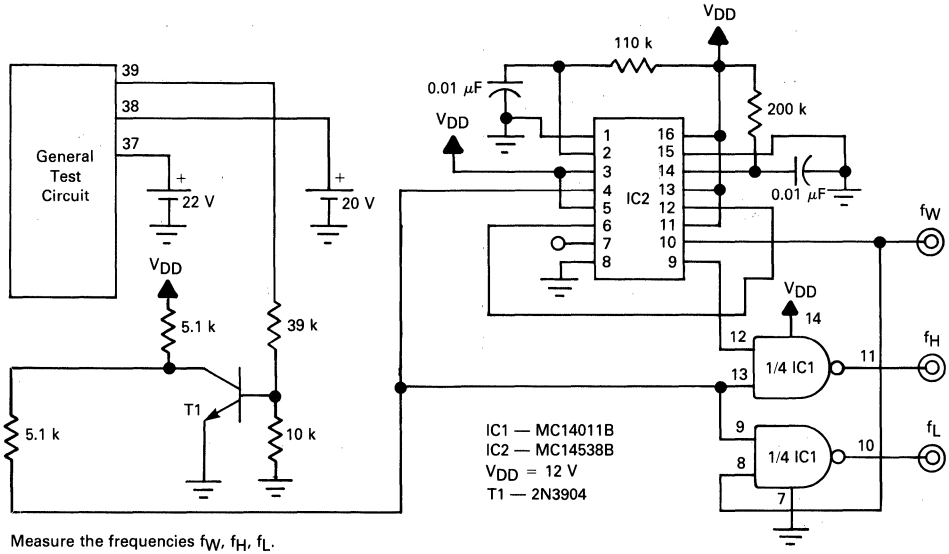
$\Delta V_{TRF} = V_1\big|_{\text{Test 16a}} - V_1\big|_{\text{Test 16b}}$

FIGURE 25 — TEST SEVENTEEN



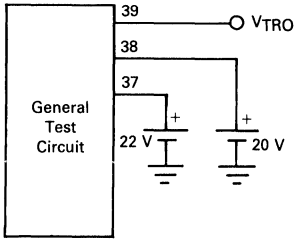
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 26 — TEST EIGHTEEN



Measure the frequencies f_W, f_H, f_L.

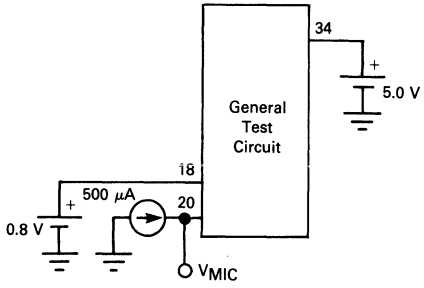
FIGURE 27 — TEST NINETEEN



Measure V_{TRO} peak-to-peak voltage swing. Using V_{TRI} from Test 14 Calculate:

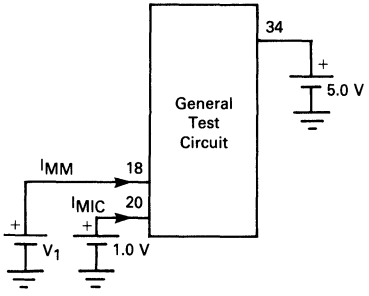
$V_{o(p-p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 28 — TEST TWENTY



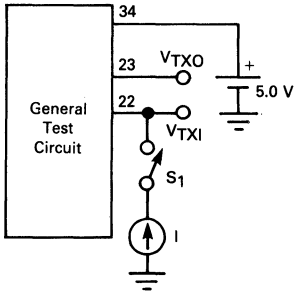
Measure V_{MIC}

FIGURE 29 — TEST TWENTY-ONE



a. Set V_1 = 2.0 V and measure I_{MIC}.
b. Set V_1 = 5.0 V and measure I_{MM}. Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

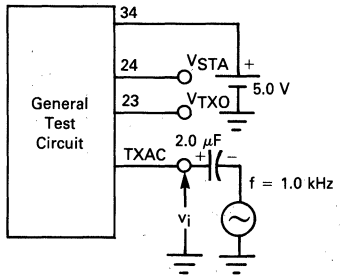
FIGURE 30 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$
c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.
d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

2

FIGURE 31 — TEST TWENTY-THREE



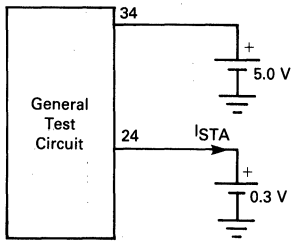
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

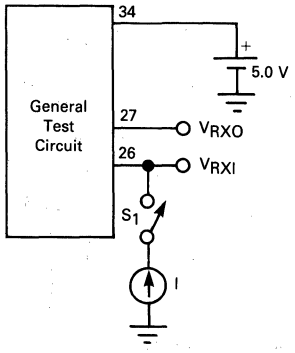
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 32 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 33 — TEST TWENTY-FIVE



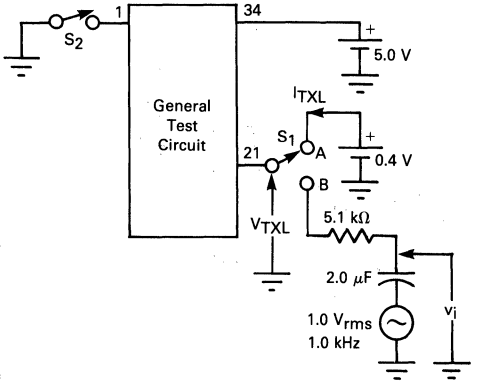
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 34 — TEST TWENTY-SIX

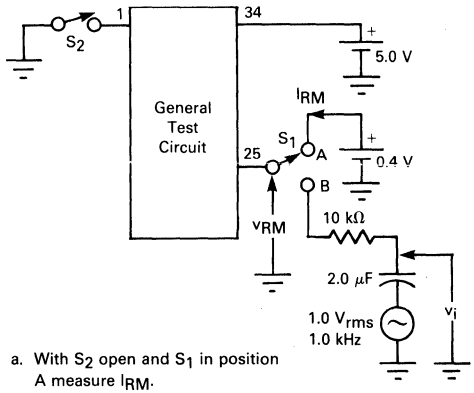


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

FIGURE 35 — TEST TWENTY-SEVEN

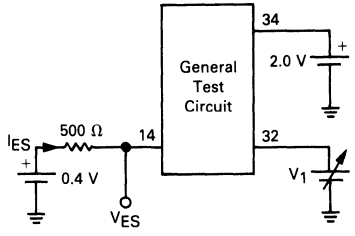


a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM(OFF)} = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:
$$R_{RM(ON)} = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

Note: Tests 28–33 intentionally omitted.

FIGURE 36 — TEST THIRTY-FOUR



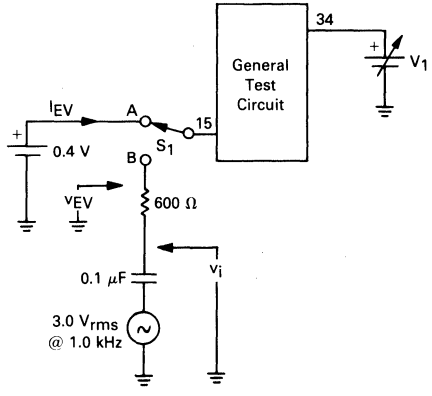
a. Set V_1 = 0 V. Measure I_{ES}. Calculate R (OFF) = 0.4 ÷ I_{ES}.

b. Increase V_1 until V_{ES} SWITCHES low (<200 mV). Measure V_1. $V_E = V_1$.

c. Decrease V_1 from the value in Test 34b until V_{ES} switches high (>200 mV). Measure V_1. Calculate $\Delta V_E = V_1 - V_1$

Test 34b — Test 34c

FIGURE 37 — TEST THIRTY-FIVE



a. With S_1 in position A set V_1 = 2.0 V. Measure I_{EV} Calculate $R_{EV(OFF)} = 0.4 \div I_{EV}$.

b. Set V_1 = 5.0 V and Set S_1 to position B. Measure v_i and v_{EV}. Calculate
$$R_{EV(ON)} = \frac{v_{EV}}{v_i - v_{EV}} \times 600\ \Omega$$

APPLICATIONS INFORMATION

Figure 38 specifies a typical application circuit for the MC34011A. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be $\leq$ 1.0 μF to satisfy 5.0 Hz impedance specifications. (EIA RS-470)

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_O) of a relaxation oscillator. Typically $f_O = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_O/10$ and $f_O/8$. The warble rate is $f_O/640$. The tone ringer will operate with f_O from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Equalization of Speech Network

Resistors R17 and R18 are switched into the circuit when the voltage at the LR terminal exceeds the equalization threshold voltage (typically 1.65 V). R17 reduces the transmit and receive gains for loop currents greater than the threshold (short loops) by attenuating signals at tip and ring. R18 reduces the sidetone level which would otherwise increase when R17 is switched into the circuit. The voltage V_{LR} at LR terminal is given by

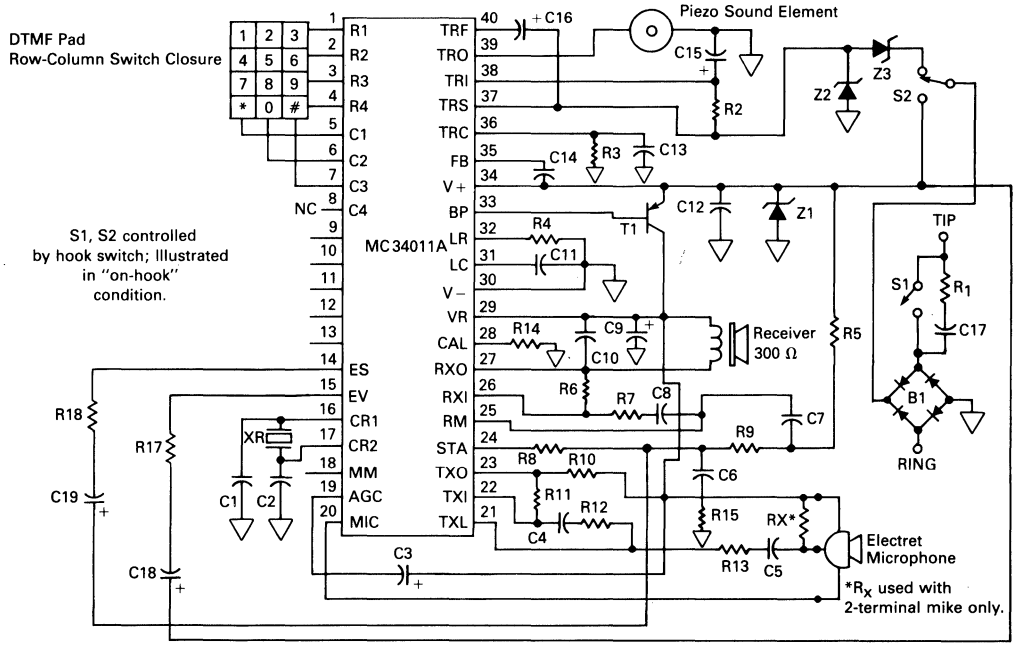
$V_{LR} = (I_L - I_S) \times R4.$

where I_L = loop current

I_S = dummy load current (6.0 mA) + speech network current (4.0 mA).

Thus resistor R4 is selected to activate the equalization circuit at the desired loop current. However, R4 must be selected keeping in mind the fact that it also controls the dc resistance of the telephone. Capacitors C18 and C19 prevent dc current flow into the EV and ES terminals. This reduces clicks and also prevents changes in the dc characteristic of the telephone when the EV and ES terminals are switched to low impedance.

FIGURE 38 — ELECTRONIC TELEPHONE APPLICATION CIRCUIT



EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 38)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.
C18	25 μF, 25 V	Speech equalization coupling capacitor. Prevents dc current flow into EV terminal. (optional)
C19	5.0 μF, 3.0 V	Sidetone equalization coupling capacitor. Prevents dc current flow into ES terminal. (optional)

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R17	600	Speech equalization resistor. Reduces transmit and receive gain when EV terminal switches on. (optional)
R18	5.1 k	Sidetone equalization resistor. Reduces sidetone level when ES terminal switches on. (optional)
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

Motorola Inc. does not endorse or warrant the suppliers referenced.

MC34012-1
MC34012-2
MC34012-3

2

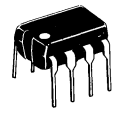
Advance Information

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options—MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

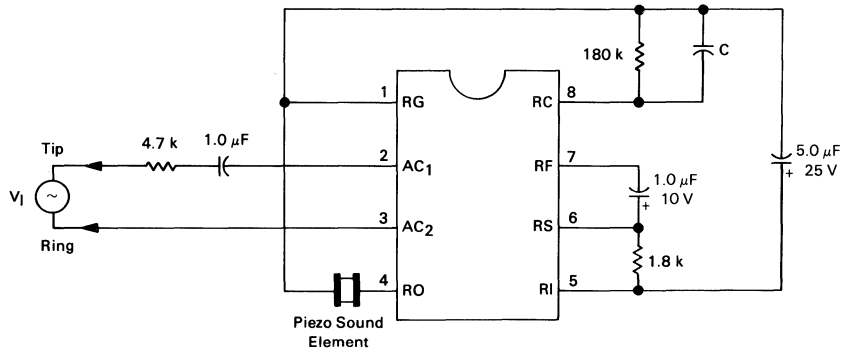
TELEPHONE
TONE RINGER

BIPOLAR LINEAR/I^2L



PLASTIC PACKAGE
CASE 626

APPLICATION CIRCUIT



MC34012-1: C = 1000 pF
MC34012-2: C = 500 pF
MC34012-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION CIRCUIT PERFORMANCE

Characteristic	Typical Value	Units
Output Tone Frequencies MC34012-1 MC34012-2 MC34012-3 Warble Frequency	 832/1040 1664/2080 416/520 13	 Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	20	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	28	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 20 10	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200–3200 Hz	 28 >1.0 55 >1.0	 kΩ MΩ kΩ MΩ
Maximum Transient Input Voltage ($T \leq 2.0$ ms)	1500	V

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The positive output of diode bridge to which an external current sense resistor is connected.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RF	The terminal for the filter capacitor used in detection of ringing input signals.
RO	The tone ringer output terminal through which the sound element is driven.
RG	The negative output of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies.

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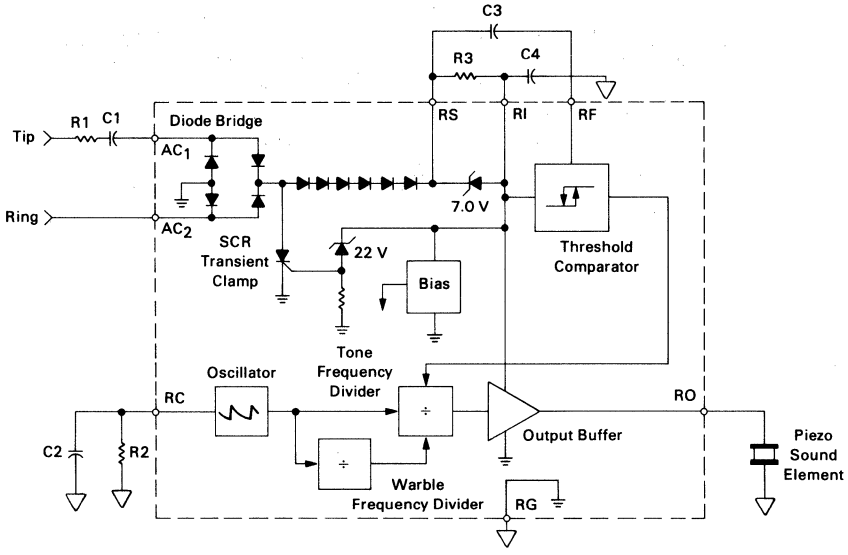
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage ($V_{Start} = V_I$ @ Ring Start)						Vdc
$V_I > 0$	1a	$V_{Start(+)}$	31	34.5	38	
$V_I < 0$	1b	$V_{Start(-)}$	-31	-34.5	-38	
Ringing Stop Voltage ($V_{Stop} = V_I$ @ Ring Stop)	1c	V_{Stop}				Vdc
MC34012-1			16	20	25	
MC34012-2			13	18	22	
MC34012-3			16	20	25	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34012-1 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	12	13	14	
MC34012-2 High Tone		f_H	1934	2080	2226	
Low Tone		f_L	1548	1664	1780	
Warble Tone		f_W	12	13	14	
MC34012-3 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	24	26	28	
Output Voltage (V_I = 50 V)	6	V_O	19	20	23	V_{p-p}
Output Short-Circuit Current	2	I_O	35	50	80	mA_{p-p}
Input Diode Voltage (I_I = 1.0 mA)	3	V_D	4.6	5.1	5.6	Vdc
Input Voltage—SCR Off (I_I = 30 mA)	4a	V_{off}	37	42	47	Vdc
Input Voltage—SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.2	6.0	Vdc
Threshold Filter Resistance $R_{RF} = 2.0\ V/I_{RF}$	5	R_{RF}	30	50	80	kΩ

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MC34012 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_O is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_O from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

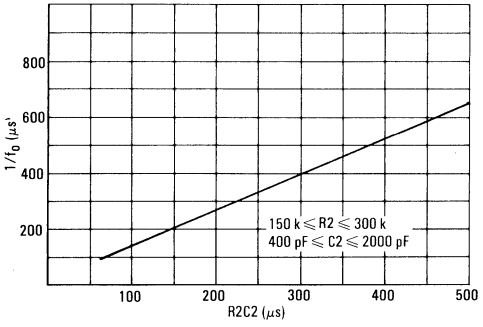
The frequency of the tone ringer output signal at pin RO alternates between $f_O/4$ to $f_O/5$. The warble rate at which the frequency changes is $f_O/320$ for the MC34012-1, $f_O/640$ for the MC34012-2, or $f_O/160$ for the MC34012-3. With a 4.0 kHz oscillator frequency, the MC34012-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34012-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 Hz oscillator frequency. The MC34012-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 20 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal will be generated at RO. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a current through R3 which is input at terminal RI. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.7 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltage regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

FIGURE 1 — OSCILLATOR PERIOD ($1/f_O$) versus OSCILLATOR R2 C2 PRODUCT

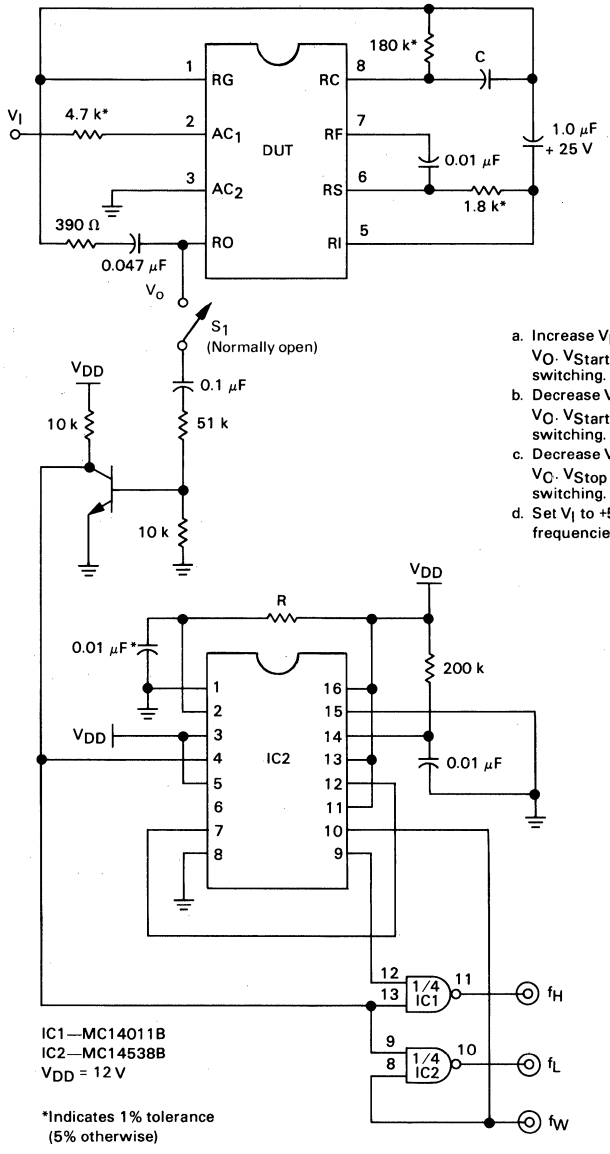


EXTERNAL COMPONENTS

R1	Line input resistor. R1 controls the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 2000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 0.8 kΩ to 2.0 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

2

FIGURE 2 — TEST ONE



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

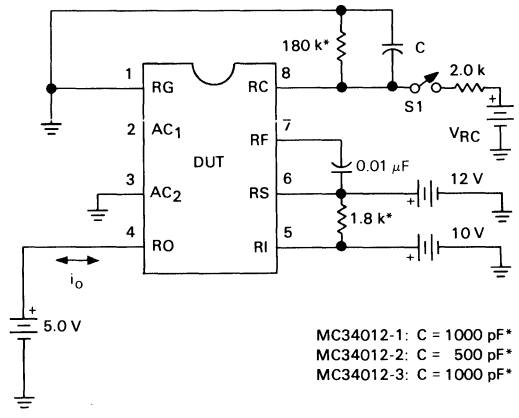
a. Increase V_I from +30 volts while monitoring V_O. $V_{Start(+)}$ equals V_I when V_O commences switching.
b. Decrease V_I from −30 volts while monitoring V_O. $V_{Start(-)}$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

*Indicates 1% tolerance (5% otherwise)

MC34012-1: R = 110 kΩ*
MC34012-2: R = 55 kΩ*
MC34012-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



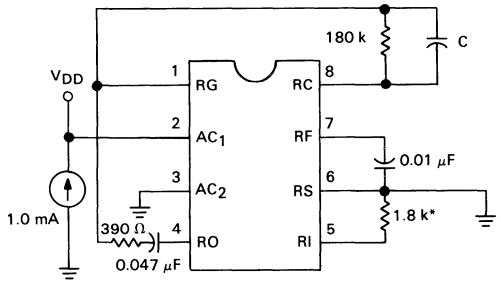
MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

With V_{RC} = 3.5 volts, close S1. Measure the current at Pin 4 (I_{O1}). Repeatedly switch V_{RC} between 3.5 volts and 0 volts until Pin 4 current changes polarity. Measure this opposite polarity current (I_{O2}).
Calculate:

$$I_O = |I_{O1}| + |I_{O2}|$$

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE



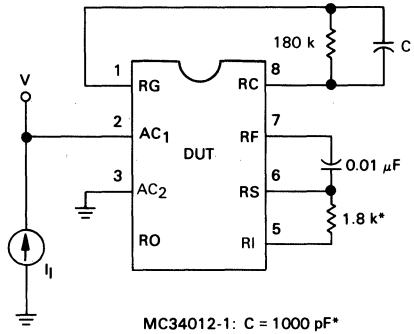
MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

Measure voltage at Pin 2.

*Indicates 1% tolerance (5% otherwise)

2

FIGURE 5 — TEST FOUR

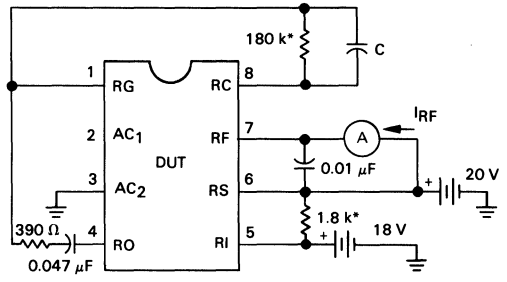


a. Set I_I to 30 mA. Measure voltage at Pin 2 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 2 (V_{on}).

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 6 — TEST FIVE



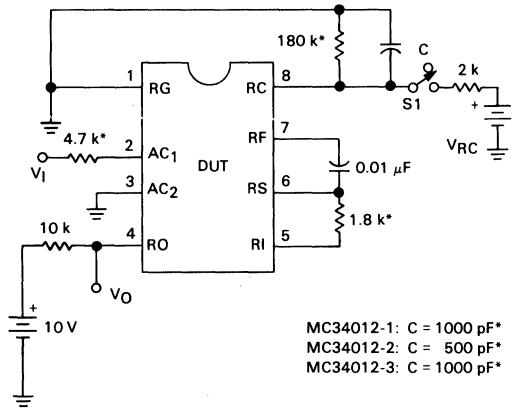
Measure current into Pin 7 (I_{RF}).
Calculate:

R_{RF} = 2 volts ÷ I_{RF}

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



With V_{RC} = 3.5 volts, close S1. Set V_I to 50 volts. Measure dc voltage at Pin 4 (V_{O1}). Repeatedly change V_{RC} between 3.5 volts and 0 volts until Pin 4 changes state. Measure the new voltage at Pin 4 (V_{O2}).
Calculate the peak-to-peak output voltage:

$$V_{Op\text{-}p} = |V_{O2} - V_{O1}|$$

MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

MC34013A

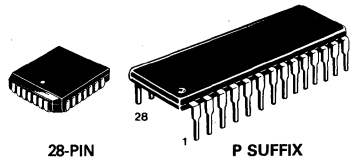
2

TELEPHONE SPEECH NETWORK AND TONE DIALER

- Linear/I^2L Technology Provides Low 1.4 Volt Operation in Both Speech and Dialing Modes
- Speech Network Provides 2–4 Wire Conversion with Adjustable Sidetone Utilizing an Electret Microphone
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- Dialer Mutes Speech Network with Internal Delay for Click Suppression on DTMF Key Release

SPEECH NETWORK AND TONE DIALER

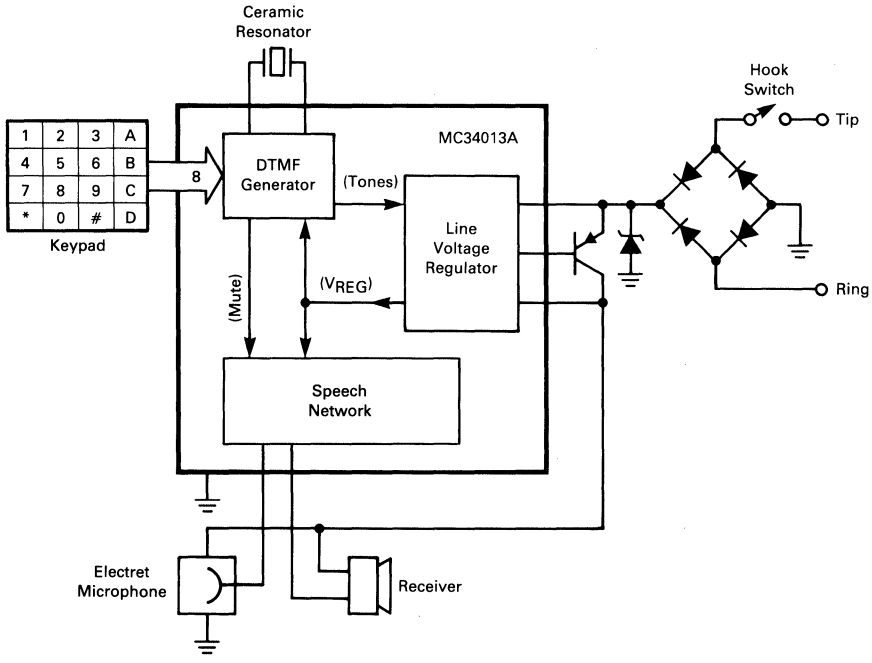
BIPOLAR LINEAR/I^2L



28-PIN
QUAD PACK
CASE 776-02

P SUFFIX
PLASTIC PACKAGE
CASE 710-02

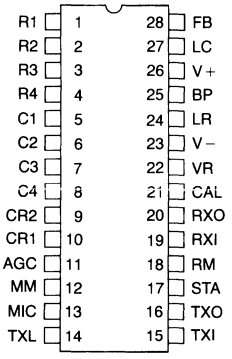
FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 26)	+18, −1.0	V
VR Terminal Voltage (Pin 22)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 20)	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



2

GENERAL CIRCUIT DESCRIPTION

The MC34013A Electronic Speech Network and Tone Dialer provides a frequency synthesizer for DTMF dialing, analog amplifiers for speech transmission and a dc line interface circuit that terminates the telephone line. When mated with the MC34012 Tone Ringer, a complete tone dialing telephone can be produced with just two ICs.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34013A in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

The dc line interface circuit (Figure 2) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the IC draws only the speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R12. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 3 illustrates the dc voltage/current characteristic of an MC34013A telephone.

Speech Network

The speech network (Figure 4) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal

FIGURE 2 — DC LINE INTERFACE BLOCK DIAGRAM

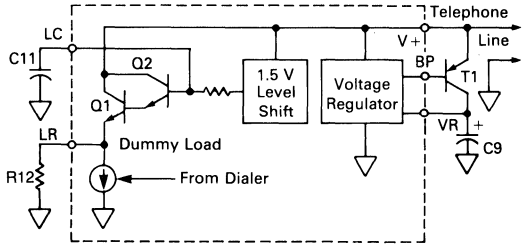
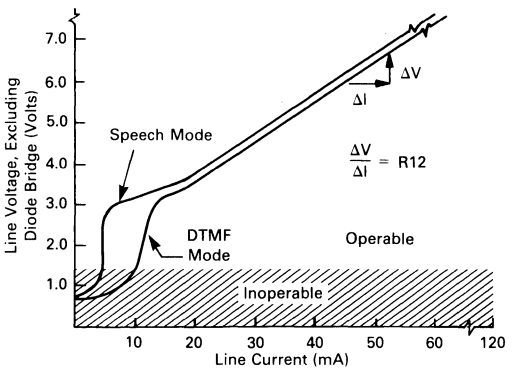
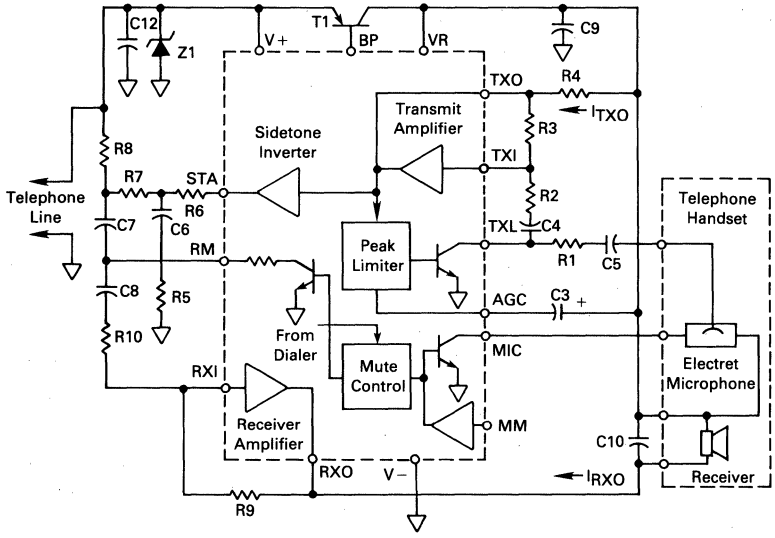


FIGURE 3 — DC V-I CHARACTERISTIC



GENERAL CIRCUIT DESCRIPTION (continued)

FIGURE 4 — SPEECH NETWORK BLOCK DIAGRAM



when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

Keypad interface comparators activate the DTMF row and column tone generators (Figure 5) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications. (EIA RS-470)

FIGURE 5 — DTMF DIALER BLOCK DIAGRAM

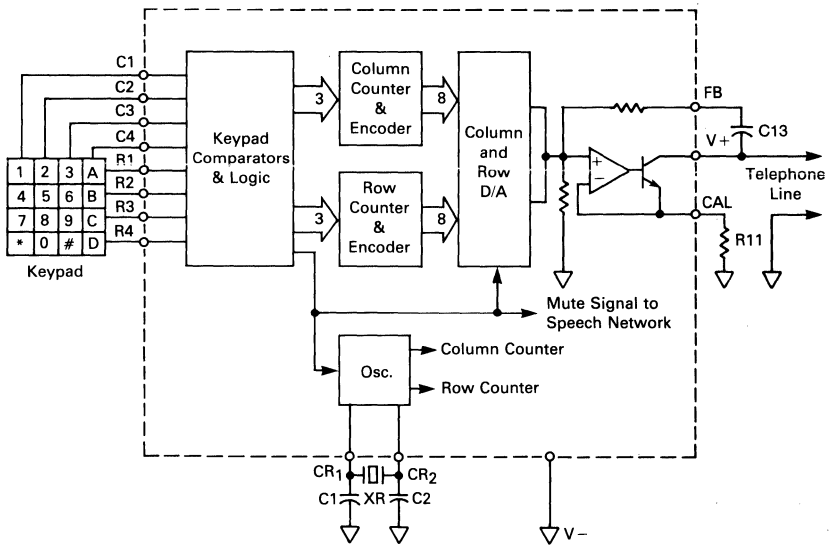


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

LINE VOLTAGE REGULATOR

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.0	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.4	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.6	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

2

ELECTRICAL CHARACTERISTICS (continued)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	5.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	5.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}, \; m = 1,2,3,4}{R_{Cn} \quad n = 1,2,3,4}$	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	950	1100	1200	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.30 V_{ROC}	Vdc

DTMF GENERATOR

Row Tone Frequency	Row 1 Row 2 Row 3 Row 4	11a, 11b	f_{Rm}	692.9 765.3 848.9 935.1	696.4 769.2 853.2 939.8	699.9 773.0 857.5 944.5	Hz
Column Tone Frequency	Column 1 Column 2 Column 3 Column 4	11c, 11d	f_{Cn}	1201.6 1330.2 1471.9 1625.2	1207.7 1336.9 1479.3 1633.4	1213.7 1343.6 1486.7 1641.5	Hz
Row Tone Amplitude		11e	V_{Row}	0.38	0.45	0.55	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.48	0.55	0.67	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_O	1.0	2.5	3.0	kΩ

SPEECH NETWORK

MIC Terminal Saturation Voltage	14	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	15a	I_{MIC}	—	0.0	5.0	μA
MM Terminal Input Resistance	15b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	16a	B_{TXO}	0.48	0.56	0.68	—
TXI Terminal Input Bias Current	16b	I_{TXI}	—	50	400	nA
TXO Terminal Positive Swing	16c	$V_{TXO}(+)$	—	25	60	mVdc
TXO Terminal Negative Swing	16d	$V_{TXO}(-)$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	17a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	17b	G_{STA}	0.40	0.45	0.54	V/V
STA Terminal Output Current	18	I_{STA}	50	100	250	μA
RXO Terminal Bias	19a	B_{RXO}	0.48	0.56	0.68	—
RXI Terminal Input Bias Current	19b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	19c	$V_{RXO}(+)$	—	1.0	20	mVdc
RXO Terminal Negative Swing	19d	$V_{RXO}(-)$	—	40	100	mVdc
TXL Terminal OFF Resistance	20a	$R_{TXL}(OFF)$	125	200	300	kΩ
TXL Terminal ON Resistance	20b	$R_{TXL}(ON)$	—	20	100	Ω
RM Terminal OFF Resistance	21a	$R_{RM}(OFF)$	125	180	300	kΩ
RM Terminal ON Resistance	21b	$R_{RM}(ON)$	410	570	770	Ω

PIN DESCRIPTION

(See Figure 28 for external component identifications.)

Pin	Designation	Function
1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500 mV) from a microprocessor port.
5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>500 mV and <3.0 volt).
10,9	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
11	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
12	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path and the transmit amplifier output are disabled.
13	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
14	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R1 and R2.
15	TXI	Transmit Amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R3 from TXO.
16	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R4. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R3/(R1 + R2) ratio.
17	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R5, R6, and C6.
18	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
19	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R9.
20	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.

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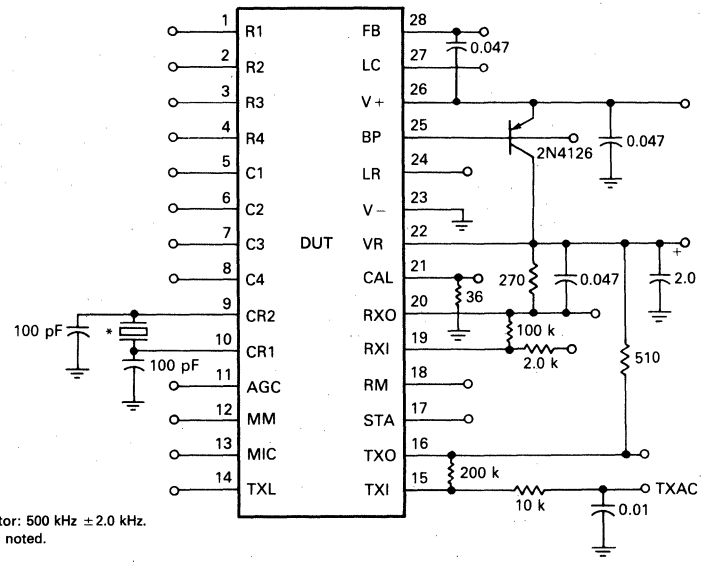
PIN DESCRIPTION (continued)

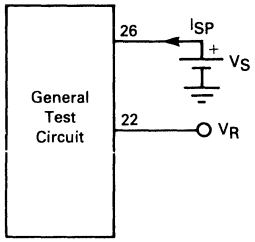
Pin	Designation	Function
21	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R11 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
22	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
23	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
24	LR	DC Load Resistor. Resistor R12 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
25	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
26	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
27	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
28	FB	FeedBack terminal for DTMF output. Capacitor C13 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.

FIGURE 6 — GENERAL TEST CIRCUIT



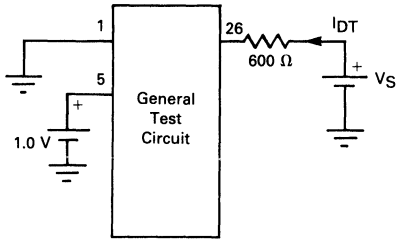
Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.

FIGURE 7 — TEST ONE



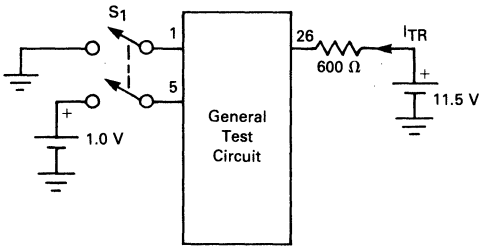
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 8 — TEST TWO



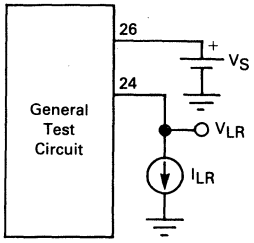
a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = |I_{DT}|_{26\ V} - |I_{DT}|_{11.5\ V}$

FIGURE 9 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:
$\Delta I_{TR} = |I_{TR}|_{S_1\ Closed} - |I_{TR}|_{S_1\ Open}$

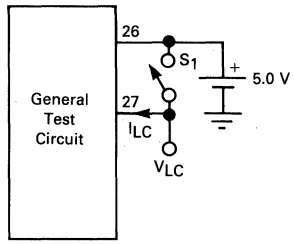
FIGURE 10 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

2

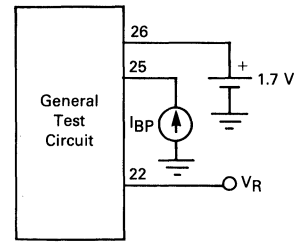
FIGURE 11 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

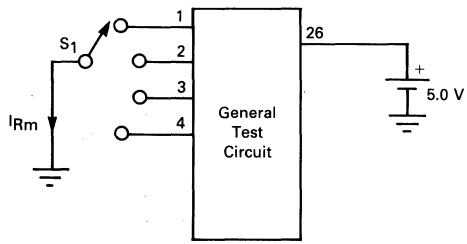
FIGURE 12 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = |V_R|_{0.0\ \mu A} - |V_R|_{150\ \mu A}$$

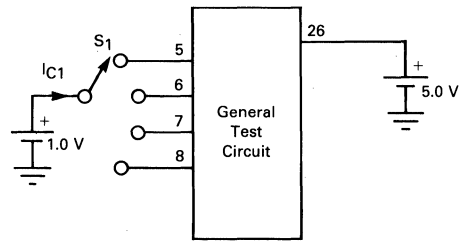
FIGURE 13 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

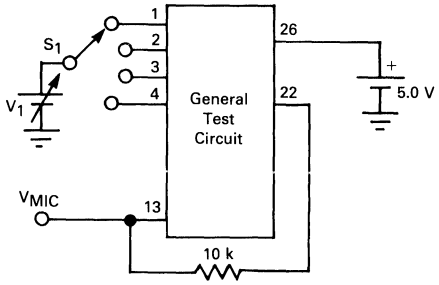
FIGURE 14 — TEST EIGHT



Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

FIGURE 15 — TEST NINE

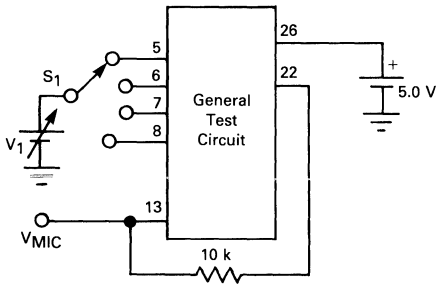


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 16 — TEST TEN

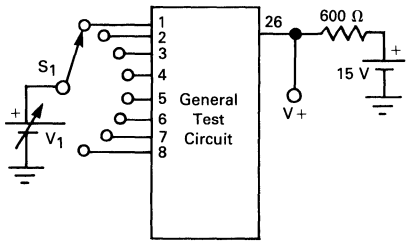


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc, Verify V_{MIC} is low (V_{MIC} <0.3 Vdc). Increase V_1 to 0.30 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 17 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

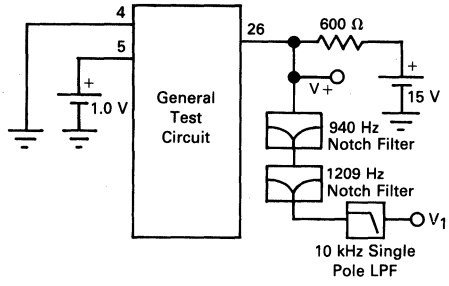
f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

2

FIGURE 18 — TEST TWELVE

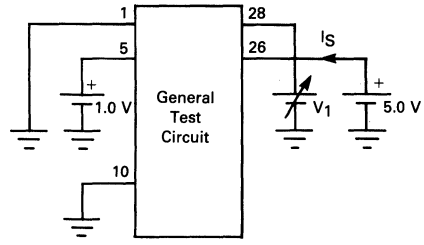


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 19 — TEST THIRTEEN

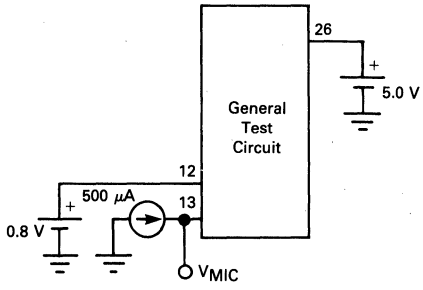


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

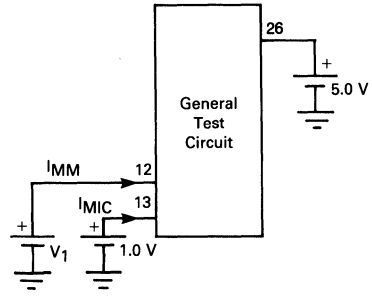
$$R_O = 1.0\text{ V} \div \left[I_S\Big|_{2.8\text{ V}} - I_S\Big|_{1.8\text{ V}} \right]$$

FIGURE 20 — TEST FOURTEEN



Measure V_{MIC}

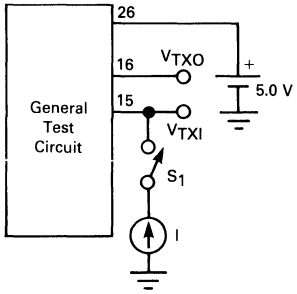
FIGURE 21 — TEST FIFTEEN



a. Set V_1 = 2.0 V and measure I_{MIC}.

b. Set V_1 = 5.0 V and measure I_{MM}.
Calculate: $R_{MM} = 5.0\text{ V} \div I_{MM}$

FIGURE 22 — TEST SIXTEEN



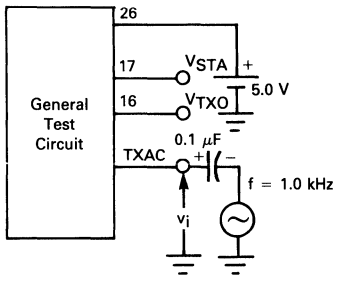
a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$

b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$

c. Close S_1 and set $I = -10\ \mu A$. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.

d. Close S_1 and set $I = +10\ \mu A$. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

FIGURE 23 — TEST SEVENTEEN



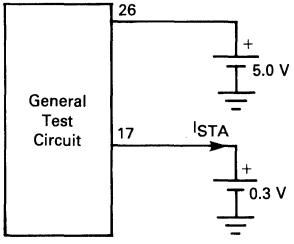
a. Set the generator for $v_i = 3.0\ mV_{rms}$. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 17a calculate:

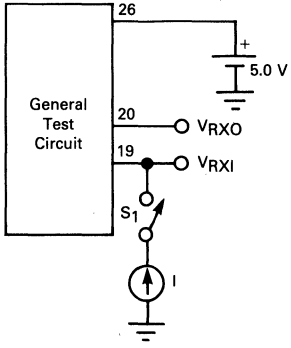
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 24 — TEST EIGHTEEN



Measure I_{STA}.

FIGURE 25 — NINETEEN



a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

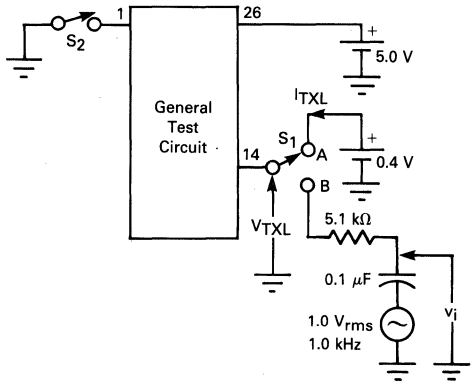
b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set $I = -10\ \mu A$. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set $I = +10\ \mu A$ and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

2

FIGURE 26 — TEST TWENTY

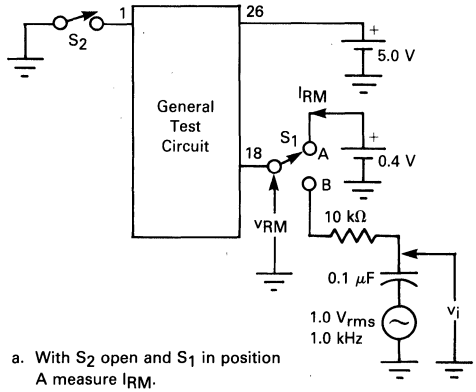


a. Set S_1 to position A with S_2 open. Measure I_{TXL}.
Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

FIGURE 27 — TEST TWENTY-ONE

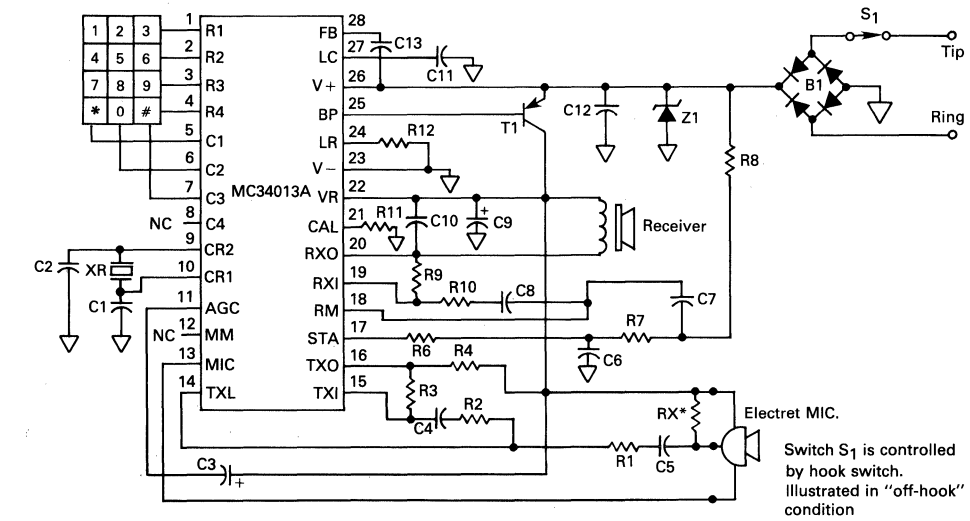


a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM}(OFF) = 0.4\ V \div I_{RM}$

b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:

$$R_{RM}(ON) = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

FIGURE 28 — APPLICATION CIRCUIT



*RX used with 2-terminal mike only.

APPLICATIONS INFORMATION

Figure 28 specifies a typical application circuit for the MC34013A. Complete listings of external components are provided at the end of this section along with nominal component values. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

Off-Hook DC Resistance

R12 conducts the dc line current in excess of the speech and dialer bias current. Increasing R12 increases the input resistance of the telephone for line currents above 10 mA. R12 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R11 controls the amplitude of the row and column DTMF tones. Decreasing R11 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R11 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R4 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R4 increases the transmit output signal at V+. R4 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R3. Increasing R3 increases the signal applied to R4 and the ac current driven through R4 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R4). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R9 adjusts the gain at the receiver amplifier. Increasing R9 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R8. R6, R7 and C6 determine the phase of the sidetone balance. The ac voltage at the junction of R6 and R7 should be 180° out of phase with the voltage at V+. R7 is selected such that the signal current in R7 is slightly greater than that in R8. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 28)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.

Resistors	Nominal Value	Description
R12	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R8, R10	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R8 subtracts from that in R7 to reduce sidetone in receiver.
R9	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R6, R7	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R7 should be opposite that in R8.
R4	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R3	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R1, R2	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R11	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

Semiconductors	Electret Mic	Receiver
B1 = MDA106A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A XR — muRata CSB500 or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

MC34014

Specifications and Applications Information

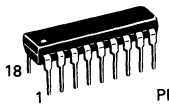
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations. The conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3″ wide) plastic DIP, a 20-pin surface mount PLCC package, and a 20-pin SOIC package.

- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

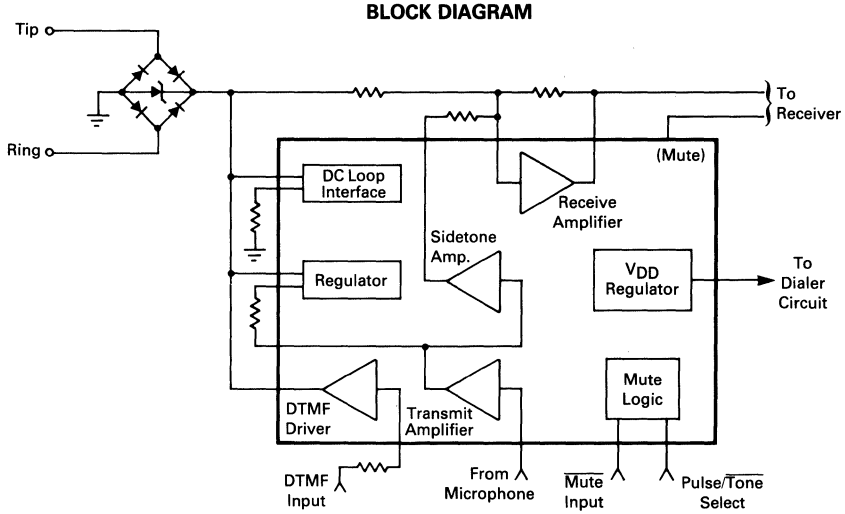


P SUFFIX
PLASTIC PACKAGE
CASE 707-02

DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03
SO-20L

FN SUFFIX
PLASTIC PACKAGE
CASE 775-02
PLCC-20

BLOCK DIAGRAM

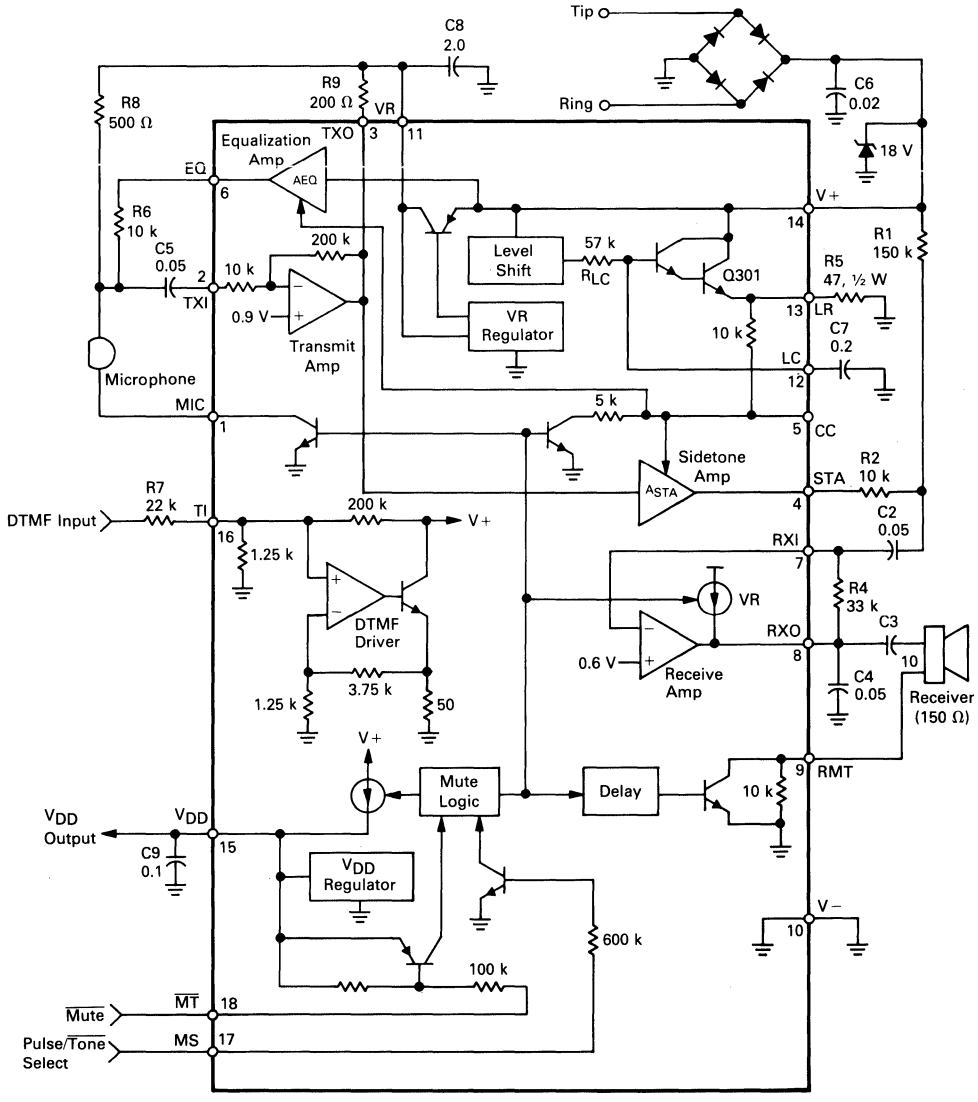


2

PIN DESCRIPTION (See Figure 1)

Pin # SOIC	Pin # PLCC	Pin # DIP	Name	Description
1	2	1	MIC	Microphone negative supply. Bias current from the electret microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off, disabling the microphone.
2	3	2	TXI	Transmit amplifier input. Input impedance is 10 kΩ. Signals from the microphone are input through capacitor C5 to TXI.
3	4	3	TXO	Transmit amplifier output. The ac signal current from this output flows through the V_R series pass transistor via R9 to drive the line at V+. Increasing R9 will decrease the signal at V+. The output is biased at ≈0.65 V to allow for maximum swing of ac signals. The closed loop gain from TXI to TXO is internally set at 26 dB.
4	6	4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
5	7	5	CC	Compensation Capacitor. A capacitor from CC to ground will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
7	8	6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the ac impedance of the circuit to increase.
8	9	7	RXI	Receive amplifier input. Input impedance is >100 kΩ. Signals from the line and sidetone amplifier are summed at RXI.
9	10	8	RXO	Receive Amplifier output. RXO is biased by a 2.5 mA current source. Feedback maintains the dc bias voltage at ≈0.65 V. Increasing R4 (between RXO and RXI) will increase the receive gain. C4 stabilizes the amplifier. C3 couples the signals to the receiver. The 2.5 mA current source is reduced to 0.4 mA when dialing.
10	11	9	RMT	Receiver Mute. The ac receiver current is returned to V− through an open collector NPN transistor and a parallel 10 kΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10 kΩ resistor in series with the receiver.
11	12	10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
12	13	11	VR	Regulated voltage output. The VR voltage is regulated at 1.2 V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5 V. Capacitor C8 stabilizes the regulator.
13	14	12	LC	DC load capacitor. An external capacitor C7 and an internal resistor form a low pass filter between V+ and LR to prevent ac signals from being loaded by the dc load resistor R5. Forcing LC to V− will turn off the dc load current and increase the V+ voltage.
14	15	13	LR	DC load resistor. Resistor R5 from LR to V− determines the dc resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode).
15	16	14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the MC34014 are powered by V+.
17	18	15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3 V. The nominal output current is increased from 550 μA to 2 mA when dialing. Capacitor C9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
18	19	16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R7. The current at TI is amplified to drive the line at V+. Increasing R7 will reduce the DTMF output levels. The input impedance at TI is nominally 1.25 kΩ.
19	20	17	MS	Mode select. This pin is connected through an internal 600 kΩ resistor to the base of an NPN transistor. A Logic "1" (>2.0 V) selects the pulse dialing mode. A Logic "0" (<0.3 V) selects the tone dialing mode.
20	1	8	$\overline{MT}$	Mute input. $\overline{MT}$ is connected through an internal 100 kΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A Logic "0" (<1.0 V) will mute the network for either pulse or tone dialing. A Logic "1" (>V_{DD} − 0.3 V) puts the MC34014 into the speech mode.

FIGURE 1 — TEST CIRCUIT



NOTE: Pin numbers are for 18 pin DIP.

2

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V−, T_A = 25°C) (See Note 1.)

Parameter	Value	Units
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0, +6	Vdc
V_{LR}	−1.0, V+ − 3.0	Vdc
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

NOTE 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (T_A = 25°C)

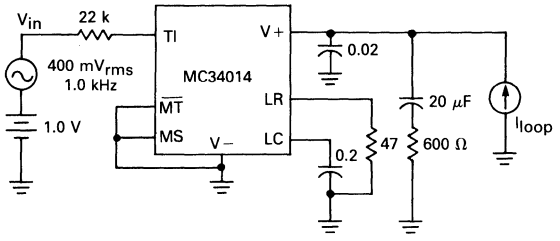
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V+ Voltage	V+				Vdc
I_{loop} = 20 mA (Speech/Pulse Mode)		2.6	3.2	3.8	
I_{loop} = 30 mA (Speech/Pulse Mode)		3.0	3.7	4.4	
I_{loop} = 120 mA (Speech/Pulse Mode)		7.0	8.2	9.5	
I_{loop} = 20 mA (Tone Mode)		4.1	4.9	5.7	
I_{loop} = 30 mA (Tone Mode)		4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	I+				mA
V+ = 1.7 V (Speech Mode)		4.0	6.6	8.5	
V+ = 12 V (Speech/Pulse Modes)		5.5	8.4	12.5	
V+ = 12 V (Tone Mode)		6.0	8.8	14.0	
LR Level Shift (V+ − V_{LR})	ΔV_{LR}				Vdc
(Speech/Pulse Mode)		—	2.7	—	
(Tone Mode)		—	4.3	—	
LC Terminal Resistance	R_{LC}	36	57	94	kΩ
VOLTAGE REGULATORS					
VR Voltage (V+ = 1.7 V)	V_R	1.1	1.2	1.3	Vdc
Load Regulation (0 mA < I_R < 6.0 mA)	ΔV_{RLD}	—	20	—	mV
Line Regulation (2.0 V < V+ < 6.5 V)	ΔV_{RLN}	—	25	—	mV
V_{DD} Voltage (V+ = 4.5 V)	V_{DD}	3.0	3.3	3.8	Vdc
Load Regulation (0 < I_{DD} < 1.6 mA) (Dialing Mode)	ΔV_{DDLD}	—	0.25	—	Vdc
Line Regulation (All Modes) (4.0 V < V+ < 9.0 V)	ΔV_{DDLN}	—	50	—	mV
Max. Output Current (Speech Mode)	I_{DDSP}	375	550	1000	μA
Max. Output Current (Dialing Mode)	I_{DDDL}	1.6	2.0	3.6	mA
V_{DD} Leakage Current (V+ = 0, V_{DD} = 3.0 V)	I_{DDLK}	—	—	1.5	μA
SPEECH AMPLIFIERS					
Transmit Amplifier					
Gain (TXI to TXO)	A_{TXO}	—	20	—	V/V
TXO Bias Voltage (Speech/Pulse Mode)	V_{TXOSP}	0.45	0.52	0.60	x V_R
TXO Bias Voltage (Tone Mode Mode)	V_{TXODL}	VR−25	VR−5.0	—	mV
TXO High Voltage (Speech/Pulse Mode)	V_{TXOH}	VR−25	VR−5.0	—	mV
TXO Low Voltage (Speech/Pulse Mode)	V_{TXOL}	—	125	250	mV
TXI Input Resistance	R_{TXI}	—	10	—	kΩ
Receive Amplifier					
RXO Bias Voltage (All Modes)	V_{RXO}	0.45	0.52	0.60	x VR
RXO Source Current (Speech Mode)	I_{RXOSP}	1.5	2.0	—	mA
RXO Source Current (Pulse/Tone Mode)	I_{RXODL}	200	400	—	μA
RXO High Voltage (All Modes)	V_{RXOH}	VR−100	VR−50	—	mV
RXO Low Voltage (All Modes)	V_{RXOL}	—	50	150	mV

ELECTRICAL CHARACTERISTICS — (continued) (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE, RECEIVER CONTROLS					
MIC Saturation Voltage (Speech Mode, I = 500 μA)	$V_{OL_{MIC}}$	—	50	125	mV
MIC Leakage Current (Dialing Mode, Pin 1 = 3.0 V)	$I_{MIC_{LK}}$	—	0	5.0	μA
RMT Resistance (Speech Mode) (Dialing Mode)	$R_{RMT_{SP}}$ $R_{RMT_{DL}}$	— 5.0	8.0 10	15 18	Ω kΩ
RMT Delay (Dialing to Speech)	$t_{\overline{RMT}}$	2.0	4.0	20	ms
DIALING INTERFACE					
$\overline{MT}$ Input Resistance	R_{MT}	58	100	—	kΩ
$\overline{MT}$ Input High Voltage	V_{IHMT}	V_{DD} − 0.3	—	—	Vdc
$\overline{MT}$ Input Low Voltage	V_{ILMT}	—	—	1.0	Vdc
MS Input Resistance	R_{MS}	280	600	—	kΩ
MS Input High Voltage	V_{IHMS}	2.0	—	—	Vdc
MS Input Low Voltage	V_{ILMS}	—	—	0.3	Vdc
TI Input Resistance	R_{TI}	—	1.25	—	kΩ
DTMF Gain (See Figure 2) (V+/V_{in})	A_{DTMF}	3.2	4.8	6.2	dB
SIDETONE AMPLIFIER					
Gain (TXO to STA) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{STA}	 — — — —	 −15 −21 −15 −21	 — — — —	dB
STA Bias Voltage (All Modes)	V_{STA}	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER					
Gain (V+ to EQ) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{EQ}	 — — — —	 −12 −2.5 −12 −2.5	 — — — —	dB
EQ Bias Voltage (Speech Mode) @ V_{LR} = 0.5 V (Pulse Mode) @ V_{LR} = 0.5 V (Speech, Pulse) @ V_{LR} = 2.5 V	V_{EQ}	 — — —	 0.66 1.3 3.3	 — — —	Vdc

NOTE: Typical values are not tested or guaranteed.

FIGURE 2 — DTMF DRIVER TEST



2

SYSTEM SPECIFICATIONS (T_A = 25°C) (See Figures 1–4)

Parameter		Min	Typ	Max	Unit
Tip-Ring Voltage (including polarity guard bridge drop of 1.4 V)					Vdc
(Speech Mode)	I_{loop} = 5.0 mA	—	2.4	—	
	I_{loop} = 10 mA	—	3.9	—	
	I_{loop} = 20 mA	—	4.6	—	
	I_{loop} = 40 mA	—	5.6	—	
	I_{loop} = 60 mA	—	6.6	—	
Transmit					
Gain from V_S to V+ (Figure 3) (I_{loop} = 20 mA)		28	30	31	dB
Gain change as I_{loop} is increased to 60 mA		−6.0	−4.5	−3.6	dB
Distortion		—	2.0	—	%
Output noise		—	11	—	dBrnc
Receive					
V_{RXO}/V_S (f = 1.0 kHz, I_{loop} = 20 mA) (See Figure 4)		−16	−15	−13	dB
Receive gain change as I_{loop} is increased to 60 mA		−5.0	−3.0	−2.0	dB
Distortion		—	2.0	—	%
Sidetone Level					dB
$V_{RXO}/V+$ (Figure 3)					
	I_{loop} = 20 mA	—	−36	—	
	I_{loop} = 60 mA	—	−21	—	
Sidetone Cancellation $\left[\frac{V_{RXO}}{V+}\text{ (Figure 4)}\right]$ dB − $\left[\frac{V_{RXO}}{V+}\text{ (Figure 3)}\right]$ dB	I_{loop} = 20 mA	20	26	—	dB
DTMF Driver		3.2	4.8	6.2	dB
$V+/V_{in}$ (Figure 2)	I_{loop} = 20 mA				
AC Impedance					Ω
Speech mode (incl. C_6, See Figure 4)	I_{loop} = 20 mA	—	750	—	
$Z_{ac} = (600)V+/(V_S - V+)$	I_{loop} = 60 mA	—	300	—	
Tone mode (including C_6)	20 mA < I_{loop} < 60 mA	—	1650	—	

NOTE: Typicals are not tested or guaranteed.

FIGURE 3 — TRANSMIT AND SIDETONE LEVEL TEST

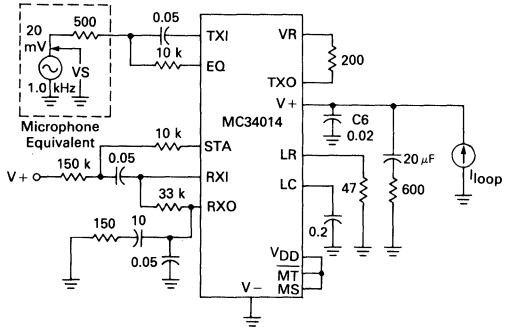
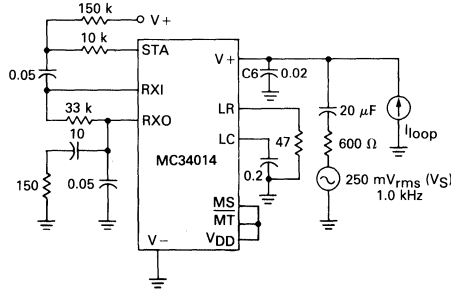


FIGURE 4 — AC IMPEDANCE, RECEIVE AND SIDETONE CANCELLATION TEST



DESIGN GUIDELINES (Refer to Figure 1)

INTRODUCTION

The MC34014 is a speech network meant for connection to the Tip & Ring lines through a polarity guard bridge. The circuit incorporates four amplifiers: transmit, receive, sidetone, and equalization. Some parameters of each amplifier are set by external components, and in addition, the gains of the sidetone and equalization amplifiers vary with loop current.

The line interface portion determines the dc voltage versus loop current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing, and tone (DTMF) dialing. When switching to either dialing mode some parameters of the various sections are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

TABLE 1 — OPERATING PARAMETERS AS A FUNCTION OF OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift ($V+ - V_{LR}$)	2.7 V	2.7 V	4.3 V
V_{DD} Source Current	550 μA	2.0 mA	2.0 mA
Transmit Amplifier	Functional	Functional	Inoperative
MIC Switch (Pin 1)	On	Off	Off
Equalization Amplifier	See Transfer Curves — Figure 8		
Sidetone Amplifier	See Transfer Curves — Figure 6		
Receive Amplifier Output Current	2.5 mA	400 μA	400 μA
RMT (Pin 9) Impedance	8.0 Ω	10 kΩ	10 kΩ
DTMF Amplifier	Inoperative	Inoperative	Functional
CC Voltage	$V_{LR}/3$	V_{LR}	V_{LR}

DC LINE INTERFACE (Figure 5)

The dc line interface circuit (Pins 10, 12–14) sets the dc voltage characteristics with respect to the loop current. The loop current enters at Pin 14 where the internal circuitry of the MC34014 draws 5–6 mA. Pin 3 sinks (typically) 3 mA through R_9. The remainder of the loop current is passed through Q_{301} and R_5. The resulting voltage across the entire circuit is therefore equal to the voltage across R_5, plus the level shift voltage from Pin 13 (LR) to Pin 14 ($V+$), nominally 2.7 volts in the speech and pulse modes. In the tone mode, the level shift increases to 4.3 volts, the internal current changes slightly (Figure 6), and the current required at Pin 3 decreases to near zero. These changes increase the equivalent dc resistance of the circuit, raising the voltage at $V+$ to ensure adequate voltage at V_{DD} for the external tone dialer. See Figure 7 for typical voltage versus loop current characteristics.

Capacitor C_7 at Pin 12 provides high frequency rolloff (above 10 Hz) so that R_5 does not load down the speech and DTMF signals.

The voltage at V_R is an internally regulated 1.2 volt supply which provides the bias currents for the microphone and the transmit amplifier output (Pin 3), as well as internal bias for the various amplifiers. Capacitor C_8 stabilizes the regulator. The use of an (internal) PNP transistor allows V_R to be regulated with a $V+$ voltage as low as 1.5 volts.

FIGURE 5 — DC LINE INTERFACE

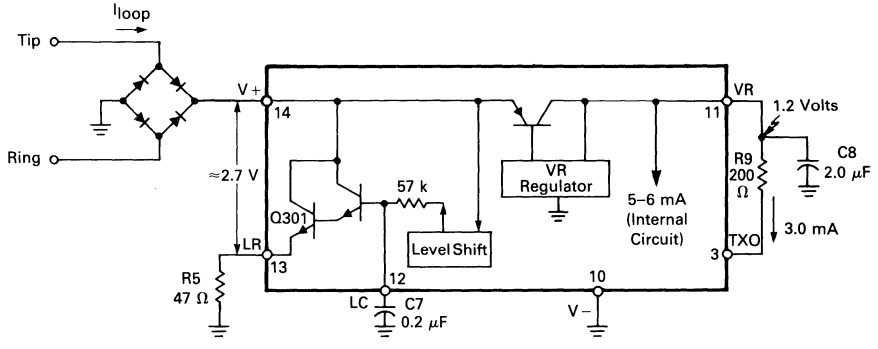


FIGURE 6 — INTERNAL CURRENT versus VOLTAGE

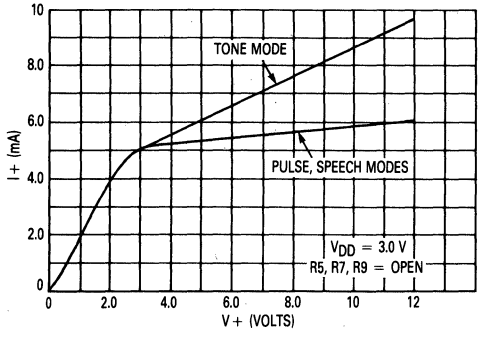
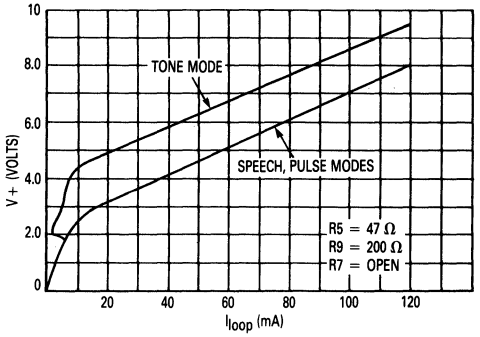


FIGURE 7 — CIRCUIT VOLTAGE versus LOOP CURRENT



TRANSMIT AMPLIFIER

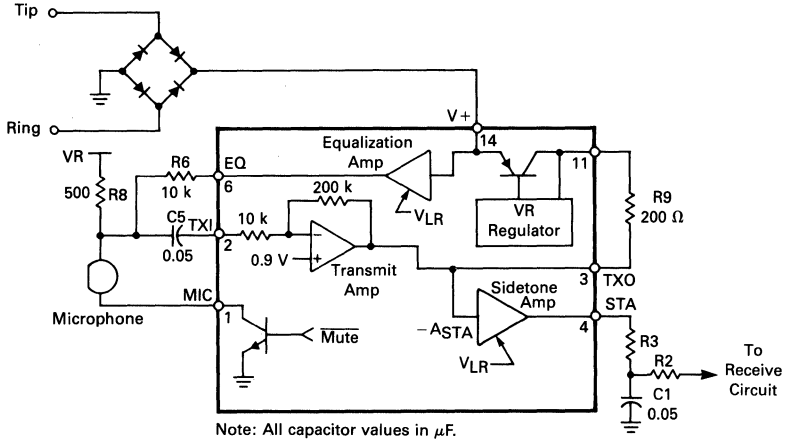
The transmit amplifier (from TXI to TXO) is inverting, with a fixed internal gain of 20 V/V (26 dB), and a typical input impedance of 10 kΩ (Figure 8). The input bias currents are internally supplied, allowing capacitive coupling of the microphone signals to the amplifier.

In the speech and pulse modes, the dc bias level at TXO is typically 0.52 x VR (≈0.63 V), which permits the output to swing 0.55 volts in both positive and negative directions without clipping. The ac voltage signal at TXO (the amplified speech signal) is converted to an ac current by Rg. The ac current passes through the VR series pass transistor to V+, modulating the loop current. The voltage signal at V+ is out of phase with the signal at TXI.

In the tone dialing mode, the TXO dc bias level is clamped at approximately VR-10 mV, rendering the amplifier inoperative. This action also reduces the TXO bias current from 3.0 mA to less than 125 μA.

MIC (Pin 1) is connected to an open-collector NPN transistor, and provides the ground path for the microphone bias current. In either dialing mode, the transistor is off, disabling the microphone.

FIGURE 8 — TRANSMIT SECTION



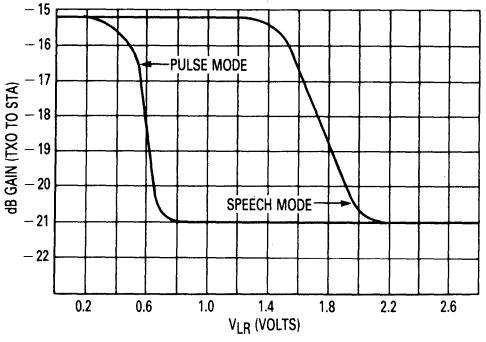
Note: All capacitor values in μF.

SIDETONE AMPLIFIER

The sidetone amplifier provides inversion of the TXO signal for the reduction of the sidetone signal at the receive amplifier (Figure 8). Resistors R_2 and R_3 determine the amount of sidetone cancellation. Capacitor C_1 provides phase shift to compensate for the phase shift created by the complex impedance of the Tip & Ring lines.

The gain of the sidetone amplifier varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −15 dB (0.17 V/V) at low loop currents, and the minimum gain is −21 dB (0.09 V/V) at high loop current (see Figure 9 for transfer curves). For example, using 47 Ω for R_5, the gain would begin to decrease at ≈30 mA, and would stop decreasing at ≈57 mA (speech mode). The dc bias voltage at STA (Pin 4) changes slightly (≈50 mV) with variations in loop current. The output is inverted from TXO, which is the input to this amplifier. Since the transmit amplifier is inoperative in the tone dialing mode, the sidetone amplifier is also inoperative in that mode.

FIGURE 9 — SIDETONE AMPLIFIER GAIN



RECEIVE AMPLIFIER

The gain of the receive amplifier (from V+ to RXO) is determined according to the following equation (refer to Figure 10):

$$\frac{V_{RXO}}{V+} = \frac{R_4}{R_1} + \frac{(X_C//R_2)\,(A_{EQ})\,(A_{TXO})\,(A_{STA}) \times R_A \times R_4}{((X_C//R_2)+R_3)\,(R_A+R_6) \times R_2}$$

Where R_A = R_8//10 kΩ (10 kΩ = R_{in} of T_X Amp)
A_{EQ} = Gain of Equalization Amp
A_{TXO} = Gain of Transmit Amp (20 V/V)
A_{STA} = Gain of sidetone Amp
X_C = Impedance of C_1 at frequency of interest

The waveform at STA (Pin 4) is in phase with that at V+ (for receive signals), hence the plus sign between the terms. Due to the variations of A_{EQ} and A_{STA} with loop current, the receive gain will vary by ≈1.5 dB. If capacitor C_1 is not used, the above equation is simplified by deleting the terms containing X_C.

The output at RXO is inverted from V+ in the receive mode. In the transmit mode, the V+-to-RXO phase relationship depends on the amount of sidetone cancellation (determined by R_2 and R_3 and C_1), and can vary from 0° to 180°.

In the speech mode, the output current capability (at RXO) is typically 2.0 mA. In either dialing mode, the current capability is reduced to 400 μA in order to reduce internal current consumption. This feature is beneficial when this device is used in conjunction with a line-powered speakerphone circuit, such as the MC34018, where the majority of the loop current is needed for the speakerphone.

RMT (Pin 9) is the return path for the receiver's ac current. This pin is internally connected to an open collector NPN transistor, paralleled by a 10 kΩ resistor. In the speech mode, the transistor is on, providing a low impedance from RMT to ground. In either dialing mode, the transistor is off, muting the receive signal. This prevents loud "clicks" or loud DTMF tones from being heard in the receiver during dialing. When switching from either dialing mode to the speech mode ($\overline{MT}$ switches from low to high), the RMT pin switches back to a low impedance after a delay of 2–20 ms. The delay reduces clicks in the receiver associated with switching from the dialing to speech mode.

EQUILIZATION AMPLIFIER

The equalization amplifier gain varies with loop current, and is configured in the circuit so as to cause a variation of the network ac impedance (when looking in from the Tip & Ring lines). The gain varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −2.5 dB (0.75 V/V) at high loop current, and the minimum gain is −12 dB (0.25 V/V) and low loop current (see Figure 11 for transfer curve). For example, using 47 Ω for R_5, the gain would begin to increase at ≈30 mA, and would stop increasing at ≈57 mA (speech mode). The output signal is in phase with the signal at V+, which is the input to this amplifier.

The dc bias level at EQ (Pin 6) varies with the voltage at LR (Pin 13) according to the curve of Figure 12. In most applications, this level shift is of little consequence, and may be ignored. If a particular circuit configuration should be sensitive to the shift, however, the output signal at EQ may be ac coupled to the rest of the circuit.

The equalization amplifier remains functional in all three modes, although in the tone mode, its function has no consequence when the circuit is configured as shown in Figure 1.

V_{DD} REGULATOR

The V_{DD} regulator is a shunt type regulator which supplies a nominal 3.3 volts for external dialers, and/or

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other circuitry. In the speech mode, the output current capability at Pin 15 is typically 550 μA. In either dialing mode, the current capacity is increased to 2.0 mA.

V_{DD} will be regulated whenever V+ is >300 mV above the regulated value. As V+ is lowered, and the internal pass transistor becomes saturated, the circuit steers current away from the external load through an internal current source, in order that the V_{DD} capacitor (C9) does not load down speech and DTMF signals at V+. As V+ is lowered below 1 volt, Pin 15 switches to a high impedance state to prevent discharging of any storage capacitors, or batteries used for memory retention.

The V_{DD} voltage is unaffected by the choice of operating mode.

DIALER INTERFACE

The dialer interface consists of the mode control pins, $\overline{MT}$ and MS (Pins 18 and 17), and the DTMF current amplifier.

The $\overline{MT}$ pin, when at a Logic "1" (> V_{DD} − 0.3 V), sets the circuit into the speech mode, independent of the state of the MS pin. When the $\overline{MT}$ pin is at a Logic "0" (< 1.0 V), the dialing mode is determined by the MS pin. When MS is at a Logic "1" (> 2.0 V), the circuit is in the pulse dialing mode, and when at a Logic "0" (< 0.3 V) the tone (DTMF) mode is in effect.

The input impedance of the $\overline{MT}$ pin is typically 100 kΩ, with the input current flowing out of the pin (from V_{DD}). The input impedance of the MS pin is typically 600 kΩ, and the input current flows into the pin (Figure 1).

The DTMF amplifier (Figure 13) is a current amplifier which transmits DTMF signals to the V+ pin, and consequently onto the Tip & Ring lines. Waveforms from a DTMF dialer are input at TI (Pin 16) through a current limiting resistor (R_7). Negative feedback around the amplifier reduces the overall gain so that return loss specifications may be met. The voltage gain is calculated using the following equation:

$$\frac{V+}{V_i} = \frac{80\ R_E}{(1\ +\ 0.795R_7\ +\ 0.4R_ER_7)}$$

(R_E, R_7 in kΩ)
where $R_E = R_L//2$ kΩ (2 kΩ = internal dynamic impedance)

Using 22 kΩ for R_7, and 600 Ω for R_L, the voltage gain is a nominal 4.3 dB. The minimum loop current at which the circuit of Figure 1 will operate without distortion is 12 mA.

The DTMF amplifier is functional only in the tone dialing mode, and the waveform at V+ is inverted from that at TI. The TI pin requires a dc bias current (into the pin) of 20–50 μA, which may be supplied by the Tone dialer circuit, or by using the biasing scheme of Figure 14.

CC (PIN 5)

The CC pin (Compensation Capacitor) has two functions: 1) to provide equalization loop stability where the normal stabilizing components are ineffective; and 2) to allow optional control of the equalization functions.

In most applications, the capacitor at LC (Pin 12) provides the required stability, and no further compensation is required. In applications where changes are forced at Pin 12 and/or 13 (e.g., see Figure 23), the LC capacitor's effectiveness may be lost. The addition of a 10 μF capacitor to Pin 5 will provide the required additional compensation.

The CC pin may be used to force the loop length compensation circuits to specific modes. Grounding CC will set the sidetone and equalization amplifiers at the low loop current values. Connecting CC to V_R will set the amplifiers at the high loop current values.

Variations in the curves of Figures 9 and 11 may be obtained by using external resistors from LR to CC, and from CC to V−.

FIGURE 10 — RECEIVE CIRCUIT

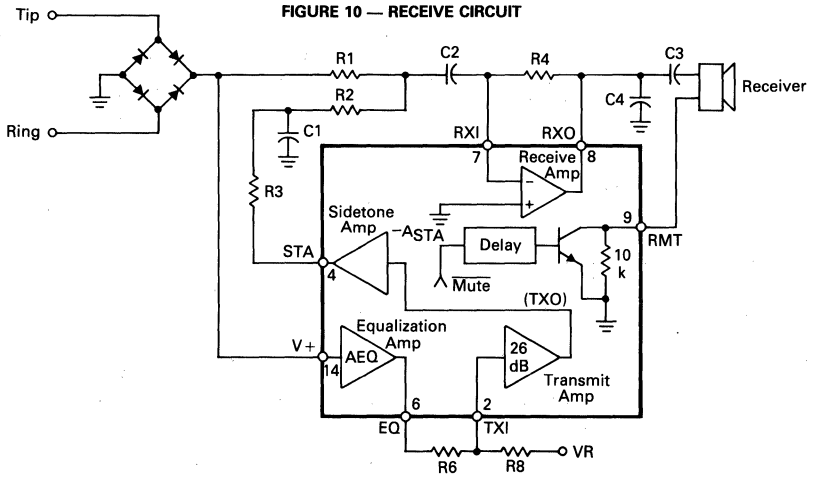


FIGURE 11 — EQUALIZATION AMPLIFIER GAIN

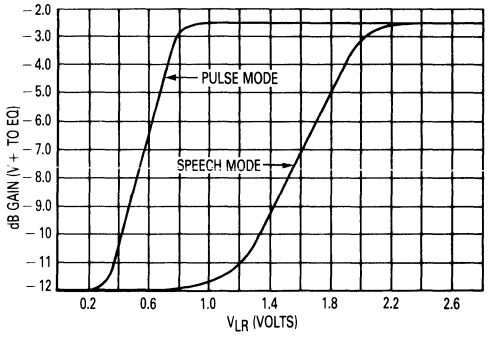


FIGURE 12 — EQ (PIN 6) DC VOLTAGE

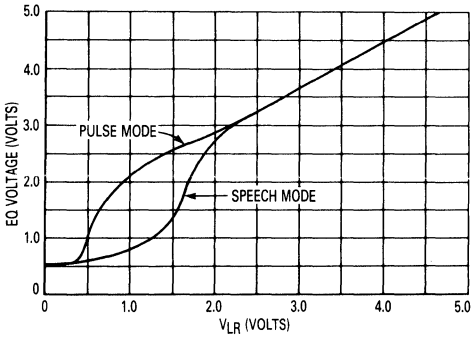


FIGURE 13 — DTMF TONE DIALER

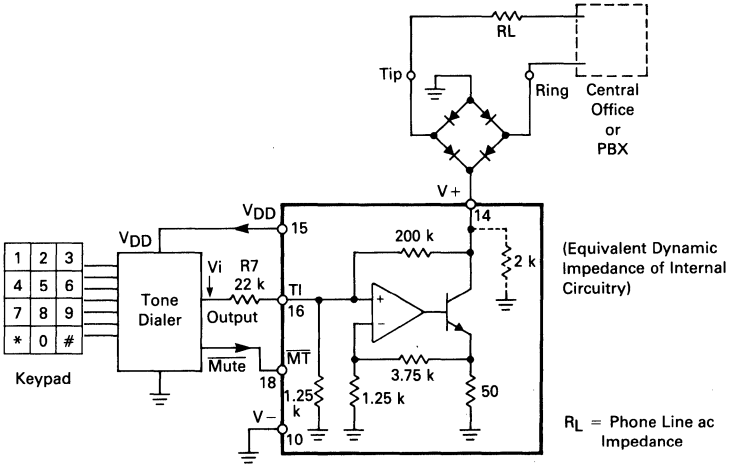
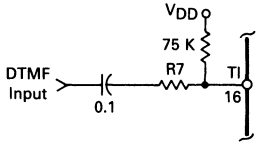


FIGURE 14 — INPUT BIASING



APPLICATIONS INFORMATION

AC IMPEDANCE

One of the basic problems with early telephones is that the performance varied with different line lengths (distance from the Central Office to the telephone). If a particular phone were optimized for short loops and then connected to a long loop, both the transmitted and receive signals would be difficult to hear. On the other hand, phones optimized for long loops would then be annoyingly loud on short loops. The process of equalization is one whereby the performance is forced to vary with loop length inversly to the expected variations. Monitoring of loop length is accomplished by monitoring the loop current at the telephone. In the MC34014, loop length equalization is provided by varying the ac impedance of the telephone circuit. In this manner the MC34014 mimics a passive network, with varistors providing the equalization.

Figure 15 depicts the situation in the receive mode. The receive signal coming from the Central Office is V_S and is independent of the loop length. Z_R is the ac impedance of the Central Office, nominally 900 Ω. Z_L is the characteristic impedance of the phone line, and is a nominal 600 Ω. The signal applied to the line (V_1) is therefore a portion of V_S. That signal is attenuated by the distributive impedance of the phone line, with a resulting signal V_2 at the telephone. The amplitude of V_2 depends on the amount of attenuation, the impedance of the phone line at the telephone and the ac impedance of the telephone (Z_{ac}), according to:

$$V_2 = \frac{V_1' \times Z_{ac}}{Z_{ac} + Z_L}$$

where V_1' is the equivalent signal source at the receive end of the phone line, providing the signal V_2 through the impedance equal to the characteristic impedance of the line (Z_L). The value of V_1' depends on how much V_1 has been attenuated by the length of phone line. By increasing Z_{ac} on long loops, V_2 is a greater portion of V_1', resulting in a stronger receive signal at the telephone.

FIGURE 15 — RECEIVE MODE

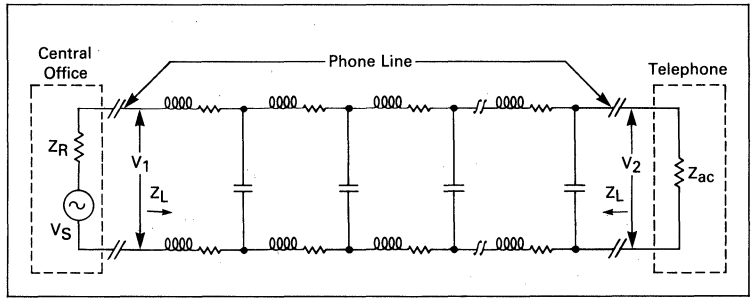
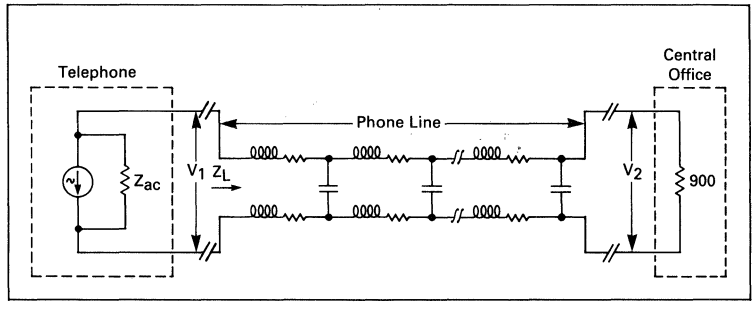


Figure 16 depicts the situation in the transmit mode. In this mode, the MC34014 is an ac current source, with a finite output impedance, modulating the loop current. The voltage signal V_1 is therefore equal to the ac signal current acting on Z_{ac} in parallel with the characteristic impedance of the phone line (Z_L). The signal is attenuated by the distributive impedance of the phone line, and so only a portion of that signal (V_2) appears at the Central Office. By increasing Z_{ac} on long loops, V_1 is increased, resulting in a higher signal level at V_2.

FIGURE 16 — TRANSMIT MODE



The ac impedance of the telephone circuit is determined by the transmit amplifier, equalization amplifier, and external resistors R_6, R_8, and R_9. In Figure 17, a portion of the receive signal at V+ appears at EQ. That signal is reduced at TXI by the R_8-R_6 divider (the electret microphone is a high impedance). The signal at TXI is then amplified by 20, and that signal (at TXO) is converted to an ac current by R9. The ac impedance of the circuit is therefore $V+/I_{TXO}$, and is defined by the following equation:

$$Z_{ac} = \frac{(1 + R_8/R_6)(R_9)}{20 \times A \times (R_8/R_6)}$$

where A = the gain of the equalization amplifier (0.25 to 0.75)

Since the gain of the equalization amplifier varies by a factor of 3, the ac impedance will vary the same amount. Using the resistor values indicated in Figure 1, the ac impedance will vary from 280 Ω (short loop) to 840 Ω (long loop).

When calculating or measuring the ac impedance, capacitor C_6 (≈8.0 kΩ at 1.0 kHz) and the dynamic impedance of the MC34014 (≈10 kΩ) must be taken into account. If the microphone has an impedance lower than that of a typical electret, then its dynamic impedance must be accounted for in the above equation.

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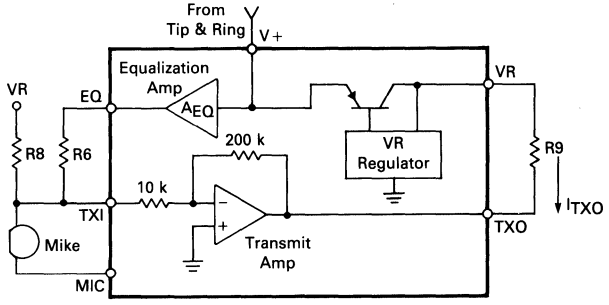
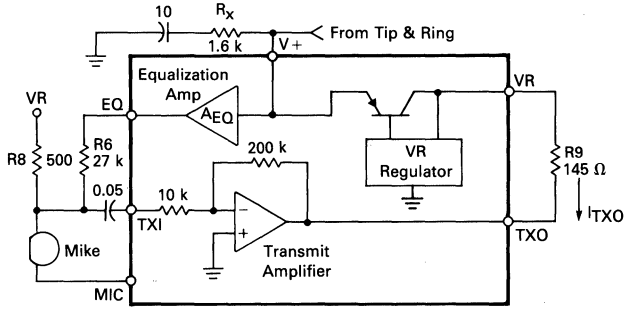
FIGURE 17 — DETERMINING AC IMPEDANCE



If a variation in Z_{ac} of less than 3:1 is desired, the circuit configuration of Figure 18 may be used. The ac impedance is the parallel combination of R_x and the impedance presented by the remainder of the circuit. With the values shown in Figure 18, the ac impedance varies from 400 Ω to 800 Ω.

FIGURE 18 — REDUCED AC IMPEDANCE VARIATION



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TRANSMIT DESIGN PROCEDURE

Referring to Figure 17, first select R_9 for the desired maximum output level at Tip & Ring, assuming a signal level at TXO of 1.0 V p-p. The maximum signal level at Tip & Ring will be approximately:

$$\frac{(V_{TXO})\ (Z_L)}{R_9}$$

where Z_L is the characteristic ac impedance of the phone line. Capacitor C_6 and the ≈10 kΩ dynamic impedance of the MC34014 must also be considered in the above computation, since they are in parallel with Z_L.

The next step is to select the R_6/R_8 ratio, according to the required Z_{ac}, using the equation on the previous page. Then R_8 is selected to set the microphone sensitivity. R_8 is typically in the range of 0.5 k to 1.5 kΩ, and is dependent on the characteristics of the microphone. R_6 is then calculated from the above mentioned ratio.

HANDSET/HANDS-FREE TELEPHONE

Figure 23 indicates a circuit using the MC34014 speech network, MC34018 speakerphone circuit, and the MC34017 tone ringer to provide a complete telephone/speakerphone. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, and placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the MC34014 to the pulse dialing mode to mute the handset microphone and receiver when using the speakerphone. To compensate for the different equalization response of the MC34014 when in the pulse dialing mode (Figures 9 and 11), the 47 Ω resistor normally found at Pin 13 of the MC34014 is instead divided into two resistors (33 Ω and 15 Ω). This arrangement provides similar equalization response in both the handset and in the speakerphone modes. Since the LC capacitor (Pin 12) is ineffective in the speakerphone mode, a capacitor is added at Pin 5 (CC) to provide compensation for the equalization loop when the speakerphone mode is in effect.

FIGURE 19 — ALTERNATE MICROPHONE BIAS

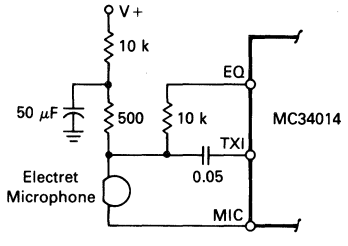
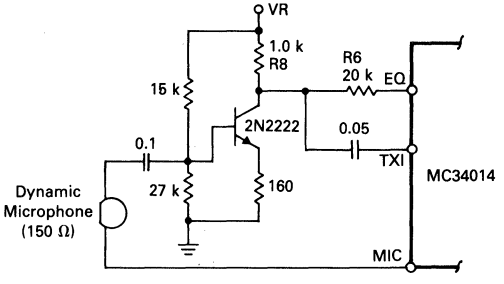


FIGURE 20 — INTERFACING A DYNAMIC MICROPHONE



The overall gain from the microphone to V+ will vary with loop current due to the influence of the equalization amplifier on TXI. The signal at EQ is out of phase with that at TXI, therefore the signal at V+ decreases as loop current (and the EQ signal) increases. Variations are typically 2.0 to 5.0 dB and depend largely on the impedance characteristics of the microphone.

ALTERNATE MICROPHONE BIASING

In the event that the microphone cannot be properly biased from the 1.2 volt VR supply, a higher voltage can be obtained by biasing from the V+ supply. The configuration shown in Figure 19, provides a higher voltage to the microphone, and also filters the speech signals at V+ from reaching it, preventing an oscillatory loop from forming. The maximum voltage limit of the microphone must be considered when biasing this way.

If a dynamic microphone is to be used in place of an electret unit, the circuit in Figure 20 will buffer its low impedance from the MC34014 circuit, maintaining the high impedance required at the junction of R_8 and R_6. The circuit shown provides a gain of ≈2.6 for the microphone signals, and can be adjusted by varying the 160 Ω resistor.

SWITCHABLE TONE/PULSE TELEPHONE

Figure 21 indicates a switchable tone/pulse telephone circuit using the MC145412 tone/pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer is programmable, and can store up to 10 phone numbers. As can be seen, the interface to the MC34014 is straightforward.

PULSE ONLY TELEPHONE

Figure 22 indicates a pulse only telephone circuit using the MC145409 pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer has last number redial, and provides a pacifier tone to the receiver during dialing.

FIGURE 21 — COMPLETE TELEPHONE WITH PULSE/TONE DIALING

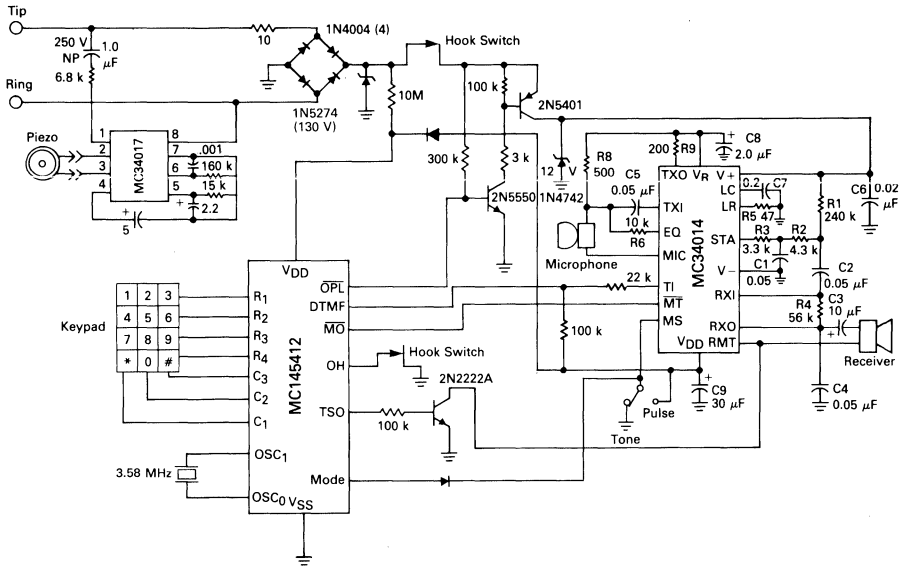
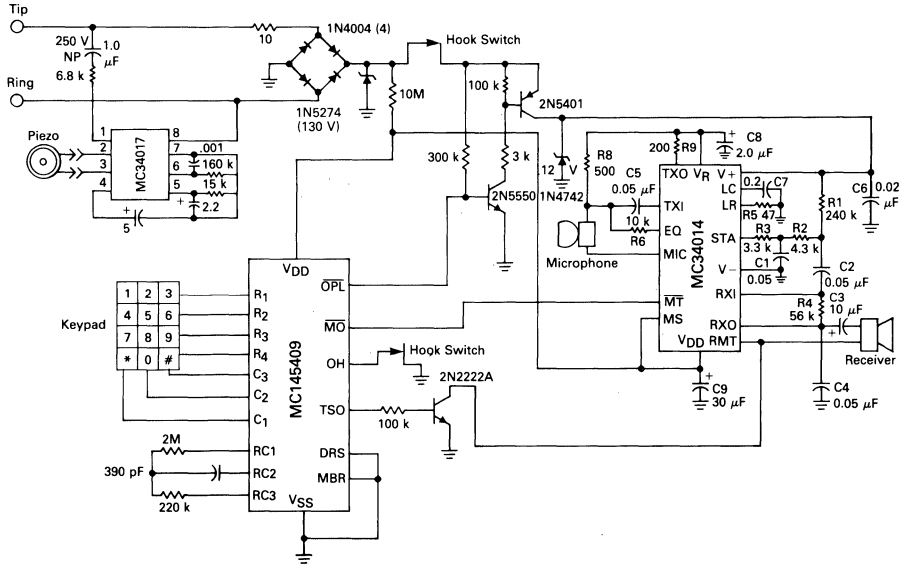


FIGURE 22 — COMPLETE TELEPHONE WITH PULSE DIALING



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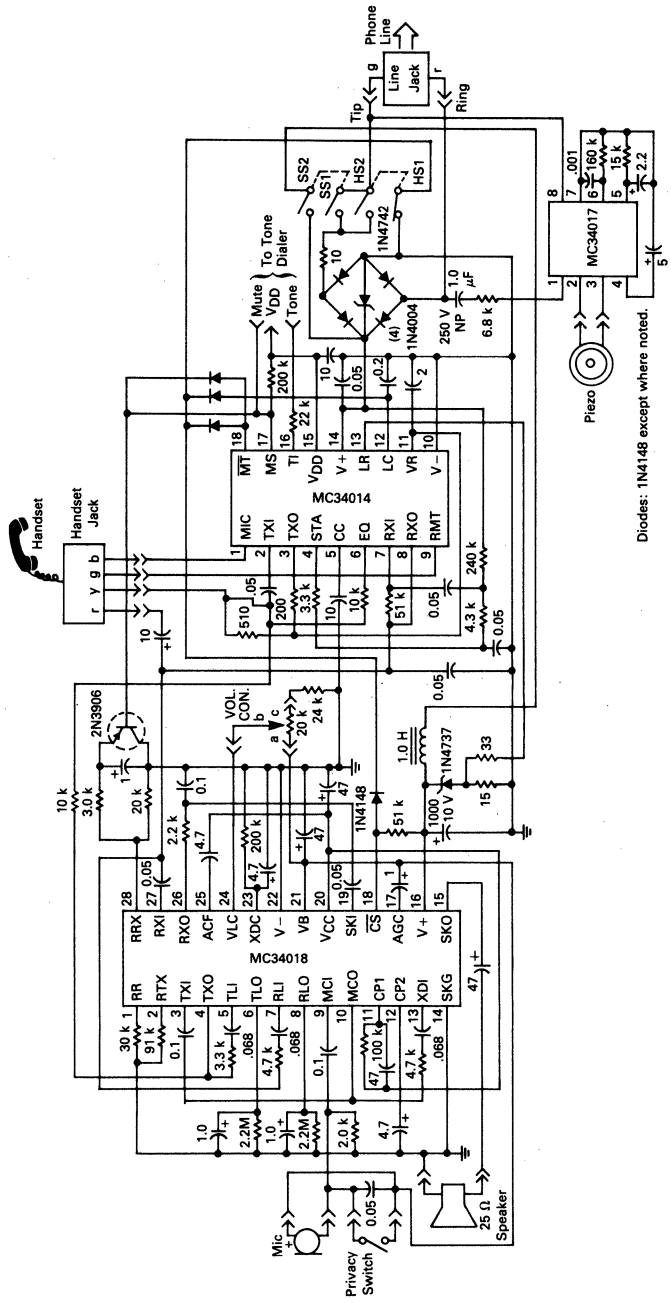

FIGURE 23 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

Recommended External Components

Piezo Sounder

Models KSN 1113-1116
Motorola, Inc.
Albuquerque, N.M.
505-822-8801

Microphone/Receiver

Microphone model EM-95
Receiver model DH-34
Primo Microphone, Inc.
Elk Grove Village, Ill.
312-595-1022

Microphone Model KUC2123
Hosiden Electronics
Chicago, Ill.
312-956-7707

TRANSIENT PROTECTION & RFI SUPPRESSION

Protection from voltage transients is necessary in most telephone circuits, and may take the form of zener diodes, RC or LC filters, transient suppressors, or a combination of the above.

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the telephone. RFI may enter the circuitry through the Tip & Ring lines, through the microphone and/or receiver leads in the handset cord, or through any of the wiring or PC board traces. Ceramic decoupling capacitors, ferrite beads, and other RFI suppression techniques may be needed. Good PC board design techniques, such as the avoidance of loops, should be used. Long tracks on high impedance nodes should be avoided.

MC34017

Advance Information

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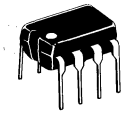
TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Push Pull Output Stage for Greater Output Power Capability
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

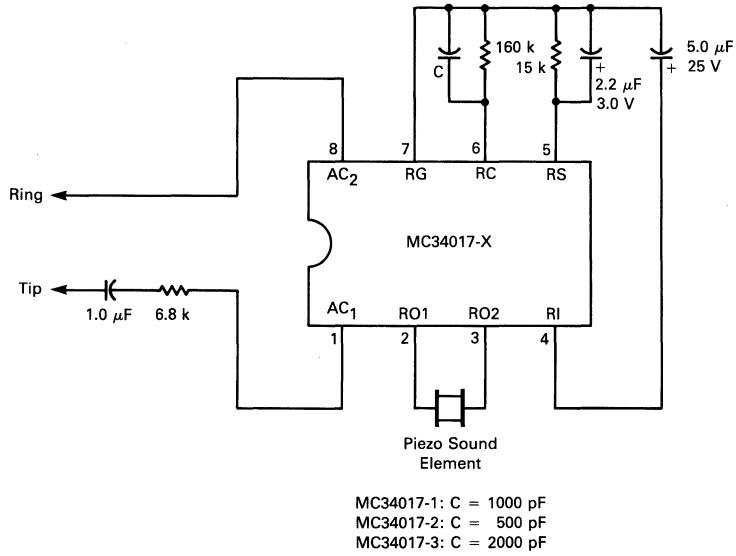
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I²L



PLASTIC PACKAGE
CASE 626-04

APPLICATION CIRCUIT



MC34017-1: C = 1000 pF
MC34017-2: C = 500 pF
MC34017-3: C = 2000 pF

This document contains information on a new product. Specifications and information herein are subject to change without notice.

APPLICATION CIRCUIT PERFORMANCE (Refer to Circuit on First Page.)

Characteristic	Typical Value	Units
Output Tone Frequencies MC34017-1 MC34017-2 MC34017-3 Warble Frequency	 808/1010 1616/2020 404/505 12.5	Hz
Output Voltage ($V_i \geq 60\ V_{rms}$, 20 Hz)	37	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	21	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing V_I = 40 V_{rms}, 15 Hz V_I = 130 V_{rms}, 23 Hz	 >16 12	kΩ
Impedance When Not Ringing V_I = 10 V_{rms}, 24 Hz V_I = 2.5 V_{rms}, 24 Hz V_I = 10 V_{rms}, 5.0 Hz V_I = 3.0 V_{rms}, 200–3200 Hz	 28 >1.0 55 >200	 kΩ MΩ kΩ kΩ
Maximum Transient Input Voltage (T $\leq$ 2.0 ms)	1500	V
Ringer Equivalence: Class A Class B	0.5 0.9	— —

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The input of the threshold comparator to which diode bridge current is mirrored and sensed through an external resistor (R3). Nominal threshold is 1.2 volts. This pin internally clamps at 1.5 volts.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RO1, RO2	The tone ringer output terminals through which the sound element is driven.
RG	The negative terminal of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies (R2, C2).

MAXIMUM RATINGS (Voltages Referenced to RG, Pin 7)

Parameter	Value	Unit
Operating AC Input Current (Pins 1, 8)	20	mA, RMS
Transient Input Current (Pins 1, 8) (T<2.0 ms)	±300	mA, peak
Voltage Applied at RC (Pin 6)	5.0	V
Voltage Applied at RS (Pin 5)	5.0	V
Voltage Applied to Outputs (Pins 2, 3)	−2.0 to V_{RI}	V
Power Dissipation (@ 25°C)	1.0	W
Operating Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

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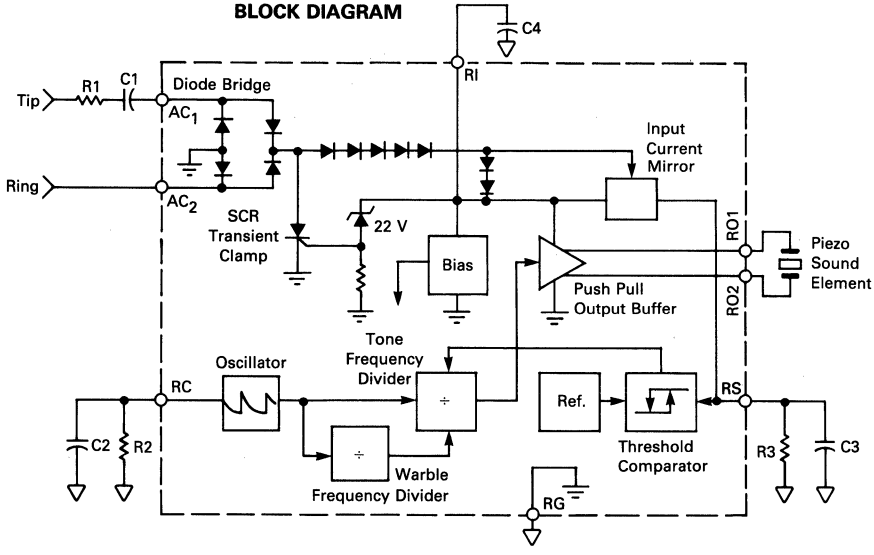
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage (V_{Start} = V_I @ Ring Start)						Vdc
V_I>0	1a	$V_{Start}(+)$	34	37.5	41	
V_I<0	1b	$V_{Start}(-)$	−34	−37.5	−41	
Ringing Stop Voltage (V_{Stop} = V_I @ Ring Stop)	1c	V_{Stop}				Vdc
MC34017-1			14	16	22	
MC34017-2			12	14	20	
MC34017-3			14	16	22	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34017-1 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	11.5	12.5	14	
MC34017-2 High Tone		f_H	1874	2020	2166	
Low Tone		f_L	1504	1616	1736	
Warble Tone		f_W	11.5	12.5	14	
MC34017-3 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	23	25	28	
Output Voltage (V_I = 50 V)	6	V_O	34	37	43	V_{p-p}
Output Short-Circuit Current	2	I_{RO1}, I_{RO2}	35	60	80	mA_{p-p}
Input Diode Voltage (I_I = 5.0 mA)	3	V_D	5.4	6.2	6.8	Vdc
Input Voltage — SCR Off (I_I = 30 mA)	4a	V_{off}	30	38	43	Vdc
Input Voltage — SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.1	6.0	Vdc
RS Clamp Voltage (V_I = 50 V)	5	V_{clamp}	1.3	1.5	1.8	Vdc

BLOCK DIAGRAM



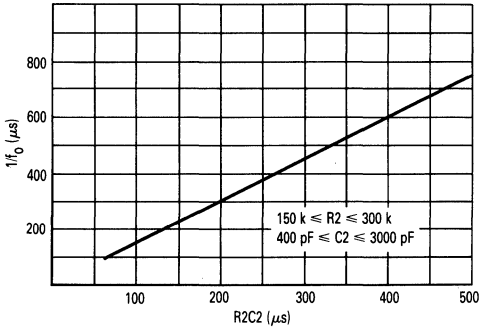
CIRCUIT DESCRIPTION

The MC34017 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_o is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_o from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

The frequency of the tone ringer output signal at RO1 and RO2 alternates between $f_o/4$ to $f_o/5$. The warble rate at which the frequency changes is $f_o/320$ for the MC34017-1, $f_o/640$ for the MC34017-2, and $f_o/160$ for the MC34017-3. With a 4.0 kHz oscillator frequency, the MC34017-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34017-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 kHz oscillator frequency. The MC34017-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 37 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal at RO1 and RO2 will be generated. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a voltage across R3 which is referenced to RG. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit.

FIGURE 1 — OSCILLATOR PERIOD ($1/f_o$) versus OSCILLATOR R2 C2 PRODUCT



($1/f_o$ = 1.45 R2C2 + 10 μs)

When the voltage on capacitor C3 exceeds 1.2 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

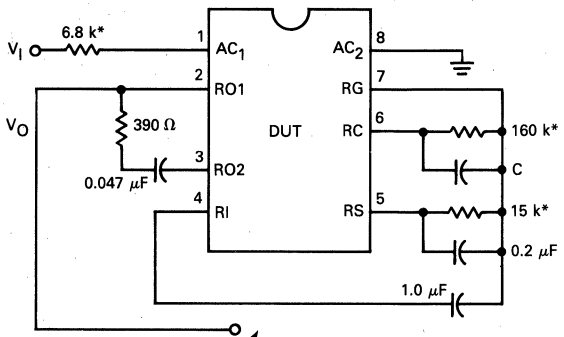
An internal shunt voltge regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

EXTERNAL COMPONENTS

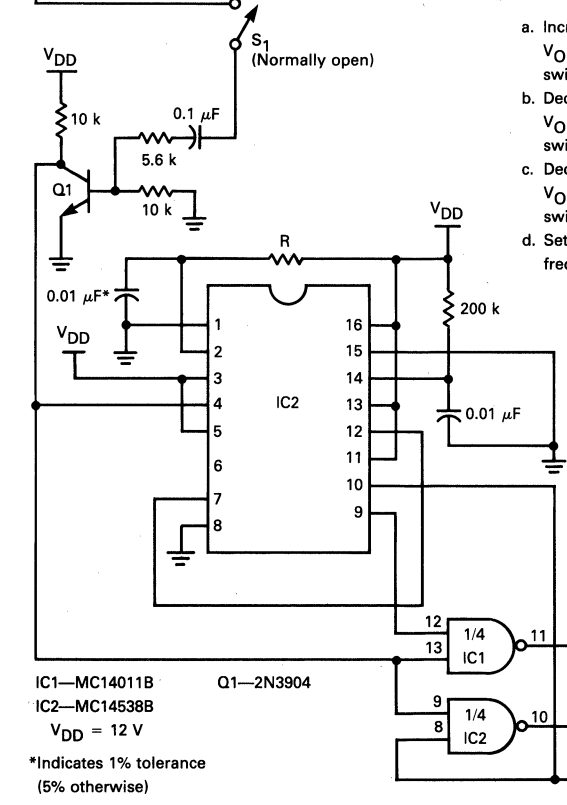
R1	Line input resistor. R1 affects the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 3000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 5.0 kΩ to 18 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

2

FIGURE 2 — TEST ONE



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*



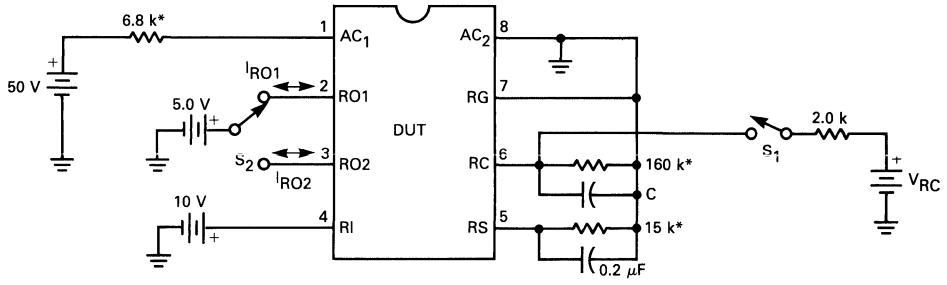
a. Increase V_I from +33 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.
b. Decrease V_I from −33 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V
*Indicates 1% tolerance (5% otherwise)

Q1—2N3904

MC34017-1: R = 110 kΩ*
MC34017-2: R = 55 kΩ*
MC34017-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



With V_{RC} = 4.0 volts, close S_1. Switch S_2 to Pin 2 and measure current at Pin 2 (Io1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pin 2 current changes polarity. Measure the opposite polarity current (Io2). Calculate:

$I_{RO1} = |Io1| + |Io2|$

Switch S2 to Pin 3 and repeat.

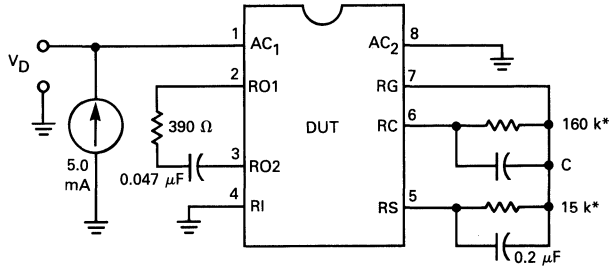
Calculate:

$I_{RO2} = |Io1| + |Io2|$

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE



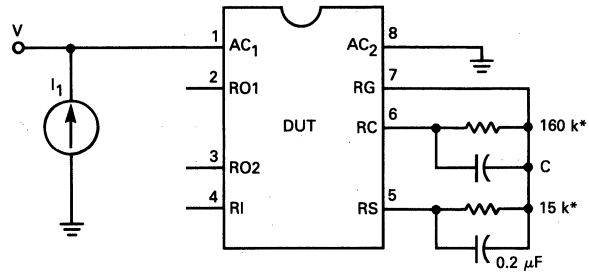
Measure voltage at Pin 1.

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

2

FIGURE 5 — TEST FOUR



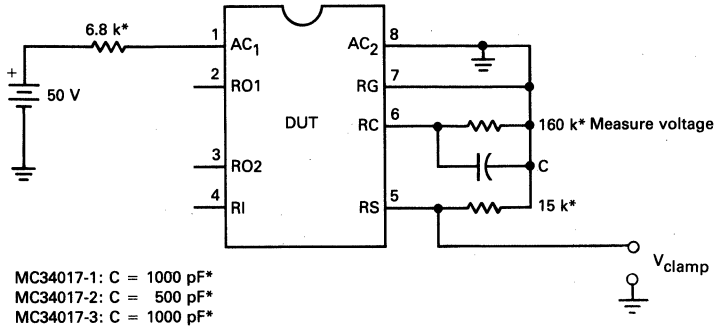
MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

a. Set I_I to 30 mA. Measure voltage at Pin 1 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 1 (V_{on}).

(Each test < 30 ms)

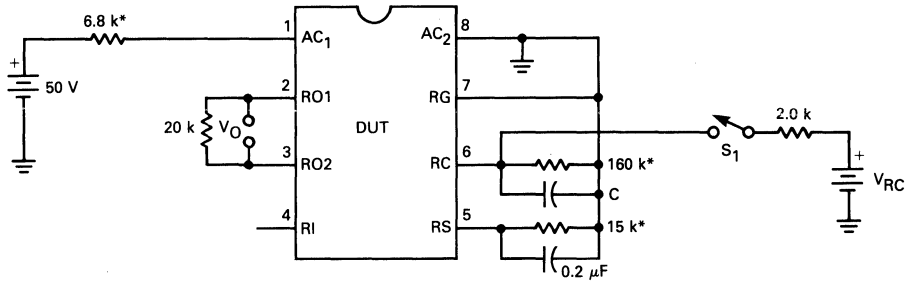
FIGURE 6 — TEST FIVE



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

With V_{RC} = 4.0 volts, close S_1. Measure dc voltage between Pins 2 and 3 (Vo1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pins 2 and 3 change state. Measure the new voltage between Pins 2 and 3 (Vo2).
Calculate:
$V_o = |Vo1| + |Vo2|$

MC34018

Specifications and Applications Information

2

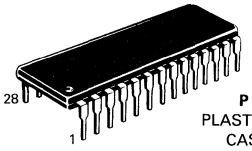
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.

- All necessary level detection and attenuation controls for a hands-free telephone in a single integrated circuit
- Background noise level monitoring with long time constant
- Wide operating dynamic range through signal compression
- On-chip supply and reference voltage regulation
- Typical 100 mW output power (into 25 Ohms) with peak limiting to minimize distortion
- Chip Select pin for active/standby operation
- Linear Volume Control Function
- Standard 28-pin plastic DIP package (0.600 inch wide), PLCC package, and SOIC package

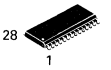
VOICE SWITCHED SPEAKERPHONE CIRCUIT

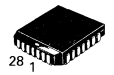
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

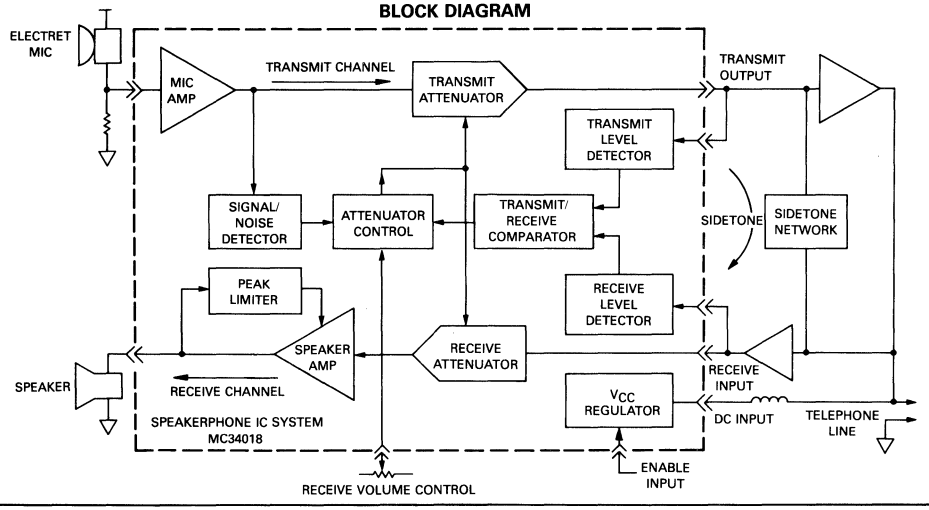
DW SUFFIX
PLASTIC PACKAGE
CASE 751F-03
SO-28





FN SUFFIX
PLASTIC PACKAGE
CASE 776-02
PLCC-28

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Description
1	RR	A resistor to ground provides a reference current for the transmit and receive attenuators.
2	RTX	A resistor to ground determines the nominal gain of the transmit attenuator. The transmit channel gain is inversely proportional to the RTX resistance.
3	TXI	Input to the transmit attenuator. Input resistance is nominally 5.0 k ohms.
4	TXO	Output of the transmit attenuator. The TXO output signal drives the input of the transmit level detector, as well as the external circuit which drives the telephone line.
5	TLI	Input of the transmit level detector. An external resistor ac coupled to the TLI pin sets the detection level. Decreasing this resistor increases the sensitivity to transmit channel signals.
6	TLO	Output of the transmit level detector. The external resistor and capacitor set the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Input of the receive level detector. An external resistor ac coupled to the RLI pin sets the detection level. Decreasing this resistor increases the sensitivity to receive channel signals.
8	RLO	Output of the receive level detector. The external resistor and capacitor set the time the comparator will hold the system in the receive mode after the receive signal ceases.
9	MCI	Microphone amplifier input. Input impedance is nominally 10 k ohms and the dc bias voltage is approximately equal to VB.
10	MCO	Microphone amplifier output. The mic amp gain is internally set at 34 dB (50 V/V).
11	CP1	A parallel resistor and capacitor connected between this pin and V_{CC} holds a voltage corresponding to the background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	A capacitor at this pin peak detects the speech signals for comparison with the background noise level held at CP1.
13	XDI	Input to the transmit detector system. The microphone amplifier output is ac coupled to the XDI pin through an external resistor.
14	SKG	High current ground pin for the speaker amp output stage. The SKG voltage should be within 10 mV of the ground voltage at Pin 22.
15	SKO	Speaker amplifier output. The SKO pin will source and sink up to 100 mA when ac coupled to the speaker. The speaker amp gain is internally set at 34 dB (50 V/V).
16	V+	Input dc supply voltage. V+ can be powered from Tip and Ring if an ac decoupling inductor is used to prevent loading ac line signals. The required V+ voltage is 6.0 to 11 V (7.5 V nominal) at 7.0 mA.
17	AGC	A capacitor from this pin to VB stabilizes the speaker amp gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SKO. The internal resistance at the AGC pin is nominally 110 k ohms.
18	$\overline{CS}$	Digital chip select input. When at a Logic "0" (<0.7 V) the V_{CC} regulator is enabled. When at a Logic "1" (>1.6 V), the chip is in the standby mode drawing 0.5 mA. An open $\overline{CS}$ pin is a Logic "0". Input impedance is nominally 140 k ohms. The input voltage should not exceed 11 V.
19	SKI	Input to the speaker amplifier. Input impedance is nominally 20 k ohms.
20	V_{CC}	A 5.4 V regulated output which powers all circuits except the speaker amplifier output stage. V_{CC} can be used to power external circuitry such as a microprocessor (3.0 mA max). A filter capacitor is required. The MC34018 can be powered by a separate regulated supply by connecting V+ and V_{CC} to a voltage between 4.5 V and 6.5 V while maintaining $\overline{CS}$ at a Logic "1".
21	VB	An output voltage equal to approximately $V_{CC}/2$ which serves as an analog ground for the speakerphone system. Up to 1.5 mA of external load current may be sourced from VB. Output impedance is 250 ohms. A filter capacitor is required.
22	Gnd	Ground pin for the IC (except the speaker amplifier).
23	XDC	Transmit detector output. A resistor and capacitor at this pin hold the system in the transmit mode during pauses between words or phrases. When the XDC pin voltage decays to ground, the attenuators switch from the transmit mode to the idle mode. The internal resistor at XDC is nominally 2.6 k ohms (see Figure 1).
24	VLC	Volume control input. Connecting this pin to the slider of a variable resistor provides receive mode volume control. The VLC pin voltage should be less than or equal to VB.
25	ACF	Attenuator control filter. A capacitor connected to this pin reduces noise transients as the attenuator control switches levels of attenuation.
26	RXO	Output of the receive attenuator. Normally this pin is ac coupled to the input of the speaker amplifier.
27	RXI	Input of the receive attenuator. Input resistance is nominally 5.0 k ohms.
28	RRX	A resistor to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RRX resistance.

Note: Pin numbers are identical for the DIP, PLCC, and SOIC packages.

2

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to Pin 22) (T_A = 25°C)

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+12, −1.0	V
$\overline{CS}$ (Pin 18)	+12, −1.0	V
Speaker Amp Ground (Pin 14)	+3.0, −1.0	V
VLC (Pin 24)	V_{CC}, −1.0	V
Storage Temperature	−65 to +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed.
They are not meant to imply that the devices should be operated at these limits.
The "Electrical Characteristics" tables provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+6.0 to +11	V
$\overline{CS}$ (Pin 18)	0 to +11	V
I_{CC} (Pin 20)	0 to 3.0	mA
VLC (Pin 24)	0.55VB to VB	V
Receive Signal (Pin 27)	0 to 250	mV_{rms}
Microphone Signal (Pin 9)	0 to 5.0	mV_{rms}
Speaker Amp Ground (Pin 14)	−10 to +10	mVdc
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1)

Parameter	Symbol	Pin	Min	Typ	Max	Units
SUPPLY VOLTAGES						
V+ Supply Current	I_{V+}	16				
V+ = 11 V, Pin 18 = 0.7 V			—	—	9.0	mA
V+ = 11 V, Pin 18 = 1.6 V			—	—	800	μA
V_{CC} Voltage (V+ = 7.5 V)	V_{CC}	20	4.9	5.4	5.9	Vdc
Line Regulation (6.5 V < V+ < 11 V)	$\Delta V_{CC\ LN}$		—	65	150	mV
Output Resistance (I_{CC} = 3.0 mA)	R_{OVCC}		—	6.0	20	ohms
Dropout Voltage (V+ = 5.0 V)	$V_{CC\ SAT}$		—	80	300	mV
VB Voltage (V+ = 7.5 V)	V_B	21	2.5	2.9	3.3	Vdc
Output Resistance (IB = 1.7 mA)	R_{OVB}		—	250	—	ohms
ATTENUATORS						
Receive Attenuator Gain (@ 1.0 kHz)		26,				
Rx Mode, Pin 24 = VB; Pin 27 = 250 mV_{rms}	G_{RX}	27	2.0	6.0	10	dB
Range (Rx to Tx Modes)	ΔG_{RX}		40	44	48	dB
Idle Mode, Pin 27 = 250 mV_{rms}	G_{RXI}		−20	−16	−12	dB
RXO Voltage (Rx Mode)	V_{RXO}		1.8	2.3	3.2	Vdc
Delta RXO Voltage (Switch from RX to TX Mode)	ΔV_{RXO}		—	—	100	mV
RXO Sink Current (Rx Mode)	I_{RXOL}		75	—	—	μA
RXO Source Current (Rx Mode)	I_{RXOH}		1.0	—	3.0	mA
RXI Input Resistance	R_{RXI}		3.5	5.0	8.0	kΩ
Volume Control Range (Rx Attenuator Gain, Rx Mode, 0.6 VB < Pin 24 < VB)	V_{CR}		24.5	—	32.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Units
ATTENUATORS						
Transmit Attenuator Gain (@ 1.0 kHz)		3,				
Tx Mode, Pin 3 = 250 mV_{rms}	G_{TX}	4	4.0	6.0	8.0	dB
Range, (Tx to Rx Mode)	ΔG_{TX}		40	44	48	dB
Idle Mode, Pin 3 = 250 mV_{rms}	G_{TXI}		−16.5	−13	−8.5	dB
TXO Voltage (Tx Mode)	V_{TXO}		1.8	2.3	3.2	Vdc
Delta TXO Voltage (Switch from Tx to Rx Mode)	ΔV_{TXO}		—	—	100	mV
TXO Sink Current (Tx Mode)	I_{TXOL}		75	—	—	μA
TXO Source Current (Tx Mode)	I_{TXOH}		1.0	—	3.0	mA
TXI Input Resistance	R_{TXI}		3.5	5.0	8.0	kΩ
ACF Voltage (V_{CC} − Pin 25 Voltage)	ΔV_{ACF}	20,				
Rx Mode		25	—	150	—	mV
Rx Mode			—	6.0	—	mV
Idle Mode			—	75	—	mV
SPEAKER AMPLIFIER						
Speaker Amp Gain (Pin 19 = 20 mV_{rms})	G_{SPK}	15, 19	33	34	35	dB
SKI Input Resistance	R_{SKI}		15	22	37	kΩ
SKO Voltage (Pin 19 = Cap Couple to GND)	V_{SKO}		2.4	3.0	3.6	Vdc
SKO High Voltage (Pin 19 = 0.1 V, −100 mA load at Pin 15)	V_{SKOH}		5.5	—	—	Vdc
SKO Low Voltage (Pin 19 = −0.1 V, +100 mA load at Pin 15)	V_{SKOL}		—	—	600	mV
MICROPHONE AMPLIFIER						
Mike Amp Gain (Pin 9 = 10 mV_{rms}, 1.0 kHz)	G_{MCI}	9, 10	32.5	34	35	dB
Mike Amp Input Resistance	R_{MCI}		6.5	10	16	kΩ
LOGAMPS						
RLO Leakage Current (Pin 8 = VB + 1.0 V)	I_{LKRLO}	8	—	—	2.0	μA
TLO Leakage Current (Pin 6 = VB + 1.0 V)	I_{LKTLO}	6	—	—	2.0	μA
Transmit-Receive Switching Threshold (Ratio of ITLI to IRLI — at 20 μA — to switch Tx-Rx Comparator)	I_{TH}	5,7 25	0.8	—	1.2	
TRANSMIT DETECTOR						
XDC Voltage — Idle Mode	V_{XDC}	23	—	0	—	Vdc
Tx Mode			—	4.0	—	Vdc
CP2 Current Source	I_{CP2}	12	5.0	10	13	μA
DISTORTION						
Rx Mode — RXI to SKO (Pin 27 = 10 mV_{rms}, 1.0 kHz)	R_{XD}	27, 15	—	1.5	—	%
Tx Mode — MCI to TXO (Pin 9 = 5.0 mV_{rms}, 1.0 kHz)	T_{XD}	4,9	—	2.0	—	%

NOTES: 1. V+ = 7.5 V, $\overline{CS}$ = 0.7 V except where noted.
2. Rx Mode: Pin 7 = −100 μA, Pin 5 = +100 μA, except where noted.
Tx Mode: Pin 5, 13 = −100 μA, Pin 7 = +100 μA, Pin 11 = 0 volts.
Idle Mode: Pin 5 = −100 μA, Pin 7, 13 = +100 μA.
3. Current into a pin designated as +; current out of a pin designated as −
4. Voltages referred to Pin 22. T_A = +25°C.

2

TEMPERATURE CHARACTERISTICS (−20 to +60°C)

Parameter	Pin	Typical Change	Units
V+ Supply Current (V+ = 11 V, Pin 18 = 0.7 V)	16	−0.2	%/°C
V+ Supply Current (V+ = 11 V, Pin 18 = 1.6 V)	16	−0.4	%/°C
V_{CC} Voltage (V+ = 7.5 V)	20	+0.1	%/°C
Attenuator Gain (Max and Min Settings)		±0.003	dB/°C
Delta RXO, TXO Voltages	4,26	±0.24	%/°C
Speaker Amp Gain	15,19	±0.003	dB/°C
Microphone Amp Gain	9,10	±0.001	dB/°C
Microphone Amp Input Resistance	9	+0.4	%/°C
Tx-Rx Switching Threshold (@ 20 μA)	5,7	±0.2	nA/°C

DESIGN GUIDELINES (Refer to Figure 1)

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain the other is at maximum attenuation, and vice versa. They are never both on or both off. Their main purpose is to control the transmit and receive paths to provide the half-duplex operation required of a speakerphone. The attenuators are controlled solely by the voltage at the ACF pin (Pin 25). The ACF voltage is provided by the Attenuator Control block, which receives 3 inputs: a) the Rx-Tx Comparator, b) the Transmit Detector Comparator, and c) the Volume Control. The response of the attenuators is based on the difference of the ACF voltage from V_{CC}, and therefore a simple method for monitoring the circuit operation is to monitor this voltage difference (referred to as ΔVacf). If ΔVacf is approximately 6 millivolts the transmit attenuator is fully on and the receive attenuator is fully off (transmit mode). If ΔVacf is approximately 150 millivolts the circuit is in the receive mode. If ΔVacf is approximately 75 millivolts, the circuit is in the idle mode, and the two attenuators are at gain settings approximately half way (in dB) between their fully on and fully off positions.

The maximum gain and attenuation values are determined by the three resistors RR, RTX, and RRX (Refer to Figures 2, 3 and 4). RR affects both attenuators according to its value RELATIVE to RTX and RRX, which is why Figure 4 indicates the variations versus the ratio of the other resistors to RR. (GRX and GTX are the maximum gains, and ARX and ATX are the maximum attenuations). RTX affects the gain and attenuation of only the transmit attenuator according to the curves of Figure 2, while RRX affects only the receive attenuator according to Figure 3. As can be seen from the figures, the gain difference (from on to off) is a reasonably constant 45 dB until the upper gain limit is approached. A value of 30 k is recommended for RR as a starting point, and then RTX and RRX selected to suit the particular design goals.

The input impedance of the attenuators (at TXI and RXI) is typically 5.0 kΩ, and the maximum input signal which will not cause output distortion is 250 mV_{rms} (707 mVp-p). The 4300 ohm resistor and 0.01 μF capacitor at RXO (in Figure 1) filters out high frequency components in the receive path. This helps minimize high frequency acoustic feedback problems which may occur if the filter were not present. The filter's insertion loss is 1.5 dB at 1.0 kHz. The outputs of the attenuators are inverted from their inputs.

Referring to the attenuator control block, the ΔVacf voltage at its output is determined by three inputs. The relationship of the inputs and output is summarized in the following truth table:

Tx-Rx Comp	Transmit Det Comp	Volume Control	ΔVacf	Mode
Transmit	Transmit	No Effect	6.0 mV	Transmit
Transmit	Idle	No Effect	75 mV	Idle
Receive	Transmit	Affects ΔVacf	50–150 mV	Receive
Receive	Idle	Affects ΔVacf	50–150 mV	Receive

As can be seen from the truth table, the Tx-Rx comparator dominates. The Transmit Detector Comparator is effective only in the transmit mode, and the Volume Control is effective only in the receive mode.

The Tx-Rx comparator is in the transmit position when there is sufficient transmit signal present over and above any receive signal. The Transmit Detector Comparator then determines whether the transmit signal is a result of background noise (a relatively stable signal), or speech which consists of bursts. If the signal is due to background noise, the attenuators will be put into the idle mode (ΔVacf = 75 mV). If the signal consists of speech, the attenuators will be switched to the transmit mode (ΔVacf = 6.0 mV.) A further explanation of this function will be found in the section on the Transmit Detector Circuit.

The Tx-Rx comparator is in the receive position when there is sufficient receive signal to overcome the background noise **AND** any speech signals. The ΔVacf voltage will now be 150 mV **IF** the volume control is at the maximum position, i.e. VLC (Pin 24) = VB. IF VLC is less than VB, the gain of the receive attenuator, and the attenuation of the transmit attenuator, will vary in a complementary manner as shown in Figure 5. It can be seen that at the minimum recommended operating level (VLC = 0.55 VB) the gain of the transmit attenuator is actually greater than that of the receive attenuator. The effect of varying VLC is to vary ΔVacf, with a resulting variation in the gains of the attenuators. Figure 6 shows the gain variations with ΔVacf.

The capacitor at ACF (Pin 25) smooths the transition between operating modes. This keeps down any "clicks" in the speaker or transmit signal when the ACF voltage switches.

The gain separation of the two attenuators can be reduced from the typical 45 dB by adding a resistor between Pins 20 (V_{CC}) and 25 (ACF). The effect is a reduction of the maximum ΔVacf voltage in the receive mode, while not affecting ΔVacf in the transmit mode. As an example, adding a 12 kΩ resistor will reduce ΔVacf by approximately 15 mV (to 135 mV), decrease the gain of the receive attenuator by approximately 5.0 dB, and increase the gain of the transmit attenuator by a similar amount. If the circuit requires the receive attenuator gain to be +6.0 dB in the receive mode, RRX must be adjusted (to ≈ 27 k) to re-establish this value. This change will also increase the receive attenuator gain in the transmit mode by a similar amount. The resistor at TLI may also require changing to reset the sensitivity of the transmit level detector.

LOG AMPLIFIERS
(Transmit and Receive Level Detectors)

The log amps monitor the levels of the transmit and receive signals, so as to tell the Tx-Rx comparator which mode should be in effect. The input signals are applied to the amplifiers (at TLI and RLI) through AC coupling capacitors and current limiting resistors. The value of these components determines the sensitivity of the respective amplifiers, and has an effect on the switching times between transmit and receive modes. The feedback elements for the amplifiers are back-to-back diodes which provide a logarithmic gain curve, thus allowing operation over a wide range of signal levels. The outputs of the amplifiers are rectified, having a quick rise time and a slow decay time. The rise time is determined primarily by the external capacitor (at TLO or RLO) and an internal 500 ohm resistor, and is on the order of a fraction of a millisecond. The decay time is determined by the external resistor and capacitor, and is on the order of a fraction of a second. The switching time is not fixed, but depends on the relative values of the transmit and receive signals, as well as these external components. Figure 7 indicates the dc transfer characteristics of the log amps, and Figure 8 indicates the transfer characteristics with respect to an ac input signal. The dc level at TLI, RLI, TLO, and RLO is approximately VB.

The Tx-Rx comparator responds to the voltages at TLO and RLO, which in turn are functions of the currents sourced out of TLI and RLI, respectively. If an offset at the comparator input is desired, e.g., to prevent noise from switching the system, or to give preference to either the transmit or receive channel, this may be achieved by biasing the appropriate input (TLI or RLI). A resistor to ground will cause a DC current to flow out of that input, thus forcing the output of that amplifier to be biased slightly higher than normal. This amplifier then becomes the preferred one in the system operation. Resistor values from 500 k to 10 M ohms are recommended for this purpose.

SPEAKER AMPLIFIER

The speaker amplifier has a fixed gain of 34 dB (50 V/V), and is noninverting. The input impedance is nominally 22 kΩ as long as the output signal is below that required to activate the Peak Limiter. Figure 9 indicates the typical output swing available at SKO (Pin 15). Since the output current capability is 100 mA, the lower curve is limited to a 5.0 volt swing. The output impedance depends on the output signal level and is relatively low as long as the signal level is not near the maximum limits. At 3 volts p-p the output impedance is <0.5 ohms, and at 4.5 volts p-p it is <3 ohms. The output is short circuit protected at approximately 300 mA.

When the amplifier is overdriven, the peak limiter causes a portion of the input signal to be shunted to ground, in order to maintain a constant output level. The effect is that of a gain reduction caused by a reduction of the input impedance (at SKI) to a value not less than 2.0 kΩ.

The capacitor at Pin 17 (AGC) determines the response time of the peak limiter circuit. When a large input signal is applied to SKI, the voltage at AGC (Pin 17) will drop quickly as a current source is applied to the external capacitor. When the large input signal is reduced, the current source is turned off, and an internal 110 kΩ resistor discharges the capacitor so the voltage at AGC can return to its normal value (1.9 Vdc). The capacitor additionally stabilizes the peak limiting feedback loop.

If there is a need to mute the speaker amplifier without disabling the rest of the circuit, this may be accomplished by connecting a resistor from the AGC pin to ground. A 100 kΩ resistor will reduce the gain by 34 dB (0 dB from SKI to SKO), and a 10 k resistor will reduce the gain by almost 50 dB.

TRANSMIT DETECTOR CIRCUIT

The transmit detector circuit, also known as the background noise monitor, distinguishes speech (which consists of bursts) from the background noise (a relatively constant signal). It does this by storing a voltage level, representative of the average background noise, in the capacitor at CP1 (Pin 11). The resistor and capacitor at this pin have a time constant of approximately 5 seconds (in Figure 1). The voltage at Pin 11 is applied to the inverting input of the Transmit Detector Comparator. In the absence of speech signals, the noninverting input receives the same voltage level minus an offset of 36 mV. In this condition, the output of the comparator will be low, the output transistor turned off, and the voltage at XDC (Pin 23) will be at ground. If the Tx-Rx comparator is in the transmit position, the attenuators will be in the idle mode (ΔVacf = 75 mV). When speech is presented to the microphone, the signal burst appearing at XDI reaches the noninverting input of the transmit detector comparator before the voltage at the inverting input can change, causing the output to switch high, driving the voltage at XDC up to approximately 4 volts. This high level causes the attenuator control block to switch the attenuators from the idle mode to the transmit mode (assuming the Tx-Rx comparator is in

the transmit mode). As long as the speech continues to arrive, and is maintained at a level above the background, the voltage at XDC will be maintained at a high level, and the circuit will remain in the transmit mode. The time constant of the components at XDC will determine how much time the circuit requires to return to the idle mode after the cessation of microphone speech signals, such as occurs during the normal pauses in speech.

The series resistor and capacitor at XDI (Pin 13) determine the sensitivity of the transmit detector circuit. Figure 10 indicates the change in DC voltage levels at CP2 and CP1 in response to a steady state sine wave applied at the input of the 0.068 μF capacitor and 4700 ohm resistor (the voltage change at CP1 is 2.7 times greater than the change at CP2). Increasing the resistor, or lowering the capacitor, will reduce the response at these pins. The first amplifier (between XDI and CP2) is logarithmic in order that this circuit be able to handle a wide range of signal levels (or in other words, it responds equally well to people who talk quietly and to people who shout). Figure 7 indicates the dc transfer characteristics of the log amp.

Figure 11 indicates the response at Pins 11, 12, and 23 to a varying signal at the microphone. The series of events in Figure 11 is as follows:

1) CP2 (Pin 12) follows the peaks of the speech signals, and decays at a rate determined by the 10 μA current source and the capacitor at this pin.

2) CP1 (Pin 11) increases at a rate determined by the RC at this pin after CP2 has made a positive transition. It will follow the decay pattern of CP2.

3) The noninverting input of the Transmit Detector Comparator follows CP2, gained up by 2.7, and reduced by an offset of 36 mV. This voltage, compared to CP1, determines the output of the comparator.

4) XDC (Pin 23) will rise quickly to 4 Vdc in response to a positive transition at CP2, but will decay at a rate determined by the RC at this pin. When XDC is above 3.25 Vdc, the circuit will be in the transmit mode. As it decays towards ground, the attenuators are taken to the idle mode.

MICROPHONE AMPLIFIER

The microphone amplifier is noninverting, has an internal gain of 34 dB (50 V/V), and a nominal input impedance of 10 kΩ. The output impedance is typically <15 ohms. The maximum p-p voltage swing available at the output is approximately 2.0 volts less than V_{CC}, which is substantially more than what is required in most applications. The input at MCI (Pin 9) should be ac coupled to the microphone so as to not upset the bias voltage. Generally, microphone sensitivity may be adjusted by varying the 2 k microphone bias resistor, rather than by attempting to vary the gain of the amplifier.

POWER SUPPLY

The voltage supply for the MC34018 at V+ (Pin 16) should be in the range of 6.0 to 11 volts, although the circuit will operate down to 4.0 volts. The voltage can be supplied either from Tip and Ring, or from a separate supply. The required supply current, with no signal to the speaker, is shown in Figure 12. The upper curve indicates the normal operating current when $\overline{\text{Chip Select}}$ (Pin 18) is at a Logic "0". Figure 13 indicates the average dc current required when supplying various power levels to a 25 ohm speaker. Figure 13 also indicates the minimum supply voltage required to provide the indicated power levels. The peak in the power supply current at 5.0–5.4 volts occurs as the V_{CC} circuit comes into regulation.

It is imperative that the V+ supply (Pin 16) be a good ac ground for stability reasons. If this pin is not well filtered (by a 1000 μF capacitor AT THE IC), any variation at V+ caused by the required speaker current flowing through this pin can cause a low frequency oscillation. The result is usually that the circuit will cut the speaker signal on and off at the rate of a few hertz. Experiments have shown that only a few inches of wire between the supply and the IC can cause the problem if the filter capacitor is not physically adjacent to the IC. It is equally imperative that both ground pins (Pins 14 and 22) have a low loss connection to the power supply ground.

V_{CC}

V_{CC} (Pin 20) is a regulated output voltage of 5.4 volts, +/−0.5 V. Regulation will be maintained as long as V+ is (typically) 80 mV greater than the regulated value of V_{CC}. Up to 3 milliamps can be sourced from this supply for external use. The output impedance is <20 ohms.

The 47 μF capacitor indicated for connection to Pin 20 is essential for stability reasons. It must be located adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the V_{CC} voltage will go to 0 volts.

If the MC34018 is to be powered from a regulated supply (not the Tip and Ring lines) of less than 6.5 volts, the configuration of Figure 14 may be used so as to ensure that V_{CC} is regulated. The regulated voltage is applied to both V+ and V_{CC}, with $\overline{\text{CS}}$ held at a Logic "1" so as to turn off the internal regulator (the Chip Select function is not available when the circuit is used in this manner). Figure 15 indicates the supply current used by this configuration, with no signal at the speaker. When a signal is sent to the speaker, the curves of Figure 13 apply.

VB

VB is a regulated output voltage with a nominal value of 2.9 volts, +/−0.4 volts. It is derived from V_{CC} and tracks it, holding a value of approximately 54% of V_{CC}. 1.5 milliamps can be sourced from this supply at a typical output impedance of 250 ohms.

The 47 μF capacitor indicated for connection to the VB pin is required for stability reasons, and must be adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the VB voltage will go to 0 volts.

CHIP SELECT

The Chip Select pin (Pin 18) allows the chip to be powered down anytime its functions are not required. A Logic "1" level in the range of 1.6 V to 11 V deselects the chip, and the resulting supply current (at V+) is shown in Figure 12. The input resistance at Pin 18 is >75 kΩ. The V_{CC} and VB regulated voltages go to 0.0 when the chip is deselected. Leaving Pin 18 open is equivalent to a Logic "0" (chip enabled).

FIGURE 1 — TEST CIRCUIT

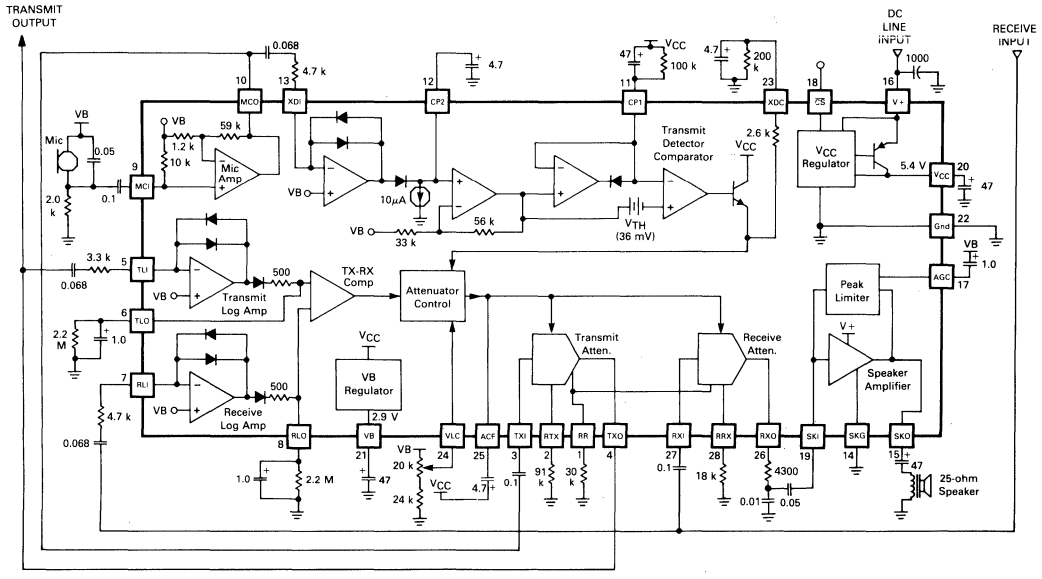


FIGURE 2 — TRANSMIT ATTENUATOR versus RTX

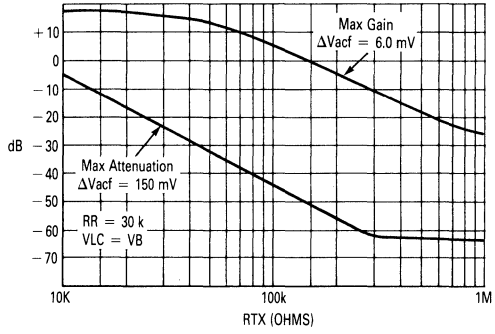


FIGURE 3 — RECEIVE ATTENUATOR versus RRX

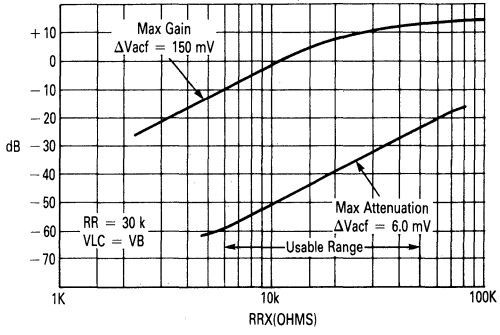


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FIGURE 4 — GAIN AND ATTENUATION versus RESISTOR RATIOS

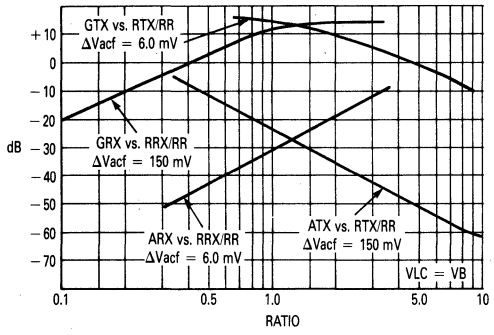

FIGURE 5 — ATTENUATOR GAIN versus VLC

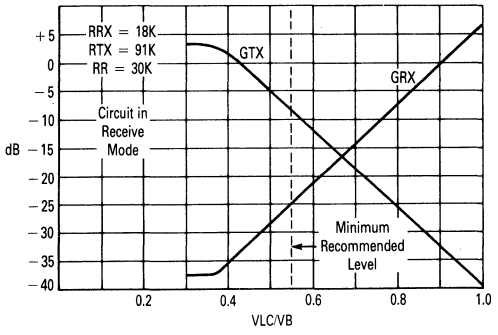

FIGURE 6 — ATTENUATOR GAIN versus ΔVacf

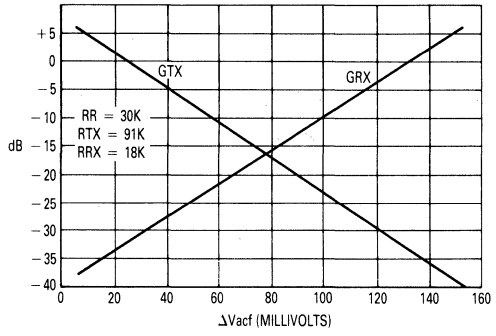

FIGURE 7 — LOG AMP TRANSFER CHARACTERISTICS

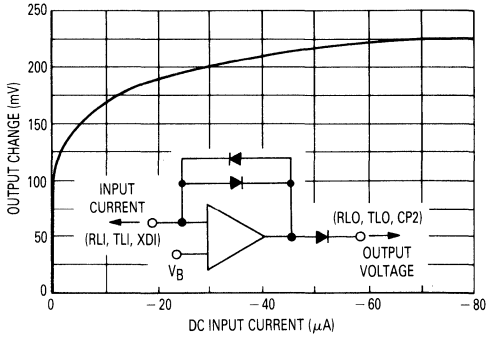

FIGURE 8 — LOG AMP TRANSFER CHARACTERISTICS

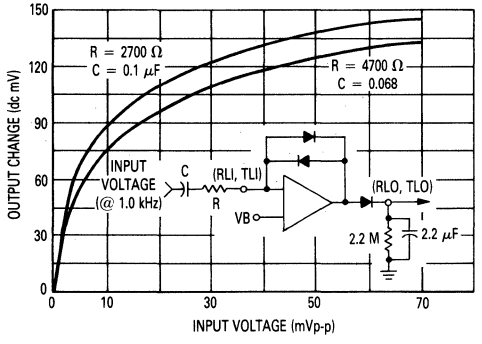

FIGURE 9 — SPEAKER AMP OUTPUT versus SUPPLY VOLTAGE

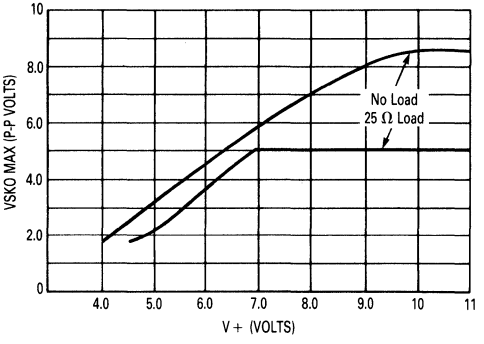

FIGURE 10 — RESPONSE AT CP2 AND CP1

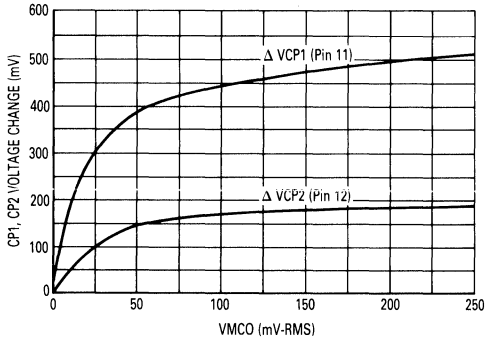

FIGURE 11 — TRANSMIT DETECTOR OPERATION

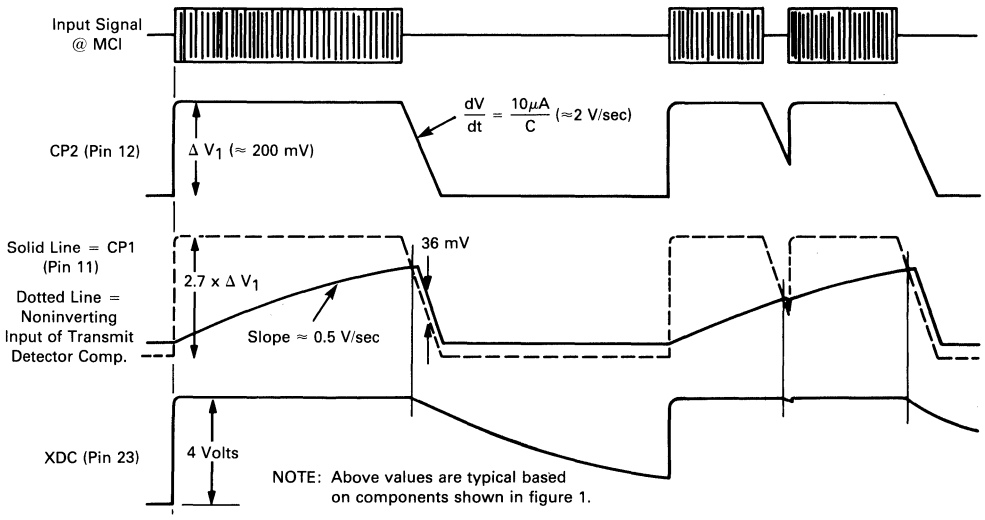

FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

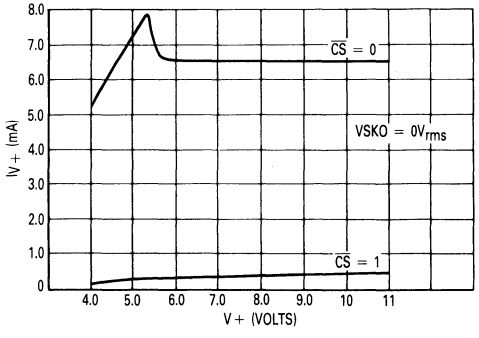

FIGURE 13 — SUPPLY CURRENT
versus SUPPLY VOLTAGE versus SPEAKER POWER

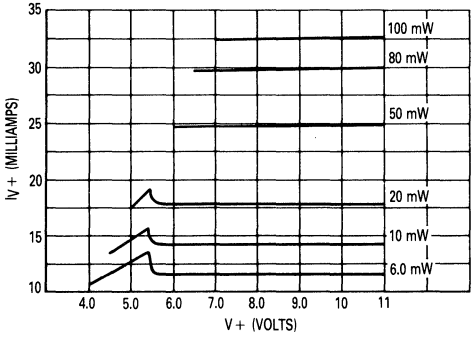

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FIGURE 14 — ALTERNATE POWER SUPPLY CONFIGURATION

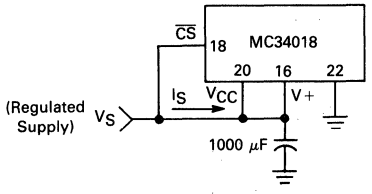
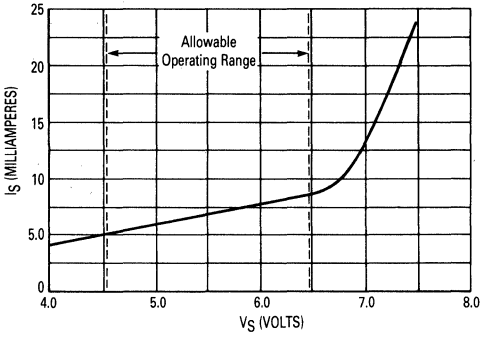


FIGURE 15 — SUPPLY CURRENT versus SUPPLY VOLTAGE (SEE FIGURE 14)



SWITCHING TIME

The switching times of the speakerphone circuit depend not only on the various external components, but also on the operating condition of the circuit at the time a change is to take effect. For example, the switching time from idle to transmit is generally quicker than the switching time from receive to transmit (or transmit to receive).

The components which most significantly affect the timing between the transmit and receive modes are those at Pins 5 (transmit turn-on), 6 (transmit turn-off), 7 (receive turn-on), and 8 (receive turn-off). These four timing functions are not independent, but interact since the Tx-Rx comparator operates on a RELATIVE Tx-Rx comparison, rather than on absolute values. The components at Pins 11, 12, 13, and 23 affect the timing from the transmit to the idle mode. Timing from the idle mode to transmit mode is relatively quick (due to the quick charging of the various capacitors), and is not greatly affected by the component values. Pins 5–8 do not affect the idle-to-transmit timing since the Tx-Rx comparator must already be in the transmit mode for this to occur.

The following table provides a summary of the effect on the switching time of the various components, including the volume control:

Additionally, the following should be noted:

1) The RCs at Pins 5 and 7 have a dual function in that they affect the sensitivity of the respective log amplifiers, or in other words, how loud the speech must be in order to gain control of the speakerphone circuit.

2) The RC at Pin 13 also has a dual function in that it determines the sensitivity of the transmit detector circuit.

3) The volume control affects the switching speed, and the relative response to transmit signals, in the following manner: When the circuit is in the receive mode, reducing the volume control setting increases the signal at TXO, and consequently the signal to the TLI pin. Therefore a given signal at TXI will switch the circuit into the transmit mode quicker at low volume settings.

The photographs of Figures 16 and 17 indicate experimentally obtained switching response times for the circuit of Figure 1. In Figure 16, the circuit is provided a continuous receive signal of 1.1 mVp-p at RXI (trace #3). A repetitive burst signal of 7.2 mVp-p, lasting 120

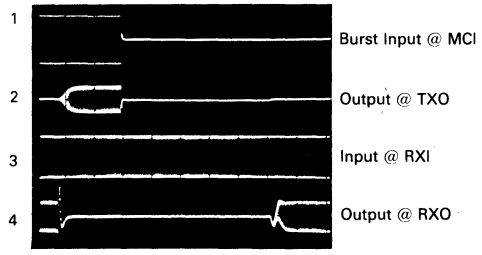
Components	Tx to Rx	Rx to Tx	Tx to Idle
RC @ Pin 5	Moderate	Significant	No effect
RC @ Pin 6	Significant	Moderate	No effect
RC @ Pin 7	Significant	Moderate	No effect
RC @ Pin 8	Moderate	Significant	No effect
RC @ Pin 11	No effect	Slight	Moderate
C @ Pin 12	No effect	Slight	Significant
RC @ Pin 13	No effect	Slight	Slight
RC @ Pin 23	No effect	Slight	Significant
V @ Pin 24	No effect	Moderate	No effect
C @ Pin 25	Moderate	Moderate	Slight

milliseconds, and repeated every 1 second, is applied to MCI (Trace #1). Trace #2 is the output at TXO, and is approximately 650 mVp-p at its maximum. Trace #4 is the output at RXO, and is approximately 2.2 mVp-p at its maximum. The time to switch from the receive mode to the transmit mode is approximately 40 ms, as indicated by the time required for TXO to turn on, and for RXO to turn off. After the signal at MCI is shut off, the switching time back to the receive mode is approximately 210 ms.

In Figure 17, a continuous signal of 7.6 mVp-p is applied to MCI (Trace #1), and a repetitive burst signal of 100 mVp-p is applied to RXI (Trace #3), lasting approximately 120 ms, and repeated every 1 second. Trace #2 is the output at TXO and is approximately 90 mVp-p at its maximum, and Trace #4 indicates the output at RXO, and is approximately 150 mVp-p at its maximum. In this sequence, the circuit switches between the idle and receive modes. The time required to switch from idle to receive is approximately 70 ms, as indicated by the first part of Traces 2 and 4. After the receive signal is shut off, the time to switch back to the idle mode is approximately 100 ms.

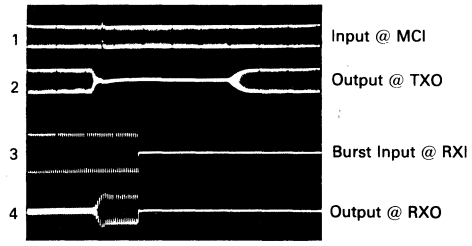
All of the above mentioned times will change significantly by varying the amplitude of the input signals, as well as by varying the external components.

FIGURE 16 — TRANSMIT-RECEIVE SWITCHING



Time Base = 40 ms/Div

FIGURE 17 — IDLE-RECEIVE SWITCHING



Time Base = 30 ms/Div

APPLICATIONS INFORMATION

The MC34018 Speakerphone IC is designed to provide the functions additionally required when a speakerphone is added to a standard telephone. The IC provides the necessary relative level detection and comparison of the speech signals provided by the talkers at the speakerphone (near end speaker) and at the distant telephone (far end speaker).

The MC34018 is designed for use with an electret type microphone, a 25 ohm speaker, and has an output power capability of (typically) 100 mW. All external components surrounding this device are passive, however, this IC does require additional circuitry to interface to the Tip and Ring telephone lines. Two suggested circuits are shown in this data sheet.

Figure 18 depicts a circuit using the MC34014 Speech Network (to provide the line interface), as well as the circuitry necessary to switch between the handset mode and the speakerphone mode. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014 speech network, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, **AND** placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the operational mode of the MC34014 so as to optimize the speakerphone operation (see the MC34014 data sheet for further details). The tone dialer interface is meant for connection to a DTMF dialer with an active low MUTE signal. The V_{DD} supply from the MC34014 is a nominal 3.3 volts. The MC34017 and piezo sounder provide the ringing function.

Figure 19 depicts a configuration which does not include a handset, dialer, or ringer. The only controls are S1 (to make the connection to the line), S2 (a "privacy" switch), and the volume control. It is meant to be used in parallel with a normal telephone which has the dialing and ringing functions.

Figure 20 depicts a means of providing logic level signals that indicate which mode of operation the MC34018 is in. Comparator A indicates whether the circuit is in the receive or transmit/idle mode, and comparator B indicates (when in the transmit/idle mode) whether the circuit is in the transmit or idle mode. The LM393 dual comparator was chosen because of its low current requirement (<1.0 mA), low voltage requirement (as low as 2.0 volts), and low cost.

2

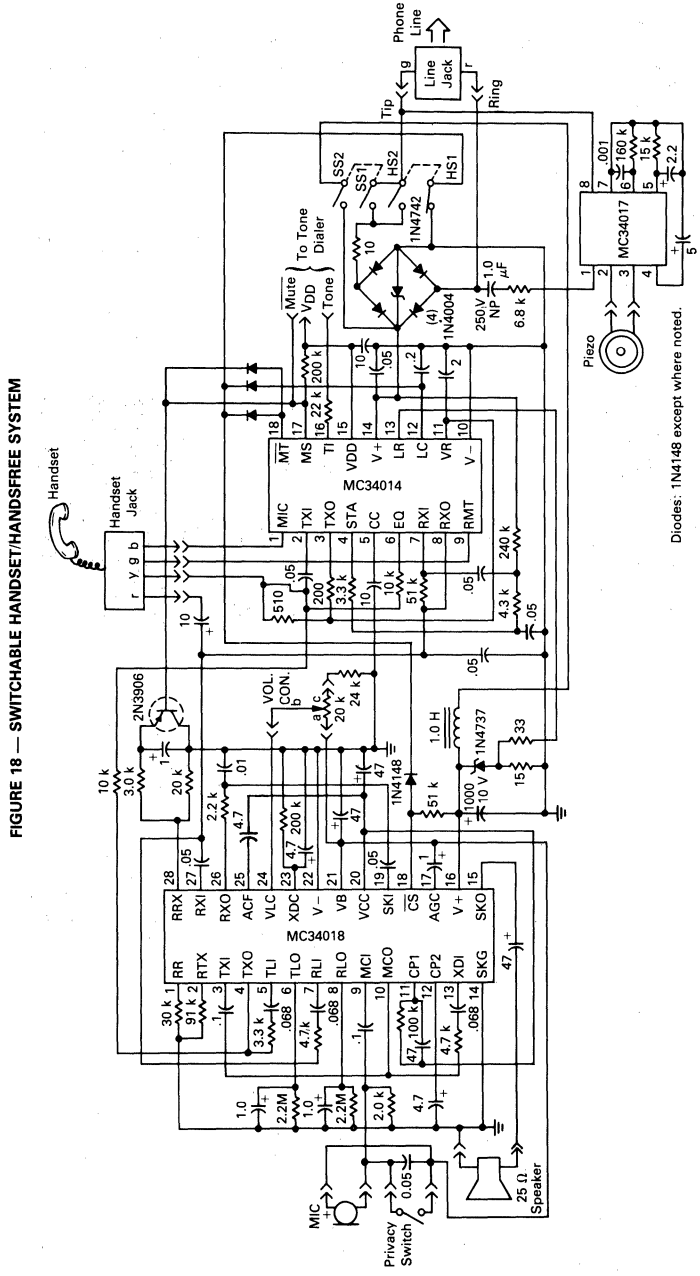
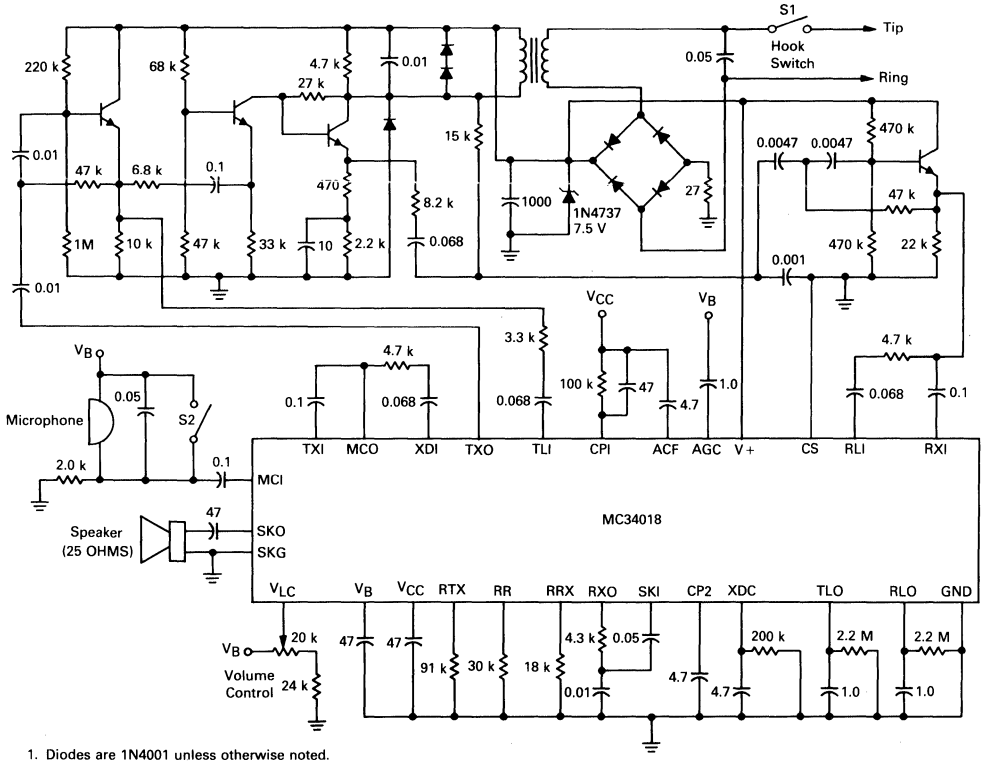


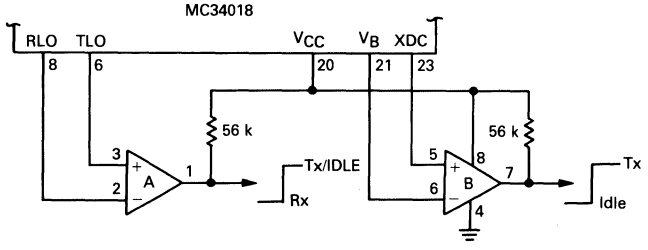
FIGURE 18 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

FIGURE 19 — BASIC LINE POWERED SPEAKERPHONE



1. Diodes are 1N4001 unless otherwise noted.
2. 4 Transistors are 2N3904.
3. Recommended Transformer: Microtran T2106.

FIGURE 20 — DIGITAL TRANSMIT/IDLE/RECEIVE INDICATION



Comparators A & B = LM393 (Dual)

MC34114

Specifications and Applications Information

2

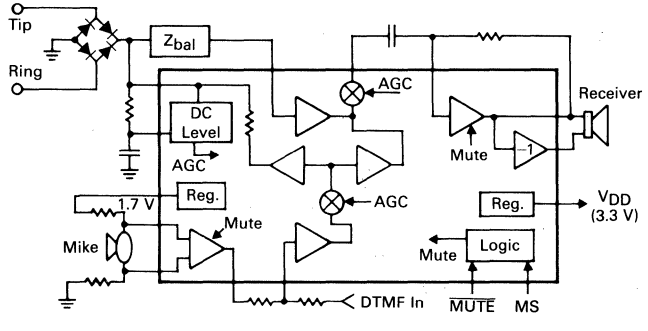
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34114 is a monolithic integrated telephone speech network designed to replace the bulky magnetic hybrid circuit of a telephone set. The MC34114 incorporates the necessary functions of transmit amplification, receive amplification, and sidetone control, each with externally adjustable gain. Loop length equalization varies the gains based on loop current. The microphone amplifier has a balanced, differential input stage designed to reduce RFI problems. A $\overline{\text{MUTE}}$ input mutes the microphone and receive amplifiers during dialing. A regulated output voltage is provided for biasing of the microphone, and a separate output voltage powers an external dialer, microprocessor, or other circuitry. The MC34114 is designed to operate at a minimum of 1.2 volts, making party line operation possible.

A circuit using the MC34114 can be made to comply with Bell Telephone, British Telecom (BT), and NTT (Nippon Telegraph & Telephone) standards. It is available in a standard 18-pin DIP, and a 20-pin SOIC (surface mount) package.

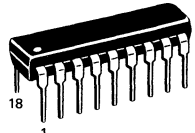
- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI Susceptibility
- Transmit, Receive, and Sidetone Equalization on Both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer or MPU
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 50 Ohms and Higher
- Complies with NTT, Bell Telephone and BT Standards

SIMPLIFIED BLOCK DIAGRAM

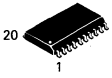


TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

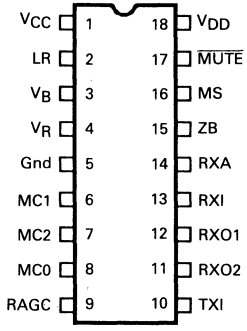


P SUFFIX
PLASTIC PACKAGE
CASE 707-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751D-03

PIN CONNECTIONS
(Top View)
(DIP Package)



ORDERING INFORMATION

Package	Part No.
18-Pin Plastic DIP	MC34114P
20-Pin Surface Mount	MC34114DW

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
V_{CC} Supply Voltage	−1.0, +12	Vdc
Voltage at V_{DD} (Externally Applied, V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	−1.0, V_{DD} + 0.5	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at RAGC (0 < V_{CC} < 12 Volts)	−1.0, +6.0	Vdc
Current through V_{CC}, LR	130	mA
Current into Z_B (Pin 15)	3.0	mA
Storage Temperature	−65, +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices can be operated at these limits. The "Recommended Operating Conditions" provides conditions for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
V_{CC} Voltage (Speech, Pulse Mode) (Tone Dialing Mode)	+1.2 +3.3	— —	+10.5 +10.5	Vdc
Loop Current (into V_{CC}) (Speech, Pulse Mode) (Tone Dialing Mode)	4.0 15	— —	120 120	mA
Receiver Impedance	50	—	—	Ω
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	0	—	V_{DD}	Vdc
R1 (Resistor from V_{CC} to V_B)	100	—	1800	Ω
Ambient Temperature	−20	—	+70	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
SUPPLY CURRENT					
Supply Current into V_{CC} (Pin 2 open, R12 = 25 k, V_{DD} unloaded)					mA
Speech Mode (Figure 2) V_{CC} = 1.2 Volts	I_{ccsp}	4.0	5.0	5.5	
V_{CC} = 3.5 Volts		9.0	11	12	
V_{CC} = 8.0 Volts		10	12	14	
V_{CC} = 10.5 Volts		—	13	—	
Tone Mode (Figure 4) V_{CC} = 3.3 Volts	I_{cct}	—	14	—	
V_{CC} = 8.0 Volts		—	16	—	
V_{CC} = 10 Volts		—	18	—	
VOLTAGE REGULATORS					
V_R Voltage (I_R = 65 μA, V_{CC} = 2.5 V, Figure 5)	V_R	1.6	1.7	1.85	Vdc
Load Regulation (0 < I_R < 300 μA, V_{CC} = 2.5 V)		—	0.2	0.5	Vdc
Line Regulation (I_R = 65 μA, 2.5 < V_{CC} < 10.5 V)		−70	±20	+70	mVdc
V_{DD} Voltage (V_{CC} ≥ 3.8 V, I_{DD} = 0, Figure 6)	V_{DD}	3.1	3.3	3.7	Vdc
Line Regulation (I_{DD} = 0, 5.0 V < V_{CC} < 10.5 V)		−70	±30	+70	mVdc
Maximum Output Current (V_{CC} = 3.8 V, V_{DD} ≥ 3.0 V)	I_{DDMAX}				mA
Speech Mode		0.8	1.0	—	
Pulse, Tone Mode		2.2	2.5	—	
Input Leakage Current (V_{CC} = 0, 3.3 Volts applied to V_{DD})	I_{lkg}				μA
$\overline{Mute}$ open or at V_{DD}		—	0.02	0.5	
$\overline{Mute}$ = 0 Volts		—	180	—	

2

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE AMPLIFIER					
Gain ($\overline{Mute}$ = V_{DD})	G_{MIC}	28	30	32	dB
Input Common Mode Rejection Ratio (1.0 kHz)	CMRR	20	26	—	dB
Input Impedance (Each Input)	R_{INMIC}	14	20	27	kΩ
MCO DC Bias Voltage (V_{CC} > 3.4 V, $\overline{Mute}$ = Hi) (V_{CC} = 1.2 V, $\overline{Mute}$ = Hi) ($\overline{Mute}$ = 0 V)	V_{MCODC}	0.85 0.6 —	1.1 0.71 0.08	1.25 0.93 —	Vdc
MCO Max Voltage Swing (THD = 5%, V_{CC} > 2.7 V) (THD = 5%, V_{CC} = 1.2 V)	V_{MCOAC}	— —	2.0 500	— —	Vp-p mVp-p
MCO Output Impedance	Z_{MCO}	—	270	—	Ω
MCO Output Current Capability (THD = 5%)	I_{MCO}	—	160	—	μA
Gain Reduction when Muted ($\overline{Mute}$ = 0 Volts, f = 1.0 kHz)	G_{MUT}	55	70	—	dB
RECEIVE AMPLIFIER					
RXI Bias Current (Mute = Hi)	I_{IBR}	—	50	—	nA
RXO1, RXO2 Bias Voltage (V_{CC} = 1.2 V) (V_{CC} > 3.0. V)	R_{XDC}	580 585	630 650	695 720	mVdc
RXO1–RXO2 Offset Voltage (V_{CC} > 3.0 V)	R_{XVOS}	−35	0	+35	mVdc
RXO1–RXO2 Max Voltage Swing (Figure 9) (THD = 5%, Receiver = ∞) (THD = 5%, Receiver = 150 Ω)	V_{RXAC}	 — —	 2.2 800	 — —	 Vp-p mVp-p
Internal Feedback Resistor (for muting)	R_{FINT}	—	1.0	—	kΩ
RXO1 & RXO2 Source Current	I_{RX}	2.6	3.2	3.5	mA
INTERNAL CURRENT AMPLIFIERS					
TXI Input Impedance	R_{TXI}	0.85	1.0	1.15	kΩ
ZB Input Impedance	R_{ZB}	—	500	—	Ω
RXA Output Impedance	R_{RXA}	—	10	—	kΩ
AC Current Gain TXI to V_{CC} (V_{RAGC} = 0 V) TXI to V_{CC} (V_{RAGC} = 1.3 V) ZB to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) ZB to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd)	 G_{TX} G_{ZB} G_{STA} 	 — — — — — —	 100 50 0.5 0.25 1.22 0.61	 — — — — — —	A/A
DC INTERFACE					
LR Level Shift (V_{CC}–V_{LR}) (I_{LOOP} = 20 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 80 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS = 0 V) (I_{LOOP} = 80 mA, $\overline{Mute}$ & MS = 0 V)	 ΔV_{LRS} ΔV_{LRT} 	 — — — —	 2.8 3.5 3.8 5.0	 — — — —	Vdc
V_{CC} Boost (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS switched from Hi to Lo, R1 = 620 Ω)	ΔV_{LRB}	0.7	1.0	1.2	Vdc
RAGC Current (V_{RAGC} = 0 V) (V_{RAGC} = 1.0 V)	I_{RAGC}	— —	−40 −12	— —	μA

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
$\overline{\text{MUTE}}$ Input Impedance (V_{CC} > 1.2 V)	R_{MUT}	—	60	—	kΩ
(V_{CC} = 0 V, 0 < $\overline{\text{Mute}}$ < 6.0 V)		—	>60	—	MΩ
Input Low Voltage	V_{ILMT}	0	—	1.0	Vdc
Input High Voltage	V_{IHMT}	V_{DD} – 0.5	—	V_{DD}	Vdc
Holdover (Delay for Receive amplifier to return to full gain after Pin 17 switches from 0 to V_{DD})	T_{MUT}	8.0	11	25	mSec
MS Input Impedance (V_{CC} > 1.2 V)	R_{MS}	—	60	—	kΩ
(V_{CC} = 0 V, $\overline{\text{Mute}}$ = open or V_{DD})		—	>50	—	MΩ
(V_{CC} = 0, $\overline{\text{Mute}}$ = 0)		—	4.0	—	kΩ
Input Low Voltage	V_{ILMS}	0	—	0.3	Vdc
Input High Voltage	V_{IHMS}	2.0	—	V_{DD}	Vdc

SYSTEM SPECIFICATIONS (f = 1.0 kHz unless noted, T_A = 25°C, Refer to Figure 1)

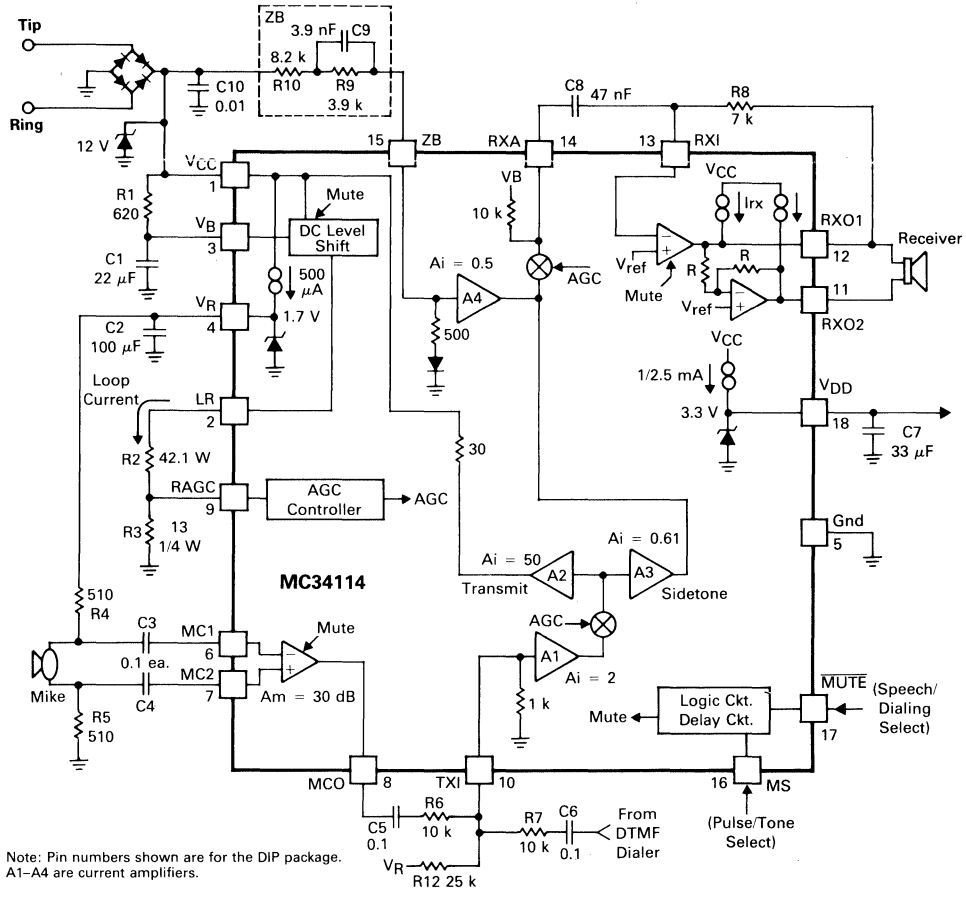
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V_{CC} DC Voltage (Pin 1)	V_{CC}				Vdc
Bell Telephone Standard and NTT Specs. (R2 = 43 Ω, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA		1.7	2.0	2.3	
I_{LOOP} = 20 mA		3.0	3.4	3.7	
I_{LOOP} = 30 mA		3.5	4.1	4.5	
I_{LOOP} = 120 mA		8.5	9.9	10.5	
Tone Mode I_{LOOP} = 20 mA		3.9	4.1	4.3	
I_{LOOP} = 30 mA		4.5	5.1	5.5	
British Telecom Standard (R2 = 43 Ω + 2.5 V Zener, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA		—	4.3	—	
I_{LOOP} = 20 mA		—	5.9	—	
I_{LOOP} = 30 mA		—	6.9	—	
I_{LOOP} = 70 mA		—	10	—	
AC Terminating Impedance (I_{LOOP} = 20 mA, Figure 11)	Z_{AC}	500	600	700	Ω
RECEIVE PATH					
Gain (V_{CC} to RXO1–RXO2, Figures 14, 15)	G_{RX}				dB
I_{LOOP} = 20 mA		–7.2	–6.1	–5.0	
I_{LOOP} = 100 mA		–13.5	–11	–9.5	
ΔGain (G_{RX} @ 100 mA versus 20 mA)	ΔG_{RX}	–7.5	–6.0	–4.5	dB
Muted Gain ($\overline{\text{Mute}}$ = Logic 0, I_{LOOP} = 20 mA)	G_{RXM}	—	–22	–20	dB
Distortion (at RXO1–RXO2, V_{CC} = 250 mVrms)	THD_R				%
f = 300 Hz		—	0.3	—	
f = 1.0 kHz		—	0.2	2.0	
f = 3.4 kHz		—	0.02	—	
Output Noise Across RXO1–RXO2 (@ 1.0 kHz)	N_{RXO}	—	4.0	—	μVrms
TRANSMIT PATH					
Gain (MC1–MC2 to V_{CC}, Figures 12, 13)	G_{TX}				dB
I_{LOOP} = 20 mA		36	38.5	40.5	
I_{LOOP} = 100 mA		29	32.5	35.5	
ΔGain (G_{TX} @ 100 mA versus 20 mA)	ΔG_{TX}	–7.5	–6.0	–4.5	dB
Max V_{CC} Voltage Swing (THD = 5%, Figure 8)	VTX_{MAX}				Vp-p
I_{LOOP} = 20 mA		—	3.0	—	
I_{LOOP} = 100 mA		—	2.3	—	
Gain Reduction when muted (MC1–MC2 to V_{CC}, $\overline{\text{Mute}}$ = 0 V)	G_{TXM}	—	68	—	dB
Distortion (0 dBm @ V_{CC})	THD_T				%
f = 300 Hz		—	0.5	—	
f = 1.0 kHz		—	1.5	3.0	
f = 3.4 kHz		—	1.3	—	
Output Noise at V_{CC} (@ 1.0 kHz)	N_{TXO}	—	17	—	μVrms
SIDETONE					
Sidetone Gain (Gain from V_{CC} to RXO1–RXO2 with signal applied to MC1/MC2, I_{LOOP} = 20 mA)	G_{ST}	—	–27	–22	dB

2

PIN DESCRIPTIONS

Symbol	Pin Number (SOIC)	Pin Number (DIP)	Description
V_{CC}	1	1	Power supply pin for the IC. Supply voltage is derived from loop current. Transmit amp output operates on this pin.
LR	2	2	Resistors R2+R3 at this pin set the DC characteristics of the circuit. The majority of the loop current flows through these resistors. Other components may be used to produce required DC characteristics for individual regulatory agencies.
V_B	3	3	A resistor or appropriate network (R1) connected from this pin to V_{CC} sets the AC terminating impedance (return loss spec).
V_R	4	4	A 1.7 volt regulated output which can be used to bias the microphone. Additionally, this voltage powers a portion of the internal circuitry. Can nominally supply 300–500 μA.
GND	5	5	Ground pin for the entire IC. Normally this is not connected to, nor to be confused with earth ground.
MC1	6	6	Inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC2	7	7	Non-inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC0	8	8	Microphone amplifier output. Amplifier's gain is fixed at 30 dB.
RAGC	10	9	Loop current sensing input. The voltage at this pin, determined by the loop current and R3, operates the loop length equalization circuit.
TXI	11	10	Input to the transmit amplifier from the microphone amplifier, DTMF source, and other sources. Input impedance ≈ 1.0 kΩ.
RXO2	12	11	Receive amplifier non-inverting differential output. Current capability to the receiver is typically set at ±3.0 mA peak.
RXO1	14	12	Receive amplifier inverting differential output. Current capability to the receiver is typically ±3.0 mA peak. Gain is set by R8.
RXI	15	13	Summing input to the receive amplifier. This pin is an AC virtual ground.
RXA	16	14	Summed outputs of the receive current amplifier, sidetone amplifier, and an AGC point. Normally connected to the receive amplifier input (RXI) through a coupling capacitor.
ZB	17	15	Input to the receive current amplifier. A balance network (ZB) is connected between this pin and V_{CC}. The network affects the receive level and sidetone performance. Input impedance is ≈500 Ω in series with a diode.
MS	18	16	Mode Select Input. A logic "1" sets the IC for pulse dialing. A logic "0" sets the IC for tone (DTMF) dialing. Effective only if $\overline{\text{MUTE}}$ is at a logic "0". Input impedance is ≈ 60 kΩ.
$\overline{\text{MUTE}}$	19	17	$\overline{\text{Mute}}$ input. A logic "1" sets normal speech mode. A logic "0" mutes the microphone and receive amplifiers and allows MS to be functional. Input impedance is ≈60 kΩ referenced to V_{DD}. An internal fixed delay of 11 mSec minimizes clicks in the receiver when returning to the speech mode.
V_{DD}	20	18	A regulated 3.3 volt output for an external dialer. Output source current capability is 1.0 mA in speech mode, 2.5 mA in tone dialing mode.

FIGURE 1 — BLOCK DIAGRAM AND TEST CIRCUIT



Note: Pin numbers shown are for the DIP package.
A1–A4 are current amplifiers.

FIGURE 2 — I_{CC} versus V_{CC} (SPEECH MODE)

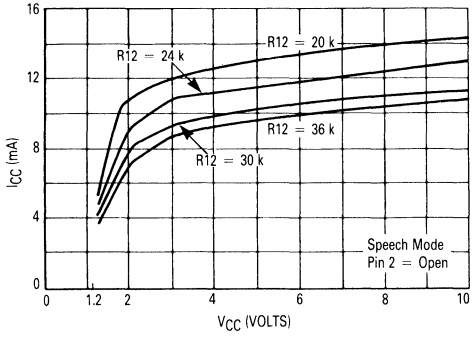


FIGURE 3 — I_{CC} versus V_{CC} (PULSE DIALING MODE)

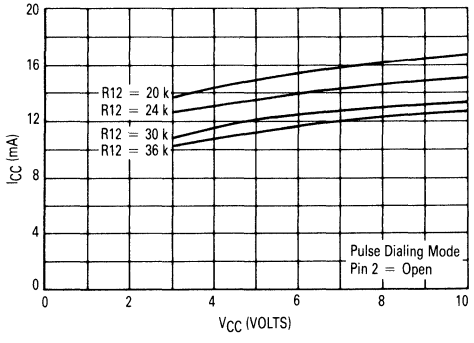


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FIGURE 4 — I_{CC} versus V_{CC} (TONE DIALING MODE)

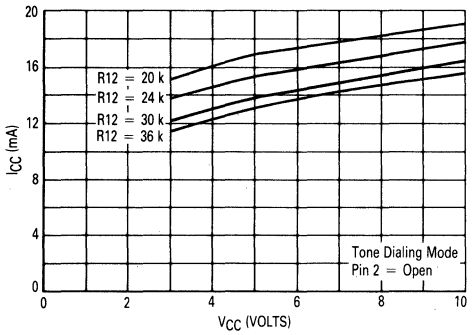


FIGURE 5 — V_R versus I_R versus V_{CC}

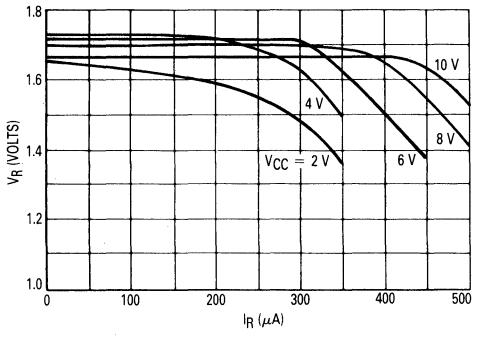


FIGURE 6 — V_{DD} versus I_{DD}

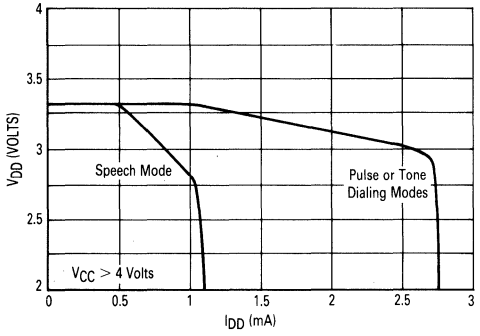


FIGURE 7 — AGC GAIN versus VOLTAGE AT PIN 9

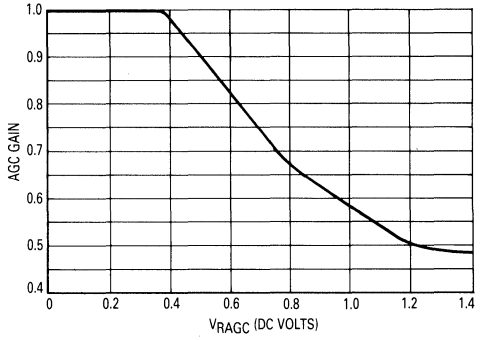


FIGURE 8 — MAXIMUM TRANSMIT SIGNAL AT V_{CC}

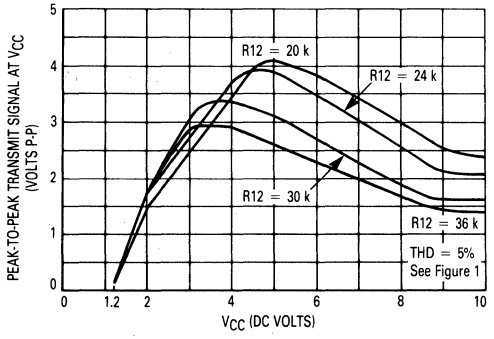
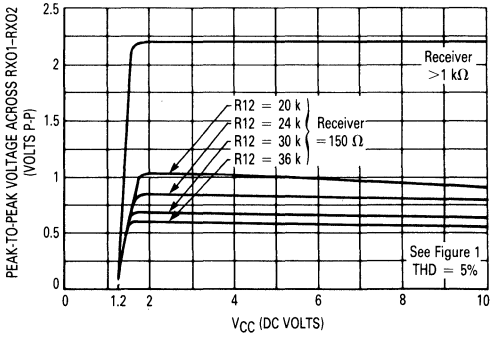


FIGURE 9 — MAXIMUM RECEIVER SIGNAL



SYSTEM PERFORMANCE

FIGURE 10 — TIP/RING VOLTAGE versus LOOP CURRENT

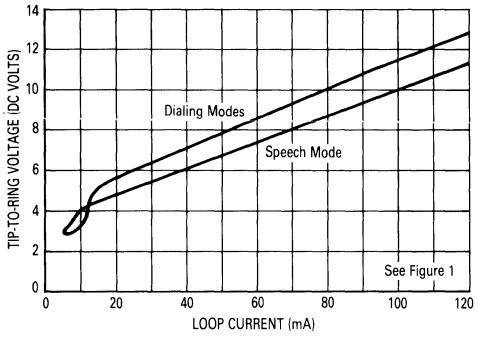


FIGURE 11 — AC TERMINATING IMPEDANCE versus LOOP CURRENT

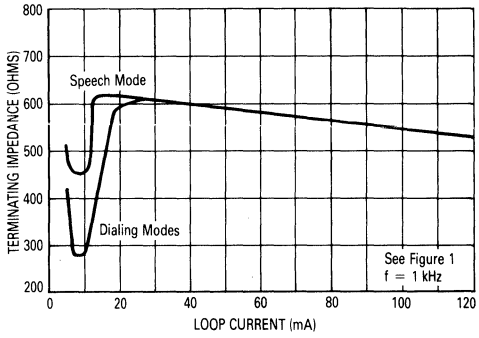


FIGURE 12 — TRANSMIT GAIN versus LOOP CURRENT

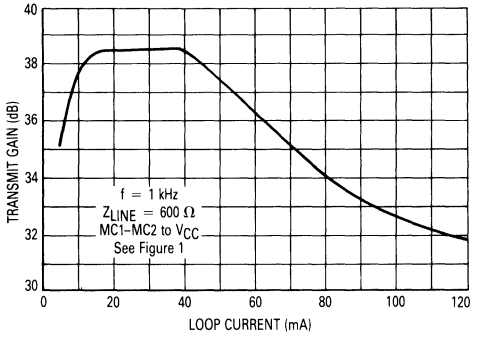


FIGURE 13 — TRANSMIT GAIN versus FREQUENCY

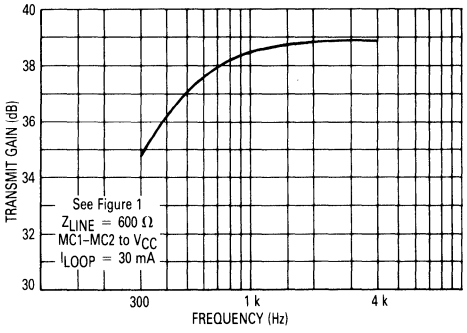


FIGURE 14 — RECEIVE GAIN versus LOOP CURRENT

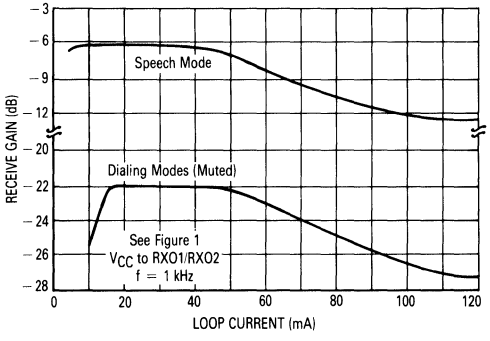
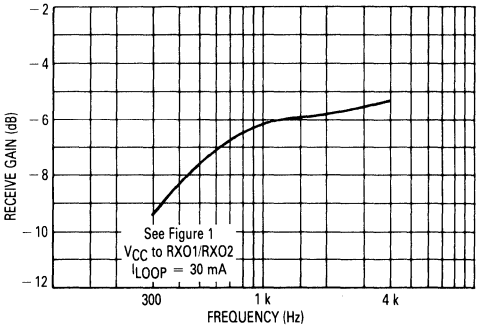


FIGURE 15 — RECEIVE GAIN versus FREQUENCY



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SYSTEM PERFORMANCE

FIGURE 16 — TRANSMIT NOISE SPECTRUM

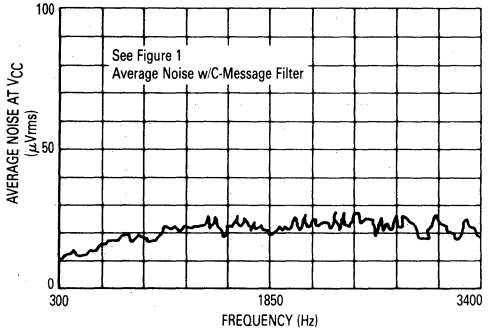


FIGURE 17 — RECEIVE NOISE SPECTRUM

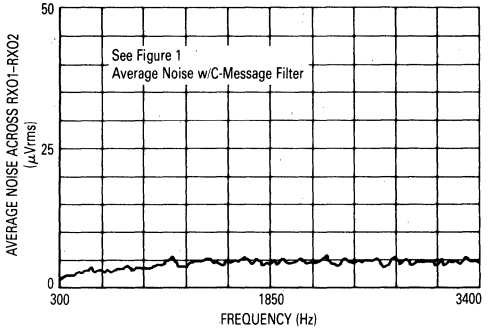


FIGURE 18 — V_{CC} versus TEMPERATURE

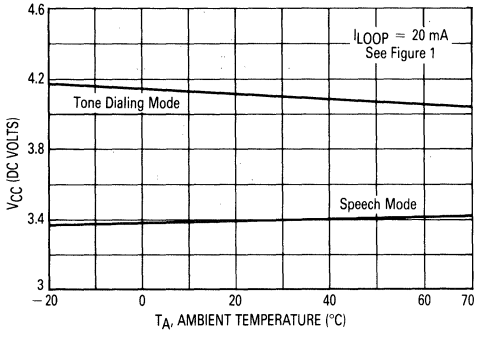


FIGURE 19 — TRANSMIT GAIN versus TEMPERATURE

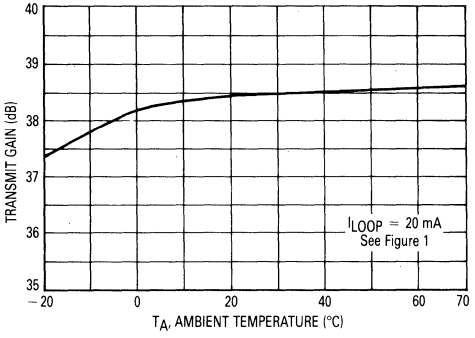


FIGURE 20 — RECEIVE GAIN versus TEMPERATURE

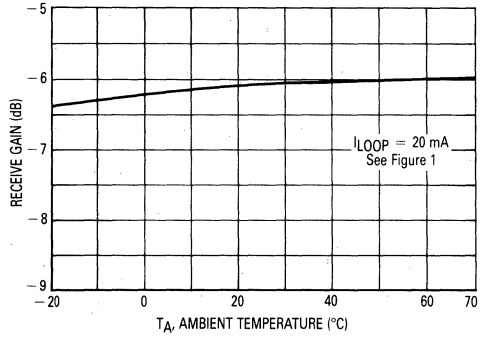
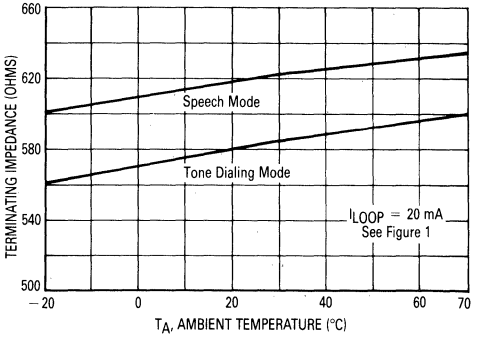


FIGURE 21 — AC TERMINATING IMPEDANCE versus TEMPERATURE



FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC34114 is a speech network which provides the hybrid function and the DC loop current interface of a telephone, and is meant to connect to Tip and Ring through a polarity guard bridge. The transmit, receive, and sidetone gains are externally adjustable, and additionally, line length compensation varies the gains with variations in loop current. The microphone amplifier employs a differential input to minimize RFI susceptibility.

The loop current interface portion determines the dc voltage versus current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing and tone (DTMF) dialing. When switching among the modes, some parameters are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

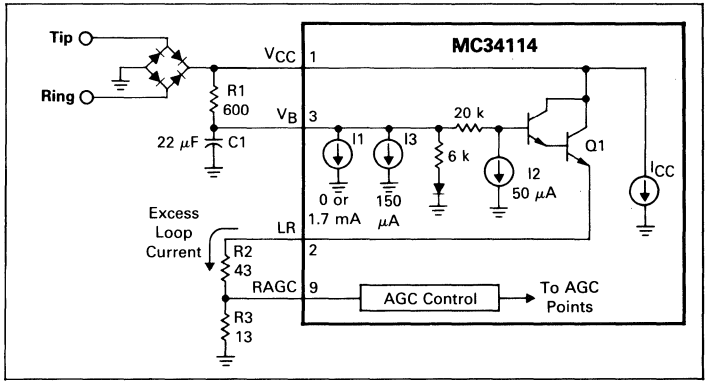
TABLE 1 — OPERATING PARAMETERS versus OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift (V_{CC} – VLR)	2.8 V	2.8 V	3.8 V
V_{DD} Current Capability	1.0 mA	2.5 mA	2.5 mA
Microphone Amplifier	Functional	Muted	Muted
Receive Amp. Internal Feedback Resistor	Switched Out	Switched In	Switched In

DC LINE INTERFACE AND LINE LENGTH COMPENSATION

The DC line interface circuit (Pins 1, 2, 3) sets the DC voltage characteristics with respect to loop current. See Figure 22.

FIGURE 22 — DC LINE INTERFACE EQUIVALENT



The DC voltage at V_{CC} is determined by the level shift from V_{CC} to LR, plus the voltage across R2 and R3. I_{CC} is the internal bias current required by the MC34114, nominally in the range of 10 mA. I_{CC} can be reduced, if necessary, by increasing R12, consistent with the transmit and receive signal requirements (see the Transmit Path section). See Figures 2–4, 8 and 9.

In the speech and pulse dialing modes current source I1 is off, and the level shift is due to Q1's base-emitter drop (≈1.4 V), 1.0 volt across the 20 k resistor, and the voltage across R1, which varies with V_{CC} from 0.15 volts to ≈1.0 volt. When the loop current coming in from Tip and Ring exceeds the I_{CC} requirement, the excess current flows through Q1, R2 and R3, to set the slope of the V-I characteristic for the circuit (Q1 has an equivalent resistance of ≈10 Ω). See Figure 10.

In the tone dialing mode, current source I1 is on, drawing an additional 1.7 mA through R1, increasing the level shift by ≈1.0 volts (for R1 = 600 Ω). This feature ensures that, at low loop currents, sufficient voltage is present at V_{CC} for the DTMF signals, and that the V_{DD} regulator supplies sufficient voltage to an external dialer. The I_{CC} current increases by ≈1.3 mA in this mode.

R1 must be kept in the range of 100 to 1800 Ω. If it is too large, insufficient current will flow into V_B to bias up the circuit. If it is too small, insufficient filtering at V_B will result unless C1 is increased accordingly. Speech signals must be well filtered from V_B.

The voltage across R3 determines the operation of the AGC circuit (line length compensation). As the voltage at RAGC increases from ≈0.4 volts to ≈1.2 volts, the AGC Control varies the current gain of the two AGC

points (Figure 1) from 1.0 to 0.5, thereby reducing the gain of the transmit and receive paths by 6.0 dB. See Figure 7. Pin 9 is a high impedance input.

The values of R2 and R3 can be varied as required to comply with various regulatory agencies, to compensate for additional circuitry powered by the loop current (microprocessor, etc.), or to change the starting point of the AGC function. If the AGC is not used, Pin 9 should be connected to ground for high gains, or to V_R for low gains.

VOLTAGE REGULATORS

The MC34114 has two internal voltage regulators which are used to power external as well as internal circuitry.

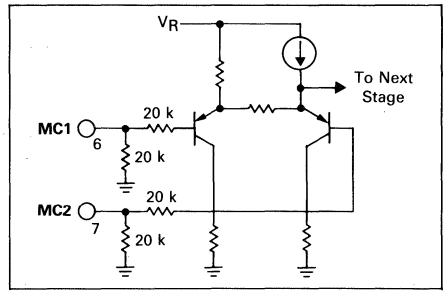
The V_R regulator provides 1.7 volts at a maximum current of 500 μA (see Figure 5). This output is normally used to set the DC bias into TXI (Pin 10), and to bias the electret microphone. V_R will typically be ≈300 mV less than V_{CC} when V_{CC} is below 2.0 volts.

The V_{DD} regulator provides 3.3 volts at a maximum of 1.0 mA in the speech mode, and 2.5 mA in the pulse or tone dialing modes (see Figure 6). It is normally used to power an external dialer, and other associated circuitry. V_{DD} is normally ≈0.5 volts less than V_{CC} until V_{DD} regulates. It is a shunt type regulator which automatically switches to a high impedance mode when V_{CC} falls below 1.4 volts. This feature prevents excessive battery drain in the event a memory sustaining battery is used with the external dialer. Leakage current (with V_{CC} = 0) is typically 0.02 μA with an applied voltage of up to 6.0 volts at V_{DD}, with pin 17 open or at V_{DD}. If Pin 17 is at ground, a current of several hundred microamps will flow into V_{DD} and out of pin 17 (see paragraph on Logic Interface).

MICROPHONE AMPLIFIER

The microphone amplifier (Pins 6, 7, 8) has a differential input, single ended output, and a fixed internal gain of +30 dB (31.1 V/V). The output is in phase with MC2, and out of phase with MC1. The inputs (see Figure 23) have a nominal impedance of 20 kΩ, and are matched to provide a high common mode rejection (typically 26 dB).

FIGURE 23 — INPUT STAGE



To preserve a high CMRR against unwanted signals induced in the microphone leads, the microphone should be biased with two equal value resistors as shown in Figure 1.

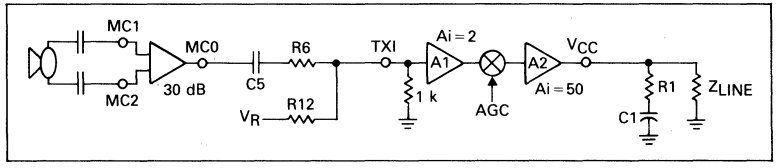
The output (MCO) has a DC bias voltage of ≈1.1 volts (V_{CC} > 3.0 volts), and can nominally swing ≈2.0 volts p-p (500 mV p-p at V_{CC} = 1.2 volts). The output impedance is ≈270 Ω, and has a peak current capability of ≈160 μA for 5% THD.

When the MC34114 is switched to either dialing mode, the microphone amplifier is muted by ≈70 dB (300 Hz–4 kHz), effectively disabling the microphone. The DC voltage at MCO is ≈80 mV when muted.

TRANSMIT PATH

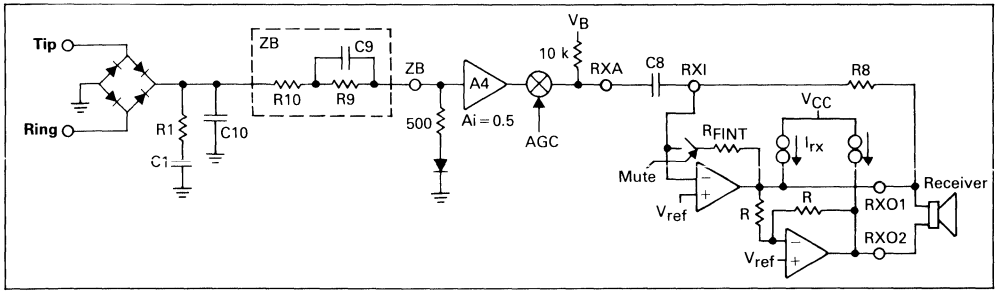
The AC transmit path consists of the components shown in Figure 24 (taken from Figure 1).

FIGURE 24 — TRANSMIT PATH



The voltage output at MCO is converted to a current into TXI by C5, R6, and TXI's 1.0 k input impedance (with a slight error due to R12). A1 and A2 are current amplifiers with a combined gain of 100. The AGC point has a current gain of 1.0 at low loop currents, and decreases to 0.5 as loop current increases. Therefore the current gain from TXI to V_{CC} varies from 100 to 50 as loop current is increased. The resulting current output at V_{CC} acts on R1 and the line impedance (nominally 600 Ω each, C1 is an AC short) to generate a voltage

FIGURE 25 — RECEIVE PATH



signal at V_{CC}, and consequently, at Tip and Ring. The voltage gain from MC1–MC2 to Tip and Ring is therefore (first order):

$$G_{TX} = \frac{Am \times 100 \times AGC \times R1//Z_{LINE}}{(R6 + 1.0\ k)} \quad \text{(Equation 1)}$$

where Am is the gain of the microphone amplifier (31.1 V/V). At low loop currents G_{TX} ≈84 V/V (38.5 dB), and decreases to ≈42 V/V (32.5 dB) at higher loop currents, for the component values shown in Figure 1 (@ 1.0 kHz).

For more precise calculations, consideration should be given to the effects of C5 (in series with R6), R12 and R7 (each in parallel with TXI's 1.0 k impedance), and C10 and the ZB network (each in parallel with R1 and Z_{LINE}). The cumulative effects of these additional components is ≈1.5 dB.

The voltage signal at V_{CC} is out of phase with that at TXI, and in phase with that at MC1.

The maximum available voltage swing at V_{CC} is a function of the impedance at V_{CC} (R1//Z_{LINE}), the DC bias current at A2's output, and the V_{CC} DC voltage. A2's bias current is determined by the bias current through R12 (V_R/R12 + 1.0 k}) which is gained up by A1, A2 and the AGC point. Figure 8 indicates the maximum voltage swing at V_{CC} (with 5% THD).

RECEIVE PATH

The AC receive path consists of the components shown in Figure 25 (taken from Figure 1).

R1, typically 600 Ω, provides the AC termination (return loss) for the receive signals coming in on Tip and Ring (C1 is an AC short). The receive signal creates an AC current through the ZB network and the 500 Ω resistor at the ZB pin. A4 reduces that current by 1/2, and then feeds it through the AGC point which has a gain of 1.0 at low loop currents. The AGC gain is reduced to 0.5 as loop current increases. The AC current out of the AGC point feeds through C8 to RXI, the receive amp's summing node (If C8 is large, RXA can be considered a virtual ground, and no AC current flows through the internal 10 k resistor). The voltage swing at RXO1 is then determined by the current through C8 and the R8 feedback resistor. The second op amp (at RXO2) is internally configured for inverting unity gain. The voltage gain from Tip and Ring to RXO1–RXO2 (differential) is (first order):

$$G_{RX} = \frac{R8 \times AGC}{(ZB + 500)} \quad \text{(Equation 2)}$$

where ZB = R10 + R9//C9 (≈R10 + R9).

For more precise calculations, the effects of C9 and C8 must be considered. C9 provides a phase shift to aid sidetone cancellation (see paragraph on Sidetone), and C8 can be selected to provide low frequency roll-off. High frequency roll-off can be obtained by adding a feedback capacitor across R8. For the component values shown in Figure 1, the receive gain measured ≈0.495 V/V (−6.1 dB) at low loop currents, and reduces to ≈0.25 V/V (−12 dB) at higher loop currents (@ 1.0 kHz).

When the MC34114 is switched to either dialing mode ($\overline{Mute}$ = low), the receive gain is muted by the switching in of the internal feedback resistor (R_{FINT} from RXO1 to RXI) — typically 1.0 kΩ. The effective feedback resistor for the amplifier is now the parallel combination of R8 and R_{FINT}. The amount of muting (in dB) can be calculated from:

$$G_{RXM} = 20 \times \log\left(\frac{R8 + R_{FINT}}{R_{FINT}}\right) \quad \text{(Equation 3)}$$

The internal resistor is switched in coincident with $\overline{Mute}$ (Pin 17) switching low. However, when $\overline{Mute}$ is switched high, a delay (nominally 11 mSec) occurs before the internal resistor is switched out. This feature prevents dialing transients (particularly during pulse dialing) from being heard as loud clicks in the receiver.

The DC bias voltages at RXI, RXO1 and RXO2 is ≈0.65 volts. The bias current at RXI is ≈50 nA into the pin. The maximum voltage swing at RXO1 and RXO2 is a function of the receiver impedance (typically 100–150 Ω), and the value of the two I_{rx} current sources in Figure 25. I_{rx}, set by R12 (between V_R and TXI), is equal to:

$$I_{rx} = \frac{V_R \times 50 \times AGC}{(R12 + 1.0\ k)} \quad \text{(Equation 4)}$$

Figure 9 indicates the maximum voltage swing available to the receiver.

2

SIDETONE CANCELLATION

Sidetone cancellation is provided by current amplifier A3 (see Figure 1) which generates a current representative of the transmit signal to cancel the reflected sidetone signal coming in through ZB and A4. To achieve perfect cancellation (no AC current out of RXA), it is necessary that:

$$ZB = (40 \times R1 // Z_{LINE}) - 500\ \Omega \quad \text{(Equation 5)}$$

where ZB is the network composed of R9, R10, and C9, and Z_{LINE} is the AC impedance of the line. The reactive components of the line's impedance can be compensated for by making the ZB network comparably reactive. In Figure 1, C9 provides a phase shift to compensate for the phase shift created by the phone line.

LOGIC INTERFACE ($\overline{\text{Mute}}$ and MS)

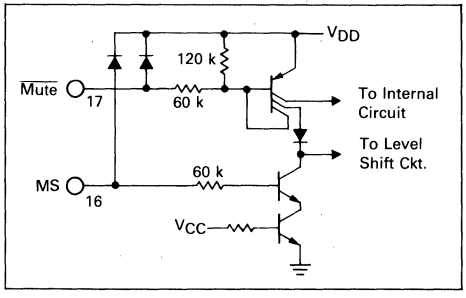
The two logic inputs ($\overline{\text{Mute}}$ and MS) are used to switch the MC34114 between the speech and dialing modes according to the following table:

TABLE 2 — LOGIC INPUTS

$\overline{\text{Mute}}$	MS	Mode
High	X	Speech
Low	High	Pulse Dialing
Low	Low	Tone Dialing

Table 2, together with Table 1, describes the condition of the MC34114 in the various modes. Figure 26 shows the input configuration for the $\overline{\text{Mute}}$ and MS pins.

FIGURE 26 — LOGIC INPUTS



The $\overline{\text{Mute}}$ input has a nominal input impedance of 60 kΩ, referenced to V_{DD}. This pin may be left open for a logic "1," or connected to V_{DD}. A logic "1" is defined as between V_{DD}–0.5 volts and V_{DD}. A logic "0" is defined as between ground and 1.0 volt. The switching threshold is ≈2.3 volts. When $\overline{\text{Mute}}$ is switched low (speech to dialing), the changes listed in Table 1 will occur within 10 μs. Upon switching high (back to speech mode), however, the receive amplifier feedback resistor will be switched out after a delay of (typically) 11 ms. This feature prevents dialing transients (particularly during pulse dialing) from being heard as loud clicks in the receiver. The other functions listed in Table 1 transfer within 10 μs.

The MS pin is functional only when $\overline{\text{Mute}}$ is low and its only function is to provide an additional voltage level shift between V_{CC} and LR in the tone dialing mode (see the section on DC Interface). The input impedance is ≈60 kΩ when $V_{CC} > 1.5$ volts. A logic "0" is between ground and 0.3 volts, and a logic "1" is between 2.0 volts and V_{DD}. The switching threshold is typically 0.75 volts. If unused, this pin must be connected to ground or V_{DD}, and not left open.

When $V_{CC} = 0$ (on-hook condition), and a voltage in the range of 0 to 6.0 volts is applied to $\overline{\text{Mute}}$, a leakage current of (typically) 0.02 μA will flow if $\overline{\text{Mute}}$ and V_{DD} are at the same voltage. If $\overline{\text{Mute}}$ is at a voltage different from V_{DD}, current will flow through the internal resistors and/or diode. If a memory sustaining battery is used in conjunction with an external dialer, and is configured so that its voltage appears at V_{DD}, $\overline{\text{Mute}}$ must be allowed to float or be connected to V_{DD} — otherwise current (in the range of 100–200 μA) will flow from the battery through V_{DD} and out of the $\overline{\text{Mute}}$ pin.

When $V_{CC} = 0$, and a voltage in the range of 0 to 6.0 volts is applied to MS, a leakage current of (typically) 0.01 μA will result as long as $\overline{\text{Mute}}$ is open or at V_{DD}. If $\overline{\text{Mute}}$ is at ground, an equivalent 3.5 kΩ parasitic resistance exists between MS and $\overline{\text{Mute}}$.

When $V_{CC} < 1.5$ volts, the Mute function is nonexistent and the MC34114 will be in the speech mode.

APPLICATIONS INFORMATION

DESIGN SEQUENCE

The design sequence for incorporating the MC34114 into most applications will be as follows (refer to Figure 1):

1) Decide on the AC terminating impedance (return loss), and select R1 to be that value (typically 600 Ω). If there are other devices powered by the loop current which will be in parallel with R1 (such as a pulse dialing circuit) which lower the effective terminating impedance, R1 can be increased accordingly.

2) Select the maximum value of R12 which will provide the minimum required transmit and receive signals according to Figures 8 and 9.

3) Select the sum {R2 + R3} to provide the desired Tip and Ring DC voltage versus loop current characteristics. Then select R3 for the desired starting point of the loop length compensation. The compensation begins when the voltage across R3 is ≈0.4 volt.

4) Select R4 and R5 (they should be equal) to properly bias the microphone. The microphone's manufacturer should be consulted for this information.

5) Select R6 for proper transmit gain. See equation 1. Then select C5 to provide low frequency roll-off. Adjust R6 as required.

6) Select the ZB network (R9, R10, C9) to provide sidetone cancellation. See equation 5.

7) Select R8 for proper receive gain (depends on the specific receiver used). See equation 2. Then select C8 to provide low frequency roll-off. Adjust R8 as required.

Additional comments on Figure 1 components:

1) Capacitors C1, C2, and C7 are required to stabilize the respective regulators. In most applications it should not be necessary to change from the values shown in Figure 1.

2) C3 and C4 can be selected to provide low frequency roll-off for the microphone signals.

3) C10 filters noise generated by the MC34114, and should be close to the V_{CC} pin. Its recommended value (0.01 μF) is such that it does not noticeably affect the system parameters. It can be increased, if desired, to provide high frequency roll-off for both transmit and receive signals. This, however, will affect the return loss specification at higher frequencies.

4) Since TXI is a (relatively) low impedance current input, it is a convenient point for injecting any signals which are to be transmitted out onto Tip and Ring. C6 and R7 are shown for transmitting the DTMF signals from a dialer. Additional RC networks can be connected to TXI for transmitting signals from speakerphones, modems, or other signal sources. The voltage gain from each signal source to Tip and Ring is:

$$G_S = \frac{Z_{LINE}//R1 \times 100 \times AGC}{(R_X + Z_{CX})} \quad \text{(Equation 6)}$$

where R_X and Z_{CX} represent the impedances of the R and C for the particular signal source. If several signal sources are connected to TXI, the parallel combination of R6, R12, the internal 1.0 k resistor, and any other RCs at this pin must be considered when setting the gain for each signal.

5) The 12 volt zener diode shown in Figure 1 is for transient protection, and normally does not conduct. Transient and overvoltage protection **MUST** be provided externally so that the Absolute Maximum Ratings are not exceeded.

BASIC TELEPHONE CIRCUIT

Figure 27 depicts a complete basic telephone using the MC34114 speech network, the MC145412 pulse/tone dialer, and the MC34017 tone ringer.

The MC34114 provides the speech network/hybrid functions, and its component values are calculated as described previously in this data sheet. The resistor from V_{CC} to V_B is 820 Ω (rather than 600 Ω) in this example since it is in parallel with the 2.0 kΩ resistor in the pulse dialing transistor network (providing and effective 600 Ω termination).

The MC145412 dialer is a pulse/tone dialer with 10 number memory, including last number redial. Power to the dialer is from the MC34114's V_{DD} output, diode connected with a memory sustaining battery.

The MC34017 tone ringer (see its data sheet for details) is connected directly to Tip and Ring as it is not necessary to disconnect it when off-hook. This circuit has an REN ≈0.5, and meets all EIA-470 and Bell system requirements for impedance, anti-bell tapping, and turn-on/off thresholds.

OPERATION WITH A POWER SUPPLY

Figure 28 indicates how to incorporate the MC34114 into a circuit where a power supply is used.

FIGURE 27 — BASIC PULSE/TONE TELEPHONE

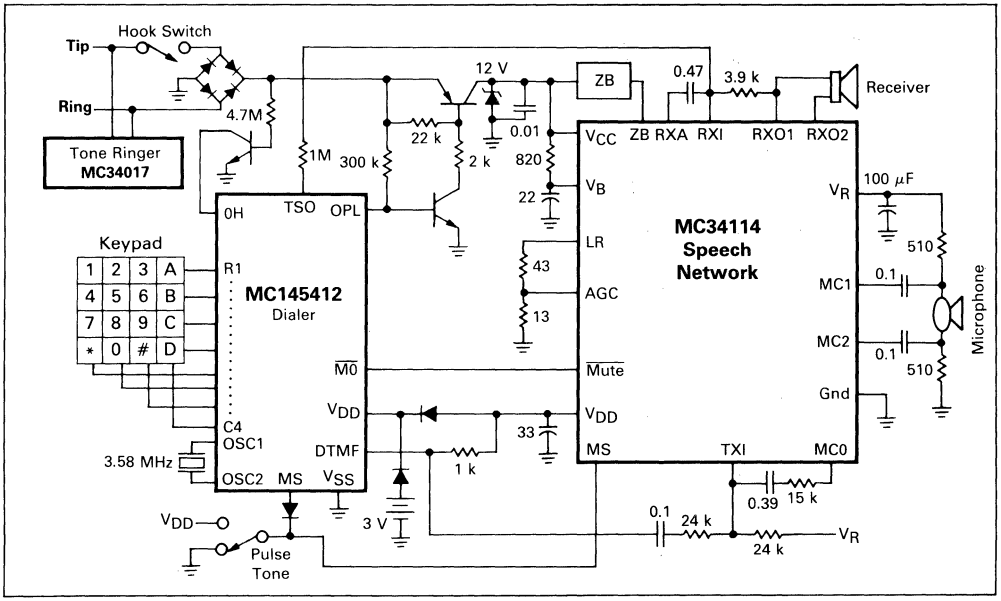
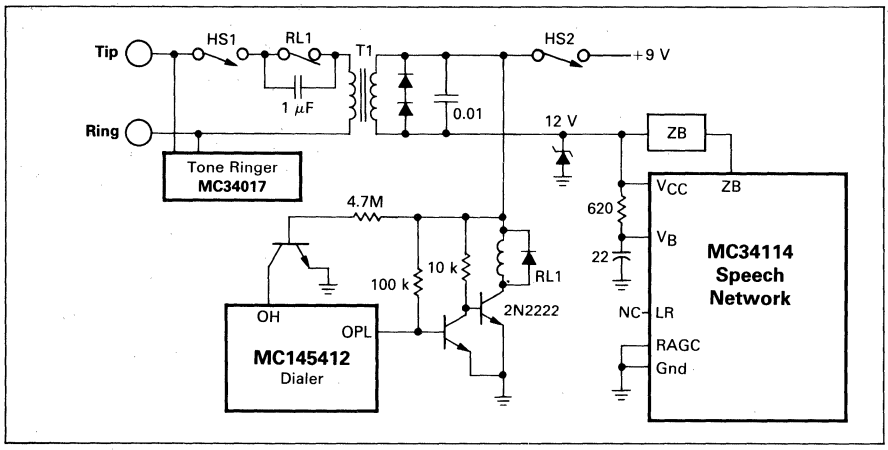


FIGURE 28 — USE WITH A POWER SUPPLY



A transformer (T1) is required at Tip and Ring to provide the isolation required between the phone line and any AC power and earth ground. (The transformer must be rated to handle the loop current.) Since the loop current does not pass through the MC34114, loop length compensation is not possible in this circuit, and pin 2 (LR) is left open. The RAGC pin is grounded, setting the transmit and receive gains to their maximum.

The transformer provides a path for the power supply to reach the MC34114, while simultaneously coupling speech signals between Tip/Ring and the MC34114. The two series diodes provide transient clamping, as does the 12 volt zener diode. Although a +9.0 volt supply is shown, other voltages can be used as long as the MC34114 receives between 4.0 and 10.5 volts at V_{CC}.

Because of the isolation requirement, the MC145412 dialer requires a relay (RL1) to break the loop current during pulse dialing. The relay is normally off, and energized only during pulse dialing. The 1.0 μF capacitor (rated 250 volts min., NPO) across the relay contacts helps absorb transients generated during pulse dialing.

ALTERNATE MICROPHONE CONFIGURATIONS

The MC34114 is designed for use with electret microphones, although dynamic microphones can be used. Carbon microphones are not recommended as they generally require considerable bias current which is not available from the MC34114's regulators.

When using an electret microphone which requires more than 1.7 volts, but less than 1.0 mA for bias, it can be biased from V_{DD} instead.

If a three terminal electret microphone (containing an internal biasing resistor or equivalent) is used, it should be connected to the MC34114 as shown in Figure 29. The common mode rejection of the balanced circuit shown in Figure 1 is not present however, and care should be taken to prevent unwanted signals (radio stations, noise, etc.) from being picked up by the microphone leads.

FIGURE 29 — 3-TERMINAL MICROPHONE

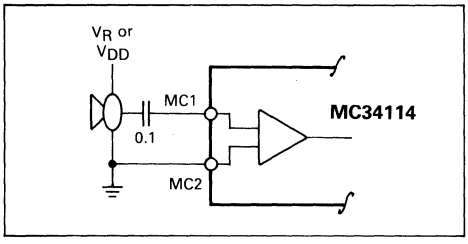
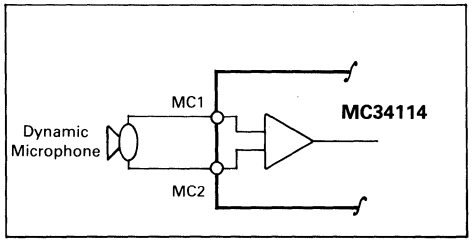


Figure 30 indicates use of the MC34114 with a dynamic microphone. The output level of dynamic microphones is generally lower than electret units, and so the gain of the transmit path will have to be adjusted accordingly.

FIGURE 30 — DYNAMIC MICROPHONE

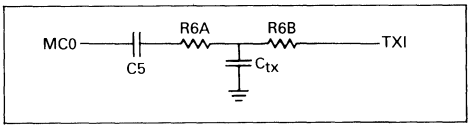


FREQUENCY CHARACTERISTICS

Frequency characteristics for both transmit and receive signals are dependent entirely on the external components. The amplifiers within the IC have bandwidths from DC extending to in excess of 50 kHz, and therefore do not provide roll-off within the voiceband.

Low frequency roll-off for the transmit signals can be set by adjusting C3 and C4, or C5, or a combination of the three. High frequency roll-off can be provided by replacing R6 with the network shown in Figure 31.

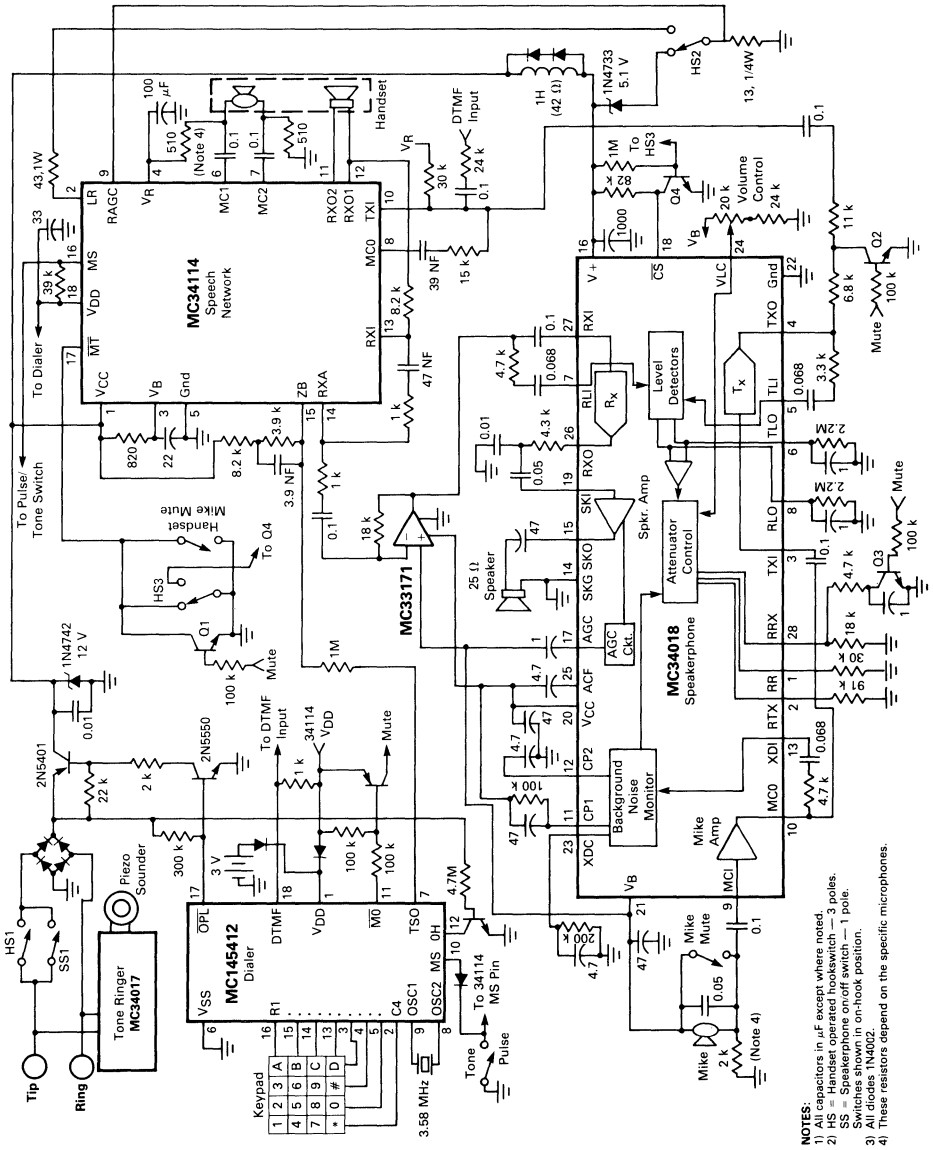
FIGURE 31 — TRANSMIT HF ROLL-OFF



The 3.0 dB upper frequency is determined by:

$$f = \frac{(R6A + R6B + 1.0\ k)}{2\pi\ (R6A \times (R6B + 1.0\ k) \times C_{tx})} \quad \text{(Equation 7)}$$

FIGURE 32 — PULSE/TONE FEATUREPHONE WITH MEMORY — LINE POWERED



Low frequency roll-off for the receive signals can be set by adjusting C8, and high frequency roll-off can be set by placing a capacitor across R8.

FEATUREPHONE DESIGN

Figure 32 and Figure 33 depict two featurephone circuits which include the following functions: selectable handset and speakerphone operation, ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike mute) function, and line length compensation for both handset and speakerphone operation. Figure 32 uses the MC34018 speakerphone IC, while Figure 33 uses the MC34118 speakerphone IC. Application notes AN1002 and AN1004 (for Figure 32 and Figure 33 respectively) should be consulted for design and performance details, as well as variations of these two circuits.

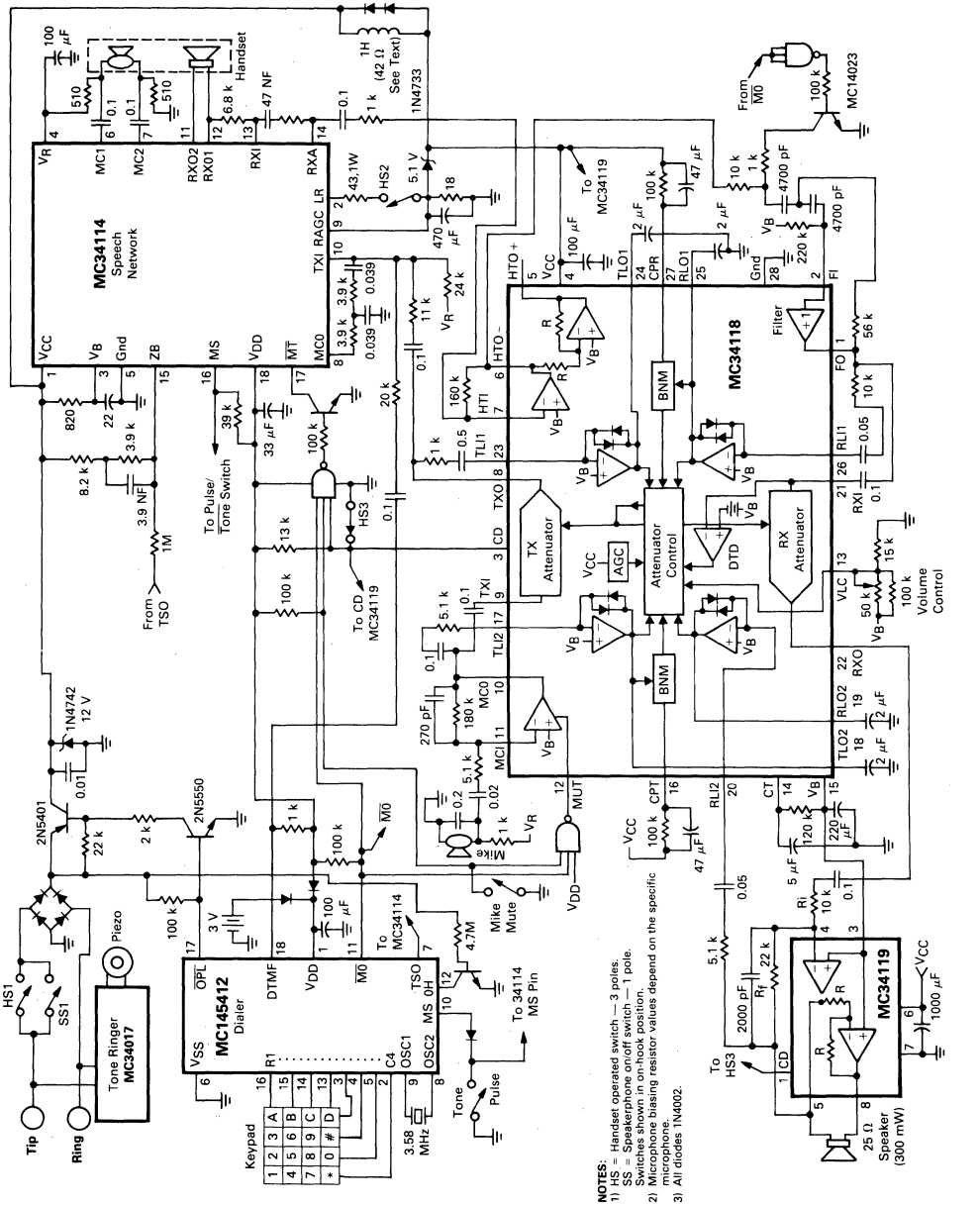


FIGURE 33 — PULSE/TONE FEATUREPHONE WITH MEMORY — LINE POWERED

EMI SUSCEPTIBILITY

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the telephone. EMI may enter the circuit through Tip and Ring, through the microphone wiring, or through any of the PC board traces. The most sensitive pins on the MC34114 are the microphone amplifier inputs (MC1, MC2). Board traces to these pins should be kept short, and the associated components should preferably be physically close to the pins. TXI, RXI, and ZB should also be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Ask for Applications
Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600

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Compliance with FCC or other regulatory agencies of the circuits described herein is not implied or guaranteed by Motorola Inc.

MC34115

Specifications and Applications Information

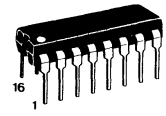
2

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC34115 CVSD is designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding functions.

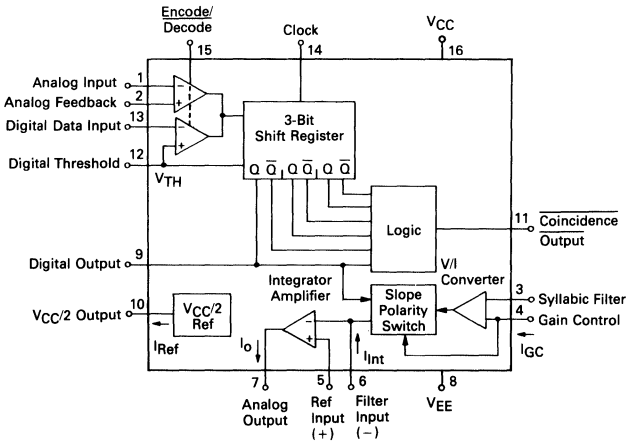
- Encode and Decode Functions Selectable with a Digital Input
- Utilization of Compatible I^2L — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- 3-Bit Algorithm

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

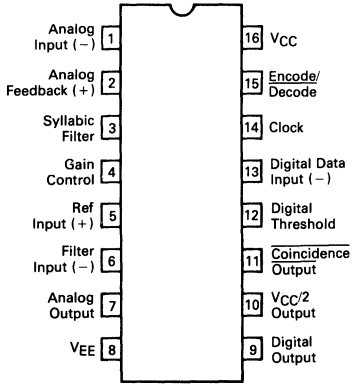


P SUFFIX
PLASTIC PACKAGE
CASE 648-08

CVSD BLOCK DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.) (See Note 2.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to + 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CC}	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}				mA
V_{CC} = 5.0 V		—	4.6	7.5	
V_{CC} = 15 V		—	7.0	12	
Clock Rate	SR	—	16 k	—	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	—	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) 4.75 V ≤ V_{CC} ≤ 16.5 V	V_I	1.3	—	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) 4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA	V_O	1.3	—	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3)	I_{IB}				μA
Comparator in Active Region					
Analog Input (I1)		—	0.5	2.5	
Analog Feedback (I2)		—	0.5	2.5	
Syllabic Filter Input (I3)		—	0.06	0.5	
Reference Input (I5)		—	−0.06	−0.5	
Input Offset Current	I_{IO}				μA
Comparator in Active Region					
Analog Input/Analog Feedback |I1−I2| — Figure 3		—	0.15	0.8	
Integrator Amplifier |I5−I6| — Figure 4		—	0.02	0.2	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	—	2.0	10	mV
Transconductance	gm				mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	—	
Integrator Amplifier, 0 to +5.0 mA Load		1.0	10	—	
Propagation Delay Times (Note 1)					μs
Clock Trigger to Digital Output	t_{PLH}	—	1.0	3.0	
C_L = 25 pF to Gnd	t_{PHL}	—	0.8	3.0	
Clock Trigger to Coincidence Output	t_{PLH}	—	1.0	3.5	
C_L = 25 pF to Gnd	t_{PHL}	—	0.8	2.5	
R_L = 4.0 kΩ to V_{CC}					

NOTES 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

2

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Coincidence Output Voltage — Low Logic State $I_{OL(Con)}$ = 3.0 mA	$V_{OL(Con)}$	—	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State V_{OH} = 15 V	$I_{OH(Con)}$	—	0.01	0.5	μA
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	—	V_{CC} −2.0	Vdc
Digital Threshold Input Current 1.2 V ≤ V_{th} ≤ V_{CC} −2.0 V	$I_{I(th)}$				μA
V_{IL} applied to Pins 13, 14 and 15		—	—	5.0	
V_{IH} applied to Pins 13, 14 and 15		—	−10	−50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	—	—	mA
V_{CC}/2 Generator Maximum Output Current (Source only)	I_{Ref}	+10	—	—	mA
V_{CC}/2 Generator Output Impedance 0 to +10 mA	z_{Ref}	—	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance 4.75 V ≤V_{CC}≤16.5 V	ϵ_r	—	—	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)					Vdc
Low Logic State	V_{IL}	Gnd	—	V_{th} −0.4	
High Logic State	V_{IH}	V_{th} +0.4	—	16.5	
Dynamic Total Loop Offset Voltage (Note 3) — Figures 3, 4 and 5	ΣV_{offset}				mV
I_{GC} = 33 μA, V_{CC} = 12 V					
T_A = 25°C		—	±2.5	±7.0	
0°C ≤ T_A ≤ +70°C		—	±3.0	±10	
I_{GC} = 33 μA, V_{CC} = 5.0 V					
T_A = 25°C		—	±4.0	±8.0	
0°C ≤ T_A ≤ +70°C		—	±4.5	±12	
Digital Output Voltage (Pin 9)					Vdc
I_{OL} = 3.6 mA	V_{OL}	—	0.1	0.4	
I_{OH} = −0.35 mA	V_{OH}	V_{CC} −1.0	V_{CC} −0.2	—	
Syllabic Filter Applied Voltage (Pin 3)	$V_{I(Syl)}$	+3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int} \rvert$				
I_{GC} = 12 μA		8.0	10	12	μA
I_{GC} = 1.5 mA		1.4	1.5	1.6	mA
I_{GC} = 3.0 mA		2.75	3.0	3.25	mA
Dynamic Integrating Current Match (Figure 6) I_{GC} = 1.5 mA	$V_{O(Ave)}$	—	±100	±300	mV
Input Current — High Logic State V_{IH} = 16.5 V	I_{IH}				μA
Digital Data Input		—	—	+5.0	
Clock Input		—	—	+5.0	
Encode/$\overline{\text{Decode}}$ Input		—	—	+5.0	
Input Current — Low Logic State V_{IL} = 0 V	I_{IL}				μA
Digital Data Input		—	—	−10	
Clock Input		—	—	−360	
Encode/$\overline{\text{Decode}}$ Input		—	—	−36	
Clock Input, V_{IL} = 0.4 V		—	—	−72	

NOTE 3. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 16 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size).

DEFINITIONS AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ on Pin 10, ground or left open.

The analog input comparator has bias currents of 2.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V–I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should typically be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and non-inverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC34115 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The coincidence output will be low whenever the content of the internal 3 bit shift register is all 1s or all 0s. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging

DEFINITIONS AND FUNCTION OF PINS (continued)

constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Typically it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

The clock input determines the data rate of the codec circuit. A 16K bit rate requires a 16 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 — Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 — V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

FIGURE 1 — POWER SUPPLY CURRENT

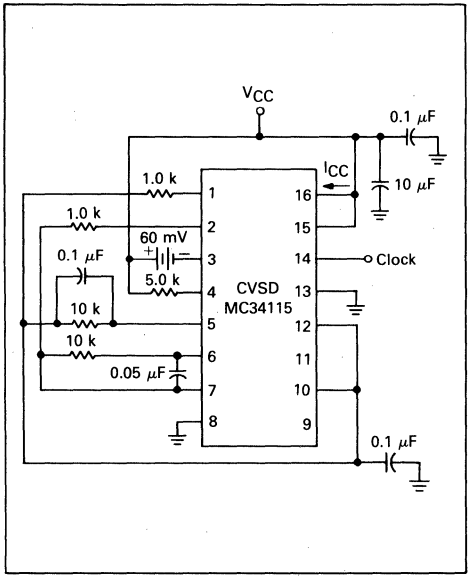
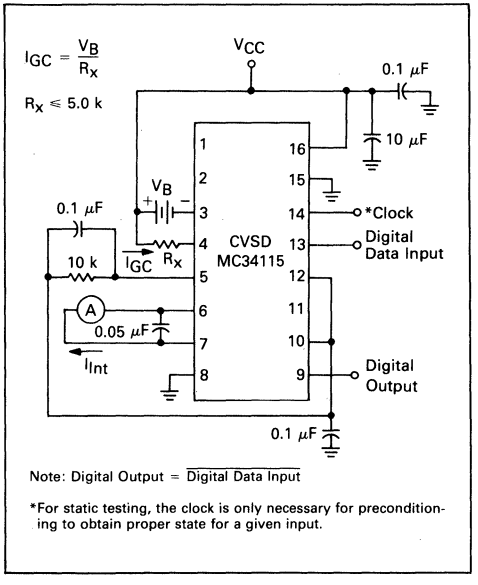


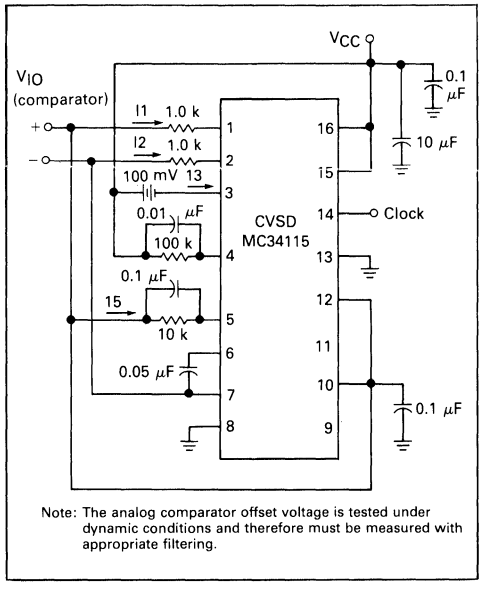
FIGURE 2 — I_{GCR}, GAIN CONTROL RANGE and I_{Int} — INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 — INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 — INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

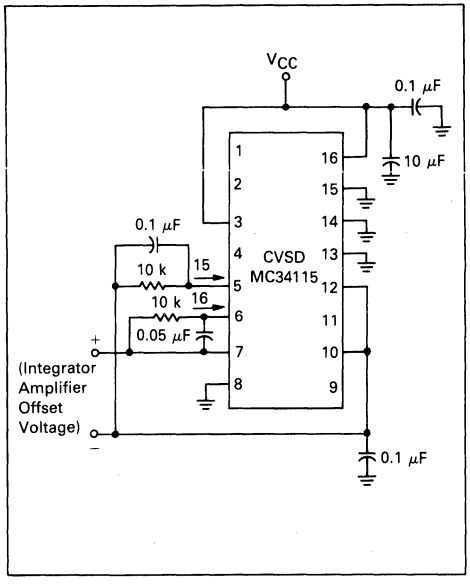
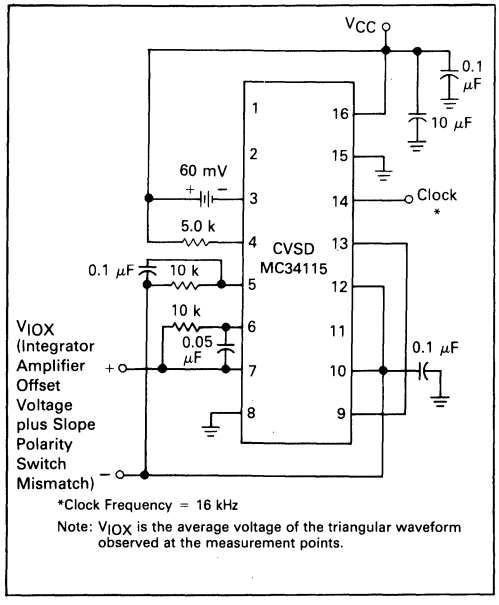


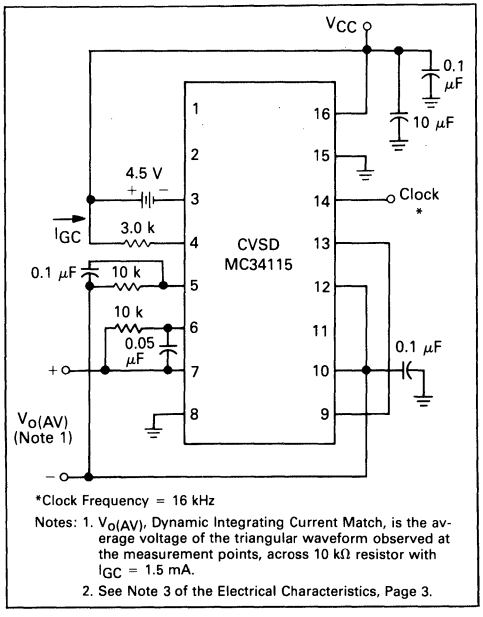
FIGURE 5 — V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



*Clock Frequency = 16 kHz

Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 — DYNAMIC INTEGRATING CURRENT MATCH



*Clock Frequency = 16 kHz

Notes: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.

2. See Note 3 of the Electrical Characteristics, Page 3.

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TYPICAL PERFORMANCE CURVES

FIGURE 7 — TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

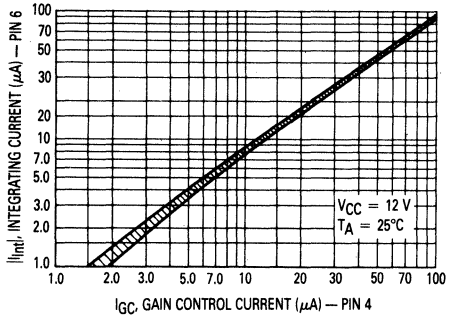


FIGURE 8 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

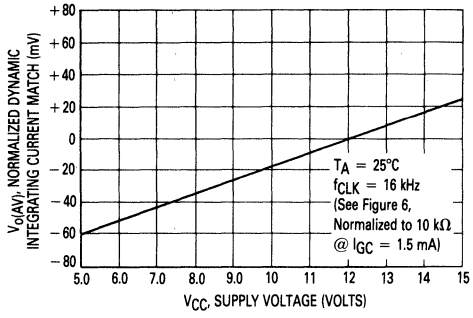


FIGURE 9 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

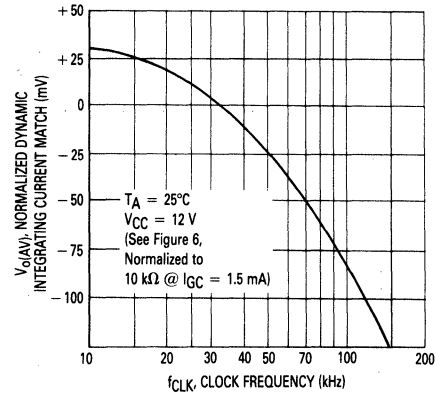


FIGURE 10 — DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

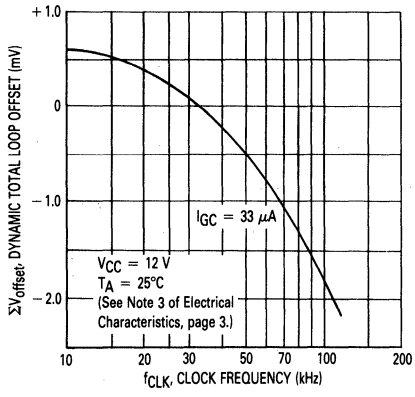


FIGURE 11 — BLOCK DIAGRAM OF THE CVSD ENCODER

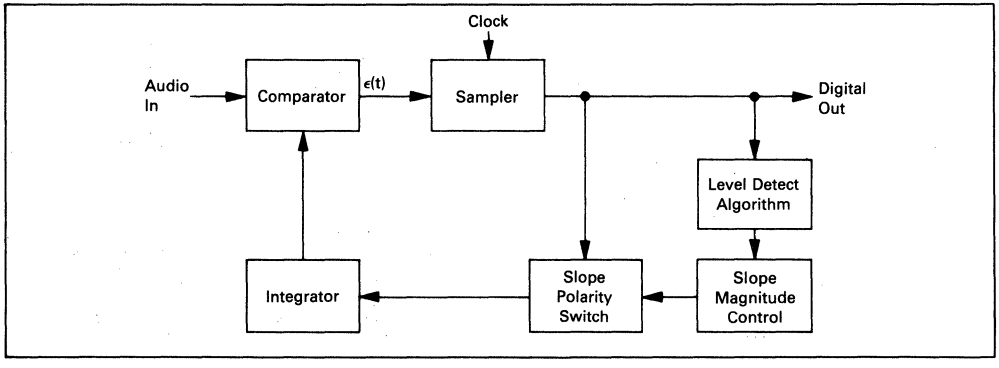


FIGURE 12 — CVSD WAVEFORMS

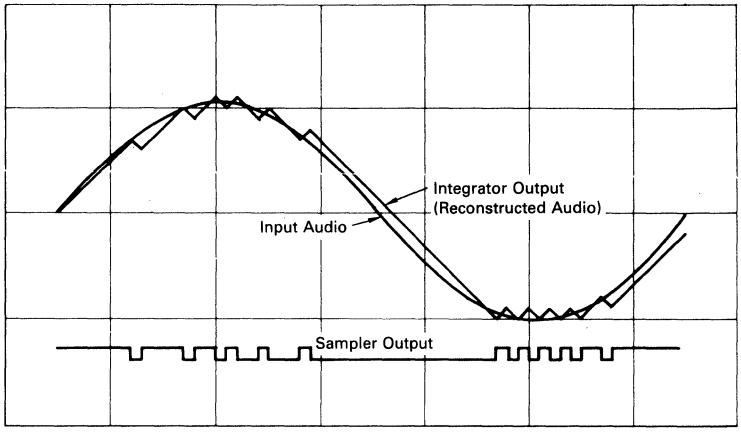
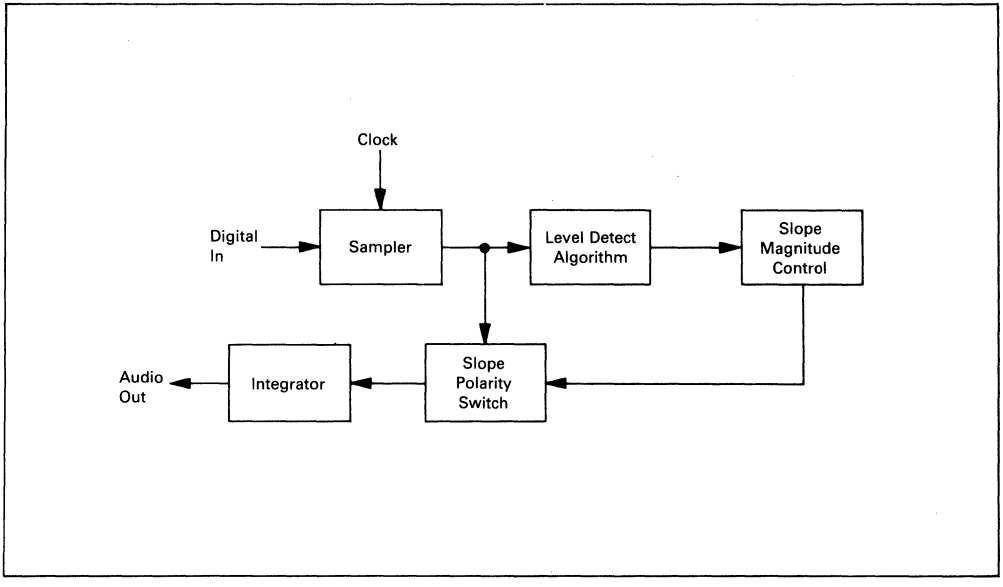


FIGURE 13 — BLOCK DIAGRAM OF THE CVSD DECODER



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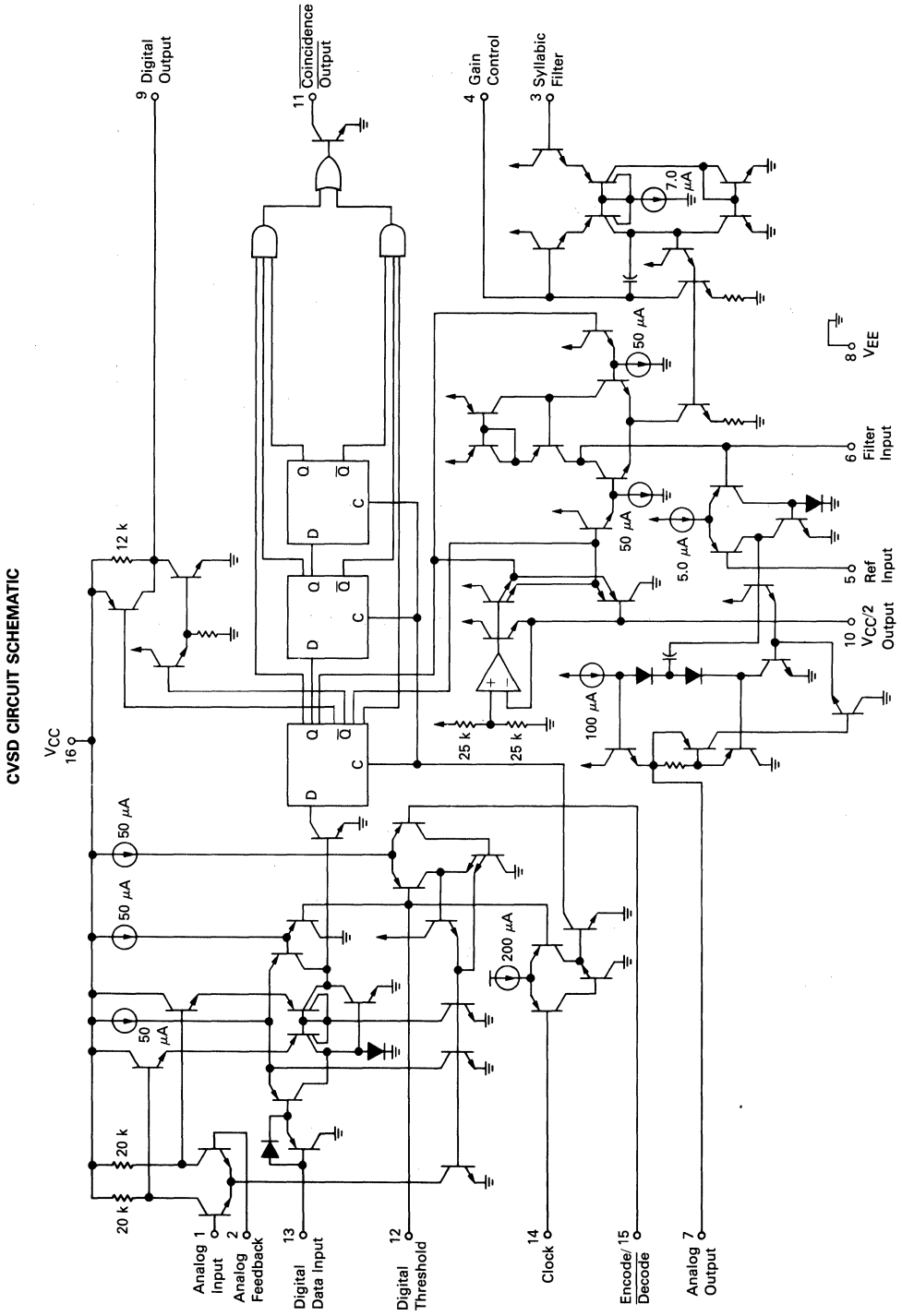
CVSD CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the intregrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

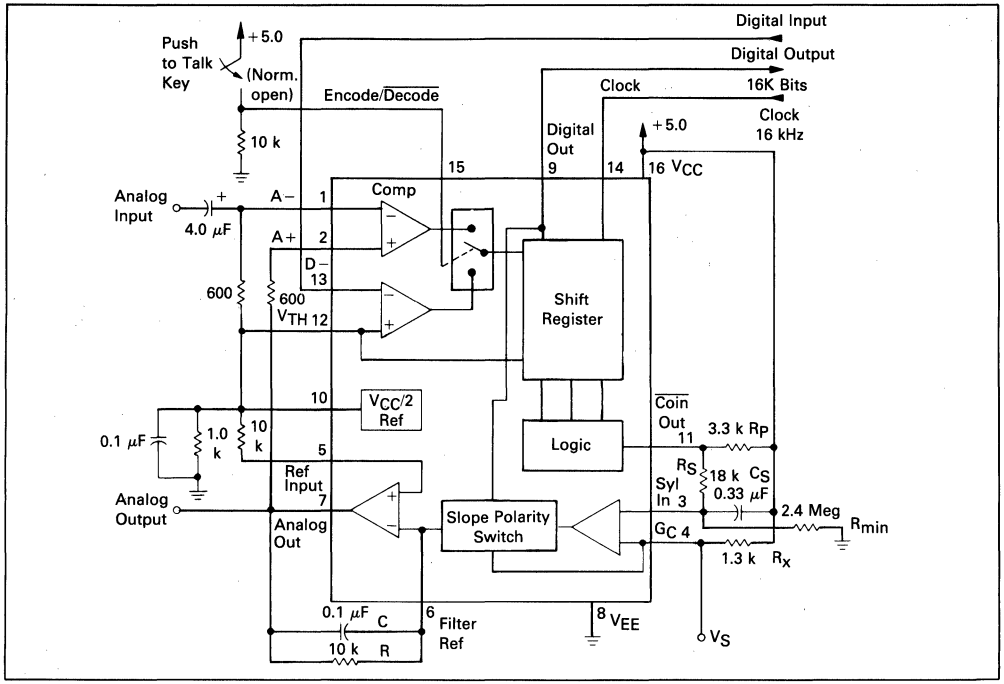
The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

2

FIGURE 14 — 16 kHz SIMPLEX VOICE CODEC
(Using MC34115, Single Pole Companding and Single Integration)



APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC34115 is shown in Figure 14. This IC is a general purpose CVSD building block which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC34115. There are six design considerations involved in designing the basic CVSD building block into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Selection of loop gain
3. Selection of minimum step size
4. Design of integration filter transfer function
5. Design of syllabic filter transfer function
6. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 4 and 5 are reduced to their simplest form. They syllabic and integration filters are both single pole networks. The selection of items 1 through 3 govern the codec performance.

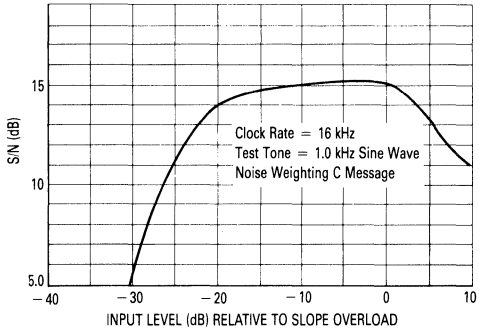
Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1–7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above.

FIGURE 15 — SIGNAL-TO-NOISE PERFORMANCE OF MC34115 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS — TYPICAL



Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_o}{i_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across R when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC34115 is tested to ensure that a 20 mVp-p mimimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

CVSD DESIGN CONSIDERATIONS (continued)

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 32\ \mu A$$

The voltage on C_S which produces a 32 μA current is determined by the value of R_X.

$I_iR_X = V_S min$; for 32 μA, $V_S min$ = 41.6 mV

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_S min \quad R_{min} \simeq 2.4\ M\Omega$$

Having established these three parameters — clock rate, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

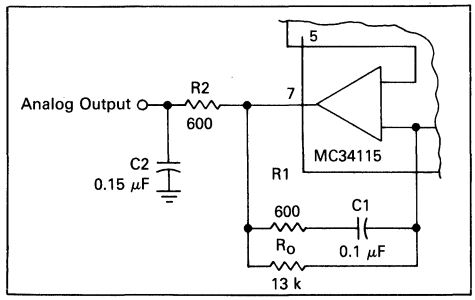
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

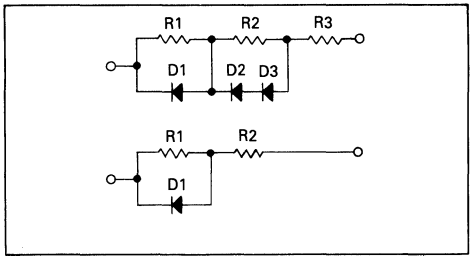
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

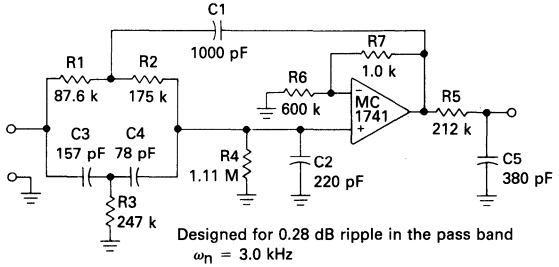
FIGURE 17 — RESISTOR-DIODE NETWORKS



Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 18 provides excellent performance for 12 kHz to 40 kHz systems.

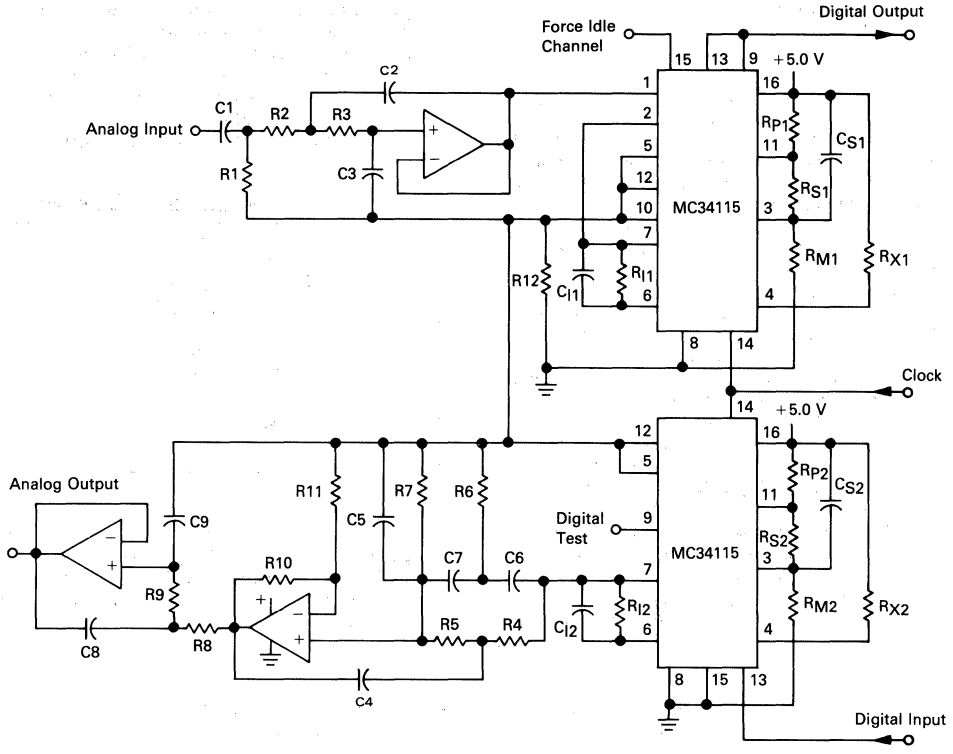
FIGURE 18 — HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT



Designed for 0.28 dB ripple in the pass band
ω_n = 3.0 kHz
ω_s = ≅ 6.0 kHz
AdB at ω_s and above 29.5 dB

2

FIGURE 19 — FULL DUPLEX/16K BIT CVSD VOICE CODEC USING MC34115 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} — 3.3 kΩ
R_{P1}, R_{P2} — 3.3 kΩ
R_{S1}, R_{S2} — 100 kΩ
R_{I1}, R_{I2} — 20 kΩ
R_{12} — 1 kΩ
R_{M1}, R_{M2} — 10 MΩ
Minimum step size = 20 mV
C_{S1}, C_{S2} — 0.05 μF
C_{I1}, C_{I2} — 0.05 μF
2 MC34115
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency — 3.3 kHz
Stop Band — 9 kHz
Stop Band Atten. — 50 dB
Rolloff — >40 dB/Octave

Filter Components

R1 — 965 Ω
R2 — 72 kΩ
R3 — 72 kΩ
R4 — 63.46 kΩ
R5 — 127 kΩ
R6 — 365.5 kΩ
R7 — 1.645 MΩ
R8 — 72 kΩ
R9 — 72 kΩ
R10 — 29.5 kΩ
R11 — 72 kΩ

C1 — 3.3 μF
C2 — 837 pF
C3 — 536 pF
C4 — 1000 pF
C5 — 222 pF
C6 — 77 pF
C7 — 38 pF
C8 — 837 pF
C9 — 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

MC34118

Specifications and Applications Information

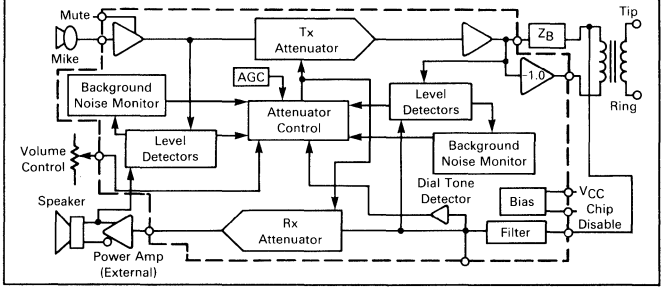
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.

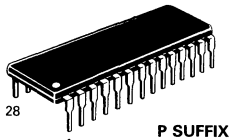
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Standard 28-Pin Plastic DIP Package and SOIC Package Available
- Compatible with MC34119 Speaker Amplifier

SIMPLIFIED BLOCK DIAGRAM

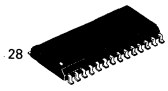


VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710-02



DW SUFFIX
PLASTIC PACKAGE
CASE 751F-03

PIN CONNECTIONS

(Top View)

FO	1	28	GND
FI	2	27	CPR
CD	3	26	RLI1
V_{CC}	4	25	RLO1
HTO+	5	24	TLO1
HTO−	6	23	TLI1
HTI	7	22	RXO
TXO	8	21	RXI
TXI	9	20	RLI2
MCO	10	19	RLO2
MCI	11	18	TLO2
MUT	12	17	TLI2
VLC	13	16	CPT
CT	14	15	V_B

(Pin assignments same for both packages)

2

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage (Pin 4)	−1.0, +7.0	Vdc
Voltage at CD (Pin 3), MUT (Pin 12)	−1.0, V_{CC} + 1.0	Vdc
Voltage at VLC (Pin 13)	−1.0, V_{CC} + 0.5	Vdc
Voltage at TXI (Pin 9), RXI (Pin 21), FI (Pin 2)	−0.5, V_{CC} + 0.5	Vdc
Storage Temperature Range	−65 to +150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Supply Voltage (Pin 4) (See Text)	3.5	—	6.5	Vdc
CD Input (Pin 3), MUT Input (Pin 12)	0	—	V_{CC}	Vdc
I_{VB} Current (Pin 15)	—	—	500	μA
VLC (Pin 13)	0.3 x V_B	—	V_B	Vdc
Attenuator Input Signal Voltage (Pins 9, 21)	0	—	350	mVrms
Microphone Amplifier, Hybrid Amplifier Gain	0	—	40	dB
Load Current @ RXO, TXO (Pins 8, 22) @ MCO (Pin 10) @ HTO−, HTO+ (Pins 6, 5)	0 0 0	— — —	±2.0 ±1.0 ±5.0	mA
Ambient Operating Temperature Range	−20	—	+60	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY					
V_{CC} Supply Current (V_{CC} = 6.5 V, CD = 0.8 V) (V_{CC} = 6.5 V, CD = 2.0 V)	I_{CC}	— —	5.5 600	8.0 800	mA μA
CD Input Resistance (V_{CC} = V_{CD} = 6.5 V) CD Input Voltage — High — Low	R_{CD} V_{CDH} V_{CDL}	50 2.0 0	90 — —	— V_{CC} 0.8	kΩ Vdc Vdc
V_B Output Voltage (V_{CC} = 3.5 V) (V_{CC} = 5.0 V)	V_B	— 1.8	1.3 2.1	— 2.4	Vdc
V_B Output Resistance (I_{VB} = 1.0 mA)	R_{OVB}	—	400	—	Ω
V_B Power Supply Rejection Ratio (C_{VB} = 220 μF, f = 1.0 kHz)	PSRR	—	54	—	dB
ATTENUATORS (T_A = +25°C)					
Receive Attenuator Gain (f = 1.0 kHz, V_{LC} = V_B) Rx Mode, RXI = 150 mVrms (V_{CC} = 5.0 V) Rx Mode, RXI = 150 mVrms (V_{CC} = 3.5 V) Gain Change − V_{CC} = 3.5 V versus V_{CC} = 5.0 V AGC Gain Change − V_{CC} = 2.8 V versus V_{CC} = 5.0 V* Idle Mode, RXI = 150 mVrms Range (Rx to Tx Mode)	 G_{RX} G_{RX} ΔG_{RX1} ΔG_{RX2} G_{RXI} ΔG_{RX3}	 +4.0 +4.0 −0.5 — −22 49	 +6.0 +6.0 0 −25 −20 52	 +8.0 +8.0 +0.5 −15 −17 54	dB
Volume Control Range (Rx Mode, 0.3 V_B < V_{LC} < V_B)	V_{CR}	27	35	—	dB
RXO DC Voltage (Rx Mode)	V_{RXO}	—	V_B	—	Vdc
ΔRXO DC Voltage (Rx to Tx Mode)	ΔV_{RXO}	—	±10	±150	mV
RXO High Voltage (I_{out} = −1.0 mA RXI = V_B + 1.5 V)	V_{RXOH}	3.7	—	—	Vdc
RXO Low Voltage (I_{out} = +1.0 mA, RXI = V_B − 1.0, Output measured with respect to V_B)*	V_{RXOL}	—	−1.5	−1.0	Vdc
RXI Input Resistance (RXI < 350 mVrms)	R_{RXI}	7.0	10	14	kΩ

(continued)

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
ATTENUATORS — continued (T_A = +25°C)					
Transmit Attenuator Gain (f = 1.0 kHz) Tx Mode, TXI = 150 mVrms Idle Mode, TXI = 150 mVrms Range (Tx to Rx Mode)	 G_{TX} G_{TXI} ΔG_{TXI}	 +4.0 −22 49	 +6.0 −20 52	 +8.0 −17 54	dB
TXO DC Voltage (Tx Mode)	V_{TXO}	—	V_B	—	Vdc
ΔTXO DC Voltage (Tx to Rx Mode)	ΔV_{TXO}	—	±30	±150	mV
TXO High Voltage (I_{out} = −1.0 mA TXI = V_B + 1.5 V)	V_{TXOH}	3.7	—	—	Vdc
TXO Low Voltage (I_{out} = +1.0 mA, TXI = V_B − 1.0 V, Output measured with respect to V_B)*	V_{TXOL}	—	−1.5	−1.0	Vdc
TXI Input Resistance (TXI < 350 mVrms)	R_{TXI}	7.0	10	14	kΩ
Gain Tracking (G_{RX} + G_{TX}, @ Tx, Idle, Rx)*	G_{TR}	—	±0.1	—	dB

*See text for explanation.

ATTENUATOR CONTROL (T_A = +25°C)

C_T Voltage (Pin 14 − V_B) Rx Mode (V_{LC} = V_B) Idle Mode Tx Mode	V_{CT}	 — — —	 +240 0 −240	 — — —	mV
C_T Source Current (switching to Rx mode)	I_{CTR}	−85	−60	−40	μA
C_T Sink Current (switching to Tx mode)	I_{CTT}	+40	+60	+85	μA
C_T Slow Idle Current	I_{CTS}	—	0	—	μA
C_T Fast Idle Internal Resistance	R_{FI}	1.5	2.0	3.6	kΩ
V_{LC} Input Current	I_{VLC}	—	−60	—	nA
Dial Tone Detector Threshold	V_{DT}	10	15	20	mV

MICROPHONE AMPLIFIER (T_A = +25°C, V_{MUT} ≤ 0.8 V, A_{VCL} = 31 dB unless otherwise noted)

Ouptut Offset (V_{MCO} − V_B, Feedback R = 180 kΩ)	MCO_{VOS}	−50	0	+50	mVdc
Open Loop Gain (f < 100 Hz)	A_{VOLM}	70	80	—	dB
Gain Bandwidth	GBW_M	—	1.0	—	MHz
Output High Voltage (I_{out} = −1.0 mA, V_{CC} = 5.0 V)	V_{MCOH}	3.7	—	—	Vdc
Output Low Voltage (I_{out} = +1.0 mA)	V_{MCOL}	—	—	200	mVdc
Input Bias Current (@ MCI)	I_{BM}	—	−40	—	nA
Muting (ΔGain) (f = 1.0 kHz, V_{MUT} = 2.0 V) (300 Hz < f < 10 kHz)	GMT	−55 —	— −68	— —	dB
MUT Input Resistance (V_{CC} = V_{MUT} = 6.5 V)	R_{MUT}	50	90	—	kΩ
MUT Input — High	V_{MUTH}	2.0	—	V_{CC}	Vdc
MUT Input — Low	V_{MUTL}	0	—	0.8	Vdc
Distortion (300 Hz < f < 10 kHz)	THD_M	—	0.15	—	%

HYBRID AMPLIFIERS (T_A = +25°C)

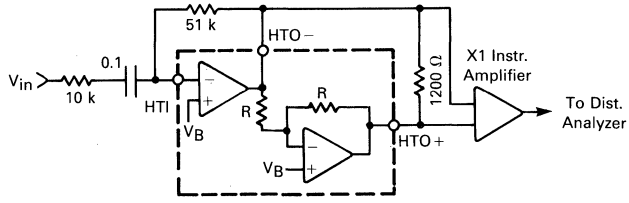
HTO− Offset (V_{HTO-} − V_B, Feedback R = 51 kΩ)	H_{VOS}	−20	0	+20	mVdc
HTO− to HTO+ Offset (Feedback R = 51 kΩ)	HB_{VOS}	−30	0	+30	mVdc
Open Loop Gain (HTI to HTO−, f < 100 Hz)	A_{VOLH}	60	80	—	dB
Gain Bandwidth	GBW_H	—	1.0	—	MHz
Closed Loop Gain (HTO− to HTO+)	A_{VCLH}	−0.35	0	+0.35	dB
Input Bias Current (@HTI)	I_{BH}	—	−30	—	nA
HTO− High Voltage (I_{out} = −5.0 mA)	V_{HT-H}	3.7	—	—	Vdc
HTO− Low Voltage (I_{out} = +5.0 mA)	V_{HT-L}	—	—	250	mVdc
HTO+ High Voltage (I_{out} = −5.0 mA)	V_{HT+H}	3.7	—	—	Vdc
HTO+ Low Voltage (I_{out} = +5.0 mA)	V_{HT+L}	—	—	450	mVdc
Distortion (300 Hz < f < 10 kHz, See Figure 1)	THD_H	—	0.3	—	%

2

Parameter	Symbol	Min	Typ	Max	Units
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS (T_A = +25°C)					
Transmit-Receive Switching Threshold (Ratio of Current at RLI1 + RLI2 to 20 μA at TLI1 + TLI2 to switch from Tx to Rx)	I_{TH}	0.8	1.0	1.2	
Source Current at RLO1, RLO2, TLO1, TLO2	I_{LSO}	—	−2.0	—	mA
Slnk Current at RLO1, RLO2, TLO1, TLO2	I_{LSK}	—	4.0	—	μA
CPR, CPT Output Resistance (I_{out} = 1.5 mA)	R_{CP}	—	35	—	Ω
CPR, CPT Leakage Current	I_{CPLK}	—	−0.2	—	μA
FILTER (T_A = +25°C)					
Voltage Offset at FO (V_{FO} − V_B, 220 kΩ from V_B to FI)	FO_{VOS}	−200	−90	0	mV
FO Sink Current	I_{FO}	150	260	400	μA
FI Bias Current	I_{FI}	—	−50	—	nA
SYSTEM DISTORTION (T_A = +25°C, f = 1.0 kHz)					
Rx Mode (From FI to RXO, FO connected to RXI)	THD_R	—	0.5	3.0	%
Tx Mode (From MCI to HTO−/HTO+, includes Tx attenuator)	THD_T	—	0.8	3.0	%

1. All currents into a device pin are positive, those out of a pin are negative. Algebraic convention rather than magnitude is used to define limits.

FIGURE 1 — HYBRID AMPLIFIER DISTORTION TEST



TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change −20 to +60°C
V_{CC} Supply Current (CD = 0.8 V)	5.0 mA	−0.3 %/°C
V_{CC} Supply Current (CD = 2.0 V)	400 μA	−0.4 %/°C
V_B Output Voltage (V_{CC} = 5.0 V)	2.1 V	+0.8 %/°C
Attenuator Gain (Max Gain)	+6.0 dB	0.0008 dB/°C
Attenuator Gain (Max Attenuation)	−46 dB	0.004 dB/°C
Attenuator Input Resistance (@ TXI, RXI)	10 kΩ	+0.6 %/°C
Dial Tone Detector Threshold	15 mV	+20 μV/°C
CT Source, Sink Current	±60 μA	−0.15 %/°C
Microphone, Hybrid Amplifier Offset	0 mV	±4.0 μV/°C
Transmit-Receive Switching Threshold	1.0	±0.02 %/°C
Sink Current at RLO1, RLO2, TLO1, TLO2	4.0 μA	−10 nA/°C
Closed Loop Gain (HTO− to HTO+)	0 dB	0.001 %/°C

PIN DESCRIPTION

Pin	Name	Description
1	FO	Filter output. Output impedance is less than 50 ohms.
2	FI	Filter input. Input impedance is greater than 1.0 Mohm.
3	CD	Chip Disable. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) disables the IC to conserve power. Input impedance is nominally 90 kΩ.
4	V_{CC}	A supply voltage of +2.8 to +6.5 volts is required, at ≈ 5.0 mA. As V_{CC} falls from 3.5 to 2.8 volts, an AGC circuit reduces the receive attenuator gain by ≈ 25 dB (when in the receive mode).
5	HTO+	Output of the second hybrid amplifier. The gain is internally set at −1.0 to provide a differential output, in conjunction with HTO−, to the hybrid transformer.
6	HTO−	Output of the first hybrid amplifier. The gain of the amp is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is ≈V_B.
8	TXO	Output of the transmit attenuator. DC level is approximately V_B.
9	TXI	Input to the transmit attenuator. Max. signal level is 350 mVrms. Input impedance is ≈10 kΩ.
10	MCO	Output of the microphone amplifier. The gain of the amplifier is set by external resistors.
11	MCI	Input and summing node of the microphone amplifier. DC level is ≈ V_B.
12	MUT	Mute input. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90 kΩ.
13	VLC	Volume control input. When VLC = V_B, the receive attenuator is at maximum gain when in the receive mode. When VLC = 0.3 V_B, the receive gain is down 35 dB. Does not affect the transmit mode.
14	C_T	An RC at this pin sets the response time for the circuit to switch modes.
15	V_B	An output voltage ≈V_{CC}/2. This voltage is a system ac ground, and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Input to the transmit level detector on the mike/speaker side.
18	TLO2	Output of the transmit level detector on the mike/speaker side, and input to the transmit background monitor.
19	RLO2	Output of the receive level detector on the mike/speaker side.
20	RLI2	Input to the receive level detector on the mike/speaker side.
21	RXI	Input to the receive attenuator and dial tone detector. Max input level is 350 mV RMS. Input impedance is ≈10 kΩ.
22	RXO	Output of the receive attenuator. DC level is approximately V_B.
23	TLI1	Input to the transmit level detector on the line side.
24	TLO1	Output of the transmit level detector on the line side.
25	RLO1	Output of the receive level detector on the line side, and input to the receive background monitor.
26	RLI1	Input to the receive level detector on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground pin for the entire IC.

Note: Pin numbers are identical for the DIP package and the SOIC package.

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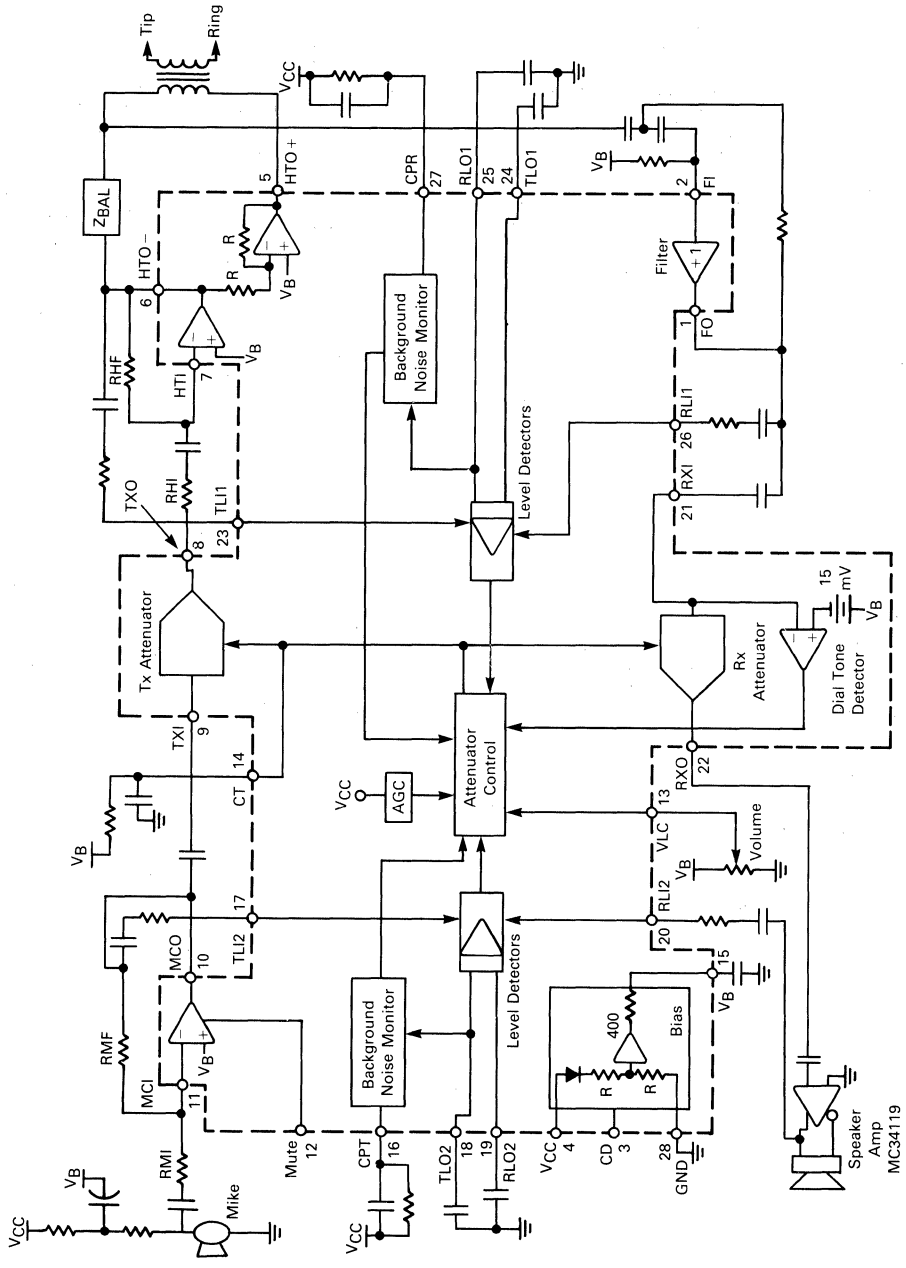


FIGURE 2 — MC34118 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

INTRODUCTION

The fundamental difference between the operation of a speakerphone and a handset is that of half-duplex versus full-duplex. The handset is full duplex since conversation can occur in both directions (transmit and receive) simultaneously. A speakerphone has higher gain levels in both paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the system. The loop is formed by the receive and transmit paths, the hybrid, and the acoustic coupling (speaker to microphone). The only practical and economical solution used to date is to design the speakerphone to function in a half duplex mode — i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking, switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands-free" mode, eliminating the need for a "push-to-talk" switch.

The handset, by the way, has the same loop as the speakerphone. But since the gains are considerably lower, and since the acoustic coupling from the earpiece to the mouthpiece is almost non-existent (the receiver is normally held against a person's ear), oscillations don't occur.

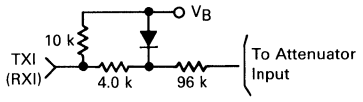
The MC34118 provides the necessary level detectors, attenuators, and switching control for a properly operating speakerphone. The detection sensitivity and timing are externally controllable. Additionally, the MC34118 provides background noise monitors which make the circuit insensitive to room and line noise, hybrid amplifiers for interfacing to Tip and Ring, the microphone amplifier, and other associated functions. Please refer to the Block Diagram (Figure 2) when reading the following sections.

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain (+6.0 dB), the other is at maximum attenuation (−46 dB), and vice versa. They are never both fully on or both fully off. The sum of their gains remains constant (within a nominal error band of ±0.1 dB) at a typical value of −40 dB (see Figure 10). Their purpose is to control the transmit and receive paths to provide the half-duplex operation required in a speakerphone.

The attenuators are non-inverting, and have a −3.0 dB (from max gain) frequency of ≈100 kHz. The input impedance of each attenuator (TXI and RXI) is nominally 10 kΩ (see Figure 3), and the input signal should be limited to 350 mVrms (990 mVp-p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. The diode clamp on the inputs limits the input swing, and therefore the maximum negative output swing. This is the reason for V_{RXOL} and V_{TXOL} specification being defined as they are in the Electrical Characteristics. The output impedance is <10 Ω until the output current limit (typically 2.5 mA) is reached.

FIGURE 3 — ATTENUATOR INPUT STAGE



The attenuators are controlled by the single output of the Control Block, which is measurable at the C_T pin (Pin 14). When the C_T pin is at +240 millivolts with respect to V_B, the circuit is in the receive mode (receive attenuator is at +6.0 dB). When the C_T pin is at −240 millivolts with respect to V_B, the circuit is in the transmit mode (transmit attenuator is at +6.0 dB). The circuit is in an idle mode when the C_T voltage is equal to V_B, causing the attenuators' gains to be halfway between their fully on and fully off positions (−20 dB each). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode.

The inputs to the Control Block are seven: 2 from the comparators operated by the level detectors, 2 from the background noise monitors, the volume control, the dial-tone detector, and the AGC circuit. These seven inputs are described below.

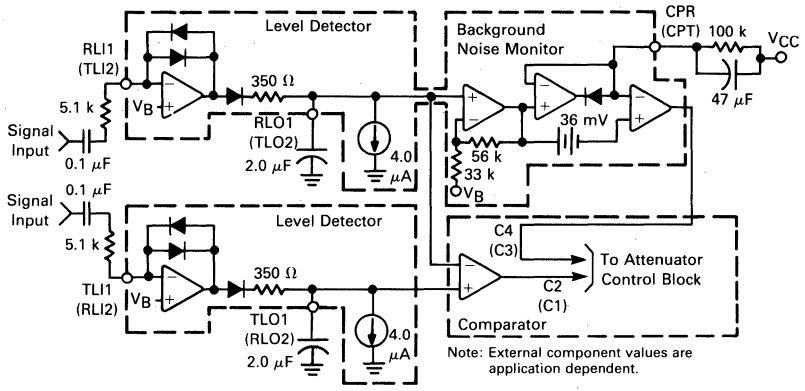
LEVEL DETECTORS

There are four level detectors — two on the receive side and two on the transmit side. Refer to Figure 4 — the terms in parentheses form one system, and the other terms form the second system. Each level detector is a high gain amplifier with back-to-back diodes in the feedback path, resulting in non-linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 11, 12 and 13 for their dc and ac transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at each input (TLI1, TLI2, RLI1, and RLI2). Each output charges an external capacitor through a diode and limiting resistor, thus providing a dc representation of the input ac signal level. The outputs have a quick rise time (determined by the capacitor and an internal 350 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the four outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 2, on the receive side, one level detector (RLI1) is at the receive input receiving the same

2

FIGURE 4 — LEVEL DETECTORS



signal as at Tip and Ring, and the other (RLI2) is at the output of the speaker amplifier. On the transmit side, one level detector (TLI2) is at the output of the microphone amplifier, while the other (TLI1) is at the hybrid output. Outputs RLO1 and TLO1 feed a comparator, the output of which goes to the Attenuator Control Block. Likewise, outputs RLO2 and TLO2 feed a second comparator which also goes to the Attenuator Control Block. The truth table for the effects of the level detectors on the Control Block is given in the section describing the Control Block.

BACKGROUND NOISE MONITORS

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background noise monitors — one for the receive path and one for the transmit path. Referring to Figure 4, the receive background noise monitor is operated on by the RLI1-RLO1 level detector, while the transmit background noise monitor is operated on by the TLI2-TLO2 level detector. They monitor the background noise by storing a dc voltage representative of the respective noise levels in capacitors at CPR and CPT. The voltages at these pins have slow rise times (determined by the external RC), but fast decay times. If the signal at RLI1 (or TLI2) changes slowly, the voltage at CPR (or CPT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage on the non-inverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the Attenuator Control Block.

The 36 mV offset at the comparator's input keeps the comparator from changing state unless the speech level exceeds the background noise by ≈4.0 dB. The time constant of the external RC (≈4.7 seconds) determines the response time to background noise variations.

VOLUME CONTROL

The volume control input at VLC (Pin 13) is sensed as a voltage with respect to V_B. The volume control affects the attenuators *only* in the receive mode. It has no effect in the idle or transmit modes.

When in the receive mode, the gain of the receive attenuator will be +6.0 dB, and the gain of the transmit attenuator will be −46 dB only when VLC is equal to V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced (see Figure 14), and the gain of the transmit attenuator is increased such that their sum remains constant. Changing the voltage at VLC changes the voltage at C_T (see the Attenuator Control Block section), which in turn controls the attenuators.

The volume control setting does not affect the maximum attenuator input signal at which noticeable distortion occurs.

The bias current at VLC is typically 60 nA out of the pin, and does not vary significantly with the VLC voltage or with V_{CC}.

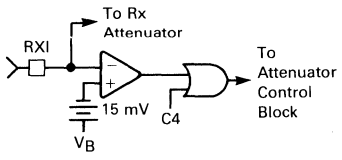
DIAL TONE DETECTOR

The dial tone detector is a comparator with one side connected to the receive input (RXI) and the other input connected to V_B with a 15 mV offset (see Figure 5). If the circuit is in the receive mode, and the incoming signal is greater than 15 mV (10 mVrms), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined solely by the volume control.

The purpose of this circuit is to prevent the dial tone

(which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to the idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

FIGURE 5 — DIAL TONE DETECTOR



AGC

The AGC circuit affects the circuit only in the receive mode, and only when the supply voltage (V_{CC}) is less than 3.5 volts. As V_{CC} falls below 3.5 volts, the gain of the receive attenuator is reduced according to the graph of Figure 15. The transmit path attenuation changes such that the sum of the transmit and receive gains remains constant.

The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long line, where the available power is limited. By reducing the speaker power, the voltage sag at V_{CC} is controlled, preventing possible erratic operation.

ATTENUATOR CONTROL BLOCK

The Attenuator Control Block has the seven inputs described above:

- The output of the comparator operated by RLO2 and TLO2 (microphone/speaker side) — designated C1.
- The output of the comparator operated by RLO1 and TLO1 (Tip/Ring side) — designated C2.
- The output of the transmit background noise monitor — designated C3.
- The output of the receive background noise monitor — designated C4.
- The volume control.
- The dial tone detector.
- The AGC circuit.

The single output of the Control Block controls the two attenuators. The effect of C1–C4 is as follows:

Inputs				Output
C1	C2	C3	C4	Mode
Tx	Tx	1	X	Transmit
Tx	Rx	y	y	Fast Idle
Rx	Tx	y	y	Fast Idle
Rx	Rx	X	1	Receive
Tx	Tx	0	X	Slow Idle
Tx	Rx	0	0	Slow Idle
Rx	Tx	0	0	Slow Idle
Rx	Rx	X	0	Slow Idle

X = Don't Care; y = C3 and C4 are not both 0.

A definition of the above terms:

1) "Transmit" means the transmit attenuator is fully on (+6.0 dB), and the receive attenuator is at max. attenuation (−46 dB).
2) "Receive" means both attenuators are controlled by the volume control. At max. volume, the receive attenuator is fully on (+6.0 dB), and the transmit attenuator is at max. attenuation (−46 dB).
3) "Fast Idle" means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to idle until one speech level dominates the other.
4) "Slow Idle" means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1 second) to the idle mode.
5) Switching to the full transmit or receive modes from any other mode is at the fast rate (≈30 ms).

A summary of the truth table is as follows:

1) The circuit will switch to transmit if: a) *both* transmit level detectors sense higher signal levels relative to the respective receive level detectors (TLI1 versus RLI1, TLI2 versus RLI2), *and* b) the transmit background noise monitor indicates the presence of speech.

2) The circuit will switch to receive if: a) *both* receive level detectors sense higher signal levels relative to the respective transmit level detectors, *and* b) the receive background noise monitor indicates the presence of speech.

3) The circuit will switch to the fast idle mode if the level detectors *disagree* on the relative strengths of the signal levels, *and* at least one of the background noise monitors indicates speech. For example, referring to the Block Diagram (Figure 2), if there is sufficient signal at the microphone amp output (TLI2) to override the speaker signal (RLI2), *and* there is sufficient signal at the receive input (RLI1) to override the signal at the hybrid output (TLI1), *and* either or both background monitors indicate speech, then the circuit will be in the fast idle mode. Two conditions which can cause the fast idle mode to occur are a) when both talkers are attempting to gain control of the system by talking at the same time, and b) when one talker is in a very noisy environment, forcing the other talker to continually override that noise level. In general, the fast idle mode will occur infrequently.

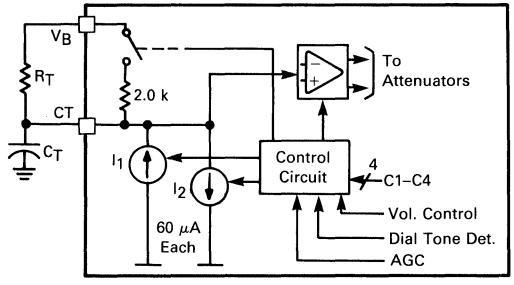
4) The circuit will switch to the slow idle mode when a) both talkers are quiet (no speech present), or b) when one talker's speech level is continuously overriden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive, fast idle and slow idle is determined in part by the components at the C_T pin (Pin 14). (See the section on Switching Times for a more complete explanation of the switching time components.) A schematic of the C_T circuitry is shown in Figure 6, and operates as follows:

- R_T is typically 120 kΩ, and C_T is typically 5.0 μF.
- To switch to the receive mode, I_1 is turned on (I_2 is off), charging the external capacitor to +240 mV above V_B. (An internal clamp prevents further charging of the capacitor.)
- To switch to the transmit mode, I_2 is turned on (I_1 is off) bringing down the voltage on the capacitor to −240 mV with respect to V_B.

— To switch to idle quickly (fast idle), the current sources are turned off, and the internal 2.0 kΩ resistor is switched in, discharging the capacitor to V_B with a time constant = 2.0 k x C_T.
— To switch to idle slowly (slow idle), the current sources are turned off, the switch at the 2.0 kΩ resistor is open, and the capacitor discharges to V_B through the external resistor R_T with a time constant = R_T x C_T.

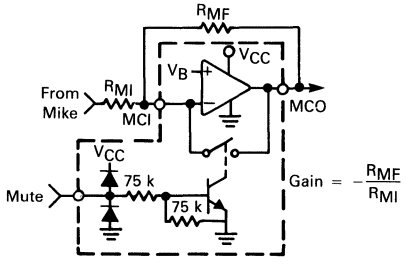
FIGURE 6 — CT ATTENUATOR CONTROL BLOCK CIRCUIT



MICROPHONE AMPLIFIER

The microphone amplifier (Pins 10, 11) has the non-inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op-amps, the amplifier has an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain-bandwidth is typically 1.0 MHz (See Figure 16). The maximum p-p output swing is typically 1.0 volt less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 1.5 mA). Input bias current at MCI is typically 40 nA out of the pin.

FIGURE 7 — MICROPHONE AMPLIFIER AND MUTE



The muting function (Pin 12), when activated, will reduce the gain of the amplifier to ≈ −39 dB (with RMI = 5.1 kΩ) by shorting the output to the inverting input (see Figure 7). The mute input has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If the mute function is not used, the pin should be grounded.

HYBRID AMPLIFIERS

The two hybrid amplifiers (at HTO +, HTO −, and HTI), in conjunction with an external transformer, provide the two-to-four wire converter for interfacing to the telephone line. The gain of the first amplifier (HTI to HTO −) is set by external resistors (gain = $-R_{HF}/R_{HI}$ in Figure 2), and its output drives the second amplifier, the gain of which is internally set at −1.0. Unlike most op-amps, the amplifiers have an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain of the first amplifier is typically 80 dB, and the gain bandwidth of each amplifier is ≈1.0 MHz (see Figure 16). The maximum p-p output swing of each amplifier is typically 1.2 volts less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 8.0 mA). The output current capability is guaranteed to be a minimum of 5.0 mA. The bias current at HTI is typically 30 nA out of the pin.

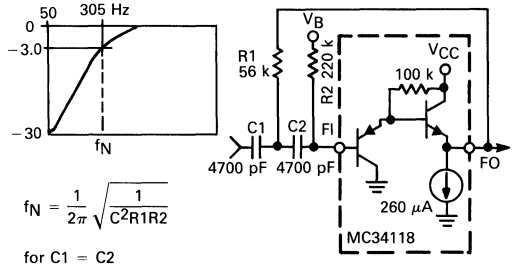
The connections to the coupling transformer are shown in the Block Diagram (Figure 2). The block labeled ZBal is the balancing network necessary to match the line impedance.

FILTER

The operation of the filter circuit is determined by the external components. The circuit within the MC34118, from pins FI to FO is a buffer with a high input impedance (>1.0 MΩ), and a low output impedance (<50 Ω). The configuration of the external components determines whether the circuit is a high-pass filter (as shown in Figure 2), a low-pass filter, or a band-pass filter.

As a high pass filter, with the components shown in Figure 8, the filter will keep out 60 Hz (and 120 Hz) hum which can be picked up by the external telephone lines.

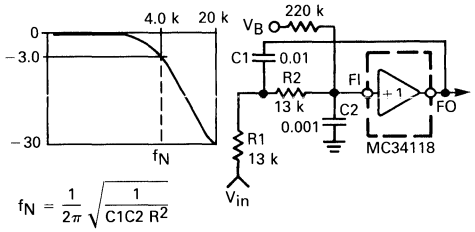
FIGURE 8 — HIGH PASS FILTER



As a low pass filter (Figure 9), it can be used to roll off the high end frequencies in the receive circuit, which aids in protecting against acoustic feedback problems.

With an appropriate choice of an input coupling capacitor to the low pass filter, a band pass filter is formed.

FIGURE 9 — LOW PASS FILTER



$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C1C2R^2}}$$

for R1 = R2

POWER SUPPLY, V_B, AND CHIP DISABLE

The power supply voltage at V_{CC} (Pin 4) is to be between 3.5 and 6.5 volts for normal operation, with reduced operation possible down to 2.8 volts (see Figure 15 and the AGC section). The power supply current is shown in Figure 18 for both the power-up and power-down mode.

The output voltage at V_B (Pin 15) is $\approx(V_{CC} - 0.7)/2$, and provides the ac ground for the system. The output impedance at V_B is ≈400 Ω (see Figure 19), and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply rejection. Figure 20 indicates the amount of rejection with different capacitors. The choice of capacitor is application dependent based on whether the circuit is powered by the telephone line or a power supply.

Since V_B biases the microphone and hybrid amplifiers, the amount of supply rejection at their outputs is directly related to the rejection at V_B, as well as their respective gains. Figure 21 depicts this graphically.

The Chip Disable (Pin 3) permits powering down the IC to conserve power and/or for muting purposes. With CD ≤0.8 volts, normal operation is in effect. With CD ≥2.0 volts and ≤V_{CC}, the IC is powered down. In the powered down mode, the microphone and the hybrid amplifiers are disabled, and their outputs go to a high impedance state. Additionally, the bias is removed from the level detectors. The bias is not removed from the filter (Pins 1, 2), the attenuators (Pins 8, 9, 21, 22), or from Pins 13, 14, and 15 (the attenuators are disabled, however, and will not pass a signal). The input impedance at CD is typically 90 kΩ, has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If CD is not used, the pin should be grounded.

FIGURE 10 — ATTENUATOR GAIN versus V_{CT} (PIN 14)

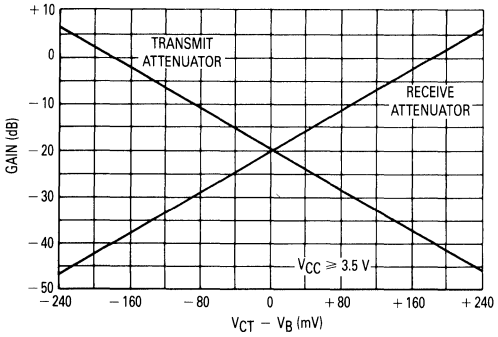


FIGURE 11 — LEVEL DETECTOR DC TRANSFER CHARACTERISTICS

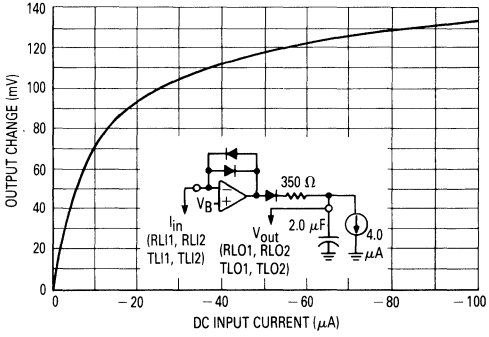


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FIGURE 12 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS

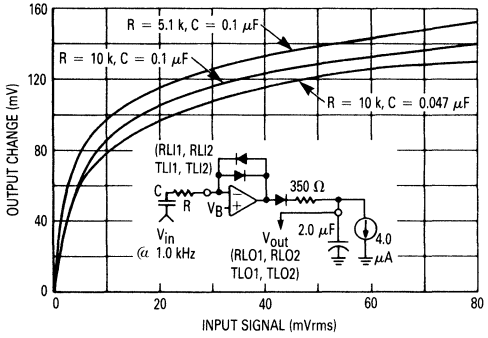


FIGURE 13 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS versus FREQUENCY

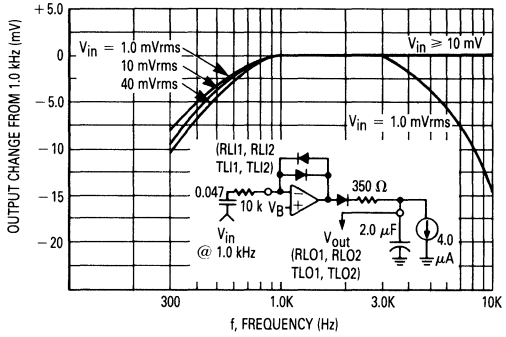


FIGURE 14 — RECEIVE ATTENUATOR versus VOLUME CONTROL

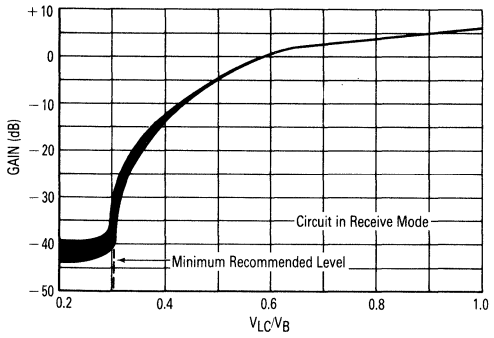


FIGURE 15 — RECEIVE ATTENUATION GAIN versus V_{CC}

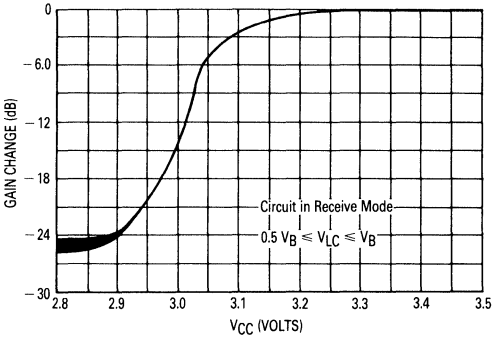


FIGURE 16 — MICROPHONE AMPLIFIER AND 1ST HYBRID AMPLIFIER OPEN LOOP GAIN AND PHASE

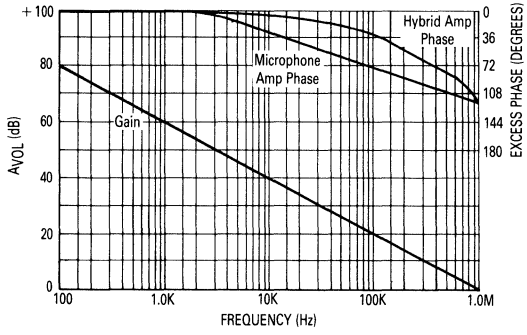


FIGURE 17 — INPUT CHARACTERISTICS @ CD, MUT

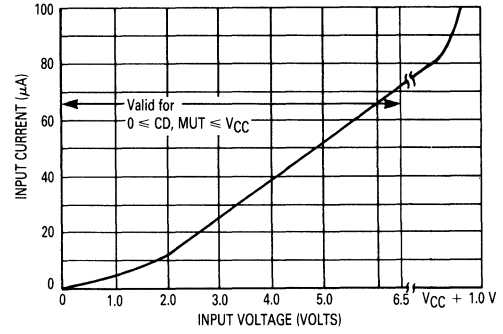


FIGURE 18 — SUPPLY CURRENT versus SUPPLY VOLTAGE

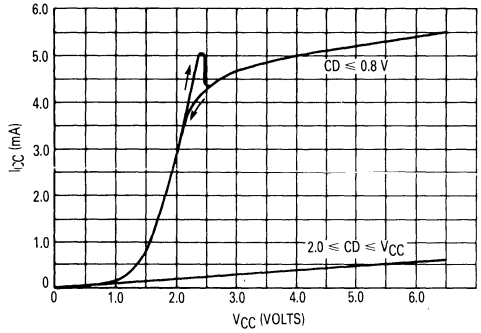


FIGURE 19 — V_B OUTPUT CHARACTERISTICS

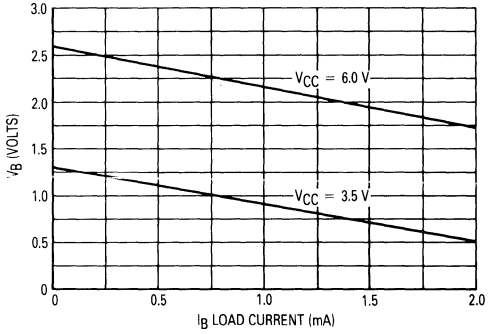


FIGURE 20 — V_B POWER SUPPLY REJECTION versus FREQUENCY AND V_B CAPACITOR

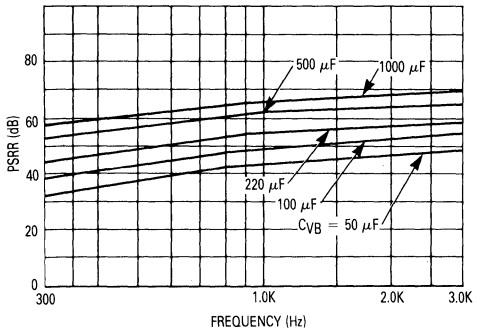


FIGURE 21 — POWER SUPPLY REJECTION OF THE MICROPHONE AND HYBRID AMPLIFIERS

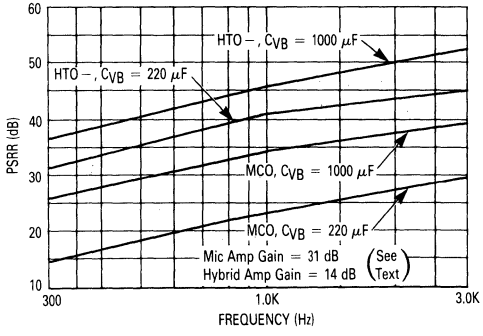
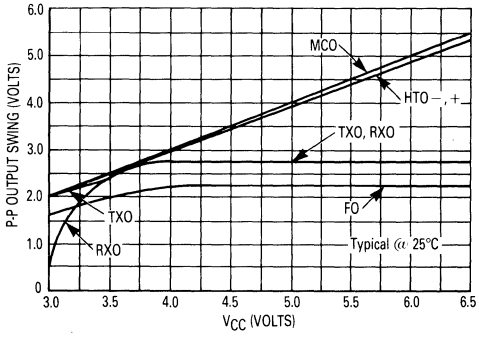


FIGURE 22 — TYPICAL OUTPUT SWING versus V_{CC}



DESIGN GUIDELINES

SWITCHING TIME

The switching time of the MC34118 circuit is dominated by the components at C_T (Pin 14, refer to Figure 6), and secondarily by the capacitors at the level detector outputs (RLO1, RLO2, TLO1, TLO2).

The time to switch to receive or to transmit from idle is determined by the capacitor at C_T, together with the internal current sources (refer to Figure 6). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

For the typical case where ΔV = 240 mV, I = 60 μA, and C_T is 5.0 μF, ΔT = 20 ms. If the circuit switches directly from receive to transmit (or vice-versa), the total switching time would be 40 ms.

The switching time from either receive or transmit to idle depends on which type of idle mode is in effect. If the circuit is going to "fast idle," the time constant is determined by the C_T capacitor, and the internal 2.0 kΩ resistor (Figure 6). With C_T = 5.0 μF, the time constant is $\approx$10 ms, giving a switching time to idle of $\approx$30 ms (for 95% change). Fast idle is an infrequent occurrence, however, occurring when both speakers are talking and competing for control of the circuit. The switching time from idle back to either transmit or receive is described above.

If the circuit is switching to "slow idle," the time constant is determined by the C_T capacitor and R_T, the external resistor (see Figure 6). With C_T = 5.0 μF, and R_T = 120 kΩ, the time constant is $\approx$600 ms, giving a switching time of $\approx$1.8 seconds (for 95% change). The switching period to slow idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the 1.8 second period, the quicker the switching time since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

The above switching times occur, however, after the level detectors have detected the appropriate signal levels, since their outputs operate the Attenuator Control Block. Referring to Figure 4, the rise time of the level detectors' outputs to new speech is quick by comparison ($\approx$1.0 ms), determined by the internal 350 Ω resistor and the external capacitor (typically 2.0 μF). The output's decay time is determined by the external capacitor, and an internal 4.0 μA current source giving a decay rate of $\approx$60 ms for a 120 mV excursion at RLO or TLO. However, the overall response time of the circuit is not a constant since it depends on the relative strength of the signals at the different level detectors, as well as the timing of the signals with respect to each other. The capacitors at the four outputs (RLO1, RLO2, TLO1, TLO2) must be equal value ($\pm$10%) to prevent problems in timing and level response.

The rise time of the level detector's outputs is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit during the normal pauses in speech.

The components at the inputs of the level detectors (RLI1, RLI2, TLI1, TLI2) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors.

DESIGN EQUATIONS

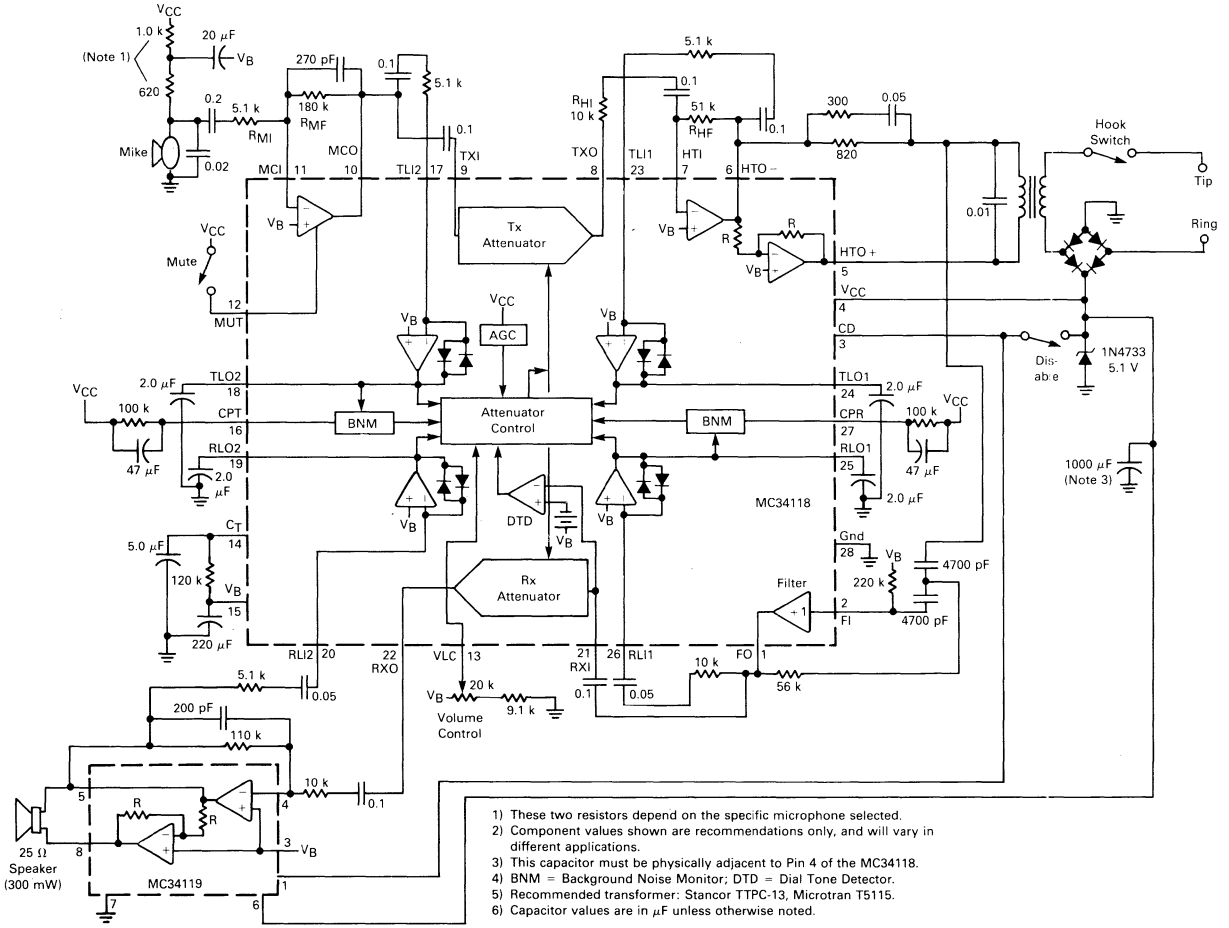
Referring to Figure 24 (the coupling capacitors have been omitted for simplicity), and the circuit of Figure 23, the following definitions will be used (all measurements are at 1.0 kHz):

- G_{MA} is the gain of the microphone amplifier measured from the microphone output to TXI (typically 35 V/V, or 31 dB);
- G_{TX} is the gain of the transmit attenuator, measured from TXI to TXO;
- G_{HA} is the gain of hybrid amplifiers, measured from TXO to the HTO−/HTO+ differential output (typically 10.2 V/V, or 20.1 dB);
- G_{HT} is the gain from HTO−/HTO+ to Tip/Ring for transmit signals, and includes the balance network (measured at 0.4 V/V, or −8.0 dB);
- G_{ST} is the sidetone gain, measured from HTO−/HTO+ to the filter input (measured at 0.18 V/V, or −15 dB);
- G_{HR} is the gain from Tip/Ring to the filter input for receive signals (measured at 0.833 V/V or −1.6 dB);
- G_{FO} is the gain of the filter stage, measured from the input of the filter to RXI, typically 0 dB at 1.0 kHz;
- G_{RX} is the gain of the receive attenuator measured from RXI to RXO;
- G_{SA} is the gain of the speaker amplifier, measured from RXO to the differential output of the MC34119 (typically 22 V/V or 26.8 dB);
- G_{AC} is the acoustic coupling, measured from the speaker differential voltage to the microphone output voltage.

I) Transmit Gain

The transmit gain, from the microphone output (V_M) to Tip and Ring, is determined by the output characteristics of the microphone, and the desired transmit level. For example, a typical electret microphone will produce $\approx$0.35 mVrms under normal speech conditions. To achieve 100 mVrms at Tip/Ring, an overall gain of 285 V/V is necessary. The gain of the transmit attenuator is fixed at 2.0 (+6.0 dB), and the gain through the hybrid of Figure 23 (G_{HT}) is nominally 0.4 (−8.0 dB). Therefore a gain of 357 V/V is required of the microphone and hybrid amplifiers. It is desirable to have the majority of that gain in the microphone amplifier for three reasons: 1) the low level signals from the microphone should be amplified as soon as possible to minimize signal/noise

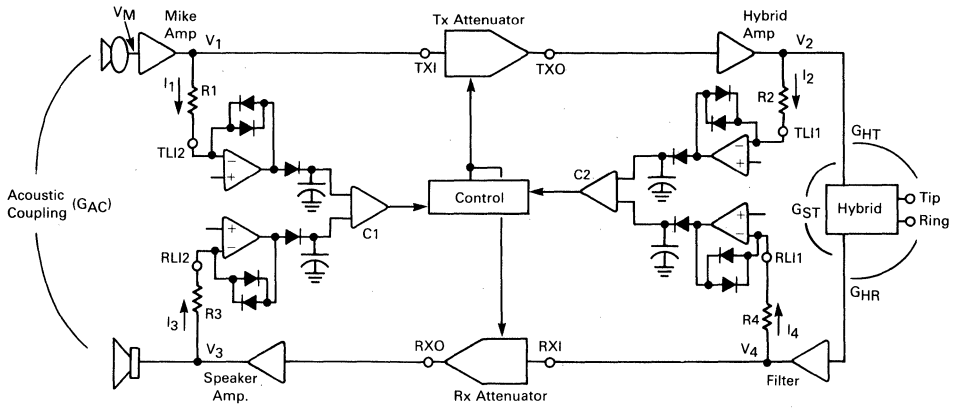
FIGURE 23 — MC34118 APPLICATION CIRCUIT (BASIC LINE POWERED SPEAKERPHONE)



1) These two resistors depend on the specific microphone selected.
2) Component values shown are recommendations only, and will vary in different applications.
3) This capacitor must be physically adjacent to Pin 4 of the MC34118.
4) BNM = Background Noise Monitor; DTD = Dial Tone Detector.
5) Recommended transformer: Stancor TTPC-13, Microtran T5115.
6) Capacitor values are in μF unless otherwise noted.

2

FIGURE 24 — BASIC BLOCK DIAGRAM FOR DESIGN PURPOSES



problems; 2) to provide a reasonable signal level to the TLI2 level detector; and 3) to minimize any gain applied to broadband noise generated within the attenuator. However, to cover the normal voiceband, the microphone amplifier's gain should not exceed 48 dB (see Figure 16). For the circuit of Figure 23, the gain of the microphone amplifier was set at 35 V/V (31 dB), and the differential gain of the hybrid amplifiers was set at 10.2 V/V (20.1 dB).

II) Receive Gain

The overall receive gain depends on the incoming signal level, and the desired output power at the speaker. Nominal receive levels (independent of the peaks) at Tip/Ring can be 35 mVrms (−27 dBm), although on long lines that level can be down to 8.0 mVrms (−40 dBm). The speaker power is:

$$P_{SPK} = \frac{10^{dBm/10} \times 0.6}{R_S} \qquad \text{(Equation 1)}$$

where R_S is the speaker impedance, and the dBm term is the incoming signal level increased by the gain of the receive path. Experience has shown that ≈30 dB gain is a satisfactory amount for the majority of applications. Using the above numbers and Equation 1, it would appear that the resulting power to the speaker is extremely low. However, Equation 1 does not consider the peaks in normal speech, which can be 10 to 15 times the rms value. Considering the peaks, the overall average power approaches 20–30 mW on long lines, and much more on short lines.

Referring to Figure 23, the gain from Tip/Ring to the filter input was measured at 0.833 V/V (−1.6 dB), the filter's gain is unity, and the receive attenuator's gain is 2.0 V/V (+6.0 dB) at maximum volume. The speaker amplifier's gain is set at 22 V/V (26.8 dB), which puts the overall gain at ≈31.2 dB.

III) Loop Gain

The total loop gain (of Figure 24) must add up to less than zero dB to obtain a stable circuit. This can be expressed as:

$$G_{MA} + G_{TX} + G_{HA} + G_{ST} + G_{FO} + G_{RX} + G_{SA} + G_{AC} < 0 \qquad \text{(Equation 2)}$$

Using the typical numbers mentioned above, and knowing that $G_{TX} + G_{RX} = -40$ dB, the required acoustic coupling can be determined:

$$G_{AC} < -[31 + 20.1 + (-15) + 0 + (-40) + 26.8] = -22.9 \text{ dB.} \qquad \text{(Equation 3)}$$

An acoustic loss of at least 23 dB is necessary to prevent instability and oscillations, commonly referred to as "singing." However, the following equations show that greater acoustic loss is necessary to obtain proper level detection and switching.

IV) Switching Thresholds

To switch comparator C1, currents I_1 and I_3 need to be determined. Referring to Figure 24, with a receive signal V_L applied to Tip/Ring, a current I_3 will flow through R3 into RLI2 according to the following equation:

$$I_3 = \frac{V_L}{R3}\left[G_{HR} \times G_{FO} \times G_{RX} \times \frac{G_{SA}}{2}\right] \qquad \text{(Equation 4)}$$

where the terms in the brackets are the V/V gain terms. The speaker amplifier gain is divided by two since G_{SA} is the differential gain of the amplifier, and V_3 is obtained from one side of that output. The current I_1, coming from the microphone circuit, is defined by:

$$I_1 = \frac{V_M \times G_{MA}}{R1} \quad \text{(Equation 5)}$$

where V_M is the microphone voltage. Since the switching threshold occurs when $I_1 = I_3$, combining the above two equations yields:

$$V_M = V_L \times \frac{R1}{R3} \frac{[G_{HR} \times G_{FO} \times G_{RX} \times G_{SA}]}{G_{MA} \times 2} \quad \text{(Equation 6)}$$

This is the general equation defining the microphone voltage necessary to switch comparator C1 when a receive signal V_L is present. The highest V_M occurs when the receive attenuator is at maximum gain (+6.0 dB). Using the typical numbers for Equation 6 yields:

$$V_M = 0.52\ V_L \quad \text{(Equation 7)}$$

To switch comparator C2, currents I_2 and I_4 need to be determined. With sound applied to the microphone, a voltage V_M is created by the microphone, resulting in a current I_2 into TLI1:

$$I_2 = \frac{V_M}{R2}\left[G_{MA} \times G_{TX} \times \frac{G_{HA}}{2}\right] \quad \text{(Equation 8)}$$

Since G_{HA} is the differential gain of the hybrid amplifiers, it is divided by two to obtain the voltage V_2 applied to R2. Comparator C2 switches when $I_4 = I_2$. I_4 is defined by:

$$I_4 = \frac{V_L}{R4}[G_{HR} \times G_{FO}] \quad \text{(Equation 9)}$$

Setting $I_4 = I_2$, and combining the above equations results in:

$$V_L = V_M \times \frac{R4}{R2} \times \frac{[G_{MA} \times G_{TX} \times G_{HA}]}{[G_{HR} \times G_{FO} \times 2]} \quad \text{(Equation 10)}$$

This equation defines the line voltage at Tip/Ring necessary to switch comparator C2 in the presence of a microphone voltage. The highest V_L occurs when the circuit is in the transmit mode (G_{TX} = +6.0 dB). Using the typical numbers for Equation 10 yields:

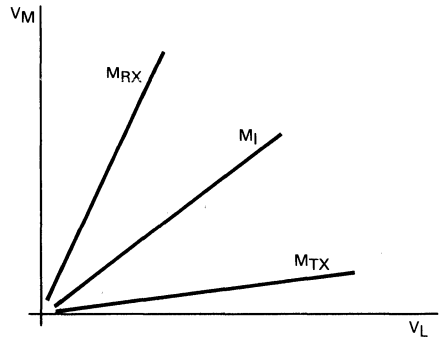
$$V_L = 840\ V_M \quad (\text{or } V_M = 0.0019\ V_L) \quad \text{(Equation 11)}$$

At idle, where the gain of the two attenuators is −20 dB (0.1 V/V), Equations 6 and 10 yield the same result:

$$V_M = 0.024\ V_L \quad \text{(Equation 12)}$$

Equations 7, 11, and 12 define the thresholds for switching, and are represented in the following graph:

FIGURE 25 — SWITCHING THRESHOLDS



The "M" terms are the slopes of the lines (0.52, 0.024, and 0.0019) which are the coefficients of the three equations. The M_{RX} line represents the receive to transmit threshold in that it defines the microphone signal level necessary to switch to transmit in the presence of a given receive signal level. The M_{TX} line represents the transmit to receive threshold. The M_I line represents the idle condition, and defines the threshold level on one side (transmit or receive) necessary to overcome noise on the other.

Some comments on the above graph:

— Acoustic coupling and sidetone coupling were not included in Equations 7 and 12. Those couplings will affect the actual performance of the final speakerphone due to their interaction with speech at the microphone, and the receive signal coming in at Tip/Ring. The effects of those couplings are difficult to predict due to their associated phase shifts and frequency response. In some cases the coupling signal will add, and other times subtract from the incoming signal. The physical design of the speakerphone enclosure, as well as the specific phone line to which it is connected, will affect the acoustic and sidetone couplings, respectively.

— The M_{RX} line helps define the maximum acoustic coupling allowed in a system, which can be found from the following equation:

$$G_{AC\text{-}MAX} = \frac{R1}{2 \times R3 \times G_{MA}} \quad \text{(Equation 13)}$$

Equation 13 is independent of the volume control setting. Conversely, the acoustic coupling of a designed system helps determine the minimum slope of that line. Using the component values of Figure 23 in Equation

13 yields a $G_{AC\text{-}MAX}$ of −37 dB. Experience has shown, however, that an acoustic coupling loss of >40 dB is desirable.

— The M_{TX} line helps define the maximum sidetone coupling (G_{ST}) allowed in the system, which can be found from the following equation:

$$G_{ST} = \frac{R4}{2 \times R2 \times G_{FO}} \qquad \text{(Equation 14)}$$

Using the component values of Figure 23 in Equation 14 yields a maximum sidetone of 0 dB. Experience has shown, however, that a minimum of 6.0 dB loss is preferable.

The above equations can be used to determine the resistor values for the level detector inputs. Equation 6 can be used to determine the R1/R3 ratio, and Equation 10 can be used to determine the R4/R2 ratio. In Figure 24, R1–R4 each represent the combined impedance of the resistor and coupling capacitor at each level detector input. The magnitude of each RC's impedance should be kept within the range of 2.0 k–15 kΩ in the voiceband (due to the typical signal levels present) to obtain the best performance from the level detectors. The specific R and C at each location will determine the frequency response of that level detector.

APPLICATION INFORMATION

DIAL TONE DETECTOR

The threshold for the dial tone detector is internally set at 15 mV (10 mVrms) below V_B (see Figure 5). That threshold can be reduced by connecting a resistor from RXI to ground. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_B}{\Delta V} - 1\right]$$

where V_B is the voltage at Pin 15, and ΔV is the amount of threshold reduction. By connecting a resistor from V_{CC} to RXI, the threshold can be increased. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

where ΔV is the amount of the threshold increase.

BACKGROUND NOISE MONITORS

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to the "on" position, by disabling the background noise monitors, and applying a signal so as to activate the level detectors. Grounding the CPR pin will disable the receive background noise monitor, thereby indicating the "presence of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

TRANSMIT/RECEIVE DETECTION PRIORITY

Although the MC34118 was designed to have an idle mode such that the attenuators are halfway between their full on and full off positions, the idle mode can be biased towards the transmit or the receive side. With this done, gaining control of the circuit from idle will be easier for that side towards which it is biased since that path will have less attenuation at idle.

By connecting a resistor from C_T (Pin 14) to ground, the circuit will be biased towards the transmit side. The resistor value is calculated from:

$$R = R_T\left[\frac{V_B}{\Delta V} - 1\right]$$

where R is the added resistor, R_T is the resistor normally between Pins 14 and 15 (typically 120 kΩ), and ΔV is the difference between V_B and the voltage at C_T at idle (refer to Figure 10).

By connecting a resistor from C_T (Pin 14) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

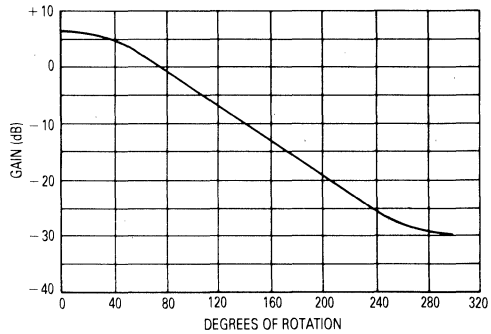
$$R = R_T\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

R, R_T, and ΔV are the same as above. Switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 100 mV.

VOLUME CONTROL

If a potentiometer with a standard linear taper is used for the volume control, the graph of Figure 14 indicates that the receive gain will not vary in a linear manner with respect to the pot's position. In situations where this may be objectionable, a potentiometer with an audio taper (commonly used in radio volume controls) will provide a more linear relationship as indicated in Figure 26. The slight non-linearity at each end of the graph is due to the physical construction of the potentiometer, and will vary among different manufacturers.

FIGURE 26 — RECEIVE ATTENUATOR GAIN versus POTENTIOMETER POSITION USING AUDIO TAPER



APPLICATION CIRCUIT

The circuit of Figure 23 is a basic speakerphone, to be used in parallel with any other telephone which con-

tains the ringer, dialer, and handset functions. The circuit is powered entirely by the telephone line's loop current, and its characteristics are shown in Figures 27–30.

FIGURE 27 — DC V-I CHARACTERISTICS

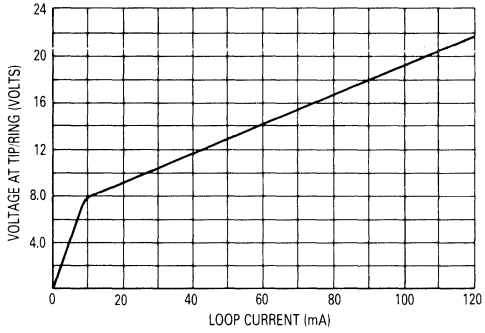


FIGURE 28 — AC TERMINATION IMPEDANCE

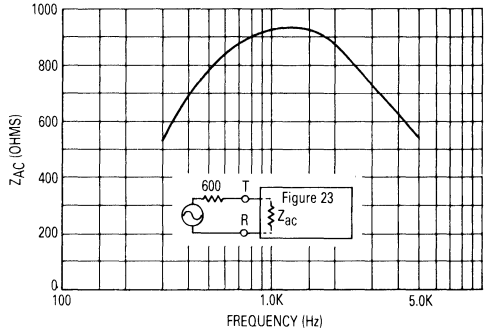


FIGURE 29 — TRANSMIT GAIN — MICROPHONE TO TIP/RING

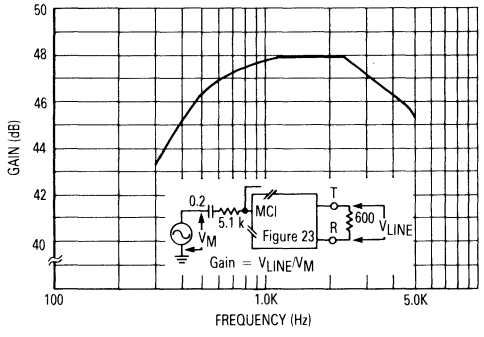


FIGURE 30 — RECEIVE GAIN

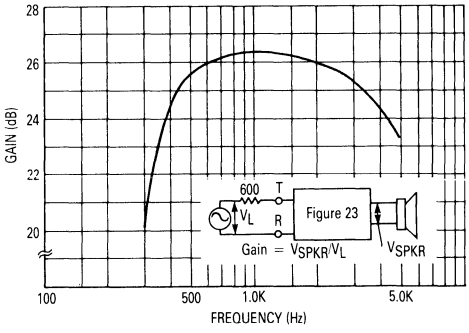
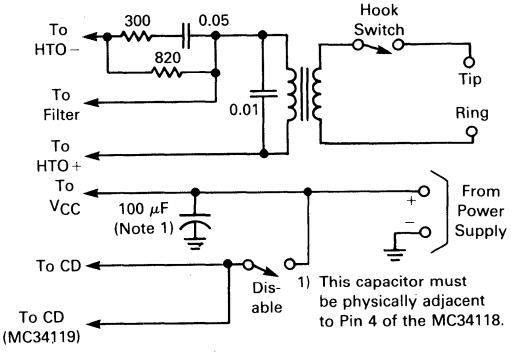


Figure 31 shows how the same circuit can be configured to be powered from a 3.5–6.0 volt power supply rather than the phone line.

FIGURE 31 — OPERATING FROM A POWER SUPPLY



ADDING A DIALER

Figure 32 shows the addition of a dialer to the circuit of Figure 23, with the additional components shown in bold. The MC145412 pulse/tone dialer is shown configured for DTMF operation. The DTMF output (Pin 18) is fed to the hybrid amplifiers at HTI, and the DTMF levels at Tip/Ring are adjusted by varying the 39 kΩ resistor. The Mute Output (active low at Pin 11) mutes the microphone amplifier, and attenuates the DTMF signals in the receive path (by means of the 10 k/3.0 k divider). The MC34118 is forced into the fast idle mode during dialing. The 3.0 volt battery provides for memory retention of the dialer's 10 number storage when the circuit is unpowered.

RFI INTERFERENCE

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the cir-

2

cuit through Tip and Ring, through the microphone wiring to the microphone amplifier, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1, TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. Any other high impedance input pin (MCI, HTI, FI, VLC) should be considered sensitive to RFI signals.

IN THE FINAL ANALYSIS . . .

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, or any combination of the two. Proper acoustic separation of the speaker and microphone, as described in the Design Equations, is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuits shown in this data sheet will have to be "fine tuned" to match the acoustics of the enclosure, the specific hybrid, and the specific microphone and speaker selected. The component values shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and speaker amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
312-595-1022
Model EM-60

Hosiden America Corp.
Elk Grove Village, IL 60007
312-981-1144
Model KUC2123

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and Application Bulletin F232

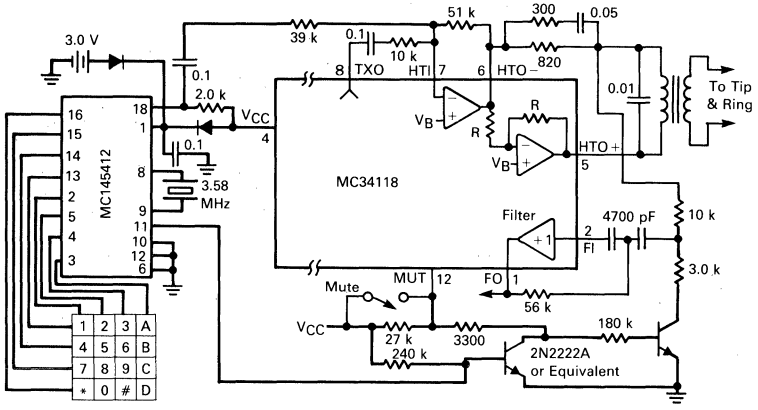
PREM Magnetics, Inc.
McHenry, IL 60050
815-385-2700
Various models — ask for catalog

Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

Motorola Inc. does not endorse or warrant the suppliers referenced.

FIGURE 32 — ADDING A DIALER TO THE SPEAKERPHONE



MC34119

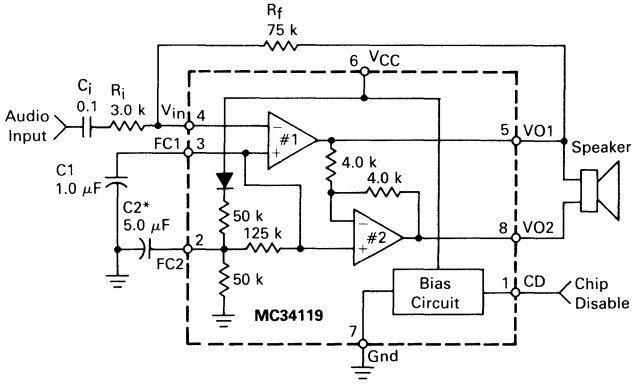
Specifications and Applications Information

LOW POWER AUDIO AMPLIFIER

The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8-pin DIP or a surface mount package.

- Wide Operating Supply Voltage Range (2–16 volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current (65 μA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT

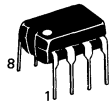


* = Optional

Differential Gain = $2 \times \frac{R_f}{R_i}$

LOW POWER AUDIO AMPLIFIER

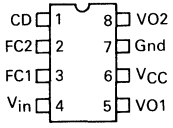
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626-05

D SUFFIX
PLASTIC PACKAGE
CASE 751-03
SO-8

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION		
Device	**Temperature Range**	**Package**
MC34119P	−20°C to +70°C	Plastic DIP
MC34119D		Plastic SOIC

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage	−1.0 to +18	Vdc
Maximum Output Current at VO1, VO2	±250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD	−1.0, V_{CC}+1.0	Vdc
Applied Output Voltage to VO1, VO2 when disabled	−1.0, V_{CC}+1.0	Vdc
Junction Temperature	−55, +140	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	+2.0	—	+16	Vdc
Load Impedance	R_L	8.0	—	100	Ω
Peak Load Current	I_L	—	—	±200	mA
Differential Gain (5.0 kHz bandwidth)	AVD	0	—	46	dB
Voltage @ CD (Pin 1)	VCD	0	—	V_{CC}	Vdc
Ambient Temperature	T_A	−20	—	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Units
AMPLIFIERS (AC CHARACTERISTICS)					
AC Input Resistance (@ V_{in})	r_i	—	>30	—	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	—	—	dB
Closed Loop Gain (Amplifier #2) (V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	−0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	—	1.5	—	MHz
Output Power, V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	P_{out3} P_{out6} P_{out12}	55 250 400	— — —	— — —	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD	 — — —	 0.5 0.5 0.6	 1.0 — —	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔV_{CC} = 3.0 V) (C1 = ∞, C2 = 0.01 μF) (C1 = 0.1 μF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 μF, C2 = 5.0 μF, f = 1.0 kHz)	PSRR	 50 — —	 — 12 52	 — — —	dB
Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	—	>70	—	dB
AMPLIFIERS (DC CHARACTERISTICS)					
Output DC Level @ VO1, VO2, V_{CC} = 3.0 V, R_L = 16 Ω (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	VO(3) VO(6) VO(12)	1.0 — —	1.15 2.65 5.65	1.25 — —	Vdc
Output High Level (I_{out} = −75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OH}	—	V_{CC}−1.0	—	Vdc
Output Low Level (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OL}	—	0.16	—	Vdc
Output DC Offset Voltage (VO1–VO2) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔV_O	−30	0	+30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	—	−100	−200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V)	R_{FC1}	100	150	220	kΩ
Equivalent Resistance @ FC2 (V_{CC} = 6.0 V)	R_{FC2}	18	25	40	kΩ
CHIP DISABLE (Pin 1)					
Input Voltage — Low	V_{IL}	—	—	0.8	Vdc
Input Voltage — High	V_{IH}	2.0	—	—	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 I_{CC3} I_{CC16} I_{CCD}	 — — —	 2.7 3.3 65	 4.0 5.0 100	 mA μA

Note: Currents into a pin are positive, currents out of a pin are negative.

PIN DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable — Digital input. A Logic "0" (<0.8 V) sets normal operation. A Logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog Ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is ≈ (V_{CC} − 0.7 V)/2.
V_{CC}	6	DC supply voltage (+2.0 to +16 volts) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ (V_{CC} − 0.7 V)/2.

TYPICAL TEMPERATURE PERFORMANCE (−20° < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current (@ V_{in})	±40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0 V)	−2.5	μA/°C
(V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	−0.03	

DESIGN GUIDELINES

GENERAL

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1–VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistors R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300–3400 Hz), a maximum closed loop gain of 46 dB is recommended. Amplifier #2 is internally set to a gain of −1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 volts above ground, and to within ≈1.3 volts below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

The output dc offset voltage (VO1–VO2) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing VO1 to shift negative by an amount equal to [R_f x I_{IB}]. VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical Characteristics is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4–7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of +6.0 volts. The turn-on time is ≈60% longer for V_{CC} = 3.0 volts, and ≈20% less for V_{CC} = 9.0 volts. Turn-off time is <10 μs upon removal of V_{CC}.

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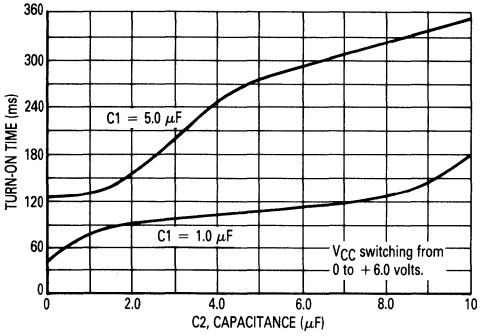
FIGURE 1 — TURN-ON TIME versus C1, C2 AT POWER-ON



CHIP DISABLE

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 to 0.8 volts), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 to V_{CC} volts), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 μs, and turn on-time is 12–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, VO1 and VO2, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

POWER DISSIPATION

Figures 8–10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature;
and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15;
and I_{RMS} is the RMS current at the load;
and R_L is the load resistance.

Figures 8–10, along with Figures 11–13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω, and 32 Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally the speaker wires should be twisted tightly, and be not more than a few inches in length.

TYPICAL CHARACTERISTICS

FIGURE 2 — AMPLIFIER #1 OPEN LOOP GAIN AND PHASE

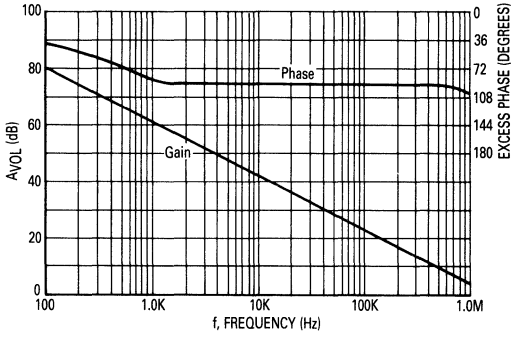
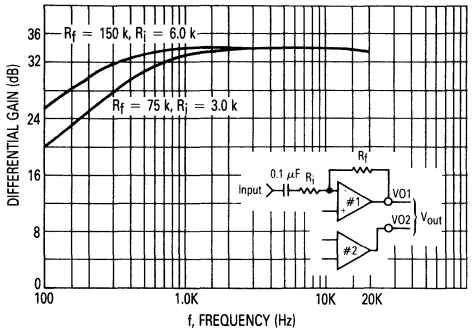


FIGURE 3 — DIFFERENTIAL GAIN versus FREQUENCY



POWER SUPPLY REJECTION versus FREQUENCY

FIGURE 4 — C2 = 10 μF

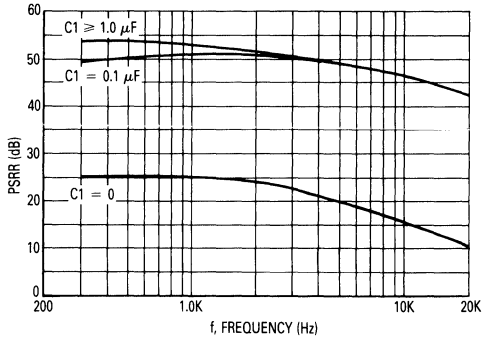


FIGURE 5 — C2 = 5.0 μF

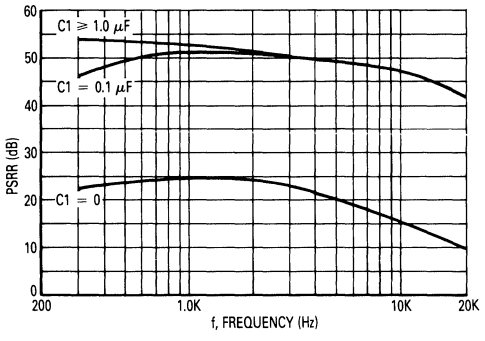


FIGURE 6 — C2 = 1.0 μF

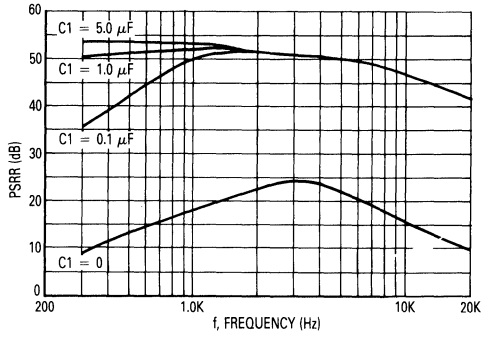


FIGURE 7 — C2 = 0

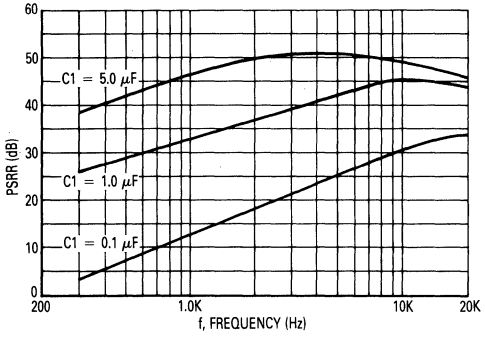


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FIGURE 8 — DEVICE DISSIPATION 8.0 Ω LOAD

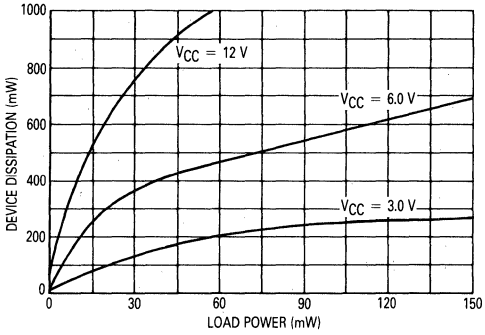

FIGURE 9 — DEVICE DISSIPATION 16 Ω LOAD

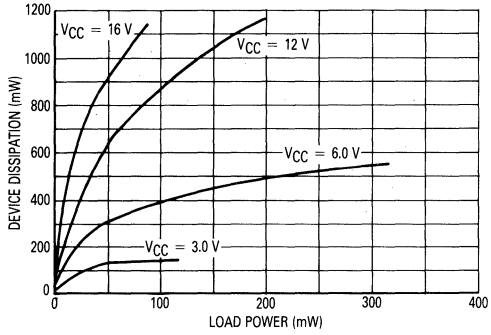

FIGURE 10 — DEVICE DISSIPATION 32 Ω LOAD

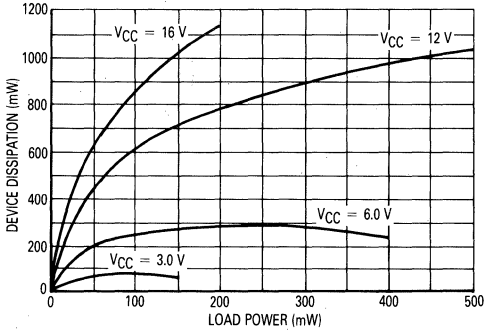

FIGURE 11 — DISTORTION versus POWER f = 1.0 kHz, AVD = 34 dB

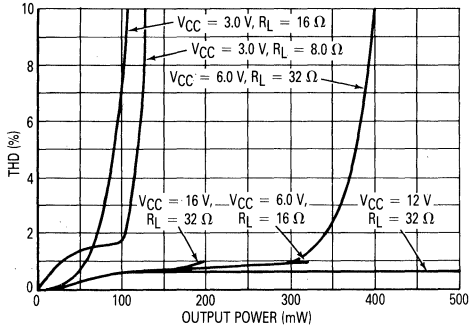

FIGURE 12 — DISTORTION versus POWER f = 3.0 kHz, AVD = 34 dB

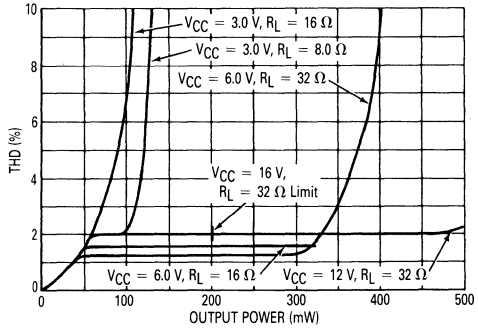

FIGURE 13 — DISTORTION versus POWER f = 1, 3.0 kHz, AVD = 12 dB

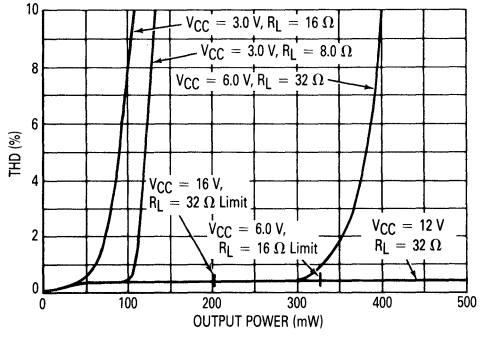

FIGURE 14 — MAXIMUM ALLOWABLE LOAD POWER

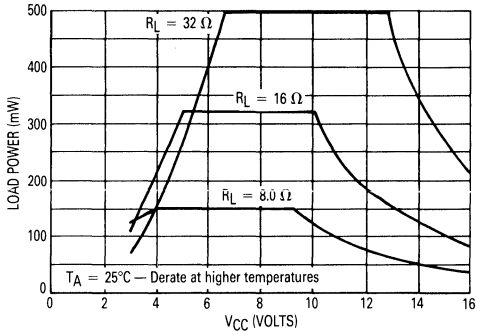

FIGURE 15 — POWER SUPPLY CURRENT

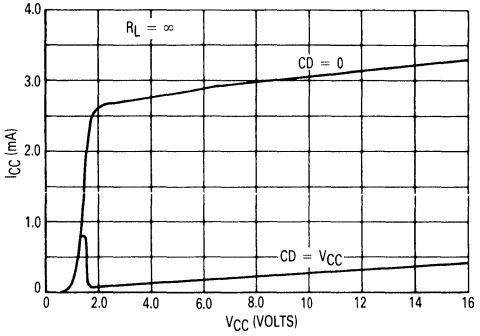

FIGURE 16 — SMALL SIGNAL RESPONSE

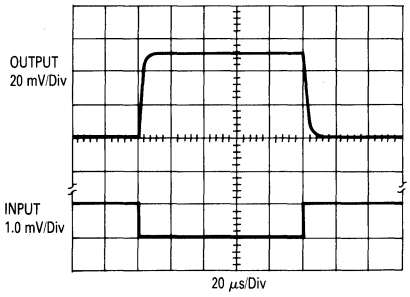

FIGURE 17 — LARGE SIGNAL RESPONSE

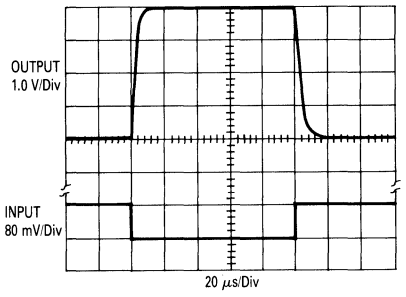

FIGURE 18 — V_{CC}–V_{OH} @ VO1, VO2 versus LOAD CURRENT

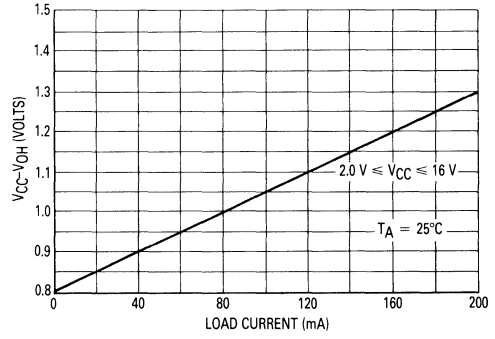

FIGURE 19 — V_{OL} @ VO1, VO2 versus LOAD CURRENT

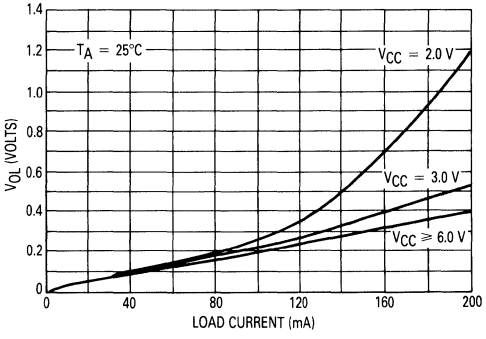

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FIGURE 20 — INPUT CHARACTERISTICS @ CD (PIN 1)

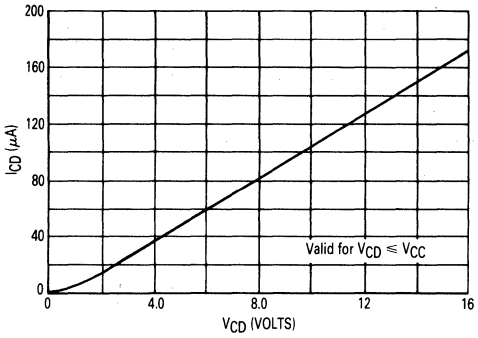
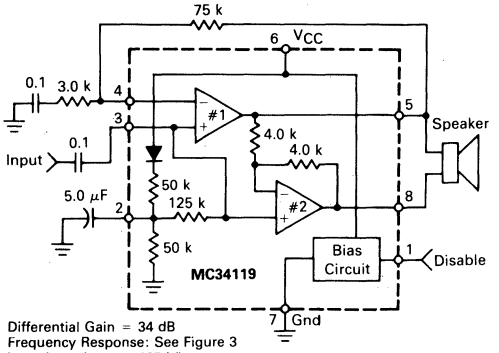


FIGURE 21 — AUDIO AMPLIFIER WITH HIGH INPUT IMPEDANCE



Differential Gain = 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

FIGURE 22 — AUDIO AMPLIFIER WITH BASS SUPPRESSION

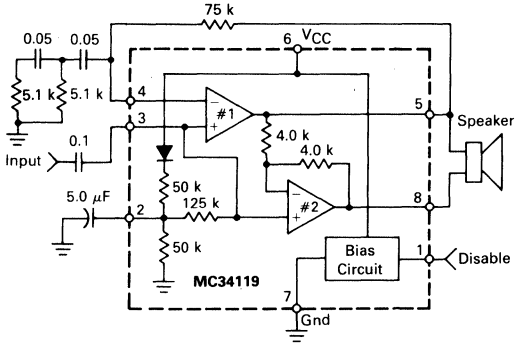


FIGURE 23 — FREQUENCY RESPONSE OF FIGURE 22

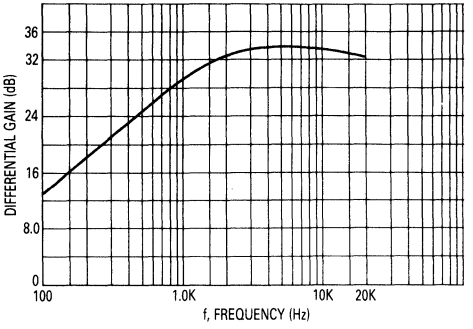


FIGURE 24 — AUDIO AMPLIFIER WITH BANDPASS

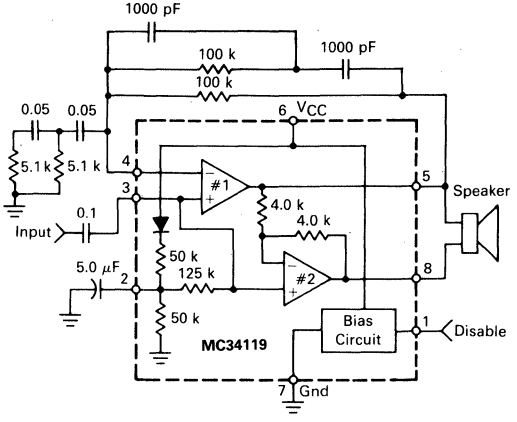


FIGURE 25 — FREQUENCY RESPONSE OF FIGURE 24

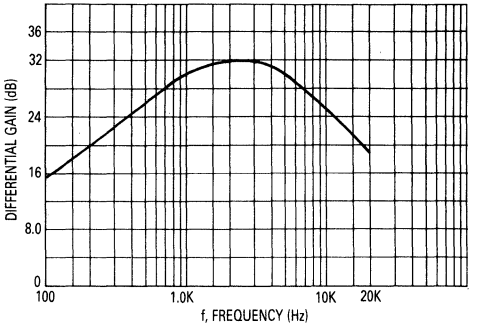
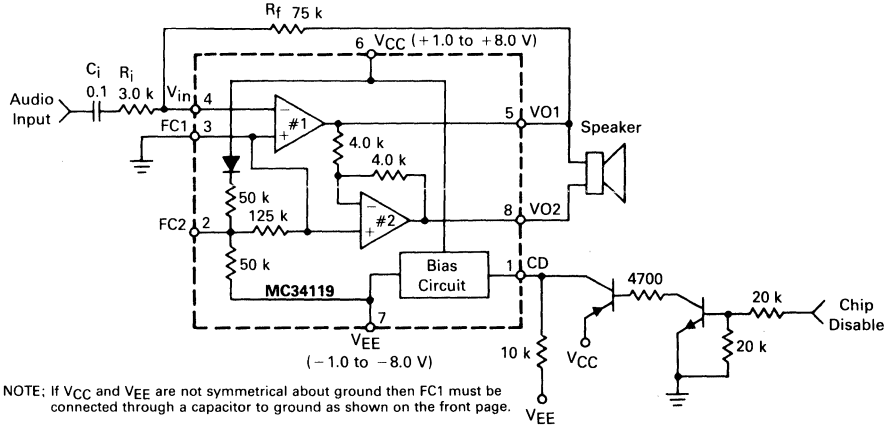


FIGURE 26 — SPLIT SUPPLY OPERATION



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

MC34129
MC33129

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Specifications and Applications Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

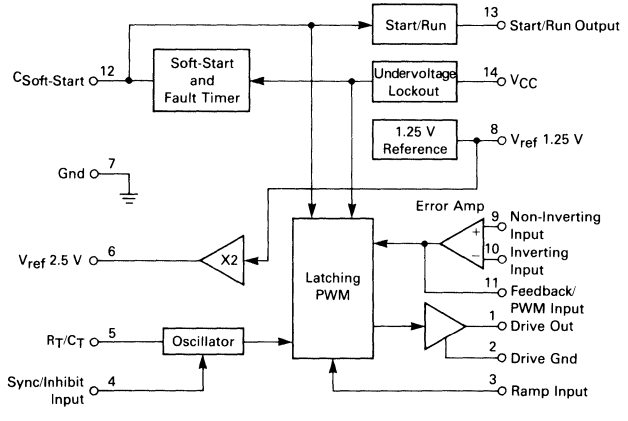
The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

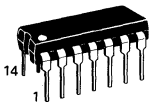
SIMPLIFIED BLOCK DIAGRAM



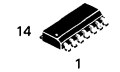
SENSEFET is a trademark of Motorola Inc.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

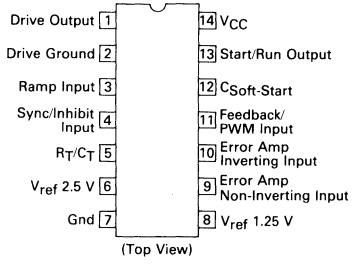


P SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-02
SO-14

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0 to +70°C	SO-14 Plastic DIP
MC34129P	0 to +70°C	Plastic DIP
MC33129D	−40 to +85°C	SO-14 Plastic DIP
MC33129P	−40 to +85°C	Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	−0.3 to 5.5	V
Sync Input Voltage	V_{sync}	−0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix Package SO-14 Case 751A-01 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air P Suffix Package Case 646-06 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 — —	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 — —	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = −10 to +500 μA 2.50 V Ref., I_L = −0.1 to +1.0 mA	Reg_{load}	 — —	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 — —	 1.5 —	 — 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	—	10	—	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 — —	 25 —	 — 200	nA
Input Common-Mode Voltage Range	V_{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	—	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 to 10 V)	PSRR	65	85	—	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	—	μA
Output Voltage Swing High State (I_{Source} = 0 μA) Low State (I_{Sink} = 500 μA)	 V_{OH} V_{OL}	 1.75 —	 1.96 0.1	 2.25 0.15	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

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ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	−120	−250	μA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	μA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	—	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 μA)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	μs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage (I_{Sink} = 500 μA)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	—	0.4	2.0	μA
Output Zener Voltage (I_Z = 10 mA)	V_Z	—	(V_{CC} + 7.6)	—	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	μA
Sync Input Current High State (V_{in} = 2.0 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 40 15	 125 35	μA
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage High State (I_{Source} = 200 mA) Low State (I_{Sink} = 200 mA)	 V_{OH} V_{OL}	 8.3 —	 8.9 1.4	 — 1.8	V
Low State Holding Current	I_H	—	225	—	μA
Output Voltage Rise Time (C_L = 500 pF)	t_r	—	100	—	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	—	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

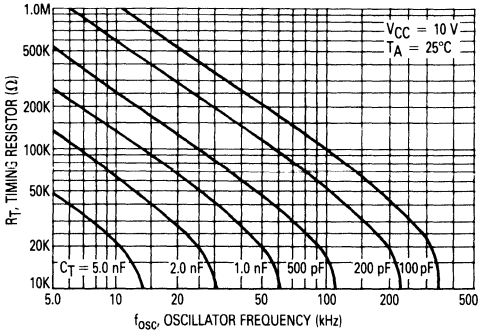

FIGURE 2 — OUTPUT DEAD-TIME versus OSCILLATOR FREQUENCY

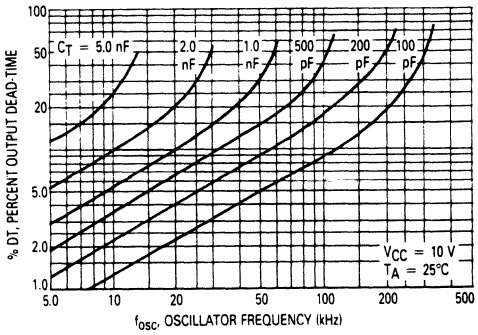

FIGURE 3 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

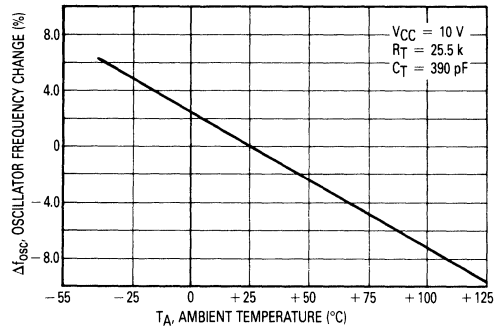

FIGURE 4 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

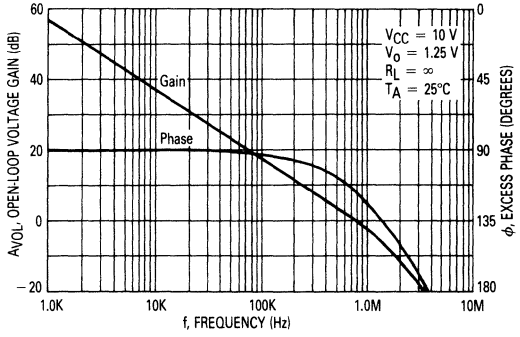

FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

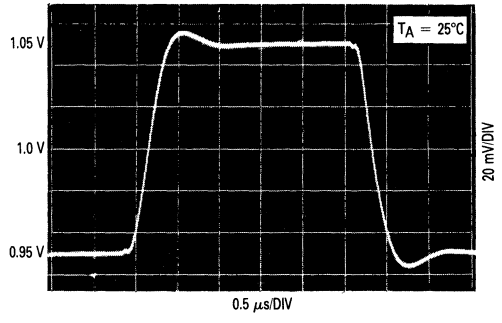

FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

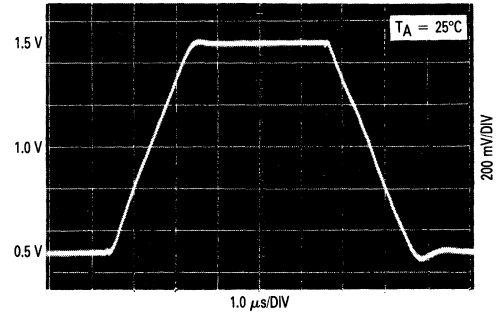

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FIGURE 7 — ERROR AMP OPEN-LOOP DC GAIN versus LOAD RESISTANCE

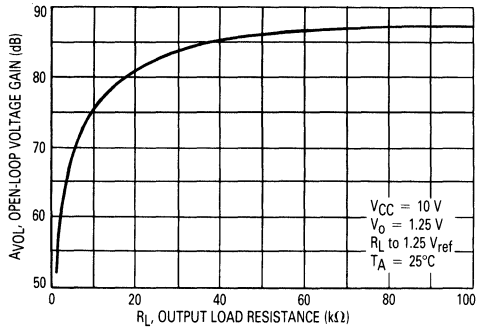


FIGURE 8 — ERROR AMP OUTPUT SATURATION versus SINK CURRENT

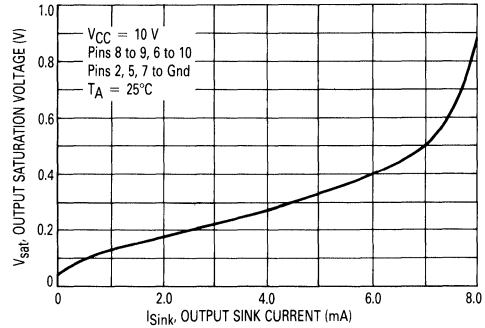


FIGURE 9 — SOFT-START BUFFER OUTPUT SATURATION versus SINK CURRENT

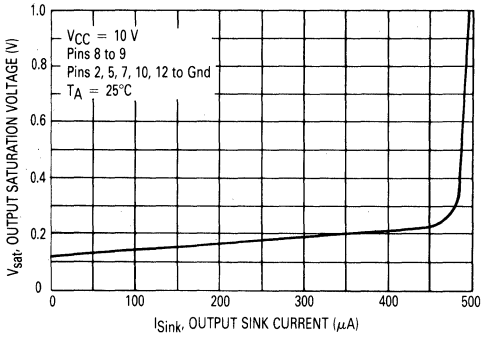


FIGURE 10 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

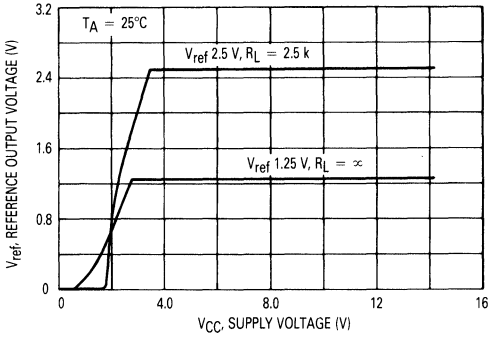


FIGURE 11 — 1.25 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

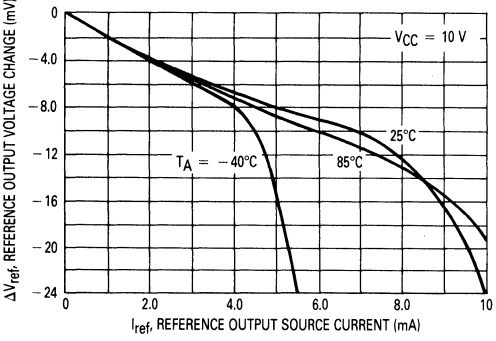


FIGURE 12 — 2.5 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

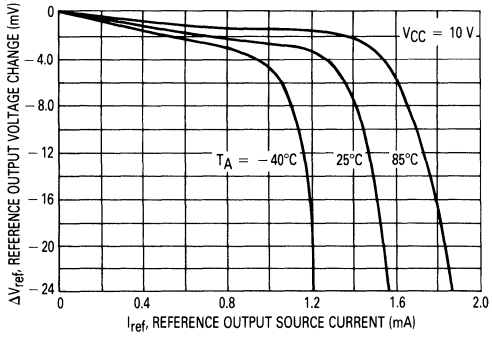


FIGURE 13 — 1.25 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

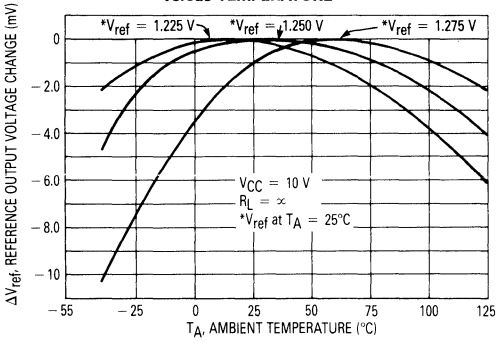


FIGURE 14 — 2.5 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

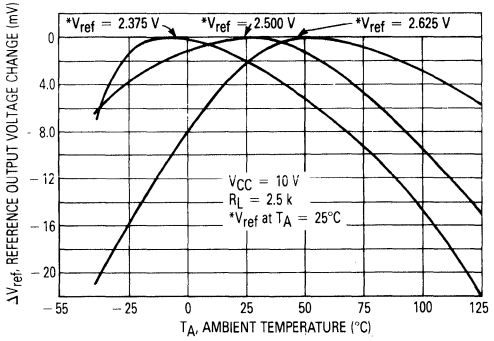


FIGURE 15 — DRIVE OUTPUT SATURATION versus LOAD CURRENT

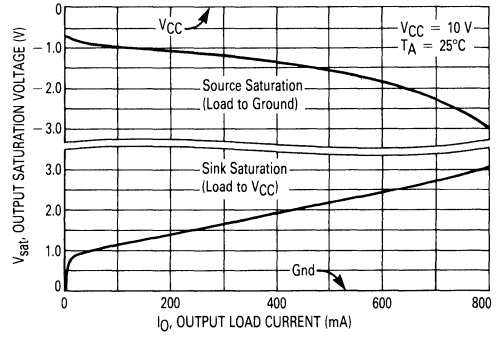


FIGURE 16 — DRIVE OUTPUT WAVEFORM

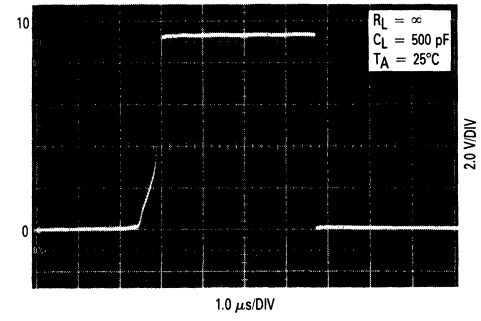
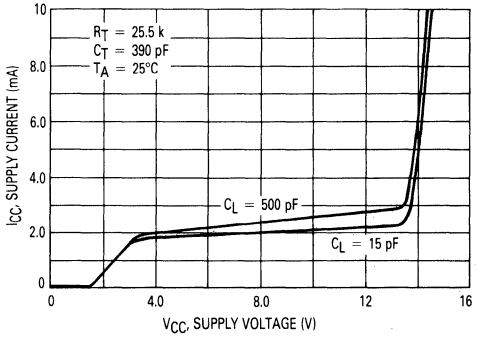


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier Non-Inverting Input.
9	Error Amp Non-Inverting Input	This is the non-inverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft\text{-}Start}$	A capacitor $C_{Soft\text{-}Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Sync/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM COMPARATOR AND LATCH

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically $-120\ \mu A$). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

ERROR AMP AND SOFT-START BUFFER

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the non-inverting input connected to Pin 12. An internal 1.0 μA

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FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

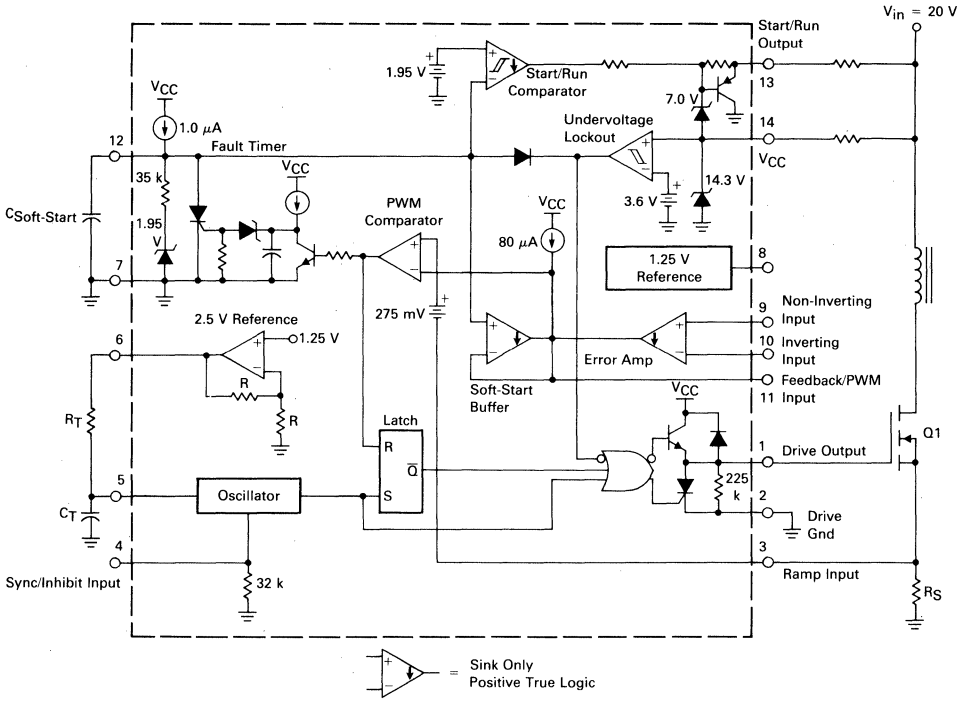
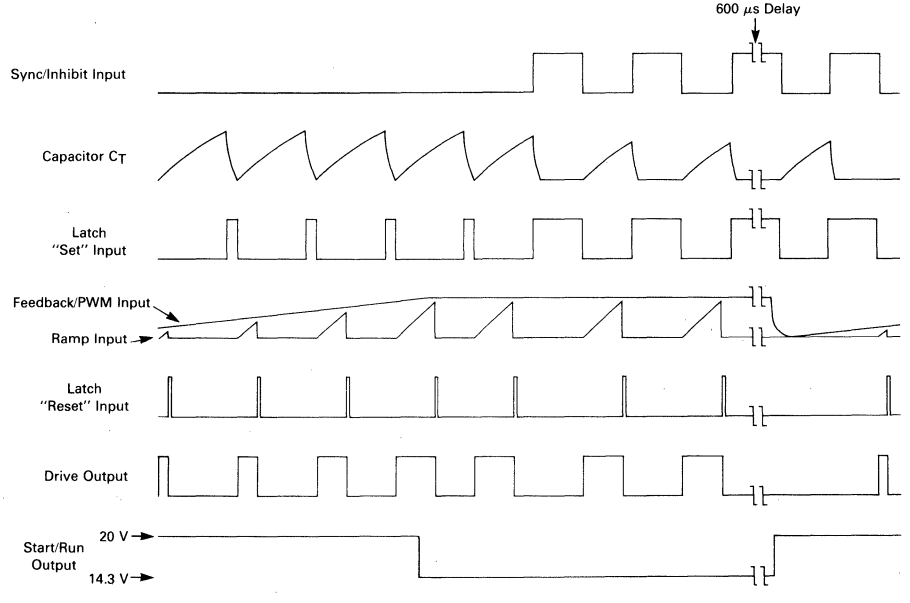


FIGURE 19 — TIMING DIAGRAM



OPERATING DESCRIPTION (continued)

current source charges the soft-start capacitor ($C_{Soft\text{-}Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

FAULT TIMER

This unique circuit prevents sustained operation in a lockout condition. This can occur with conventional switching control IC's when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{Soft\text{-}Start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

START/RUN COMPARATOR

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft\text{-}Start}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft\text{-}Start}$ reaches the 1.95 V clamp level, the Start-Run output switches low (V_{CC} – 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95\ V\ C_{Soft\text{-}Start}}{1.0\ \mu A} = 1.95\ C_{Soft\text{-}Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base-emitter junction.

DRIVE OUTPUT AND DRIVE GROUND

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control IC's that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low-state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

UNDERVOLTAGE LOCKOUT

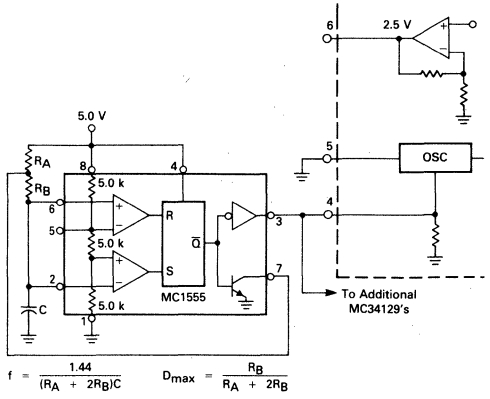
The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft\text{-}Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

REFERENCES

The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

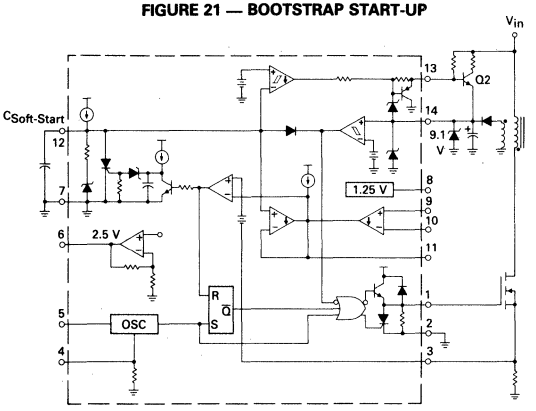
2

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



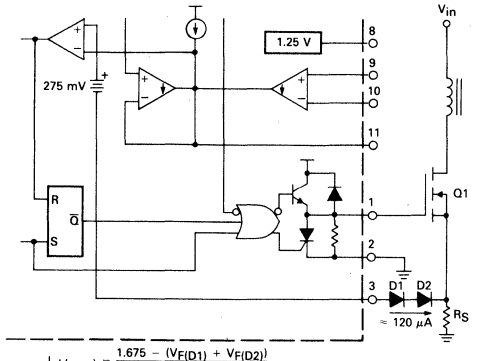
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

FIGURE 21 — BOOTSTRAP START-UP



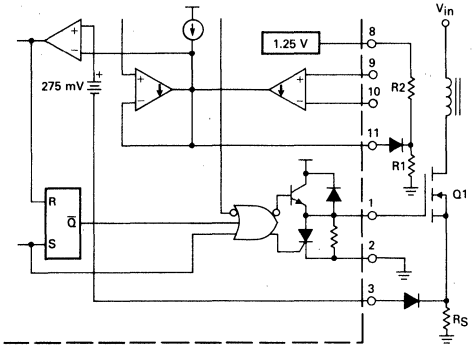
The external 9.1 V zener is required when driving low threshold MOSFETs.

FIGURE 22 — DISCRETE STEP REDUCTION OF CLAMP LEVEL



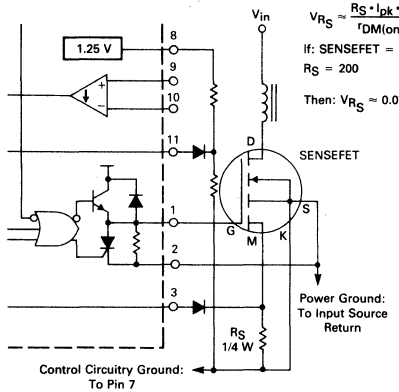
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

FIGURE 23 — ADJUSTABLE REDUCTION OF CLAMP LEVEL



If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{\frac{1.25}{\left(\frac{R2}{R1} + 1\right)} - 0.275}{R_S}$

FIGURE 24 — CURRENT SENSING POWER MOSFET



$$V_{R_S} \approx \frac{R_S \cdot I_{pk} \cdot r_{DS(on)}}{r_{DM(on)} + R_S}$$

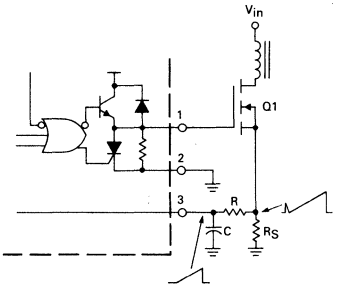
If: SENSEFET = MTP10N10M

R_S = 200

Then: $V_{R_S} \approx 0.075\ I_{pk}$

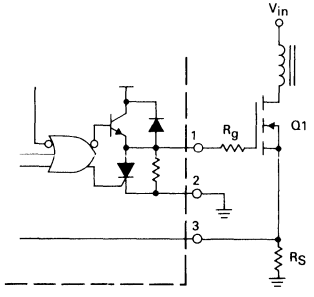
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

FIGURE 25 — CURRENT WAVEFORM SPIKE SUPPRESSION



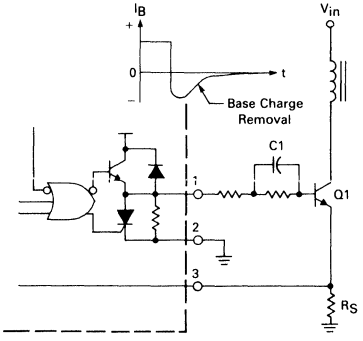
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 26 — MOSFET PARASITIC OSCILLATIONS



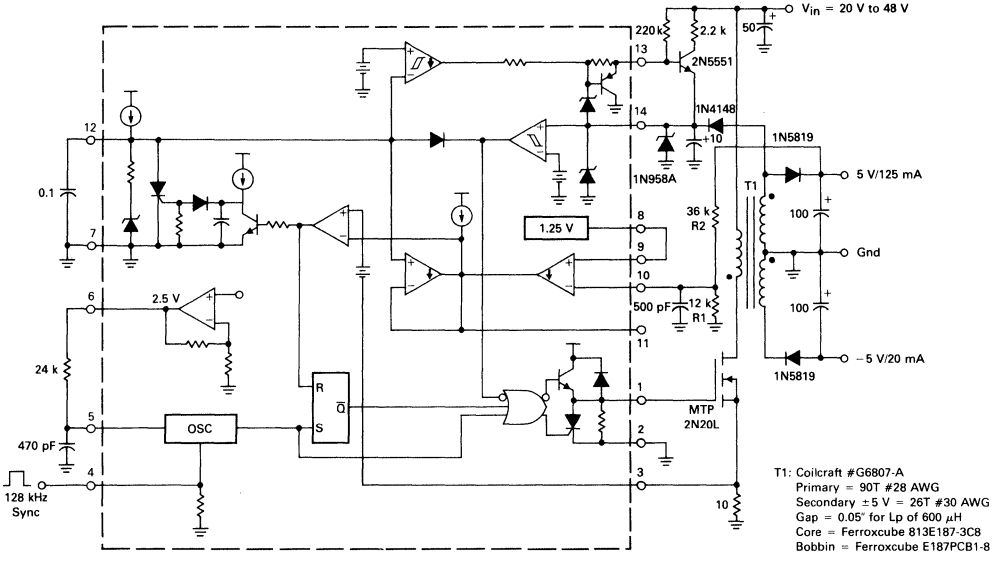
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 27 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 28 — NON-ISOLATED 725 mW FLYBACK REGULATOR



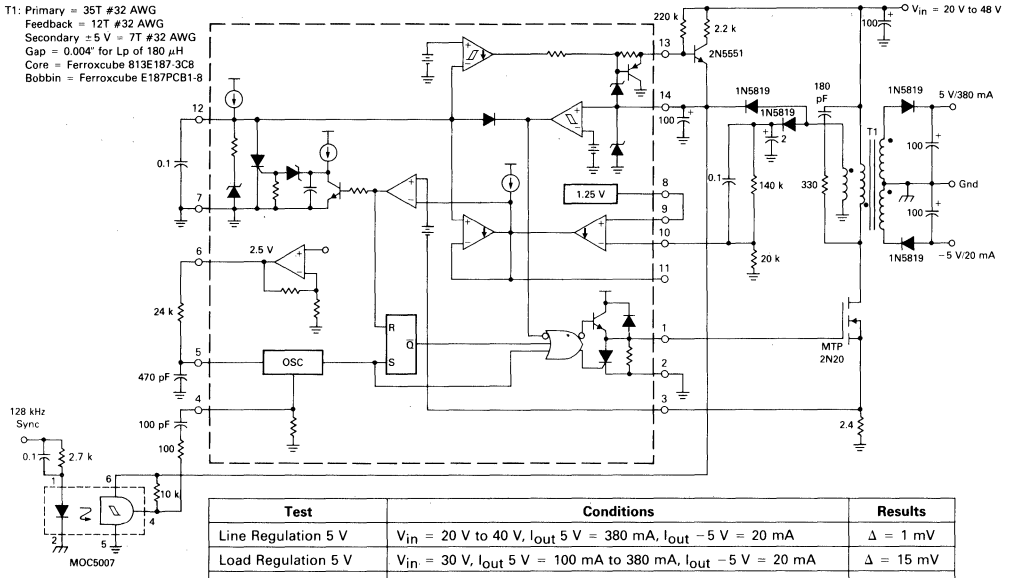
T1: Coilcraft #G6807-A
Primary = 90T #28 AWG
Secondary ±5 V = 26T #30 AWG
Gap = 0.05" for Lp of 600 μH
Core = Ferroxcube 813E187-3C8
Bobbin = Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 125 mA, I_{out} –5 V = 20 mA	Δ = 1.0 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 0 mA to 150 mA, I_{out} –5 V = 20 mA	Δ = 2.0 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} –5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} –5 V = 20 mA	77%

$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

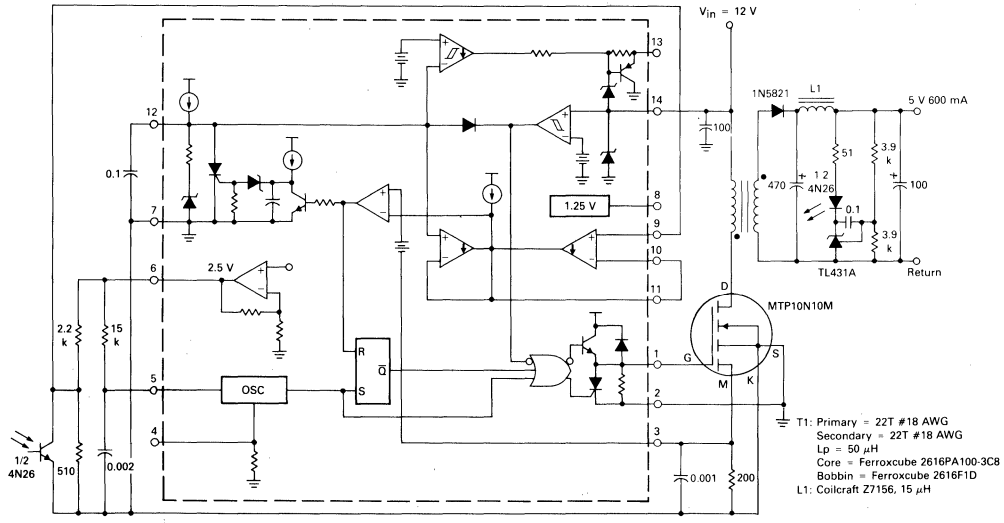
2

FIGURE 29 — ISOLATED 2.0 W FLYBACK REGULATOR



Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	Δ = 1 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 100 mA to 380 mA, I_{out} −5 V = 20 mA	Δ = 15 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	73%

FIGURE 30 — ISOLATED 3.0 W FLYBACK REGULATOR WITH SECONDARY SIDE SENSING



Test	Conditions	Results
Line Regulation	V_{in} = 8 V to 12 V, I_{out} 600 mA	Δ = 1 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp-p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MC142100
MC145100

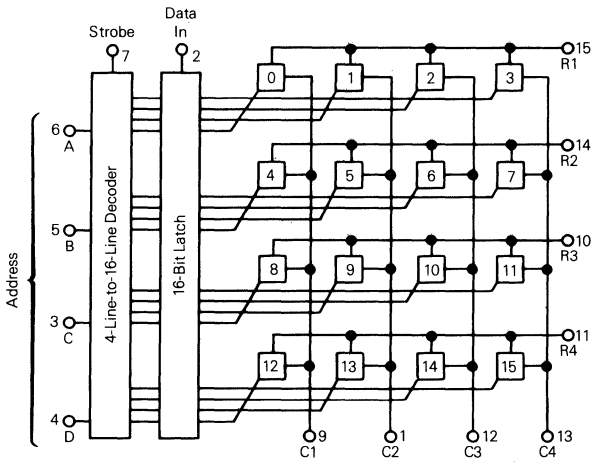
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

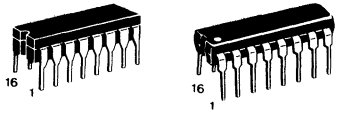
4 × 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

4 × 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

The MC142100 and MC145100 consist of 16 crosspoint switches (analog transmission gates) organized in 4 rows and 4 columns. Both devices have 16 latches, each of which controls the state of a particular switch. Any of the 16 switches can be selected by applying its address to the device and a pulse to the strobe input. The selected crosspoint will turn on if during strobe, Data In was a one and will turn off if during strobe, Data In was a zero. In addition the MC145100 will reset all non-selected switches in the same row as the selected switch. Other switches are unaffected. In the MC145100, an internal power-on reset turns off all switches as power is applied.

- Internal Latches Control State of Switches
- Power-On Reset (MC145100 Only)
- Low On Resistance — Typically on 110 Ω @ 10 Vdc
- Large Analog Range ($V_{DD} - V_{SS}$)
- All Pins Are Diode Protected
- Matched Switch Characteristics
- High CMOS Noise Immunity
- MC142100 Pin-for-Pin Replacement for CD22100





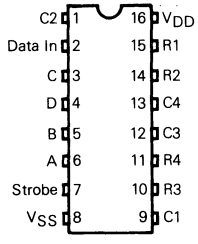
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENTS



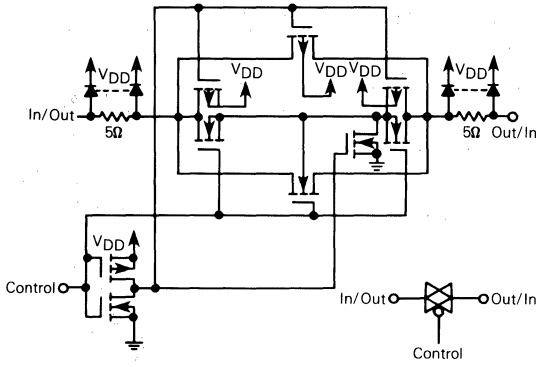
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

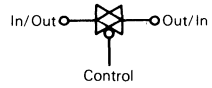
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused control inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

2

ANALOG TRANSMISSION GATE
(CROSSPOINT) SCHEMATIC





ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Operating Voltage MC145100	V_{DD}	–	4.25	18	4.25	–	18	4.25	18	Vdc
MC142100			3	18	3	–	18	3	18	
Input Voltage (Logic) "0" Level	V_{IL}									Vdc
Control Input		5	–	1.5	–	2.25	1.5	–	1.5	
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
		5	3.5	–	3.5	2.75	–	3.5	–	
		10	7.0	–	7.0	5.50	–	7.0	–	
See Figure 1		15	11.0	–	11.0	8.25	–	11.0	–	
Input Current AL	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pins 2, 3, 4, 5, 6, 7 CL, CP	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	
Input Capacitance (V_{in} = 0)	C_{in}									pF
Digital Inputs		10	–	–	–	7	15	–	–	
Switch Inputs/Outputs		10	–	–	–	50	75	–	–	
Feedthrough Capacitance	$C_{in/out}$	–	–	–	–	0.4	–	–	–	pF
Quiescent Current (AL) MC145100	I_{DD}	5	–	200	–	55	110	–	70	μA
		10	–	400	–	115	230	–	100	
		15	–	600	–	170	340	–	200	
MC142100	I_{DD}	5	–	5	–	0.003	5	–	150	μA
		10	–	10	–	0.004	10	–	300	
		15	–	20	–	0.005	20	–	600	
Quiescent Current MC145100	IDD	5	–	250	–	55	150	–	80	μA
(CL, CP Device)		10	–	500	–	115	300	–	150	
		15	–	800	–	170	600	–	300	
MC142100	I_{DD}	5	–	5	–	0.003	5	–	150	μA
		10	–	10	–	0.004	10	–	300	
		15	–	20	–	0.005	20	–	600	
On-State See Figures 6-10	R_{on}	5	–	270	–	250	300	–	375	Ω
Resistance		10	–	140	–	110	170	–	230	
$V_{in} = \frac{V_{DD} - V_{SS}}{2}$		15	–	90	–	85	115	–	145	
On-State Resistance Difference	$\triangle R_{on}$	5	–	–	–	25	30	–	–	Ω
Between Any Two Switches		10	–	–	–	15	25	–	–	
$V_{in} = \frac{V_{DD} - V_{SS}}{2}$ See Figure 6		15	–	–	–	15	20	–	–	
Input/Output Leakage AL	$I_{in/out}$	15	–	±100	–	±0.4	+100	–	±1000	nA
Current, Switch Off CL, CP		15	–	±300	–	±0.4	±300	–	±1000	

* T_{low} = 55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, ±85°C for CL/CP Device.

SWITCHING CHARACTERISTICS ($V_{SS}=0$, $T_A=25°C$, $C_L=50$ pF)

Characteristics		Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times	$V_{SS}=0$ Vdc						
Input to Output		t_{PLH}, t_{PHL}	5	–	30	60	ns
			10	–	15	30	
			15	–	10	20	
Strobe to Output							
Output "1" to High Impedance	MC142100	t_{PLZ}, t_{PHZ}	5	–	350	700	ns
Output "0" to High Impedance			10	–	175	350	
			15	–	125	250	
Output "1" to High Impedance	MC145100	t_{PLZ}, t_{PHZ}	5	–	520	1040	ns
Output "0" to High Impedance			10	–	215	430	
			15	–	140	280	
High Impedance to Output "1"	MC142100	t_{PZH}, t_{PZL}	5	–	300	600	ns
High Impedance to Output "0"			10	–	150	250	
			15	–	80	160	
High Impedance to Output "1"	MC145100	t_{PZH}, t_{PZL}	5	–	550	1100	ns
High Impedance to Output "0"			10	–	200	400	
			15	–	130	260	
Data In to Output	MC142100	t_{PZH}, t_{PHZ}	5	–	300	600	ns
		t_{PZL}, t_{PLZ}	10	–	110	220	
			15	–	75	150	
Data In to Output	MC145100	t_{PZH}, t_{PHZ}	5	–	500	1000	ns
		t_{PZL}, t_{PLZ}	10	–	200	400	
			15	–	120	240	
Address to Output	MC142100	t_{PZH}, t_{PHZ}	5	–	350	700	ns
		t_{PZL}, t_{PLZ}	10	–	135	270	
			15	–	90	180	
Address to Output	MC145100	t_{PZL}, t_{PLZ}	5	–	500	1000	ns
		t_{PZH}, t_{PHZ}	10	–	180	360	
See Figure 2			15	–	115	230	
Minimum Setup Time							
Data In to Strobe	MC142100	t_{su}	5	–	50	190	ns
			10	–	10	50	
			15	–	0	30	
Data In to Strobe	MC145100	t_{su}	5	–	100	200	ns
			10	–	40	80	
			15	–	25	50	
Minimum Hold Time							
Data In to Strobe	MC142100	t_h	5	–	50	250	ns
			10	–	20	150	
			15	–	10	50	
Data In to Strobe	MC145100	t_h	5	–	40	400	ns
			10	–	10	200	
			15	–	0	80	
Minimum Set Up Time	MC142100	t_{su}	5	–	0	180	ns
Address to Strobe	MC145100		10	–	0	50	
			15	–	0	30	ns
Minimum Hold Time	MC142100	t_h	5	–	0	110	ns
Address to Strobe	MC145100		10	–	0	45	
			15	–	0	30	
Minimum Strobe Pulse Width	MC142100	t_{WH}	5	–	150	320	ns
	MC145100		10	–	50	160	
			15	–	40	80	

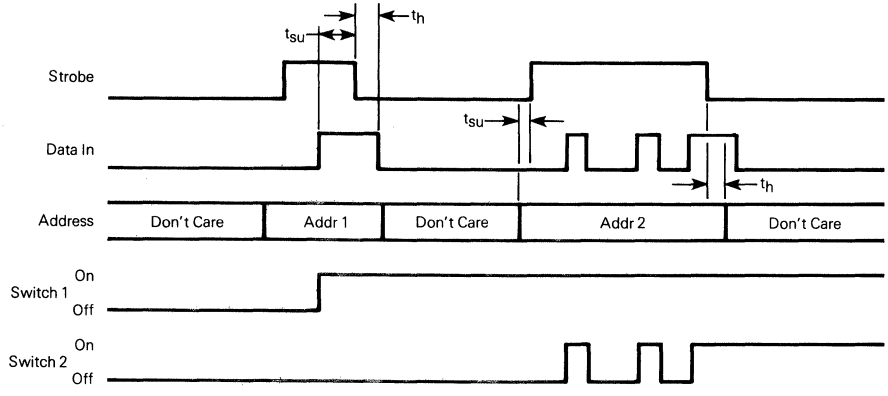
2

SWITCHING CHARACTERISTICS (continued) ($V_{SS}=0$, $T_A=25°C$, $C_L=50$ pF)

Characteristics		Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Sine Wave Distortion ($R_L=1$ kΩ, f=1 kHz)	See Figure 3	–	10	–	0.5	–	%
Frequency Response (Switch On) ($R_L=1$kΩ, 20 Log_{10} $V_{out}/V_{in}=-3.0$ dB)	See Figure 3	–	10	–	15	–	MHz
Feedthrough Attenuation (Switch Off) ($V_{in}=10$ V_{PP}, F=1.6 kHz, $R_L=1$ kΩ, $C_L=15$ pF)	See Figure 3	–	10	–	−80	–	dB
Frequency for Signal Crosstalk ($V_{in}=10$ V_{PP}, Switch A	−40 dB	–	10	–	1500	–	kHz
On, Switch B Off, $R_L=1$ kΩ, $C_L=15$ pF)	−110 dB See Figure 4	–	–	–	0.1	–	kHz
Crosstalk Controls to Output ($R_L=10$ kΩ)	See Figure 5	–	10	–	70	–	mV

Address				Switch Selected		MC145100 Only Switches Cleared			Address				Switch Selected		MC145100 Only Switches Cleared		
A	B	C	D						A	B	C	D					
0	0	0	0	C1R1	0	1	2	3	0	0	0	1	C1R3	8	9	10	11
1	0	0	0	C2R1	1	0	2	3	1	0	0	1	C2R3	9	8	10	11
0	1	0	0	C3R1	2	0	1	3	0	1	0	1	C3R3	10	8	9	11
1	1	0	0	C4R1	3	0	1	2	1	1	0	1	C4R3	11	8	9	10
0	0	1	0	C1R2	4	5	6	7	0	0	1	1	C1R4	12	13	14	15
1	0	1	0	C2R2	5	4	6	7	1	0	1	1	C2R4	13	12	14	15
0	1	1	0	C3R2	6	4	5	7	0	1	1	1	C3R4	14	12	13	15
1	1	1	0	C4R2	7	4	5	6	1	1	1	1	C4R4	15	12	13	14

TIMING DIAGRAM
MC145100/MC142100



TEST CIRCUITS

FIGURE 1 — INPUT VOLTAGE

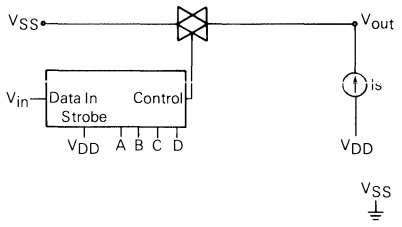


FIGURE 2 — PROPAGATION DELAY TIME

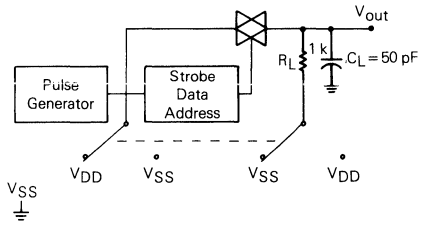


FIGURE 3 — BANDWIDTH AND FEEDTHROUGH ATTENUATION

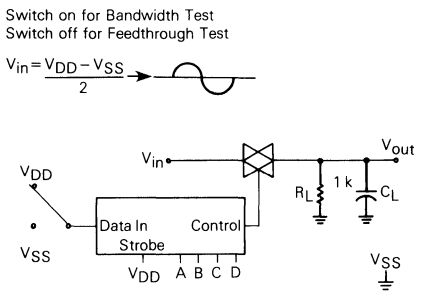


FIGURE 4 — CROSSTALK BETWEEN ANY TWO SWITCHES

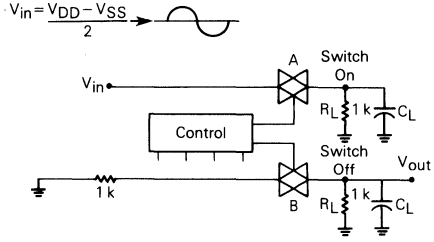


FIGURE 5 — CROSSTALK CONTROL TO OUTPUT

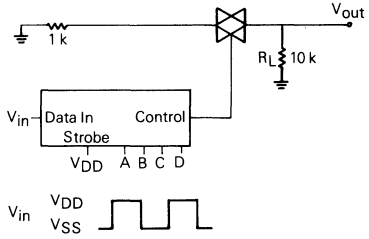


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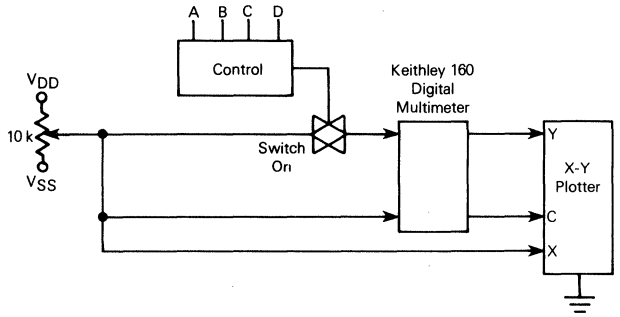
FIGURE 6 — CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 7 — COMPARISON AT 25°C

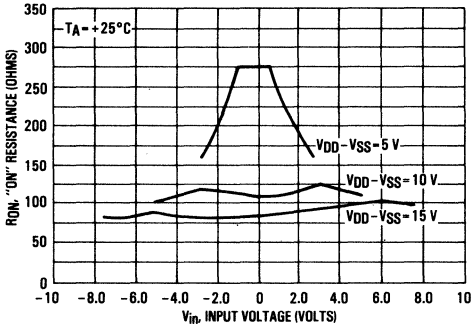


FIGURE 8 — V_{DD} = 2.5 V, V_{SS} = −2.5 V

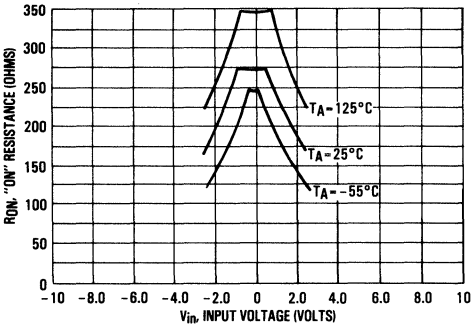


FIGURE 9 — V_{DD} = 5.0 V, V_{SS} = −5.0 V

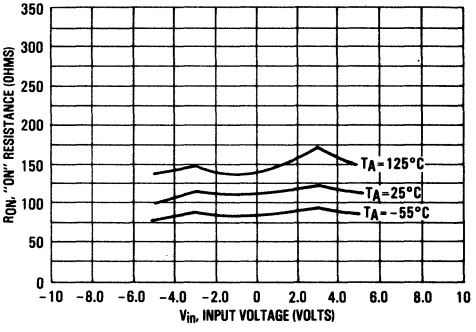
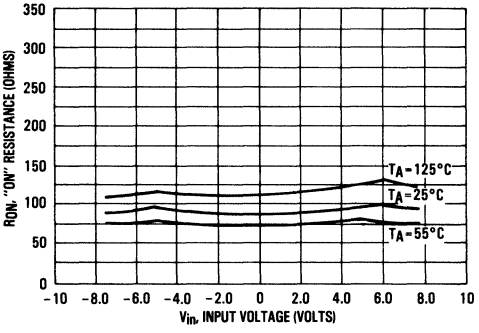


FIGURE 10 — V_{DD} = 7.5 V, V_{SS} = −7.5 V



MC143403
MC143404

Advance Information

CMOS MSI

QUAD LINE DRIVER

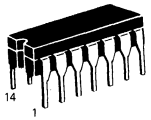
2

QUAD LINE DRIVER

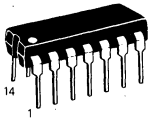
The MC143403 and MC143404 are low power, quad line drivers with true differential inputs. The device has electrical characteristics similar to the popular LM324 and MC3403. However, the MC143403 has several distinct advantages over standard operational amplifier types. The low power quad driver, MC143403, draws only 1.5 mA (typ) and the micro power quad driver, MC143404, draws only 400 μA (typ) and provides high output drive capabilities. The common mode rejection ratio is typically 80 dB.

These units are excellent building blocks for communications, consumer, industrial and instrument applications where low power is required, particularly in telecommunications equipment. These units are useful in both battery operated communications systems and phone line powered equipment.

- Low Power and Micropower Communication Devices
- True Differential Input Stage
- Single or Split Supply Operation
- High Input Impedance
- Very Low Input Bias Current: 1 nA
- Four Drivers per Package
- Pinout Compatible with LM324 and MC3403
- Wide Input Voltage Range
- High Output Current Drive, MC143403
- Typical Input Offset Voltage: 10 mV



L SUFFIX
CERAMIC PACKAGE
CASE 632



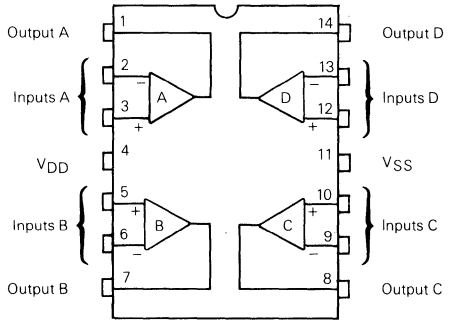
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXX

Suffix	Denotes
L	Ceramic Package
P	Plastic Package

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +15	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	V_{DD}	+4.75 to +12.6	V

ELECTRICAL CHARACTERISTICS (V_{SS}=0 V, T_A=0 to 70°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	10	–	10	±30	mV
Input Offset Current	I_{IO}	10	–	–	200	pA
Open Loop Voltage Gain, MC143404 Only, R_L = 10 kΩ	A_{VOL}	12 10 5	60 60 60	70 70 70	– – –	dB
Open Loop Voltage Gain, MC143403 Only, R_L = 600 Ω		10	45	55	–	
Common Mode Rejection Ratio	CMRR	10	50	60	–	dB
Input Bias Current	I_{IB}	10	–	–	1	nA
Output Voltage Range MC143404: R_L = 10 kΩ MC143403: R_L = 600 Ω	V_{OR}	12 10 5	1.0 1.0 1.0	– – –	10.0 8.5 4.0	V
Input Common Mode Voltage Range	V_{ICR}	12 10 5	0 0 0	– – –	10 8 3	V
Power Supply Current, MC143403	I_{DC}	12 5	– –	1.5 1.5	3.0 3.0	mA
Power Supply Current, MC143404	I_{DC}	12	–	0.4	0.8	

ELECTRICAL CHARACTERISTICS (V_{SS}=0 V, T_A=0 to 70°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Small Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	10	–	500	–	kHz
Slew Rate MC143404: A_V = 1, R_L = 10 kΩ, 200 pF MC143403: R_L = 600 Ω, 200 pF	SR	 10 10	 – –	 1 1.5	 – –	V/μs
Phase Margin MC143404: A_V = 1, R_L = 10 kΩ, 200 pF MC143403: R_L = 600 Ω, 200 pF	ϕ_m	10	–	75	–	deg
Power Supply Rejection Ratio	PSRR	10	–	60	–	dB
Average Temperature Coefficient of V_{IO}		10	–	20	–	μV/°C

FIGURE 1 — TYPICAL OPEN LOOP FREQUENCY RESPONSE

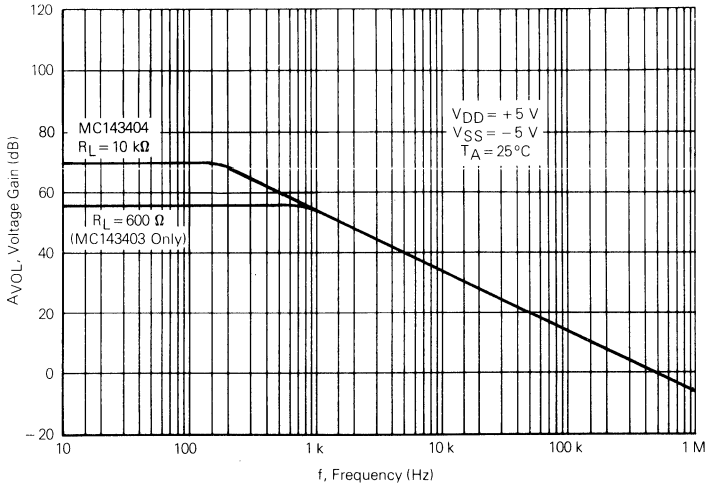


FIGURE 2 — TYPICAL POWER BANDWIDTH
(Large Signal Swing vs. Frequency)

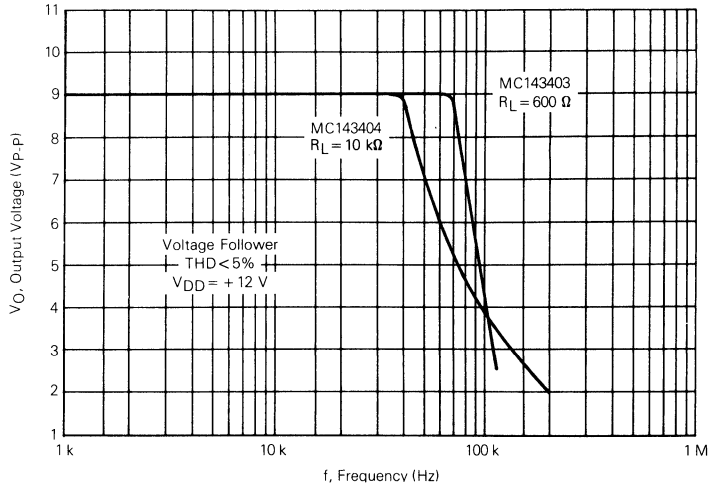


FIGURE 3 — GENERAL PURPOSE DUPLEXER (2-Wire to 4-Wire Converter)

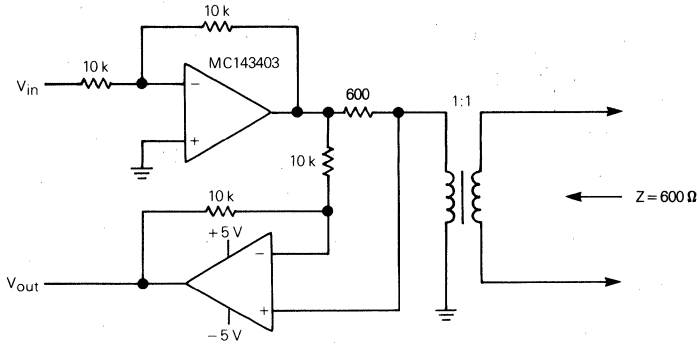
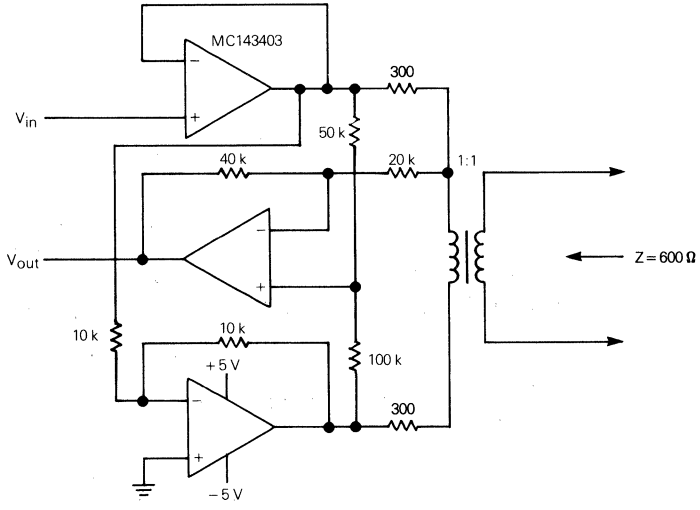


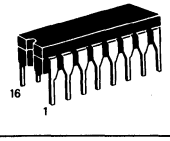
FIGURE 4 — HIGH POWER DUPLEXER (2-Wire to 4-Wire Converter)



MC145402

Advance Information

Serial 13-Bit Linear Codec (A/D and D/A)



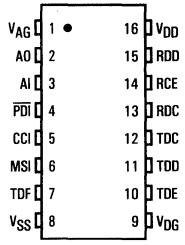
L SUFFIX
CERAMIC
CASE 620

2

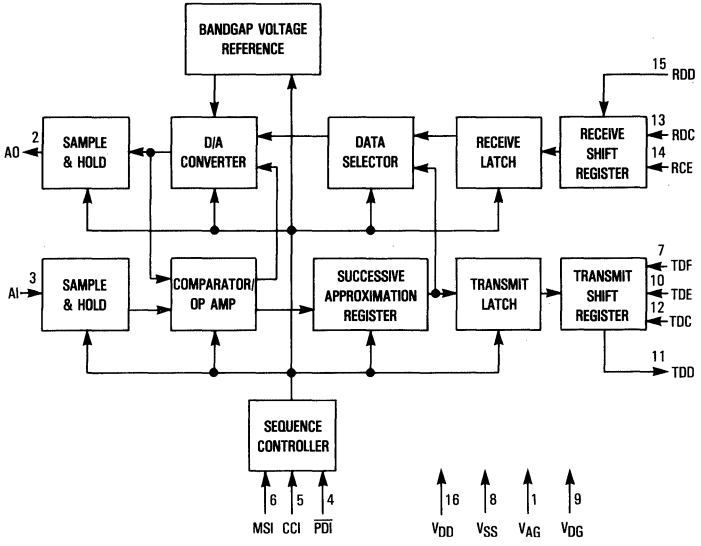
The MC145402 is a 13-bit linear monotonic digital-to-analog and analog-to-digital converter implemented in a single silicon-gate CMOS IC. Potential applications include analog interface for Digital Signal Processor (DSP) applications, high speed modems, telephone systems, SONAR, Adaptive Differential Pulse Code Modulation (ADPCM) converters, echo cancellers, repeaters, voice synthesizers, and music synthesizers.

- 60 dB Signal-to-(Noise Plus Distortion) Ratio Typical
- On-Chip Precision Voltage Reference
- Serial Data Ports
- 2's Complement Coding
- ±5 Volt Supply Operation
- Sample Rates from 100 Hz to 16 kHz (Both A/D and D/A), 100 Hz to 21.3 kHz (A/D Only), and 100 Hz to 64 kHz (D/A Only)
- Input Sample and Hold Provided On-Chip
- 5 Volt CMOS Inputs; Outputs Capable of Driving Two LSTTL Loads
- Available in a 16-Pin DIP
- Low Power Consumption: 50 mW Typical, 1 mW Power Down

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	−0.5 to 11	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on analog inputs/outputs and $V_{DG} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on digital inputs/outputs. Reliability of operation is enhanced if unused digital inputs are tied to an appropriate logic voltage level (e.g., either V_{DG} or V_{DD}) and unused analog inputs are tied to V_{AG}.

RECOMMENDED OPERATING CONDITIONS

Parameter		Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage		V_{DD} to V_{SS}	9.5	10	10.5	V
Power Dissipation, $\overline{PDI}=1$		V_{DD} to V_{SS}	–	50	80	mW
Power Dissipation, $\overline{PDI}=0$		V_{DD} to V_{SS}	–	1	5	mW
Conversion Rate	Full Cycle A/D and D/A	MSI	0.1	–	16	kHz
	Short Cycle A/D		0.1	–	21.3	
	Short Cycle D/A		0.1	–	64	
Conversion Sequence Rate		CCI	3.2	–	512	kHz
Data Rate		TDC, RDC	$16 \times f_{MSI}$	–	4096	kHz
Full Scale Analog Levels (Referenced to 600 Ω)		AI, AO	–	3.27	–	Vp
			–	9.5	–	dBm

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD}=5 V, V_{SS}=−5 V, $V_{AG}=V_{DG}$=0 V, T_A=0 to 70°C)

Characteristic			Symbol	Min	Max	Unit
High Level Input Voltage			V_{IH}	3.5	–	V
Low Level Input Voltage			V_{IL}	–	1.5	V
Input Current			I_{in}	–	±1.0	μA
Input Capacitance			C_{in}	–	10	pF
High Level Output Voltage	TDD	I_{out}=−20 μA	V_{OH}	4.9	–	V
		I_{out}=−1 mA		4.3	–	
Low Level Output Voltage	TDD	I_{out}=20 μA	V_{OL}	–	0.1	V
		I_{out}=2 mA		–	0.4	

CODER AND DECODER PERFORMANCE (V_{DD}=5 V ±5%, V_{SS}=−5 V ±5%, $V_{AG}=V_{DG}$=0 V, 0 dBm0=1.60 Vrms=6.30 dBm (600 Ω), T_A=0 to 70°C, MSI=TDE=RCE=8 kHz, TDC=RDC=2.048 MHz, CCI=256 kHz)

Characteristic		Coder (A/D)			Decoder (D/A)			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution		13	–	13	13	–	13	Bits
Conversion Time	Full Cycle A/D and D/A	62.5	–	10,000	62.5	–	10,000	μs
	Short Cycle A/D	46.9	–	10,000	–	–	–	
	Short Cycle D/A	–	–	–	15.6	–	10,000	
Differential Nonlinearity		–	–	±1	–	–	±1	LSB
Gain Error		−0.35	–	+0.35	−0.35	–	+0.35	dB
Offset		−15	–	+15	–	–	–	LSB
		–	–	–	−20	–	+20	mV
Idle Channel Noise, 3 kHz Lowpass		–	15	–	–	11	–	dBrn0
Signal-to-Noise Ratio	3.2 dBm0	–	61	–	–	62	–	dB
(Referenced to 1.02 kHz through	0 dBm0	–	60	–	–	60	–	
a $f_{MSI}/2$ Lowpass Filter)	−10 dBm0	–	57	–	–	59	–	
	−20 dBm0	–	50	–	–	52	–	
	−30 dBm0	–	40	–	–	42	–	
	−40 dBm0	–	30	–	–	32	–	
	−50 dBm0	–	20	–	–	22	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ±5%, V_{SS} = −5 V ±5%, V_{AG} = V_{DG} = 0 V, 0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input Current	AI	I_{in}	—	0.01	±1	μA
AC Input Impedance	AI	Z_{in}	0.5	—	—	MΩ
Input Capacitance	AI	C_{in}	—	—	15	pF
Output Voltage Range	AO	V_{out}	−3.4	—	3.4	V
Power Supply Rejection Ratio (100 mV RMS on V_{DD} or V_{SS}, 0-50 kHz)	AO, TDD	PSRR	—	40	—	dB
Crosstalk, AI to AO and RDD to TDD referenced to 0 dBm0 @ 1.02 kHz	AO, TDD	—	—	−90	−75	dB
Slew Rate	AO	SR	1.5	3	—	V/μs
Settling Time (Full Scale)	AO	t_{settle}	—	8	—	μs

SWITCHING CHARACTERISTICS

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C, C_L = 50 pF, See Figure 1)

Characteristic		Symbol	Min	Max	Unit
Input Rise Time	RCE, RDC, TDC, TDE, CCI, MSI	t_r	—	100	ns
Input Fall Time	RCE, RDC, TDC, TDE, CCI, MSI	t_f	—	100	ns
Output Rise Time	TDD	t_r	—	80	ns
Output Fall Time	TDD	t_f	—	80	ns
Pulse Width High	RDC, MSI, CCI, TDC, RCE	t_{wH}	100	—	ns
Pulse Width Low	TDE, MSI, TDC, RCE, RDC	t_{wL}	100	—	ns
CCI Pulse Width Low		t_{wL}	500	—	ns
MSI Clock Frequency		f_{MSI}	0.1	64	kHz
CCI Clock Frequency		f_{CCI}	3.2	512	kHz
TDC and RDC Clock Frequency		f_{DC}	16 × f_{MSI}	4.1	MHz
TDC Rising Edge to TDD Data Valid During TDE High		t_{p1}	—	150	ns
TDE Rising Edge to TDD Data Valid During TDC High		t_{p2}	—	150	ns
TDE Rising Edge to TDD Low Impedance Propagation Delay		t_{p3}	0	100	ns
TDE Falling Edge to TDD High Impedance Propagation Delay		t_{p4}	—	40	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su1} t_{su2}	20 100	— —	ns
RDC Bit 0 Falling Edge to Last CCI Falling Edge Prior to MSI		t_{su3}	20	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su4} t_{su5}	20 100	— —	ns
Last CCI Rising Edge (Prior to MSI) to TDE Rising Edge		t_{su6}	100	—	ns
Last CCI Rising Edge (Prior to MSI) to First TDC Rising Edge		$t_{su6'}$	100	—	ns
First TDC Falling Edge to Last CCI Rising Edge Prior to MSI		t_{su7}	0	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su8} t_{su9}	20 100	— —	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su10}	60	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	ns

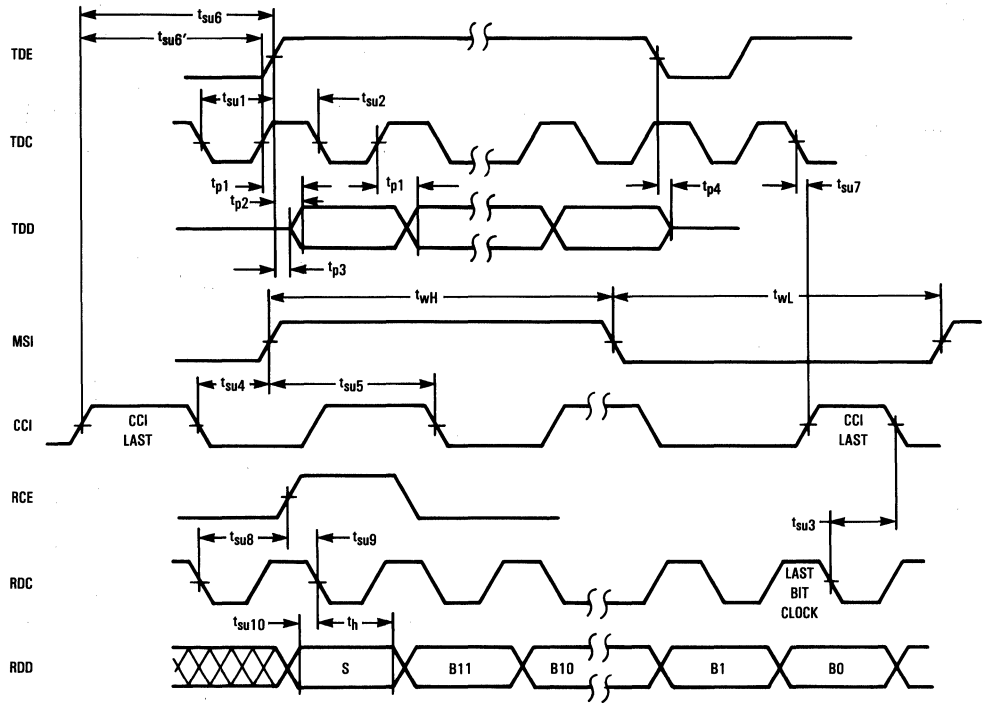


Figure 1. AC Timing Diagram

PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY (PIN 16)

The most positive power supply, typically +5 volts in split power supply configurations or +10 volts in single supply systems.

V_{SS}—NEGATIVE SUPPLY (PIN 8)

The most negative power supply, typically −5 volts in split power supply configurations or 0 volts in single supply systems.

V_{AG}—ANALOG GROUND (PIN 1)

This is the analog signal reference point. This pin is normally tied to 0 volts in split supply operation or $V_{DD}/2$ in single supply systems.

V_{DG}—DIGITAL GROUND (PIN 9)

This is the ground reference for all of the digital input and output pins. CMOS compatible logic signals swing from V_{DG} to V_{DD} where V_{DG} can be established anywhere from $V_{DD}-4.75$ volts to V_{SS}.

AO—ANALOG OUTPUT (PIN 2)

This is the output of the decoder's sample and hold circuit and is a 100 percent duty cycle analog output of the last digital word received and decoded by the decoder. The analog output is updated approximately 60 nanoseconds after the rising edge of the last CCI prior to MSI. See Figure 2. AO is capable of driving a 10 kilohm, 50 picofarad load.

AI—ANALOG INPUT (PIN 3)

This is the high impedance input to the coder. An A/D cycle begins on the first falling edge of CCI following the rising edge of MSI. The AI input is sampled approximately 50 nanoseconds after the rising edge of CCI prior to the start of the A/D cycle.

$\overline{PDI}$—POWER DOWN INPUT (PIN 4)

In normal operation this input should be tied high. A logic low on this input puts the device into a minimum power dissipation mode. During power down, all functions stop. Two complete MSI conversion cycles are required to establish normal operation after leaving the power down mode.

CCI—CONVERT CLOCK INPUT (PIN 5)

This input controls the complete conversion sequence during one MSI cycle and must receive a clock which is 32 times the frequency of MSI. The only exception to 32 times the frequency of MSI is during short-cycle operation. See **Modes of Operation**. CCI must be synchronous and approximately rising edge aligned with MSI.

MSI—MASTER SYNC INPUT (PIN 6)

This pin determines the conversion rate for both the coder and the decoder. One A/D and D/A conversion takes place during each period of the digital clock applied to this input (except in short-cycle operation, see **Modes of Operation**). MSI must be synchronous and approximately rising edge aligned with CCI.

TDC—TRANSMIT DATA CLOCK (PIN 12)

Digital data from the coder is serially transmitted from TDD on rising TDC edges whenever TDE is a logic high. TDC must be approximately rising edge aligned with TDE. Generally, if TDC is low when TDE rises, the first rising edge of TDC clocks the first data bit. If TDC is high when TDE rises, the first bit will be clocked by TDE and the first rising edge of TDC after TDE rises will clock out the second data bit.

TDE—TRANSMIT DATA ENABLE (PIN 10)

This pin is used to initiate the serial transfer of data from the coder and provides three-state control of the TDD pin. The rising edge of TDE (or TDC if it follows TDE) signals the start of data transfer from the TDD pin. A resulting high logic level on TDE also releases TDD from its high-impedance state. TDE must remain high throughout the data transfer to keep TDD in the low impedance state and must return to a low state prior to each data transfer. If TDE remains high for more than 16 TDC clocks, the 16 bits of TDD data will be recirculated. (Note: The A/D cycle begins on the first falling edge of CCI after the rising edge of MSI. The internal transmit latch is updated one and one half CCI periods prior to the start of the A/D cycle. A pulse generated by the logical AND of TDE and the first TDC transfers data to the transmit shift register, and this pulse must not occur when the transmit latch is updated. See Figure 2 and see t_{su6}, $t_{su6'}$, and t_{su7} of Figure 1.)

TDD—TRANSMIT DIGITAL DATA (PIN 11)

This is the three-state output data pin from the coder and is controlled by the TDE and TDC pins. TDD is in the high-impedance state whenever TDE is a logic low. The first data bit is output from TDD on the rising edge of TDE (or TDC if it follows TDE) and each subsequent bit is output on rising edges of TDC. Two output data formats are available as described in the TDF pin description below.

TDF—TRANSMIT DATA FORMAT (PIN 7)

The 13-bit digital output of the coder is available in one of two sixteen-bit two's complement formats as determined by the state of this pin. A logic zero at this pin causes the data from TDD to be in a 16-bit sign-extended format as follows: SSSSM . . . L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. A logic one on this pin formats the data as follows: SM . . . LSSS. See Figure 3. RDD data is not affected by the state of this pin and if a "digital loopback" is needed (TDD data looped back into RDD), this pin should be high.

RDC—RECEIVE DATA CLOCK (PIN 13)

Receive digital data is accepted by the decoder on the first 13 falling edges of RDC after an RCE rising edge.

RCE—RECEIVE CLOCK ENABLE (PIN 14)

This pin identifies the beginning of a data transfer into the RDD pin of the decoder. The first 13 falling edges of RDC after an RCE rising edge will clock data into the decoder data input, RDD. RCE must return low prior to each data transfer. Since receive data is latched into the receive latch on the last CCI falling edge prior to MSI, data transfers may not span this falling edge of CCI without loss of data.

RDD—RECEIVE DIGITAL DATA (PIN 15)

This pin is the data input to the decoder and is controlled by the RDC and RCE pins described above. Two's complement data are loaded in the following sequence: SM . . . L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. Only the first 13 bits clocked by RDC after RCE rises will be accepted for decoding. Any additional bits will be ignored. See Figure 3.

GENERAL INFORMATION

MODES OF OPERATION—GENERAL

The MC145402 has three modes of operation; a "full" cycle mode and two "short" cycle modes. The full cycle mode allows simultaneous analog to digital (A/D) and digital to analog (D/A) operation. The short cycle modes allow either A/D only or D/A only operation. Two MSI cycles are required for the MC145402 to detect which operating mode has been selected. See Figure 2 for full versus short cycle clocking.

FULL CYCLE OPERATION

When operating in the full cycle mode, the MC145402 performs a 13-bit A/D conversion followed by a 13-bit D/A conversion. Full cycle operation is selected by using a CCI frequency that is 32 times the frequency of MSI. MSI is the sample rate frequency.

SHORT CYCLE ANALOG TO DIGITAL OPERATION

If CCI is 24 times the frequency of MSI, short cycle analog to digital operation is selected. This allows a 13-bit A/D conversion only. In this mode, the D/A is not operational and any data applied to the RDD input is ignored.

SHORT CYCLE DIGITAL TO ANALOG OPERATION

Short cycle digital to analog operation is selected by using a CCI clock frequency that is eight times the MSI sample rate. During short cycle D/A operation, A/D operation is disabled and digital data read from TDD is not valid.

2

CLOCKING RECOMMENDATIONS

For optimum differential nonlinearity performance, all data transitions on TDD and RDD should be limited to the first four CCI cycles following the rising edge of MSI. This may be achieved by setting MSI = TDE = RCE having a duration of 16 data clock cycles, and TDC = RDC ≥ 4 × CCI clock frequency. Figure 6 shows a circuit that generates this clocking configuration; see **APPLICATION CIRCUITS**.

SIGNAL TO DISTORTION RATIO

Figures 4 and 5 show graphs of typical signal to distortion ratios versus signal level for the MC145402. The presented data is referenced to a 1020 hertz input sinusoidal frequency with signal levels referenced to 600 ohms and transmission level point adjusted (e.g., 0 dBm0 at 600 ohms with a TLP of 6.30 dB is 4.53 volts peak to peak). For comparison, ideal signal to noise ratios for 9-, 10-, 11-, 12-, and 13-bit A/D and D/A converters are also shown. The equation used for an ideal RMS to RMS signal to distortion ratio is:

$$S/D = N \times 6\ dB + 1.76\ dB$$

where N is the number of bits of resolution, 6 dB per bit, and $1.76 = 20\log(\sqrt{3}/\sqrt{2})$.

$(\sqrt{3}/\sqrt{2})$ is approximately the RMS to RMS ratio of a sine wave to white noise.

The signal to noise plus distortion ratio is measured through a brickwall low-pass filter set to the Nyquist frequency of the A/D and D/A sample rate. For an 8 kilohertz sample rate, the low-pass filter is set to block all signals above 4 kilohertz.

APPLICATION CIRCUITS

Figure 6 shows a typical circuit for generating the clock frequencies for the MC145402. This circuit uses an MC74HC4040 and a 2.048 megahertz crystal to generate the 256 kilohertz frequency for internal sequencing, 1.024 megahertz for the data clocks, and an 8 kilohertz sample frequency. A 4.096 megahertz crystal could be used for a sample rate of 16 kilohertz.

Figure 7 shows the MC145402 interfaced to the DSP56000 digital signal processor. The DSP56000 can internally generate the clocks for the MC145402 using the SSI serial interface. SCK provides the sequencing and data clocks (non-gated continuous clock) and SC2 (setup as the Frame Sync Out, FSL = 0) provides the sample rate and data enables for the MC145402. The divide-by-four circuit to generate the CCI clock is recommended for optimum MC145402 performance, and allows the DSP56000 to clock data in and out of the MC145402 quickly, leaving time available for processing by the DSP before another sample is available. SC0 and SC1 could be used to gate the enables to select up to four devices on the SSI bus.

TELEPHONE SYSTEM TRANSMISSION LEVEL POINT FOR A LINEAR A/D OR D/A CONVERTER REFERENCED TO MU-LAW COMPANDING

Mu-law companding, as specified by AT&T and CCITT, requires 8159 quantization levels to implement both A/D and D/A conversion schemes. This is to be mirrored about signal ground for the negative part of the wave form.

To implement a 13-bit (±12-bit) linear converter scheme requires 8192 quantization levels mirrored about signal ground. To specify this converter such that it can be used to interface with, or as an alternative to, telephony based Mu-law applications, the following is an explanation of the gain translation.

A 13-bit linear converter scheme has 8192 quantization levels. The goal is to be able to convert between these two encoding schemes with minimal distortion. This dictates setting the LSBs to the same level. For this to be achieved requires the reference voltage of the linear converter to be 8192/8159 times the reference voltage of the Mu-law converter. The peak amplitude of a Mu-law converter is 3.17 dBm0. The peak level of the linear converter will be 8192/8159 times the peak level of the Mu-law converter, which is $8192/8159 \times 3.17$ dBm0. However, you cannot multiply a gain factor by a dBm value without using common term units and math; i.e., we must convert this gain factor to a dB equivalent which is:

$$20 \log_{10} (8192/8159) = 0.03\ dB$$

With the gain factor in dB, we can add it to the Mu-law peak level:

$$3.17\ dBm0 + 0.03\ dB = 3.20\ dBm0$$

Therefore, the linear converter peak level is 3.20 dBm0.

This is another way of saying the 0 dBm0 level for the linear converter is 3.20 dB below the maximum amplitude.

To determine the absolute 0 dBm0 level for the linear converter from the peak level, we calculate the peak level in dBm by:

$$10 \log_{10} \frac{(3.27\ VpK/\sqrt{2})^2/(600\ ohm)}{1\ mW} = 9.50\ dBm\ (600\ ohm)$$

and 3.20 dB below this level is the 0 dBm0 absolute amplitude, which is

$$9.50\ dBm - 3.20\ dB = 6.30\ dBm\ (600\ ohm)$$

Therefore, the calibration level, or transmission level point (TLP), for this part is 6.30 dBm (600 ohm), which is 1.6 Vrms based on the reference voltage of 3.27 V.

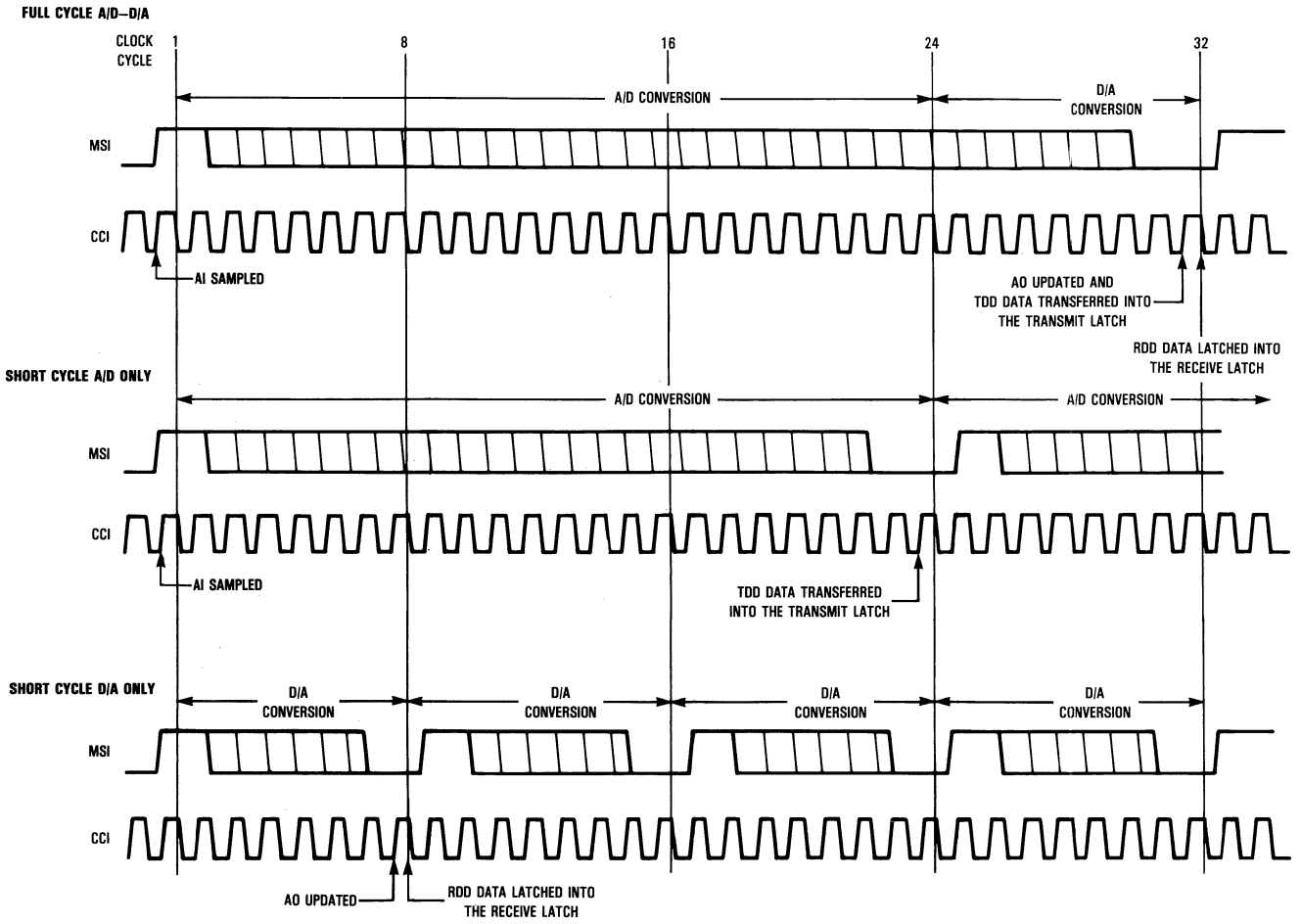


Figure 2. MC145402 Full and Short Cycle Timing

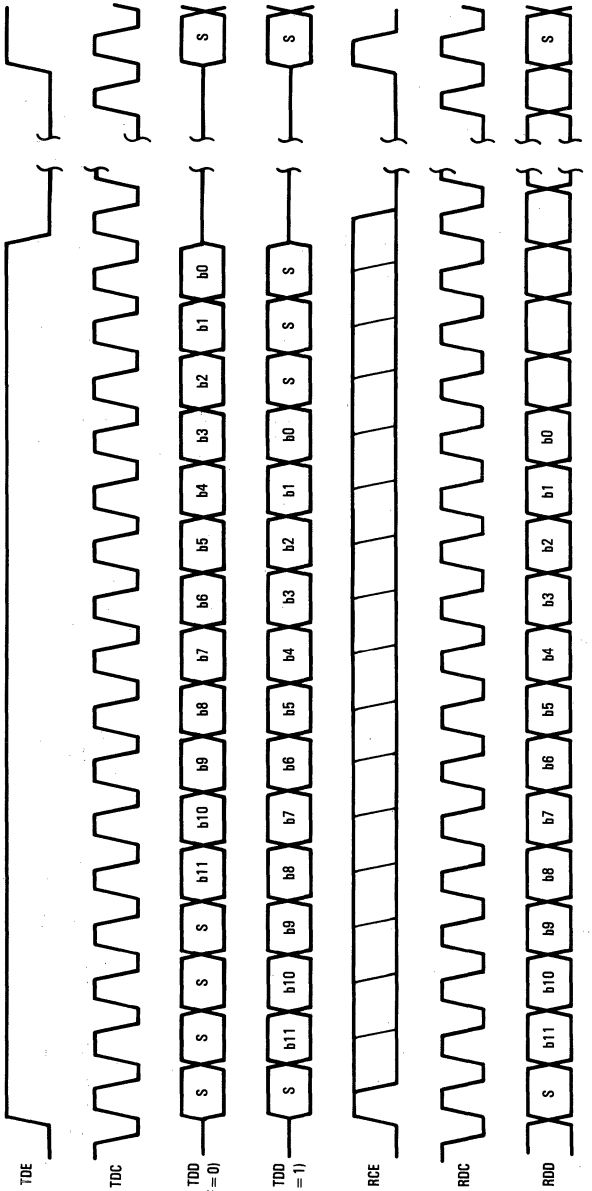


Figure 3. MC145402 Digital Data Timing

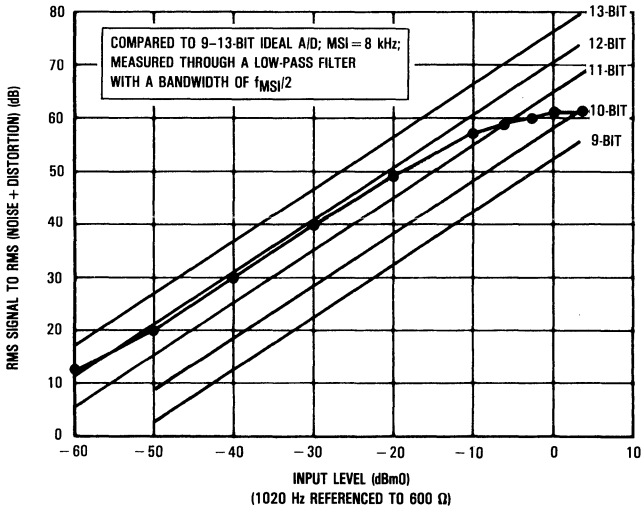


Figure 4. MC145402 Encoder (A/D) Signal to Noise Plus Distortion Ratio

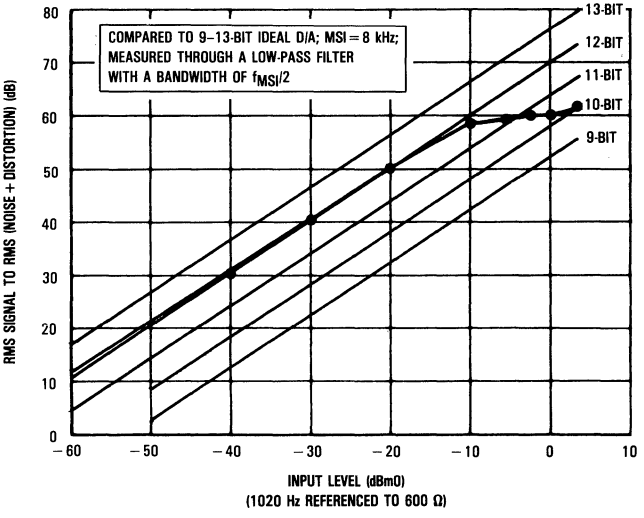


Figure 5. MC145402 Decoder (D/A) Signal to Noise Plus Distortion Ratio

2

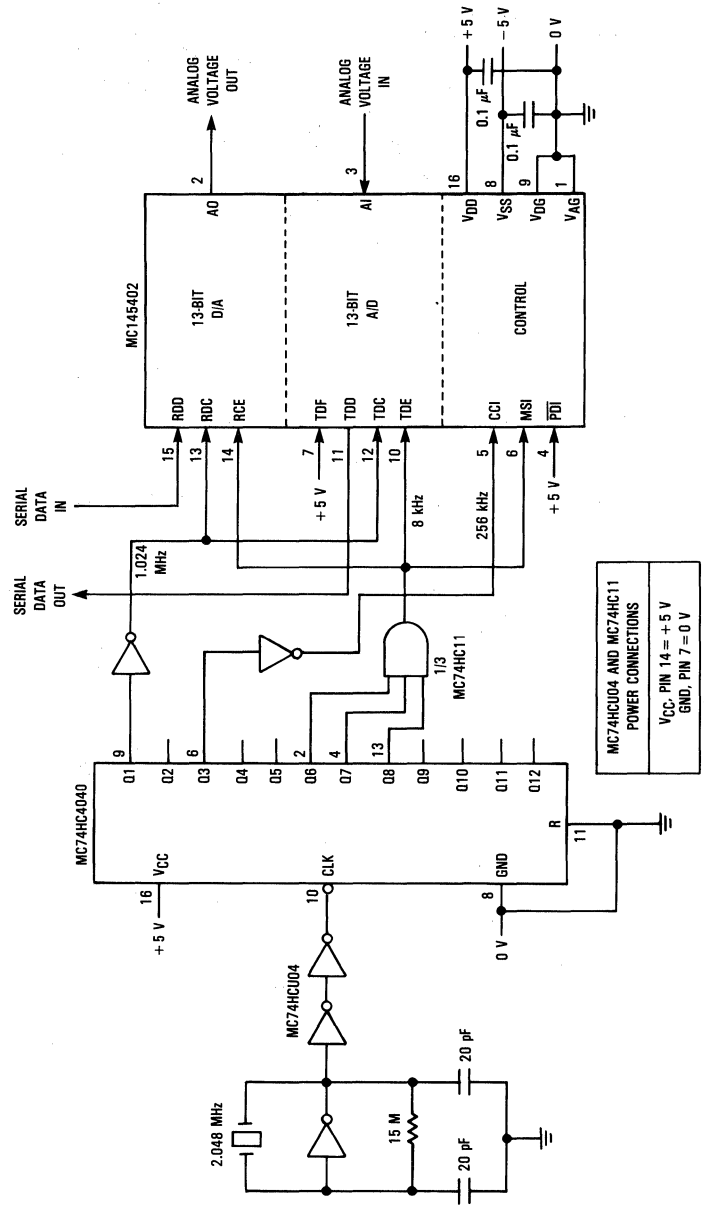


Figure 6. Typical MC145402 Configuration

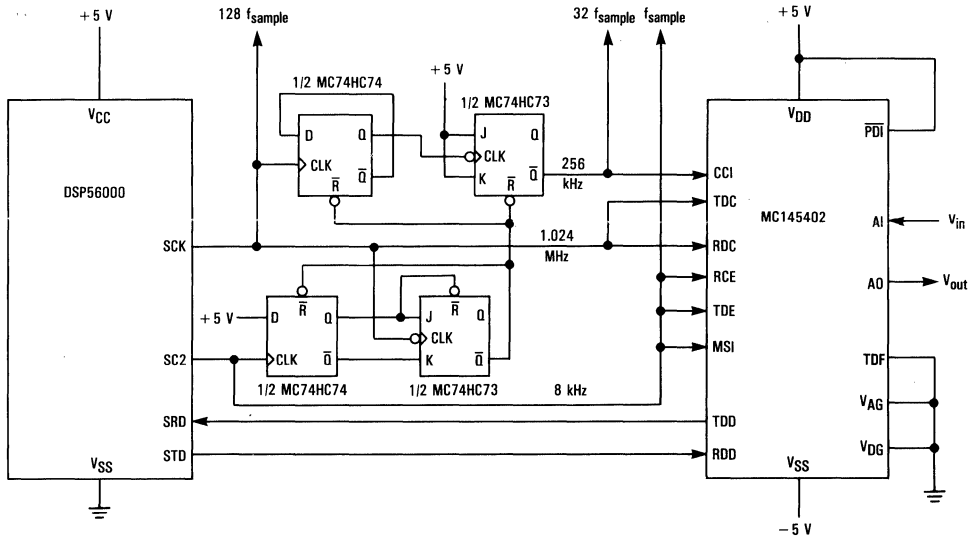


Figure 7. The MC145402, 13-Bit Linear Codec, Interfaced to a Motorola DSP56000, Digital Signal Processor, SSI Port

MC145406

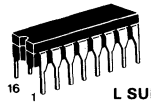
EIA-232-D/V.28 Driver/Receiver
(Formerly RS-232-C)

2

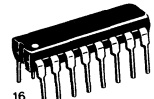
The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate-limited output, 300 ohms power-off source impedance, and output typically switching to within 25 percent of the supply rails. The receivers can handle up to ±25 volts while presenting 3 to 7 kilohms impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

Drivers
- ±5 to ±12 V Supply Range
- 300 Ohms Power-Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Maximum Slew Rate = 30 V/μs

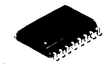
Receivers
- ±25 V Input Voltage Range When V_{DD} = 12 V, V_{SS} = −12 V
- 3 to 7 Kilohms Input Impedance
- Hysteresis on Input Switchpoint



L SUFFIX
CASE 620
CERAMIC

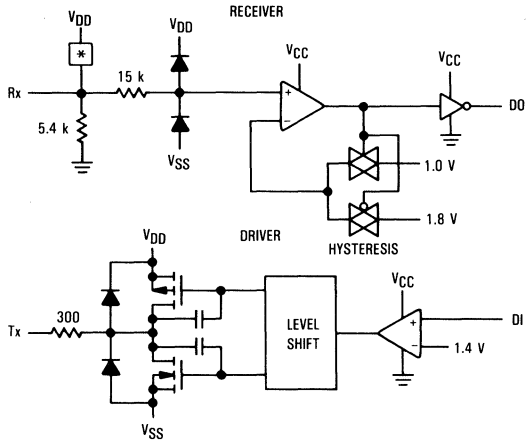


P SUFFIX
CASE 648
PLASTIC



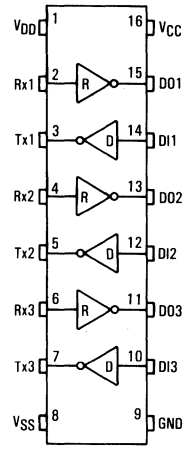
DW SUFFIX
CASE 751G
SOIC

FUNCTION DIAGRAM



*Protection circuit

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	−0.5 to +13.5 +0.5 to −13.5 −0.5 to 6.0	V
Input Voltage Range Rx1-3 Inputs DI1-3 Inputs	V_{IR}	 (V_{SS} − 15) to (V_{DD} + 15) −0.5 to (V_{CC} + 0.5)	V
DC Current Per Pin		±100	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{DD}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15\ V) \leq V_{Rx1\text{-}3} \leq (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \leq V_{Tx1\text{-}3} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = −40 to 85°C)

Parameter	Symbol	MC145406 Min	MC145406 Typ	MC145406 Max	Unit
DC Supply Voltage					V
V_{DD}	V_{DD}	4.5	5 to 12	13.2	
V_{SS}	V_{SS}	−4.5	−5 to −12	−13.2	
V_{CC} ($V_{DD} \geq V_{CC}$)	V_{CC}	4.5	5.0	5.5	
Quiescent Supply Current (Outputs unloaded, inputs low)					μA
V_{DD} = +12 V	I_{DD}	—	140	400	
V_{SS} = −12 V	I_{SS}	—	340	600	
V_{CC} = +5 V	I_{CC}	—	300	450	

RECEIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{DD} = +5 to +12 V, V_{SS} = −5 to −12 V, $V_{DD} \geq V_{CC}$, T_A = −40 to 85°C)

Characteristic		Symbol	MC145406 Min	MC145406 Typ	MC145406 Max	Unit
Input Turn-on Threshold $V_{DO1\text{-}3} = V_{OL}$, V_{CC} = 5.0 V ±5%	Rx1-3	V_{on}	1.35	1.80	2.35	V
Input Turn-off Threshold $V_{DO1\text{-}3} = V_{OH}$, V_{CC} = 5.0 V ±5%	Rx1-3	V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis V_{CC} = 5.0 V ±5%	Rx1-3	V_{on}-V_{off}	0.6	0.8	—	V
Input Resistance (V_{SS} − 15 V) ≤ $V_{Rx1\text{-}3}$ ≤ (V_{DD} + 15 V)	Rx1-3	R_{in}	3.0	5.4	7.0	kΩ
High-Level Output Voltage $V_{Rx1\text{-}3}$ = −3 V to (V_{SS} − 15 V)*	DO1-3	V_{OH}				V
I_{OH} = −20 μA, V_{CC} = +5.0 V			4.9	4.9	—	
I_{OH} = −1 mA, V_{CC} = +5.0 V			3.8	4.3	—	
Low-Level Output Voltage $V_{Rx1\text{-}3}$ = +3 V to (V_{DD} + 15 V)*	DO1-3	V_{OL}				V
I_{OL} = +20 μA, V_{CC} = +5.0 V			—	0.01	0.1	
I_{OL} = +2 mA, V_{CC} = +5.0 V			—	0.02	0.5	
I_{OL} = +4 mA, V_{CC} = +5.0 V			—	0.5	0.7	

*This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

2

DRIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{CC} = +5 V ±5%, T_A = −40 to 85°C)

Characteristic		Symbol	MC145406 Min	MC145406 Typ	MC145406 Max	Unit
Digital Input Voltage	DI1-3					V
Logic 0		V_{IL}	–	–	0.8	
Logic 1		V_{IH}	2.0	–	–	
Input Current	DI1-3	I_{in}	–	–	±1.0	μA
$V_{DI1-3} = V_{CC}$						
Output High Voltage	Tx1-3	V_{OH}				V
V_{DI1-3} = Logic 0, R_L = 3.0 kΩ						
V_{DD} = +5.0 V, V_{SS} = −5.0 V			3.5	3.9	–	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			4.3	4.7	–	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			9.2	9.5	–	
Output Low Voltage*	Tx1-3	V_{OL}				V
V_{DI1-3} = Logic 1, R_L = 3.0 kΩ						
V_{DD} = +5.0 V, V_{SS} = −5.0 V			−4.0	−4.3	–	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			−4.5	−5.2	–	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			−10.0	−10.3	–	
Off Source Resistance (Figure 1)	Tx1-3		300	–	–	Ω
$V_{DD} = V_{SS} = GND = 0$ V, V_{Tx1-3} = ±2.0 V						
Output Short-Circuit Current	Tx1-3	I_{SC}				mA
V_{DD} = +12.0 V, V_{SS} = −12.0 V						
Tx1-3 shorted to GND**			–	±22	±60	
Tx1-3 shorted to ±15.0 V***			–	±60	±100	

*The voltage specifications are in terms of absolute values.

**Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

***This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V ±5%, T_A = −40 to 85°C; See Figures 2 and 3)

Characteristic		Symbol	MC145406 Min	MC145406 Typ	MC145406 Max	Unit
Drivers						
Propagation Delay Time	Tx1-3	t_{PLH}				ns
Low-to-High						
R_L = 3 kΩ, C_L = 50 pF			–	300	500	
High-to-Low		t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF			–	300	500	
Output Slew Rate	Tx1-3	SR				V/μs
Minimum Load						
R_L = 7 kΩ, C_L = 0 pF, V_{DD} = 6 to 12 V, V_{SS} = −6 to −12 V			–	±6	±30	
Maximum Load						
R_L = 3 kΩ, C_L = 2500 pF						
V_{DD} = 12 V, V_{SS} = −12 V			–	±3.0	–	
V_{DD} = 5 V, V_{SS} = −5 V			–	–	–	
Receivers (C_L = 50 pF)						
Propagation Delay Time	DO1-3					ns
Low-to-High		t_{PLH}	–	150	425	
High-to-Low		t_{PHL}	–	150	425	
Output Rise Time	DO1-3	t_r	–	250	400	ns
Output Fall Time	DO1-3	t_f	–	40	100	ns

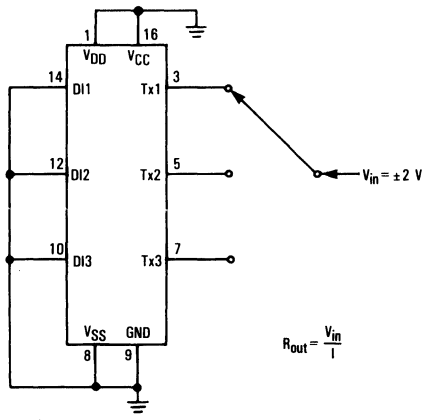


Figure 1. Power-Off Source Resistance (Drivers)

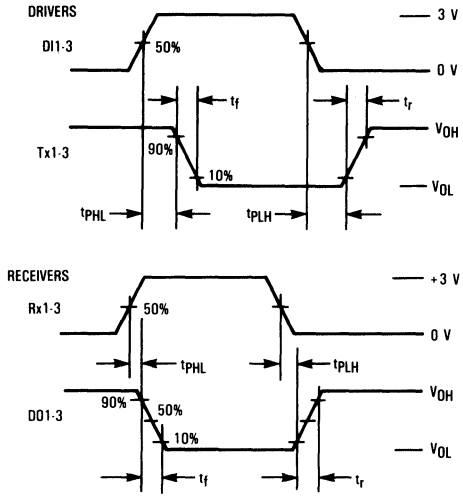


Figure 2. Switching Characteristics

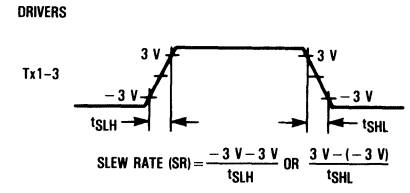


Figure 3. Slew Rate Characterization

PIN DESCRIPTIONS

V_{DD}—POSITIVE POWER SUPPLY (PIN 1)

The most positive power supply pin, which is typically 5 to 12 volts.

V_{SS}—NEGATIVE POWER SUPPLY (PIN 8)

The most negative power supply pin, which is typically −5 to −12 volts.

V_{CC}—DIGITAL POWER SUPPLY (PIN 16)

The digital supply pin, which is connected to the logic power supply (maximum +5.5 volts). V_{CC} *must* be less than or equal to V_{DD}.

GND—GROUND (PIN 9)

Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (connector pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx3—RECEIVE DATA INPUT (PINS 2, 4, 6)

These are the EIA-232-D receive signal inputs whose voltages can range from (V_{DD} + 15 V) to (V_{SS} − 15 V). A voltage between +3 and (V_{DD} + 15 V) is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between −3 and (V_{SS} − 15 V) is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8 volts above ground, and includes 800 millivolts of hysteresis for noise rejection. The nominal input impedance is 5 kilohms. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3—DATA OUTPUT (PINS 11, 13, 15)

These are the receiver digital output pins, which swing from V_{CC} to ground. A space on the Rx pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3—DATA INPUT (PINS 10, 12, 14)

These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 volts above ground. However, 5-volt CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and ground.

Tx1, Tx2, Tx3—TRANSMIT DATA OUTPUT (PINS 3, 5, 7)

These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corrresponding Tx output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 volts per microsecond. When the MC145406 is off ($V_{DD} = V_{SS} = V_{CC} = GND$), the minimum output impedance is 300 ohms.

2

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D and CCITT V.28. EIA-232-D defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads. These leads, referred to as interchange circuits, allow the transfer of timing, data, control, and test signals. Electrically this transfer requires level shifting between the TTL/CMOS logic levels of the computer or modem and the high voltage levels of EIA-232-D, which can range from ±3 to ±25 volts. The MC145406, provides the necessary level shifting as well as meeting other aspects of the EIA-232-D specification.

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15 volts into a load of between 3 to 7 kilohms. A logic one at the driver input results in a voltage of between −5 to −15 volts. A logic zero results in a voltage between +5 to +15 volts. When operating V_{DD} and V_{SS} at ±7 to ±12 volts, the MC145406 meets this requirement. When operating at ±5 volts, the MC145406 drivers produce less than ±5 volts at the output (when terminated), which does not meet EIA-232-D specification. However, the output voltages when using a ±5 volt power supply are high enough (around ±4 volts) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15 volt source that is current limited to 500 milliamperes. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300 ohm output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40 mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30 volts per microsecond.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of −25 to +25 volts down to TTL/CMOS logic levels (0 to +5 volts). A voltage of between −3 and −25 volts on Rx1 is defined as a mark and produces a logic one at DO1. A voltage between +3 and +25 volts is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kilohms. Nominally, the input resistance of the Rx1-3 inputs is 5.4 kilohms.

The input threshold of the Rx1-3 inputs is typically biased at 1.8 volts above ground (GND) with typically 800 millivolts of hysteresis included to improve noise immunity. The 1.8 volt bias forces the appropriate DO pin to a logic one when its Rx input is open or grounded as called for in the EIA-232-D specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (Tx1-3) to TTL inputs since TTL operates off +5 volts only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5 volts and the EIA-232-D signals at ±12 volts.

POWER SUPPLY CONSIDERATIONS

V_{CC} should not exceed V_{DD} by more than 0.5 volts. Due to an internal diode between V_{DD} and V_{CC}, the power-up or power-down power supply sequences may permit V_{CC} to be greater than V_{DD} for a short period of time. This condition could cause parts to fail for longer periods of time. A diode as shown in Figure 4 can be used to protect the device from this condition.

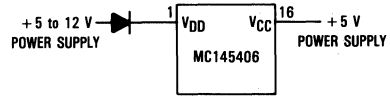
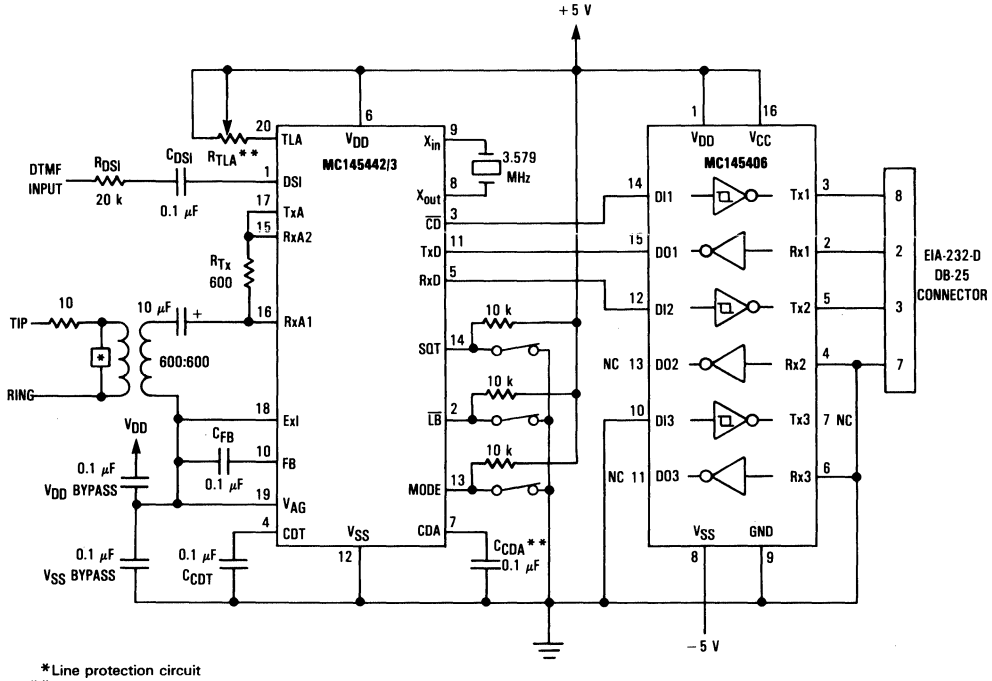


Figure 4. Protection Diode for $V_{CC} > V_{DD}$ Condition



*Line protection circuit
**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 5. 5-Volt 300-Baud Modem with EIA-232-D Interface

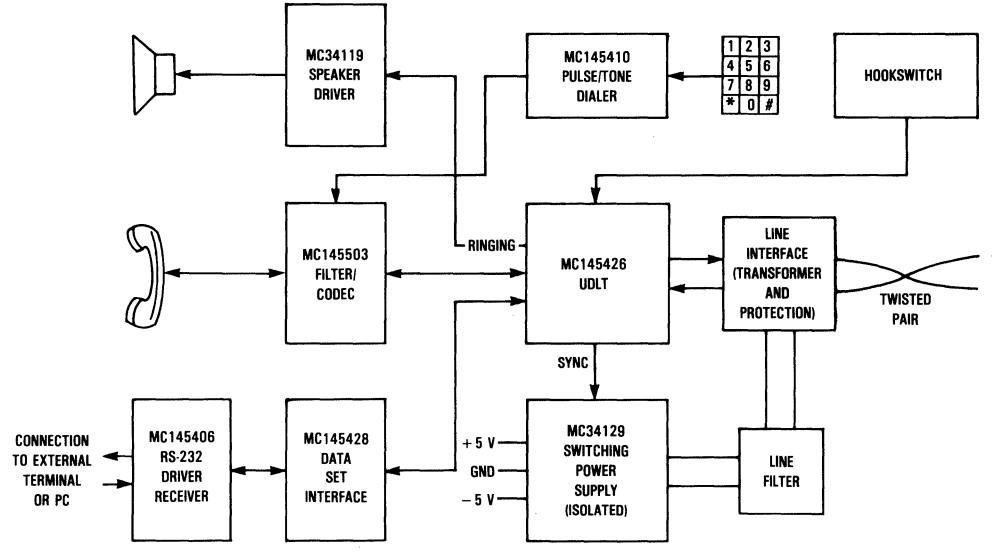


Figure 6. Line-Powered Voice/Data Telephone with Electrically Isolated EIA-232-D Interface

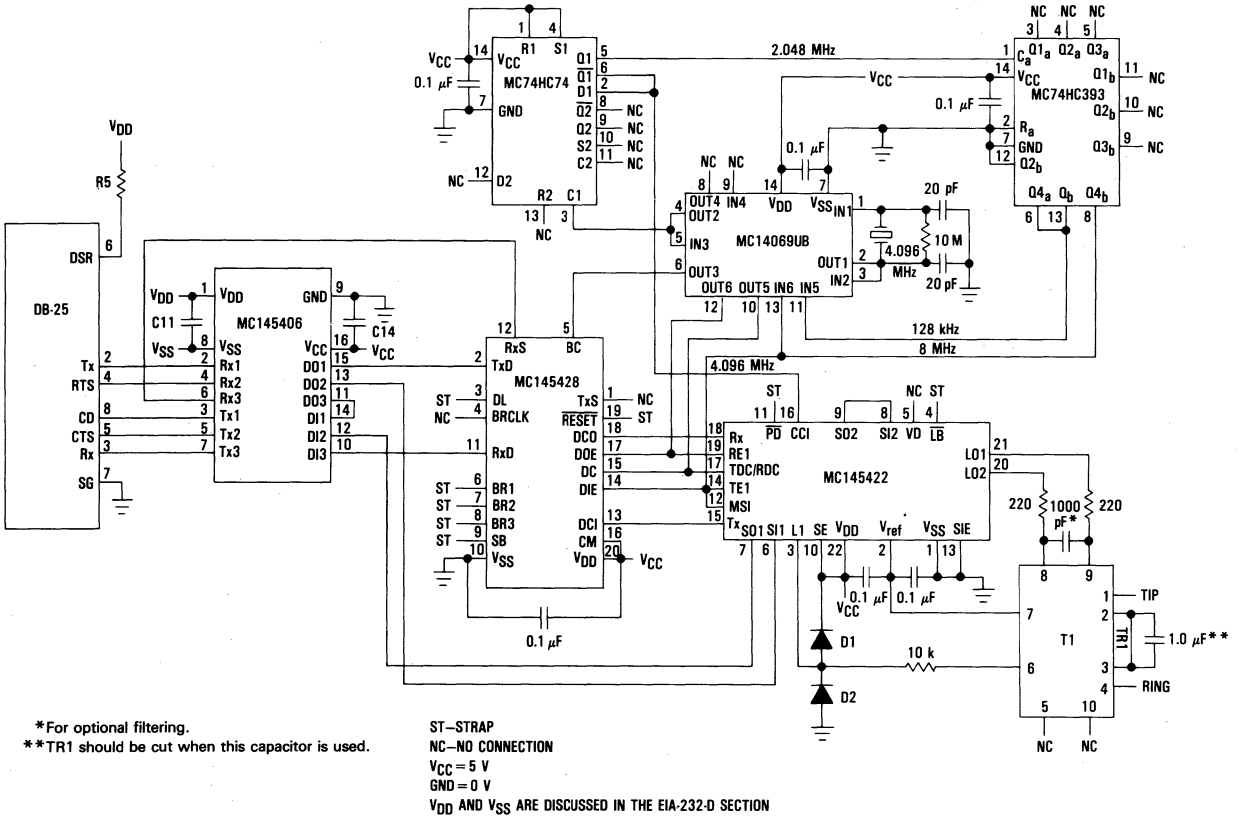


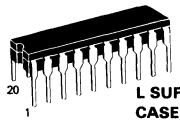
Figure 7. 80 kbps Limited Distance Modem with EIA-232-D Interface (Master)

MC145407

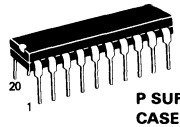
Advance Information

5-Volt-Only Driver/Receiver

EIA-232-D and CCITT V.28



L SUFFIX
CASE 732
CERAMIC



P SUFFIX
CASE 738
PLASTIC

DW SUFFIX
CASE 751D
SOIC

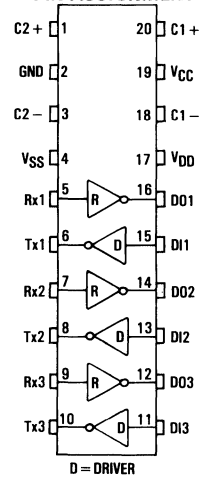
The MC145407 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA-232-D and CCITT V.28 while operating from a single +5 volt power supply. A voltage doubler and inverter convert the +5 volts to ±10 volts. This is accomplished through an on-board 20 kHz oscillator and four inexpensive external electrolytic capacitors. The three drivers and three receivers of the MC145407 are virtually identical to those of the MC145406. Therefore, for applications requiring more than three drivers and/or three receivers, an MC145406 can be powered from an MC145407, since the MC145407 charge pumps have been designed to guarantee ±5 volts at the output of up to six drivers. Thus the MC145407 provides a high-performance, low-power, stand-alone solution or, with the MC145406, a +5 volt-only, high-performance two-chip solution.

Drivers
- ±7.5 Volt Output Swing
- 300 Ohms Power-Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Slew Rate Range Limited from 4 V/μs to 30 V/μs

Receivers
- ±25 Volt Input Range
- 3 to 7 Kilohms Input Impedance
- 0.8 Volt Hysteresis for Enhanced Noise Immunity

Charge Pumps
- +5 Volts to ±10 Volt Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three On-Chip Drivers and Three Drivers on the MC145406 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On-Chip 20 kHz Oscillator

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{CC}	−0.5 to 6.0	V
Input Voltage Range Rx1-3 Inputs DI1-3 Inputs	V_{IR}	 $V_{SS}-15$ to $V_{DD}+15$ −0.5 to ($V_{CC}+0.5$)	V
DC Current Per Pin	I	±100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \le V_{DI} \le V_{DD}$ and $GND \le V_{DO} \le V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS}-15\ V) \le V_{Rx1-3} \le (V_{DD}+15\ V)$, and Tx should be constrained to $V_{SS} \le V_{Tx1-3} \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V; CI, C2, C3, C4 = 10 μF; T_A = −40 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Outputs unloaded, inputs low)		I_{CC}	—	1.2	2.5	mA
Output Voltage	I_{load} = 0 mA	V_{DD}	8.5	10	11	V
	I_{load} = 5 mA		7.5	9.5	—	
	I_{load} = 10 mA		6	9	—	
	I_{load} = 0 mA	V_{SS}	−8.5	−10	−11	
	I_{load} = 5 mA		−7.5	−9.2	—	
	I_{load} = 10 mA		−6	−8.6	—	

RECEIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn-on Threshold $V_{DO1-3} = V_{OL}$	Rx1-3	V_{on}	1.35	1.8	2.35	V
Input Turn-off Threshold $V_{DO1-3} = V_{OH}$	Rx1-3	V_{off}	0.75	1.0	1.25	V
Input Threshold Hysteresis ($V_{on} - V_{off}$)	Rx1-3	V_{hys}	0.6	0.8	—	V
Input Resistance	Rx1-3	R_{in}	3.0	5.4	7.0	kΩ
High-Level Output Voltage V_{Rx1-3} = −3 V to −25 V	DO1-3	V_{OH}				V
I_{OH} = −20 μA			$V_{CC}-0.1$	—	—	
I_{OH} = −1 mA			$V_{CC}-0.7$	4.3	—	
Low-Level Output Voltage V_{Rx1-3} = +3 V to +25 V	DO1-3	V_{OL}				V
I_{OL} = +20 μA			—	0.01	0.1	
I_{OL} = +1.6 mA			—	0.5	0.7	

DRIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1-3					V
Logic 0		V_{IL}	–	–	0.8	
Logic 1		V_{IH}	2.0	–	–	
Input Current $GND \le V_{DI1-3} \le V_{CC}$	DI1-3	I_{in}	–	–	±1.0	μA
Output High Voltage	Tx1-3	V_{OH}	6	7.5	–	V
V_{DI1-3} = Logic 0, R_L = 3.0 kΩ	Tx1-6*		5	6.5	–	
Output Low Voltage	Tx1-3	V_{OL}	−6	−7.5	–	V
V_{DI1-3} = Logic 1, R_L = 3.0 kΩ	Tx1-6*		−5	−6.5	–	
Off Source Impedance (Figure 1)	Tx1-3	Z_{off}	300	–	–	Ω
Output Short-Circuit Current	Tx1-3	I_{SC}				mA
V_{CC} = +5.5 V						
Tx1-3 shorted to GND**			–	–	±60	
Tx1-3 shorted to ±15 V***			–	–	±100	

*Specifications for an MC145407 powering an MC145406 with three additional drivers/receivers.

**Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

***This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 μF; T_A = −40 to 85°C; See Figures 2 and 3)

Characteristic		Symbol	Min	Typ	Max	Unit
Drivers						
Propagation Delay Time	Tx1-3	t_{PLH}				μs
Low-to-High						
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			–	0.5	1	
High-to-Low		t_{PHL}				
R_L = 3 kΩ, C_L = 50 pF or 2500 pF			–	0.5	1	
Output Slew Rate	Tx1-3	SR				V/μs
Minimum Load						
R_L = 7 kΩ, C_L = 0 pF			–	±6	±30	
Maximum Load						
R_L = 3 kΩ, C_L = 2500 pF			–	±5.0	–	
Receivers (C_L = 50 pF)						
Propagation Delay Time	DO1-3					μs
Low-to-High		t_{PLH}	–	–	1	
High-to-Low		t_{PHL}	–	–	1	
Output Rise Time	DO1-3	t_r	–	250	400	ns
Output Fall Time	DO1-3	t_f	–	40	100	ns

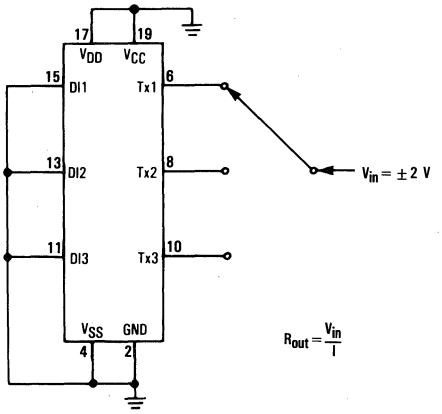


Figure 1. Power-Off Source Resistance

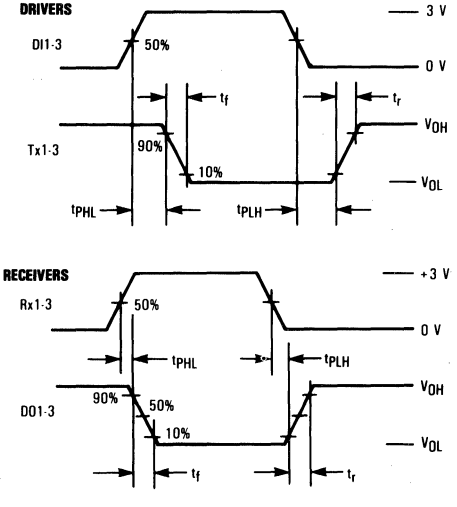


Figure 2. Switching Characteristics

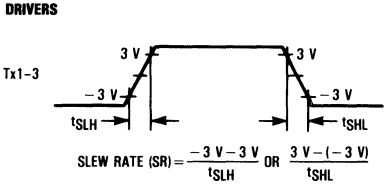


Figure 3. Slew Rate Characteristics

PIN DESCRIPTIONS

V_{CC}—DIGITAL POWER SUPPLY (PIN 19)

The digital supply pin, which is connected to the logic power supply. This pin should have a 0.33 μF capacitor to ground.

GND—GROUND (PIN 2)

Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (connector pin 7) as well as to the logic power supply ground.

V_{DD}—POSITIVE POWER SUPPLY (PIN 17)

This is the positive output of the on-chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}—NEGATIVE POWER SUPPLY (PIN 4)

This is the negative output of the on-chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

C2+, C2−, C1−, C1+—VOLTAGE DOUBLER AND INVERTER (PINS 1, 3, 18, 20)

These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2, Rx3—RECEIVE DATA INPUT (PINS 5, 7, 9)

These are the EIA-232-D receive signal inputs. A voltage between +3 and +25 volts is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between −3 and −25 volts is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2, DO3—DATA OUTPUT (PINS 16, 14, 12)

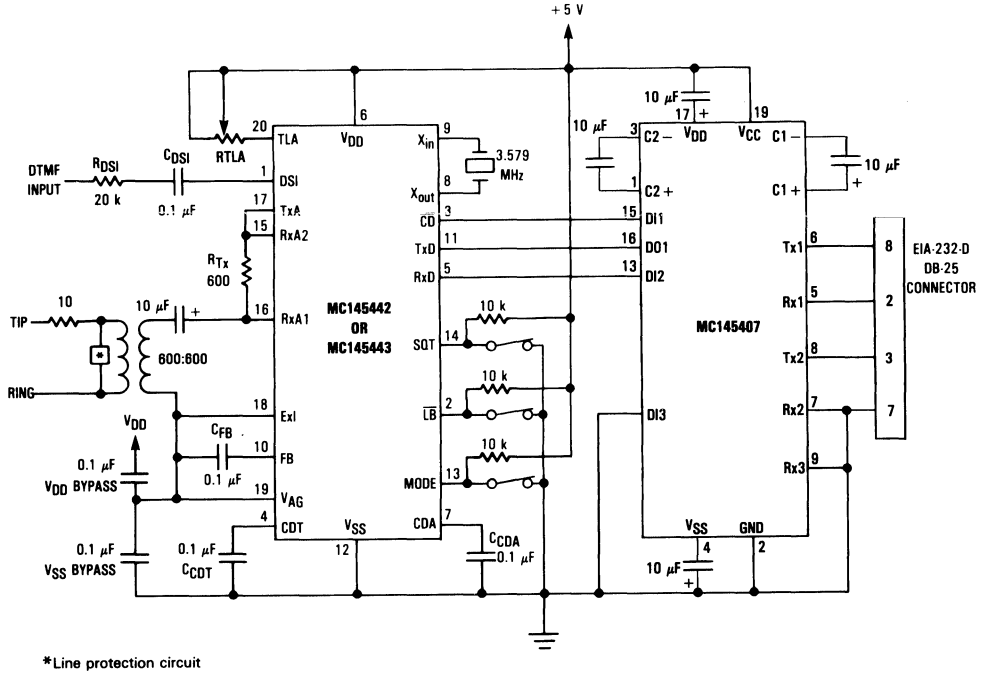
These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3—DATA INPUT (PINS 15, 13, 11)

These are the high-impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3—TRANSMIT DATA OUTPUT (PINS 6, 8, 10)

These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corrresponding Tx output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD}. The actual levels and slew rate achieved will depend on the output loading ($R_L \| C_L$).



*Line protection circuit

Figure 4. 5-Volt 300-Baud Modem with EIA-232-D Interface

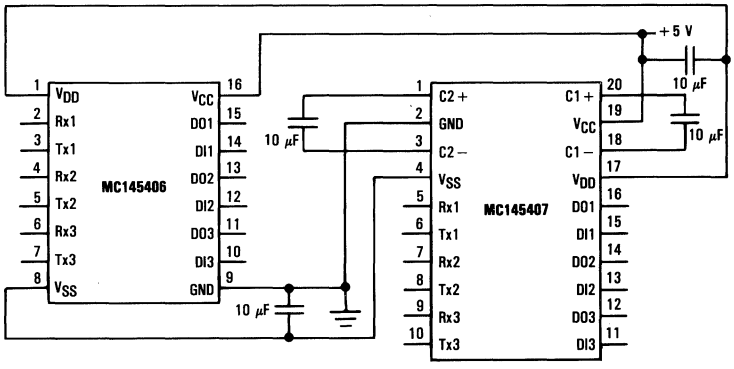


Figure 5. MC145406/MC145407 5-Volt-Only Solution for up to Six EIA-232-D Drivers and Receivers

MC145411

Advance Information

2

BIT RATE GENERATOR

The MC145411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

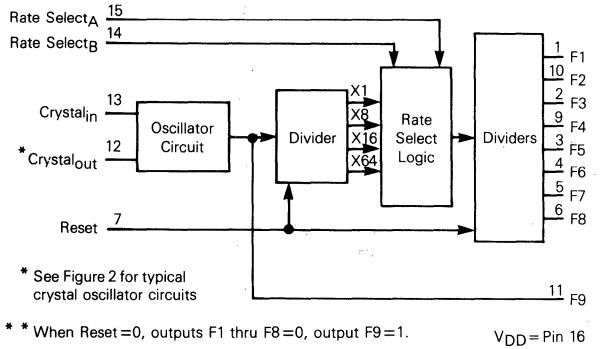
Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 V (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (to 4 MHz)
- 21 Different Bit Rates
- Nine Different Bit Rate Output Pins
- Programmable Time Bases for One of Four Multiple Output Rates
- 50% Output Duty Cycle
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 13
- Internal Pullup Resistor on Reset Input

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	5.25 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



* See Figure 2 for typical crystal oscillator circuits

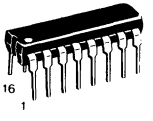
* * When Reset = 0, outputs F1 thru F8 = 0, output F9 = 1.

V_{DD} = Pin 16
V_{SS} = Pin 8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

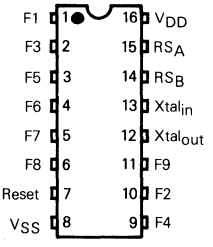
CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

BIT RATE GENERATOR



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	0		25°C			+70°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Supply Voltage	V_{DD}	–	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	V
"1" Level		5.0	4.99	–	4.99	5.0	–	4.99	–	V
Input Voltage (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	
Output Drive Current (V_{OH} = 2.5 V) Source	I_{OH}	5.0	−0.23	–	−0.20	−1.7	–	−0.16	–	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	
Input Current Pins 13, 14, 15	I_{in}	–	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Pin 7		5.0	–	–	−1.5	–	−7.5	–	–	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q	5.0	–	2.5	–	0.015	2.5	–	15	mW
Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	P_D	5.0	–	–	$P_D = (7.5\ mW/MHz)\ f + P_Q$					mW
Output Rise Time** t_r = (3.0 ns/pF) C_L + 25 ns	t_{TLH}	5.0	–	–	–	70	200	–	–	ns
Output Fall Time** t_f = (1.5 ns/pF) C_L + 47 ns	t_{THL}	5.0	–	–	–	70	200	–	–	ns
Input Clock Frequency	f_{CL}	5.0	–	4.0	–	–	4.0	–	4.0	MHz
Clock Pulse Width	$t_{W(C)}$	–	200	–	200	–	–	200	–	ns
Reset Pulse Width	$t_{W(R)}$	–	500	–	500	–	–	500	–	ns

†For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T(C_L = P_D + 2.6 \times 10^{-3}(C_L - 15\ pF)\ V_{DD}{}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in V, and f in MHz.
**The formula given is for the typical characteristics only.

TABLE 1A — OUTPUT CLOCK RATES

Rate Select B	Rate Select A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

TABLE 1B — 1.843 MHz Crystal Output Rates

Output Number	Output Rates (Hz)			
	×64	×16	×08	×01
F1	614.4 k	153.6 k	76.8 k	9600
F2	230.4 k	57.6 k	28.8 k	3600
F3	153.6 k	38.4 k	19.2 k	2400
F4	115.2 k	28.8 k	14.4 k	1800
F5	76.8 k	19.2 k	9600	1200
F6	38.4 k	9600	4800	600
F7	19.2 k	4800	2400	300
F8	9600	2400	1200	150
F9*	1.843 M	1.843 M	1.843 M	1.843 M

*F9 is buffered oscillator output.

TABLE 1C — 3.6864 MHz Output Rates

Output Number	Output Rates (Hz)		
	×16	×08	×01
F1	307.2 K	153.6 k	19.2 k
F2	115.2 k	57.6 k	7200
F3	76.8 k	38.4 k	4800
F4	57.6 k	28.8 k	3600
F5	38.4 k	19.2 k	2400
F6	19.2 k	8600	1200
F7	9600	4800	600
F8	4800	2400	300
F9*	3.6864 M	3.6864 M	3,6864 M

*F9 is buffered oscillator output.

2

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS

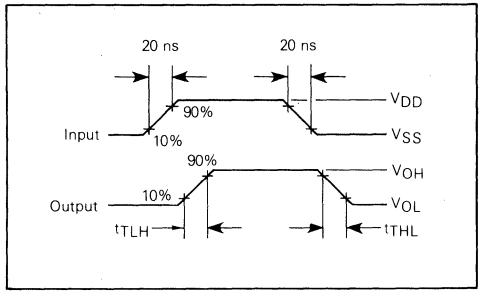
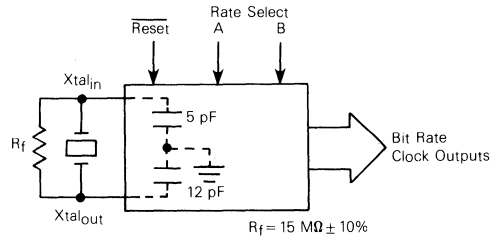


FIGURE 2 — TYPICAL CRYSTAL OSCILLATOR CIRCUIT



Crystal Specifications

Crystal Mode	Parallel
Frequency	1.8432 MHz or 3.6864 MHz ±0.05% @ 13 pF
R_S	540 Ω max
C_0	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS — 330/TSM or Equivalent

MC145412
MC145413
MC145512

2

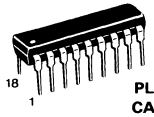
Advance Information

Pulse/Tone Repertory Dialer

Low Power Silicon-Gate CMOS

The MC145412/13 and MC145512 are silicon gate, monolithic CMOS integrated circuits which convert keyboard inputs into either pulse or DTMF outputs. They are packaged in a standard 18 pin (0.3" wide) plastic DIP.

- 3×4 or 4×4 Keyboard Compatibility Which Allows the Use of 2-of-7, 2-of-8, or Form A Type Keyboards
- MC145413 Adds Keyboard Selectable Pause Switch Function
- Single Pin Switchable Between DTMF, 10 pps and 20 pps
- 500 Hz Tone Signal Output in the Pulse Dialing Mode
- Memory Storage for Ten 18 Digit Numbers, Including Last Number Redial
- Uses 3.579545 MHz Colorburst Crystal
- Telephone Line Powered
- Silicon Gate CMOS Technology for 1.7-5.5 V Low Power Operation
- Stand Alone DTMF Dialer/Stand Alone Pulse Dialer
- Mute Output Used to Isolate Receiver from Dialing Output
- Memory Programming Options by Keyboard Configuration



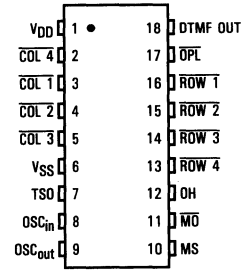
PLASTIC
CASE 707

Ordering Information

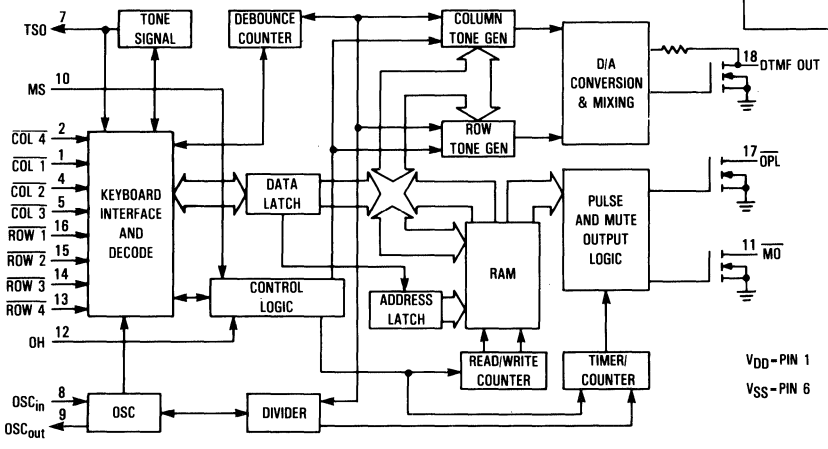
MC145 X X X X

- P Plastic
- 4 40/60 M/B Ratio
- 5 32/68 M/B Ratio

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
DC Supply Voltage	V_{DD}	−0.5 to +8.0	V
Operating Temperature	T_A	−30 to +60	°C
Storage Temperature	T_{stg}	−65 to +150	°C
DC Current Drain Per Pin	I	10	mA
Maximum Voltage On Any Pin Relative to V_{SS} On Any Pin Relative to V_{DD}	 V_{in1} V_{in2}	 −0.5 +0.5	V

ELECTRICAL CHARACTERISTICS (T_A = −30 to 60°C, V_{DD} = 2.5 V, V_{SS} = 0 V, Unless Otherwise Noted)

Characteristics		Symbol	Min	Typ	Max	Unit
DC Supply Voltage	Pulse Mode DTMF Mode	V_{DD}	2.0 2.5	– –	5.5 5.5	V
Operating Current	Pulse Mode (MS = V_{DD}) DTMF Mode (MS = V_{SS})	I_{DD}	– –	0.25 1.0	0.7 2.0	mA
Memory Retention Voltage		V_{stby}	1.7	–	–	V
Memory Retention Current	(V_{DD} = 1.7 V) (V_{DD} = 2.5 V)	I_{stby}	– –	1.0 1.2	2.0 2.5	μA
Input Voltage, Row/Column/OH	"0" Level "1" Level	V_{IL} V_{IH}	– 0.8 V_{DD}	– –	0.2 V_{DD} –	V
Row/Column Input Impedance	To V_{DD} To V_{SS}	Z_{in}	– –	100 2	– –	kΩ
OH Pull-Up Resistance		R	–	50	–	kΩ
Input Capacitance (All Inputs)		C_{in}	–	10	–	pF
MS Pin Input Impedance		Z_{in}	50	200	–	kΩ
Output Sink Current	(V_{DD} = 2.5 V) TSO Pin $\overline{MO}$ Pin $\overline{OPL}$ Pin (V_{DD} = 4.0 V) $\overline{MO}$ Pin $\overline{OPL}$ Pin	I_{OL}	0.5 1.0 1.0 3.0 4.5	0.7 2.0 2.0 – –	– – – – –	mA
TSO Output Source Current (V_{out} = 2.0 V)		I_{OH}	0.5	0.7	–	mA
Output Leakage Current	$\overline{MO}$, $\overline{OPL}$ Pins	I_{lkg}	–	–	1.0	μA
DTMF Output Level Referenced to V_{DD}/2 (V_{DD} = 2.5 to 4.0 V, RL = 600 Ω to V_{DD})	Row Tone Column Tone	V_{out}	260 330	310 390	370 460	mV RMS
DTMF Output Tone Leakage (V_{DD} = 3.5, RL = 600 Ω, 300 to 4000 Hz)			–	–	−80	dBm
DTMF Output Tone Distortion (V_{DD} = 3.5, RL = 600 Ω, 300 to 4000 Hz)			–	–	5	%
Pre-Emphasis			1	2	2.5	dB
DTMF Output Leakage Current While Not Dialing Tones (V_{DD} = 2.5 V)			–	–	1.0	μA
DTMF Output Sink Current While Dialing Tones			20	–	–	μA

SWITCHING CHARACTERISTICS (T_A=25°C, V_{DD}=2.5 V, Osc. Freq.=3.579545 MHz, Unless Otherwise Noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Row/Column Scan Frequency		f	–	250	–	Hz
Key Debounce Time		t_{DB}	16	–	20	ms
DTMF Tone Duration for Keypad Dialing		t_{w1}	60	78	–	ms
DTMF Tone Duration for Memory Dialing		t_{w2}	90	102	110	ms
Inter-Digit Pause Time	DTMF (Memory Dialing)	t_{ID}	90	98	110	ms
	Pulse 10 pps		0.8	1.0	1.2	s
	20 pps		0.4	0.5	0.6	
MS Pin Scan Rate		t_{rms}	–	1	–	kHz
Make/Break Ratio	MC145412/13	MBR	–	40/60	–	%
(MS=Open or V_{DD})	MC145512		–	32/68	–	
Outpulsing Rate	MS=Open	f_{OPL}	–	10	–	pps
	MS=V_{DD}		–	20	–	
MUTE Output ($\overline{MO}$) Overlap Time		t_{MO}	–	2	–	ms
TSO Output Frequency		f_{TSO}	–	500	–	Hz
TSO Output Duration		t_{TSO}	35	–	40	ms
DTMF Cycle Time	(Memory Dialing)		–	5	–	tones/s
	(Keypad Dialing)		–	10	–	
DTMF Frequency Deviation			–	–	+1.0	%
Predigit Mute	MC145412/13 Pulse 10 pps	t_d	–	40	–	ms
	20 pps		–	20	–	
	MC145512 Pulse 10 pps		–	32	–	
	20 pps		–	16	–	
	DTMF		–	1	–	

PIN DESCRIPTIONS

V_{DD}, V_{SS}—POWER SUPPLY (PIN 1, PIN 6)

DC power is supplied to the part on these two pins, with V_{DD} being the most positive. Permissible ranges are from 1.7 to 5.5 V.

MS—MODE SELECT (PIN 10)

The MS pin is a three state input for switching between DTMF, 10 pps, and 20 pps dialing modes. Mode selection is done during the first key entry debounce period after the dialer has completed a dialing sequence or has just come off hook. When this pin is not scanned it is high impedance.

This pin is a combination input and weak output. The input circuitry has the capability to determine each of these three states. When the pin is open the weak driver will be able to clock the pin at 1 kHz. The relationship between pin input voltage and operating mode is shown in Table 1 below.

Table 1. Mode Select Options

MS	Dialing Mode
V_{DD}	20 pps Pulse Dialing
Open	10 pps Pulse Dialing
V_{SS}	DTMF Dialing

OH-ON-HOOK (PIN 12)

Connecting the OH pin to V_{DD}, or allowing it to float sets the device in the on-hook mode. Connecting this pin to V_{SS} selects the off-hook mode. When in the on-hook mode, repertory memory can be programmed without a dialing output.

TSO—TONE SIGNAL OUTPUT (PIN 7)

TSO emits 500 Hz tone signals after valid key inputs are accepted providing audio feedback for key depressions, except when DTMF tones are generated. This pin also outputs a tone during on-hook programming.

DTMF OUT—DUAL TONE MULTIFREQUENCY OUTPUT (PIN 18)

When the MS pin is set to V_{SS} the DTMF OUT pin outputs tones corresponding to the row and column of the key depressed. Simultaneously depressing two or more keys in a single row (or column) will generate the corresponding row (or column) tone on 4×4 keypad mode only.

In pulse dialing mode (MS=V_{DD} or float) and during on-hook programming this pin is high impedance. While outputting tones, this pin has a dc bias at ($V_{DD}-V_{SS}$)/2. DTMF OUT is an open drain output requiring an external pull-up to V_{DD}. This pull-up resistor must satisfy the instantaneous current requirements of the internal feedback network in addition to the load applied to the pin.

$\overline{OPL}$—OUTPULSING (PIN 17)

This pin outputs pulses at 10 pps (MS is open) or 20 pps (MS=V_{DD}). The MC145412/13 have a make/break ratio of 40/60, while the MC145512 has a make/break ratio of 32/68. In the DTMF dialing mode (MS=V_{SS}), this output is high impedance. During on-hook programming this pin will not outpulse. This pin is an open drain N-channel output which pulls low to break the loop current.

$\overline{MO}$—MUTE OUTPUT (PIN 11)

The Mute Output is an open drain N-channel output that pulls to V_{SS} during $\overline{OPL}$ outpulsing and during off-hook key depressions and memory dialing in DTMF mode.

2

KEYBOARD INPUTS—(PINS 2, 3, 4, 5, 13, 14, 15, 16)

The keyboard inputs allow either a single contact (Class A) keyboard, or a standard 2-of-8 or 2-of-7 keyboard with V_{SS} tied to common. A valid key entry occurs when either a single row is tied to a single column, or a single row and column are simultaneously connected to V_{SS}. Connecting pin 2, $\overline{\text{COL 4}}$, to V_{DD} sets the part to 3 × 4 keyboard mode. Keyboard mode selection is performed during application of power.

Typical keyboard configurations are shown in Figure 1.

OSC_{in}, OSC_{out} (PIN 8, PIN 9)

A 3.579545 MHz crystal is required as the frequency reference for the on-chip oscillator. Crystal biasing is accomplished by an internal resistor and capacitors.

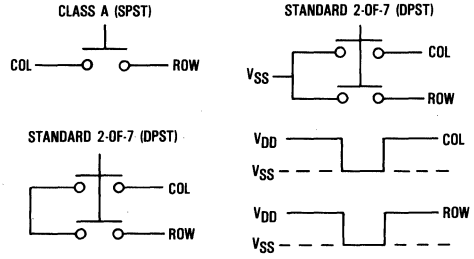


Figure 1. Keyboard Configurations

GENERAL DEVICE DESCRIPTION

The MC145412/MC145512 and the MC145413 provide users with switchable pulse and DTMF dialing functions. The MC145412/MC145512 change dialing modes via the MS pin. The MC145413 allows users to switch dialing modes via the keyboard in addition to the MS pin. All devices have 10 memories, LNR (last number redial) inclusive, each 18 digits long.

On application of power, there is a 64 ms initialization period during which the oscillator is enabled and the keyboard inputs are disabled. During initialization $\overline{\text{COL 4}}$ is scanned to set the keyboard mode. If the $\overline{\text{COL 4}}$ input is high (V_{DD}) the dialer is set to the 3 × 4 keypad mode, otherwise the 4 × 4 keypad mode is selected. Changing modes is not possible after this initialization period.

During normal dialing, the oscillator starts when a key is depressed. The key input is debounced for 32 ms. During this debounce period the RAM and dialing circuits are disabled, the mode select pin is scanned to determine the dialing mode (either 10 pps, 20 pps, or DTMF). After debounce, the keypad entry is checked and the input is latched into LNR memory followed by a stop code. This process continues until 18 digits have been entered. If a 19th digit is entered, it will over-write the first digit and will be followed by a stop code. When dialing, the device fetches data from memory until a stop code is encountered or 18 digits have been dialed.

During manual DTMF dialing, a minimum tone duration of 60 ms DTMF is output and will continuously output in 32 ms increments as long as the key is depressed. The DTMF OUT pin is designed to drive an external PNP transistor which can be used to modulate tip and ring voltage at the DTMF frequencies.

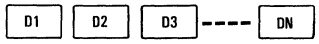
If the first key is for redial or recall, the device will respond accordingly, either redialing the last number entered, or recalling and dialing the number selected by a subsequent key depression. Responses to dialing sequences for 4 × 4 keyboards are shown in Figure 2, and 3 × 4 keyboard responses are shown in Figure 3.

The MC145412 series can be configured with an external battery to provide memory retention power and allow on-hook programming of the repertory memory. If the part is in the on-hook mode and a key is depressed, the oscillator will start and the key entry will be stored in the last number redial memory. Dialing outputs will not be activated while the device is in the on-hook condition. Dialing inputs will be stored in last number redial memory, as during off-hook operation. After the number has been entered in the on-hook mode, it can be stored in repertory memory. For the 4 × 4 keyboard, pressing the STORE key (* for 3 × 4 keyboard), followed by a digit (1 through 9) will store the number in the repertory memory location specified by the digit.

The RECALL key for the 4 × 4 keypad is used to recall and dial numbers stored in the repertory memory. The digit immediately following the RECALL key designates the memory location of the number to be auto-dialed. For the 4 × 4 keyboard, a last number redial can be accomplished if the RED/P key ($\overline{\text{COL 4}}$, $\overline{\text{ROW 1}}$) is the first key depressed after an on-hook to off-hook transition. Otherwise the RED/P key will effect a 4 second pause. If the pulse mode is selected, redial can be accomplished if the first key depressed on a transition to off-hook is #. For the 3 × 4 keyboard, redial occurs if the first key depressed is *,0.

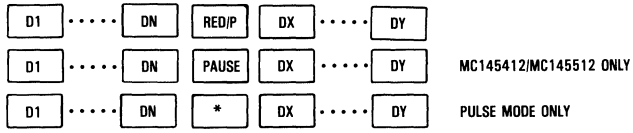
The PAUSE key ($\overline{\text{COL 4}}$, $\overline{\text{ROW 2}}$) for the MC145412/MC145512 will cause a 4 second pause. The PAUSE/S key ($\overline{\text{COL 4}}$, $\overline{\text{ROW 2}}$) is a feature offered on the MC145413. Depressing this key will cause a 4 second delay, and will switch dialing modes. PAUSE (and PAUSE/S) is stored in memory for pauses (and mode switching) during auto-dialing.

1. **MANUAL DIALING—OFF-HOOK** (PULSE OF DTMF MODE)



ALL DIGITS ENTERED WILL BE STORED IN THE LAST NUMBER REDIAL REGISTER. PRESSING * OR # WILL DIAL OUT THE DTMF SIGNAL IN TONE MODE ONLY.

2. **MANUAL DIALING WITH AUTO ACCESS PAUSE—OFF-HOOK** (PULSE OR DTMF MODE)

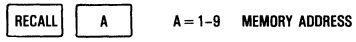


THE AUTO ACCESS PAUSE WILL NOT OCCUR DURING MANUAL DIALING IN DTMF MODE. IT IS RETRIEVED DURING RECALL OR REDIAL.

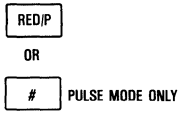
3. **STORING NUMBERS INTO MEMORY—ON-HOOK/OFF-HOOK** (PULSE OR DTMF MODE)

THIS OPERATION TRANSFERS THE DIGITS D1 TO DN FROM THE LAST NUMBER REDIAL REGISTER TO AN ADDRESS SPACE SPECIFIED BY "A". DIALING OUTPUTS ARE NOT ACTIVATED DURING ON-HOOK PROGRAMMING.

4. **MEMORY REDIAL—OFF-HOOK** (PULSE OR DTMF MODE)



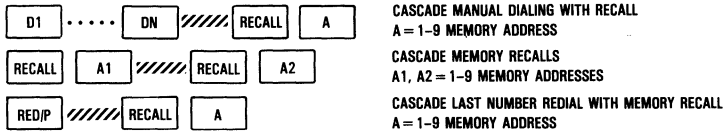
5. **LAST NUMBER REDIAL—OFF-HOOK** (PULSE OR DTMF MODE)



REDIALS THE NUMBER THAT WAS PREVIOUSLY ENTERED INTO THE LAST NUMBER REDIAL REGISTER.

6. **PULSE-TO-TONE MODE SWITCH—OFF-HOOK** (PULSE OR DTMF MODE)

7. **CASCADED DIALING—OFF-HOOK** (PULSE OR DTMF MODE)



////// WAIT UNTIL PREVIOUS REDIAL OR RECALL SIGNALS HAVE BEEN SENT BEFORE SUBSEQUENT ENTRIES ARE MADE.

8. **SIGNALING * AND # TONES—OFF-HOOK** (DTMF MODE ONLY)

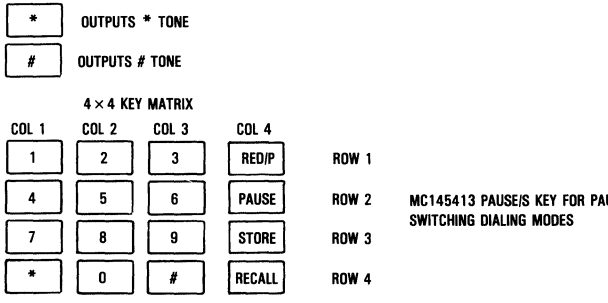
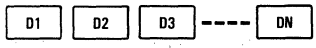


Figure 2. 4 × 4 Keyboard Dialing Sequences

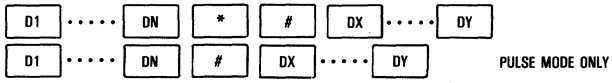
2

1. **MANUAL DIALING–OFF-HOOK** (PULSE OF DTMF MODE)



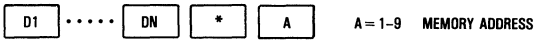
ALL KEY ENTRIES, EXCEPT * AND #, WILL BE STORED IN THE LAST NUMBER REDIAL REGISTER. PRESSING * OR # WILL NOT DIAL OUT THE DTMF SIGNAL IN TONE MODE. FOR SIGNALING, * OR # SHOULD BE PRESSED TWICE.

2. **MANUAL DIALING WITH AUTO ACCESS PAUSE–OFF-HOOK** (PULSE OR DTMF MODE)



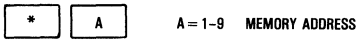
THE AUTO ACCESS PAUSE WILL NOT OCCUR ON MANUAL DIALING IN DTMF MODE. IT CAN ONLY BE RETRIEVED DURING RECALL OR REDIAL.

3. **STORING NUMBERS INTO MEMORY–ON-HOOK** (PULSE OR DTMF MODE)

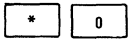


THIS OPERATION TRANSFERS THE DIGITS D1 TO DN FROM THE LAST NUMBER REDIAL REGISTER TO AN ADDRESS SPACE SPECIFIED BY "A".

4. **MEMORY REDIAL–OFF-HOOK** (PULSE OR DTMF MODE)

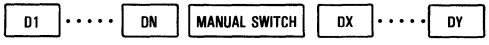


5. **LAST NUMBER REDIAL–OFF-HOOK** (PULSE OR DTMF MODE)



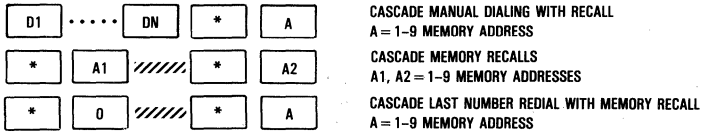
THIS OPERATION REDIALS THE LAST NUMBER ENTERED OFF-HOOK AND RETRIEVES DATA FROM MEMORY ADDRESS 0.

6. **PULSE-TO-TONE AND TONE-TO-PULSE SWITCHING–OFF-HOOK** (PULSE OR DTMF MODE)



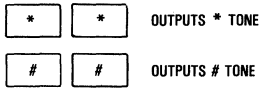
MODE SELECT (MS) PIN HAS TO BE MANUALLY SWITCHED TO DETERMINE THE DIALING MODE. DIALING MODE SELECTION WITH MANUAL SWITCH IS NOT PROGRAMMED INTO THE LAST NUMBER REDIAL MEMORY.

7. **CASCADED DIALING–OFF-HOOK** (PULSE OR DTMF MODE)



////////, WAIT UNTIL PREVIOUS REDIAL OR RECALL SIGNALS HAVE BEEN SENT BEFORE SUBSEQUENT ENTRIES ARE MADE.

8. **SIGNALING * AND # TONES–OFF-HOOK** (DTMF MODE ONLY)



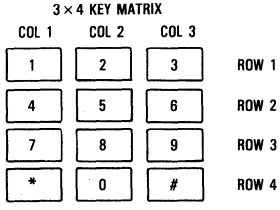


Figure 3. 3×4 Keyboard Dialing Sequences

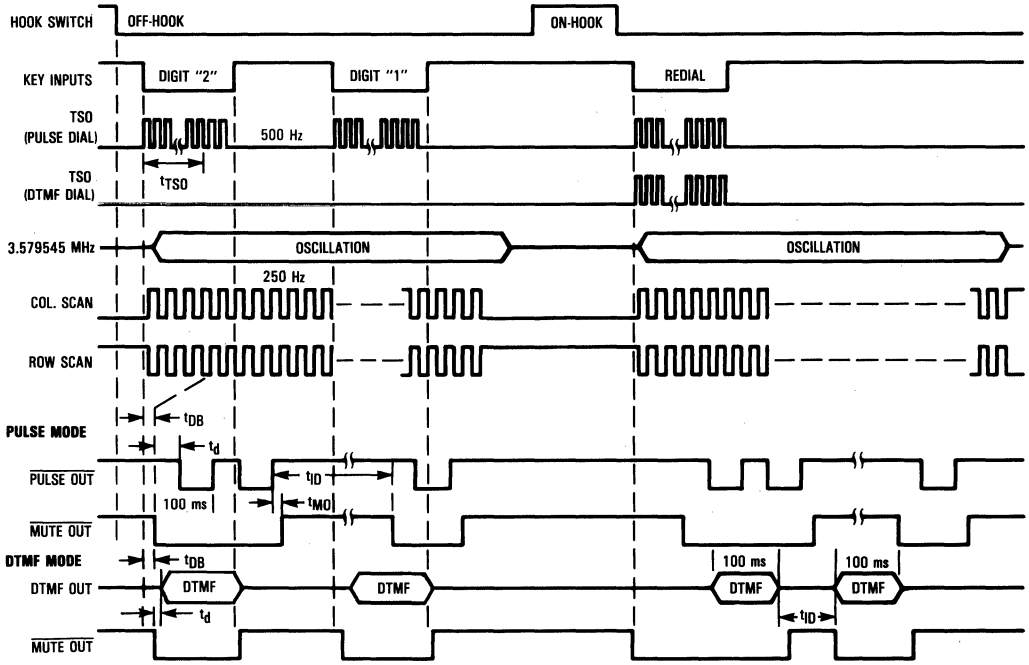


Figure 4. Timing Diagram

MC145414

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

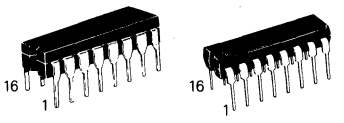
DUAL TUNABLE
LOW PASS
SAMPLED DATA FILTERS

2

DUAL TUNABLE
LOW PASS SAMPLED DATA FILTERS

The MC145414 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two totally uncommitted op amps for use elsewhere in the system as I to V converters, gain adjust buffers, etc.

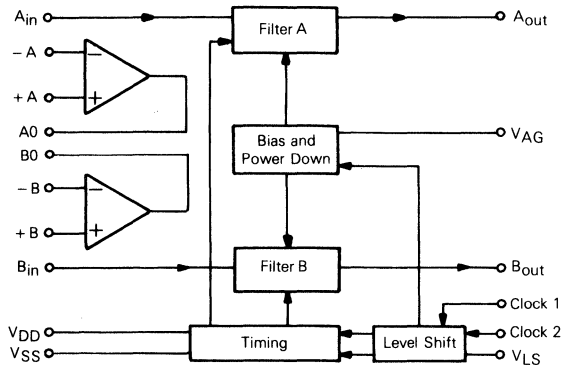
- Two General Purpose 5th Order Elliptic Low Pass Filters
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- ±5 to ±8 Volt Power Supply Ranges
- TTL or CMOS Compatible Inputs Using VLS Pin
- Two Operational Amplifiers Available to Reduce Component Count
- Useful in LPC or CVSD Speech Applications
- Passband Edges Tunable With Clock Frequency From 1.25 kHz to 10 kHz



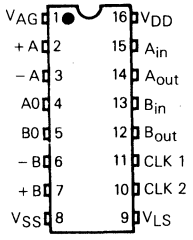
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	0 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Clock 1, 2 Frequency	CLK 1, 2	50	128	400	kHz

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD} Vdc	25°C Min	25°C Typ	25°C Max	Unit
Operating Current		I_{DD}	12	–	2.0	4.0	mA
Power-Down Current (PDI = V_{SS})		I_{PD}	12	–	10	40	μA
Input Capacitance		C_{in}	12	–	5.0	–	pF
MODE CONTROL LOGIC LEVELS							
VLS Power-Down Mode		V_{IH}	12 15	11.5 14.5	11 13	– –	V
VLS TTL Mode		–	12 15	4.0 5.0	– –	8 9	V
VLS CMOS Mode		V_{IL}	12 15	– –	– –	0.8 0.8	V
VAG Power-Down Mode		V_{IH}	12 15	11.5 14.5	10.5 13.5	– –	V
VAG Analog-Ground Mode		V_{IL}	12 15	– –	– –	7.0 9.0	V
CMOS LOGIC LEVELS (V_{LS} = V_{SS})							
Input Current Clock 1, 2 (Internal Pulldown Resistors)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level	V_{IL}	12 15	– –	5.25 6.75	3.0 3.5	V
	"1" Level	V_{IH}	12 15	9.0 11.5	6.75 8.25	–	V
TTL LOGIC LEVELS (VLS = 6 V, V_{SS} = 0 V)							
Input Current Clock 1, 2 (Internal Pulldown Resistor)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level "1" Level	V_{IL} V_{IH}	12 12	– V_{LS} + 2.0	– –	VLS + 0.8 –	V

2

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	25°C Min	25°C Typ	25°C Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±1.0	μA
Input Current	VAG	I_{in}	–	±0.00001	±10	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range (R_L = 20 kΩ to VAG, R_B = ∞) (R_L = 600 Ω to VAG, R_B = 1.6 kΩ to V_{DD}) (R_L = 900 Ω to VAG, R_B = 1.8 kΩ to V_{DD})	A0, B0, A_{out}, B_{out}	V_{OR}	 1.5 3.0 2.5	 – – –	 10.5 8.3 9.0	V
Small Signal Output Impedance (1 kHz)	A_{out} B_{out}	Z_o	– –	50 50	– –	Ω
Output Current (V_O = 10.5 V) (V_O = 1.5 V)	 A_{out}, B_{out}, A0, B0 A_{out}, B_{out}, A0, B0	 I_{OH} I_{OL}	 −200 5	 −400 7.5	 – –	 μA mA
Unity Gain Output Noise	A0, B0	–	–	15	–	μVrms

FILTER A SPECIFICATIONS

($V_{DD} - V_{SS}$ = 12 V, Clock 1, 2 = 128 kHz, V_{in} = −10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		25°C Min	25°C Typ	25°C Max	Unit
Gain (1020 Hz)		17.4	18	18.6	dB
Passband Ripple (50 Hz to 3000 Hz)		–	0.24	1.0	dB
Out of Band Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz		 – −10 −25	 −0.8 −15.5 −33.0	 −1.5 – –	dB
Output Noise (A_{in} = VAG)	ref to 900 Ω	–	10	17	dBrnc0
Dynamic Range		76	83	–	dB
Differential Group Delay 1150 to 2300 Hz Delay 1000 to 2500 Hz Delay 800 to 2700 Hz Delay		 – – –	 – – –	 – – –	μs
Power Supply Rejection Ratio (V_{DD} = 12 V +0.1 V_{RMS} @ 1 kHz)		–	36	–	dB
Crosstalk (A_{in} = VAG, B_{in} = 0 dBm0 Output at A_{out} at 3 kHz)		–	76	–	dB

FILTER B SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock 1, 2 = 128 kHz, V_{in} = −10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic	25°C Min	25°C Typ	25°C Max	Unit
Gain (1020 Hz)	−0.7	±0.15	+0.7	dB
Passband Ripple (300 Hz to 3000 Hz)	–	0.22	1.0	dB
Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz	 – −10 −28	 −0.8 −15.5 −33.0	 −1.7 – –	dB
Output Noise (300 Hz-3400 Hz)	–	8	14	dBrnc0
Dynamic Range (7 V p-p Max)	79	87	–	dB
Differential Group Delay 1150 to 2300 Hz Delay 1000 to 2500 Hz Delay 800 to 2700 Hz Delay	 – – –	 – – –	 – – –	μs
Crosstalk (B_{in} = VAG, A_{in} = 0dBm0 @ 3 kHz Output at B_{out} @ 3 kHz)	–	76	–	dB
Power Supply Rejection Ratio	–	36	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ V, $T_A = 25°C$)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	Clock 1, 2	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width	Clock 1, 2	t_{WH}	200	–	–	ns
Clock Pulse Frequency	Clock 1, 2	f_{CL}	50	–	400	kHz
Clock 1, 2 Duty Cycle		–	40	–	60	%

2

FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)
This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A
Non-inverting input of op-amp A.

Pin 3 — −A
Inverting input of op-amp A.

Pin 4 — A0
Output of uncommitted op-amp A.

Pin 5 — B0
Output of uncommitted op-amp B.

Pin 6 — −B
Inverting input of op-amp B.

Pin 7 — +B
Non-inverting input of op-amp B.

Pin 8 — V_{SS}
This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)
The voltage on this pin determines the logic compatibility for the Clock 1, 2 inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If VLS is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD}-2$ V and $V_{SS}+2$ V, the thresholds for logic inputs at Clock 1, 2 will be between $V_{LS}+0.8$ V and $V_{LS}+2.0$ V for TTL compatibility.

Pin 10 — Clock 1
Always tie clock 1 and clock 2 together.

Pin 11 — Clock 2
Always tie clock 1 and clock 2 together.

Pin 12 — B_{out} (Lowpass Filter B)
This is the output of B lowpass filter.

Pin 13 — B_{in} (Lowpass Filter B)
This is the input to filter B.

Pin 14 — A_{out} (Low pass Filter A)
This pin is the output to filter A.

Pin 15 — A_{in} (Lowpass Filter A)
This is the input to filter A.

Pin 16 — V_{DD}
Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance inputs.

FILTER DESCRIPTION

FILTER A DESCRIPTION

Filter A of the MC145414 is a 5-pole elliptic tunable lowpass filter operating at a sampling rate determined by clock 1 and clock 2. This filter provides band limiting that is a direct function of clock 1 and clock 2. With a 128 kHz clock, the band limiting frequency is 3.6 kHz. By dividing the clock in half to 64 kHz, the band limiting frequency is cut in half to 1.8 kHz (as illustrated in Figure 1). Likewise by doubling the clock, the cutoff point will double (as illustrated in Figures 3 and 4). The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 db. Because the MC145414 is a switch capacitance filter, the sampled output signal will have switching noise present near multiples of the switching frequency; a single-pole RC filter may be required to reduce this.

To provide 50/60 Hz and 15 Hz rejection, a 3-pole Chebychev highpass filter can be externally realized with the MC145414 by using the uncommitted op-amps as an active filter. This is shown in Figure 5 and 6.

FILTER B DESCRIPTION

Filter B in the MC145414 consists of a 5-pole elliptic tunable lowpass filter operating at a sampled rate determined by clock 1 and clock 2. Filter B is functionally similar to filter A, except filter B has unity gain.

Clock 1 and 2

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, VLS. Clock 1, 2 pins should be tied together.

Power Down

The MC145414 may be powered down by bringing VAG to within 1.7 V of V_{CC} or by bringing VLS to within 1.7 V of V_{DD}

2

FIGURE 1 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 64 kHz

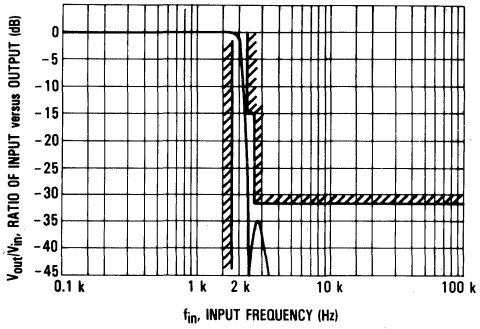


FIGURE 2 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 128 kHz

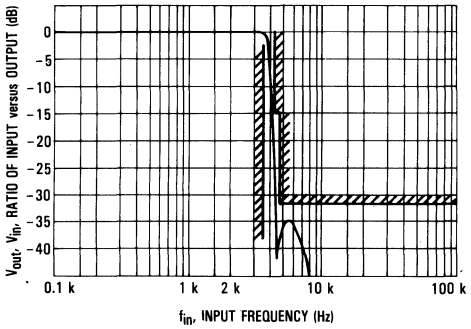


FIGURE 3 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 256 kHz

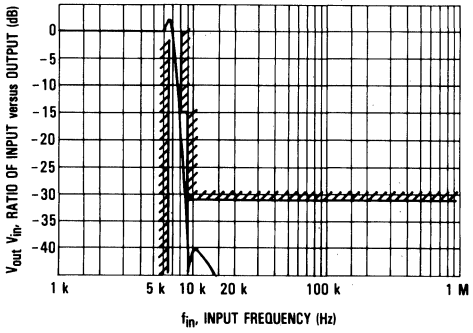


FIGURE 4 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 400 kHz

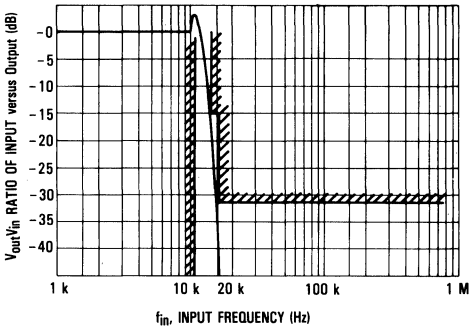
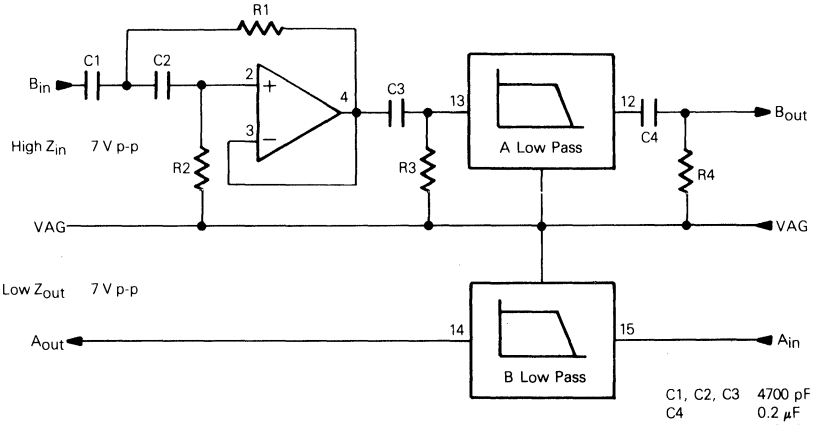


FIGURE 5 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECT FILTER

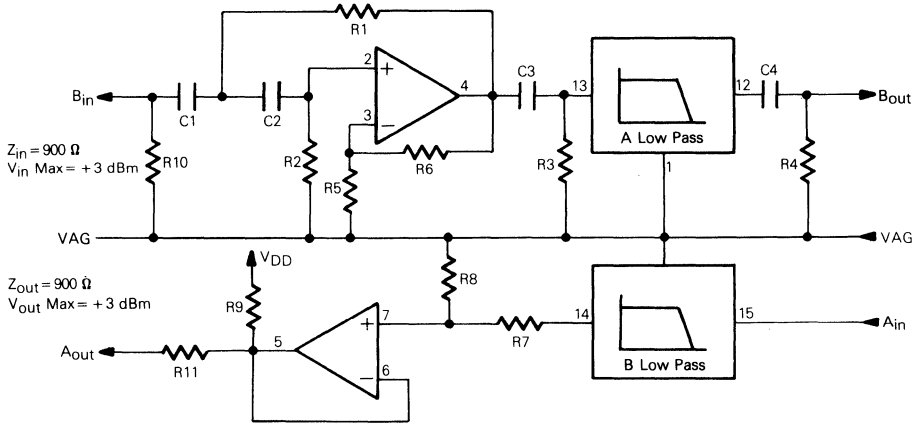


C1, C2, C3	4700 pF	±1%
C4	0.2 μF	−20% +80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

AD0318

FIGURE 6 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECTION AND 900 TERMINATION



C1, C2, C3	4700 pF	±1%	R6	169 kΩ ¼ W	1%
C4	0.2 μF	−20% +80%	R7	24 kΩ ¼ W	1%
R1	236 kΩ ¼ W	1%	R8	33 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%	R9	1.8 kΩ ¼ W	10%
R3	223 kΩ ¼ W	1%	R10	900 Ω ¼ W	1%
R4	100 kΩ ¼ W	10%	R11	900 Ω ¼ W	1%
R5	200 kΩ ¼ W	1%			

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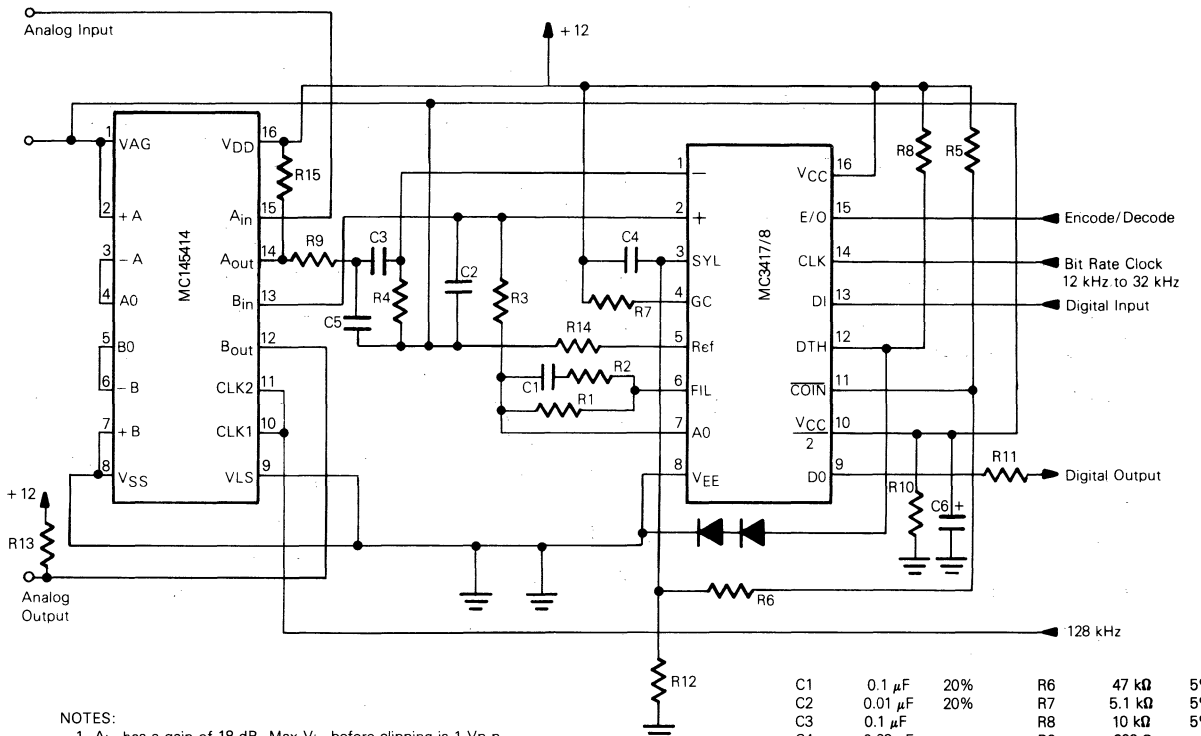
NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

FIGURE 7 — DELTAMOD VOICE DIGITIZER USING MC3417 AND MC145414



NOTES:
1. A_{in} has a gain of 18 dB. Max V_{in} before clipping is 1 Vp-p.
2. Clock must be full V_{DD} to V_{SS} swing.
3. Digital I/O on MC3417/18 is TTL compatible.

C1	0.1 μF	20%	R6	47 kΩ	5%
C2	0.01 μF	20%	R7	5.1 kΩ	5%
C3	0.1 μF		R8	10 kΩ	5%
C4	0.33 μF		R9	200 Ω	
C5	0.1 μF		R10	1 kΩ	
C6	10 μF		R11	4.7 kΩ	
R1	9.6 kΩ	5%	R12	22 M	
R2	400 kΩ	5%	R13	2 kΩ	
R3	7.5 kΩ	5%	R14	10 kΩ	
R4	15 kΩ	5%	R15	2 kΩ	
R5	8.2 kΩ	5%			

MC145415

Advance Information

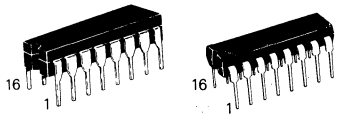
DUAL TUNABLE LINEAR PHASE LOW-PASS SAMPLED DATA FILTERS

The MC145415 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two uncommitted comparators for use elsewhere in the system.

- Two Linear Phase 5th Order Low-Pass Filters
- Low Operating Power Consumption — 20 mW (Typical)
- ±2.5 to ±8 Volt Power Supply Ranges
- CMOS Compatible Inputs Using V_{DG} Pin
- Two Comparators Available to Reduce Component Count
- Useful in High Speed Data Modem Applications
- Pass-Band Edges Tunable With Clock Frequency from 1.25 kHz to 10 kHz

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

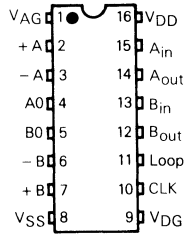
DUAL TUNABLE
LINEAR PHASE LOW-PASS
SAMPLED DATA FILTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

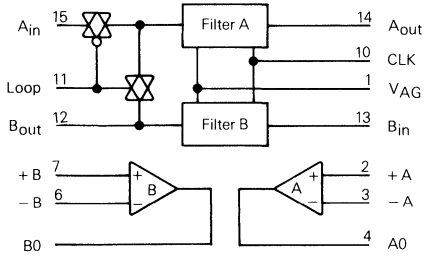
PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



V_{DG} = Pin 9
V_{DD} = Pin 16

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MAXIMUM RATINGS (V_{SS} = 0)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	5	16	V
Clock Frequency*	CLK	50	128	400	kHz

*Filter frequency response may degrade slightly as clock frequency is increased above 200 kHz.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0 V, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic	Symbol	Min	Max	Unit
Operating Current	I_{DD}	–	4	mA
Input Capacitance	C_{in}	–	10	pF
Input Low Voltage (Pins 10, 11)	V_{IL}	–	V_{DG} + 0.3 (V_{DD} − V_{DG})	V
Input High Voltage (Pins 10, 11)	V_{IH}	0.7 × (V_{DD} − V_{DG}) + V_{DD}	–	V
Input Leakage Current (Pins 10, 11)	I_{IL}	V_{DD} − 0.3 (V_{DD} − V_{DG})	2.5	μA
V_{DG} Reference Voltage (Pin 9)	V_{DG}	V_{SS}	V_{DD} − 4.5	V

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, V_{SS} = 0, V_{AG} = V_{DD}/2, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±10	μA
Input Current	V_{AG}	I_{in}	–	±0.00001	±50	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±1.0	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range	A_{out}, B_{out}	V_{OR}				V
(R_L = 20 kΩ to V_{AG}, R_B = ∞)			1.5	–	10.5	
(R_L = 900 Ω to V_{AG}, R_B = 1.8 kΩ to V_{DD})			2.5	–	9.0	
(R_L = 600 kΩ to V_{AG}, R_B = 1.6 kΩ to V_{DD})			3.0	–	8.3	
Small Signal Output Impedance (1 kHz)	A_{out}	Z_o	–	50	–	Ω
	B_{out}		–	50	–	
Output Current						
(V_O = 10.5 V)	A_{out}, B_{out}	I_{OH}	−200	−400	–	μA
(V_O = 1.5 V)	A_{out}, B_{out}	I_{OL}	5	7.5	–	mA
Comparator Output Current	A0, B0					
(V_O = 9.5 V)		I_{OH}	−1.1	−2.25	–	mA
(V_O = 0.5 V)		I_{OL}	−3.0	−8.8	–	

FILTER A SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 0.875 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	17	18	19	dB
Responses (Ref. 300 Hz)				dB
2400 Hz	−3.6	−3.0	−2.4	
4800 Hz	−16	−13.8	−12.8	
Idle Noise (A_{in} = V_{AG}, Ref. to 600 Ω)	–	13	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	87	–	dB
Deviation From Linear Phase dc to 2400 Hz	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V + 0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (A_{in} = V_{AG}, B_{in} = 0 dBm0, Output at A_{out} at 3 kHz)	–	76	–	dB

FILTER B SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock = 153.6 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V p-p, T_A = −40 to 85°C)

Characteristic	Min	Typ	Max	Unit
Gain (300 Hz)	−0.7	±0.15	+0.7	dB
Response (Ref. 300 Hz)				dB
2400 Hz	−3.6	−3.0	−2.4	
4800 Hz	−16	−14.1	−12.8	
Idle Noise (300 Hz, Ref to 600 Ω)	–	9	24	dBrnc
Dynamic Range (Full Scale Output/Idle Noise)	76	91	–	dB
Deviation From Linear Phase (dc to 2400 Hz)	–	2.5	–	deg
Power Supply Rejection Ratio (V_{DD} = 12 V + 0.1 V_{RMS} @ 1 kHz)	–	36	–	dB
Crosstalk (B_{in} = V_{AG}, A_{in} = 0 dBm0 @ 2 kHz, Output at B_{out})	–	76	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 12$ V, $T_A = -40$ to 85°C)

Characteristics	Symbol	Min	Typ	Max	Units
Input Rise Time (Pin 10)	t_{TLH}	–	–	4	μs
Input Fall Time (Pin 10)	t_{THL}	–	–	4	μs
Pulse Width (Pin 10)	t_{WH}	200	–	–	ns
Clock Pulse Frequency (Pin 10)	f_{CL}	50	–	400	kHz
Clock Duty Cycle (Pin 10)	–	40	–	60	%

2

FUNCTIONAL DESCRIPTION OF PINS

V_{DD} (PIN 16)
Positive supply pin.

V_{SS} (PIN 8)
This is the most negative supply pin.

V_{AG}, ANALOG GROUND (PIN 1)
This pin should be held at approximately $(V_{DD} - V_{SS})/2$. All analog inputs and outputs are referenced to this pin.

+A (PIN 2)
Non-inverting input of comparator A.

–A (PIN 3)
Inverting input of comparator A.

A0 (PIN 4)
Output of comparator A. This is a standard 'B' series CMOS output.

B0 (PIN 5)
Output of comparator B. This is a standard 'B' series CMOS output.

–B (PIN 6)
Inverting input of comparator B.

+B (PIN 7)
Non-inverting input of comparator B.

V_{DG}, DIGITAL GROUND (PIN 9)
This pin is logic ground reference for the CLK and LOOP pins.

CLK, CLOCK (PIN 10)
This is the clock input that determines the location of the cutoff frequency of the filters as given below:

$$-3 \text{ dB frequency} = f_{CLK} \div 64$$

LOOP (PIN 11)
When this pin is high, the input to filter A is disconnected from the pad and shorted to the filter B output pin. With this pin low, the loop back mode is disabled.

B_{out}, LOW-PASS FILTER B OUTPUT (PIN 12)
This is the output from Filter B.

B_{in}, LOW-PASS FILTER B INPUT (PIN 13)
This is the input to filter B.

A_{out}, LOW-PASS FILTER A OUTPUT (PIN 14)
This pin is the output from Filter A.

A_{in}, LOW-PASS FILTER A INPUT (PIN 15)
This is the input to Filter A.

NOTE: V_{AG} is a high-impedance input.

FILTER DESCRIPTION

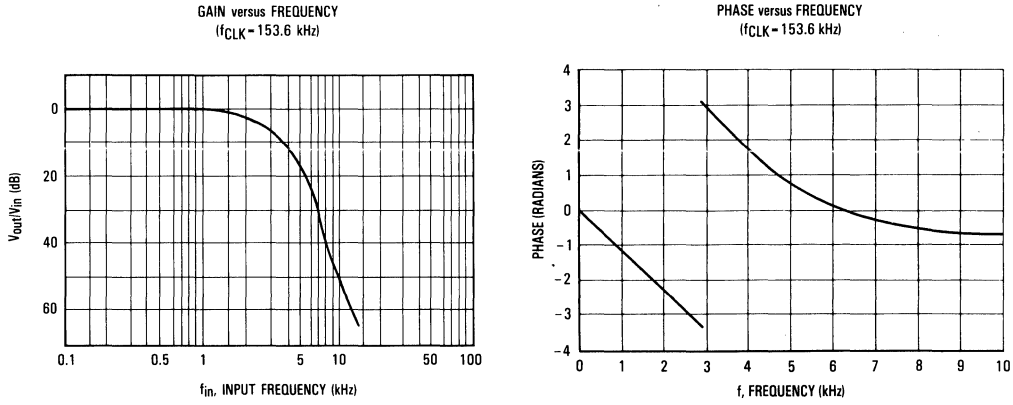
FILTER A DESCRIPTION

Filter A of the MC145415 is a 5-pole tunable linear phase low-pass filter operation at a sampling rate determined by the clock. The break frequency, which is a function of the clock, is calculated by dividing the input clock frequency by 64. With a 128 kHz clock, the band limiting frequency is 2 kHz. By dividing the clock in half to 64 kHz the band limiting frequency is cut in half to 1 kHz. Likewise, by doubling the clock, the cutoff point with double in frequency. The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 dB. Because the MC145415 is a switch capacitance filter, the sampled output signal will have switching components present near multiples of the switching frequency and inputs to these filters should be band-limited to under ~3/4 f_{CLK} to prevent aliasing.

FILTER B DESCRIPTION

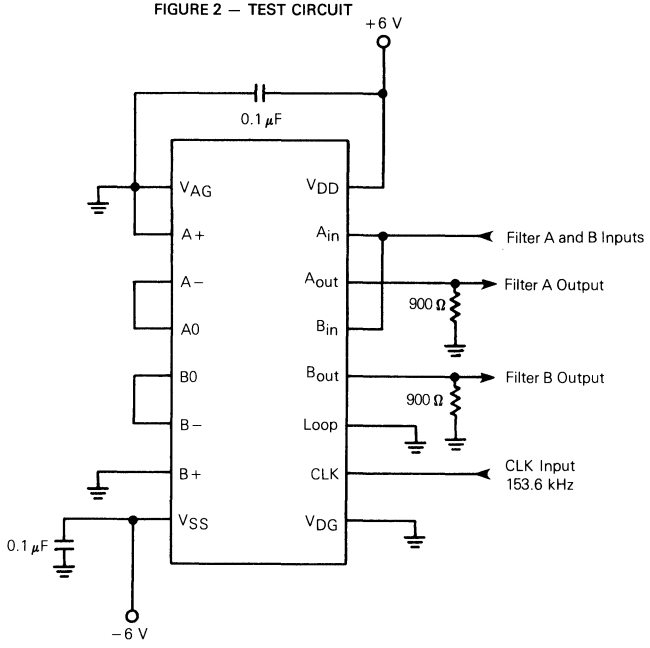
Filter B in the MC145415 consists of a 5-pole tunable linear phase low-pass filter operating at a sampled rate determined by the clock. Filter B is functionally similar to filter A, except filter B has unity gain.

FIGURE 1 — FILTER A AND B LOW-PASS CHARACTERISTICS



NOTES: 1. Break frequency is equal to the clock frequency ÷ 64.
2. Figure 1 illustrates Filter B performance.
Filter A would be 18 dB higher.

FIGURE 2 — TEST CIRCUIT



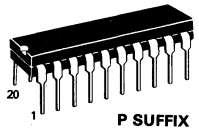
MC145416

2

Product Preview

Tone/Pulse Repertory Dialer with Flash

HCMOS



P SUFFIX
PLASTIC
CASE 738

The MC145416 is a member of the Motorola HCMOS dialer family. In addition to the necessary basic features of pulse, tone, or mixed dialing, and 10 × 18 memories inclusive of LNR, it provides the advanced features of flash, 3 × 18 dedicated memories, signal output inhabited during memory storage, note pad programming, and convenient operation sequence by 5 × 4 keyboard interface.

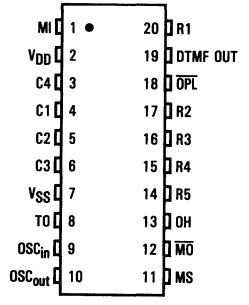
The power-on memory reset has the highest priority if the voltage drops below the minimum voltage level, regardless of hook switch status, to ensure no wrong data in memory content.

The pin-out is compatible with other members of dialer family except the additional two pins at one end of the device (pins 1 and 20).

Options: MC145416-1 40/60 make-break ratio with indefinite pause
MC145416-2 33/67 make-break ratio with 4 ms pause

Other feature combinations can be done as a special part upon customer request.

PIN ASSIGNMENT



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC145418
MC145419

2

Advance Information

Digital Loop Transceivers (DLT)

The MC145418 and MC145419 DLTs are high-speed data transceivers that provide 80 kbps full duplex data communication. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in any digital data transfer scheme (i.e., limited distance modems) where bidirectional data transfer is needed. These devices utilize a 256 kilobaud "squared" modified - DPSK burst modulation technique for transmission.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The DLT chip set consists of the MC145418 master DLT for use at the telephone switch linecard and the MC145419 slave DLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 kbps Voice/Data Channel and Two 8 kbps Signalling/Data Channels
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes
- Full Duplex 80 Kilobits Transmission for an 8 kHz Frame Rate
- Protocol Independent
- Single 5 Volt Power Supply
- 22 Pin Package

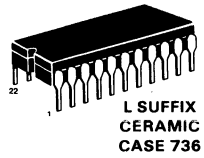
NOT RECOMMENDED FOR NEW DESIGN

MC145418 Master DLT

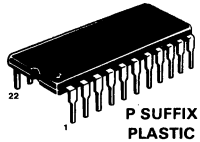
- Pin Controlled Power-Down Feature
- Signalling and Control I/O Capable of Sharing Common Bus Wiring with Other DLTs
- Variable Data Clock - 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbps Channel into LSB of 64 kbps Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145419 Slave DLT

- Compatible with MC14400 Series PCM Mono-Circuits
- Pin Controlled Loop-Back Feature
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

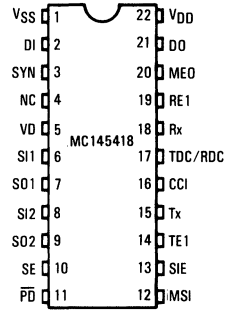


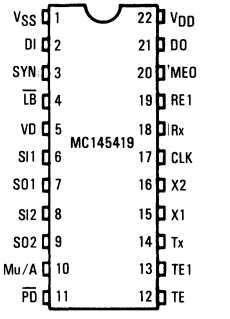
L SUFFIX
CERAMIC
CASE 736



P SUFFIX
PLASTIC
CASE 708

PIN ASSIGNMENTS

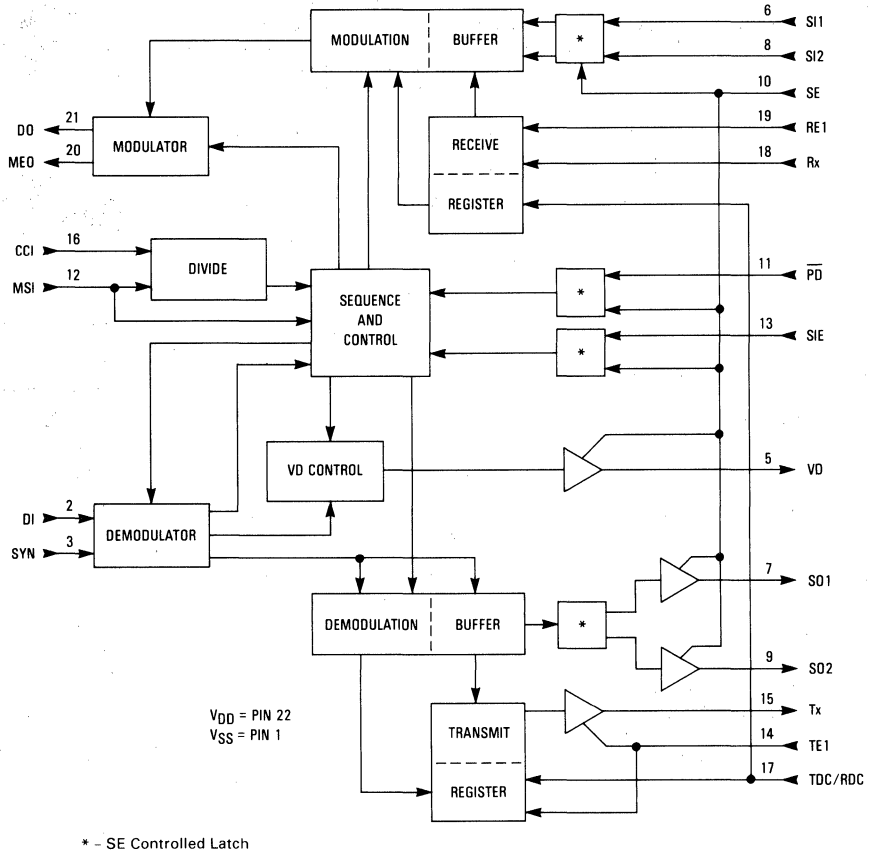




This document contains information on a new product. Specifications and information herein are subject to change without notice.

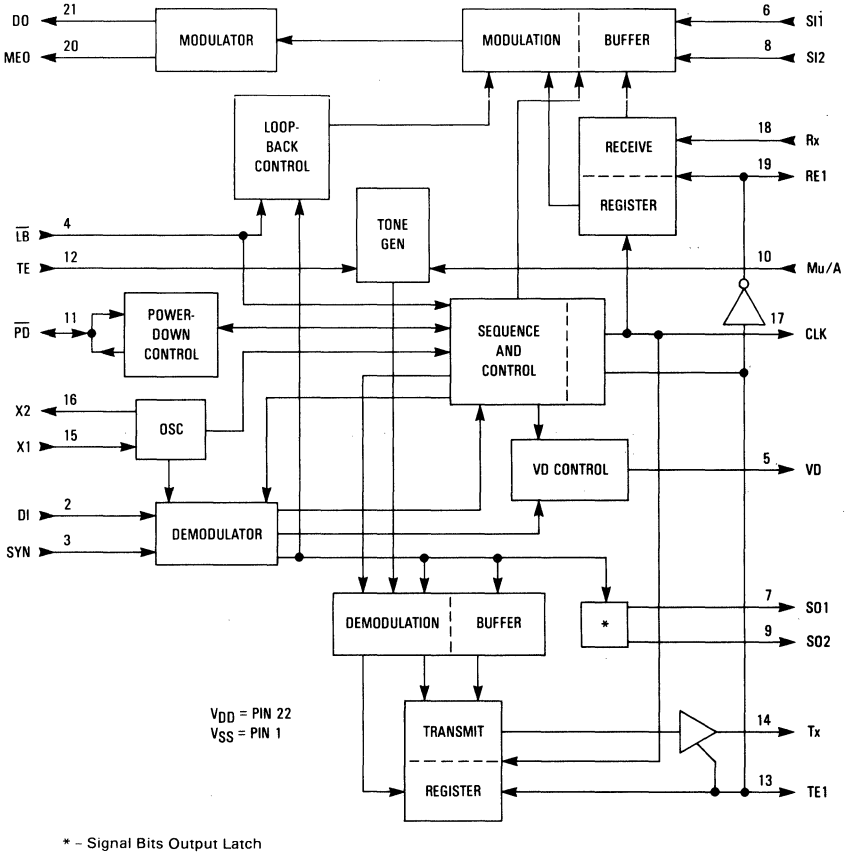
2

MC145418 MASTER DLT BLOCK DIAGRAM



* - SE Controlled Latch

MC145419 SLAVE DLT BLOCK DIAGRAM



2

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} - V_{SS}	-0.5 to 9.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-85 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation ($\overline{PD}$ = V_{DD}, V_{DD} = 5 V)	V_{DD}	—	15	mW
Power Dissipation ($\overline{PD}$ = V_{SS}, TE = V_{SS})	V_{DD}	—	10	mW
Frame Rate MC145418	MSI	7.9	8.1	kHz
MC145418 - MC145419 Frame Rate Slip (See Note 1)	—	—	0.25	%
CCI Clock Frequency (MSI = 8 kHz)	CCI	—	2.048	MHz
Data Clock Rate MC145418	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	DO	—	256	kHz

NOTES:
1. The MC145419 crystal frequency divided by 512 must equal the MC145418 MSI frequency ± 0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145419 and 2.048 MHz CCI for the MC145418.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current		—	±1.0	μA
Input Capacitance		—	10	pF
Output High Current (Except Tx on MC145418 and Tx and $\overline{PD}$ on MC145419)	V_{OH} = 2.5 V V_{OH} = 4.6 V	-1.7 -0.36	— —	mA
Output Low Current (Except Tx on MC145418 and Tx and $\overline{PD}$ on MC145419)	V_{OL} = 0.4 V V_{OL} = 0.8 V	0.36 0.8	— —	mA
$\overline{PD}$ Output High Current (MC145419) (See Note 5)	V_{OH} = 2.5 V V_{OH} = 4.6 V	-90 -10	— —	μA
$\overline{PD}$ Output Low Current (MC145419) (See Note 5)	V_{OL} = 0.4 V V_{OL} = 0.8 V	60 100	— —	μA
Tx Output High Current	V_{OH} = 2.5 V V_{OH} = 4.6 V	-3.4 -0.7	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	1.7 3.5	— —	mA
Tx Input Impedance (TE1 = V_{SS}, MC145418)		100	—	kΩ
Crystal Frequency (MC145419) (See Note 3)		4.0	4.4	MHz
PCM Tone (TE = V_{DD}, MC145419)		-22	-18	dBm0
Three-State Current (SO1, SO2, VD, Tx on MC145418, Tx on MC145419)		—	±1	μA
X2 - Oscillator Output High Drive Current (MC145419) (See Note 4)	V_{OH} = 4.6 V	-450	—	μA
X2 - Oscillator Output Low Drive Current (MC145419) (See Note 4)	V_{OL} = 0.4 V	450	—	μA

NOTES:
3. The MC145419 crystal frequency divided by 512 must equal the MC145418 MSI frequency ±0.25% for optimum performance.
4. Output drive when X1 is being driven from an external clock.
5. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

MC145418 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	μs
Input Fall Time	All Digital Inputs	1	t_f	—	4	μs
Pulse Width	TDC/RDC, RE1, MSI	1	$t_{W(H,L)}$	90	—	ns
CCI Duty Cycle		1	$t_{W(H,L)}$	45	55	%
Data Clock Frequency	TDC/RDC	—	t_{DC}	64	2560	kHz
Propagation Delay Time						
MSI to SO1, SO2, VD ($\overline{PD}$ = V_{DD})		2	t_{PLH}, t_{PHL}	—	90	ns
TDC to Tx		3		—	90	
MSI to TDC/RDC Setup Time			t_{su3}	90	—	ns
		4	t_{su4}	40	—	
TE1/RE1 to TDC/RDC Setup Time			t_{su3}	90	—	ns
		4	t_{su4}	40	—	
Rx to TDC/RDC Setup Time		5	t_{su5}	60	—	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	—	ns
DO Valid to MEO Rising		10	t_{p7}	—	90	ns
DO Valid to MEO Falling		10	t_{p8}	—	90	ns
DI Valid to SYN Rising		11	t_{su7}	488	1200	ns
DI Valid to SYN Falling		11	t_{su8}	—	3900	ns

MC145419 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	—	4	μs
Input Fall Time	All Digital Inputs	1	t_f	—	4	μs
Clock Output Pulse Width	CLK	1	$t_{W(H,L)}$	3.8	4.0	μs
Crystal Frequency		—	f_{X1}	4.086	4.1	MHz
Propagation Delay Times						ns
TE1 Rising to CLK (TE = V_{DD})		7	t_{p1}	-50	50	
TE1 Rising to CLK (TE = V_{SS})		7	t_{p1}	438	538	
CLK to TE1 Falling		7	t_{p2}	—	40	
CLK to RE1 Rising		8	t_{p3}	—	40	
RE1 Falling to CLK (TE = V_{DD})		8	t_{p4}	-50	50	
RE1 Falling to CLK (TE = V_{SS})		8	t_{p4}	438	538	
CLK to Tx		9	t_{p5}	—	90	
TE1 to SO1, SO2		9	t_{p6}	—	90	
Rx to CLK Setup Time		5	t_{su5}	60	—	ns
Rx to CLK Hold Time		5	t_{h1}	60	—	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	—	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	—	ns

2

TIMING DIAGRAMS

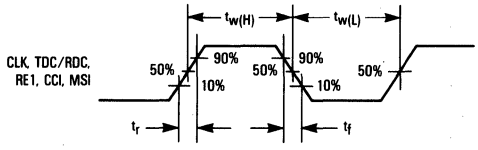


Figure 1

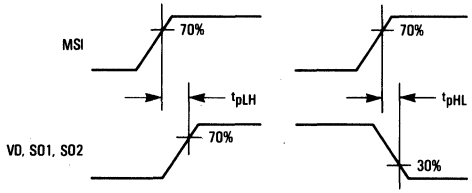


Figure 2

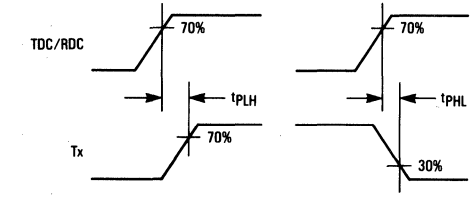


Figure 3

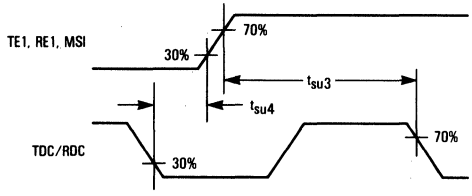


Figure 4

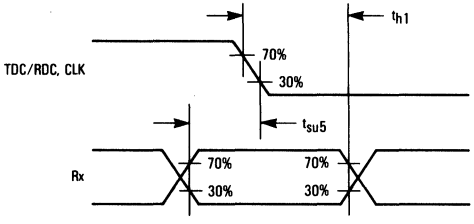


Figure 5

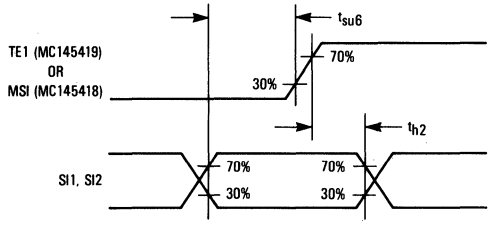


Figure 6

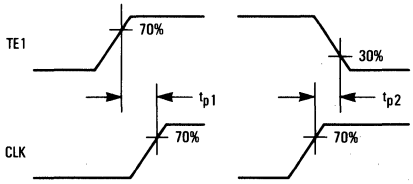


Figure 7

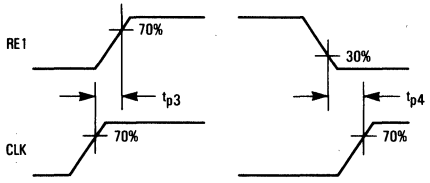


Figure 8

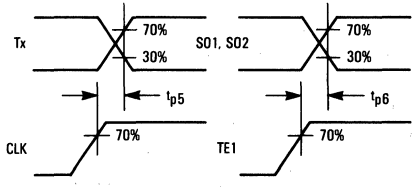


Figure 9

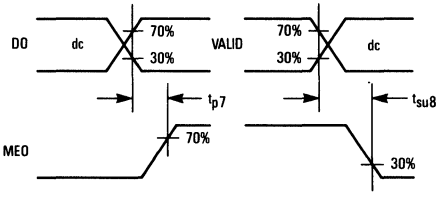


Figure 10

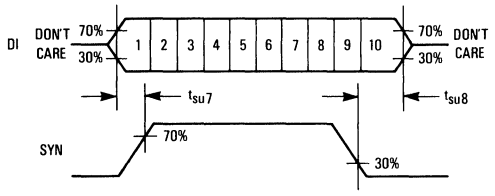


Figure 11

MC145418 MASTER DLT PIN DESCRIPTIONS

V_{DD} — POSITIVE SUPPLY

Normally 5 volts.

V_{SS} — NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

DI — DATA INPUT

This input to the demodulator circuit should be a squared and limited version of the received line signal. (See Figure 15.)

SYN — SYNC INPUT

This input to the demodulator circuit should be a signal which is high when signal energy is detected on the line. (See Figure 14 for typical line interface circuit.)

This signal should be the output of a window comparator with a threshold of approximately 40% of the smallest received line signal. (See Figure 15.)

NC — NO CONNECTION

This pin is not available for use and should be left floating.

VD — VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B-series CMOS output and is high impedance when SE is held low.

SI1, SI2 — SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2 — SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the slave DLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B-series CMOS drive capability and are high impedance if the SE pin is held low.

SE — SIGNAL ENABLE INPUT

If held high, the $\overline{PD}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the states of these inputs are latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other DLTs to a common controller.

$\overline{PD}$ — POWER-DOWN INPUT

If held low, the DLT ceases modulation. In power-down, the only active circuitry is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the DLT powers up, and waits three positive MSI edges or until the end of an incoming transmission from the slave DLT and begins transmitting every MSI period to the slave DLT on the next rising edge of the MSI.

MSI — MASTER SYNC INPUT

This pin is the master 8 kHz input system sync and inititates modulation. MSI should be approximately leading-edge aligned with TDC/RDC.

SIE — SIGNAL INSERT ENABLE

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in its place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have its LSB forced low in this mode. In this manner, signal bit 2 to/from the slave DLT is inserted into the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1 — TRANSMIT DATA ENABLE 1 INPUT

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high-impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading-edge aligned.

Tx — TRANSMIT DATA OUTPUT

This three-state output pin presents new voice data on the rising edges of TDC/RDC when TE1 is high. (See TE1.)

CCI — CONVERT CLOCK INPUT

A 2.048 MHz clock signal should be applied to this pin. This signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC — TRANSMIT/RECEIVE DATA CLOCK

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the DLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading-edge aligned with MSI.

Rx — RECEIVE DATA

Voice data is clocked into the DLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1 — RECEIVE DATA ENABLE 1 INPUT

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next falling edges of the data clock, RDC. RE1 and RDC should be approximately leading-edge aligned.

DO — DATA OUTPUT

This B-series output is the square wave Modified - DPSK modulation waveform to be externally buffered and applied to the line. This output is valid only when the MEO output pin is high and is undefined while MEO is low. The external line driver should drive the line in a tri-level manner, controlled by DO and MEO as shown in Figure 15.

MEO — MODULATION ENABLE OUTPUT

This pin, when high, defines the valid data at the DO pin to be valid.

MC145419 SLAVE DLT PIN DESCRIPTIONS

V_{DD} — POSITIVE SUPPLY

Normally 5 volts.

V_{SS} — NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

DI — DATA INPUT

This input to the demodulator circuit should be a squared and limited version of the received line signal. (See Figure 15.)

SYN — SYNC INPUT

This input to the demodulator circuit should be a signal which is high when signal energy is detected on the line. (See Figure 14 for typical line interface circuit.)

This signal should be the output of a window comparator with a threshold of approximately 40% of the smallest received line signal. (See Figure 15.)

$\overline{LB}$ — LOOP-BACK CONTROL

When this pin is held low and $\overline{PD}$ is high (the DLT is receiving transmissions from the master), the DLT will use the eight bits of demodulated PCM data in place of the eight bits of Rx data in the return burst to the master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loop-back operation.

VD — VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master. (See TE pin description for the one exception to this.)

SI1, SI2 — SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2 — SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the master DLT and change state on the rising edge of TE1. These outputs have standard B-series CMOS output drive capability.

$\overline{PD}$ — POWER-DOWN INPUT/OUTPUT

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the DLT is powered down and the only active circuitry is: that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation: the outputting of data received from the master and updating of VD status. When held high, the DLT is powered up and transmits in response to received transmissions from the master. If no received bursts from the master have occured when powered up, for 250 μs (derived from the internal oscillator frequency), the DLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave DLT to self power-up and down in demand powered-loop systems.

TE — TONE ENABLE

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono-circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the mono-circuit. This feature allows the user to provide audio feedback for the telset keyboard depressions except during loop-back. During loop-back of the slave DLT, CLK is defeated so a tone cannot be generated in this mode.

TE1 — TRANSMIT DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for eight CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx — TRANSMIT DATA OUTPUT

This is a standard B-series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high-impedance when TE1 is low.

X1 — CRYSTAL INPUT

A 4.096 MHz crystal is tied between this pin and X2. A 10 MΩ resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to insure start-up. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2 — CRYSTAL OUTPUT

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance. (See X1.)

CLK — CLOCK OUTPUT

This is a standard B-series CMOS output which provides the data clock for the telset mono-circuit. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master; however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx — RECEIVE DATA INPUT

Voice data from the telset mono-circuit is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A — TONE DIGITAL FORMAT INPUT

This pin determines if the PCM code of the 500 Hz square wave tone, generated when TE is high, is D3 (Mu/A = 1) or CCITT (Mu/A = 0) format.

RE1 — RECEIVE DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which is the inverse of TE1 (see TE1). Data is clocked into Rx on the falling edges of CLK while RE1 is high.

DO — DATA OUTPUT

This B-series output is the square wave Modified-DPSK modulation waveform to be externally buffered and applied to the line. This output is valid only when the MEO output pin is high and is undefined while MEO is low. The external line driver should drive the line in a tri-level manner, controlled by DO and MEO as shown in Figure 15.

MEO — MODULATION ENABLE OUTPUT

This pin, when high, defines the valid data at the DO pin to be valid.

BACKGROUND

The MC145418 Master and MC145419 Slave DLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec/filter-digital PABX backplane interface over transmission mediums such as telephone wire pairs or fiber optics. This allows the remoting of the mono-circuit in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the DLT allows each PABX subscriber direct access to the inherent 64 kbps data routing capabilities of the PABX.

The DLT provides a means for transmitting and receiving 64 kbps of voice data and 16 kbps of signaling data. The DLT is a two chip set consisting of a Master and a Slave. The master DLT replaces the codec/filter and SLIC on the PABX linecard, and transmits and receives data over the intended transmission medium to the telset. The DLT appears to the linecard and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The slave DLT is located in the telset and interfaces the mono-circuit to the transmission medium. By hooking two DLTs back-to-back, a repeater can also be formed. The master and slave DLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The communication between master and slave DLTs require a single data link in the transmission medium. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half duplex manner; i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master. Transmission occurs at 256 kHz bit rate using a "squared" modified form of DPSK. This "ping-pong" mode will allow transmission of data at distances up to 2 km before turnaround delay becomes a problem. The DLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched 64 kbps voice or data communications throughout its service area by simply replacing a subscriber's linecard and telset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. The slave DLT has a loop-back feature by which the device can be tested in the user system.

The slave DLT has the additional feature of providing a 500 Hz Mu or A law coded square wave to the mono-circuit when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

Although the DLT was originally designed for a PABX environment, it can be used in any digital synchronous serial environment; such as, computer to computer communications or industrial control.

CIRCUIT DESCRIPTION

GENERAL

The DLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers inter-

face to the linecard or mono-circuit digital interface signals, the modulator and demodulator provide Modified - DPSK transmission and reception, while the intermediate data registers buffer data between these two sections. The DLT is intended to operate on a single 5 volt supply and can be driven by TTL or CMOS logic.

2

MASTER OPERATION

In the master, data is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the received voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI rising edge and formats the ten bits into a specific order. This data field is then transmitted in a 256 kHz "squared" Modified-DPSK burst to the remote slave DLT. An example of the modulated data field at DO is shown with the Modulation Enable Output (MEO) in Figure 15. V2-V1 is the differentially driven waveform onto the line in a twisted pair application.

The received signal coming into the demodulator should be a squared digital version of the line signal, shown as DI in Figure 15. The SYN signal which is the output of a window comparator is internally integrated and used by the demodulator's synchronization circuitry along with the first zero crossing of DI to establish the exact position (in time) of the incoming burst for demodulation purposes. The SYN pulse or pulses (output of the window comparator circuitry) must be present for the first eight baud periods of the incoming burst. They may persist longer but they must not occur within one full baud period before the arrival of the following burst. Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 12.

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming transmission from the master as indicated by the completion of demodulation. (The SYN signal and DI function the same as in the Master.) When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer. At the same time SO1, SO2, and VD are output. Modulation of the burst begins four 256 kHz periods after the completion of demodulation.

While TE1 is high, data is output at Tx on the rising edges of CLK. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and data is input to the receive register from the Rx pin on the next eight falling edges of CLK.

The CLK pin is a 128 kHz output that is formed by dividing down the 4.096 MHz crystal frequency by 32. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the 16th low period of CLK until the next completion of demodulation. This is shown in the slave DLT timing diagram of Figure 13.

POWER-DOWN OPERATION

In the master, when $\overline{PD}$ is low, the DLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the DLT receives a burst from the slave, the SO1, SO2, and VD pins will be updated upon completion of the demodulation instead of on the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master DLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power-up is loaded into the DLT during the RE1 period prior to the burst for Rx data, and on the present rising edge of MSI for signaling data.

In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the DLT slave is powered down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, the outputting of Tx data, signaling bits, and VD is active. When held high, the DLT slave is powered up and transmits normally in response to received transmissions from the master. If no bursts have been received from the master within 250 μs after power-up (derived from the internal oscillator frequency), the DLT generates an internal 125 μs free-running clock from the internal oscillator. The slave DLT then bursts a transmission to the master DLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave DLT to self power-up and down in demand powered-loop systems.

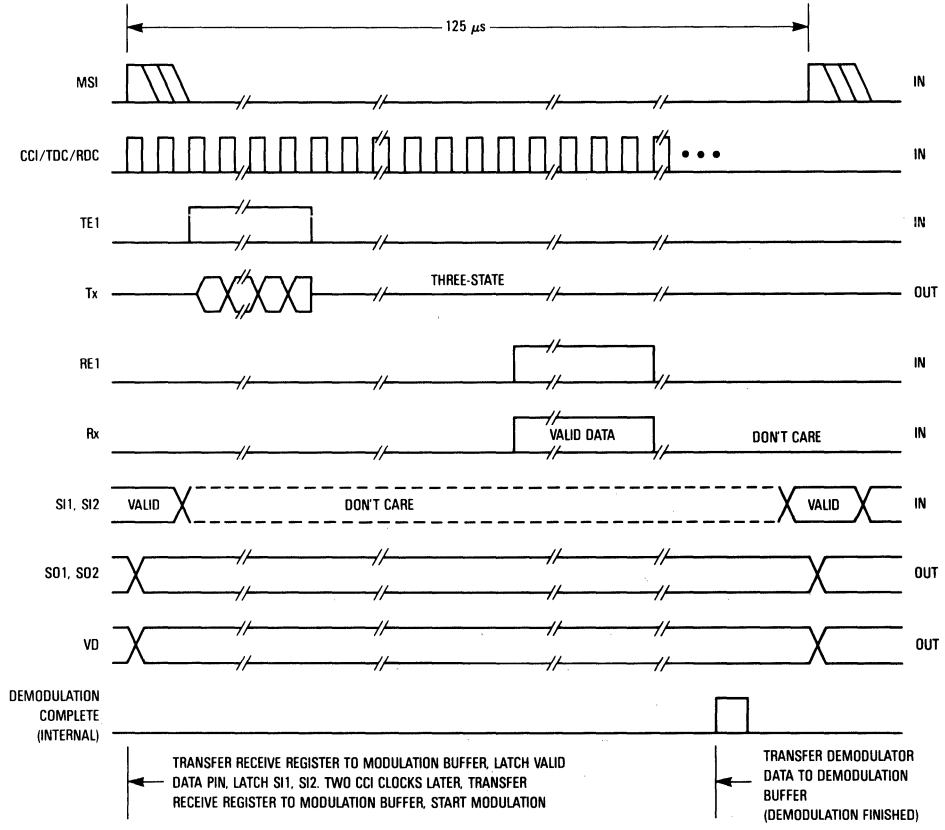


Figure 12. Master DLT Timing

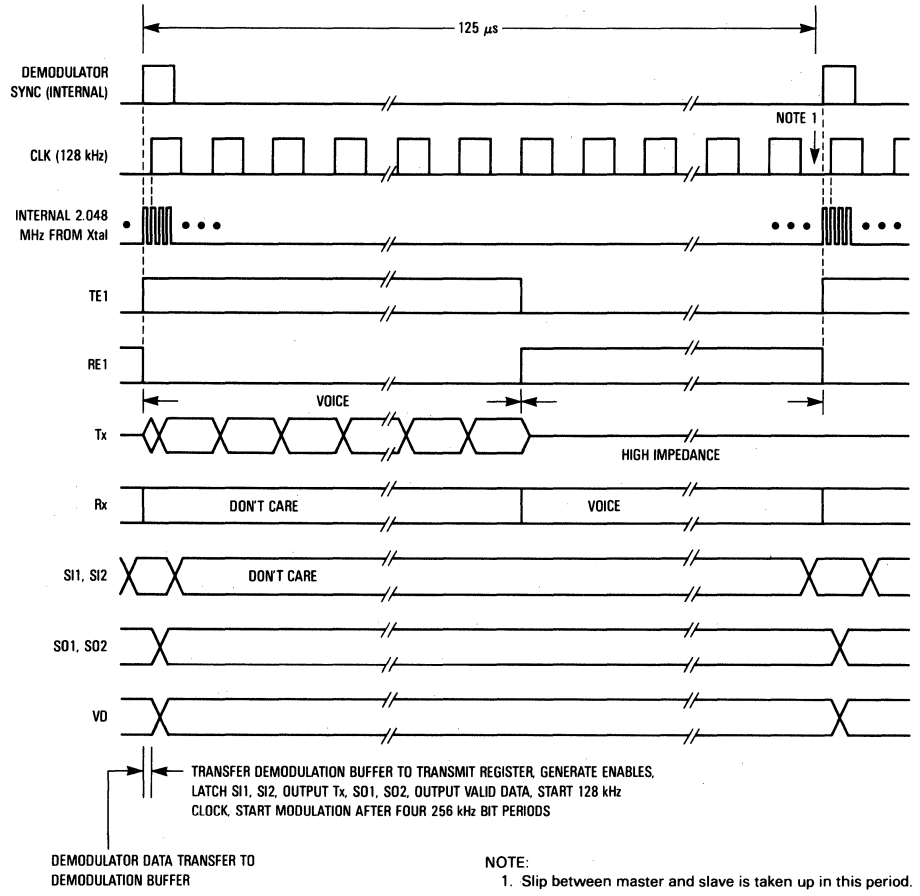


Figure 13. Slave DLT Timing

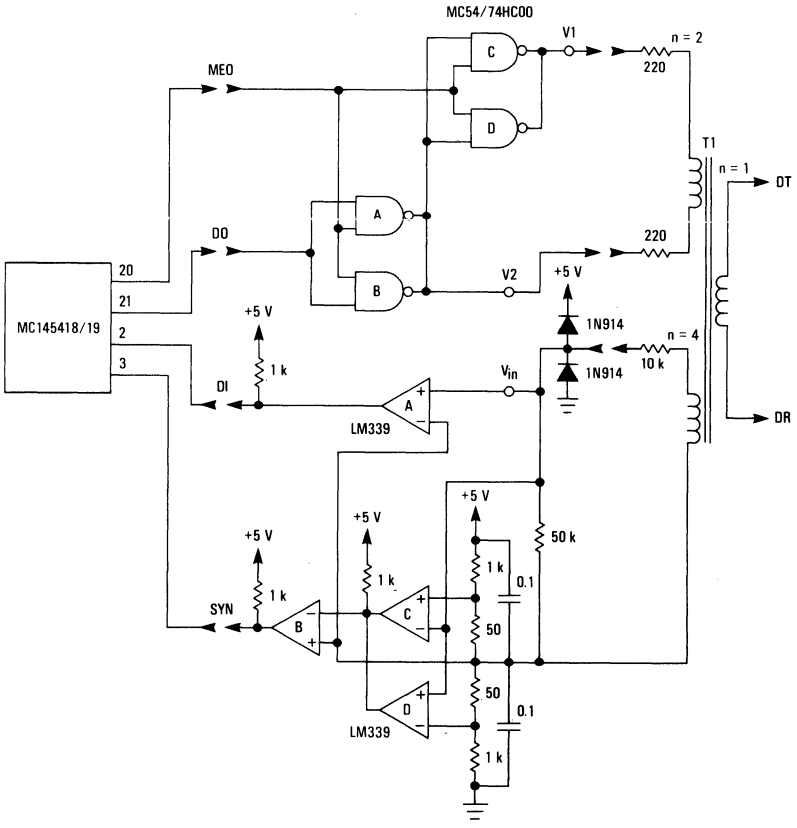
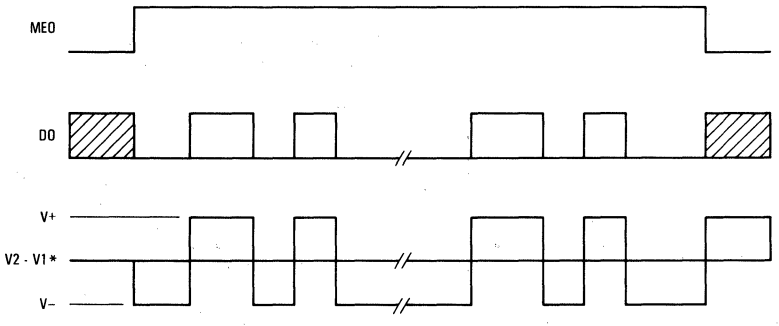
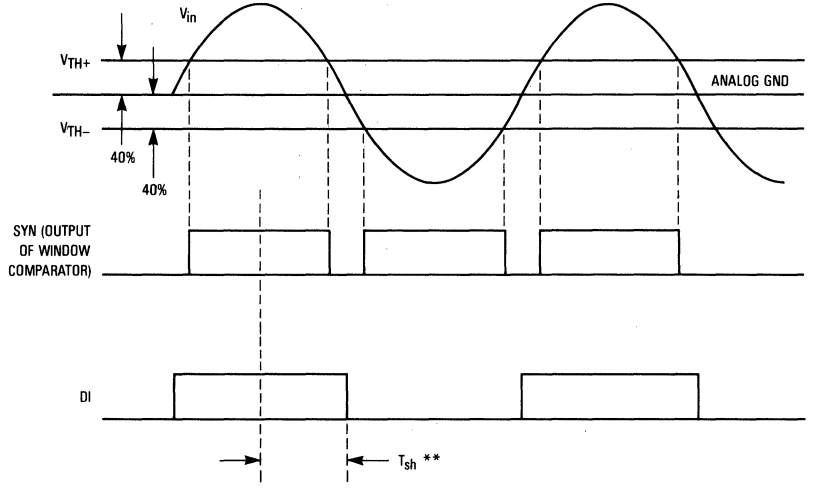


Figure 14. Typical DLT Line Interface



*See Figure 14 for voltages V2, V1. |V+| must equal |V–| within 5%.
V2-V1, when MEO is low, must equal (V+ - V–)/2 within 5%



**T_{sh} – SYN should be high a minimum of three 4.096 MHz clock periods before the first zero crossing as indicated by DI state change.

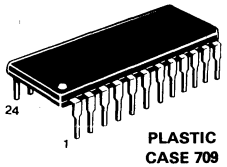
Figure 15. Line Driver Waveforms

MC145421
MC145425

2

Advance Information

ISDN Universal Digital Loop Transceivers II (UDLT II)



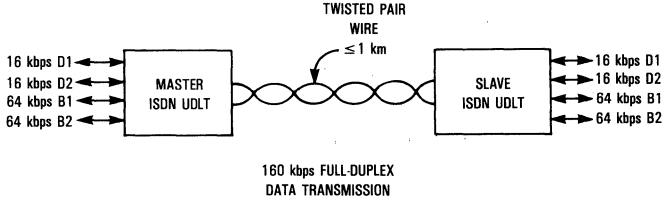
PLASTIC
CASE 709

The MC145421 and MC145425 UDLTs are high-speed data transceivers capable of providing 160 kbps full duplex data communication over 26 awg and larger twisted-pair cable up to 1 km in length. These devices are primarily used in digital subscriber voice and data telephone systems. In addition, the devices meet and exceed the CCITTs recommendations for data transfer rates of ISDNs on a single twisted pair. The devices utilize a 512 kilobaud MDPSK burst modulation technique to supply the 160 kbps full duplex data transfer rates. The 160 kbps rate is provided through four channels. There are two B channels, which are 64 kbps each. In addition, there are two D channels which are 16 kbps each.

The MC145421 and MC145425 UDLTs are designed for upward compatibility with the existing MC145422 and MC145426 80 kbps UDLTs, as well as compatibility with existing and evolving telephone switching hardware and software architectures.

The MC145421 (MASTER) UDLT is designed for use at the telephone switch line card while the MC145425 (SLAVE) UDLT is designed for use at the remote digital telset or data terminal.

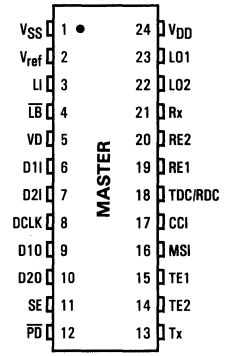
- Employs CMOS Technology, in Order to Take Advantage of Its Proven Capability for Complex Analog and Digital LSI Functions.
- Provides Synchronous Full Duplex 160 kbps Voice and Data Communication in a 2B + 2D Format For ISDN Compatibility.
- Provides the CCITT's Basic Access Data Transfer Rate (2B + D) for ISDNs on a Single Twisted Pair up to 1 km.
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes.
- Protocol Independent
- Single +5 V Power Supply



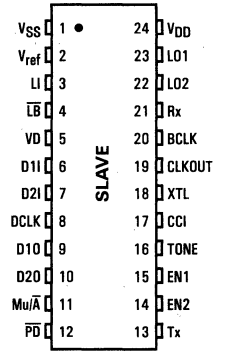
160 kbps FULL-DUPLEX
DATA TRANSMISSION

PIN ASSIGNMENTS

MC145421



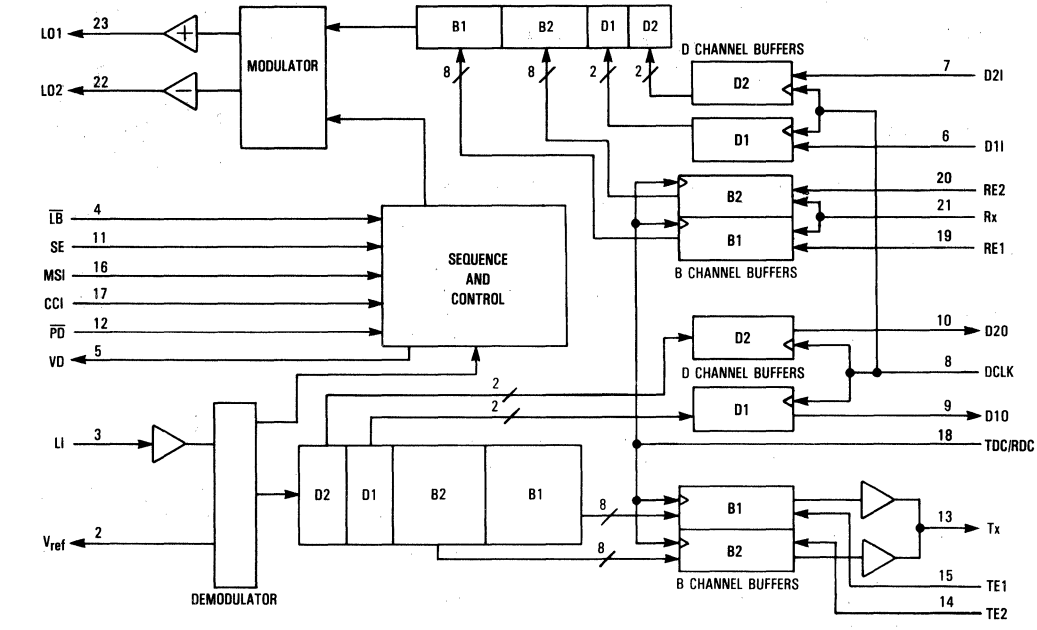
MC145425



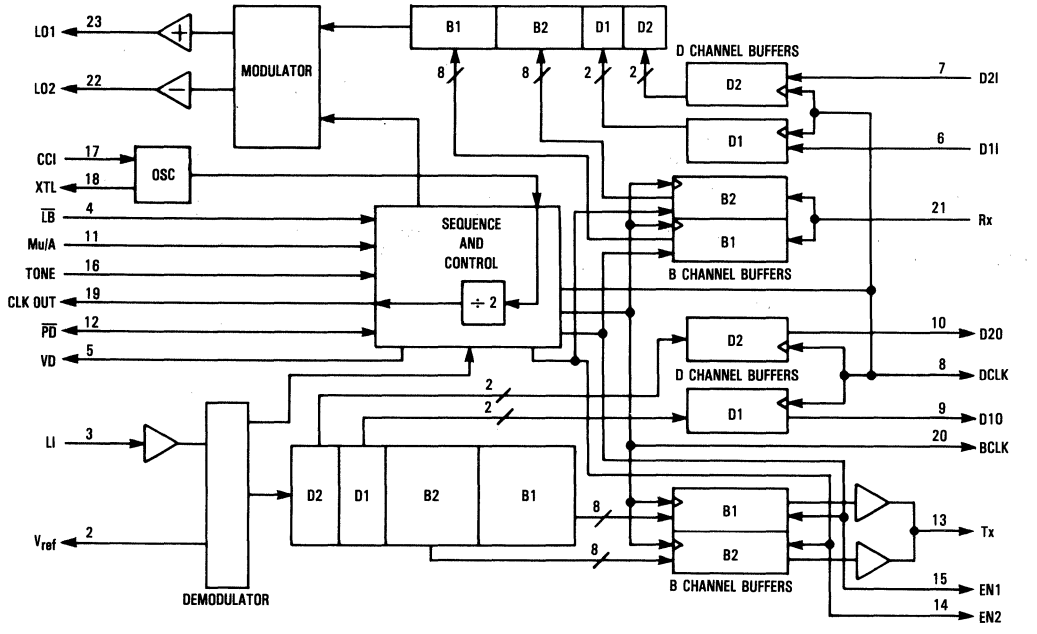
This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MC145421 MASTER ISDN BLOCK DIAGRAM



MC145425 SLAVE ISDN BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 6.5	V
Voltage Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = −40 to +85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Frame Rate MC145421 (See Note 1)	MSI	—	8.0	—	kHz
MC145421/25 Frame Slip Rate (See Note 1)	—	—	—	0.25	%
CCI Clock Frequency	—	—	8.192	8.29	MHz
TDC/RDC Data Clocks (for Master)	—	0.128	—	4.1	MHz
DCLK	—	0.016	—	4.1	MHz
Modulation Baud Rate (CCI/16)	LO1, LO2	—	512	—	kHz

NOTE:
1. The slave's crystal frequency divided by 1024 must equal the master's MSI frequency ±0.25% for optimum operation. Also, the 8.192 MHz input at the master divided by 1024 must be within 0.048% of the master's 8 kHz MSI clock frequency.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V, T_A = −40 to +85°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current, V_{DD}		—	15	mA
Input Current (Digital Pins)		—	5	μA
Input Capacitance		—	10	pF
Output High Current (Except Tx on Master and Slave, and $\overline{PD}$ on the Slave)	V_{OH}=2.5 V_{OH}=4.6	−1.7 −0.36	— —	mA
Tx Output High Current	V_{OH}=2.5 V_{OH}=4.6	−3.4 −0.7	— —	mA
$\overline{PD}$ (Slave Output High Current (See Note 2)	V_{OH}=2.5	—	−90	μA
Output Low Current (Except Tx on Master and Slave, and $\overline{PD}$ on Slave)	V_{OL}=0.4 V_{OL}=0.8	0.36 0.8	— —	mA
Tx Output Low Current	V_{OL}=0.4 V_{OL}=0.8	1.7 3.5	— —	mA
$\overline{PD}$ (Slave) Output Low Current (See Note 2)	V_{OL}=0.4	30	60	μA
Tx Three-State Impedance		100	—	kΩ
XTL Output High Current	V_{OH}=4.6	—	−450	μA
XTL Output Low Current	V_{OH}=0.4	450	—	μA

NOTE:
2. To overdrive $\overline{PD}$ from a low level to 3.5 V, or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter	Min	Max	Unit
Modulation Differential Amplitude RL = 880 Ω (LO1-LO2)	4.6	—	Vpeak
Modulation Differential DC Offset	—	40	mV
V_{ref} Voltage (Typically 9/20•(V_{DD} − V_{SS}))	2.0	2.5	V
PCM Tone Level	−22	−18	dBm
Demodulator Input Amplitude	50	—	mVpeak
Demodulator Input Impedance (LI to V_{ref})	200	300	kΩ

2

MC145421 MASTER PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY (PIN 24)

The most positive power supply pin, normally +5 volts with respect to V_{SS}.

V_{SS}—NEGATIVE SUPPLY (PIN 1)

The most negative supply pin and logic ground, normally 0 volts.

V_{ref}—REFERENCE OUTPUT (ANALOG GROUND) (PIN 2)

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external dc load should be placed on this pin.

LI—LINE INPUT (PIN 3)

This pin is an input to the demodulator for the incoming bursts. The input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LO1, LO2—LINE DRIVER OUTPUTS (PINS 23, 22)

These push-pull outputs drive the twisted pair transmission line with a 512 kHz modified DPSK (MDPSK) burst each 125 μs, in other words at an 8 kHz rate. When not modulating the line, these pins are driven to the active high state—being the same potential, they create an ac short. When used in conjunction with feed resistors, proper line termination is maintained.

SE—SIGNAL ENABLE INPUT (PIN 11)

At the time of a negative transition on this pin, an internal latch stores the states of $\overline{LB}$ and $\overline{PD}$ for as long as SE is held low. During this time, the VD, DO1, and DO2 outputs are driven to the high impedance state. When SE is high, all pins function normally.

$\overline{LB}$—LOOP BACK CONTROL (PIN 4)

A low level on this pin ties the internal modulator output to the internal demodulator input which loops the entire burst for testing purposes. During the loopback operation, the LI input is ignored and the LO1 and LO2 drivers are driven to the active high level. The state of this pin is internally latched if the SE pin is held low. This feature is only active when the $\overline{PD}$ input is high.

$\overline{PD}$—POWER DOWN INPUT (PIN 12)

When held low the ISDN UDLT powers down, except the circuitry that is necessary to demodulate an incoming burst and to output VD, B channel and D channel data bits. When $\overline{PD}$ is brought high, the ISDN UDLT powers up. Then, it begins transmitting every MSI period to the slave device, shortly after the rising edge of MSI. The state of this pin is latched if the SE pin is held low.

VD—VALID DATA OUTPUT (PIN 5)

A high level on this pin indicates that a valid line transmission has been demodulated. A valid transmission burst is determined by proper synchronization and the absence of detected bit errors. VD changes state on the rising edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a transmission burst and does not change again until three MSI rising edges have occurred, at which time it goes low, or until the next demodulation of a burst. VD is a standard B-series CMOS output and is high-impedance when SE is low.

MSI—MASTER SYNC INPUT (PIN 16)

This pin is the master, 8 kHz, frame reference input. The rising edge of MSI loads B and D channel data which had been input during the previous frame into the modulator section of the device and initiates the out-bound burst onto the twisted-pair cable. The rising edge of MSI also initiates the buffering of the B and D channel data demodulated during the previous frame. MSI should be approximately leading edge aligned with the TDC/RDC data clock input pin.

CCI—HIGH-SPEED CLOCK INPUT (PIN 17)

An 8.192 MHz clock should be supplied to this input. The 8.192 MHz input should be 50% duty cycle, however it may free-run with respect to all other clocks without performance degradation.

D1I, D2I—D CHANNEL SIGNALING BIT INPUTS (PINS 6, 7)

These inputs are 16 kbps serial data inputs. Two bits should be clocked into each of these inputs between the rising edges of the MSI frame reference clock. The first bit of each D channel is clocked into an intermediate buffer on the first falling edge of the DCLK following the rising edge of MSI. The second bit of each D channel is clocked in on the next negative transition of the DCLK. If further DCLK negative edges occur, new information is serially clocked into the buffer replacing the previous data one bit at a time. Buffered D channel data bits are burst to the slave device on the next rising edge of the MSI frame reference clock.

D1O, D2O—D CHANNEL SIGNAL OUTPUTS (PINS 9, 10)

These serial outputs provide the 16 kbps D channel signaling information from the incoming burst. Two data bits should be clocked out of each of these outputs between the rising edges of the MSI frame reference clock. The rising edge of MSI produces the first bit of each D channel on its respective pin. Circuitry then searches for a negative D clock edge. This tells the D channel data shift register to produce the second D channel bit on the next rising edge of the DCLK. Further positive edges of the DCLK recirculate the D channel output buffer information.

DCLK—D CHANNEL CLOCK INPUT (PIN 8)

This input is the transmit and receive data clock for both D channels. D channel input and output operation is described in the D1O, D2O pin description.

Tx—TRANSMIT DATA OUTPUT (PIN 13)

This pin is high impedance when both TE1 and TE2 are low. This pin serves as an output for B channel information received from the slave device. The B channel data is under the control of TE1, TE2, and TDC/RDC. (See TE1, TE2 description.)

Rx—RECEIVE DATA INPUT (PIN 21)

B channel data is input on this pin and is controlled by the RE1, RE2, and TDC/RDC pins. (See RE1, RE2 description.)

TE1, TE2—TRANSMIT DATA ENABLE INPUT (PIN 15)

These two pins control the output of data for their respective B channel on the Tx output pin. When both TE1 and TE2 are low, the Tx pin is high impedance. The rising edge of the respective enable produces the first bit of the selected B channel data on the Tx pin. Internal circuitry then scans for the next negative transition of the TDC/RDC clock. Following this event the next seven bits of the selected B channel data are output on the next seven rising edges of the TDC/RDC data clock. When TE1 and TE2 are high simultaneously, data on the Tx pin is undefined. TE1 and TE2 should be approximately leading-edge aligned with the TDC/RDC data clock signal. In order to keep the Tx pin out of the high-impedance state, these enable lines should be high while the respective B channel data is being output.

RE1, RE2—RECEIVE DATA ENABLE INPUTS (PINS 19, 20)

These inputs control the input of B channel data on the Rx pin of the device. The rising edge of the respective enable signal causes the device to load the selected receive data buffer with data from the Rx pin on the next eight falling edges of the TDC/RDC clock input. The RE1 and RE2 enables should be roughly leading-edge aligned with the TDC/RDC data clock input. These enables are rising edge sensitive and need not be high for the entire B-channel input period.

TDC/RDC—TRANSMIT/RECEIVE DATA CLOCK INPUT (PIN 18)

This input is the transmit and receive data clock for the B channel data. As described in the TE1/TE2 and the RE1/RE2 sections, output data changes state on the rising edge of this signal, and input data is read on the falling edges of this signal. TDC/RDC should be roughly leading-edge aligned with the TE1, TE2, RE1, and RE2 enables, as well as the MSI frame reference signal.

MC145425 SLAVE PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY (PIN 24)

The most positive power supply pin, normally +5 volts with respect to V_{SS}.

V_{SS}—NEGATIVE SUPPLY (PIN 1)

The most negative supply pin and logic ground, normally 0 volts.

V_{ref}—REFERENCE OUTPUT (ANALOG GROUND) (PIN 2)

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external dc load should be placed on this pin.

LI—LINE INPUT (PIN 3)

This pin is an input to the demodulator for the incoming bursts. The input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

LO1, LO2—LINE DRIVER OUTPUTS (PINS 23, 22)

These push-pull outputs drive the twisted pair transmission line with a 512 kHz modified DPSK (MDPSK) burst each 125 μs; in other words at an 8 kHz frame rate. When not modulating the line, these pins are driven to the active high state—being the same potential, they create an ac short. So when used in conjunction with feed resistors, proper line termination is maintained.

CLK OUT—CLOCK OUTPUT (PIN 19)

This pin serves as a buffered output of the crystal frequency divided by two. This clock is provided for systems using the MC145428 Data Set Interface asynchronous/synchronous terminal adaptor device.

$\overline{LB}$—LOOPBACK CONTROL INPUT (PIN 4)

When this pin is low, the incoming B channels from the master are burst back to the master—instead of the Rx B channel input data. The B channel data from the master continues to be output at the slave's Tx pin during loopback. If the TONE and the loopback function are active simultaneously, the loopback function overrides the TONE function. D channel data is not affected by $\overline{LB}$.

VD—VALID DATA OUTPUT (PIN 5)

A high on this pin indicates that a valid transmission burst has been demodulated. A valid burst is determined by proper synchronization and the absence of detected bit errors. If no transmissions from the master have been received in the last 250 μs, as determined by an internal oscillator, VD will go low.

Mu/$\overline{A}$—TONE FORMAT INPUT (PIN 11)

This pin determines the PCM code for the 500 Hz square wave tone generated when the TONE input is high—Mu law (Mu/$\overline{A}$ = 1) or CCITT A law (Mu/$\overline{A}$ = 0) format.

TONE—TONE ENABLE INPUT (PIN 16)

A high on this pin causes a 500 Hz square wave PCM tone to be inserted in place of the demodulated B channel data on B channel 1. This feature allows the designer to provide audio feedback for telset keyboard operations.

$\overline{PD}$—POWER DOWN INPUT/OUTPUT (PIN 12)

This is a bidirectional pin with a weak output driver so that it can be externally overdriven. When held low, the ISDN UDLT is powered down, and the only active circuitry is that which is necessary for demodulation, generation of EN1, EN2, BCLK, and DCLK, and outputting of the data bits and VD. When held high, the ISDN UDLT is powered up and transmits normally in response to received bursts from the master. If the ISDN UDLT is powered up for 250 μs—which is derived from an internal oscillator and no bursts from the master have occurred, the ISDN slave UDLT generates a free-running set of

EN1, EN2, BCLK, and DCLK signals and sends a burst to the master device every other 125 μs frame. This is a wake-up signal to the master.

When $\overline{PD}$ is floating and a burst from the master is demodulated, the weak output drivers will try to force $\overline{PD}$ high. It will try to force $\overline{PD}$ low if 250 μs have elapsed without a burst from the master being successfully demodulated. This allows the slave device to self power up and down in demand-powered loop systems.

CCI—CRYSTAL INPUT (PIN 17)

Normally, an 8.192 MHz crystal is tied between this pin and the XTL pin. A 10 MΩ resistor between CCI and XTL and 25 pF capacitors from CCI and XTL to V_{SS} are required to ensure stability and start-up. CCI may also be driven with an external 8.192 MHz signal if a crystal is not desired.

XTL—CRYSTAL OUTPUT (PIN 18)

This pin is capable of driving one external CMOS input and 15 pF of additional load capacitance.

D1I, D2I—D CHANNEL INPUTS (PINS 6, 7)

These two pins are inputs for the 16 kbps D data channels. The D channel data bits are clocked in serially on the negative edge of the 16 kbps DCLK output pin.

D1O, D2O—D CHANNEL OUTPUTS (PINS 9, 10)

These two pins are outputs for the 16 kbps D data channels. These pins are updated on the rising edges of the slave DCLK output pin.

Tx—TRANSMIT DATA OUTPUT (PIN 13)

This line is an output for the B channel data received from the master. B channel 1 data is output on the first eight cycles of the BCLK output when EN1 is high. B channel 2 data is output on the next eight cycles of the BCLK, when EN2 is high. B channel data bits are clocked out on the rising edge of the BCLK output pin.

DCLK—D CHANNEL CLOCK OUTPUT (PIN 8)

This output is the transmit and receive data clock for both D channels. It starts upon demodulation of a burst from the master device. This signal is rising edge aligned with the EN1 and BCLK signals. After the demodulation of a burst, the DCLK line completes two cycles and then remains low until another burst from the master is demodulated. In this manner synchronization with the master is established and any clock slip between master and slave is absorbed each frame.

Rx—RECEIVE DATA INPUT (PIN 21)

This pin is an input for the B channel data. B channel 1 data is clocked in on the first eight falling edges of the BCLK output following the rising edge of the EN1 output. B channel 2 data is clocked in on the next eight falling edges of the BCLK following the rising edge of the EN2 output.

EN1—B CHANNEL 1 ENABLE OUTPUT (PIN 15)

This line is an 8 kHz enable signal for the input and output of the B channel 1 data. While EN1 is high, B channel 1 data is clocked out on the Tx pin on the first eight rising edges of the BCLK. During this same time B channel 1 input data is clocked in on the Rx pin on the first eight falling edges of the BCLK. The VD pin is also updated on the rising edge of the EN1 signal. EN1 serves as the slave device's 8 kHz frame reference signal.

EN2—B CHANNEL 2 ENABLE OUTPUT (PIN 14)

This pin is the logical inverse of the EN1 output and is used to signal the time slot for the input and output of data for the B channel 2 data.

BCLK—B CHANNEL DATA CLOCK OUTPUT (PIN 20)

This is a standard B series output which provides the data clock for the B channel data. This clock signal is 128 kHz and begins operating upon the successful demodulation of a burst from the master. At this time, EN1 goes high and BCLK starts toggling. BCLK remains active for 16 periods, at the end of which time it remains low until another burst is received from the master. In this manner synchronization between the master and slave is established and any clock slippage is absorbed each frame.

BACKGROUND

The MC145421 and the MC145425 ISDN UDLTs provide an economical means of sending and receiving two B channels (64 kbps each) of voice/data and two D channels (16 kbps each) of signal data in a two wire configuration at distances up to one kilometer. There are two ISDN UDLTs, master and slave. The master UDLT is compatible with existing and evolving PABX architectures. This device transmits 2B + 2D channels of data to the remote slave. At the remote end, the slave device presents a replica of the PBX backplane to the terminal devices.

These devices permit existing digital PBX architectures to remain unchanged and provide enhanced voice/data communication services throughout the PBX service area by simply replacing a subscriber's line card and telset.

All operations occur within the boundaries of an 8 kHz frame (125 μs). In the master, the frame sequence begins on the rising edge of MSI. In the slave, the frame begins after the demodulation of a burst from the master. The slave initializes its timing controls at this point to stay synchronized with the master.

During one 125 μs frame four main activities are performed:

1. Previously buffered 2B + 2D channel data is burst to the other end.
2. New 2B + 2D channel data is accepted for the next frame's transmission.
3. An incoming burst is demodulated and stored.
4. 2B + 2D channel data from the previous demodulated frame is output.

The bursts are 20 bits long, composed of two 8-bit B channels and two 2-bit D channels. Bursts are encoded using a modified DPSK method at 512 kHz. Since a single wire pair is used, half duplex operation is used. A 512 kHz burst is sent from end to end in a ping-pong fashion. This method provides apparent full duplex 160 kbps transmission of data at distances up to one kilometer.

GENERAL

The ISDN UDLT consists of a modulator, a demodulator, intermediate data registers, receive and transmit data registers, and sequencing and control logic. The Rx and Tx buffers interface digitally to the line card backplane signals, while the modulator and demodulator interface to the twisted pair transmission media. Intermediate data registers buffer data between these main components. The ISDN UDLT is intended to operate with a 5 volt power supply and can be driven by CMOS or TTL logic.

MASTER OPERATION

In the master, the rising edge of MSI initiates the 125 μs frame. B channel data is clocked into the Rx registers under control of TDC/RDC, RE1, and RE2. This data is combined with the D channel data clocked in on pins D1I and D2I by the DCLK. The resulting 20 bit packet is stored for the next frame transmission to the slave UDLT.

The burst output to the slave consists of the 2B + 2D data loaded during the previous frame. The burst received from the slave is demodulated and stored for outputting in the following frame.

B channel bits demodulated in the previous frame are output on the Tx pin under control of TDC/RDC, TE1, and TE2. Demodulated D channel bits are output on the D1O and D2O output pins. The indication of a valid burst demodulation is the VD output, which is updated at the start of every frame.

SLAVE OPERATION

In normal slave operation, the main synchronizing event is completion of demodulating a burst from the master UDLT. This action initializes the 125 μs frame boundary of the slave. During the slave frame, B channel data is loaded and stored under control of the BCLK, EN1, and EN2 outputs. D channel data is loaded at D1I and D2I under control of the DCLK output.

The demodulated burst from the master is separated into its D channel and B channel components and output on the D1O, D2O, and Tx pins. The return burst to the master consisting of previously loaded 2B + 2D data is transmitted eight bauds after the completion of demodulation of the master's burst. This provides a period for line transients to diminish.

The start of the slave frame initiates two cycles of the 16 kHz DCLK, and one cycle each of the 8 kHz EN1 and EN2 enables. After completing their cycles, these outputs remain low until another demodulation signals the start of a new slave frame. In this manner, clock slip between the master and slave UDLTs is absorbed each frame.

POWER-DOWN OPERATION

When $\overline{PD}$ is low in the master, the ISDN UDLT is powered down and only that circuitry necessary to demodulate incoming bursts is active. No transmissions to the slave occur during power down. If the master is receiving bursts from the slave, the VD pin will change state upon completion of the demodulation.

When the $\overline{PD}$ input pin is driven high, the master ISDN UDLT is powered up. In this mode, the master bursts to the slave every frame. B and D channel data can be loaded and unloaded and VD is updated on the MSI rising edge.

If no bursts are received by the master, whether powered up or not, the B channel data is unknown and the D channel bits will remain at their last known values.

The $\overline{PD}$ pin on the slave UDLT is bidirectional with a weak output driver that can be overdriven externally. When low—either externally or internally derived, the slave is powered down. No bursts to the master can be transmitted. EN1, EN2, BCLK, and DCLK outputs are inactive during power down except when TONE is high or a burst has been received from the master. B and D channel data can be loaded and unloaded, and VD is updated upon completion of demodulation of an incoming burst from the master. Input B and D channel data is not transmitted until the slave is powered up, in which case the first burst contains the most recently loaded data.

When the $\overline{PD}$ pin is high, the slave is powered up and transmits every frame. The data enables and clocks are output and data can be loaded and unloaded.

TIMEOUT OPERATION

Timeout is an operating state in both the UDLT master and slave devices. This state indicates that no incoming bursts have been demodulated, forcing the VD pin low. An internal counter is incremented for each frame that does not contain an incoming burst. The counter is reset upon demodulating a burst from the far end. Timeout can occur whether the device is powered up or down.

In the master, timeout begins on the rising edge of the third MSI following the last received burst. This is equivalent to two MSI frames. The VD output is forced low during timeout. The B channel output data will be unknown, but the D channel bits will remain at their last values. Successful demodulation of a burst from the slave will result in leaving the timeout state on the next rising MSI edge.

Timeout in the slave begins during the third frame without an incoming burst. The VD pin is forced low and the last D channel bits are saved. Normally, the slave timing is synchronized to the incoming master bursts, but in timeout, the slave operates from a free-running internal frame clock accompanied by BCLK, EN1, and EN2. These clocks are not generated during the two frames prior to entering timeout. If powered up during timeout, the slave will burst to the master on every other frame. This mode allows the terminal equipment to transmit its status to the master even though it is not receiving data. Demodulation of a burst from the master will cause the slave to exit the timeout mode.

When the $\overline{PD}$ pin is used as an output on the slave UDLT, timeout controls the pin. Timeout forces the $\overline{PD}$ output low to indicate that the device has powered itself down. In this case, the slave will not transmit to the master. However, when a valid burst is received, timeout ends and the $\overline{PD}$ pin is driven high to indicate power up. This feature allows the slave UDLT to self-power-up and down in demand-powered loop systems.

NOTE

The slave uses a free running clock during timeout. After a long period without a burst from the master, the timing between master and slave could be such that more than one burst will be needed to resync the two devices.

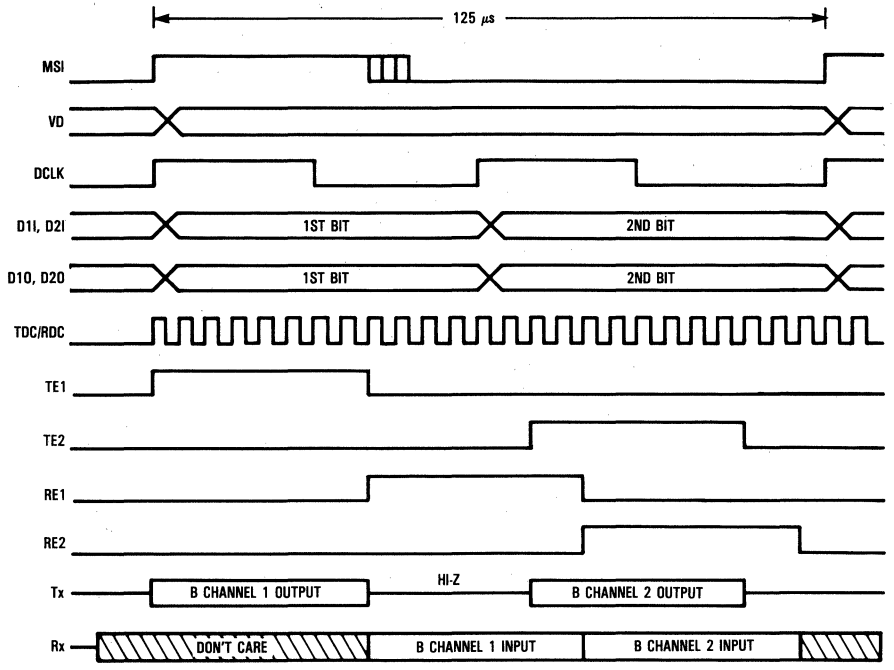


Figure 1. Typical MC145421 Master ISDN UDLT Timing

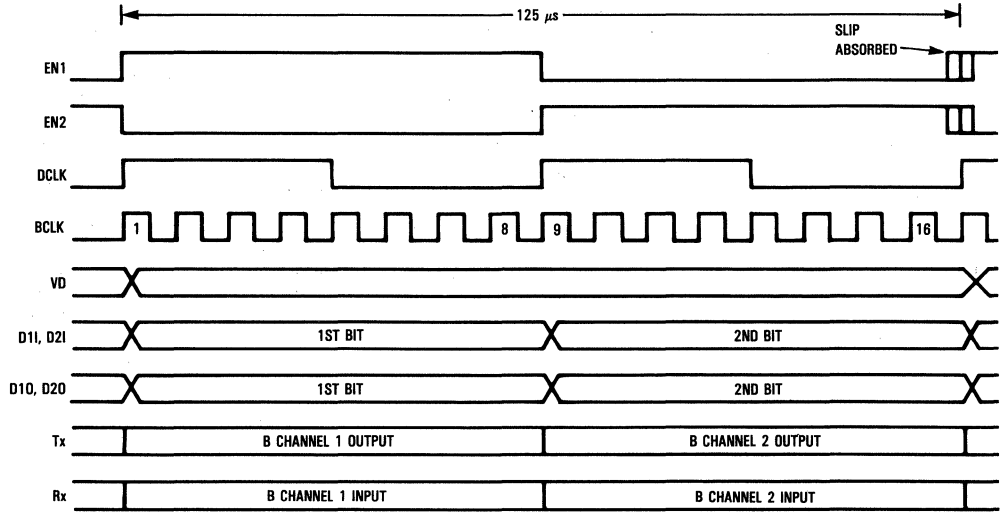
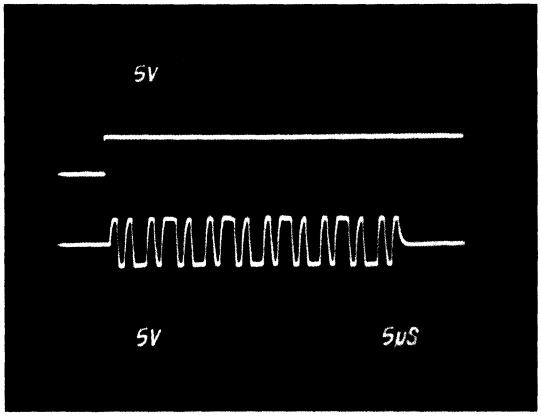
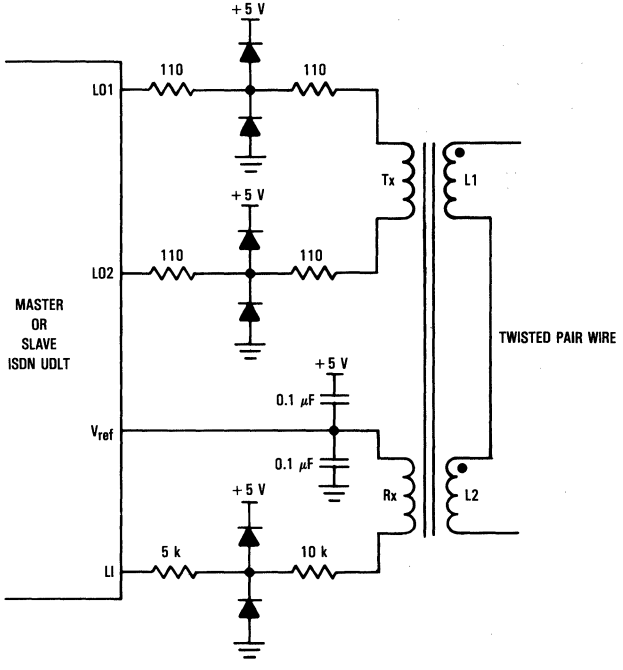


Figure 2. MC145425 Slave ISDN UDLT Timing



Top Trace: MSI
Bottom Trace: Outgoing burst measured at LI (with respect to V_{ref})

Figure 3. Master Burst



TRANSFORMER PARAMETERS

INDUCTANCE OF Tx WINDING: 1.75 mH
TURNS RATIO: Tx: L1 + L2 2:1
TURNS RATIO: Rx: L1 + L2 4:1

DIODES: 1N4148 OR EQUIVALENT

Figure 4. Interface to Twisted Pair Wire

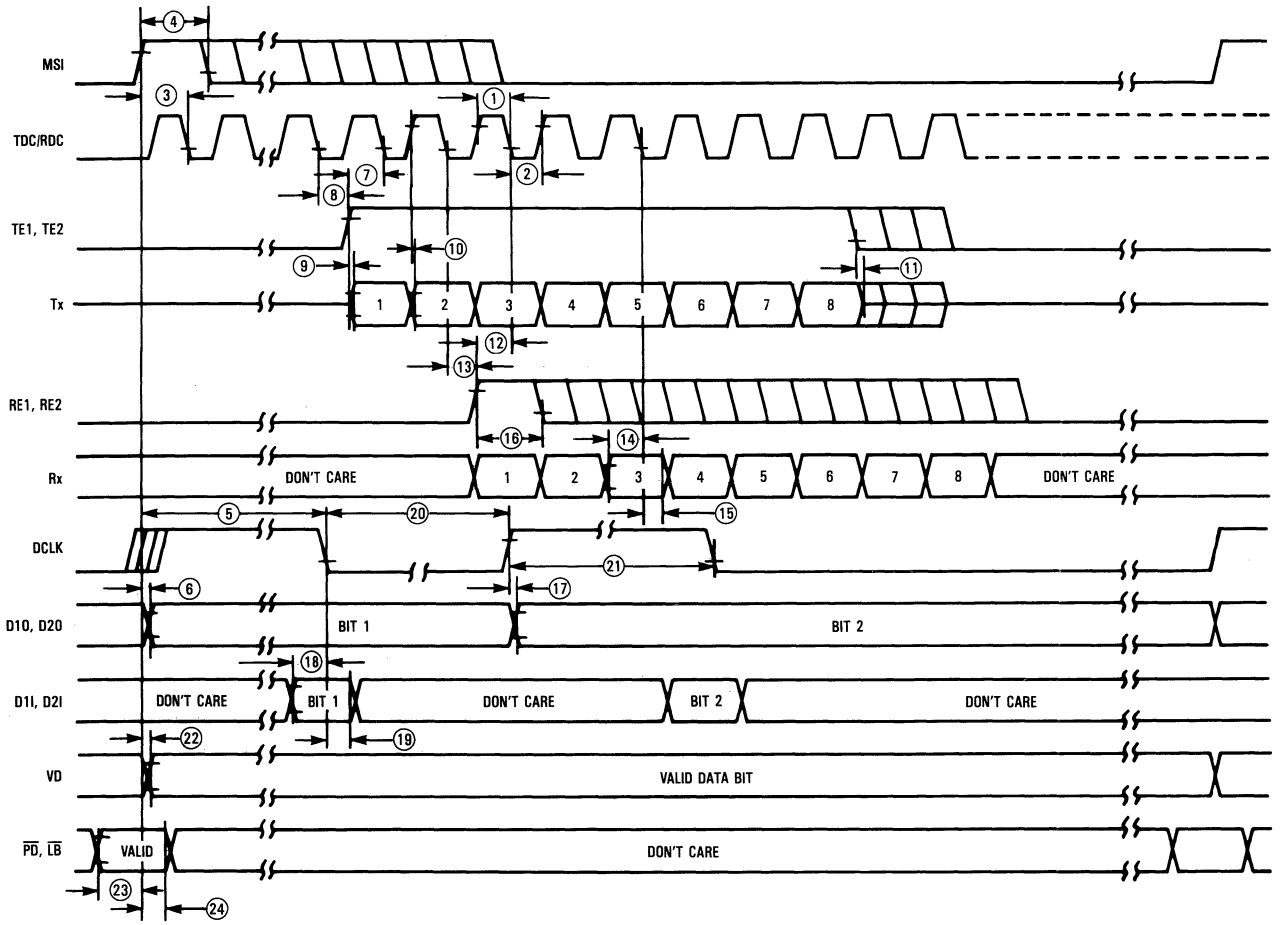
2

SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

No.*	Parameter	Min	Max	Unit
Master Timing				
1	TDC/RDC Pulse Width High	110		ns
2	TDC/RDC Pulse Width Low	110		ns
3	MSI Rising Edge to TDC/RDC Falling Edge	90		ns
4	MSI Pulse Width	200		ns
5	MSI Rising Edge to First DCLK Falling Edge	90		ns
6	MSI Rising Edge to First D1O, D2O Bit Valid		–	ns
7	TE1, TE2 Rising Edge to TDC/RDC Falling Edge	110		ns
8	TDC/RDC Falling Edge to TE1, TE2 Rising Edge	20		ns
9	TE1, TE2 Rising Edge to First Tx Data Bit Valid		50	ns
10	TDC/RDC Rising Edge to Tx Data Bits 2 Through 8 Valid		50	ns
11	TE1, TE2 Falling Edge to Tx High-Impedance		70	ns
12	RE1, RE2 Rising Edge to TDC/RDC Falling Edge	110		ns
13	TDC/RDC Falling Edge to RE1, RE2 Rising Edge	20		ns
14	Rx Data Setup (Data Valid Before TDC/RDC Falling Edge)	50		ns
15	Rx Data Hold (Data Valid After TDC/RDC Falling Edge)	20		ns
16	RE1, RE2 Pulse Width	220		ns
17	DCLK Rising Edge to D1O, D2O Bit Valid		–	ns
18	D1I,D2I Data Setup (Data Valid Before DCLK Falling Edge)	50		ns
19	D1I, D2I Data Hold (Data Valid After DCLK Falling Edge)	20		ns
20	DCLK Pulse Width Low	110		ns
21	DCLK Pulse Width High	110		ns
22	MSI Rising Edge to VD Valid		–	ns
23	$\overline{PD}$, $\overline{LB}$ Setup ($\overline{PD}$, $\overline{LB}$ Valid Before MSI Rising Edge)	50		ns
24	$\overline{PD}$, $\overline{LB}$ Hold ($\overline{PD}$, $\overline{LB}$ Valid After MSI Rising Edge)	20		ns
Slave Timing				
25	BCLK Pulse Width High (CCI = 8.192 MHz)	3.66	4.15	μs
26	BCLK Pulse Width Low (CCI = 8.192 MHz)	3.66	4.15	μs
27	EN1 or EN2 Rising Edge to BCLK Rising Edge		±50	ns
28	EN1 or EN2 Rising Edge to DCLK Rising Edge		±50	ns
29	EN1 or EN2 Rising Edge to First Tx Data Bit Valid		50	ns
30	BCLK Rising Edge to Tx Data Bits 2 Through 8 Valid		50	ns
31	DCLK Pulse Width High (CCI = 8.192 MHz)	31.0	31.5	μs
32	DCLK Pulse Width Low (CCI = 8.192 MHz)	31.0	31.5	μs
33	DCLK Rising Edge to D1O, D2O Bits Valid		50	ns
34	Rx Setup (Rx Data Valid Before BCLK Falling Edge)	50		ns
35	Rx Hold (Rx Data Valid After BCLK Falling Edge)	20		ns
36	D1I, D2I Setup (D1I, D2I Valid Before DCLK Falling Edge)	50		ns
37	D1I, D2I Hold (D1I, D2I Valid After DCLK Falling Edge)	20		ns
38	EN1 Rising Edge to VD Valid		50	ns
SE Pin Timing				
39	$\overline{LB}$, $\overline{PD}$ Hold ($\overline{LB}$, $\overline{PD}$ Valid After SE Falling Edge)	20		ns
40	D1O, D2O, VD High-Impedance After SE Falling Edge		70	ns
41	D1O, D2O, VD Valid After SE Rising Edge)	60		ns
42	$\overline{LB}$, $\overline{PD}$ Setup ($\overline{LB}$, $\overline{PD}$ Valid Before SE Rising Edge)	50		ns

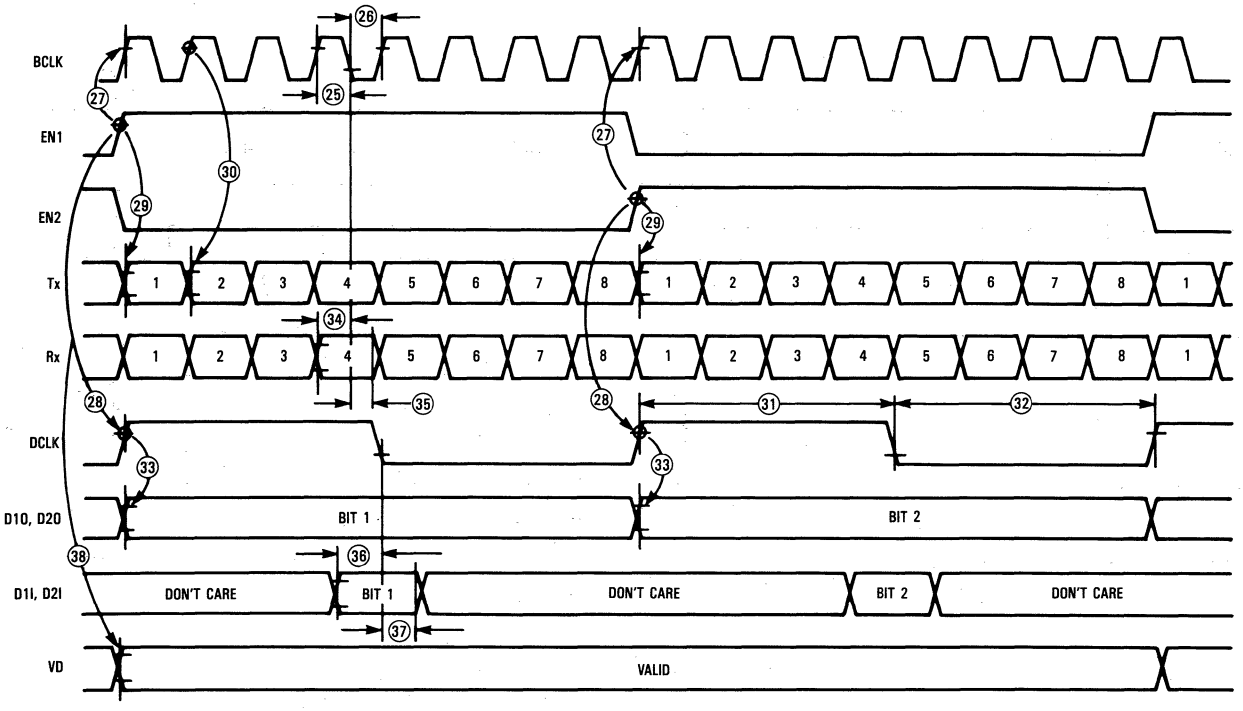
*See Switching Characteristics waveforms

MASTER SWITCHING CHARACTERISTICS

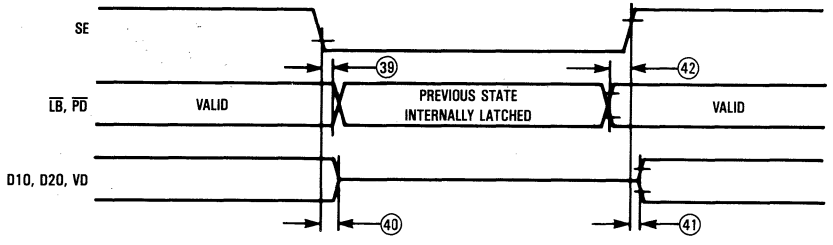


NOTE: All measurement thresholds are 30% or 70% of V_{DD}.

SLAVE SWITCHING CHARACTERISTICS



MASTER SE PIN TIMING



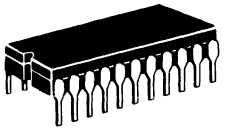
NOTE: All measurement thresholds are 30% or 70% of V_{DD}.

MC145422
MC145426

2

Advance Information

Universal Digital-Loop Transceivers (UDLT)



L SUFFIX
CERAMIC
CASE 736

The MC145422 and MC145426 UDLTs are high-speed data transceivers that provide 80 kilobits per second full duplex data communication over 26 AWG and larger twisted pair cable up to two kilometers in distance. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used in remote data acquisition and control systems. These devices utilize a 256 kilobaud modified differential phase shift keying burst modulation technique for transmission to minimize RFI/EMI and crosstalk. Simultaneous power distribution and duplex data communication can be obtained using a single twisted pair wire.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The UDLT chip-set consists of the MC145422 master UDLT for use at the telephone switch linecard and the MC145426 slave UDLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 Kilobits-Per-Second Voice/Data Channel and Two Eight Kilobits-Per-Second Signaling Data Channels Over One 26 AWG Wire Pair Up to Two Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single Five Volt Power Supply
- 22 Pin Package

MC145422 Master UDLT

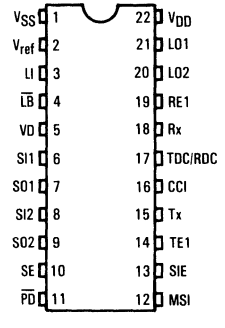
- Pin Controlled Power-Down and Loop-Back Features
- Signaling and Control I/O Capable of Sharing Common Bus Wiring with Other UDLTs
- Variable Data Clock—64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of Eight Kilobits/Second Channel into LSB of 64 Kilobits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

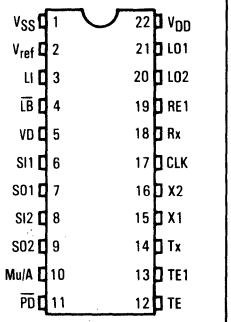
- Compatible with MC14400 Series PCM Mono-Circuits
- Pin Controlled Loop-Back Feature
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

PIN ASSIGNMENTS

MC145422



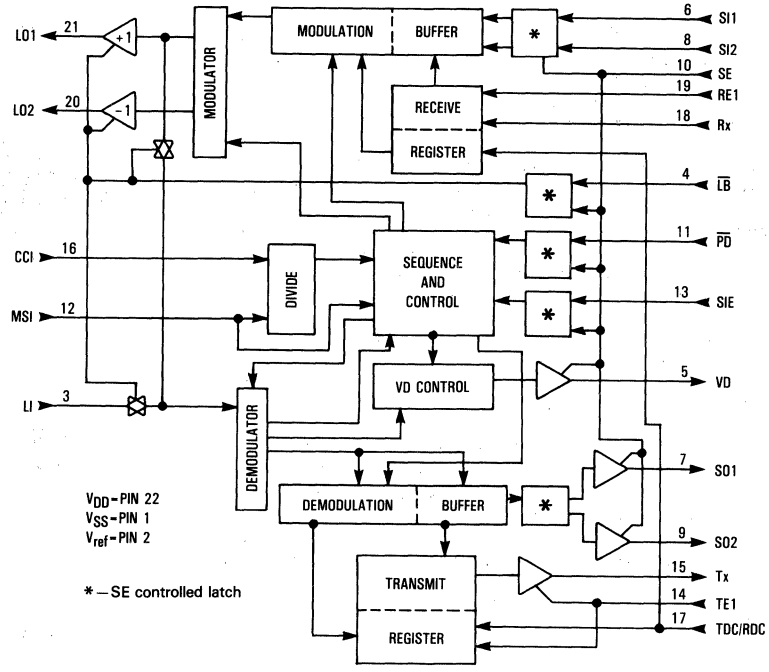
MC145426



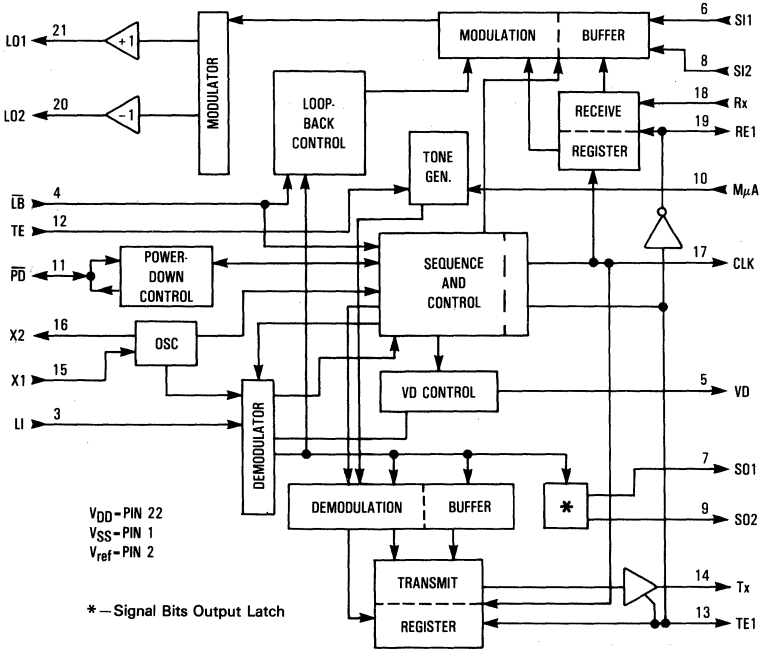
This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MC145422 MASTER UDLT BLOCK DIAGRAM



MC145426 SLAVE UDLT BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 9.0	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Parameter	Pins	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5.5	V
Power Dissipation (PD=V_{DD}, V_{DD}=5 V)	V_{DD}	—	80	mW
Power Dissipation (PD=V_{SS}, TE=V_{SS})	V_{DD}	—	75	mW
Frame Rate MC145422	MSI	7.9	8.1	kHz
MC145422-MC145426 Frame Rate Slip (See Note 1)	—	—	0.25	%
CCI Clock Frequency (MSI=8 kHz)	CCI	—	2.048	MHz
Data Clock Rate MC145422	TDC, RDC	64	2560	kHz
Modulation Baud Rate (See Note 2)	LO1, LO2	—	256	kHz

NOTES: 1. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ±0.25% for optimum operation.
2. Assumes crystal frequency of 4.096 MHz for the MC145426 and 2.048 MHz CCI for the MC145422.

DIGITAL CHARACTERISTICS (V_{DD}=5 V, T_A=0 to 70°C)

Parameter		Min	Max	Unit
Input High Level		3.5	—	V
Input Low Level		—	1.5	V
Input Current	Except LI LI	−1.0 −100	1.0 100	μA
Input Capacitance		—	7.5	pF
Output High Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OH}=2.5 V V_{OH}=4.6 V	−1.7 −0.36	— —	mA
Output Low Current (Except Tx on MC145422 and Tx and $\overline{PD}$ on MC145426)	V_{OL}=0.4 V V_{OL}=0.8 V	0.36 0.8	— —	mA
$\overline{PD}$ Output High Current (MC145426) (See Note 7)	V_{OH}=2.5 V V_{OH}=4.6 V	−90 −10	— —	μA
$\overline{PD}$ Output Low Current (MC145426) (See Note 7)	V_{OL}=0.4 V V_{OL}=0.8 V	60 100	— —	μA
Tx Output High Current	V_{OH}=2.5 V V_{OH}=4.6 V	−3.4 −0.7	— —	mA
Tx Output Low Current	V_{OL}=0.4 V V_{OL}=0.8 V	1.7 3.5	— —	mA
Tx Input Impedance (TE1=V_{SS}, MC145422)		100	—	kΩ
Crystal Frequency (MC145426, Note 3)		4.0	4.4	MHz
PCM Tone (TE=V_{DD}, MC145426)		−22	−18	dBm0
Three-State Current (SO1, SO2, VD, Tx on MC145422, Tx on MC145426)		—	±1	μA
V_{ref} Voltage (See Note 6)		2	3	V
X2—Oscillator Output High Drive Current (MC145426) (See Note 5)	V_{OH}=4.6 V	−450	—	μA
X2—Oscillator Output Low Drive Current (MC145426) (See Note 5)	V_{OL}=0.4 V	450	—	μA

2

ANALOG CHARACTERISTICS (V_{DD} = 5 V, T_A = 0 to 70°C)

Parameter		Min	Max	Unit
Modulation Differential Amplitude (R_L = 440 Ω)	LO1 to LO2	4.5	6.0	V_{p-p}
Modulation Differential DC Offset		0	300	mV
Demodulator Input Amplitude (See Note 4)		0.050	2.5	V peak
Demodulator Input Impedance		50	150	kΩ

NOTES:
3. The MC145426 crystal frequency divided by 512 must equal the MC145422 MSI frequency ±0.25% for optimum performance.
4. The input level into the demodulator to reliably demodulate incoming bursts. Input referenced to V_{ref}.
5. Output drive when X1 is being driven from an external clock.
6. V_{ref} typically (9/20 V_{DD}-V_{SS})
7. To overdrive $\overline{PD}$ from a low level to 3.5 V or a high level to 1.5 V requires a minimum of ±800 μA drive capability.

MC145422 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	–	4	μs
Input Fall Time	All Digital Inputs	1	t_f	–	4	μs
Pulse Width	TDC/RDC, RE1, MSI	1	$t_{w(H,L)}$	90	–	ns
CCI Duty Cycle		1	$t_{w(H,L)}$	45	55	%
Data Clock Frequency	TDC/RDC	–	t_{DC}	64	2560	kHz
Propagation Delay Time						ns
MSI to SO1, SO2, VD ($\overline{PD}$ = V_{DD})		2	t_{PLH}, t_{PHL}	–	90	
TDC to Tx		3		–	90	
MSI to TDC/RDC Setup Time			t_{su3}	90	–	ns
		4	t_{su4}	40	–	
TE1/RE1 to TDC/RDC Setup Time			t_{su3}	90	–	ns
		4	t_{su4}	40	–	
Rx to TDC/RDC Setup Time		5	t_{su5}	60	–	ns
Rx to TDC/RDC Hold Time		5	t_{h1}	60	–	ns
SI1, SI2 to MSI Setup Time		6	t_{su6}	60	–	ns
SI1, SI2 to MSI Hold Time		6	t_{h2}	60	–	ns

MC145426 SWITCHING CHARACTERISTICS (V_{DD} = 5 V, T_A = 25°C, C_L = 50 pF)

Parameter		Fig	Symbol	Min	Max	Unit
Input Rise Time	All Digital Inputs	1	t_r	–	4	μs
Input Fall Time	All Digital Inputs	1	t_f	–	4	μs
Clock Output Pulse Width	CLK	1	$t_{w(H,L)}$	3.8	4.0	μs
Crystal Frequency		–	f_{X1}	4.086	4.1	MHz
Propagation Delay Times						ns
TE1 Rising to CLK (TE = V_{DD})		7	t_{P1}	50	50	
TE1 Rising to CLK (TE = V_{SS})		7	t_{P1}	438	538	
CLK to TE1 Falling		7	t_{P2}	–	40	
CLK to RE1 Rising		8	t_{P3}	–	40	
RE1 Falling to CLK (TE = V_{DD})		8	t_{P4}	−50	50	
RE1 Falling to CLK (TE = V_{SS})		8	t_{P4}	438	538	
CLK to Tx		9	t_{P5}	–	90	
TE1 to SO1, SO2		9	t_{P6}	–	90	
Rx to CLK Setup Time		5	t_{su5}	60	–	ns
Rx to CLK Hold Time		5	t_{h1}	60	–	ns
SI1, SI2 to TE1 Setup Time		6	t_{su6}	60	–	ns
SI1, SI2 to TE1 Hold Time		6	t_{h2}	60	–	ns

SWITCHING WAVEFORMS

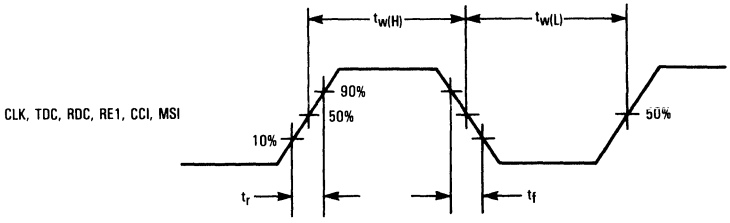


Figure 1

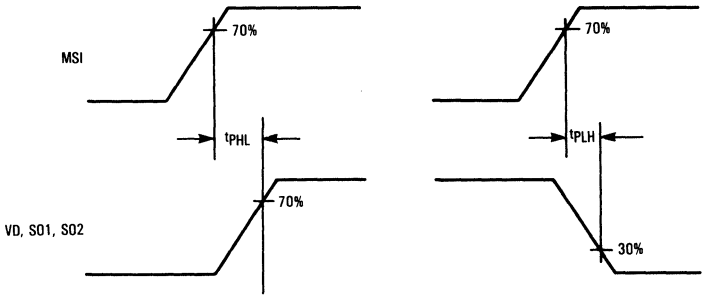


Figure 2

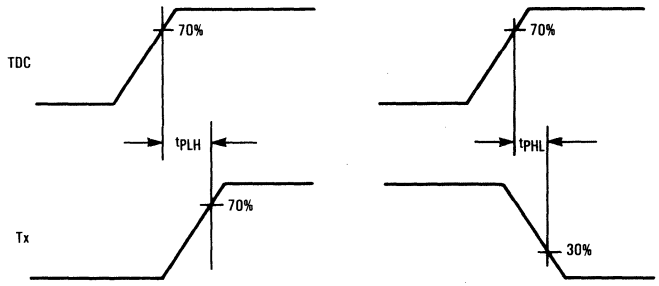


Figure 3

2

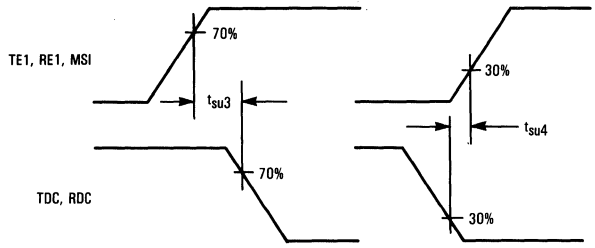


Figure 4

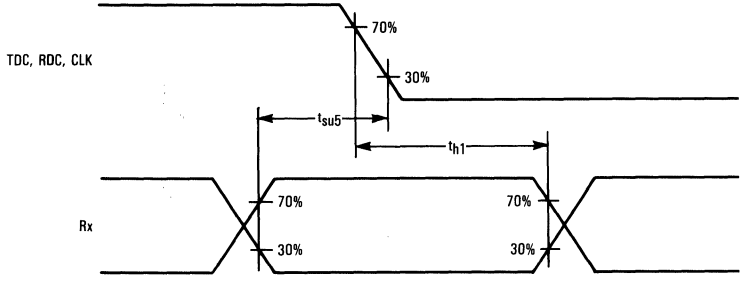


Figure 5

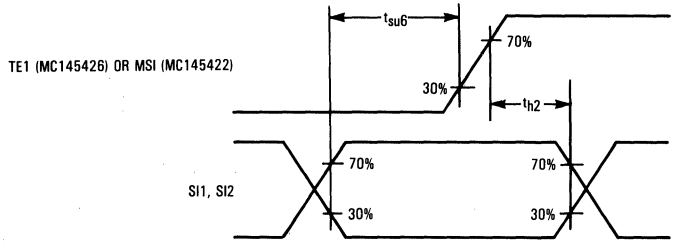


Figure 6

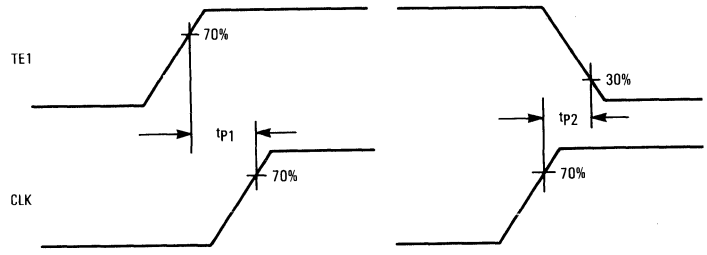


Figure 7

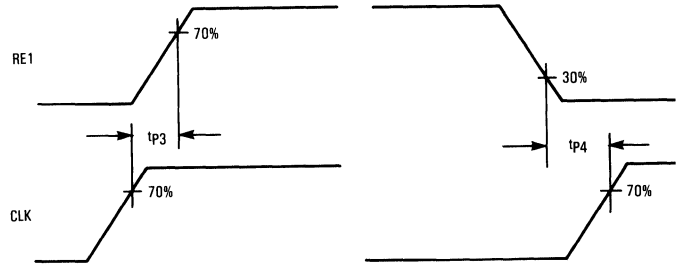


Figure 8

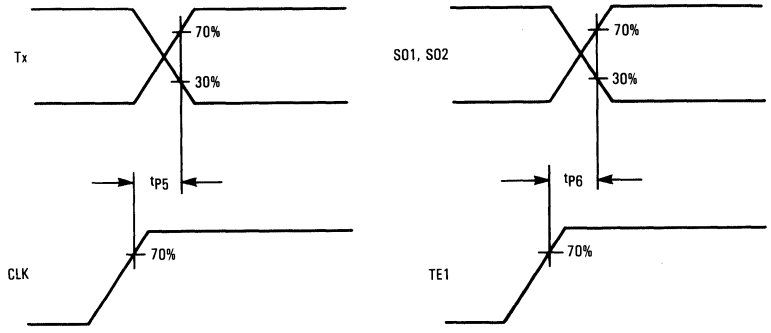


Figure 9

2

MC145422 MASTER UDLT PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

Normally 5 volts.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

V_{ref}—REFERENCE OUTPUT

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI—LINE INPUT

This input to the demodulator circuit has an internal 100 k resistor tied to the internal reference node so that an external capacitor and/or line transformer may be used to couple the input signal to the part with no dc offset.

$\overline{LB}$—LOOP-BACK CONTROL

A low on this pin disconnects the LI pin from internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator output to the demodulator input which loops the part on itself for testing in the system. The state of this pin is internally latched if the SE pin is brought and held low. Loop-Back is active only when $\overline{PD}$ is high.

VD—VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of MSI when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a line transmission. VD is a standard B-series CMOS output and is high impedance when SE is held low.

SI1, SI2—SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is internally latched if SE is held low.

SO1, SO2—SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the slave UDLT and change state on the rising edge of MSI if $\overline{PD}$ is high, or at the completion of demodulation if $\overline{PD}$ is low. These outputs have standard B-series CMOS drive capability and are high impedance if the SE pin is held low.

SE—SIGNAL ENABLE INPUT

If held high, the $\overline{PD}$, $\overline{LB}$, SI1, SI2, and SIE inputs and the SO1, SO2, and VD outputs function normally. If held low, the state of these inputs are latched and held internally while the outputs are high impedance. This allows these pins to be bussed with those of other UDLTs to a common controller.

$\overline{PD}$—POWER-DOWN INPUT

If held low, the UDLT ceases modulation. In power-down, the only active circuitry is that which is necessary to demodulate an incoming burst and output the signal and valid data bits. Internal data transfers to the transmit and receive registers cease. When brought high, the UDLT powers-up, and waits three positive MSI edges or until the end of an incoming transmission from the slave UDLT and begins transmitting every MSI period to the slave UDLT on the next rising edge of the MSI.

MSI—MASTER SYNC INPUT

This pin is the system sync and initiates the modulation on the twisted pair. MSI should be approximately leading-edge aligned with TDC/RDC.

SIE—SIGNAL INSERT ENABLE

This pin, when held high, inserts signal bit 2 received from the slave into the LSB of the outgoing PCM word at Tx and will ignore the SI2 pin and use in place the LSB of the incoming PCM word at Rx for transmission to the slave. The PCM word to the slave will have LSB forced low in this mode. In this manner, signal bit 2 to/from the slave UDLT is inserted into the PCM words the master sends and receives from the backplane for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

TE1—TRANSMIT DATA ENABLE 1 INPUT

This pin controls the outputting of data on the Tx pin. While TE1 is high, the Tx data is presented on the eight rising edges of TDC/RDC. TE1 is also a high-impedance control of the Tx pin. If MSI occurs during this period, new data will be transferred to the Tx output register in the ninth high period of TDC/RDC after TE1 rises; otherwise, it will transfer on the rising edge of MSI. TE1 and TDC/RDC should be approximately leading-edge aligned.

Tx—TRANSMIT DATA OUTPUT

This three-state output pin presents new voice data during the high periods of TDC/RDC when TE1 is high (see TE1).

CCI—CONVERT CLOCK INPUT

A 2.048 MHz clock signal should be applied to this pin. The signal is used for internal sequencing and control. This signal should be coherent with MSI for optimum performance but may be asynchronous if slightly worse error rate performance can be tolerated.

TDC/RDC—TRANSMIT/RECEIVE DATA CLOCK

This pin is the transmit and receive data clock and can be 64 kHz to 2.56 MHz. Data is output at the Tx pin while TE1 is high on the eight rising edges of TDC/RDC after the rising edge of TE1. Data on the Rx pin is loaded into the receive register of the UDLT on the eight falling edges of TDC/RDC after a positive transition on RE1. This clock should be approximately leading-edge aligned with MSI.

Rx—RECEIVE DATA

Voice data is clocked into the UDLT from this pin on the falling edges of TDC/RDC under the control of RE1.

RE1—RECEIVE DATA ENABLE 1 INPUT

A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next eight falling edges of the data clock, TDC/RDC. RE1 and TDC/RDC should be approximately leading-edge aligned.

LO1, LO2—LINE DRIVER OUTPUTS

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push-pull. These pins are driven to V_{ref} when not modulating the line.

MC145426 SLAVE UDLT PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

Normally 5 volts.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative supply pin, normally 0 volts.

V_{ref}—REFERENCE OUTPUT

This pin is the output of the internal reference supply and should be bypassed to V_{DD} and V_{SS} by 0.1 μF capacitors. No external dc load should be placed on this pin.

LI—LINE INPUT

This input to the demodulator circuit has an internal 100 kilohm resistor tied to the internal reference node (V_{ref}) so that an external capacitor and/or line transformer may be used to couple the signal to this part with no dc offset.

$\overline{LB}$—LOOP-BACK CONTROL

When this pin is held low and $\overline{PD}$ is high (the UDLT is receiving transmissions from the master), the UDLT will use the eight bits of demodulated PCM data in place of the eight bits of Rx data in the return burst to the master, thereby looping the part back on itself for system testing. SI1 and SI2 operate normally in this mode. CLK will be held low during loop-back operation.

VD—VALID DATA OUTPUT

A high on this pin indicates that a valid line transmission has been demodulated. A valid transmission is determined by proper sync and the absence of detected bit errors. VD changes state on the leading edge of TE1. If no transmissions from the master have been received in the last 250 μs (derived from the internal oscillator), VD will go low without TE1 rising since TE1 is not generated in the absence of received transmissions from the master (see TE pin description for the one exception to this).

SI1, SI2—SIGNALING BIT INPUTS

Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

SO1, SO2—SIGNALING BIT OUTPUTS

These outputs are received signaling bits from the master UDLT and change state on the rising edge of TE1. These outputs have standard B-series CMOS output drive capability.

$\overline{PD}$—POWER-DOWN INPUT/OUTPUT

This is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT is powered down and the only active circuitry is: that which is necessary for demodulation, TE1/RE1/CLK generation upon demodulation the outputting of data received from the master and updating of VD status. When held high, the UDLT is powered-up and transmits in response to received transmissions from the master. If no received bursts from the master have occurred when powered-up, for 250 μs (derived from the internal oscillator frequency), the UDLT will generate a free running 125 μs internal clock from the internal oscillator and will burst a transmission to the master every other internal 125 μs clock using data on the SI1 and SI2 pins and the last data word loaded into the receive register. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power-up and down in demand powered loop systems.

TE—TONE ENABLE

A high on this pin generates a 500 Hz square wave PCM tone and inserts it in place of the demodulated voice PCM word from the master for outputting to the Tx pin to the telset mono-circuit. A high on TE will generate TE1 and CLK from the internal oscillator when the slave is not receiving bursts from the master so that the PCM square wave can be loaded into the mono-circuit. This feature allows the user to provide audio feedback for the telset keyboard depressions except during Loop-Back. During Loop-Back of the slave UDLT, CLK is defeated so a tone cannot be generated in this mode.

TE1—TRANSMIT DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which goes high after the completion of demodulation of an incoming transmission from the master. It remains high for eight CLK periods and then low until the next burst from the master is demodulated. While high, the voice data just demodulated is output on the first eight rising edges of CLK at the Tx pin. The signaling data just demodulated is output on SO1 and SO2 on TE1's rising edge, as is VD.

Tx—TRANSMIT DATA OUTPUT

This is a standard B-series CMOS output. Voice data is output on this pin on the rising edges of CLK while TE1 is high and is high impedance when TE1 is low.

X1—CRYSTAL INPUT

A 4.096 MHz crystal is tied between this pin and X2. A 10 megohm resistor across X1 and X2 and 25 pF capacitors from X1 and X2 to V_{SS} are required for stability and to insure start-up. X1 may be driven by an external CMOS clock signal if X2 is left open.

X2-CRYSTAL OUPUT

This pin is capable of driving one external CMOS input and 15 pF of additional capacitance. (SEE X1)

CLK—CLOCK OUTPUT

This is a standard B-series CMOS output which provides the data clock for the telset mono-circuit. It is generated by dividing the oscillator down to 128 kHz and starts upon the completion of demodulation of an incoming burst from the master. At this time, CLK begins and TE1 goes high. CLK will remain active for 16 periods, at the end of which it will remain low until another transmission from the master is demodulated. In this manner, sync from the master is established in the slave and any clock slip between the master and the slave is absorbed each frame. CLK is generated in response to an incoming burst from the master; however, if TE is brought high, then CLK and TE1/RE1 are generated from the internal oscillator until TE is brought low or an incoming burst from the master is received. CLK is disabled when $\overline{LB}$ is held low.

Rx—RECEIVE DATA INPUT

Voice data from the telset mono-circuit is input on this pin on the first eight falling edges of CLK after RE1 goes high.

Mu/A—TONE DIGITAL FORMAT INPUT

This pin determines if the PCM code of the 500 Hz square wave tone, generated when TE is high, is D3 (Mu/A = 1) or CCITT (Mu/A = 0) format.

RE1-RECEIVE DATA ENABLE 1 OUTPUT

This is a standard B-series CMOS output which is the inverse of TE1 (see TE1).

LO1, LO2—LINE DRIVER OUTPUTS

These outputs drive the twisted pair line with 256 kHz modified DPSK bursts each frame and are push-pull. These pins are driven to V_{ref} when the device is not modulating.

BACKGROUND

The MC145422 master and MC145426 slave UDLT transceiver ICs main application is to bidirectionally transmit the digital signals present at a codec/filter-digital PABX backplane interface over normal telephone wire pairs. This allows the remoting of the mono-circuit in a digital telephone set and enables each set to have a high speed data access to the PABX switching facility. In effect, the UDLT allows each PABX subscriber direct access to the inherent sixty-four kilobits per second data routing capabilities of the PABX.

The UDLT provides a means for transmitting and receiving sixty-four kilobits of voice data and sixteen kilobits-per-second of signaling data in two wire format over normal telephone pairs. The UDLT is a two chip set consisting of a master and a slave. The master UDLT replaces the codec/filter and SLIC on the PABX line card, and transmits and receives data over the wire pair to the telset. The UDLT appears to the linecard and backplane as if it were a PCM codec/filter and has almost the same digital interface features as the MC14400 series mono-circuits. The slave UDLT is located in the telset and interfaces the mono-circuit to the wire pair. By hooking two UDLTs back-to-back, a repeater can also be formed. The master and slave UDLTs operate in a frame synchronous manner, sync being established at the slave by the timing of the master's transmission. The master's sync is derived from the PABX frame sync.

The UDLT operates using one twisted pair. Eight bits of voice data and two bits of signaling data are transmitted and received each frame in a half duplex manner; i.e., the slave waits until the transmission from the master is completely received before transmitting back to the master. Transmission occurs at 256 kilohertz bit rate using a modified form of DPSK. This "ping-pong" mode will allow transmission of data at distances up to two kilometers before turnaround delay becomes a problem. The UDLT is so defined as to allow this data to be handled by the linecard, backplane, and PABX as if it were just another voice conversation. This allows existing PABX hardware and software to be unchanged and yet provides switched sixty-four kilobits per second voice or data communications throughout its service area by simply replacing a subscriber's linecard and telset. A feature in the master allows one of the two signaling bits to be inserted and extracted from the backplane PCM word to allow simultaneous voice and data transmission through the PABX. Both UDLTs have a loop-back feature by which the device can be tested in the user system.

The slave UDLT has the additional feature of providing a 500 hertz Mu or A-law coded square wave to the mono-circuit when the TE pin is brought high. This can be used to provide audio feedback in the telset during keyboard depressions.

CIRCUIT DESCRIPTION

GENERAL

The UDLT consists of a modulator, demodulator, two intermediate data buffers, sequencing and control logic, and transmit and receive data registers. The data registers interface to the linecard or mono-circuit digital interface signals, the modulator and demodulator interface the twisted pair transmission medium, while the intermediate data registers buffer data between these two sections. The UDLT is intended to operate on a single five volt supply and can be driven by TTL or CMOS logic.

MASTER OPERATION

In the master, data from the linecard is loaded into the receive register each frame from the Rx pin under the control of the TDC/RDC clock and the receive data enable, RE1. RE1 controls loading of eight serial bits, henceforth referred to as the voice data word. Each MSI, these words are transferred out of the receive register to the modulation buffer for subsequent modulation onto the line. The modulation buffer takes the received voice data word and the two signaling data input bits on SI1 and SI2 loaded on the MSI transition and formats the ten bits into a specific order. This data field is then transmitted in a 256 kilohertz modified DPSK burst onto the line to the remote slave UDLT.

Upon demodulating the return burst from the slave, the decoded data is transferred to the demodulation buffer and the signaling bits are stripped ready to be output on SO1 and SO2 at the next MSI. The voice data word is loaded into the transmit register as described in the TE1 pin description for outputting via the Tx pin at the TDC/RDC data clock rate under the control of TE1. VD is output on the rising edge of MSI. Timing diagrams for the master are shown in Figure 10.

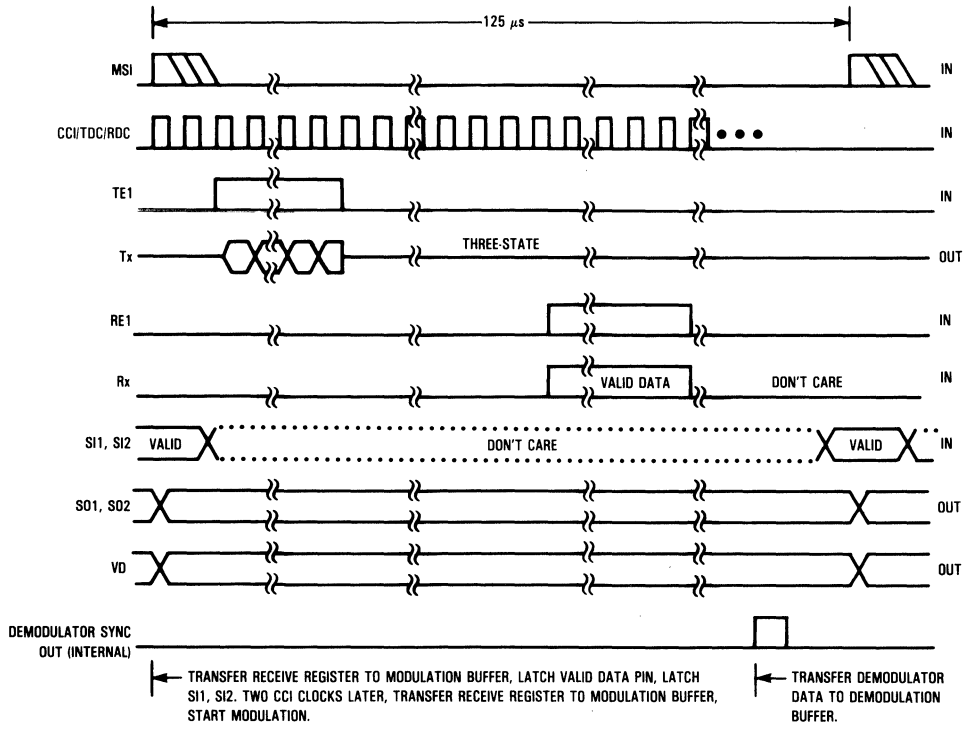


Figure 10. Master UDLT Timing

SLAVE OPERATION

In the slave, the synchronizing event is the detection of an incoming line transmission from the master as indicated by the completion of demodulation. When an incoming burst from the master is demodulated, several events occur. As in the master, data is transferred from the demodulator to the demodulation buffer and the signaling bits are stripped for outputting at SO1 and SO2. Data in the receive register is transferred to the modulation buffer. TE1 goes high loading in data at SI1 and SI2, which will be used in the transmission burst to the master along with the data in the transmit data buffer, and outputting SO1, SO2, and VD. Modulation of the burst begins four 256 kilohertz periods after the completion of demodulation.

While TE1 is high, voice data is output on Tx to the telset mono-circuit on the rising edges of the data clock output on the CLK pin. On the ninth rising edge of CLK, TE1 goes low, RE1 goes high, and voice data from the mono-circuit is input to the receive register from the Rx pin on the next eight falling edges of CLK. RE1 is TE1 inverted and is provided to facilitate interface to the mono-circuit.

The CLK pin 128 kilohertz output is formed by dividing down the 4.096 megahertz crystal frequency by thirty-two. Slippage between the frame rate of the master (as represented by the completion of demodulation of an incoming transmission from the master) and the crystal frequency is absorbed by holding the sixteenth low period of CLK until the next completion of demodulation. This is shown in the slave UDLT timing diagram of Figure 11.

POWER-DOWN OPERATION

In the master, when $\overline{PD}$ is low, the UDLT stops modulating and only that circuitry necessary to demodulate the incoming bursts and output the signaling and VD data bits is active. In this mode, if the UDLT receives a burst from the slave, the SO1, SO2, and VD pins will change state upon completion of the demodulation instead of the rising edge of MSI. The state of these pins will not change until either three rising MSI edges have occurred without the reception of a burst from the slave or until another burst is demodulated, whichever occurs first.

When $\overline{PD}$ is brought high, the master UDLT will wait either three rising MSI edges or until the MSI rising edge following the demodulation of an incoming burst before transmitting to the slave. The data for the first transmission to the slave after power—up is loaded into the UDLT during the RE1 period prior to the burst in the case of voice, and on the present rising edge of MSI for signaling data.

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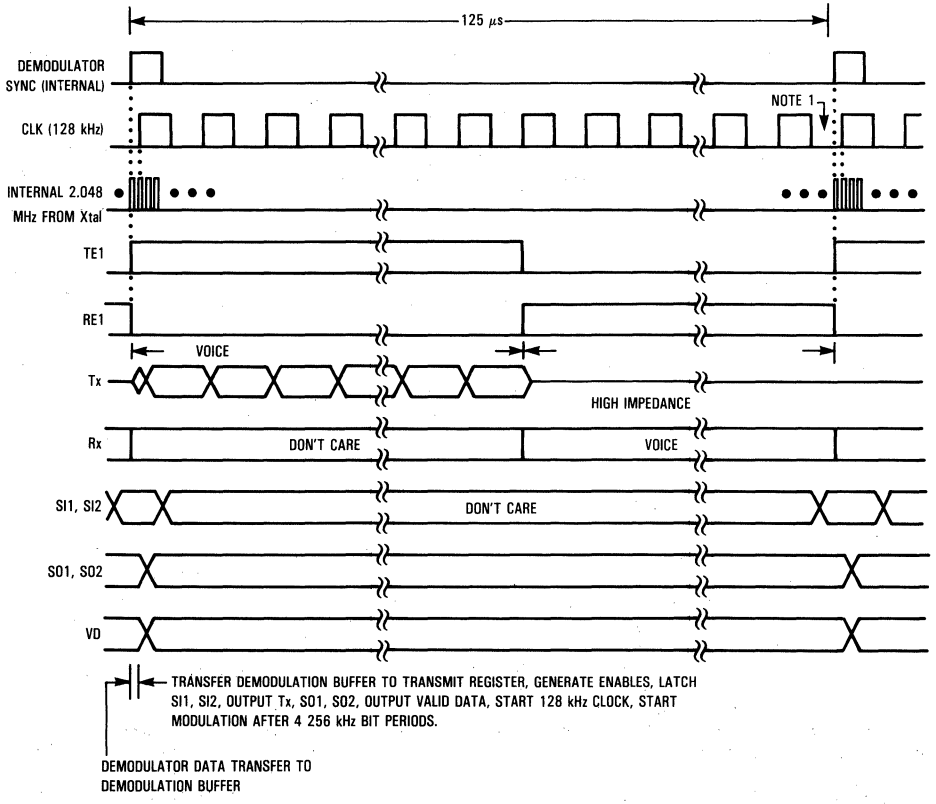
In the slave, $\overline{PD}$ is a bidirectional pin with weak output drivers such that it can be overdriven externally. When held low, the UDLT slave is powered—down and only that circuitry necessary for demodulation, TE1/RE1/CLK generation upon demodulation, and the outputting of voice and signaling bits is active. When held high, the UDLT slave is powered-up and transmits normally in response to received transmissions from the master. If no bursts have been received from the master within 250 μs after power-up (derived from the internal oscillator frequency), the UDLT generates an internal 125 μs free-running clock from the internal oscillator. The slave UDLT then bursts a transmission to the master UDLT every other 125 μs clock period using data loaded into the Rx pin during the last RE1 period and SI1, SI2 data loaded in on the internal 125 μs clock edge. The weak output drivers will try to force $\overline{PD}$ high when a transmission from the master is demodulated and will try to force it low if 250 μs have passed without a transmission from the master. This allows the slave UDLT to self power-up and down in demand powered-loop systems.



NOTE:
1. Slip between master and slave is taken up in this period.

Figure 11. Slave UDLT Timing

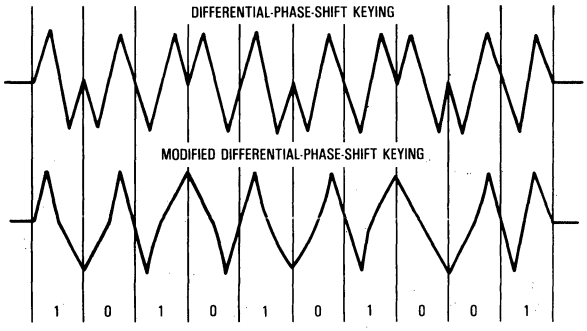
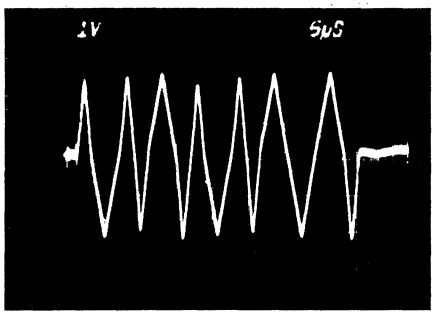


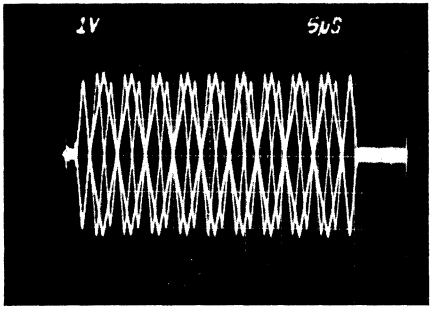
Figure 12. Modified Differential Phase Shift Keying

Both the Differential-Phase Shift Keying and the Modified Differential-Phase-Shift Keying waveforms are shown above. The DPSK encodes data as phase reversals of a 256 kHz carrier. A "0" is indicated by a 180 degree phase shift between bit boundaries, while the signal continues in phase to indicate a "1". This method needs no additional bits to indicate the start of the burst.

The Modified DPSK waveform actually used in the transceivers is a slightly modified form of DPSK, as shown in the figure. The phase-reversal cusps of the DPSK waveform have been replaced by a 128 kHz half cycle to lower the spectral content of the waveform, which, save for some key differences, appears quite similar to frequency-shift keying. The burst always begins and ends with a half cycle of 256 kHz, which helps locate bit boundaries.



13a–BIT PATTERN–1010101000



13b–BIT PATTERN–RANDOM

The bit pattern shown above in Figure 13a shows a stable waveform due to the even number of phase changes or zeros. The waveform shown in Figure 13b shows random data patterns being modulated.

Figure 13. Typical Modulated Waveforms

"Ping pong" signals on 3000 feet of 26 AWG twisted pair wire as viewed at LI (Line Input) of the master ULDT and the slave UDLT.

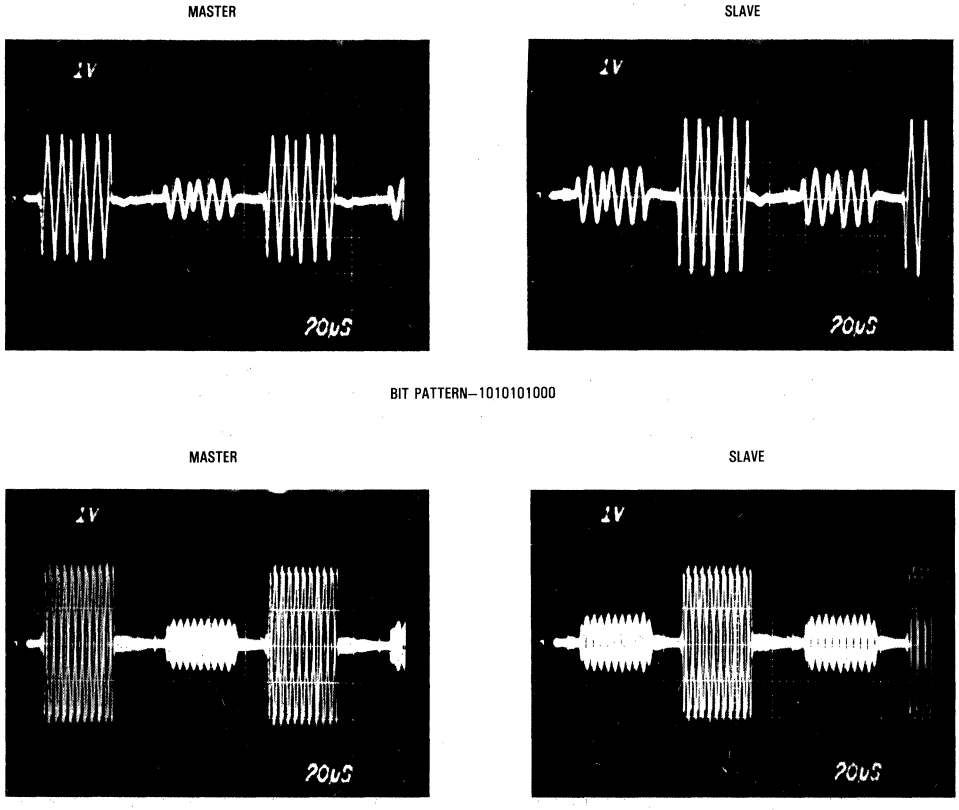


Figure 14. Typical Signal Waveforms at Demodulator

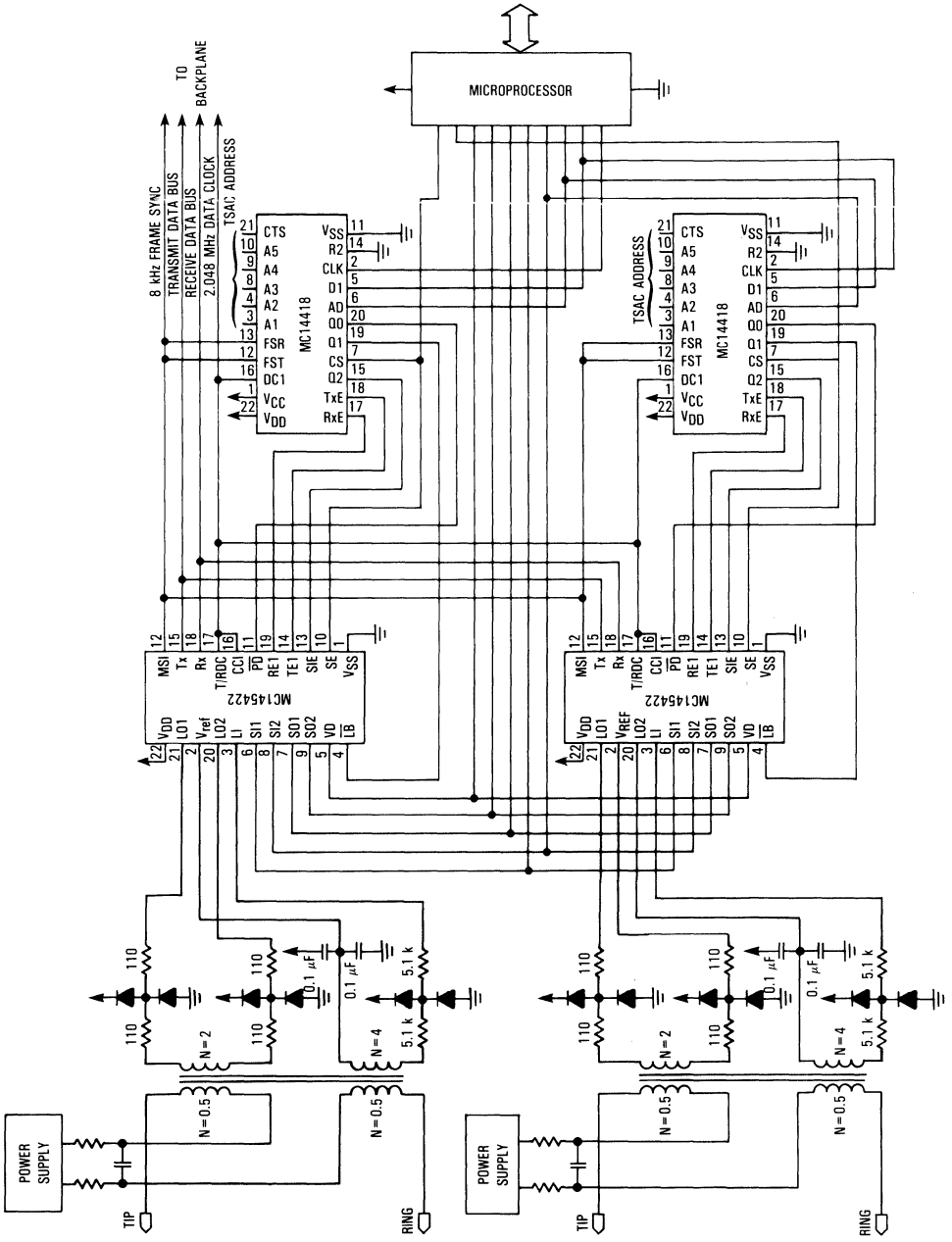


Figure 15. Typical Multichannel Digital Line Card

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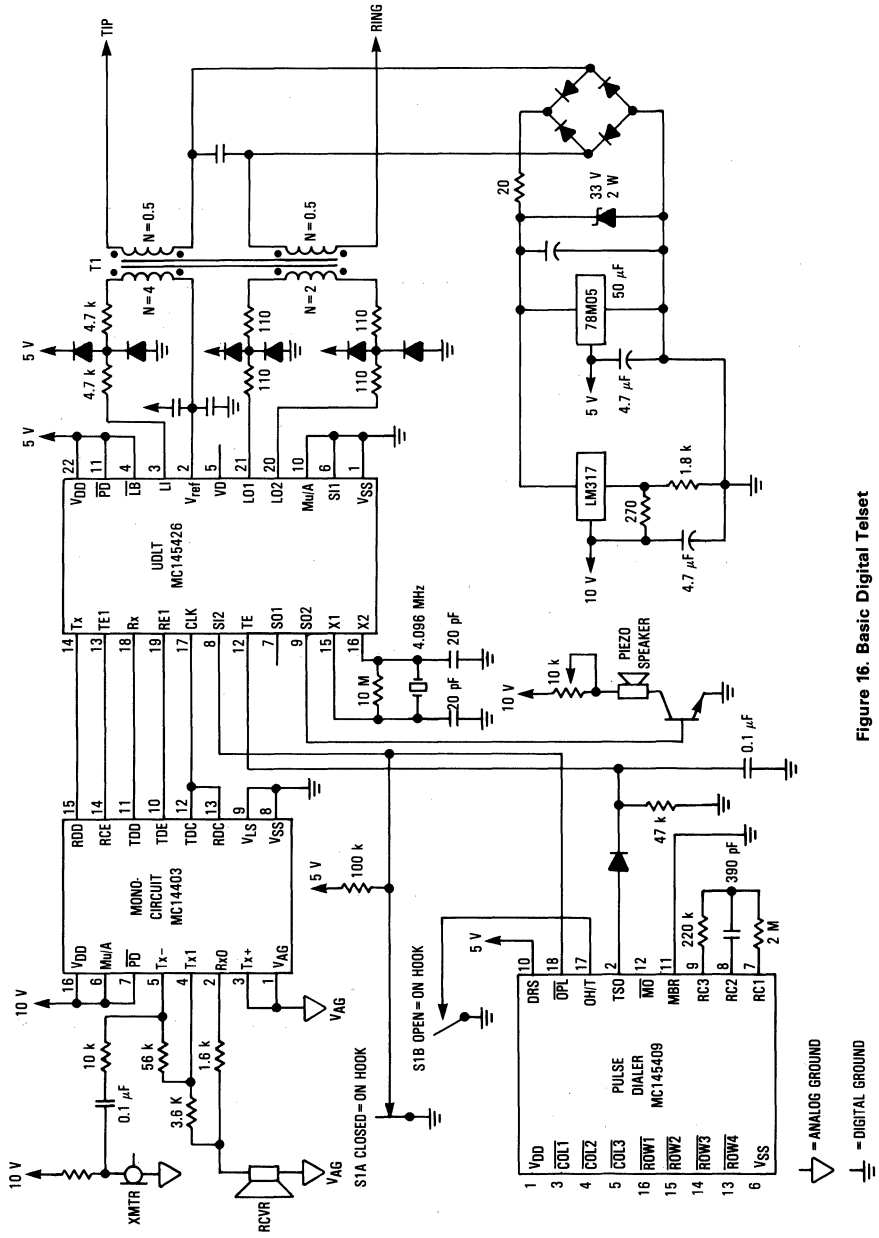

Figure 16. Basic Digital Telset

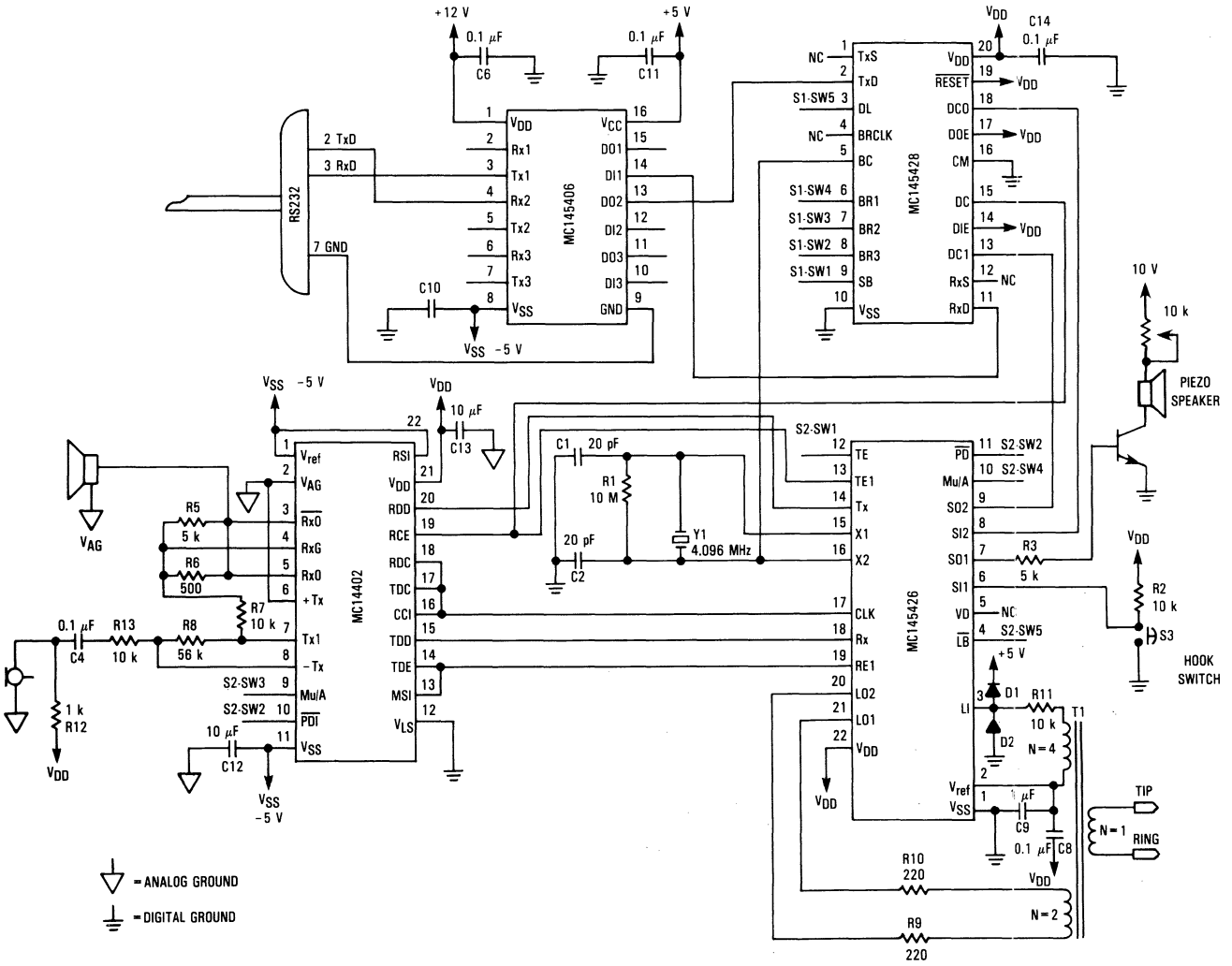

Figure 17. Full Featured Digital Telset

MC145428

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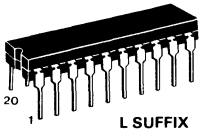
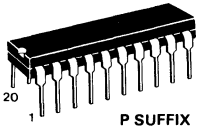
Advance Information

Data Set Interface

Asynchronous-To-Synchronous Synchronous-To-Asynchronous Converter



L SUFFIX
CERAMIC
CASE 732

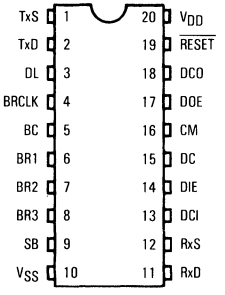


P SUFFIX
PLASTIC
CASE 738

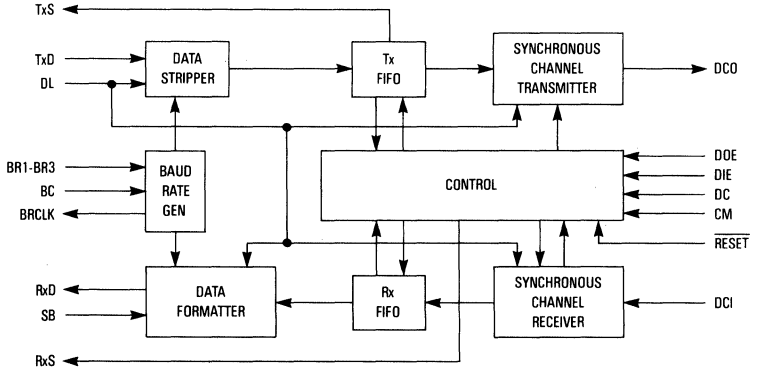
The MC145428 Data Set Interface provides asynchronous to synchronous and synchronous to asynchronous data conversion. It is ideally suited for voice/data digital telsets supplying an RS-232 compatible data port into a synchronous transmission link. Other applications include, data multiplexers, concentrators, data-only switching and PBX-based local area networks. This low power CMOS device directly interfaces with either the 64 kbps or 8 kbps channel of Motorola's MC145422 and MC145426 Universal Digital Loop Transceivers (UDLTs), as well as the MC145418 and MC145419 Digital Loop Transceivers (DLTs).

- Provides the Interface Between Asynchronous Data Ports and Synchronous Transmission Links
- Up to 128 kbps Asynchronous Data Rate Operation
- Up to 2.1 Mbps Synchronous Data Rate Operation
- On-board Bit Rate Clock Generator with Pin Selectable Bit Rates of 300, 1200, 2400, 4800, 9600, 19200 and 38400 bps or an Externally Supplied 16 Times Bit Rate Clock
- Accepts Asynchronous Data Words of Eight or Nine Bits in Length
- False Start Detection Provided
- Automatic Sync Insertion and Checking
- Single 5 Volt Power Supply
- Low Power Consumption of 5 mW Typical
- Applications Notes AN943 and AN946

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} - V_{SS}	-0.5 to 6.0	V
Voltage, Any Pin to V_{SS}	V	-0.5 to V_{DD} +0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	+10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{stg}	-85 to +150	°C

DIGITAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C)

Parameter	Symbol	V_{DD}	Min	Max	Unit
Input High Level	V_{IH}	5	3.5	—	V
Input Low Level	V_{IL}	5	—	1.5	V
Input Current	I_{in}	—	—	+1.0	μA
Input Capacitance	C_{in}	—	—	7.5	pF
Output High Current (Source) V_{OH} = 2.5 V V_{OH} = 4.6 V	I_{OH}	 5 5	 -1.7 -0.36	 — —	mA
Output Low Current V_{OL} = 0.4 V V_{OL} = 0.8 V	I_{OL}	 5 5	 0.36 0.8	 — —	mA
Operating Current (DC = 128 kHz, BC = 4.096 MHz)	I_{DD}	5	—	2.0	mA

SWITCHING CHARACTERISTICS (C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C)

Characteristic	Min	Typ	Max	Unit
Baud Clock Bit Rate Input Frequency (BR1, BR2, BR3) = (0,0,0) (BR1, BR2, BR3) = non-zero	 — —	 — —	 2.1 4.1	MHz
Baud Clock Pulse Width	100	—	—	ns
Data Clock Frequency	—	—	2.1	MHz
Data Clock Pulse Width	200	—	—	ns

MC145428 DSI PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY

The most positive power supply pin, normally 5 volts.

V_{SS}, NEGATIVE POWER SUPPLY

The most negative supply pin, normally 0 volts.

TxD, TRANSMIT DATA INPUT

Input for asynchronous data. Idle is logic high; break is 11 baud or more of logic low. One stop bit is required.

RxD, RECEIVE DATA OUTPUT

Output for asynchronous data. The number of stop bits and the data word length are selected by the SB and DL pins. Idle is logic high; break is a continuous logic low.

TxS, TRANSMIT STATUS OUTPUT

This pin will go low if the transmit FIFO holds 2 or more data words or if $\overline{\text{RESET}}$ is low.

RxS, RECEIVE STATUS OUTPUT

This pin will go low if framing of the synchronous channel is lost or not established or if $\overline{\text{RESET}}$ is low, or if the receive FIFO is overwritten.

SB, STOP BITS INPUT

This pin controls the number of stop bits the DATA FORMATTER will re-create when outputting data at the RxD asynchronous output. A high on this pin selects two stop bits; a low selects one stop bit.

DL, DATA LENGTH INPUT

This pin instructs the DSI to look for either 8 or 9 bits of data to be input at the TxD asynchronous input between the start and stop bits. The DL input also instructs the DSI's SYNCHRONOUS CHANNEL RECEIVER and SYNCHRONOUS CHANNEL TRANSMITTER to expect 8 or 9 bit data words and also instructs the DSI's DATA FORMATTER to re-create 8 or 9 data bits between the start and stop bits when outputting data at its RxD asynchronous output. A high on this pin selects a 9 bit data word; a low selects an 8 bit data word length.

2

MC145428 DSI PIN DESCRIPTIONS — cont'd.

BC, BAUD CLOCK INPUT

This pin serves as an input for an externally supplied 16 times data clock. Otherwise, the BC pin expects a 4.096 MHz clock signal which is internally divided to obtain the 16 times clock for the most frequently used standard bit rates (see BR1-BR3 pin description).

BRCLK, 16 TIMES CLOCK INTERNAL OUTPUT

This pin outputs the internal 16 times asynchronous data rate clock.

BR1, BR2, BR3, BIT RATE SELECT INPUTS

These three pins select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the internally supplied bit rates. (See Table 1.)

DCO, DATA CHANNEL OUTPUT

This pin is a three-state output pin. Synchronous data is output when DOE is high. This pin will go high impedance when DOE or $\overline{\text{RESET}}$ are low. When CM is low, synchronous data is output on DCO on the falling edges of DC as long as DOE is high. When CM is high, synchronous data is output on DCO on the rising edges of DC, while DOE is held high. No more than eight data bits can be output during a given DOE high interval when CM = high. This feature allows the DSI to interface directly with the MC145422/26 Universal Digital Loop Transceivers (UDLT's) and PABX time division multiplexed highways.

DOE, DATA OUTPUT ENABLE INPUT

See DCO pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DIE, DATA INPUT ENABLE INPUT

See DCI pin description and the SYNCHRONOUS CHANNEL INTERFACE section.

DC, DATA CLOCK INPUT

See DCI and DCO pin descriptions and the SYNCHRONOUS CHANNEL INTERFACE section.

CM, CLOCK MODE INPUT

See the SYNCHRONOUS CHANNEL INTERFACE section and the SYNCHRONOUS CLOCKING MODE SUMMARY. (See Table 2.)

$\overline{\text{RESET}}$, RESET INPUT

When held low, this pin clears the internal FIFO's, forces the TxD asynchronous input to appear high to the DSI's internal circuitry, forces TxS and RxS low. When returned high, normal operation results.

When the $\overline{\text{RESET}}$ input is returned high the DSI's SYNCHRONOUS CHANNEL RECEIVER will not accept or transfer any incoming data words on the DCI pin to the Rx FIFO until one "flag" word is input at the DCI pin. (Also see RxS pin description.)

DCI, DATA CHANNEL INPUT

Synchronous data is input on this pin on the falling edges of DC when DIE is high.

Table 1. Programmable Baud Rates

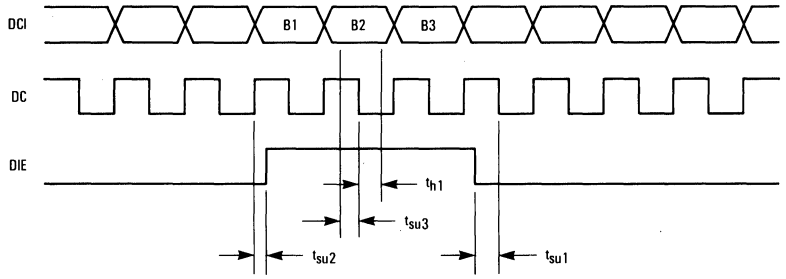
BR3	BR2	BR1	Bit Rate (bps)	BC in MHz	BRCLK
0	0	0	Variable 0 to 128 kbps	0 to 2.1 MHz	0 to 2.1 MHz
0	0	1	38.4 k	4.096	614.4 kHz
0	1	0	19.2 k	4.096	307.2 kHz
0	1	1	9600	4.096	153.6 kHz
1	0	0	4800	4.096	76.8 kHz
1	0	1	2400	4.096	38.4 kHz
1	1	0	1200	4.096	19.2 kHz
1	1	1	300	4.096	4.8 kHz

CM = LOW, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1A)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Fall Before DC Falls	t_{su1}	40	-9	—	ns	1
DIE Rise After Rise of DC	t_{su2}	40	+24	—	ns	2
DCI Data Stable Before DC Falling Edge	t_{su3}	40	-5	—	ns	3
DCI Data Stable After DC Falling Edge	t_{h1}	40	0	—	ns	4

NOTES:
1. Time DIE must fall before DC falls in order to avoid reading the bit after B3.
2. Time DC must be high before DIE rise in order to avoid clocking in the bit before B1. (See Synchronous Channel Interface for further details and see Figure 1A.)
3. Time data must be stable on the DCI pin before falling edge of the data clock DC.
4. Time data must be stable on the DCI pin after the falling edge of the data clock DC.



NOTE: When CM = 0, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL NAND of $\overline{DC}$ and DIE.
i.e. ⇓ of $\overline{DC}$ • DIE

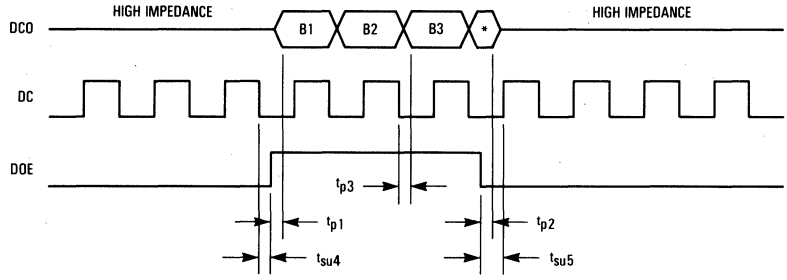
Figure 1A. CM = Low, Synchronous Channel Receiver Input Switching Characteristics

CM = LOW, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1B)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su4}	0	10	—	ns	5
DOE Falling to DC Rising	t_{su5}	40	-5	—	ns	6
DOE Rising to DCO Active	t_{p1}	50	28	—	ns	7
DOE Falling to High-Z of DCO	t_{p2}	50	26	—	ns	8
DC Falling to DCO	t_{p3}	80	71	—	ns	9

NOTES:
5. Time DC must be low before the rising edge of DOE in order to avoid clocking out a data bit before B1. (See Synchronous Channel Interface section for further details and also Figure 1B.)
6. Time DOE must be low before the rising edge of DC in order for the (*) bit to be output in the B1 position in the next cycle.
7. Propagation delay time from the rising edge of DOE to the low output impedance state of the DCO pin.
8. Propagation delay time from the falling edge of DOE to the high output impedance state of the DCO pin.
9. Propagation delay time from the falling edge data of the data clock DC to valid data on the DCO pin.



*This bit will be output in the B1 position on the next cycle of DOE.

NOTE: When CM = Low, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL NAND of DC and DOE. i.e. ↑ of $\overline{DC \bullet DOE}$

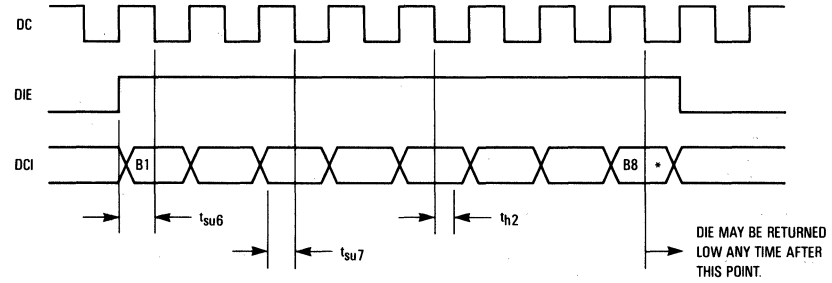
Figure 1B. CM = Low, Synchronous Channel Transmitter Output Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL RECEIVER INPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1C)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DIE Rising to DC Falling	t_{su6}	100	76	—	ns	10
DCI to DC Falling	t_{su7}	40	-4	—	ns	11
DC Falling to DCI	t_{h2}	20	0	—	ns	12

NOTES:
10. Time DIE must be high before the falling edge of DC in order for the data bit to be accepted by the synchronous data input of the DSI. (See Synchronous Channel Interface for further details.)
11. Time DCI data must be stable before the falling edge of the data clock DC.
12. Time DCI data must be stable after the falling edge of the data clock DC.



*Last bit accepted.

NOTE: When CM = 1, data bits are read into the DSI's SYNCHRONOUS CHANNEL RECEIVER at the DCI pin on the falling edge of the signal formed by the LOGICAL AND of DC and DIE. (DC ● DIE)

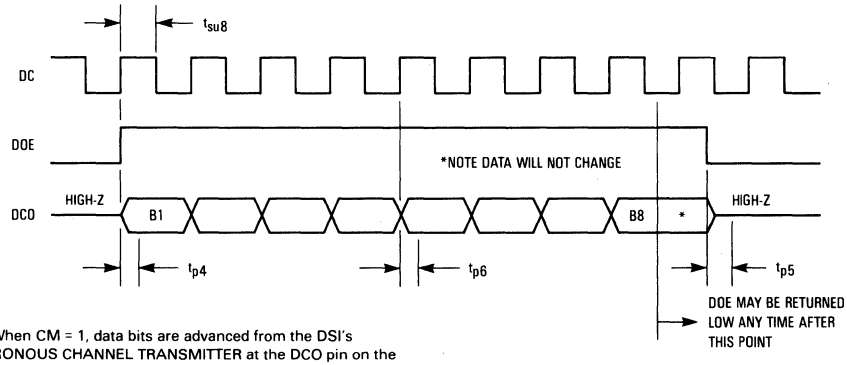
Figure 1C. CM = High, Synchronous Channel Receiver Input Switching Characteristics

CM = HIGH, SYNCHRONOUS CHANNEL TRANSMITTER OUTPUT SWITCHING CHARACTERISTICS

(C_L = 50 pF, V_{DD} = 5 V, T_A = 25°C) (See Figure 1D)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
DC Falling to DOE Rising	t_{su8}	100	82	—	ns	13
DOE Rising to Active Data on DCO	t_{p4}	105	87	—	ns	14
DOE Falling to High-Z on DCO	t_{p5}	50	28	—	ns	15
DC Rising to DCO	t_{p6}	100	74	—	ns	16

NOTES:
13. Time DOE must be high before the falling edge of the data clock DC.
14. Time delay between the rise of the DOE pin and the time the DCO reaches the low impedance state.
15. Time delay between the fall of the DOE pin and the time the DCO pin reaches the high impedance state.
16. Delay from the rising edge of the data clock DC to the valid data on the DCO pin.



NOTE: When CM = 1, data bits are advanced from the DSI's SYNCHRONOUS CHANNEL TRANSMITTER at the DCO pin on the rising edge of the signal formed by the LOGICAL AND of DC and DOE. (DC • DOE)

Figure 1D. CM = High, Synchronous Channel Transmitter Output Switching Characteristics

CIRCUIT DESCRIPTION

The MC145428 Data Set Interface provides a means for conversion of an asynchronous (start/stop format) data channel to a synchronous data channel and synchronous to asynchronous data channel conversion. Although primarily intended to facilitate the implementation of RS-232 compatible asynchronous data ports in digital telephone sets using the MC145422/26 UDLTs, this device is also useful in many applications that require the conversion of synchronous and asynchronous data.

TRANSMIT CIRCUIT

Asynchronous data is input on the TxD pin. This data is expected to consist of a start bit (logic low) followed by eight or nine data bits and one or more stop bits (logic high). The length of the data word is selected by the DL pin. The data baud rate is selected with the BR1, BR2, and BR3 pins to obtain the internal sampling clock. This internal sampling clock is selected to be 16 times the baud rate at the TxD pin. An externally supplied 16 times clock may also be used, in which case, the BR1, BR2, and BR3 pins should all be at logic zero and the 16 times sampling clock supplied at the BC pin.

Data input at the TxD pin is stripped of start and stop bits and is loaded into a four-word deep FIFO register. A break condition is also recognized at the TxD pin and this information is relayed to the synchronous channel transmitter which codes this condition so it may be re-created at the remote receiving device.

The synchronous channel transmitter sends one bit at a time under control of the DC, CM, and DOE pins. The synchronous channel transmitter transmits one of three possible data patterns based on whether or not the top of the Tx FIFO is full and whether or not a break condition has been recognized by the data stripper. When no data is available at the top of the Tx FIFO for transmission, the synchronous data transmitter sends a special synchronizing flag pattern (01111110). When a break condition is detected by the data stripper and no data is available at the top of the Tx FIFO, the break pattern (11111110) is sent. Figure 2A depicts this operation.

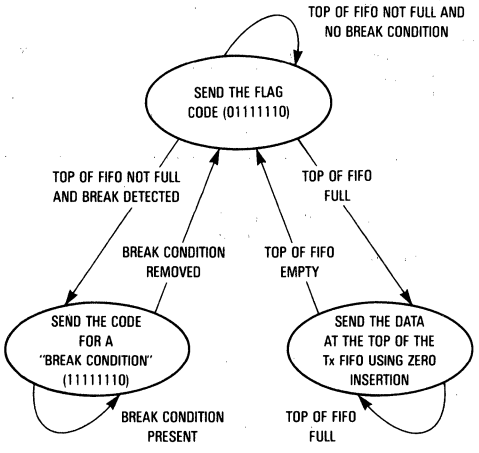


Figure 2A. Synchronous Data Channel Transmitter Operation

When stripped data words reach the top of the Tx FIFO they are loaded into the SYNCHRONOUS CHANNEL TRANSMITTER and are sent using a special zero insertion technique. When stripped data is being transmitted, the synchronous data transmitter will insert a binary 0 after any succession of five continuous 1's of data. Therefore, using this technique, no pattern of (01111110) or (11111110) can occur while sending data. This also allows the DSI to synchronize itself to the incoming synchronous data word boundaries based on the data alone.

The receive section of the DSI (synchronous channel receiver) performs the reverse operation by removing a binary 0 that follows five continuous 1's in order to recover the transmitted data. (Note that a binary 1 which follows five continuous 1's is not removed so that flags and breaks may be detected.) Figure 2B shows an example of this process.

ASYNCHRONOUS DATA WORD RECEIVED AT THE TxD PIN
11111111, 11000000, 11111100

ACTUAL SYNCHRONOUS WORDS TRANSMITTED BY THE SYNCHRONOUS CHANNEL TRANSMITTER
FLAG, 01111110, 111110111, 110000000, 111110100, 01111110, FLAG, FLAG, ···

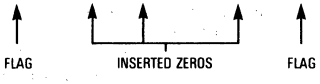


Figure 2B. Data Format Protocol

If the incoming data rate at TxD exceeds the rate at which it is output at DCO, the FIFO will fill. The TxS pin will go low when the FIFO contains two or more words. TxS may, therefore, be used as a local Clear-to-Send control line at the asynchronous interface port to avoid transmit data over-runs.

In order to insure synchronization during the transfer of a continuous stream of data the DSI's synchronous channel transmitter will insert a flag synchronizing word (01111110) every 61st data word. The DSI's synchronous channel receiver checks for this synchronizing word and if not present, the loss of synchronization will be indicated by the RxS pin being latched low until the flag synchronizing word is received. Note that under these conditions the data will continue to output at RxD.

RECEIVE CIRCUIT

Data incoming from the synchronous channel is loaded into the MC145428 at the DCI pin under the control of the DC and DIE pins (see SYNCHRONOUS CHANNEL INTERFACE section). Framing information, break code detection, and data word recovery functions are performed by the SYNCHRONOUS CHANNEL RECEIVER. Recovered data words are loaded into the four word deep Rx FIFO. When the recovered data words reach the top of the Rx FIFO they are taken by the DATA FORMATTER, start and stop bits are re-inserted and the reconstructed asynchronous data is output at the RxD pin at the same baud rate as the transmit side. The number of stop bits and word length are those selected by the SB and DL pins.

Loss of framing, if it occurs, is indicated by the RxS pin going low. Data will continue to be output under these conditions, but RxS will remain low until frame synchronization, i.e., the detection of a framing flag word, is re-established. If the output data rate is less than the data rate of the incoming synchronous data channel, data will be lost at a rate of one word at a time due to the bottom word on the Rx FIFO being overwritten. In order to prevent data loss (in the form of asynchronous terminal to asynchronous terminal over-runs) due to clock slip between remote DSI links, (during long bursts of continuous data) the DSI purposely reduces the length of the stop bit which it re-creates at its RxD output by 1/32nd. This action allows the originator of a transmission (of asynchronous data) to be up to 3% faster than the receive device is expecting for any given data rate. This tolerance is well within the normally expected differences in clock frequencies between remote stations. If the Rx FIFO is overwritten the RxS line will pulse low for one DC clock period following the over-writing of the bottom level of the Rx FIFO.

INITIALIZATION

Initialization is accomplished by use of the $\overline{\text{RESET}}$ pin. When held low, the internal FIFOs are cleared, the TxD input appears high to the data strippers internal circuitry, DCO is forced to a high impedance state, TxS and RxS are forced low. When brought high normal operation resumes and the synchronous channel transmitter sends the flag code until data has reached the top of the Tx FIFO. Note that the TxS line will immediately go high after $\overline{\text{RESET}}$ goes high, while RxS

will remain low until framing is detected. The synchronous channel receiver section of the DSI is forced into a "HOLD" state while the $\overline{\text{RESET}}$ line is low. The synchronous channel receiver remains in the "HOLD" state after $\overline{\text{RESET}}$ goes high until a flag code word (01111110) is received at the DCI pin. While in the "HOLD" state no data words can be transferred to the Rx FIFO and, therefore, the DATA FORMATTER and RxD line are held in the MARK idle state. After receiving the flag code pattern the RxS line goes high and normal operation proceeds. $\overline{\text{RESET}}$ should be held low when power is first applied to the DSI. $\overline{\text{RESET}}$ may be tied high permanently, if a short period of undefined operation at initial power application can be tolerated.

SYNCHRONOUS CHANNEL INTERFACE

The synchronous channel interface is generally operated in one of three basic modes of operation. The first is a continuous mode. A new data bit is clocked out of the DCO pin on each successive falling edge of the DC clock, and a new data bit is accepted by the DSI at its DCI pin on each successive falling edge of the DC clock. In this mode of operation, the CM control line is always low and the DOE and DIE enable control lines are always high. This is the typical setup when interfacing the DSI to the 8 kbps signal bit inputs and outputs of the MC145422/26 UDLTs. (See Figures 3A and 4.)

The second synchronous clocking mode is one in which 8 bits at a time are clocked out of the SYNCHRONOUS CHANNEL TRANSMITTER, and 8 bits are read by the SYNCHRONOUS CHANNEL RECEIVER at a time. The transferring of these 8 bit groups of data would normally be repeated on some cyclic basis. An example is a time division multiplexed data highway. In this mode (CM = 1), the rising edge of the enable signal DIE and DOE should be roughly aligned to the rising edge of the DC clock signal. When enabled, the data is clocked out on the rising edge of the DC clock through the DCO pin and clocked in on the falling edge of the DC clock through the DCI pin. A variation of this clocking mode is to transfer less than 8 bits of data into or out of the DSI on a cyclic basis. If less than eight bits are to be transmitted and received, enable pins DIE and DOE should be returned low while the DC clock is low. This is illustrated in Figure 3D where five bits are being clocked out of the DSI through the DCO pin and four bits are being input to the DSI through the DCI pin.

This restriction does not apply if eight bits are to be clocked into or out of the synchronous channels of the DSI; i.e., the DSI has internal circuitry to prevent more than eight clocks following the rising edge of the respective enable signals). Figure 3B illustrates a timing diagram depicting an eight bit data format. If the DOE enable is held high beyond the eight clock periods the last data bit B8 will remain at the output of the DCO pin until the DOE enable is brought low to reinitialize the sequence. Similarly the DSI's SYNCHRONOUS CHANNEL RECEIVER will read (at its DCI input) a miximum of eight data bits for any given DIE high period.

The CM = high mode, using 8 bits of data, is the typical setup for interfacing the DSI to the 64 kbps channel of the MC145422 or MC145426 Universal Digital Loop Transceivers. (See Figure 3B and Figure 5.)

In the third mode of operation, an unlimited variable number of data bits may be clocked into or out of the synchronous side of the DSI at a time. When the CM line is low, any number of data bits may be clocked into or out of the DSI's synchronous channels provided that the respective enable signal is high. Figure 3C illustrates three data bits being clocked out of the DCO pin and three data bits being clocked into the DCI pin.

In the CM = low mode of operation, an internal clock is formed, which is the logical NAND of DC, DOE and $\overline{\text{CM}}$, ($\overline{\text{DC} \bullet \text{DOE} \bullet \text{CM}}$). It is on the rising edge of this signal that a new data bit is clocked out of the DCO pin. Therefore, the DOE signal should be raised and lowered following the falling edge of the DC clock (i.e., when the DC clock is low).

Also in the CM = low mode of operation, another internal clock is formed which is the logical NAND of $\overline{\text{DC}}$, DIE, and $\overline{\text{CM}}$ ($\overline{\text{DC} \bullet \text{DIE} \bullet \text{CM}}$). It is on the falling edge of this signal that a new bit is clocked into the DCI pin. Therefore the DIE signal should be raised and lowered following the rising edge of the DC clock (i.e., when the DC clock is high).

The following table summarizes when data bits are advanced from the synchronous channel transmitter and when data bits are read by the synchronous channel receiver dependent on the CM control line. (Shown below in Table 2.)

Table 2. Synchronous Clocking Mode Summary

Mode	Bits Advanced From The Synchronous Channel Transmitter On;	Bits Read By The Synchronous Channel Receiver On:
CM = 0	The rising edge of an internal clock formed by the logical NAND of DOE and DC. i.e ↑ of $\overline{\text{DOE} \bullet \text{DC}}$	The falling edge of an internal clock formed by the logical NAND of DIE and $\overline{\text{DC}}$. i.e. ↓ of $\overline{\text{DIE} \bullet \overline{\text{DC}}}$
CM = 1	The rising edge of an internal clock formed by the logical AND of DOE and DC. i.e. ↑ of DOE • DC	The falling edge of an internal clock formed by the logical AND of DIE and DC. i.e. ↓ of DIE • DC

2

TIMING DIAGRAMS

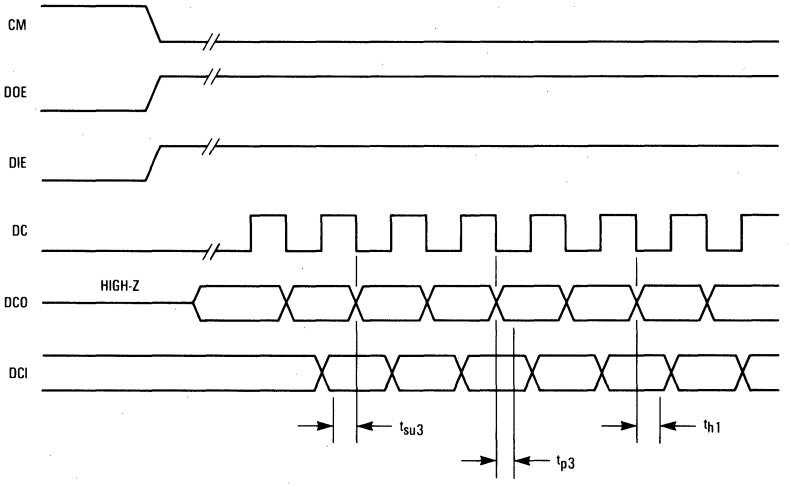


Figure 3A. Synchronous I/O, Continuous Bit Rate, Clock Mode Low

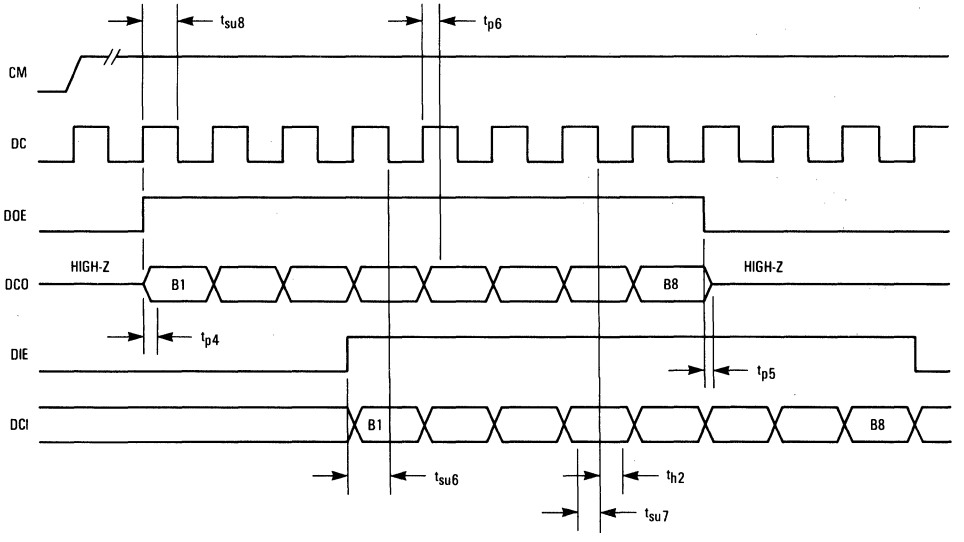


Figure 3B. Synchronous I/O, Eight Bit, Clock Mode High

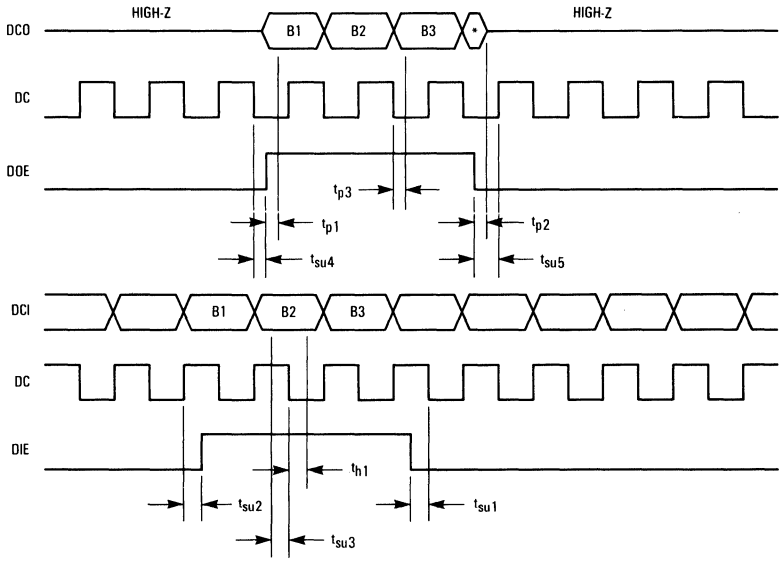


Figure 3C. Synchronous I/O, Variable Bit Length, Clock Mode Low

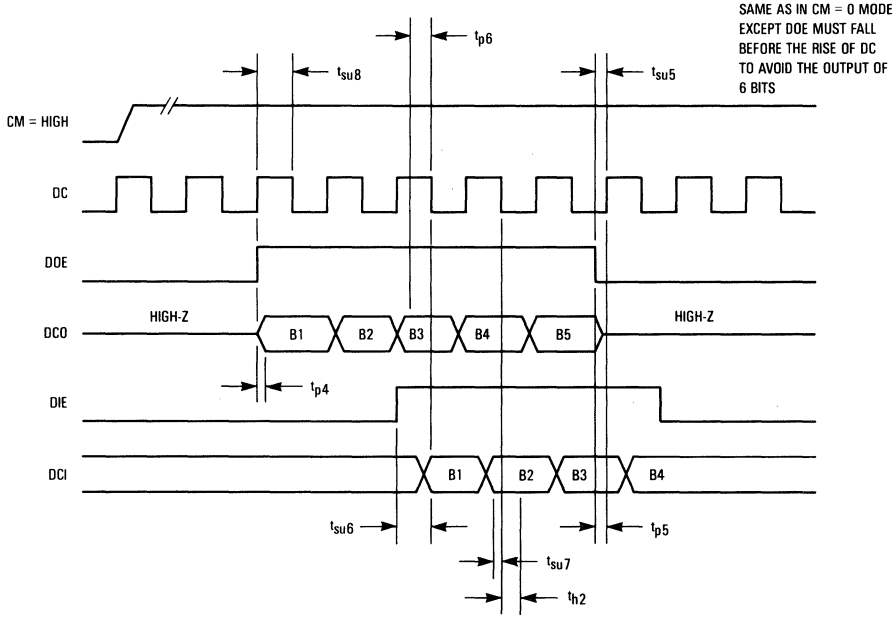
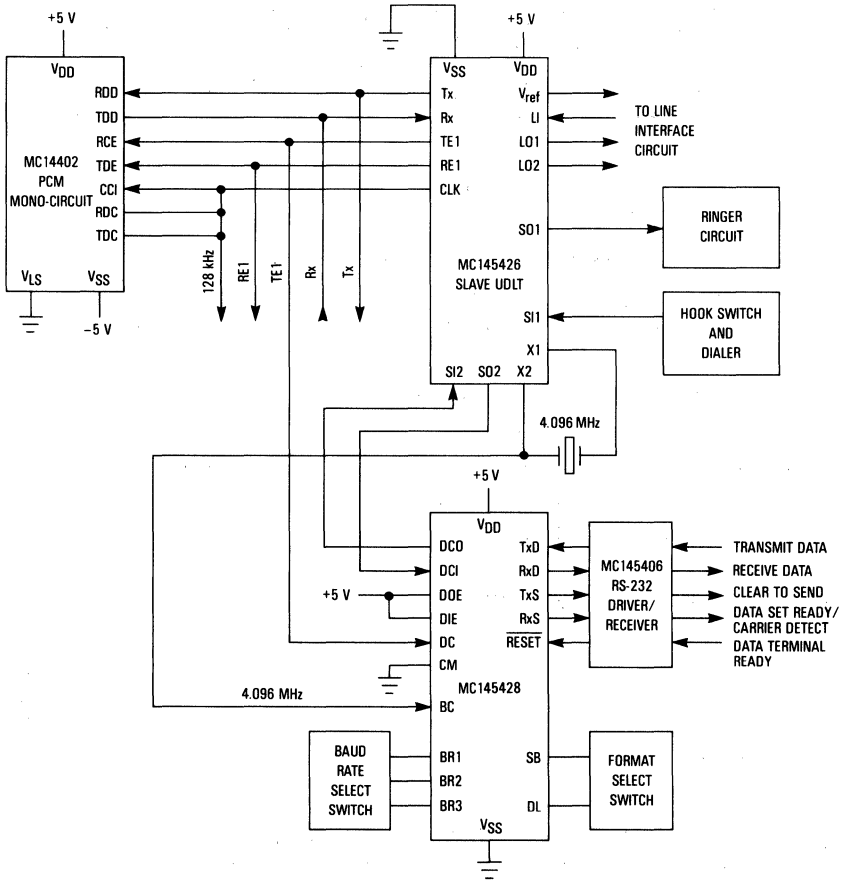
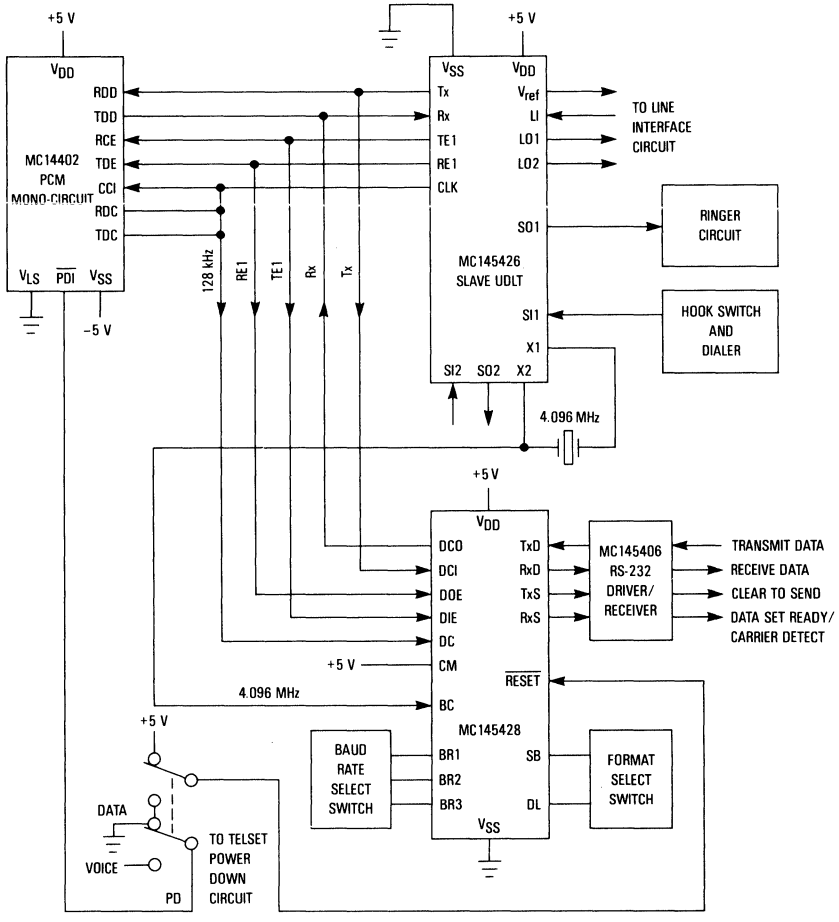


Figure 3D. Synchronous I/O, Variable Bit Length, Clock Mode High



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 4. Digital Telset RS-232 Port Using 8 Kilobits/Second Channel of MC145426



NOTE: Some pin connections on the MC145426 and MC14402 have been omitted. Consult MC145426 and MC14402 data sheets for more details.

Figure 5. Digital Telset RS-232 Port Using 64 Kilobits/Second Channel of MC145426 for Voice or Data

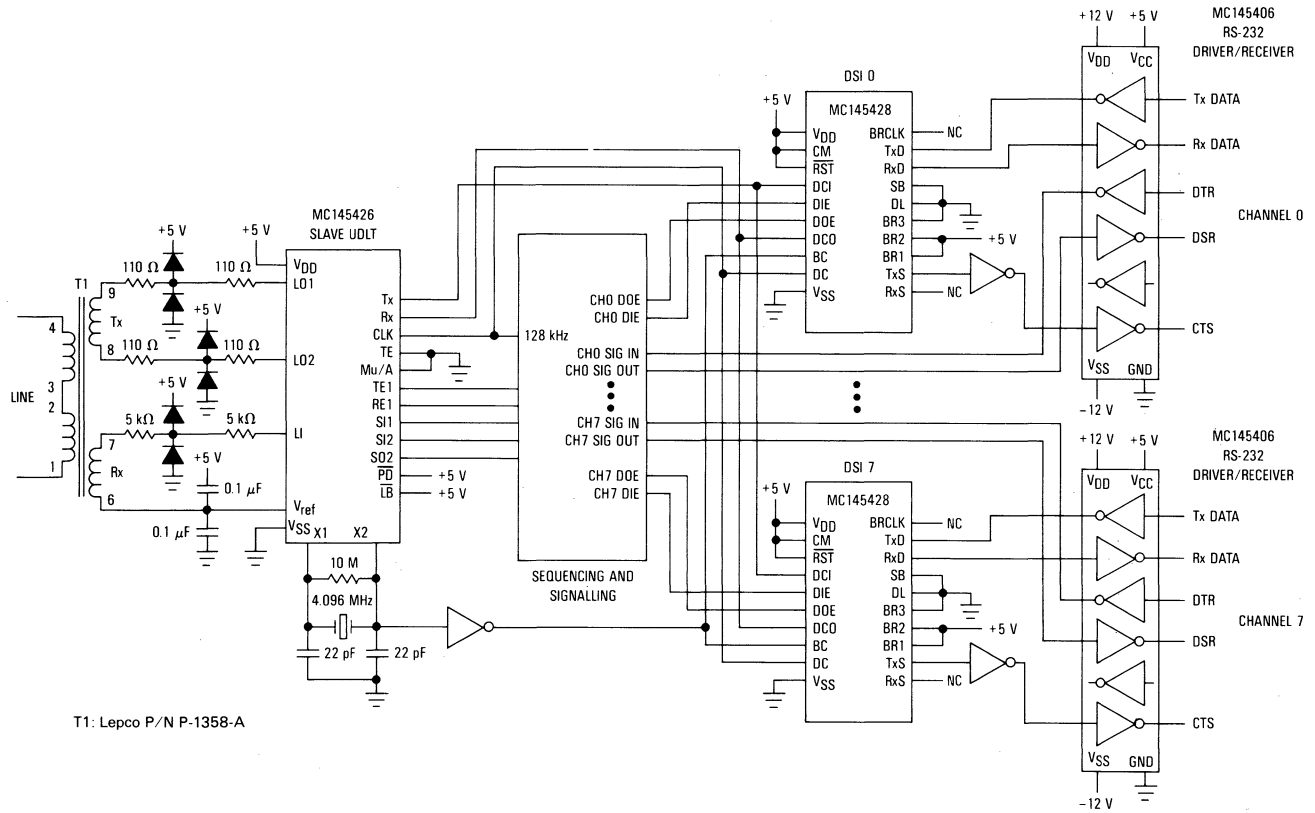


Figure 6. Multiplexing Eight RS-232 Telset Ports Into 64 Kilobits/Second Channel of MC145426

MC145429

Advance Information

CMOS
(LOW-POWER COMPLEMENTARY MOS)

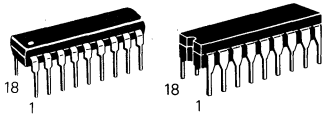
TELSET
AUDIO INTERFACE
CIRCUIT

2

TELSET AUDIO INTERFACE CIRCUIT

The MC145429 is a silicon-gate CMOS Telset Audio Interface Circuit (TAIC) intended for microcomputer controlled digital or analog telset applications. The device provides the interface between a codec/filter or analog speech network and the telset mouthpiece, earpiece, ringer/speaker amplifier, and an auxiliary input and output. The configuration of the device is programmed via a serial digital data port. Features provided on the device include:

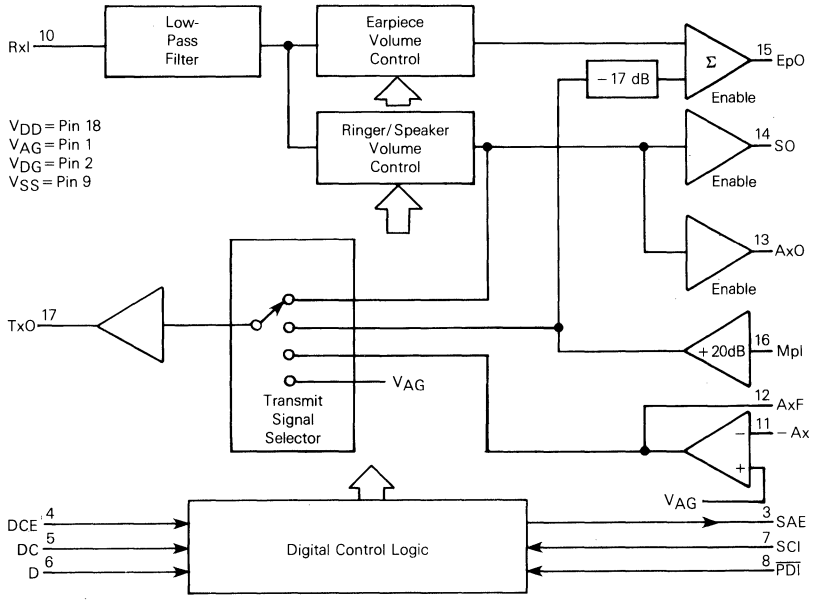
- Independent Adjustment of Earpiece, Speaker, and Ringer Volume
- Transient Suppression Circuitry to Prevent Acoustic "Pops"
- Receive Low-Pass Filter for 8 kHz Attenuation
- Sixteen Possible Audio Configurations
- Power-Down Mode with Data Retention
- 20 dB Mouthpiece Input Gain
- Receive to Transmit Loopback Test Mode
- Provision for Auxiliary Input and Output
- Externally Adjustable Auxiliary Input Gain
- PCM Mono-circuit Compatible Power Supply Range
- Digital Output for Speaker Amplifier Control
- Versatile Logic Input Levels
- 18-Pin Package



P SUFFIX
PLASTIC PACKAGE
CASE 707

L SUFFIX
CERAMIC PACKAGE
CASE 726

SIMPLIFIED BLOCK DIAGRAM



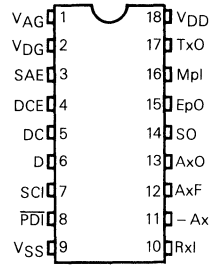
This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

PIN ASSIGNMENTS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	6	10 to 12	13	V
DC Supply Voltage Nominally $(V_{DD}-V_{SS})/2$	$V_{DD}-V_{DG}$	3	5 to 7	7.5	V
Power Dissipation	P_D				mW
$V_{DD}-V_{SS}$ = 10 V		–	25	50	
$V_{DD}-V_{SS}$ = 12 V		–	30	60	
Power-Down Dissipation	P_D				mW
$V_{DD}-V_{SS}$ = 12 V		–	3	5	
Full Scale Input Levels					Vpk
$V_{DD}-V_{SS}$ = 10 V RxI, AxF		–	–	3.15	
MpI		–	–	0.315	
$V_{DD}-V_{SS}$ = 12 V RxI, AxF		–	–	3.8	
MpI		–	–	0.38	
Sampling Clock Input Frequency		–	128	–	kHz

TRANSMISSION CHARACTERISTICS

(V_{DD} to V_{SS} = 10 to 12 V ±5%; T_A = 0 to 70°C; 0 dBm0 = 6 dBm ref 600 Ω; +3.17 dBm0 = 3.15 Vp; SCI = 128 kHz)

Characteristic		Min	Max	Unit
Gain				dB
840 Hz @ 0 dBm0, Max Gain Setting	RxI to EpO	−0.3	0.3	
	RxI to SO	−0.3	0.3	
	RxI to AxO	−0.3	0.3	
	RxI to TxO	−0.3	0.3	
	AxF to TxO	−0.3	0.3	
840 Hz @ −20 dBm0	MpI to TxO	19.5	20.5	
	MpI to EpO	2.5	3.5	
Gain vs Volume				dB
Relative to Volume Setting, with 840 Hz @ 0 dBm0 Input				
(−3 to −21 dB)	RxI to EpO	−0.5	0.5	
(−5 to −35 dB)	RxI to SO or AxO	−0.5	0.5	
Idle Noise				
0 to 15 kHz, AxF = −Ax, RxI = MpI = 600 Ω to V_{AG}	TxO, EpO, SO, or AxO	–	−75.0	dBm0
C-Message		–	9.0	dBrnC0
In-Band Spurious Outputs				dBm0
840 Hz @ 0 dBm0, 0.3 to 3.4 kHz, 2nd and 3rd Harmonic		–	−43.0	
Out-Band Spurious Outputs				dBm0
840 Hz @ 0 dBm0, 0 to 20 kHz		–	−40.0	
Gain vs Frequency				dB
Relative to 840 Hz @ 0 dBm0				
(0.3 to 3.0 kHz, All Gain Paths)		−0.25	0.25	
(3.4 kHz, Rx Path)		−1.0	0.25	
(8.0 kHz, Rx Path)		–	−26.0	
Crosstalk				dBm0
840 Hz @ 0 dBm0	Rx to Tx and Tx to Rx	–	−65.0	
Isolation from Any Input to Any Deselected Output				dBm0
Input = 840 Hz @ 0 dBm0		–	−75.0	

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ to 12 V ±5%, $T_A = 0$ to 70°C)

Characteristic		Min	Typ	Max	Unit
Input Leakage Current	SCI, D, DC, DCE, RxI, −Ax	–	±10	±30	nA
	V_{AG}, MpI	–	±50	±60	μA
AC Input Impedance	RxI	100	200	–	kΩ
	MpI to V_{AG}	8	10	–	
$\overline{PDI}$ Internal Input Pull Down Resistor Impedance to V_{SS}		50	100	200	kΩ
Output Voltage Range	TxO, EpO, SO, AxO				V
$V_{DD} - V_{SS} = 10$ V, $R_L = 600$ to V_{AG}		−3.2	–	3.2	
$V_{DD} - V_{SS} = 12$ V, $R_L = 900$ to V_{AG}		−3.8	–	3.8	
Output Current	TxO, EpO, SO, AxO				mA
Source		−5.5	–	–	
Sink		5.5	–	–	
Power Supply Rejection Ratio	TxO, EpO, SO, AxO	20	30	–	dB
$V_{AC} = 100$ mVrms, 0 to 20 kHz, V_{DD}, V_{SS}					

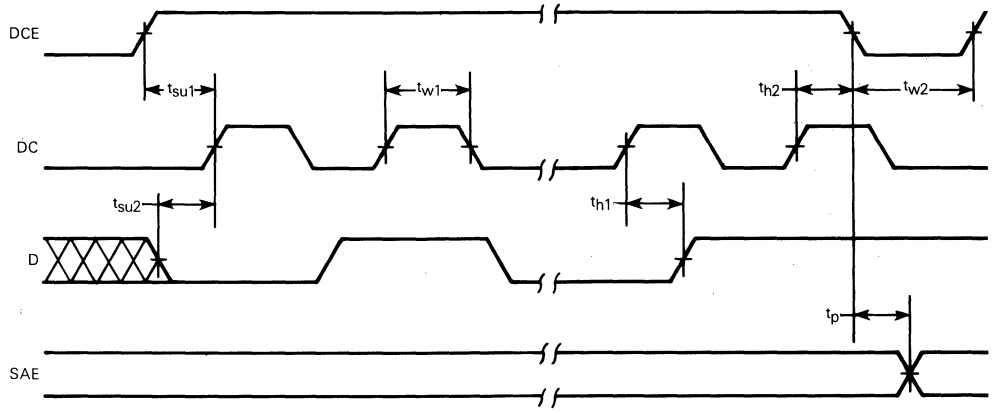
DIGITAL ELECTRICAL CHARACTERISTICS ($T_A = 0$ to 70°C, $V_{DD} = 5.0$ V, $V_{SS} = -5.0$ V, V_{DG}, $V_{AG} = 0$)

Characteristic		Symbol	Min	Max	Unit
Logic Input Voltage ($V_{DG} = 0$ V)	SCI, D, DC, DCE, $\overline{PDI}$				V
V_{SS} to V_{DD} Mode		V_{IL}	–	−3.5	
		V_{IH}	2.0	–	
V_{DG} to V_{DD} Mode		V_{IL}	–	0.8	
		V_{IH}	2.0	–	
V_{SS} to V_{DG} Mode		V_{IL}	–	−3.5	
		V_{IH}	−1.5	–	
Logic Output Voltage ($V_{DG} = 0$ V, $\|I_O\| < 1$ μA)	SAE	V_{OL}	–	−4.95	V
		V_{OH}	4.95	–	
Output Current ($V_O = -4.5$ V)	SAE	I_{OL}	0.9	–	mA
($V_O = 4.5$ V)		I_{OH}	−0.3	–	

SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C, $V_{DD} = 5.0$ V, $V_{SS} = -5.0$ V, V_{DG}, $V_{AG} = 0$)

Characteristic		Symbol	Min	Max	Unit
Maximum Frequency	DC (Data Clock)	f_{max}	–	1.0	MHz
Minimum Pulse Width	DC	t_{w1}	0.5	–	μs
Minimum Pulse Width Low (SCI = 128 kHz)	DCE	t_{w2}	33	–	
Propagation Delay (SCI = 128 kHz)	DCE to SAE	t_p	30	60	μs
Setup Times	DCE to DC	t_{su1}	0.5	–	μs
	D to DC	t_{su2}	0.5	–	
Hold Times	D to DC	t_{h1}	0.5	–	μs
	DCE to DC	t_{h2}	0.5	–	

FIGURE 1 — DATA INPUT TIMING



2

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18) — Typically +3 to +6.5 volts with V_{AG}=0 volts.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9) — Typically −3 to −6.5 with V_{AG}=0 volts.

V_{AG}, ANALOG GROUND (PIN 1) — Typically 0 volts supplied by a mono-circuit in digital telset applications. All analog signals are referenced to this pin.

V_{DG}, DIGITAL GROUND (PIN 2) — Typically common to logic ground. All internal digital logic operates between V_{DG} and V_{DD}. V_{DG} preferably equals $(V_{DD}-V_{SS})/2$.

SAE, SPEAKER AMPLIFIER ENABLE (PIN 3) — The SAE output will be at V_{DD} whenever the external speaker amplifier is required, otherwise SAE is at V_{SS}.

DCE, DATA CLOCK ENABLE (PIN 4) — This digital input enables the serial data entry circuitry and also latches the serial data into the appropriate data register.

DC, DATA CLOCK (PIN 5) — This digital input allows data on the D pin to be shifted into the serial input data register on rising edges of DC whenever DCE is active.

D, DATA (PIN 6) — Digital data, required to set the configuration or gain of the audio interface, is applied to the D pin and will be shifted into the serial input register by DC whenever DCE is active.

SCI, SAMPLING CLOCK INPUT (PIN 7) — The clock applied to this digital input is used to sample the audio signals. This frequency is nominally 128 kHz and is typically provided by the slave Universal Digital Loop Transceiver such as the MC145426 in digital telset applications. This clock must be applied during data transfers.

$\overline{PDI}$, POWER-DOWN INPUT (PIN 8) — This pin allows all analog circuitry on the device to be powered down while retaining all digital data. An internal pull-down resistor connected to V_{SS} will insure the powered-down state during system power up.

RxI, RECEIVE INPUT (PIN 10) — This pin is the input to the receive low-pass filter and volume controls, and is typically driven from RxO of a mono-circuit in digital telset applications.

−Ax, INVERTING AUXILIARY INPUT (PIN 11), AxF, AUXILIARY FEEDBACK (PIN 12) — These two pins are the inverting input and output, respectively, of the auxiliary input operational amplifier and are used to set the gain of the auxiliary input. The noninverting input of the Ax amp is internally connected to V_{AG}.

AxO, AUXILIARY OUTPUT (PIN 13) — This output drives the input to an external auxiliary circuit and will be at V_{AG} when disabled.

SO, SPEAKER OUTPUT (PIN 14) — This output drives an external speaker amplifier, and when disabled will be at V_{AG}.

EpO, EARPIECE OUTPUT (PIN 15) — This output drives the handset earpiece which may require a series resistor to set the correct signal level. This output will be at V_{AG} when disabled.

MpI, MOUTHPIECE INPUT (PIN 16) — The mouthpiece microphone circuit is connected to this pin.

TxO, TRANSMIT OUTPUT (PIN 17) — This is the audio output pin of the device and is typically used to drive the TxI pin of a mono-circuit in digital telset applications.

DEVICE OPERATION

The telset audio interface IC consists of two major sections: an analog subsystem and a digital subsystem. The digital subsystem provides an interface to a microcomputer and generates the necessary control signals to configure the analog subsystem as desired.

ANALOG SUBSYSTEM

The analog subsystem provides the low-pass filtering, audio-signal routing, gain adjustment, and signal summing required for a digital or analog telset application. This subsystem consists of a receive and a transmit signal path.

RECEIVE SIGNAL PATH

The receive audio signal, typically from the RxO output of a PCM mono-circuit or a speech network, is input to the audio interface via the RxI pin. Once buffered into the device and passed through the low-pass filter, the audio signal has four possible destinations: earpiece output, speaker output, auxiliary output, or loopback to the TxO output.

The audio path to the earpiece output consists of an earpiece volume control and summing output amplifier. The volume control is an eight-step attenuation circuit with −3 dB steps and unity gain at the maximum setting. The steps are selected by a 3-bit binary code with 0_8 and 7_8, the minimum and maximum settings, respectively. The output of the earpiece volume control is summed (0 dB gain) with a sidetone (−17 dB gain) from the mouthpiece input. The earpiece output is capable of driving an earpiece transducer which typically requires 200 mVp-p into 150 ohms. The gain to the earpiece to attain the proper sound pressure level may be adjusted with a resistor in series with the earpiece. When the audio interface is configured such that the earpiece is not selected, the earpiece volume control and the summing output amplifier are powered down.

The audio path to the speaker output consists of a volume control and an output driver. The volume control is an eight-step attenuation circuit with −5 dB steps and unity gain at the maximum setting. The steps are selected by a 3-bit binary code with 0_8 and 7_8, the minimum and maximum settings, respectively. The binary code may be from either of two volume registers: the speaker volume register, selected when the speaker is used for voice, or the ringer volume register, selected when the speaker is used for ringing. The register used is determined by the current configuration of the audio interface. The output of the volume control is fed into a unity gain output buffer which is intended to drive a speaker power amplifier. The speaker/ringer volume control and output buffer power down when not selected.

The auxiliary output is similar to the speaker output and is powered down when not needed. This output can be used to drive a conference phone circuit or the receive portion of a modem.

The three analog outputs, EpO, SO, and AxO, have a transient suppression circuit which eliminates the possibility of acoustic "pops" during configuration or volume changes. This same circuit keeps the output at V_{AG} when it is not selected. When enabled, the output signal slews directly from V_{AG} to the audio signal.

The other possible destination for the receive audio is the TxO audio output. This is an audio loopback configuration

which allows a system to test the operation of the audio path in the telset. In the loopback configuration, the output of the ringer/speaker volume control is switched into the TxO output amplifier input.

TRANSMIT SIGNAL PATH

The transmit portion of the analog subsystem consists of a unity gain output driver which has three possible inputs. The input selection depends upon the current configuration of the audio interface. One of these inputs is used in the loopback configuration discussed above. The auxiliary inputs, AxF and −Ax, allow gain adjustment from an auxiliary circuit, and the third input, MpI, is from the mouthpiece microphone and is amplified 20 dB by the input amplifier. Two configurations allow use of the auxiliary inputs as a mouthpiece input without sidetone, which is useful in analog telset applications.

DIGITAL SUBSYSTEM

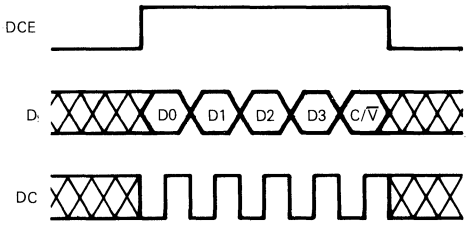
The digital subsystem provides a three-wire serial input which allows a microcomputer to program the audio configuration of the audio interface.

Data is clocked into the audio interface using the DCE, DC, and D pins. DCE going high enables the data input circuitry. While DCE is high, data appearing on the D pin is clocked into the serial input data register on rising edges of DC. The falling edge of DCE latches the serial data into the appropriate register.

The serial data input format consists of five bits as shown in Figure 2.

Configuration/$\overline{\text{Volume}}$ bit (C/$\overline{\text{V}}$), loaded last, indicates the type of data contained in the data field D0-D3. When C/$\overline{\text{V}}$ is a "1", the data indicates the device configuration to be established. When C/$\overline{\text{V}}$ is a "0", the data indicates a volume level. The volume control which receives the data depends upon the current configuration of the audio interface.

FIGURE 2 — DATA FORMAT



When C/$\overline{\text{V}}$ is "1", D0-D3 are loaded into the configuration register. The four configuration register bits then address a ROM which has outputs to control the analog subsystem elements, enable the appropriate volume register, select the appropriate volume register for the speaker/ringer volume control, and provide the SAE output.

When C/$\overline{\text{V}}$ is "0", the data bits D1-D3 are loaded into the volume register which has been selected by the ROM. For volume changes, only D1-C/$\overline{\text{V}}$ need be transferred. However, if five bits are loaded into the serial input data register and C/$\overline{\text{V}}$ is low, D0 will be ignored.

If six or more data bits are clocked in while DCE is high, the last five bits clocked will be accepted when DCE goes low.

The digital input SCI is used by the analog subsystem as a sampling clock for signal processing and by the data input circuitry as a sequencing clock during data transfers.

The $\overline{\text{PDI}}$ input, when low, powers down the analog subsystem; however, all data is retained in the data registers and data may still be loaded into the serial input data register as usual as long as SCI is present. An internal pull-down resistor to V_{SS} is connected to $\overline{\text{PDI}}$ to insure the power-down state upon application to V_{DD} and V_{SS}.

The five digital inputs are DCE, DC, D, SCI and PDI. After one logic transition change, the input logic determines which of the three possible input voltage swings is used, and responds accordingly to future input levels.

There are two input logic circuits per input pin. The first operates from V_{DG} to V_{DD} with TTL levels referenced from V_{DG}. The second circuit uses V_{DG} as the positive supply and V_{SS} as the negative, sensing CMOS input levels from V_{SS} to V_{DG}. The internal logic looks at the output of these two circuits and determines the input logic levels used. This permits logic level swings of V_{SS} to V_{DG}, V_{DG} to V_{DD}, or V_{SS} to V_{DD}.

CONFIGURATION MODES

The audio interface configuration set provides a total of 16 possible configurations. A description of each of the modes follows.

LOOPBACK

This is a system test mode which loops received audio through the ringer/system volume control and out the TxO output amp.

The ring volume register controls the ringer/speaker volume control and new volume data enters the same register.

STANDBY

This mode accomplishes the same result as the $\overline{\text{PDI}}$ pin except for powering down the TxO amplifier. All other amplifiers are powered down and all transmission gates are turned off. Volume data is latched into the ring volume register.

STANDARD A

The standard A mode resembles that of the ordinary telephone. RxI audio is passed through the earpiece volume control and summed with a sidetone from the mouthpiece before being presented to the earpiece. Tx audio originates at the mouthpiece input, receives 20 dB of gain, and is then passed to the TxO output. New volume data is stored in the earpiece volume register. Transmit mute in this mode disable the path from the mouthpiece amplifier to the TxO amplifier.

RING

This is a receive only mode in which the receive audio is passed through the ringer/speaker volume control and output via the SO output. The ring volume register is selected to properly attenuate the ringing signal in the ringer/speaker volume control and any new volume data is written into the same register. Transmit mute has no effect in this mode and SAE goes high.

ON HOOK DIALING

This mode will allow a user to dial without taking the handset off hook. Audible feedback from the speaker could indicate dial tone, key depressions, etc. Receive audio passes through the ringer/speaker volume control and out the SO output. The transmit signal will originate at the auxiliary input which could be used for a DTMF dialer input. The speaker volume register is applied to the volume control and new volume data is latched into the same register. Mute will disable the transmit path from the auxiliary input. SAE will be high in this mode, enabling the speaker amplifier.

RECEIVER MONITOR A

This mode is similar to the standard A mode except the receive audio is also applied to the speaker output. Receive audio passes through both volume controls and out the EpO and SO pins. The speaker volume register controls the ringer/speaker volume control and new volume data is written into the speaker volume register. Transmit audio is taken from the mouthpiece input and output via the TxO amplifier. Transmit mute disables and mouthpiece amp to TxO amp path. SAE is high, enabling the speaker amplifier.

AUXILIARY

A suggested application for this mode would be for an optional conference phone circuit to be connected to the auxiliary input and output pins. Basically, a conference phone is a voice activated half-duplex controller which allows hands free conversation without audio feedback problems. Another useful application would be to connect a modem to the auxiliary input and output, thus eliminating the requirement for several components. In this mode the receive audio is passed through the ringer/speaker volume control and out the AxO pin. The SAE pin goes high, enabling the speaker amplifier. The transmit audio enters the audio interface via the auxiliary input amplifier and is connected directly to the TxO output amp. The speaker volume register controls the volume control and new volume data enters the same register. Transmit mute disables AxF from the input to the TxO output amp, disables AxO and enables the SO output.

STANDARD B

This mode is identical to the Standard A mode with one exception: the TxO signal originates at the auxiliary input instead of Mpl. This allows use of the Telset Audio Interface in applications that generate sidetone in a speech network. Mute disables the transmit path from the auxiliary input.

RECEIVE MONITOR B

This mode is identical to the Receive Monitor A mode with the same exception as the Standard B mode described above.

MODE AND VOLUME CONTROL

The data patterns required to program the audio interface mode or set the volume levels are summarized in Figures 3 and 4.

FIGURE 3 — MODE CONTROL SUMMARY

Mode	C/$\overline{V}$	D3	D2	D1	D0	Volume Register Selected	SAE State
Loopback	1	0	0	0	0	Ring	0
Standby	1	0	0	0	1	Ring	0
Standard A	1	0	0	1	0	Earpiece	0
Standard A/Mute	1	0	0	1	1	Earpiece	0
Ring	1	0	1	0	0	Ring	1
Ring/Mute	1	0	1	0	1	Ring	1
On-Hook Dialing	1	0	1	1	0	Speaker	1
On-Hook Dialing/Mute	1	0	1	1	1	Speaker	1
Receive Monitor A	1	1	0	0	0	Speaker	1
Receiver Monitor A/Mute	1	1	0	0	1	Speaker	1
Auxiliary	1	1	0	1	0	Speaker	1
Auxiliary/Mute	1	1	0	1	1	Speaker	1
Standard B	1	1	1	0	0	Earpiece	0
Standard B/Mute	1	1	1	0	1	Earpiece	0
Receive Monitor B	1	1	1	1	0	Speaker	1
Receive Monitor B/Mute	1	1	1	1	1	Speaker	1

FIGURE 4 — VOLUME CONTROL SUMMARY

Attenuation (dB)						
Earpiece	Speaker/ Ringer	C/$\overline{V}$	D3	D2	D1	D0
0	0	0	1	1	1	X
3	5	0	1	1	0	X
6	10	0	1	0	1	X
9	15	0	1	0	0	X
12	20	0	0	1	1	X
15	25	0	0	1	0	X
18	30	0	0	0	1	X
21	35	0	0	0	0	X

X = Don't Care

2

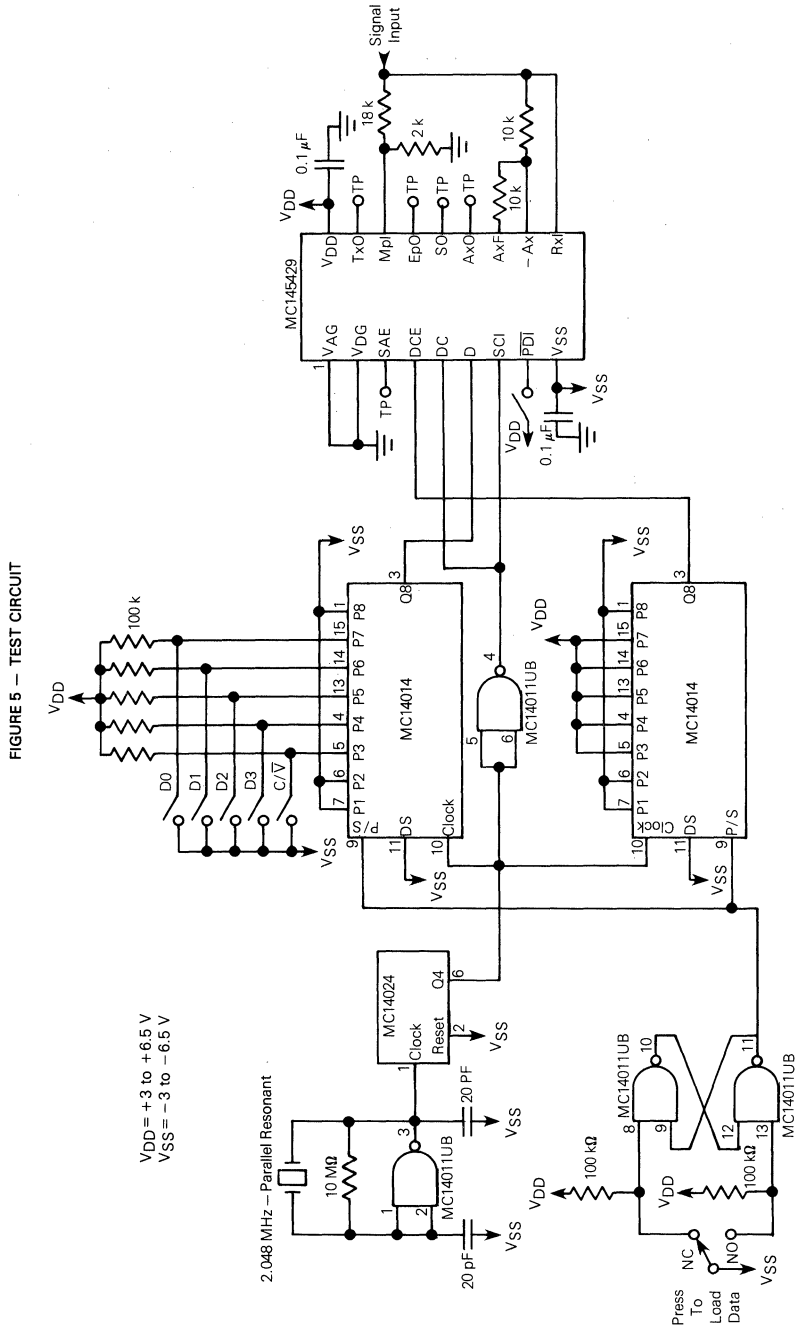


FIGURE 5 – TEST CIRCUIT

V_{DD} = +3 to +6.5 V
V_{SS} = –3 to –6.5 V

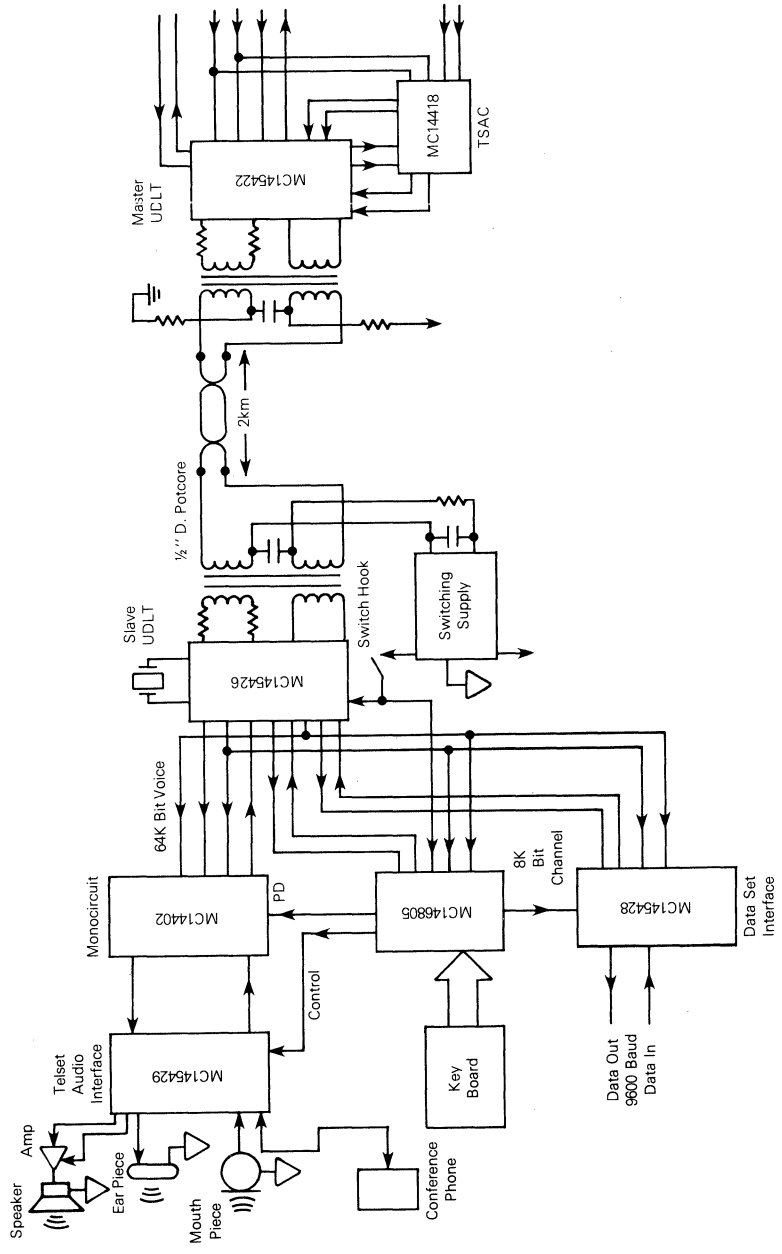


FIGURE 6 — DIGITAL WORK STATION

MC145432

Advance Information

2

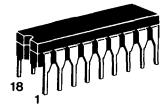
2600 Hz TONE SIGNALLING FILTER

This device contains a bypassable 6 pole 2600 Hz notch filter, a 2600 Hz band-pass filter and a 2600 Hz sinewave generator for SF signalling/detection applications.

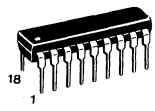
- ±5 V to ±8 V Single or Split Supply Operation
- Low Power Consumption, 80 mW @ 10 V
  200 mW @ 15 V
- On-Board Crystal Oscillator or External Clocks
- Notch Filter Gain Adjustable
- Uncommitted Op Amp Capable of Driving 600 Ω Loads
- TTL or CMOS Compatible Inputs
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

2600 Hz TONE SIGNALLING FILTER

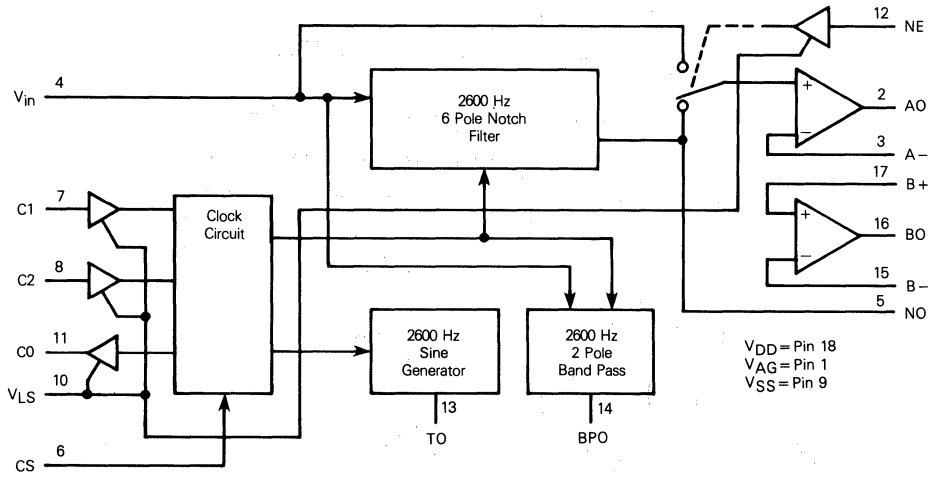


L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

BLOCK DIAGRAM

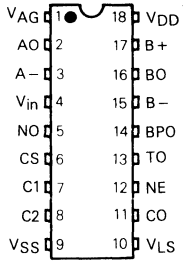


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	9.5	15	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	–	8.0	10	mA
(TTL Mode) @ 2.048 MHz			–	12	15	
Input Capacitance		Cin	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		–	V_{SS}	–	$V_{DD}-4$	V
V_{LS} (CMOS Mode)		V_{IH}	$V_{DD}-0.5$	–	V_{DD}	V
Clock Select (CS), $V_{AG}=(V_{DD}-V_{SS})/2$	State 1	V_{IH}	$V_{DD}-0.5$	–	V_{DD}	V
	State 2	V_{IM}	$V_{AG}-0.5$	–	$V_{AG}+0.5$	
	State 3	V_{IL}	V_{SS}	–	$V_{SS}+0.5$	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	$V_{LS}+2.0$	–	–	V
	"0" Level	V_{IL}	–	–	$V_{LS}+0.8$	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	–	–	V
I_O = 2.5 mA	"0" Level	V_{OL}	–	–	0.8	
CMOS LOGIC LEVELS ($V_{LS}=V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS, NE)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS, NE)	"1" Level	V_{IH}	7.5	5.6	–	V
	"0" Level	V_{IL}	–	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

2

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	±50	μA
DC Input Current (V_{in})		I_I	–	–	±10	μA
AC Input Impedance (1 kHz) (V_{in})		Z_{in}	0.2	0.1	–	MΩ
Input Voltage Range (V_{in})		V_{in}	V_{SS} + 1.5	–	V_{DD} – 1.5	V
Output Drive Current (TO, BPO, NO)	V_{OH} = V_{DD} – 1.2 V V_{OL} = V_{SS} + 1.2 V	I_{OH} I_{OL}	–0.4 +0.9	– –	– –	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, NE = V_{SS}, V_{LS} = V_{DD}, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO, BO)		V_{IO}	–50		+50	MV
Open Loop Gain (AO, BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45		dB
Input Bias Current (V_{in}, A–, B–, B+)		I_{IB}	–	±0.1	–	μA
Output Voltage Range (AO, BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1.0 1.1 1.8	 – – –	 9.0 8.9 8.2	V
Output Current (AO, BO)	V_{OH} = V_{DD} – 1.2 V VOL = V_{SS} + 1.2 V	I_{OH} I_{OL}	–5 +5	– –	– –	mA
Output Noise (AO, BO), 900 Ω		P_N	–	3	–	dBrnc
Slew Rate (AO, BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 70°C, NE = V_{DD})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7.0	Vpp
Gain (+2 dBm into 900 Ω @ 1 kHz)	–0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	25	dBrnC
Pass-Band Gain, Ref. 1 kHz Note Figure 1 300 Hz to 2 kHz 2 kHz to 2.2 kHz 2.2 kHz to 2.4 kHz 2.8 kHz to 3 kHz 3 kHz to 3.38 kHz 3.38 kHz to 4 kHz	 –0.25 –0.5 –5.0 –5.0 –0.5 –0.5	 +0.25 +0.5 +0.5 +0.5 +0.5 +0.5	dB
Rejection, Ref. 1 kHz 2.58 kHz to 2.59 kHz 2.59 kHz to 2.61 kHz 2.61 kHz to 2.62 kHz	 –45 –55 –45	 – – –	dB
Output Offset	–500	+500	mV

BY-PASS CHARACTERISTICS (V_{in} to AO, NE Low, V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Gain, 400 Hz to 4 kHz	−0.1	+0.1	dB
Noise, V_{in} = V_{AG}, 900 Ω	–	23	dBrnC
Output Offset	−50	+50	mV

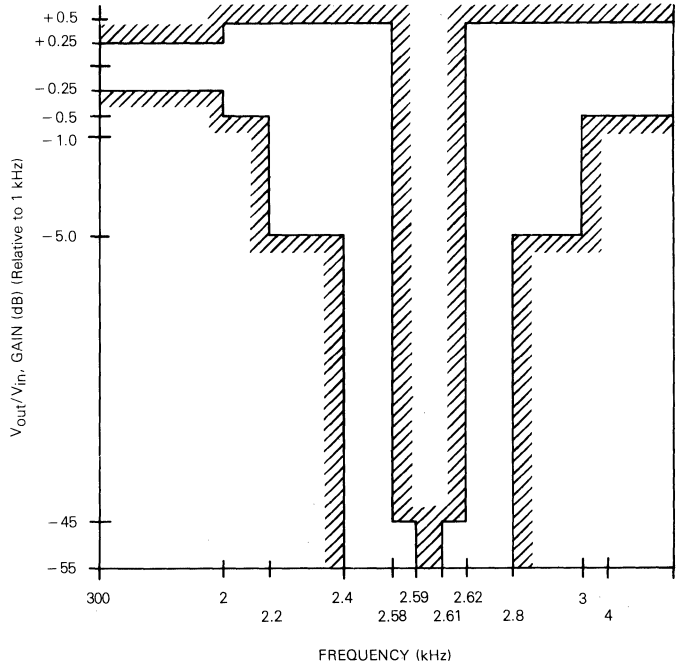
BAND-PASS CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency, f_o	2590	2610	Hz
Q	20	23	–
Gain (+2 dBm into 900 Ω @ 2.6 kHz)	−0.5	+0.5	dB
Idle Noise, V_{in} = V_{AG}, 900 Ω	–	45	dBrnC
Output Offset	−500	+500	mV

TONE OUT CHARACTERISTICS (V_{DD} = 10 V, V_{AG}/2, CS = V_{SS} = 0, T_A = 0 to 70°C)

Characteristics	Min	Max	Unit
Center Frequency	2598	2602	Hz
Output Level	0.40	0.725	Vp-p
Output Offset	−300	+300	mV

FIGURE 1 — NOTCH RESPONSE PARAMETER



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PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 18)
Most positive supply.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 9)
Most negative supply.

V_{AG}, ANALOG GROUND (PIN 1)
This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD}-V_{SS})/2$.

AO, OP-AMP OUT (PIN 2)
A−, OP-AMP IN (PIN 3)
These pins are for the output buffer amp which is capable of driving 600 Ω loads. A− is the inverting input of this amp while AO is its output. This amp buffers either the output of the notch filter or the input signal at V_{in} depending on the state of the NE pin.

V_{in}, INPUT (PIN 4)
This pin is the input to the notch filter, band-pass filter, and notch by-pass switch.

NO, NOTCH OUTPUT (PIN 5)
This pin is the output of the notch filter and can drive 20 kΩ loads.

NE, NOTCH ENABLE (PIN 12)
When high (see V_{LS} pin) the notch filter output is applied to the line buffer output amp. When held low (see V_{LS} pin) the input at V_{in} is applied to this op amp.

TO, TONE OUTPUT (PIN 13)
A 2600 Hz sine wave is output at this pin. This pin can drive a 20 kΩ load.

BPO, BAND-PASS OUT (PIN 14)
This pin is the output of the 2600 Hz band-pass filter and can drive a 20 kΩ load.

B+, OP-AMP NONINVERTING INPUT (PIN 17)
This pin is the noninverting input to the uncommitted op-amp provided on the circuit.

B−, OP-AMP INVERTING INPUT (PIN 15)
This pin is the inverting input of the uncommitted op-amp provided on the circuit.

BO, OP-AMP OUTPUT (PIN 16)
This pin is the inverting input of the uncommitted op-amp provided on the circuit.

CS, CLOCK SELECT (PIN 6)
C1, C2, CLOCK INPUTS (PINS 7 AND 8)
When held at V_{DD}, CS selects the internal crystal oscillator clock mode. A 3.579545 MHz crystal is connected between pins C1 and C2. A 10 MΩ resistor should be tied across C1 and C2 along with 20 pF capacitors to V_{SS} to insure stable oscillator operation. When tied to V_{SS}, a 2.048 MHz external clock should be applied to C2. When tied to V_{AG}, a 1.536 MHz external clock should be applied to C2. In both external clock modes, C1 should be tied to V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10)
This pin determines CMOS or TTL level compatibility for C1, C2, NE and CO. If tied to V_{DD}, CMOS device levels are expected; if tied to a voltage less than $V_{DD}-4$ V, TTL levels are expected with V_{LS} equal to logic ground.

CO, CLOCK OUTPUT (PIN 11)
A 128 kHz square wave is available at this pin. This is the sample clock of both the notch and band-pass filters.

FIGURE 2A — FREQUENCY SELECTION TABLE

Clock Select (CS)	Clock Source	Filter Switching Frequency f_s	Notch/Bandpass Center Frenquency f_c	Digital Clock Out (CO)
V_{DD}	Crystal (C1, C2)	Clock (Hz) / 28	Clock (Hz) / 1376	f_s
V_{AG}	External (C1 = V_{SS})	Clock (Hz) / 12	Clock (Hz) / 590	f_s
V_{SS}	External (C1 = V_{SS}	Clock (Hz) / 16	Clock (Hz) / 787.7	f_s

NOTE: Switching Frequency (f_s) Range = 10 kHz to 256 kHz

FIGURE 2B — FREQUENCY SELECTION TABLE

Clock Select (CS)	Clock Source	Filter Switching Frequency	Clock Out (CO)	Tone Out (TO)
V_{DD}	Crystal (C1, C2)	3.579 MHz	127.8 kHz	2601 Hz
V_{AG}	External (C1 = V_{SS})	1.536 MHz	128 KHz	2603.4 Hz
V_{SS}	External (C1 = V_{SS})	2.048 MHz	128 kHz	2599 Hz

FIGURE 3 — TEST CIRCUIT

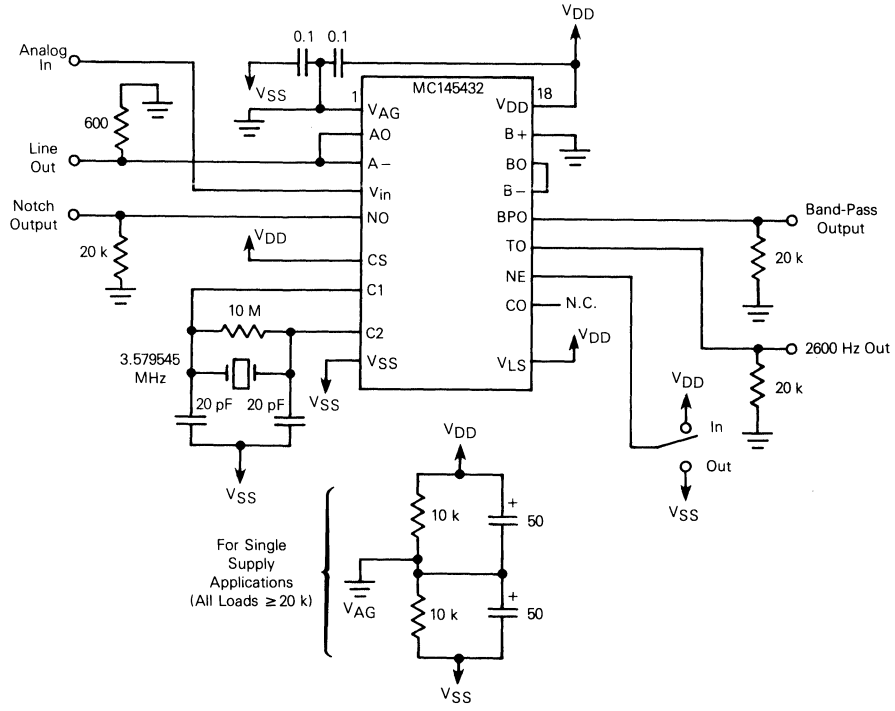
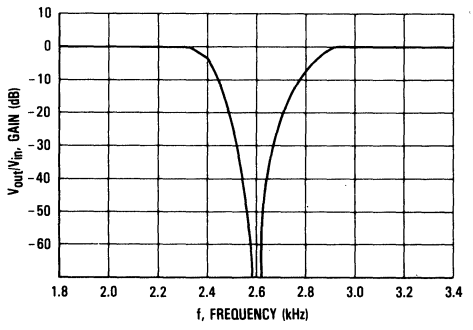
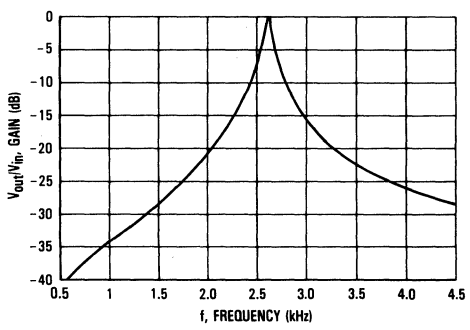


FIGURE 4—TYPICAL RESPONSE CURVES

NOTCH FREQUENCY RESPONSE



BAND-PASS FREQUENCY RESPONSE



MC145433

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Advance Information

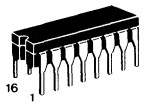
CMOS
(LOW-POWER COMPLEMENTARY MOS)

TUNEABLE NOTCH/
BAND-PASS FILTER

TUNABLE NOTCH/BAND-PASS FILTERS

This device contains a 6-pole filter and 4-pole band-pass filter which are frequency programable.

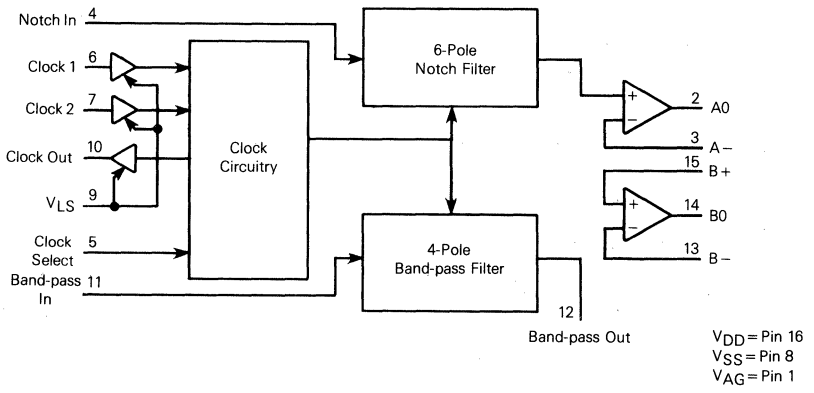
- ±5 to ±8 V Supply Operation
- Low Power Consumption, 150 mW Typical
- Tuneable Notch and Band-pass Filters
- On-board Crystal Oscillator or External Clocks
- Clock Output Pin
- An Uncommitted Op-Amp Is Provided, Capable of Driving 600 Ω Loads
- Notch Filter Output Gain Adjustable
- TTL or CMOS Compatible Inputs
- 16-Pin Package



L SUFFIX
CERAMIC PACKAGE
CASE 620

NOT RECOMMENDED
FOR NEW DESIGN

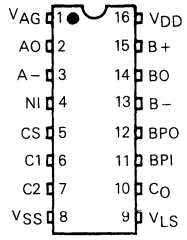
BLOCK DIAGRAM



MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain Per Pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	9.5	15	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 10 V, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current (CMOS Mode) @ 2.048 MHz		I_{DD}	–	10	18	mA
(TTL Mode) @ 2.048 MHz			–	15	22	
Input Capacitance		Cin	–	5.0	7.5	pF
MODE CONTROL LOGIC LEVELS						
V_{LS} (TTL Mode)		–	V_{SS}	–	V_{DD} − 4	V
V_{LS} (CMOS Mode)		V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
Clock Select (CS), $V_{AG} = (V_{DD} - V_{SS})/2$	State 1	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2	V_{IM}	V_{AG} − 0.5	–	V_{AG} + 0.5	
	State 3	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
TTL LOGIC LEVELS (V_{LS} = 0 V, V_{SS} = 0 V)						
Input Current (C1, C2, CS)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS)	"1" Level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" Level	V_{IL}	–	–	V_{LS} + 0.8	
Output Voltage (CO) I_O = 8 mA	"1" Level	V_{OH}	2.4	–	–	V
I_O = 2.5 mA	"0" Level	V_{OL}	–	–	0.8	
CMOS LOGIC LEVELS ($V_{LS} = V_{DD}$, V_{SS} = 0 V)						
Input Current (C1, C2, CS)	"1" Level	I_{IH}	–	–	±0.3	μA
	"0" Level	I_{IL}	–	–	±0.3	
Input Voltage (C1, C2, CS)	"1" Level	V_{IH}	7.5	5.6	–	V
	"0" Level	V_{IL}	–	4.4	3.0	
Output Current (CO)	V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

2

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})		I_I	–	–	±75	μA
DC Input Current (NI and BPI)		I_I	–	–	±10	μA
AC Input Impedance (1 kHz) (NI and BPI)		Z_{in}	0.2	0.1	–	MΩ
Input Voltage Range (NI and BPI)		V_{in}	V_{SS} + 1.5	–	V_{DD} – 1.5	V
Output Drive Current (BPO)	V_{OH} = V_{DD} – 1.2 V V_{OL} = V_{SS} + 1.2 V	I_{OH} I_{OL}	–0.4 +0.9	– –	– –	mA

OP AMP PERFORMANCE (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, V_{LS} = V_{DD}, T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage (BO)		V_{IO}	–50	–	+50	MV
Open Loop Gain (BO)	Z_L = 600 Ω + 200 pF to V_{AG}	A_{OL}	–	45	–	dB
Input Bias Current (A–, B–, B+)		I_{IB}	–	±0.1	–	μA
Output Voltage Range (BO) (R_L = 20 kΩ to V_{AG}) (R_L = 900 Ω to V_{AG}) (R_L = 600 Ω to V_{AG})		V_O	 1.0 1.1 1.8	 – – –	 9.0 8.9 8.2	V
Output Current (BO)	V_{OH} = V_{DD} – 1.2 V VOL = V_{SS} + 1.2 V	I_{OH} I_{OL}	–5 +5	– –	– –	mA
Output Noise (BO), 900 Ω		P_N	–	–3	–	dBrnC
Slew Rate (BO)		S_R	–	2	–	V/μs

NOTCH FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, CS = V_{SS} = 0 V, T_A = 0 to 85°C, BPI = V_{AG})

Characteristics	Min	Max	Unit
Input Overload Voltage	–	7.0	Vpp
Gain (+2 dBm into 900 Ω @ 1 kHz)	–1.0	+1.0	dB
Idle Noise, NI = V_{AG}, R_L = 900 Ω	–	28	dBrnC
Pass-Band Gain, Ref. 1 kHz (Note Figure 1) 300 Hz to 2.2 kHz 2.2 kHz to 2.4 kHz 2.8 kHz to 3 kHz 3 kHz to 4 kHz	 –1.0 –7.0 –7.0 –1.0	 +1.0 +1.0 +1.0 +1.0	dB
Rejection, Ref. 1 kHz 2.58 kHz to 2.62 kHz	 –45	 –	dB
Output Offset	–750	+750	mV
Dynamic Range (VFS/Idle Noise)	–70	–	dB

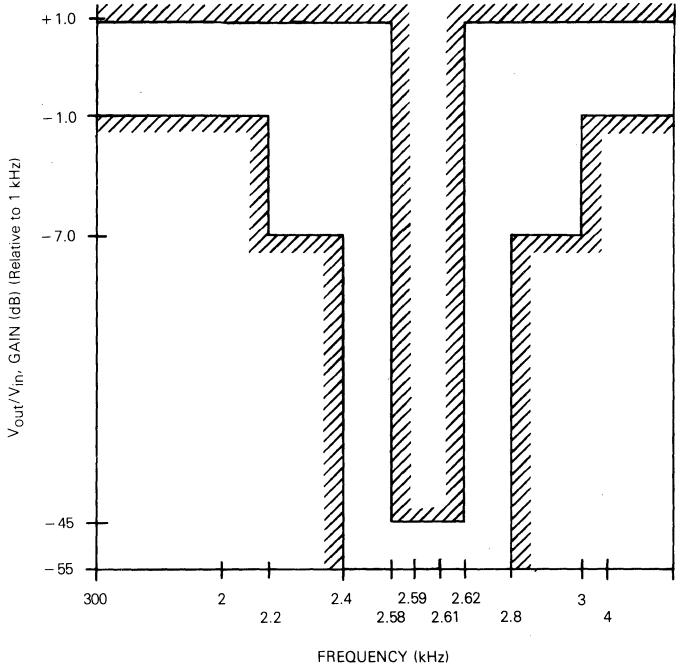
BAND—PASS FILTER ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, NI = V_{AG}, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 85°C)

Characteristic*	Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dbm0)	V_{FS}	7	–	–	V_{PP}
Gain (+2 dBm into 900 Ω @ 2.6 kHz	A_r	−1	0.0	+1	dB
Idle Noise, BPI = V_{AG}, R_L = 900 Ω	P_N	–	–	35	dBrnC
Dynamic Range (V_{FS}/Idle Noise)	DR	63	–	–	dB
Total Harmonic Distortion (0 dbm into 900 Ω)	THD	–	–	1.0	%
Output offset		−500	–	+500	mV
Q (−3db bandwidth/center frequency)	Q	28	–	38	–

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 10 V, V_{SS} = 0, V_{AG} = V_{DD}/2 T_A = 0 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, C2	t_r, t_f	–	–	1.5	μs
Input Pulse Width (TTL Mode)	C1, C2	t_W	200	–	–	ns
Clock Frequency (TTL Mode)	C1, C2	f_C	–	–	2.048	MHz
Clock Frequency (CMOS Mode)	C1, C2	f_C	–	–	6	MHz
Crystal Frequency	C1, C2	f_X	1	–	6	MHz
Input Pulse Width (CMOS Mode)	C1, C2	t_W	125	–	–	ns
Switching Frequency (Internal)		f_S	10	–	256	kHz

FIGURE 1 — NOTCH RESPONSE PARAMETER



2

PIN DESCRIPTIONS

V_{DD} (PIN 16)
Most positive supply, nominally +12 V to +15 V.

V_{SS} (PIN 8)
Most negative supply, nominally 0 V.

V_{AG} (PIN 1)
Analog ground. This pin is a high impedance input which serves as analog ground reference. This pin is nominally held at $(V_{DD} - V_{SS})/2$.

CS, CLOCK SELECT (PIN 5)
This pin controls the configuration of the digital section of the circuit. Three different clock divide configurations can be obtained by tying this pin to either V_{DD}, V_{AG} or V_{SS}.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 9)
This determines the logic levels expected at the digital input C1 and C2. If tied to V_{DD}, CMOS logic levels are expected; if tied to a voltage less than $V_{DD} - 4$ V, TTL levels are expected with V_{LS} equal to logic ground. This pin also controls the output swing at pin C0 in a similar manner, i.e., TTL or CMOS levels.

CO, CLOCK OUT (PIN 10)
This pin is the digital clock output pin. It is equal to the switching frequency, f_S of the notch and band-pass filters.

C1, C2, CLOCK 1, CLOCK 2 (PINS 6 AND 7)
When CS is tied to V_{DD}, a 1 to 4 MHz crystal is tied to C1 and C2. The switching frequency, f_S, of both filters is determined by the crystal frequency and is given by:

$$\frac{\text{f crystal}}{28} = f_S$$

With CS tied to V_{AG}, an external clock frequency must be applied into C1 and C2 tied together. The switching frequency f_S for the notch and band-pass filters are equal to the external clock frequency divided by 16. When CS is tied to V_{SS}, operation is identical to that when tied to V_{AG}, except that the clock is divided by 1 instead of 16.

NI, NOTCH INPUT (PIN 4)
This pin is the analog input to the notch filter.

AO, OP-AMP OUT (PIN 2), A−, OP-AMP INOUT (PIN 3)
These pins are for the output buffer amp of the notch filter. A− is the inverting input of this amp while AO is its output. This op-amp is capable of driving a 600 ohm load.

B+, OP-AMP NONINVERTING INPUT (PIN 15)
This pin is the non inverting input to the uncommitted op-amp provided on chip.

B−, OP-AMP INVERTING INPUT (PIN 13)
This pin is the inverting input to the uncommitted op-amp.

BO, OP-AMP OUTPUT (PIN 14)
This pin is the output of this uncommitted op-amp. This op-amp is capable of driving a 600 ohm load.

BPI, BAND-PASS IN (PIN 11)
This is the input to the band-pass filter.

BPO, BAND-PASS OUT (PIN 12)
This is the output of the band-pass filter.

FUNCTIONAL TRUTH TABLE

Clock Select CS	Clock	Filter Switching Frequency f_S	Notch/Bandpass Center Frequency f_C	Digital Clock Out CO
V_{DD}	Crystal	$\frac{\text{Clock (Hz)}}{28}$	$\frac{\text{Clock (Hz)}}{137.844}$	f_S
V_{AG}	External	$\frac{\text{Clock (Hz)}}{16}$	$\frac{\text{Clock (Hz)}}{787.69}$	f_S of Notch
V_{SS}	External	Clock (Hz)	$\frac{\text{Clock (Hz)}}{49.23}$	f_S of Notch

NOTE: Switching Frequency (f_S) Range = 10 kHz to 256 kHz

FIGURE 1 — TEST CIRCUIT

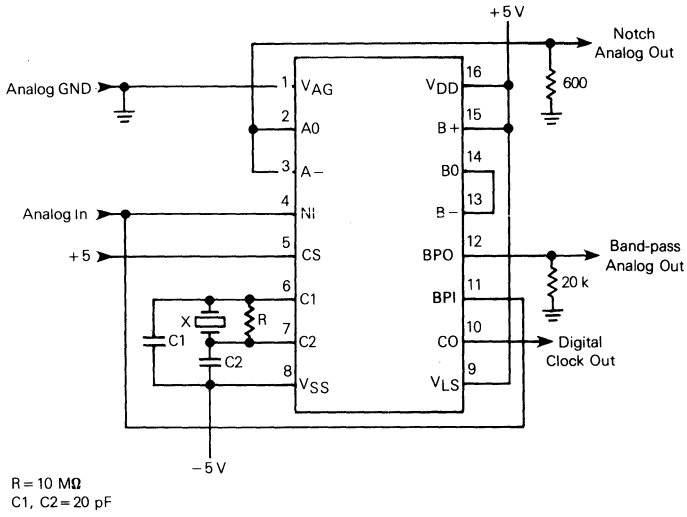


FIGURE 2 — TYPICAL NOTCH FILTER RESPONSE CURVES

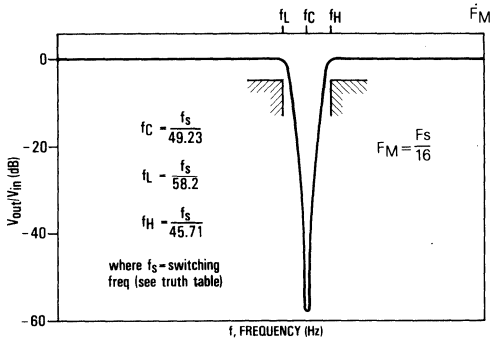
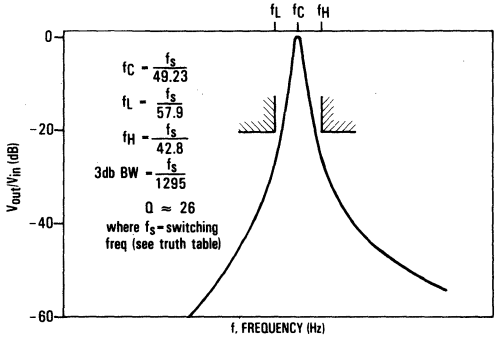


FIGURE 3 — TYPICAL BAND-PASS FILTER RESPONSE CURVES

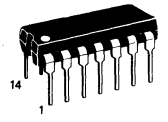


MC145436

2

Advance Information

Dual Tone Multiple Frequency Receiver

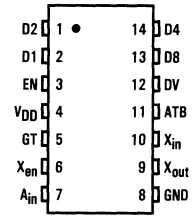


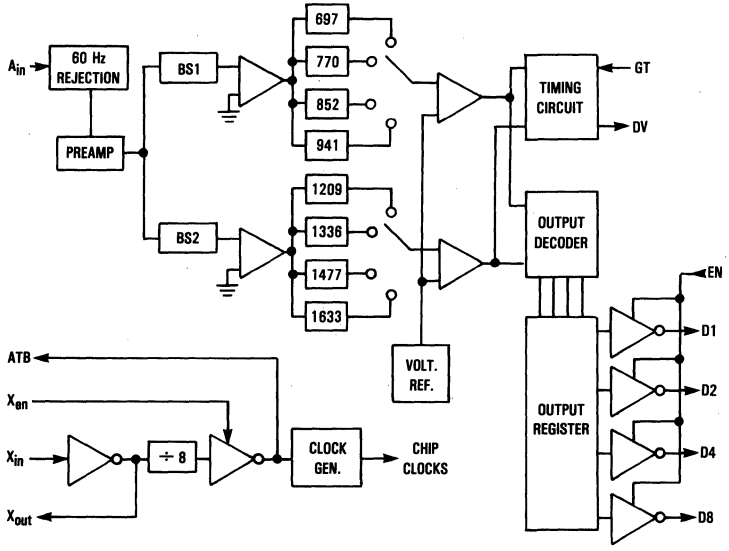
P SUFFIX
PLASTIC
CASE 646

The MC145436 is a silicon-gate CMOS LSI device containing the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436 provides excellent power-line noise and dial tone rejection, and is suitable for applications in central office equipment, PABX, keyphone systems, remote control equipment, and consumer telephony products.

- Single +5 V Power Supply
- Detects All 16 Standard Digits
- Uses Inexpensive 3.579545 MHz Colorburst Crystal
- Provides Guard Time Controls to Improve Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Built-In 60 Hz and Dial Tone Rejection
- Pin Compatible with SSI-204

PIN ASSIGNMENT





This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND Unless Otherwise Noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +6.0	V
Input Voltage, Any Pin Except A_{in}	V_{in}	−0.5 to V_{DD}+0.5	V
Input Voltage, A_{in}	V_{in}	V_{DD}−10 to V_{DD}+0.5	V
DC Current Drain per Pin	I	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

(All Polarities Referenced to V_{DD}=5.0 V ±10%, T_A= −40 to +85°C Unless Otherwise Noted)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{DD}	4.5	5	5.5	V
Supply Current (f_{CLK}=3.58 MHz)		I_{DD}	–	7	15	mA
Input Current	GT	I_{in}	–	–	200	μA
	EN, X_{in}, X_{en}		–	–	±1	
Input Voltage Low	EN, GT, X_{en}	V_{IL}	–	–	1.5	V
Input Voltage High	EN, GT, X_{en}	V_{IH}	3.5	–	–	V
High Level Output Current (V_{OH}=V_{DD}−0.5 V; Source)	Data, DV	I_{OH}	800	–	–	μA
Low Level Output Current (V_{OL}=0.4 V; Sink)	Data, DV	I_{OL}	1.0	–	–	mA
Input Impedance	A_{in}	R_{in}	90	100	–	kΩ
Fanout	ATB	FO	–	–	10	
Input Capacitance	X_{en}, EN	C_{in}	–	6	–	pF

ANALOG CHARACTERISTICS (V_{DD}=5.0 V ±10%, T_A= −40 to +85°C)

Parameter	Min	Typ	Max	Unit
Signal Level for Detection (A_{in})	−32	–	−2	dBm
Twist = High Tone/Low Tone	−10	–	10	dB
Frequency Detect Bandwidth (Notes 1 and 2)	±(1.5+2 Hz)	±2.5	±3.5	% f_C
60 Hz Tolerance	–	–	0.8	Vrms
Dial Tone Tolerance (Note 3) (Dial Tone 330+440)	–	–	0	dB
Noise Tolerance (Notes 3 and 4)	–	–	−12	dB
Power Supply Noise (Wide Band)	–	–	10	mV p-p
Talk Off (Mitel Tape #CM7290)	–	2	–	Hits

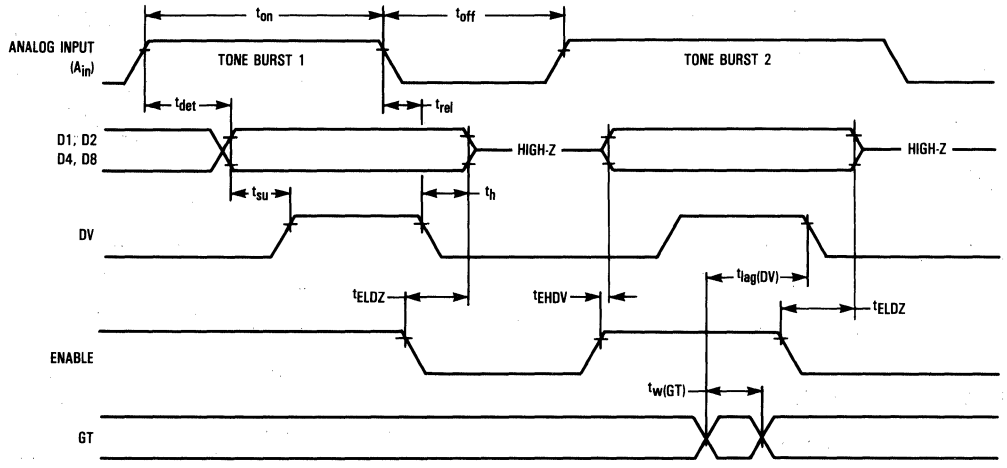
NOTES:
1. f_C is center frequency of bandpass filters.
2. Maximum frequency detect bandwidth of the 1477 Hz filter is +3.5% to −4%.
3. Referenced to lower amplitude tone.
4. Bandwidth limited (0 to 3.4 kHz) Gaussian noise.

2

AC CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = −40 to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Tone On Time	For Detection	$Tone_{on}$	40	–	–	ms
	For Rejection		–	–	20	
Pause Time	For Detection	$Tone_{off}$	40	–	–	ms
	For Rejection		–	–	20	
Detect Time	GT = 0	t_{det}	22	–	40	ms
	GT = 1		32	–	50	
Release Time	GT = 0	t_{rel}	28	–	40	ms
	GT = 1		18	–	30	
Data Setup Time		t_{su}	7	–	–	μs
Data Hold Time		t_h	4.2	4.6	5	ms
Pulse Width	GT	$t_{w(GT)}$	18	–	–	μs
DV Reset Lag Time		$t_{lag(DV)}$	–	–	5	ms
Enable High to Output Data Valid		t_{EHDV}	–	200	–	ns
Enable Low to Output High-Z		t_{ELDZ}	–	150	–	ns

TIMING



PIN DESCRIPTION

D1, D2, D4, D8—DATA OUTPUT

These digital outputs provide the hexadecimal codes corresponding to the detected digit (see Table 1). The digital outputs become valid after a tone pair has been detected, and are cleared when a valid pause is timed. These output pins are high impedance when Enable is at a logic 0.

EN—ENABLE

Outputs D1, D2, D4, D8 are enabled when EN is at a logic 1, and high impedance (disabled) when EN is at a logic 0.

GT—GUARD TIME

The Guard Time control input provides two sets of detected time and release time, both within the allowed ranges of tone on and tone off. A longer tone detect time rejects signals too short to be considered valid. With GT = 1, talk off performance is improved, since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be accepted. In addition, a shorter release time reduces the probability that a pause simulated by an interruption in speech will be detected as a valid pause. On the other hand, a shorter tone detect time with a long release time would be appropriate for an extremely noisy environment where fast acquisition time and immunity to drop-outs would be required. In general, the tone signal time generated by a telephone is 100 ms, nominal, followed by a pause of about 100 ms. A high-to-low, or low-to-high transition on the GT pin resets the internal logic, and the MC145436 is immediately ready to accept a new tone input.

X_{en}—OSCILLATOR ENABLE

A logic 1 on X_{en} enables the on-chip crystal oscillator. When using alternate time base from the ATB pin, X_{en} should be tied to GND.

A_{in}—ANALOG INPUT

This pin accepts the analog input, and is internally biased so that the input signal may be ac coupled. The input may be dc coupled so long as it does not exceed the positive supply. (See Figure 1.)

X_{in}/X_{out}—OSCILLATOR IN AND OSCILLATOR OUT

These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from X_{in} to X_{out}, as well as a 1 MΩ resistor in parallel with the crystal. When using the alternate clock source from ATB, X_{in} should be tied to V_{DD}.

ATB—ALTERNATE TIME BASE

This pin serves as a frequency reference when more than one MC145436 is used, so that only one crystal is required for multiple MC145436s. In this case, all ATB pins should be tied together as shown in Figure 2. When only one MC145436 is used, this pin should be left unconnected. The output frequency of ATB is 447.4 kHz.

DV—DATA VALID

DV signals a detection by going high after a valid tone pair is sensed and decoded at output pins D1, D2, D4, D8. DV remains high until a loss of the current DTMF signal occurs, or until a transition in GT occurs.

V_{DD}—POSITIVE POWER SUPPLY

The digital supply pin, which is connected to the positive side of the power supply.

GND—GROUND

Ground return pin is typically connected to the system ground.

Table 1. Hexadecimal Codes

Digit	Output Code			
	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

OPERATIONAL INFORMATION

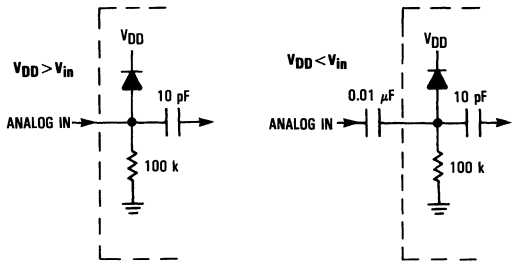


Figure 1. Analog Input

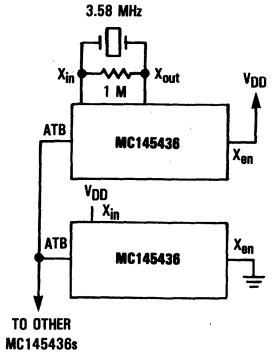


Figure 2. Multiple MC145436s

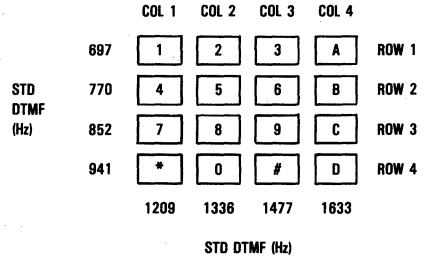


Figure 3. 4 x 4 Keyboard Matrix

MC145439
MC142103

2

Advance Information

Encoder/Decoder (Transcoder)

For Transmission Applications

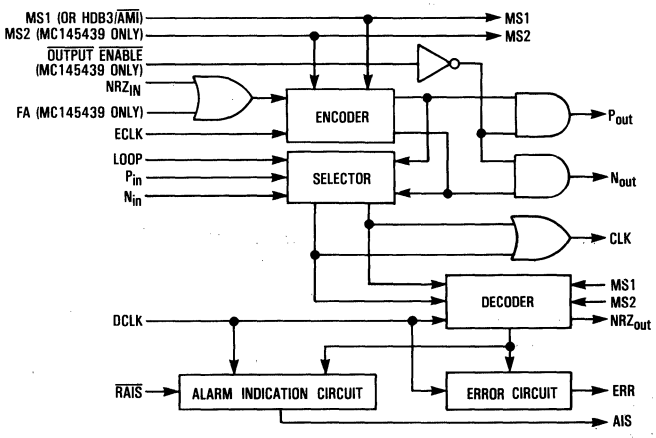
The MC145439 and MC142103 are high speed CMOS integrated circuits designed to perform the coding translation of clocked serial data into two streams of return to zero (RZ) digital pulses, which are externally mixed to form either AMI, HDB3, B6ZS, or B8ZS (MC142103—AMI or HDB3 only) ternary signals for driving transmission lines. They perform the reverse operation by translating two streams of clocked pulses [which have been derived from an incoming AMI, HDB3, B6ZS, or B8ZS (MC142103—AMI or HDB3 only) ternary encoded signal] into a single stream of clocked binary data. They also feature loopback and error monitoring functions. The coding and decoding functions perform independently at clock rates from zero (dc) to 9 megabits per second. The HDB3 coding and decoding are performed in a manner consistent with the CCITT G.703 recommendations.

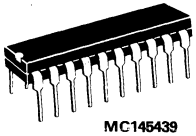
Both Devices:
- Low Power CMOS Operation
- Single 5 Volt Power Supply Operation
- Error Monitor Functions Provided
- Loopback Feature Provided
- Encode and Decode Clock Rates to 9 Megabits per Second
- Pin Selectable Modes of Operation
- TTL Compatible Inputs and Outputs

MC145439 Only:
- 20-Pin Package
- NRZ to AMI, HDB3, B6ZS, B8ZS; AMI, HDB3, B6Z6, B8ZS to NRZ
- Force Alarm and Output Enable Function
- Pin Compatible with HC-5560

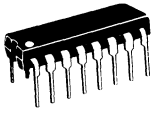
MC142103 Only:
- 16-Pin Package
- NRZ to AMI, HDB3; AMI, HDB3 to NRZ
- Pin Selectable HDB3 or AMI Operation
- Pin Compatible with CD22103 and MJ1471

BLOCK DIAGRAM



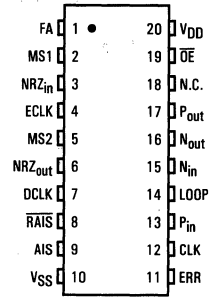


MC145439
PLASTIC
CASE 738

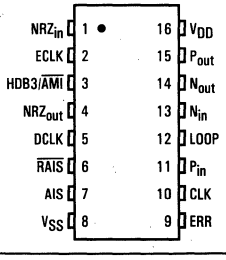


MC142103
PLASTIC
CASE 648

PIN ASSIGNMENTS
MC145439



MC142103



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	−0.5 to 6	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage	V_{DD} to V_{SS}	4.5	5.0	5.5	V
Power Dissipation @ 5.0 V					
Static	V_{DD} to V_{SS}	–	50	500	μA
Dynamic—ECLK = DCLK = 9 MHz	V_{DD} to V_{SS}	–	5	8.5	mA
Encoder Clock Frequency	ECLK	–	–	9	MHz
Decoder Clock Frequency	DCLK	–	–	9	MHz
Encoder Clock Duty Cycle	ECLK	40	50	60	%
Decoder Clock Duty Cycle	DCLK	40	50	60	%

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Max	Unit
High Level Input Voltage		V_{IH}	2.2	–	V
Low Level Input Voltage		V_{IL}	–	0.8	V
Input Current		I_{in}	–	±1.0	μA
Input Capacitance		C_{in}	–	10	pF
High Level Output Voltage (NRZ_{out}, AIS, ERR, CLK)	I_{out} = −0.36 mA I_{out} = −1.7 mA	V_{OH}	4.6 2.5	– –	V
High Level Output Voltage (P_{out}, N_{out})	I_{out} = −0.7 mA I_{out} = −3.4 mA	V_{OH}	4.6 2.5	– –	V
Low Level Output Voltage (NRZ_{out}, AIS, ERR, CLK)	I_{out} = 0.36 mA I_{out} = 0.8 mA	V_{OL}	– –	0.4 0.8	V
Low Level Output Voltage (P_{out}, N_{out})	I_{out} = 1.7 mA I_{out} = 3.5 mA	V_{OL}	– –	0.4 0.8	V

SWITCHING CHARACTERISTICS (V_{DD} = 4.75 V, T_A = 0 to 70°C, C_L = 50 pF)

Characteristic	Figure	Symbol	Min	Max	Unit
ECLK and DCLK Rise and Fall Times	A	t_r, t_f			ns
@ 1.544 MHz			–	60	
@ 2.048 MHz			–	40	
@ 6.312 MHz			–	30	
@ 8.488 MHz			–	10	
Minimum ECLK and DCLK Pulse Width Low or High		t_{wL}, t_{wH}	47	–	ns
ECLK to P_{out} or N_{out} Propagation Delay	B	t_{PLH}, t_{PHL}	–	60	ns
DCLK to NRZ_{out} Propagation Delay	B	t_{PLH}, t_{PHL}	–	40	ns
P_{in} or N_{in} to CLK Propagation Delay	B	t_{PLH}, t_{PHL}	–	50	ns
DCLK to ERR Propagation Delay	B	t_{PLH}, t_{PHL}	–	50	ns
$\overline{RAIS}$ to AIS Propagation Delay	B	t_{PLH}, t_{PHL}	–	60	ns
NRZ_{in} Setup Time to the Falling Edge of ECLK	C	t_{su}	20	–	ns
NRZ_{in} Hold Time After the Falling Edge of ECLK	C	t_h	0	–	ns
P_{in} or N_{in} Setup Time to Rising Edge of DCLK	D	t_{su}	20	–	ns
P_{in} or N_{in} Hold Time After the Rising Edge of DCLK	D	t_h	0	–	ns
Minimum $\overline{RAIS}$ Low Setup Time to DCLK Rising Edge to Include the Current Decoded Bit in the AIS Count	E	t_{su}	20	–	ns
Minimum $\overline{RAIS}$ High Setup Time to DCLK Rising Edge to Ensure the Next Bit on NRZ_{out} will be Included in the AIS Count	E	t_{su}	–	10	ns

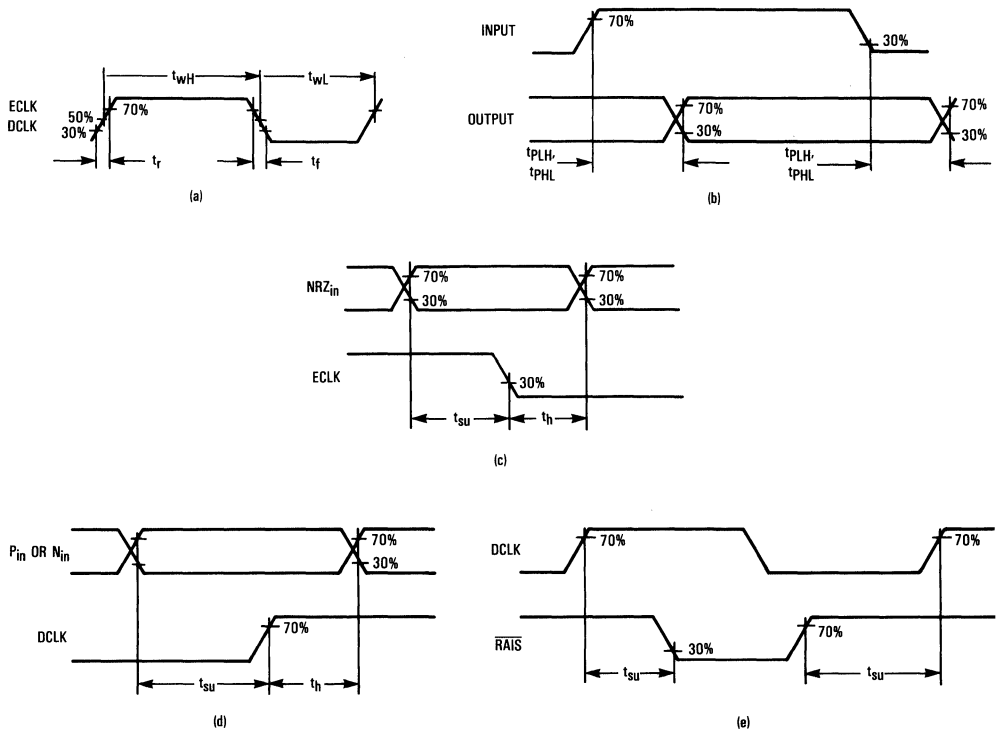


Figure 1. AC Timing Diagrams

PIN DESCRIPTIONS

V_{DD}—POSITIVE SUPPLY

This is the most positive power supply input. Normally +5 volts with respect to V_{SS}.

V_{SS}—NEGATIVE SUPPLY

This pin is the most negative power supply input and is logic ground. Normally 0 volts.

NRZ_{in}—NRZ DATA IN

This input accepts binary inputs for encoding into ternary form according to the appropriate rules. Data is clocked in on the high to low transition of the encoder clock (ECLK).

P_{out}—POSITIVE DRIVE OUTPUT
N_{out}—NEGATIVE DRIVE OUTPUT

These two RZ outputs are clocked out of the encoder on the low to high transition of the encoder clock. The length (high time) of the drive pulses is set by the length of the high level of the encoder clock signal. These two outputs are to be externally mixed to form the ternary transmission line code.

ECLK—ENCODER CLOCK

A negative transition of this input is used to clock NRZ data into the encoder section of the device. The high level time of this clock signal also controls the output pulse width of the encoder output drive signals.

P_{in}—POSITIVE INPUT
N_{in}—NEGATIVE INPUT

These two inputs are RZ representations of the received ternary inputs which have been externally separated. These inputs are clocked into the decoder on the positive (low to high) edge of the decoder clock signal simultaneously.

NRZ_{out}—NRZ DATA OUTPUT

This is the decoded output of the ternary encoded data after being decoded from the positive and negative inputs to the decoder. Data is clocked out serially on the low to high transition of the decoder clock (DCLK) and remains valid for the entire DCLK period.

DCLK—DECODER CLOCK

This input is used to clock in the negative and positive inputs to the decoder on the low to high transition of this line. This

pin also serves as a synchronous clock output for decoded data. The decoded data is updated on each low to high transition of the decoder clock.

CLK—CLOCK OUT

This output is the logical OR of the two RZ inputs to the decoder (i.e., the logical OR of the positive and negative inputs).

MS1—MODE SELECT 1 (MC145439 ONLY)
MS2—MODE SELECT 2 (MC145439 ONLY)

These two inputs work together to select the operating mode of the transcoders encoder, decoder, and error criterion, etc., according to the following truth table.

MS1	MS2	Mode of Operation
0	0	AMI
0	1	B8ZS
1	0	B6ZS
1	1	HDB3

HDB3/$\overline{\text{AMI}}$—MODE SELECT (MC142103 ONLY)

This pin determines the operation mode of the MC142103. A logic one (high) selects HDB3 operation and a logic zero (low) selects AMI operation.

HDB3/$\overline{\text{AMI}}$	Mode of Operation
0	AMI
1	HDB3

AIS—ALARM INDICATION SIGNAL

This output is updated on the falling edge of the $\overline{\text{RAIS}}$ input and functions as delineated in the $\overline{\text{RAIS}}$ pin description.

$\overline{\text{RAIS}}$—RESET AIS

This input, when low, resets and holds a counter which counts the number of zeros decoded by the decoder. The counter is enabled while $\overline{\text{RAIS}}$ is high. The falling edge of the $\overline{\text{RAIS}}$ input sets the AIS output low if three or more zeros have been decoded in the preceding $\overline{\text{RAIS}} = 1$ period. The falling edge of the $\overline{\text{RAIS}}$ input also causes the AIS output to go high if less than three zeros have been decoded in the preceding two successive $\overline{\text{RAIS}}$ high periods.

ERR—ERROR

This output is flagged (the term "flagged" is defined to be: setting the error output pin high for one decoder clock cycle following the input of the error) for one decoder clock period following the reception of an error at the decoder input. The error output is updated on the rising edge of the decoder clock pin. In all modes if both inputs to the decoder are high at the rising edge of the decoder clock an error is flagged (on the next rising edge of the decode clock). In the AMI mode, an error is flagged if a bipolar violation is discovered. In the HDB3 mode, an error is flagged if a violation is detected of the same polarity as a previously detected violation (for example three marks in a row of the same polarity). An error is also flagged (in the HDB3 mode) if the polarity of the violation pulse is correct but not preceded by two zeros. In the B8ZS and B6ZS modes of operation, an error is flagged if a violation pulse is received which is not preceded by a zero.

LOOP—LOOP TEST

This input when high, disconnects the normal inputs to the decoder and internally ties the two encoder outputs (positive and negative drive outputs) to the decoder inputs. In this mode, an external decoder clock must be supplied. Also note that the clock out line is a function of whichever set of inputs are selected for the decoder.

$\overline{\text{OE}}$—OUTPUT $\overline{\text{ENABLE}}$ (MC145439 ONLY)

This input, when high forces both encoder outputs low. When the output enable input is low, normal operation proceeds.

FA—FORCE ALARM (MC145439 ONLY)

The force alarm input inhibits the normal input to the encoder by logically "ORing" a "one" in with the incoming NRZ data. This forces the coder to code the all ones alarm pattern. The encoder operates normally when this pin is low.

N.C.—NO CONNECT (MC145439 ONLY)

This pin is not connected to any internal circuitry and may be either high or low. The line is ignored by the MC145439 Transcoder.

BACKGROUND

The basic goal of the international Integrated Services Digital Network (ISDN) standards effort is to develop a 64 kbps customer data channel. Thus, in order to expand the capabilities of the emerging digital network, support future services, and be compatible with the ISDN movement throughout the international community, the U.S. network is evolving to a 64 kbps clear channel capability (64 CCC) from the present 56 kbps capability. Today the T1 network is constrained by the line code restriction of at least a 1/8 average mark density, and is further constrained by a restriction of not more than 15 consecutive spaces (zeros) on DS1 signals, which is imposed by the clock recovery circuits of some T1 repeaters. The clock recovery circuit of these repeaters will begin to lose timing accuracy in the presence of long strings of zeros or low marks density. These restrictions do not limit PCM voice signals, however, they are a constraint on the transmission of digital data. Due to these restrictions, existing T1 and T1C transmission systems do not provide 64 CCC. To provide this capability, a coding and decoding scheme which allows the transmission of any data pattern and still satisfy the line code restrictions will be required. This coding scheme has been specified in the U.S. and is known as B8ZS for T1 systems and B6ZS for T2 systems. The CCITT on the other hand has recommended a scheme known as HDB3. Each of these coding schemes are variants of the existing alternate mark inversion (AMI) scheme, and each has specific rules for the coding of strings of consecutive zeros. AMI is a three level line code, where binary ones are coded as pulses above or below the mid level, and zeros are coded as no signal (the mid level). In this coding scheme, each mark is coded as pulses of a polarity opposite to the polarity of the preceding pulse (mark). The HDB3, B8ZS, and B6ZS coding schemes have special rules

for the coding of strings of binary zeros with pulses that violate the rule of alternate mark inversion. These purposeful violations can be detected by the decoder and the true data (a string of zeros) substituted by the decoder. The B8ZS and B6ZS schemes substitute (for strings of eight or six zeros) one of two possible patterns to represent the string of zeros based on the polarity of the previous mark. (See Figures 2 and 3.) Note that there are bipolar violations in the 2nd and 5th bit positions in the B6ZS scheme and bipolar violations in the 4th and 7th bit positions in the B8ZS coding scheme. The HDB3 scheme selects one of four possible code patterns for a string of four zeros based on the polarity of the previous pulse and if an even or odd number of pulses have occurred since the previous code violation (see Figure 4). Coding of a binary signal into an HDB3 signal is done (per CCITT G703 annex) according to the following rules:

1) HDB3 signal is pseudo ternary; the three states are denoted B+, B−, and 0.
2) Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however special rules apply (see item 4 following).
3) Marks in the binary signal are coded alternately in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces.
4) Strings of four spaces in the binary signal are coded according to the following rules:
   a) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself.
   b) It is coded as a mark (i.e., not a violation) if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation. This rule ensures that successive violations are of alternate polarity so that no dc component is introduced. The second and third spaces of a string are always coded as spaces. The last space of a string of four zeros is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion.

CIRCUIT OPERATION

The MC145439 encoder/decoder performs AMI, HDB3, B6ZS, or B8ZS (MC142103 AMI or HDB3 only) coding and decoding functions with error detection. They are generally used in telephony transmission applications and are operated in the 0 to 9 megabits per second frequency range. Coding and decoding are performed in independent sections. The encoder accepts a serial NRZ unipolar input signal and a synchronous transmission clock and creates two binary RZ output signals (positive and negative output drives) which are externally mixed to generate the ternary bipolar signals for driving transmission lines. The decoder section accepts ternary bipolar signals which have been externally split to provide two binary RZ input signals (positive and negative inputs) which are clocked into the decoder by an externally supplied synchronous clock signal.

ENCODER SECTION

The encoder of the MC145439 and MC142103 operate on 4-bit serial strings of data while operating in the AMI and HDB3 modes of operation. When operating in the B8ZS or B6ZS modes (MC145439 only), the encoder operates on 8- or 6-bits of serial data respectively. In all cases binary data is serially clocked into the encoder on the high to low transition of the encoder clock. The outputs of the encoder (positive and negative drive) are delayed from the input data by four, six, or eight encoder clock pulses depending on the mode selection of the device. (See timing diagrams.) The duty cycle or high time of the encoders drive lines is equal to the high time of the encoder clock.

DECODER SECTION

The Decoder Section of the MC145439 and the MC142103 operates on serial strings of ternary data that have been split into two RZ inputs (positive and negative inputs). The decoder however, accepts these two inputs simultaneously on the positive transition of the decoder clock. The output of the decoder is delayed from the input by four, six, or eight decoder clocks and appears as binary NRZ data on the NRZ output pin on the positive transition of the decoder clock. The NRZ data is updated on each successive positive transition of the decoder clock.

ERROR DETECTION SECTION

The Error Detection circuitry of the MC145439 and MC142103 operates as follows, according to the mode selection of the device. In all cases, the error signal is flagged for one full decoder clock period following the input of the error. In all modes, when a high level appears simultaneously on both positive and negative inputs to the decoder, the error output is flagged for one period of the decoder clock. In this case, a positive input (logic one) is assumed as an input to the decoder. In the AMI mode, errors are flagged when a bipolar violation is received. In the HDB3 mode, the error output is flagged if a violation pulse is received of the same polarity as the last received violation pulse. For example, three or more received pulses of the same polarity. An error is also flagged if a bipolar violation is received without being preceded by two spaces. In the B8ZS and B6ZS modes of operation (MC145439 only), the error line is flagged if a violation is received and not preceded by a zero.

LOOP TEST

When in the Loop Test mode, the encoders positive and negative outputs are internally connected to the decoders positive and negative inputs. The normal inputs are ignored in this mode. In the Loop Test mode, the appropriate decoder clock must be supplied to the MC145439 or MC142103. The Clock Out line of the MC145439 and MC142103 are a logical OR of the decoder inputs and is generally used by external timing recovery circuits.

AIS SECTION

The AIS (Alarm Indication Signal) circuitry contains a counter that increments (to a maximum of three) each time a zero is decoded by the decoder. This counter is reset and held to zero by a low level on the $\overline{RAIS}$ input. A logic one on the $\overline{RAIS}$ input enables the decoder zero counter to increment on the positive edge of the decoder clock. The AIS output is set two zero (on the falling edge of $\overline{RAIS}$ input) provided three or more zeros have been decoded in the preceding $\overline{RAIS} = 1$ period. The AIS output is set high (on the falling edge of the $\overline{RAIS}$ input) if less than three zeros have been decoded in the preceding two $\overline{RAIS} = 1$ periods.

2

POLARITY OF PREVIOUS MARK	B6ZS CODING SCHEME CODE USED FOR SIX CONSECUTIVE ZEROS						
+	0	+	−	0	−	+	
−	0	−	+	0	+	−	

*2ND *5TH

*NOTE: + implies a positive pulse
0 implies no pulse
− implies a negative pulse

Figure 2. B6ZS Coding Scheme

POLARITY OF PREVIOUS MARK	B8ZS CODING SCHEME CODE USED FOR EIGHT CONSECUTIVE ZEROS							
+	0	0	0	+	−	0	−	+
−	0	0	0	−	+	0	+	−

*4TH *7TH

*NOTE: + implies a positive pulse
0 implies no pulse
− implies a negative pulse

Figure 3. B8ZS Coding Scheme

POLARITY OF PREVIOUS MARK	ODD NUMBER OF PULSES SINCE VIOLATION					EVEN NUMBER OF PULSES SINCE VIOLATION			
+	0	0	0	+		−	0	0	−
−	0	0	0	−		+	0	0	+

VIOLATION *4TH VIOLATION *4TH

*NOTE: + implies a positive pulse
0 implies no pulse
− implies a negative pulse

Figure 4. HDB3 Coding Scheme

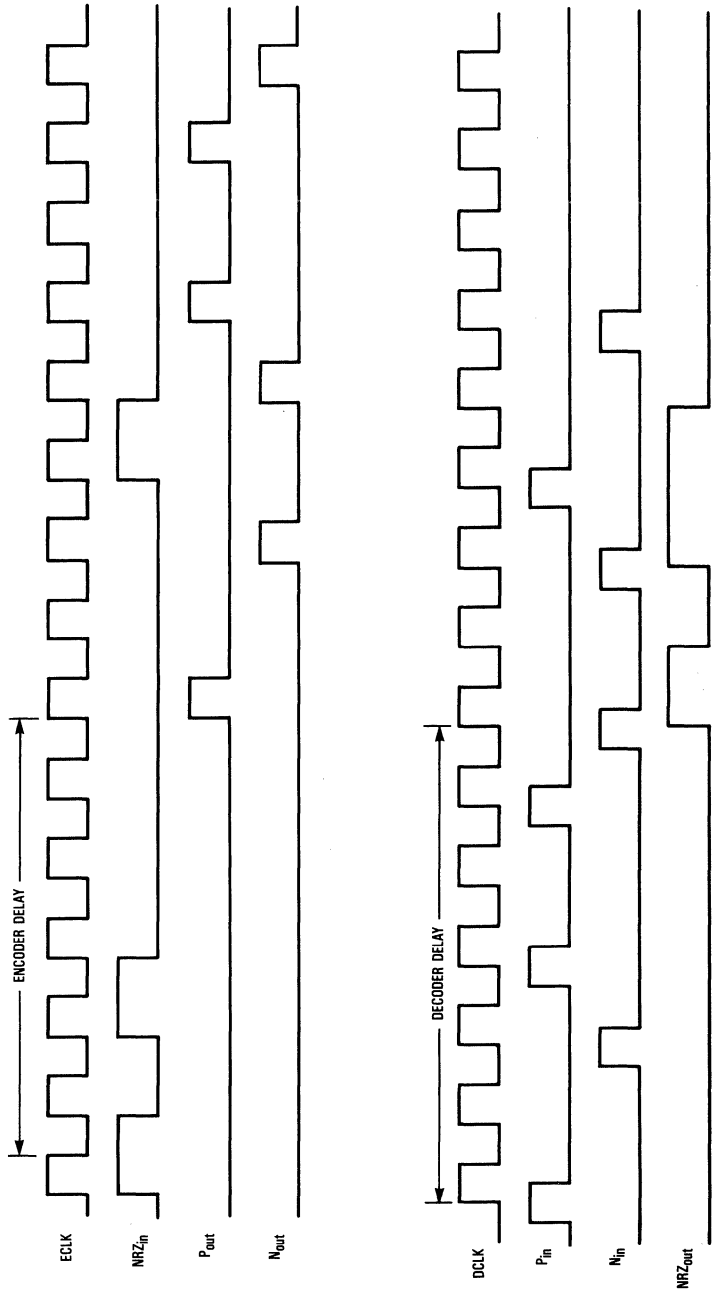


Figure 5. B6ZS Encode and Decode Timing

2

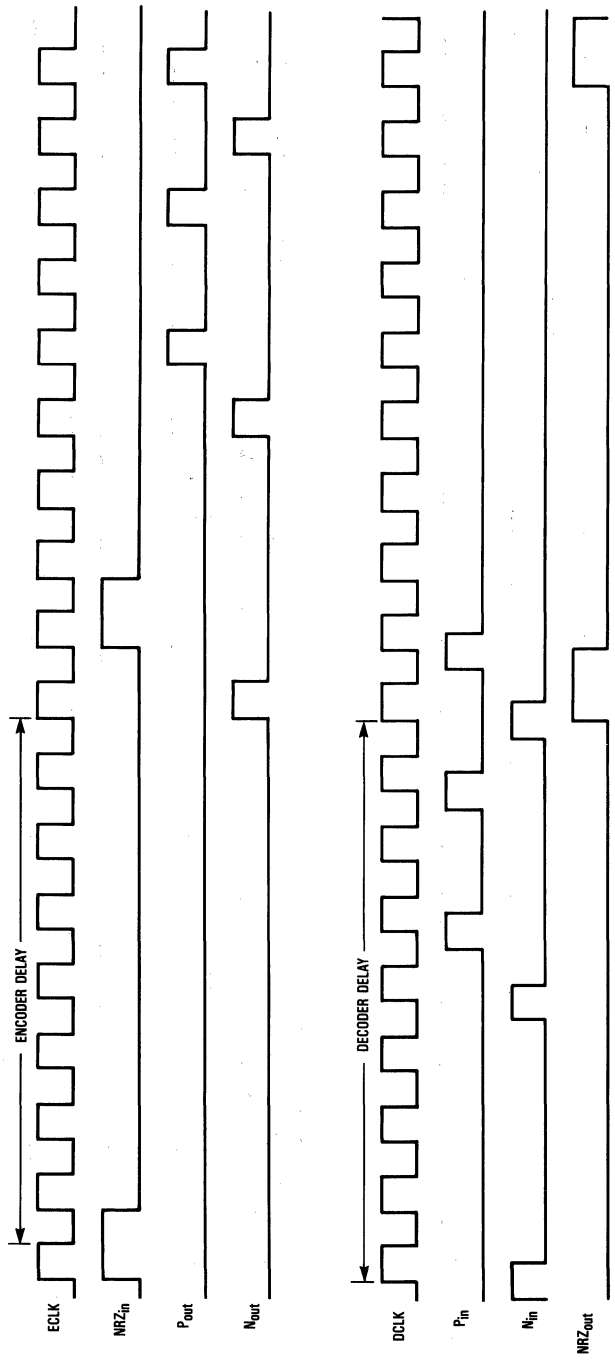


Figure 6. B8ZS Encode and Decode Timing

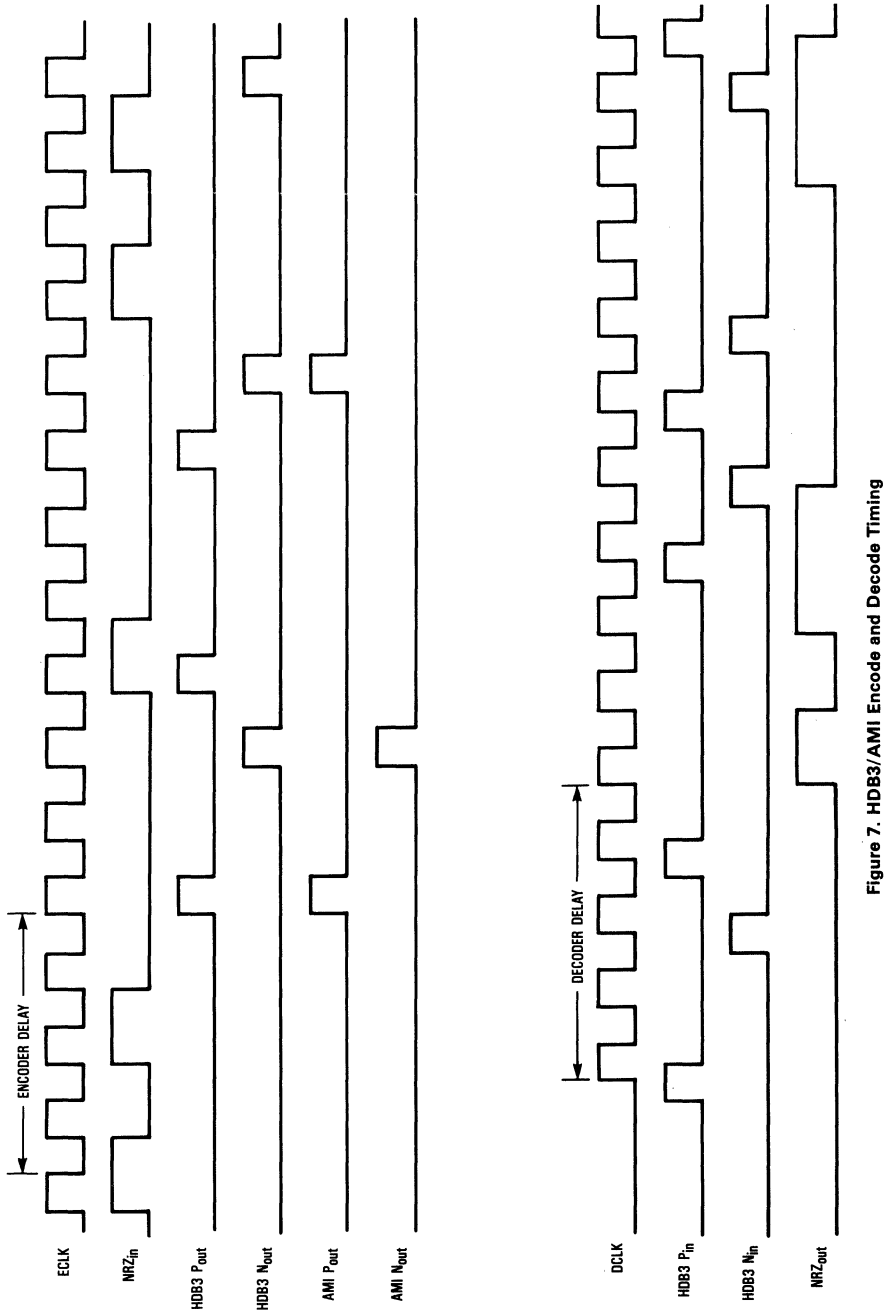


Figure 7. HDB3/AMI Encode and Decode Timing

2

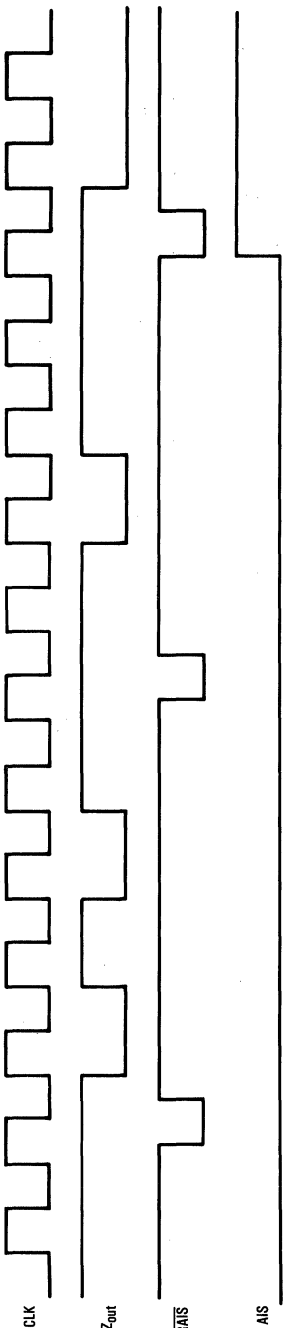


Figure 8. AIS Timing

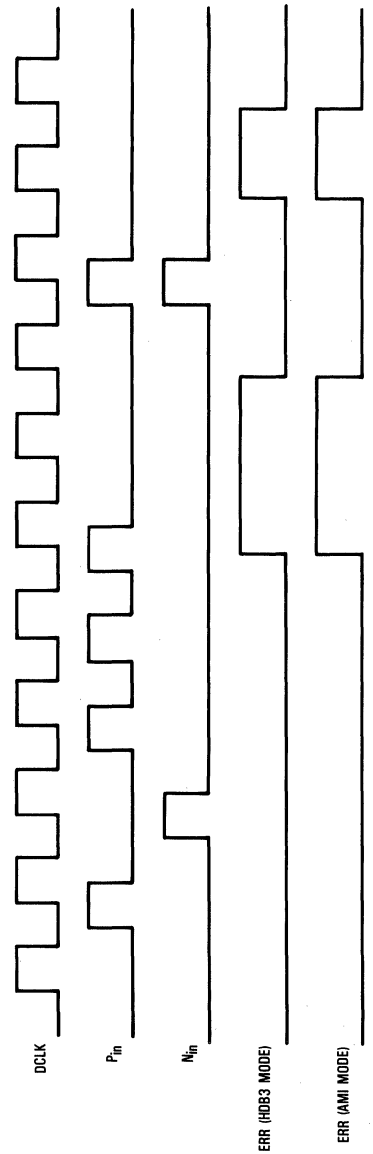


Figure 9. Error Timing

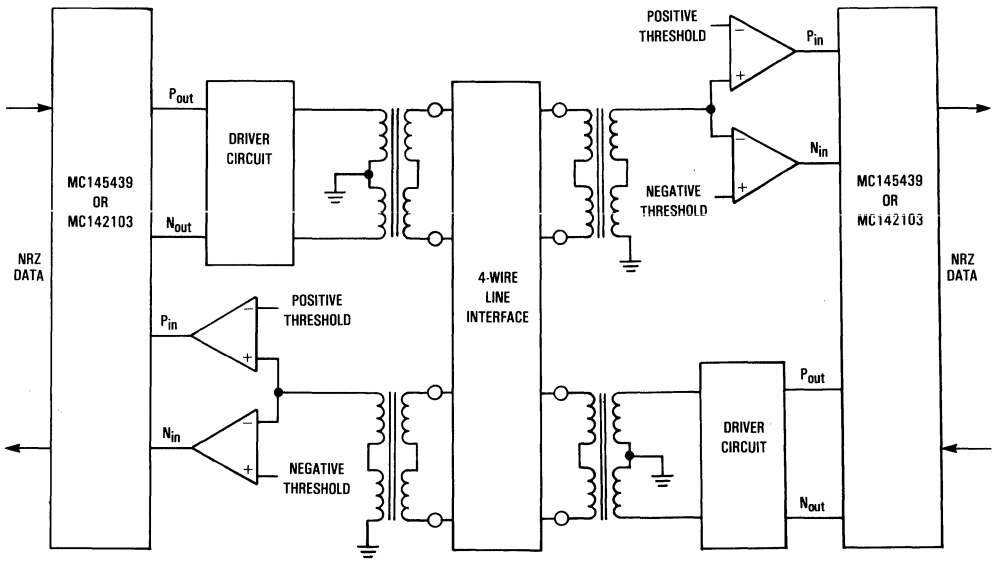


Figure 10. Typical Line Interface

MC145440

2

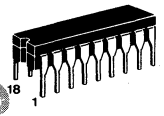
BELL 103 300 BAUD MODEM BAND-PASS FILTER

The MC145440 is a 300 baud modem filter designed to be used with the MC14412, MC145445, or MC6860 modems. These modem/filter combinations fulfill the major requirements of a complete Bell 103 300 baud modem system. The MC145441 is also available to fulfill the CCITT V.21 equivalent filtering function. Features of the MC145440 include:

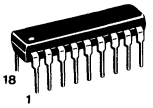
- Low Band Band-pass Filter
- High Band Band-pass Filter
- Bell 103 Frequency Compatible
- Spare Operational Amplifier
- Answer or Originate Mode
- Self Test Loopback Configuration
- Single or Split Power Supply Operation
- 18-Pin Package

CMOS
(LOW-POWER COMPLEMENTARY MOS)

300 BAUD MODEM BAND-PASS SWITCHED CAPACITOR FILTER



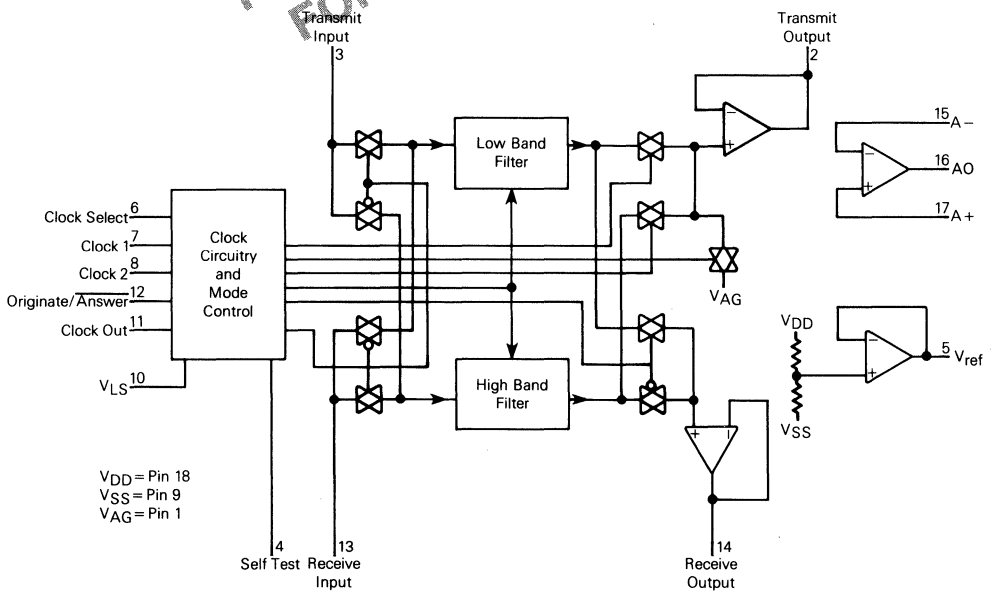
L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

NOT RECOMMENDED FOR NEW DESIGN

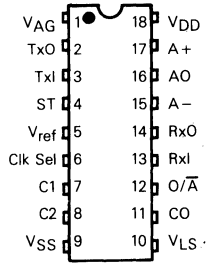
BLOCK DIAGRAM



MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, all pins	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	10	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 10 V, V_{SS} = 0 V, 1 MHz Crystal		I_{DD}	–	–	10	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
Mode Control Logic Levels						
V_{LS}	TTL Mode	–	V_{SS}	–	V_{DD} − 4.0	V
	CMOS Mode	V_{IH}	V_{DD} − 0.5	–	V_{DD}	
Clock Select (CS)	State 1, 4.0 MHz	V_{IH}	V_{DD} − 0.5	–	V_{DD}	V
	State 2, 3.684 MHz	V_{IM}	(V_{DD} − V_{SS})/2 − 0.5	–	(V_{DD} − V_{SS})/2 + 0.5	
	State 3, 1.0 MHz	V_{IL}	V_{SS}	–	V_{SS} + 0.5	
O/$\overline{A}$ TTL Logic Levels (V_{DD} = 5 V, V_{SS} = −5 V, V_{LS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" Level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level	V_{IH}	V_{LS} + 2.0	–	–	V
	"0" level	V_{IL}	–	–	V_{LS} + 0.8	
ST, C1, O/$\overline{A}$ CMOS Logic Levels (V_{LS} = V_{DD}, V_{SS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level, V_{DD} = 10 V	V_{IH}	7.5	5.75	–	V
	"0" level, V_{DD} = 10 V	V_{IL}	–	4.25	3.0	
CO Output Characteristics (V_{DD} = 10, V_{SS} = 0 V)						
TTL Output Voltage (TTL Mode)	"1" level, I_O = 8 mA	V_{OH}	2.4	–	–	V
	"0" level, I_O = 2.5 mA	V_{OL}	–	–	0.8	
CMOS Output Current	V_{DD} = 10 V, V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{DD} = 10 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})	I_I	−50	–	+50	μA
DC Input Current (TxI, RxI)	I_I	−10	–	+10	μA
AC Input Impedance (TxI, RxI)	Z_{in}	0.2	1.0	–	MΩ
Input Voltage Range (TxI, RxI)	V_{in}	V_{SS} + 1.5	–	V_{DD} − 1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 5 to 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO)	I_{IO}	−50	–	+50	mV
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	–	45	–	dB
Input Bias Current (A+, A−)	I_{IB}	–	±0.1	–	μA
Output Noise (900 Ω)	P_N	–	−3	–	dBrnC
Slew Rate	S_R	–	2	–	V/μs
Output Voltage Swing (R_L = 600 Ω to V_{AG})	–	1.5 V	–	V_{DD} − 1.5 V	V

2

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, O/A, ST	t_r, t_f	–	–	4	μs
Input Pulse Width	(TTL Mode) O/A	t_W	200	–	–	ns
	(CMOS Mode) C1, O/A, ST	t_W	125	–	–	
Clock Frequency (Driven by External Clock) (C1 Pin)	(CMOS)	f_c	–	1.0	4.0	MHz
Crystal Frequency	C1, C2	f_x	1.0	–	4.0	MHz

LOW-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 1170 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	20	26	dBrnC
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Pass-Band Ripple	1070 Hz to 1270 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 1070 Hz, 0 dBmO	1270 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 1170 Hz)	2025 Hz to 2225 Hz	–	−55	–	–	dB
Differential Group Delay	1070 Hz to 1270 Hz	–	–	–	600	μs

HIGH-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 2125 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	20	26	dBrnC
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Pass-Band Ripple	2025 Hz to 2225 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 2025 Hz, 0 dBmO	2225 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 2125 Hz)	1070 Hz to 1270 Hz	–	−55	–	–	dB
Differential Group Delay	2025 Hz to 2225 Hz	–	–	–	600	μs

V_{ref} CHARACTERISTICS (V_{DD} = 5 to 15 V, V_{ref} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
V_{ref} Output Voltage	I_O = ±5 mA	V_{ref}	−250	±75	+250	mV

PIN DESCRIPTIONS

V_{DD} (PIN 18) — Positive power supply.

V_{SS} (PIN 9) — Negative power supply.

V_{AG} (PIN 1) — Analog ground. In single supply applications, V_{AG} is driven from V_{ref}.

V_{ref} (PIN 5) — This pin provides an output DC voltage at approximately (V_{DD}-V_{SS})/2 for use as an external analog ground in single supply applications. In symmetric dual power supply applications, V_{ref} is not used.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10) — This pin determines the input/output logic level compatibility of O/$\overline{A}$ and CO. When the voltage on this pin is greater than $V_{DD}-0.5$ V and less than V_{DD}, these digital inputs and outputs are CMOS compatible. When the voltage on this pin is less than $V_{DD}-4$ V and greater than V_{SS}, these digital inputs and outputs are TTL compatible, and V_{LS} is connected to digital ground.

C1, C2, CLOCK 1, CLOCK 2 (PIN 7, PIN 8) — These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from C1 to C2 as well as a 10 MΩ resistor in parallel with the crystal and 20 pF capacitors from C1 and C2 to V_{SS}. Crystal frequencies of 1.0, 3.6864, or 4.0 MHz may be used. Alternatively, an external CMOS level signal at the crystal frequency may be applied to C1 in lieu of the crystal, capacitors, and resistor. The inverted clock signal will appear at C2 and will be a CMOS output from V_{SS} to V_{DD}.

Clk Sel, CLOCK SELECT (PIN 6) — This pin is a three-state selector used to select one of the three crystal/clock options. When at V_{DD}, V_{AG}, or V_{SS}, this pin selects the 4.0, 3.6864, or 1.0 MHz crystal/clock option, respectively, for C1 and C2.

Clock Select Pin 6	Clock Frequency *	Clock Output Pin 11
V_{DD}	4.0 MHz	1.0 MHz
V_{AG}	3.6864 MHz	N/A
V_{SS}	1.0 MHz	1.0 MHz

*Use either an external clock to drive C1 Pin 7 or external crystal across C1 and C2 Pins 7 and 8.

CO, CLOCK OUT (PIN 11) — This provides a 1.0 MHz output clock signal when either the 1.0 or 4.0 MHz clock is selected and is typically used to drive the clock input to a MC14412 or MC6860 modem. The clock output is not usable when the 3.6864 MHz option is used. The logic family compatibility (CMOS or TTL) of this output is determined by V_{LS}.

O/$\overline{A}$, ORIGINATE, ANSWER (PIN 12) — The mode of the device, originate or answer, is selected with this pin. In the originate mode, selected with a logic "1", the low band band-pass filter is switched into the transmit path and the high band band-pass filter is switched into the receive path. In the answer mode, the filters switch position. The input levels of this pin are determined by V_{LS}.

TxI, TRANSMIT INPUT (PIN 3) — TxI is the input to the transmit band-pass filter which is the low band filter in the originate mode and the high band filter in the answer mode. In the self test mode, this input is routed to the appropriate band-pass filter input so as to pass the modulated data to the demodulator.

TxO, TRANSMIT OUTPUT (PIN 2) — This pin is the output of the Tx output amplifier and typically drives the modulated data into the duplexer or hybrid circuit (see ST pin).

RxI, RECEIVE INPUT (PIN 13) — RxI is the input to the receive band-pass filter which is the high band filter in the originate mode and the low band filter in the answer mode. In the self test mode, this input is disabled.

RxO, RECEIVE OUTPUT (PIN 14) — The output of the receive band-pass filter, whether low band or high band, is provided at RxO. Typically, this signal is capacitively coupled to the input of the external carrier detector and limiter. The AC coupling capacitor is required because of the variable DC offset of the receive filter.

ST, SELF TEST (PIN 4) — A "1" on ST puts the device into a self test mode which routes the modulated carrier from TxI, through the appropriate filter,and out RxO back to the receive carrier input of the modem. TxO remains at V_{AG} during a self test operation. This pin is a standard CMOS input regardless of the state of V_{LS}.

A+ (PIN 17) — This is the noninverting input to the spare operational amplifier.

A− (PIN 15) — This is the inverting input to the spare operational amplifier.

AO (PIN 16) — This is the output of the spare operational amplifier.

2

FUNCTIONAL DESCRIPTION

This device is capable of four basic analog configurations determined by the state of O/$\overline{A}$ and ST. The normal (non-self test) and self test modes in both the answer and originate modes will be discussed.

In the normal originate mode, O/$\overline{A}$ is a "1" and self test, ST, is a "0". When in this mode, the Tx carrier from the modem is input on TxI and routed through the low band band-pass filter. The filter output is switched to the input of the Tx op-amp which typically drives the Tx carrier off chip into a duplexer circuit which could be implemented with the spare operational amplifier. The output of the duplexer drives RxI which is switched to the input of the high band band-pass filter. The filter output is available at RxO which is typically the input to a limiter and carrier detector.

The normal answer mode is established by a "0" on both O/$\overline{A}$ and ST. This mode is identical to the normal originate mode with one exception: the band-pass filters swap positions, i.e., the high band band-pass filter is switched into the transmit path, and the low band band-pass filter is switched into the receive path.

When used with the MC14412 in the self test mode, the device will function as follows. A "1" on the self test pin of both devices enables the self test mode. The modem switches its demodulator to its modulator frequency and demodulates its own modulated carrier. The modem filter switches the transmit carrier of the modem from TxI through the low band filter and out the RxO pin to the limiter when in the originate mode. When the system is in the answer mode, the modulated signal is instead routed through the high-band filter. TxO will remain at mid-supply (V_{AG}) during self test operations.

FIGURE 1 — TEST CIRCUIT

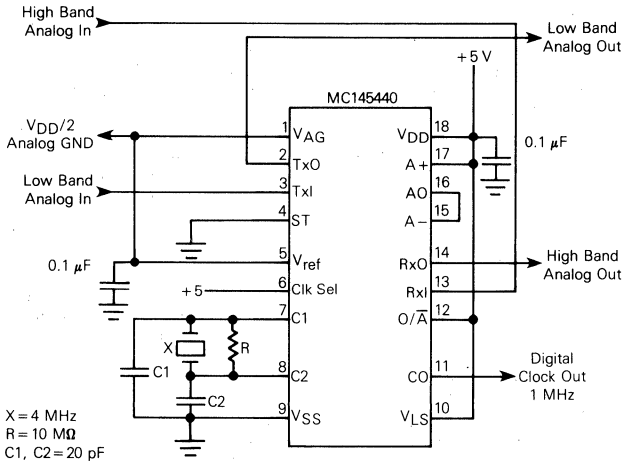


FIGURE 2 — MC145440 FREQUENCY RESPONSE

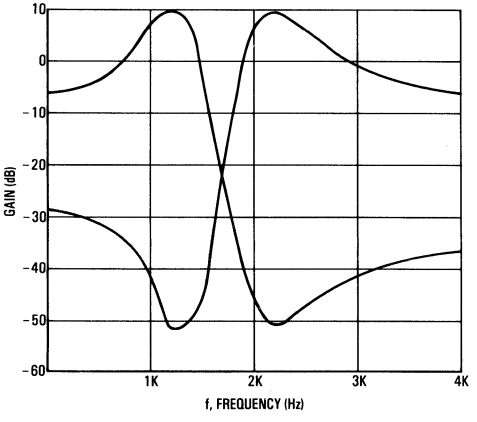
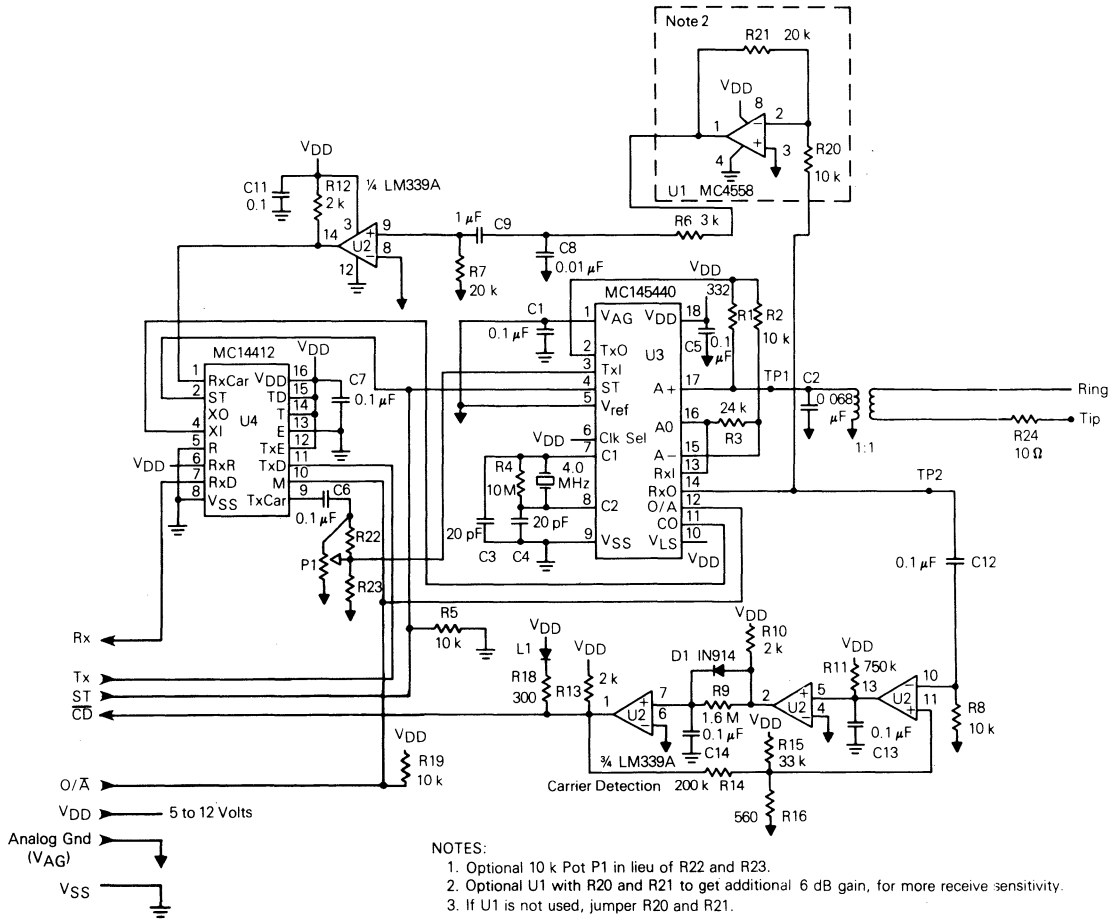


FIGURE 3 – TYPICAL MC145440 APPLICATION (+5 V SINGLE SUPPLY)



NOTES:
1. Optional 10 k Pot P1 in lieu of R22 and R23.
2. Optional U1 with R20 and R21 to get additional 6 dB gain, for more receive sensitivity.
3. If U1 is not used, jumper R20 and R21.

MC145441

Advance Information

2

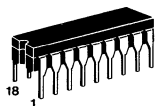
CCITT V.21 300 BAUD MODEM BAND-PASS FILTER

The MC145441 is a 300 baud modem filter designed to be used with the MC14412 or MC145445 modems. These modem/filter combinations fulfill the major requirements of a complete CCITT V.21 300 baud modem system. The MC145440 is also available to fulfill the Bell 103 equivalent filtering function. Features of the MC145441 include:

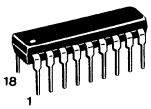
- Low Band Band-Pass Filter
- High Band Band-Pass Filter
- Spare Operational Amplifier
- Answer or Originate Mode
- Self Test Loopback Configuration (Optional)
- Single or Split Power Supply Operation
- 18-Pin Package
- CCITT V.21 Compatible

CMOS
(LOW-POWER COMPLEMENTARY MOS)

300 BAUD MODEM BAND-PASS SWITCHED CAPACITOR FILTER



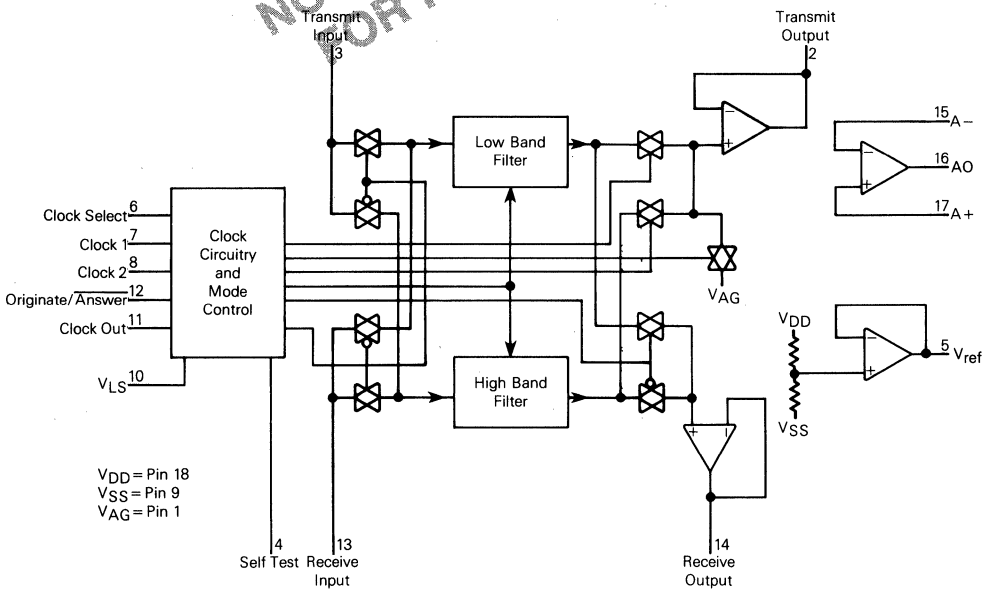
L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

NOT RECOMMENDED FOR NEW DESIGN

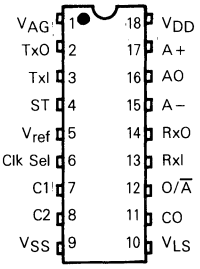
BLOCK DIAGRAM



MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 18	V
Input Voltage, all pins	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain per pin (Not V_{DD} or V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	4.5	10	16	V

DIGITAL ELECTRICAL CHARACTERISTICS (T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Operating Current, V_{DD} = 10 V, V_{SS} = 0 V, 1 MHz Crystal		I_{DD}	–	–	10	mA
Input Capacitance		C_{in}	–	5.0	7.5	pF
Mode Control Logic Levels						
V_{LS}	TTL Mode	–	V_{SS}	–	V_{DD}−4.0	V
	CMOS Mode	V_{IH}	V_{DD}−0.5	–	V_{DD}	
Clock Select (CS)	State 1, 4.0 MHz	V_{IH}	V_{DD}−0.5	–	V_{DD}	V
	State 2, 3.684 MHz	V_{IM}	(V_{DD}−V_{SS})/2−0.5	–	(V_{DD}−V_{SS})/2+0.5	
	State 3, 1.0 MHz	V_{IL}	V_{SS}	–	V_{SS}+0.5	
O/Ā TTL Logic Levels (V_{DD} = 5 V, V_{SS} = −5 V, V_{LS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" Level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level	V_{IH}	V_{LS}+2.0	–	–	V
	"0" level	V_{IL}	–	–	V_{LS}+0.8	
ST, C1, O/Ā CMOS Logic Levels (V_{LS} = V_{DD}, V_{SS} = 0 V)						
Input Current	"1" level	I_{IH}	–	–	+0.3	μA
	"0" level	I_{IL}	−0.3	–	–	
Input Voltage	"1" level, V_{DD} = 10 V	V_{IH}	7.5	5.75	–	V
	"0" level, V_{DD} = 10 V	V_{IL}	–	4.25	3.0	
CO Output Characteristics (V_{DD} = 10, V_{SS} = 0 V)						
TTL Output Voltage (TTL Mode)	"1" level, I_O = 8 mA	V_{OH}	2.4	–	–	V
	"0" level, I_O = 2.5 mA	V_{OL}	–	–	0.8	
CMOS Output Current	V_{DD} = 10 V, V_{OH} = 9.5 V	I_{OH}	−1.3	−2.25	–	mA
	V_{DD} = 10 V, V_{OL} = 0.5 V	I_{OL}	1.1	2.25	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = 5 V, V_{SS} = 0 V, T_A = 0 to 70°)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Input Current (V_{AG})	I_I	−50	–	+50	μA
DC Input Current (TxI, RxI)	I_I	−10	–	+10	μA
AC Input Impedance (TxI, RxI)	Z_{in}	0.2	1.0	–	MΩ
Input Voltage Range (TxI, RxI)	V_{in}	V_{SS}+1.5	–	V_{DD}−1.5	V

OP-AMP CHARACTERISTICS (V_{DD} = 5 to 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (AO)	I_{IO}	−50	–	+50	mV
Open Loop Gain (R_L = 10 kΩ)	A_{OL}	–	45	–	dB
Input Bias Current (A+, A−)	I_{IB}	–	±0.1	–	μA
Output Noise (900 Ω)	P_N	–	−3	–	dBrnC
Slew Rate	S_R	–	2	–	V/μs
Output Voltage Swing (R_L = 600 Ω to V_{AG})	–	1.5 V	–	V_{DD}−1.5 V	V

2

DIGITAL SWITCHING CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Rise and Fall Times	C1, O/A, ST	t_r, t_f	–	–	4	μs
Input Pulse Width	(TTL Mode) O/A	t_W	200	–	–	ns
	(CMOS Mode) C1, O/A, ST	t_W	125	–	–	
Clock Frequency (Driven by External Clock) (C1 Pin)	(CMOS Mode)	f_C	–	1.0	4.0	
Crystal Frequency	C1, C2	f_X	1.0	–	4.0	MHz

LOW-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 1080 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	−70	−64	dBmp
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Power Supply Rejection Ratio		PSRR	–	20	–	dB
Pass-Band Ripple	980 Hz to 1180 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 980 Hz, 0 dBmO	1180 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 1080 Hz)	1650 Hz to 1850 Hz	–	−55	–	–	dB
Differential Group Delay	980 Hz to 1180 Hz	–	–	–	600	μs

HIGH-BAND FILTER CHARACTERISTICS (V_{DD} = 10 V, V_{AG} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Full Scale Input Voltage (+3 dBmO)		V_{FS}	2.13	–	–	V_{P-P}
Gain at 1750 Hz, 0 dBmO		A_r	9.0	10.0	11.0	dB
Idle Noise, Input = V_{AG}, 900 Ω load		P_N	–	−70	−64	dBmp
Dynamic Range (Full Scale Output/Idle Noise)		DR	72	78	–	dB
Total Harmonic Distortion		THD	–	1.0	–	%
Power Supply Rejection Ratio		PSRR	–	20	–	dB
Pass-Band Ripple	1650 Hz to 1850 Hz	–	–	–	2	dBp-p
Pass-band Response, Ref. 1650 Hz, 0 dBmO	1850 Hz	–	−1.5	–	1.5	dB
Rejection (Ref. 1750 Hz)	980 Hz to 1180 Hz	–	−55	–	–	dB
Differential Group Delay	1650 Hz to 1850 Hz	–	–	–	600	μs

V_{ref} CHARACTERISTICS (V_{DD} = 5 to 15 V, V_{ref} = V_{DD}/2, V_{SS} = 0 V, T_A = 0 to 70°C)

Characteristic		Symbol	Min	Typ	Max	Unit
V_{ref} Output Voltage	I_O = ±5 mA	V_{ref}	−250	±75	+250	mV

PIN DESCRIPTIONS

V_{DD} (PIN 18) — Positive power supply.

V_{SS} (PIN 9) — Negative power supply.

V_{AG} (PIN 1) — Analog ground. In single supply applications, V_{AG} is driven from V_{ref}.

V_{ref} (PIN 5) — This pin provides an output DC voltage at approximately (V_{DD}-V_{SS})/2 for use as an external analog ground in single supply applications. In symmetric dual power supply applications, V_{ref} is not used.

V_{LS}, LOGIC SHIFT VOLTAGE (PIN 10) — This pin determines the input/output logic level compatibility of O/$\overline{A}$ and CO. When the voltage on this pin is greater than $V_{DD}-0.5$ V and less than V_{DD}, these digital inputs and outputs are CMOS compatible. When the voltage on this pin is less than $V_{DD}-4$ V and greater than V_{SS}, these digital inputs and outputs are TTL compatible, and V_{LS} is connected to digital ground.

C1, C2, CLOCK 1, CLOCK 2 (PIN 7, PIN 8) — These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from C1 to C2 as well as a 10 MΩ resistor in parallel with the crystal and 20 pF capacitors from C1 and C2 to V_{SS}. Crystal frequencies of 1.0, 3.6864, or 4.0 MHz may be used. Alternatively, an external CMOS level signal at the crystal frequency may be applied to C1 in lieu of the crystal, capacitors, and resistor. The inverted clock signal will appear at C2 and will be a CMOS output from V_{SS} to V_{DD}.

Clk Sel, CLOCK SELECT (PIN 6) — This pin is a three-state selector used to select one of the three crystal/clock options. When at V_{DD}, V_{AG}, or V_{SS}, this pin selects the 4.0, 3.6864, or 1.0 MHz crystal/clock option, respectively, for C1 and C2.

Clock Select Pin 6	Clock Frequency *	Clock Output Pin 11
V_{DD}	4.0 MHz	1.0 MHz
V_{AG}	3.6864 MHz	N/A
V_{SS}	1.0 MHz	1.0 MHz

*Use either an external clock to drive C1 Pin 7 or external crystal across C1 and C2 Pins 7 and 8.

CO, CLOCK OUT (PIN 11) — This provides a 1.0 MHz output clock signal when either the 1.0 or 4.0 MHz clock is selected and is typically used to drive the clock input to a MC14412 or MC6860 modem. The clock output is not usable when the 3.6864 MHz option is used. The logic family compatibility (CMOS or TTL) of this output is determined by V_{LS}.

O/$\overline{A}$, ORIGINATE, ANSWER (PIN 12) — The mode of the device, originate or answer, is selected with this pin. In the originate mode, selected with a logic "1", the low band band-pass filter is switched into the transmit path and the high band band-pass filter is switched into the receive path. In the answer mode, the filters switch position. The input levels of this pin are determined by V_{LS}.

TxI, TRANSMIT INPUT (PIN 3) — TxI is the input to the transmit band-pass filter which is the low band filter in the originate mode and the high band filter in the answer mode. In the self test mode, this input is routed to the appropriate band-pass filter input so as to pass the modulated data to the demodulator.

TxO, TRANSMIT OUTPUT (PIN 2) — This pin is the output of the Tx output amplifier and typically drives the modulated data into the duplexer or hybrid circuit (see ST pin).

RxI, RECEIVE INPUT (PIN 13) — RxI is the input to the receive band-pass filter which is the high band filter in the originate mode and the low band filter in the answer mode. In the self test mode, this input is disabled.

RxO, RECEIVE OUTPUT (PIN 14) — The output of the receive band-pass filter, whether low band or high band, is provided at RxO. Typically, this signal is capacitively coupled to the input of the external carrier detector and limiter. The AC coupling capacitor is required because of the variable DC offset of the receive filter.

ST, SELF TEST (PIN 4) — A "1" on ST puts the device into a self test mode which routes the modulated carrier from TxI, through the appropriate filter,and out RxO back to the receive carrier input of the modem. TxO remains at V_{AG} during a self test operation. This pin is a standard CMOS input regardless of the state of V_{LS}.

A+ (PIN 17) — This is the noninverting input to the spare operational amplifier.

A− (PIN 15) — This is the inverting input to the spare operational amplifier.

AO (PIN 16) — This is the output of the spare operational amplifier.

FUNCTIONAL DESCRIPTION

This device is capable of four basic analog configurations determined by the state of O/$\overline{A}$ and ST. The normal (non-self test) and self test modes in both the answer and originate modes will be discussed.

In the normal originate mode, O/$\overline{A}$ is a "1" and self test, ST, is a "0". When in this mode, the Tx carrier from the modem is input on TxI and routed through the low band band-pass filter. The filter output is switched to the input of the Tx op-amp which typically drives the Tx carrier off chip into a duplexer circuit which could be implemented with the spare operational amplifier. The output of the duplexer drives RxI which is switched to the input of the high band band-pass filter. The filter output is available at RxO which is typically the input to a limiter and carrier detector.

The normal answer mode is established by a "0" on both O/$\overline{A}$ and ST. This mode is identical to the normal originate mode with one exception: the band-pass filters swap positions, i.e., the high band band-pass filter is switched into the transmit path, and the low band band-pass filter is switched into the receive path.

When used with the MC14412 in the self test mode, the device will function as follows. A "1" on the self test pin of both devices enables the self test mode. The modem switches its demodulator to its modulator frequency and demodulates its own modulated carrier. The modem filter switches the transmit carrier of the modem from TxI through the low band filter and out the RxO pin to the limiter when in the originate mode. When the system is in the answer mode, the modulated signal is instead routed through the high-band filter. TxO will remain at mid-supply (V_{AG}) during self test operations.

FIGURE 1 — TEST CIRCUIT

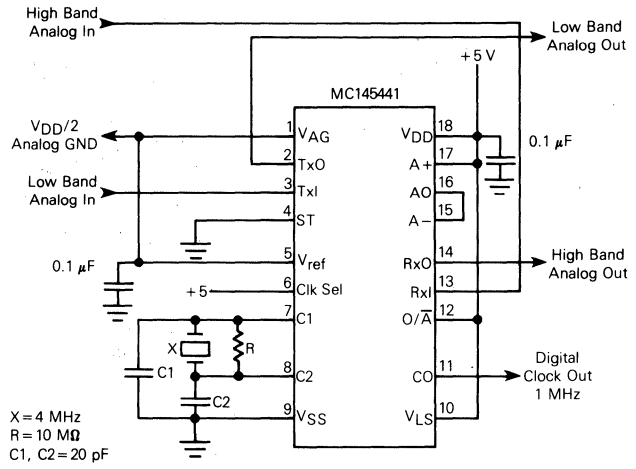


FIGURE 2 — MC145441 FREQUENCY RESPONSE

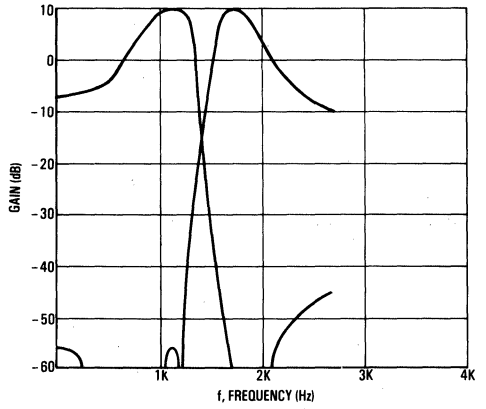
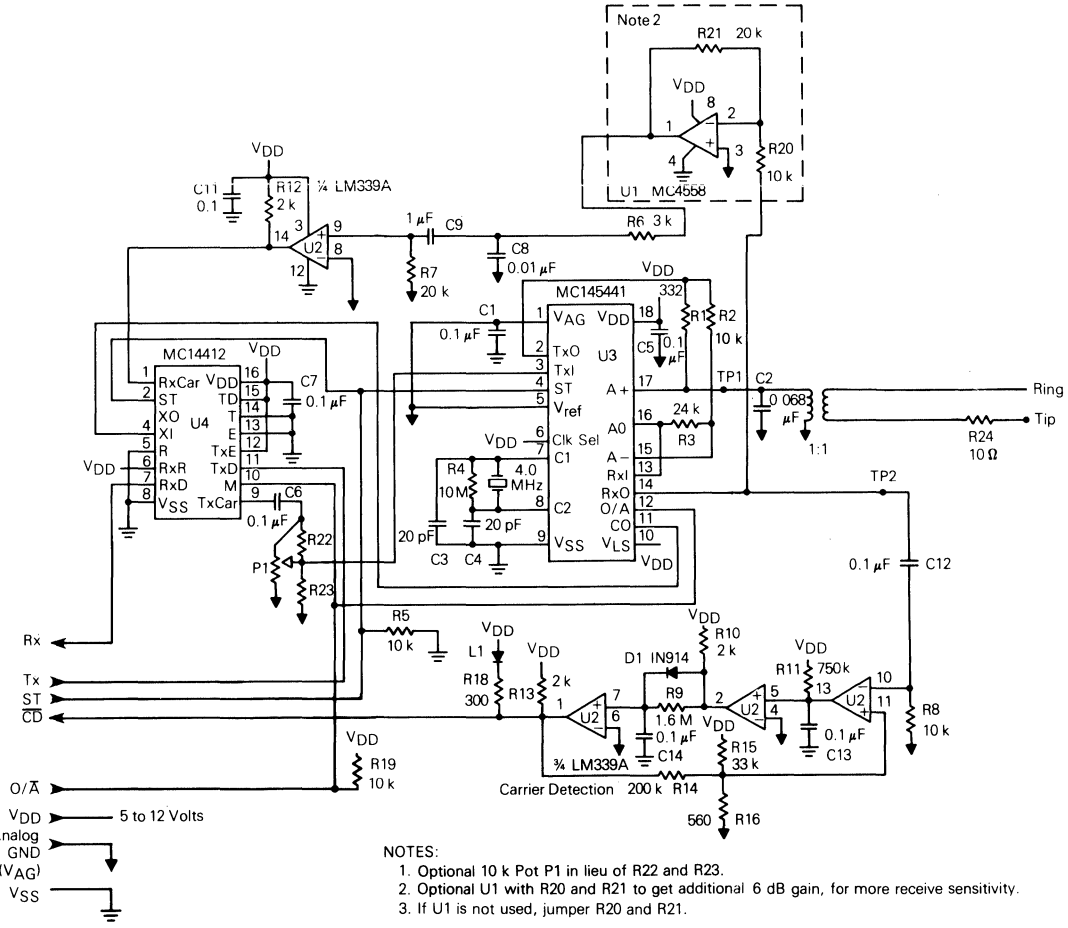


FIGURE 3 — TYPICAL MC145441 APPLICATION (+5 V SINGLE SUPPLY)



NOTES:
1. Optional 10 k Pot P1 in lieu of R22 and R23.
2. Optional U1 with R20 and R21 to get additional 6 dB gain, for more receive sensitivity.
3. If U1 is not used, jumper R20 and R21.

MC145442
MC145443

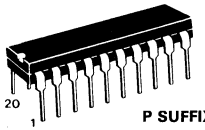
2

Advance Information

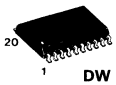
Single Chip 300 Baud Modem

The MC145442 and MC145443 silicon-gate CMOS single-chip low-speed modems contain a complete frequency shift keying (FSK) modulator, demodulator, and filter. These devices are compatible with CCITT V.21 (MC145442) and Bell 103 (MC145443) specifications. Both devices provide full-duplex or half-duplex 300 baud data communicaton over a pair of telephone lines. They also include a carrier detect circuit for the demodulator section and a duplexer circuit for direct operation on a telephone line through a simple transformer.

- MC145442 Compatible with CCITT V.21
- MC145443 Compatible with Bell 103
- Low-Band and High-Band Bandpass Filters On-Chip
- Simplex, Half-Duplex, and Full-Duplex Operation
- Originate and Answer Mode
- Analog Loopback Configuration for Self Test
- Hybrid Network Function On-Chip
- Carrier Detect Circuit On-Chip
- Adjustable Transmit Level and $\overline{CD}$ Delay Timing
- On-Chip Crystal Oscillator (3.579 MHz)
- Single +5 Volt Power Supply Operation
- Internal Mid-Supply Generator
- Power-Down Mode
- Pin Compatible with MM74HC943
- Capable of Driving −9 dBm into a 600-Ohm Load

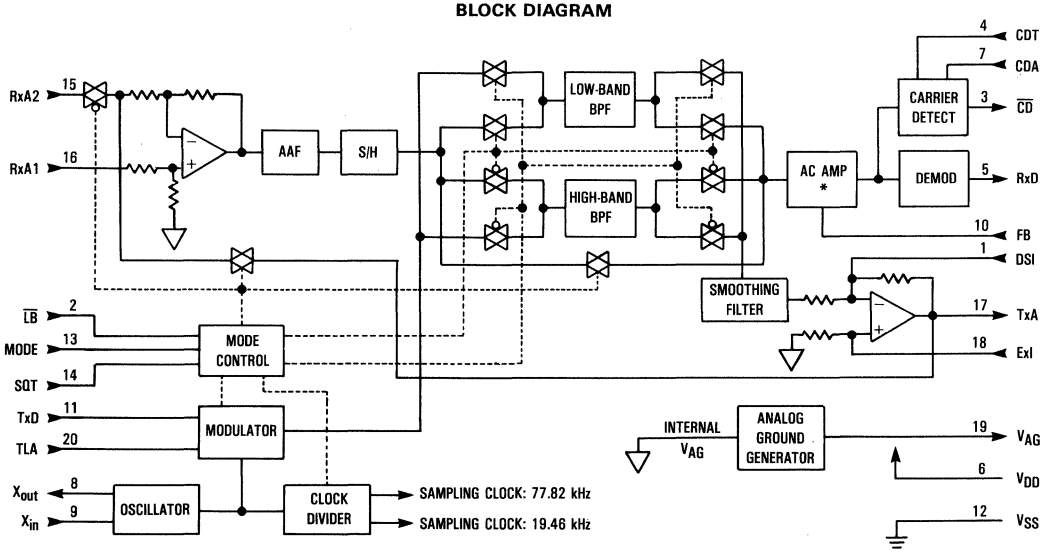


P SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

BLOCK DIAGRAM



*Refer to the FB pin description.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to 7.0	V
DC Input Voltage	V_{in}	−0.5 to V_{DD}+0.5	V
DC Output Voltage	V_{out}	−0.5 to V_{DD}+0.5	V
Clamp Diode Current, per Pin	I_{IK}, I_{OK}	±20	mA
DC Output Current, per Pin	I_{out}	±28	mA
Power Dissipation	PD	500	mW
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused outputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input or Output Voltage	V_{in}, V_{out}	0	V_{DD}	V
Input Rise or Fall Time	t_r, t_f	—	500	ns
Crystal Frequency*	$f_{crystal}$	3.2	5.0	MHz

*Changing the crystal frequency from 3.579 MHz will change the output frequencies. The change in output frequency will be proportional to the change in crystal frequency.

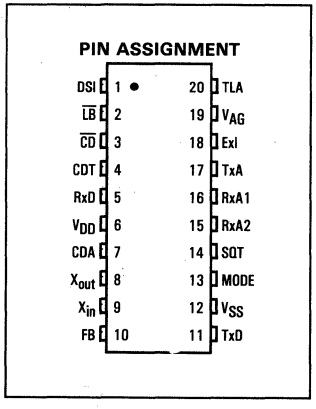
DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 V ±10%, T_A= −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	$\overline{LB}$	V_{IH}	V_{DD}−0.8	—	—	V
	X_{in}, TxD, Mode, SQT		3.15	—	—	
Low-Level Input Voltage	$\overline{LB}$	V_{IL}	—	—	0.8	V
	X_{in}, TxD, Mode, SQT		—	—	1.1	
High-Level Output Voltage		V_{OH}				V
I_{OH}=20 μA	$\overline{CD}$, RxD		V_{DD}−0.1	—	—	
I_{OH}=2 mA	$\overline{CD}$, RxD		3.7	—	—	
I_{OH}=20 μA	X_{out}		—	V_{DD}−0.05	—	
Low-Level Output Voltage		V_{OL}				V
I_{OL}=20 μA	$\overline{CD}$, RxD		—	—	0.1	
I_{OL}=2 mA	$\overline{CD}$, RxD		—	—	0.4	
I_{OL}=20 μA	X_{out}		—	0.05	—	
Input Current	$\overline{LB}$, TxD, Mode, SQT	I_{in}	—	—	±1.0	μA
	RxA1, RxA2		—	10	±12	
	X_{in}		—	—	±10	
Quiesent Supply Current X_{in} or $f_{crystal}$=3.579 MHz		I_{DD}	—	7	10	mA
Power-Down Supply Current			—	200	300	μA
Input Capacitance	X_{in}	C_{in}	—	10	—	pF
	All Other Inputs		—	—	10	
V_{AG} Output Voltage (I_O = ±10 μA)		V_{AG}	2.4	2.5	2.6	V
CDA Output Voltage (I_O = ±10 μA)		V_{CDA}	1.1	1.2	1.3	V
Line Driver Feedback Resistor		R_f	10	20	30	kΩ

2

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = −40 to 85°C, Crystal Frequency = 3.579 MHz ±0.1%; See Figure 1)

Characteristic		Min	Typ	Max	Unit
TRANSMITTER					
Power Output on TxA RL = 1.2 kΩ, R_{TLA} = ∞ RL = 1.2 kΩ, R_{TLA} = 5.5 kΩ		 −13 −10	 −12 −9	 −11 −8	dBm
Second Harmonic Power RL = 1.2 kΩ		—	−56	—	dBm
RECEIVE FILTER AND HYBRID					
Hybrid Input Impedance RxA1, RxA2		40	50	—	kΩ
FB Output Impedance		—	16	—	kΩ
Adjacent Channel Rejection		−48	—	—	dBm
DEMODULATOR					
Receive Carrier Amplitude		−48	—	−12	dBm
Dynamic Range		—	36	—	dB
Bit Jitter (S/N = 30 dB, Input = −38 dBm, Bit Rate = 300 baud)		—	100	—	μs
Bit Bias		—	5	—	%
Carrier Detect Threshold (CDA = 1.2 V or CDA grounded through a 0.1 μF capacitor)	On to Off Off to On	— —	−44 −47	— —	dBm



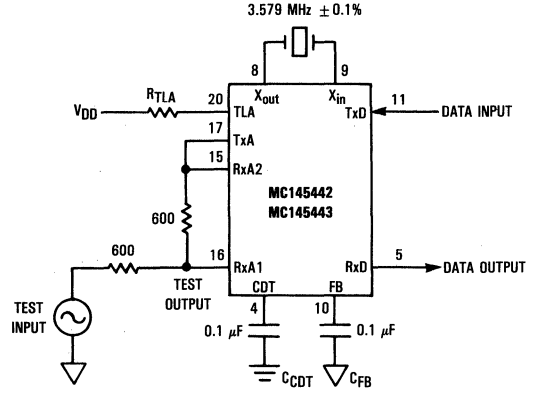


Figure 1. AC Characteristics Evaluation Circuit

PIN DESCRIPTIONS

V_{DD}—POSITIVE POWER SUPPLY (PIN 6)

This pin is normally tied to 5.0 V.

V_{SS}—NEGATIVE POWER SUPPLY (PIN 12)

This pin is normally tied to 0 V.

V_{AG}—ANALOG GROUND (PIN 19)

Analog ground is internally biased to $(V_{DD} - V_{SS})/2$. This pin must be decoupled by a capacitor from V_{AG} to V_{SS} and a capacitor from V_{AG} to V_{DD}. Analog ground is the common bias line used in the switched capacitor filters, limiter, and slicer in the demodulation circuitry.

TLA—TRANSMIT LEVEL ADJUST (PIN 20)

This pin is used to adjust the transmit level. Transmit level adjustment range is typically from −12 dBm to −9 dBm. (See Applications Information.)

TxD—TRANSMIT DATA (PIN 11)

Binary information is input to the transmit data pin. Data entered for transmission is modulated using FSK techniques. A logic high input level represents a mark and a logic low represents a space. (See Table 1.)

Table 1. Bell 103 and CCITT V.21 Frequency Characteristics

Bell 103 (MC145443)				
Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
CCITT V.21 (MC145442)				
Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Space	1180 Hz	1850 Hz	1850 Hz	1180 Hz
Mark	980 Hz	1650 Hz	1650 Hz	980 Hz

NOTE: Actual frequencies may be ±5 Hz assuming a 3.579545 MHz crystal is used.

TxA—TRANSMIT CARRIER (PIN 17)

This is the output of the line driver amplifier. The transmit carrier is the digitally synthesized sine wave output of the modulator derived from a crystal oscillator reference. When a 3.579 MHz crystal is used the frequency outputs shown in Table 1 apply. (See Applications Information.)

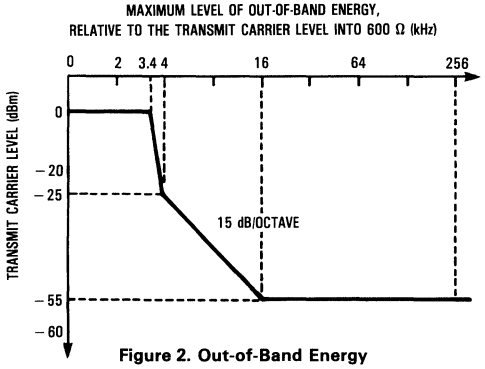


Figure 2. Out-of-Band Energy

ExI—EXTERNAL INPUT (PIN 18)

The external input is the noninverting input to the line driver. It is provided to combine an auxiliary audio signal or speech signal to the phone line using the line driver. This pin should be connected to V_{AG} if not used. The average level must be the same as V_{AG} to maintain proper operation. (See Applications Information.)

DSI—DRIVER SUMMING INPUT (PIN 1)

The driver summing input may be used to connect an external signal, such as a DTMF dialer, to the phone line. A series resistor, R_{DSI}, is needed to define the voltage gain A_V (see Applications Information and Figure 6). When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (pin 14) to a logic high level. The voltage gain, A_V, is calculated by the formula $A_V = -R_f/R_{DSI}$ (where $R_f \approx 20$ kΩ). For example, a 20 kΩ resistor for R_{DSI} will provide unity gain ($A_V = -20$ kΩ/20 kΩ $= -1$). This pin MUST be left OPEN if not used.

RxD—RECEIVE DATA (PIN 5)

The receive data output pin presents the digital binary data resulting from the demodulation of the receive carrier. If no carrier is present, $\overline{CD}$ high, the receive data output (RxD) is clamped high.

RxA2, RxA1—RECEIVE CARRIER (PINS 15, 16)

The receive carrier is the FSK input to the demodulator through the receive band-pass filter. RxA1 is the noninverting input and RxA2 is the inverting input of the receive hybrid (duplexer) operational amplifier.

$\overline{LB}$—ANALOG LOOPBACK (PIN 2)

When a high level is applied to this pin (SQT must be low), the analog loopback test is enabled. The analog loopback test connects the TxA pin to the RxA2 pin and the RxA1 to analog ground. In loopback, the demodulator frequencies are switched to the modulation frequencies for the selected mode. (See Tables 1 and 2 and Figures 4c and 4d.)

When $\overline{LB}$ is connected to analog ground (V_{AG}), the modulator generates an echo cancellation tone of 2100 Hz for MC145442 CCITT V.21 and 2225 Hz for MC145443 Bell 103 systems. For normal operation, this pin should be at a logic low level (V_{SS}).

The power-down mode is enabled when both $\overline{LB}$ and SQT are connected to a logic high level. (See Table 2.)

Table 2. Functional Table

MODE Pin 13	SQT Pin 14	$\overline{LB}$ Pin 2	Operating Mode
1	0	0	Originate Mode
0	0	0	Answer Mode
X	0	V_{AG} ($V_{DD}/2$)	Echo Tone
X	0	1	Analog Loopback
X	1	0	Squelch Mode
X	1	V_{AG} ($V_{DD}/2$)	Squelch Mode
X	1	1	Power Down

MODE—MODE (PIN 13)

This input selects the pair of transmit and receive frequencies used during modulation and demodulation. When a logic high level is placed on this input, originate (Bell) or channel 1 (CCITT) is selected. When a low level is placed on this input, answer (Bell) or channel 2 (CCITT) is selected. (See Tables 1 and 2 and Figure 4.)

CDT—CARRIER DETECT TIMING (PIN 4)

A capacitor on this pin to V_{SS} sets the amount of time the carrier must be present before $\overline{CD}$ goes low. (See Applications Information for the capacitor values.)

2

$\overline{CD}$—CARRIER DETECT OUTPUT (PIN 3)

This output is used to indicate when a carrier has been sensed by the carrier detect circuit. This output goes to a logic low level when a valid signal above the minimum threshold level (defined by CDA pin 7) is maintained on the input to the hybrid circuit longer than the response time (defined by CDT pin 4). This pin is held at the logic low level until the signal falls below the maximum threshold level for longer than the turn off time. (See Applications Information and Figure 5.)

CDA—CARRIER DETECT ADJUST (PIN 7)

An external voltage may be applied to this pin to adjust the carrier detect threshold. The threshold hysteresis is internally fixed at 3 dB. (See Applications Information.)

X_{out}, X_{in}—CRYSTAL OSCILLATOR (PINS 8, 9)

A crystal reference oscillator is formed when a 3.579 MHz crystal is connected between these two pins. X_{out} (pin 8) is the output of the oscillator circuit, and X_{in} (pin 9) is the input to the oscillator circuit. When using an external clock, apply the clock to the X_{in} (pin 9) pin and leave X_{out} (pin 8) open. An internal 10 mΩ resistor and internal capacitors, typically 10 pF on X_{in} and 16 pF on X_{out}, allow the crystal to be connected without any other external components. Printed circuit board layout should keep external stray capacitance to a minimum.

FB—FILTER BIAS (PIN 10)

This is the negative input to the ac amplifier. In normal operation, this pin is connected to analog ground through a 0.1 μF bypass capacitor in order to cancel the input offset voltage of the limiter. It has a nominal input impedance of 16 kΩ. (See Figure 3.)

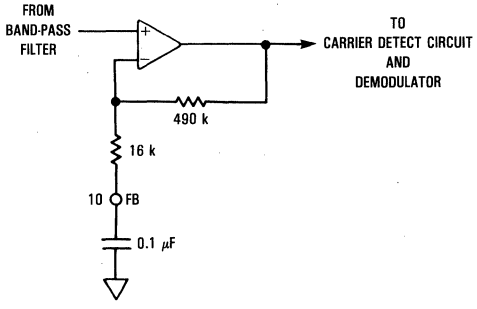


Figure 3. AC Amplifier Circuit

SQT—TRANSMIT SQUELCH (PIN 14)

When this input pin is at a logic high level, the modulator is disabled. The line driver remains active if $\overline{LB}$ is at a logic low level. (See Table 2.)

When both $\overline{LB}$ and SQT are connected to a logic high level, see Table 2, the entire chip is in a power down state and all circuitry except the crystal oscillator is disabled. Total power supply current decreases from 10 mA (maximum) to 300 μA (maximum).

GENERAL DESCRIPTION

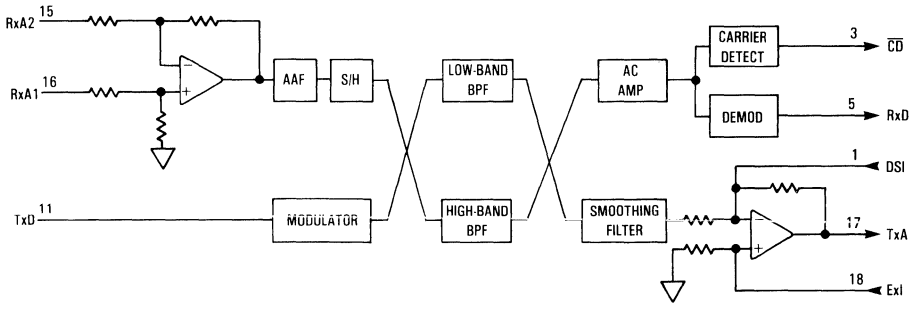
The MC145442 and MC145443 are full-duplex low-speed modems. They provide a 300 baud FSK signal for bidirectional data transmission over the telephone network. They can be operated in one of four basic configurations as determined by the state of MODE (pin 13) and $\overline{LB}$ (pin 2). The normal (non-loopback) and self test (loopback) modes in both answer and originate modes will be discussed.

For an originate or channel 1 mode, a logic high level is placed on MODE (pin 13) and a logic low level is placed on $\overline{LB}$ (pin 2). In this mode, transmit data is input on TxD, where it is converted to a FSK signal and routed through a low-band band-pass filter. The filtered output signal is then buffered by the Tx op-amp line driver, which is capable of driving −9 dBm onto a 600 Ω line. The receive signal is connected through a hybrid duplexer circuit on pins 15 and 16, RxA2 and RxA1. The signal then passes through the anti-aliasing filter, the sample-and-hold circuit, is switched into the high-band band-pass filter, and then switched into the ac amplifier circuit. The output of the ac amplifier circuit is routed to the demodulator circuit and demodulated. The resulting digital data is then output through RxD (pin 5). The carrier detect circuit receives its signal from the output of the ac amplifier circuit and goes low when the incoming signal is detected. (See Figure 4a.)

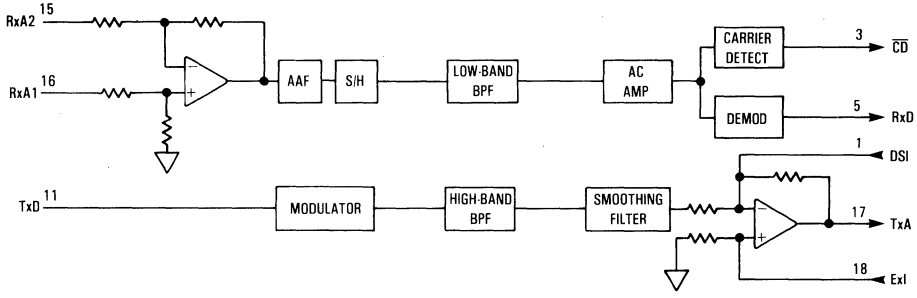
In the answer or channel 2 mode, a logic low level is placed on MODE (pin 13) and on $\overline{LB}$ (pin 2). In this mode, the data follows the same path except the FSK signal is routed to the high-band band-pass filter and the sample-and-hold signal is routed through the low-band band-pass filter. (See Figure 4b.)

In the analog loopback originate or channel 1 mode, a logic high level is placed on MODE (pin 13) and on $\overline{LB}$ (pin 2). This mode is used for a self check of the modulator, demodulator, and low-band pass-band filter circuit. The modulator side is configured exactly like the originate mode above except the line driver output (TxA pin 17) is switched to the negative input of the hybrid op-amp. The RxA2 input pin is open in this mode and the noninverting input of the hybrid circuit is connected to V_{AG}. The sample-and-hold output bypasses the filter so that the demodulator receives the modulated Tx data (see Figure 4c). This test checks all internal device components except the high-band band-pass filter which can be checked in the answer or channel 2 mode loopback test.

In the analog loopback answer or channel 2 mode, a logic low level is placed on MODE (pin 13) and a logic high level on $\overline{LB}$ (pin 2). This mode is used for a self check of the modulator, demodulator, and high-band pass-band filter circuit. This configuration is exactly like the originate loopback mode above, except the signal is routed through the high-band pass-band filter. (See Figure 4d.)

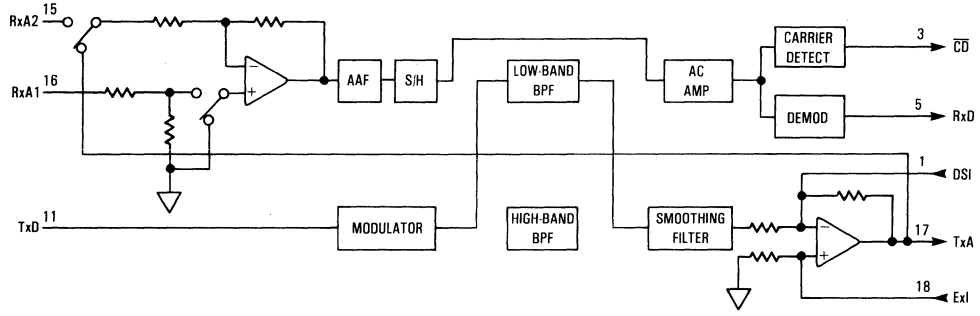


(a) ORIGINATE/CHANNEL 1 MODE (MODE = HIGH, $\overline{LB}$ = LOW)

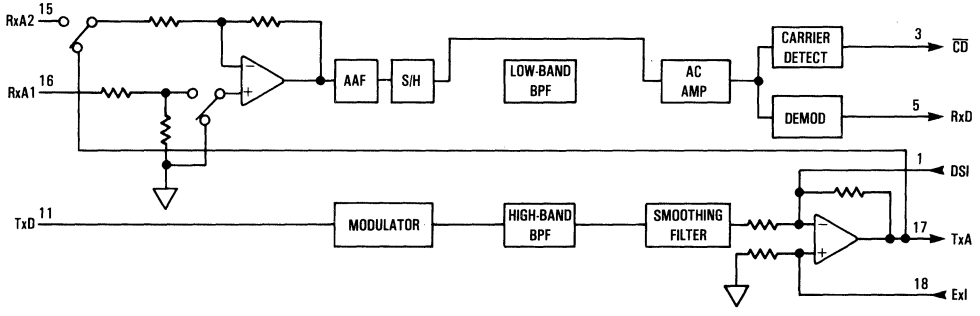


(b) ANSWER/CHANNEL 2 MODE (MODE = LOW, $\overline{LB}$ = LOW)

Figure 4. Basic Operating Modes



(c) ORIGINATE/CHANNEL 1 MODE AND ANALOG LOOPBACK STATE (MODE = HIGH, $\overline{LB}$ = HIGH)



(d) ANSWER/CHANNEL 2 MODE AND ANALOG LOOPBACK STATE (MODE = LOW, $\overline{LB}$ = HIGH)

Figure 4. Basic Operating Modes

APPLICATIONS INFORMATION

CARRIER DETECT TIMING ADJUSTMENT

The value of a capacitor, C_{CDT} at CDT (pin 4) determines how long a received modem signal must be present above the minimum threshold level before $\overline{CD}$ (pin 3) goes low. The C_{CDT} capacitor also determines how long the $\overline{CD}$ pin stays low after the received modem signal goes below the minimum threshold. The $\overline{CD}$ pin is used to distinguish a strong modem signal from random noise. The following equations show the relationship between t_{CDL}, the time in seconds required for $\overline{CD}$ to go low; t_{CDH}, the time in seconds required for $\overline{CD}$ to go high; and C_{CDT}, the capacitor value in μF.

Valid signal to $\overline{CD}$ response time: $t_{CDL} \approx 6.4 \times C_{CDT}$

Invalid signal to $\overline{CD}$ off time: $t_{CDH} \approx 0.54 \times C_{CDT}$

Example: $t_{CDL} \approx 6.4 \times 0.1\ \mu F \approx 0.64$ seconds

$t_{CDH} \approx 0.54 \times 0.1\ \mu F \approx 0.054$ seconds

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is set by internal resistors to activate $\overline{CD}$ with a typical −44 dBm (into 600 Ω) signal and deactivate $\overline{CD}$ with a typical −47 dBm signal applied to the input of the hybrid circuit. The carrier detect threshold level can be adjusted by applying an external voltage on CDA (pin 7). The following equations may be used to find the CDA voltage required for a given threshold voltage. (V_{on} and V_{off} are in volts RMS.)

$$V_{CDA} = 244 \times V_{on}$$

$$V_{CDA} = 345 \times V_{off}$$

Example (internally set)

$V_{on} = 4.9$ mV ≈ −44 dBm: $V_{CDA} = 244 \times 4.9$ mV = 1.2 V

$V_{off} = 3.5$ mV ≈ −47 dBm: $V_{CDA} = 345 \times 3.5$ mV = 1.2 V

Example (externally set):

$V_{on} = 7.7$ mV ≈ −40 dBm: $V_{CDA} = 244 \times 7.7$ mV = 1.9 V

$V_{off} = 5.4$ mV ≈ −43 dBm: $V_{CDA} = 345 \times 5.4$ mV = 1.9 V

The CDA pin has an approximate Thevenin equivalent voltage of 1.2 V and an output impedance of 100 kΩ. When using the internal 1.2 volt reference a 0.1 μF capacitor should be connected between this pin and V_{SS}. (See Figure 5.)

TRANSMIT LEVEL ADJUSTMENT

The power output at TxA (pin 17) is determined by the value of resistor R_{TLA} that is connected between TLA (pin 20) to V_{DD} (pin 6). Table 3 shows the R_{TLA} values and the corresponding power output for a 600 Ω load. The voltage at TxA is twice the value of that at ring and tip because TxA feeds the signal through a 600 Ω resistor R_{Tx} to a 600 Ω line transformer. (See Figure 7.) When choosing resistor R_{TLA}, keep in mind that −9 dBm is the maximum output level allowed from a modem onto the telephone line (in the U.S.). In addition, keep in mind that maximizing the power output from the modem optimizes the signal-to-noise ratio, improving accurate data transmission.

Table 3. Transmit Level Adjust

Output Transmit Level (Typical into 600 Ω)	R_{TLA}
−12 dBm	∞
−11 dBm	19.8 kΩ
−10 dBm	9.2 kΩ
−9 dBm	5.5 kΩ

THE LINE DRIVER

The line driver is a power amplifier used for driving the telephone line. Both the inverting and noninverting input to the line driver are available for transmitting externally generated tones.

Exl (pin 18) is the noninverting input to the line driver and gives a fixed gain of 2 (R_i = 50 kΩ). The average signal level must be the same as V_{AG} to maintain proper operation. This pin should be connected to V_{AG} if not used.

The driver summing input (DSI, pin 1) may be used to connect an external signal, such as a DTMF dialer, to the phone line. When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (pin 14) to a logic high level. DSI MUST be left OPEN if not used.

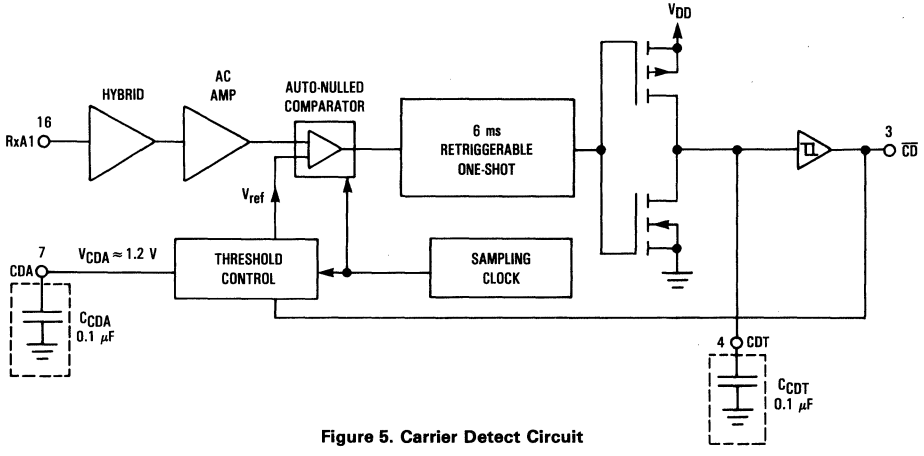


Figure 5. Carrier Detect Circuit

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In addition, the DSI pin is the inverting side of the line driver and allows adjustable gain with a series resistor R_{DSI}. (See Figure 6.) The voltage gain, A_V, is determined by the equation:

$$A_V = -\frac{R_f}{R_{DSI}}$$

where $R_f \approx 20$ kΩ.

Example: A resistor value of 20 kΩ for R_{DSI} will provide unity gain.

$$A_V = -(20\ k\Omega / 20\ k\Omega) = -1$$

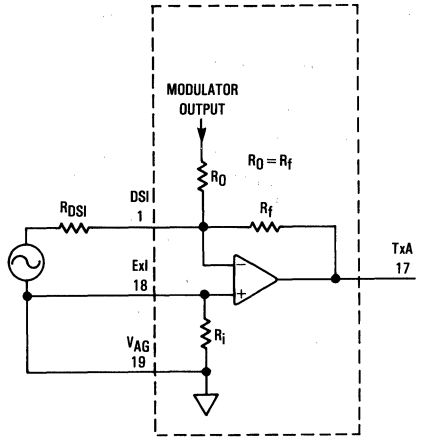
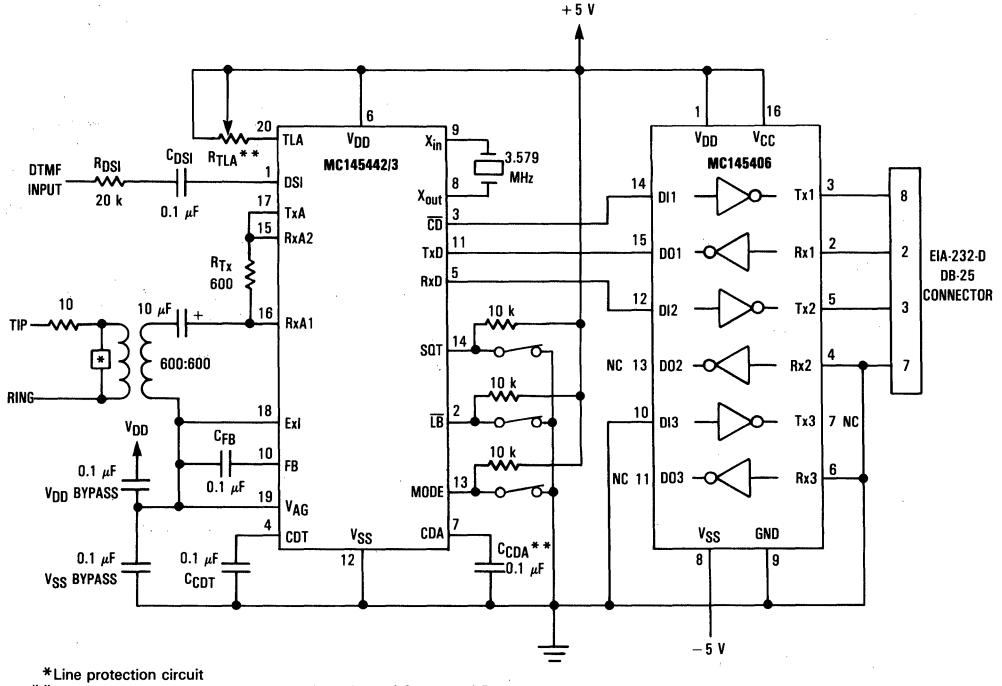


Figure 6. Line Driver Using the DSI Input



*Line protection circuit
**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 7. Typical MC145442/MC145443 Applications Circuit

MC145445

CMOS

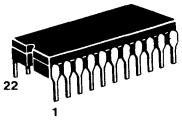
300 BAUD FSK MODEM

2

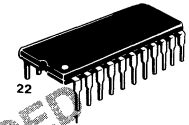
0—300 BAUD FSK MODEM

The MC145445 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 103/113 and CCITT V. 21 applications. Features of the device include:

- Bell 103/113 Answer and Originate Compatible, 0-300 Baud
- CCITT V. 21 Modes 1 and 2 Compatible, 0-300 Baud
- Eight Selectable $\overline{RTS}$ to $\overline{CTS}$ Delay Options
- Answer-Back Tone Generator (U.S. and CCITT Tones)
- Carrier Detect Input
- TTL Compatible
- 22 Pin Package
- Compatible to the MC145440 Bell 103 or MC145441 CCITT V. 21 Modem Filter



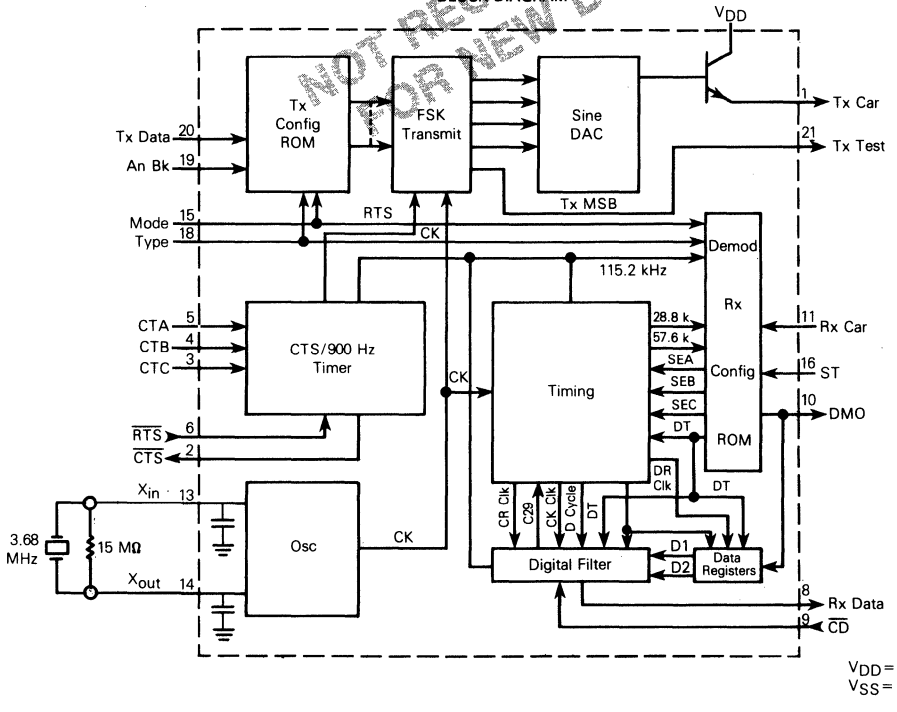
L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

NOT RECOMMENDED FOR NEW DESIGN

MC145445 300 BAUD FSK MODEM BLOCK DIAGRAM



2

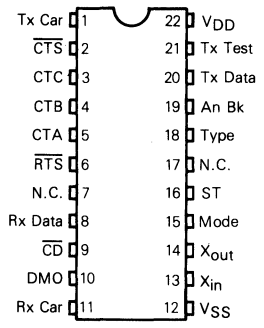
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $0°C \le T_A \le 70°C$)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	–	–	–	V
Pins 3-6, 9, 15, 16, 18, 19, 20	–	2.8	–	–	
Pin 13, 11	–	4.0	–	–	
Input Low Voltage	V_{IL}	–	–	–	V
Pin 3-6, 9, 15, 16, 18, 19, 20	–	–	–	0.5	
Pin 13, 11	–	–	–	0.6	
Input Current	I_{in}	–	–	–	μA
All Inputs (V_{IL} 0 V)	–	–	–	−5.0	
All Inputs Except Pins 11, 13, ($V_{IH}>2.8$ V) (Note 1)	–	–	–	500	
Output High Current ($V_{OH}=2.4$ V)	I_{OH}	–	–	–	mA
Pins 2, 8 (Test Load A)	–	0.75	–	–	
Pins 10, 21 (Test Load B)	–	0.75	–	–	
Output Low Current ($V_{OL}=0.4$ V)	I_{OL}	–	–	–	mA
Pins 2, 8 (Test Load A)	–	1.2	–	–	
Pins 10, 21 (Test Load B)	–	0.6	–	–	
Operating Current	I_{DD}	–	2.5	6	mA
Input Capacitance	C_{in}	–	–	–	pF
All Except Pin 13	–	–	–	12	
Pin 13 (X_{in})	–	–	8	–	
Output Capacitance	C_{out}	–	–	–	pF
All Except Pin 14	–	–	–	12	
Pin 14 (X_{out})	–	–	13	–	
Transmit Audio Signal Level (Pin 1 $R_L=10$ kΩ (Note 2)	–	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	–	−50	−40	dB

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $0°C \le T_A \le 70°C$)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)	t_r	–	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)	t_r	–	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)	t_f	–	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)	t_f	–	20	100	ns
Input Rise and Fall Times (Except Pin 13)	t_r, t_f	–	–	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	t_d	–	1	–	μs

NOTES:
1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (±10%) and offset by a dc bias of 0.5 V_{DD} (±10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

N.C., NO CONNECTION (PINS 7 AND 17)
These pins are not bonded internally. They should be left open in normal operation.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATIOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resisitor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects answer mode when Bell type is selected or channel 2 when CCITT type is selected. A "1" on this pin selects originate mode when Bell type is selected or channel 1 when CCITT type is selected.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back). Loopback can be done using a hardwire scheme, or automatically using the internal loopback feature of the filter, such as found on the MC145440/41.

TYPE (PIN 18)
This pin is used to select between Bell 103/113 type operation and CCITT V.21 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

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FIGURE 1 — An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

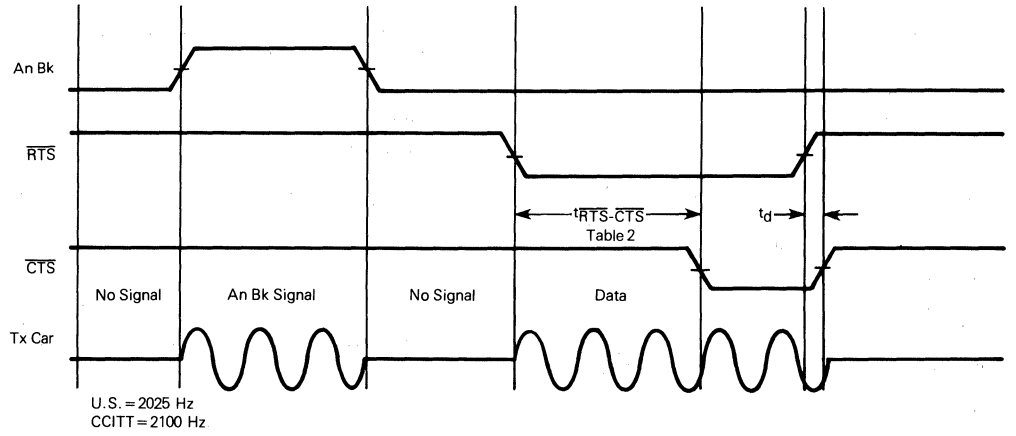


TABLE 1 — $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

*All delays are ±1.7 ms.

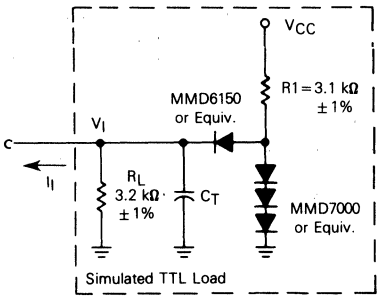
TABLE 2—OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Application
0	0	0	1850	1850.6	CCITT V. 21
		1	1650	1650.13	0-300 Baud, Channel 2
0	1	0	1180	1180.03	CCITT V.21
		1	980	979.9	0-300 Baud, Channel 1
1	0	0	2025	2025.5	Bell 103
		1	2225	2226.09	0-300 Baud, Answer Mode
1	1	0	1070	1069.76	Bell 103
		1	1270	1270.3	0-300 Baud, Originate Mode

Data = 0 = Space
= 1 = Mark

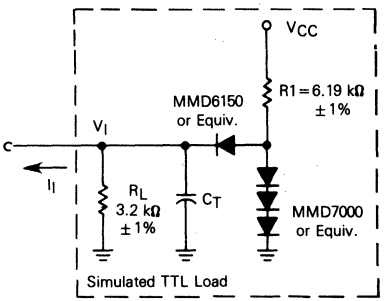
Crystal Frequency = 3.6864 MHz

FIGURE 2 — OUTPUT TEST LOAD A



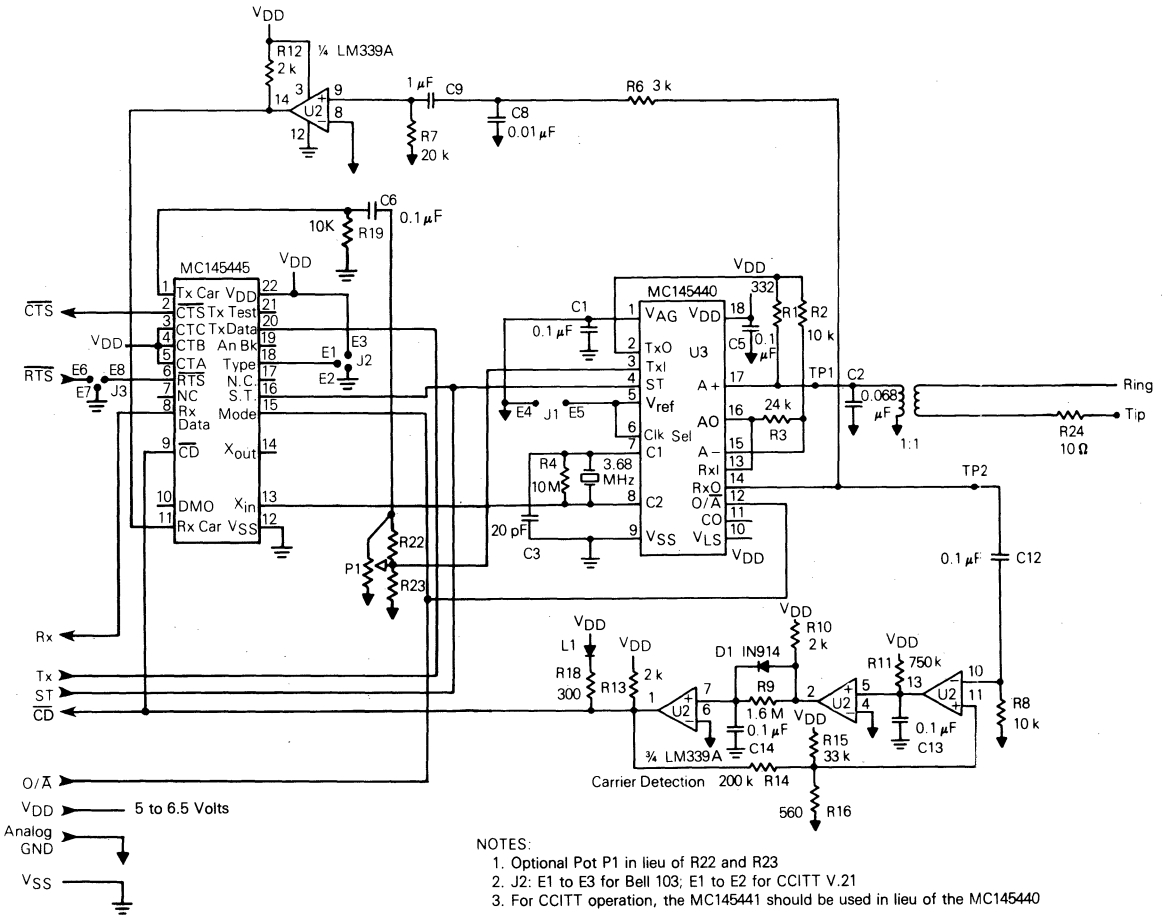
C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 3 — OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 — TYPICAL BELL 103/113 ORIGINATE/ANSWER MODEM



NOTES:
1. Optional Pot P1 in lieu of R22 and R23
2. J2: E1 to E3 for Bell 103; E1 to E2 for CCITT V.21
3. For CCITT operation, the MC145441 should be used in lieu of the MC145440

MC145450

Advance Information

CMOS

1200 BAUD FSK MODEM

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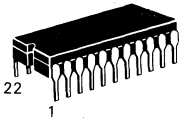
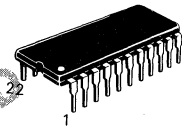
1200 BAUD FSK MODEM

The MC145450 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 202 and CCITT V.23 applications. Features of the device include:

- Bell 202 Compatible 0 to 1800 Baud Main Channel
- 0 to 150 Baud Reverse Channel
- CCITT V.23 Mode 2 Compatible 0 to 1800 Main Channel
- CCITT V.23 0 to 75 Baud Compatible Reverse Channel
- TTL Compatible
- Eight Selectable $\overline{RTS}$-$\overline{CTS}$ Delay Options
- Soft Turn-Off Capability
- Answer Back Tone Generator (US and CCITT Tones)
- Carrier Detect Input
- 22 Pin Package



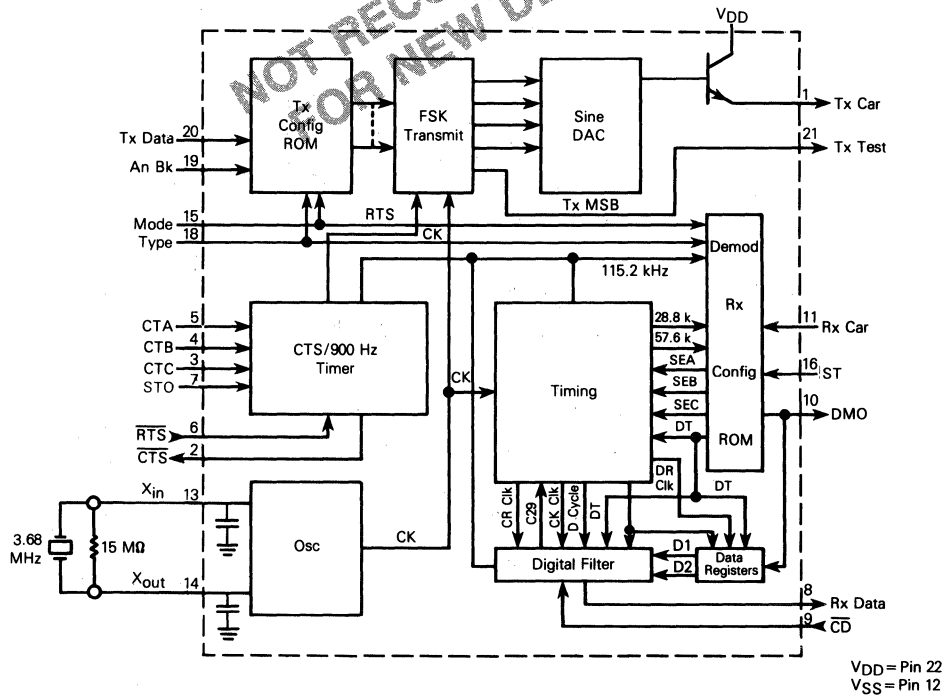
L SUFFIX
CERAMIC PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

NOT RECOMMENDED FOR NEW DESIGN

MC145450 1200 BAUD FSK MODEM
BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

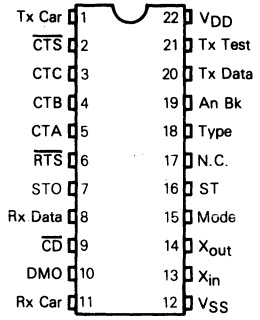
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	10	V
Input Voltages, All Inputs	V_{in}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	I_{out}	 10 35	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	4.5	5.0	6.5	V

PIN ASSIGNMENTS



DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				V
Pins 3-7, 9, 15, 16, 18, 19, 20	–	2.8	–	–	
Pin 13, 11	–	4.0	–	–	
Input Low Voltage	V_{IL}				V
Pins 3-7, 9, 15, 16, 18, 19, 20		–	–	0.5	
Pin 13, 11		–	–	0.6	
Input Current	I_{in}				μA
All Inputs (V_{IL} 0 V)		–	–	−5.0	
All Inputs Except Pins 11, 13, ($V_{IH}>2.8$ V) (Note 1)		–	–	600	
Output High Current ($V_{OH}=2.4$ V)	I_{OH}				mA
Pins 2, 8 (Test Load A)		0.75	–	–	
Pins 10, 21 (Test Load B)		0.75	–	–	
Output Low Current ($V_{OL}=0.4$ V)	I_{OL}				mA
Pins 2, 8 (Test Load A)		1.2	–	–	
Pins 10, 21 (Test Load B)		0.6	–	–	
Operating Current	I_{DD}	–	2.5	6	mA
Input Capacitance	C_{in}				pF
All Except Pin 13		–	–	12	
Pin 13 (X_{in})		–	8	–	
Output Capacitance	C_{out}				pF
All Except Pin 14		–	–	12	
Pin 14 (X_{out})		–	13	–	
Transmit Audio Signal Level (Pin 1 $R_L=10$ kΩ (Note 2)	–	0.428	0.5	0.578	Vp-p
Total Harmonic Distortion (2nd to 14th) (Note 2)	THD	–	−50	−40	dB

AC ELECTRICAL CHARACTERISTICS ($V_{DD}=5.0$ V ±5%, $V_{SS}=0$, $T_A=0$ to 70°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)		t_r	–	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)		t_r	–	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)		t_f	–	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)		t_f	–	20	100	ns
Input Rise and Fall Times (Except Pin 13)		t_r, t_f	–	–	1000	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	STO = Low	$t_{d(low)}$	–	1	–	μs
Delay From $\overline{RTS}$ to $\overline{CTS}$	STO = High	$t_{d(high)}$	18.3	–	21.7	ms

NOTES:
1. Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The I_{in} specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the V_{DD} level.
2. Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

PIN DESCRIPTIONS

V_{DD}, POSITIVE POWER SUPPLY (PIN 22)
This is nominally 5.0 V.

V_{SS}, NEGATIVE POWER SUPPLY (PIN 12)
This is usually 0 volts.

Tx Car, TRANSMIT CARRIER (PIN 1)
The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of 0.1 V_{DD} (p-p) (±10%) and offset by a dc bias of 0.5 V_{DD} (±10%). The output load should be 10 kilohms or greater.

$\overline{CTS}$, CLEAR TO SEND (PIN 2)
The clear to send output goes low in response to a high-to-low translation of $\overline{RTS}$ following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of $\overline{RTS}$. During the time following activation of $\overline{RTS}$ and before the activation of $\overline{CTS}$, Tx Data should be held in the mark condition.

CTA, CLEAR TO SEND SELECT A (PIN 5)
CTB, CLEAR TO SEND SELECT B (PIN 4)
CTC, CLEAR TO SEND SELECT C (PIN 3)

For delay times for clear to send delay select inputs, see Table 1.

$\overline{RTS}$, REQUEST TO SEND (PIN 6)
The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

STO, SOFT TURN OFF INPUT (PIN 7)
Activation of STO causes a 900 Hz tone to be transmitted and $\overline{CTS}$ to remain active for 20 ms following the loss of $\overline{RTS}$. See Figure 5.

Rx Data, RECEIVE DATA (PIN 8)
The receive data output is the serial data output from the demodulator. Rx Data is clamped high when $\overline{CD}$ is not active.

$\overline{CD}$, CARRIER DETECT (PIN 9)
When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

DMO, DEMODULATOR OUTPUT (PIN 10)
The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

Rx Car, RECEIVER CARRIER (PIN 11)
The receiver carrier input is the FSK input to the demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

X_{in}, OSCILLATOR INPUT (PIN 13)
X_{out}, OSCILLATOR OUTPUT (PIN 14)
X_{in} should be driven from either an AT-cut crystal or a digital signal source at 3.6864 MHz ±0.01%. When driven by a crystal, a 15 megohm resisitor should be connected from X_{in} to X_{out} in parallel with the crystal.

MODE (PIN 15)
The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects forward channel operation; i.e. high-speed transmit and low-speed receive. A "1" on this pin selects reverse channel operation; i.e. low-speed transmit and high-speed receive.

ST, SELF TEST (PIN 16)
When a high level is placed on this pin, the demodulator is switched to the modulator frequencies and baud rate (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back).

N.C. NO CONNECTION (PIN 17)
This pin is not bonded internally and should be left open in normal operation.

TYPE (PIN 18)
This pin is used to select Bell 202 type operation and CCITT V.23 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

An Bk, ANSWER BACK (PIN 19)
The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and $\overline{CTS}$ will go to a high state, regardless of the state of $\overline{RTS}$ (see Figure 1).

Tx Data, TRANSMIT DATA (PIN 20)
The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

Tx Test, TRANSMIT TEST (PIN 21)
The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

FIGURE 1 — An Bk AND $\overline{RTS}$-$\overline{CTS}$ TIMING

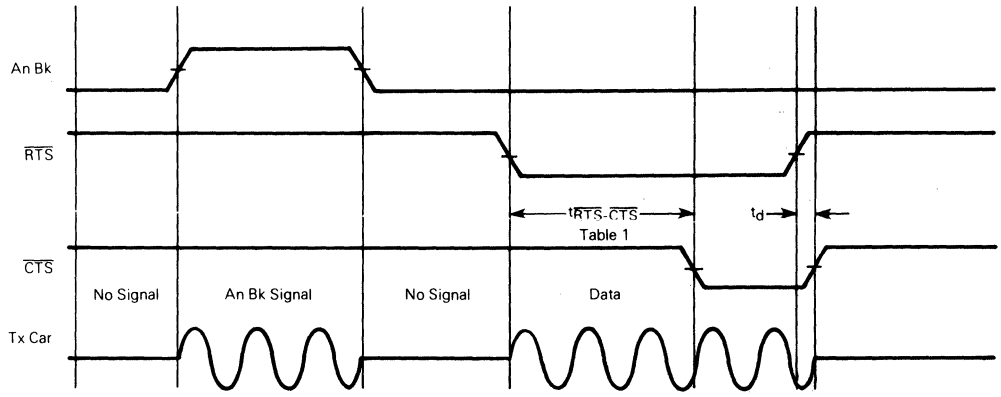


TABLE 1 — $\overline{RTS}$-$\overline{CTS}$ DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

*All delays are ±1.7 ms.

TABLE 2 — OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency Spec	Transmit Frequency Actual	Answer Back Tone	Application
0	0	0	2100	2099.32	2100	CCITT V.23 75 Baud Receive 1200 Baud Transmit
		1	1300	1299.86		Forward Channel
0	1	0	450	450	2100	CCITT V.23 1200 Baud Receive 75 Baud Transmit
		1	390	390.5		Reverse Channel
1	0	0	2200	2199.52	2025	U.S. 150 Baud Receive 1200 Baud Transmit (Bell 202)
		1	1200	1200		Forward Channel
1	1	0	510	509.73	390	U.S. 1200 Baud Receive (Bell 202) 150 Baud Transmit
		1	390	390.5		Reverse Channel

Data = 0 = Space
= 1 = Mark

*Crystal Frequency = 3.6864 MHz

2

FIGURE 2 — STO TIMING

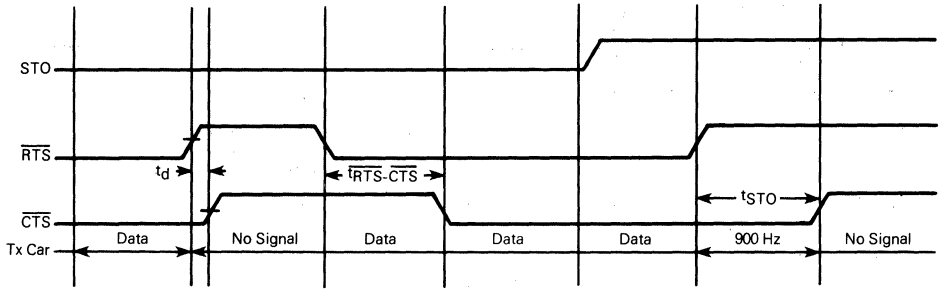
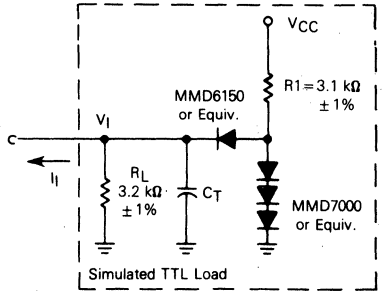
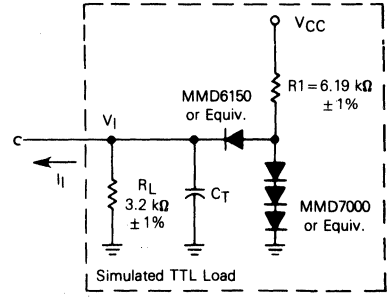


FIGURE 3 — OUTPUT TEST LOAD A



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 — OUTPUT TEST LOAD B



C_T = 20 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 5 — TYPICAL MEDIUM-SPEED MODEM APPLICATION

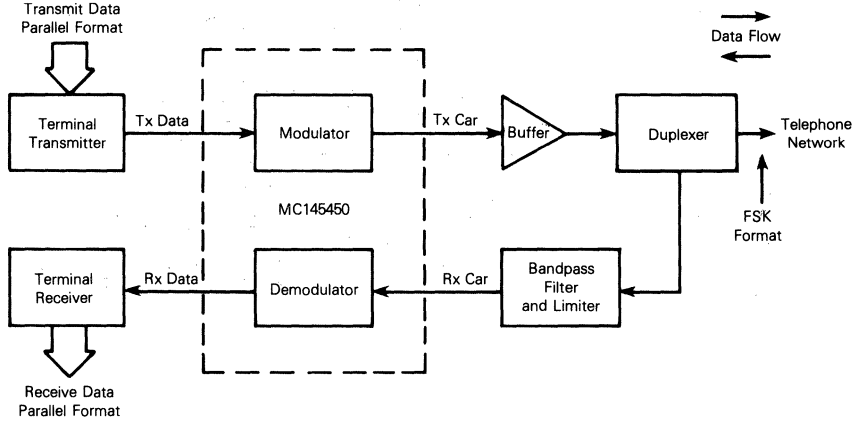
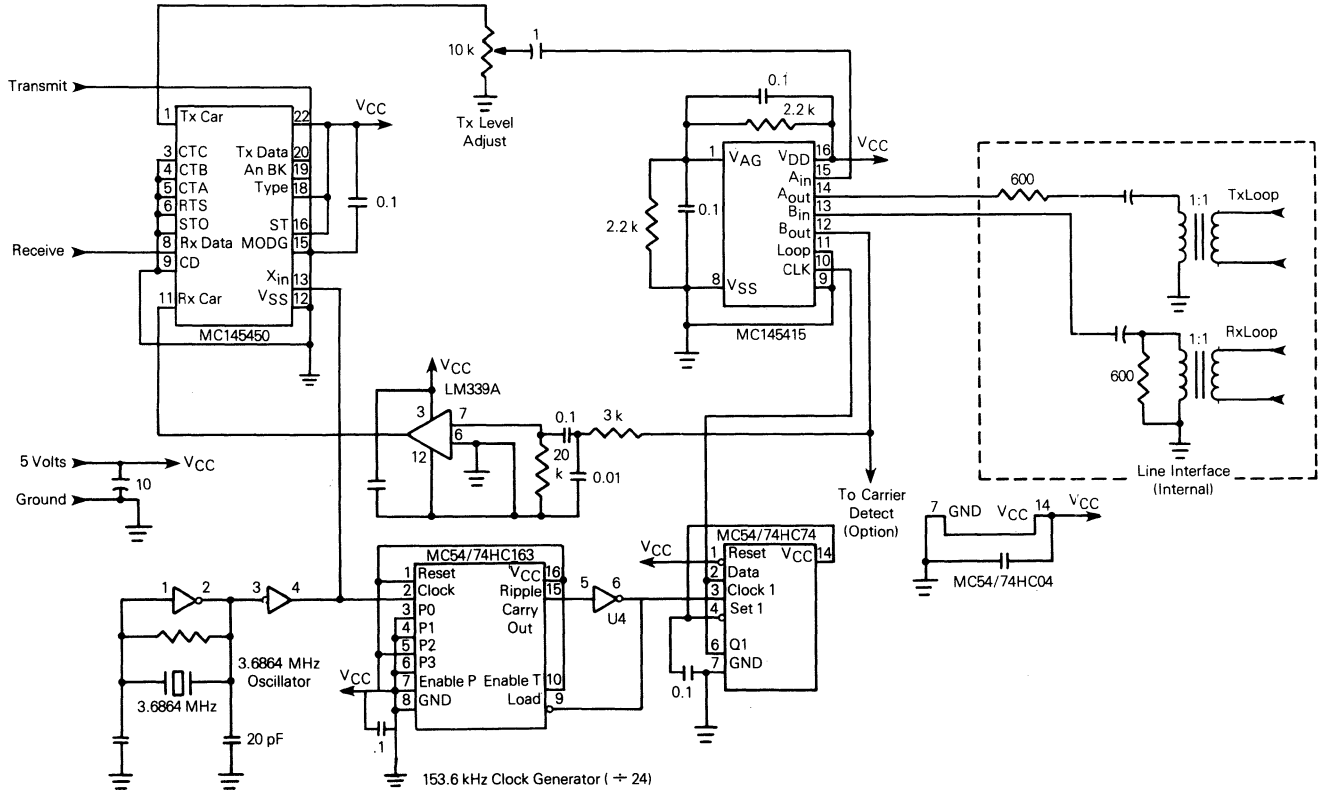


FIGURE 6 — TYPICAL 1200 BAUD 4 WIRE MODEM APPLICATION



2

MC145472

Product Preview

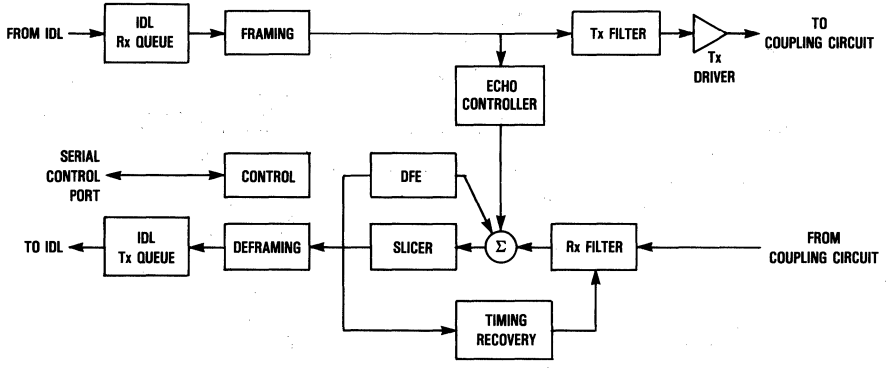
ISDN U Reference Point Transceiver

2

The MC145472 is an Integrated Services Digital Network-Basic Access Transceiver for metallic loops for application on the network side of the NT-Layer 1. It provides a 144 kbps full duplex transmission capability for twisted pair loops.

- A Single Chip 2B1Q, Echo Cancelling, Adaptively Equalized Transceiver
- Conforms to the American National Standard for ISDN Basic Access Interface for Application at the Network Side of the NT, Layer 1 Specification (ANSI T1.xxx-1988)
- Customer Data (2B + D) Provided To/From the Industry Standard Inter-Chip Digital Link (IDL)
- Control, Status, and Extended Maintenance Functions are Provided Via the Industry Standard Serial Peripheral Interface (SPI) Serial Control Port (SCP)
- On-Chip Conformance with Activation/Deactivation as Specified in the American National Standard
- Basic Maintenance Functions are Provided On-Chip
- Automatic, Internal Compliance with the Embedded Operations Channel (EOC) Protocol as Specified in the American National Standard
- Extended Maintenance Functions Provided Via the Serial Control Port
- Complete Set of Loopbacks for Both the IDL and U Reference Point Directions
- Pin Selectable NT/LT Mode of Operation
- Low Power Consumption When in the Deactivated State
- On Chip Transmit Driver
- Low Power CMOS

BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC145474
MC145475

Advance Information

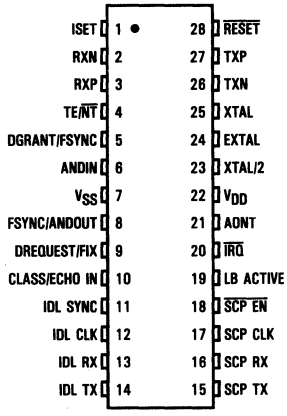
ISDN S/T Interface Transceiver

The MC145474/75 ISDN S/T transceiver provides an economical VLSI layer one interface for the transportation of 2B + D information between network termination and terminal equipment applications. The MC145474/75 conforms to the CCITT I.430 and ANSI TI.605 recommendations. It provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145474/75 provides the activation/deactivation, error monitoring, framing, bit and octet timing. The MC145474/75 also provides the control signals for the interface to the layer two devices, complete multiframe capability and maintenance signalling channels. The MC145474/75 features the Interchip Digital Link (IDL) for the exchange of 2B + D channel information between ISDN components and systems. The MC145474/75 provides an industry standard serial control port (SCP) to program the operation of the transceiver.

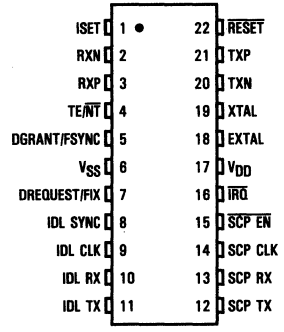
- Conforms to the CCITT I.430 Recommendations
- Features the Interchip Digital Link (IDL)
- Pin Selectable Network or Terminal Operating Modes
- Industry Standard Microprocessor Serial Control Port
- Supports 1:1 Transformers for Transmit and Receive
- Extended Range Operation in Both Point-to-Point and Passive-Bus Operation
- Supports Multiframing on SC1 through SC5 and Q Channels
- Optional B Channel Idle, Exchange, or Invert
- Supports Full Range of S/T and IDL Loopbacks
- Supports Low Power Wake-Up Mode
- Supports Crystal or Clock Input
- 1.5 μ CMOS Design for 5-Volt Low Power Operation

PIN ASSIGNMENTS

MC145475



MC145474



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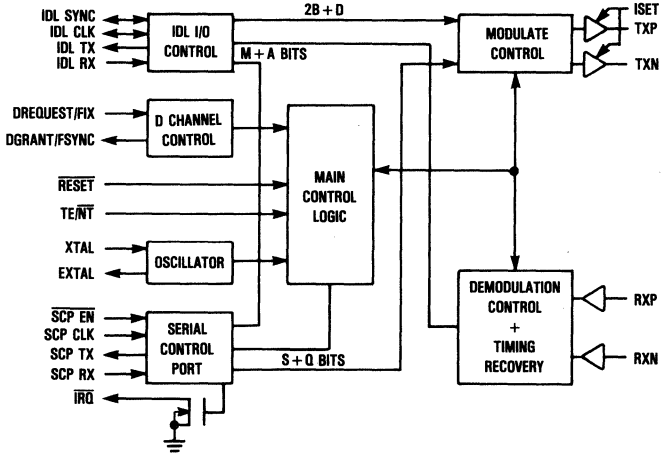


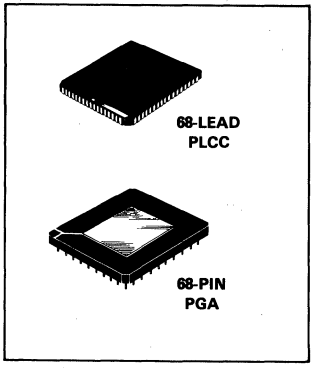
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC145488

2

Advance Information★

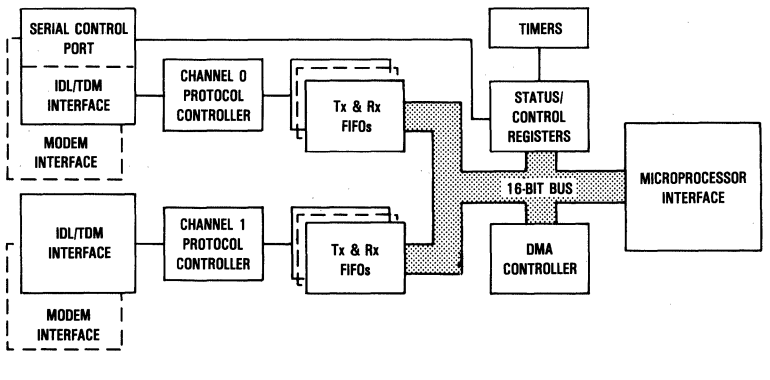
Dual Data Link Controller (DDLC)



The MC145488 is a two-channel ISDN LAPD controller with an on-chip direct memory access (DMA) controller. It is intended for ISDN terminal and switch applications where one or two channels of data will use HDLC-type protocols. The DDLC is ideally suited for use with the MC145474 S/T Transceiver. The Interchip Digital Link (IDL) easily connects the chips together, providing a powerful layer one/layer two ISDN solution. A serial control port efficiently controls the MC145474 or other ISDN family devices. The DDLC is compatible with 68000 and 80186 bus structures.

- Two Independent Full-Duplex Bit-Oriented Protocol Controllers Support HDLC, SDLC, CCITT X.25, CCITT Q.921 (LAPD), and V.120 at Basic and Primary Rates
- Four Channel On-Chip DMA Controller
  - 64 Kbyte Address Range with Expansion Control
  - Internal Programmable Wait-State Generator
  - Two Buffer Descriptors for Each Receiver Channel
- Compatible with 68000 and 80186 Bus Structures
- Nonmultiplexed 16- and 8-Bit Data Bus
- Bit-Level HDLC Processing Including:
  - Flag Generation/Detection
  - Abort Generation/Detection
  - Zero Insertion/Deletion
  - CRC-CCITT Generation/Checking
  - Residue Bit Handler
- TEI/SAPI Address Comparison
  - Three Address Comparisons
  - Wildcard Bits for Block Comparisons
- Transparent Mode for Codec Compatibility
- Programmable Interrupt Vector Generator
- Two Independent Timers Configurable as a Watchdog Timer
- Flexible Serial Interface with:
  - IDL Interface for Connection to Other ISDN Family Devices
  - Timeslot Interface for Connection to PBX-Type Backplanes
  - Modem Interface for Other Applications
- Supports CCITT Specification I.460
- Supports DMI Specification 3.1 Modes 0, 1, 2, and 3
- Serial Control Port for ISDN Family Device Control
- Low-Power CMOS with Automatic Power-Down

BLOCK DIAGRAM



★Contact your Motorola representative for samples and complete data.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC145500
MC145501
MC145502
MC145503
MC145505

2

Advance Information

PCM Codec/Filter Mono-Circuit

The MC145500, MC145501, MC145502, MC145503, and MC145505 are all per channel PCM codec/filter mono-circuits. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. The MC145500 and MC145503 are general purpose devices that are offered in a 16-pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on chip precision reference voltage. The MC145501 is offered in an 18-pin package and adds the capability of selecting from three peak overload voltages (2.5, 3.15, and 3.78 V). The MC145505 is a synchronous device offered in a 16-pin DIP and wide body SOIC package intended for instrument use. The MC145502 is the full-featured device which presents all of the options of the chip. This device is packaged in a 22-pin DIP and a 28-pin chip carrier package and contains all the features of the MC145500 and MC145501 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

These devices are pin-for-pin replacements for Motorola's first generation of MC14400/01/02/03/05 PCM mono-circuits and upwardly compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of TSACs and MC3419 SLIC products.

The MC145500 family of PCM codec/filter mono-circuits utilizes CMOS due to its reliable low-power performance and proven capability for complex analog/digital VLSI functions.

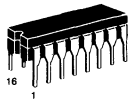
MC145500
- 16-Pin Package
- Transmit Bandpass and Receive Low-Pass Filters on Chip
- Pin Selectable Mu/A Law Companding with Corresponding Data Format
- On Chip Precision Reference Voltage (3.15 V)
- Power Dissipation of 50 mW, Power Down of 0.1 mW at ±5 Volts
- Automatic Prescaler Accepts 128 kHz, 1.536, 1.544, 2.048, and 2.56 MHz for Internal Sequencing

MC145501—All of the Above Plus:
- 18-Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15, 3.78 Volts)
- Access to the Inverting Input of the Txl Input Operational Amplifier

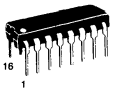
MC145502—All of the Above Plus:
- 22-Pin Package
- Variable Data Clock Rates (64 kHz to 4.1 MHz)
- Complete Access to the Three Terminal Transmit Input Operational Amplifier
- An External Precision Reference May Be Used

MC145503—All the Above Features of the MC145500 Plus:
- 16-Pin Package
- Complete Access to the Three Terminal Transmit Input Operational Amplifier

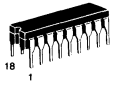
MC145505—Same as MC145503 Except:
- 16-Pin Package
- Common 64 kHz to 4.1 MHz Transmit/Receive Data Clock



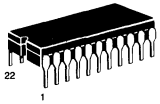
L SUFFIX
CERAMIC
CASE 620
MC145500/03/05



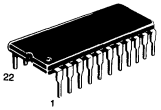
P SUFFIX
PLASTIC
CASE 648
MC145503/05



L SUFFIX
CERAMIC
CASE 726
MC145501



L SUFFIX
CERAMIC
CASE 736



P SUFFIX
PLASTIC
CASE 708
MC145502

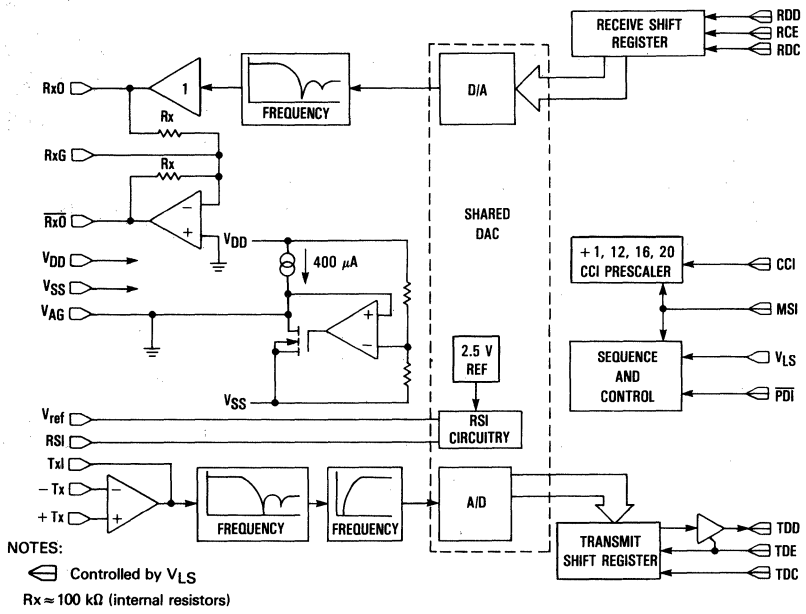
DW SUFFIX
SO
CASE 751
MC145503
MC145505

FN SUFFIX
CHIP CARRIER
CASE 776
MC145502

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

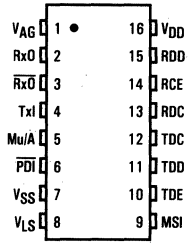
MC145500/01/02/03/05 PCM CODEC/FILTER MONO-CIRCUIT BLOCK DIAGRAM



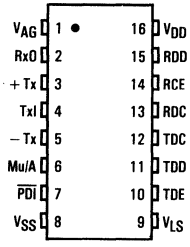
PIN ASSIGNMENT

(Drawings Do Not Reflect Relative Size)

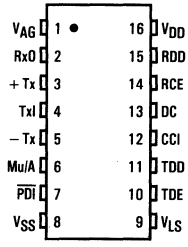
MC145500L



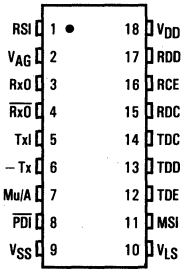
MC145503L,P



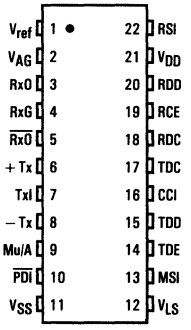
MC145505L,P



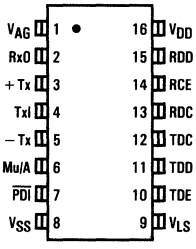
MC145501L



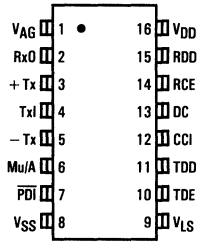
MC145502L,P

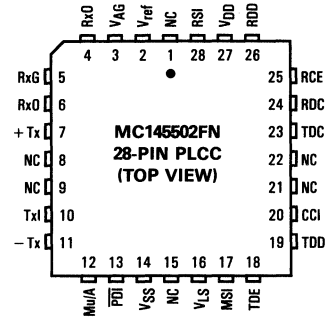


MC145503DW



MC145505DW





MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}-V_{SS}$	−0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Drain Per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused outputs must always be tied to an appropriate logic voltage level (e.g., V_{SS}, V_{DD}, V_{LS}, or V_{AG}).

RECOMMENDED OPERATING CONDITIONS (T_A = −40 to +85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage					V
Dual Supplies: V_{DD} = $-V_{SS}$, (V_{AG} = V_{LS} = 0 V)		4.75	5.0	6.3	
Single Supply: V_{DD} to V_{SS} (V_{AG} is an Output, V_{LS} = V_{DD} or V_{SS})					
MC145500, MC145501, MC145502, MC145503, MC145505 (Using Internal 3.15 V Reference)		8.5	–	12.6	
MC145501, MC145502 Using Internal 2.5 V Reference		7.0	–	12.6	
MC145501, MC145502 Using internal 3.78 V Reference		9.5	–	12.6	
MC145502 Using External 1.5 V Reference, Referenced to V_{AG}		4.75	–	12.6	
Power Dissipation					mW
CMOS Logic Mode (V_{DD} to V_{SS} = 10 V, V_{LS} = V_{DD})		–	40	70	
TTL Logic Mode (V_{DD} = +5 V, V_{SS} = −5 V, V_{LS} = V_{AG} = 0 V)		–	50	90	
Power Down Dissipation		–	0.1	1.0	mW
Frame Rate Transmit and Receive		7.5	8.0	8.5	kHz
Data Rate		–	128	–	kHz
MC145500, MC145501, MC145503		–	1536	–	
Must Use One of These Frequencies ±2%, Relative to MSI Frequency of 8 kHz		–	1544	–	
		–	2048	–	
		–	2560	–	
Data Rate for MC145502, MC145505		64	–	4096	kHz
Full Scale Analog Input and Output Level					V_P
MC145500, MC145503, MC145505		–	3.15	–	
MC145501, MC145502 (V_{ref} = V_{SS})	RSI = V_{DD}	–	3.78	–	
	RSI = V_{SS}	–	3.15	–	
	RSI = V_{AG}	–	2.5	–	
MC145502 Using an External Reference Voltage Applied at V_{ref} Pin	RSI = V_{DD}	–	1.51 × V_{ref}	–	
	RSI = V_{SS}	–	1.26 × V_{ref}	–	
	RSI = V_{AG}	–	V_{ref}	–	

DIGITAL LEVELS (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = −40 to +85°C)

Characteristic		Symbol	Min	Max	Unit
Input Voltage Levels (TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI, PDI)					V
CMOS Mode (V_{LS} = V_{DD}, V_{SS} is Digital Ground)	"0"	V_{IL}		0.3 × V_{DD}	
	"1"	V_{IH}	0.7 × V_{DD}		
TTL Mode ($V_{LS} \le V_{DD}-4.0$ V, V_{LS} is Digital Ground)	"0"	V_{IL}		V_{LS} + 0.8 V	
	"1"	V_{IH}	V_{LS} + 2.0 V		
Output Current for TDD (Transmit Digital Data)					mA
CMOS Mode (V_{LS} = V_{DD}, V_{SS} = 0 V and is Digital Ground)					
	(V_{DD} = 5 V, V_{out} = 0.4 V)	I_{OL}	1.0	–	
	(V_{DD} = 10 V, V_{out} = 0.5 V)		3.0	–	
	(V_{DD} = 5 V, V_{out} = 4.5 V)	I_{OH}	−1.0	–	
	(V_{DD} = 10 V, V_{out} = 9.5 V)		−3.0	–	
TTL Mode ($V_{LS} \le V_{DD}-4.75$ V, V_{LS} = 0 V and is Digital Ground)	V_{OL} = 0.4 V	I_{OL}	1.6	–	
	V_{OH} = 2.4 V	I_{OH}	−0.2	–	

2

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, V_{LS} = V_{AG} = 0 V, V_{ref} = RSI = V_{SS} (Internal 3.15 V Reference), 0 dBm0 = 1.546 Vrms = +6 dBm @ 600 Ω, T_A = −40 to +85°C, TDC = RDC = CCI, TDE = RCE = MSI, Unless Otherwise Noted)

Characteristic	End to End		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz), T_A = 25°C, V_{DD} = 5 V, V_{SS} = 5 V	–	–	−0.30	+0.30	−0.30	+0.30	dB
Absolute Gain Variation With Temperature 0° to +70°C	–	–	–	±0.03	–	±0.03	dB
Absolute Gain Variation With Temperature −40° to +85°C	–	–	–	±0.1	–	±0.1	dB
Absolute Gain Variation With Power Supply (V_{DD} = 5 V, V_{SS} = 5 V, 5%)	–	–	–	±0.02	–	±0.02	dB
Gain vs Level Tone (Relative to −10 dBm0, 1.02 kHz) +3 to −40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
−40 to −50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
−50 to −55 dBm0	−1.6	+1.6	−0.8	+0.8	−0.8	+0.8	
Gain vs Level Pseudo Noise (A-Law Relative to −10 dBm0)							dB
CCITT G.714 −10 to −40 dBm0	–	–	−0.25	+0.25	−0.25	+0.25	
−40 to −50 dBm0	–	–	−0.30	+0.30	−0.30	+0.30	
−50 to −55 dBm0	–	–	−0.45	+0.45	−0.45	+0.45	
Total Distortion—1.02 kHz Tone (C-Message) 0 to −30 dBm0	35	–	35	–	36	–	dBC
−40 dBm0	29	–	29	–	30	–	
−45 dBm0	24	–	24	–	25	–	
Total Distortion With Pseudo Noise (A-Law), CCITT G.714 −3 dBm0	27.5	–	28	–	28.5	–	dB
−6 to −27 dBm0	35	–	35.5	–	36	–	
−34 dBm0	33.1	–	33.5	–	34.2	–	
−40 dBm0	28.2	–	28.5	–	30.0	–	
−55 dBm0	13.2	–	13.5	–	15.0	–	
Idle Channel Noise (For End-End and A/D, See Note 1)							
(Mu-Law, C-Message Weighted)	–	15	–	15	–	9	dBrnC0
(A-Law, Psophometric Weighted)	–	−69	–	−69	–	−78	dBmOp
Frequency Response (Relative to 1.02 kHz @ 0 dBm0) 15 to 60 Hz	–	−23	–	−23	–	0.15	dB
300 to 3000 Hz	−0.3	+0.3	−0.15	+0.15	−0.15	+0.15	
3400 Hz	−1.6	0	−0.8	0	−0.8	0	
4000 Hz	–	−28	–	−14	–	−14	
≥4600 Hz	–	−60	–	−32	–	−30	
Inband Spurious (1.02 kHz @ 0 dBm0, Transmit and RxO) 300 to 3000 Hz	–	–	–	−43	–	−43	dBm0
Out-of-Band Spurious at RxO (300-3400 Hz @ 0 dBm0 In)							dB
4600 to 7600 Hz	–	−30	–	–	–	−30	
7600 to 8400 Hz	–	−40	–	–	–	−40	
8400 to 100,000 Hz	–	−30	–	–	–	−30	
Idle Channel Noise Selective @ 8 kHz, Input = V_{AG}, 30 Hz Bandwidth	–	−70	–	–	–	−70	dBm0
Absolute Delay @ 1600 Hz (TDC = 2.048 MHz, TDE = 8 kHz)	–	–	–	310	–	180	μs
Group Delay Referenced to 1600 Hz (TDC = 2048 kHz, TDE = 8 kHz)							μs
500 to 600 Hz	–	–	–	200	−40	–	
600 to 800 Hz	–	–	–	140	−40	–	
800 to 1000 Hz	–	–	–	70	−30	–	
1000 to 1600 Hz	–	–	–	40	−20	–	
1600 to 2600 Hz	–	–	–	75	–	90	
2600 to 2800 Hz	–	–	–	110	–	120	
2800 to 3000 Hz	–	–	–	170	–	160	
Crosstalk of 1020 Hz @ 0 dBm0 From A/D or D/A (Note 2)	–	–	–	−75	–	−80	dB
Intermodulation Distortion of Two Frequencies of Amplitudes −4 to −21 dBm0 From the Range 300 to 3400 Hz	–	–	–	−41	–	−41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ −50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ −50 dBm0.

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} = -V_{SS} = 5$ V to 6 V $\pm 5\%$, $T_A = -40$ to $+85°C$)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	+Tx, −Tx (TxI for MC145500)	I_{in}	—	±0.01	±0.2	μA
AC Input Impedance to V_{AG} (1 kHz)	+Tx, −Tx (TxI for MC145500)	Z_{in}	5 0.1	10 0.2	— —	MΩ
Input Capacitance	+Tx, −Tx		—	—	10	pF
Input Offset Voltage of TxI Op Amp			—	< ±30	—	mV
Input Common Mode Voltage Range	+Tx, −Tx	V_{ICR}	$V_{SS}+1.0$	—	$V_{DD}-2.0$	V
Input Common Mode Rejection Ratio	+Tx, −Tx	CMRR	—	70	—	dB
TxI Unity Gain Bandwidth	$R_L \geq 10$ kΩ	BW_p	—	1000	—	kHz
TxI Open Loop Gain	$R_L \geq 10$ kΩ	A_{VOL}	—	75	—	dB
Equivalent Input Noise (C-Message) Between +Tx and −Tx, at TxI			—	−20	—	dBrnC0
Output Load Capacitance for TxI Op Amp			0	—	100	pF
Output Voltage Range TxI Op Amp, RxO or $\overline{RxO}$ $R_L = 10$ k to V_{AG} $R_L = 600$ Ω to V_{AG}		V_{out}	 $V_{SS}+0.8$ $V_{SS}+1.5$	 — —	 $V_{DD}-1.0$ $V_{DD}-1.5$	V
Output Current TxI, RxO, $\overline{RxO}$	$V_{SS}+1.5\ V \leq V_{out} \leq V_{DD}-1.5$ V		±5.5	—	—	mA
Output Impedance RxO, $\overline{RxO}$*	0 to 3.4 kHz	Z_{out}	—	3	—	Ω
Output Load Capacitance for RxO and $\overline{RxO}$*			0	—	200	pF
Output dc Offset Voltage Referenced to V_{AG} Pin	RxO $\overline{RxO}$*		— —	— —	±100 ±150	mV
Internal Gainsetting Resistors for RxG to RxO and $\overline{RxO}$			62	100	225	kΩ
External Reference Voltage Applied to V_{ref} (Referenced to V_{AG})			0.5	—	$V_{DD}-1.0$	V
V_{ref} Input Current			—	—	20	μA
V_{AG} Output Bias Voltage			— —	0.53 V_{DD} + 0.47 V_{SS}	— —	V
V_{AG} Output Current	Source Sink	I_{VAG}	0.4 10.0	— —	0.8 —	mA
Output Leakage Current During Power Down for the TxI Op Amp, V_{AG}, RxO, and $\overline{RxO}$			—	—	±30	μA
Positive Power Supply Rejection Ratio, 0-100 kHz @ 250 mV, C-Message Weighting	Transmit Receive		45 55	50 65	— —	dBC
Negative Power Supply Rejection Ratio, 0-100 kHz @ 250 mV, C-Message Weighting	Transmit Receive		50 50	55 60	— —	dBC

*Assumes that RxG is not connected for gain modifications to $\overline{RxO}$.

2

MODE CONTROL LOGIC (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = −40 to +85°C)

Characteristic	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode (TTL Logic Levels Referenced to V_{LS})	V_{SS}	–	$V_{DD}-4.0$	V
V_{LS} Voltage for CMOS Mode (CMOS Logic Levels of V_{SS} to V_{DD})	$V_{DD}-0.5$	–	V_{DD}	V
Mu/A Select Voltage				V
Mu-Law Mode	$V_{DD}-0.5$	–	V_{DD}	
Sign Magnitude Mode	$V_{AG}-0.5$	–	$V_{AG}+0.5$	
A-Law Mode	V_{SS}	–	$V_{SS}+0.5$	
RSI Voltage for Reference Select Input (MC145501 and MC145502)				V
3.78 V Mode	$V_{DD}-0.5$	–	V_{DD}	
2.5 V Mode	$V_{AG}-0.5$	–	$V_{AG}+0.5$	
3.15 V Mode	V_{SS}	–	$V_{SS}+0.5$	
V_{ref} Voltage for Internal or External Reference (MC145502 only)				V
Internal Reference Mode	V_{SS}	–	$V_{SS}+0.5$	
External Reference Mode	$V_{AG}+0.5$	–	$V_{DD}-1.0$	
Analog Test Mode Selection Frequency, MS = CCI (MC145500, MC145501, MC145502 only) See Pin Description; Test Modes	–	128	–	kHz

SWITCHING CHARACTERISTICS (V_{SS} to V_{DD} = 9.5 V to 12.6 V, T_A = −40 to +85°C, C_L = 150 pF CMOS or TTL Mode)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Rise Time	TDD	t_{TLH}	–	30	80	ns
Output Fall Time		t_{THL}	–	30	80	
Input Rise Time	TDE, TDC, RCE, RDC, DC, MSI, CCI	t_{TLH}	–	–	4	µs
Input Fall Time		t_{THL}	–	–	4	
Pulse Width	TDE Low, TDC, RCE, RDC, DC, MSI, CCI	t_w	100	–	–	ns
Data Clock Pulse Frequency	TDC, RDC, DC	f_{CL}	64	–	4096	kHz
CCI Clock Pulse Frequency (MSI = 8 kHz)		f_{CL1}	–	128	–	kHz
This Pin will Accept One of These Discrete Clock Frequencies and will		f_{CL2}	–	1536	–	
Compensate to Produce Internal Sequencing		f_{CL3}	–	1544	–	
		f_{CL4}	–	2048	–	
		f_{CL5}	–	2560	–	
Propagation Delay Time						ns
TDE Rising to TDD Low Impedance	TTL	t_{P1}	–	90	180	
	CMOS		–	90	150	
TDE Falling to TDD High Impedance	TTL	t_{P2}	–	–	55	
	CMOS		–	–	40	
TDC Rising Edge to TDD Data, During TDE High	TTL	t_{P3}	–	90	180	
	CMOS		–	90	150	
TDE Rising Edge to TDD Data, During TDC High	TTL	t_{P4}	–	90	180	
	CMOS		–	90	150	
TDC Falling Edge to TDE Rising Edge Setup Time		t_{su1}	20	–	–	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su2}	100	–	–	ns
TDE Falling Edge to TDC Rising Edge to Preserve the Next TDD Data		t_{su8}	20	–	–	ns
RDC Falling Edge to RCE Rising Edge Setup Time		t_{su3}	20	–	–	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su4}	100	–	–	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su5}	60	–	–	ns
CCI Falling Edge to MSI Rising Edge Setup Time		t_{su6}	20	–	–	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su7}	100	–	–	ns
RDD Hold Time from RDC Falling Edge		t_h	100	–	–	ns
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Capacitance			–	–	10	pF
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Current			–	±0.01	±0.2	µA
TDD Capacitance During High Impedance (TDE Low)			–	12	15	pF
TDD Input Current During High Impedance (TDE Low)			–	±0.1	±10.0	µA

DEVICE DESCRIPTIONS

A codec/filter is a device which is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "coder" for the A/D used to digitize voice, and "decoder" for the D/A used for reconstructing voice. A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13-bit A/D and D/A, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. With the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of 6-bits (sign + chord + four step bits) across a 42 dB dynamic range (7 chords above zero, by 6 dB per chord). There are two companding schemes used; Mu-255 Law specifically in North America, and A-Law specifically in Europe. These companding schemes are accepted world wide. The tables show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling which must be attenuated from the signal by a high-pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired inband signal which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145500 series PCM codec/filters have the codec, both presampling and reconstruction filters, a precision voltage reference on chip, and require no external components. There are five distinct versions of the Motorola MC145500 Series.

MC145500

The MC145500 PCM mono-circuit is intended for standard byte interleaved synchronous and asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle) 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies see MC145502 or MC145505.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM codec/filter. All other functions are described in the pin description.

MC145501

The MC145501 PCM codec/filter offers the same features and is for the same application as the MC145500, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 V_P, 3.15 V_P, or 3.78 V_P. The −Tx pin allows for external transmit gain adjust and simplifies the interface to the MC3419 SLIC. Otherwise, it is identical to MC145500.

MC145502

The MC145502 PCM codec/filter is the full feature 22-pin device. It is intended for use in applications requiring maximum flexiblity. The MC145502 contains all the features of the MC145500 and MC145501. The MC145502 is intended for bit interleaved or byte interleaved applications with data clock frequencies which are nonstandard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input, and the data clock inputs can be any frequency between 64 kHz and 4.096 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference. The RxG pin accommodates gain adjustments for the inverted analog output. All three pins of the input gain-setting operational amplifier are present which provide maximum flexibility for the analog interface.

MC145503

The MC145503 PCM mono-circuit is intended for standard byte interleaved synchronous or asynchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle), 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies see MC145502 or MC145505.) The internal reference is set for 3.15 volts peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 volts peak-to-peak. This is the +3 dBm0 level of the PCM codec/filter. The +Tx and −Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC145505

The MC145505 PCM mono-circuit is intended for byte interleaved synchronous applications. The MC145505 has all the features of the MC145503 but internally connects TDC and RDC (see pin description) to the DC pin. One of the five standard frequencies (listed above) should be applied to CCI. The data clock input (DC) can be any frequency between 64 kHz and 4.096 MHz.

PIN DESCRIPTION

DIGITAL

V_{LS}—Logic Level Select Input and TTL Digital Ground

V_{LS} controls the logic levels and digital ground reference for all digital inputs and the digital output. These devices can operate with logic levels from full supply (V_{SS} to V_{DD}) or with TTL logic levels using V_{LS} as digital ground. For $V_{LS}=V_{DD}$, all I/O is full supply (V_{SS} to V_{DD} swing) with CMOS switch points. For $V_{SS}<V_{LS}<(V_{DD}-4$ volts), all inputs and outputs are TTL compatible with V_{LS} being the digital ground. The pins controlled by V_{LS} are inputs MSI, CCI, TDE, TDC, RCE, RDC, RDD, $\overline{PDI}$, and output TDD.

MSI—Master Synchronization Input

MSI is used for determining the sample rate of the transmit side and as a time base for selecting the internal prescale divider for the convert clock input (CCI) pin. The MSI pin should be tied to an 8 kHz clock which may be a frame sync or system sync signal. MSI has no relation to transmit or receive data timing, except for determining the internal transmit strobe as described under the TDE pin description. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied internally to TDE in MC145503/05.)

CCI—Convert Clock Input

CCI is designed to accept five discrete clock frequencies. These are 128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The duty cycle of CCI is dictated by the minimum pulse width except for 128 kHz, which is used directly for internal sequencing and must have a 40 to 60% duty cycle. In asynchronous applications, CCI should be derived from transmit timing. (CCI is tied internally to TDC in MC145500/01/03.)

TDC—Transmit Data Clock Input

TDC can be any frequency from 64 kHz to 4.096 MHz, and is often tied to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and its rising edges produce successive data bits at TDD. TDE should be derived from this clock. (TDC and RDC are tied together internally in the MC145505 and are called DC.)

TDE—Transmit Data Enable Input

TDE serves three major functions. The first TDE rising edge following an MSI rising edge generates the internal transmit strobe which initiates an A/D conversion. The internal transmit strobe also transfers a new PCM data word into the transmit shift register (sign bit first) ready to be output at TDD. The TDE pin is the high impedance control for the transmit digital data (TDD) output. As long as this pin is high, the TDD output stays low impedance. This pin also enables the output shift register for clocking out the 8-bit serial PCM word. The logical AND of the TDE pin with the TDC pin clocks out a new data bit at TDD. TDE should be held high for eight consecutive TDC cycles to clock out a complete PCM word for byte interleaved applications. The transmit shift register feeds back on itself to allow multiple reads of the transmit data. If the PCM word is clocked out once per frame in a byte interleaved system, the MSI pin function is transparent and may be connected to TDE.

The TDE pin may be cycled during a PCM word for bit interleaved applications. TDE controls both the high impedance state of the TDD output and the internal shift clock. TDE must fall before TDC rises (t_{su8}) to ensure integrity of the next data bit. There must be at least two TDC falling edges between the last TDE rising edge of one frame and the first TDE rising edge of the next frame. MSI must be available separate from TDE for bit interleaved applications.

TDD—Transmit Digital Data Output

The output levels at this pin are controlled by the V_{LS} pin. For V_{LS} connected to V_{DD}, the output levels are from V_{SS} to V_{DD}. For a voltage of V_{LS} between $V_{DD}-4$ V and V_{SS}, the output levels are TTL compatible with V_{LS} being the digital ground supply. The TDD pin is three-state output controlled by the TDE pin. The timing of this pin is controlled by TDC and TDE. When in TTL mode, this output may be made high-speed CMOS compatible using a pullup resistor. The data format (Mu-Law, A-Law, or sign magnitude) is controlled by the Mu/A pin.

RDC—Receive Data Clock Input

RDC can be any frequency from 64 kHz to 4.096 MHz. This pin is often tied to the TDC pin for applications that can use a common clock for both transmit and receive data transfers. The receive shift register is controlled by the receive clock enable (RCE) pin to clock data into the receive digital data (RDD) pin on falling RDC edges. These three signals can be asynchronous with all other digital pins. The RDC input is internally tied to the TDC input on the MC145505 and called DC.

RCE—Receive Clock Enable Input

The rising edge of RCE should identify the sign bit of a receive PCM word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive PCM word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In asynchronous applications with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive PCM words may be decoded and analog summed each transmit frame to allow on chip conferencing. The two PCM words should be clocked in as two single PCM words, a minimum of 31.25 μs apart, with a receive data clock of 512 kHz or faster.

RDD—Receive Digital Data Input

RDD is the receive digital data input. The timing for this pin is controlled by RDC and RCE. The data format is determined by the Mu/A pin.

Mu/A Select

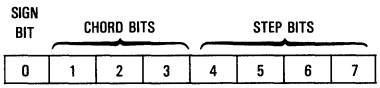
This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu255 Companding D3 Data Format with Zero Code Suppress

Mu/A = V_{AG}; Mu255 Companding with Sign Magnitude Data Format

Mu/A = V_{SS}; A-law Companding with CCITT Data Format Bit Inversions

CODE	SIGN/ MAGNITUDE	Mu-LAW	A-LAW (CCITT)
+ FULL SCALE	1111 1111	1000 0000	1010 1010
+ ZERO	1000 0000	1111 1111	1101 0101
− ZERO	0000 0000	0111 1111	0101 0101
− FULL SCALE	0111 1111	0000 0010	0010 1010



NOTE: Starting from sign magnitude, to change format:

To Mu-Law—

MSB is unchanged (sign)

Invert remaining seven bits

If code is 0000 0000, change to 0000 0010 (for zero code suppression)

To A-Law—

MSB is unchanged (sign)

Invert odd numbered bits

Ignore zero code suppression

$\overline{PDI}$—Power Down Input

The power down input disables the bias circuitry and gates off all clock inputs. This puts the V_{AG}, TxI, RxO, $\overline{RxO}$, and TDD outputs into a high impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI}$ is a low logic level. The circuit operates normally with $\overline{PDI} = V_{DD}$ or with a logic high as defined by connection at V_{LS}. TDD will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DC—Data Clock Input

DC—in the MC145505, TDC and RDC are internally connected to this pin.

ANALOG

V_{AG}—Analog Ground Input/Output Pin

V_{AG} is the analog ground power supply input/output. All analog signals into and out of the device use this as their ground reference. Each version of the MC145500 PCM codec/filter family can provide its own analog ground supply internally. The dc voltage of this internal supply is 6% positive of the midway between V_{DD} and V_{SS}. This supply can sink more than 8 mA but has a current source limited to 400 μA. The output of this supply is internally connected to the analog ground input of the part. The node where this supply and the analog ground are connected is brought out to the V_{AG} pin. In symmetric dual supply systems (±5, ±6, etc.), V_{AG} may be externally tied to the system analog ground supply. When RxO or $\overline{RxO}$ drive low impedance loads tied to V_{AG}, a pullup resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground. All analog signals for the part are referenced to V_{AG}, including noise, therefore, decoupling capacitors (0.1 μF) should be used from V_{DD} to V_{AG} and V_{SS} to V_{AG}.

V_{ref}—Positive Voltage Reference Input (MC145502 Only)

The V_{ref} pin allows an external reference voltage to be used for the A/D and D/A conversions. If V_{ref} is tied to V_{SS}, the internal reference is selected. If $V_{ref} > V_{AG}$, then the external mode is selected and the voltage applied to V_{ref} is used for generating the internal converter reference voltage. In either internal or external reference mode, the actual voltage used for conversion is multiplied by the ratio selected by the RSI pin. The RSI pin circuitry is explained under its pin description below. Both the internal and external references are inverted within the PCM codec/filter for negative input voltages such that only one reference is required.

External Mode—In the external reference mode ($V_{ref} > V_{AG}$), a 2.5 volt reference like the MC1403 may be connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref} pins and V_{AG} pins from different codec/filters. In special applications, the external reference voltage may be between 0.5 and 5 volts. However, the reference voltage gain selection circuitry associated with RSI must be considered to arrive at the desired codec/filter gain.

Internal Mode—In the internal reference mode ($V_{ref} = V_{SS}$), an internal 2.5 volt reference supplies the reference voltage for the RSI circuitry. The V_{ref} pin is functionally connected to V_{SS} for the MC145500, MC145501, MC145503, and MC145505 pinouts.

RSI—Reference Select Input (MC145501/02 Only)

The RSI input allows the selection of three different overload or full scale A/D and D/A converter reference voltages independent of the internal or external reference mode. The RSI pin is a digital input that senses three different logic states; V_{SS}, V_{AG}, and V_{DD}. For RSI = V_{AG}, the reference voltage is used directly for the converters. The internal reference is 2.5 volts. For RSI = V_{SS}, the reference voltage is multiplied by the ratio of 1.26, which results in an internal converter reference of 3.15 volts. For RSI = V_{DD}, the reference voltage is multiplied by 1.51, which results in an internal converter reference of 3.78 volts. The device requires a minimum of 1.0 volt of headroom between the internal converter reference to V_{DD}. V_{SS} has this same absolute valued minimum, also measured from V_{AG} pin. The various modes of operation are summarized in the table below. The RSI pin is functionally connected to V_{SS} for the MC145500, MC145503, and MC145505 pinouts.

RxO, $\overline{RxO}$—Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak-to-peak signal described with the reference. If a 3.15 volt reference is used with RSI tied to V_{AG}

2

and a +3 dBm0 sine wave is decoded, the RxO output will be a 6.3 volt peak-to-peak signal. $\overline{\text{RxO}}$ will also have an inverted signal output of 6.3 volt peak-to-peak. External loads may be connected from RxO to $\overline{\text{RxO}}$ for a 6 dB push-pull signal gain or from either RxO or $\overline{\text{RxO}}$ to V_{AG}. With a 3.15 volt reference each output will drive 600 Ω to +9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to +9 dBm.

RxG—Receive Output Gain Adjust (MC145502 Only)

The purpose of the RxG pin is to allow external receive gain adjustment for the $\overline{\text{RxO}}$ pin. If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{\text{RxO}}$. Thus the push-pull gain to a load from RxO to $\overline{\text{RxO}}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{\text{RxO}}$ (RG), the gain of $\overline{\text{RxO}}$ can be set differently from inverting unity. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{\text{RxO}}$ gain is approximately equal to minus RG/RI. The actual gain is determined by taking into account the internal resistors which will be in parallel to these external resistors. The internal resistors have a large tolerance, but they match each other very closely. This matching tends to minimize the affects of their tolerance on external gain configurations. The circuit for RxG and $\overline{\text{RxO}}$ is shown in the block diagram.

TxI—Transmit Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC145501/02/03/05. The input impedance is greater than 100 k to V_{AG} in the MC145500. The TxI input has an internal gain of 1.0, such that a +3 dBm0 signal at TxI corresponds to the peak converter reference voltage as described in the V_{ref} and RSI pin descriptions. For 3.15 volt reference, the +3 dBm0 input should be 6.3 volts peak-to-peak.

+Tx-Positive Tx Amplifier Input (MC145502/03/05 Only)
−Tx-Negative Tx Amplifier Input (MC145501/02/03/05 Only)

The TxI pin is the input to the transmit band-pass filter. If +Tx or −Tx are available, then there is an internal amplifier preceding the filter whose pins are +Tx, −Tx, and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 kΩ. If +Tx is not available, it is internally tied to V_{AG}. If −Tx and +Tx are not available, the TxI is a unity gain high impedance input.

Power Supplies

V_{DD}—Most Positive Supply V_{DD} is typically 5 to 12 volts.

V_{SS}—Most Negative Supply. V_{SS} is typically 10 to 12 volts negative of V_{DD}.

For a ±5 volt dual-supply system, the typical power supply configuration is V_{DD} = +5 V, V_{SS} = −5 V, V_{LS} = 0 V (digital ground accommodating TTL logic levels), and V_{AG} = 0 V being tied to system analog ground.

For single-supply applications, typical power supply configurations include:

V_{DD} = 10 V to 12 V
V_{SS} = 0 V
V_{AG} generates a mid supply voltage for referencing all analog signals.
V_{LS} controls the logic levels. This pin should be connected to V_{DD} for CMOS logic levels from V_{SS} to V_{DD}. This pin should be connected to digital ground for true TTL logic levels referenced to V_{LS}.

Testing Considerations (MC145500/01/02 Only)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the A/D (the output of the Tx filter) is available at the $\overline{\text{PDI}}$ pin. This input is direct coupled to the A/D side of the codec. The A/D is a differential design, this results in the gain of this input being effectively attenuated by half. If monitored with a high-impedance buffer, the output of the Tx low-pass filter can also be measured at the $\overline{\text{PDI}}$ pin. This test mode allows independent evaluation of the transmit low-pass filter and A/D side of the codec. The transmit and receive channels of these devices are tested with the codec/filter fully functional.

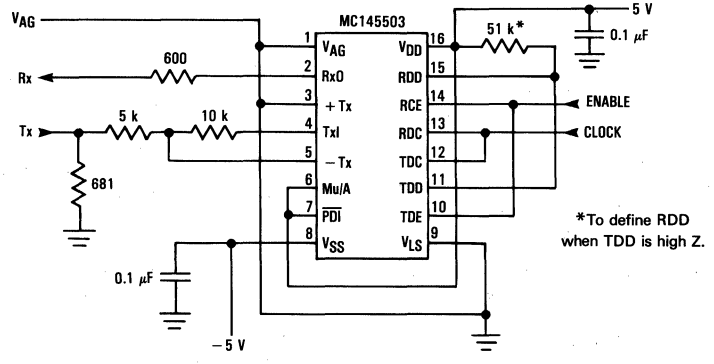


Figure 1. Test Circuit

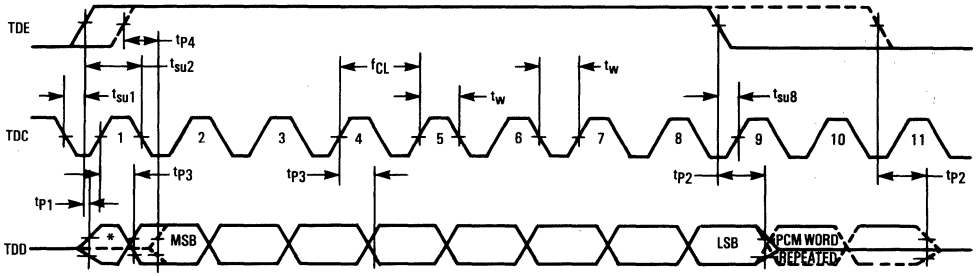
Table 1. Options Available by Pin Selection

RSI* Pin Level	V_{ref}* Pin Level	Peak-to-Peak Overload Voltage (TxI, RxO)
V_{DD}	V_{SS}	7.56 Vpp
V_{DD}	$V_{AG}+V_{EXT}$	$(3.02 \times V_{EXT})$ Vpp
V_{AG}	V_{SS}	5 Vpp
V_{AG}	$V_{AG}+V_{EXT}$	$(2 \times V_{EXT})$ Vpp
V_{SS}	V_{SS}	6.3 Vpp
V_{SS}	$V_{AG}+V_{EXT}$	$(2.52 \times V_{EXT})$Vpp

*On MC145500/03/05, RSI and V_{ref} internally to V_{SS}. On MC145501, V_{ref} tied internally to V_{SS}.

Table 2. Summary of Operation Conditions User Programmed Through Pins V_{DD}, V_{AG}, and V_{SS}

Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu-Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu-Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A-Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up



*Data output during this time will vary depending on TDC rate and TDE timing.

Figure 2. Transmit Timing Diagram

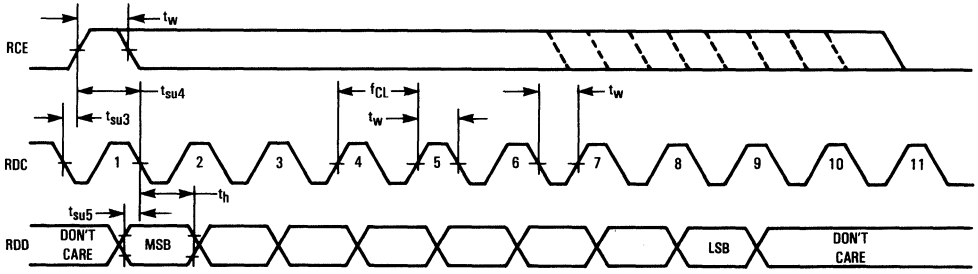


Figure 3. Receive Timing Diagram

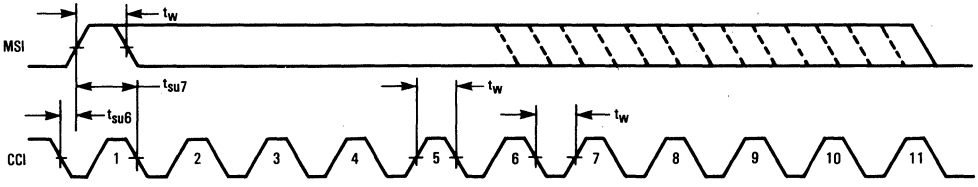


Figure 4. MSI/CCI Timing Diagram

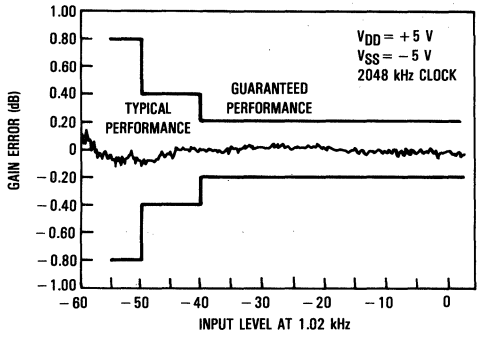


Figure 5. MC145502 Gain vs Level Mu-Law Transmit

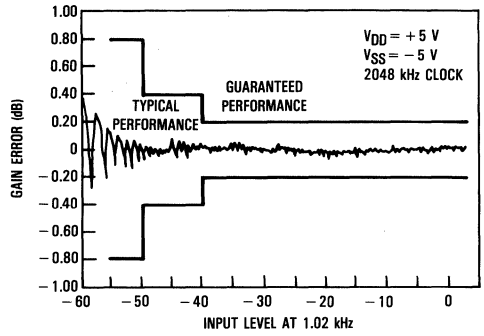


Figure 6. MC145502 Gain vs Level Mu-Law Receive

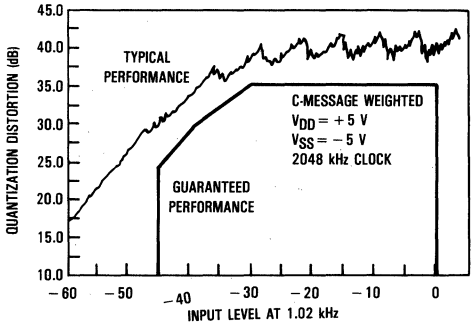


Figure 7. MC145502
Quantization Distortion Mu-Law Transmit

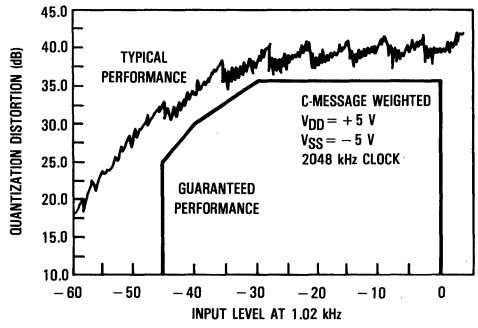


Figure 8. MC145502
Quantization Distortion Mu-Law Receive

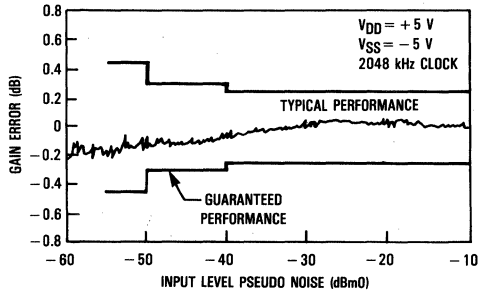


Figure 9. MC145502 Gain vs Level A-Law Transmit

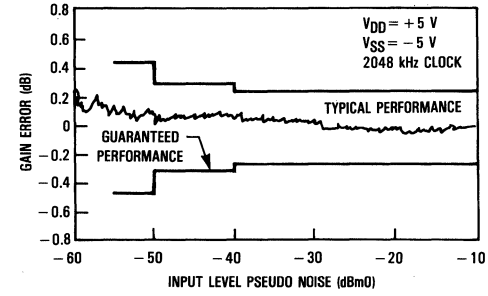


Figure 10. MC145502 Gain vs Level A-Law Receive

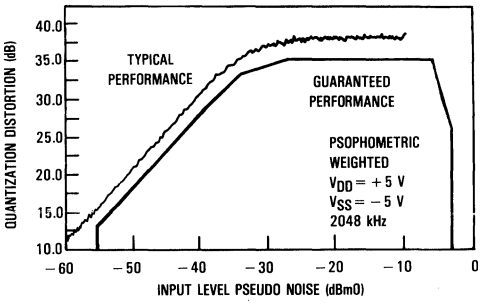


Figure 11. MC145502
Quantization Distortion A-Law Transmit

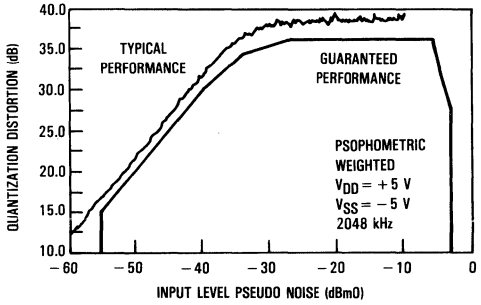


Figure 12. MC145502
Quantization Distortion A-Law Receive

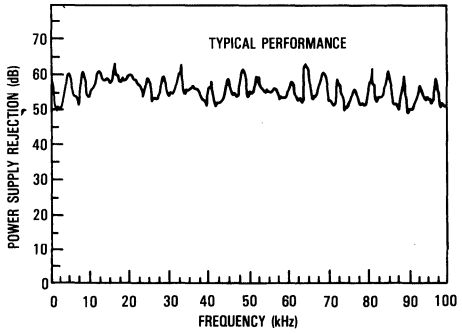


Figure 13. MC145502 Power Supply Rejection Ratio Positive Transmit VAC = 250 mVrms, C-Message Weighted

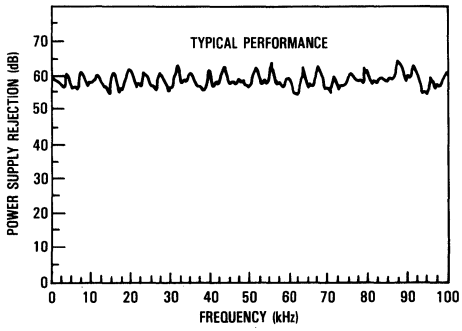


Figure 14. MC145502 Power Supply Rejection Ratio Negative Transmit VAC = 250 mVrms, C-Message Weighted

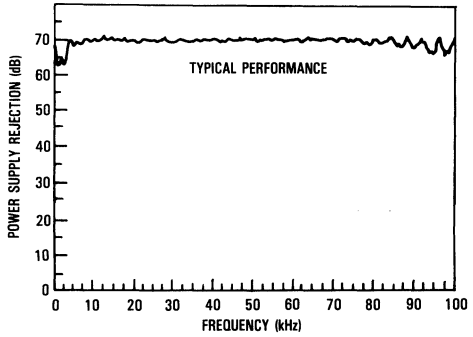


Figure 15. MC145502 Power Supply Rejection Ratio Positive Receive VAC = 250 mVrms, C-Message Weighted

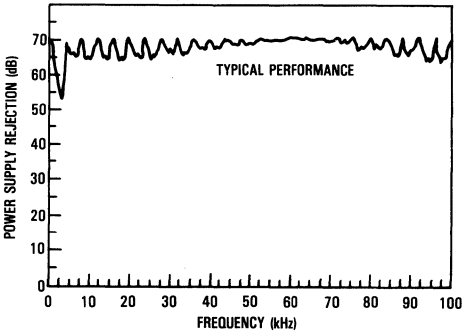


Figure 16. MC145502 Power Supply Rejection Ratio Negative Receive VAC = 250 mVrms, C-Message Weighted

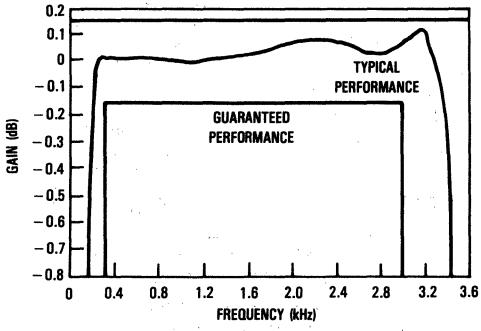


Figure 17. MC145502
Passband Filter Response Transmit

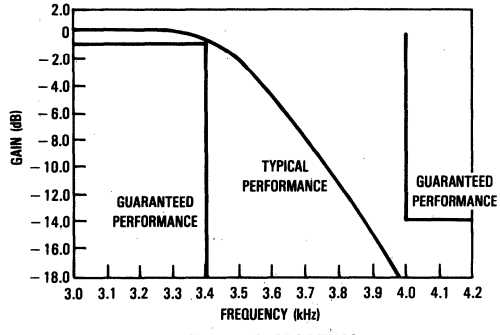


Figure 18. MC145502
Low-Pass Filter Response Transmit

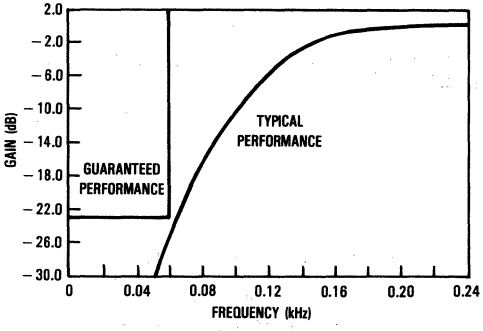


Figure 19. MC145502
High-Pass Filter Response Transmit

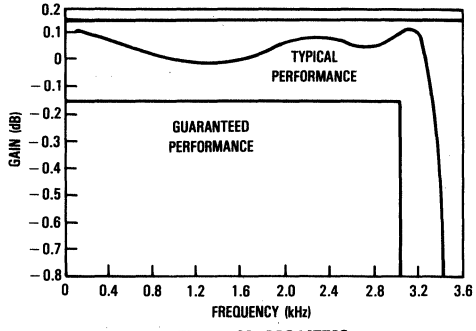


Figure 20. MC145502
Passband Filter Response Receive

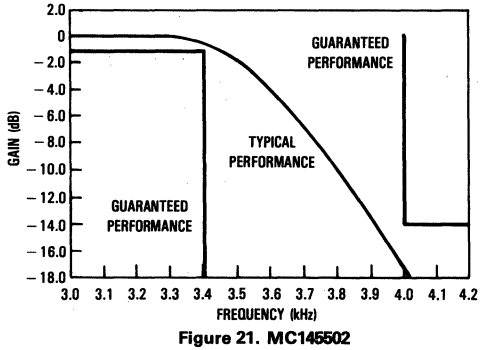


Figure 21. MC145502
Low-Pass Filter Response Receive

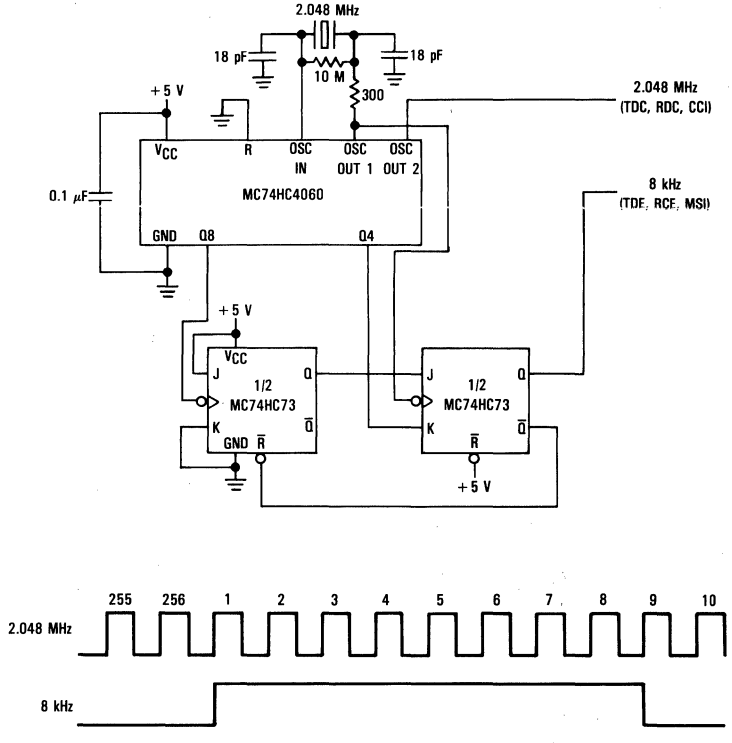
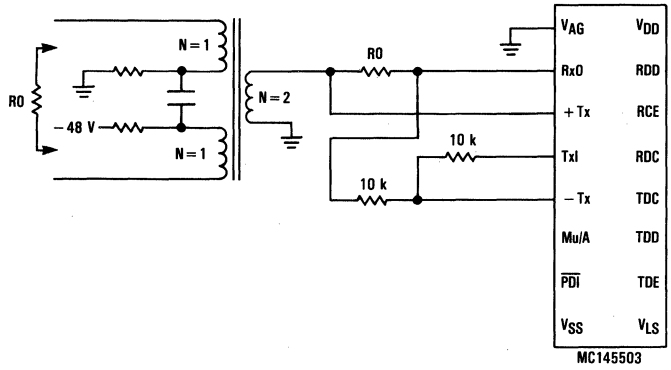
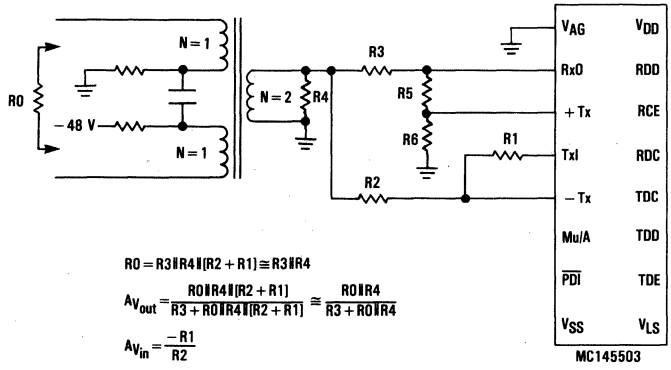


Figure 22. Simple Clock Circuit for Driving MC145500/01/02/03/05 Codec/Filters



(a) SIMPLIFIED TRANSFORMER HYBRID USING MC145503



$$RO = R3 \| R4 \| [R2 + R1] \cong R3 \| R4$$

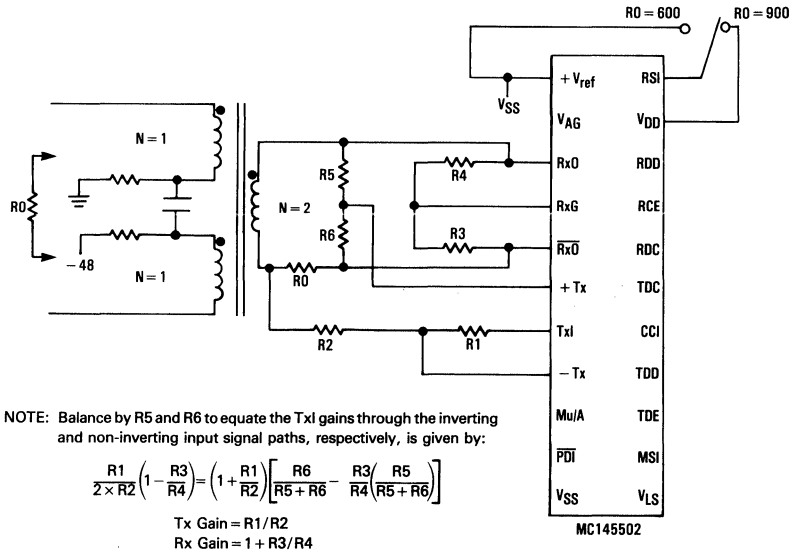
$$A_{V_{out}} = \frac{RO \| R4 \| [R2 + R1]}{R3 + RO \| R4 \| [R2 + R1]} \cong \frac{RO \| R4}{R3 + RO \| R4}$$

$$A_{V_{in}} = \frac{-R1}{R2}$$

NOTE: Hybrid Balance by R5 and R6 to equate the RxO signal gain at TxI through the inverting and non-inverting signal paths.

(b) UNIVERSAL TRANSFORMER HYBRID USING MC145503

Figure 23. Hybrid Interfaces to the MC145503 PCM Codec/Filter Mono-Circuit

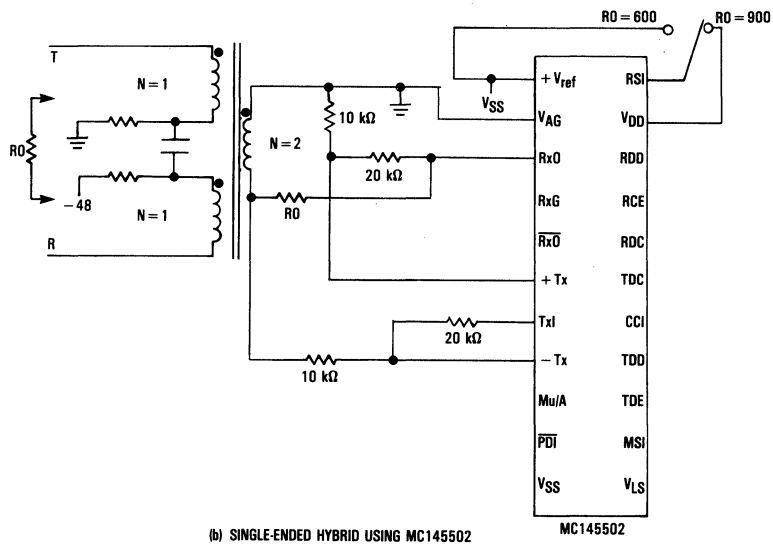


NOTE: Balance by R5 and R6 to equate the TxI gains through the inverting and non-inverting input signal paths, respectively, is given by:

$$\frac{R1}{2\times R2}\left(1-\frac{R3}{R4}\right)=\left(1+\frac{R1}{R2}\right)\left[\frac{R6}{R5+R6}-\frac{R3}{R4}\left(\frac{R5}{R5+R6}\right)\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≅ 10 k
Adjust Rx Gain with R3
Adjust Tx Gain with R1

(a) UNIVERSAL TRANSFORMER HYBRID USING MC145502



(b) SINGLE-ENDED HYBRID USING MC145502

Figure 24. Hybrid Interfaces to the MC145502 PCM Codec/Filter Mono-Circuit

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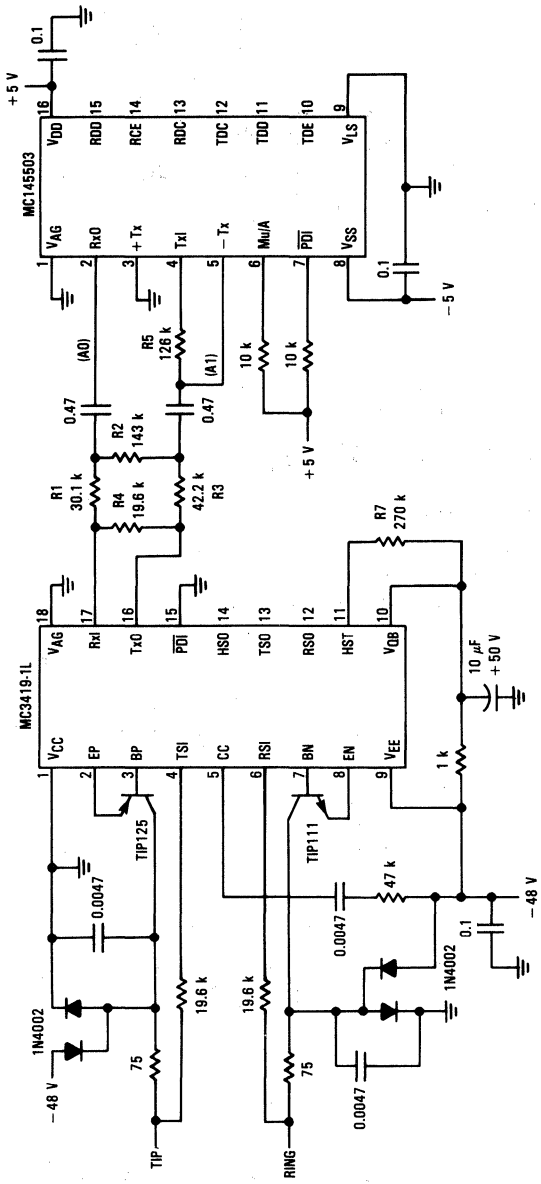
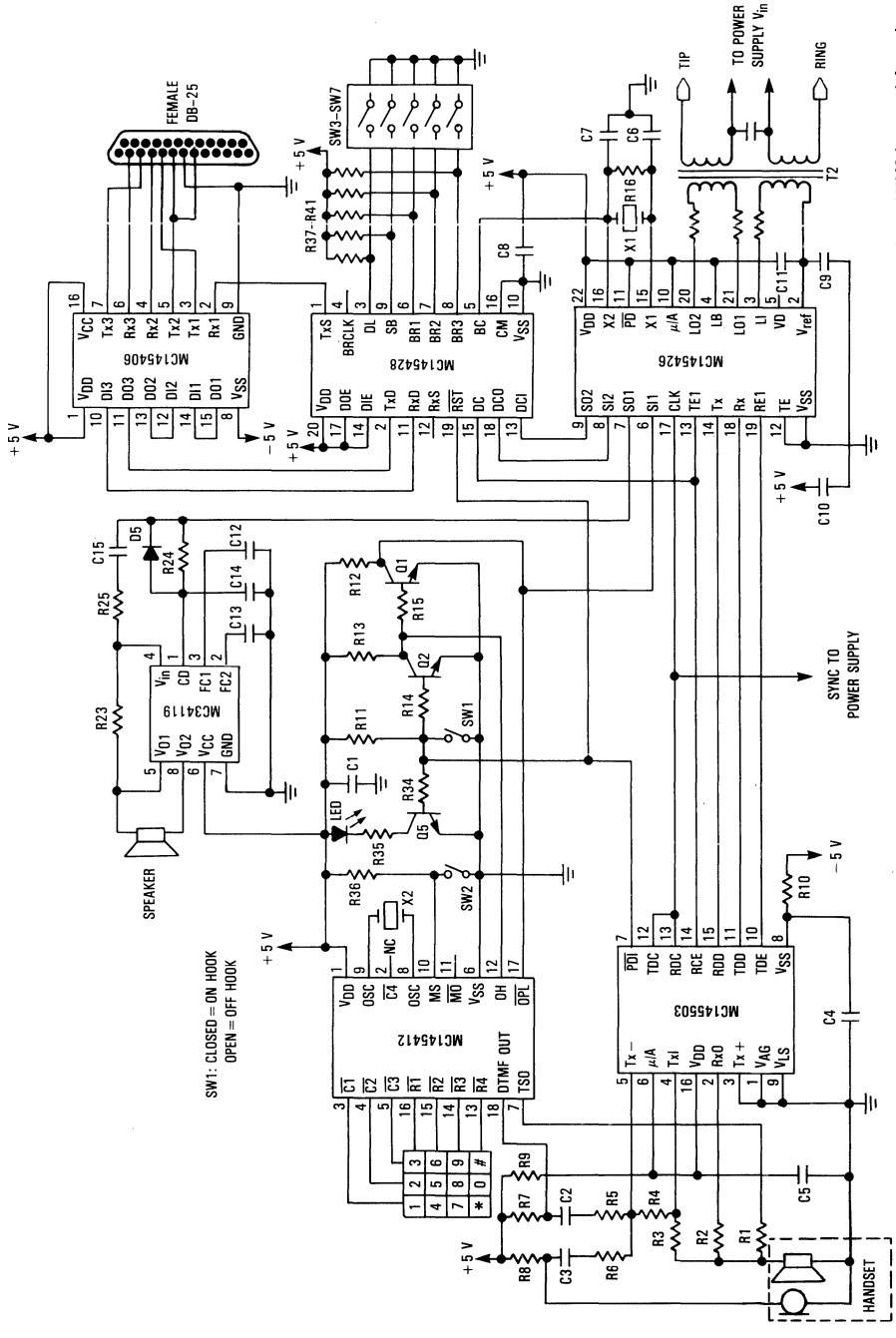


Figure 25. A Complete Single Party Channel Unit Using MC3419 SLIC and MC145503 PCM Mono-Circuit



Refer to AN968 for more information.

Figure 26. Digital Telephone Schematic

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Table 3. Mu-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256	7903	1	0	0	0	0	0	0	0	8031
			:					:				:
			4319	1	0	0	0	1	1	1	1	4191
			4063									
7	16	128	:					:				:
			2143	1	0	0	1	1	1	1	1	2079
			2015									
6	16	64	:					:				:
			1055	1	0	1	0	1	1	1	1	1023
			991									
5	16	32	:					:				:
			511	1	0	1	1	1	1	1	1	495
			479									
4	16	16	:					:				:
			239	1	1	0	0	1	1	1	1	231
			223									
3	16	8	:					:				:
			103	1	1	0	1	1	1	1	1	99
			95									
2	16	4	:					:				:
			35	1	1	1	0	1	1	1	1	33
			31									
1	15	2	:					:				:
			3	1	1	1	1	1	1	1	0	2
	1	1	1	1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
				1	0	1	0	1	0	1	0	4032
			3968									
7	16	128	:					:				:
			2176									
				1	0	1	0	0	1	0	1	2112
			2048									
			:					:				:
6	16	64	1088									
				1	0	1	1	0	1	0	1	1056
			1024									
			:					:				:
5	16	32	544									
				1	0	0	0	0	1	0	1	528
			512									
			:					:				:
4	16	16	272									
				1	0	0	1	0	1	0	1	264
			256									
			:					:				:
3	16	8	136									
				1	1	1	0	0	1	0	1	132
			128									
			:					:				:
2	16	4	68									
				1	1	1	1	0	1	0	1	66
			64									
			:					:				:
1	32	2	2									
				1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.

MC145532

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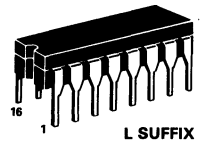
Product Preview

ADPCM Transcoder

Conforms to G.721 and T1.301-1987

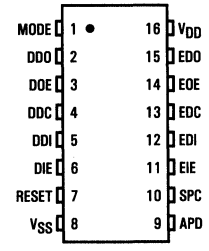
The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low-cost, full-duplex, single-channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721 (Geneva 1986)
- Complies with the American National Standard (T1.301-1987)
- Full-Duplex, Single-Channel Operation
- μ-Law or A-Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with Any Member of Motorola's PCM Codec/Filter Mono-Circuit Family or Other Industry Standard Codec
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power Down Capability for Low Current Consumption
- The Reset State, an Option Specified in the Standards, is Automatically Initiated When the RESET Pin is Released
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5-Volt Power Supply
- 16-Pin Package

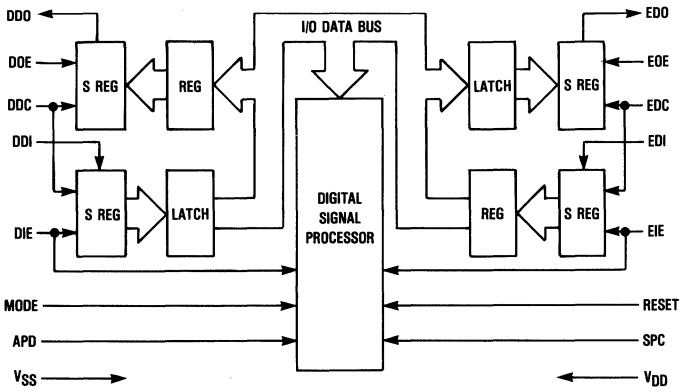


L SUFFIX
CERAMIC
CASE 620

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

DEVICE DESCRIPTION

An Adaptive Differential PCM (ADPCM) transcoder is used to reduce the data rate required to transmit a PCM encoded voice signal while maintaining the voice fidelity and intelligibility of the PCM signal.

The transcoder is used on 64 kbps data streams which represent either voice or voice band data signals that have been digitized by a codec (e.g., MC145557). The transcoder uses a filter to attempt to predict the next PCM input value based on previous PCM input values. The error between the predicted and the true PCM input value is the information that is sent to the other end of the line. Hence the word differential, since the ADPCM data stream is the difference between the true PCM input value and the predicted value. The term "adaptive" applies to the filter that is performing the prediction. It is adaptive in that its transfer function changes based on the PCM input data. That is, it adapts to the statistics of the signals presented to it.

PIN DESCRIPTION

ENCODER INPUT

EDI—Encoder Data Input (Pin 12)

PCM data to be encoded are applied to this input pin which operates synchronously with EDC and EIE to enter the data in a serial format.

EDC—Encoder Data Clock (Pin 13)

Data applied to EDI are latched into the transcoder on a falling edge of EDC and data are output from EDO on a rising edge of this input pin. The frequency of EDC may be as low as 64 kHz or as high as 5.12 MHz.

EIE—Encoder Input Enable (Pin 11)

The beginning of a new PCM word is indicated to the transcoder by a rising edge applied to this input. The frequency of EIE may not exceed 8 kHz.

ENCODER OUTPUT

EDO—Encoder Data Output (Pin 15)

ADPCM data are available in a serial format from this output which operates synchronously with EDC and EOE. EDO is a three-state output which remains in a high impedance state, except when presenting data.

EOE—Encoder Output Enable (Pin 14)

Each ADPCM word is requested by a rising edge on this input which causes the EDO pin to provide the data when clocked by EDC. One EOE must occur for each EIE.

DECODER INPUT

DDI—Decoder Data Input (Pin 5)

ADPCM data to be decoded are applied to this input pin which operates in conjunction with DDC and DIE to enter the data in a serial format.

DDC—Decoder Data Clock (Pin 4)

Data applied to DDI are latched into the transcoder on the falling edge of DDC and data are output from DDO on the rising edge of DDC. The frequency of DDC may be as low as 64 kHz or as high as 5.12 MHz.

DIE—Decoder Input Enable (Pin 6)

The beginning of a new ADPCM word is indicated by a rising edge applied to this input. Data are serially clocked into DDI on the subsequent falling edges of DDC following the DIE rising edge. The frequency of DIE may not exceed 8 kHz.

DECODER OUTPUT

DDO—Decoder Data Output (Pin 2)

PCM data are available in a serial format from this output which operates in conjunction with DDC and DOE. DDO is a three-state output which remains at a high impedance state except when presenting data.

DOE—Decoder Output Enable (Pin 3)

Each ADPCM word is requested by a rising edge on this input which causes the EDO pin to provide the data when clocked by EDC. One DOE must occur for each DIE.

CONTEXT

MODE—Mode Select (Pin 1)

A logic "zero" applied to this input makes the transcoder compatible with μ-255 companding and D3 data format. A logic "one" applied to this pin makes the transcoder compatible with A-law companding with even bit inversion data format.

SPC—Signal Processor Clock (Pin 10)

This input requires a 20.48 MHz clock signal which is used as the digital signal processor master clock. This pin has a CMOS compatible input.

RESET (Pin 7)

A logic "zero" applied to this input forces the transcoder into a low power dissipation mode. A rising edge on this pin causes power to be restored and the optional transcoder RESET state (specified in the standards) to be forced. Valid data is available at the output pins four input enables after a rising edge on this pin. This pin has a CMOS compatible input.

APD—Absolute Power Down (Pin 9)

A logic "one" applied to this input forces the transcoder into a power saving mode. This pin has a CMOS compatible input.

POWER SUPPLY

V_{DD}—Positive Power Supply (Pin 16)

The most positive power supply pin, normally 5 volts.

V_{SS}—Negative Power Supply (Pin 8)

The most negative power supply pin, normally 0 volts.

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FUNCTIONAL DESCRIPTION

ENCODING/DECODING RATES

The MC145532 allows for the encoding and decoding of data at one of four rates on a sample by sample basis. Each data sample which is provided to the part is accompanied by an indication of the rate at which it is to be encoded or decoded. The width of the enable pulse determines the encoding/decoding rate chosen for each sample.

The 64 kbps rate allows for PCM data to be passed directly through the part. The 32 kbps rate is either the G.721 or the T1.301-1987 standard depending on the state of the mode pin. The 24 kbps encoding rate is a T1 draft standard (T1Y1/87-040). The 16 kbps rate is a modified quantizer from the 32 kbps technique and is not a standard.

TIMING

Figures 1 through 8 show the timing of the input and output pins. The MC145532 determines the mode of the timing signals, either short or long frame, for each enable, independent of the mode of any previous enables. A transition from short frame to long frame mode or vice versa will cause at least one frame of data to be destroyed. Each of the four sets of I/O pins determines its mode independent of the other sets. Thus the encoder input could be operating with long frame timing and the encoder output could be operating with short frame timing. Note that the short frame timing on the input enables can only be used with the 32 kbps transcoding rate. The number of data clock falling edges enclosed by the input enable line (EIE or DIE) determines both the short frame or long frame mode and the transcoding rate. The mode of the input or output is determined each frame. In all modes, the data is captured by the MC145532 on the falling edge of either EDC or DDC.

ENCODER INPUT—SHORT FRAME

Figure 1 shows the timing of the encoder data clock (EDC), the encoder input enable (EIE), and the encoder data input (EDI) pins in short frame operation.

The determination of short frame mode is made by the MC145532 based on observing one falling EDC edge while EIE is high. Note that only a 32 kbps encoding rate can be specified when using short frame mode on the encoder input.

ENCODER INPUT—LONG FRAME

Figure 2 shows the clock, enable, and data signals for the encoder input in long frame mode. In this mode the data is captured by the MC145532 on the falling edge of EDC.

The determination of the encoding rate is made based on the number of falling EDC edges seen by the MC145532 while EIE is high. Four edges implies a 32 kbps encoding rate, three edges implies a 24 kbps encoding rate, two edges implies a 16 kbps rate, and from five to eight inclusive imply a 64 kbps rate. The encoding rate may be changed on a frame by frame basis. The encoded word is available at EDO (via EOE and EDC) from 250 μs to 375 μs after it is requested.

ENCODER OUTPUT—SHORT FRAME

Figure 3 shows the timing of the encoder output in short frame mode. The length of the LSB is always one half of an EDC cycle.

The EDO will provide the correct number of bits for the encoding rate which was selected for this frame of data on the encoder input pins. The data is loaded into the MC145532 during one frame, encoded on the next frame, and read during the next frame.

ENCODER OUTPUT—LONG FRAME

Figure 4 shows the timing of the encoder output in long frame mode. The enable must be wider than two falling edges of the EDC to be in long frame mode. If the enable falls before the correct number of bits have been presented to the output (EDO), the transcoder will complete the presentation of the bits to the output with the LSB being one half of an EDC period wide. If the enable falls after the one half EDC period of the LSB, then the LSB will be extended up to the full EDC clock period and the subsequent data will be a recirculation of the previous data which repeats until the enable pin falls. This is shown on the second enable for the 16 kbps encoding rate example in Figure 4.

DECODER INPUT—SHORT FRAME

Figure 5 shows the timing of the decoder data clock, the decoder input enable, and the decoder data input pins in short frame operation. Note that in this mode only a 32 kbps decoding rate can be selected.

DECODER INPUT—LONG FRAME

Figure 6 shows the clock, enable, and data signals for the decoder input in long frame mode.

The determination of the decoding rate is made based on the number of falling DDC edges seen by the MC145532 while DIE is high. Four edges implies a 32 kbps decoding rate, three edges implies a 24 kbps decoding rate, two edges implies a 16 kbps rate, and from five to eight edges inclusive imply a 64 kbps rate. The decoding rate may be changed on a frame by frame basis.

DECODER OUTPUT—SHORT FRAME

Figure 7 shows the timing of the decoder output in short frame mode.

The DDO will provide the correct number of bits for the decoding rate which was selected for this frame of data on the decoder input pins. The data is loaded into the MC145532 during one frame, decoded on the next frame, and read during the next frame.

DECODER OUTPUT—LONG FRAME

Figure 8 shows the timing of the decoder output in long frame mode. Note that at least eight bits are presented to the output provided that at least two falling edges of DDC are seen while DOE is high. The enable can be used to extend the LSB to a full DDC period and/or cause the eight bits of data to be recirculated to the output pin until the enable falls.

STANDARDS INFORMATION

The following standards apply to the MC145532:

T1.301-1987—32 kbps APDCM
T1.303-1988—24 and 40 kbps ADPCM.

For copies, contact the Exchange Carriers Standards Association, 5430 Grosvenor Lane, Bethesda, MD 20814-2122, phone (301) 564-4505.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +7.0	V
Voltage, Any Pin to V_{SS}	V	−0.5 to V_{DD}+0.5	V
DC Current, Any Pin	I_{in}	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{SS} or V_{DD}).

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RECOMMENDED OPERATING CONDITIONS (T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.50	5.50	V
Power Dissipation	P_D	–	0.28	W

DIGITAL CHARACTERISTICS (V_{DD}=5.0 V, T_A = −40 to +85°C)

Parameter		Symbol	Min	Max	Unit
High Level Input Voltage	Mode, DDO, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE, EDO	V_{IH}	2.0	–	V
Low Level Input Voltage	Mode, DDO, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE, EDO	V_{IL}	–	0.8	V
High Level Input Voltage	RESET, APD, SPC	V_{IH}	0.7 V_{DD}	–	V
Low Level Input Voltage	RESET, APD, SPC	V_{IL}	–	0.3 V_{DD}	V
Input Current		I_{in}	–	±1.0	μA
Input Capacitance		C_{in}	–	10	pF
High Level Output Voltage (I_{OH} = −2.0 mA)		V_{OH}	4.6	–	V
Low Level Output Voltage (I_{OL} = 2.0 mA)		V_{OL}	–	0.4	V
Output Leakage Current (V_{DD} = 5.5 V)		I_{lkg}	–	±5.0	μA

SWITCHING CHARACTERISTICS (V_{DD}=5.0 V, T_A = −40 to +85°C)

Parameter	Min	Max	Unit
SPC Frequency	20.48	–	MHz
SPC Duty Cycle	45	55	%

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ENCODER INPUT—SHORT FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time	$t_{su(EIE)L}$	15	–	ns
Enable Low Hold Time	$t_{h(EIE)H}$	30	–	ns
Enable Valid Time	$t_{v(EIE)}$	15	–	ns
Enable Hold Time	$t_{h(EIE)}$	15	–	ns
Data Valid Time	$t_{v(EDI)}$	15	–	ns
Data Hold Time	$t_{h(EDI)}$	15	–	ns

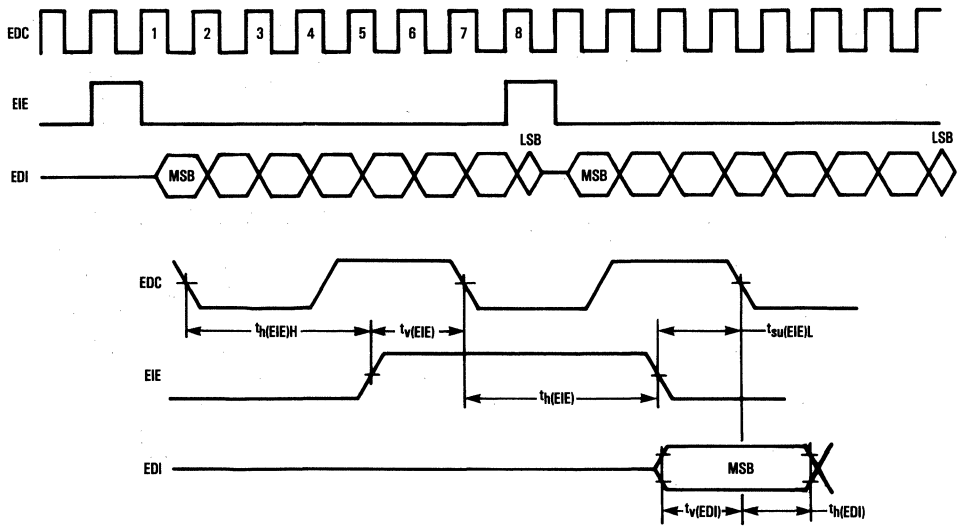


Figure 1. Encoder Input Timing—Short Frame

ENCODER INPUT—LONG FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EIE)L}$	30	—	ns
Enable Valid Time	$t_{v(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

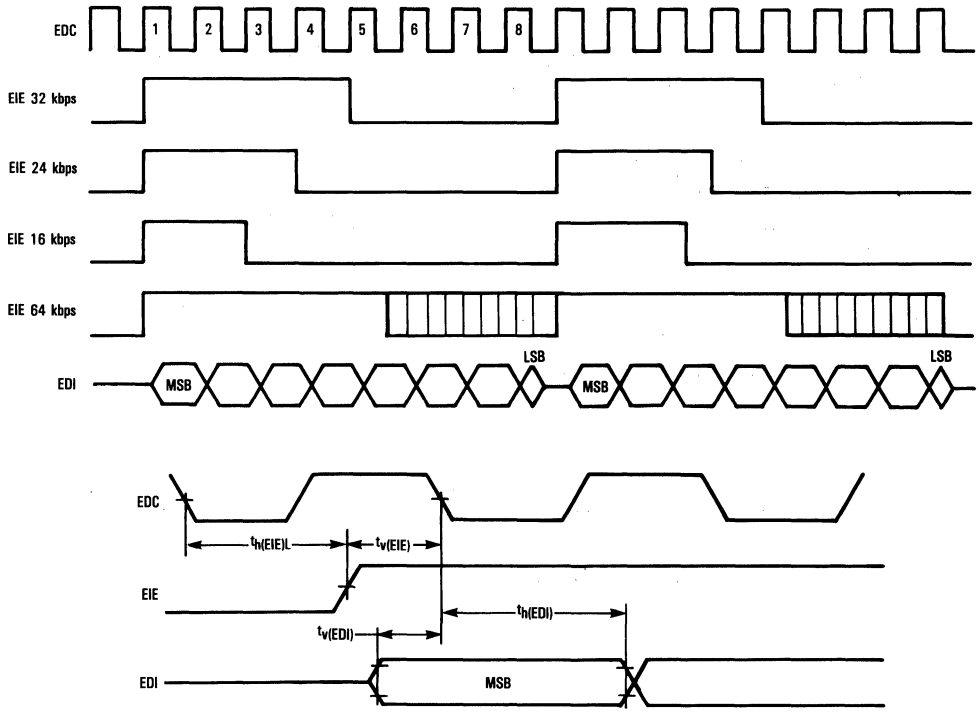


Figure 2. Encoder Input Timing—Long Frame

ENCODER OUTPUT—SHORT FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable Hold Time	$t_{h(EOE)}$	15	—	ns
Data Valid Time	$t_{v(EDO)}$	—	40	ns
Data Three-State Time (with 150 pF Load)	$t_{z(EDO)}$	1	30	ns

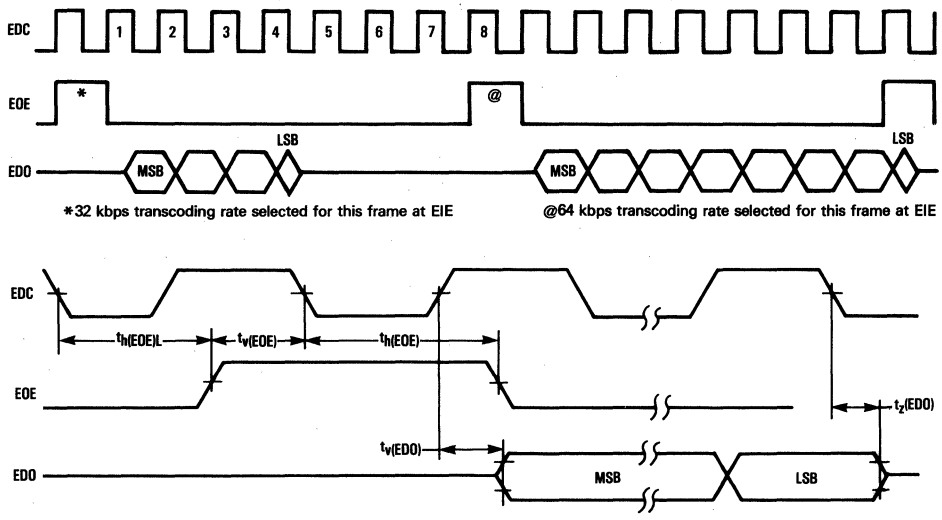
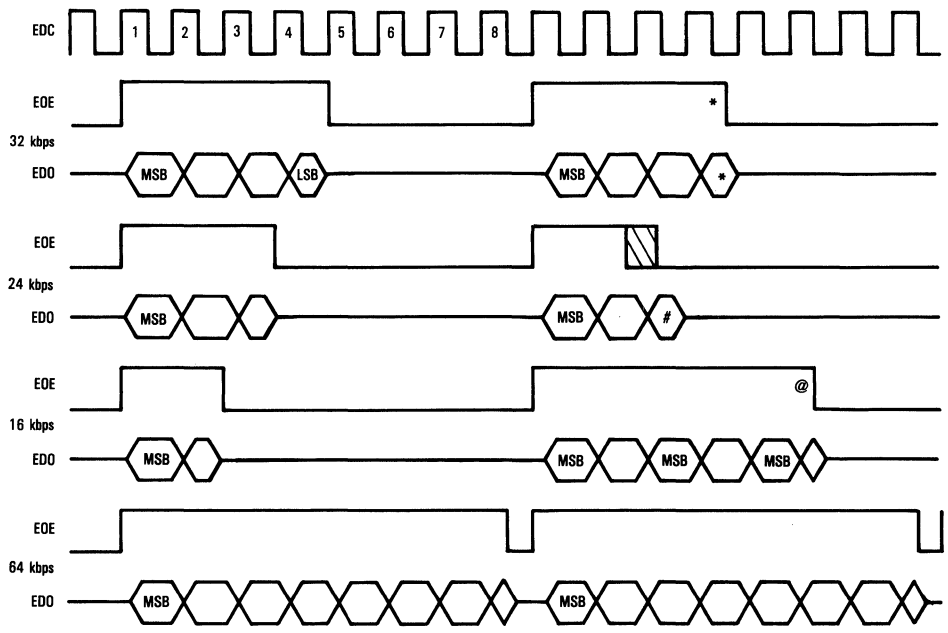


Figure 3. Encoder Output Timing—Short Frame

ENCODER OUTPUT—LONG FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable to Data Time (Whichever Edge Occurs Last)	$t_{EOE-EDO}$	—	40	ns
Clock to Data Time (Whichever Edge Occurs Last)	$t_{EDC-EDO}$	—	45	ns



*EDO Driver is controlled by EOE
#EDO completes the presentation of data
@Data recirculates

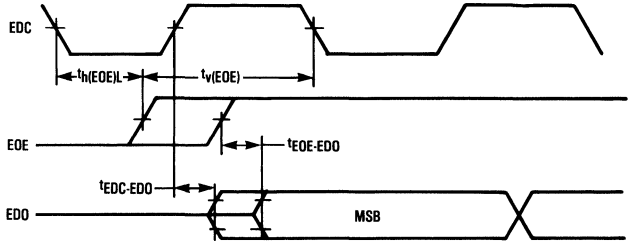


Figure 4. Encoder Output Timing—Long Frame

DECODER INPUT—SHORT FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time to Falling DDC	$t_{su(DIE)L}$	15	–	ns
Enable Low Hold Time from Falling DDC	$t_{h(DIE)H}$	30	–	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	–	ns
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	15	–	ns
Data Valid Time Before Falling DDC	$t_{v(DDI)}$	15	–	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	–	ns

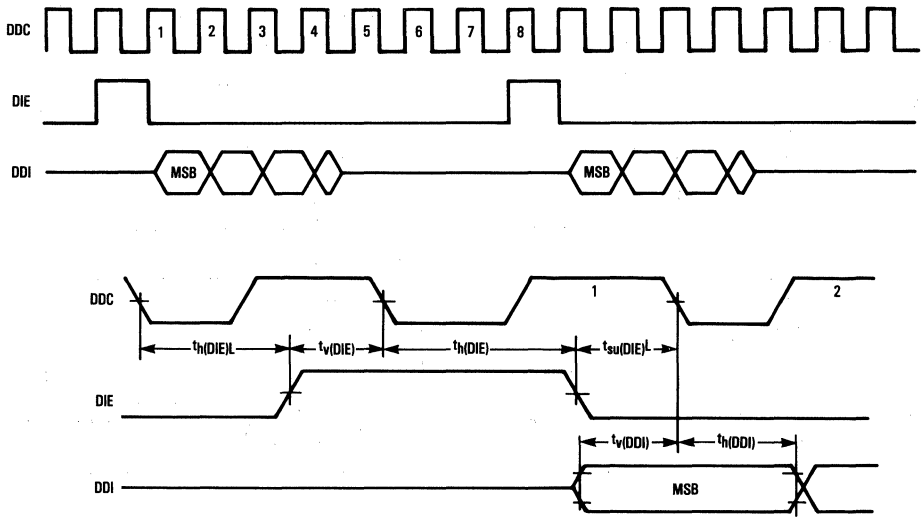
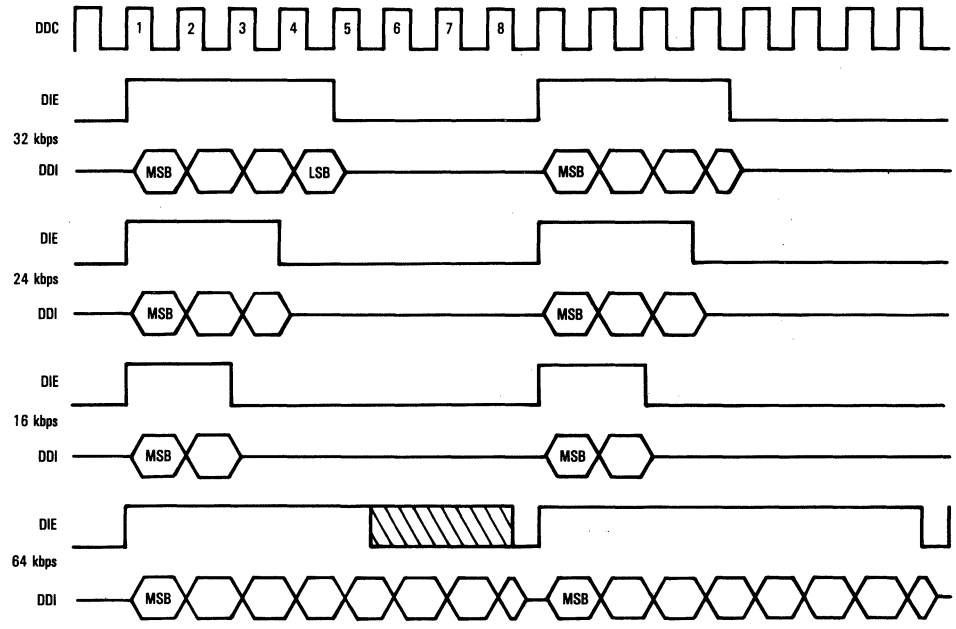


Figure 5. Decoder Input Timing—Short Frame

DECODER INPUT—LONG FRAME (V_{DD}=5.0 V, T_A= −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Data Valid Time to Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns



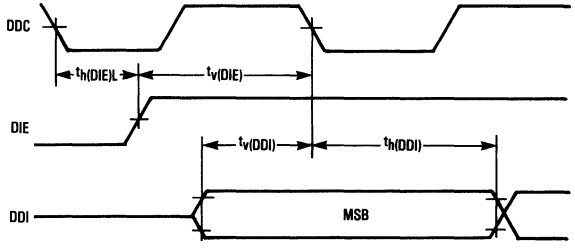


Figure 6. Decoder Input Timing—Long Frame

DECODER OUTPUT—SHORT FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Enable Hold Time	$t_{h(DOE)}$	15	—	ns
Rising Edge of DDC to Valid DDO	$t_{v(DDO)}$	—	40	ns
Delay Time from 8th DDC Low to DDO Output Disabled	$t_{z(DDO)}$	—	30	ns

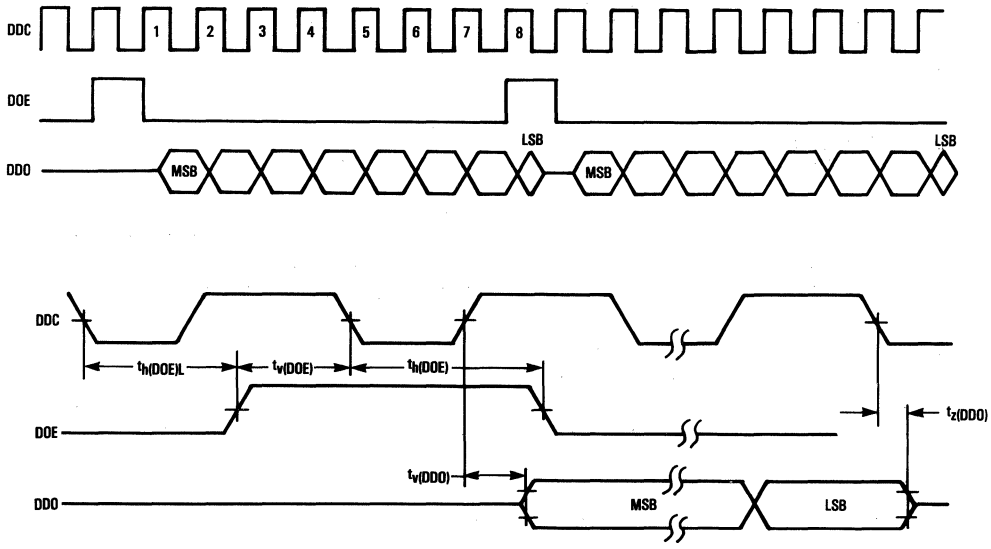
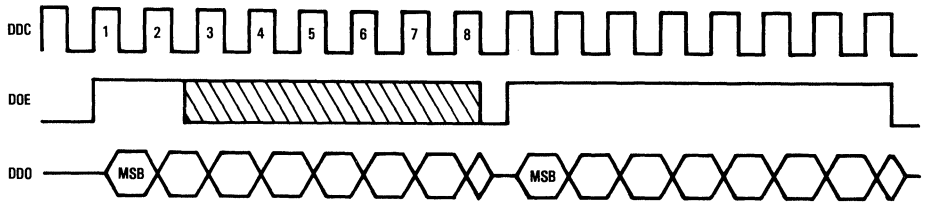


Figure 7. Decoder Output Timing—Short Frame

DECODER OUTPUT—LONG FRAME (V_{DD} = 5.0 V, T_A = −40 to +85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Rising Edge of DOE to Valid DDO (When DDC is High)	$t_{DOE-DDO}$	—	40	ns
Rising Edge of DDC to Valid DDO (When DOE is High)	$t_{DDC-DDO}$	—	45	ns
Delay Time from 8th DDC Low or DOE Low to DDO Output Disabled	$t_{z(DDO)}$	0	30	ns



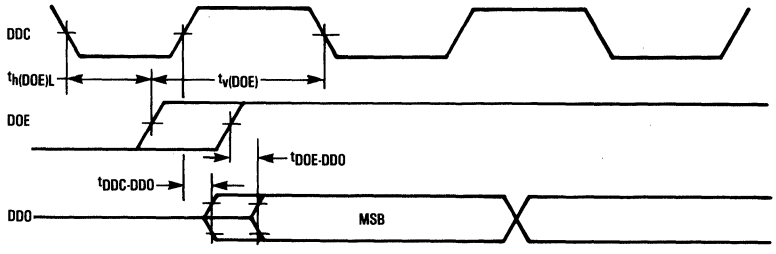


Figure 8. Decoder Output Timing—Long Frame

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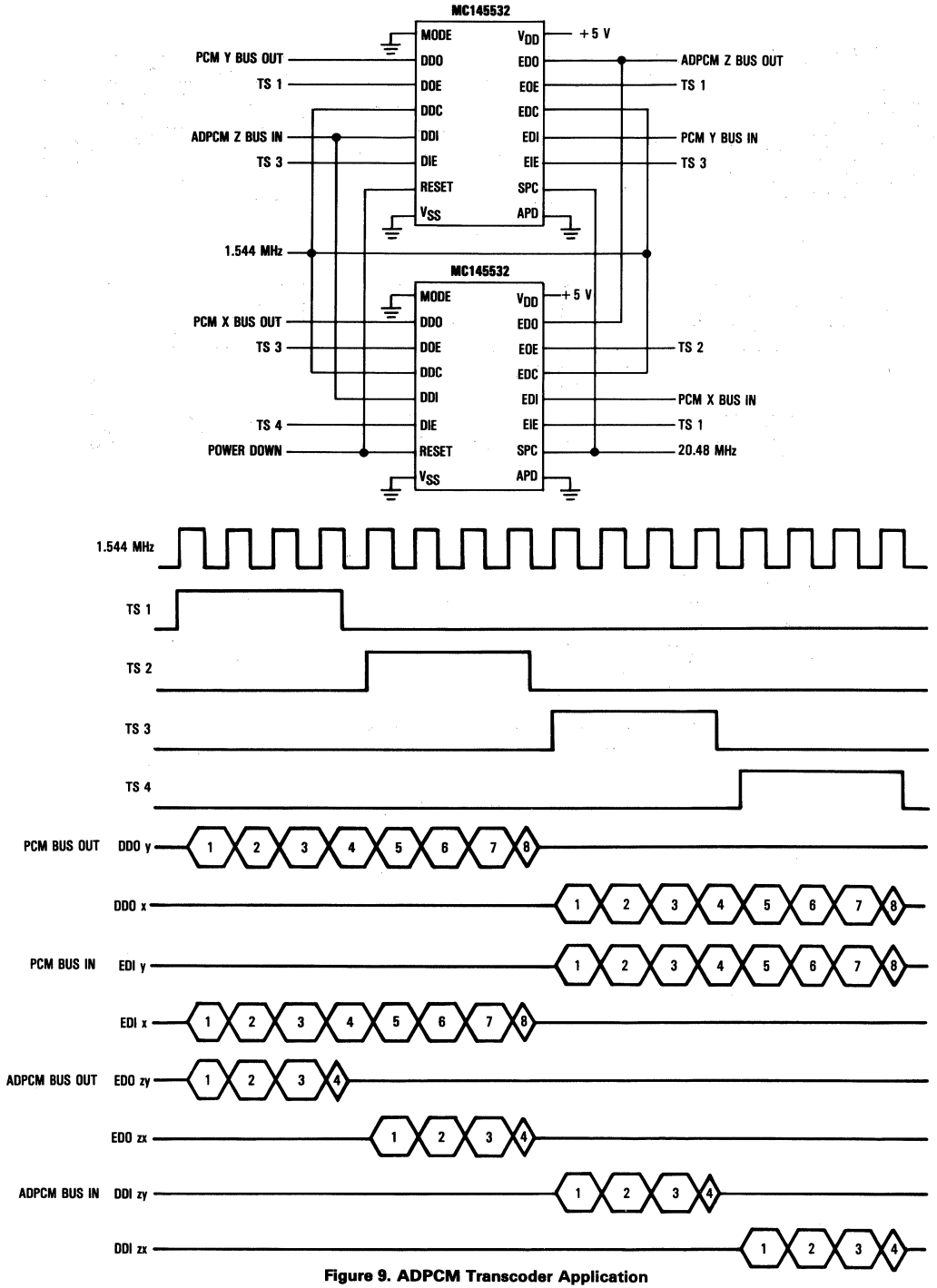


Figure 9. ADPCM Transcoder Application

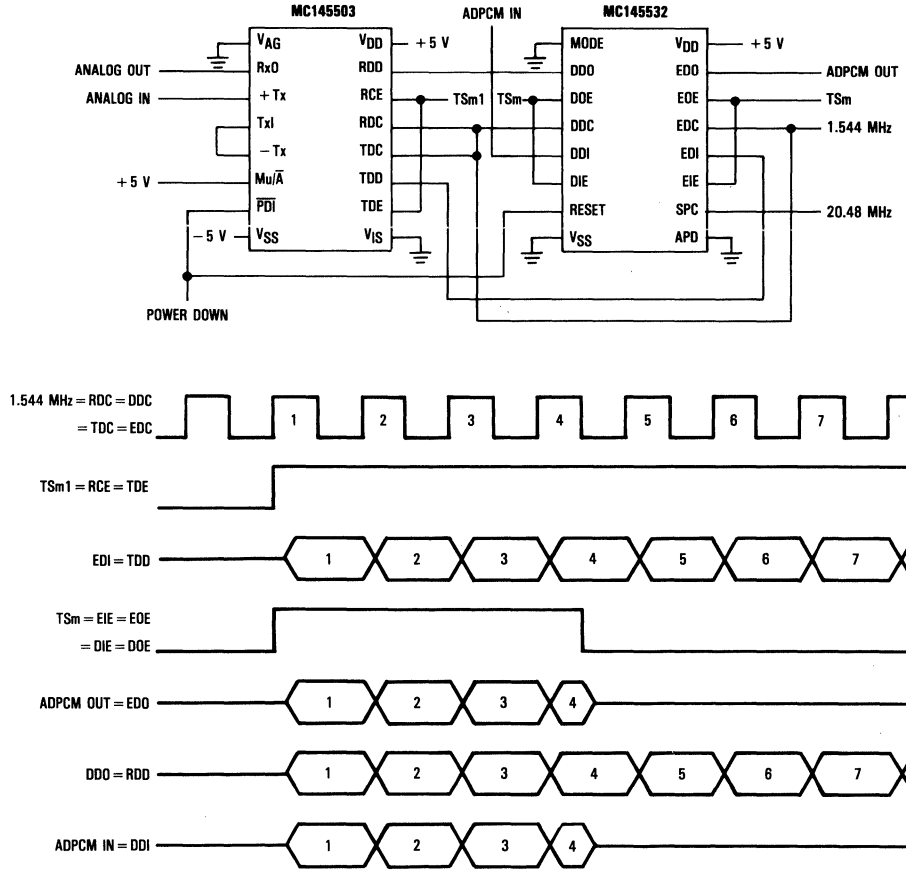
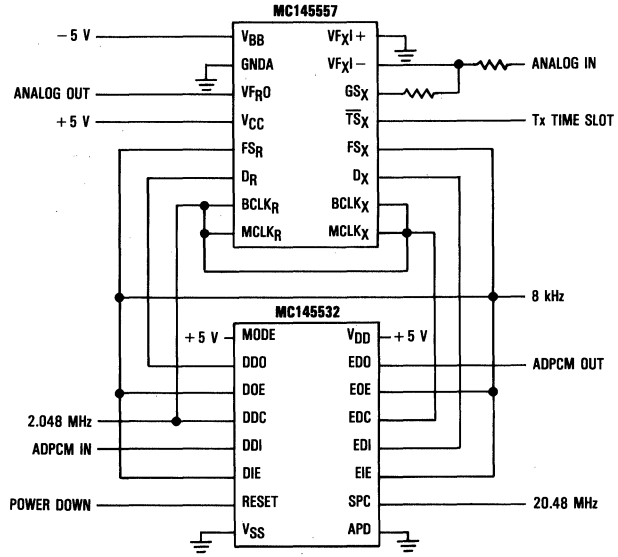


Figure 10. ADPCM Transcoder/Codec Application



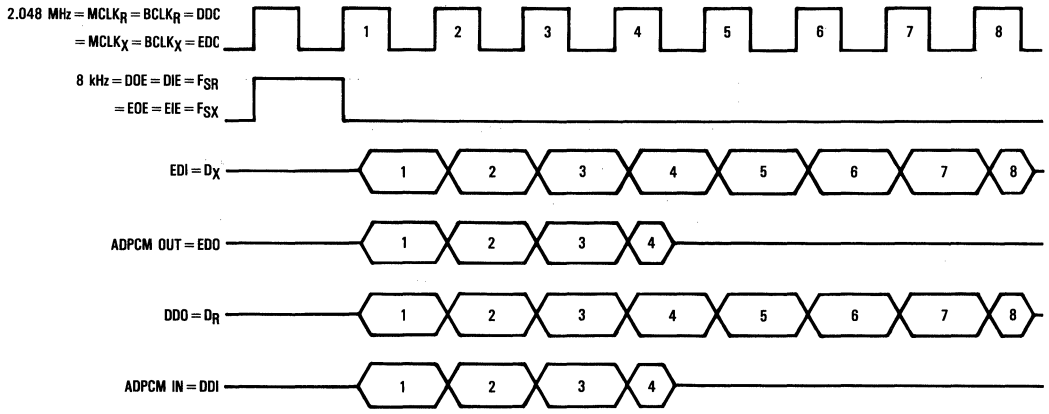


Figure 11. ADPCM Transcoder/Codec Application (A-Law)

MC145554
MC145557
MC145564
MC145567

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Advance Information

PCM Codec-Filter

The MC145554, MC145557, MC145564, and MC145567 are all per channel PCM codec-filters. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on-chip precision voltage reference. The MC145554 (Mu-Law) and MC145557 (A-Law) are general purpose devices that are offered in 16-pin packages. The MC145564 (Mu-Law) and MC145567 (A-Law), offered in 20-pin packages, add the capability of analog loop-back and push-pull power amplifiers with adjustable gain.

These devices have an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low-pass filters the analog signal with an active R-C filter to eliminate very-high-frequency noise from being modulated down to the pass band by the switched capacitor filter. From the active R-C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single-ended design, which reduces the significance of noise to both the inverted and noninverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common-mode signal that is cancelled when the inverted and noninverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low-pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R-C filter to eliminate the out of band energy of the switched capacitor filter.

These PCM codec-filters accept both industry standard clock formats. They also maintain compatibility with Motorola's family of TSACs and MC3419/MC34120 SLIC products.

The MC145554/57/64/67 family of PCM codec-filters utilizes CMOS due to its reliable low-power performance and proven capability for complex analog/digital VLSI functions.

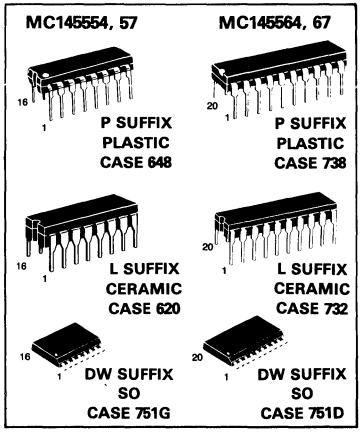
MC145554/57 (16-Pin Package)

- Fully Differential Analog Circuit Design for Lowest Noise
- Performance Specified for Extended Temperature Range of −40 to +85°C
- Transmit Band-Pass and Receive Low-Pass Filters On-Chip
- Active R-C Pre-Filtering and Post-Filtering
- Mu-Law Companding MC145554
- A-Law Companding MC145557
- On-Chip Precision Voltage Reference (2.5 V)
- Typical Power Dissipation of 40 mW, Power Down of 1.0 mW at ±5 V

MC145564/67 (20-Pin Package)

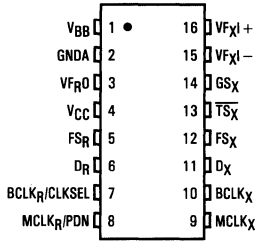
All of the Features of the MC145554/57 Plus:

- Mu-Law Companding MC145564
- A-Law Companding MC145567
- Push-Pull Power Drivers with External Gain Adjust
- Analog Loop-Back

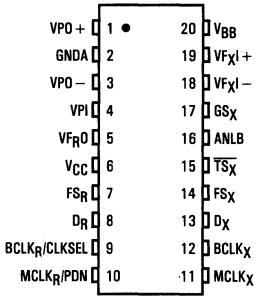


PIN ASSIGNMENT

MC145554, MC145557



MC145564, MC145557



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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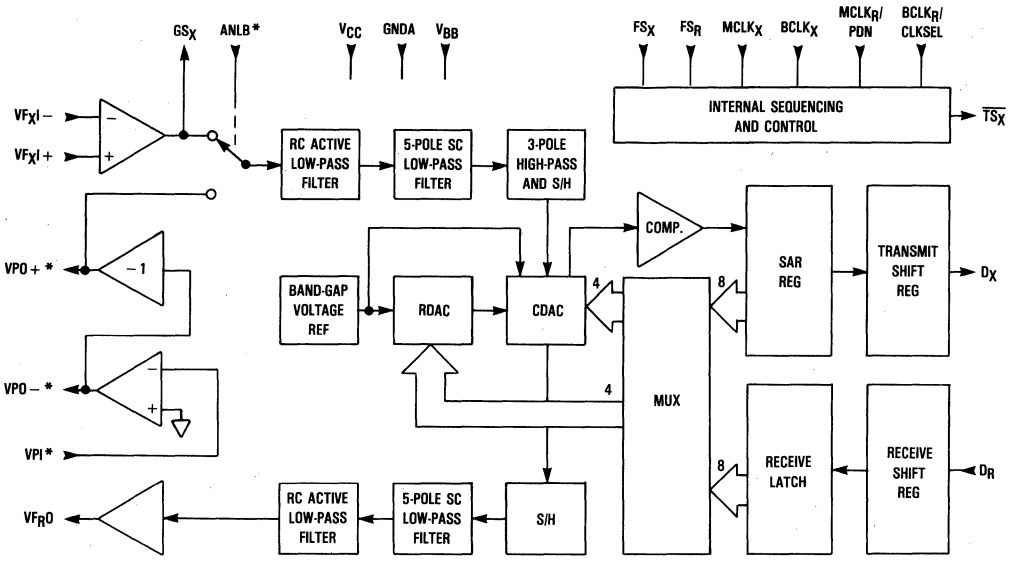
FUNCTIONAL BLOCK DIAGRAM



*MC145564 and MC145567 only.

DEVICE DESCRIPTION

A codec-filter is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder", for the A/D used to digitize voice, and "DECoder", for the D/A used for reconstructing voice. A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal-to-distortion ratio of about 30 dB over a dynamic range of about 40 dB. This can be accomplished with a linear 13-bit A/D and D/A, but will far exceed the required signal-to-distortion ratio at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. There are two companding schemes used: Mu-255 Law specifically in North America, and A-Law specifically in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above zero, by 6 dB per chord). Tables 3 and 4 show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the in-band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attentuated from the signal by a high-pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired in-band signal, which has spectral images of the in-band signal modulated about the sample frequency and its harmonics. These spectral images, called aliasing components, need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145554/57/64/67 PCM codec-filters have the codec, both presampling and reconstruction filters, and a precision voltage reference on chip, and require no external components.

PIN DESCRIPTION

DIGITAL

FS_R—Receive Frame Sync

This is an 8 kHz enable that must be synchronous with $BCLK_R$. Following a rising FS_R edge, a serial PCM word at D_R is clocked by $BCLK_R$ into the receive data register. FS_R also initiates a decode on the previous PCM word. In the absence of FS_X, the length of the FS_R pulse is used to determine whether the I/O conforms to the short frame sync or long frame sync convention.

D_R—Receive Digital Data Input

$BCLK_R$/CLKSEL—Receive Data Clock and Master Clock Frequency Selector

If this input is a clock, it must be between 128 kHz and 4.096 MHz, and synchronous with FS_R. In synchronous applications this pin may be held at a constant level; then $BCLK_X$ is used as the data clock for both the transmit and receive sides, and this pin selects the assumed frequency of the master clock (see Table 1 in **FUNCTIONAL DESCRIPTION**).

$MCLK_R$/PDN—Receive Master Clock and Power Down Control

Because of the shared DAC architecture used on these devices, only one master clock is needed. Whenever FS_X is clocking, $MCLK_X$ is used to derive all internal clocks, and the $MCLK_R$/PDN pin merely serves as a power-down control. If $MCLK_R$/PDN pin is held low or is clocked (and at least one of the frame syncs is present), the part is powered up. If this pin is held high, the part is powered down. If FS_X is absent but FS_R is still clocking, the device goes into receive half-channel mode, and $MCLK_R$ (if clocking) generates the internal clocks.

$MCLK_X$—Transmit Master Clock

This clock is used to derive the internal sequencing clocks; it must be 1.536 MHz, 1.544 MHz, or 2.048 MHz.

$BCLK_X$—Transmit Data Clock

$BCLK_X$ may be any frequency between 128 kHz and 4.096 MHz, but it should be synchronous with $MCLK_X$.

D_X—Transmit Digital Data Output

This output is controlled by FS_X and $BCLK_X$ to output the PCM data word; otherwise this pin is in a high-impedance state.

FS_X—Transmit Frame Sync

This is an 8-kHz enable that must be synchronous with $BCLK_X$. A rising FS_X edge initiates the transmission of a serial PCM word, clocked by $BCLK_X$, out of D_X. If the FS_X pulse is high for more than eight $BCLK_X$ periods, the D_X and $\overline{TS_X}$ outputs will remain in a low-impedance state until FS_X is brought low. The length of the FS_X pulse is used to determine whether the transmit and receive digital I/O conforms to the short frame sync or to the long frame sync convention.

$\overline{TS_X}$—Transmit Time Slot Indicator

This is an open-drain output that goes low whenever the D_X output is in a low-impedance state (i.e., during the transmit time slot when the PCM word is being output) for enabling a PCM bus driver.

ANLB—Analog Loop-Back Control Input (MC145564/67 Only)

When held high, this pin causes the input of the transmit RC active filter to be disconnected from GS_X and connected to VPO+ for analog loop-back testing. This pin is held low in normal operation.

ANALOG

GS_X—Gain-Setting Transmit

This output of the transmit gain-adjust operational amplifier is internally connected to the encoder section of the device. It must be used in conjunction with VF_XI- and VF_XI+ to set the transmit gain for a maximum signal amplitude of 2.5 V peak. This output can drive a 600 Ω load to 2.5 V peak.

VF_XI-—Voice-Frequency Transmit Input (Inverting)

This is the inverting input of the transmit gain-adjust operational amplifier.

VF_XI+—Voice-Frequence Transmit Input (Noninverting)

This is the noninverting input of the transmit gain-adjust operational amplifier.

VF_RO—Voice-Frequency Receive Output

This receive analog output is capable of driving a 600 Ω load to 2.5 V peak.

VPI—Voltage Power Input (MC145564/67 Only)

This is the inverting input to the first receive power amplifier. Both of the receive power amplifiers can be powered down by connecting this input to V_{BB}.

VPO−—Voltage Power Output (Inverted) (MC145564/67 Only)

This inverted output of the receive push-pull power amplifiers can drive 300 Ω to 3.3 V peak.

VPO+—Voltage Power Output (Noninverted) (MC145564/67 Only)

This noninverted output of the receive push-pull power amplifier pair can drive 300 Ω to 3.3 V peak.

POWER SUPPLY

GNDA—Analog Ground

This terminal is the reference level for all signals, both analog and digital. It is 0 V.

V_{CC}—Positive Power Supply

V_{CC} is typically 5 V.

V_{BB}—Negative Power Supply

V_{BB} is typically −5 V.

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FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of these codec/filters includes a low-noise gain setting amplifier capable of driving a 600 Ω load. Its output is fed to a three-pole anti-aliasing pre-filter. This pre-filter incorporates a two-pole Butterworth active low-pass filter, and a single passive pole. This pre-filter is followed by a single ended-to-differential converter that is clocked at 256 kHz. All subsequent analog processing utilizes fully differential circuitry. The next section is a fully-differential, 5-pole switched-capacitor low-pass filter with a 3.4 kHz pass band. After this filter is a 3-pole switched-capacitor high-pass filter having a cutoff frequency of about 200 Hz. This high-pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated operational amplifier offsets in the preceding filter stages. The last stage of the high-pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital-to-analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched-capacitor band-gap reference generates precise positive and negative reference voltages that are independent of temperature and power supply voltage. A binary-weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame-by-frame autozeroed comparator to implement a successive-approximation conversion algorithm. All of the analog circuitry involved in the data conversion—the voltage reference, RDAC, CDAC, and comparator—are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a five-pole 3400 Hz switched capacitor low-pass filter with sinX/X correction, and a two-pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is a power amplifier that is capable of driving a 600 Ω load. The MC145564 and MC145567 add a pair of power amplifiers that are connected in a push-pull configuration; two external resistors set the gain of both of the complementary outputs. The output of the second amplifier may be internally connected to the input of the transmit anti-aliasing filter by bringing the ANLB pin high. The power amplifiers can drive unbalanced 300 Ω loads or a balanced 600 Ω load; they may be powered down independent of the rest of the chip by tying the VPI pin to V_{BB}.

MASTER CLOCKS

Since this codec-filter design has a single DAC architecture, only one master clock is used. In normal operation (both frame syncs clocking), $MCLK_X$ is used as the master clock, regardless of whether the $MCLK_R$/PDN pin is clocking or low. The same is true if the part is in transmit half-channel mode (FS_X clocking, FS_R held low). But if the codec-filter is in the receive half-channel mode, with FS_R clocking and FS_X held low, $MCLK_R$ is used for the internal master clock if it is clocking; if $MCLK_R$ is low, then $MCLK_X$ is still used for the internal master clock. Since only one of the master clocks is used at any given time, they need not be synchronous.

The master clock frequency must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. The frequency that the codec-filter expects depends upon whether the part is a MU-law or an A-law part, and on the state of the $BCLK_R$/CLKSEL pin. The allowable options are shown in Table 1. When a level (rather than a clock) is provided for $BCLK_R$/CLKSEL, $BCLK_X$ is used as the bit clock for both transmit and receive.

Table 1. Master Clock Frequency Determination

$BCLK_R$/CLKSEL	Master Clock Frequency Expected	
	MC145554/64	MC145557/67
Clocked, 1, or Open	1.536 MHz 1.544 MHz	2.048 MHz
0	2.048 MHz	1.536 MHz 1.544 MHz

FRAME SYNCS AND DIGITAL I/O

These codec-filters can accommodate both of the industry standard timing formats. The long frame sync mode is used by Motorola's MC145500 family of codec-filters and the UDLT family of digital loop transceivers. The short frame sync mode is compatible with the IDL (Interchip Digital Link) serial format used in Motorola's ISDN family and by other companies in their telecommunication devices. These codec/filters use the length of the transmit frame sync (FS_X) to determine the timing format for both transmit and receive unless the part is operating in the receive half-channel mode.

In the long frame sync mode, the frame sync pulses must be at least three bit clock periods long. The D_X and $\overline{TS_X}$ outputs are enabled by the logical ANDing of FS_X and $BCLK_X$; when both are high, the sign bit appears at the D_X output. The next seven rising edges of $BCLK_X$ clock out the remaining seven bits of the PCM word. The D_X and $\overline{TS_X}$ outputs return to a high impedance state on the falling edge of the eighth bit clock or the falling edge of FS_X, whichever comes later. The receive PCM word is clocked into D_R on the eight falling $BCLK_R$ edges following an FS_R rising edge.

For short frame sync operation, the frame sync pulses must be one bit clock period long. On the first $BCLK_X$ rising edge after the falling edge of $BCLK_X$ has latched FS_X high, the D_X and $\overline{TS_X}$ outputs are enabled and the sign bit is presented on D_X. The next seven rising edges of $BCLK_X$ clock out the remaining seven bits of the PCM word; on the eighth $BCLK_X$ falling edge, the D_X and $\overline{TS_X}$ outputs return to a high impedance state. On the second falling $BCLK_R$ edge followng an FS_R rising edge, the receive sign bit is clocked into D_R. The next seven $BCLK_R$ falling edges clock in the remaining seven bits of the receive PCM word.

Table 2 shows the coding format of the transmit and receive PCM words.

HALF-CHANNEL MODES

In addition to the normal full duplex operating mode, these codec-filters can operate in both transmit and receive half-channel modes. Transmit half-channel mode is entered by holding FS_R low. The VF_RO output goes to analog ground but remains in a low impedance state (to facilitate a hybrid interface); PCM data at D_R is ignored. Holding FS_X low while clocking FS_R puts these devices in the receive half-channel mode. In this state, the transmit input operational amplifier continues to operate, but the rest of the transmit circuitry is disabled; the D_X and $\overline{TS_X}$ outputs remain in a high impedance state. $MCLK_R$ is used as the internal master clock if it is clocking. If $MCLK_R$ is not clocking, then $MCLK_X$ is used for

Table 2. PCM Data Format

Level	Mu-Law (MC145554/64)			A-Law (MC145557/67		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	0 0 0	0 0 0 0	1	0 1 0	1 0 1 0
+Zero	1	1 1 1	1 1 1 1	1	1 0 1	0 1 0 1
−Zero	0	1 1 1	1 1 1 1	0	1 0 1	0 1 0 1
−Full Scale	0	0 0 0	0 0 0 0	0	0 1 0	1 0 1 0

the internal master clock, but in that case it should be synchronous with FS_R. If $BCLK_R$ is not clocking, $BCLK_X$ will be used for clocking the receive data, just as in the full channel operating mode. In receive half-channel mode only, the length of the FS_R pulse is used to determine whether short frame sync or long frame sync timing is used at D_R.

POWER DOWN

Holding both FS_X and FS_R low causes the part to go into the power down state. Power down occurs approximately 2 ms after the last frame sync pulse is received. An alternative way to put these devices in power down is to hold the $MCLK_R$/PDN pin high. When the chip is powered down, the D_X, $\overline{TS_X}$, and GS_X outputs are high impedance, the VF_RO, VPO−, and VPO+ operational amplifiers are biased with a trickle current so that their respective outputs remain stable at analog ground. To return the chip to the power up state, $MCLK_R$/PDN must be low or clocking and at least one of the frame sync pulses must be present. The D_X and $\overline{TS_X}$ outputs will remain in a high impedance state until the second FS_X pulse after power up.

MAXIMUM RATINGS (Voltages Referenced to GNDA)

Rating	Symbol	Value	Unit
DC Supply Voltage V_{CC} to V_{BB} V_{CC} to GNDA V_{BB} to GNDA		−0.5 to 13 −0.3 to 7.0 −7.0 to +0.3	V
Voltage on any Analog Input or Output Pin		V_{BB} − 0.3 to V_{CC} + 0.3	V
Voltage on any Digital Input or Output Pin		GNDA − 0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused outputs must always be tied to an appropriate logic voltage level (e.g., V_{BB}, GNDA, or V_{CC}).

POWER SUPPLY (T_A = −40 to +85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{BB}	−4.75	−5.0	−5.25	
Active Power Dissipation (No Load)	MC145554/57	—	40	60	mW
	MC145564/67	—	45	70	
	MC145564/67, VPI = V_{BB}	—	40	60	
Power Down Dissipation (No Load)	MC145554/57	—	1.0	3.0	mW
	MC145564/67	—	2.0	5.0	
	MC145564/56, VPI = V_{BB}	—	1.0	3.0	

DIGITAL LEVELS (V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GNDA = 0 V, T_A = −40 to +85°C)

Characteristic		Symbol	Min	Max	Unit
Input Low Voltage		V_{IL}	—	0.6	V
Input High Voltage		V_{IH}	2.2	—	V
Output Low Voltage	D_X or $\overline{TS_X}$, I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Output High Voltage	D_X, I_{OH} = −3.2 mA	V_{OH}	2.4	—	V
	I_{OH} = −1.6 mA		V_{CC} − 0.5	—	
Input Low Current	GNDA ≤ V_{in} ≤ V_{CC}	I_{IL}	−10	+10	μA
Input High Current	GNDA ≤ V_{in} ≤ V_{CC}	I_{IH}	−10	+10	μA
Output Current in High Impedance State	GNDA ≤ D_X ≤ V_{CC}	I_{OZ}	−10	+10	μA

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ANALOG ELECTRICAL CHARACTERISTICS

(V_{CC} = +5 V ±5%, V_{BB} = −5 V ±5%, VF_XI- Connected to GS_X, T_A = −40 to +85°C)

Characteristic		Min	Typ	Max	Unit
Input Current (−2.5 V ≤ V_{in} ≤ +2.5 V)	VF_XI+, VF_XI-	—	±0.05	±0.2	μA
AC Input Impedance to GNDA (1 kHz)	VF_XI+, VF_XI-	10	20	—	MΩ
Input Capacitance	VF_XI+, VF_XI-	—	—	10	pF
Input Offset Voltage of GS_X Op Amp	VF_XI+, VF_XI-	—	—	±25	mV
Input Common Mode Voltage Range	VF_XI+, VF_XI-	−2.5	—	+2.5	V
Input Common Mode Rejection Ratio	VF_XI+, VF_XI-	—	65	—	dB
Unity Gain Bandwidth of GS_X Op Amp (R_{load} ≥ 10 kΩ)		—	1000	—	kHz
DC Open Loop Gain of GS_X Op Amp (R_{load} ≥ 10 kΩ)		75	—	—	dB
Equivalent Input Noise (C-Mess) Between VF_XI+ and VF_XI- at GS_X			−20		dBrnC0
Output Load Capacitance for GS_X Op Amp		0	—	100	pF
Output Voltage Range for GS_X	R_{load} = 10 kΩ to GNDA R_{load} = 600 Ω to GNDA	−3.5 −2.8	— —	+3.5 +2.8	V
Output Current (−2.8 V ≤ V_{out} ≤ +2.8 V)	GS_X, VF_RO	±5.0	—	—	mA
Output Impedance VF_RO (0 to 3.4 kHz)		—	1	—	Ω
Output Load Capacitance for VF_RO		0	—	500	pF
VF_RO Output DC Offset Voltage Referenced to GNDA		—	—	±100	mV
Transmit Power Supply Rejection	Positive 0 to 100 kHz, C-Message Negative 0 to 100 kHz, C-Message	45 45	— —	— —	dBC
Receive Power Supply Rejection	Positive, 0 to 100 kHz, C-Message Positive, 4 kHz to 25 kHz Positive, 25 kHz to 50 kHz Negative, 0 to 100 kHz, C-Message Negative, 4 kHz to 25 kHz Negative, 25 kHz to 50 kHz	50 50 43 50 45 38	— — — — — —	— — — — — —	dBC dB dB dBC dB dB
MC145564/67 Power Drivers					
Input Current (−1 V ≤ VPI ≤ +1 V)	VPI	—	±0.05	±0.5	μA
Input Resistance (−1 V ≤ VPI ≤ +1 V)	VPI	5	10	—	MΩ
Input Offset Voltage (VPI Connected to VPO−)	VPI	—	—	±50	mV
Output Resistance, Inverted Unity Gain	VPO+ or VPO−	—	1	—	Ω
Unity Gain Bandwidth, Open Loop	VPO−	—	400	—	kHz
Load Capacitance (∞Ω ≥ R_{load} ≥ 300 Ω)	VPO+ or VPO− to GNDA	0	—	1000	pF
Gain from VPO− to VPO+ (R_{load} = 300 Ω, VPO+ to GNDA Level at VPO− = 1.77 Vrms, +3 dBm0)		—	−1	—	V/V
Maximum 0 dBm0 Level for Better than ±0.1 dB Linearity Over the Range −10 dBm0 to +3 dBm0 (For R_{load} between VPO+ and VPO−)	R_{load} = 600 Ω R_{load} = 1200 Ω R_{load} = 10 kΩ	3.3 3.5 4.0	— — —	— — —	Vrms
Power Supply Rejection of V_{CC} or V_{BB} (VPO− Connected to VPI) VPO+ or VPO− to GNDA	0 to 4 kHz 4 to 50 kHz	55 35	— —	— —	dB
Differential Power Supply Rejection of V_{CC} or V_{BB} (VPO− Connected to VPI)	VPO+ to VPO−, 0 to 50 kHz	50	—	—	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{CC} = +5 V ±5%, V_{BB} = −5 V ±5%, GNDA = 0 V, 0 dBm0 = 1.2276 Vrms = +4 dBm @ 600 Ω, FS_X = FS_R = 8 kHz, $BCLK_X$ = $MCLK_X$ = 2.048 MHz Synchronous Operation, VF_XI- Connected to GS_X, T_A = −40 to +85°C) Unless Otherwise Noted

Characteristic		End-to-End		A/D		D/A		Unit
		Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{CC} = 5 V, V_{BB} = −5 V)		—	—	−0.25	+0.25	−0.25	+0.25	dB
Absolute Gain Variation with Temperature	0 to +70°C	—	—	—	±0.03	—	±0.03	dB
	−40 to +85°C	—	—	—	±0.06	—	±0.06	
Absolute Gain Variation with Power Supply (V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%)		—	—	—	±0.02	—	±0.02	dB
Gain vs Level Tone (Relative to −10 dBm0, 1.02 kHz)	+3 to −40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
	−40 to −50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
	−50 to −55 dBm0	−1.6	+1.6	−0.8	+0.8	−0.8	+0.8	
Gain vs Level Pseudo Noise CCITT G.712	−10 to −40 dBm0	—	—	−0.25	+0.25	−0.25	+0.25	dB
(MC145557/67 A-Law Relative to −10 dBm0)	−40 to −50 dBm0	—	—	−0.30	+0.30	−0.30	+0.30	
	−50 to −55 dBm0	—	—	−0.45	+0.45	−0.45	+0.45	
Total Distortion, 1.02 kHz Tone (C-Message)	+3 dBm0	33	—	33	—	33	—	dBC
	0 to −30 dBm0	35	—	36	—	36	—	
	−40 dBm0	29	—	30	—	30	—	
	−45 dBm0	24	—	25	—	25	—	
	−55 dBm0	15	—	15	—	15	—	
Total Distortion with Pseudo Noise CCITT G.714	−3 dBm0	27.5	—	28	—	28.5	—	dB
(MC145557/67 A-Law)	−6 to −27 dBm0	35	—	35.5	—	36	—	
	−34 dBm0	33.1	—	33.5	—	34.2	—	
	−40 dBm0	28.2	—	28.5	—	30	—	
	−55 dBm0	13.2	—	13.5	—	15	—	
Idle Channel Noise (For End-End and A/D, Note 1)								
(MC145554/64 Mu-Law, C-Message Weighted)		—	15	—	15	—	7	dBrnC0
(MC145557/67 A-Law, Psophometric Weighted)		—	−70	—	−70	—	−83	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)	15 Hz	—	−40	—	−40	−0.15	0	dB
	50 Hz	—	−30	—	−30	−0.15	0	
	60 Hz	—	−26	—	−26	−0.15	0	
	200 Hz	—	—	−1.0	−0.4	−0.15	0	
	300 to 3000 Hz	−0.3	+0.3	−0.15	+0.15	−0.15	+0.15	
	3300 Hz	−0.70	+0.3	−0.35	+0.15	−0.35	+0.15	
	3400 Hz	−1.6	0	−0.8	0	−0.8	0	
	4000 Hz	—	−28	—	−14	—	−14	
	4600 Hz	—	−60	—	−32	—	−30	
In-band Spurious (1.02 kHz @ 0 dBm0, Transmit and Receive)	300 to 3000 Hz	—	−48	—	−48	—	−48	dBm0
Out-of-Band Spurious at VF_RO (300-3400 Hz @ 0 dBm0 In)								dB
	4600 to 7600 Hz	—	−30	—	—	—	−30	
	7600 to 8400 Hz	—	−40	—	—	—	−40	
	8400 to 100,000 Hz	—	−30	—	—	—	−30	
Idle Channel Noise Selective (8 kHz, Input = GNDA, 30 Hz Bandwidth)		—	−70	—	—	—	−70	dBm0
Absolute Delay (1600 Hz)		—	—	—	315	—	215	μs
Group Delay Referenced to 1600 Hz	500 to 600 Hz	—	—	—	220	−40	—	μs
	600 to 800 Hz	—	—	—	145	−40	—	
	800 to 1000 Hz	—	—	—	75	−40	—	
	1000 to 1600 Hz	—	—	—	40	−30	—	
	1600 to 2600 Hz	—	—	—	75	—	90	
	2600 to 2800 Hz	—	—	—	105	—	125	
	2800 to 3000 Hz	—	—	—	155	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)		—	—	—	−75	—	−75	dB
Intermodulation Distortion of Two Frequencies of Amplitudes −4 to −21 dBm0 from the Range 300 to 3400 Hz		—	−41	—	−41	—	−41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ −50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ −50 dBm0.

2

DIGITAL SWITCHING CHARACTERISTICS (V_{CC} = 5 V ±5%, V_{BB} = −5 V ±5%, GNDA = 0 V, All Signals Referenced to GNDA, T_A = −40 to +85°C, C_{load} = 150 pF Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	$MCLK_X$ or $MCLK_R$	f_M	—	1.536	—	MHz
			—	1.544	—	
			—	2.048	—	
Minimum Pulse Width High or Low	$MCLK_X$ or $MCLK_R$	$t_{w(M)}$	100	—	—	ns
Minimum Pulse Width High or Low	$BCLK_X$ or $BCLK_R$	$t_{w(B)}$	50	—	—	ns
Minimum Pulse Width Low	FS_X or FS_R	$t_{w(FL)}$	50	—	—	ns
Rise Time for all Digital Signals		t_r	—	—	50	ns
Fall Time for all Digital Signals		t_f	—	—	50	ns
Bit Clock Data Rate	$BCLK_X$ or $BCLK_R$	f_B	128	—	4096	kHz
Setup Time from $BCLK_X$ Low to $MCLK_X$ High		$t_{su(BRM)}$	50	—	—	ns
Setup Time from $MCLK_X$ High to $BCLK_X$ Low		$t_{su(MFB)}$	20	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) High		$t_{h(BF)}$	20	—	—	ns
Setup Time for FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low for Long Frame		$t_{su(FB)}$	80	—	—	ns
Delay Time from $BCLK_X$ High to D_X Data Valid		$t_{d(BD)}$	20	60	140	ns
Delay Time from $BCLK_X$ High to $\overline{TS_X}$ Low		$t_{d(BTS)}$	20	50	140	ns
Delay Time from the 8th $BCLK_X$ Low or FS_X Low to D_X Output Disabled		$t_{d(ZC)}$	50	70	140	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Is Later		$t_{d(ZF)}$	20	60	140	ns
Setup Time from D_R Valid to $BCLK_R$ Low		$t_{su(DB)}$	0	—	—	ns
Hold Time from $BCLK_R$ Low to D_R Invalid		$t_{h(BD)}$	50	—	—	ns
Setup Time from FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low in Short Frame		$t_{su(F)}$	50	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Short Frame		$t_{h(F)}$	50	—	—	ns
Hold Time from 2nd Period of $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Long Frame		$t_{h(BFI)}$	50	—	—	ns

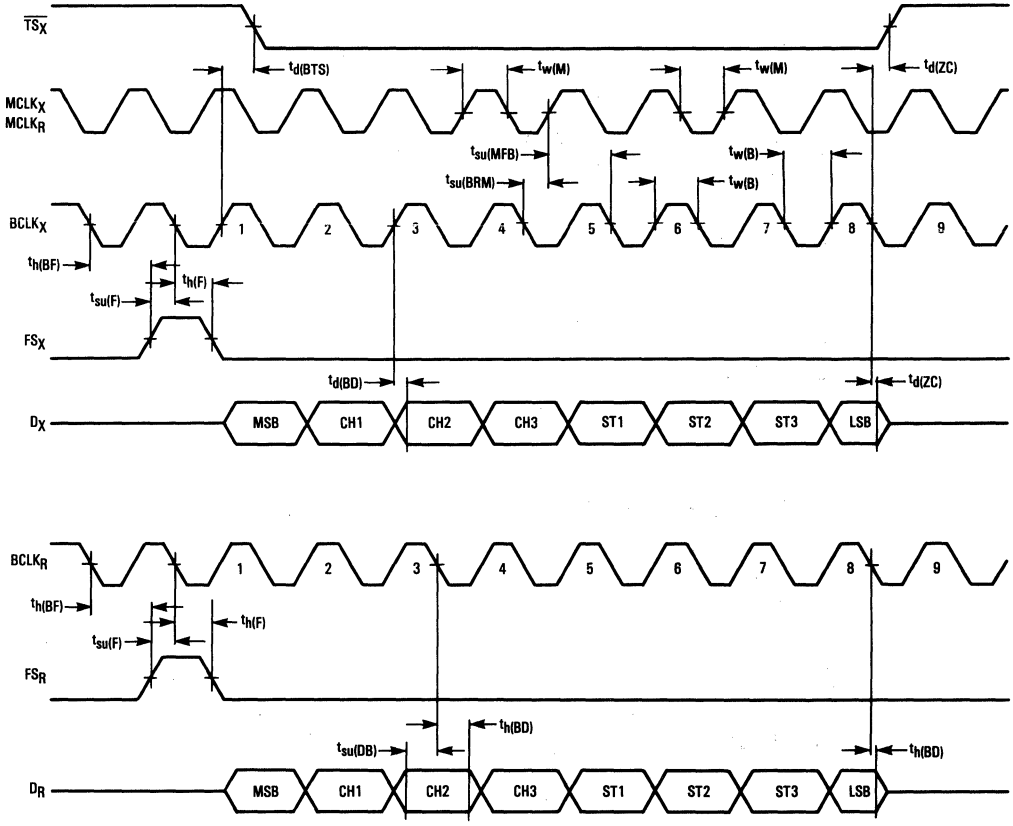


Figure 1. Short Frame Sync Timing

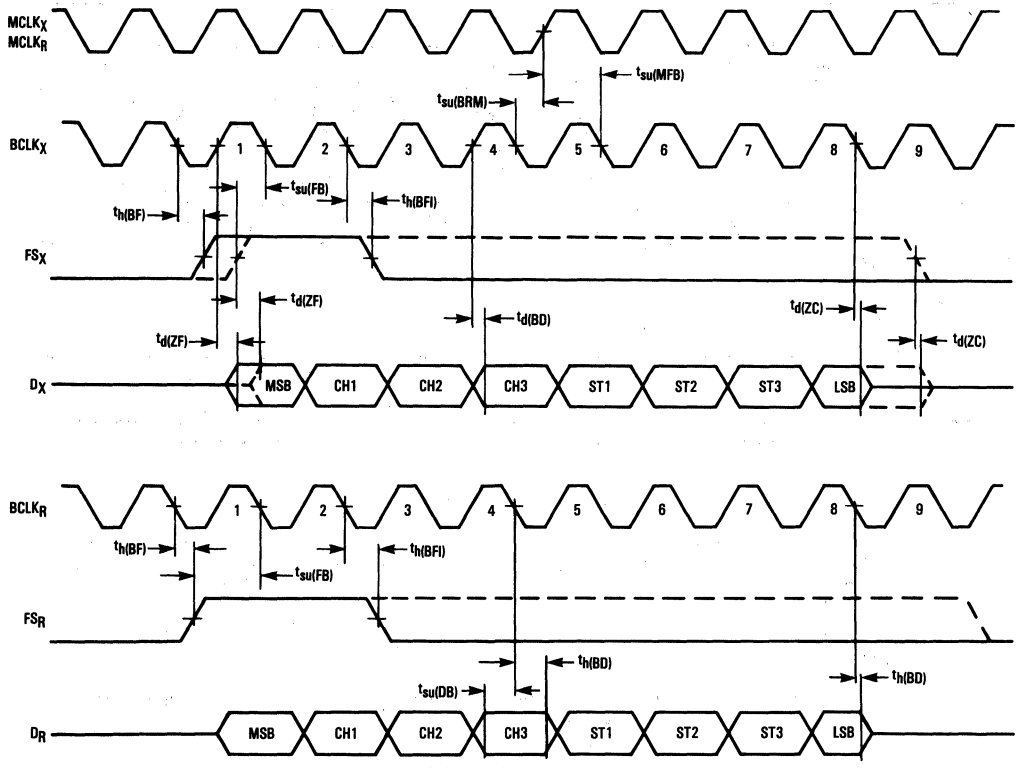


Figure 2. Long Frame Sync Timing

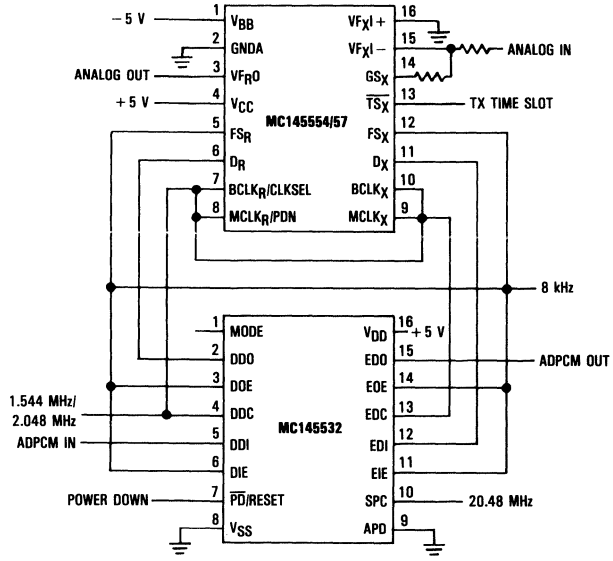


Figure 3. ADPCM Transcoder Application

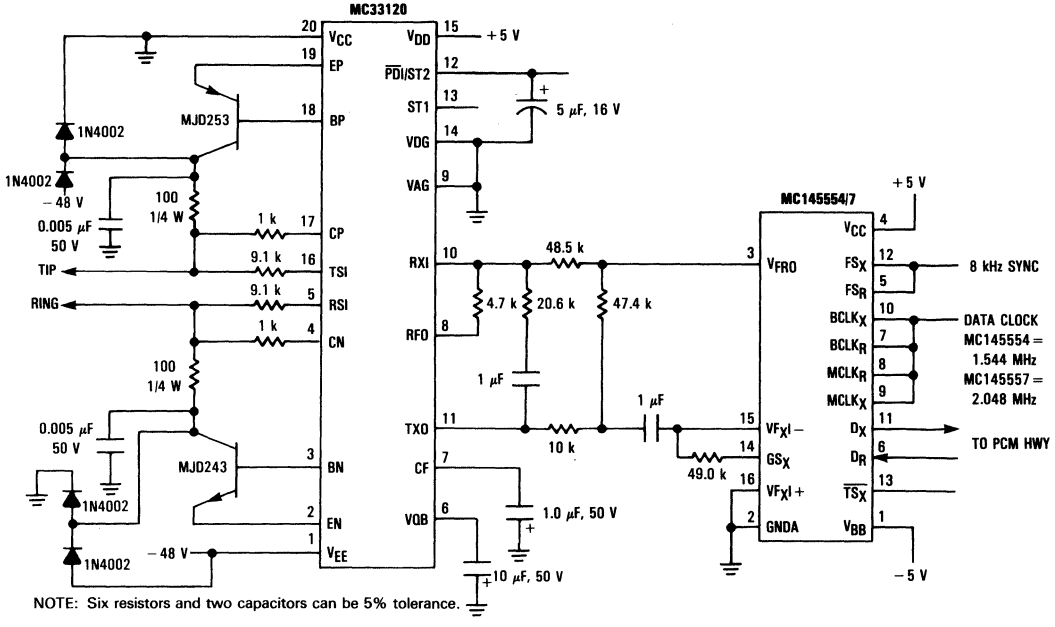


Figure 4. A Complete Single Party Channel Unit Using MC145554/57 PCM Codec/Filter and MC33120 SLIC

2

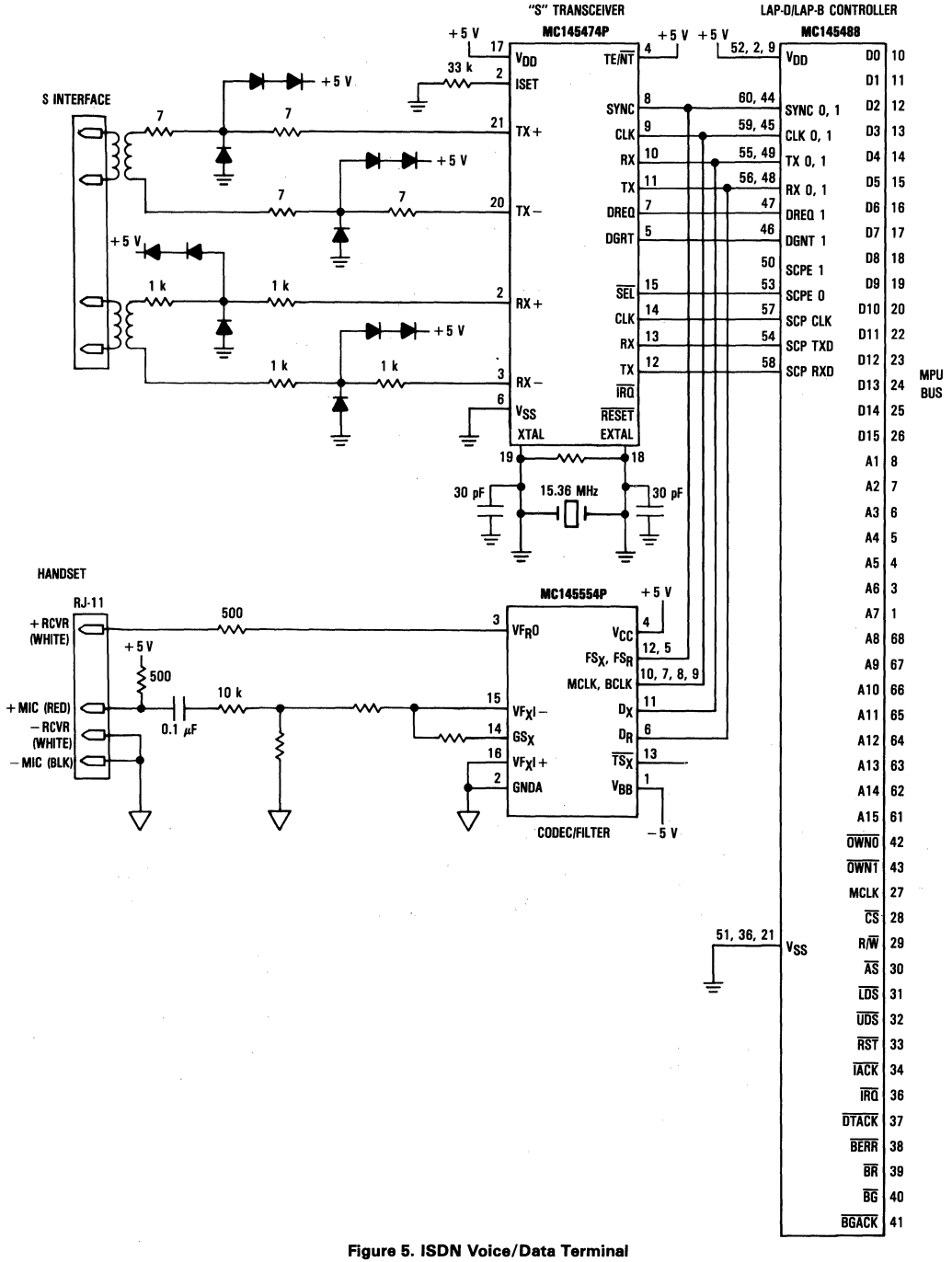


Figure 5. ISDN Voice/Data Terminal

Table 3. Mu-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256	7903	1	0	0	0	0	0	0	0	8031
			:					:				:
			4319									
			4063	1	0	0	0	1	1	1	1	4191
7	16	128	:					:				:
			2143									
			2015	1	0	0	1	1	1	1	1	2079
6	16	64	:					:				:
			1055									
			991	1	0	1	0	1	1	1	1	1023
5	16	32	:					:				:
			511									
			479	1	0	1	1	1	1	1	1	495
4	16	16	:					:				:
			239									
			223	1	1	0	0	1	1	1	1	231
3	16	8	:					:				:
			103									
			95	1	1	0	1	1	1	1	1	99
2	16	4	:					:				:
			35									
			31	1	1	1	0	1	1	1	1	33
1	15	2	:					:				:
			3									
			1	1	1	1	1	1	1	1	0	2
	1	1		1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

2

Table 4. A-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
				1	0	1	0	1	0	1	0	4032
			3968									
7	16	128	:					:				:
			2176									
				1	0	1	0	0	1	0	1	2112
			2048									
			:					:				:
6	16	64	1088									
				1	0	1	1	0	1	0	1	1056
			1024									
			:					:				:
5	16	32	544									
				1	0	0	0	0	1	0	1	528
			512									
			:					:				:
4	16	16	272									
				1	0	0	1	0	1	0	1	264
			256									
			:					:				:
3	16	8	136									
				1	1	1	0	0	1	0	1	132
			128									
			:					:				:
2	16	4	68									
				1	1	1	1	0	1	0	1	66
			64									
			:					:				:
1	32	2	2									
				1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

MC145601

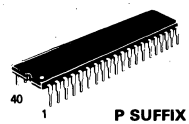
Product Preview

Time Slot Interchange Circuit

Silicon-Gate CMOS

The MC145601 time slot interchange circuit (TSIC) is a CMOS IC designed for switching pulse code modulation (PCM) voice or data, under microprocessor control, in a digital exchange or central office. It connects any of 256 incoming PCM channels to any of 256 outgoing PCM channels.

- 5-Volt Supply
- 8 × 32 Channel Input
- 8 × 32 Channel Output
- 256-Port Nonblocking Digital Switching Matrix
- Building Block for Digital PABX
- Expandable to Larger Capacity Block
- 32 Serial Channels Per Frame
- Typical Bit Rate: 2.048 Mbit/s
- Typical Synchronization Rate: 8 kHz
- Interface to MC68XXX Family Microprocessors
- 8 Instructions Available
- 40-Pin Dual-In-Line Package



P SUFFIX
PLASTIC
CASE 711

PIN ASSIGNMENT

OC4	1	40	$\overline{\text{RESET}}$
OC3	2	39	CLOCK
OC2	3	38	SYNC
OC1	4	37	Tx7
OC0	5	36	Tx6
Rx7	6	35	Tx5
Rx6	7	34	Tx4
Rx5	8	33	V_{DD}
Rx4	9	32	Tx3
V_{SS}	10	31	Tx2
Rx3	11	30	Tx1
Rx2	12	29	Tx0
Rx1	13	28	D7
Rx0	14	27	D6
READY	15	26	D5
$\overline{\text{DTACK}}$	16	25	D4
RS1	17	24	D3
RS0	18	23	D2
R/$\overline{\text{W}}$	19	22	D1
$\overline{\text{CS}}$	20	21	D0

2

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC145610

2

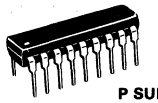
Product Preview

Tone Pulse Dialer with Last Number Redial

The MC145610 silicon-gate CMOS IC converts keyboard inputs into either pulse or DTMF outputs for telephone dialing. All of the features for implementing pulse or DTMF dialing are provided, including 21-digit last number redial in either pulse or DTMF mode.

The MC145610 is pin-compatible with the previously-available MC145410, but has some modifications of features and specifications.

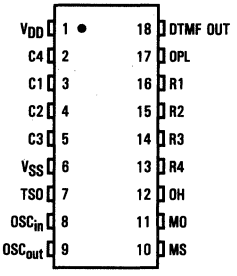
- Stand-Alone Pulse or DTMF Dialer, Pin Selectable Only
- Pacifier Tone Output at Pulse Dialing
- 4 × 4 Keyboard Interface Only
- Uses Low-Cost 3.5795 MHz TV Color Burst Crystal
- PABX Pause Storage
- Manual and LNR Number Can Be Cascaded
- Low Standby Current Typically 0.2 μA at 3.5 V
- 21-Digit Last Number Redial
- Hold Function
- Flash Function for Transfer Call in a PBX Environment



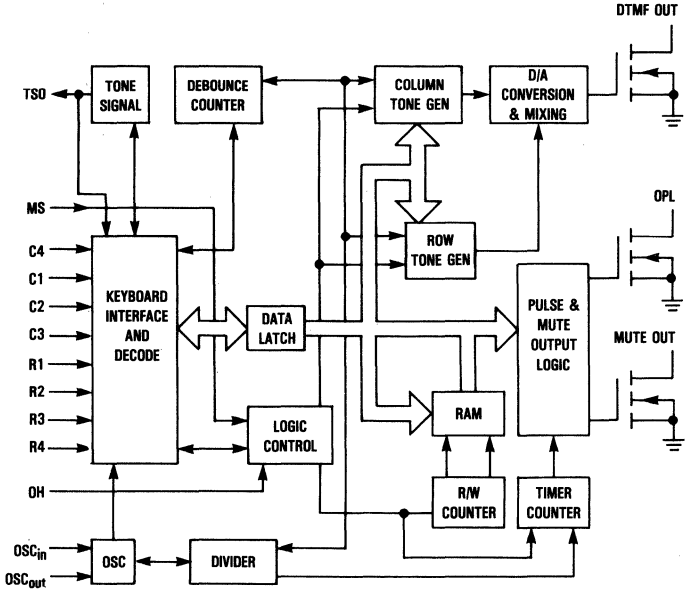
P SUFFIC
PLASTIC
CASE 707

PIN ASSIGNMENT

DIP



BLOCK DIAGRAM



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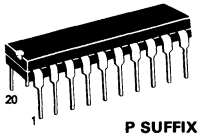
MC145611

Product Preview

PCM Conference Circuit



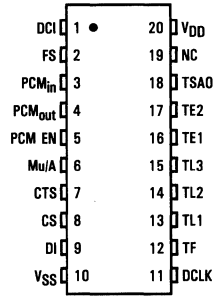
P SUFFIX
PLASTIC
CASE 738

The MC145611 PCM conference circuit is an HCMOS device designed for voice conference in a digital (PCM) telephone switch such as a TDM PABX. The device is capable of providing mixing of up to eight channels (parties) such that every party can hear when one or more parties speak at the same time.

The technique of level priority coding is used. It provides a low cost means of mixing of PCM voice codes for voice conference applicaton.

- 20-Pin Dual-In-Line Package
- Single +5-V Power Supply
- Support Standard Mu-Law or A-Law PCM Codes
- Directly Off the PCM Highways
- 4.096 MHz Clock, 8 kHz Frame Sync and Serial PCM Data Comply with Codec Timing Used in the PABX System
- One-Frame Delay to PCM Data
- Built-In Time Slot Assignment Circuit
- Serial Data with MCU Interface
- 8 Parties Conference in Single Group or Split into Two Groups
- Intrusion Party Channel Time Slot Assignment Provided
- Built-In Maskable Tone Signalling. Tone Level and Frequency External Adjustable

PIN ASSIGNMENT



TCA 3381

TELEPHONE RING SIGNAL IMPEDANCE MATCHING AND PROTECTION CIRCUIT

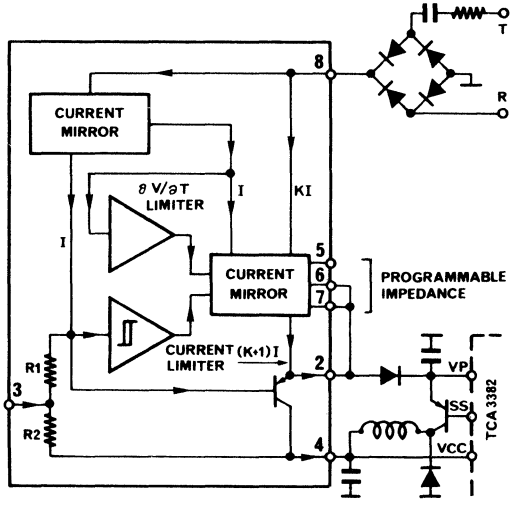
The TCA 3381 Ring Signal Impedance Matching and Protection Circuit is designed for use with the companion TCA 3383A/B Transmission Circuit, and TCA 3382 Telephone Set Speaker Amplifier Circuit. These devices, together with a microcomputer unit form the basis of a fully electronic telephone set. With the telephone on-hook, the TCA 3381 is connected to the line and converts the ring voltage into a current which feeds the TCA 3382. The conversion voltage/current is necessary to decrease the harmonic distortion of the ring signal.

The input impedance of the circuit is programmable so that it can be matched by the designer to the line impedance in order to maximize the available energy in the case of a long line. Five programmed impedance values can be pin-selected, other values by adding external resistors.

The inputs include circuitry to protect the device against overvoltage surges due to lightning and accidental connection to the mains.

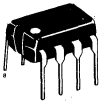
- Line impedance matching, programmable
- Lightning and mains protection
- Voltage/current conversion
- Breakdown voltage 150V

FIGURE 1 – TCA 3381 REPRESENTATIVE CIRCUIT SCHEMATIC



TELEPHONE RING SIGNAL IMPEDANCE MATCHING AND PROTECTION CIRCUIT

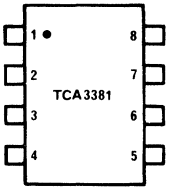
BIPOLAR INTEGRATED CIRCUIT



8 PIN DIL PACKAGE
CASE 626

ORDERING INFORMATION
TCA 3381-DP

Pin Connections



1 – Must not be connected
2 – Z_{output}
3 – Threshold selection
4 – V_{CC}
5 – Z_{adjust}
6 – Z_{adjust}
7 – Z_{adjust}
8 – V_{line}

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

Rating	Symbol	Value	Unit
Line Voltage	V_L	150	V
Operating Ambient Temperature	T_A	– 20 to 60	°C
Storage Temperature	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	150	°C
Thermal Resistance Plastique Package	R_t	65 to 95	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic ($T_A = 25°C$)	Figure	Symbol	Min	Typ	Max	Unit
Input Impedance (T_A = – 20 to +60)	2	Z_L	50 ·R_{ext}	65 ·R_{ext}	75 ·R_{ext}	Ω
$Z_L = \frac{\Delta V_L}{\Delta I_L}$ = impedance	3	Z_L	4.2	4.9	6.2	KΩ
between pin 8 and 4	4	Z_L	4.4	5.2	6.6	KΩ
(Slope between 20 and 80 V)	5	Z_L	5.5	6.5	8.3	KΩ
	6	Z_L	6.6	7.8	10.5	KΩ
	7	Z_L	7.1	8.3	11.0	KΩ
I_L (V_L) Characteristics	9					
Threshold up	10	V_{LU}	110		130	V
Threshold down	10	V_{LD}	90		120	V
Hysteresis	10	V_L	5		30	V
Inhibited current	10	I_{LI}	–		5	mA
Breakdown (I pin8 = 10 mA)	10	V_{BK}	150		–	V
Distortion						
Level of each harmonic	11	L_H	–	–14	0	dBm

FIGURE 2 – INPUT IMPEDANCE

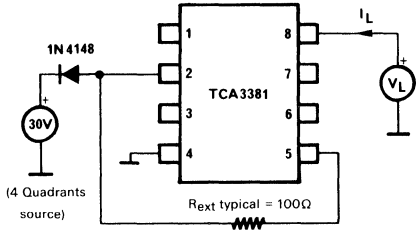


FIGURE 3 – INPUT IMPEDANCE

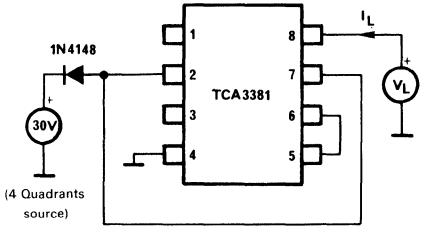


FIGURE 4 – INPUT IMPEDANCE

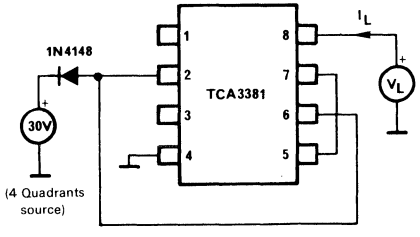


FIGURE 5 – INPUT IMPEDANCE

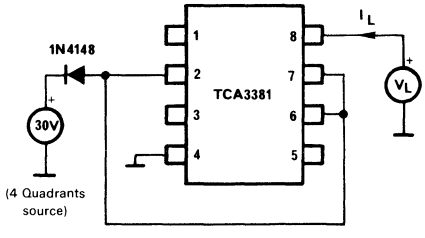


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FIGURE 6 – INPUT IMPEDANCE

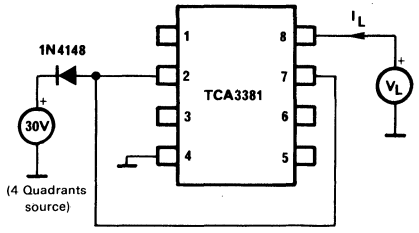


FIGURE 7 – INPUT IMPEDANCE

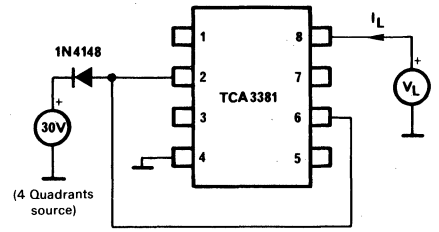


FIGURE 8 – CHOICE OF Z_L

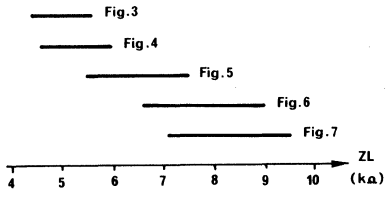


FIGURE 9 – CURRENT/VOLTAGE CHARACTERISTIC MEASUREMENT SET-UP

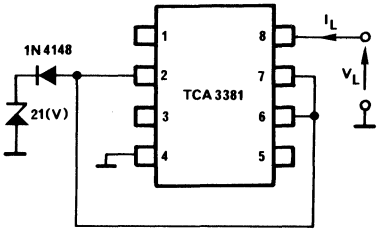
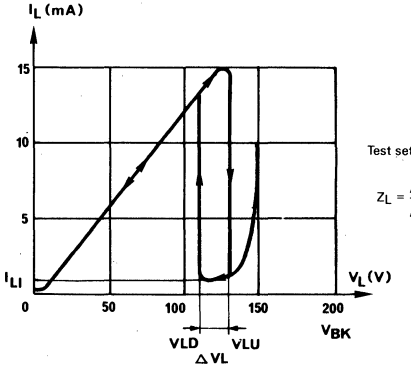


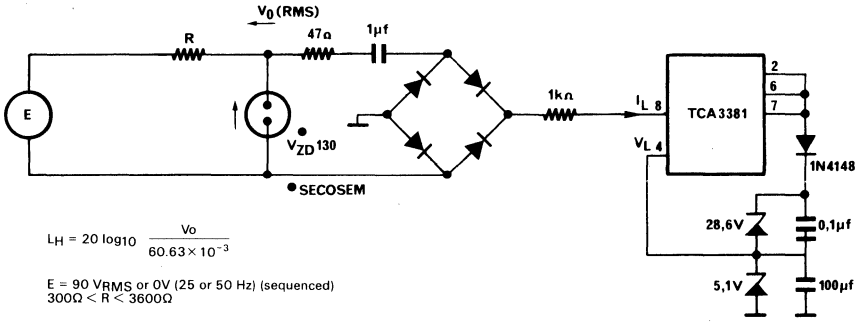
FIGURE 10 – CURRENT/VOLTAGE CHARACTERISTICS



Test set-up like fig. 9

$$Z_L = \frac{\Delta V_L}{\Delta I_L} = \frac{80\text{-}20}{(10.4\text{-}2)\cdot 10^{-3}} = 7143\ \Omega$$

FIGURE 11 – RINGING DISTORTION TEST SET-UP



$$L_H = 20 \log_{10} \frac{Vo}{60.63 \times 10^{-3}}$$

E = 90 V_{RMS} or 0V (25 or 50 Hz) (sequenced)
$300\Omega < R < 3600\Omega$

FIGURE 12 – LIGHTNING PROTECTION MEASUREMENT
as described in TMA/PRL/192 recommendation edited by the CNET-France

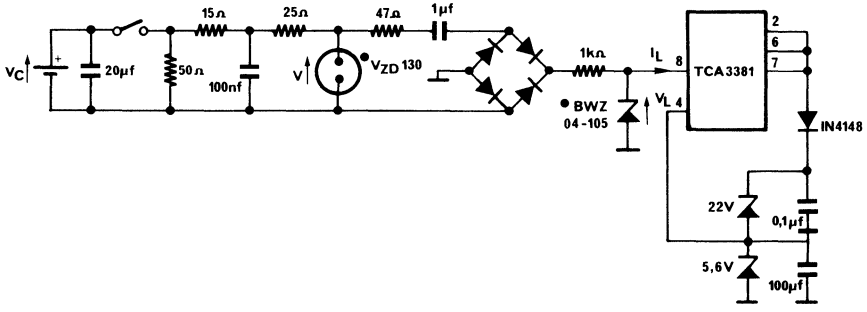


FIGURE 13 – SHAPE OF THE SURGE APPLIED ON THE SPARK-GAP (Fig. 14)

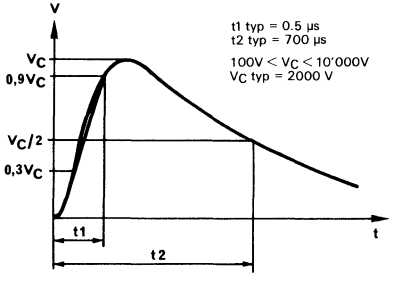
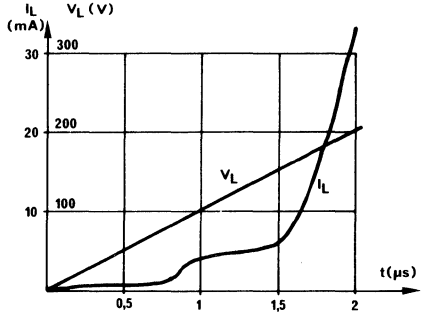


FIGURE 14 – TYPICAL PERFORMANCE UNDER LIGHTNING TEST CONDITIONS (Computer simulation)



TCA 3382
TCA 3382A
TCA 3382B

2

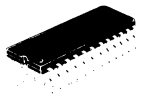
TELEPHONE SET RING DETECTION AND LOUDSPEAKER AMPLIFIER CIRCUIT

The TCA 3382 Telephone Set Speaker Amplifier I.C. is designed for use with the companion TCA 3383 Transmission Circuit, and TCA 3381. These devices together with a microcomputer form the basis of a fully electronic telephone set. With the telephone on-hook, the TCA 3382 detects the presence of a call signal on the line and energy is derived from this signal to power up the system so that a ring melody generated by the microcomputer is heard at the loudspeaker. With the telephone off-hook, the received speech signal is heard at the loudspeaker. Sidetone and line length compensation of the speaker amplifier gain are provided by the TCA 3383.

- Power derived from Ring Signal
- Reset/$\overline{\text{Reset}}$ and $\overline{\text{Ring}}$ outputs for microcomputer
- Amplifier gain controlled by microcomputer
- Guaranteed ring signal detection limits
- On-chip protection against microphone/loudspeaker howl ("Antilarsen")
- TCA 3382 B: Input Voltage of Switching Power Supply (Ring Mode) lower
- TCA 3382 A: Like TCA 3382 B but external feedback for loudspeaker amplifier gain.

TELEPHONE SET RING DETECTION AND LOUDSPEAKER AMPLIFIER CIRCUIT

BIPOLAR INTEGRATED CIRCUIT

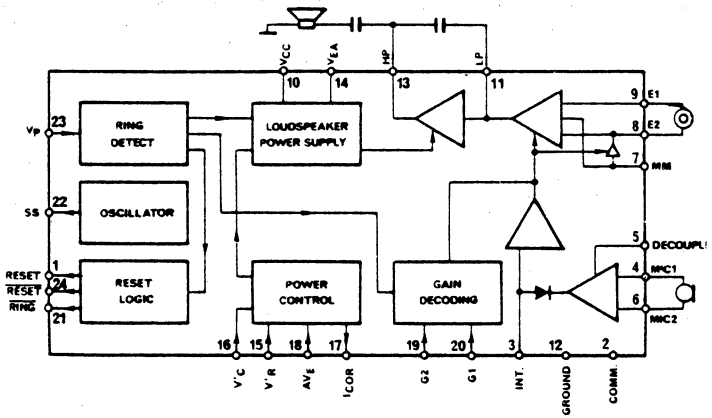


24 PIN DIL PACKAGE

ORDERING INFORMATION:

TCA 3382-DP
TCA 3382A-DP
TCA 3382B-DP

TCA 3382 BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Speech Mode						
1) Inhibited Circuit						
($G_1 = G_2 = 0$: pulled to V_{COMM})						
V_C = 14 V						
V_{CC} Consumption I_{CC}	1	I_{CCOO}	–	300	700	µA
Line Current I_{EA}	1	I_{EAOO}	–	5	100	µA
2) Working Circuit						
($G_1 \neq 0$; $G_2 \neq 0$; G_1 and/or						
G_2 pushed to V_{CC})						
V_{CC} Consumption ($G_1 = G_2 = 1$)	1	I_{CC11}	–	600	800	µA
V_{CC} Consumption ($G_1 = 0$; $G_2 = 1$)	1	I_{CC01}	–	1.1	1.6	mA
a) A_{VE} = 2 V						
Line Current (I_{EA})	1	I_{EA2}	–	100	500	µA
Line Current Correction (I_{COR})	1	I_{COR2}	–	0.5	1	µA
b) A_{VE} = 2.9 V						
Line Current (I_{EA})	1	I_{EA29}	5.5	7	9.5	mA
Correction Ratio: $k = I_{EA}/I_{COR}$	1	k_{29}	530	550	600	None
Amplifier Power Supply (V_{EA})	1	V_{EA29}	V_{CC}–1	V_{CC}–0.6	V_{CC}	
c) A_{VE} = 3.25 V						
Line Current (I_{EA})	1	I_{EA325}	7	10	14	mA
Correction Ratio: $K = I_{EA}/I_{COR}$	1	K_{325}	530	550	610	None
Amplifier Power Supply (V_{EA})	1	V_{EA325}	V_{CC}–1	V_{CC}–06	V_{CC}	
d) A_{VE} = 3.55 V						
Line Current ($\overline{I_{EA}}$)	1	I_{EA355}	10	12	17	mA
Correction Ratio: $k = I_{EA}/I_{COR}$	1	K_{335}	530	560	610	None
Amplifier Power Supply (V_{EA})	1	V_{EA355}	V_{CC}–1	V_{CC}–0.6	V_{CC}	
e) A_{VE} = 6.0 V						
Line Current (I_{EA})	1	I_{EA6}	11	14	18	mA
Correction Ratio: $k = I_{EA}/I_{COR}$	1	K6	530	570	620	None
Amplifier Power Supply (V_{EA})	1	V_{EA6}	6.5	7.5	8.5	V
3) Any G_1, G_2						
Reference Voltage Input Bias	1	$I_{V'R}$	–	15	200	nA
Line Length Sense Input Bias	1	I_{AVE}	–	10	200	nA
Earphone Input Bias E_1	1	I_{E1}	–	10	50	µA
Earphone Input Bias E_2	1	I_{E2}	–	10	50	µA
Microphone Input Bias	1	I_M	–	0.05	1	µA
4) Gain Control						
Logical "0" Level (G_1 or G_2)		V_{G0}	V_{COM}	–	V_{com} +0.4	V
Logical "1" Level (G_1 or G_2)		V_{G1}	V_{CC}–1	–	V_{CC}	V
Bias Current at Logical "0" (G_1 or G_2)		$\lvert I_{G0} \rvert$	–	1	10	µA
Bias Current at Logical "1" (G_1 or G_2)		$\lvert I_{G1} \rvert$	–	35	100	µA
5) Ringing Information Off						
V_{RING}	1	V_{RGS}	V_{CC}–0.4	V_{CC}–0.1	V_{CC}	V
6) Amplified Speech Gains						
$G_1 = G_2$ = "1"						
•TCA 3382 – TCA 3382 B	2	G_{AS11}	18	20	22	dB
•TCA 3382 A	2	G_{AS11}	23	27	31	dB
a) Gain Variation (Ref. $G_1 = G_2 = 1$)						
G_1 = "1"; G_2 = "0"	2	ΔG_{AS10}	5	7	9	dB
G_1 = "0"; G_2 = "1"	2	ΔG_{AS01}	13	15	17	dB
b) Inhibited Amplified Speech						
G_1 = "0"; G_2 = "0"						
•TCA 3382 – TCA 3382 B	2	G_{AS00}	–	–30	–20	dB
•TCA 3382 A	2	G_{AS00}	–	–25	–15	dB
7) Max. Power on Loudspeaker						
$G_1 = G_2$ = "1"; Distortion ≤ 3%	2	P_L	500	600	–	mV_{RMS}

2

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Speech Mode						
8) "Larsen" Effect Cancellation						
a) $V_{M2} \leq 0.1$ mV Peak						
•TCA 3382 – TCA 3382 B	3	G_{AS11A0}	18	20	22	dB
•TCA 3382 A	3	G_{AS11A0}	23	27	31	dB
b) $V_{M2} \geq 0.8$ mV Peak						
•TCA 3382 – TCA 3382 B	3	G_{AS11A1}	–	–4	0	dB
•TCA 3382 A	3	G_{AS11A1}	–	3	8	dB
9) Amplified Melody/Supervision						
a) $G_1 = G_2$ = "1"						
Gain to Loudspeaker						
•TCA 3382 – TCA 3382 B	4	G_{AM11}	4	7	10	dB
•TCA 3382 A	4	G_{AM11}	9	14	19	dB
Gain to Earphone						
•TCA 3382 – TCA 3382 B	4	G_{AME11}	–	–60	–30	dB
•TCA 3382 A	4	G_{AME11}	–	–55	–25	dB
b) $G_1 = G_2$ = "0" (Long Test)						
Gain to Loudspeaker						
•TCA 3382 – TCA 3382 B	4	G_{AM00}	4	7	10	dB
•TCA 3382 A	4	G_{AM00}	9	14	19	dB
Gain to Earphone						
•TCA 3382 – TCA 3382 B	4	G_{AME00}	–23	–17	–11	dB
•TCA 3382 A	4	G_{AME00}	–23	–17	–11	dB
c) Gain Variation (Loudspeaker)						
Reference $G_1 = G_2$ = "1"						
G_1 = "1"; G_2 = "0"	4	ΔG_{AM10}	1	4	7	dB
G_1 = "0"; G_2 = "1"	4	ΔG_{AM01}	8	11	15	dB
Microprocessor Protection						
Limitation of $V_{CC} - V_{COM}$	5	V_{ALM}	5.2	5.6	6	V
Start-Up Information						
1) $V_{CC} - V_{COM}$ = 3.2 V						
V_{RESET}	6	V_{RST1}	V_{CC}–0.4	–	V_{CC}	V
$V_{\overline{RESET}}$	6	V_{RSTNO}	V_{COM}	–	V_{COM}+0.4	V
$V_{\overline{RING}}$	6	V_{RGL32}	V_{CC}–0.4	–	V_{CC}	V
2) $V_{CC} - V_{COM}$ = 3.7 V						
V_{RESET}	7	V_{RSTO}	V_{COM}	–	V_{COM}+0.4	V
$V_{\overline{RESET}}$	7	V_{RSTN1}	V_{CC}–0.4	–	V_{CC}	V
$V_{\overline{RING}}$	7	V_{RGL37}	V_{CC}–0.4	–	V_{CC}	V
Ringing						
1) Ringing Information						
a) I = 2.8 mA; $V_{\overline{RING}}$	8	V_{RG1}	V_{CC}–04	–	V_{CC}	V
b) I = 8.5 mA; $V_{\overline{RING}}$	8	V_{RG0}	V_{COM}	–	V_{COM}+0.4	V
2) Max. Loudspeaker Power						
I = 14 mA; V_{MM} = 1 kHz Large Square Waves Signal						
V_{HP} peak to peak						
•TCA 3382	8	P_{LR}	2.8	3	–	V
•TCA 3382 A – TCA 3382 B	8	P_{LR}	2.4	2.7	–	V
3) Amplified Melody (I = 8.5 mA)						
a) $G_1 = G_2$ = "1"; Gain to Loudspeaker						
•TCA 3382 – TCA 3382 B	8	G_{AMR11}	3	6	9	dB
•TCA 3382 A	8	G_{ARM11}	9	13	17	dB
b) Variations to Loudspeaker						
Reference $G_1 = 1$; $G_2 = 1$						
G_1 = "1"; G_2 = "0"	8	ΔG_{AMR10}	8	11	14	dB
G_1 = "0"; G_2 = "1"	8	ΔG_{AMR01}	20	24	28	dB
4) Input Switching Power Supply						
I = 8.5 mA; V_p						
•TCA 3382	8	V_p	26	28.5	31	V
•TCA 3382 A – TCA 3382 B	8	V_p	19	22	25	V
5) Correction Saturation						
I = 8.5 mA; V_{ICOR}	8	V_{ICOR}	0	–	0.8	V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Ambient Temperature	T_A	−20 to +60	°C
Storage Temperature	T_S	−65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Thermal Resistance (Plastique Package)	R_θ	70 to 95	°C/W

CIRCUIT DESCRIPTION

On-hook mode

In this mode, the functions realized by the TCA 3382 are:

- Threshold detection of a ring signal current, normally provided by the TCA 3381, establishing the power for the microcomputer via the TCA 3383 power supply output.
- Logic signals $\overline{\text{RING}}$, RESET and $\overline{\text{RESET}}$ for the microcomputer.
- Amplification to the loudspeaker of a ring melody signal (square waves) generated by the microcomputer.
- Control of amplifier gain by two bits from microcomputer.

In this mode of operation, the current consumption of the TCA 3383 is limited to 600 μA typically in order to allow the maximum of power to drive the loudspeaker.

The ring melody applied on pin 7 is active when the signal reaches 1.5 V above COMM (pin 2). Above this level an audio signal on this pin is transmitted analogically to the HP output (loudspeaker) and to the earphone. Below this level the HP output maintains a steady DC level equal to $V_{CC}/2$ ($V_{EA}/2$ in Off-Hook mode).

Off-hook mode

In this mode, the 3382 is powered by the TCA 3383 and provides a voice signal amplification. The voice signal inputs (pin 8,9) are directly connected to the earphone output pin 4 and 5 of the TCA 3383.

The mean current of the output amplifier (pin 13) is controlled as a function of the line length by the TCA 3383 and, due to I_{COR} (pin 17) the total current consumption of the system respects the same limits of line current/voltage characteristic as the TCA 3383 transmission circuit alone (see TCA 3383 data sheet, fig. 8). The gain of the speaker amplifier can be set by two logic inputs G_1, G_2 (pin 20,19). If $G_1 = G_2 = 0$, the speaker amplifier is turned off.

The power delivered to the loudspeaker is a function of the line length and the loudspeaker impedance (50 Ω recommended). A system (Antilarsen) minimizes the howling caused by mic./speaker coupling.

TCA 3382 PIN DESCRIPTION

V_{CC} : Positive power supply, voltage controlled externally e.g. by TCA 3383 (pin 28). Amplifier power supply in ring mode.

GROUND : Most negative voltage of line bridge.

COMM : Digital ground. Regulated 4V supply is provided between V_{CC} and V_{COMM} by TCA 3383 in Off-Hook mode.

V_P : Ring signal sense input (Switching power supply input).

SS : Switched supply. A square wave signal (50 kHz typically) appears between V_P and SS for switch-mode power supply to external PNP transistor.

V_{EA} : Amplifier power supply in amplifier speech mode, derived from V'c.
Must be decoupled by a grounded capacitor.

V'c : Unregulated supply from pin 15 of TCA 3383.

AVE : Part of DC line voltage needed for loudspeaker amplifier peak current limiting as function of line length. Must be connected to pin 17 of TCA 3383.

V'R : Input: 2.4 V provided by TCA 3383 as a reference for current limiting as function of line length, connected to pin 25 of TCA 3383.

I_{COR} : DC current feedback to pin 13 of TCA 3383 providing a compensation to retain same line current/voltage characteristic when TCA 3382 is connected.

DECOUPLE : Decoupling capacitor to COMM for sidetone cancellation by howling effect.

INT. : Connection for integrator capacitor for microphone sidetone reduction and minimisation of howling caused by mic./speaker coupling.

MM : External ring melody inputs.

HP : Loudspeaker output. Typically loaded by 50 Ω.

LP : Connection for external feedback between LP and HP (TCA 3382 only). This feedback is internal (typ. 220K) in TCA 3382 and TCA 3382 B.

MIC1, MIC2 : Microphone inputs for howling effect sensing.

E1, E2 : Earphone inputs for amplified speech.

G1, G2 : Logic inputs for gain control of loudspeaker amplifier.

RESET, $\overline{\text{RESET}}$: Push-Pull outputs saturated to V_{CC} or V_{COMM} logic signals for microcomputer initialisation or re-initialisation.
RESET follows V_{CC} if ($V_{CC} - V_{COMM} < 3.4$ V (typ.)
RESET = V_{COMM} for ($V_{CC} - V_{COMM} > 3.4$ V (typ.)
$\overline{\text{RESET}}$ = V_{COMM} for ($V_{CC} - V_{COMM} < 3.4$ V (typ.)
$\overline{\text{RESET}}$ follows V_{CC} if ($V_{CC} - V_{COMM} > 3.4$ V (typ.)

$\overline{\text{RING}}$: Open collector output saturated to V_{COMM} during ring signal. MUST be pulled up.

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BASIC TEST CIRCUIT

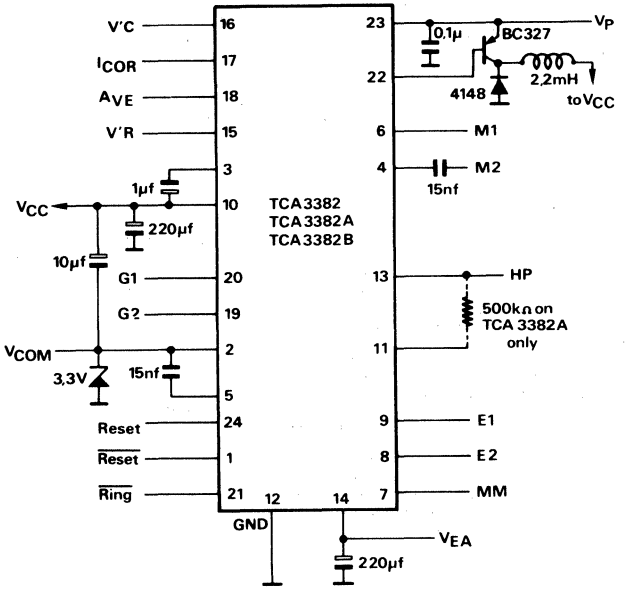

FIGURE 1 – SPEECH MODE CURRENTS/VOLTAGES MEASURES

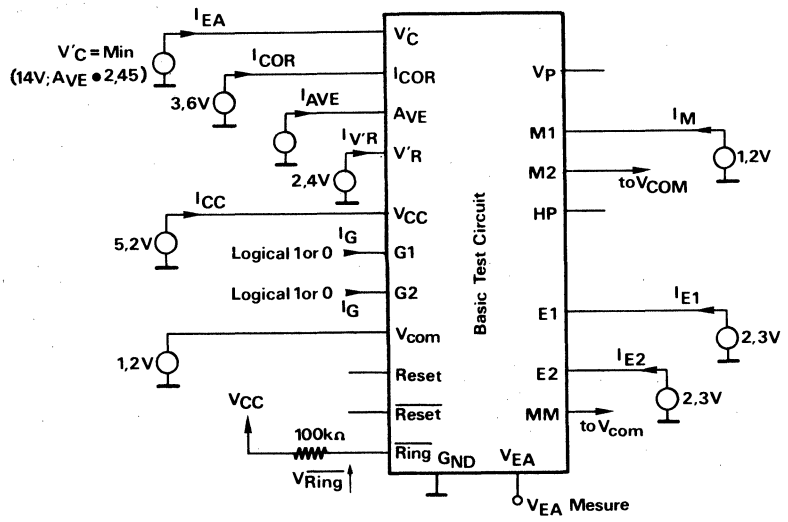

FIGURE 2 – SPEECH GAINS/MAX. LOUDSPEAKER POWER

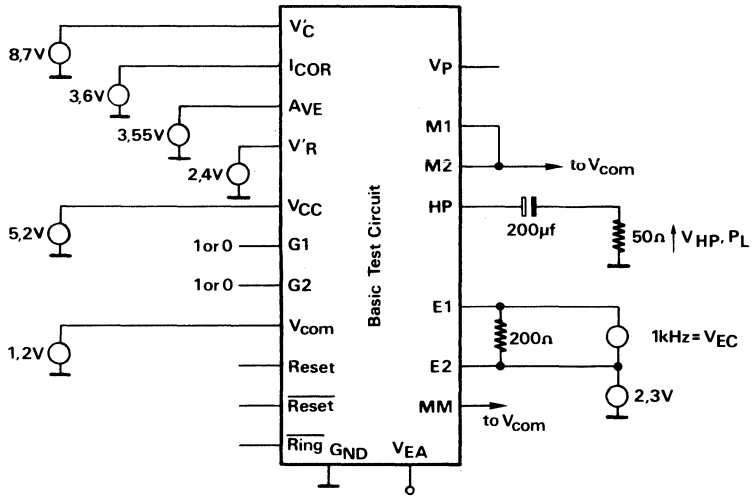

FIGURE 3 – ANTILARSEN

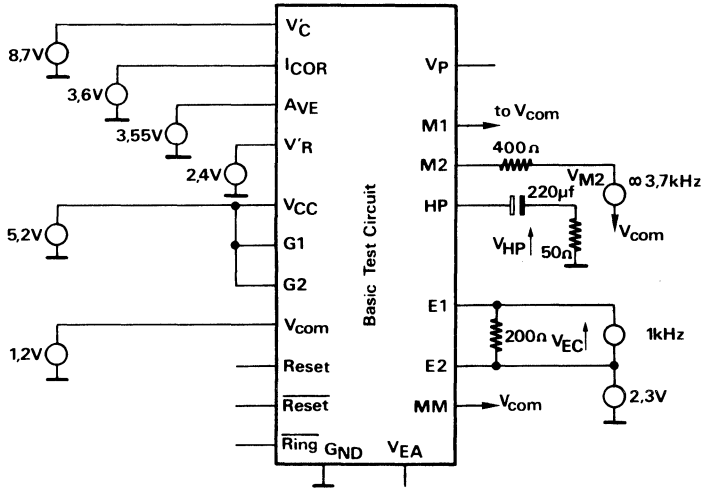

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FIGURE 4 – AMPLIFIED MELODY

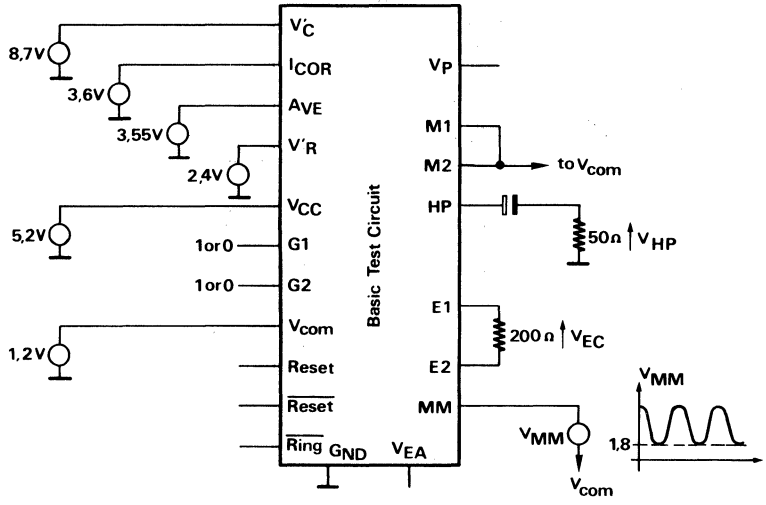

FIGURE 5 – LIMITATION OF V_{AL}

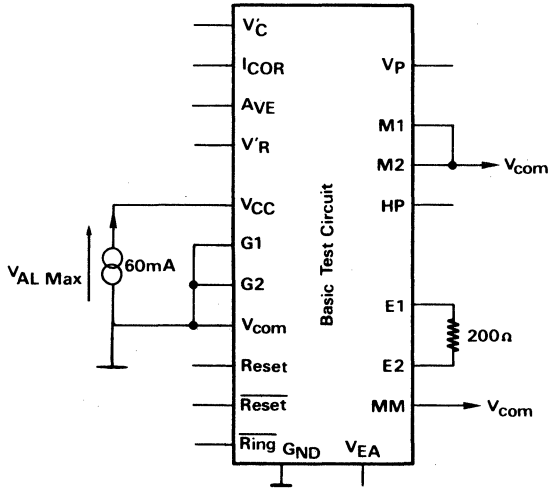

FIGURE 6 – RESET, $\overline{\text{RESET}}$, $V_{\overline{\text{RING}}}$ for V_{AL} = 3.2 V

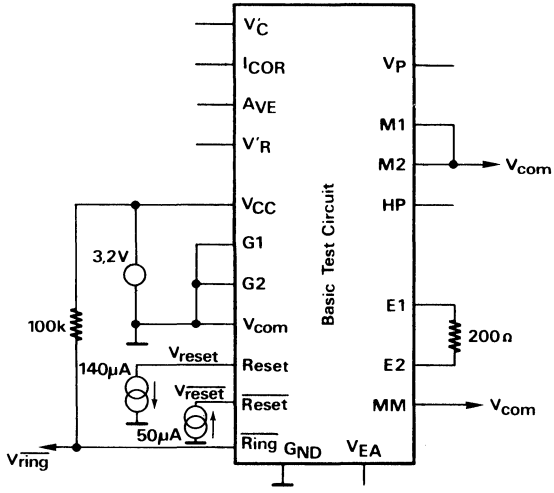

FIGURE 7 – RESET, $\overline{\text{RESET}}$, $V_{\overline{\text{RING}}}$ for V_{AL} = 3.7 V

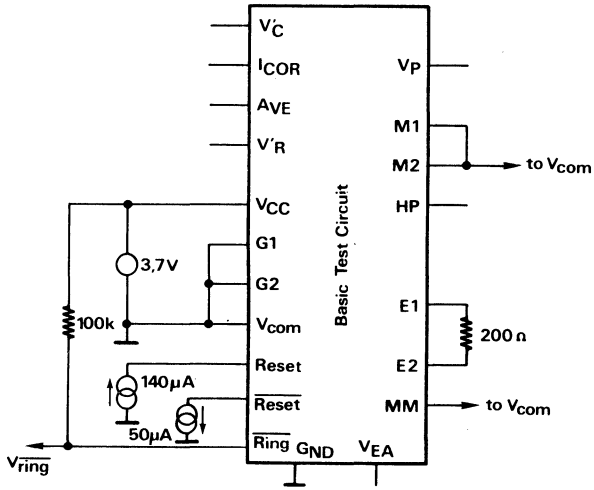

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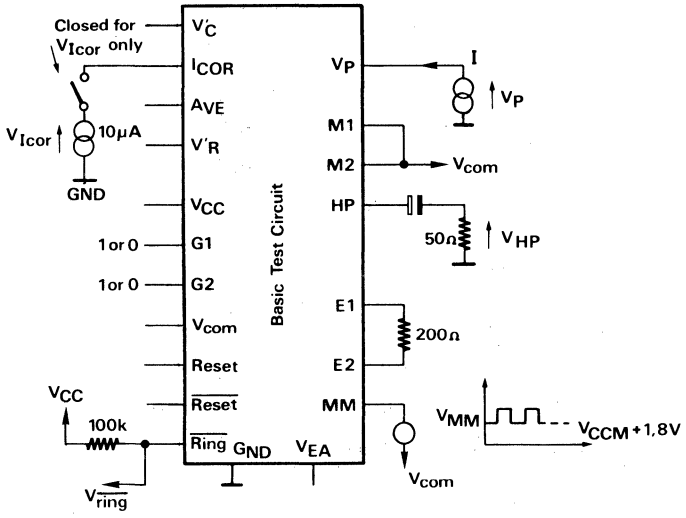
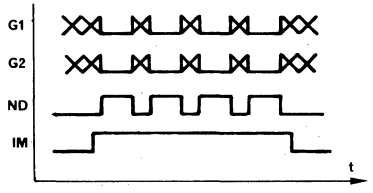
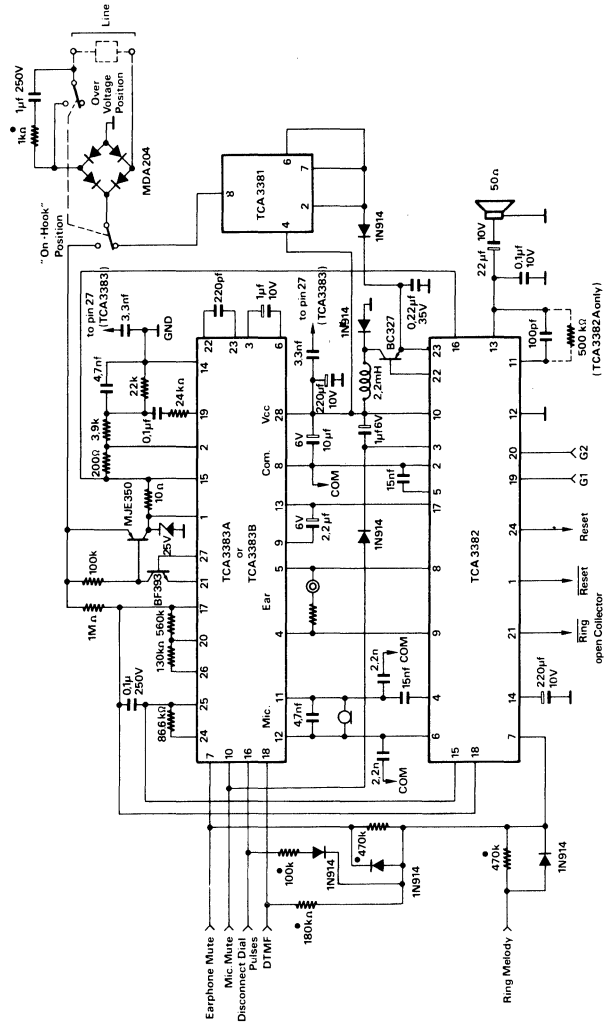
FIGURE 8 – RINGING





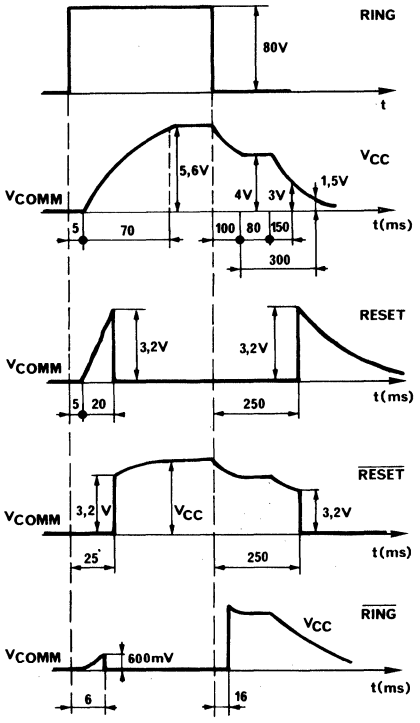
TIMING EXAMPLE

Disconnect dial pulse ("4") output (ND) from the microcomputer. Microinhibit (IM) can go low with ND (or MF) but not before. G1, G2 should be different from 0,0 between train of pulses in order to load the capacity c1 (see application circuit).



❶ ALL RESISTORS 1% EXCEPT (●) = 5%
❷ AVOID TANTALUM CAPACITORS
❸ RECOMMENDED EARPHONE IMPEDANCE: 200Ω (WITHOUT SERIAL RESISTOR)
❹ ALL LOGIC SIGNALS REFERENCED TO COM (INCLUDING DTMF) ↓

2


RING
80V
t
VCC
5,6V
1,5V
4V
3V
VCOMM
5
70
100
80
150
300
t(ms)
RESET
3,2V
3,2V
VCOMM
5
20
250
t(ms)
RESET
3,2
V
VCC
3,2V
VCOMM
25
250
t(ms)
RING
VCC
VCOMM
600mV
6
16
t(ms)

TCA 3383 A/B

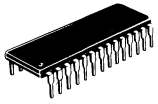
TELEPHONE SET TRANSMISSION CIRCUIT

The TCA3383A and TCA3383B telephone set transmission circuits replace the hybrid transformer in a telephone set, include transmit and receive amplifiers and provide line matching and sidetone cancellation. Automatic gain control is available for line length compensation. Together with companion TCA3381 and TCA3382, plus a CMOS microcomputer, a fully electronic telephone set with loudspeaker amplified reception can be built.

- Nominal transmit and receive gains accurate to ±1 dB
- Automatic preset sidetone network adjustment, compensates for line length variations
- Optional microphone and earphone amplifier automatic gain control to compensate variations in line length
- Regulated D.C. output to power external circuitry
- Multifrequency or Loop Disconnect Dialling Inputs
- Mute facility for transmit and receive amplifiers
- Low noise
- Low current consumption.

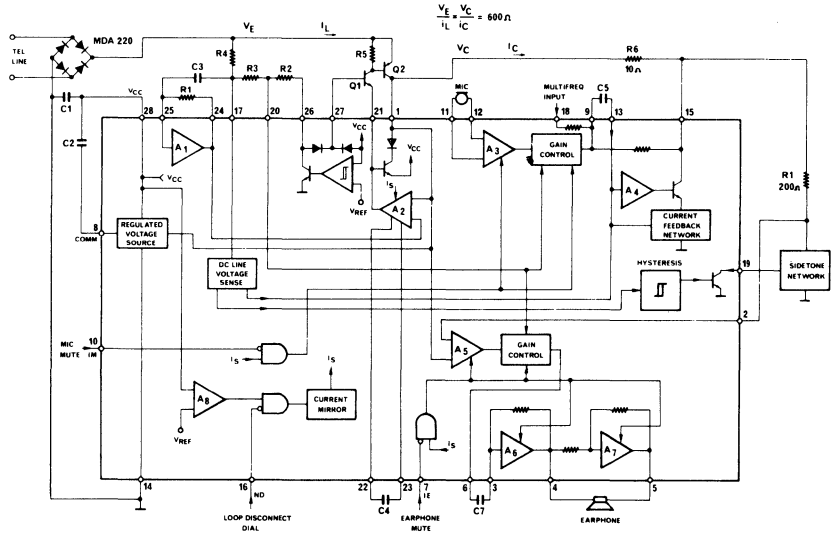
TELEPHONE SET TRANSMISSION CIRCUIT

BIPOLAR INTEGRATED CIRCUIT



28 PIN DIL PACKAGE
Ordering Information:
TCA3383A-DP/TCA3383B-DP

TCA 3383 BLOCK DIAGRAM



2

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Ambient Temperature	T_A	−20 to +60	°C
Storage Temperature	T_S	−65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Thermal Resistance: Plastic Package	R_T	80 to 110	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Start-up Characteristics (I_{CH} = 1mA max)	2					
Line current (V_E >10V)		I_{LD}	28	120	150	mA
Q_2 Emitter voltage (I_{LD} <28 mA)		V_{ED}	–	4.6	5.6	V
Start-up delay time	13	t_D	150	–	350	ms
(C_1 = 220 µF, C_5 = 2,2 µF)						
Power Supply Characteristics	2					
(−25°C ≤ T_A ≤ 70°C, I_{CH} = 1 mA)						
Line current (V_E > 11 V)		I_L	27.5		57.5	mA
Q2 Emitter voltage		V_E				
I_L = 15 mA			–	6.3	6.9	V
I_L = 25 mA			–	7.8	10.9	V
Regulated supply:						
Voltage (V_{AL} = V_{CC} − V_{COM})		V_{AL}	3.8	4	4.2	V
Regulation (0 < I_{CH} < 3 mA)		ΔV_{AL}	–	10	80	mV
Internal supply:						
Voltage (I_{CH} = 0)		V_{CC}	4.8	5.2	5.6	V
Regulation (0 < I_{CH} < 5 mA)		ΔV_{CC}	–	500	–	mV
Output impedance (0 < I_{CH} < 5 mA)		Zout	–	150	300	Ω
Transmit Gain						
(300-3400 Hz)						dB
TCA 3383 A	3					
Nominal gain, DC Resist. = 1280 Ω, 0 dBm on line		G_{EN}	45.5	46.5	47.5	
Short line gain, DC Resist. = 300 Ω, 0 dBm on line		G_{EC}	39	41	43	
TCA 3383 B						
Nominal Gain, DC Resist. = 1280 Ω, 0 dBm on line		G_{EN}	51.5	52.5	53.5	
Short line gain, DC Resist. = 300 Ω, 0 dBm on line		G_{EC}	45	47	49	
Receive Gain	4					
(300-3400 Hz)						dB
Nominal gain, DC Resist. = 1280 Ω − 10 dBV receive level		G_{RN}	3	4	5	
Short line gain, DC Resist. = 300 Ω, − 10 dBV receive level		G_{RC}	−4.5	−2.5	−0.5	
Line Terminating Impedance	4					
(I_L ≥ 18 mA)						
300 − 500 Hz		Z_p	360	600	1000	Ω
500 − 3400 Hz		Z_p	450	600	750	
Microphone Amplifier Input Impedance	3					
300 − 3400 Hz TCA 3383 A		Z_E	350	400	450	Ω
TCA 3383 B			9000	14000		
Earphone Amplifier Output Impedance	4					
300 − 3400 Hz		Z_R	–	3	10	Ω
Common Mode Rejection						
Receive amplifier	5	R_{RCM}	–	65	–	dB
Microphone Muting	3					
Gain reduction (300-3400 Hz, I_L ≥ 18 mA, 0dBm, V_{IM} ≥ V_{IMH} min.)		A_{HM}	−60	−71	–	dB
Mute level "High" (COMM = Reference)		V_{IMH}	V_{AL} −0.8	–	–	V
Mute level "Low" (COMM = Reference)		V_{IMB}		–	0.8	V

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Earphone Muting						
Gain reduction	4	A_{HR}	−60	−69	–	dB
(300-3400 Hz, I_L > 18 mA, −10 dBV, $V_{IE} > V_{IEH}$)						
Mute level "High" (COMM = Reference)		V_{IEH}	V_{AL} −0.8	–	–	V
Mute level "Low" (COMM = Reference)		V_{IEB}	–	–	1.5	V
Logic Ports Input Current						
IM, IE, ND	3,4	I	–	1	50	µA
Dialling Input Characteristics	3,4					
Input "High"		V_{NDH}	V_{AL} −0.8	–	–	V
Input "Low"		V_{NDB}	–	–	0.8	V
Open loop line current (V_E = 46.5V)		I_{LD}	–	45	150	µA
Switching of Sidetone Network Resistors	6					
Q_2 Emitter voltage, β off		V_{EIOFF}	10.5	11.2	–	V
Q_2 Emitter voltage, β on		V_{EION}	–	11.2	13	V
"ON" Resistance β (300-3400 Hz)		R_{ONR}	–	–	2	KΩ
"OFF" Resistance β (300-3400 Hz)		R_{OFFR}	100	–	–	KΩ
Transmit Harmonic Distortion RBC < 1280 Ω	3	d_E				
Line level +3 dBm (F = 1kHz)			–	0.4	3	%
Line level +6 dBm (F = 1kHz)			–	–	10	%
Receive Harmonic Distortion	4	d_R				
RBC < 1280 Ω, R_{phone} = 200 Ω)						
Receive level −11.5 dBV (F = 1 kHz)			–	1.5	3	%
Receive level −10 dBV (F = 1 kHz)			–	–	10	%
Receive Noise	2	B_R	–	–	500	µV
Transmit Noise (e = 0V, DCR = 300 Ω)	3	B_E	–	–	−64	dBmp
MF Input Gain						
Pin 18 to line (600 Ω)	7	G_{MF}	4.0	5.0	6.0	dB
MF Input Impedance	7	Z_{MF}	50	80	110	KΩ
Side Tone Cancellation	3					
F = 300 − 3400 Hz	3					
DCR = 1280 Ω						
− 10 dBV (316 mV_{RMS}) on line		G_{ST}	–	−38	−32	dBV

Note: The line voltage is equal to the voltage on the emitter of Q_2 (V_E) plus the forward voltage drop across the diode bridge (max. 1.5 V).

TCA3383A/B TELEPHONE SET TRANSMISSION CIRCUITS

CIRCUIT DESCRIPTION (See block diagram)

The TCA3383 A/B bipolar integrated circuits interface the microphone and earphone of a telephone set to the two-wire circuit of the telephone line. Controlled gain amplifiers are included for the microphone signal output to the line and the incoming line signal to the earphone. Automatic switching between two preset sidetone networks* is available and inputs are available for either multifrequency (DTMF) or loop disconnect dialling.

DC SUPPLY (See block diagram)

Power for the IC is derived from the line via external transistor Q_2 and pin 1, which supply current to the V_{CC} rail internally.

C_1 is a smoothing capacitor for the unstabilised 5V supply voltage V_{CC} (pin 28 − pin 14). The 4V stabilised supply between COMM and V_{CC} (pin 28 − pin 8) is smoothed by C_2. Power is available for external circuitry such as DTMF generator, MCU, etc.

In the start-up condition immediately after connection to the line C_1 (V_{CC}) is charged rapidly by biasing Q_2 on via Q_1, which in turn is biassed on by the resistor network R_4, R_3, R_2 and the internal circuitry on pins 26, 27. Fig. 8 shows the typical line current vs line voltage characteristic of the circuit and fig. 9 shows the typical regulation of the supply voltages (pins 28,8) as a function of external load current.

2

CONTROLLED GAIN

The gain of the microphone amplifier and earphone amplifier can be automatically controlled by the D.C. level on the line by the divider R_3/R_2 on pin 20. Additionally, the DC line voltage sensed at pin 17 is used to switch in or out additional resistors in the sidetone network to obtain preset levels of sidetone cancellation as a function of line length.

Fig. 11 shows how to suppress, with two diodes, the AGC for microphone and earphone if the compensation in line length is not needed.

The variation in amplifier gains between different units under given conditions is tightly controlled in manufacture – nominal gain variation in transmission is ±1 dB max, so that the performance in a given system is well defined.

MUTE FUNCTIONS

Separate microphone and earphone muting is provided through pins 10 and 7 respectively if they are logic level "high".

Muting is also provided during the start-up delay time.

DIALLING

Loop disconnect dialling pulses can be applied at pin 16 ("High" to disconnect). In order to avoid dial clicks, the earphone and the microphone amplifiers ought to be muted externally by applying a logic "1" on pin 7 and 10.

The line current is interrupted by switching of the transistor Q_1 which obtains emitter drive from amplifier A_2, which in turn derives its supply current from the current mirror controlled by the AND gate at pin 16.

Multifrequency dialling tones can be transmitted to the line via pin 18, which is linked internally to pin 9 via a 80k resistor.

*See application circuit: R8 serial + R9, C6 parallel to ground when beta OFF or R8 serial + R9, C6, R11 parallel to ground when beta ON (short line)

PIN DESCRIPTION

Pin 1: V_C	Low voltage line image
Pin 2: V''_C	Speech signal to earphone
Pin 3: V_{EAR}	Negative input of earphone amplifier
Pin 4, 5: E1, E2	Earphone connections
Pin 6: E_{CONT}	Speech signal to earphone, controlled in function of line length
Pin 7: IE	Inhibit earphone (Active "High")
Pin 8: COMM	Internal reference. External available ground.
Pin 9: I_{AC}	Input of AC line current amplifier
Pin 10: IM	Inhibit microphone (Active "High")
Pin 11, 12: M1, M2	Differential input for 2-wires microphone
Pin 13: I_{COR}	Input of DC line current controller
Pin 14: GROUND	Most negative voltage
Pin 15: V'_C	Analog signal output to line. Line terminating impedance matching
Pin 16: ND	Loop disconnect dial pulses input ("High" to disconnect)
Pin 17: AV_E	DC line voltage sense input
Pin 18: MF	DTMF input
Pin 19: Beta	Open collector output to switch sidetone network with regard to line length
Pin 20: V_{CONT}	Part of DC line voltage for gain control of microphone and earphone amplifiers with regard to line length and Controlling DC part
Pin 21: I_{REG}	Current line regulation control
Pin 22, 23: C1, C2	Connection of an external capacity (typ. 470 pF) for internal stability
Pin 24: V_{AC}	Op-amp output for AC impedance transfer
Pin 25: V'_R	Op-amp negative input for AC impedance transfer
Pin 26: V_{DEM}	Internally input connected to ground, except during start-up phase, providing then the control on external transistor Q1
Pin 27: V'_{DEM}	Output to be connected to the base of external transistor Q1 start-up characteristic
Pin 28: V_{CC}	Positive supply, regulated to 4.0 V between V_{CC} and COMM

FIGURE 1 – BASIC TEST CIRCUIT

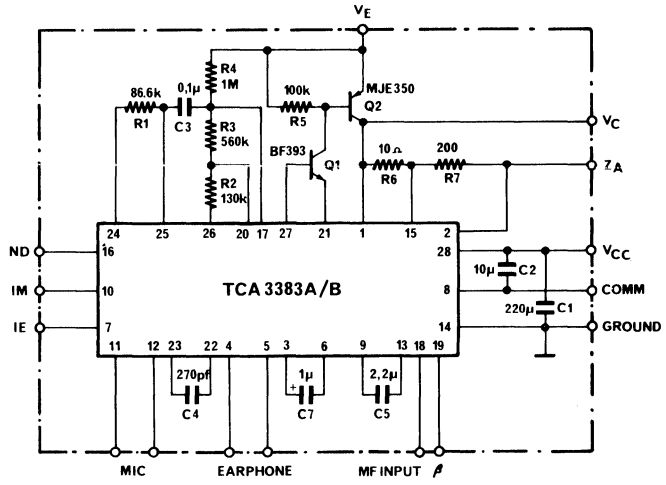


FIGURE 2 – I_{LD}, V_{ED}, t_D, I_L, V_E, V_{AL}, V_{CC}, BR TESTS

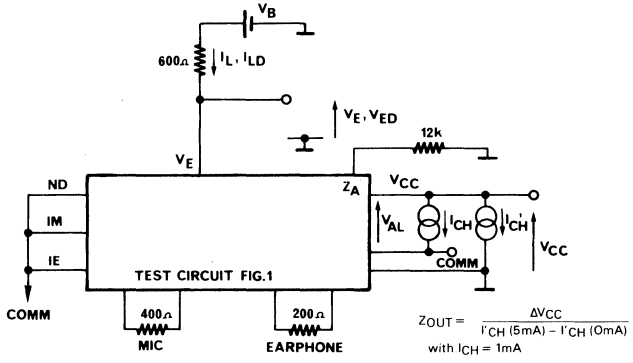


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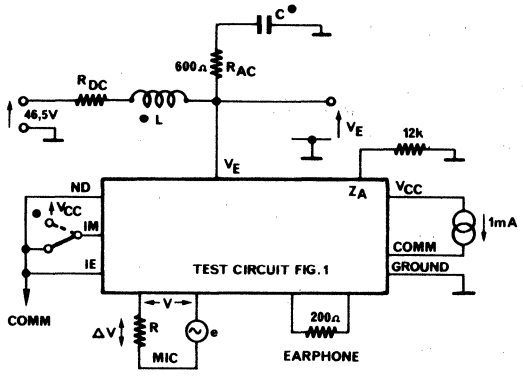
FIGURE 3 – G_{EN}, G_{EC}, Z_E, A_{HM}, V_{IMH}, V_{IMB}, B_E TESTS

$G_{EN} = G_E$ for nominal lines
$G_{EC} = G_E$ for short lines



● $L\omega >> 600\ \Omega$

$1/C\omega << 600\ \Omega$

$$A_{HM} = 20 \log \frac{U_E\ (I_M = 0)}{U_E\ (I_M = 1)}$$

$$G_E = 20 \log \frac{U_E}{e}$$

$$Z_E = \frac{V_{MIC} \cdot R^*}{\Delta V}$$

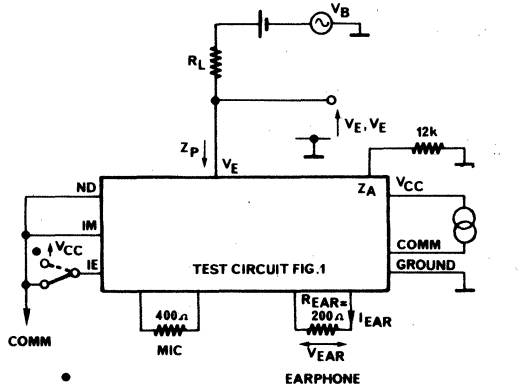
* R = 400 Ω for TCA3383A
R = 14000 Ω for TCA3383B

$$G_{ST} = 20 \log \frac{U_{EAR}}{1\ V}$$

(Note: A_{HM}, G_E, B_E, G_{ST} with R = 400 Ω)

FIGURE 4 – G_{RN}, G_{RC}, Z_P, Z_R, A_{HR} TESTS

$G_{RN} = G_R$ for nominal lines
$G_{RC} = G_R$ for short lines



$$A_{HR} = 20 \log \frac{U_{EAR}\ (I = 0)}{U_{EAR}\ (I = 1)}$$

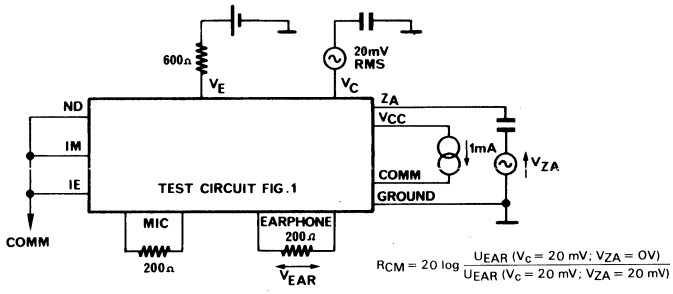
$$G_R = 20 \log \frac{U_{EAR}}{U_E}$$

$$Z_P = \frac{R_L\ U_E}{V_B - U_E}$$

$$Z_R = \frac{400\ (U_{EAR}\ (400) - U_{EAR}\ (200)}{2\ U_{EAR}\ (200) - U_{EAR}\ (400)}$$

(R_{EAR} = 400 Ω or 200 Ω for Z_R calculation)

FIGURE 5 – COMMON MODE REJECTION – RECEIVE AMPLIFIER TEST CIRCUIT



$$R_{CM} = 20 \log \frac{U_{EAR}\,(V_C = 20\ mV;\ V_{ZA} = 0V)}{U_{EAR}\,(V_C = 20\ mV;\ V_{ZA} = 20\ mV)}$$

FIGURE 6 – $V_{E(}$, $R_{ON(}$, $R_{OFF)}$ TEST CIRCUIT

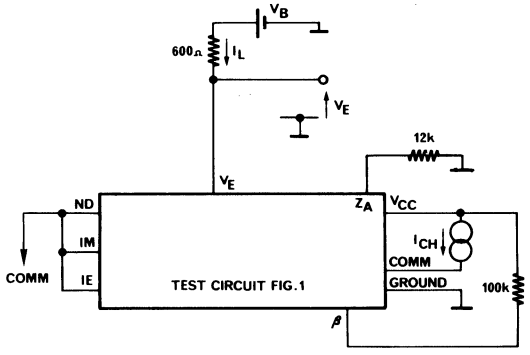


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FIGURE 7 – MF TRANSMISSION

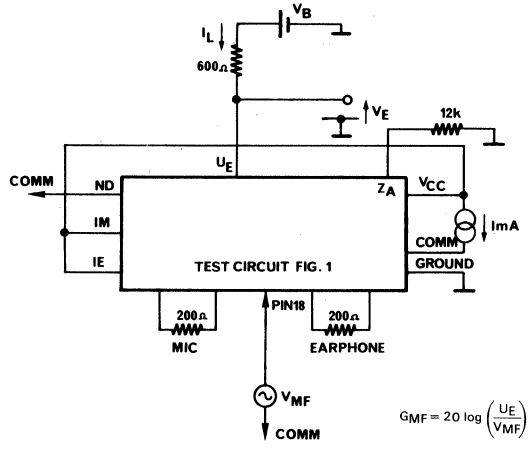


FIGURE 8 – DC SUPPLY MASK
(including dioμ Bridge)

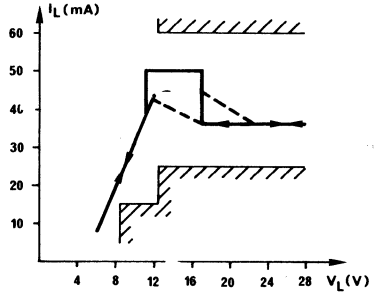


FIGURE 9 – TYPICAL REGULATION CHARACTERISTICS OF SUPPLY VOLTAGES

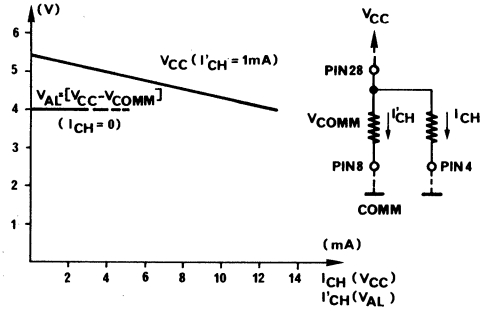


FIGURE 10 – TYPICAL VARIATION OF TRANSMIT AND RECEIVE GAINS WITH LINE VOLTAGE

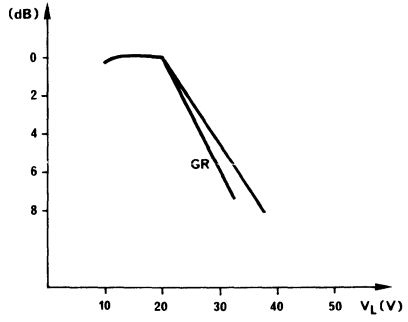
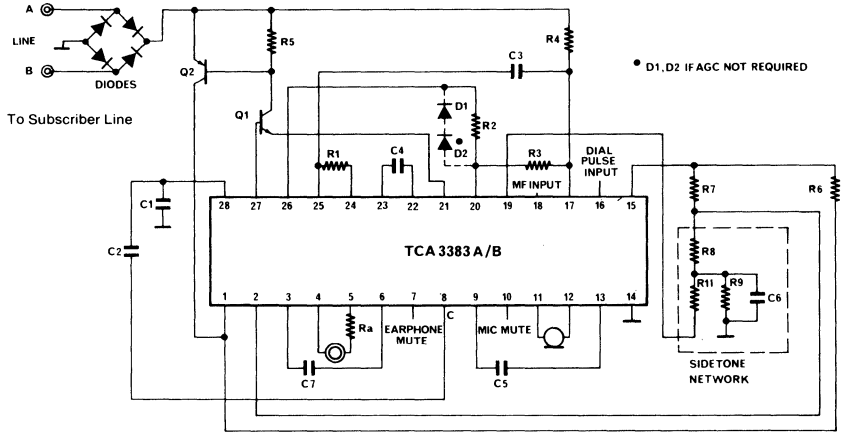


FIGURE 11 – TCA 3383A/B BASIC APPLICATION CIRCUIT
ND, IM, IE tied to COM if not used.

Typical Application



COMPONENT LIST – APPLICATION FIGURE 11

1. Transistors

Type	Nr	V_{CEOmin}	βomin (I_C = 10 mA)	I_{Cmax}(mA)	I_{Cpeak}(mA)	Location
PNP	MJE350	150V	30	60	150	Q2
NPN	BF393	150V	30	5	15	Q1

2. Diode bridge: MDA 204

V_{min} = 200 V

3. Resistors

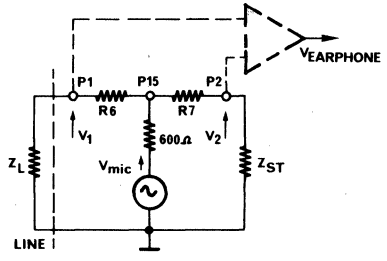
R_1 = 86.6 KΩ ±1%
R_2 = 130 KΩ ±1%
R_3 = 560 KΩ ±1%
R_4 = 1 MΩ ±1%
R_5 = 100 KΩ ±10%
R_6 = 10 Ω ±1%
R_7 = 200 Ω ±1%
$R_8 + R_9$ = 12 K for 600Ω line (modulus)

4. Capacitors

C_1 = 220 µF V= 6V
C_2 = 10 µF V= 5V
C_3 = 100 µF V= 20V
C_4 = 270 µF V= 6V
C_5 = 2.2 µF V= 5V
*C_6 = 3.3 nF V= 10V
C_7 = 1.0 µF V= 5V

*indicative value

FIGURE 12 – CALCULATION OF SIDETONE NETWORK



In balance, $U_{earphone}$ resulting from U_{mic} = 0

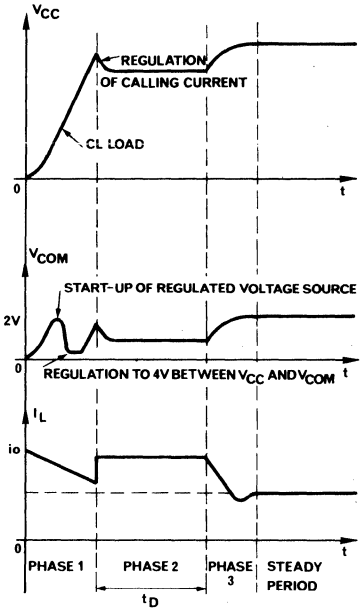
ie $U_1 = U_2$

hence $\frac{Z_L}{Z_L + R_6} = \frac{Z_{ST}}{Z_{ST} + R_7}$

thus $Z_{ST} = Z_L \frac{R_7}{R_6}$

(For Z_L = 600 Ω, R_6 = 10 Ω, R_7 = 200 Ω ∴Z_{ST} = 12K)

FIGURE 13 – START-UP PERIOD (See block diagram)



TCA 3385

Product Preview

TELEPHONE RING SIGNAL CONVERTER

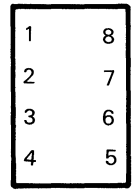
The TCA3385 is a high density bipolar telephone ring converter. This circuit is designed for use with the TCA3386 (speech circuit and monitoring speaker amplifier). These devices, together with a microprocessor form the basis of a fully electronic telephone set. In On-Hook position, this circuit detects the presence of a ring signal on the line, sends this information to the MPU and powers all the system (MPU and TCA3386). Energy is derived from ring line signal. A switching regulator, with high efficiency, converts the available high voltage, low current into a low voltage, high current.

Threshold level detection and input impedance may be set by an external resistor.

The output for microprocessor can optionally contain ring signal frequency information which can be used by the microprocessor to distinguish between different tones (useful for German specifications). This circuit includes protection against over-voltages.

- Power derived from Ring Signal
- Regulated supply voltage: 5.25V
- Ring detection output for microprocessor
- High efficiency switching regulator
- Line impedance matching, programmable
- Threshold ring detector, programmable
- Lightning and mains protection.

PIN ASSIGNMENT



This document contains information on a new product.
Specifications and information herein are subject to change without notice.

TCA3386

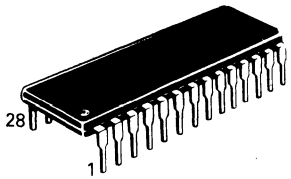
Product Preview

FEATURE TELEPHONE SET I.C.

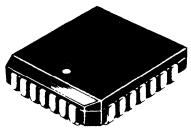
TCA3386 is designed to be used in mid- and high-end telephone sets, associated with a microcomputer. It contains the circuitry for the d.c. mask, transmit and receive amplifiers, 2-4 wire conversion, impedance matching, sidetone balance, for a high performance speech circuit. It also contains a monitor amplifier to drive a loudspeaker, with anti-acoustic feedback. Tone generators for dtmf dial and ring signal generation are also on chip.

The d.c. mask, volume control, muting, dial pulse timing, dtmf frequencies and levels, ring tones, and monitor functions are all programmable/controllable through the 2-wire MCU port. Power supply and reset for the MCU are provided, and the TCA3386 can be used in ring mode with the addition of the Ring Power circuit TCA3385. TCA3386 is implemented in an advanced high density bipolar process.

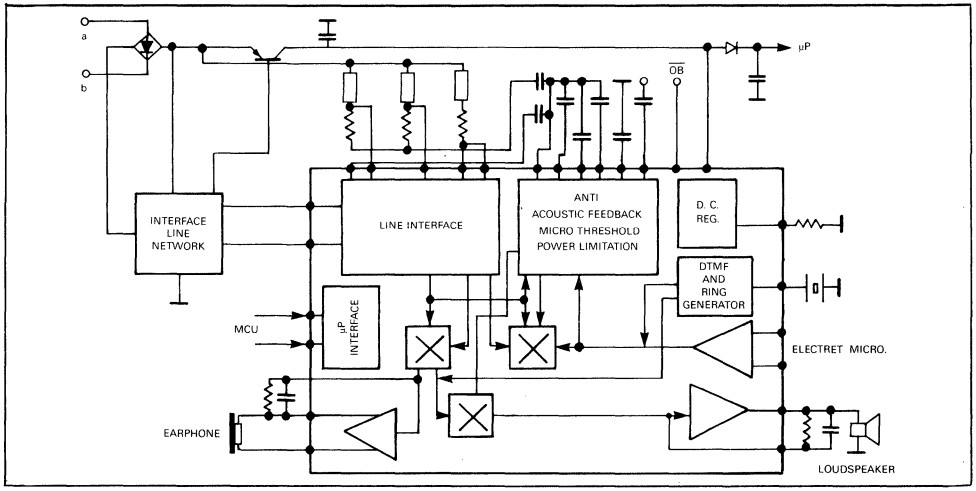
- MCU controlled feature telephone set with integrated loudspeaker monitor.
- Software programmable d.c. mask (France, UK, German, PABX)
- 2-4-wire conversion with programmable impedance and sidetone balance, and automatic adjustment with line length
- DTMF and ring tone generator, with timing and level controlled by MCU
- 2-wire serial MCU port, and regulated d.c. supply with reset for MCU
- Loudspeaker monitor with anti-howl circuit and automatic power adjustment to available line current, and facility to inter face external Speakerphone (MC34118)
- Uses low cost 500 kHz ceramic resonator



P SUFFIX
PLASTIC PACKAGE
CASE 710



FN SUFFIX
PLCC-28
CASE 776



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TCA 3388

Product Preview

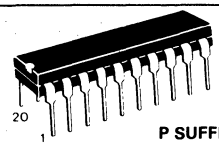
SPEECH CIRCUIT

The TCA3388 is a high density bipolar telephone speech network to replace the hybrid circuit in a telephone set.

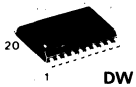
This circuit includes sidetone balance, microphone and push pull earphone amplifier with loop length compensation, programmable impedance (real or complex), programmable DC mask (French, UK Low voltage and PABX configuration for each), direct interface for a DTMF/pulse dialer (adjustble DTMF input, pulse input, hook status output and mute input), regulated power supply and protection against excess signal voltage.

Design precautions have been taken to increase RFI immunity. This circuit associated with a DTMF/pulse dialer (MC145516) and a tone ringer (MC34017) forms the basis of a low cost telephone set.

- Low voltage, low current operation: high peak-to-peak signal on the line
- DC mask programmable by external pins
- 2 to 4 wire conversion
- Programmable impedance (real or complex)
- Programmable sidetone balance with automatic line length tracking
- Automatic line length receiving and sending gain control
- Microphone amplifier with externally adjustable gain (piezo or electret transducers)
- Earphone push pull amplifier with externally adjustable gain (piezo or electrodynamic transducers)
- Mute facility for transmit and receive amplifier
- Regulated supply voltage (3.6V) with high output current capability
- Protection against excess signal voltage
- Interface for DTMF/pulse dialer
- Positive and negative logic input for pulse and mute
- Hook status output

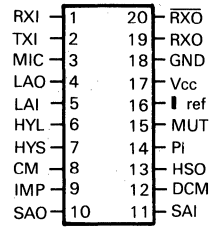


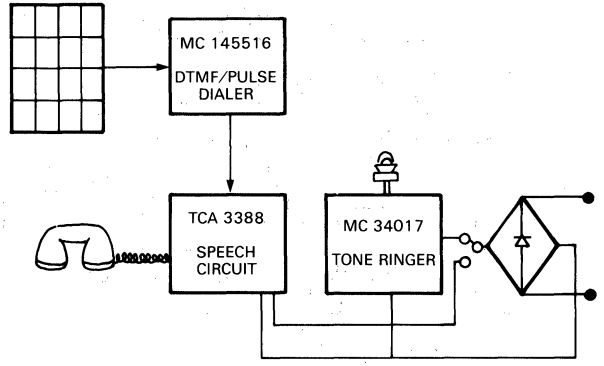
P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN ASSIGNMENT

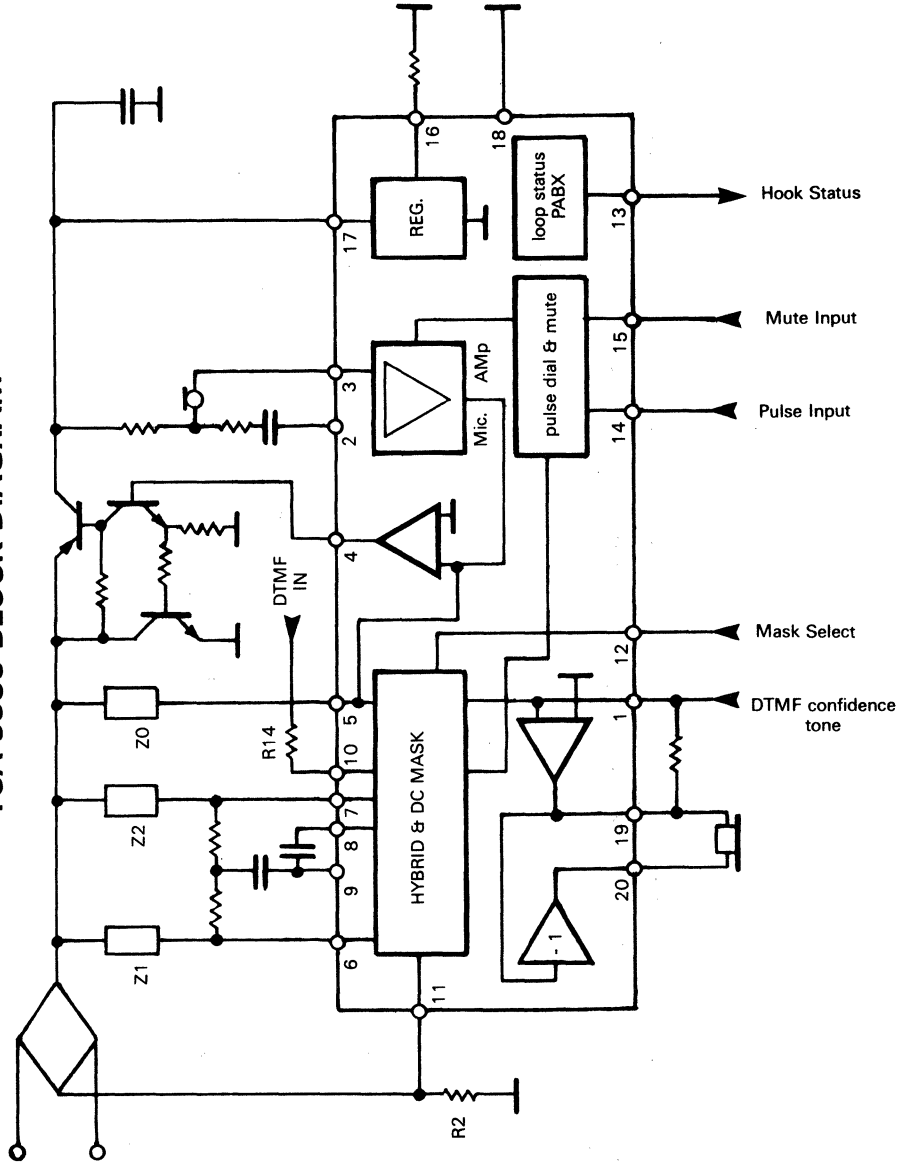




LOW END TELEPHONE SET

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

TCA 3388 BLOCK DIAGRAM



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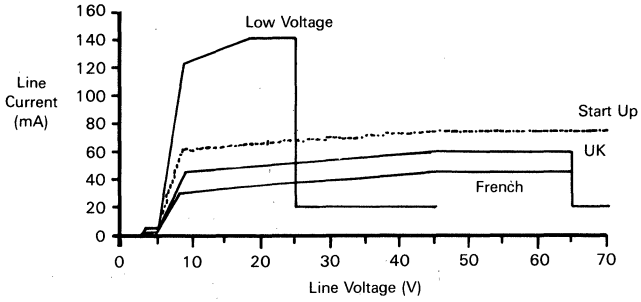
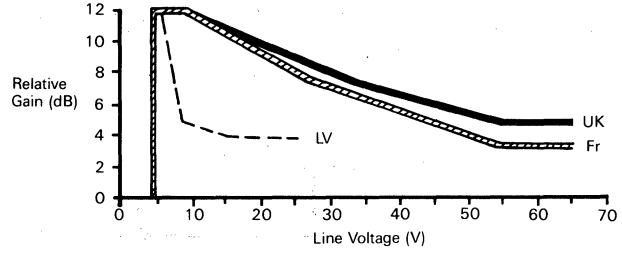
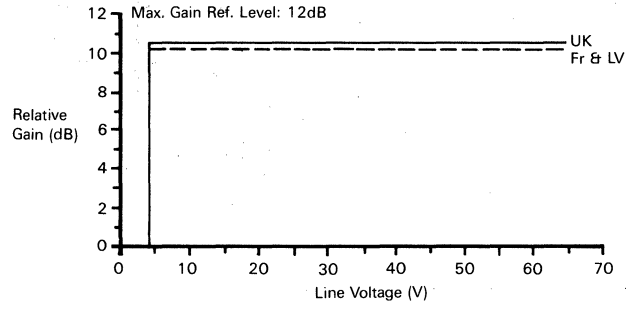


TCA 3388: DC MASKS



TCA 3388: GAIN REGULATION



TCA 3388: GAIN REGULATION, PABX MODE

PIN DESCRIPTION

1:RXI - Input for Earphone Amplifier and Confidence Tone

This pin receives the line signal via the hybrid balance and gain regulation circuits. A confidence tone (current) may also be applied to this point.

2:TXI - Microphone Current Amplifier Input

3:MIC - Microphone Negative Supply

Bias current from the electret microphone is returned to ground through this pin.

4:LAO - Line Interface Drive Amplifier Output

This pin controls the base of the high voltage line interface transistor.

5:LAI - Line Interface Drive Amplifier Input

This pin receives the AC line voltage from the input impedance network and the current for DTMF signalling. The circuit input impedance is determined by line voltage and current feedback to this pin (which is at virtual earth). The line current signal developed at pin 11 and transferred to pin 10 is received via R14 and the line voltage signal via the network Z0.

This pin may also receive a current for DTMF signalling.

6:HYL - Input for Long Line Hybrid Network

7:HYS - Input for Short Line Hybrid Network

The line signal is received between pins 6 and 10 and between pins 7 and 10. Pin 6 is connected to a network providing hybrid balance for long lines and pin 7 to a network providing hybrid balance for short lines. The received signals are weighted, according to the line length detected, summed and fed via the gain regulation and mute circuit to the earphone amplifier input (pin 1).

Both the hybrid balance impedance and the gain are therefore adapted to the line length. If this pin 7 is left open, the circuit will operate with a fixed hybrid balance impedance defined by the network on pin 6. In PABX mode, the receive mode and hybrid balance impedance are independant of the line length.

8:CM - Mask Decoupling Capacitor

For a return loss greater than 20 dB, and an imput impedance equal to 600 ohms at 300 Hz, C = 0.68µF.

9:IMP - Impedance Network Return Point

10:SAO - Line Current Sense Amplifier Output

11:SAI - Line Current Sense Amplifier Input

Voltage at this pin is proportional to the line current (I line x R2).

12:DCM - DC Mask Selection

Four dc masks are selected according to the DC voltage at this pin. An internal current generator sources (loop closed) or sinks (during line break) a constant current. The DC mask can be chosen by connecting appropriate external components (resistor, capacitor, or resistor plus capacitor) between this pin and ground.

13:HSO - Hook Status Output/PABX Mode

This pin is a digital output and reflects the status of the loop. HSO is high when the loop is closed, and low when loop is open. This pin also sets PABX mode if the load current is greater than 20µA. In PABX mode the transmission and reception gains are fixed. The hybrid balance impedance is fixed whether a single or double network is used.

14:PI - Pulse Dialing Input

This pin is a bidirectional input current for pulse dialing.

15:MUT - Mute Input

This pin is bidirectional input current for combined microphone and earphone mute.

16:I Ref - Reference Current

A programmable resistance connected to this pin sets a reference current for the circuit.

17:V_{CC} - Regulated Supply Voltage

18:GND - Ground

This pin is ground for the entire circuit.

19:RXO - Receive Amplifier Output

This pin is the output of the first receive amplifier. Receive gain is set by connecting a resistor between RXO and RX1.

20:$\overline{RXO}$ - Complementary Receive Amplifier Output

This pin is the output of the second receive amplifier.

Protection Mode

Protection is incorporated. Detection of excess continuous or signal voltage causes a transfer to a low dissipation mode after a delay.

TCA4901

Product Preview

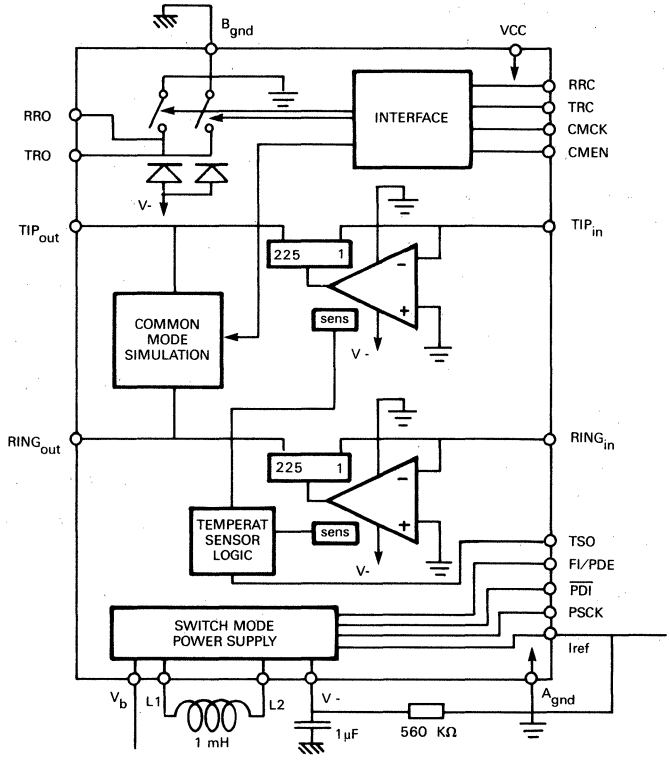
2

HV SUBSCRIBER LINE INTERFACE (HV MALC)

The TCA4901 is the high voltage line interface circuit part of the Motorola Advanced Line Card system (MALC). Together with the TCA4905 PCM Subscriber Line Interface Circuit, it performs the BORSCHT functions for an analog subscriber line for Central Office or PBX exchanges. The TCA4901 contains current amplifiers which act as slaves to the low voltage device. It is equipped with Buck-Boost switch-mode power supply unit for optimum power dissipation, and has an on-chip temperature sensor in case of excessive power dissipation. TCA4901 is fabricated in a Dielecrically isolated process, with a voltage handling capability of over 150V.

- Switch Mode Power Supply for optimum power saving
- Step Down to Feed Short Loop
- Step Up to Supply Up to -80V to Long Loop
- Power Down and Power Denial
- On Chip Temperature Sensor
- Test and Unbalanced Ring Relay Driver
- Common Mode Simulation to Calibrate Longitudinal Rejection
- Standard Battery of -48 Volts (-20 to -80 Volts)

BLOCK DIAGRAM



This document contains information on a new product.
Specifications and information herein are subject to change without notice.

TCA4905

Product Preview

PCM SUBSCRIBER LINE CIRCUIT
(LV MALC)

The TCA4905 is the low voltage digital signal processing VLSI circuit part of the Motorola Advanced Line Card system (MALC). Together with the TCA4901 High Voltage Line Interface Circuit, it performs the BORSCHT functions for an analog subscriber line for PCM Central Office or PBX exchanges. The TCA4905 contains: D/A and A/D converters; digital filters to define balance and input impedance and receive and transmit gains; d.c. characteristic; and ring-trip detection. High transhybrid rejection is achieved by an adaptive 24 filter set which continually assures that the echo return loss is optimal.

TCA4905 is fabricated in a 2μ BiMOS process, combining high density CMOS with high performance Bipolar circuitry.

FEATURES OF THE MOTOROLA ADVANCED LINE CARD

- 2-chip subscriber line interface providing most of the BORSCHT functions of Battery feed, Ring feed, Supervision, Cofidec, Hybrid 2 to 4 and 4 to 2 wire conversion.
- Adaptive, Programmable Hybrid balance digital filters
- Programmable 2-wire impedance matching digital filter
- Programmable Transmit and Receive gains
- Programmable d.c. line feed characteristics (feed voltage, feed resistance, constant current, battery reversal)
- Switched mode power supply
- 120V line drive circuit
- Self calibrating for balance about earth
- Balanced ringing through SLIC
- Ring trip detection (balanced/unbalanced)
- Loop status detection
- Tax tone injection (Subscriber Private Meter)
- Oversampled sigma-delta A/D, D/A conversion
- A- or μ-law data conversion
- Universal PCM interface
- Performance exceeds CCITT G.713 and Q.517
- Power Saving Power Down/Service denial modes

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

2

MALC DESCRIPTION

The Motorola Advanced Line Card I.C.s interface the subscriber line to the PCM digital bus. They offer the designer of an analogue subscriber line card an economical response to the problem of matching the large range of impedances to be found in the local network.

The 2-to 4-wire converter balance impedance is programmable and adaptive to line conditions. Gains and terminating impedances are programmable. These features are provided by DSP techniques with control by an MPU port on the TCA4905 LV chip.

A/D and D/A conversion is performed by 2nd order Σ-Δ converters operating at 4096k sample/s, having a dynamic range greater than 90 dB, in order to achieve the required performance margins.

The 2-wire terminating impedance is synthesised by means of a digital filter. The 4-wire balance impedance uses a repertoire of 24 predetermined programmable filters. At any one time two of the filters are implemented, one actively supplying the inter-path coupling, the other supplying coupling only for comparison. The implemented filters are updated every 32 ms, based on estimates of the received and echoed speech signals from the two implemented filters.

DC Loop

The three sections of the battery feed characteristics are software programmable through the interface bus: constant current, resistive voltage and constant voltage.

Constant current feed is provided in 4 mA steps from 0 to 64 mA.

Resistive feed is 0, 400, 800 and 1600 ohms.

Constant voltage feed is provided in 4V steps from -20V to -80V, 4 mA d.c. Feed with full longitudinal rejection allows hook status detection and telephone battery charging. Battery feed reversal is possible, maintaining all performance features.

Balance about Earth

A longituduinal balance adjustment mode is available which can be used to detect or compensate for any differential components, and achieve high common mode rejection.

Taxation Pulses

Taxation pulses can be input in the range 12k Hz to 18k Hz. The pulse duration is programmable at 50, 100, 150, and 200 ms. The d.c. voltage is adjusted automatically to avoid saturation, and an AGC system adjusts the output to the required level.

Ring Trip

Ring trip detection is performed by the digital filters, giving 100 ms ring trip time.

Standby Modes

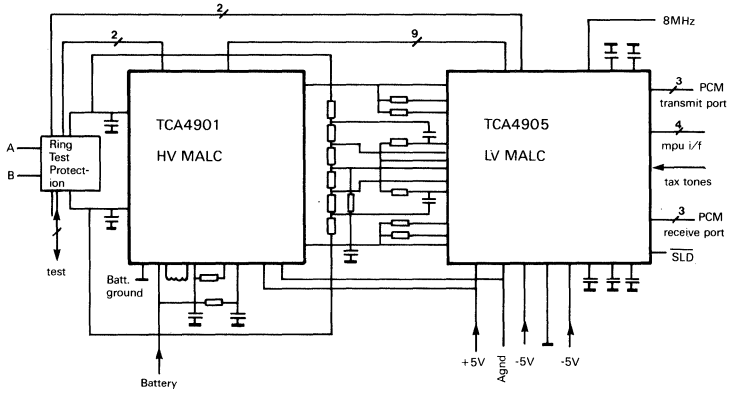
The loop can be placed in a service denial condition where there is no output, or longitudinal rejection. It can also be placed in a zero d.c. loop current condition with longitudinal rejection maintained, allowing hook status detection in a reduced power mode.

PCM and MPU Interface

Two modes for exchange of control and PCM data are possible, pin selectable by the SLD pin. In the first mode the control data is exchanged through a 4-wire MPU port and PCM data passes through separate transmit and receive parts. In the second mode, PCM and control data are multiplexed on the same 3-wire bus. MPU control information includes loop status, reset, digital filter coefficients and other control and status bits arranged in words of 3 bytes.

TCA4905 synchronizes to PCM bus clock frequencies of 512k Hz, 2 MHz, and 8 MHz. The internal synchronisation is adjusted to the appropriate time slot, or in SLD mode is adjusted to the frame sync.

Motorola ALC System Configuration



NPN
MJE270
PNP
MJE271

2.0 AMPERE

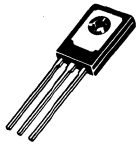
COMPLEMENTARY POWER DARLINGTON TRANSISTORS

100 VOLTS
15 WATTS

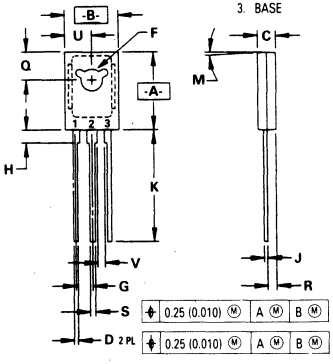
COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed specifically for use with the MC3419 Solid-State Subscriber Loop Interface Circuit (SLIC).

- High Safe Operating Area
  $I_{S/B}$ @ 40 V, 1.0 s = 0.375 A — TO-126
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- High DC Current Gain
  h_{FE} @ 120 mA, 10 V = 1500 (Min)



STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.17	0.115	0.125
G	2.39 BSC		0.094 BSC	
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-06
TO-225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	2.0 4.0	Adc
Base Current	I_B	0.1	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.3	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, non-repetitive)	$I_{S/b}$	375	—	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 20 mAdc, V_{CE} = 3.0 Vdc) (I_C = 120 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 500 1500	 — —	—
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 0.2 mAdc) (I_C = 120 mAdc, I_B = 1.2 mAdc)	$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base-Emitter On Voltage (I_C = 120 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 0.05 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	—	MHz

NOTES:
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 — DC CURRENT GAIN

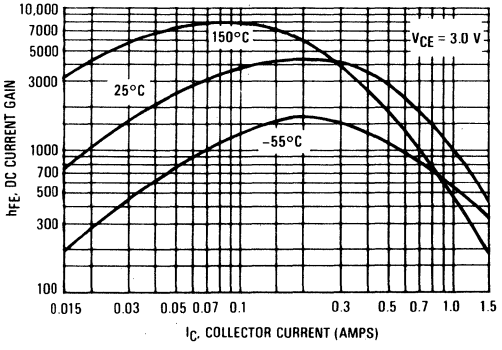
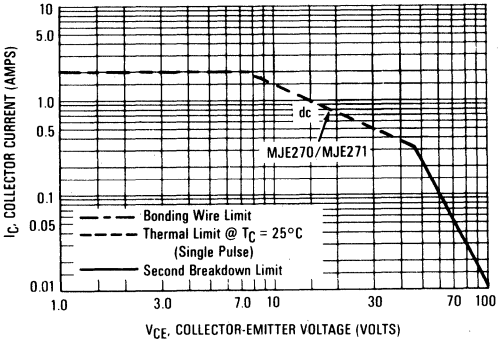
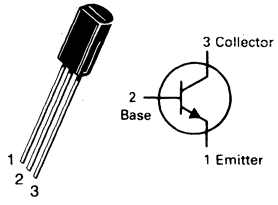


FIGURE 2 — SAFE OPERATING AREA



MPS6716
MPS6717

CASE 29-03, STYLE 1
TO-92 (TO-226AE)



ONE WATT
AMPLIFIER TRANSISTORS
NPN SILICON

Refer to MPSW05 for graphs.

2

MAXIMUM RATINGS

Rating	Symbol	MPS6516	MPS6517	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	5.0		Vdc
Collector Current — Continuous	I_C	500		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.5 20		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	 MPS6716 MPS6717	$V_{(BR)CEO}$	 60 80	 — —	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	 MPS6716 MPS6717	$V_{(BR)CBO}$	 60 80	 — —	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	 MPS6716 MPS6717	I_{CBO}	 — —	 0.1 0.1	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	 80 50	 — 250	—
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	—	30	pF
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)		h_{fe}	2.5	25	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

6-Pin DIP Optoisolators
Transistor Output

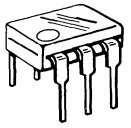
4N35
4N36
4N37

6-PIN DIP OPTOISOLATORS TRANSISTOR OUTPUT

2

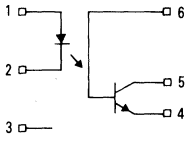
These devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Convenient Plastic Dual-In-Line Package
- High Current Transfer Ratio — 100% Minimum at Spec Conditions
- Guaranteed Switching Speeds
- High Input-Output Isolation Guaranteed — 7500 Volts Peak
- UL Recognized. File Number E54915
- VDE approved per standard 0883/6.80 (Certificate number 41853), with additional approval to DIN IEC380/VDE0806, IEC435/VDE0805, IEC65/VDE0860, VDE0110b, covering all other standards with equal or less stringent requirements, including IEC204/VDE0113, VDE0160, VDE0832, VDE0833, etc.
- Meets or Exceeds All JEDEC Registered Specifications
- Special lead form available (add suffix "T" to part number) which satisfies VDE0883/6.80 requirement for 8 mm minimum creepage distance between input and output solder pads.
- Various lead form options available. Consult "Optoisolator Lead Form Options" data sheet for details.



CASE 730A-02
PLASTIC

SCHEMATIC



1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT TRANSISTOR			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Base Voltage	V_{EBO}	7	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Source Voltage (1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac
Total Device Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Ambient Operating Temperature Range	T_A	−55 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Soldering Temperature (10 seconds, 1/16" from case)	—	260	°C

(1) Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = −55°C T_A = 100°C	V_F	0.8 0.9 0.7	1.15 1.3 1.05	1.5 1.7 1.4	V
Reverse Leakage Current (V_R = 6 V)		I_R	—	—	10	μA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector-Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C) (V_{CE} = 30 V, T_A = 100°C)		I_{CEO}	— —	1 —	50 500	nA μA
Collector-Base Dark Current (V_{CB} = 10 V)	T_A = 25°C T_A = 100°C	I_{CBO}	— —	0.2 100	20 —	nA
Collector-Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	V
Collector-Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)CBO}$	70	100	—	V
Emitter-Base Breakdown Voltage (I_E = 100 μA)		$V_{(BR)EBO}$	7	7.8	—	V
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	400	—	—
Collector-Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector-Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter-Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	T_A = 25°C T_A = −55°C T_A = 100°C	I_C	10 4 4	30 — —	— — —	mA
Collector-Emitter Saturation Voltage (I_C = 0.5 mA, I_F = 10 mA)		$V_{CE(sat)}$	—	0.14	0.3	V
Turn-On Time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100 Ω, Figure 11)	t_{on}	—	7.5	10	μs
Turn-Off Time		t_{off}	—	5.7	10	
Rise Time		t_r	—	3.2	—	
Fall Time		t_f	—	4.7	—	
Isolation Voltage (f = 60 Hz, t = 1 sec)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Current (V_{I-O} = 3550 Vpk) (V_{I-O} = 2500 Vpk) (V_{I-O} = 1500 Vpk)	4N35 4N36 4N37	I_{ISO}	— — —	— — 8	100 100 100	μA
Isolation Resistance (V = 500 V)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)		C_{ISO}	—	0.2	2	pF

TYPICAL CHARACTERISTICS

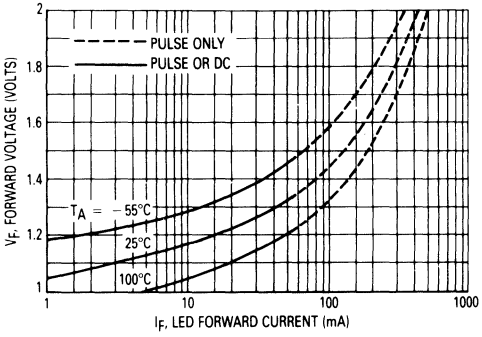


Figure 1. LED Forward Voltage versus Forward Current

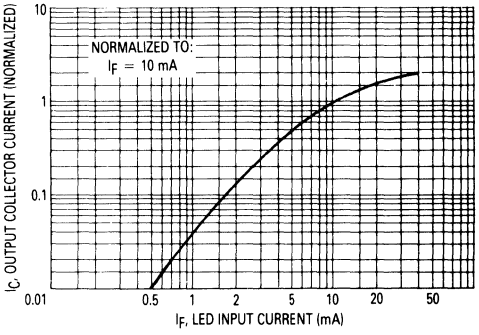


Figure 2. Output Current versus Input Current

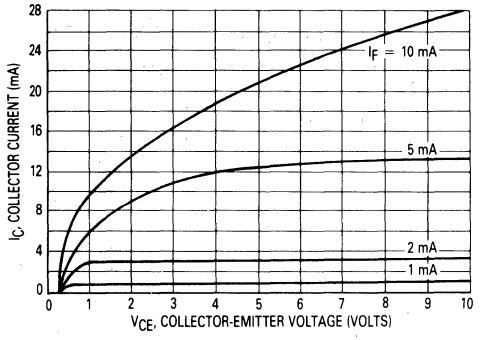


Figure 3. Collector Current versus Collector-Emitter Voltage

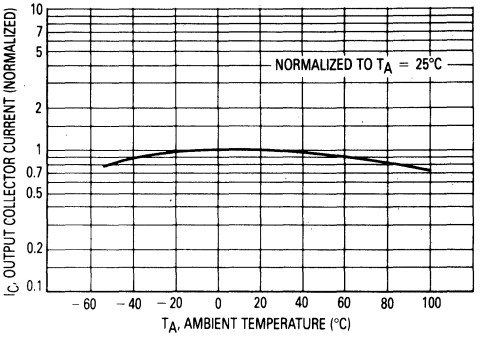


Figure 4. Output Current versus Ambient Temperature

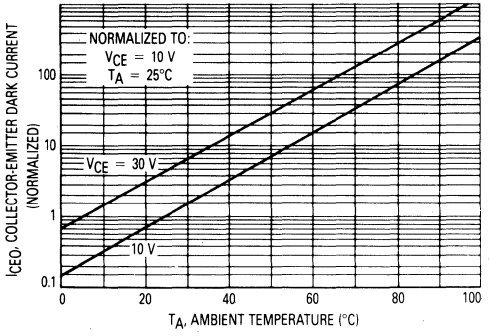


Figure 5. Dark Current versus Ambient Temperature

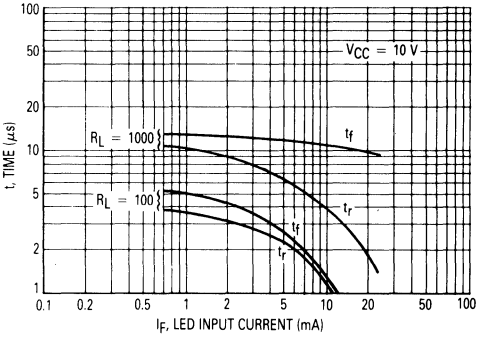


Figure 6. Rise and Fall Times

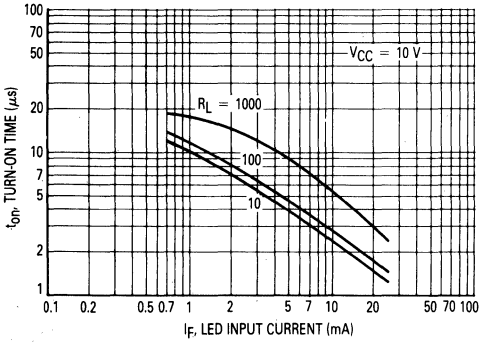


Figure 7. Turn-On Switching Times

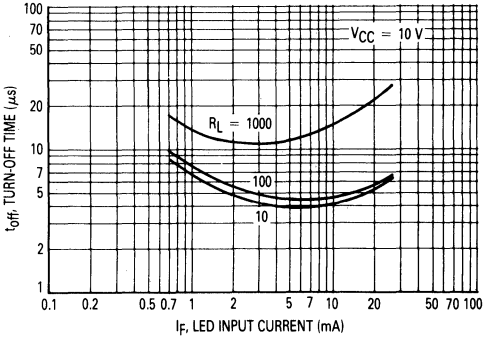


Figure 8. Turn-Off Switching Times

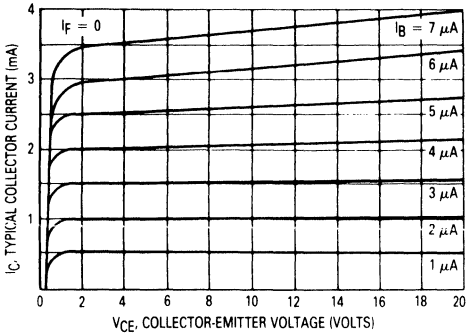


Figure 9. DC Current Gain (Detector Only)

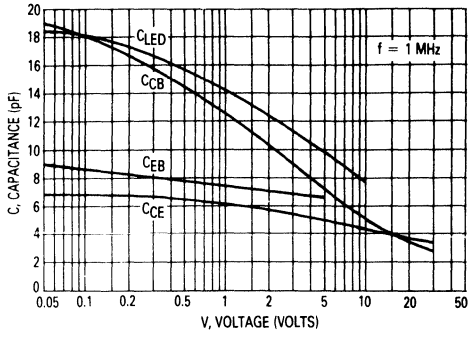


Figure 10. Capacitances versus Voltage

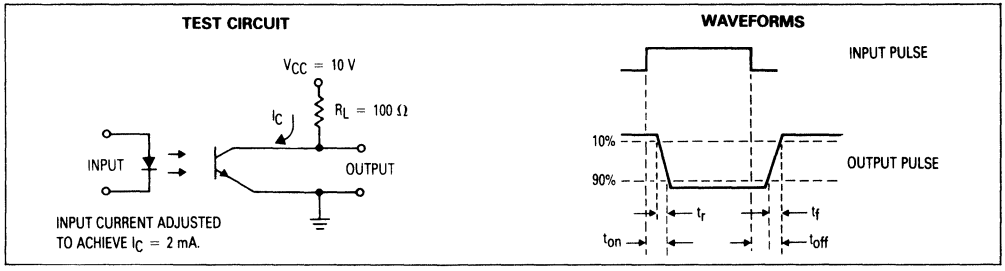
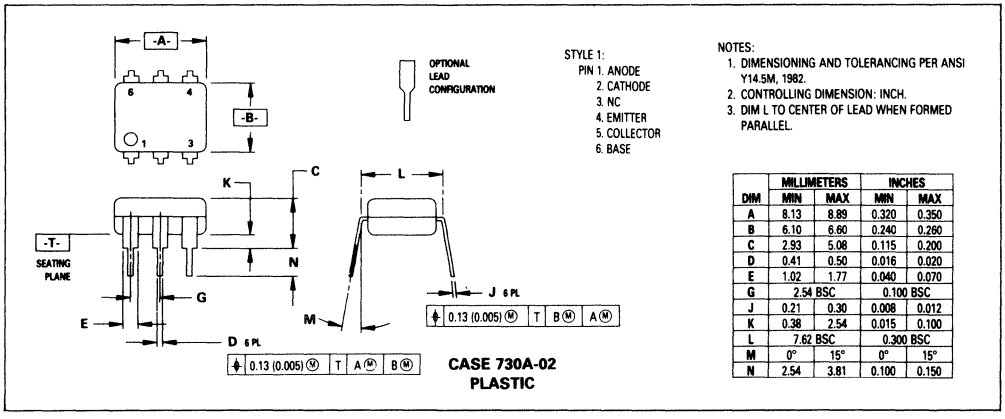


Figure 11. Switching Times

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.13	8.89	0.320	0.350
B	6.10	6.60	0.240	0.260
C	2.93	5.08	0.115	0.200
D	0.41	0.50	0.016	0.020
E	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	0.38	2.54	0.015	0.100
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	2.54	3.81	0.100	0.150

Application Notes and Technical Articles

3

3

AN-872
Application Note

MC14402 MONO-CIRCUIT APPLICATIONS INFORMATION

by
Richard L. Hall and Michael D. Floyd
Telecom Systems Engineering

This application note is intended to ease customer evaluation of the Motorola MC14402 PCM mono-circuit, particularly when using the Motorola Mono-circuit Evaluation Board. Schematics and artwork of this board are given as well as layout guidelines for designing the mono-circuit into a custom PC board. Analog testing considerations are mentioned to help sidestep some of the troublesome aspects of codec/filter evaluations.

EVALUATION BOARD DESCRIPTION

The Motorola Mono-circuit Evaluation Board is a small PC board that contains all necessary clock circuitry for operating the MC14402. Coaxial connectors allow access to the analog input/output ports and the only other connections required are to the three power terminals—V_{DD}, V_{SS} and V_{AG}. The schematic for this board is shown in Figure 1 while the artwork is given in Figure 2.

The clock circuitry uses a 2.048 Mhz crystal to produce the 2.048 Mhz data clock as well as the 8 kHz sync signal. The 8 kHz sync is an 8-data-clock-wide pulse that is connected to the RCE, TDE and MSI inputs of the mono-circuit. RCE and TDE are the receive and transmit enables respectively, while MSI is the 8 kHz reference input. The 8 kHz sync is generated by the MC14417 TSAC (Time Slot Assigner Circuit).

Options are available to help evaluate different channel parameters. These include:

* 600 or 900 ohm channel impedance
* RSI peak overload voltage of 3.15 or 3.78 volts
* TTL or CMOS logic levels
* Transmit and Receive gain adjustment ($\overline{RxO}$ gain only)
* A or MU-law coding
* Power-down capability

These options are selected by solderable wire straps (S1-S6) as described in the Strapping Information Chart. The straps can be replaced by DIP switches if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1	1
78J02	S2,S3	2
78J01	S4-S6	3

Figure 3 shows the physical location of the strap points as well as the component layout. The solid lines indicate the normal strap positions as shipped from the factory which select Mu-law, 900 ohm, CMOS, 3.78 volts peak operation. The straps E1-E10 allow reprogramming of the clock lines to provide different clock schemes. Refer to the schematic in Figure 1 for changing these straps.

TEST CONSIDERATIONS

Input/Output Levels

Obtaining valid test data is highly dependent upon establishing the proper input/output voltage levels. However, this can be a somewhat confusing task since the mono-circuit can use three different peak overload voltages—2.5, 3.1 and 3.8 volts. The evaluation board permits selection of either 3.1 or 3.8 volts. For 3.1 volts, the proper input/output level for a 0 dBm0 test signal is +6 dBm/600 ohms (1.5455 volts rms). For 3.8 volts, 0 dBm0 corresponds to +6 dBm/900 ohms (1.893 volts rms). Usually, measurement levels are referenced

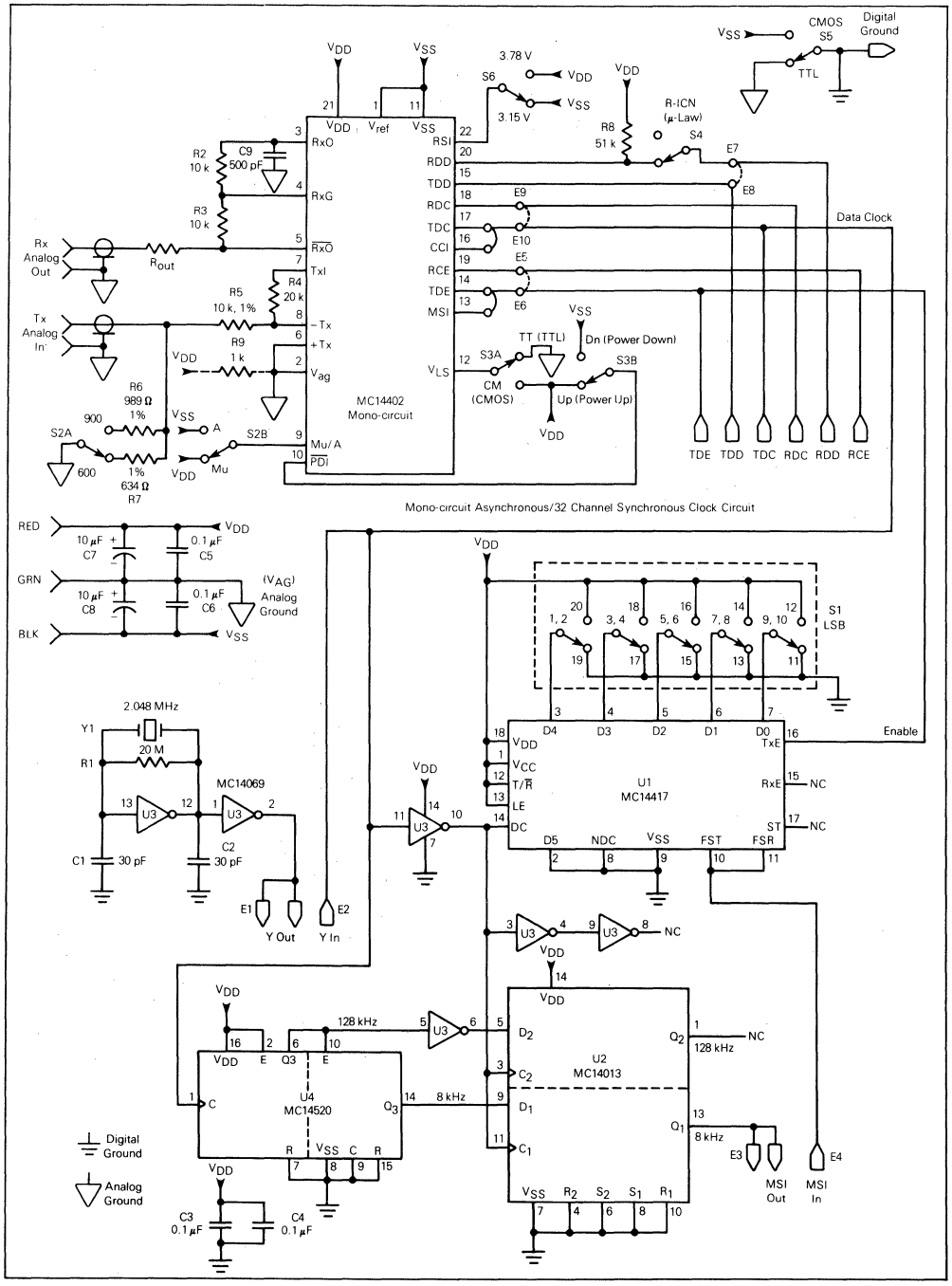


FIGURE 1 — MC14402 Switch Programmable Evaluation Board P/N 618-1030

to 0 dBm0 to avoid possible confusion over absolute levels. For example, an absolute idle noise measurement of 21 dBrnC becomes 15 dBrnC0 when referenced to 0 dBm0 (where 0 dBm0 = +6 dBm in our system).

Noise

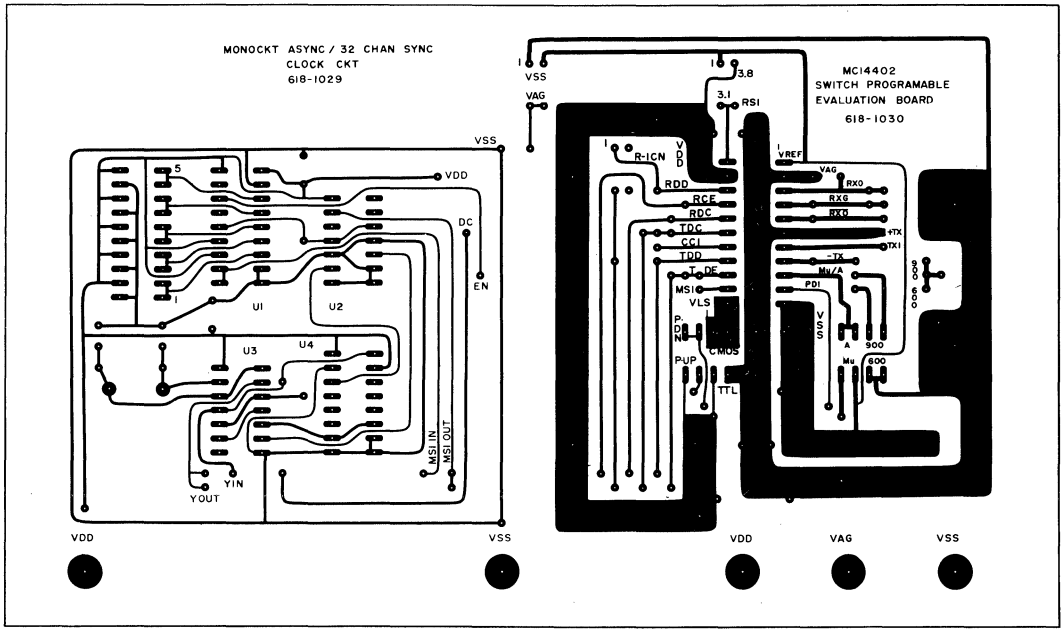
Special care has been taken in the layout of the evaluation board to minimize noise corruption. The analog and digital sections are isolated from each other and bypassing is present to reduce high frequency noise. The use of shielded cable for analog test lines is recommended to prevent extraneous environmental noise pickup as well as the use of a power supply reasonably free of high frequency noise. A 500 pF capacitor has been put on the RxO output to bypass any radiated asynchronous noise that might be picked up at this node.

Test Equipment

There are many different pieces of telecommunications test gear on the market and most will be more than adequate for testing codec/filter parameters. However, the use of wideband measurement devices for such tests as quantizing distortion and gain tracking should be avoided since these parameters involve very low voltage levels that require a selective voltmeter function for accurate results. Also, attention should be given to correct selection of input/output parameters on programmable test gear such as the Hewlett-Packard 3779 PMA and others.

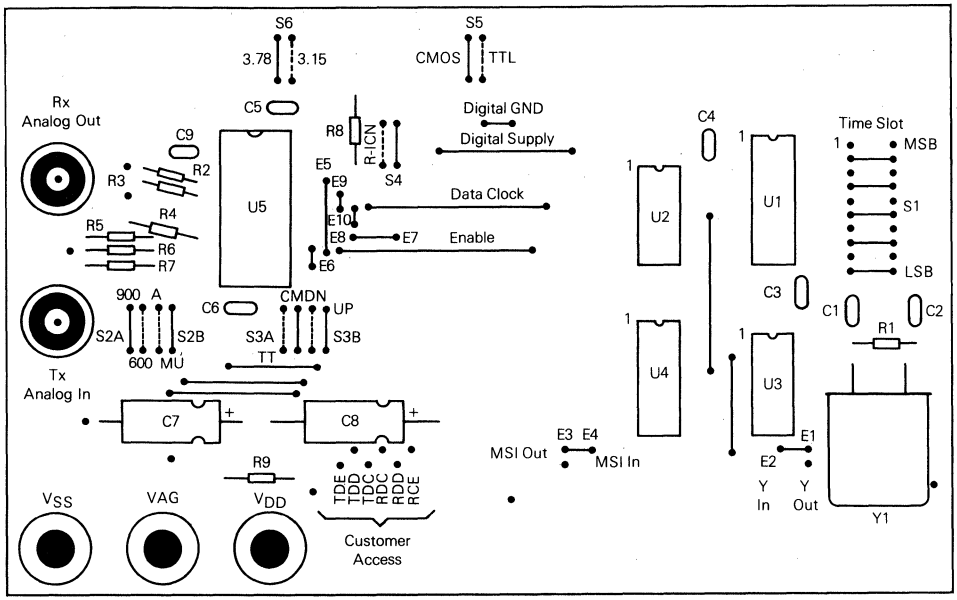
LAYOUT GUIDELINES FOR PC BOARDS

* Bypassing of both V_{DD} and V_{SS} to V_{AG} with 0.1 microfarad ceramic capacitors (or any other capacitors with good high frequency behavior) as close to the part as possible.
* Isolate analog lines from digital sections. The monocircuit pinout facilitates this by keeping digital and analog pins on opposite sides of the chip.
* Use gain-setting resistors in the range of 50 kΩ > R > 5 kΩ to avoid high impedance nodes in the analog section.
* If V_{LS} is tied to V_{AG} for TTL level selection, then this connection should be a short, direct, low inductance trace.
* In a dual supply environment, V_{DD} and V_{SS} should be connected before V_{AG} (ground).



NOTE: Drawings are not actual size.

FIGURE 2 — Evaluation Board Artwork



NOTE: Solid line indicates normal strapping as shipped from factory; dashed lines indicate optional straps as described below in the Strapping Information Chart.

Reference Voltage (S6)	Reference Impedance (S2A)	Input/Output Levels (dBm)	R2	R3	R4	R5	R_{out}*
3.15 V	600 Ω	+6/+6	–	–	10 k	10 k	Jumper
		+6/0	–	–	10 k	10 k	600 Ω
		0/0	–	–	20 k	10 k	600 Ω
	900 Ω	0/0	16.6 k	10 k	16.6 k	10 k	Jumper
3.78 V	900 Ω	+6/+6	–	–	10 k	10 k	Jumper
		+6/0	–	–	10 k	10 k	900 Ω
		0/0	–	–	20 k	10 k	900 Ω
	600 Ω	0/0	12.5 k	10 k	25 k	10 k	600 Ω

*R_{out} is located between Rx analog out and $\overline{RxO}$ output underneath the board.

NOTE: Drawings are not actual size.

FIGURE 3 — Component Layout

Strapping Information Chart

S1 These straps select via U1 (MC14417 TSAC) one of 32 possible time slots in the 8 kHz frame. When used in conjunction with another board, performance in different time slots can be evaluated. (that is TDE ≠ RCE).

S2A Selects 600 or 900 ohm input impedance.

S2B Selects A or Mu-law coding.

S3A Selects either TTL(TT) or CMOS(CM) logic levels. The TTL levels swing from V_{DD} and V_{AG}; CMOS levels swing from V_{DD} to V_{SS}.

S3B Powers device up or down. DN = Powered down and UP = Powered up.

S4 Normally loops RDD to TDD. When R-ICN is strapped, Mu-law receive idle channel noise can be measured (RDD = 1 111 1111).

S5 Controls digital ground of clock logic. When CMOS is strapped, digital ground = V_{SS}; when TTL is strapped, digital ground = V_{AG}. Note that this strap must agree with the selection on S3A.

S6 Selects either 3.78 or 3.15 volts peak overload voltage.

R2,R3 Adjusts RxO output level where gain = − R3/R2 (optional).

R4,R5 Adjusts Tx Analog In level where gain = − R4/R5.

R9 A 1 kilohm pullup resistor is needed when V_{AG} output is used by itself to provide ground return for RxO or $\overline{RxO}$. If V_{AG} is tied to system power ground, this resistor can be deleted.

R_{out} Determines output impedance.

APPENDIX

A DB By Any Other Name. . .

The following is a brief discussion of decibels and how they are used in the telephone industry in an attempt to lessen the notorious confusion this term can create.

Engineers are very familiar with the equation definition of a decibel which is:

$$\text{Decibels} = \text{dB} = 20 \log \frac{V2}{V1} \qquad (1)$$

or its corollary:

$$\text{dB} = 10 \log \frac{P2}{P1}. \qquad (2)$$

The use of the logarithmic function eases the use of the large range of voltage numbers encountered in the telephone industry. A decibel is only a relative term; it defines the difference between two absolute voltage levels.

Which now brings us to the absolute decibel—the dBm (decibel milliwatt). A dBm is equivalent to a milliwatt of power delivered into a reference impedance—usually 600 ohms. An equation commonly used to calculate dBm levels can be derived from equation (2):

$$\begin{aligned} \text{dBm} &= 10 \log (P2/P_{ref}) \\ &= 10 \log (P2/0.001\ \text{W}) \\ &= 10 \log 1000\ (P2) \\ &= 10 \log \frac{1000\ (\text{Vrms}^2)}{600\ \text{ohm}} \end{aligned}$$

where reference impedance = 600 ohms.

For example, to calculate the peak-to-peak voltage of a 0 dBm sinusoidal signal:

$$\begin{aligned} 0 &= 10 \log \frac{1000\ (\text{Vrms}^2)}{600} \\ 10^0 &= (5/3)\text{Vrms}^2 \\ \text{Vrms}^2 &= 0.6 \\ \text{Vrms} &= 0.7746 \\ \text{Vp-p} &= 2(2)^{1/2}\text{Vrms} \\ &= 2.191 \text{ volts peak-to-peak.} \end{aligned}$$

In order to understand the proper level at a certain point in a system, the term dBm0 is used for reference. A dBm0 defines the nominal signal level at a test point node. Absolute levels can then be referred to in dBm0 for comparison to the nominal level. For example, suppose that at a certain point in a system 0 dBm0 = +6 dBm/600 ohms. Then a −20 dBm signal would be equal to −20−(+6) = −26 dBm0. Therefore, a −20 dBm signal would be 26 dB down from the nominal level.

Noise measurements require a different decibel unit as they usually involve some bandwidth or filtering constraint. One such unit commonly used (especially in North America) is dBrn or decibels above reference noise. The reference noise level is defined as one picowatt into 600 ohms or −90 dBm. Telephone measurements typically refer to dBrnC which is the noise level measured through a C-message weighting filter (a filter that simulates the response of the human ear). European systems use a related term called dBmp which is the dBm level noise measured through a psophometric filter. Both dBrnC and dBmp can be referenced to 0 dBm0 by adding a zero—dBrnC0 and dBm0p. Two examples are shown below to illustrate the use of these units:

1) 0 dBm0 = +6 dBm/600 ohms
   Noise measurement = 20 dBrnC
   = 14 dBrnC0

2) 0 dBm0 = +9 dBm/600 ohms
   Noise measurement = −70 dBmp
   = −79 dBm0p.

Understanding these units should help avoid any possible correlation problems between measurements and published specifications.

UNDERSTANDING TELEPHONE KEY SYSTEMS

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INTRODUCTION

This application note is intended to give an understanding of key systems and how they differ. A theoretical architecture based loosely on many of the 16 station key systems now in existence will be presented. Possible variations and the impact on overall design will also be discussed.

WHAT IS A KEY SYSTEM?

A key system is a telephone system that can be used behind a PBX or central office. Generally, key systems are designed to support as many as 100 telephones, and provide service to these phones with up to 50 percent trunking (a trunk may be either a PBX or central office line connecting the key system to the rest of the world). The telephone set has several push buttons that are not generally found on a K500-type desk set. These push buttons allow direct access to several trunks, intercom lines and system features such as hold and do-not-disturb. The major difference between a key system and a PBX is that a key system allows the user full control over individual trunks, while a PBX assigns whatever trunk is available when requested (usually this is done by dialing a "9").

HOW DOES "SQUARENESS" AFFECT THE SIZE?

There are two basic architectural types of key systems, one known as a "square" system, and the other a "non-square" system. In a square system, every subset has control over every trunk so there can be no special reserved lines. Some designs go one step further by forcing a button appearance for each station. The most obvious size limiting factor in a square system is the number of buttons on the phone. In a non-square system, each phone is provided with a subset of the available trunks. While this makes the non-square system design appear more attractive, one must understand the complexity involved. In a square system, only one set of tip and ring wire pair must be routed to the phone, and since each phone looks identical, bookkeeping by the CPU is held to a minimum. In a non-square system there must either be a separate voice pair for each trunk and intercom link, as in 1A2 system, or there must be a way to program the telephone's "profile" into the CPU so it can control the station accesses. This presents real problems as there must be some input and display device associated with the CPU plus some form of non-volatile data storage. This storage can be anything as simple as several dip switches, or as complicated as an intelligent controller that hooks into the system with a CRT terminal and programs several EEPROMs.

WHAT IS A 1A2 SYSTEM?

The 1A2 key system is an older system that relied on electro-mechanical devices to accomplish the tasks now replaced by modern integrated circuit technology. These systems generally included several pairs of tip and ring signals which led to each station, where complicated mechanical switches selected the desired pair. The connections to the outside world were metallic, and therefore were of the non-protected variety. The biggest expense was cabling and installation labor, because the system required a 25-pair cable for each phone.

WHAT IS MEANT BY "PROTECTION"?

A protected key system is designed in such a way to prevent stressful voltages reaching the trunk under any circumstances. Generally, this is accomplished by transformer coupling the trunk to the system at the interface and adding overvoltage protection. This will prevent any accidents from causing problems with the trunk, such as 110 Vac getting to the trunk from an improperly installed telephone. When a key system is not protected, it must be installed by a registered agent of the manufacturing company. Both distributor and manufacturer are burdened by expensive agency agreements if a system is not protected.

KEY SYSTEM ARCHITECTURE

A 16-station square system with protection is outlined in Figure 1. The trunk interfaces provide the necessary protection to pass the FCC requirements, plus the circuitry to condition the voice and signaling information to make them

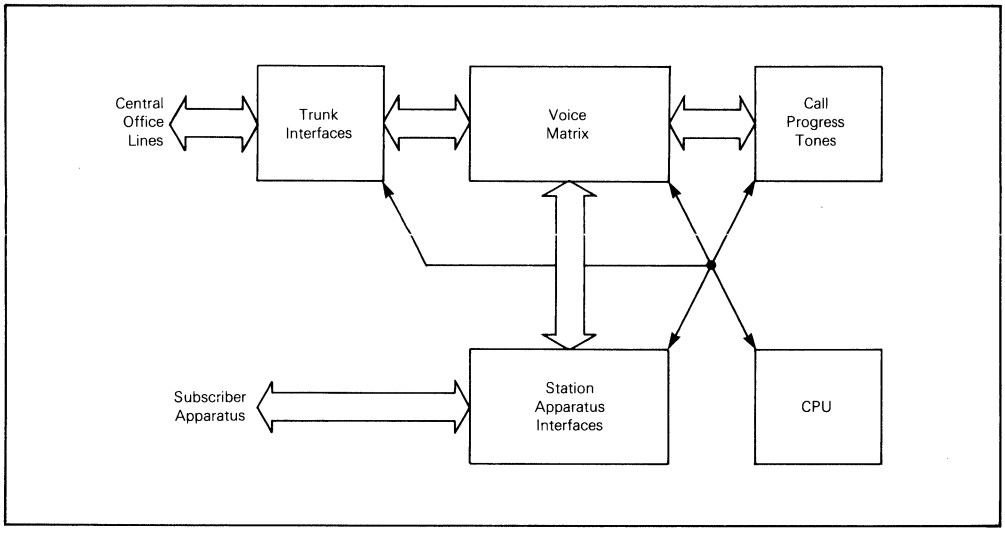


FIGURE 1 — Key System Unit

easier for the system to handle. The voice information is passed to a voice matrix, where the information can be routed to the proper destinations, and the signaling goes to the CPU to indicate what is happening at the interface. The station apparatus interfaces provide the voice and data interfaces to the phones. The progress tones are for internal supervisory signaling within the switch. The CPU is charged with the supervisory and monitoring tasks for all other parts of the system.

A much more detailed look at the voice matrix is provided in Figure 2. The voice matrix is an analog crosspoint variety which may be composed of relays or CMOS switches. Relays are a good voice switch medium for systems with eight or less stations, but the newer crosspoint ICs, such as the MC142100 and MC142101, are much more cost effective. There is some loss associated with the switches (about 100 ohms) that does not occur in the relays. In our example we will consider a $4 \times 4 \times 2$ crosspoint and the dotted lines outlining the three chips needed for the matrix. The music-on-hold (MOH) music and the tones are separated to help alleviate crosstalk within the switch structure. The design includes the ability to handle 3 trunks and 1 internal conversion. This appears to be a standard that was implemented through the years. Most systems allow expansion to either 2 more trunks or a trunk and an intercom link by adding to the matrix. Bridging more than one trunk or station can be easily accomplished by setting multiple contact points.

The loss the switch introduces into the system is the major drawback to using the CMOS crosspoint switch. The FCC requires that the electrical-to-acoustical loss of the system from the trunk to the station must not exceed 2.5 dB. A look at Figure 3A shows that a typical trunk-to-station loop has loss in two areas. The two crosspoint switches represent a typical 200 ohm resistance when they are in an on state which creates about 2.5 dB of loss in a 600 ohm system. Each transformer also introduces some loss so the electrical-to-electrical loss exceeds 2.5 dB. Changing the internal resistance of the loop minimizes the switch resistance but the transformer efficiency is greatly decreased so no advantage is found here. The loop could be amplified, but this is costly and leads to unstable circuitry so the phone must be designed to operate on different levels from a standard phone. The FCC allows another 2.5 dB of loss for a station-to-station talk path as shown in Figure 3B so the extra switches in the loop are not a problem.

Figure 4A is a block diagram of the trunk circuit. When the trunk is idle, the tip and ring are bridged by the loop relay across the ring detect circuit. This circuit signals the CPU when a call is ringing in from the central office or PBX. When the trunk is accessed by the system the loop relay connects tip and ring to the transformer. The protect circuit helps prevent surge and static damage. The battery reversal detector is an optional circuit that alerts the CPU when the tip and ring polarity has been reversed. This usually happens momentarily when a central office toll circuit has been accessed, so this is for toll restriction. The loop detect circuit is needed to indicate when the connection has been terminated by the outside caller. This prevents the hold function from locking up a trunk. If pulse dialing is to be provided a relay circuit similar to the one in Figure 4B must be added to the loop. The CPU must read the pulses from the station and transfer them to the trunk. Another possible optional circuit is a ground loop detector. This is needed to detect grounds on a groundstart trunk. These trunks use a ground to start where loopstart trunks (the most common kind) use loop continuity to start.

The station interface in Figure 5 is a four-wire design. The first pair (tip and ring) are used to provide voice communications while the second pair (D+ and D−) provide data communications. The two resistors in the voice circuit provide a current limiting function to prevent catastrophic system failures should tip and ring get shorted together. The protect circuit functions in a manner similar to the trunk protect circuit and the loop detect is used to detect the making and

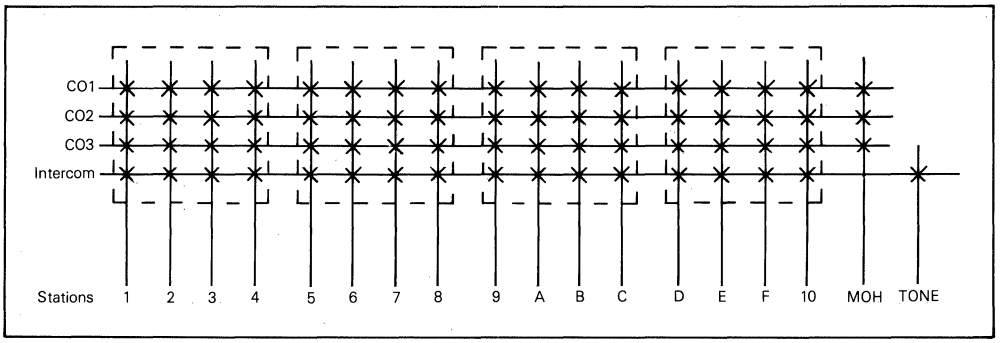


FIGURE 2 — Voice Matrix

breaking of the loop to pass pulse dialing signaling to the trunk. The resistors in the data interface do the same job in the voice circuit as does the protect circuit. The differential mode transmitter and receiver provide a serial data stream interface for the data communications. The data is generally in a half-duplex ping-pong arrangement, where the outgoing data tells the station which lamps should be on, whether the ringer is to ring, and whether the call announcer should be energized. The incoming data gives the status of the phone's hookswitch and the buttons on the keypad.

Another name for the station apparatus is the keyphone or the subset. Figure 6 is a block diagram of the subset. Tip and ring come into the subset through the hookswitch. When the handset is on-hook, the tip and ring are directed to the handsfree/call announcer circuit. This circuit is similar to a speakerphone circuit. When the handset is removed from its cradle, the tip and ring is routed to the speech network for normal telephone operation. Each voice network is powered by the battery voltage on tip and ring. The data circuit is powered by its own battery feed to help prevent crosstalk between voice and data. The data is brought into the control logic to activate the lamps, ringer, and in some cases, the handsfree/call announcer.

There are several variations on the voice and data links to the subset. Some systems impress the data, which generally has a rate well above the voice channel, onto the tip and ring for a single pair run. Extra filtering is needed to separate voice and data. Another variation connects tip and ring to the speech network causing the handsfree/call announcer to receive voice over the same wire pair as the data. This allows "off-hook call announcing" where the user can be paged via the call announcer while off-hook talking. Generally the output level of the call announcer is greatly attenuated when the handset is not in the cradle.

Another interesting variation to the architecture deals with how the dialing is controlled by the system. In this arrangement all DTMF tones or dial pulses originate at the subset and are passed through the system as though it is transparent. This is known as end-to-end signaling. An alternative is to place the pulse or tone dialer on the trunk interface and read the dial by the control logic so the dialing information is passed through the CPU to be interpreted at the trunk. The major drawback here is that there must be extra circuitry in the subset to produce aural feedback. In a normal phone the DTMF encoder mutes the speech network. Since the encoder is not here the mute is lost. The levels needed at the trunk may be uncomfortable, so they must not reach the user, therefore some feedback must be generated to indicate dialing has taken place.

Adaptation of this system into a non-square system requires several major system modifications. Since a non-square system allows only a portion of the trunks and available features to be represented as buttons on the subset, some scheme of accessing other non-appearing trunks and features must be employed. This is usually done by dial access. In a dial access system, every subset must have a dial intercom button. When this button is accessed the system must provide a dial tone and a dialing register. The dialing register must be capable of counting dial pulses and decoding DTMF data. Since DTMF decoders alone are in the $20-$30 price range the number of registers are generally restricted. This can cause bottlenecking problems when there is a need for more dial accesses than the number of registers available. There is generally a tone associated with this overload (the overload is called blocking) that indicates to the user that all circuits are busy. If all intercom links are busy when access is needed, then blocking also occurs. Now that the buttons must have some flexible assignments a data base of the subset "profiles" must be retained by the CPU. In addition to this data base duty, new software overheads are necessary for the CPU to allow dial and button accesses, as well as the addition of new, extended features such as dial intercom that are generally included in the non-square system.

There are several alternatives in operation during a power failure. One solution is called powerfail cutthrough. In this scheme certain trunks are metalically connected to certain phones. Our subset design does not support this arrangement since ringing would be impossible and the call announcer would be bridged across tip and ring when the subset is on-hook. The system can be designed so that ringing occurs in a normal manner, but a ringing generator is necessary. The ringing generator is a specialized ac power source. An alternative is battery back-up, and since most systems have a master power supply of 24-48 Vdc, this can be easily accomplished. The major advantage to this that no calls are lost on the power loss as in cut-through, and unless a sophisticated cut-through system is employed, calls are lost on the return to power which again is not a problem in a battery backed-up system. The system must be a low-power design or the battery back-up system may become prohibitively expensive.

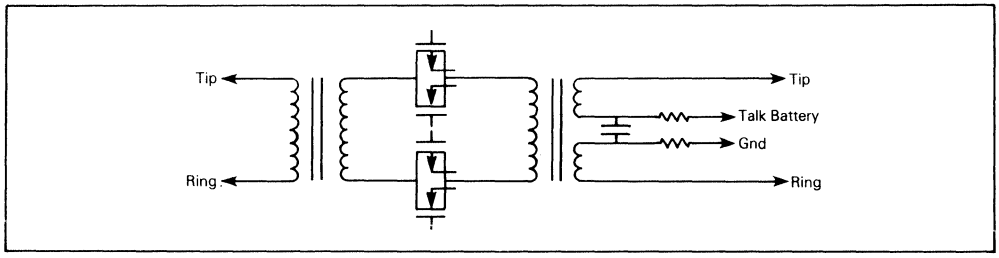


FIGURE 3A — Trunk-to-Station Loop

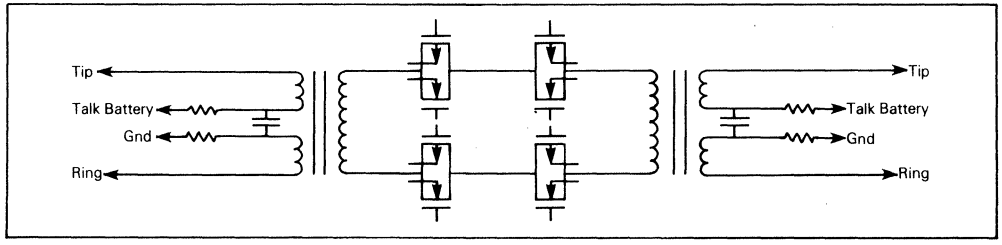


FIGURE 3B — Station-to-Station Loop

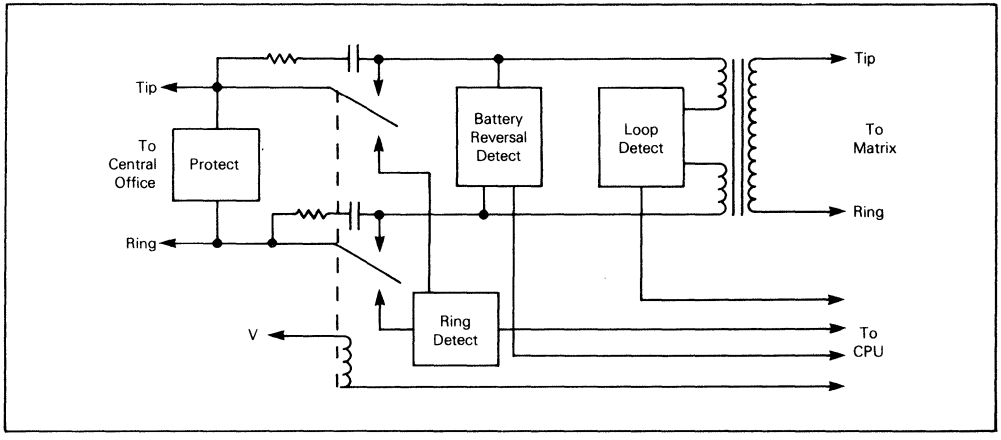


FIGURE 4A — Trunk Interface (Without Pulse Dialing)

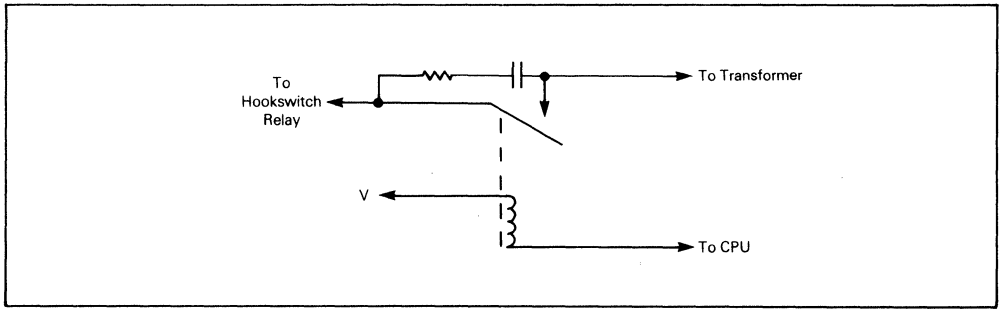


FIGURE 4B — Pulse Dialer

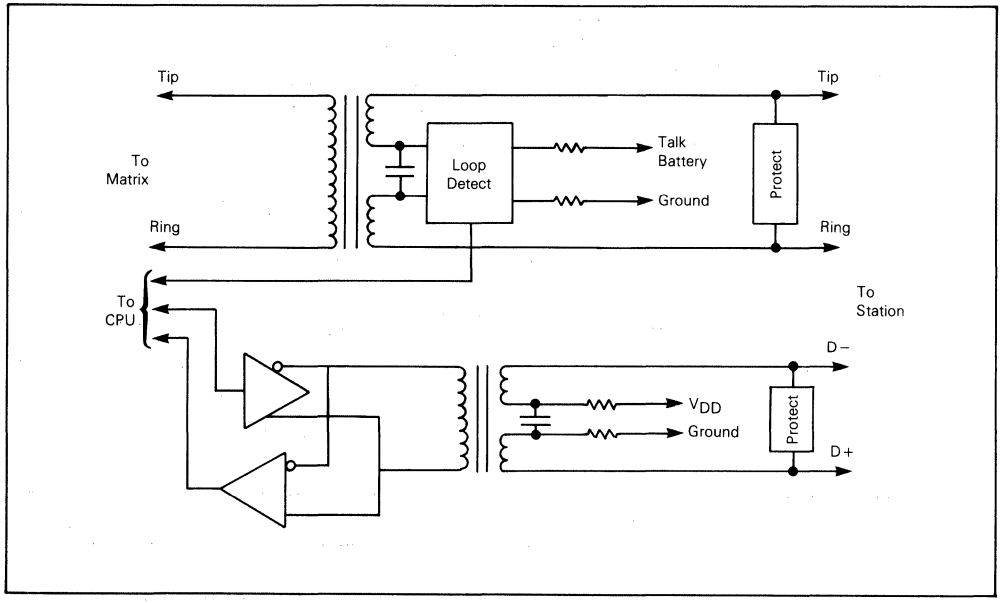


FIGURE 5 — Station Interface (Without Ring Generator)

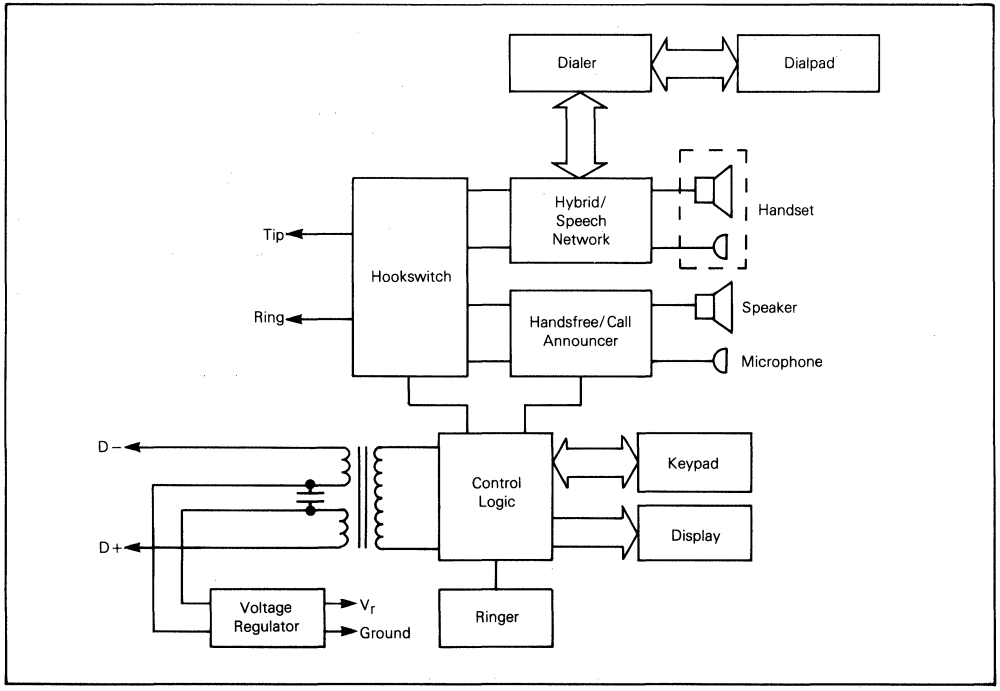


FIGURE 6 — Subset

GLOSSARY OF KEY SYSTEM FEATURES

All Call — This is where all of the call announcers are energized in the system for a general announcement. This is similar to a page except the call announcers are used instead of auxiliary amps and speakers.

Background Music — This is a feature that requires an external music source. The music is routed to all of the call announcers so that, if desired, the call announcer can provide music when the subset is idle.

Busy Lamp Field — This is an array of lamps or LEDs that indicate when each station in the system is busy or idle. This is usually abbreviated as BLF.

Call Announce — This function is performed instead of ringing. When an individual phone is call announced, the call announce circuitry is energized. A warning tone is then sent to both parties and then the parties are connected as in a conversation. The called party can talk over the call announcer as if it were a speakerphone.

Call Forward-Busy — An incoming call is routed to a secondary subset when first subset is busy.

Call Forward-Follow Me — An incoming call to one subset is routed directly to another subset.

Call Forward-No Answer — If a call is not answered in a specified period of time, the call is rerouted to a second subset.

Call Park — This feature is only used in non-square systems. When a call comes in it can be "parked," then any subset can pick the call up by accessing the parked call. This allows the subsets to pick up calls on non-appearing trunks.

Call Progress Monitor — This is a device that allows the monitoring of the calling function prior to completing the connection. All dial tones, dialing tones and ring back tones are heard over an auxiliary speaker as it would sound over a handset. This is a simplex device so no conversation can be held.

Camp On-Auto Call Back — When a called station is busy, the caller can camp on to that station so that when the subset becomes idle, it will ring. If the caller hangs up prior to the subset becoming idle, the caller's subset will ring and after he answers, the other subset will ring. The second case is known as auto call back and is an extension of the first case being camp on.

Conference — A conference is a call that has more than two parties involved in the call at one time.

Dial Intercom — A dial intercom is an intercom that when accessed allows the user to access other subsets, trunks and features with dial codes. This is only found in systems where there is not an access button for each subset.

Do Not Disturb — When this feature is activated at a subset, no incoming calls will ring the subset, however, the phone can still be used for outgoing calls. The subset will not acknowledge the call announcer either.

Direct Station Select — This allows one subset to establish an intercom call with a second subset by using a dedicated button as opposed to a dial code. This is a very popular feature in small square systems and is generally referred to as DSS.

Exclusion-Privacy — When active, this feature prevents other subsets from barging in on your call.

Executive Override-Barge In — Barge in is a feature that allows one to enter an already active conversation so that a conference is created. Executive override is the same feature applied to special phones to overcome an exclusive call (see Exclusion).

Handsfree — In an apparatus sense, this is known as speakerphone operation. In essence, a conversation is held over the subset's speaker and microphone while the handset is in the cradle. This frees the hands for other uses and several people can participate in the conversation at the handsfree end.

Music-On-Hold — This is a feature that requires an outside music source that may or may not be the same source used in background music. When someone is parked or put on hold they are provided with music instead of silence.

Page — This feature is similar to All Call except the general announcements are made over a user-supplied public address system instead of call announcers. This is especially useful in warehouse situations.

Recall — The recall feature is designed to prevent excessively long holds and call parks. When a call has exceeded the recall timeout while on hold or parked, it will ring the subset that either put it there or an attendant station.

Remote Answer — This feature exists only on non-square systems. When an incoming call rings a subset, it can be answered at another subset that does not have that particular line by invoking the remote answer feature.

Repertory Dial — This feature can be associated with either the subset or the system. This is where several commonly called phone numbers are internally stored and can be automatically dialed when accessed. This is also known as speed or abbreviated dialing.

Secretarial Intercom — This is a special case DSS where the called subset rings only while the access button is depressed. This allows private ring codes to be used between subsets to alert the users to special conditions.

Station Hunting — Station hunting is an advanced feature found usually on large, complex system. This feature allows groups of subsets to be "hunted". When a call is placed to this group, the first phone rings for a preset period of time, and if there is no answer, the second phone in the group rings. This will progress through all the subsets and the call can be answered at any subset at any time.

Tie Trunks — A tie trunk is used to link systems together. Generally the two systems are remotely located and can even be in different cities. The tie trunk does not rely on central office intervention.

Toll Restriction — This feature prevents unauthorized subsets from making toll calls.

Transfer — This feature is needed only in non-square systems and it allows a call to be moved to a subset that does not have a button appearance for that call.

ARTICLE 1

TELEPHONE QUALITY CVSD CODECS USING NEW BIPOLAR LINEAR/I2L I.C.

Stephen H. Kelley
and
John J. Price

INTRODUCTION

Principles of continuously variable slope delta modulation for communications systems are discussed including an S plane model for a simple delta modulator with adjustable gain. A new bipolar I^2L circuit for implementing CVSD systems is presented. System performance and design techniques for a basic voice band codec and a telephone quality codec are included. Double integration and active companding ratio control techniques for improving codec performance is discussed. The emphasis is on a practical, mass producible telephone codec.

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conversion schemes in systems requiring digital communication of analog signals. Voice and audio communications are analog, but digital transmission of any signal over great distance is more attractive. S/N ratios of the recovered signal do not vary with distance when using digital transmission; and multiplexing, switching, and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not easily meet the bandwidth constraints of communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economical, efficient means of digitizing analog inputs for digital transmission.

THE DELTA MODULATOR

The innermost control loop of a CVSD converter is a simple delta modulator. That portion of the CVSD is shown in Figure 1. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and controls the direction of ramp in the integrator. The comparator is clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting location tracks the input signal, the remote receiver reconstructs the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise if the clock rate of a the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates of 8 kHz and up are possible. Thus, the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins

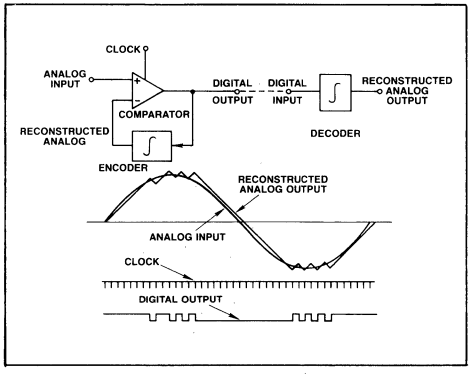


FIGURE 1 — SIMPLE DELTA MODULATION
An Analog Input Signal Can Be Digitalized and Transmitted by Synthesizing a Minimum Error Set of Voltage Ramps. The Comparator Clock Establishes the Channel Bandwidth.

without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporatic bit errors.

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be frequency limited and amplitude limited. The frequency limitations are governed by the Nyquist rate while the amplitude capabilities are set by the gain of the integrator. For a given signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

THE COMPANDING ALGORITHM

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth, the additional circuitry increases the delta modulator's dynamic range. A block diagram of a complete CVSD codec is shown in Figure 2. A new bipolar/I^2L integrated circuit has been built to provide all of the active elements. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The CVSD algorithm simply monitors the contents of shift register and indicates if it contains all ones or zeros. This condition is called a coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output drives a low pass filter. The voltage output of this syllabic filter controls the integrator gain through a V to I converter and a slope polarity switch whose other input is the sign bit or the up/down control of the delta modulator.

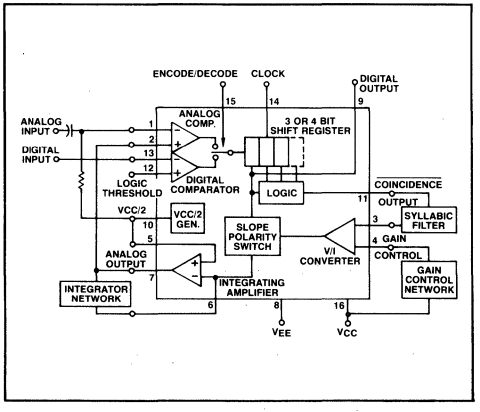


FIGURE 2 — CVSD BLOCK DIAGRAM
A Delta Modulator Is Enclosed in a Digitally Controlled Gain Loop and Composes a Continuously Variable Slope Delta Modulator. A Bipolar/I^2L Integrated Circuit Has Been Designed to Provide All the Active Circuitry Required.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other schemes provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus, a measure of the average input level is needed. By monitoring both the coincidence of ones and zeros, the shift register performs a function similar to a full wave bridge rectifier.

The algorithm is repeated in the receiver and thus the level data is recoverable at the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

SYLLABIC AND INTEGRATION FILTER PROPERTIES

The circuit in Figure 3 is the most basic CVSD circuit possible. For many intelligible voice channel applications, it is adequate. In this circuit, both the syllabic filter and the integration filter are composed of single-pole networks.

The integration network is chosen to meet two simple constraints. First, it must be an integrator throughout the voice band and second, it must be leaky so that bit errors can be tolerated and loss of receiver contact does not require an external reset for reacquisition. $C_I 5.1\ \mu F$ and $R_I = 10$ k produce a 159 Hz break/frequency and a lossy network.

The selection of the syllabic filter components illustrates an interesting property of the codec. The operation of the simple delta modulator may be investigated by deriving its S plane transfer function. The comparator is modeled with a unit limiter and a summer. The unit limiter has a describing function in S if the system is analyzed for sinusoidal inputs of the form e sin wt, that is

$$\text{Digital Output} = \frac{4A}{\pi e} \text{ e sin wt where A is the peak voltage of the unit limiter.}$$

It is obviously a non-linear element since the transfer function is dependent on the magnitude of the input signal.

The integration filter has a straightforward transfer function description:

$$\frac{\text{Analog } V_{out}}{\text{Digital } V_{out}} = \frac{Rx}{C_I(S + 1/R_I C_I)}$$

where Rx is connected from the comparator output to the integrator input and sets the gain of the simple delta modulator.

The closed loop delta modulator model is then

$$\frac{\text{Analog Vout}}{\text{e sin wt}} = \frac{1}{1 + \dfrac{4ARx}{e\ C_I\ (S + 1/R_I C_I)}}$$

Note that the response of the codec is a function of the magnitude of the input level. Closed loop CVSD systems can be analyzed for steady state inputs by substituting the syllabic filter voltage which corresponds to an applied e for A. Thus, the gain of the delta modulator is varied to accommodate the applied input level.

For a CVSD circuit to perform as an adjusted delta modulator, the model equation indicates that A ∝ e must be nearly constant. The syllabic filter time constant must be large compared to the input frequency. For a maximum input frequency of 3300 Hz, the time constant must be much larger than the 0.3 ms. Thus 3 ms is the minimum allowed RC product for the syllabic filter in voice band applications. The syllabic nature of voice is responsible for the name "syllabic filter". A CVSD codec can only effectively transmit signals whose e varies at a frequency much lower than the fundamental frequency of the signal. Conveniently, voice, modem signals and DTMF signals have this syllabic property.

In Figure 3, a 6 ms time constant is used. In Figure 5, 3 ms charge and 9 ms discharge time constants are used to improve attack time without sacrificing constant A. Voice syllables tend to have this kind of shewed envelope.

CLOCK RATE AND SHIFT REGISTER LENGTH

The prime design constraint of a CVSD channel is the channel bit rate. Since delta modulator produces a serial unframed bit stream, the bit rate and sample frequency are the same. Obviously, as the clock rate increases so will the end to end performance. Clocks from 9600 kHz to 64 kHz can be used in various applications. 16 kHz, 32 kHz, and 37.7 kHz have the greatest acceptance in practical voice communication equipment.

After fixing the system bit rate, the shift register length selection must be made. The length of the shift register determines the amount of past history which will be taken into account in predicting slope. As the clock rate changes, so does the amount of signal time recorded by the shift register. Therefore, at rates below 16 kHz a three bit algorithm produces the best results. From 16 kilobits and up, either 3 or 4 bits may be used. Four bit algorithms provide flatter S/N performance because they account for a longer average past history of steady state signals. However, the transient response to level changes is slightly degraded because of the slower companding response.

The integrated circuit is produced with either 3 or 4 bit registers and is selected by laser link cutting rather than mask option. Depending on the results of the idle channel trim corrections, the die requiring the smallest step sizes is made into a 4 bit register.

LOOP GAIN CONSIDERATIONS

The feedback gain of the CVSD codec is set by the selection of Rx in Figure 3. After the clock rate, this gain is the most critical parameter of codec performance. Since the CVSD algorithm improves the dynamic range of the delta modulator for lower level inputs, the selection of loop gain should be based on the near maximum amplitude and frequency signal which must be transmitted. Experimental data shows that a CVSD codec produces optimum S/N ratio when the companding algorithm is active between 5% and 25% of the time. Taking this into account, the gain resistor Rx can be selected by determining the required integrator current which will produce the needed step size for a specified input signal. Then the resistor should source the required current when the syllabic filter output is about 25% of its maximum value.

The current required to move the integrator output a specific voltage from zero is simply

$$I_I = \frac{Vo}{R_I} + \frac{C_I dVo}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of the sine wave centered around the zero crossing the sine wave changes by approximately its peak value. The CVSD step should track that change. The required current for a 0 dBm 1 kHz sine wave is

$$I_I = \frac{1.1 \text{ volt}}{*2(10k)} + \frac{0.1\ \mu F\ 1.1}{0.125 \text{ ms}} = 0.935 \text{ mA}$$

*The maximum voltage across R_I when maximum slew is required is $\frac{1.1\ V}{2}$

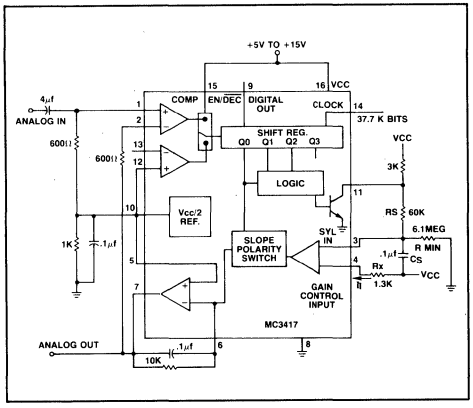


FIGURE 3 — BASIC CVSD ENCODER
Single Pole Integration and a Single Pole Syllabic Filter Are Sufficient for Many Voice Channel Applications. Selection of External Components Tailors the Integrated Circuit to the Application.

Now the voltage range of the syllabic filter is the power supply voltage, thus

$$Rx = 0.25(V_{CC})\ \frac{1}{0.935 \text{ mA}}$$

for a 5 volt supply Rx = 1.3 k

MINIMUM STEP SIZE

The final parameter to be determined for the simple encoder in Figure 3 is the minimum step size. With no input, the CVSD digital output becomes a one zero alternating pattern and the analog output becomes a small triangle wave. The peak to peak value of that triangle wave is the idle channel step size. Its meaning is analogous to the 1½ LSB quantization error of a conventional D to A converter. The codec

cannot resolve or transmit signal levels smaller than the minimum step size. In theory, one would wish to make this parameter go to zero. However, practical errors such as up and down ramp matching, comparator hysteresis, and filter op amp offsets combine to cause the idle channel analog output to drift away from the zero dc reference. The codec then produces two ones or two zeros in order to restore the level.

To set the idle channel step size, the value of R min must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter, the voltage divider of R_S and Rmin (see Figure 3) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage divided by Rx must produce the desired ramps at the analog output. Again we write the integrator current equation

$$I_I = \frac{Vo}{R_I} + C_I \frac{dVo}{dt}. \text{ For small Vo } \frac{Vo}{R_I} \rightarrow 0.$$

$I_I = C_I \frac{\Delta Vo}{\Delta T}$ where ΔT is the clock period and ΔVo is the desired peak to peak value of the idle output.

Thus if Rx and R_S are known, R min may be calculated for any system. The design of Figure 3 is complete.

Figure 4 describes the performance of the codec in Figure 3 with two sets of curves. The codec was optimized around 0 dBm but the S/Nc ratio falls only 6 dB at −30 dBm. The low pass nature of the codec and the change of frequency response with input level is documented on the left of the figure.

S/N IMPROVEMENT USING TWO POLE INTEGRATION

One pole integration filters are not the only possibility. If a two pole integration network is used instead of the simple one pole, an S/N improvement can be realized. An encoder using such a network is shown in Figure 5. Adding a second pole in the transfer function of the integrator simply reduces the total noise bandwidth of the analog output without affecting the relevant voice energies. From another point of view, a 11110111 input to a single pole integrator produces a large ramp reversal at the 0 value since the 0 step will be in the opposite direction but equal in magnitude to the 1 ramp before and after it. Since the analog signal is band limited, it was obviously continuing to decrease at the 0 step and an error in tracking is encountered. If two pole integration is used, the 101 reversal is filtered and the 0 step is much smaller than the 1 step preceding it in the long string of ones. Thus the total error is less. A two pole filter can improve noise performance by 3 or more dB across the entire input level range.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephone circuits, the second pole can be placed at 1.8 kHz to exceed the 1633 DTMF frequency. The lower the second pole frequency, the greater the noise improvement. To ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 244 Hz, 1.8 kHz and 5.3 kHz is used for telephone application in Figure 5 while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. The integration filter in Figure 5 has a transfer function of

$$\frac{V_{out}}{I_{in}} = \frac{R_0R_1\left(S+\frac{1}{R_1C_1}\right)}{R_2C_2(R_0+R_1)\left(S+\frac{1}{(R_0+R_1)C_1}\right)\left(S+\frac{1}{R_2C_2}\right)}$$

The selection of the two pole filter network affects the selection of the loop gain value and the minimum step size

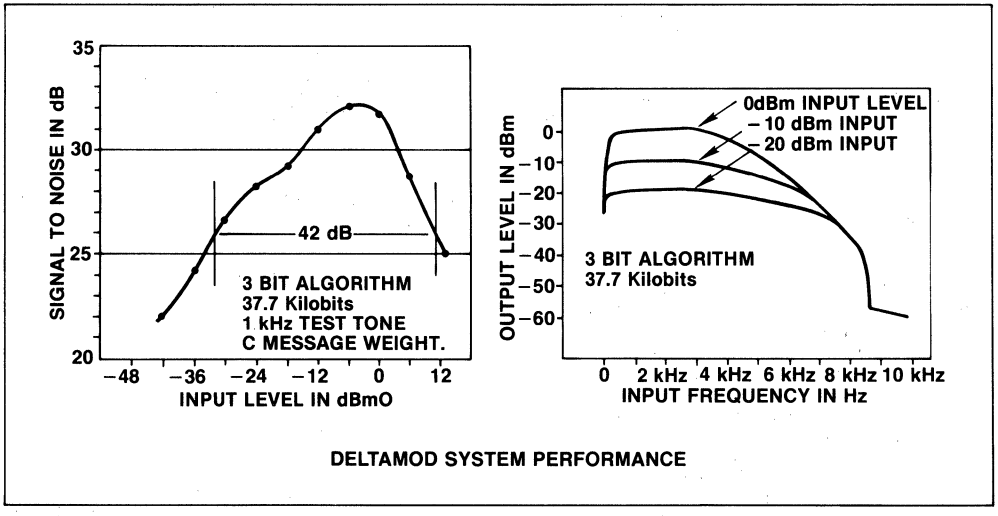


FIGURE 4 — SIGNAL TO NOISE PERFORMANCE AND FREQUENCY RESPONSE
Data Result From Testing the Circuit in Figure 3.

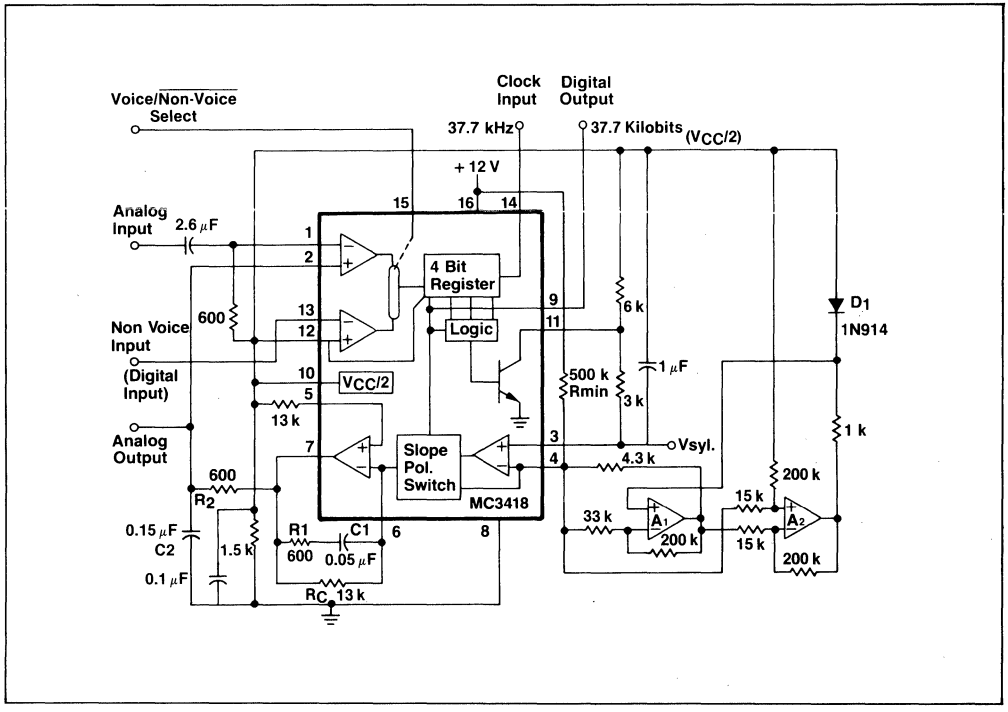


FIGURE 5 — TELEPHONE QUALITY DELTA MODULATOR CODER
Both Double Integration and Active Companding Control Are Used to Obtain Improved CVSD Performance.
Laser Trimming of the Integrated Circuit Provides Reliable Idle Channel and Step Size Range Characteristics.

resistor. The required integrator current for a given change in voltage now becomes

$$I_{in} = \frac{V_{out}}{R_0} + \frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1 \frac{\Delta V_{out}}{\Delta T} +$$

$$R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0} \frac{\Delta V_{out2}}{\Delta T2}$$

The calculation of desired gain resistor Rx then proceeds exactly as previously described using this current equation.

SUBSCRIBER CARRIER TELEPHONE QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 10 μA $\tau o \approx \mu\Delta$. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four bit algorithm currently used in subscriber loop telephone systems.

With these specifications and the circuit of Figure 5, a telephone quality codec can be mass produced.

The circuit in Figure 5 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7 kilobit rate. At 37.7 kilobits, 40 voice channels may be multiplexed on a standard 1.544 megabit TI facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

THE ACTIVE COMPANDING NETWORK

The unique feature of the codec in Figure 5 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 5, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pin 10 and 4 by means of the virtual short across pin 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2 - 0.7$).

The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

The present step size of the operating codec is directly related to the voltage across Rx which established the integrator current. In Figure 5, the voltage across Rx in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on Rx, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across Rx and the gain of A2 and A1. The gain of A2 is also experimentally determined but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across Rx goes to zero. The voltage at the output of A2 becomes zero since there is no drop across Rx. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is, therefore, independently selectable.

The signal to noise results of the active companding network are shown in Figure 6. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dbm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm. The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across Rx. The curves demonstrate that the level linearity has been maintained or improved.

The codec in Figure 5 is designed specifically for 37.7 kilobit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 5 represents a significant step forward in the art and cost of CVSD codec designs.

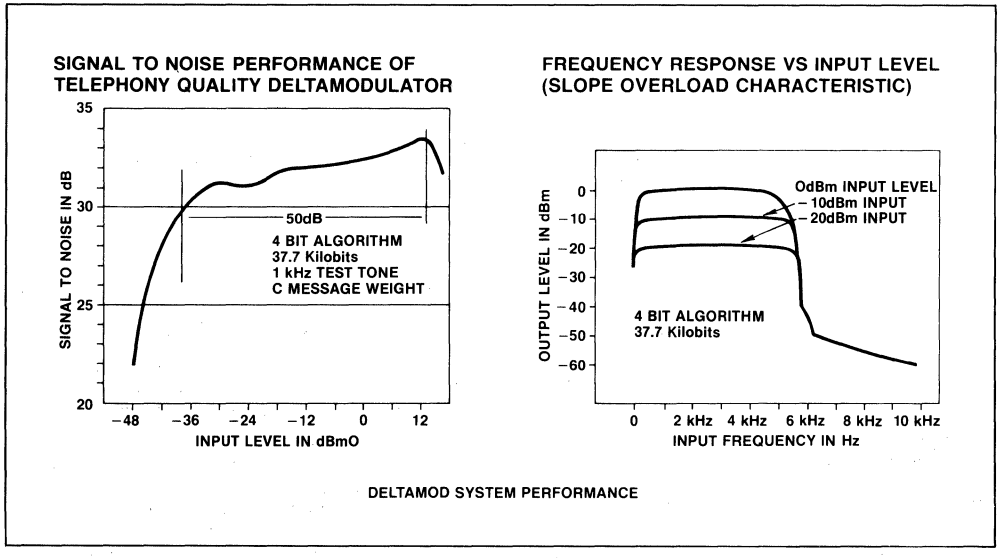


FIGURE 6 — SIGNAL TO NOISE PERFORMANCE AND FREQUENCY RESPONSE
Data Document the Improvement Realized with the Circuit in Figure 5.

Time-slot assigner chip cuts multiplexer parts count

by Henry Wurzburg
Motorola Inc., Semiconductor Group, Phoenix, Ariz.

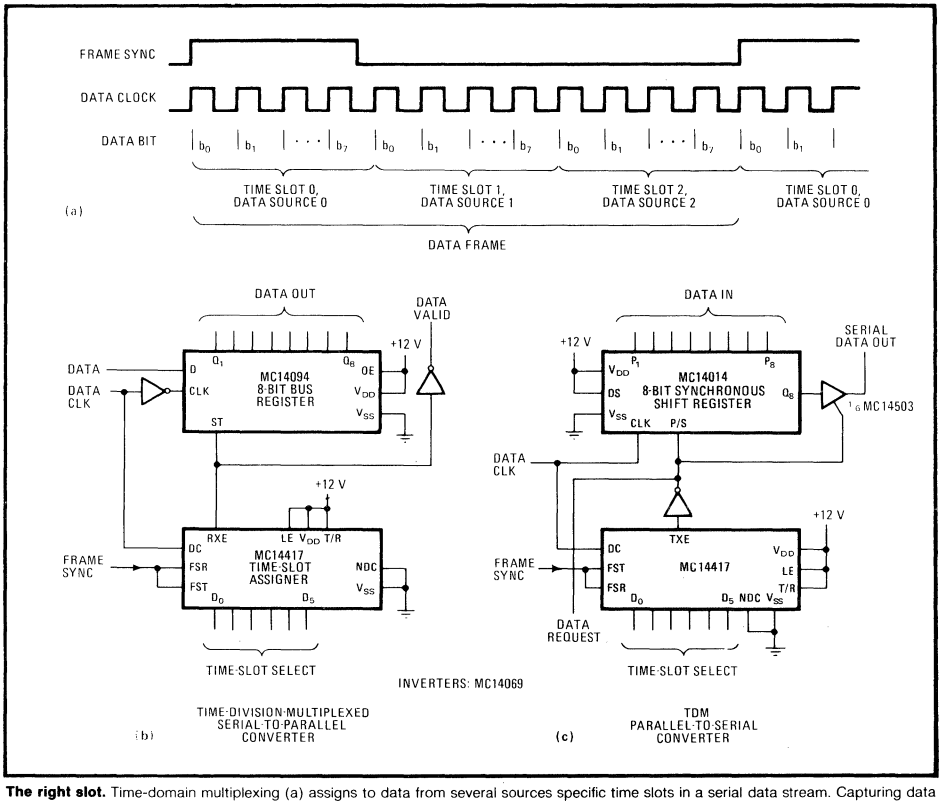
In some communications systems, particularly digital telephony equipment, it is hard to examine the data from a given source after it has been time-division-multiplexed with other data for serial transmission over a common data line. Capturing the data from its time slot and converting it into parallel form for examination usually requires many integrated circuits, since the slot must be programmable.

A special-purpose IC, the MC14417 time-slot assigner carries out this serial-to-parallel function with the aid of only a few inverters and one other IC. What's more, the cost of implementing the circuit is only a few dollars.

The timing of a simple three-slot TDM system is shown in (a). In digital telephone systems, a data frame may consist of anywhere from 24 to 40 time slots, each containing 8 bits of data transmitted at rates of up to 2.56 megabits per second.

In the all-complementary-MOS capture circuit of (b), the MC14094 shift register acts as a serial-to-parallel converter, while the 14417 computes when the data is to be captured and converted. Just which time slot it captures is determined by the binary data present at inputs D_0–D_5 of the 14417. The circuit also provides a valid-data output signal. As for speed, the circuit works for clock rates of up to 2.56 MHz with systems having up to 40 time slots.

Implementing a parallel-to-serial converter for multiplexing data onto the TDM data line is equally simple if the 14417 is used as shown in (c). Here, a three-state buffer prevents the serial data bus from being loaded during idle time-slot periods. The frequency limitations of this second circuit are the same as for the capture circuit. □



The right slot. Time-domain multiplexing (a) assigns to data from several sources specific time slots in a serial data stream. Capturing data from a specific slot is made easy with the MC14417 time-slot assigner (b), which works with the MC14094 shift register to provide data from the source dictated by the select inputs of the 14417. The versatile chip can also provide parallel-to-serial multiplexing (c).

Telecomm ICs create low-cost phone links 4 miles long

Although the maximum recommended length for communications links over uncompensated 24 AWG twisted-pair wires is 4000 ft, a few off-the-shelf integrated circuits, when configured as a line driver, will drive a communications link with a maximum length of over 4 miles. The bandwidth of over 3000 Hz is adequate for remote control, sensing, and even private-telephone voice communications.

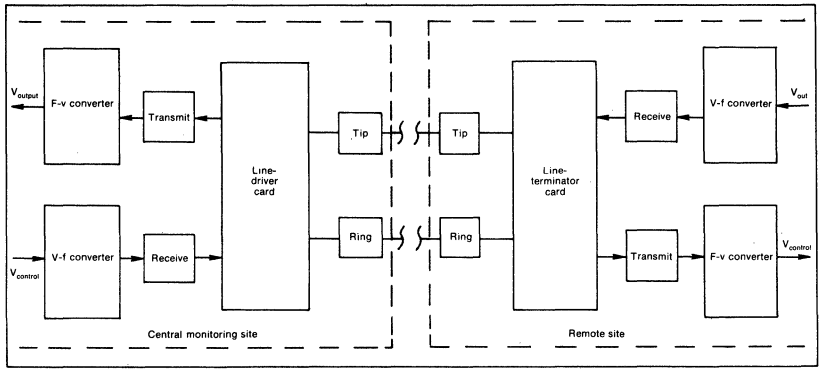
Any subscriber-loop interface circuit (SLIC) can be used to drive the line. In Fig. 1, a SLIC interfaces with voltage-to-frequency and frequency-to-voltage converters and a line terminator. Thus a dc voltage related to a process at a remote site can be measured from a central location and a corrective dc voltage can be sent in the reverse direction to adjust or control the process.

A variety of ICs can be interfaced with the basic driver for signaling or for data or voice transmission. Analog-to-digital and digital-to-analog converters—such as codecs and CVSDs (continuously variable-slope delta modulators used for voice companding)—perform the front-end data conversion for a low-cost computer link. A variety of dual-tone multifrequency (DTMF) encoders and decoders facilitate simple signaling over privately owned twisted pairs.

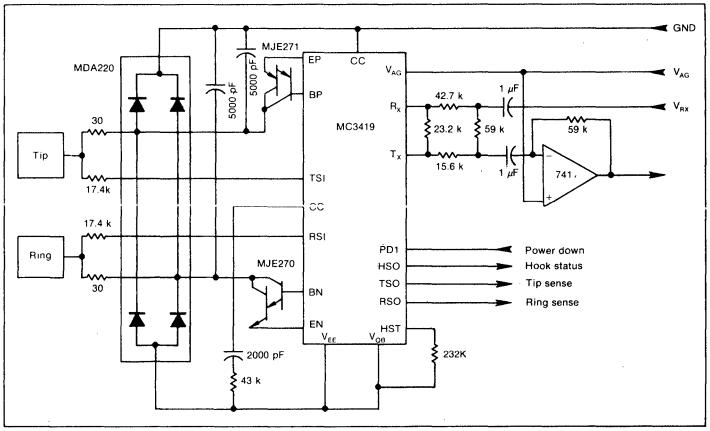
A line-driver card exemplifies the simple hardware configuration required (Fig. 2). The SLIC uses two Darlington pairs as pass transistors to handle currents of up to 120 mA. Changing the value of the 59-kΩ resistor used in the feedback path of the 741 operational amplifier will adjust the transmission output gain. The MDA220 rectifier bridge protects the circuit against lightning damage.

The line-terminator card converts a bidirectional two-wire line into two pairs of unidirectional lines, one transmit and one receive, and then amplifies the received and transmitted signals. A simple terminator can be made with the hybrid transformer and two varistors from a telephone handset. Even if a more sophisticated terminator card were built using a speech-network IC, the cost of the entire system would be less than the cost of the modems, PBX lines, or rf transceivers used for short-range, private communication links.

John Hines, Design Engineer, Motorola Inc., Bipolar Integrated Circuits Group, Linear IC Division, 5005 E. McDowell Rd., Phoenix, Ariz. 85008.



1. The maximum range of an RS-232 or RS-422 communications link can be extended to over 4 miles of uncompensated 24 AWG wires by a line-driver card based on a single-chip subscriber-loop interface circuit.



2. A line-driver card requires a SLIC, two Darlington pairs, a rectifier bridge for lightning protection, and an operational amplifier. A resistor in the op amp's feedback path adjusts the transmission output gain.

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AN943

UDLT Evaluation Board

INTRODUCTION

To help meet the demands for a cost effective solution to the ever growing voice/data world within the digital telephone and PBX realm, Motorola has created the Universal Digital Loop Transceiver (UDLT) voice/data circuit family. The purpose of this application note is to render an understanding of the UDLT voice/data family and show a typical application for these CMOS parts. This is an evaluation of the application and performance of the MC145422/26 UDLT demonstration board, which was designed and built for customer evaluation.

3

FUNCTION OF PARTS

UDLT's

The UDLT master (MC145422) and slave (MC145426) are transceivers that provide 80 kilobit-per-second full duplex synchronous voice and data communication to distances of two kilometers on 26 AWG twisted pair and further on heavier gauge pairs. The modulation technique used is a 256 kilobaud Modified Differential Phase Shift Keying (MDPSK) type burst. The MDPSK triangular waveform used in this modulation technique reduces radiation, EMI, and crosstalk due to its compact frequency spectrum.

The master which is used at the telephone switch linecard bursts ten bits to the slave, consisting of eight bits of voice/data and two signaling bits. The slave, which is used at the terminal or digital telephone, receives the burst from the master and upon demodulation of the burst synchronizes its clocks, and bursts ten bits back to the master. This "ping-pong" technique occurs within a 125 microsecond frame period and allows end to end full duplex, synchronous operation. This full duplex operation between the master, at the digital linecard and the slave/mono-circuit, at the digital telephone, enables each set to have high speed access to the PABX switching facility.

At the linecard a microprocessor has complete control of the master. The Signal Enable input (SE) is a three state controller pin which if held high enables the power down, loopback and the two signaling bits, thus allowing these signals to be bussed to the microprocessor. The master can be programmed via the Signal Insert Enable (SIE) pin to insert signaling bit two into the LSB of the PCM word at Tx. This allows simultaneous voice and data transmission through the PABX without the need of changing existing hardware and software. Both the master and the slave have power down and loopback features for system power conservation and testing. The power down pin on the slave is a bidirectional pin. It can be used as an input to initiate a call. When the PD pin is pulled high, the slave will continue to burst every other frame (once every 250 microseconds) until the master responds by bursting. Once the master responds, the slave synchronizes to ping-pong with the master at an eight kilohertz rate. The PD pin can be left floating as an output, in which case the slave will pull PD high until the slave stops receiving bursts from the master then it will take PD low and stop bursting until PD is brought high or the master bursts again. A three state control can be used on this pin if the designer wants to send data to the master during a power down. The slave also has a Tone Enable input pin (TE) which when held high generates a 500 hertz square wave tone at approximately −20 dBm0 which can be used in the digital telset to provide audio feedback.

MONO-CIRCUITS

Motorola's family of Pulse Code Modulation (PCM) mono-circuits incorporate a codec, filter and voltage reference into a single IC. The general block diagram for Motorola's mono-circuits is shown in Figure 1. These devices perform the digitizing and recovery, as well as the band-limiting and reconstruction filtering necessary for voice digitization in telephone systems. The mono-circuits are tailored for a variety of telephone switch architectures. The family consists of five different device types. The MC14400, MC14403, and MC14405 16 pin devices, the MC14401 18 pin device and the MC14402 22 pin device allow designers to optimize for minimal configurations or select a full set of features. The MC14403, for example, can be used where minimal space is desired for the digital phone design whereas the MC14402 is available for maximum flexibility. The mono-circuit incorporates the band-pass filter required for antialiasing and 60 hertz rejection, the A/D, the D/A, both for either U.S. Mu-Law or European A-Law companding formats, the lowpass filter required for reconstruction smoothing, on-board precision voltage reference and does not require any external components.

In this demonstration board, the full featured 22 pin MC14402 mono-circuit is used in the slave circuit showing its ability to adjust the receive gain while maintaining a low impedance output using the RxO, RxG, and $\overline{\text{RxO}}$ pins, The MC14403 is used on the master board showing a simple 16 pin solution for the telephone handset interface.

DATA SET INTERFACE (DSI)

The MC145428 Data Set Interface (DSI) provides the asynchronous to synchronous and synchronous to asynchronous data conversion. This low power five volt CMOS device is ideally suited to interface between the RS-232 compatible data port of any voice/data digital telset or terminal and the synchronous data channel of the UDLT. A block diagram of the Data Set Interface is shown in Figure 2.

There are two basic modes of operation for the synchronous channel interface. In the first mode the DSI inter-

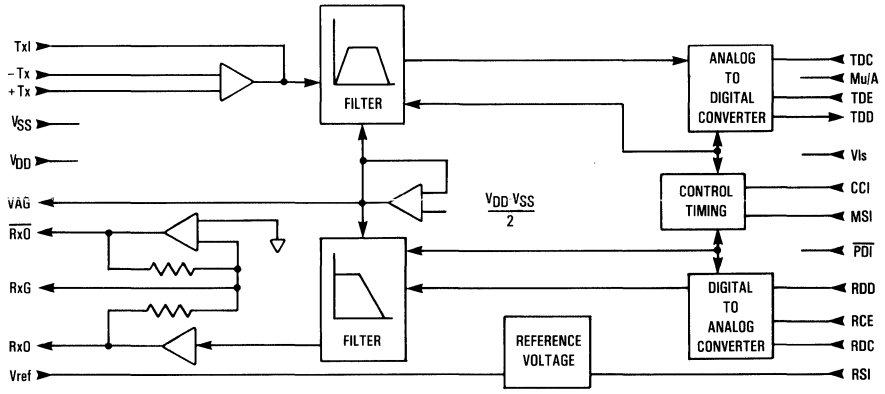


Figure 1. Block Diagram of the Mono-circuits

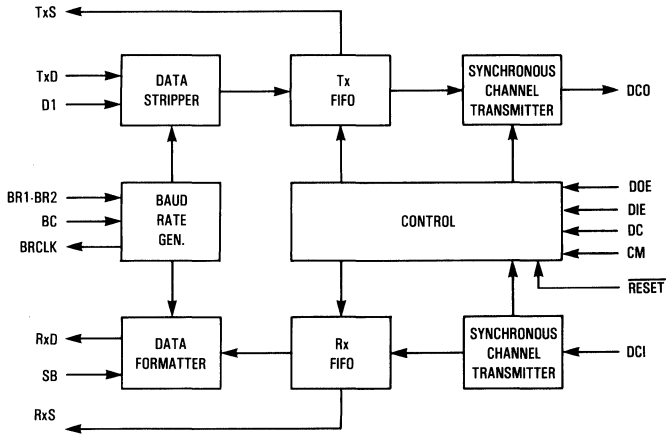


Figure 2. Block Diagram of the Data Set Interface

faces to the eight kilobits-per-second data channel of the UDLT. The Clock Mode input (CM) is tied low while the Data Output Enable (DOE) and Data Input Enable (DIE) are tied high. In this mode a new data bit is clocked out of Data Channel Output (DCO), a new data bit is clocked in at Data Channel Input (DCI), on each falling edge of the Data Clock (DC).

In the second mode of operation, the clock mode is held high. In this mode the DSI is intended to interface with the UDLT's 64 kilobits-per-second data channel. Data is clocked out under control of DOE and the rising edge of DC. Data may be clocked out at a maximum length of eight bits per enable high period. Data is clocked into DCI under control of DIE high and the falling edge of DC. The maximum word size is also eight bits per DIE high period.

Asynchronous data is input on the TxD pin from the output of the RS-232 receiver. This data must have at least one start and one stop bit and at least eight data bits, but will accept nine. The length of the data word is set by the DL pin. A high on DL selects a nine bit data word and a low selects an eight bit data word. The baud rate at which the DSI accepts data on the TxD pin, and outputs data on the RxD pin, is selected with the BR1, BR2, and BR3 pins which derive the internal sampling clock. The internal baud rate generator may be programmed to accept common asynchronous data rates from 300 to 38.4 kilobits-per-second. This internal sampling clock is 16 times the selected baud rate. If BR1-BR3 are all set to logic zero then an externally supplied 16 times clock can be used on the Baud Clock pin (BC) thus giving the user a variable data

rate from zero to 128 kilobits-per-second. For the internal baud rate generator to be accurate, a 4.096 megahertz clock must be used at the BC pin. If the internal baud rate generator dividers are used with a BC clock other than 4.096 megahertz, the data rate may be directly scaled.

Data input on the TxD pin is stripped of its start and stop bits and is loaded into the transmit FIFO register. If the transmit FIFO holds more than two data words or if RESET is held low, then the (TxS) Transmit Status output pin will go low.

Data coming in from the synchronous side is loaded into the receive FIFO, the data has its start and stop bits inserted and is output at RxD at the same baud rate as the transmit side. If the receive FIFO is overwritten, RESET is held low, or if loss of synchronization occurs by the loss of the synchronizing flag word, then the (RxS) Receive Status output pin will transition low.

3

RS-232 DRIVERS/RECEIVERS

The RS-232 Driver/Receiver chips interface the data terminal equipment with data communications equipment. Motorola manufactures both the MC1488 Quad Line Driver as well as the MC1489 Quad Line Receiver. Both 14 pin packages were used in this evaluation board. Motorola also manufactures the MC145406 Driver/Receiver chip which is a silicon-gate CMOS integrated circuit that combines three drivers and three receivers compatible with the electrical specifications of EIA standard RS-232-C, and CCITT V.28. This part has the capability of running with power supplies ranging from ±5 volts to ±12 volts while operating with a maximum quiescent current supply of 1.45 milliamperes. By combining both the drivers and receivers in a single CMOS chip, the MC145406 provides an efficient, low-power solution for RS-232-C/V.28 applications. A footprint for the MC145406 is included on the evaluation board design.

TRANSFORMER INTERFACE

The transformer interface between the UDLT and the twisted pair wire is of primary importance. The major transformer specifications can be determined from the specifications of the UDLT, driver/receiver, modulation technique, effective characteristic impedance of the wire, attenuation of the wire and dc current feed capacity. The UDLT has a differential output (LO1, LO2) that can drive 440 ohms differentially to five volts peak to peak. The receiver has an input threshold of ±25 millivolts. The UDLT modulation method has maximum power bandwidth from eight kilohertz to 512 kilohertz. To improve line settling between bursts, a bandwidth of 20 kilohertz to 512 kilohertz is used. The effective characteristic impedance of 26 AWG telephone twisted pair wire is approximately 110 ohms with an attenuation of 18 decibels-per-kilometer at a frequency of 256 kilohertz. The transformer configuration is shown in Figure 3.

The source impedance resistors for the LO1 and LO2 driver outputs were chosen to be 220 ohms on the transmit tap. This dictates a turns ratio of 2:1 to the line side of the transformer to result in an impedance match to the 110 ohms characteristic impedance of the twisted pair.

To set the 20 kilohertz low-frequency cut off of the transformer interface, the inductance of the transmit winding of the transformer should be 1.75 millihenries. To set the 512

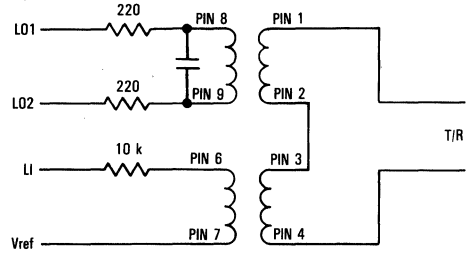


Figure 3. Transformer Configuration

kilohertz high-frequency cut off, a 0.001 microfarads capacitor is connected in parallel with the transmit tap. The turns ratio for the receive winding is determined by the maximum attenuation of the line and the threshold of the receiver detecter. With an initial amplitude of 2.5 volts peak (five volts peak to peak) at LO1 and LO2 halved by the source resistors to 1.25 volts peak at the transmit tap, which is halved again via the turns ratio to the line windings, yields 0.625 volts peak at the line side of the transformer. This 0.625 volts peak is reduced by 36 decibels or a factor of 63 to ten millivolts at the receiving transformer. The receiver of the UDLT has a positive and negative 25 millivolt threshold, which means the receive transformer tap needs a gain of approximately four to meet the needs of the receiver circuitry of the LI pin. This results in the transformer of the schematics, which may be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
P/N P-1358-A

The signals from LO1 and LO2 on the transmit tap are 1.25 volts peak which through the turns ratio to the receive tap becomes 2.5 volts peak at LI. This can exceed the maximum and minimum voltage specification for LI requiring input protection such as the clamping diodes on LI, shown in Figure 4.

When using battery feed through the transformer, further protection is required due to loop current induced spikes at both transmit and receive taps of the transformer. There are several factors to take into consideration when determining the specifications for battery feed current by the center tap of the line side of the transformer. The maximum power is transferred when half of the source voltage is dropped across the effect source resistance. Based on a loop length of two kilometers with a dc resistance of 270 ohms per loop kilometer, a current of 44 milliampheres is the maximum power transfer current. The loop current chosen for the specification is 100 milliampheres. The circuit of Figure 4 is an example of this type of protection.

EVALUATION BOARD DESCRIPTION

The Motorola UDLT evaluation board is a single sided PC board that consists of all the necessary circuitry for end to end operation and demonstration of the 80 kilobits-per-second full duplex synchronous data link of the UDLT master and slave. The evaluation board itself consists of two smaller boards; a master board and a slave board. These two boards may be

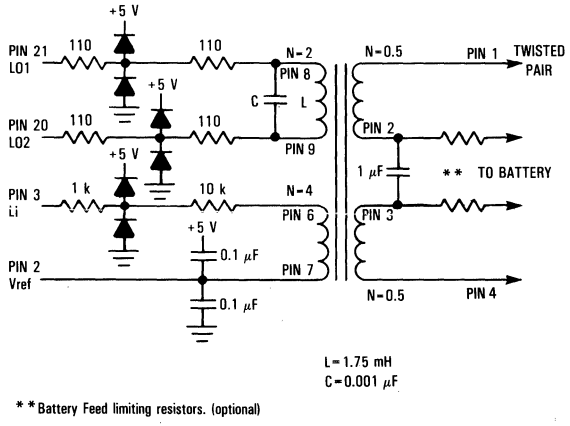


Figure 4. Application Circuit For the Transformer Interface

separated by cutting the panel in half along the two markers, shown in Figure 7. The master board schematic is shown in Figure 5 and the slave board schematic is shown in Figure 6, while the artwork is shown in Figure 7.

The master board contains the master UDLT (MC145422), DSI (MC145428), Mono-circuit (MC14403), the MC1488/1489 or MC145406 RS-232 drivers and receivers, and the necessary clock circuitry to drive these parts. The master board emulates both another digital telset plus the telephone switch interface to the slave board. The master typically is used in the digital switch at the PBX, networked with other digital and analog interface circuits.

The slave board contains the slave UDLT (MC145426), DSI (MC145428), Mono-circuit (MC14402), MC1488/1489, or MC145406 RS-232 Driver/Receiver chips. The slave side emulates a digital telephone where the analog information is digitized at the phone and the information from the phone is digital.

Both master and slave boards have their second eight kilobit signaling channel connected to a DSI for up to 9600 baud of user data simultaneously independent of voice. The baud rates are selected with switches BR1-BR3 (see strapping information). Each board has a DB-25 connector for easy connection to any terminal. Only TxD, RxD, and Ground are connected on the DB-25. Data to and from the DB-25 is fed through the MC1488, MC1489 and the MC145406 Driver/Receiver chips. The socket for the MC145406 RS-232 Driver/Receiver chip is included on each board for evaluation. This part can replace both the driver and receiver chips. Once replaced, the user at his option can cut the MC1488 and MC1489 pads out of the PC board along the dashed lines. This enables each board to fit in a K-2500 phone.

Each board has an RJ-11 socket for easy connection to any modular handset. The signal from each handset is fed through the respective mono-circuit into the 64 kilobit voice channel on the UDLTs. Both master and slave boards have space for a push button switch which can be hardwired onto the SI1, along with an LED on SO1 for signaling on channel one. This channel is optional to the user and can be used with a microprocessor in the phone or a pulse dialer. Signaling bits one and two provide eight kilobits-per-second each of protocol independent data. Switches permit access to particular features of the voice/data integrated circuits on both boards, as explained below.

STRAPPING INFORMATION

The component layout is shown in Figure 8. The layout shows the footprints for switches which can be used with wire straps. The solid lines indicate the normal strap positions which; select Mu law, 9600 baud data rate, with one start bit, eight data bits and one stop bit. The dip switches can be used if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1, S2	3
78J02	S3	1

STRAPPING ON THE MASTER

S1 — These straps select via U2 (MC145428 DSI) the number of stop bits, the length of the data word and the baud rate selected for the asynchronous data.

SW1 — (SB) A high selects two stop bits; a low selects one stop bit.

SW2-SW4-(BR3-BR1) — These bit rate inputs select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the supplied bit rates shown in the table on page 2-309 of the Telecommunications data book.

SW5 — (DL) This Data Length input pin selects a nine bit data word when high or an eight bit word when low.

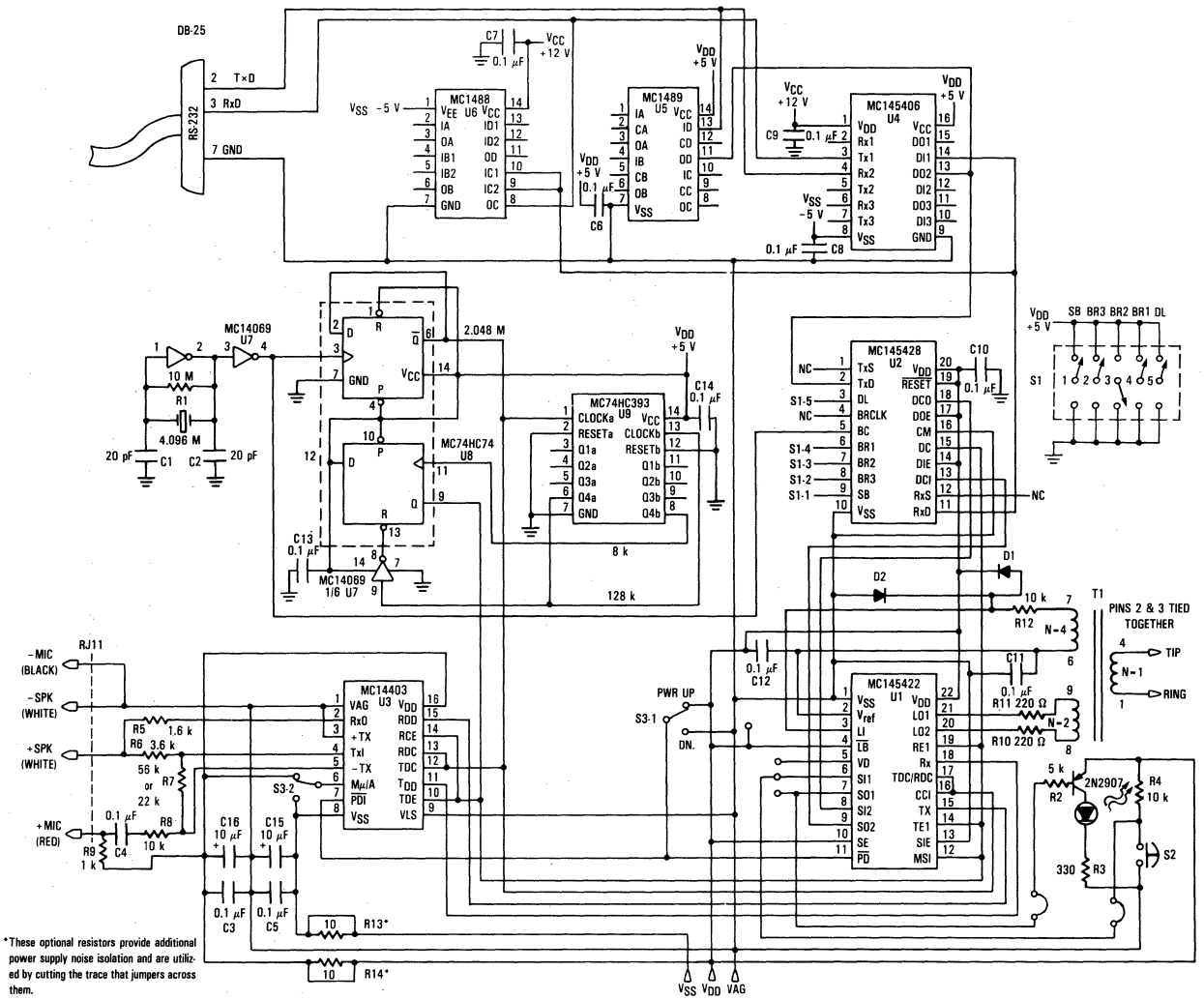


Figure 5. Master UDLT Demo Board

MASTER UDLT DEMO BOARD
PARTS LIST

PART	QUANTITY (PART NUMBER)
MC145422	1-U1
MC145428	1-U2
MC14403	1-U3
MC145406	1-U4
MC1489	1-U5
MC1488	1-U6
MC14069UB	1-U7
MC74HC74	1-U8
MC74HC393	1-U9
LEPCO P-1358A	1-T1
DB25	1
RJ11	1
GRAYHILL (SPDT 78J05)	1-S1
CUTLER-HAMMER B8500W/PZ81R	1-S2
GRAYHILL (SPDT 78J02)	1-S3
BANANA JACKS	6
20 pF	2-C1 & C2
0.1 μF	12-C3-C14
10 μF	2-C15, C16
10 M	1-R1
5 K	1-R2
330 Ω	1-R3
1.6 K	1-R5
3.6 K	1-R6
56 K	1-R7
10 K	1-R8
1 K	1-R9
220 Ω	2-R10, R11
10 K	2-R12, R4
10 Ω	2-R13, R14
CRYSTAL	1-4.096 M
JUMPERS	10
DIODES 1N914	2-D1, D2
LED (T1)	1
2N2907	1
SOLDER TAIL SOCKETS	
14 PIN	5
16 PIN	2
20 PIN	1
22 PIN	1

S2 — This switch is optional and is hardwired to signaling channel one for demonstration using LEDs. The footprint for this switch is included on the board.

This switch can be obtained from:

Cutler-Hammer
P/N B8500W/P281R

S3 — These straps select Mu or A laws and power down on the MC14403 Mono-circuit and MC145422 master UDLT.

SW1 — (PD) This strap when high, powers both the mono-circuit and master UDLT. When low, both parts are powered down.

SW2 — (Mu/A) Selects Mu or A law coding.

Loopback and Valid Data on the master can be accessed via pads.

STRAPPING ON THE SLAVE

S1 — Same as S1 on the master; selects asynchronous data format and bit rate.

S2 — These straps select Tone Enable, Power Down, Mu/A, and Loopback features of the slave (MC145426) as well as Mu/A and Power Down on the MC14402 Mono-circuit.

SW1 — (TE) A high enables a 500 hertz tone.

SW2 — (PD) Powers both the slave and mono-circuit up or down. High = powered up, and Low = powered down.

SW3 — (Mu/A) Selects Mu or A law coding for the mono-circuit.

SW4 — (Mu/A) Selects Mu or A law coding for the slave UDLT.

SW5 — (LB) When low, the 64 kilobits-per-second of information coming from the master will loop through the slave and return to the master. The signaling bits are unaffected.

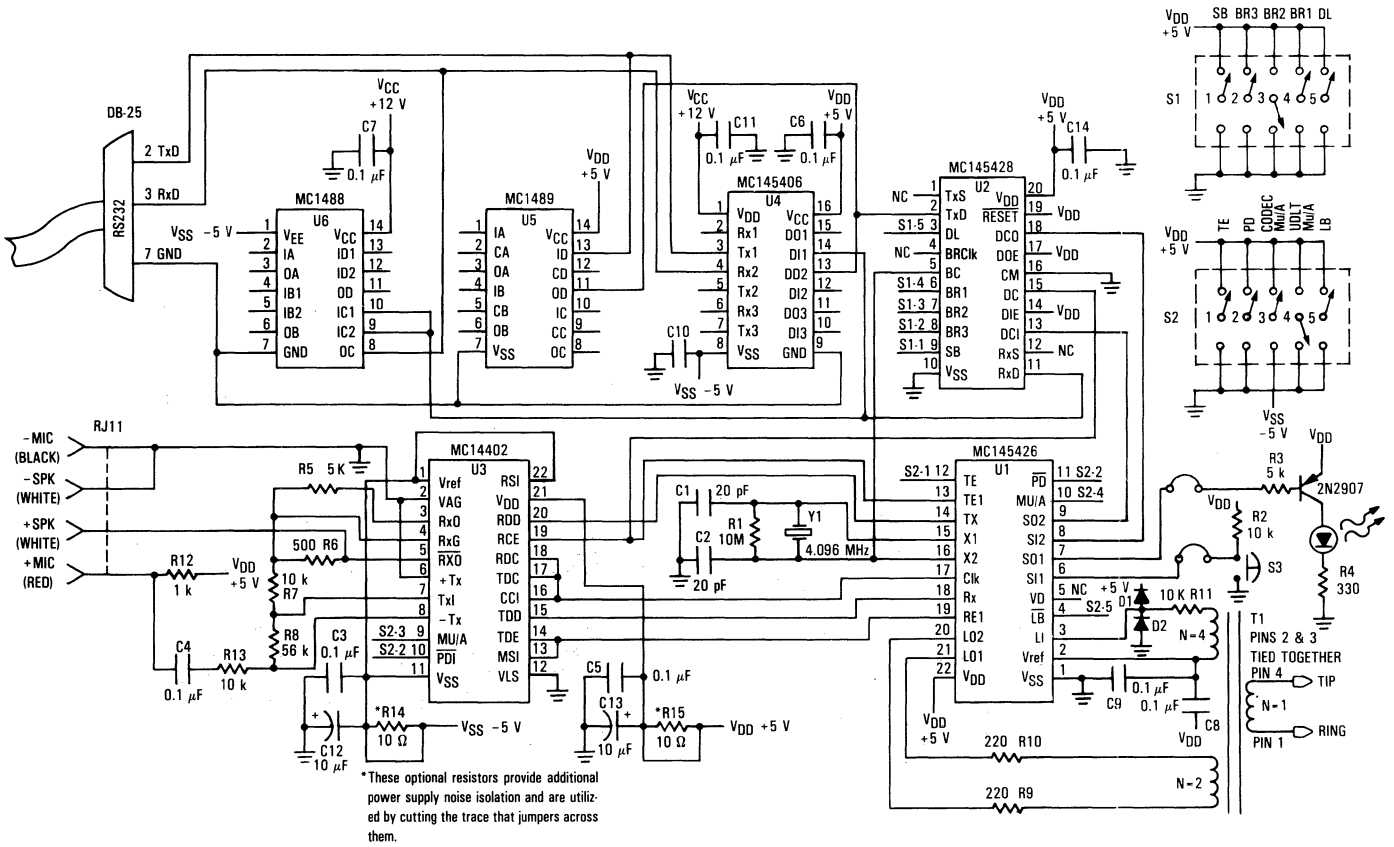
S3 — Same as the S2 switch on the master.

POWER SUPPLY CONSIDERATIONS/LAYOUT GUIDELINES

The power supply requirements for these boards are V_{DD} at +5 volts, V_{SS} at −5 volts and V_{CC} which is the RS-232 driver positive voltage of +7 to +12 volts for the MC1488. V_{CC} may be as low as +5 volts with the MC145406 Driver/Receiver chip. The power supply current required by each of these voltages is less than 30 milliamperes. This results in a total slave board power consumption of less than 400 milliwatts. This amount of power may be supplied by the loop using a linear supply. To isolate the RS-232 port with respect to earth ground, a switching regulator powered by the loop or an external power supply will be required. If a switching regulator is used, it should be synchronized to the eight kilohertz and 128 kilohertz clocks of the slave UDLT to reduce the affects of aliasing noise into the analog circuitry of either the UDLT or audio voice channel. This function will be supported by the MC34129 Digital Telephone Switching Power Supply Controller chip. This device has the capability to power-up and regulate on its internal oscillator. After regulation is established it can synchronize to an external clock such as the slave's 128 kilohertz clock.

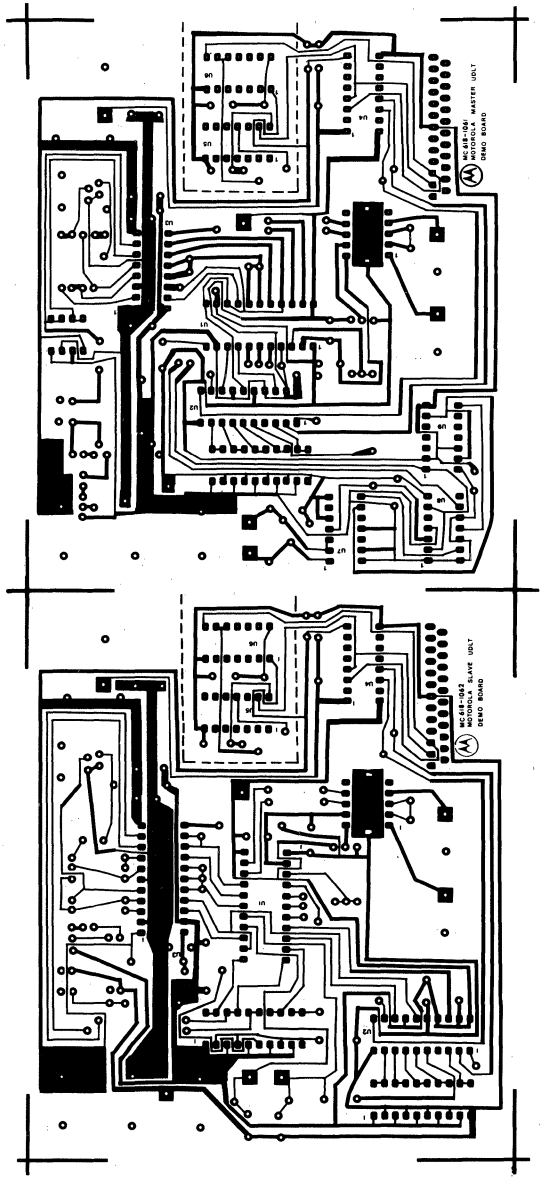
SLAVE UDLT DEMO BOARD PARTS LIST

PART	QUANTITY (PART NUMBER)	PART	QUANTITY (PART NUMBER)
MC145426	1-U1	500 Ω	1-R6
MC145428	1-U2	10 K	1-R7
MC14402	1-U3	56 K	1-R8
MC145406	1-U4	220 Ω	2-R9, R10
MC1489	1-U5	10 K	3-R11, R13, R2
MC1488	1-U6	1 K	1-R12
LEPCO P-1358A	1-T1	10 Ω	2-R14, R15
DB25	1	JUMPERS	12
RJ11	1	CRYSTAL	1-4.096 M
GRAYHILL (SPDT 78J05)	2-S1 & S2	LED (T1)	1
CUTLER-HAMMER B8500W/P281R	1-S3	DIODES 1N914	2-D1, D2
BANANA JACKS	6	2N2907	1
20 pF CAPS	2-C1 & C2		
0.1 μF CAPS	10-C3-C11, C14	**SOLDER TAIL SOCKETS**	
10 μF CAPS	2-C12, C13	14 PIN	2
10 M	1-R1	16 PIN	1
5 K	1-R3	20 PIN	1
330 Ω	1-R4	22 PIN	2
5 K	1-R5		



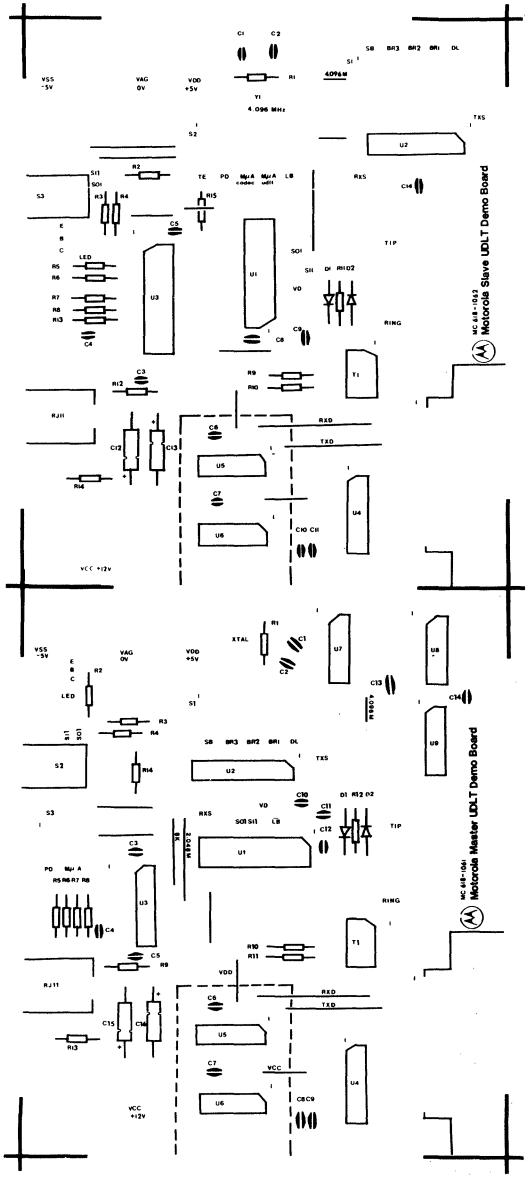
*These optional resistors provide additional power supply noise isolation and are utilized by cutting the trace that jumpers across them.

Figure 6. Slave UDLT Demo Board



NOTE: Drawings are not actual size.

Figure 7. Artwork of UDLT Voice/Data Evaluation Board



NOTE: Drawings are not actual size.

Figure 8. Component Layout

A Voice/Data Modem Using the MC145422/26, MC145428 and MC14403

GENERAL APPLICATIONS

This voice/data application allows an analog telephone system to support simultaneous voice and data across a single twisted-wire pair. Figure 1 shows how this system is implemented. To use the voice/data modem, the analog telephone line must be intercepted at the telephone system by one modem (the PBX-CPU Interface). The analog signals are then converted to digital signals, combined with data and transmitted down the remaining line as a digital loop. The second modem (the Telset-Terminal Interface) terminates the digital loop, reconstructs the analog signals and sends this information to the telephone that is plugged into the modem. The digital data is removed from the digital loop information and routed to the endpoint terminal. Any signalling information (hookswitch status and ringing) is handled by a second data channel, and it too is combined with the data and digitized voice for transmission on the digital loop.

ANALOG CODING AND DECODING

Analog signal digitization and reconstruction on both modems are done by the MC14403 Mono-circuit. The mono-circuit band limits incoming analog signals to prevent aliasing and then samples them with a sample and hold amplifier. This information is then digitized by an on-board analog-to-digital converter. This converter creates an eight bit 'companded' word for each sample by converting the signal to a pseudo-logarithmic form known as Mu-Law companding (A-Law companding is also available). In this manner approximately 78 dB of dynamic range can be represented by compromising the signal-to-distortion specifications. The mono-circuit is also capable of performing the reverse digital-to-analog conversion for this 'companding' technique. There is a reconstruction filter to convert the resultant stepped waveforms into a continuous waveform that very closely approximates the original analog input.

THE DIGITAL LOOP TRANSMISSION

The MC145422 master Universal Digital Loop Transceiver (UDLT) and MC145426 slave UDLT are used to transmit the digital information between the modems. In addition, the slave UDLT must be capable of determining and maintaining synchronization with the master UDLT so that word boundaries may be defined. The UDLT transmits a 10 bit, 256 kilobaud burst of information at an 8 kHz rate. By controlling the frequency of the burst from the master, the slave can sense and generate syncs. In this 10 bit word is the 8 bit voice sample along with one signalling bit and one data bit. Since each burst carries one digital "voice" word, the UDLT must create bursts at a rate of 8 kHz. This obviously means that both the data channel and the signalling channel operate at an 8 kbps speed.

ASYNCHRONOUS TO SYNCHRONOUS DATA CONVERSION

Since data is transferred at an 8 kbps rate in a synchronous mode, the MC145428 Data Set Interface (DSI) is used to convert an asynchronous data stream into the 8 kbps synchronous stream. The DSI can take data at speeds up to 9600 baud on the asynchronous channel and convert it to 8 kbps synchronous. The DSI is capable of supporting asynchronous speeds well in excess of 9600 baud, however, with an 8 kbps synchronous channel, dynamic handshaking on the asynchronous channel would be required. The DSI is also capable of converting the received synchronous data back into asynchronous data at the same time.

THE PBX-CPU INTERFACE

Figure 2 shows the block diagram of the PBX-CPU Interface. This circuit contains an analog interface that mimics the telephone electrical characteristics with respect to the PBX. This makes the voice/data modem transparent to the telephone system. The RS-232-C terminal interface is a 9600 baud asynchronous interface that appears to be a modem (data set equipment) to the data device (data terminal equipment). The digital loop is a specially devised transmission scheme that uses the UDLT to its fullest advantage. The digital loop is capable of excellent data performance (better than 8×10^{-8} bit-error-rate in 95% of the installations) on twisted pair up to 2 kilometers in length (26 gauge wire worst case).

The analog loop as shown in Figure 3 must be able to provide all the necessary interface considerations to simulate a telephone. The interface must be able to control the loop like a phone and it must be able to interface the voice signals, i.e., provide a 2-to-4 wire hybrid. In an idle condition (the handset is in the cradle or "on-hook"), the telephone appears as a high dc impedance. The relay provides this by "breaking" the loop and preventing dc current flow. When the phone goes off-hook, the dc impedance is drastically reduced. In a normal environment the phone must draw a minimum 20 mA of loop current, and since 48 volts is supplied to the loop at all times, this can be accomplished with resistor R6 or R7. This would energize a "ring-trip" relay coil which would disconnect any ring signals in the telephone system. At the same time an analog voice path would be established. The ac impedance of the telephone is typically held to 600 ohms to maintain transmission line balance and to minimize 60 Hz noise.

When the phone is on hook, it must be capable of detecting a ring signal. Ringing is typically a 100 volt RMS 20 Hz signal impressed on the 48 volt dc level. In this scheme ringing is detected with the MC34012 (U9) bipolar ringer chip. The 2-to-4 wire hybrid not only preserves the 600 ohm ac impedance, but it also converts a 4-wire system (separate transmit and receive) into a 2-wire current loop environment. In this design this is done with a duplexer circuit made up from the mono-circuit op-amps and resistors R12 through R16. Diodes 4 and 5 prevent excessive voltage transients from damaging the mono-circuit (U7). Engineering Bulletin EB111 provides a detailed analysis of the duplexer design.

TIMING SIGNAL GENERATION

The timing signals that drive the mono-circuit, UDLT (U4) and DSI (U5) are derived from U1, U2 and U3. U1A is a standard CMOS crystal oscillator topology designed for AT-cut parallel resonant crystals. U1B buffers the master clock signal (4.096 MHz) and then sends it to the DSI and U2A. U2A is a flip-flop that divides the signal by 2 to get the mono-circuit and UDLT master (CCI) and data clocks (2.048 MHz). U3 and U2B are a divider network that creates the 8 kHz master sync signal from the 2.048 MHz clock. This 8 kHz signal is also used as the enable signals for data communication between the UDLT and mono-circuit, and the DSI and UDLT.

Voice data is clocked out of both the UDLT and mono-circuit in 8 bit packets. These packets are defined by the 8 kHz sync positive-going level. This level is eight 2.048 MHz clocks long so the 2.048 MHz clock is the transport clock. The information is clocked out on leading edges. The information is clocked in on falling edges of the same 2.048 MHz clock and is likewise controlled by the positive portion of the 8 kHz signal.

Digital data and signalling information is directly controlled by the 8 kHz sync. The data is clocked into and out of the UDLT on the leading edge of the 8 kHz signal, and into and out of the DSI on the falling edge of the 8 kHz signal. This scheme is guaranteed on the UDLT but must be set up by tying the CM pin low on the DSI. Data out of the DSI can be three-stated through the DC0 pin, but in this application this is not necessary. The UDLT data-channel output can also be put into a high impedance mode by the SE pin, and again, this is not necessary in this application.

The asynchronous output and input of the DSI is an NRZ (Non-Return to Zero) 5-volt CMOS signal that requires level conversion to be RS-232-C compatible. The MC145406 CMOS RS-232-C Driver-Receiver chip (U6) performs this function quite nicely.

THE DIGITAL LOOP INTERFACE

The UDLT provides the needed signals for digital loop transmission. The interface circuit shown is a typical circuit designed to utilize the UDLT features to the fullest. For a detailed description of the digital loop, consult application note AN-943.

THE TELSET-TERMINAL INTERFACE

Figure 4 is the block diagram of the Telset-Terminal Interface. In a telephone system this unit must look like a line card to the telephone. The data communications port is once again intended to look like a modem. This portion of the design is the same as the digital loop interface. The only other variable part of the design is clock generation.

Clock generation is the sole responsibility of the slave UDLT. The UDLT has an on-board crystal oscillator that uses a 4.096 MHz crystal to generate a master clock. From this clock an 8 kHz sync similar to the one used in the PBX-CPU Interface is generated. This sync is now called TEI and is used like MSI except for communication from the mono-circuit. A sync that is basically the inverse of TEI, called REI, is used to enable the mono-circuit to output digital voice, and for the UDLT to receive this voice. The data clock that is generated (128 kHz) is used to clock the data with respect to TEI and REI. The DSI will use TEI to clock data to and from the UDLT, and it will get a master 4.096 MHz clock by tapping off the crystal oscillator output (X2).

The analog loop interface (see the schematic in Figure 5) uses the same duplexer circuit for regeneration of the 2-wire loop, but it must provide the complimentary signalling functions. It must first supply power to the telephone at all times and be able to tell when the phone is off-hook. Power is supplied by feeding the ±5 volt supplies over the loop through current limiting resistors (R13 + R14). Current flow is detected through the opto-coupler (U5) when the phone is off-hook, and then hook status is passed to the loop relay on the PBX-CPU interface. Ringing is handled within the modem as opposed to generating the ring voltage and sending it to the phone. The output of the UDLT signalling channel toggles at the typical 34012 rate when the PBX is ringing out, so this output is used to drive a transistor which in turn drives a piezo speaker. An alternate solution would be to drive a small PM-type speaker that has a capacitor filter to eliminate harsh harmonics from the square waves.

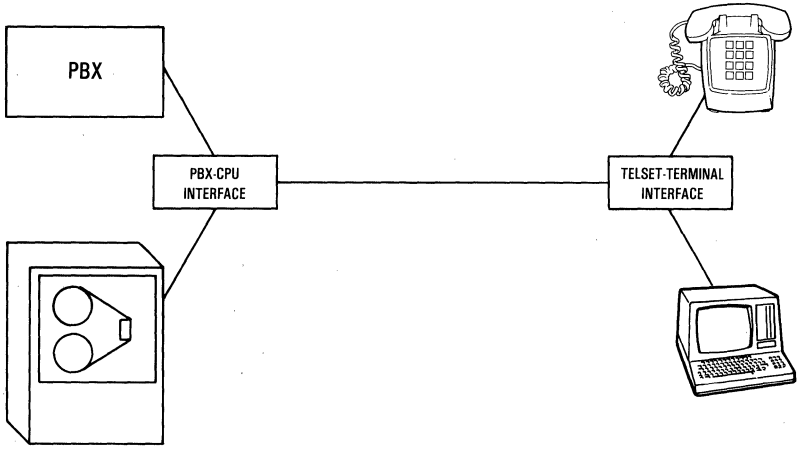


Figure 1. Typical Voice/Data Modem Implementation

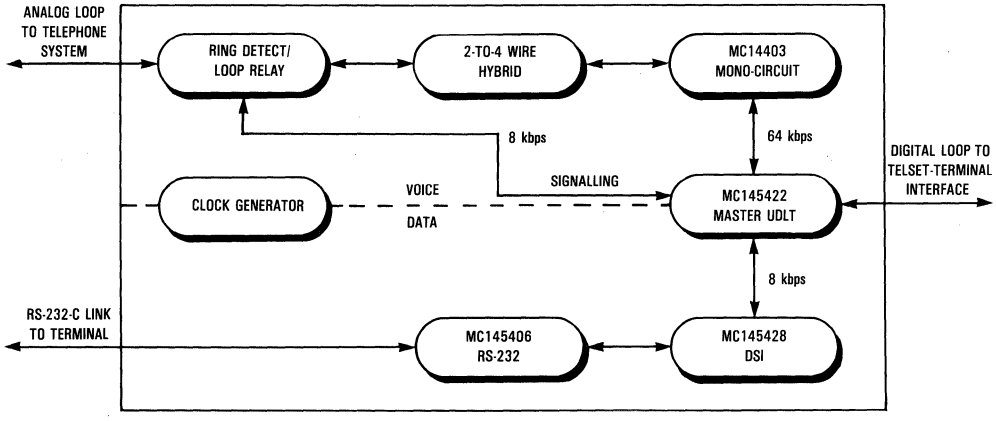


Figure 2. PBX-CPU Interface Block Diagram

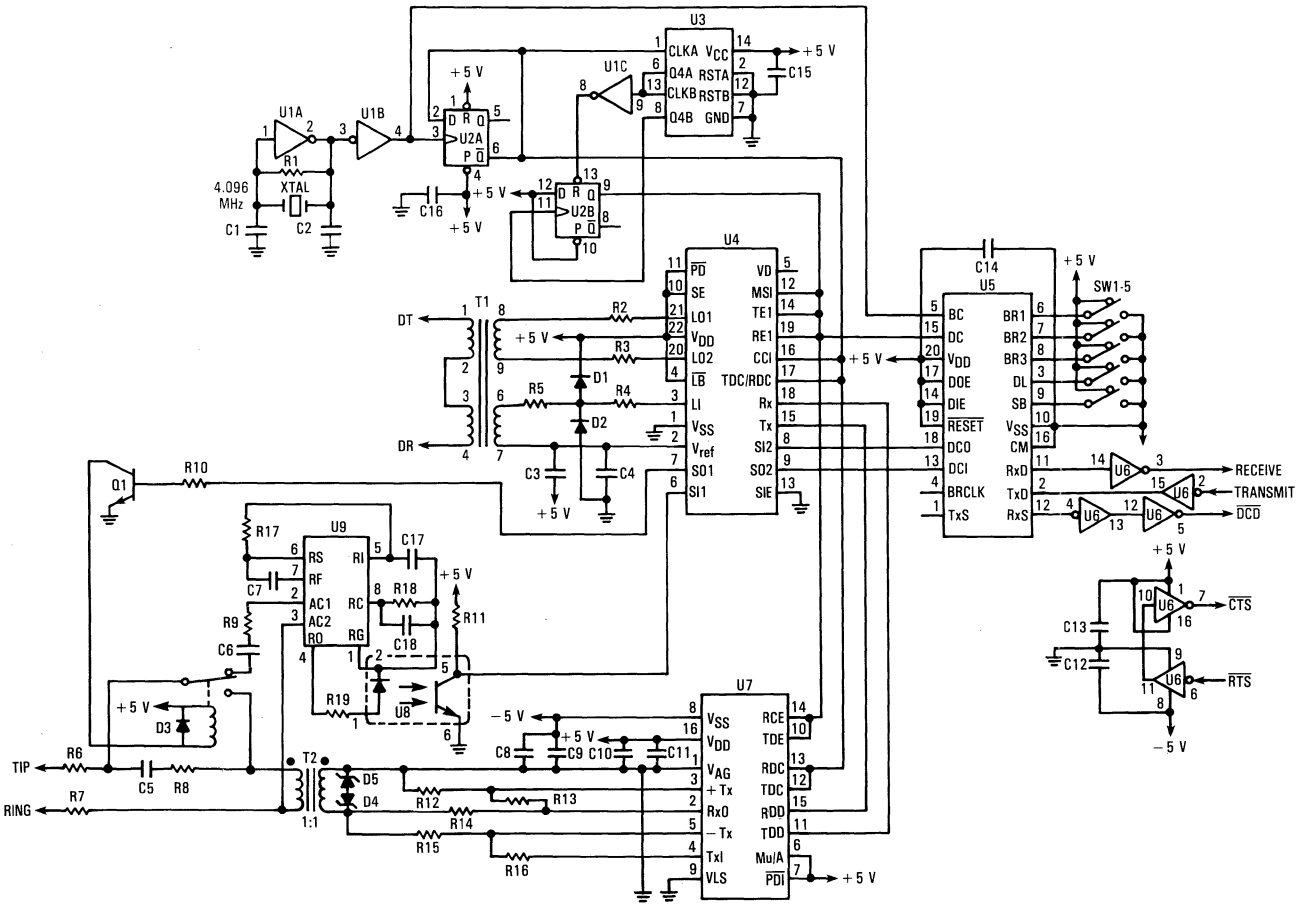


Figure 3. PBX-CPU Interface

PBX-CPU Interface Parts List

R1- 10 MΩ
R2- 220 Ω
R3- 220 Ω
R4- 1 kΩ
R5- 10 kΩ
R6- 67 1/2 W
R7- 67 1/2 W
R8- 560 Ω
R9- 4.7 kΩ
R10-4.7 kΩ
R11-270 kΩ
R12-10 kΩ
R13-20 kΩ
R14-600 Ω
R15-10 kΩ
R16-20 kΩ
R17-1.8 kΩ
R18-180 kΩ
R19-330 Ω

C1- 20 pF
C2- 20 pF
C3- 0.1 μF
C4- 0.1 μF
C5- 0.005 μF 1 kV
C6- 0.47 μF
C7- 2 μF
C8- 10 μF
C9- 0.1 μF
C10-10 μF
C11-0.1 μF
C12-0.1 μF
C13-0.1 μF
C14-0.1 μF
C15-0.1 μF
C16-0.1 μF
C17-4.7 μF
C18-1000 pF

D1- 1N914
D2- 1N914
D3- 1N4001
D4- 1N4683
D5- 1N4683
XTAL-4.096 MHz
U1- 74HCU04
U2- 74HC74
U3- 74HC393
U4- MC145422
U5- MC145428
U6- MC145406
U7- MC14403
U8- 4N26 Optocoupler
U9- MC34012
Q1- 2N2222

T1- Lepco P-1358-A
T2- 600 Ω:600 Ω
SW1-5:SPDT

Telset Terminal Interface Parts List

R1- 10 MΩ
R2- 1 kΩ
R3- 220 Ω
R4- 220 Ω
R5- 1 kΩ
R6- 10 kΩ
R7- 270 kΩ
R8- 10 kΩ
R9- 20 kΩ
R10-600 Ω
R11-10 kΩ
R12-20 kΩ
R13-92 1/2 W
R14-92 1/2 W

C1- 20 pF
C2- 20 pF
C3- 0.1 μF
C4- 0.1 μF
C5- 47 μF
C6- 0.1 μF
C7- 10 μF
C8- 10 μF
C9- 0.1 μF
C10-0.1 μF
C11-1 μF
C12-0.1 μF
C13-0.1 μF

D1- 1N914
D2- 1N914
D3- 1N4683
D4- 1N4683
Q1- 2N2222
Q2- 2N2907
XTAL-4.096 MHz
U1- MC145426
U2- MC145428
U3- MC14403
U4- MC145406
U5- 4N26 Optocoupler

T1- Lepco P-1358-A
T2- 600 Ω:600 Ω
SW1-5:SPDT

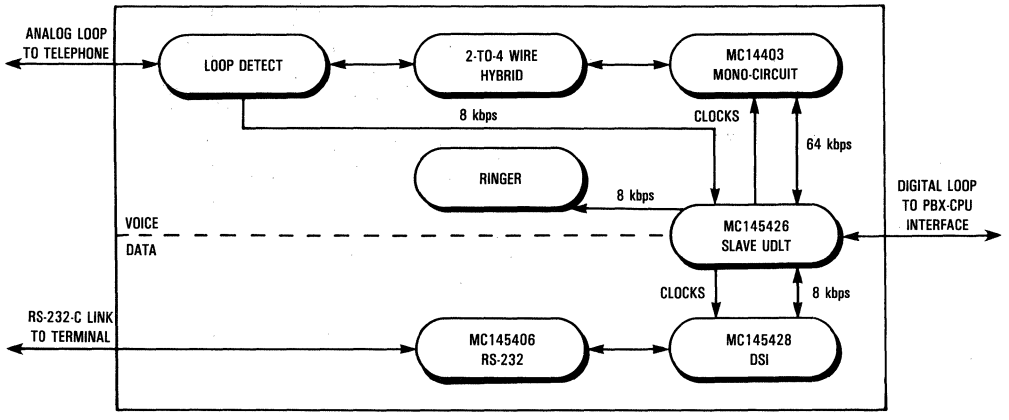


Figure 4. Telset-Terminal Interface Block Diagram

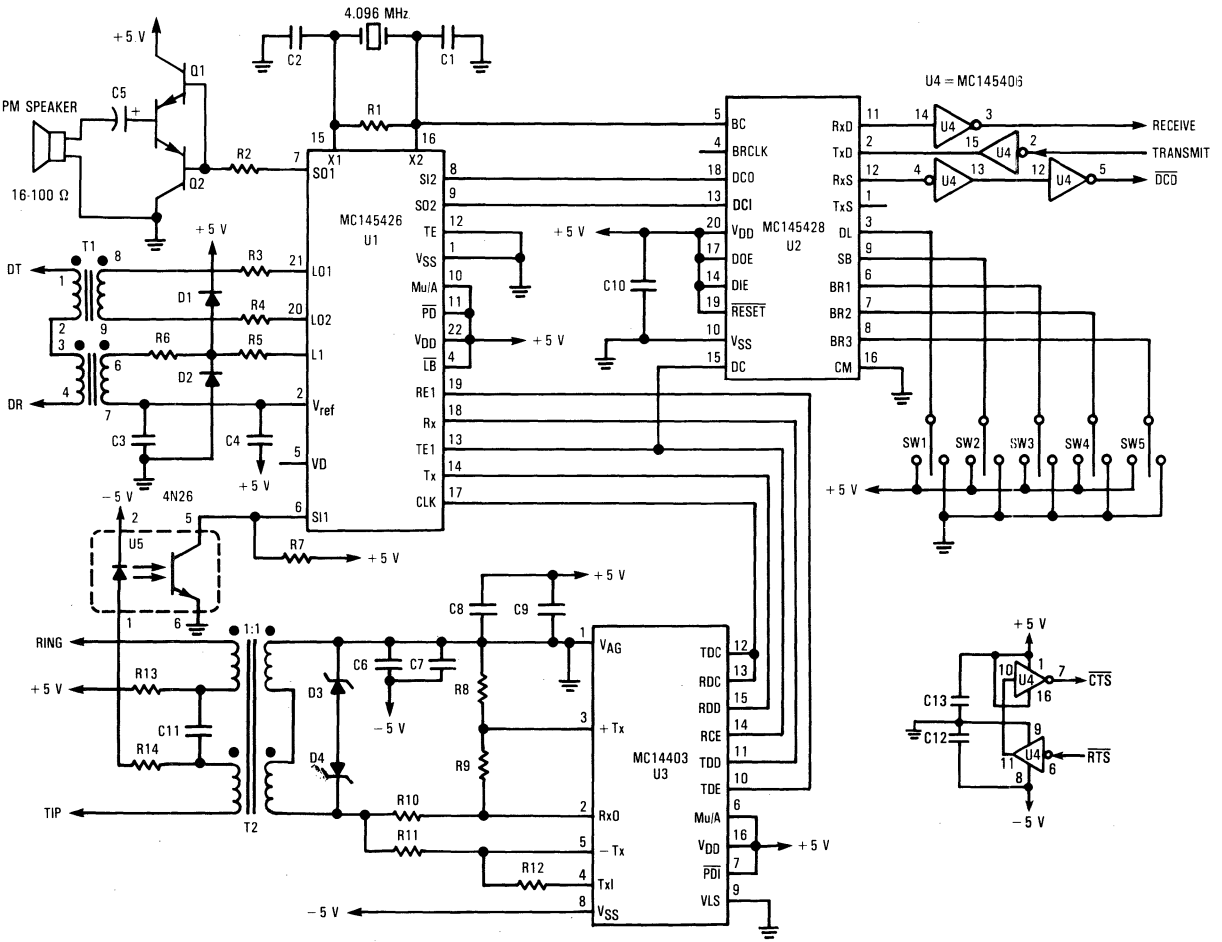


Figure 5. Telset-Terminal Interface

AN968

A Digital Voice/Data Telephone Set

by
Eric Fiene, Telecom Design Engineering, and
Glen Zoerner, Telecom Systems Design

OVERVIEW

This application note presents the design of a digital voice/data telephone set which provides standard analog telephone functions while simultaneously transmitting 9600 baud asynchronous data. This telephone set is built around Motorola's MC145422/26 UDLT (universal digital loop transceiver) family of voice/data ICs. The UDLTs provide 80 kbps full-duplex synchronous communication at distances of up to two kilometers on a single 26 AWG twisted pair telephone wire. The MC14403 codec/filter and MC145428 data set interface (DSI) convert voice and data signals respectively into digital formats compatible with the UDLTs' transmission scheme. The design includes the MC145413, a full-featured pulse/tone dialer, and the MC145406, a CMOS RS-232 driver/receiver for communicating with an external terminal or PC. An efficient switching power supply utilizing the MC34129 provides isolated power for the digital telephone set directly from the 48 V available on the transmission twisted pair.

BACKGROUND

Data has been transported over telephone lines for years, but the techniques for compressing the data into the voice bandwidth are getting more elaborate and expensive as data rates increase. Digital telephones simplify the task by directly sending high-speed digital data over the wires for distances of up to 2 km. The data is combined with voice information digitized by the codec/filter and signalling. This combined signal is transported over existing wiring to a digital linecard in a PBX or a voice/data multiplexer.

Digital PBXs used with analog telephones convert analog voice information into digital signals on the linecards for routing through the switch matrix. In a system where the analog telephones are replaced by digital phones, the digitization is still performed, but it is done in the phone itself and digital information is transported on the wires. Data from an attached PC or terminal can easily be combined with the digital voice and be transported to the PBX. At the linecard, the data can either be routed through the switch matrix or separated from the voice and connected directly to a data-only PBX or computer. Signalling between a digital telephone and the PBX is typically done by packet messages, with a microprocessor in the telephone to interpret the messages. This digital telephone uses traditional tone signalling on the voice channel. Hookswitch status is sent to the PBX on the inbound (to the PBX) link of the 8 kbps Signalling Channel One, and ringing information is sent to the phone on the outbound (from the PBX) link of Signalling Channel One.

This digital telephone could be used with a special digital linecard in a PBX or a voice/data multiplexer. To maintain generality, this application note will describe a system where a multiplexer is used rather than a linecard in a specific PBX system. The general principles, however, can be used in a linecard design. This telephone design has been used with both a digital linecard and a voice/data multiplexer.

The voice/data multiplexer in Figure 1 is described in detail in application note AN949. However, a brief description will be made here. From the PBX's point of view, the multiplexer appears to be an ordinary telephone. The telephone hookswitch is replaced by a relay which is controlled by a signal from the digital telephone. The ringing signal from the PBX is detected, sampled, and transported to the digital telephone where it is amplified and applied to a speaker. Analog voice signals are digitized and reconstructed and applied to the wires connected to the PBX through the duplexer in the codec/filter. Asynchronous data from the computer or data switch is synchronized to the UDLT timing by the DSI and added to the digital data stream. The combined signal is transported to the digital telephone which separates the signals and attaches to the data terminal. DC power is applied to the twisted pair wire at the multiplexer and transported over the wires so no extra power cords are required for the telephone.

The following sections describe the details of the digital telephone. Figure 2 shows a block diagram of the digital telephone set. Figures 3 and 4 are complete schematics of the telephone circuitry and the power supply respectively.

UDLT

The heart of the digital telephone set is the UDLT slave (MC145426). This chip is essentially a modem transceiver which operates over standard twisted pair telephone wiring. A 256 kbps data rate using modified differential phase shift keying (MDPSK) in a half-duplex time compression multiplex or "ping-pong" scheme provides full-duplex 80 kbps transmission. Transmission begins with the UDLT master (MC145422), which is located at the other end of the twisted pair in the voice/data multiplexer, bursting 10 bits of information to the slave. A similar burst is returned from the slave to the master a short time after the master's burst has been demodulated. This exchange occurs 8000 times per second

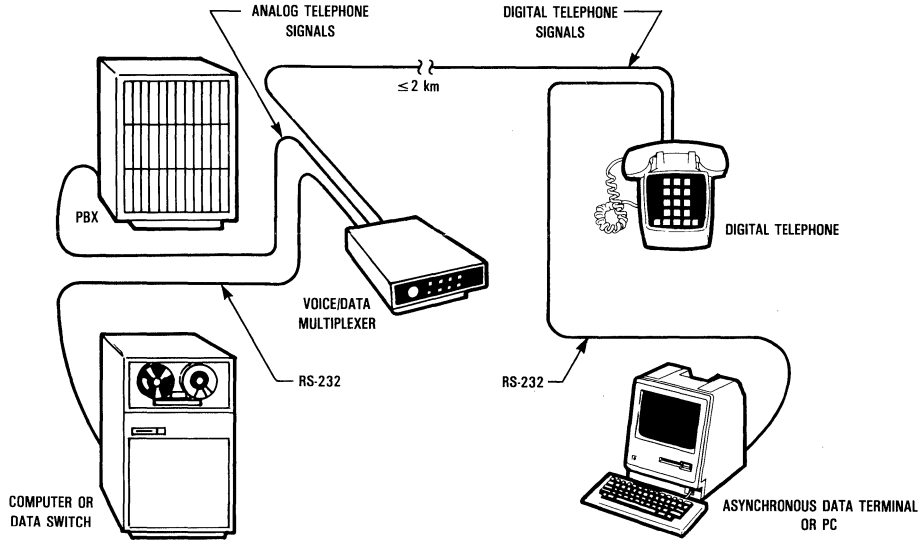


Figure 1. Voice/Data System

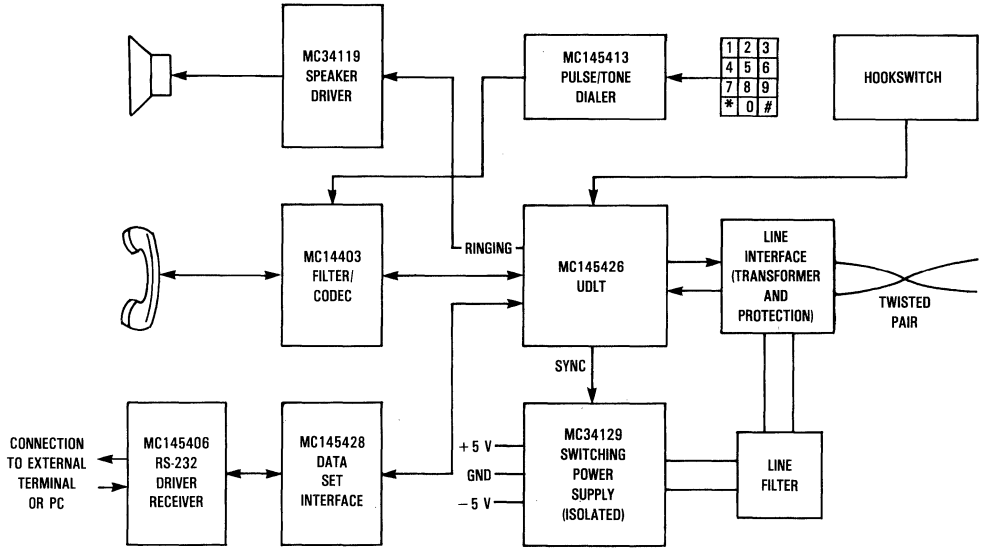


Figure 2. Digital Telephone Block Diagram

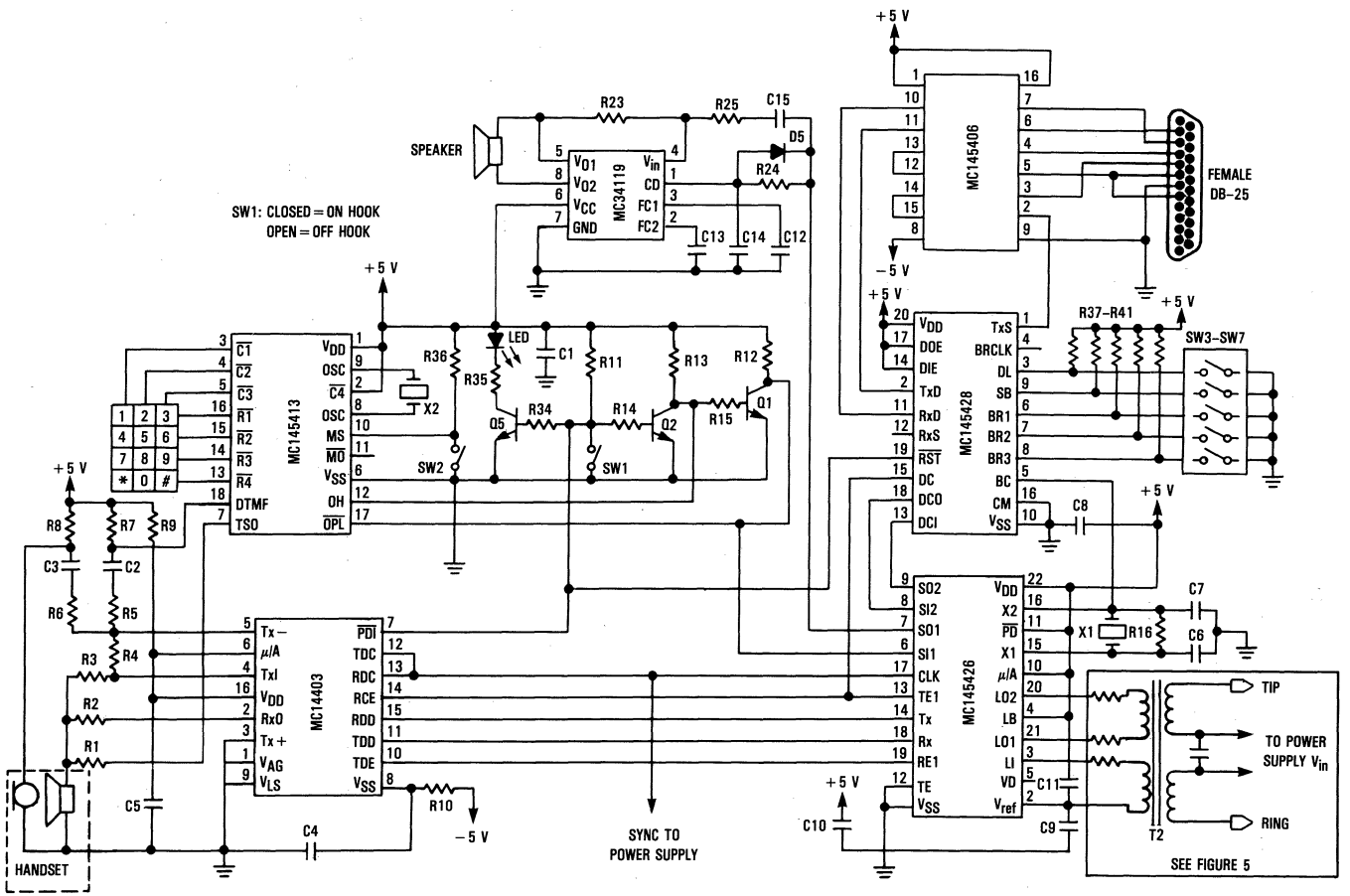


Figure 3. Digital Telephone Schematic

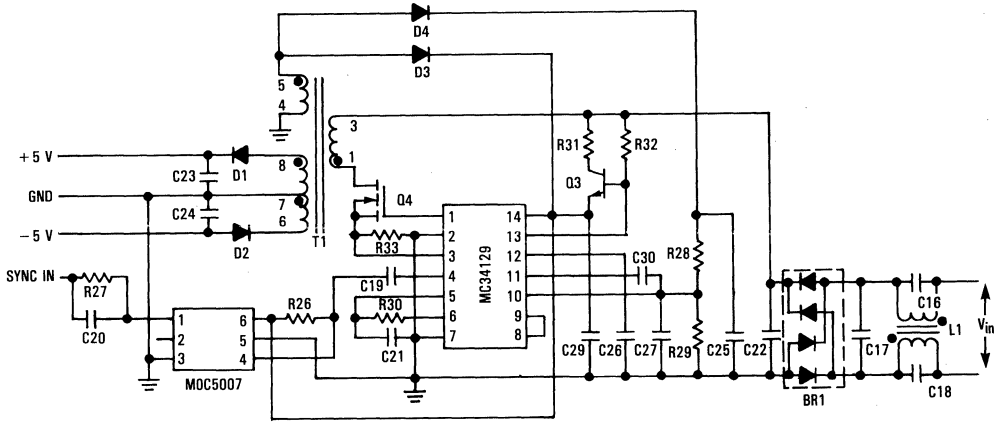


Figure 4. Switching Power Supply

PARTS LIST FOR FIGURES 3, 4, AND 5

Resistors

R1	22 kΩ
R2	3.3 kΩ
R3	7.5 kΩ
R4	47 kΩ
R5	22 kΩ
R6	10 kΩ
R7	620 Ω
R8	1 kΩ
R9-R10	10 Ω
R11-R13	10 kΩ
R14-R15	100 kΩ
R16	10 MΩ
R17	10 kΩ
R18	5 kΩ
R19-R22	110 Ω
R23	75 kΩ
R24-R25	100 kΩ
R26	10 kΩ
R27	3 kΩ
R28	9.1 kΩ
R29	1.3 kΩ
R30	22 kΩ
R31	2.2 kΩ
R32	220 kΩ
R33	10 Ω
R34	100 kΩ
R35	560 Ω
R36-R41	10 kΩ

Inductor

L1 80 μH each winding on a common core

Capacitors

C1-C3	0.1 μF
C4-C5	10 μF
C6-C7	20 pF
C8-C9	0.1 μF
C10	10 μF
C11-C15	0.1 μF
C16	0.005 μF
C17	0.1 μF
C18	0.005 μF
C19	100 pF
C20	0.01 μF
C21	330 pF
C22	100 μF (50 V)
C23-C24	100 μF (16 V)
C25	10 μF (16 V)
C26	0.1 μF
C27	510 pF
C28	0.1 μF
C29	10 μF (16 V)
C30	0.01 μF

Transformers

T1: Power Transformer
Coilcraft G6808-A
T2: Line Transformer
Coilcraft G6320-D or
Lepco P-1358-A

Diodes

D1	1N5819
D2-D11	1N4148
BR1	3N248 Bridge Rectifier

Integrated Circuits

MC14513	Dialer
MC14403	Mono-circuit
MC145428	Data Set Interface
MC145426	Slave UDLT
MC145406	RS-232 Transceiver
MC34119	Speaker Driver
MC34129	Power Supply Controller

Optocoupler

MOC5007 High-speed Optocoupler

Transistors

Q1-Q2	2N3904
Q3	2N5551 160 V NPN
Q4	MTP2N20 Power MOSFET
Q5	2N3904

Switches

SW1	SPST Hookswitch
SW2-SW7	DIP Switches

(every 125 μs), so the transceivers effectively exchange 80 kbps of full-duplex synchronous data. The data is arranged into three channels, a 64 kbps full-duplex voice channel and two 8 kbps full-duplex data channels.

The slave UDLT generates all timing signals used by the digital telephone. Timing is synchronized to the received bursts from the master UDLT. A 4.096 MHz on-chip crystal oscillator is the basis for all clocks. A 128 kHz clock (CLK), which drives the mono-circuit's D/A and A/D circuits and synchronizes the power supply, is produced. An 8 kHz clock (TE1 and RE1) is also produced. Any timing slip from master to slave UDLTs is corrected every 125 μs, keeping the master and slave devices in perfect synchronism. The baud rate generator in the data set interface is driven by the 4.096 MHz clock on the slave UDLT.

The burst received from the master's transmission is input on the slave's line input (LI) pin. The burst is demodulated, separated into the three channels, then output on the digital side of the slave every 125 μs. Eight voice bits are output serially from the transmit data output (Tx) on the rising edges of CLK while TE1 is high. One signalling bit is output on signalling output 1 (SO1) on the rising edge of TE1. The outbound signalling channel one provides the ringing signal for the speaker amplifier (MC34119). The other signalling bit is output on signalling output 2 (SO2) to the data set interface (MC145428), also on the rising edge of TE1. This channel, both inbound and outbound, carries the data between the attached terminal and the data switch or computer at the voice/data multiplexer or PBX.

After the slave receives a burst from the master, it transmits a 10-bit burst of its own back to the master. The slave outputs this burst on its line driver outputs (LO1, LO2) which are push-pull drivers configured as a balanced bridge. These outputs directly drive the line transformer through a resistor loading and protection network (see Figure 5). The 10 bits of data which are transmitted to the master are input every 125 μs. Eight bits of voice data are input serially on the receive data input (Rx) on the falling edges of CLK while receive data enable (RE1) is high. A signalling bit which carries the digital telephone's hookswitch status back to the voice/data multiplexer is input on signalling input 1 (SI1) on the rising edge of TE1. Data from the attached terminal or PC is input on signalling input 2 (SI2), also on the rising edge of TE1.

Transformer T2 interfaces the twisted pair wire to the UDLT's LO1, LO2, and LI pins. It performs the functions of impedance matching, bandwidth limiting, and gain adjustment for the receive signals. At the frequencies of interest (128 kHz and 256 kHz), ordinary telephone wire has a characteristic impedance of about 110 ohms. The loading resistors R19–R22 between LO1, LO2 and the Tx winding of the transformer are set to 110 ohms. The series combination of these resistors is significantly higher than the 20-ohm output impedance of the LO1 and LO2 drivers causing the resistance presented to the transformer to be set primarily by the resistors alone. Clamp diodes D6–D9 protect the LO1 and LO2 outputs from transient signals on the twisted pair. Line settling between data bursts is improved by selecting a bandwidth of 20 to 512 kHz for the transformer interface. The lower corner frequency is set by adjusting the inductance of the transformer's Tx winding to 1.75 mH. The upper corner frequency is determined by the design of the transformer winding technique.

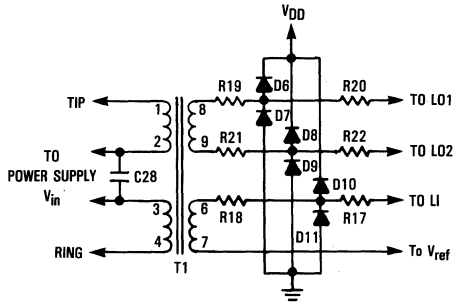


Figure 5. Line Interface and Protection

The impedance matching network on the transmit side of the transformer attenuates the transmitted signal by 12 dB. This loss is recovered in the receive side of the transformer. A step-up of 4:1 directly compensates for the 12 dB loss. As with the transmit side, a protection network is required. D10 and D11 clamp the received signal to a safe level but are sufficiently isolated by R17 so that they do not load the transformer when they are conducting. At 192 kHz (the spectral peak of MDPSK), 26 AWG wire attenuates signals about 17 dB/km. The receiver in the UDLTs has sufficient input dynamic range to operate on loops as long as 2 km. Transformers which are designed for the UDLT system may be obtained from:

Coilcraft, Inc.
1102 Silver Lake Rd.
Cary, Illinois 60013
Part Number: G6320-D

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
Part Number: P-1358-A

The transformer from Coilcraft is similar to the Leonard Electric device, except it has a Faraday shield between the Rx and Tx windings and the line windings. The shield helps reduce the spurious radiation from the digital circuitry onto the twisted pair.

CODEC/FILTER

The MC14403 codec/filter is a PCM codec-filter which performs D/A, A/D, band-limiting, and reconstruction filtering for the voice signals in the digital telephone. Analog voice signals in the 300 Hz to 3400 Hz frequency band are sampled at an 8 kHz rate. The samples are converted into a pseudo-logarithmic code known as PCM and passed to the UDLT for transmission to the voice/data multiplexer or PBX. Received digital signals are reconstructed at an 8 kHz rate back into analog voice signals.

Three signals are available for use on the analog input amplifier. They are Tx+ (noninverting input), Tx− (inverting input), and TxI (filter input). Sidetone (feedback from the handset microphone to earpiece) and gain balance are controlled with external components around the Tx and Rx operational amplifiers in the codec/filter. Tx+ is tied to ground and a gain setting resistor is placed between Tx− and TxI.

The microphone output from the handset and the DTMF output from the dialer are both ac coupled to the Tx− input. The output of this amplifier is digitized and output to the UDLT on TDD on the eight rising edges of TDC when TDE is high. Digital data is input from the UDLT on RDD on the first eight falling edges of RDC after the rising edge of RCE. This data is reconstructed and output on the analog output pin (RxO). This signal is summed with TSO from the dialer and TxI and applied to the speaker in the handset.

A decoupling RC filter is used to attenuate any power supply noise seen at V_{CC} and V_{SS} of the codec/filter. This filter consists of 10-ohm resistors in series with the power feed to V_{CC} and V_{SS} with 10 μF capacitors from V_{CC} and V_{SS} to ground. Also, to reduce noise in the ground paths, a star-grounding scheme is used where all ground pins of the circuits are connected to the power supply's central isolated ground.

DATA SET INTERFACE

The MC145428 data set interface (DSI) is an interface between an asynchronous data terminal and the synchronous 8 kbps full-duplex data channel of the UDLT. The DSI performs basic UART functions of start-bit and stop-bit detection of the asynchronous data. It also detects and transports break signals over the synchronous link. Start and stop bits are stripped from the data which is then loaded into a FIFO. The data is then sent to the UDLT for transmission to the far end of the digital link. On the receive side, the reverse of these actions is performed. Special synchronization characters (transparent to the user) are exchanged between DSIs to maintain synchronization. The DSI has an internal clock generator which produces the most commonly used baud rates. The DSI is capable of operating at data rates up to 128 kbps, however this application uses 9600 baud.

On the synchronous side of the DSI, data is output to the UDLT on the data channel output (DCO) on the falling edge of data clock (DC) while the data output enable (DOE) is high. Data from the DSI is input and output by the UDLT on SI2 and SO2 respectively. DC is connected to TE1 of the UDLT. DIE and DOE are connected to V_{DD}, permanently enabling the synchronous inputs and outputs. RESET is connected to the hookswitch, clearing the FIFOs and resetting the device when the digital telephone is not in use.

RS-232 DRIVER/RECEIVER

The RS-232 interface is connected as follows. Asynchronous serial data from the attached data terminal (Tx DATA, RS-232 pin 2) is through a receiver on the MC145406 RS-232 driver/receiver and connected to the transmit data input (TxD) of the DSI. Asynchronous serial data from the DSI is output on the receive data output (RxD) and fed through a driver on the MC145406 to the data terminal (Rx DATA, RS-232 pin 3). Another output of the DSI, transmit data status (TxS), is used to generate a clear-to-send signal for local flow control (CLEAR-TO-SEND, RS-232 pin 5). TxS goes low when there are two words in the DSI's transmit FIFO and must be inverted to provide the CTS function. TxS is applied to a receiver of the MC145406 for inversion and then fed through a driver to convert the signal to RS-232 levels. The MC145406 threshold for the RS-232 receivers is 1.8 volt so it may be used as an inverter for ordinary digital signals. The receive data status (RxS) pin of the DSI may be used as a carrier detector. Since it goes high when synchronization with the far-end DSI is established, it must also be inverted before conversion to RS-232 levels. As with the TxS signal, an RS-232 receiver is used an an inverter. The inverted signal is then converted to RS-232 levels by a transmitter and applied to RECEIVED LINE SIGNAL DETECT, RS-232 pin 8. The baud rate, word length, and number of stop bits used on the asynchronous side of the DSI are controlled by five pins: BR1-BR3, DL, SB. These inputs are controlled by a DIP switch. Table 1 shows the switch settings to configure the asynchronous data port.

DIALER

The pulse tone repertory dialer (MC145413) converts keyboard inputs to either pulses or dual tone multiple frequency (DTMF) or Touch-Tone outputs for use in telephone dialing. This device also provides last number redial and a nine number repertory memory. The digital telephone in this application uses a 3×4 class A single contact keyboard, although a 4×4 keyboard could have been used for enhanced features. The MC145413 operates in pulse mode at either 10 or 20 pulses per second, or tone dialing modes. These modes are determined by the mode select (MS) pin.

When the pulse dialing mode is used in this telephone, dialing information is output at 20 pulses per second. Note: The PBX used with this telephone is capable of accepting dialing pulses at this rate. Other applications may require the pulses at 10 pulses per second, in which case the wiring of the DIP switch would have to be modified appropriately. The pulse output OPL, is an N-channel open-drain transistor which is wire-ORed with the hookswitch. This point is sampled 8000 times each second by the UDLT, and the status is passed to the loop monitoring circuitry in the voice/data multiplexer on signalling channel 1. In the tone dialing mode, dialing information is output as tones corresponding to the row and column pressed. This signal is output on the DTMF OUT pin of the dialer and is coupled to the analog input of the codec/filter. The analog DTMF signal is thus carried to the PBX in digital form on the 64 kbps voice channel.

Table 1. DIP Switch Settings

Pin Name	Low	High
DL	8 bits	9 bits
SB	One	Two
MS	Tone	Pulse

Baud	BR3	BR2	BR1
9600	0	1	1
4800	1	0	0
2400	1	0	1
1200	1	1	0
300	1	1	1

SWITCHING POWER SUPPLY

Figure 4 shows the schematic of the switching power supply for the digital telephone. This power supply has the capability of supplying about 900 mW of power at ± 5 V when the length of the loop is 2 km. As the loop length is increased, the power available at the phone is reduced. To maintain stability of the power supply, the maximum power consumed by the phone (including the efficiency losses in the power supply) must be

less than 90% of the maximum power available (MPA) at the maximum loop length.

$$MPA = V_{source}^2/(4 \cdot R_{loop})$$

Example: R_{loop} for 2 km of 26 AWG wire = 576 Ω

$$MPA = 48^2/(4 \cdot 576\ \Omega) = 1\ Watt$$

The ±5 V outputs are isolated from the twisted pair so that a local ground reference may be established with the terminal attached to the RS-232 port.

The switching power supply operates by repetitively storing and releasing energy in a transformer. The energy is stored in the primary winding of transformer T1 for part of the switching cycle and discharged into the load through the secondary during the remaining part of the cycle. The controller for this power supply is the MC34129 high-performance current-mode power-supply controller. The MC34129 controls the current (energy) in the primary winding by varying the duty cycle of the power switch (Q4). As the duty cycle is changed, more or less energy is stored under control of the MC34129 to maintain regulation of the output voltage. The switching frequency of the power supply is synchronized to the 128 kHz clock signal used by the codec/filter by bringing CLK from the UDLT through an opto-isolator (MOC5007) into the sync input (pin 4) of the MC34129. Synchronization improves the idle-channel noise performance of the codec/filter and minimizes the filter requirements on the output of the power supply.

The input voltage for the power supply is taken from the 48 V available on the twisted pair. A 0.1 μf capacitor is placed between the two line windings of transformer T2. The dc voltage across the capacitor is then routed through a balanced three-pole elliptical lowpass LC filter (L1 and C16–C18) and a full-wave rectifier before being applied to the input of the power supply.

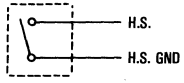
The power supply is regulated by two methods. Current in the primary winding is sensed as a voltage across resistor R30. Also, the +10 V nonisolated output is sensed by being fed back to the voltage divider formed by resistors R25 and R26. The controller maintains the voltage across R26 at 1.25 V by varying the switching duty cycle. This forces the output voltage to be 10 V. Regulation of the +5 V isolated outputs is maintained by the magnetic coupling from the 10 V winding to the +5 V windings. Because the primary current is sensed by the MC34129, pulse-by-pulse overcurrent limiting is automatically achieved. The power supply is thus fully protected against short circuits on the outputs. If an overload occurs, the MC34129 will shut the power supply down and attempt to restart. When the overload is removed, the power supply will again begin normal operation.

During normal operation, the MC34129 is powered by the +10 V output. However, since there is no voltage at this output when the circuit is first started-up, provisions must be made to power the circuit from another source until the outputs are stable. Transistor Q3 and the Start/Run output perform this task. During start-up, Q3 is biased on and power for the MC34129 is taken from the 48 V on the twisted pair through R28. After the power supply has completed the soft-start cycle and stabilized, transistor Q3 is turned off by the Start/Run pin (pin 13) and power is supplied by the +10 V output. This start-up sequence allows the power supply to reliably start in the presence of high source resistance seen at the end of a long twisted pair wire. Efficiency of this power supply is approximately 80%.

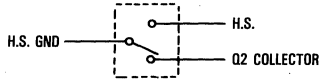
APPENDIX

On the printed circuit board there are three connections available for the hookswitch (SW1). These are +5 V, GND, and SI1. The following is a list of several implementations of the hookswitch.

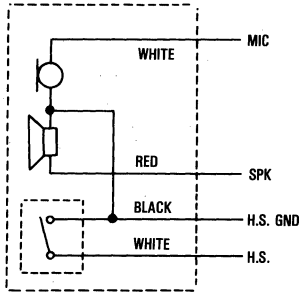
1. **Mechanical SPST switch (normally open)** — In this configuration the LED, R32, R31, and Q5 are not needed unless an LED signal is desired.



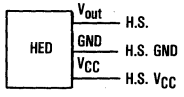
2. **Mechanical SPDT switch (normal position shown)** — In addition to the components listed in the above implementation, R14 and Q2 are not needed.



3. **Reed relay in handset (magnet in telephone case)** — The figure below shows how to modify the handset for this application.



4. **Hall Effect Device in telephone case (magnet in handset)** — For this and the previous application, a mechanical SPST switch can be used in parallel for on-hook operation.



IMPLEMENTING INTEGRATED OFFICE COMMUNICATIONS

By Tanya Tussing
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INTRODUCTION

ISDN has gotten a lot of attention during the course of the last year, and rightfully so. It's a revolutionary concept. The idea of being able to send high-speed data over a public network to anywhere in the world is phenomenal. But the hard questions concerning ISDN quickly become evident when a company contemplates designing a real ISDN system with an introduction date in the near future. Although the "U" interface being defined by the T1D1.3 committee in North America has a well defined function in the ISDN wide area network system, the local area network is a different situation.

ISDN discusses three local area network interfaces: the "S", "T", and "R" interface. (The ISDN reference model is shown in Figure 1.) The "S" and "T" interfaces have an identical specification, but the "R" interface is open, in other words—user defined. A key product strategy question asks which interface best services a particular function of the ISDN local area network. When formulating an answer, there are many parameters to consider. They all revolve around manufacturing costs vs. providing customers with the features they feel they need at the time the products are introduced. Some of these customer-driven parameters include price, performance, and compatibility to standards of terminals, peripherals—e.g., printers and the wide area network. These kinds of questions need to be addressed before a design specification can be completed.

ISDN REFERENCE MODEL

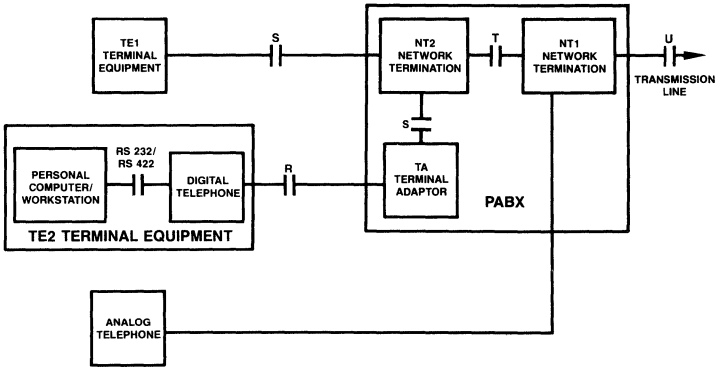


Figure 1

K5056

Originally prepared for Mini/Micro Northeast 1986.

Question 1: Which terminal standards must be supported by an ISDN local area network in the near future?

Answer: RS-232 is now, and will be for some time to come, the most prominent terminal interface specification. So, whatever method is used to transmit data to the terminal—"S/T" or another—an RS-232 interface will be needed for many terminals for quite awhile.

Question 2: Is ISDN a mature standard?

Answer: No, ISDN is not a mature standard. So, any product designed today will probably have to be modified to fulfill the final ISDN specification.

Question 3: Will an ISDN terminal using an "S/T" interface for layer 1 communication and LAP-D for layer 2 communication be the best voice/data solution available for most applications?

Answer: The "S/T" interface and LAP-D are both specifications which try to accommodate many different functions. In some cases they may provide more features than are needed— for a price that consequently cannot be justified.

Because of these kinds of reasons, Motorola has a two-part product strategy. First, Motorola introduced a family of cost-effective voice/data integrated circuits which are compatible with the evolution of ISDN. The second part of the voice/data strategy is to develop an "S/T" transceiver, an LAP-D controller, and a "U" transceiver, as the specifications become more clearly defined.

MOTOROLA'S VOICE/DATA I.C. SOLUTIONS

There are many different ways to design a voice/data terminal. The following paragraphs describe three different approaches which vary in complexity/cost, data rate throughput, transmission distance, and system flexibility.

SYSTEM I: BASIC VOICE/DATA TERMINAL—B + D

A basic terminal, as shown in Figure 2, uses the slave UDLT, MC145426, to communicate the voice and data information to a switch. In the switch's line card is a master UDLT, MC145422. It converts the signals back into the original PCM, data, and signalling format. So, the PCM code can be transmitted through the switch as if a monocircuit (codec/filter) were sitting on the line card, and one of the signalling channels can convey the switchhook and ringing information. In this configuration, the dialing information is transmitted in the voice path and would be handled like a normal analog line card in a digital PABX. Because the UDLT interfaces to the switch like a monocircuit, the conversion from analog line cards to digital line cards is relatively painless.

The other signalling channel sends data to the line card. At the master UDLT, this data can either be put into a separate time slot on the line card—allowing the data to be switched separately from the voice, or it can be stuffed into the least significant bit of the PCM word—allowing it to be routed around with the voice information. Routing voice and data through one time slot per phone decreases the number of time slots needed for the system, and consequently, the switching system's complexity decreases.

The Universal Digital Loop Transceiver

The UDLT is an 80 kilobit per second (kbps) synchronous transceiver chip set capable of transmitting data up to two kilometers on 26 awg twisted pair wire. Between the UDLT master—MC145422 and the UDLT slave—MC145426, 10 bit data bursts at a 256 kHz rate are sent back and forth from the master and the slave. This is called a "ping pong" transmission scheme.

B + D VOICE/DATA TERMINAL

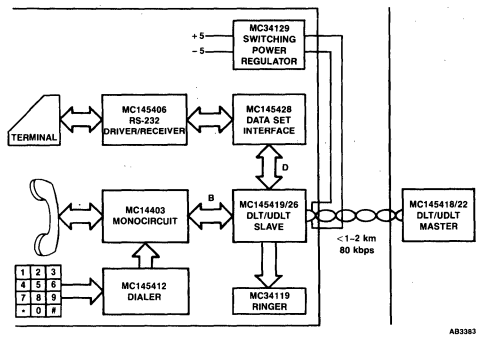


Figure 2

Figure 3 is a timing diagram showing the relationship between the master ane slave bursts, as well as the master sync input (MSI). First, a burst is differentially driven from the master's LO1 and LO2 pins to the slave's LI pin, referenced to V_{ref}. From this master burst, the slave synchronizes its clocks to the master's clocks and responds with a burst from its LO1 and LO2 pins to the master's LI pin.

The bursts are coded into a triangular Modified Differential Phase Shift Keyed (MDPSK) waveform. The MDPSK method was chosen because it minimizes radio frequency, electromagnetic, and crosstalk interference. Tests have shown that this MDPSK ping pong transmission technique can achieve better than a 10^{-7} bit error rate over two-kilometer distances.

The 10 bit data burst, from either the slave or the master, is derived from three different inputs of the chip. The Rx pin contributes 8 of the 10 bits, and the SI1 and the SI2 pins each contribute 1 of the 10 bits. Because both the master and slave bursts are typically sent at an 8 kHz rate, the data rates through these pins are 64 kbps, 8 kbps, and 8 kbps, respectively. The output of the 64 kbps channel is the Tx pin and the output of the 8 kbps channels are the SO1 and the SO2 pins. With the same data rate as the CCITT B channel, the 64 kbps channel can be used for standard PCM voice or it can be used to transmit high speed data. The 8 kbps channels are well suited for transmitting signalling—such as dialing, switchhook, and ringing information—or data. With a little external logic, the two 8 kbps channels can be combined into one 16 kbps channel—which is the same data rate as the CCITT LAP-D channel. This chip is available today in production quantities.

The Digital Loop Transceivers vs. the UDLT

The Digital Loop Transceiver (DLT) chip set, MC145418/MC145419, is very similar to the UDLT in function but is designed for applications requiring shorter loop lengths (< 1 k). There are three main differences between the UDLT and the DLT chips. The most important difference between the chip sets is that the UDLT automatically adjusts the threshold on the receive circuitry. This allows the UDLT to optimize its reception to a particular line's attenuation level. The DLT's threshold is externally set, so typically this receive optimization will not be achieved—unless some rather complex circuitry is implemented. Also, the DLT requires external drivers and usually transmits square waves instead of triangular waves. In conclusion, the UDLT has more features than the DLT, but the DLT's basic approach allows driver and threshold design flexibility. The DLT is available today in production quantities.

The Monocircuit Family

The single chip codec/filter (monocircuit) family consists of five different devices ranging in size from a 16 pin package to a 22 pin package. They are the 14400, the 14401, the 14402, the 14403, and the 14405. These chips perform standard PCM voice digitization and reconstruction. They will operate in both the U.S. standard, Mu-Law, and in the European standard, A-Law, companding formats. The chip includes on-board antialiasing/60 Hz rejection filtering, as well as low pass reconstruction smoothing filtering.

As opposed to just operating with split power supplies of ± 5 volts, the chip will operate well using a variety of

80 KBIT/SECOND CHANNEL TIMING

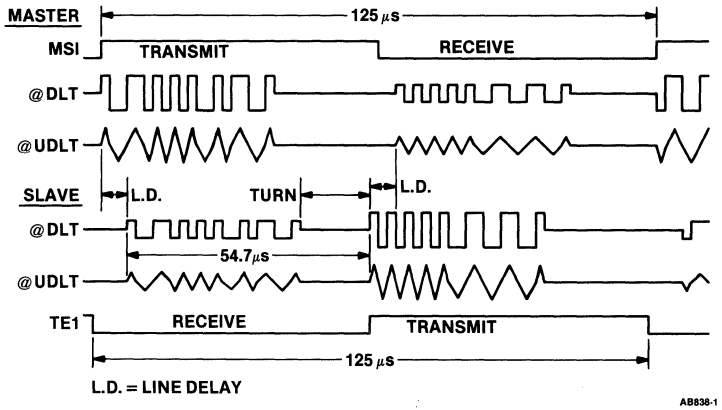


Figure 3

power supplies, 6 to 13 volt single supplies— or the equivalent in a split supply. In addition, by giving the V_{LS} pin the appropriate voltage level, the monocircuits' inputs and outputs will interface to other chips with either CMOS or TTL signal levels.

Although the monocircuits are available today in production quantities, an enhanced version of the existing monocircuit family is now being introduced. It features a typical idle channel noise of 9 dBrnco and a typical Power Supply Rejection Ratio (PSRR) of 55 dB over a 0-50 kHz range.

The Switching Power Supply Controller

A major consideration in designing a voice/data PBX is power. Providing power to digital phones, which may be on a two kilometer loop, is not a trivial task. The typical number of phones powered by a PBX alone means that the power supply in the PBX is a very significant design consideration. Also, because digital telephones require more power than analog phones, the maximum power available at the end of a two kilometer, 26 awg loop is not much more than the power required to operate a voice/data digital phone. Therefore, the efficiency of the power conversion method in the phone is critical—hence the importance of the efficiencies gained by using a switching power regulator.

Motorola's new switching power regulator, the MC34129, is especially designed to fulfill a digital telephone's power regulation requirements, although the regulator is popular for non-telecom applications as well. One of the most important features of this regulator is that it gives the designer the ability to synchronize his switching power supply to the sampling rate of the codec/filter in the phone. This is important because non-synchronized switching noise on the power supply of a codec can make meeting codec/filter idle channel noise specifications difficult. However, synchronized switching noise does not degrade a codec/filter's system performance.

A switching power regulator also offers another important feature for voice/data phones—line isolation. When driving the RS-232 input of a terminal with a local ground reference, isolation between the terminal's ground and the ground of the telephone line is necessary. This regulator can operate in an isolated or a non-isolated mode. The isolated mode simply requires an auxiliary winding on the transformer to supply power and a feedback signal. Otherwise, the chip is applied the same to isolated and non-isolated applications.

The Data Set Interface

The Data Set Interface (DSI), MC145428, is an asynchronous to synchronous converter. It takes data in a start/stop format of various speeds, and puts it into a new format. This new format has no stop or start bits and can be clocked out of the DSI using the input enable and data clocks of a synchronous data transmitter— such as the UDLT.

The chip has an on-board baud rate generator. By feeding a 4.096 MHz clock to the DSI, it will generate a 16x clock to sample the incoming asynchronous data. The data rates that can be programmed are 300, 1200, 2400, 4800, 9600, 19.2 k, and 38.4 k baud. Other asynchronous data rates may be fed to the DSI by supplying an (async data rate) × 16 clock.

In order to maintain synchronization when input data is unable to fill the output channel, the DSI will supplement its output channel with flag patterns. On the receiving side of the data transmission, another DSI will return the data to its original start/stop format.

The RS-232-C Driver/Receiver

The MC145406 has three drivers and three receivers on one CMOS integrated circuit. This device meets all of the EIA RS-232-C specifications. In general, it replaces the 1488/1489. The chip consumes less than 15 mW, which is critical when designing a line-powered digital telephone. A slew-rate limiting circuit is integrated into the chip, which removes the need for external slew-rate limiting capacitors.

SYSTEM II: VOICE/DATA WITH 2B + 2D DATA RATES

Figure 4 shows a more sophisticated terminal. This terminal supports full ISDN 2B + D data rates, as well as an additional D channel. In this case all of the signalling is handled by a microprocessor. One 64 kbps B channel can be used to transmit voice, while the other B channel can be used for transmitting high speed data. In addition, one 16 kbps D channel can be used for transmitting signalling information, while the other one can be used to transmit more specialized functions or additional data.

2B + 2D VOICE/DATA TERMINAL

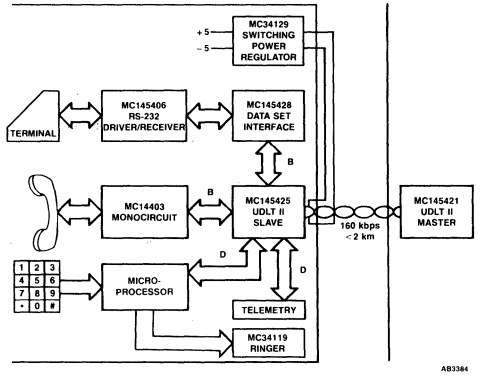


Figure 4

The interface between the data source and the ISDN UDLT, MC145421/MC145425, can be one of various types of data formatters. It could be a DSI handling up to 38.4 kbps, using the internal clock or a faster rate with an external clock. Data could also enter the ISDN UDLT II through an HDLC controller chip, or a clear channel configuration could be used.

This chip will transmit on two wires up to 2 kilometers, with the addition of a passive filter to compensate for the increased attenuation of the higher frequency spectrum.

The ISDN UDLT II—2B + 2D

The ISDN UDLT II, MC145421/MC145425, is very similar to the UDLT. However, instead of 80 kbps, the ISDN UDLT II sends 160 kbps. Also, a 512 kHz burst rate is used, instead of a 256 kHz rate. The data is formatted into four channels: two 64 kbps and two 16 kbps. Both of the 64 kbps channels are clocked out of the Tx pin under the direction of the TDC/RDC, TE1, and TE2 pins. Both of the 64 kbps channels are clocked into the Rx pin, and similarly their input is separately controlled by the RE1 and RE2 pins. The 16 kbps channels are input on the D1I and the D2I pins under control of the DCLK, and they are output on the D1O and D2O pins. Although the ISDN UDLT II does not transmit triangular bursts like the UDLT does, it will drive a twisted pair without external drivers. It also contains the on-board threshold-adjust circuitry. The ISDN UDLT II is being introduced today.

SYSTEM III: ISDN TERMINAL WITH LAP-D

The terminal in Figure 5 uses the "S/T" transceiver, MC145474, for data communication. This four wire transceiver can transmit 192 kbps up to 1 km on one pair of wires, and receives 192 kbps on an additional pair of wires. Besides having a four wire interface, the "S/T" transceiver's transmission method differs from the UDLT's in that alternate mark inversion (AMI) is used instead of MDPSK.

Of the 192 kbps, 144 kbps are used for the two B channels and one D channel. The additional 48 kbps provide framing, DC balance, D channel echoing, activation, and two other bits whose function will be defined in future definitions. Through the transceiver, a codec/filter

2B + D VOICE/DATA TERMINAL

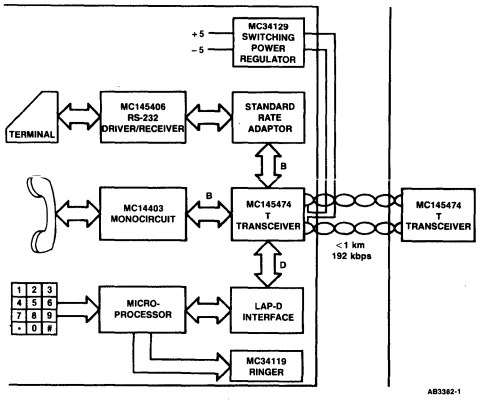


Figure 5

sends digitized voice; signalling information is sent through a LAP-D controller, packetized data can also be sent through the LAP-D controller, and high speed data can be sent through the other 64 kbps B channel. Although the chip offers point-to-point communication, the S/T transceiver is also capable of point-to-multipoint operation—if shorter loop lengths (150 m to 500 m) are acceptable.

CONCLUSION

Motorola's wide variety of integrated circuits offer flexibility to the design engineer. If low-cost voice/data communication is the top priority, the UDLT/DSI system provides a lot of functionality for a minimal cost. If higher data rates are needed, the ISDN UDLT is a solution to consider. And of course, Motorola plans to introduce an S/T transceiver chip and a LAP-D controller chip to provide the extensive features ISDN has to offer.

A VARIETY OF USES FOR THE MC34012 AND MC34017 TONE RINGERS

Prepared by
Dennis Morgan

INTRODUCTION

The MC34012 and MC34017 electronic tone ringers were developed to replace the bulky electromechanical bell assembly of a telephone, while providing the same basic function. When used in conjunction with a piezo ceramic transducer, these circuits will output a warbling sound in response to the applied ringing voltage. With some imagination, however, the circuits can be used in a variety of ways, including non-telephone applications, — wherever an alerting sound or indication is required. Applications include appliance buzzers, burglar alarms, safety alerting functions, special sound effects, visual ringing indicators, and others. The circuits in this application note show how a variety of effects can be obtained.

HOW THE MC34012 WORKS

A block diagram is shown in Figure 1. An AC voltage is applied to the input terminals, and the current is rectified by the full wave bridge. The six series diodes provide the high impedance required by telephone systems at low input voltages, and are therefore not significant where the use does not involve a telephone. A small portion of the I_S current (I_a) flows through D_a and R_a setting the inverting input of the comparator at 1.5 volts below R_S (pin 6). The majority of the input current, however, flows through R3, and the waveform across it is filtered by C3 and the internal 50 k resistor before being applied to the non-inverting input of the comparator. When the input voltage is increased sufficiently so that the current through R3 causes the voltage at the non-inverting input to be more than 1.5 volts below R_S, the comparator's output changes to a low state, allowing the oscillator's signal to reach the piezo transducer. Additionally the value of I_a is reduced by 20% in order to provide hysteresis to the comparator.

The 22 volts zener diode provides regulation for the internal circuitry, and C4 filters noise and ripple from this voltage. The input current must be at least 0.5 mA for the regulation and bias circuits to function properly.

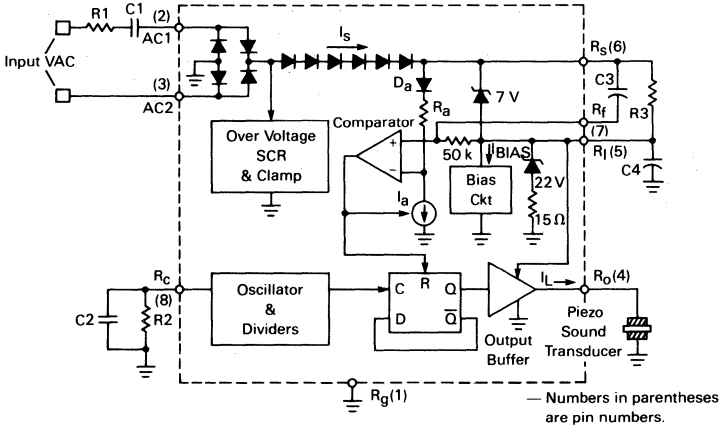


FIGURE 1 — MC34012 Block Diagram

The oscillator is a relaxation type, with the frequency determined by the values of R2 and C2. The base frequency (f = (0.671/R2C2) + 200 Hz) is divided down to produce two output frequencies (f/4 and f/5) which are outputted alternately at a warble rate determined by the base frequency, and the specific tone ringer model used. The MC34012-1 produces a warble rate of f/320, the MC34012-2 produces a warble rate of f/640, and the MC34012-3 produces a warble rate of f/160. The base frequency (f) should be selected to be between 1500 Hz and 10 kHz.

The output buffer is a totem-pole configuration with a 25 mA source-sink capability, and is intended to drive a piezo ceramic transducer. The output waveform is a 20 V p-p square wave.

HOW THE MC34017 WORKS

A block diagram is shown in Figure 2. The external components are labeled the same as in Figure 1. Operation is very similar to the MC34012 with the following differences:

a) The output to the piezo transducer is a push-pull configuration, rather than single ended, providing 40 Volts p-p.

b) The comparator's inputs are referenced to ground rather than to the supply voltage. V_r is 1.2 volts when the comparator's output is off (low), and 0.9 volts when the output is on.

c) The configuration consisting of the comparator, R3, and C3 sense the incoming current to determine the turn-on and turn-off trip points. When the voltage at R_S exceeds 1.2 volts, the comparator changes state to turn on the output.

SAMPLE CIRCUITS

The circuits of Figures 3 & 4 provide ON-DELAY, i.e., after applying voltage to the input terminals, sound is not produced until a delay period has elapsed. The output sound is continuous after that. The delay is primarily determined by C3 in the Figures, although R3 and R1 also affect the timing. The circuit may be controlled by turning on and off the voltage to the input terminals, or by leaving the input voltage applied continuously, and using a normally closed switch across C3 (open switch to start timing). Power consumption is typically less than 3/4 watt. Applications include time out circits for burglar alarms, dark room equipment, and others.

The circuits of Figures 5 and 6 provide OFF-DELAY, i.e., sound is produced immediately upon applying an input voltage, but then turns itself off after a delay. The delay time is determined by C_t. The circuits (as shown) have a long reset time (time for C_t to discharge after removing the input voltage) and so the user may want to consider providing a quick discharge path for C_t whenever the input voltage is removed (such as an extra set of contacts on the on-off switch). The particular application will determine the need for this. Applications include warning buzzers in washing machines, microwave ovens, alarm clocks, and other appliances.

The circuits of Figures 7 and 8 cause the sound output to be cycled on and off at a rate determined by C_t. The duty cycle can be varied by changing R_d. The LM393A dual comparator (configured as an oscillator) needs only 1 mA of power supply current, and so it is powered directly from the tone ringer's R_I pin. Several cycle times are listed in the Figures, and can be used to indicate different conditions, such as "WARNING" (slow cycle), and "EMERGENCY" (fast cycle). Applications include appliances, alarm clocks, emergency indicators on hot water heaters (overtemperature) and furnaces, smoke detectors, and any place where an attention getting sound is required.

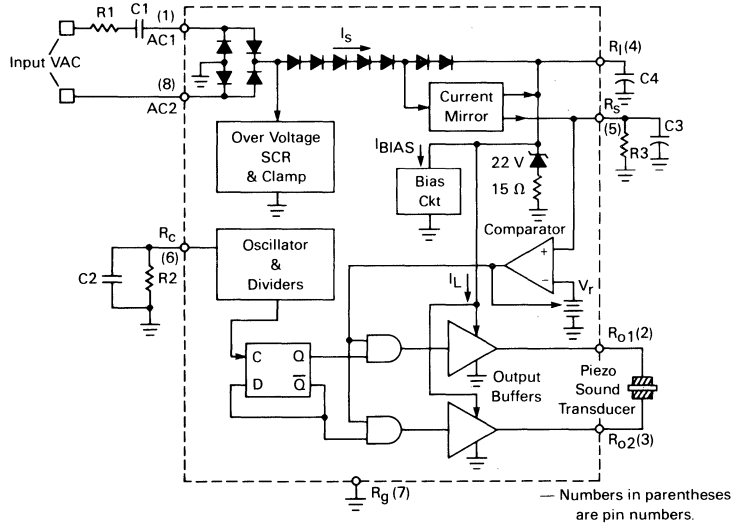
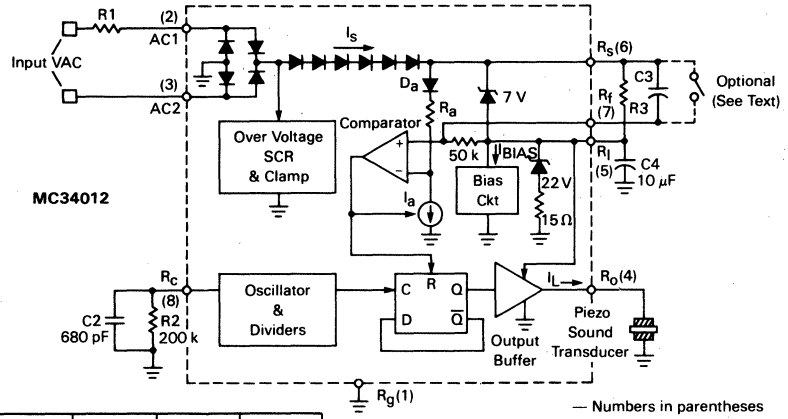
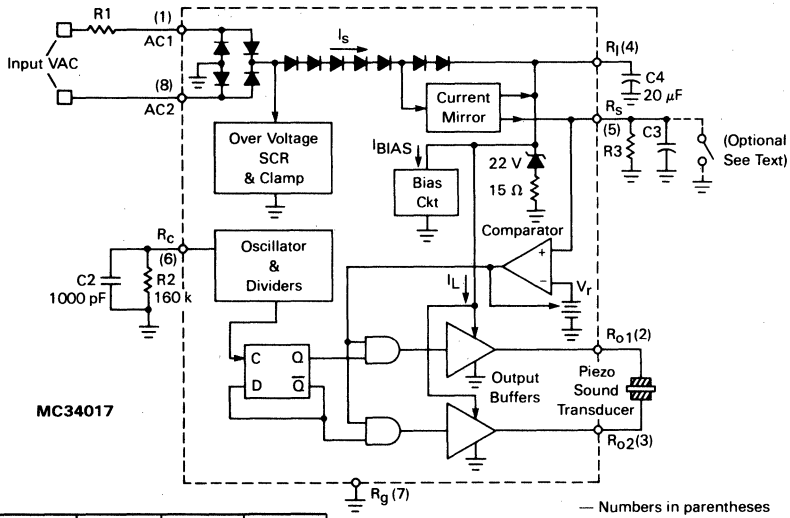


FIGURE 2 — MC34017 Block Diagram



Input VAC	R1	R3	C3	On Delay
24	100	1600	100 μF	30 Sec
120	16 k	750	1000 μF	30 Sec
120	16 k	750	100 μF	10 Sec

FIGURE 3 — On Delay Timer Using MC34012



Input VAC	R1	R3	C3	On Delay
24	1.0 k	15 k	500 μF	15 Sec
24	1.0 k	15 k	2200 μF	75 Sec
120	33 k	15 k	500 μF	8 Sec
120	33 k	15 k	2200 μF	40 Sec

FIGURE 4 — On Delay Timer Using MC34017

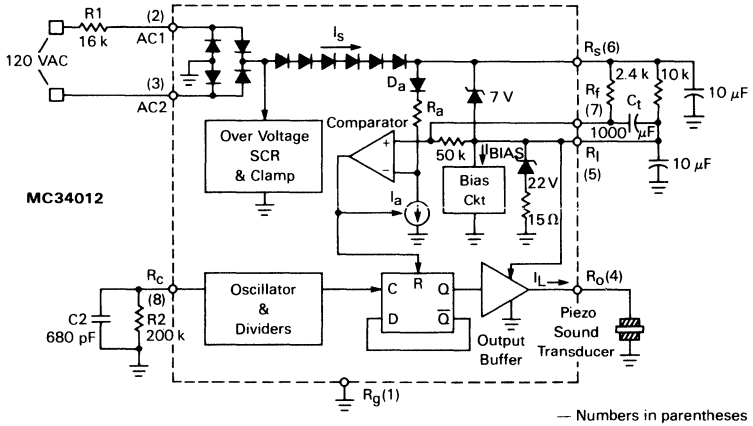
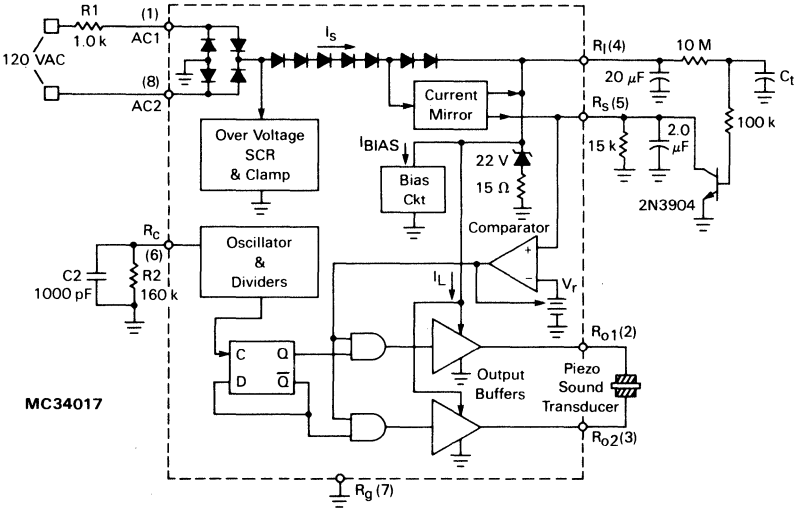
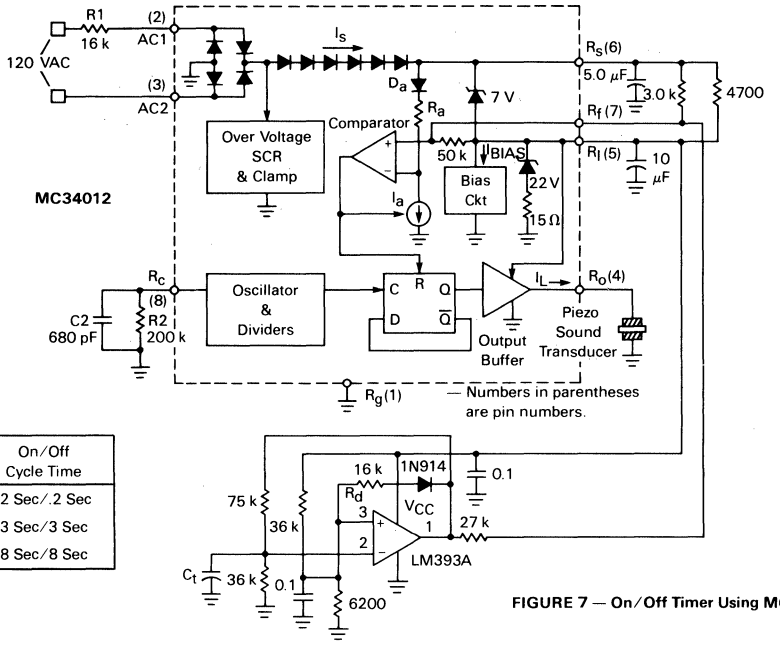


FIGURE 5 — Off Delay Timer Using MC34012



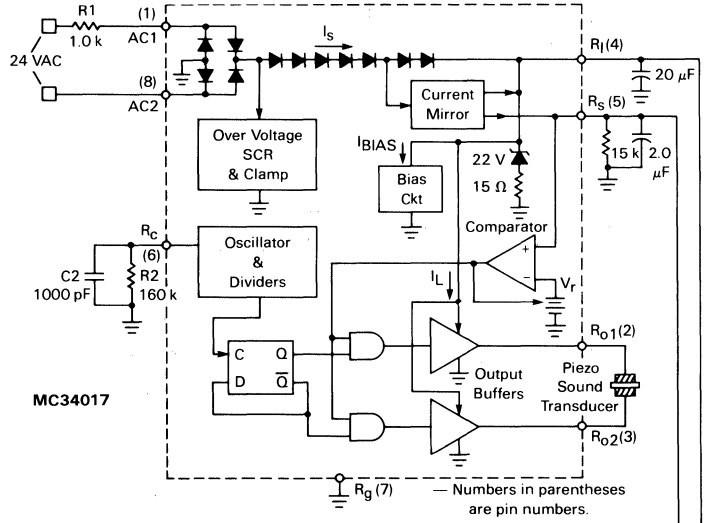
C_t	Off Delay
20 μF	17 Sec
10 μF	7 Sec
5.0 μF	4 Sec

FIGURE 6 — Off Delay Timer Using MC34017



C_t	On/Off Cycle Time
100 μF	.2 Sec/.2 Sec
500 μF	3 Sec/3 Sec
1000 μF	8 Sec/8 Sec

FIGURE 7 — On/Off Timer Using MC34012



C_t	On/Off Cycle Time
2.0 μF	.2 Sec/.2 Sec
20 μF	1.5 Sec/1.5 Sec
100 μF	2.5 Sec/5 Sec

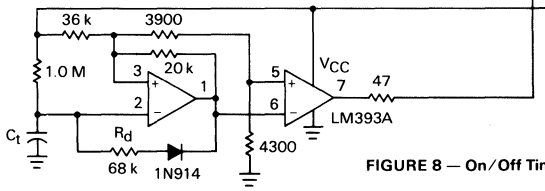


FIGURE 8 — On/Off Timer Using MC34017

The circuits of Figures 9 and 10 provide a special effects sound by varying the frequency of the base oscillator. The 2N3904 transistor is slowly turned on (as C_S charges up) thus varying the equivalent resistance at the R_C pin. This causes the frequency of the base oscillator to vary from low to high over a period of several seconds. C_S determines the rate at which the audio frequency is swept, and C_t determines how often the sweep cycle is repeated. The sound effects produced by this circuit are similar to those heard in many video games (home and arcade type), and in children's games and toys with sound effects. The two sweep circuits are different as they produce different effects. The circuit of Figure 9 uses feedback (via the 51 k resistor and the two portions of C_S) to generate a different linearity sweep curve than the simpler circuit of Figure 10. Either circuit can be used with the MC34012 or the MC34017 by making appropriate connections at R_I and R_C.

The circuits of Figure 11 & 12 are Ring Detector Circuits. Designed for use on the telephone line, they provide an output voltage level to indicate the presence of a ringing signal. (The 1.0 μF capacitor at terminal AC1 is necessary to meet FCC impedance requirements.) The output, at V_{out}, is high (+12 V) as long as an AC voltage is present on the Tip and Ring terminals. The optocoupler provides isolation from the circuit to be controlled, since telephone lines cannot be referenced to earth ground. The 1.0 k and 100 k resistors, and the 0.1 μF capacitor, filter the square wave output of the integrated circuit to provide a steady voltage at V_{out}. The output can be used to turn on a light, activate an answering machine, alert a computer that data is to be sent to it, and for many other uses. The circuit shown is not limited to telephones, however. By changing the value of R1 to 15 kohms for 120 VAC, or to 100 ohms for 24 VAC and deleting the 1.0 μF capacitor (as in the previous examples), the output will indicate the presence of an input voltage while providing isolation. Isolation can be used to prevent unwanted ground loops, or for safety reasons such as to meet UL requirements (the 4N25A and 4N35 optocouplers are UL listed).

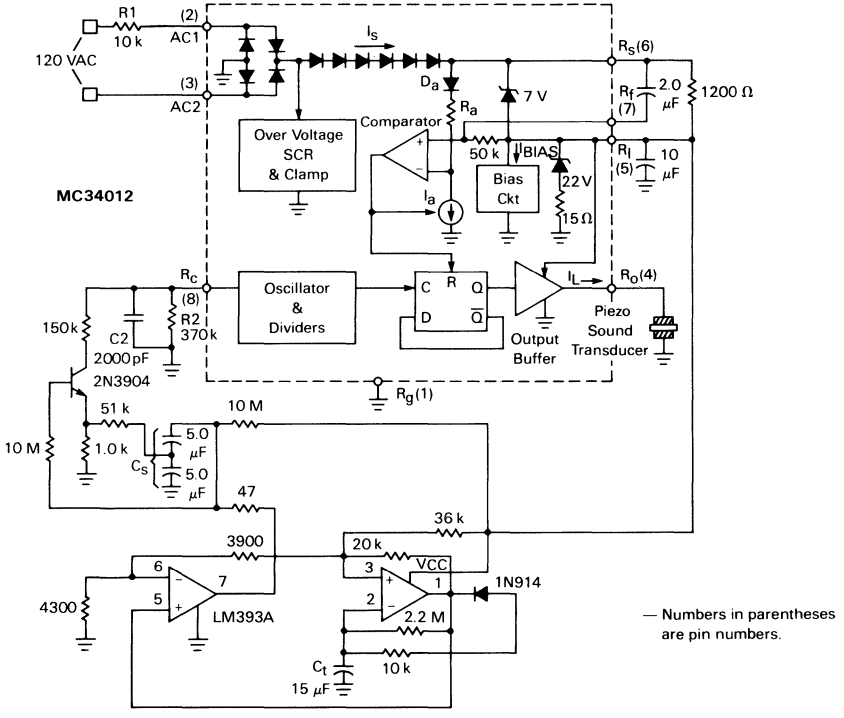


FIGURE 9 — Audio Frequency Sweeper Using MC34012

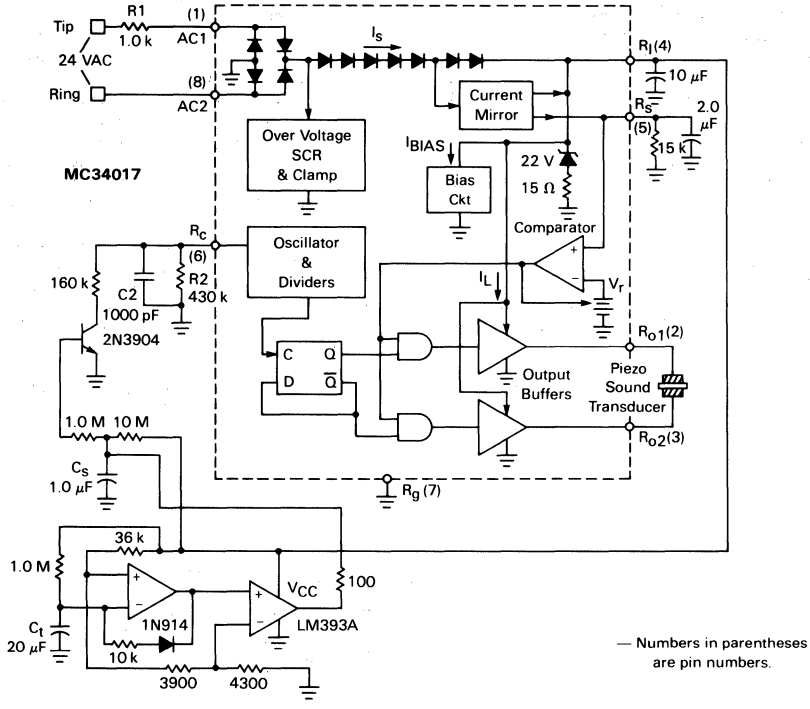


FIGURE 10 — Audio Frequency Sweeper Using MC34017

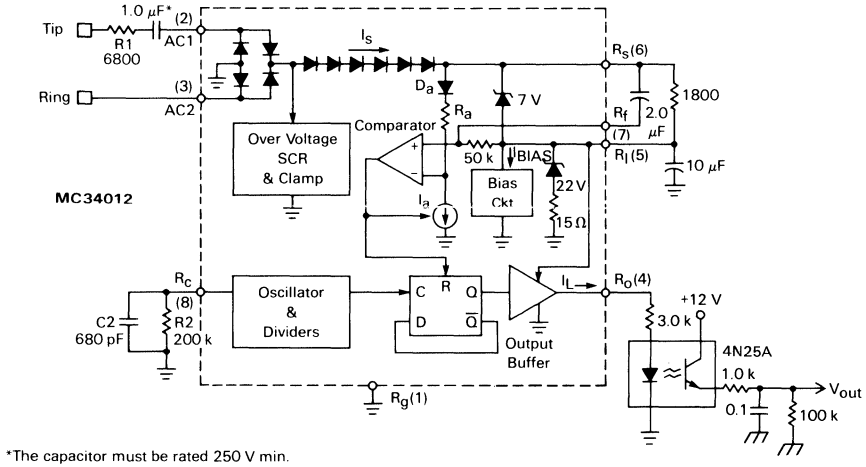


FIGURE 11 — Ring Detector Circuit Using MC34012

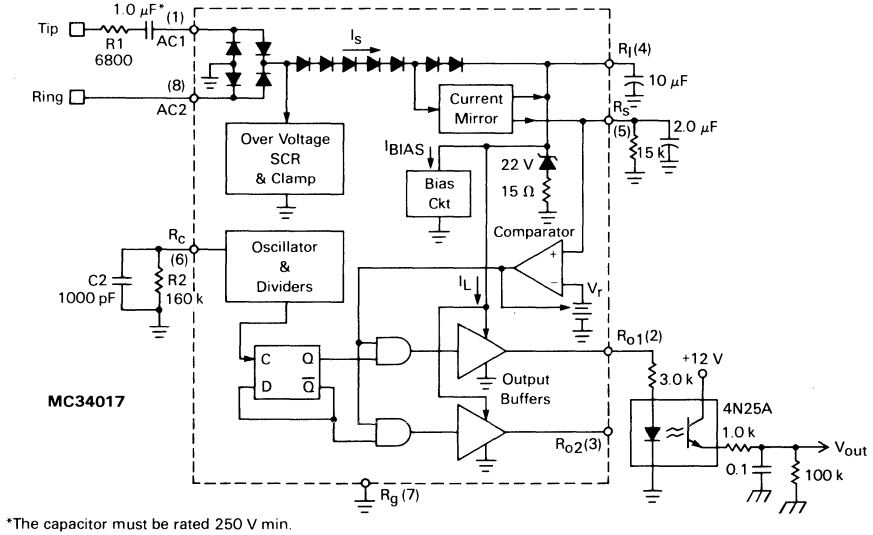


FIGURE 12 — Ring Detector Circuit Using MC34017

The circuit of Figure 13 will count the number of times the ringing voltage is sent to the telephone, and will not allow the piezo transducer to sound until a certain number of ring cycles (selected by S1) have passed. The circuit values are based on a typical ringing cadence of 2 seconds on, 4 seconds off. The outputs of the MC14017 counter (Q1-Q9) become active sequentially with each cycle of the ringing signal. When the selected output becomes active, the MC14013 flip-flop changes state, and the piezo transducer sounds. The Q output of the MC14013 can be used to activate other circuitry such as an answering machine. After the ringing signal stops due to answering the phone, or the caller hangs up, the counters and the flip-flop are reset. Note the two separate grounds - the telephone line must be kept separate from the circuit ground.

As a final note, many applications will be enhanced by the addition of a volume control. Simply connect a 10 k potentiometer in series with the piezo sound transducer. The sound output level will then be controllable over a substantial range. Additionally, if the particular transducer being used has a high frequency shrill in its sound, the series resistance can remove the high frequencies, and produce a more pleasant sound.

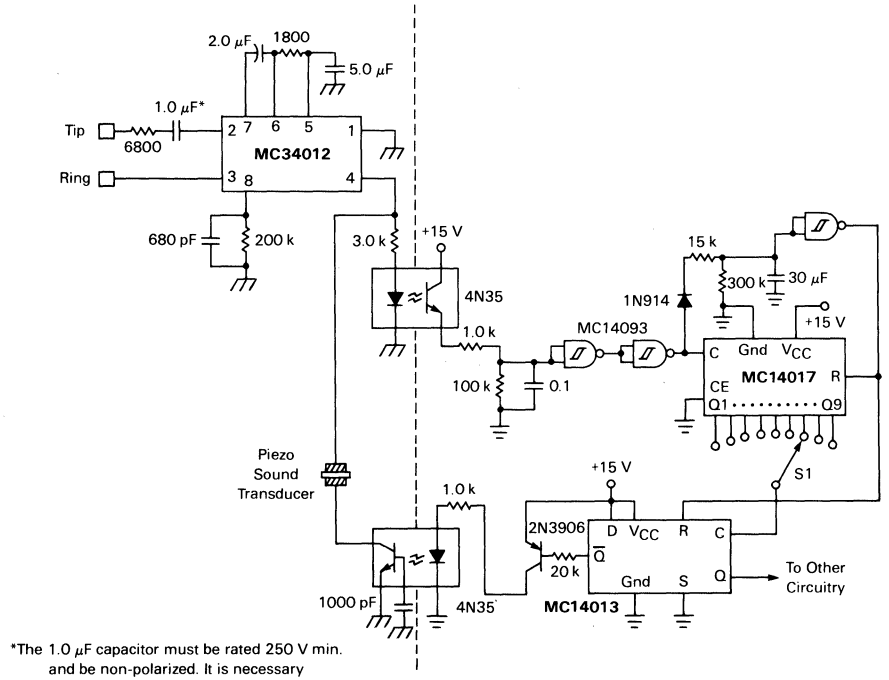


FIGURE 13 — Ring Signal Counter

A TELEPHONE RINGER WHICH COMPLIES WITH FCC AND EIA IMPEDANCE STANDARDS

Prepared by
Dennis Morgan

INTRODUCTION

The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. This application note discusses how the IC's operate, the specific operational requirements to be met, and how they are met. Only "on-hook" requirements are discussed since off-hook operation is not applicable.

ON HOOK IMPEDANCE REQUIREMENTS

The FCC Rules & Regulations, Part 68, define the on-hook impedance (while ringing) requirements, as well as the ringing voltages and frequencies. EIA Standard RS-470 expands upon the requirements to include minimum impedance during the non-ringing (quiescent) state. The FCC requirements were promulgated so that any newly designed equipment, meant for connection to the Tip and Ring lines, be compatible with the already existing Bell Telephone network and central office equipment. The measured impedance, in all cases, is defined as the quotient of the applied rms ac voltage divided by the true rms measured current.

For the quiescent state, EIA Standard RS-470 provides the minimum impedance requirements at low voltages ($<10\ V_{rms}$) in the 5-3200 Hz range to provide for the loading presented by an on-hook extension phone's ringer circuit to the dialing and speech signals coming from a parallel off-hook phone. Table 1 and Figures 1 & 2 indicate the minimum values. The dc resistance limits of Table 1 keep the telephone from consuming significant power when idle since most phones are on-hook the majority of the time. The lower frequency range of the ac resistance limits includes all of the standard ringing frequencies, and so has a higher applied voltage limit than the upper frequency range, which covers the speech and DTMF signals.

In the ringing state, the limitations for ringer impedance are based on the REN (Ringer Equivalence Number), which is an indication of the power consumed by the ringer circuit during ringing. The FCC regulations state that the total REN for any individual telephone line cannot exceed 5.0, where the total REN is the sum of the REN of each device connected to the line (answering machine, protection devices, as well as each telephone). The specific impedance values listed in the FCC Regulations (Section 68.312, paragraphs b & c, and Table 1) correspond to a REN of 5.0, and are therefore the minimum allowable system impedances. EIA Standard RS-470 provides the same information for the on-hook dc and ac resistance (while ringing), except that the listed values differ by a factor of 5 from those listed in the FCC Rules. The EIA information is, therefore, not a set of limits, but rather a definition of a 1.0 REN. (Originally the 1.0 REN was defined as the load presented by the electromechanical type ringer of a standard Bell Telephone Co. 2500 series telephone.)

TABLE 1

QUIESCENT STATE LIMITS
DC RESISTANCE (between Tip and Ring)
>50 Mohms for 0 - 100 VDC
>150 kohms for 100-200 VDC
AC RESISTANCE (between Tip and Ring)
For 5 Hz<f<200 Hz, 1-10 V_{rms}, see Figure 1
For 200 Hz<f<3200 Hz, 0-3 V_{rms}, see Figure 2
At 24 Hz, Z at 2.5 V_{rms} > 4 x Z at 10 V_{rms}

The specifications of Table 2 includes not only the ringing impedance guidelines of RS-470, but also the voltages and frequencies at which the ringer circuit MUST ring. When testing a circuit to the conditions of Table 2, the minimum measured impedance within each voltage and frequency range is divided into the impedance listed for that range. The largest number obtained over the full set of ranges for a ringing type is the REN for that circuit. In addition to the specifications of Table 2, RS-470 and the FCC Rules require that the ac ringing impedance of an individual device be less than 40 kohms, unless that requirement is already provided for by some other parallel device.

In addition to the above ac specifications, the dc requirements impose an upper limit of 0.6 dc mA when any of the Table 2 ringing signals are applied.

(NOTE: The type A ringers mentioned in Table 2 refer to the inherently frequency selective electro-mechanical type ringers used for decades in the typical single-line (non-party line) telephone. Type B ringer specifications cover a wider frequency range, and were developed with the advent of electronic ringers which are generally not frequency selective. Ringer types C through Q, listed in the FCC and EIA specifications, are selective to specific frequency ranges for the purpose of party line applications, and are not discussed here.)

TABLE 2

RINGING CHARACTERISTICS

Ringing Type	Frequency (Hz)	Voltage (V_{rms})	Bias (Vdc)	Impedance (kohms)
A	17	40-130	0-105	7
A, B	17	55	0-105	10
A	20	40-130	0-105	7
A	20	40	0-105	8
A	23	40-130	0-105	6
A	27-33	40-130	0-52.5	5
B	15.3-68	40-150	0-105	8

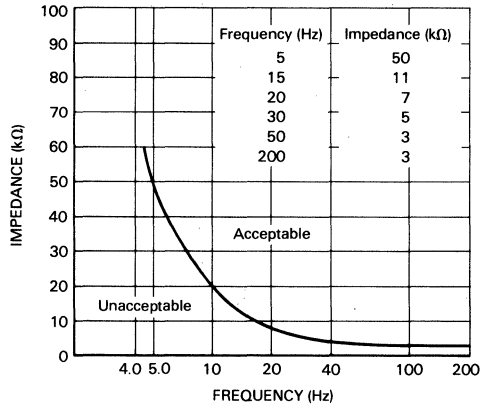


FIGURE 1 — Quiescent State Minimum Impedance (1-10 V_{rms}) (EIA Standard RS-470)

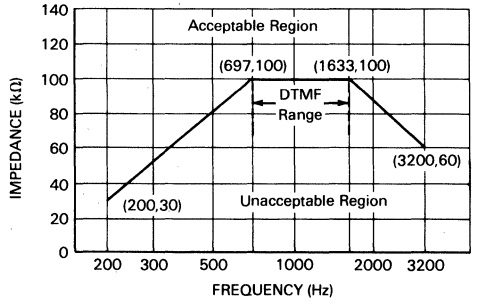


FIGURE 2 — Quiescent State Minimum Impedance (0-3 V_{rms}) (EIA Standard RS-470)

CIRCUIT DESCRIPTION - MC34012

A block diagram is shown in Figure 3 (R1-R3, C1-C4, and the piezo transducer are external). A ringing signal (From Table 2) is applied to the Tip and Ring terminals, and the current is rectifed by the full wave bridge. The string of six diodes following the bridge provide the high impedance required at low voltage (non-ringing) levels (see Figures 1 & 2). When the voltage across AC1-AC2 exceeds approximately 5.6 volts (8 diode drops) current will flow (several microamps), primarily through R3 and into the Bias Circuit block (I_a is relatively small). As the current reaches approximately 0.5 mA, the internal biasing becomes well established, and so further increases in voltage result in little increase in current. When the voltage at pin R_I reaches 22 volts, the zener diode conducts and the current increases rapidly with voltage.

The two inputs of the comparator are referenced to pin R_S (the output of the diodes), rather than to ground. The inverting input is kept at 1.5 volts below R_S by I_a, R_a, and D_a. The voltage at the non-inverting input depends on the current through R3. When the voltage at this input is more than 1.5 volts below R_S the output of the comparator changes state, allowing the oscillator's signals to reach the piezo transducer. On-Off hysteresis of the comparator is provided for in two ways: 1) the comparator's output (when low) reduces the value of I_a, thus reducing the voltage across D_a and R_a to 1.2 volts; and 2) The load current (I_L) passes through R3, increasing the voltage across it. When the current through R3 is reduced sufficiently to turn off the comparator, I_a is returned to the higher value, and the flip-flop is reset, turning off the output.

Capacitor C3 filters the waveform across R3 so that the comparator does not turn on & off with every cycle of the applied ringing signal. In effect, the comparator responds to the AVERAGE voltage across R3. C3 also filters out transient voltages and noise to prevent false ringing. C3 should be large enough (typically 1.0 μF) to reject dialing transients, as well as to ensure the comparator stays on at the lowest ringing voltage and frequency listed in Table 2 (40 V_{rms}, 15.3 Hz). Values larger than 3.0 μF will significantly affect the response time of the circuit.

C4 is a filter for the internal 22 volt supply. With a 5.0 μF capacitor, a ripple of about 3 volts p-p (at 15.3 Hz) results at the R_I pin, which shows up on the output pin. With a 2.0 μF capacitor, the ripple increases to 6 volts p-p, with a slight reduction in output sound level of the piezo transducer, since the output's average value is lowered. Values less than 2.0 μF are not recommended. Neither C3 nor C4 affect the impedance of the overall circuit during ringing.

The values of C3 and R3 determine the turn-on trip point of the circuit, while the turn-off trip point is determined by R3, C3, and the load (piezo transducer) since the load current (I_L) passes through R3. (The line input resistor and capacitor, R1 and C1, also affect the on-off trip points, and will be discussed later). 1800 ohms is the recommended value for R3. A higher value will lower the trip points, but will make the circuit more susceptible to noise. Additionally, if R3 is too large, it is possible the comparator may turn on the output before the internal circuitry is fully biased, resulting in erratic operation. R3 must therefore be selected to pass sufficient current to supply the bias current, AND some

through the 22 volt zener diode, BEFORE the comparator switches the output on. On the other hand, a lower value of R3 will increase the circuit's noise rejection, while raising the on-off trip voltages.

Components R2 and C2 set the base frequency of the oscillator, and have no effect on the on-off trip points, or circuit impedance. Refer to the data sheet for proper component values.

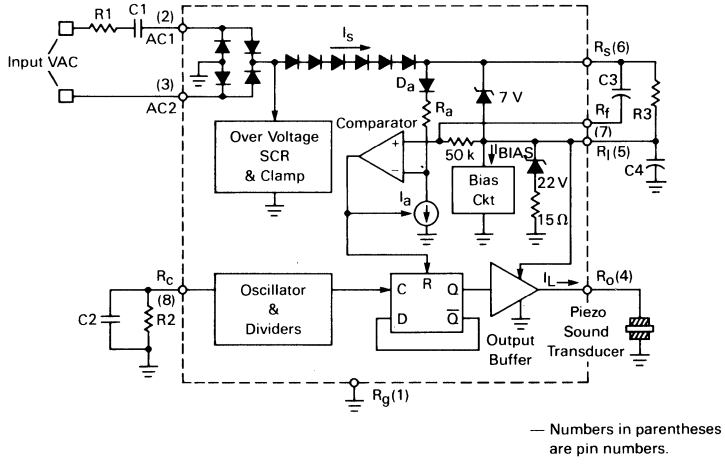


FIGURE 3 — MC34012 Block Diagram

CIRCUIT DESCRIPTION - MC34017

A block diagram is shown in Figure 4. The external components are labeled the same as in Figure 3. The following provides a functional comparison of the MC34017 with that of the MC34012:

- The output to the piezo transducer is a push-pull configuration, rather than single ended, providing 40 volts p-p.
- The comparator's inputs are referenced to ground rather than to the supply voltage. V_r is 1.2 volts when the comparator's output is off (low), and 0.9 volts when the output is on.
- The configuration consisting of the comparator, R3, and C3 sense the incoming current (I_S) to determine the turn-on and turn-off trip points. Since I_S contains the load current (I_L), the same hysteresis effect that exists in the MC34012 is provided for in this circuit.
- Five diodes are shown in series with the input bridge rather than six. The Current Mirror block provides an effective sixth diode, providing the same high impedance at low voltage as provided for by the MC34012.
- Typical values for R3 and C3 are 15 kohms and 2.2 μF, respectively.

MC34012/34017 IMPEDANCE CHARACTERISTICS

The circuit of Figure 5 was used to determine the dc characteristics, and the results are shown in Figure 6. The component values (R2, R3, C2-C4) are typical recommended values, and the 0.047 μF capacitor and 390 ohms resistor simulate a typical piezo transducer. The circuit is obviously very non-linear, resembling, in effect, a 29 volt zener diode in series with a 450 ohm resistor (for $V_{in} > 29$ volts).

QUIESCENT STATE IMPEDANCE

The very high dc impedance requirements, and the fairly high ac impedance requirements (particularly at the lowest frequencies) of Table 1, require the use of a capacitor in series with the input to the I_C. A series resistor is not practical because of the values involved. Figure 7 depicts the circuit configuration. The maximum capacitor value (for C1), which results in the circuit exceeding the EIA requirements, was experimentally determined. Figures 8 & 9 indicate the impedance curves of the resulting circuit. Figure 8 shows the results at 10 V_{rms} only since any lower input voltage results in a higher circuit impedance.

Typically, mylar, polycarbonate, and Teflon capacitors are best suited to meet the dc impedance requirements.

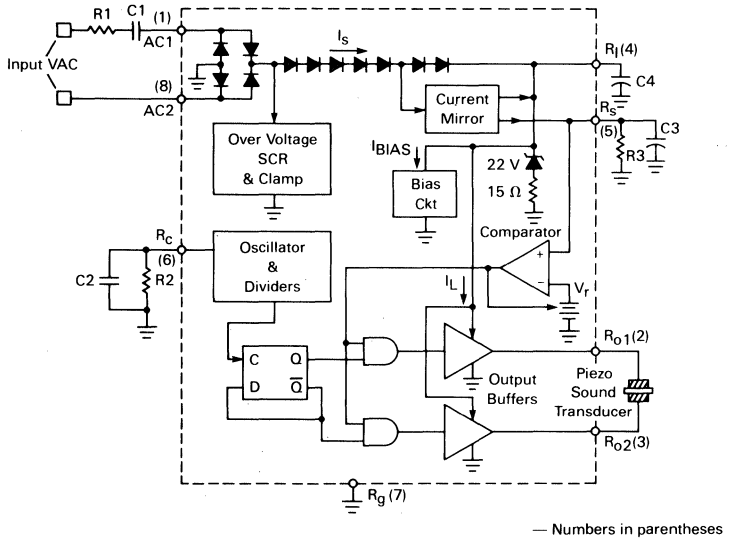


FIGURE 4 — MC34017 Block Diagram

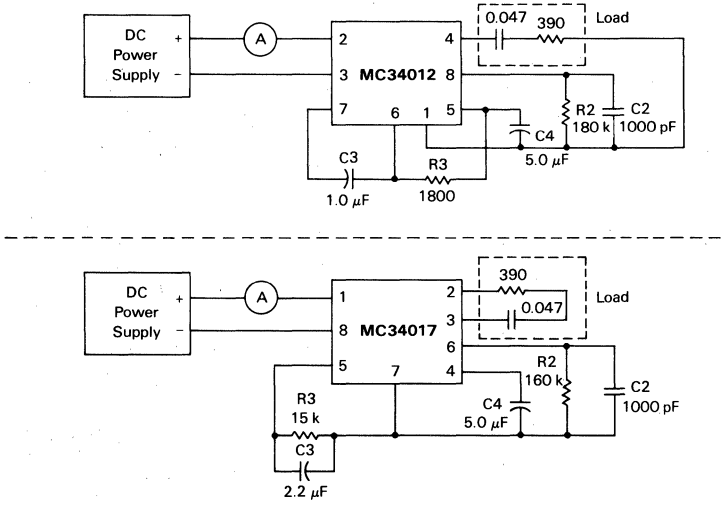


FIGURE 5 — DC Test Circuit

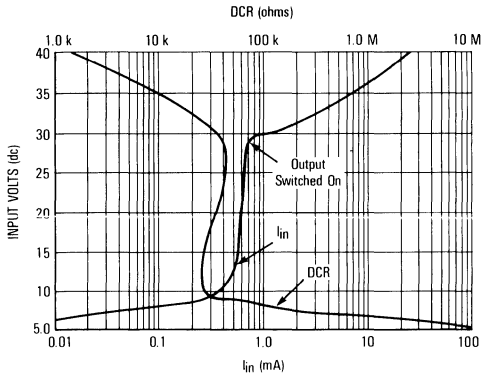


FIGURE 6 — DC Characteristics

RINGING STATE

Considering (temporarily) the impedance values of Table 2 as minimums in order to guarantee a REN of 1.0 or less, reasoning will indicate that the circuit of Figure 7 will not provide the necessary impedance since: 1) the impedance of the ringer I_C drops off quickly at the higher voltages (Figure 6); and 2) the impedance of the capacitor (C1) drops off at the higher frequencies. (The capacitor's impedance can be roughly estimated using $1/2\pi fC$, but this is a VERY rough estimate since the current through the capacitor is anything but sinusodial.) A series resistor (R1) is therefore added (Figure 10) to provide the additional impedance. The limits on the value of R1 are that it must be low enough to allow the circuit to operate (output on) at the lowest voltage AND frequency of Table 2, and yet high enough to provide sufficient impedance at the highest voltage AND frequency. Since an optimum value for R1 is difficult to calculate, different values were tested experimentally with the following results:

1) 7200 ohms is the maximum value which will allow the circuit to turn on at 40 V_{rms}, 15.3 Hz.

2) 7800 ohms is the maximum value which will allow the circuit to turn on at 40 V_{rms}, 17 Hz.

3) 2000 ohms is the minimum value which will result in a REN of 1.0 for a type A ringer.

4) 5500 ohms is the minimum value which will result in a REN of 1.0 for a type B ringer.

5) With R1 chosen within the above mentioned range of values, the highest measured circuit impedance was approximately 23 kohms, well below the maximum allowable of 40 kohms. Choosing a value of 6200 or 6800 ohms (2 watts) for R1 will then result in a circuit which is functional at all of the voltages and frequencies listed in Table 2, but also provides a REN of less than 1.0 for both type A and B ringers.

The allowable values for C1 are fairly narrow. Reducing C1 will increase the circuit impedance and lower the REN, but testing indicated that 0.6 μF is the lowest value which will allow the circuit to turn on at 40 V_{rms} and 17 Hz. It was previously determined (see Figure 8) that C1's value could not be much higher than 1.0 μF and still meet the quiescent state impedance requirements. The voltage rating for C1 must be at least 250 volts, and must be non-polarized.

The load (represented in Figure 10 by the 0.047 μF capacitor and the 390 ohm resistor) affects the overall circuit impedance when ringing since the load current must be supplied on the Tip and Ring lines, and so the actual sound transducer must be installed when making the impedance measurements of a production circuit.

Variations in performance over temperature (-20° C to +60° C) are minor, and generally do not present a problem in most applications. Variations in R1, C1, R3, and C3 will affect input impedance, and the on-off trip points, if they drift with temperature.

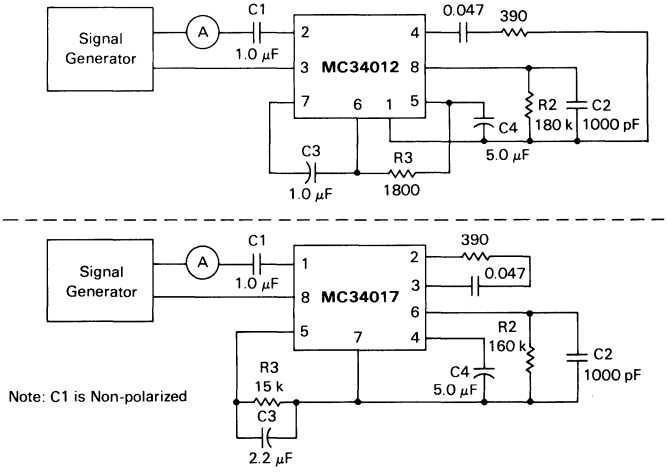


FIGURE 7

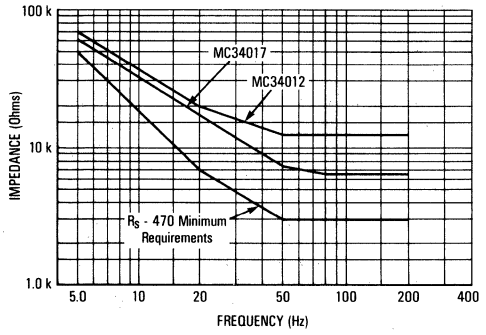


FIGURE 8 — AC Impedance at 10 V_{rms}

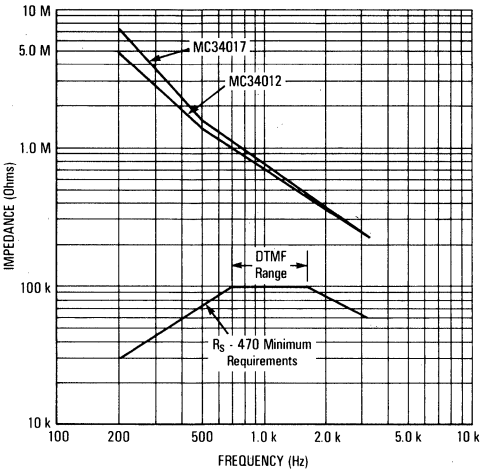
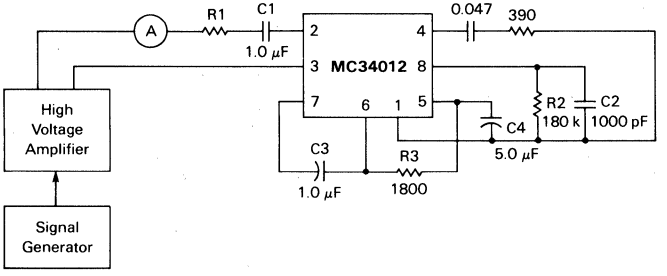


FIGURE 9 — AC Impedance at 3.0 V_{rms}



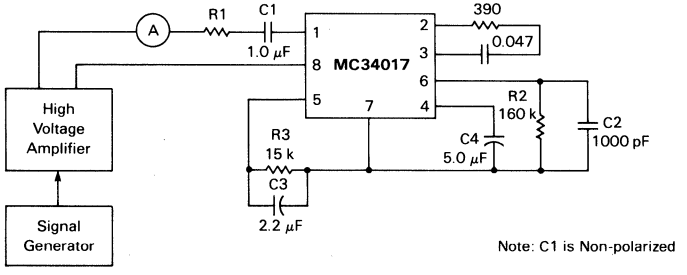


FIGURE 10 — Ringing State Test Circuits

SUMMARY

The MC34012 and MC34017 provide a simple and inexpensive means to construct a telephone ringer which meets the FCC and EIA impedance and operational requirements. The output frequencies to the sound transducer are selectable over a 6.5:1 range, and three different warble rates are available by appropriate suffix choice (-1, -2, or -3). The circuits are designed for use with piezo sound transducers, rather than a bulky speaker/transformer arrangement. Only 3 resistors and 4 capacitors (all standard values) are required to make the circuit operational.

A REN of 1.0 is easily obtained for a type B ringer, as is a REN of 0.5 for a type A ringer.

ACKNOWLEDGEMENT

Figures 1 and 2 were taken from RS Standard 470 with permission of the Electronic Industries Association, 2001 Eye St. NW, Washington, DC 20006. (202-457-4900).

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Federal Communications Commission Rules and Regulations, Part 68 "Connection of Terminal Equipment to the Telephone Network", October 1982.

MC34012 Data Sheet, Motorola Inc., 1983.

MC34017 Data Sheet, Motorola Inc., 1984.

DEFINITION OF TERMS

RINGER CIRCUIT -
The bell, or other alerting device (circuit) in a telephone.

ON-HOOK -
The circuit condition of a telephone when it is not in use (handset is on-hook).

OFF-HOOK -
The circuit condition of a telephone when it is in use (handset is off-hook).

DTMF -
Dual Tone MultiFrequency - The dialing system where (somewhat musical) tones are produced by a pushbutton telephone.

REN -
Ringer Equivalence Number - see text.

TIP, RING -
The connection points whereby an individual telephone is connected to a switching network. Ring is traditionally negative with respect to Tip.

TURN-ON TRIP POINT -
The voltage (at Tip & Ring) at which the ringer circuit switches on.

TURN-OFF TRIP POINT -
The voltage (at Tip & Ring) at which the ringer circuit switches off.

AN957

Interfacing The Speakerphone To The MC34010/11/13 Speech Networks

Prepared by
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INTRODUCTION

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the newer "A" version of each of those. The interface is applicable to existing designs, as well as to new designs.

FUNCTIONAL REQUIREMENTS

Figure 1 shows the basic MC34010 telephone circuit as described in the data sheet. It is a completely functional telephone meant for use with a handset, and provides the additional function of a microprocessor interface for the DTMF dialing function. The MC34011 does not have the microprocessor interface, but otherwise is identical, including the pin numbers. The MC34013 has the same speech network, dialer, and line interface circuit as the MC34010, but does not have the microprocessor interface or the tone ringer. Except for a minor difference between the speech networks of the "A" version parts and the "non-A" parts, the interface to the speakerphone circuit is virtually the same for all 6 parts.

Figure 2 shows the basic MC34018 speakerphone circuit as described in the data sheet. It is NOT a complete telephone, but provides only the speakerphone functions. It requires a speech network, such as the MC34010, to transfer the speech signals to/from the Tip & Ring lines, and to provide the required supply voltage. The four external connections — transmit output, receive input, dc line input, and chip select — are the points which must be interfaced to the speech network.

In the following text, only the MC34010 interface will be described. The interface to the other parts is the same except where noted.

When combining a speech network which operates a handset, with a speakerphone circuit, certain changes are required in the circuit operation when switching between the handset mode and the speakerphone mode, and additionally when the dialing mode is in effect. The four modes to be considered are: 1) using the handset for speech, 2) using the speakerphone for speech, 3) dialing in the handset mode, and 4) dialing in the speakerphone mode. The requirements are summarized in the following table:

Mode	MC34018	Vlr	Handset Mike	Speaker-phone Mike
Handset-Speech	Unpowered	Low	Live	N/A
Spkrphone Speech	Powered	High	Dead	Live
Handset-Dialing	Unpowered	Low	Dead	N/A
Spkrphone Dialing	Powered	High	Dead	Dead

Since the entire circuit is to be powered by the phone line, the speakerphone circuit is powered up only when it is to be used since it uses a portion of the loop current, (a significant portion on long loops). The MC34010, however, must be powered all the time since it is the interface to the phone line. The Vlr voltage mentioned in the table is the voltage across the resistor at the LR pin of the MC34010, which sets the dc characteristics of the circuit. By increasing that resistor, the dc supply voltage (and the voltage at Tip & Ring) will be increased in the speakerphone modes, where additional power is required.

The handset mike is to be functional only in the handset-speech mode. If it were functional in the speakerphone-speech mode, system oscillations and/or additional echoes could occur. Disabling the microphone is accomplished by activating the MM (Mike Mute) pin on the MC34010. On the MC34010A, activating the MM pin results in disabling the transmit amplifier, so in that case, a transistor is added to the microphone circuit as the means to disable it. In both dialing modes, muting is automatic whenever the dialer is activated, so the DTMF tones are not distorted by sounds entering the microphone.

The speakerphone mike is listed as N/A in the handset modes since the MC34018 circuit is unpowered, effectively disabling the mike. In the speakerphone dialing mode it must be non-functional for the same reason as mentioned above. That is accomplished by the fact that the MC34010 (and MC34010A) transmit amplifier is inoperative when its DTMF dialer is activated.

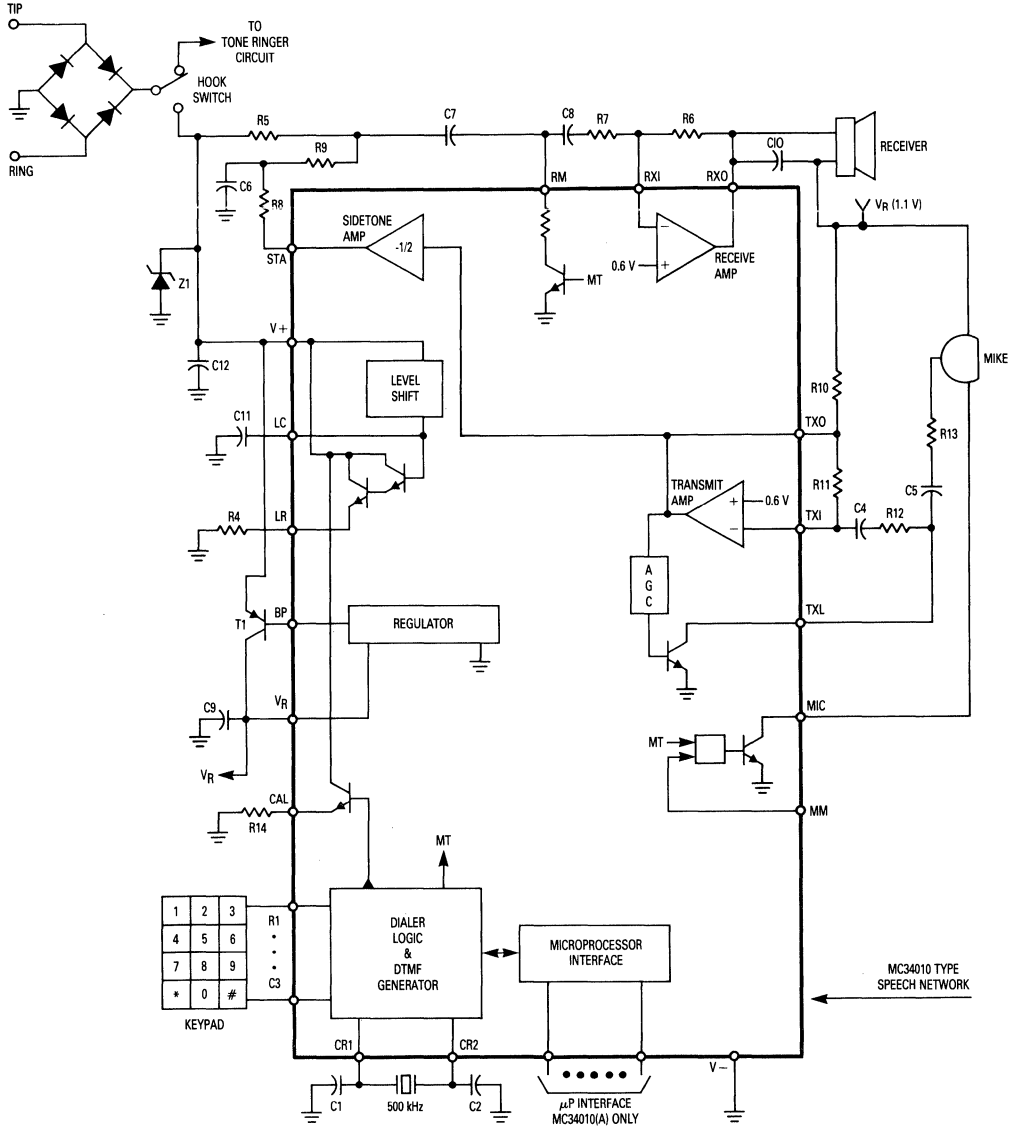


Figure 1. Basic MC34010 Type Telephone

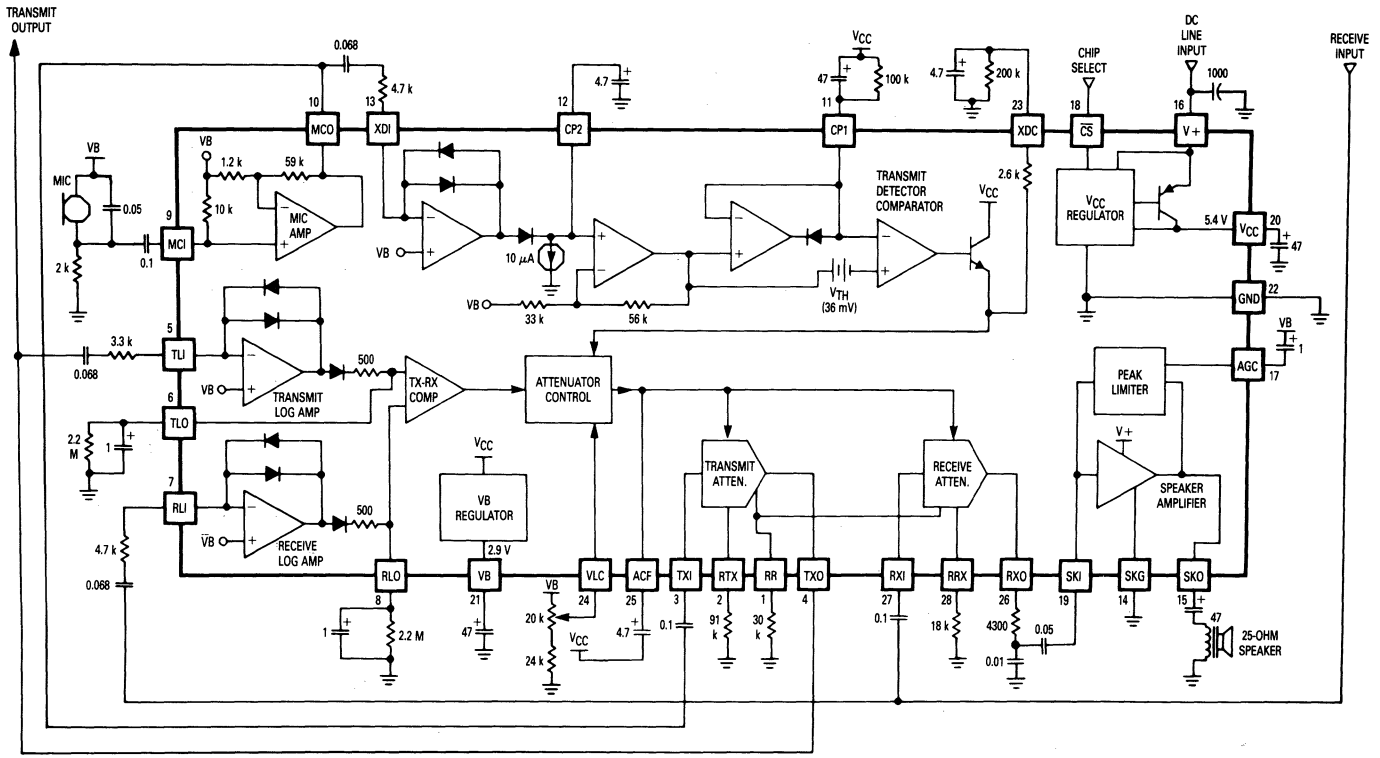


Figure 2. MC34018 Speakerphone Circuit

CIRCUIT DESCRIPTION

SWITCHING ARRANGEMENT

Figure 3 indicates the switching arrangement for going off-hook in either the handset mode or speakerphone mode, and for switching between them. S1 (a two pole switch) is the normal hook switch activated by lifting the handset. S2 (a two pole switch) is a manually operated switch which activates the speakerphone.

Whenever the handset is off-hook, and S2 is in the off position, power from Tip & Ring is applied to the MC34010 through the diode bridge and S1A. S1B's position is of no consequence in this mode. Should S2 be switched on while the handset is off-hook, power is then applied to the speakerphone IC through S2B. However, since S1B is open, the MC34018's $\overline{CS}$ pin (Chip Select) is taken high through R33, disabling the IC.

Anytime the handset is on-hook, and S2 is on (both poles closed), power is applied to both the MC34010 and the MC34018. Since S1B is closed, $\overline{CS}$ is taken low, enabling the speakerphone circuit. Anytime the handset is taken off-hook the circuit will revert back to the handset mode.

The 1.0 Henry inductor isolates the speech signals at Tip & Ring from the V+ pin of the MC34018, preventing an oscillatory loop from forming. The diode bridge, B2, is added for the tone ringer circuit of the MC34010(A), or MC34011(A), to keep the switches S1 and S2 from requiring 3 poles each.

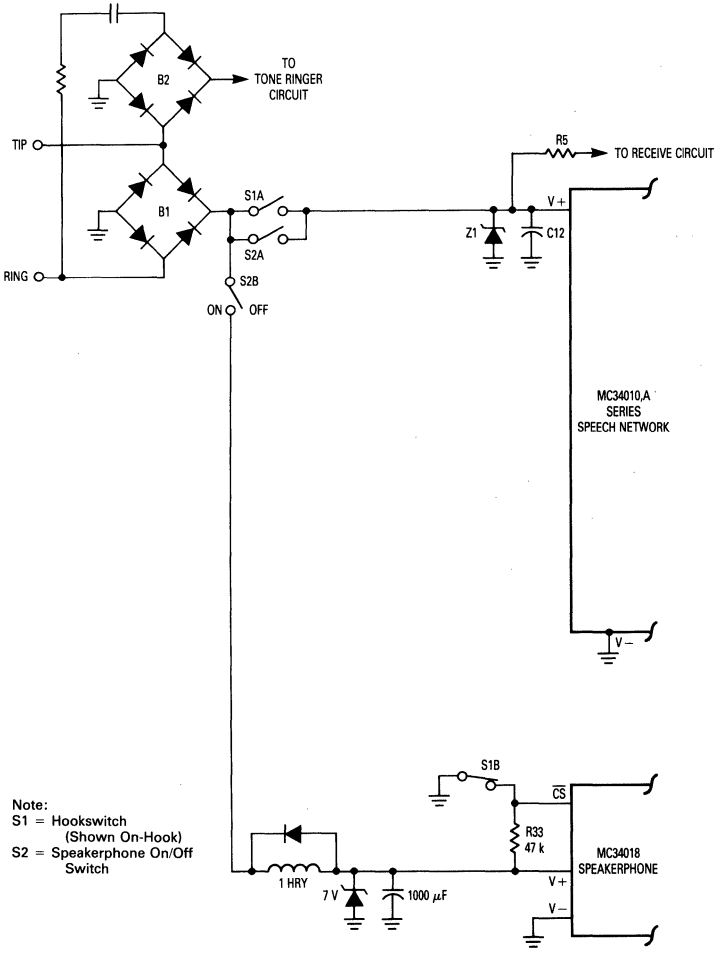


Figure 3. Handset/Speakerphone Power Switching

Vlr SHIFT

Since a speakerphone requires more power than a handset, it is necessary, particularly on long loops, to increase the Tip-Ring voltage. Since on long loops the Tip & Ring lines act more like a current source than a voltage source, increasing the voltage does not significantly decrease the available loop current. In order to shift the dc voltage, the additional components shown in Figure 4 are used. The voltage at the output of the diode bridge (B1) is equal to the voltage across the LR resistor, plus an internal level shift of approximately 3 volts between V+ and LR.

In the handset mode, the transistor T2 is on, and the equivalent LR resistance is approximately 80 ohms. The majority of the loop current (all except about 10 mA) flows through the LR resistor. In the speakerphone mode, the transistor is off, and the dc voltage is determined by the 390 ohm resistor, the internal 3 volt level shift, the resistance of the 1 Henry inductor, the 7 volt zener diode, the current draw of the two ICs, and the loop current. Figure 5 indicates the Tip-Ring voltage versus loop current for the two modes (the inductor resistance is 38 ohms).

To facilitate the design of the base drive to T2, diode D1 is added to the collector of T1, providing approximately 1.8 volts at that point. At the cathode of D1, the voltage is still regulated at 1.1 volts.

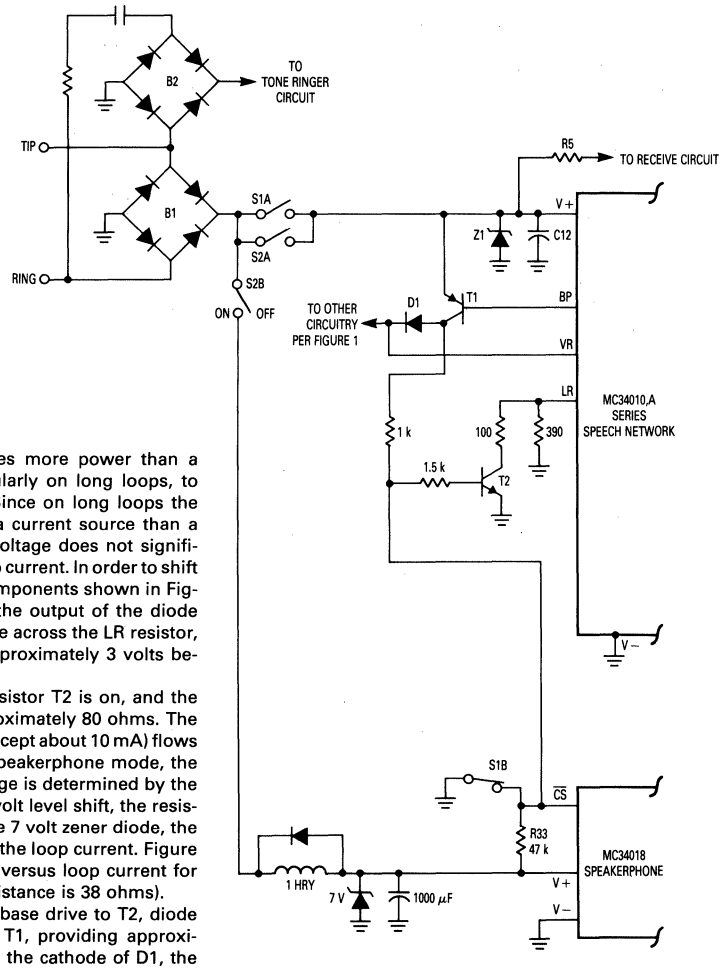


Figure 4. DC Level Shift

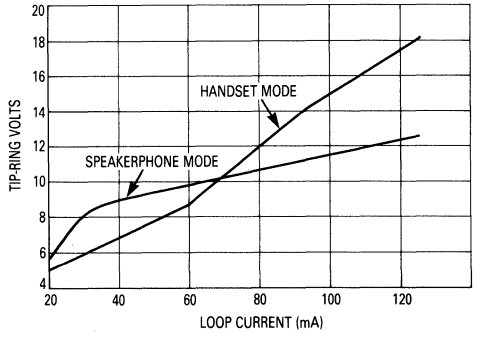


Figure 5. Tip-Ring Voltage versus Loop Current

MICROPHONE CONTROLS

To mute the handset microphone when the speakerphone speech mode is in effect, the circuit of Figure 6 is used for the MC34010 (MC34011, MC34013), and the circuit of Figure 7 is used for the MC34010A (MC34011A, MC34013A).

In Figure 6, when the handset mode is in effect, S1B takes the MM pin low, enabling the handset microphone by turning on the MIC pin (to ground). When the speakerphone mode is in effect, MM is taken high through R32, disabling the handset microphone (MIC pin is open).

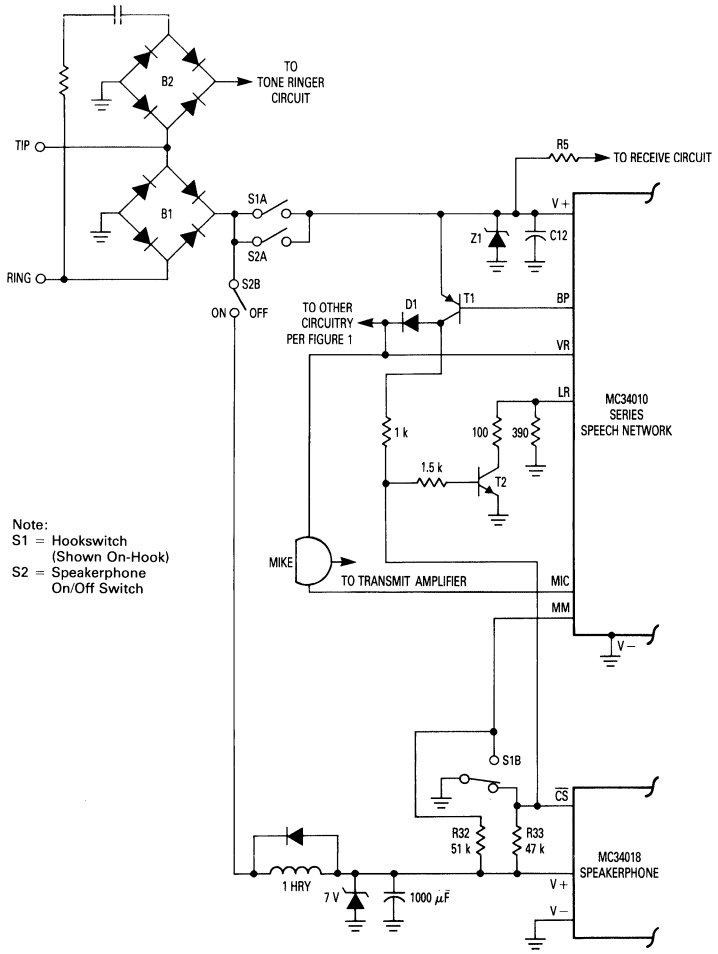


Figure 6. Microphone Muting — MC34010 Series

In Figure 7, in the handset mode, S1B is open, T3 is on, and the microphone bias current flows through the MIC pin. In the speakerphone mode, S1B is closed, turning off T3, disabling the microphone. T3 is required for disabling the microphone with the "A" series speech networks since the transmit amplifier is disabled when the MM pin is taken high.

In both the "non-A" and the "A" version circuits, the handset microphones are muted during dialing due to the fact that the MIC pin is opened by the dialer circuit.

SPEECH SIGNALS

Referring to the complete schematics (Figures 8, 9, 10, and 11) the receive signals coming in on Tip & Ring are sent to the handset receiver (at RXO) and to the speakerphone circuit's "receive input" path by the MC34010's hybrid function. It is not necessary to mute the handset receiver during speakerphone operation.

The transmit signals from the handset microphone are put onto the Tip & Ring lines through the MC34010's hybrid function, with a gain determined by resistors R27–R30. In the speakerphone mode, the transmit output signals (at TXO of the MC34018) are attenuated by R35 before being applied to the MC34010's transmit amplifier. The level of the speakerphone transmit signals at Tip & Ring can be adjusted by varying R35.

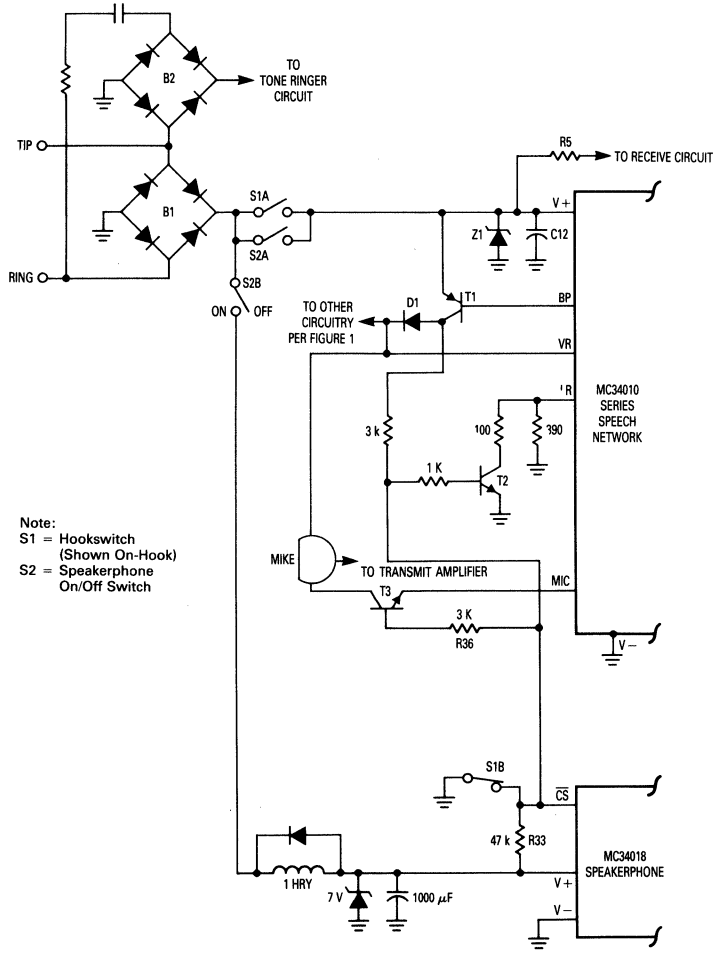
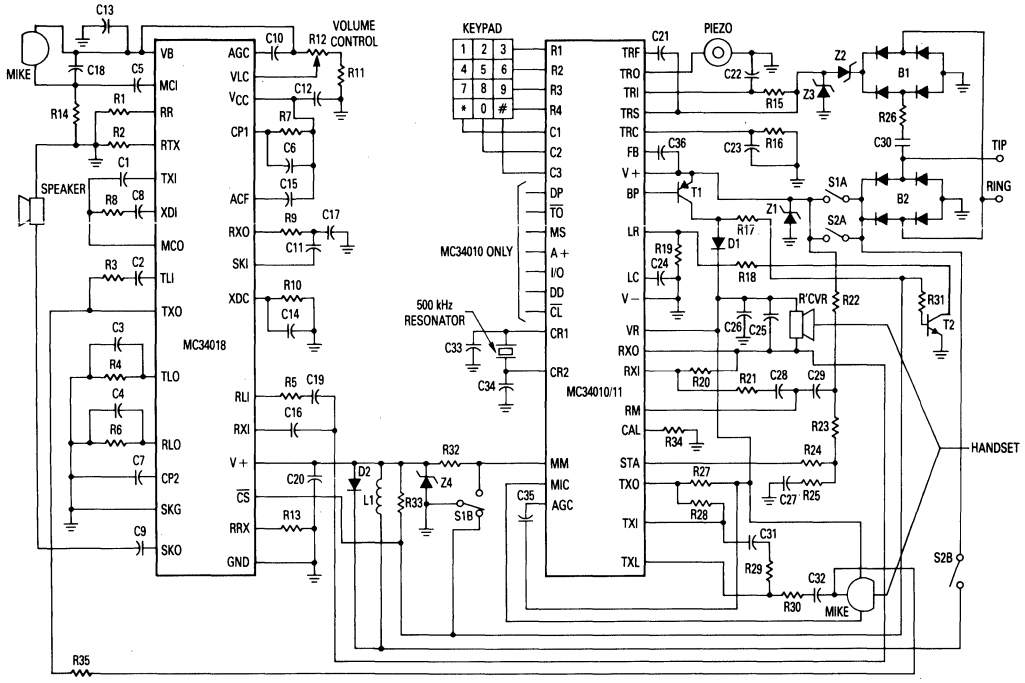


Figure 7. Microphone Muting — MC34010A Series



MC34010/11 and MC34018
COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R15 — 1.8 k
R16 — 200 k
R17 — 1 k
R18 — 100
R19 — 390
R20 — 200 k
R21 — 56 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R26 — 6.8 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1.5 k
R32 — 51 k
R33 — 47 k
R34 — 36
R35 — 33 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C21 — 1 μF
C22 — 4.7 μF
C23 — 620 pF
C24 — 0.01
C25 — 0.01 μF
C26 — 2.2 μF
C27 — 0.1
C28 — 0.05
C29 — 0.05
C30 — 1 μF, NP
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z2 — 4.7 V
Z3 — 30 V
Z4 — 7 V
D1, D2 — 1N4001

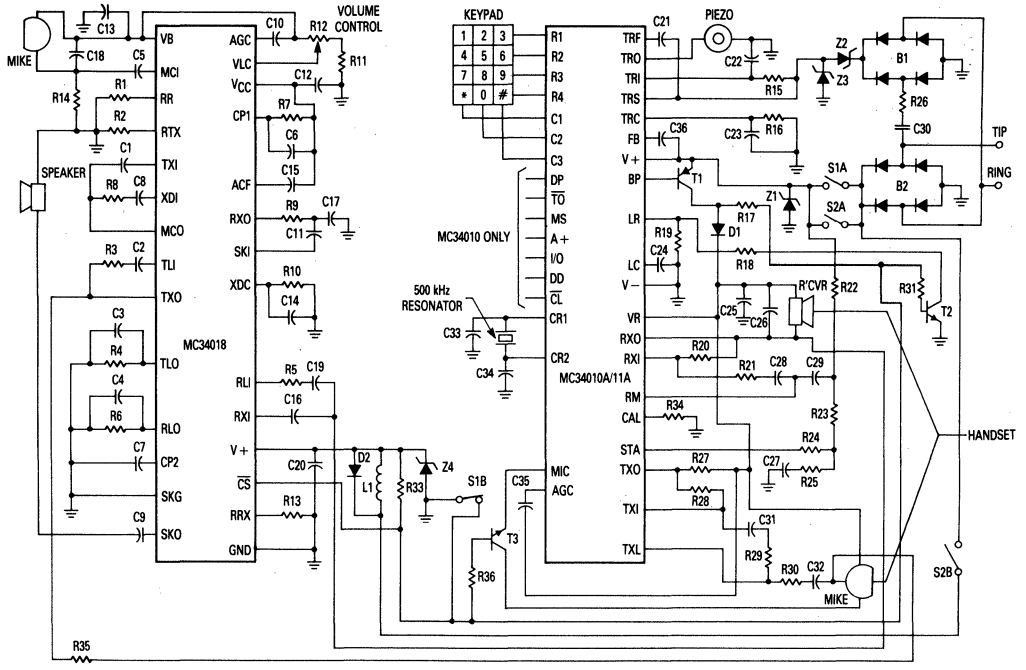
T1 — 2N4126
T2 — 2N2222A

B1 — 1N4004's
B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 8. Handset/Handsfree System Using the MC34010/11 and MC34018



MC34010A/11A and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R15 — 1.8 k
R16 — 200 k
R17 — 3 k
R18 — 100
R19 — 390
R20 — 200 k
R21 — 56 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R26 — 6.8 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1 k
R33 — 47 k
R34 — 36
R35 — 33 k
R36 — 3 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C21 — 1 μF
C22 — 4.7 μF
C23 — 620 pF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C30 — 1 μF, NP
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z2 — 4.7 V
Z3 — 30 V
Z4 — 7 V

D1, D2 — 1N4001

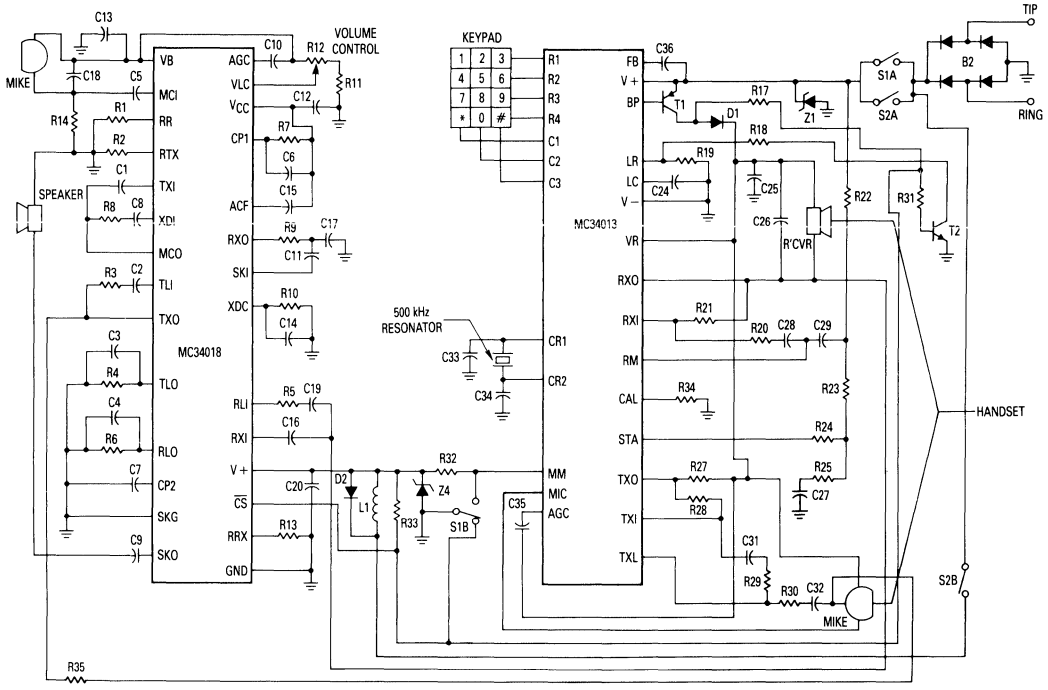
T1 — 2N4126
T2, T3 — 2N2222A

B1 — 1N4004's
B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 9. Handset/Handsfree System Using the MC34010A/11A and MC34018



MC34013 and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R17 — 1 k
R18 — 100
R19 — 390
R20 — 56 k
R21 — 200 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1.5 k
R32 — 51 k
R33 — 47 k
R34 — 36
R35 — 33 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z4 — 7 V

D1, D2 — 1N4001

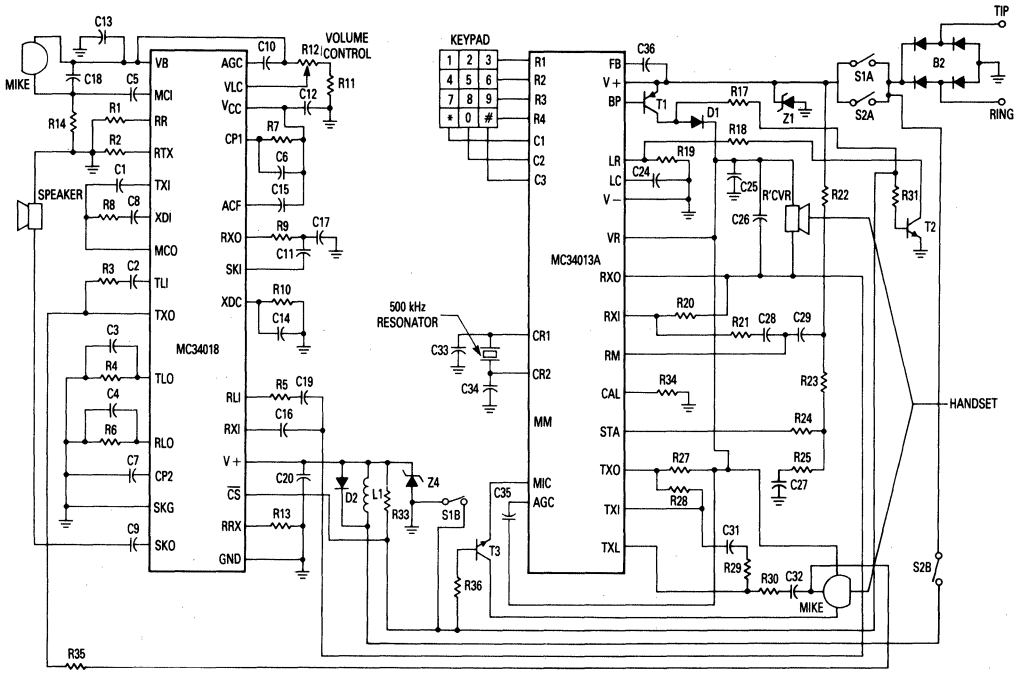
T1 — 2N4126
T2 — 2N2222A

B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 10. Handset/Handsfree System Using the MC34013 and MC34018



MC34013A and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R17 — 3 k
R18 — 100
R19 — 390
R20 — 56 k
R21 — 200 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1 k
R33 — 4.7 k
R34 — 36
R35 — 33 k
R36 — 3 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z4 — 7 V

D1, D2 — 1N4001

T1 — 2N4126
T2, T3 — 2N2222A

B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 11. Handset/Handsfree System Using the MC34013A and MC34018

CONCLUSION

Interfacing the MC34018 speakerphone circuit to the MC34010 series of speech networks has been shown to be simple and straightforward. The interface requires the addition of 2 diodes, 5 resistors, either 1 or 2 transistors (depending on the speech network), and one diode bridge for the tone ringer circuit in the MC34010(A) and the MC34011(A). Any existing MC34010 type circuit can be easily modified to accept the speakerphone circuit.

REFERENCES

MC34010 Data Sheet, Dec. 1983, Motorola, Inc.
MC34010A Data Sheet, May, 1985, Motorola, Inc.
MC34013 Data Sheet, Nov. 1983, Motorola, Inc.
MC34013A Data Sheet, Feb. 1985, Motorola, Inc.
MC34018 Data Sheet, Apr. 1985, Motorola, Inc.

AN958

Transmit Gain Adjustments For The MC34014 Speech Network

By
Scott Bader and Dennis Morgan
Bipolar Analog IC Division

3

INTRODUCTION

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatability with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters.

CIRCUIT DESCRIPTION

Refer to Figure 1. The microphone is assumed to be an electret type, characterized by a high dynamic impedance. It is therefore considered to be an ac current source rather than a voltage source. If the microphone used has a dynamic impedance which is not high (compared to R_8), then the microphone must be modeled as a current source paralleled by its dynamic impedance. That impedance value must then be considered to be in parallel with R_8 in the following equations. The T_X amplifier has a fixed gain of -20, and the EQ amplifier gain varies from 0.25 to 0.75, depending on the loop current. Z_L is the line impedance. The transmit gain is defined as $V+/I_{mic}$ and is equal to:

$$\frac{V+}{I_{mic}} = \frac{R_6 \times Z_L \times A_{TX}}{(1 + R_6/R_A)R_9 + (A_{TX})\ (A_{EQ})\ (Z_L)}$$

where A_{TX} = gain of the transmit amplifier (20 V/V)
A_{EQ} = gain of the equalization amp. (0.25 to 0.75 V/V)
R_A = R_8//10 kΩ (10 kΩ = input impedance of Tx amp.)

The ac impedance of the circuit is defined as:

$$Zac = \frac{R_9\ (1 + R_6/R_A)}{(A_{TX})\ (A_{EQ})}$$

The receive gain (see data sheet for the equivalent circuit) is defined as:

$$Grx = \frac{R_4}{R_1} + \frac{(X_C//R_2)\ (A_{EQ})\ (A_{TXO})\ (A_{STA}) \times R_4}{((X_C//R_2) + R_3)\ (1 + R_6/R_A) \times R_2}$$

As can be seen from the above equations, changing R_6 while maintaining the R_6/R_A ratio constant will result in a transmit gain change (proportional to R_6) but will not affect the other parameters. For example, increasing R_8 and R_6 by a factor of 3 will increase the transmit gain by ≈10 dB.

Using the above procedure to increase the transmit gain results in increasing R_8, which supplies the bias current to the microphone. If the higher value of R_8 results in insufficient bias voltage at the microphone, then the alternate biasing scheme of Figure 2 should be used.

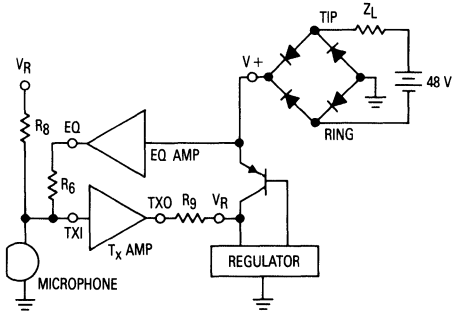


Figure 1. MC34014 Transmit Section

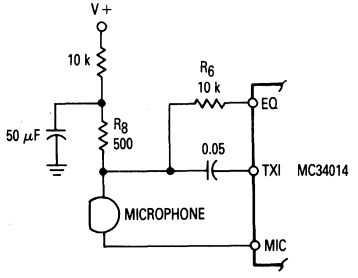


Figure 2. Alternate Biasing Scheme for Higher Voltage Microphones

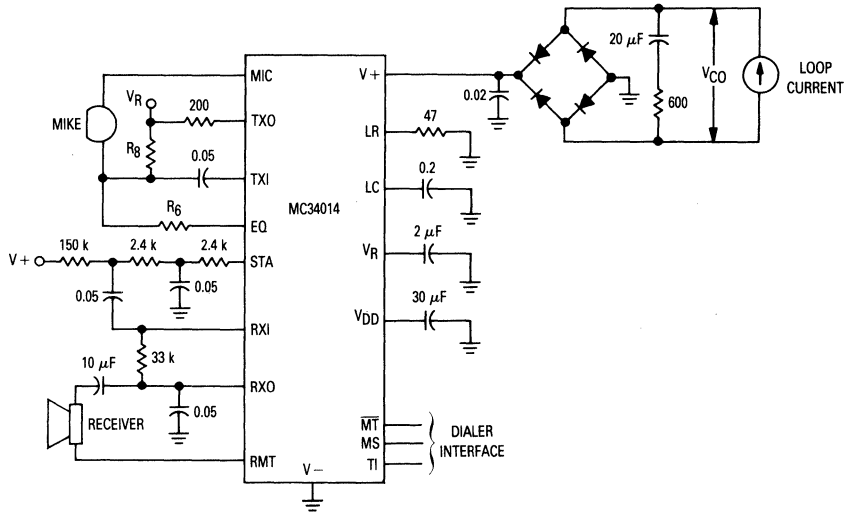
TEST RESULTS

Tests were conducted with a Primo EM-95A microphone, having a sensitivity of −53 dB ±3 dB (0 dB = 1 V/μbar), and a Hosiden KUC2123 microphone which has a sensitivity of −60 dB ±3 dB. The test circuit is shown in Figure 3. The tests consisted of applying a constant sound level to the microphones, and measuring the output at V_{CO}, while simulating line lengths of 0–21 Kfeet. The outputs of the two circuits were nearly identical at all line lengths.

CONCLUSION

Although the designs of the various parameters (transmit gain, receive gain, ac impedance, etc.) of the MC34014 speech network are not mutually exclusive due to the commonality of various components, it is possible to adjust the transmit gain independently to suit a particular microphone.

For further information on the MC34014 speech network, refer to the data sheet.



For Primo EM-95A microphone R_B = 500 Ω, R_6 = 10 k
For Hosiden KUC2123 microphone R_B = 1.5 k, R_6 = 30 k

Figure 3. Microphone Gain Test Circuit

AN959

A Speakerphone With Receive Idle Mode

By
Dennis Welty and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. Under conditions where noise from the telephone line (in the receive path) exceeds the background noise in the transmit path, the speakerphone will switch easily, or even lock, into the receive mode. Under these conditions the conversation will sound "dead" to the party at the far-end. It will also be more difficult for the near-end party to activate the transmit channel since the transmit detection is at the output of the transmit attenuator, which will be at maximum attenuation during this time. The addition of a receive idle mode can alleviate this problem by ensuring that the transmit and receive gains will be approximately equal when no voice signals are present. This allows the far-end party to hear ambient noises, and also increases the sensitivity to transmit signals.

CIRCUIT DESCRIPTION

The additional circuitry is shown in Figure 1. The receive signal normally applied to RXI also drives XDI through a 2.7 kΩ resistor and a 0.1 μF capacitor. XDC is connected to VLC through the NPN and PNP emitter followers. When voice signals in the receive channel exceed the background noise by 4.6 dB, XDC switches high and turns off the PNP transistor (the 4.6 dB threshold is built into the MC34018). The voltage at VLC is then determined by the volume control potentiometer. When voice signals are no longer present, XDC decays to 0.5 VB and turns on the emitter followers. The voltage at VLC is now determined by the voltage at XDC. By decreasing the VLC voltage with the emitter followers the transmit and receive gains are adjusted to produce a receive-idle mode.

A peak detector using an external voltage comparator and diode is required to hold the receive attenuator fully on (out of the idle mode) when constant level signals, such as dial tone, are intentionally presented to the re-

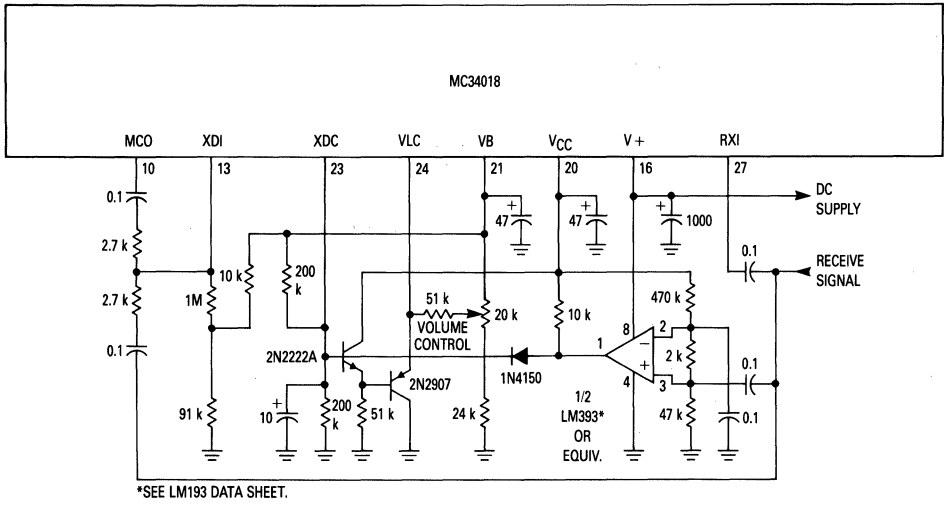


Figure 1. Receive-Idle Circuit

ceive channel. When the receive signal at the receive input exceeds the threshold on the comparator (typically 20 mV) the peak detector charges the capacitor at XDC which prevents the speakerphone from relaxing to the idle mode. The PNP transistor is turned off and the voltage at VLC is then determined by the volume control potentiometer. Under these conditions the speakerphone will be in the receive mode.

The sensitivity threshold of the voice detector circuitry can be changed by applying a dc current to XDI. The threshold current (nominally 250 nA) also prevents XDC from switching sporadically in quiet signal conditions. The threshold current is determined by the 1 Megohm resistor between XDI and the 10 kΩ/91 kΩ divider referenced to VB. Whenever receive signal currents exceed the threshold current by 4.6 dB, the voice detector will respond and allow XDC to switch high.

CONCLUSION

The receive-idle mode is simple to implement, and improves the performance of the speakerphone system by allowing noise rejection in both the receive and transmit channels. The voice-switching function operates only on valid speech, and ignores background noises.

REFERENCES

MC34018 data sheet, Motorola, 1985
LM193 data sheet, Motorola

AN960

Equalization of DTMF Signals Using the MC34014

by
Scott Bader and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. While the MC34014 does not have an internal dialer, it has the interface for a dialer so as to provide the means for putting the DTMF tones onto the Tip & Ring lines. The Equalization amplifier, whose gain varies with loop current, was meant primarily to equalize the speech signals. However, by adding one resistor, it can be used to equalize the DTMF signals as well.

CIRCUIT DESCRIPTION

Referring to Figure 1, the gain of the equalization amplifier varies with loop current as it is a function of the voltage at the LR pin (Pin 13). The gain varies from a minimum of −12 dB at low loop currents (long line), to −2.5 dB at high loop currents (short line). The output at EQ (Pin 6) is in phase with the signals going out onto Tip & Ring, but is out of phase with the DTMF input signals from the dialer at R7 (see Figure 2). Because of the out-of-phase relationship, the signal at EQ can be used to partially cancel the signals at the Tone Input (Pin 16). The addition of resistor R10 provides the path for this function, with the result that the DTMF gain increases as loop current decreases.

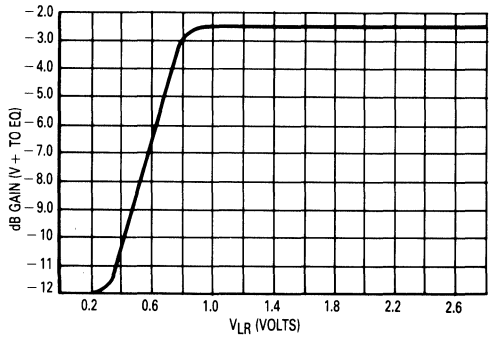


Figure 1. Equalization Amplifier Gain

Because the addition of R10 cancels some of the signal going into Pin 16, resistor R7 must be decreased in order to restore the overall gain from the dialer to Tip & Ring.

The DTMF gain values indicated in Figures 3 and 4 is the gain from the tone dialer (input at R7) to the Tip & Ring lines terminated with a 600 ohm resistor. Figure 3 indicates the gain CHANGE (as the loop current is varied from 60 to 20 mA) versus different values of R10. The gain change is a function of R10, and independent of R7. Figure 4 indicates the DTMF gain versus R7 for different values of R10 at a loop current of 20 mA.

Because the typical telephone line is not purely resistive, there will be a phase shift of other than 180° from the DTMF dialer to Tip & Ring in most applications. For this reason, the values of R10 and R7 will have to be adjusted slightly from those in the graphs to compensate for the phase shift.

The MC34014 data sheet mentions that a dc bias current of 20–50 μA is required into Pin 16 in order to bias the DTMF amplifier. The addition of R10 will provide the bias current from the EQ output for most applications, in which case it may be desirable to ac couple the dialer to R7 with a 0.5 μF capacitor. Excessive bias current will result in clipping of the signals at Tip & Ring. If just the addition of R10 results in excessive bias current, then the EQ output should be ac coupled to R10 with a 0.5 μF capacitor, and the bias current supplied either from the dialer or from an additional resistor as shown in Figure 5.

For further information on the MC34014, refer to its' data sheet.

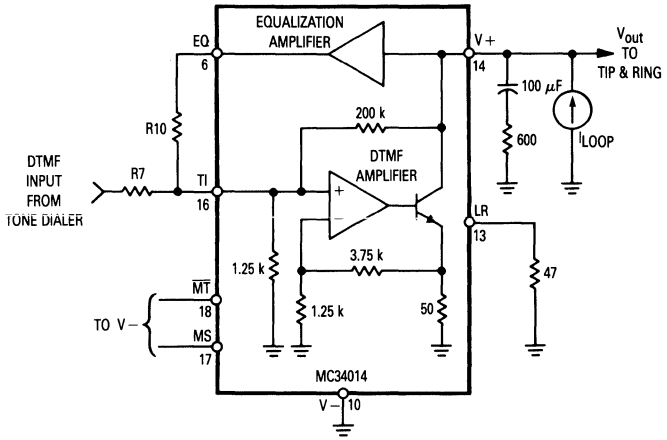


Figure 2. DTMF Driver

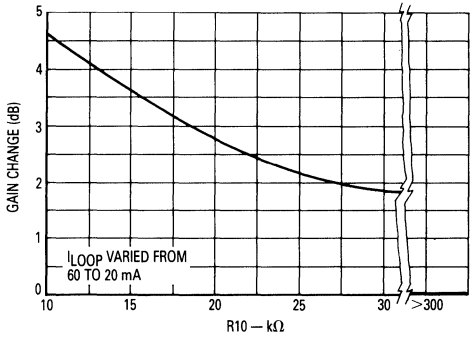


Figure 3. Gain Change

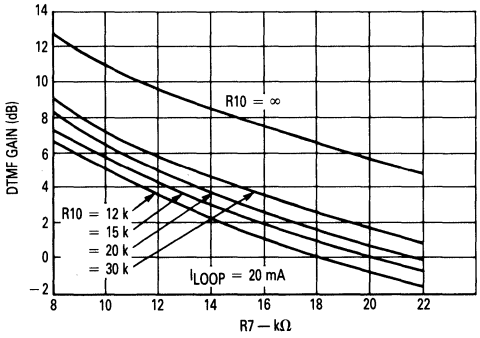


Figure 4. DTMF Gain

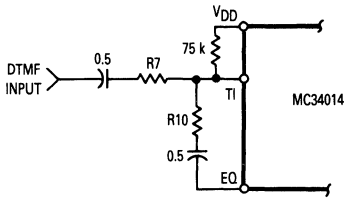


Figure 5. Alternate Biasing

AN1002

A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs

Prepared by
Dennis Morgan
Bipolar Analog IC Division

3

INTRODUCTION

This application note describes the procedure for combining the MC34114 speech network with the MC34018 speakerphone circuit into a featurephone which includes the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function, and line length compensation for both handset and speakerphone operation.

Three circuits are developed in this discussion: a line-powered featurephone, a line-powered featurephone with a booster (for using the speakerphone on long lines), and one powered from a power supply. The circuits are nearly identical, except for the Tip/Ring interface. Their performance, however, differs noticeably, particularly in the low loop current range. Initially, the discussion will focus on the line-powered circuit.

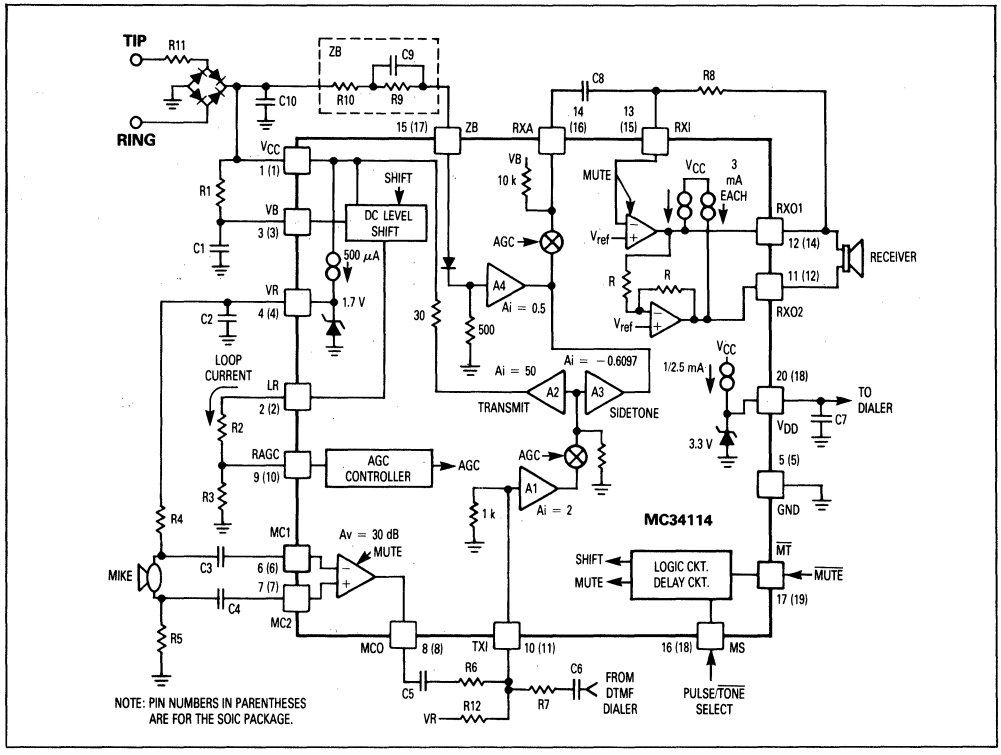


Figure 1. MC34114 Block Diagram

DESCRIPTION OF THE BUILDING BLOCKS

NOTE: Several pins on the ICs used in this application note have identical nomenclature (V_{CC}, VB, TXI, MS, V_{DD} and RXI). They provide separate functions, and are not to be connected together, unless so noted.

MC34114 Speech Network

The MC34114 is a speech network which interfaces with Tip & Ring and provides the 2-to-4 wire conversion (see Figure 1). The transmit gain is determined by the microphone amplifier (fixed gain of 30 dB), R6, C5, the internal current gains of A1, A2, the AGC, and the line impedance in parallel with R1. The receive gain is determined by ZB, the internal current gains of A4 and AGC, C8 and R8. The sidetone cancellation is determined by A3 and the ZB network. The AGC points have a current gain of 1 at low loop current, and decrease to 0.5 (−6 dB) at higher loop currents, thus providing line length compensation. R1 (typically 600 Ω) sets the circuit's terminating impedance for ac (return loss) purposes.

The $\overline{\text{MUTE}}$ input (when low) disables the microphone amplifier, and partially mutes the receive amplifier (with an internal 1 k feedback resistor), when dialing. DTMF dialing signals are injected at TXI through R7 and C6. The Mode Select (MS) input (when low, and $\overline{\text{MT}}$ is low) provides a voltage boost at V_{CC} to ensure adequate voltage during DTMF dialing at low loop currents. The 3.3 volt regulated output (V_{DD}) powers the dialer, and the 1.7 volt regulated output (VR) is used to bias the microphone.

The dc characteristics at Tip & Ring are determined by the diode bridge (1.4 volts), a level shift of approximately 2.9 volts from V_{CC} to LR, and the voltage across R2 + R3 (typically 43 Ω and 13 Ω). All the loop current, minus ≈10 mA, flows through those two resistors. The level shift (V_{CC} − LR) increases to ≈3.9 volts when both $\overline{\text{MUTE}}$ and MS are low (tone dialing mode). The voltage at RAGC, when within the range of 0.5 to 1 volt, controls the internal AGC as a function of loop current.

MC34018 Speakerphone

The MC34018 speakerphone IC (see Figure 2) provides all of the necessary functions for a complete speakerphone circuit in a single integrated circuit. Included are the transmit and receive attenuators, which operate in a complementary manner, to provide the necessary half-duplex function. The two level detectors, in conjunction with the background noise monitor and control algorithm, provide a two point sensing and decision making system to control the attenuators based on the levels and timing of the transmit and receive signals. Additional functions include the microphone amplifier, speaker amplifier, volume control for the receive path, and a chip select pin. The gain of the speaker amplifier, normally +34 dB, is reduced by the AGC circuit in the presence of strong signals to prevent clipping at SKO. The component values shown are typical.

Connections to the speakerphone circuit are made to the four points at the right end of Figure 2 (Receive Input, DC Supply, Chip Select, & Transmit Output).

The DC supply requires 4 to 11 volts dc, and it must be well filtered to prevent oscillations when the speaker amp is operating. In a typical line powered circuit, an inductor (1H) is used, in conjunction with the 1000 μF capacitor shown, to filter the voltage derived from the loop current.

The Receive Input of Figure 2 is derived from the 4-wire side of the speech network. The gain from RXI to the speaker is +40 dB when in the receive mode at maximum volume (+6 dB in the attenuator, +34 dB in the speaker amp). At minimum volume, the attenuator's gain reduces by ≈30 dB, for an overall gain of +10 dB. In the transmit mode, the receive gain is ≈ −4 dB.

The transmit gain, from the microphone to Transmit Output, is +40 dB (+34 dB in the mike amp, +6 dB in the attenuator), and does not vary with the volume control. In the receive mode, the transmit gain is ≈ −4 dB. The Transmit Output will connect to the 4-wire side of the speech network.

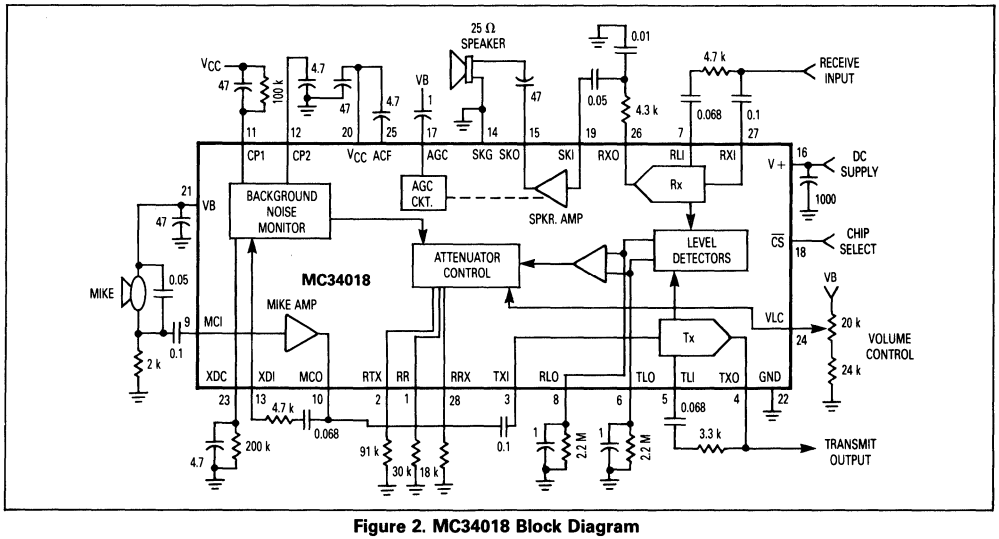


Figure 2. MC34018 Block Diagram

The overall speakerphone's transmit and receive gains to/from Tip & Ring will be adjusted at the interface from Figure 2 to the speech network.

Chip Select enables the MC34018 when at a logic low. The MC34018's supply current is normally ≈5 mA. When $\overline{CS}$ is taken higher than 1.6 volts, the IC is disabled, and the supply current drops to ≈500 μA.

V_{CC} (Pin 20) is a regulated 5.4 volt output, and VB (Pin 21) is a regulated 2.9 volt output. VB is typically used to bias the microphone.

MC145412 Dialer

The dialer is a pulse/tone dialer with 10 number memory, including last number redial (Figure 3). The pulse and tone functions are selectable by Pin 10 (MS). The circuit uses a standard 3.58 MHz crystal, and a standard 3x4 or 4x4 keypad.

The NPN transistor at Pin 12 indicates the on-hook/off-hook status to the IC. Power for the dialer is the MC34114's V_{DD} (3.3 volts), diode connected with a memory sustaining battery. The DTMF output goes to C6/R7 of Figure 1, which sets the gain.

The $\overline{OPL}$ ($\overline{OUTPULSING}$) pin is used to interrupt the loop current when pulse dialing. The pin is active low, open drain. TSO (Tone Signal Output) provides a pacifier tone during pulse dialing. The tone is a 500 Hz square wave, which swing from V_{DD} to V_{SS}.

The Mute Output ($\overline{MO}$) is active low, open drain, and pulls to ground while dialing. It is used to mute the speech paths during dialing.

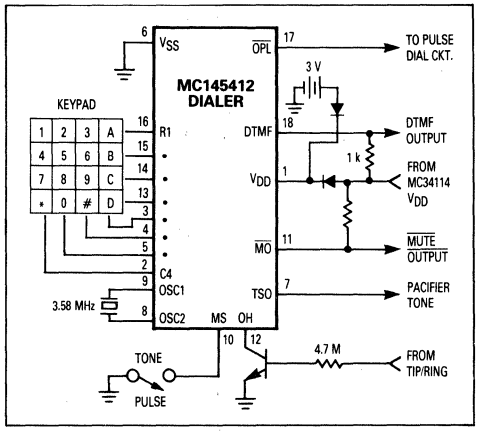


Figure 3. Pulse/Tone Dialer

SWITCHING THE CIRCUIT AROUND

The logic functions involve: a) switching the circuit from handset mode to/from speakerphone mode, b) switching in and out of either dialing mode while in either handset or speakerphone mode, and c) muting the two microphones for the "Privacy" function. Table 1 tabulates the fundamental requirements applicable to any featurephone:

Table 1.

Function	HANDSET		SPEAKERPHONE	
	Mike	R'cvr	Mike	Speaker
Handset Speech	On	On	Off	Off
Handset Dialing	Off	Mute	Off	Off
Handset Mike Mute	Off	On	Off	Off
Speakerphone Speech	Off	Off	On	On
Speakerphone Dialing	Off	Off	Off	Mute
Speakerphone Mike Mute	Off	Off	Off	On

In Table 1, "ON" means fully functional, "OFF" means non-functional, and "MUTE" means partially muted (10 to 20 dB). To apply Table 1 to the specific ICs described above, the requirements are expanded as follows:

Table 2.

Function	MC34114 $\overline{MT}$	MC34114 MS	MC34018 $\overline{CS}$	Loop Current	MC145412 MS
Handset Speech	Hi	X	Hi	Thru MC34114	X
Handset Pulse Dialing	Lo	Hi	Hi	Thru MC34114	Open
Handset Tone Dialing	Lo	Lo	Hi	Thru MC34114	Gnd
Handset Mike Mute	Lo	X	Hi	Thru MC34114	X
Speakerphone Speech	Lo	X	Lo	To MC34018	X
Speakerphone Pulse Dialing	Lo	Hi	Lo	To MC34018	Open
Speakerphone Tone Dialing	Lo	Lo	Lo	To MC34018	Gnd
Speakerphone Mike Mute	Lo	X	Lo	To MC34018	X

X = Don't Care

A summary of Table 2 is:

a) The MC34114 speech network is put into the Mute mode ($\overline{MT}$ = Lo) not only for dialing, but also to mute the microphone and receiver for the Privacy function (Mike Mute), and when in the speakerphone mode.
b) The MC34018 is disabled for all the handset functions, and enabled for all the speakerphone functions.
c) The loop current, which normally flows through the LR pin of the MC34114 (see Figure 1), is directed instead to the MC34018 in the speakerphone mode so as to make the power available to the speaker.
d) The MS pins of the dialer, and of the MC34114, are significant only during dialing.

PUTTING IT ALL TOGETHER

Switching Between Handset and Speakerphone Modes

To switch between modes, two actions are necessary: 1) Divert the excess loop current, which normally flows through the MC34114, to the MC34018 during speakerphone mode, and 2) enable and disable the speech network and speakerphone circuits appropriately. The circuit of Figure 4 fullfills those requirements:

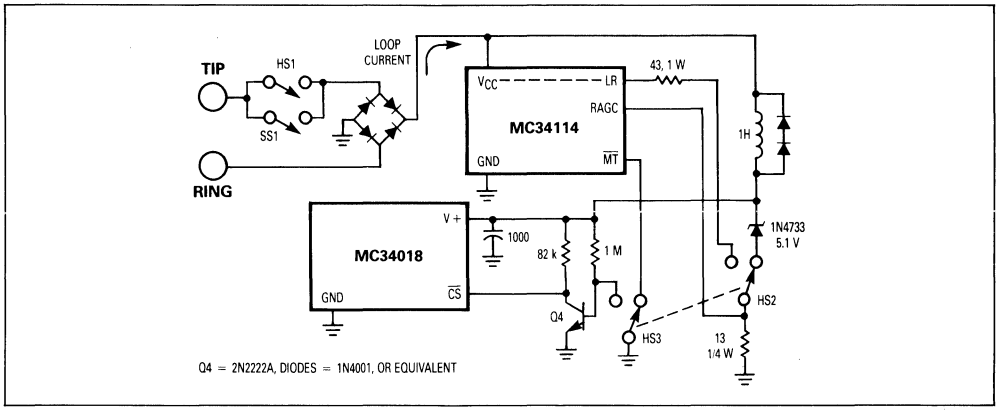


Figure 4. Switching Between Modes

HS (3 poles) is the hookswitch operated by lifting the handset. SS (1 pole) activates the speakerphone when the handset is on-hook. The switches are shown on-hook in Figure 4.

If the handset is lifted (HS transfers), the MC34114 consumes ≈10 mA internally, and the excess loop current flows out of the LR pin and through the 43 Ω and 13 Ω resistors. The voltage across the 13 Ω resistor controls the AGC function. The configuration in this position is similar to that of Figure 1. Additionally, Q4 is off, allowing $\overline{CS}$ to be pulled high, disabling the MC34018.

If the handset is on-hook, and switch SS is closed, the MC34114 still consumes ≈10 mA internally, but the excess loop current now flows through the 1 Henry choke, the zener diode, and the 13 Ω resistor. The voltage across the 13 Ω resistor still controls the AGC function of the MC34114. The MC34018's $\overline{CS}$ is held low by Q4, enabling the speakerphone, and the MC34114's $\overline{MT}$ is low, muting its microphone and receive amplifiers. If the handset is lifted while the speakerphone is in operation, the circuit reverts to the handset mode.

It may appear that $\overline{CS}$ and $\overline{MT}$ could be connected together and to HS3 to provide the same functions, thereby eliminating Q4. The fact, however, that other parts of the circuit will be connected to $\overline{MT}$ in subsequent sections of this application note negates that possibility.

Joining the Receive Paths

Refering to Figure 1, receive signals arriving at Tip & Ring generate a current through the ZB network, into Pin 15. That current is modified by A4, the AGC, made available (as a current) at RXA, and coupled to RXI, where it is converted to a voltage by the receive amplifiers and R8. The ZB network is typically 12 kΩ, and R8 is typically 3.9 kΩ. The receive gain to the handset receiver is therefore nominally −10 dB at low loop currents.

To feed the receive signals to the speakerphone, the circuit of Figure 5 is used.

The current out of RXA is now split (by the 1 kΩ resistors) so that approximately half goes to RXI (of the MC34114) via C8, and the other half is converted to a voltage (by the op amp) for the speakerphone's Receive Input (Figure 2). The MC33171 was chosen for its very low supply current (typically 180 μA). The op amp is powered from the MC34018's V_{CC} output (5.4 volts), and biased by the MC34018's VB (2.9 volts). The receive gain for the speakerphone is determined by the following equation:

$$G_{RX} = 20 \log \left(\frac{R_{RSP} \times A4 \times AGC \times 0.5}{ZB + 500\ \Omega} \right) + 40\ dB$$

The terms A4, ZB, and AGC (from Figure 1) are set at 0.5, 12 kΩ, and 1 respectively for low loop currents. The 0.5 in the above equation is due to the current splitting of Figure 5, and the +40 dB is the gain of the MC34018's receive attenuator and speaker amp. For a nominal overall gain of +30 dB, R_{RSP} calculates to ≈18 kΩ. At higher loop currents, the overall gain will be ≈ +24 dB. The above equation assumes the volume control is set to maximum.

To compensate for the reduced current going to the MC34114's receive amplifiers, R8 (Figure 1) is increased to 8.2 kΩ.

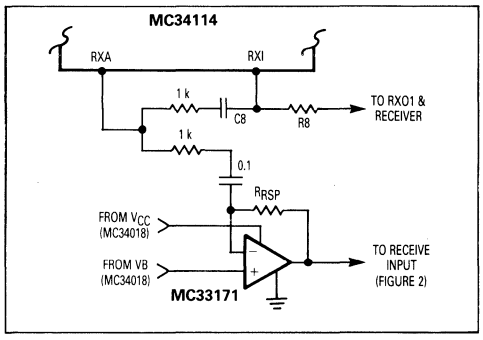


Figure 5. Joining the Receive Paths

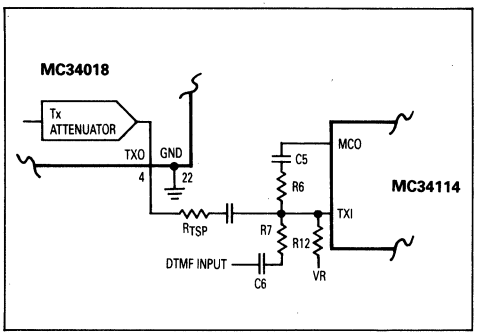


Figure 6. Joining the Transmit Paths

Joining the Transmit Paths

In the transmit path of Figure 1, the microphone signals are gained up by 30 dB by the mike amplifier. The output at MCO creates a current into TXI through R6 and C5. That current is gained up by 100 by A1 and A2 (assume AGC = 1), and A2's output current then acts on the parallel combination of R1 and the line's ac impedance. Typical values are: R6 = 15 kΩ, R1 = 600 Ω, and 600 Ω for the line's impedance. Neglecting the slight loading of R7, R12, and ZB, the overall handset transmit gain is ≈ +36 dB at low loop currents.

The transmit output (voltage signals) from the speakerphone circuit (Figure 2) is applied to the speech network at TXI (a current input) in Figure 1, through a resistor (R_{TSP}) and a coupling capacitor (see Figure 6). For a nominal gain of +44 dB (from the microphone to the MC34114's V_{CC}), R_{TSP} calculates to be ≈18 kΩ. The coupling capacitor (nominally 0.1 μF) can be varied to set the low frequency rolloff.

Fitting in the Dialer and Another Switch

The $\overline{\text{Mute Output}}$ of Figure 3 must mute three items: 1) The MC34114 by pulling its $\overline{\text{MT}}$ pin low, 2) the MC34018's transmit path, and 3) the MC34018's receive path. This is accomplished with the circuit of Figure 7:

During dialing, Q1–Q3 are turned on by the dialer. Q1 mutes the MC34114, which shuts off its microphone amplifier, and mutes the receive amplifier by ≈27 dB. To mute the speakerphone's transmit path, R_{TSP} (of Figure 6) is divided into two resistors, and the junction pulled low by Q2, providing ≈35 dB muting of TXO's signal. Since the MC34018 will switch to the receive mode during DTMF dialing, the transmit attenuator will provide an additional muting of 44 dB, for a total of ≈79 dB. The speakerphone's receive path is muted by reducing the effective resistance at RRX (MC34018's Pin 28) from 18 kΩ to ≈3.7 kΩ with Q3. From Figure 3 of the MC34018's data sheet, the receive attenuator's gain is reduced by ≈23 dB. The 1 μF capacitor on Q3 softens any "pops" in the speaker when switching out of muting.

The DTMF output in Figure 3 is simply connected to C6/R7 of Figure 1 (or Figure 6) to get the DTMF signals to Tip & Ring. Using 24 kΩ for R7, and 0.1 μF for C6, DTMF levels of ≈ −3.8 dBm will result at Tip & Ring.

For pulse dialing, Pin 17 of the MC145412 dialer ($\overline{\text{OPL}}$) is connected to a standard two transistor network to interrupt the loop current (Figure 8). The 12 volt zener diode protects the circuitry from voltage spikes during pulse dialing, and whenever a hook switch is opened.

The TSO output (pacifier tone), which is generated only when a keypad button is depressed in the pulse dialing mode, is injected to the MC34114's ZB pin so as to make it available to both the handset receiver and the speakerphone. This tone is not generated during DTMF dialing.

To select between pulse and tone dialing modes, the switch on the dialer's Pin 10 (Figure 3) is connected to the MC34114's MS pin (Pin 16). Since the MC34114's MS pin requires a pull-up resistor for a logic high, a diode must be added (Figure 8) so the dialer's MS pin is open when the switch is in the pulse position.

Switching in Some Privacy

The Privacy function (Mike Mute of Tables 1 and 2) requires only a 2 pole switch. One pole mutes the MC34114 to disable its microphone amplifier. The other pole is wired directly across the speakerphone's microphone.

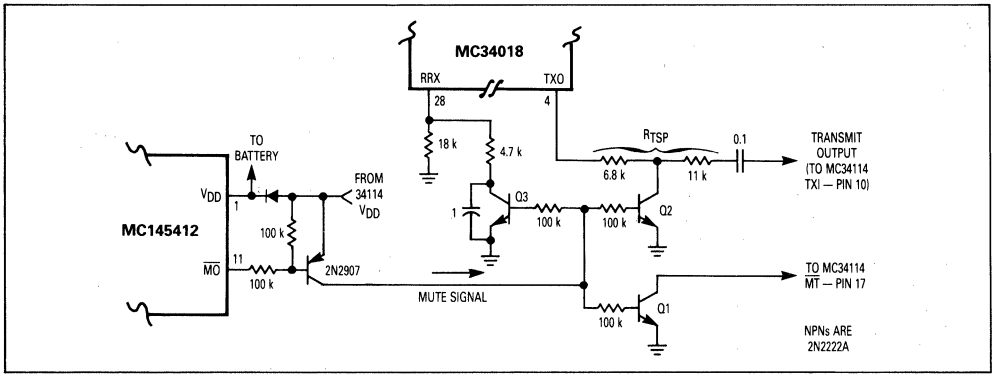


Figure 7. Muting Circuit

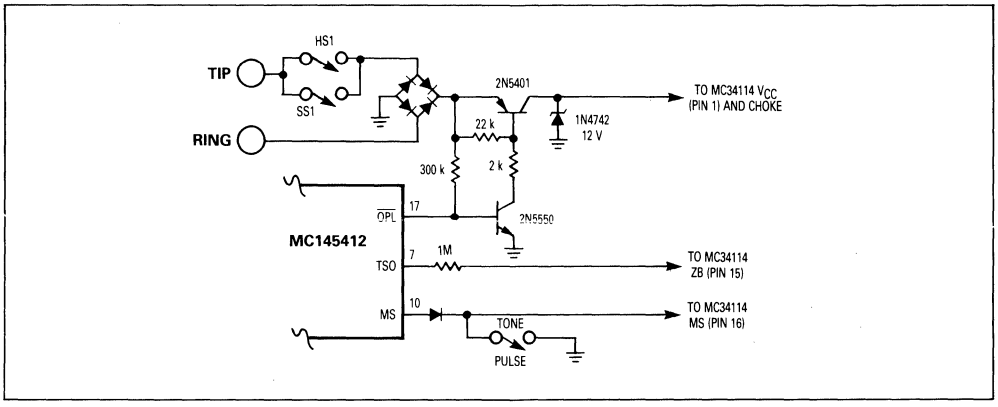


Figure 8. Pulse Dialing Circuit

Adding the Tone Ringer

The MC34017 tone ringer circuit, shown in Figure 9, is added to the circuit by simply connecting it directly across Tip & Ring. It is not necessary to disconnect the tone ringer when off-hook. This circuit will provide a ringer with an REN of ≈0.5, and meet all the EIA-470 and Bell system requirements for impedance, anti-bell tapping, and turn-on/off thresholds.

Finally, the Complete Circuit

The complete line-powered featurephone is shown in Figure 10. The performance curves for this circuit are shown in Figures 11–16. The "Speaker Amp Max Output Swing" is the maximum rms voltage available at the speaker amp output (Pin 15) of the MC34018 (its internal AGC circuit limits the maximum output to prevent clipping). The transmit gain tests involved replacing each microphone with a signal generator, and adjusting for a level of approximately −11 dBm at Tip & Ring into a 600 Ω resistive load. The receive tests involve applying approximately −27 dBm to Tip & Ring, and measuring the gain to the receiver or speaker.

As can be seen in Figure 12, the maximum available speaker power is a function of the loop current since all of the speaker current must come from the loop. Consequently, the receive gain for the speakerphone (Figure 15) shows a marked decrease at low loop currents. It must be remembered that in a line powered speakerphone, as the speaker draws current in response to a receive signal, the voltage at Tip & Ring decreases quickly. As the MC34018's V+ falls with the Tip & Ring voltage, the speaker amp's output capability is reduced. Consequently, a 25 Ω speaker is recommended for a line powered speakerphone as this makes the best use of the power available from the phone line. A lower impedance speaker will require more current, causing V+ to sag further for a given signal level. A higher impedance speaker draws less current, but produces less sound power.

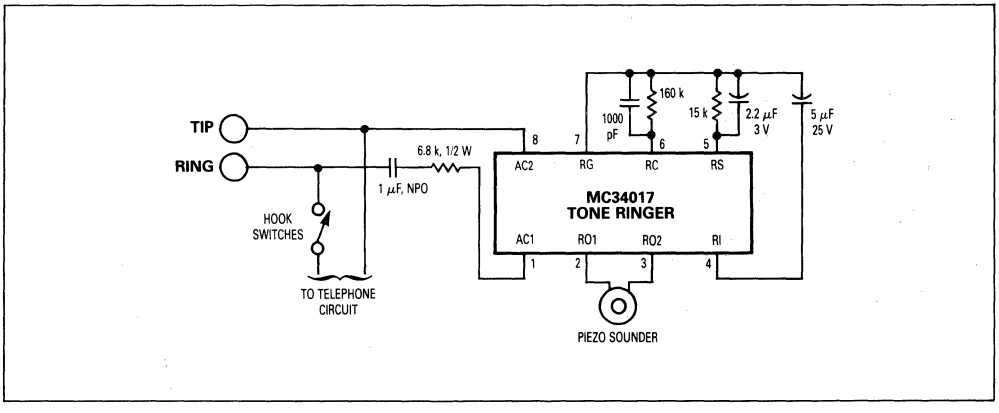
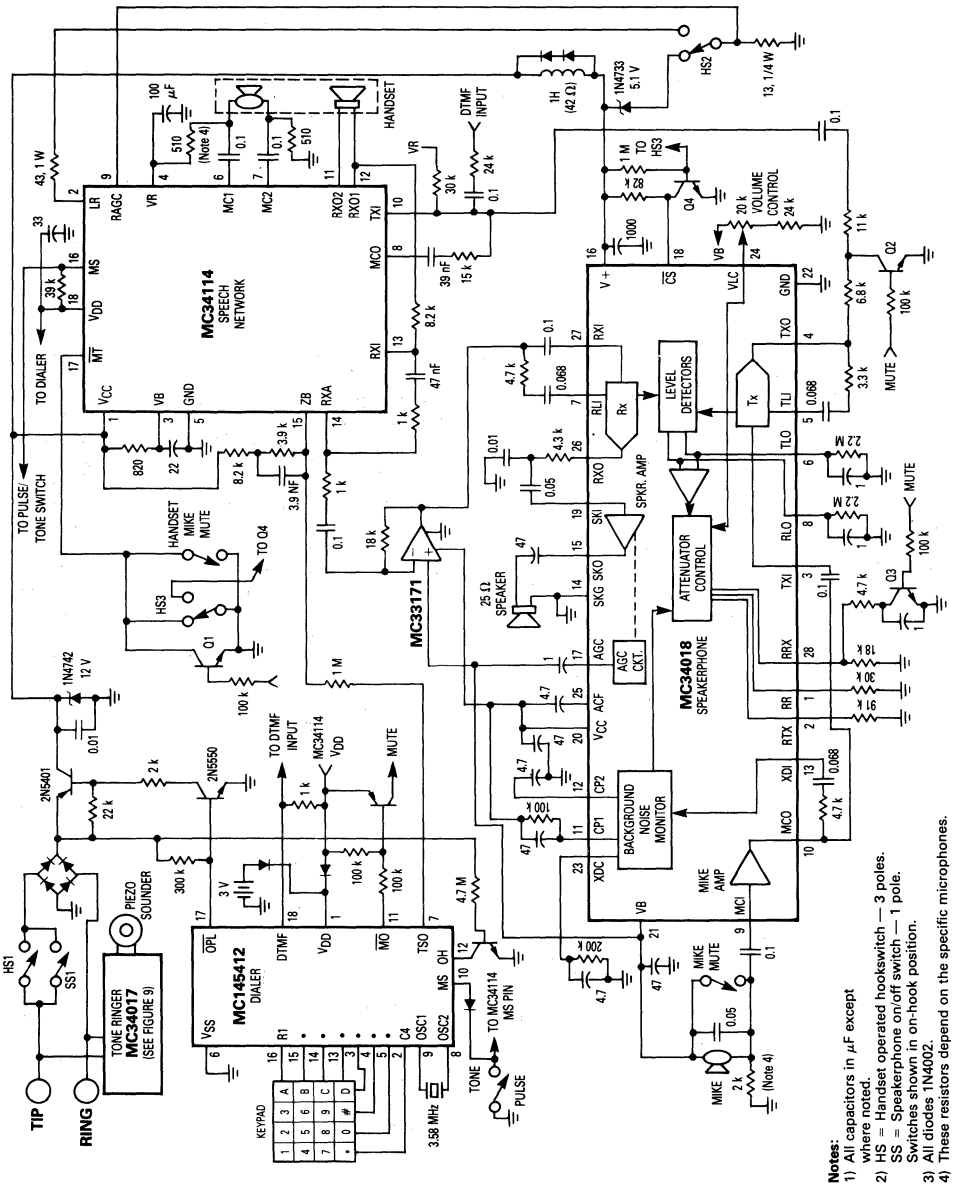


Figure 9. Tone Ringer Circuit

Additionally, the following muting specs apply:

1) **Handset microphone:** ≈62 dB while dialing, in speakerphone mode, or when Mike mute switch is closed.
2) **Speakerphone microphone:** ≈35 dB while dialing, plus an additional 44 dB due to the MC34018 switching to the receive mode. >60 dB while in the handset mode, or when the Mike mute switch is closed.
3) **Handset receiver:** ≈27 dB while dialing, or when in the speakerphone mode.
4) **Speaker:** ≈23 dB while dialing, >100 dB when in handset mode.



Notes:
1) All capacitors in μF except where noted.
2) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
3) All diodes 1N4002.
4) These resistors depend on the specific microphones.

Figure 10. Pulse/Tone Featurephone w/Memory — Line Powered

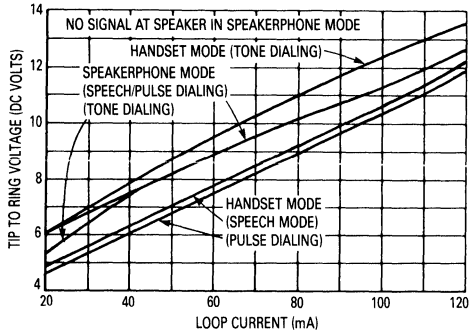


Figure 11. Tip to Ring DC Voltage versus Loop Current

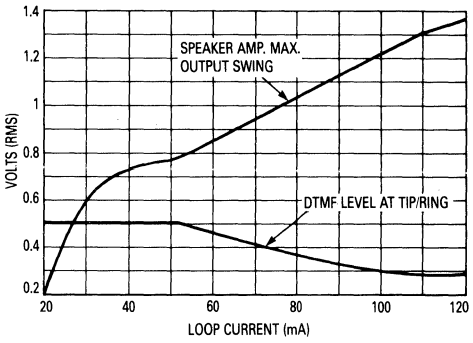


Figure 12. Speaker Amplifier Output and DTMF Level versus Loop Current

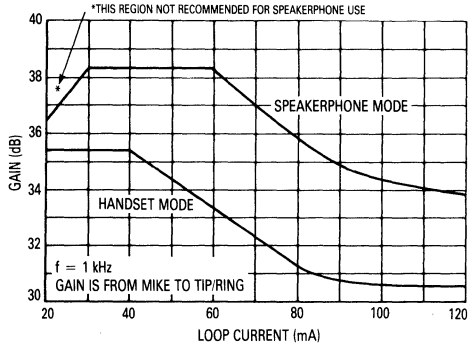


Figure 13. Transmit Gain versus Loop Current

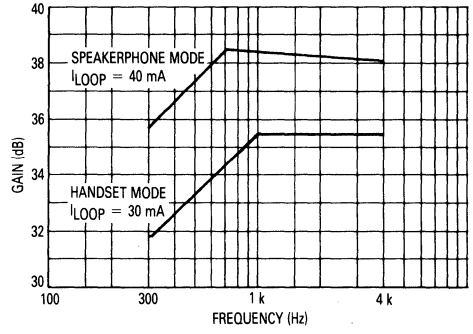


Figure 14. Transmit Gain versus Frequency

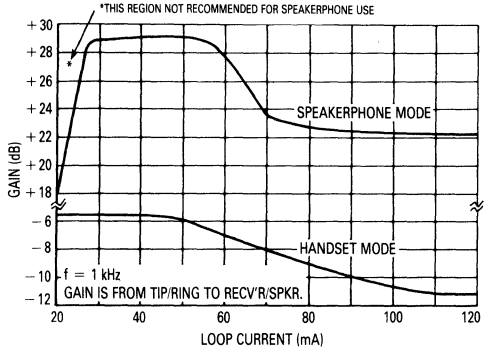


Figure 15. Receive Gain versus Loop Current

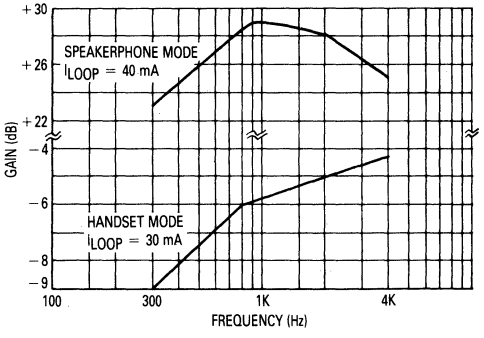


Figure 16. Receive Gain versus Frequency

BOOSTING THE SPEAKERPHONE AT LOW LOOP CURRENTS

Adding a Booster

To improve the performance of the speakerphone at low loop currents (below 30 mA), a minimal cost approach is to add an optional booster to the power supply portion of the MC34018. The approach in this application note is to use a wall mount transformer, similar to calculator chargers. A 9 volt ac Adapter, Radio Shack model #273-1455A, which contains the diode bridge and filter capacitor, was used to minimize the additional circuitry within the speakerphone itself. Since this particular ac adapter is specified for use with Radio Shack's speakerphones (model Duofone 102), it is this author's assumption that it complies with applicable FCC specifications, although that is not so stated on the transformer.

This application does not require a regulated voltage from the ac adapter, which further simplifies the design. The circuit of Figure 17 adds the ac adapter to the circuit of Figure 10:

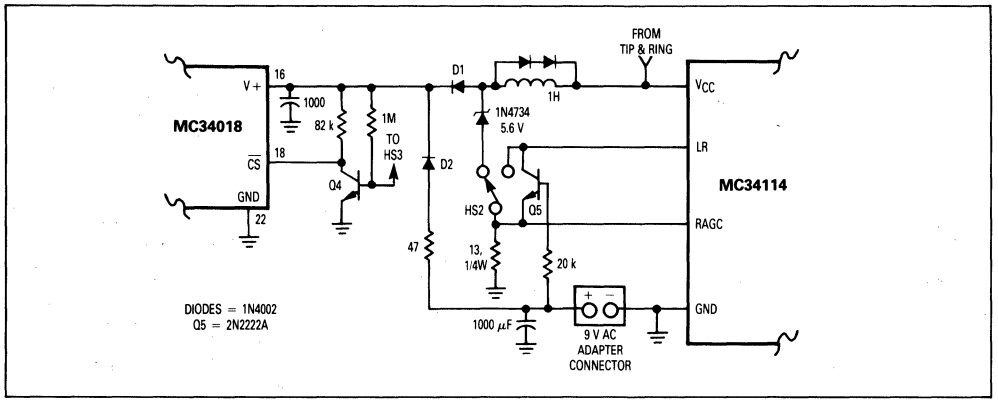


Figure 17. Adding a Speakerphone Booster

The circuit is the same as in Figure 10, but with the addition of Q5, the 20 k and 47 Ω resistors, 2 diodes, the 1000 μF capacitor, and the power supply connector for the ac adapter. The zener diode is changed to 5.6 volts to provide slightly more voltage to the MC34018 when the ac adapter is not used (at higher loop currents). The 47 Ω resistor provides short circuit protection for the ac adapter, and also aids in filtering 60 Hz ripple from the MC34018.

At low loop currents, and with the adapter plugged in, and the circuit in the speakerphone mode (HS2 as shown in Figure 17), D1 is reverse biased by the adapter's higher voltage. All of the speakerphone's current is now supplied by the ac adapter. Q5 is on, allowing the excess loop current to flow through the MC34114's LR pin. The dc characteristics at Tip & Ring are similar for the handset mode and the speakerphone mode.

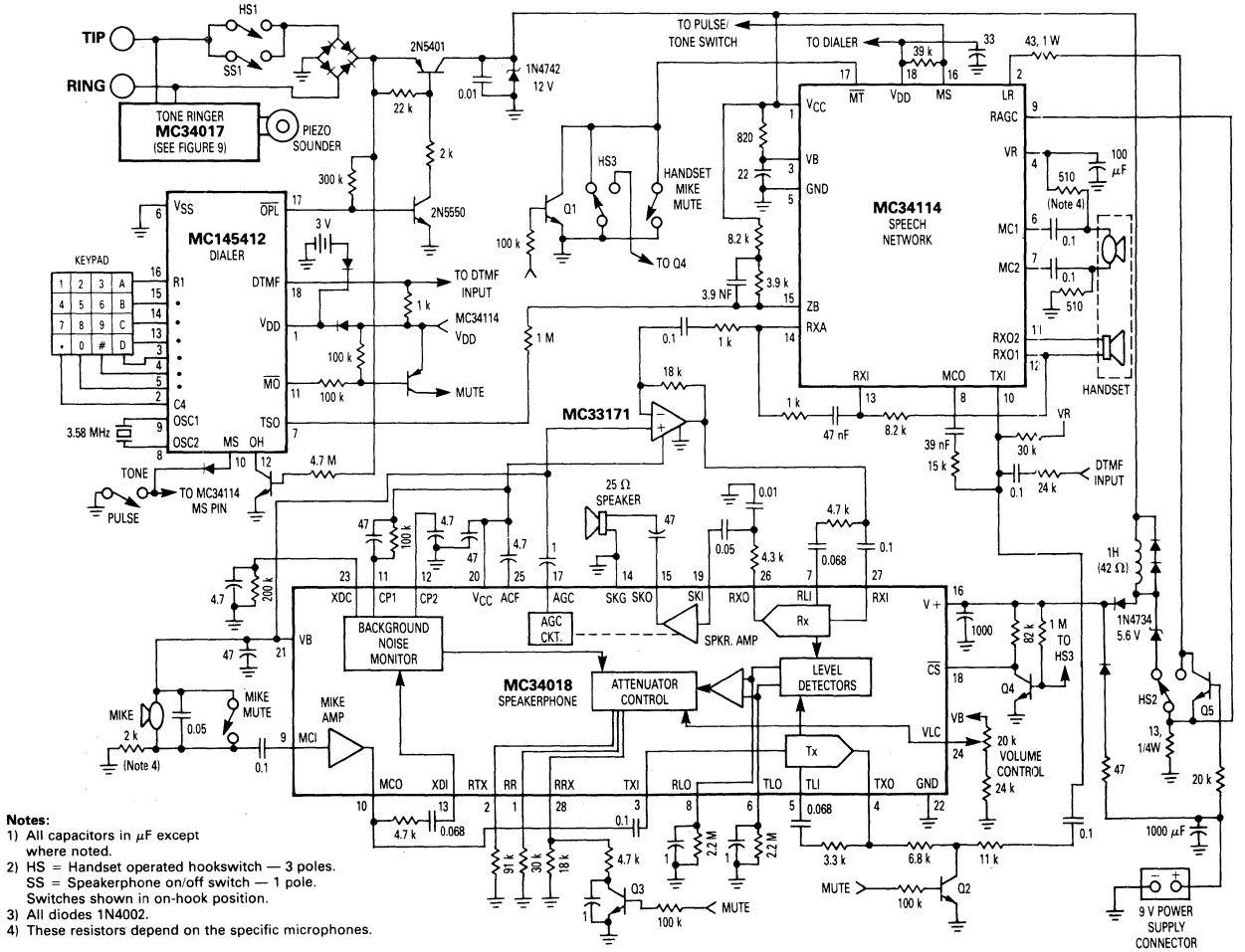
At higher loop currents, the dc characteristics of the two modes will differ slightly as some of the MC34018's current may be supplied by the loop.

Without the adapter plugged in, the circuit will act the same as that of Figure 10. Diode D2 prevents Q5 from being turned on.

In the handset mode, the circuit operates the same as that in Figure 10 when it is in the handset mode.

The Complete Circuit with the Booster

The complete circuit is shown in Figure 18. A quick comparison shows it is identical to that of Figure 10, except for the booster section in the lower right hand corner. The performance curves for this circuit are shown in Figures 19–24. As can be seen in Figures 20 and 23, the speakerphone's performance does not degrade below 30 mA as had happened in Figures 12 and 15. The muting specs for this circuit are the same as for Figure 10.



Notes:
1) All capacitors in µF except where noted.
2) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
3) All diodes 1N4002.
4) These resistors depend on the specific microphones.

Figure 18. Pulse/Tone Featurephone w/Memory — Line Powered w/Booster

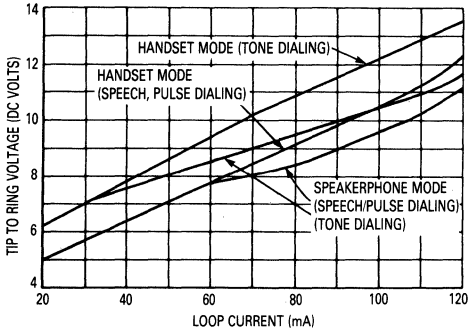


Figure 19. Tip to Ring DC Voltage versus Loop Current

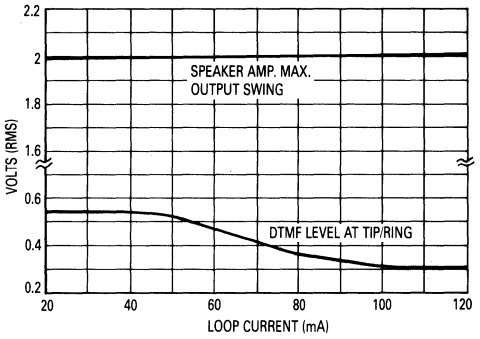


Figure 20. Max. Speaker Amplifier Output and DTMF Level versus Loop Current

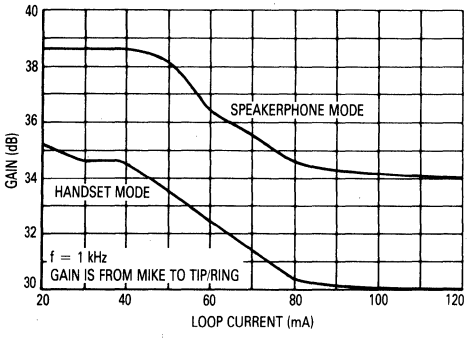


Figure 21. Transmit Gain versus Loop Current

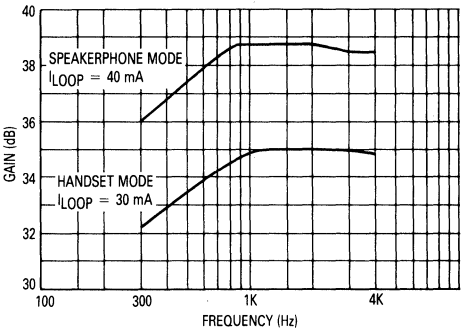


Figure 22. Transmit Gain versus Frequency

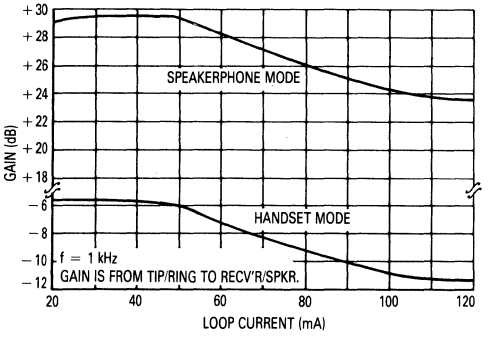


Figure 23. Receive Gain versus Loop Current

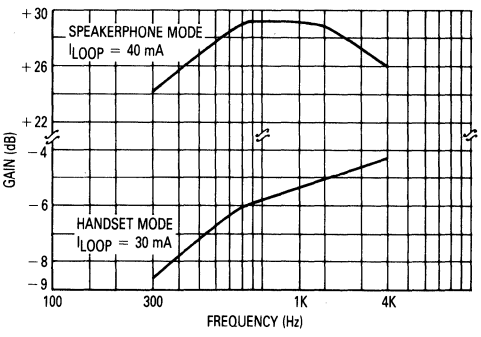


Figure 24. Receive Gain versus Frequency

USING A POWER SUPPLY INSTEAD OF LINE POWER

Using A Transformer

For those cases where it is desireable to power the featurephone from a regulated power supply, rather than from loop current, a transformer is required to provide the isolation needed between the phone line and any ac power and earth ground. The primary change to the circuit of Figure 10 is in the area of the Tip & Ring interface, as shown in Figure 25. It must be remembered that loop length compensation is not possible in this circuit since the loop current is not monitored. The MC34114's RAGC pin is grounded in this circuit, setting the transmit and receive gains to maximum.

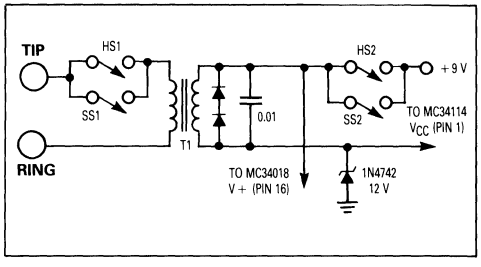


Figure 25. Tip/Ring Interface with a Power Supply

The +9 volt supply powers the MC34114 through the transformer winding. In this manner the speech signals are coupled between the MC34114 and Tip/Ring. The two diodes provide transient clamping, as does the 12 volt zener diode. The MC34018 is powered directly from the +9 volt supply, eliminating the need for the 1H choke.

The SS switch (speakerphone on/off) requires one more pole now, as shown in Figure 25. (Note: Although a +9 volt supply is shown, a lower voltage supply could be used as well.)

Changes in the Dialer and Logic Circuit

To reduce the parts count of the logic portion of the previous circuits, Q1–Q3 were replaced with logic gates. A triple 3-input AND gate, with open collector outputs (74LS15), fulfills the requirements of Tables 1 and 2. (The use of an LSTTL logic gate was not feasible in the previous two circuits due to the current consumption of the LS device.) The 5 volt power for the gates is derived from the +9 volt supply using a 1N4733 zener diode. Since the dialer's mute output drives the gate inputs, it is necessary to power the dialer from the same +5 volt supply, rather than the MC34114's V_{DD} supply. The resulting logic circuit is shown in Figure 26.

The use of the logic gate also simplifies the selection of handset versus speakerphone mode of operation. The diversion of the excess loop current is not an issue in this circuit, so the switching of that current is eliminated, along with Q4. The Mike Mute function can now be provided from a single pole switch, rather than the two pole switch of the previous circuits.

With this circuit, the handset operated switch (HS) remains a 3-pole switch.

Because of the isolation requirement, the MC145412 dialer requires a relay to break the loop current during pulse dialing. Figure 27 depicts this circuit.

The relay is normally off, and energized only for the pulse dialing function. The 1 μF capacitor (rated 250 volts min., NPO) helps absorb the transients generated during pulse dialing.

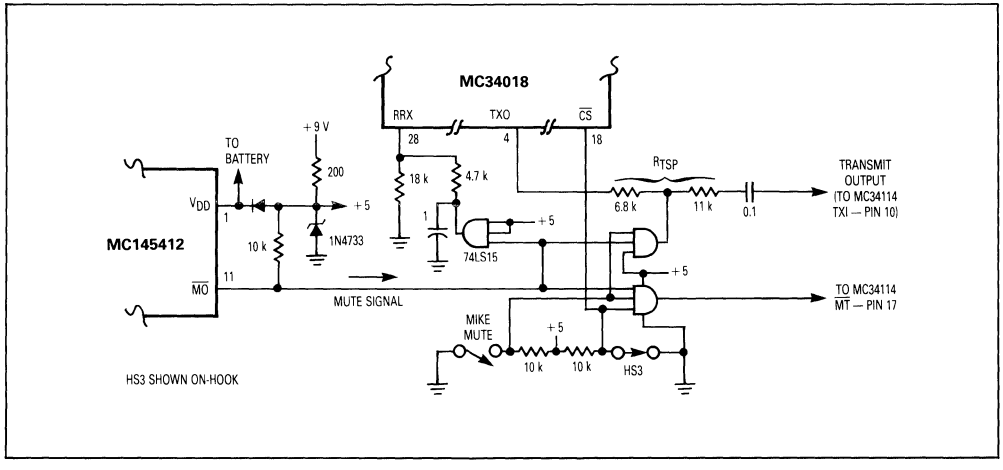


Figure 26. Switching Modes Using Logic Gates

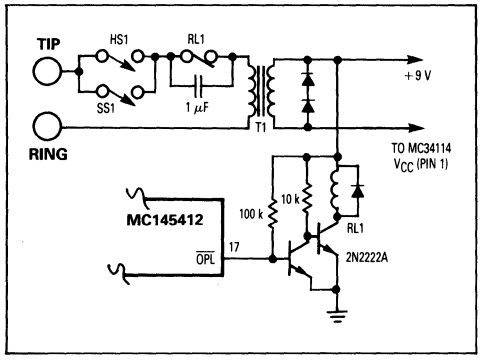


Figure 27. Pulse Dialer Circuit

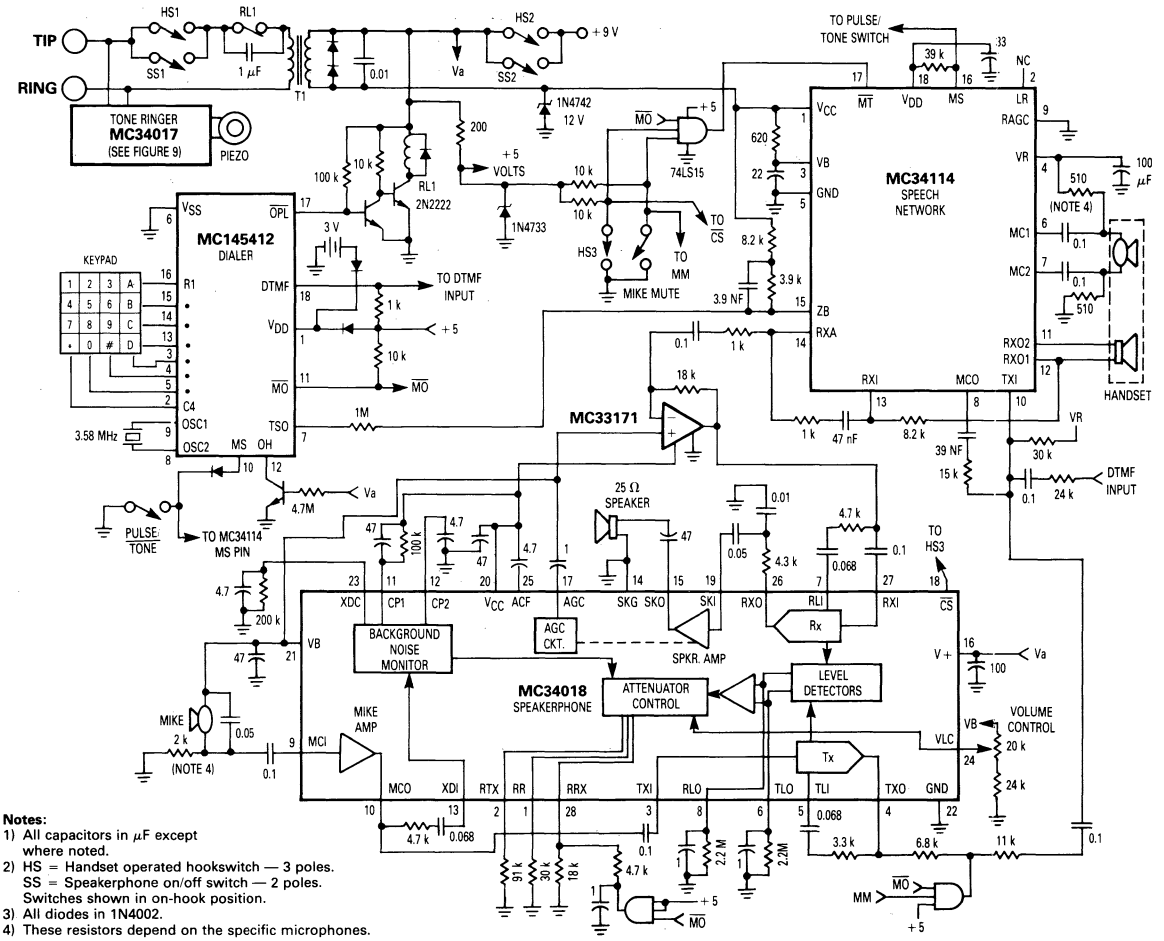
The Complete Circuit with the Power Supply

The complete circuit is shown in Figure 28. The performance curves are shown in Figures 29–34. The Tip to Ring dc voltage (Figure 29), determined solely by the dc resistance of the transformer winding, is somewhat lower than in the previous circuits. Figures 30, 31, and 33 show the performance is fairly constant with loop current, except for a slight reduction in gain at the higher currents. This is due to the characteristics of the transformer used in developing this circuit (model #TTPC-13 from Stancor, Inc.). Also noticeable in the curves, compared to Figures 11–16 and 19–24, is the lack of loop length compensation — a natural consequence of this type of circuit.

The muting specifications for this circuit are the same as for the line powered circuit. The current required from the +9 volt power supply is as follows:

a) Handset mode: ≈32 mA.
b) Speakerphone mode (no sound at the speaker): ≈41 mA.
c) Speakerphone mode (max. volume at the speaker): ≈82 mA.

Although Figure 28 indicates the use of a 25 ohm speaker, any impedance speaker within the range of 16 to 40 Ω can be used, since this circuit is not line powered. The receive gain may have to be adjusted, however, if a different speaker is used.



Notes:
1) All capacitors in μF except where noted.
2) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 2 poles.
   Switches shown in on-hook position.
3) All diodes in 1N4002.
4) These resistors depend on the specific microphones.

Figure 28. Pulse/Tone Featurephone w/Memory — Powered From a Power Supply

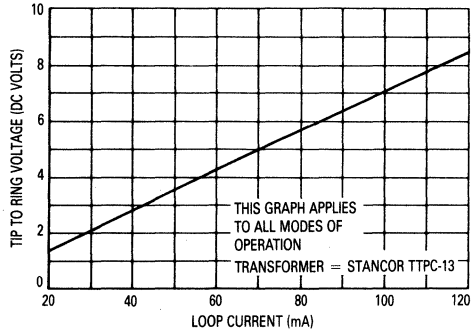


Figure 29. Tip to Ring DC Voltage versus Loop Current

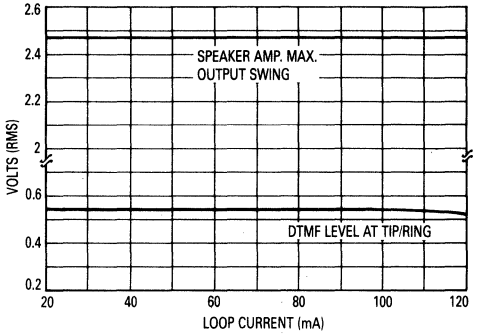


Figure 30. Max. Speaker Amplifier Output and DTMF Level versus Loop Current

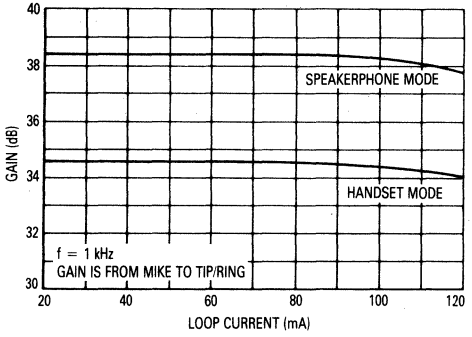


Figure 31. Transmit Gain versus Loop Current

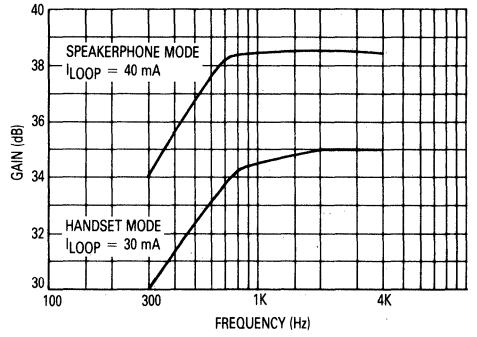


Figure 32. Transmit Gain versus Frequency

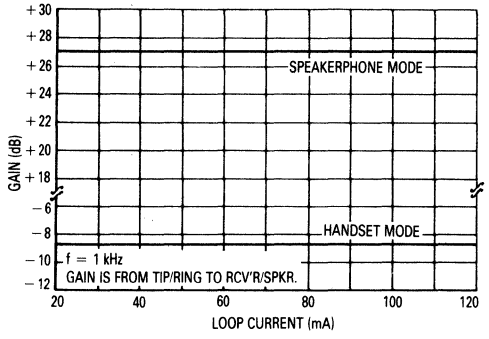


Figure 33. Receive Gain versus Loop Current

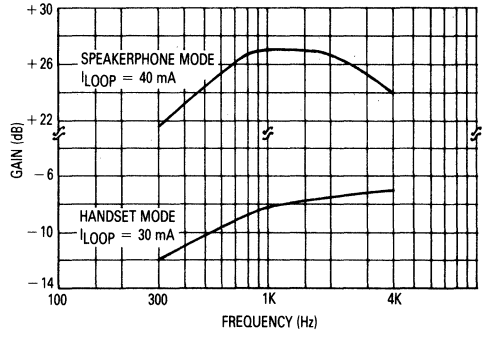


Figure 34. Receive Gain versus Frequency

CONSTRUCTION HINTS

Board Layout

The filter capacitor for the MC34018 speakerphone IC (typically 1000 μF) must be physically adjacent to Pin 16 of the IC, within 1". This is particularly important in the line-powered versions, where V_{CC} can vary with the speech intensity. Since most of the current is used in the speaker amplifier, the PC board track leading to Pin 16 of the MC34018 should be laid out with care, preferably close to the zener diode, or the power supply connector. The ground tracks should be as wide as possible, and laid out with care.

EMI Susceptibility

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the speakerphone. EMI may enter the circuit through Tip & Ring, through the microphone wiring to the amplifiers, or through any of the PC board traces. The most sensitive pins on the MC34108 are the inputs to the level detectors (RLI, TLI), since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. These board traces should be kept short, and the resistor and capacitor for each input should be physically close to the pins. Other high impedance input pins (MCI, VLC) should be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

Acoustics

a) In the design of any speakerphone, acoustics are extremely important, and **must** be considered from the very beginning. Building a breadboard with the microphone and speaker "hanging out in mid air" simply **will not work!!!** One of the most common problems in a speakerphone design is acoustic feedback (the speaker is closely coupled to the microphone) which results either in oscillations (2–10 kHz) or "motor-boating" (1–10 Hz switching). A properly designed enclosure for the finished product should provide at least 50 dB of acoustic loss (speaker drive voltage to microphone output voltage). The physical location of the microphone, along with the characteristics of the microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

b) The quality of the speaker, and the acoustic cavity in which it resides, have a major impact on the quality of the sound. A little time spent here can go a long way towards improving the sound of the finished speakerphone. As a general rule, good electronics cannot compensate for poor acoustics and/or low speaker quality.

In the Final Analysis . . .

In the final analysis, the circuits shown in this application note will have to be "fined tuned" to match the acoustics of the enclosure, and the specific microphone and speaker selected. The component values shown in this application note should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at key points in the circuits (see appropriate text). The switching response of the speakerphone can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines. The references can be consulted for additional speakerphone design theory.

GLOSSARY

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

C-Message Filter — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office — Abbreivated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 x log (P_1/P_2) for power measurements, and
20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

dBrnC0 — Noise measured in dBrnC referred to zero transmission level.

DTMF — Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four Wire Circuit — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone), and one pair is for the Receive path (generally to the receiver).

Full Duplex — A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full duplex.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half Duplex — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

Hookswitch — A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Line Length Compensation — Also referred to as loop compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop — The loop formed by the two subcriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loop Current — The dc current which flows through the subscriber loop. Typically provided by the central office or PBX, it ranges from 20 to 120 mA.

Off Hook — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On Hook — The condition when the telephone is disconnected from the phone system, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Pulse Dialing — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 times per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

REN — Ringer Equivalence Number. An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1 equals ≈8 k ohms. The Bell system typically permits a maximum of 5 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Widetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Speech Network — A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip — One of the two wires connecting to the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 Vrms, 20 Hz.

Two-Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Voiceband — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

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MC34017 Data Sheet, January, 1984, Motorola Inc.
MC34114 Product Preview Data Sheet, Sept. 1987, Motorola Inc.
MC33171 Data Sheet, February, 1988, Motorola Inc.
MC145412 Data Sheet, February, 1987, Motorola Inc.
Busala, A., Fundamental Considerations in the Design of a Voice Switched Speakerphone, B.S.T.J., 39, 1960, p. 265.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and Applications Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

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AN1003

A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC

Prepared by
Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

This application note describes how to add a handset, dialer and tone ringer to the MC34118 speakerphone circuit. Although any one of several speech networks could be used as an interface between the MC34118 and the phone line (those possibilities are discussed in separate application notes) this application note covers the case where simplicity and low cost are paramount. A "Privacy" (Mike Mute) function is included, but not pulse dialing, nor line length compensation.

Two circuits are developed in this discussion: a line-powered featurephone and one powered from a power supply. The circuits are nearly identical, except for the Tip and Ring interface. Their parameters however, differ noticeably, particularly in the low loop current range.

MC34118 DESCRIPTION

The MC34118 speakerphone IC provides all of the necessary functions for a complete speakerphone circuit, except for the speaker amplifier, in a single integrated circuit. Included are the transmit and receive attenuators, which operate in a complementary manner, to provide the half-duplex function. The four level detectors, in conjunction with the background noise monitors and the control algorithm, provide a four point sensing and decision making system to control the attenuators based on the levels and timing of the transmit and receive signals. A filter, user selectable to be high pass, low pass, or bandpass, is included for filtering either the transmit or receive signals. Additional functions include volume control for the receive path, a Mute input for the microphone amplifier and a chip disable pin. A simplified block diagram is shown in Figure 1.

Unlike many other speakerphone ICs, the MC34118 includes the hybrid amplifiers for the two-to-four wire conversion when used in conjunction with a transformer. Figure 2 depicts a basic line powered speakerphone using the MC34119 speaker amplifier. When used in parallel with any standard telephone, all of the necessary telephone functions are then provided.

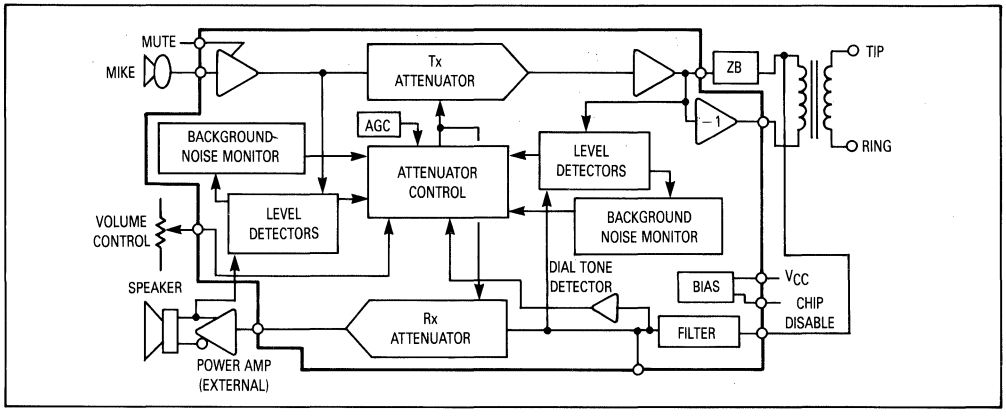


Figure 1. Simplified Block Diagram

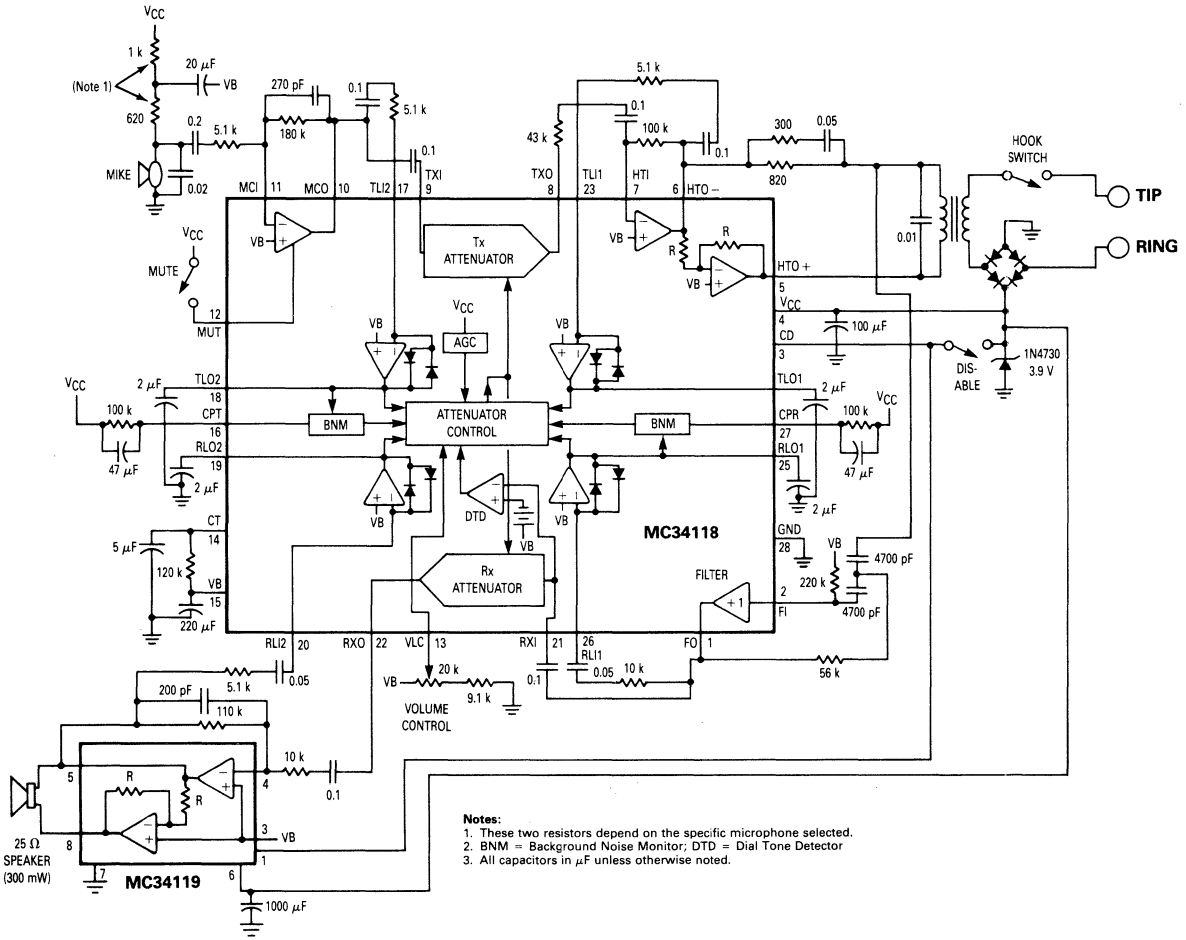


Figure 2. Basic Line-Powered Speakerphone

LINE-POWERED FEATUREPHONE

DC Characteristics

The DC characteristics of the circuit (Figure 2) are determined by the resistance of the transformer winding (Stancor TTPC-13 in this circuit development), the diode bridge and the zener diode. Using a 3.9 volt zener diode (to power the speakerphone and the various parts of the circuit) the voltage at Tip and Ring is within the EIA-470 guidelines.

With a V_{CC} of 3.9 volts, the MC34118 provides a VB voltage (Pin 15) of ≈1.6 volts. The VB voltage is used as an AC ground for the entire circuit.

Adding the Handset Microphone

The microphone used in developing this circuit was the Primo EM-95 which operates with a bias current of 500 μA to 1 mA. The bias current is obtained from the V_{CC} supply voltage, but the bias resistor is composed of two resistors, with the center tap AC coupled to VB, as shown in Figure 3. The AC output level of the microphone is determined by the 3.9 kΩ resistor, while the DC bias level is determined by the sum of the 3.9 k and 3 k resistors, and V_{CC}. The 0.047 μF capacitor provides high frequency roll-off. The AC output of the above circuit goes to Pin 7 (HTI) of the MC34118, which is the summing junction of the first hybrid amplifier. The 1 k resistor, in conjunction with the 100 k feedback resistor on the amplifier (Figure 3), sets the gain. In this way, the microphone signals are fed to Tip and Ring. The gain of this circuit can be adjusted by varying the 1 k or the 3.9 k resistor, or both. Different microphone models generally have different biasing requirements for optimum output levels.

The transistor, activated by an active high Mute signal, will shut off the microphone when it is to be inoperative, such as during dialing and during speakerphone operation.

Adding the Handset Receiver

Although the receive signals are available at the filter's output (FO, Pin 1), the low impedance of a typical receiver (100–150 Ω) requires a separate amplifier, depicted in Figure 4, to drive it. The MC33171 was chosen due to its low supply current (typically 180 μA). It is biased from VB and set for a gain of ≈0.43 (−7.3 dB). Low frequency roll-off is provided by the 0.047 μF input capacitor, as well as by the filter. High frequency roll-off is not provided since the presence of high frequencies generally make the sound "crisper" and therefore easier to understand. If roll-off is desired, simply add a capacitor across the 4.3 k feedback resistor.

The addition of the op amp facilitates providing sidetone control, which is obtained by sampling the transmit signal at HTO− (Pin 6) and using that to cancel part of the sidetone signal. The 20 k resistor and 0.02 μF capacitor provide a phase shift to compensate for the signal's phase shift at FO relative to HTO−, caused by the transformer and the line's complex impedance. The combination of the phase shift and the 10 k resistor (RS) determine the amount of sidetone cancellation.

Since the op amp is driving an inductive receiver at the end of a 2 to 3 foot cord, the 0.01 μF capacitors at the inputs are necessary for stability.

The diode provides a simple means for disabling this circuit during speakerphone operation. With "Shutoff" at ground, the amplifier is disabled.

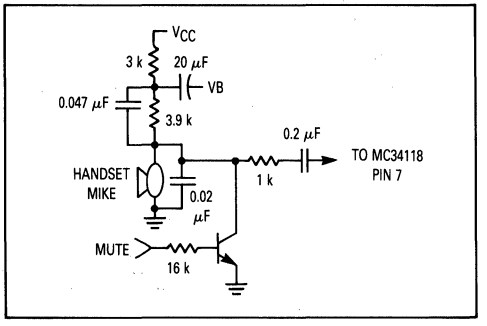


Figure 3. Handset Microphone Circuit

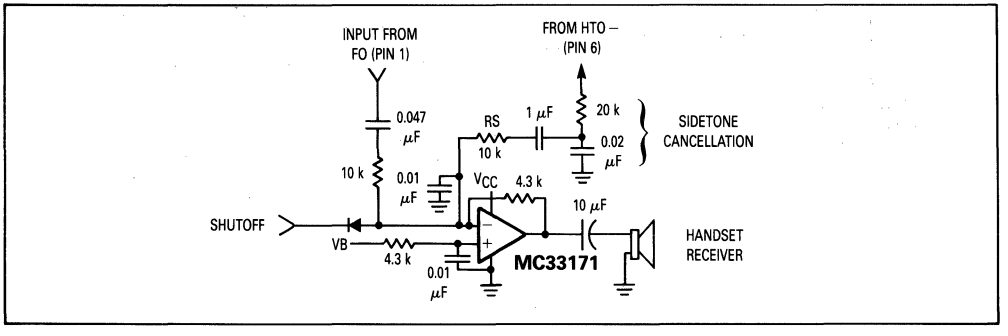


Figure 4. Handset Receiver Circuit

Adding the Dialer

The dialer is the MC145412 pulse/tone dialer with 10 number memory. Since the pulse dialing function is not used, the MS pin is grounded and the OPL (Outpulsing) and TSO (Pacifier tone) outputs are not used. The circuit uses a standard 3.58 MHz crystal and standard 3 x 4 or 4 x 4 keypads.

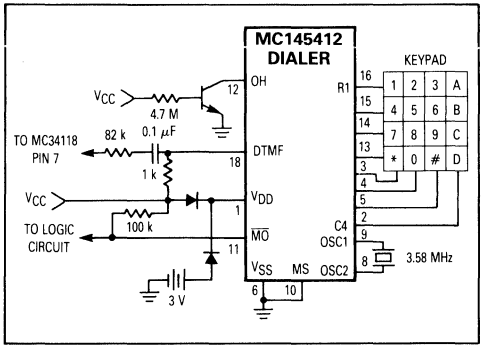


Figure 5. Dialer Circuit

Referring to Figure 5, the NPN transistor at Pin 12 indicates the on-hook/off-hook status to the IC. Power for the dialer is V_{CC}, diode connected with a memory sustaining battery. The DTMF output goes to Pin 7 (HTI) of the MC34118, which is the summing junction of the first hybrid amplifier. The 82 k resistor, in conjunction with the 100 k feedback resistor on the amplifier, determines the gain. With the values shown, the DTMF output at Tip and Ring is approximately 550 mVrms (−3 dBm). To change the output level, vary the 82 k resistor appropriately.

The Mute Output ($\overline{MO}$) is active low, open drain and pulls to ground while dialing. It is used to mute the speech paths during dialing.

Switching the Circuit Around

The logic functions involve: a) switching the circuit from handset mode to/from speakerphone mode, b) switching in and out of the dialing mode while in either handset or speakerphone mode and c) muting the two microphones for the "Privacy" function. Table 1 tabulates the requirements:

Table 1.

	Handset		Speakerphone	
Function	**Mike**	**R'cvr**	**Mike**	**Speaker**
Handset Speech	On	On	Off	Off
Handset Dialing	Off	Mute	Off	Off
Handset Mike Mute	Off	On	Off	Off
Speakerphone Speech	Off	Off	On	On
Speakerphone Dialing	Off	Off	Off	Mute
Speakerphone Mike Mute	Off	Off	Off	On

In Table 1, "ON" means fully functional, "OFF" means non-functional and "MUTE" means partially muted (10 to 20 dB).

To provide the logic functions and with the intent of keeping the number of mechanical switches to a minimum and simplicity at an optimum, an MC14023 triple 3-input CMOS NAND gate was used. See Figure 6.

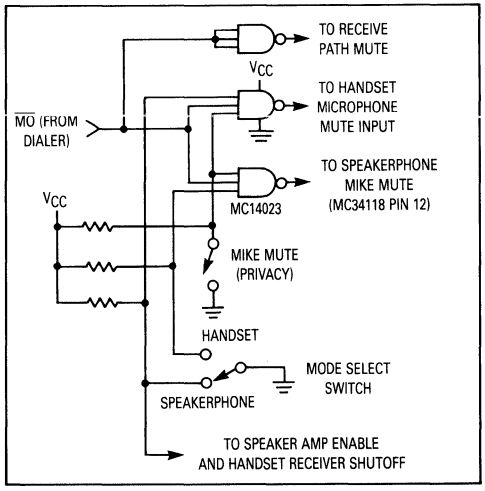


Figure 6. Logic Circuit

The inputs are the Mute Output ($\overline{MO}$) from the dialer (described above), the Mike Mute switch and the Mode Select switch. The outputs are:

1. An active low output which enables the MC34119 speaker amplifier (at its Pin 1) and disables the handset receiver;
2. An active high output which disables the speakerphone microphone at the MC34118's Pin 12 (MUT);
3. An active high output which disables the handset microphone;
4. An active high output which partially mutes the receive path during dialing. The circuit which does the partial muting is shown in Figure 7.

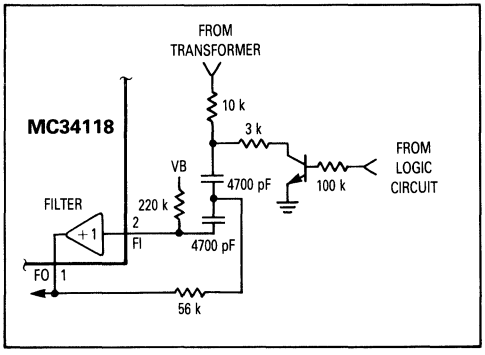


Figure 7. Receive Path Muting

The muting circuit, consisting of the transistor and the 3 k and 10 k resistors, is inserted in the line from the transformer to the filter. Normally the transistor is off and the 10 k resistor has little effect on the circuit due to the high input impedance of the filter (>200 kΩ @ 1 kHz). When Mute is asserted, the signal to the filter is muted by ≈12.7 dB.

The MC34118's Disable pin (Pin 3) is hard wired to ground since the MC34118 must be functional for both the speakerphone and handset modes.

Adding the Tone Ringer

The MC34017 tone ringer circuit, shown in Figure 8, is added to the circuit by simply connecting it across Tip and Ring. It is not necessary to disconnect the tone ringer when off-hook. This circuit will provide a ringer with an REN of ≈1 and meet all the EIA-470 and Bell System requirements for impedance, anti-bell tapping and turn-on/off thresholds.

Finally, the Complete Circuit

The complete line-powered featurephone is shown in Figure 9. HS1 and HS2 are the two poles of the hook-switch activated by lifting the handset off-hook (HS2 is the Mode Select Switch of Figure 6). SS1 is a single pole switch which, when closed (and the handset is on-hook), powers up the circuit into the speakerphone mode. Should the handset be taken off-hook, the circuit reverts to the handset mode.

The performance curves for the circuit are shown in Figures 10–15. The "Speaker Amp Max Output Swing" is the maximum rms voltage available across pins 5 and 8 of the MC34119 without noticeable clipping. The transmit gain tests involved replacing each microphone with a signal generator and adjusting for a level of approximately −11 dBm at Tip and Ring into a 600 Ω resistive load. The receive tests involve applying approximately −27 dBm to Tip and Ring, and measuring the gain to the receiver or speaker.

As can be seen in Figure 11, the maximum available speaker power is a function of the loop current since all of the speaker current must come from the loop. Consequently, the receive gain for the speakerphone (Figure 14) shows a marked decrease at low loop currents. It must be remembered that in a line powered speakerphone, as the speaker draws current in response to a receive signal, the voltage at Tip and Ring decreases quickly. As V_{CC} falls with the Tip and Ring voltage, not only is the speaker amp's output capability reduced, but the MC34118's AGC circuit automatically reduces the receive gain as V_{CC} falls below 3.5 volts. This feature prevents slow oscillations (motor-boating) due to the speaker's current demands. A 25 Ω speaker is recommended as this makes the best use of the power available from the phone line. A lower impedance speaker will require more current, causing V_{CC} to sag further for a given signal level. A higher impedance speaker draws less current, but produces less sound power.

The slight degradation of DTMF levels in Figure 11 and in the transmit levels in Figure 12, at higher loop currents is a function of the transformer's performance at those current levels.

Additionally, the following muting specs apply:

1. **Handset microphone:** ≈37 dB while dialing, in speakerphone mode, or when Mike mute switch is closed.
2. **Speakerphone microphone:** >60 dB while dialing or due to Mike Mute switch, plus an additional 52 dB due to the MC34118 switching to the receive mode. >60 dB while in the handset mode.
3. **Handset receiver:** ≈12.7 dB while dialing, ≈45 dB when in the speakerphone mode.
4. **Speaker:** ≈12.7 dB while dialing, >100 dB when in handset mode.

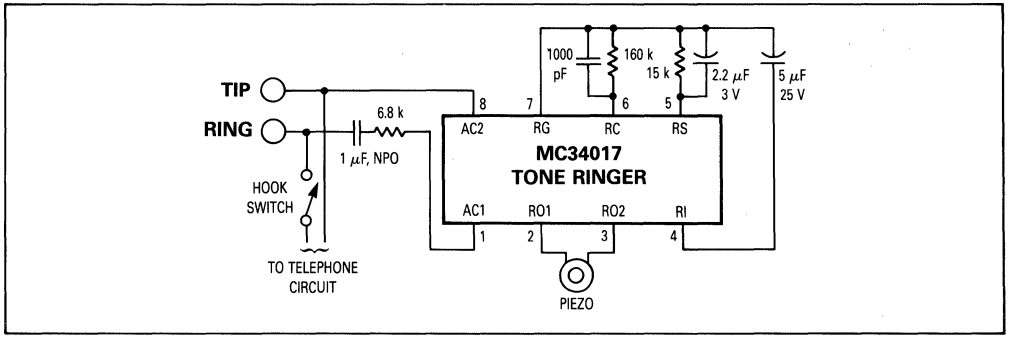
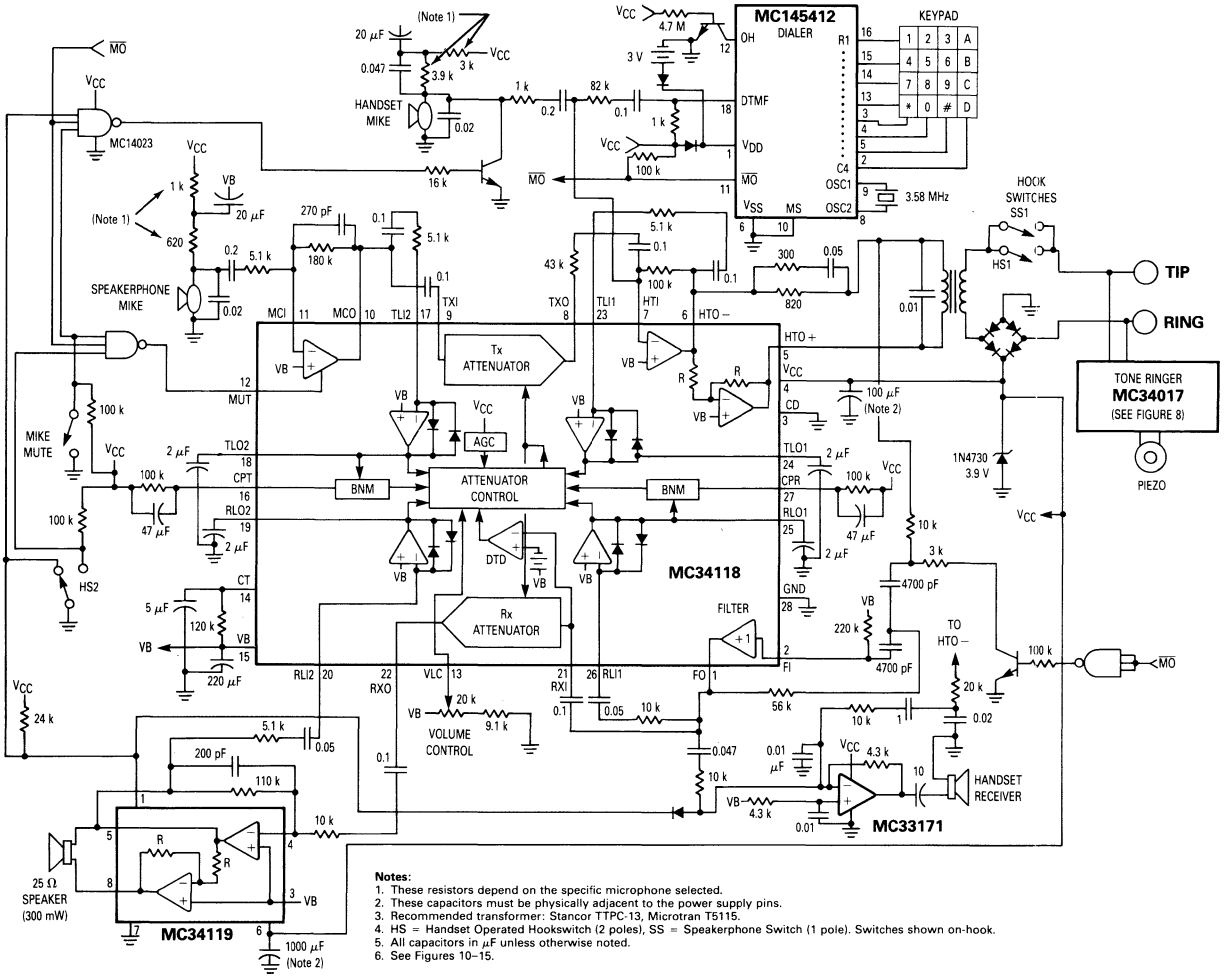


Figure 8. Tone Ringer Circuit



Notes:
1. These resistors depend on the specific microphone selected.
2. These capacitors must be physically adjacent to the power supply pins.
3. Recommended transformer: Stancor TTPC-13, Microtran T5115.
4. HS = Handset Operated Hookswitch (2 poles), SS = Speakerphone Switch (1 pole). Switches shown on-hook.
5. All capacitors in μF unless otherwise noted.
6. See Figures 10–15.

Figure 9. Line-Powered Featurephone

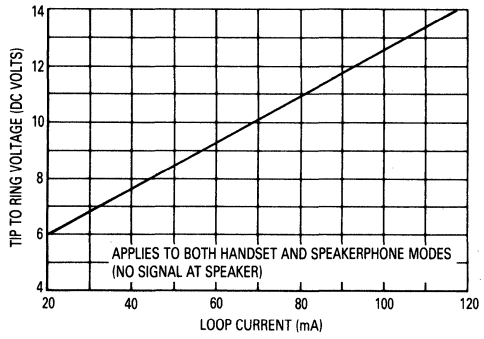


Figure 10. Tip to Ring DC Voltage versus Loop Current

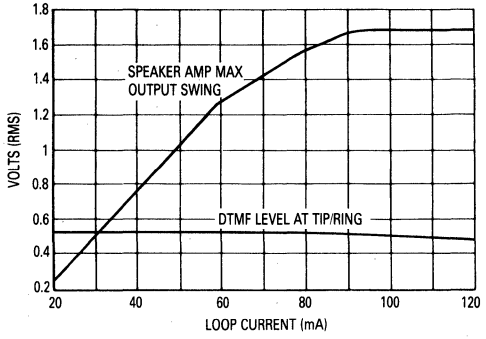


Figure 11. Speaker Amp. Output and DTMF Level versus Loop Current

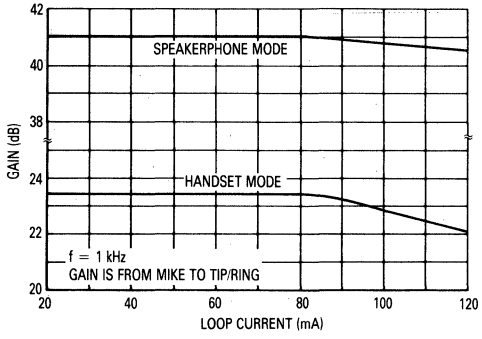


Figure 12. Transmit Gain versus Loop Current

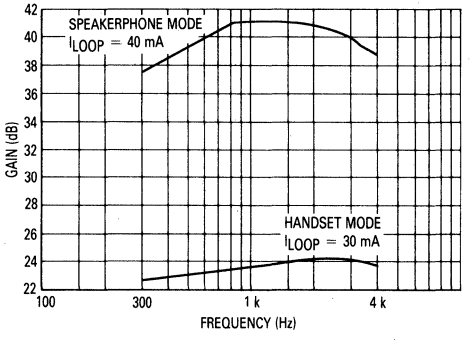


Figure 13. Transmit Gain versus Frequency

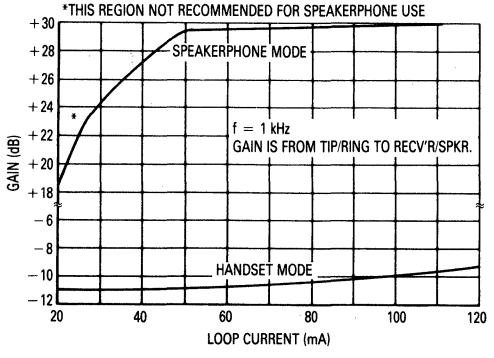


Figure 14. Receive Gain versus Loop Current

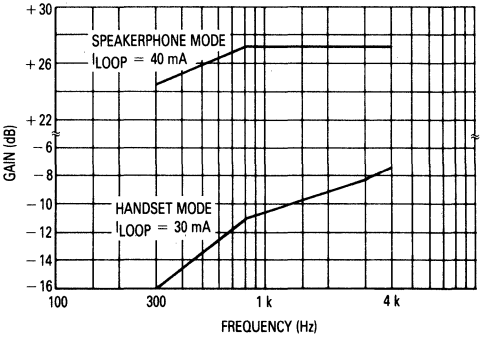


Figure 15. Receive Gain versus Frequency

USING A POWER SUPPLY INSTEAD OF LINE POWER

Figure 16 shows the circuit of Figure 9 modified for use with a +5 volt power supply. The only changes are at the Tip and Ring interface where the zener diode and bridge have been eliminated, but the two hook switches (HS and SS) require one more pole each. The transformer is used to pass the speech signals and to provide the required isolation.

Current required from the +5 volt power supply is as follows:

1. Handset speech mode: 6 mA.
2. Handset dialing mode: 11 mA
3. Speakerphone speech mode (no speech signals): 9 mA.
4. Speakerphone receive mode, −27 dBm at Tip and Ring: 51 mA.
5. Speakerphone receive mode, −9 dBm at Tip and Ring: 100 mA.
6. Speakerphone dialing mode: 19 mA.

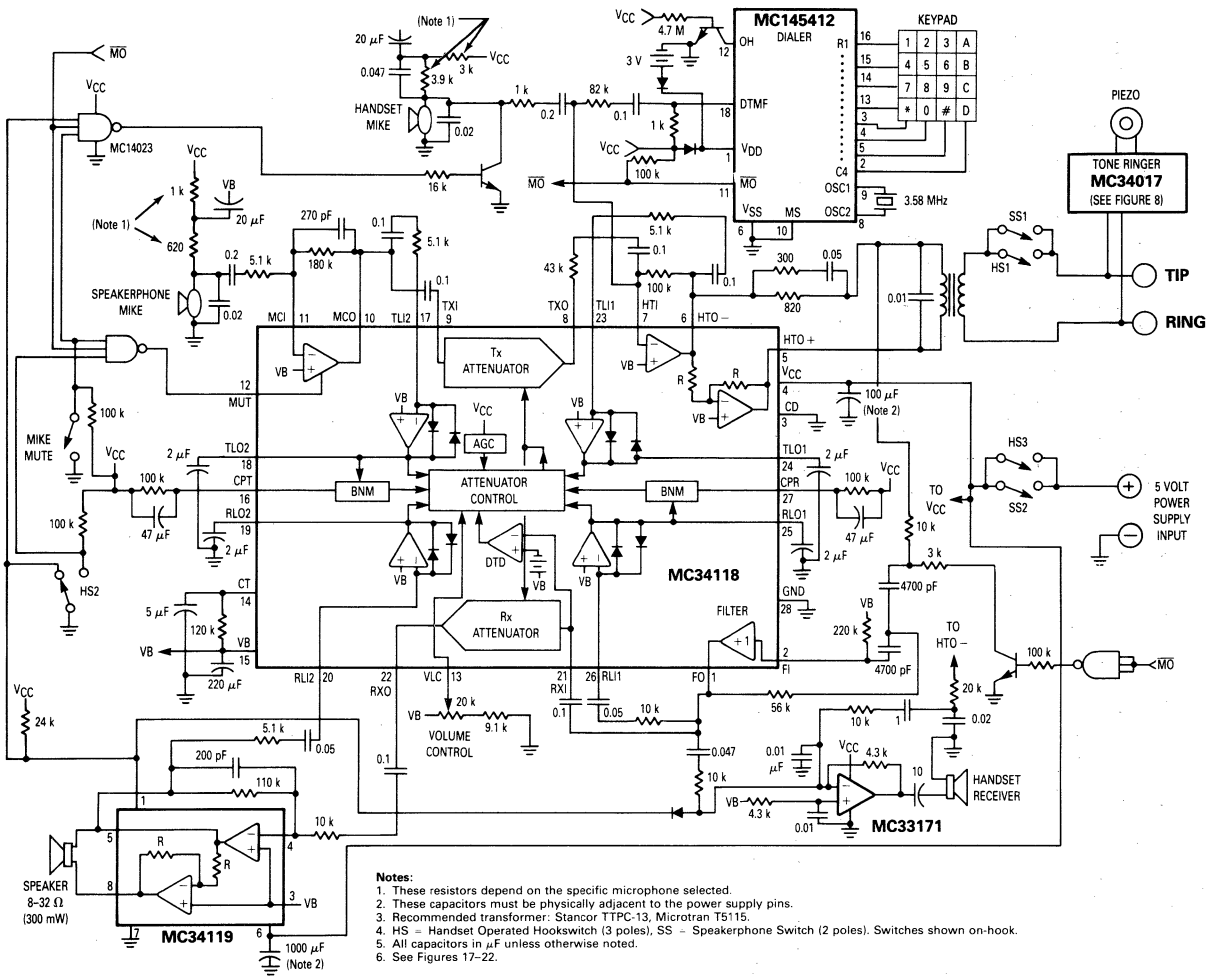
Items 4, 5 and 6 above were measured with a 25 Ω speaker and the volume control set to maximum.

The performance characteristics are shown in Figures 17–22. The Tip and Ring DC voltage (Figure 17) is now a function only of the transformer winding resistance and so is somewhat lower than in the previous circuit.

The speakerphone performance (Figures 18 and 21) is now constant with respect to loop current since V_{CC} is fixed. Performance at 20 mA is similar to that at higher loop currents, unlike the previous circuit. Although the speaker can be 25 Ω as in the previous circuit, it need not be since the available power is not limited as before. The recommended range for speaker impedance is 8–32 Ω. For different speaker impedances, however, the gain of the speaker amplifier may have to be changed to compensate for the different power level.

The slight degradation in the transmit curves at high loop currents is evident in Figures 18 and 19, as was in the previous circuit.

The muting specs of the transmit and receive paths are the same for this circuit as for the previous one.



Notes:
1. These resistors depend on the specific microphone selected.
2. These capacitors must be physically adjacent to the power supply pins.
3. Recommended transformer: Stancor TTPC-13, Microtran T5115.
4. HS = Handset Operated Hookswitch (3 poles), SS = Speakerphone Switch (2 poles). Switches shown on-hook.
5. All capacitors in μF unless otherwise noted.
6. See Figures 17–22.

Figure 16. Featurephone With Power Supply

MC34118 Featurephone With Power Supply

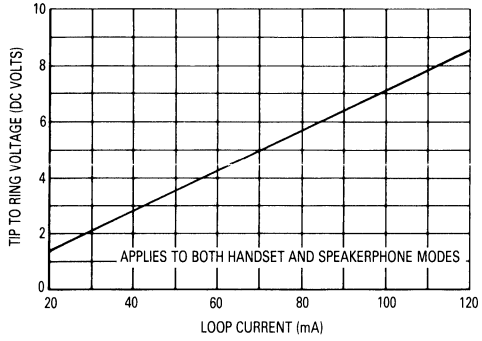


Figure 17. Tip to Ring DC Voltage versus Loop Current

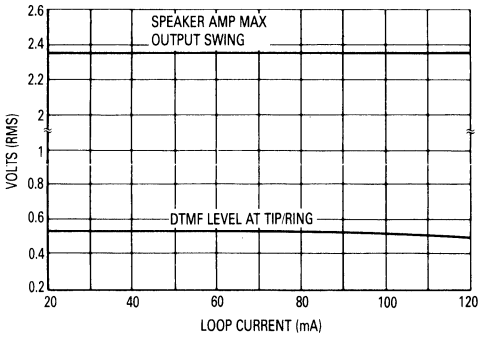


Figure 18. Speaker Amp. Output and DTMF Level versus Loop Current

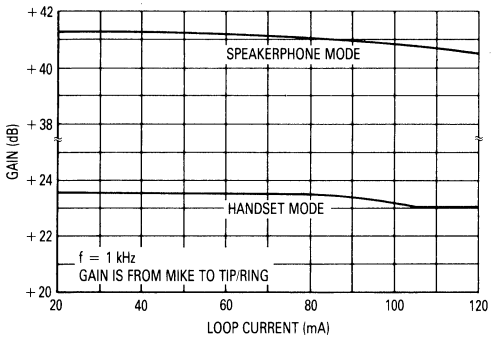


Figure 19. Transmit Gain versus Loop Current

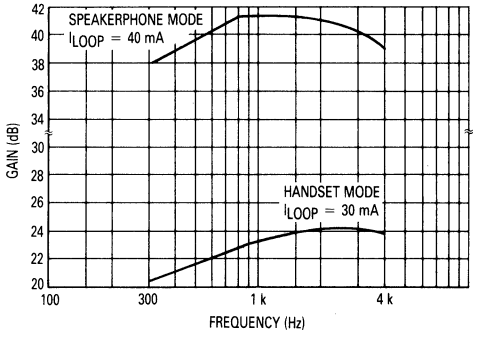


Figure 20. Transmit Gain versus Frequency

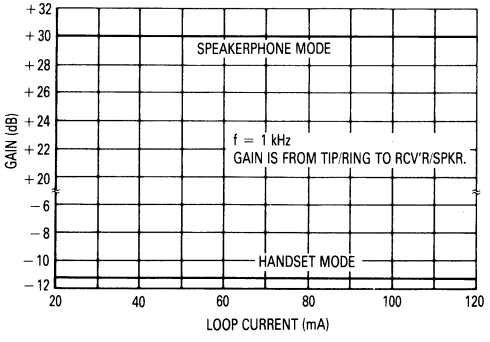


Figure 21. Receive Gain versus Loop Current

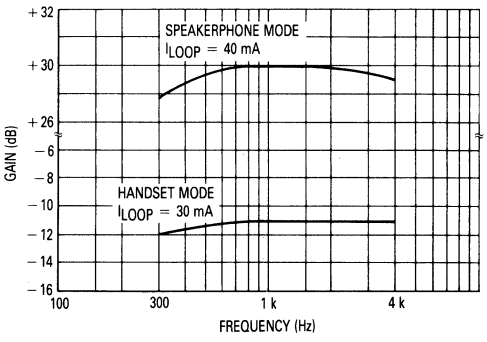


Figure 22. Receive Gain versus Frequency

CONSTRUCTION HINTS

Board Layout

The filter capacitors for the speakerphone IC and the speaker amplifier IC (100 μF and 1000 μF respectively) must be physically adjacent to the pins of the ICs, within 1". This is especially important in the line-powered version, where V_{CC} varies with the speech intensity. Since most of the current is used in the speaker amp, the PC board track leading to Pin 6 of the MC34119 should be laid out with care, preferrably close to the zener diode, or the power supply connector. The ground tracks should be as wide as possible, and laid out with care.

RFI Interference

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the amplifiers, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1 and TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. These board traces should be kept short and the resistor and capacitor for each input should be physically close to the pins. Other high impedance input pins (MCI, HTI, FI and VLC) should be considered sensitive to RFI signals.

The microphone wires within the handset cord can act as an antenna and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

Acoustics

a. In the design of any speakerphone, acoustics are extremely important and **must** be considered from the very beginning. Building a breadboard and having the microphone and speaker "hanging out in mid air" simply **will not work!** One of the most difficult problems in a speakerphone design is acoustic feedback (the speaker talks to the microphone) which results either in oscillations (2–10 kHz) or "motor-boating" (1–10 Hz switching). A properly designed enclosure for the finished product should provide at least 50 dB of acoustic loss (speaker voltage to microphone output voltage). The physical location of the microphone, along with the characteristics of the microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

b. The quality of the speaker and the acoustic cavity in which it resides, have a major impact on the quality of the sound. A little time spent here can improve the sound of the finished speakerphone. As a general rule, good electronics cannot compensate for poor acoustics and/or low speaker quality.

In The Final Analysis . . .

In the final analysis, the circuits shown in this application note will have to be "fine tuned" to match the acoustics of the enclosure and the specific microphone and speaker selected. The component values shown in this application note should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphones and speaker/receiver amplifiers, respectively. The switching response of the speakerphone can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines. The MC34118 data sheet should be consulted for additional speakerphone design theory.

GLOSSARY

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

C-Message filter — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office — Abbreviated CO, it is a main telephone office, usually within of a few miles of its subscribers, that houses switching gear for interconnection within its exchange area and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 x log (P_1/P_2) for power measurements and
20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

dBrnCO — Noise measured in dBrnC referred to zero transmission level.

DTMF — Dual Tone MultiFrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four wire circuit — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone) and one pair is for the Receive path (generally to the receiver).

Full duplex — A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full duplex.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

Half duplex — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches and voice activated speakerphones, are half duplex.

Hookswitch — A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Line length compensation — This is also referred to as loop compensation. It involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loop Current — The dc current which flows through the subscriber loop. Typically provided by the central office or PBX, it ranges from 20 to 120 mA.

Off hook — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On hook — The condition when the telephone is disconnected from the phone system and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. This is a customer owned switching system servicing the phones within a facility. It is in effect, a miniature central office. A portion of the PABX connects to the Bell (or other local) telephone system.

Pulse dialing — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed and the interruption rate is typically 10 times per second. The old rotary phones and many new pushbutton phones, use pulse dialing.

REN — Ringer Equivalence Number. This is an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. A REN of 1 equals ≈8 k ohms. The Bell system typically permits a maximum of 5 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Ring — This is one of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as being necessary for a person to be able to speak properly while using a handset.

Speech network — A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control and in many cases, the dc loop current interface.

Subscriber Line — This is the system consisting of the user's telephone, the interconnecting wires and the central office equipment dedicated to that subscriber. It is also referred to as a loop.

Tip — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 Vrms, 20 Hz.

Two wire circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Voiceband — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

REFERENCES

MC34118 Data Sheet, April, 1987, Motorola Inc.
MC34119 Data Sheet, October, 1986, Motorola Inc.
MC33171 Data Sheet, July, 1985, Motorola Inc.
MC145412 Data Sheet, February, 1987, Motorola Inc.
Busala, A., Fundamental Considerations in the Design of a Voice Switched Speakerphone, B.S.T.J., 39, 1960, p. 265.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and applications Bulletin F232

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700
Various models — ask for catalog

Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

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AN1004

A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs

Prepared by
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INTRODUCTION

This application note describes the procedure for combining the MC34114 speech network with the MC34118 speakerphone circuit into a featurephone which includes the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function and line length compensation for both handset and speakerphone operation.

Three circuits are developed in this discussion: a line-powered featurephone, a line-powered featurephone with a booster (for using the speakerphone on long lines), and one powered from a power supply. The circuits are nearly identical, except for the Tip and Ring interface. Their performance however, differs noticeably, particularly in the low loop current range. Initially, the discussion will focus on the line-powered circuit.

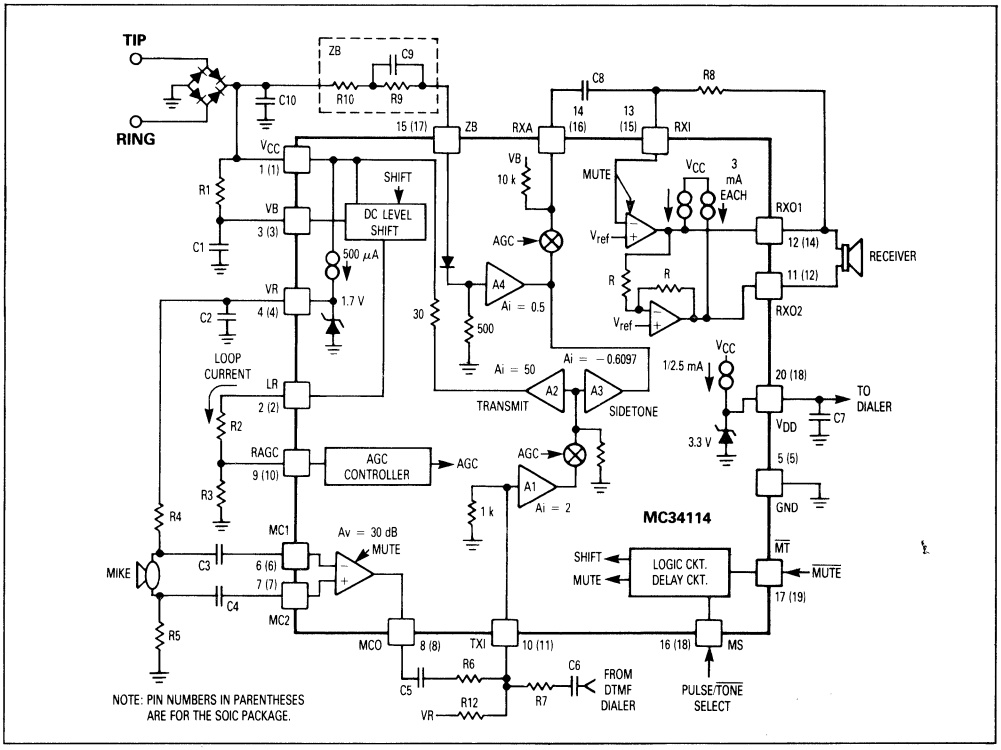


Figure 1. MC34114 Block Diagram

DESCRIPTION OF THE BUILDING BLOCKS

NOTE: Several pins on the ICs used in this application note have identical nomenclature (V_{CC}, VB, TXI, MS, V_{DD} and RXI). They provide separate functions, and are not to be connected together unless so noted.

MC34114 Speech Network

The MC34114 is a speech network which interfaces with Tip and Ring, and provides the 2-to-4 wire conversion (see Figure 1). The transmit gain is determined by the microphone amplifier (fixed gain of 30 dB), R6, C5, the internal current gains of A1, A2, the AGC, and the line impedance in parallel with R1. The receive gain is determined by ZB, the internal current gains of A4 and the AGC, C8 and R8. The sidetone cancellation is determined by A3 and the ZB network. The AGC points have a current gain of 1 at low loop current, and decrease to 0.5 (−6 dB) at higher loop currents, thus providing line length compensation. R1 (typically 600 Ω) sets the circuit's terminating impedance for ac (return loss) purposes.

The $\overline{\text{MUTE}}$ input (when low) disables the microphone amplifier, and partially mutes the receive amplifier (with an internal 1 k feedback resistor), when dialing. DTMF dialing signals are injected at TXI through R7 and C6. The Mode Select (MS) input (when low, and $\overline{\text{MT}}$ is low) provides a voltage boost at V_{CC} to ensure adequate voltage during DTMF dialing at low loop currents. The 3.3 volt regulated output (V_{DD}) powers the dialer, and the 1.7 volt regulated output (VR) is used to bias the microphone.

The dc characteristics at Tip and Ring are determined by the diode bridge (1.4 volts), a level shift of approximately 2.9 volts from V_{CC} to LR, and the voltage across R2 + R3 (typically 43 Ω and 13 Ω). All the loop current, minus ≈10 mA, flows through those two resistors. The level shift (V_{CC} − LR) increases to ≈3.9 volts when both $\overline{\text{MUTE}}$ and MS are low (tone dialing mode). The voltage at RAGC, when within the range of 0.5 to 1 volt, controls the internal AGC as a function of loop current.

MC34118 Speakerphone

The MC34118 speakerphone IC (see Figure 2) provides all the necessary functions for a complete speakerphone circuit in a single integrated circuit. Included are the transmit and receive attenuators, which operate in a complementary manner, to provide the necessary half-duplex function. The four level detectors, in conjunction with the two background noise monitors and control algorithm, provide a four point sensing and decision making system to control the attenuators based on the levels and timing of the transmit and receive signals. Additional functions include the microphone amplifier, a Mute input for the microphone amplifier, volume control for the receive path, a filter, and a Chip Disable pin. The gain of the receive attenuator, normally +6 dB at max. volume, is reduced by the AGC circuit as V_{CC} falls below 3.5 volts to control the amount of voltage sag in a line powered application. The component values shown are typical.

Connections to the MC34118 circuit are made to several points around the circuit as follows:

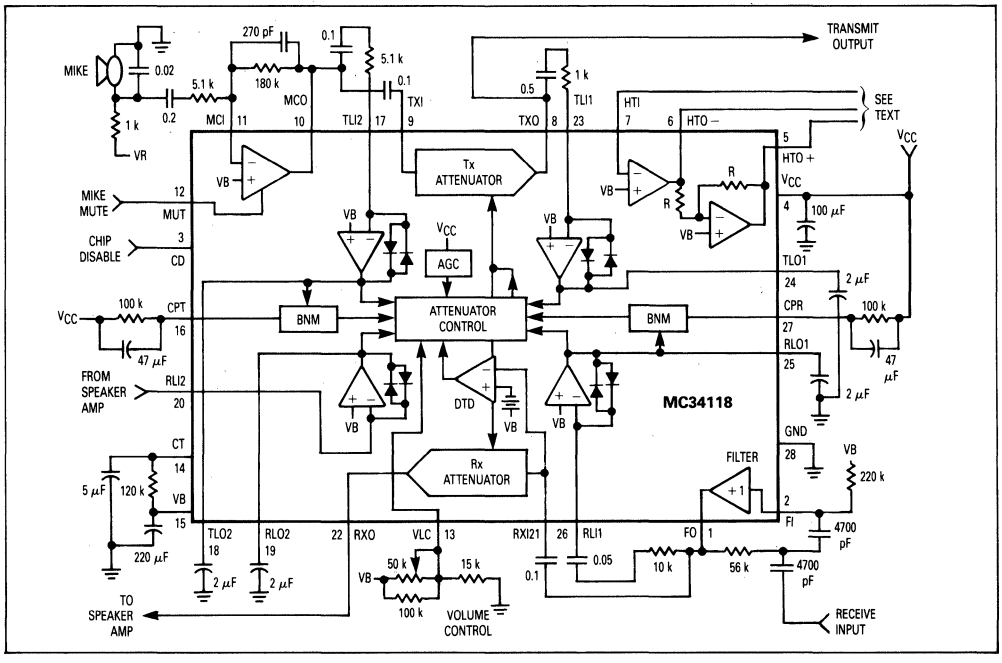


Figure 2. MC34118 Block Diagram

The TRANSMIT OUTPUT (upper right) connects to the 4 wire side of the speech network. The transmit gain, from the microphone to TRANSMIT OUTPUT, is +37 dB (+31 dB in the mike amp, +6 dB in the Tx attenuator), and does not vary with the volume control. In the receive mode, the transmit gain is ≈ −15 dB.

The RECEIVE INPUT (lower right) is derived from the 4 wire side of the speech network. The gain from RXI to RXO is +6 dB when in the receive mode at maximum volume. At minimum volume, the attenuator's gain reduces by ≈46 dB, for an overall gain of −40 dB. In the transmit mode, the gain is ≈ −46 dB. Pins 22 (Receive out) and 20 (Receive level detector input) connect to the external speaker amplifier (MC34119).

The overall speakerphone's transmit and receive gains to and from Tip and Ring are adjusted at the mike and speaker amplifier and at the 4-wire interface.

The MIKE MUTE input disables the mike amplifier when at a logic high. Chip Disable disables the MC34118 when at a logic high, reducing the MC34118's supply current from a normal ≈5.5 mA to ≈600 μA.

The two op amps (pins 5, 6, 7) are available for a variety of uses. Figure 23 of the MC34118 data sheet, for example, indicates their use with a transformer to form a stand-alone speakerphone. Later in this application note however, they will be used with the MC34114 as part of the receive path.

V_{CC} (Pin 4) is the power supply input, requiring 3 − 6.5 volts @ ≈5.5 mA. The 100 μF capacitor must be physically adjacent to pin 4 in the board layout to prevent oscillations.

VB is the ac ground for the IC, and must be well filtered, as shown.

MC34119 Speaker Amplifier

The MC34119 (Figure 3) is a 400 mW speaker amplifier, capable of 500 mW peaks. With a supply voltage range down to 2 volts, it is well suited for speakerphone applications. The gain is adjustable from less than 0 dB (it is unity gain stable) to a maximum of ≈46 dB to cover the voiceband. It provides a differential output to the speaker, eliminating the bulky series capacitor normally needed with single-ended outputs. Additionally, the device has a Chip Disable pin which, when taken high, sets the outputs to a high impedance state.

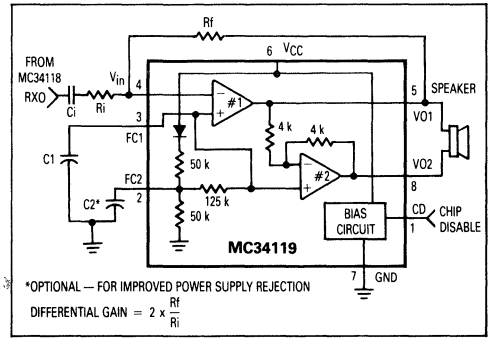


Figure 3. Speaker Amplifier

The dc supply at V_{CC} must be well filtered to prevent oscillations when the speaker amplifier is operating. In a typical line powered circuit, an inductor (1H) is used, in conjunction with a 1000 μF capacitor at V_{CC}, to filter the voltage derived from the loop current. Capacitors C1 and C2 shown in Figure 3 are not used in this application. Instead, bias is provided to Pin 3 from the MC34118's VB pin.

MC145412 Dialer

The dialer is a pulse/tone dialer with 10 number memory, including last number redial (Figure 4). The pulse/tone functions are selectable at Pin 10 (MS). The circuit uses a standard 3.58 MHz crystal, and a standard 3x4 or 4x4 keypad.

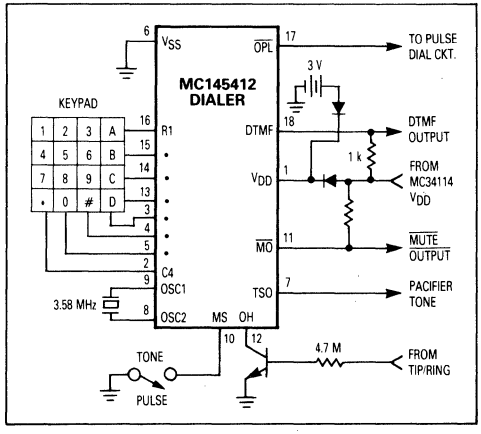


Figure 4. Pulse/Tone Dialer

The NPN transistor at Pin 12 indicates the on-hook/off-hook status to the IC. Power for the dialer is the MC34114's V_{DD} (3.3 volts), diode connected with a memory sustaining battery. The DTMF output goes to C6/R7 of Figure 1.

The OPL (OUTPULSING) pin is used to interrupt the loop current when pulse dialing. The pin is an active low open drain. TSO (Tone Signal Output) provides a 500 Hz pacifier tone during pulse dialing. The tone is a square wave, which swing from V_{DD} to V_{SS}.

The Mute Output (MO) is active low, open drain and pulls to ground while dialing. It is used to mute the speech paths during dialing.

SWITCHING THE CIRCUIT AROUND

The logic functions involve: a) switching the circuit from handset mode to and from speakerphone mode, b) switching in and out of either dialing mode while in either handset or speakerphone mode, and c) muting the two microphones for the "Privacy" function. Table 1 tabulates the fundamental requirements applicable to any featurephone:

Table 1.

Function	HANDSET		SPEAKERPHONE	
	Mike	R'cvr	Mike	Speaker
Handset Speech	On	On	Off	Off
Handset Dialing	Off	Mute	Off	Off
Handset Mike Mute	Off	On	Off	Off
Speakerphone Speech	Off	Off	On	On
Speakerphone Dialing	Off	Off	Off	Mute
Speakerphone Mike Mute	Off	Off	Off	On

In Table 1, "ON" means fully functional, "OFF" means non-functional, and "MUTE" means partially muted (10 to 20 dB). To apply Table 1 to the specific ICs described previously, the requirements are expanded in Table 2:

Table 2.

Function	MC34114		MC34118		MC34119	Loop	MC145412
	$\overline{MT}$	MS	CD	MUT	CD	Current	MS
Handset Speech	Hi	X	Hi	X	Hi	Thru MC34114	X
Handset Pulse Dialing	Lo	Hi	Hi	X	Hi	Thru MC34114	Open
Handset Tone Dialing	Lo	Lo	Hi	X	Hi	Thru MC34114	Gnd
Handset Mike Mute	Lo	X	Hi	X	Hi	Thru MC34114	X
Speakerphone Speech	Lo	X	Lo	Lo	Lo	To MC34119	X
Speakerphone Pulse Dialing	Lo	Hi	Lo	Hi	Lo	To MC34119	Open
Speakerphone Tone Dialing	Lo	Lo	Lo	Hi	Lo	To MC34119	Gnd
Speakerphone Mike Mute	Lo	X	Lo	Hi	Lo	To MC34119	X

X = Don't Care

A summary of Table 2 is:

a) The MC34114 speech network is put into the Mute mode ($\overline{MT}$ = Lo) not only for dialing, but also to mute the microphone and receiver for the Privacy function (Mike Mute), and when in the speakerphone mode.
b) The MC34118 and MC34119 are disabled for all the handset functions, and enabled for all the speakerphone functions.
c) The MC34118's Mike Mute function is activated for dialing and for the Privacy function.
d) The loop current, which normally flows through the LR pin of the MC34114 (see Figure 1), is directed instead to the MC34119 in the speakerphone mode so as to make the power available to the speaker.
d) The MS pins of the dialer and of the MC34114, are significant only during dialing.

PUTTING IT ALL TOGETHER

Switching Between Handset and Speakerphone Modes

To switch between modes, two actions are necessary: 1) Divert the excess loop current, which normally flows through the MC34114, to the MC34119 during speakerphone mode, and 2) enable and disable the speech network and speakerphone circuits appropriately. The circuit of Figure 5 fullfills those requirements:

HS (3 poles) is the hookswitch operated by lifting the handset. SS (1 pole) activates the speakerphone when the handset is on-hook. The switches are shown on-hook in Figure 5.

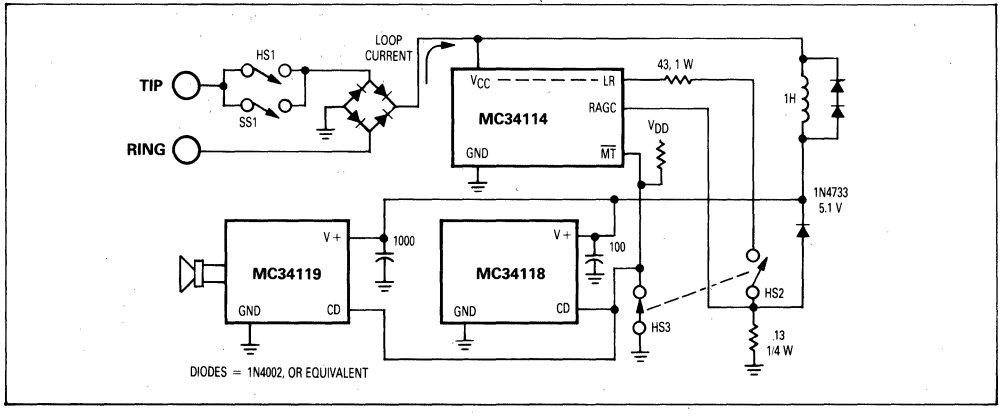


Figure 5. Switching Between Modes

If the handset is on-hook, and switch SS1 is closed (speakerphone mode), the MC34114 uses ≈10 mA internally, but the excess loop current flows through the 1 Henry choke, the zener diode and the 13 Ω resistor. The voltage across the 13 Ω resistor controls the line length compensation function of the MC34114. The MC34118 and MC34119's CD pins are held low by HS3, enabling the speakerphone circuit. The MC34114's $\overline{MT}$ is low, muting its microphone and receive amplifiers. If the handset is lifted while the speakerphone is in operation, the circuit automatically switches to the handset mode.

When the handset is lifted (HS transfers), the MC34114 consumes ≈10 mA internally, but the excess loop current now flows through the MC34114, out of the LR pin and through the 43 Ω and 13 Ω resistors. The voltage across the 13 Ω resistor still controls the line length compensation. This configuration is similar to that of Figure 1. Since the MC34118 and MC34119 are disabled (their CD pins are pulled high), their current consumption is reduced to <1 mA.

Joining the Receive Paths

Referring to Figure 1, receive signals arriving at Tip and Ring generate a current through the ZB network, into pin 15. That current is modified by A4 and the AGC, made available (as a current) at RXA, and coupled to RXI, where it is converted to a voltage by the receive amplifiers and R8. The ZB network is typically 12 kΩ, and R8 is typically 3.9 kΩ. The receive gain to the handset receiver is therefore nominally −10 dB at low loop currents.

To feed the receive signals to the speakerphone, the circuit of Figure 6 is used.

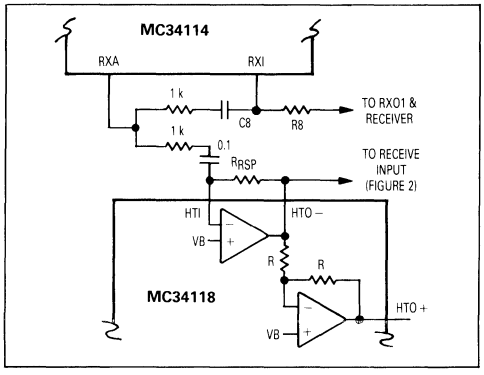


Figure 6. Joining the Receive Paths

The current out of RXA is now split by the 1 kΩ resistors so that approximately half goes to RXI (of the MC34114) via C8, and the other half is converted to a voltage (by the op amp) for the speakerphone's Receive Input (Figure 2). The second op-amp (at HTO+) is unused in this application. The receive gain for the speakerphone (from Tip/Ring to the speaker) is determined by the following equation:

$$G_{RX} = 20 \log \left(\frac{R_{RSP} \times A4 \times AGC \times 0.5}{ZB + 500\ \Omega} \right) + 6\ dB + 20 \log \left(\frac{2 \times Rf}{Ri} \right)$$

The terms A4, ZB, and AGC (from Figure 1) are set at 0.5, 12 kΩ, and 1 respectively for low loop currents. The 0.5 in the first term is due to the current splitting of Figure 6. The +6 dB is the gain of the MC34118's receive attenuator at maximum volume. The third term is the gain of the speaker amplifier.

It is desirable to have as much gain as possible early in the receive path to minimize the effects of noise generated or picked up by the circuit. Since the maximum allowable input at RXI is 350 mVrms, a gain of 3.5 (10.9 dB) was chosen for the first term above, in order to accommodate receive signals of 100 mVrms (−17.8 dBm) at Tip and Ring. R_{RSP} calculates to approximately 160 kΩ. For an overall gain of ≈+30 dB, Rf/Ri must be ≈2.2. At higher loop currents, the overall gain will be ≈+24 dB, due to the line length compensation function.

Joining the Transmit Paths

In the transmit path of Figure 1, the microphone signals are gained up by 30 dB by the mike amplifier. The output at MCO creates a current into TXI through R6 and C5. That current is gained up by 100 by A1 and A2 (assume AGC = 1), and A2's output current then acts on the parallel combination of R1 and the line's ac impedance. Typical values are: R6 = 15 kΩ, R1 = 600 Ω, and 600 Ω for the line's impedance. Neglecting the slight loading of R7, R12, and ZB, the overall handset transmit gain is ≈+36 dB at low loop currents.

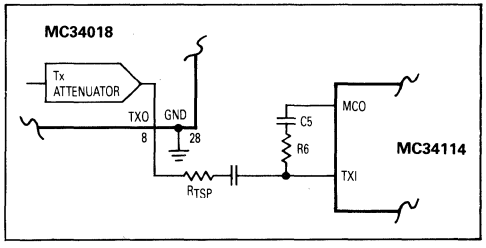


Figure 7. Joining the Transmit Paths

The transmit output from the speakerphone circuit (Figure 2) is applied to the speech network at TXI in Figure 1, through a resistor (R_{TSP}) and a coupling capacitor (see Figure 7). For a nominal gain +40 dB (from the microphone to the MC34114's V_{CC}), R_{TSP} calculates to be ≈11 kΩ. The coupling capacitor (typically 0.1 μF) can be adjusted to set the low frequency rolloff.

Fitting in the Dialer

The DTMF output in Figure 4 is simply connected to C6 and R7 of Figure 1 to get the DTMF signals to Tip and Ring. Using 20 kΩ for R7, and 0.1 μF for C6, DTMF levels of ≈−2.2 dBm will result at Tip and Ring at low loop currents.

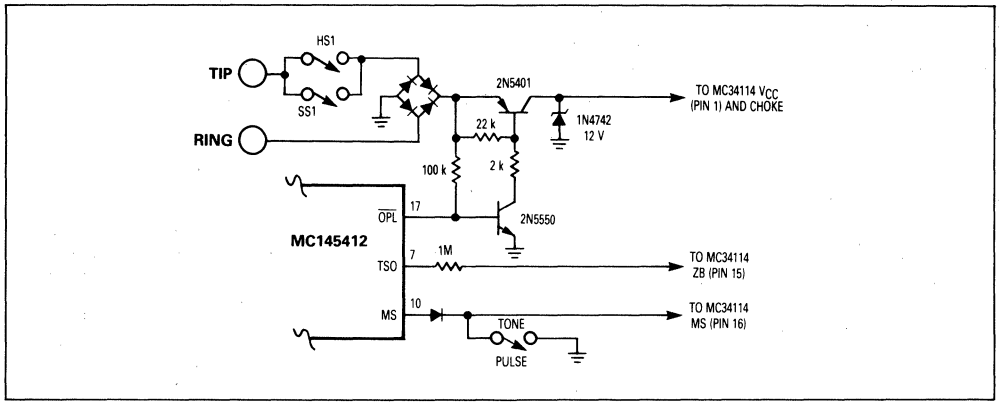


Figure 8. Pulse Dialing Circuit

For pulse dialing, Pin 17 of the MC145412 dialer ($\overline{OPL}$) is connected to a standard two transistor network to interrupt the loop current (Figure 8). The 12 volt zener diode protects the circuitry from voltage spikes during pulse dialing (and whenever a hook switch is opened).

The TSO output (pacifier tone), which is generated only when a keypad button is depressed in the pulse dialing mode, is injected to the MC34114's ZB pin so as to make it available to both the handset receiver and the speakerphone. This tone is not generated during DTMF dialing.

To select between pulse and tone dialing modes, the switch on the dialer's Pin 10 (Figure 4) is connected to the MC34114's MS pin (Pin 16). Since the MC34114's MS pin requires a pull-up resistor for a logic high, a diode must be added (Figure 8) so the dialer's MS pin is open when the switch is in the pulse position.

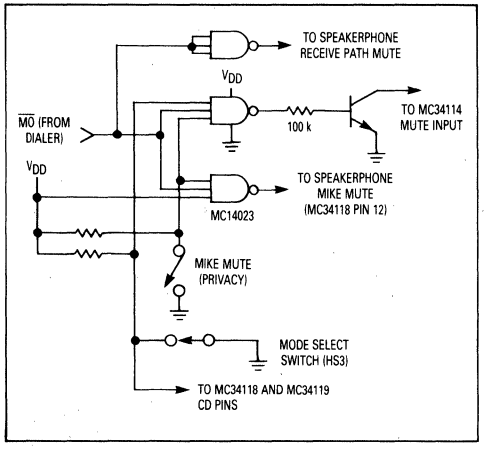


Figure 9. Muting Circuit

Muting and Privacy

The Mute Output of Figure 4 must mute (by at least 45 dB) both microphone paths, and partially mute (10–20 dB) both receive paths during dialing. The privacy (Mike Mute) function requires muting the microphones only by at least 55 dB. This is accomplished with the circuit of Figure 9 using an MC14023 CMOS triple NAND gate. The inputs to the logic circuit are the Mute Output ($\overline{MO}$) from the dialer, the Mike Mute (Privacy) switch and the speakerphone/handset mode select switch HS3 (same as that of Figure 5). The outputs are to the speakerphone's receive path, the MC34114's Mute (which mutes both its transmit and receive paths), the speakerphone's microphone, and to the speakerphone and speaker amp's CD pins. The MC14023 is powered by the MC34114's V_{DD} output.

The circuit of Figure 9 will:

a) Mute the receiver and speaker and disable both microphones during dialing;

b) Disable both microphones when the Privacy switch is closed;

c) Enable either the MC34114 or the MC34118/MC34119 combination in response to the Mode Select

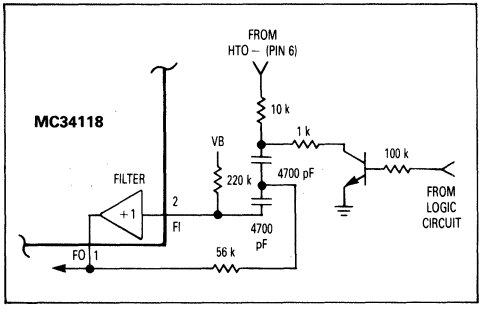


Figure 10. Receive Path Muting

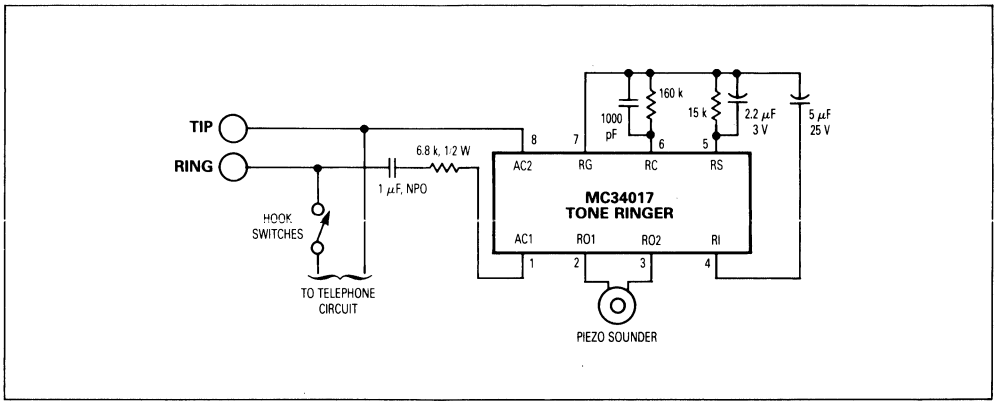


Figure 11. Tone Ringer Circuit

Switch. HS3 is shown on-hook in Figure 9, which enables the speakerphone when SS1 of Figure 5 is closed. (Note: In Figure 5, HS3 is shown controlling the MC34114's $\overline{MT}$ pin directly. In Figure 9 the same function is achieved through the NAND gate).

Muting of the speakerphone's receive path (from the above circuit) is accomplished with the circuit of Figure 10. The muting is inserted in the speakerphone's receive path leading to the filter. Normally, the transistor is off and the 10 k resistor has little effect on the circuit due to the filter's high input impedance (>200 kΩ @ 1 kHz). When Mute is asserted, the signal to the filter is muted by ≈20 dB.

Adding the Tone Ringer

The MC34017 tone ringer circuit, shown in Figure 11, is simply connected directly across Tip and Ring. It is not necessary to disconnect the tone ringer when off-hook. This circuit will provide a ringer with an REN of ≈0.5, and meet all the EIA-470-A and Bell system requirements for impedance, anti-bell tapping and turn-on/off thresholds.

Finally, the Complete Circuit

The complete line-powered featurephone is shown in Figure 12. Some notes concerning this circuit:

a) The resistor and capacitor (R6/C5 shown in Figure 1) between MCO and TXI of the MC34114 was replaced with the network of Figure 12 to provide high frequency roll off.

b) The 13 Ω resistor normally spec'd for R3 of the MC34114 (and shown in Figure 5) was increased to 18 Ω to decrease the point at which line length compensation begins.

c) A 470 μF capacitor was added across the 18 Ω resistor to suppress interaction which occurs between the line length compensation function of the MC34114 and the AGC function of the MC34118.

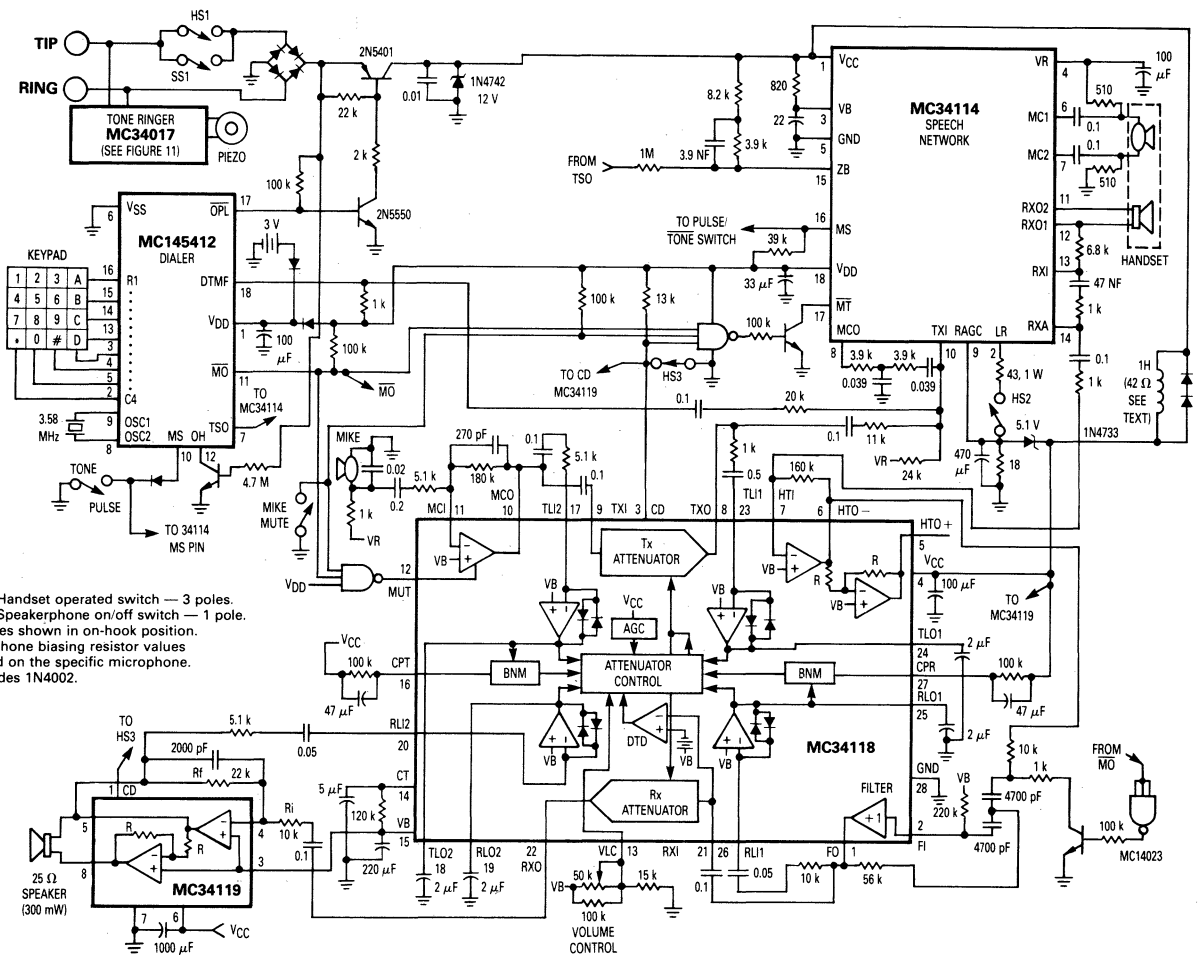
d) The dc resistance of the 1 Henry inductor must be kept below 50 Ω to keep the dc voltage at Tip and Ring and at the MC34114's V_{CC} pin within safe bounds at both low and high loop current values.

The performance curves for this circuit are shown in Figures 13–18. The "Speaker Amp Max Output Swing" is the maximum rms voltage available at the speaker terminals. The transmit gain tests involved replacing each microphone with a signal generator and adjusting for a level of approximately −11 dBm at Tip and Ring into a 600 Ω resistive load. The receive tests involve applying approximately −27 dB to Tip and Ring, and measuring the gain to the receiver or speaker.

As can be seen in Figure 14, the maximum available speaker power is a function of the loop current since all of the speaker current must come from the loop. Consequently, the receive gain for the speakerphone (Figure 17) shows a marked decrease at low loop currents. It must be remembered that in a line powered speakerphone, as the speaker draws current in response to a receive signal, the voltage at Tip and Ring decreases quickly. As the V_{CC} at the MC34119 falls with the Tip and Ring voltage, the speaker amp's output capability is reduced. Consequently, a 25 Ω speaker is recommended for a line powered speakerphone as this makes the best use of the power available from the phone line. A lower impedance speaker will require more current, causing V+ to sag further for a given signal level. A higher impedance speaker draws less current, but produces less sound power.

Additionally, the following muting specs apply:

1) **Handset microphone:** >70 dB while dialing, or when Mike mute switch is closed. 80 dB in speakerphone mode.
2) **Speakerphone microphone:** >90 dB while dialing, in the handset mode, or when the Mike mute switch is closed.
3) **Handset receiver:** ≈17 dB while dialing, or when in the speakerphone mode.
4) **Speaker:** ≈20 dB while dialing, >100 dB when in handset mode.



Notes:
1) HS = Handset operated switch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone.
3) All diodes 1N4002.

Figure 12. Pulse/Tone Featurephone w/Memory — Line Powered

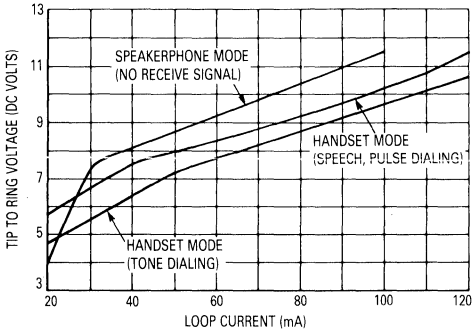


Figure 13. Tip to Ring DC Voltage versus Loop Current

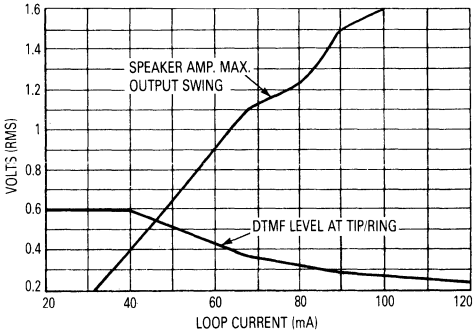


Figure 14. Speaker Amplifier Output and DTMF Level versus Loop Current

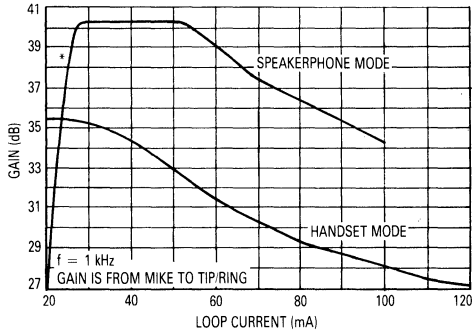


Figure 15. Transmit Gain versus Loop Current

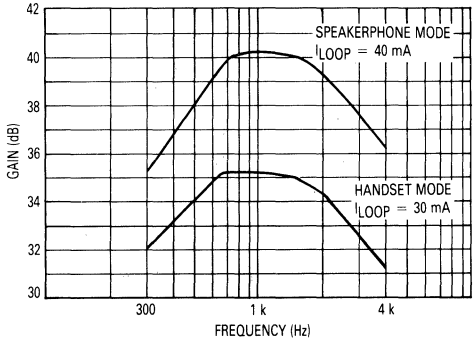


Figure 16. Transmit Gain versus Frequency

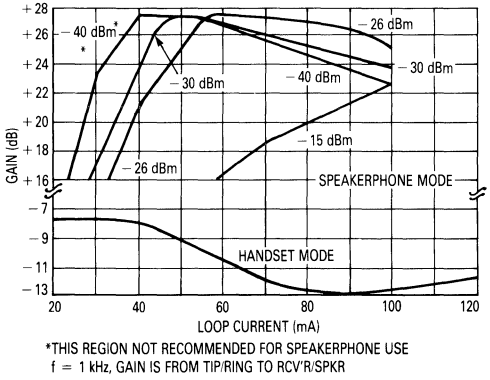


Figure 17. Receive Gain versus Loop Current and Input Signal

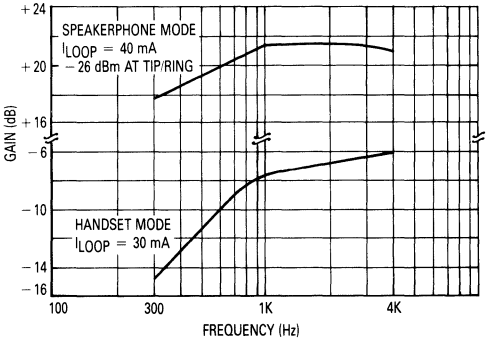


Figure 18. Receive Gain versus Frequency

BOOSTING THE SPEAKERPHONE AT LOW LOOP CURRENTS

Adding a Booster

To improve the performance of the speakerphone at low loop currents (below 40 mA), a minimal cost approach is to add an optional booster to the power supply portion of the MC34119. The approach in this application note is to use a wall mount transformer, similar to calculator chargers. A 6 volt ac Adapter, Radio Shack model #273-1454A, which contains the diode bridge and filter capacitor, was used to minimize the additional circuitry within the speakerphone itself. Since this particular ac adapter is specified for use with Radio Shack's speakerphones, it is this author's assumption that it complies with applicable FCC specifications, although that is not so stated on the transformer.

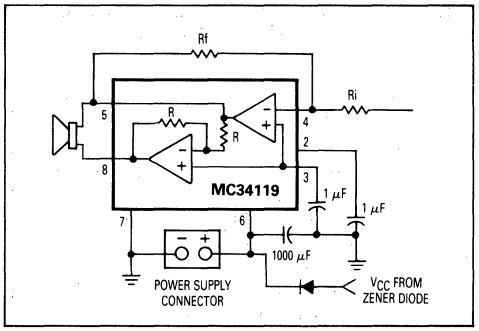


Figure 19. Adding a Speakerphone Booster

This application does not require a regulated voltage from the ac adapter, which further simplifies the design. The circuit of Figure 19 adds the ac adapter to the circuit of Figure 12.

The power supply connector is added to the MC34119 V_{CC} pin, and diode connected to the system's 5.1 volt zener diode of Figure 12. Pin 3 of the MC34119, which previously had been connected to the VB bias line of the MC34118, now is biased from an internal circuit. The 1 μF capacitors on pins 2 and 3 provide power supply noise and ripple rejection.

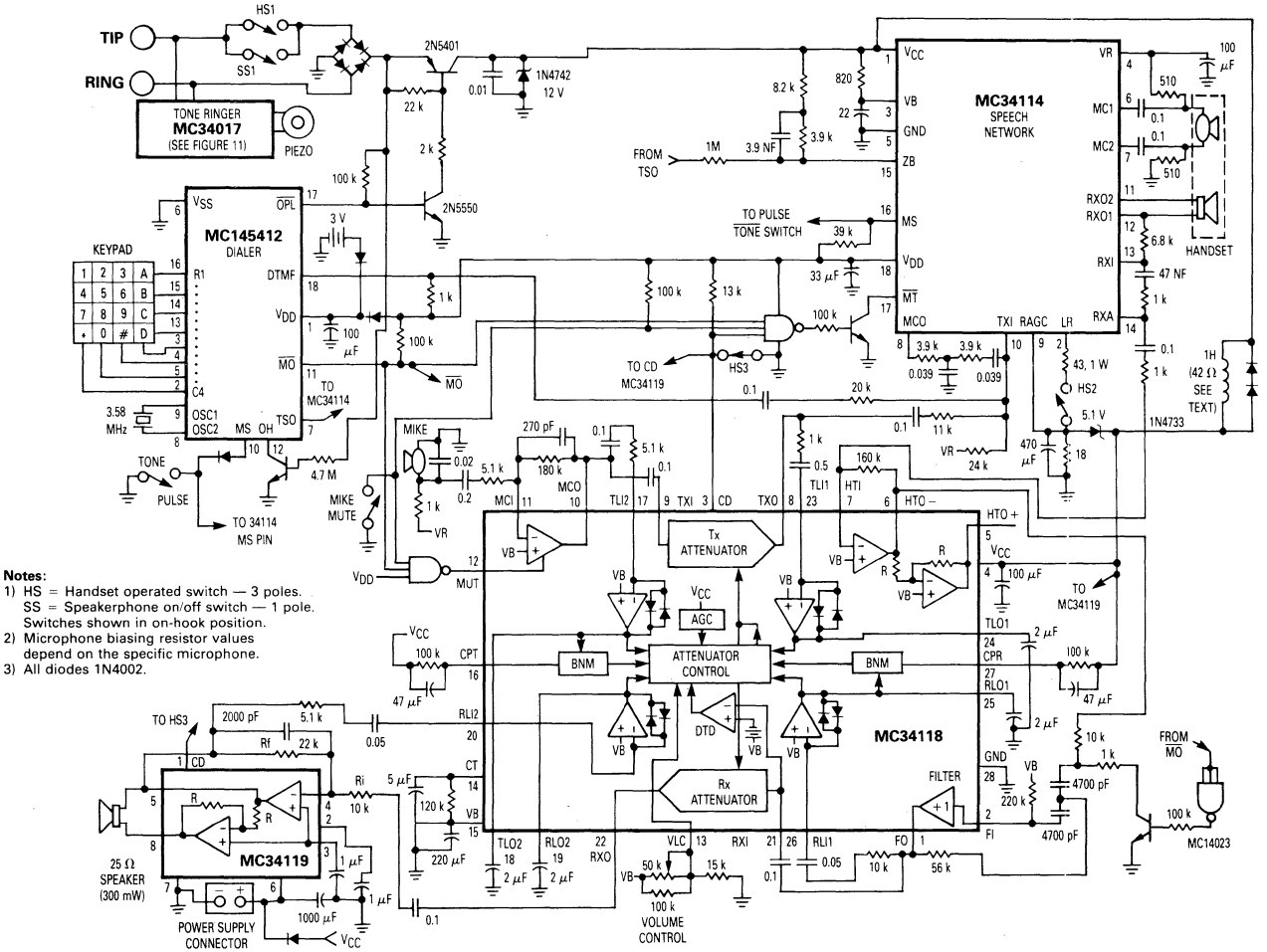
On long lines, where the system V_{CC} tends to sag easily in the presence of receive signals, the booster provides the current to the speaker amplifier. The system V_{CC}, in turn, does not sag, but remains at a stable and consistent level over all values of loop current.

Without the adapter plugged in, the circuit will act similar to that of Figure 12. In the handset mode, the circuit characteristics are the same as that of Figure 12 when it is in the handset mode.

The Complete Circuit with the Booster

The complete circuit is shown in Figure 20. A quick comparison shows it is identical to that of Figure 12, except for the booster section in the lower left hand corner. The performance curves for this circuit are shown in Figures 21–26. As can be seen in Figures 22, 23 and 25, the speakerphone's performance does not degrade below 40 mA as had happened in Figures 14, 15 and 17. The muting specs for this circuit are the same as for Figure 12.

The current required from the booster varies from ≈3 mA (no receive signal) to ≈120 mA with a −15 dBm signal at Tip and Ring.



Notes:
1) HS = Handset operated switch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone.
3) All diodes 1N4002.

Figure 20. Pulse/Tone Featurephone w/Memory — Line Powered w/Booster

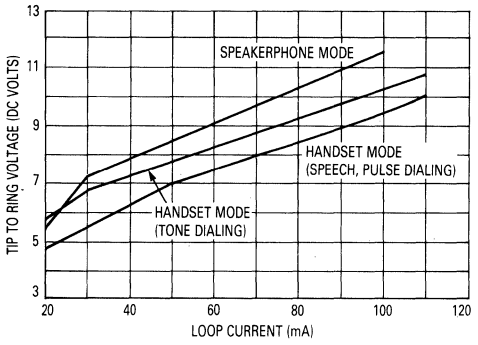


Figure 21. Tip to Ring DC Voltage versus Loop Current

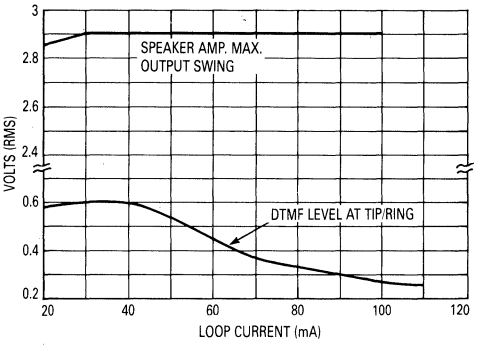


Figure 22. Speaker Amplifier Output and DTMF Level versus Loop Current

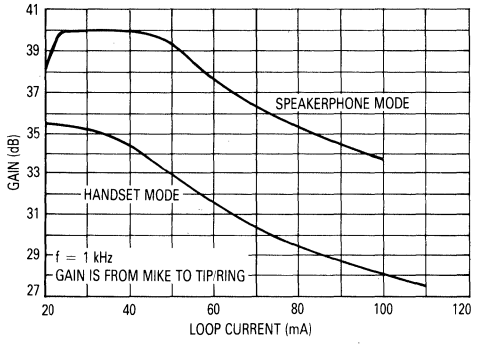


Figure 23. Transmit Gain versus Loop Current

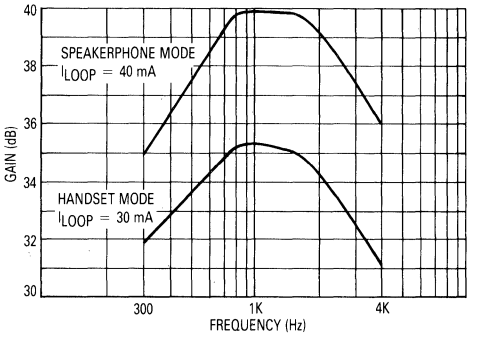


Figure 24. Transmit Gain versus Frequency

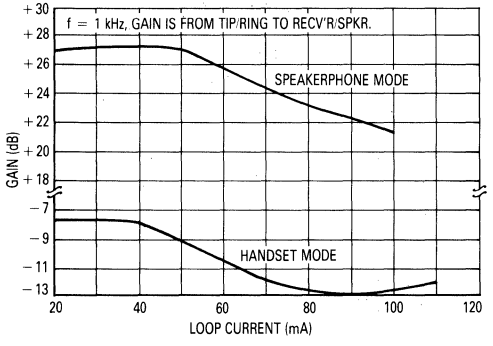


Figure 25. Receive Gain versus Loop Current

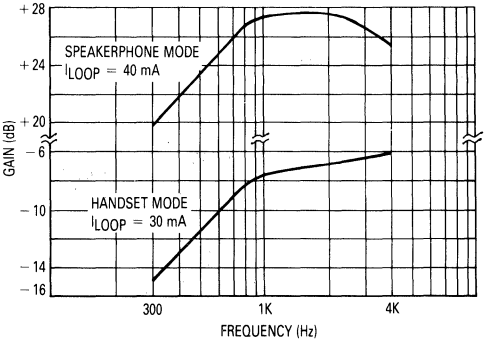


Figure 26. Receive Gain versus Frequency

USING A POWER SUPPLY INSTEAD OF LINE POWER

Using A Transformer

For those cases where it is desirable to power the featurephone from a regulated power supply, rather than from loop current, a transformer is required at Tip and Ring to provide the isolation needed between the phone line and any ac power and earth ground. The primary change to the circuit of Figure 12 is in the area of the Tip and Ring interface, as shown in Figure 27. It must be remembered that loop length compensation is not possible in this circuit since the loop current is not monitored. The MC34114's RAGC pin is grounded in this circuit, setting the transmit and receive gains to maximum.

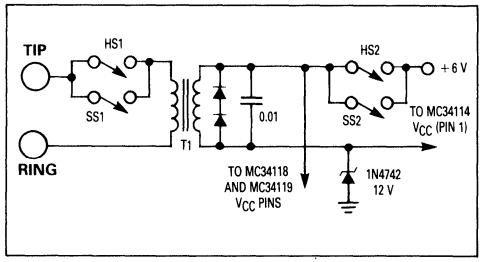


Figure 27. Tip/Ring Interface with a Power Supply

The +6 volt supply powers the MC34114 through the transformer winding. In this manner the speech signals are coupled between the MC34114 and Tip and Ring. The two diodes provide transient clamping, as does the 12 volt zener diode. The MC34118 and MC34119 are powered directly from the +6 volt supply, eliminating the need for the 1H choke. The SS switch (speakerphone on/off) requires one more pole, as shown in Figure 27. The tolerance on the +6 volt supply is ±0.5 volt.

Changes in the Switching and the Dialer

The use of a power supply simplifies the selection of handset versus speakerphone mode of operation. The diversion of the excess loop current is not an issue in this circuit, so the switching of that current is eliminated, along with 5.1 volt zener diode.

Because of the isolation requirement, the MC145412 dialer requires a relay to break the loop current during pulse dialing. Figure 28 depicts this circuit.

The relay is normally off, and energized only for the pulse dialing function. The 1 μF capacitor (rated 250 volts min., NPO) helps absorb the transients generated during pulse dialing.

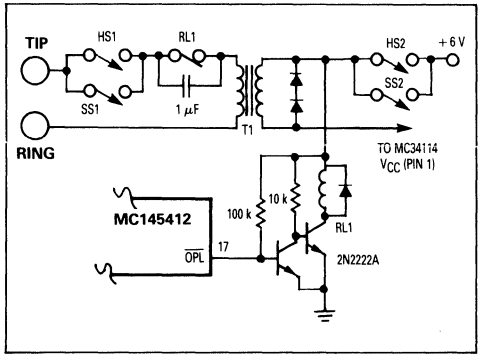


Figure 28. Pulse Dialer Circuit

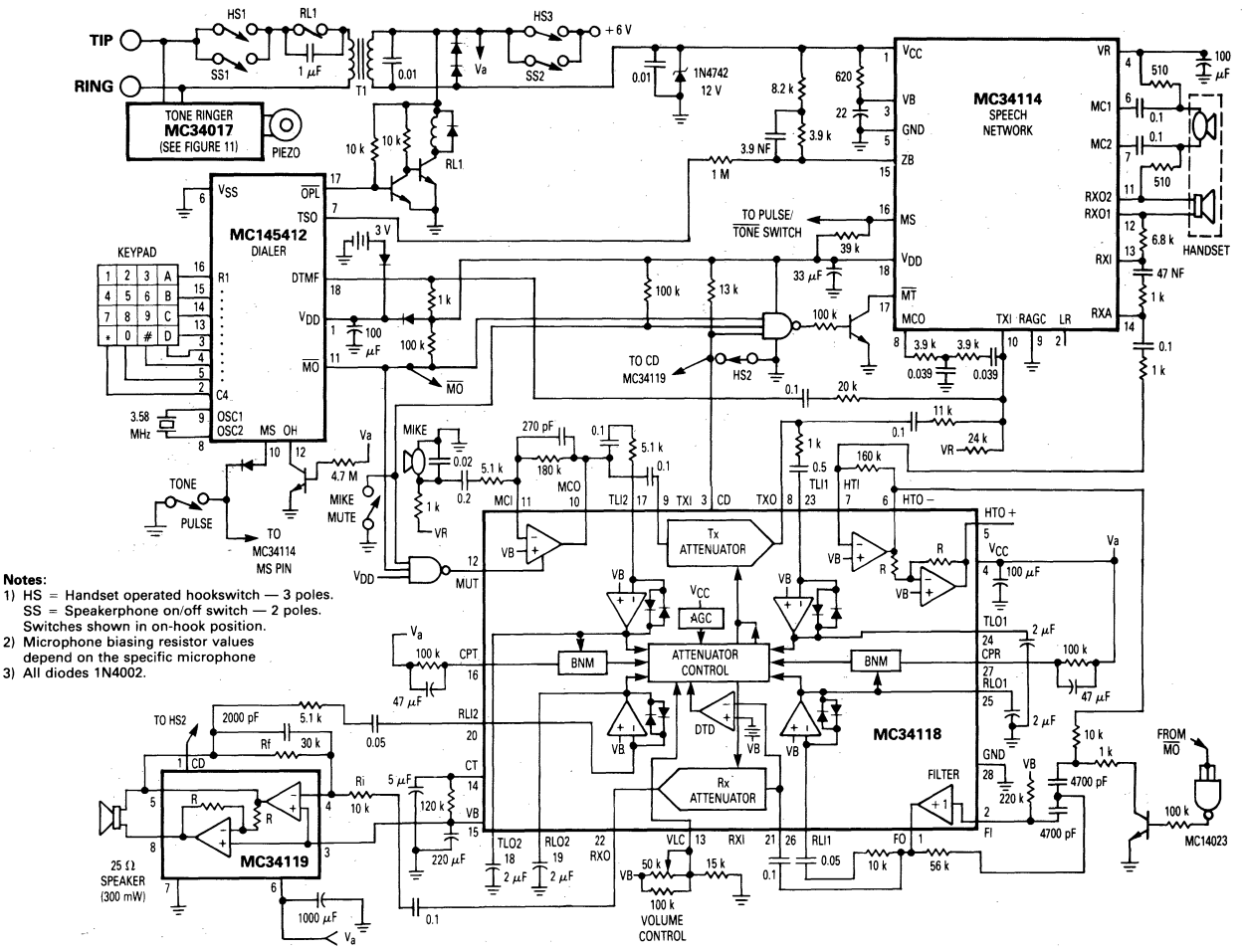
The Complete Circuit with the Power Supply

The complete circuit is shown in Figure 29. The performance curves are shown in Figures 30–35. The Tip to Ring dc voltage (Figure 30), determined solely by the dc resistance of the transformer winding, is somewhat lower than in the previous circuits at low loop currents. Figures 31, 32, and 34 show the performance is fairly constant with loop current, except for a slight reduction in gain at the higher currents. This is due to the characteristics of the transformer used in developing this circuit (model #TTPC-13 from Stancor, Inc.). Also noticeable in the curves, compared to Figures 13–18 and 21–26, is the lack of loop length compensation — a natural consequence of this type of circuit.

The muting specifications for this circuit are the same as for the line powered circuit. The current required from the +6 volt power supply is as follows:

a) Handset mode: ≈13 mA.
b) Speakerphone mode (no sound at the speaker): ≈24 mA.
c) Speakerphone mode (max. volume at the speaker): ≈144 mA.

Although Figure 29 indicates the use of a 25 ohm speaker, any impedance speaker within the range of 8 to 50 Ω can be used, since this circuit is not line powered. The receive gain may have to be adjusted, however, if a different speaker is used.



Notes:
1) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 2 poles.
   Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone
3) All diodes 1N4002.

Figure 29. Pulse/Tone Featurephone w/Memory — Powered From a Power Supply

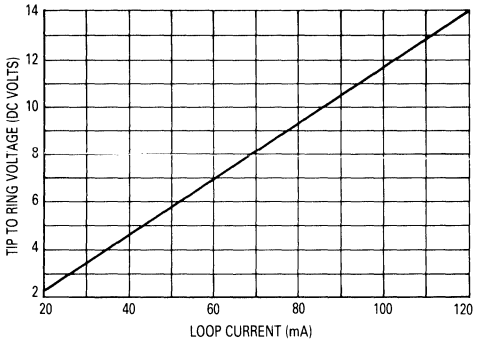


Figure 30. Tip to Ring DC Voltage versus Loop Current

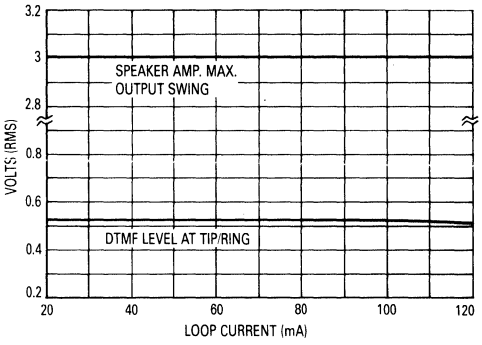


Figure 31. Speaker Amplifier Output and DTMF Level versus Loop Current

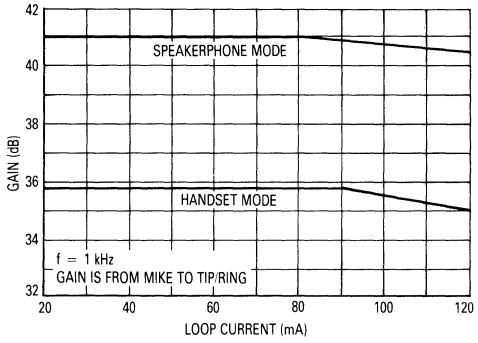


Figure 32. Transmit Gain versus Loop Current

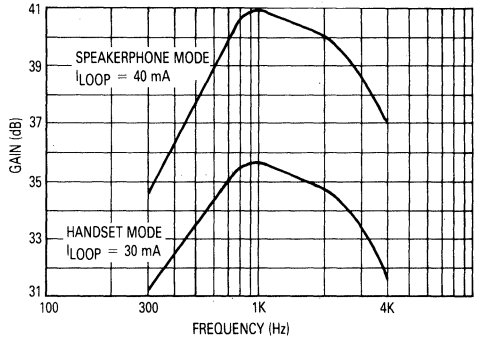


Figure 33. Transmit Gain versus Frequency

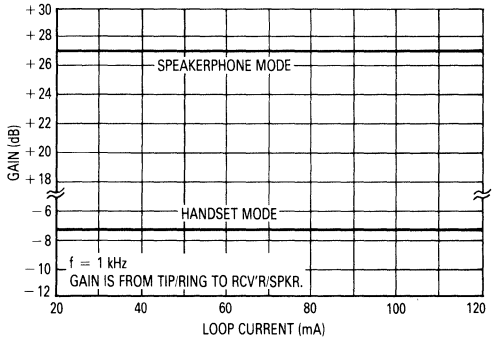


Figure 34. Receive Gain versus Loop Current

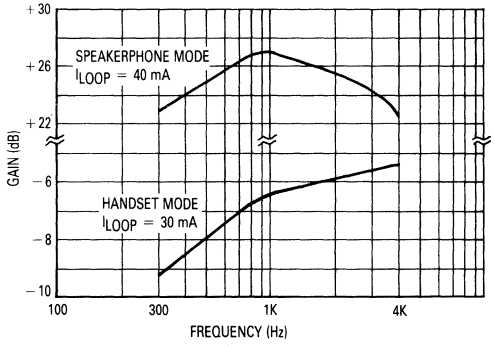


Figure 35. Receive Gain versus Frequency

CONSTRUCTION HINTS

Board Layout

The filter capacitor for the speakerphone IC and for the speaker amp (typically 100 μF and 1000 μF respectively) must be physically adjacent to the ICs, within 1". This is particularly important in the line-powered versions, where V_{CC} can vary with the speech intensity. Since most of the current is used in the speaker amplifier, the PC board track leading to Pin 6 of the MC34119 should be laid out with care, preferably close to the zener diode, or the power supply connector. The ground tracks should be as wide as possible, and laid out with care.

EMI Susceptibility

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the speakerphone. EMI may enter the circuit through Tip and Ring, through the microphone wiring to the amplifiers, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1, and TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. These board traces should be kept short, and the resistor and capacitor for each input should be physically close to the pins. Other high impedance input pins (MCI, VLC, HTI, FI) should be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

Acoustics

a) In the design of any speakerphone, acoustics are extremely important, and **must** be considered from the very beginning. Building a breadboard with the microphone and speaker "hanging out in mid air" simply **will not work!!!** One of the most common problems in a speakerphone design is acoustic feedback (the speaker is closely coupled to the microphone) which results either in oscillations (2–10 kHz) or "motor-boating" (1–10 Hz switching). A properly designed enclosure for the finished product should provide at least 50 dB of acoustic loss (speaker drive voltage to microphone output voltage). The physical location of the microphone, along with its characteristics, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

b) The quality of the speaker, and the acoustic cavity in which it resides, have a major impact on the quality of the sound. A little time spent here can go a long way towards improving the sound of the finished speakerphone. As a general rule, good electronics cannot compensate for poor acoustics and/or low speaker quality.

In the Final Analysis . . .

In the final analysis, the circuits shown in this application note will have to be "fined tuned" to match the acoustics of the enclosure, and the specific microphone and speaker selected. The component values shown in this application note should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at key points in the circuits (see appropriate text). The switching response of the speakerphone can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines. The references can be consulted for additional speakerphone design theory.

GLOSSARY

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

C-Message Filter — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 x log (P_1/P_2) for power measurements, and
20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

dBrnC0 — Noise measured in dBrnC referred to zero transmission level.

DTMF — Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four Wire Circuit — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone), and one pair is for the Receive path (generally to the receiver).

Full Duplex — A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full duplex.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half Duplex — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

Hookswitch — A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Line Length Compensation — Also referred to as loop compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop — The loop formed by the two subcriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loop Current — The dc current which flows through the subscriber loop. Typically provided by the central office or PBX, it ranges from 20 to 120 mA.

Off Hook — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On Hook — The condition when the telephone is disconnected from the phone system, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Pulse Dialing — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 times per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

REN — Ringer Equivalence Number. An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1 equals ≈8 k ohms. The Bell system typically permits a maximum of 5 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Speech Network — A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip — One of the two wires connecting to the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 Vrms, 20 Hz.

Two-Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Voiceband — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

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MC34119 Data Sheet, March, 1988, Motorola Inc.
MC34017 Data Sheet, January, 1984, Motorola Inc.
MC34114 Product Preview Data Sheet, Sept. 1987, Motorola Inc.
MC145412 Data Sheet, February, 1987, Motorola Inc.
Busala, A., Fundamental Considerations in the Design of a Voice Switched Speakerphone, B.S.T.J., 39, 1960, p. 265.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Ask for Applications
Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600

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AN1006

Linearize the Volume Control of the MC34118 Speakerphone

Prepared by
Dennis Morgan
Bipolar Analog IC Division

The volume control level of the MC34118 speakerphone IC has a nonlinear relationship with respect to the position of the volume control potentiometer, evident in Figure 14 of the data sheet. Since the input impedance at VLC (Pin 13) is very high, the horizontal axis in the graph of Figure 14 can be said to represent the potentiometer's mechanical position (using a linear taper potentiometer), with the two extreme ends of the potentiometer's position at 0.3 and 1.0. As can be seen, the gain changes at a slow rate when near maximum volume, but changes rapidly when near the minimum volume setting.

By changing the potentiometer/resistor circuit to that shown in Figure 1 (below), the volume control relationship is linearized to an almost perfect straight line (the values were selected to maintain [VLC = 0.3 x VB] at minimum volume). The result is shown in Figure 2 (below), with the only nonlinearity near the maximum volume end (the vertical axis is the gain of the receive attenuator). The circuit requires the addition of only one resistor. The potentiometer can be rotary, or a linear movement type, as long as it has a linear taper.

3

Figure 1.

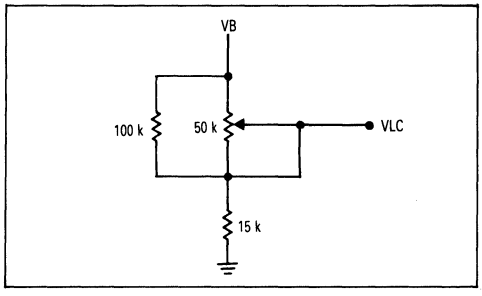
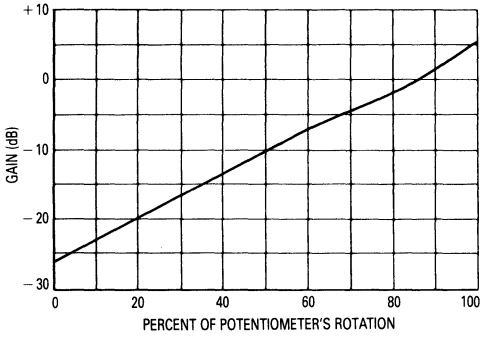


Figure 2.



Thanks to Alan Long (Motorola, Toulouse) for this circuit idea.

EB112

Engineering Bulletin

By Tanya Tussing and Glen Zoerner
Telecommunication Applications
Austin, Texas

3

THE APPLICATION OF A TELEPHONE TONE RINGER AS A RING DETECTOR

Telephone ringers are driven by high voltage, low frequency ac signals which are superimposed on the 48 volt dc tip-ring feed voltage. An electronic ring detector must sense the presence of an ac signal on the line and produce a dielectrically isolated logic level to the system processor. To isolate the line from the system, an on-chip piezoelectric driver drives the LED of an optocoupler. A 1 μF capacitor filters the transistor output of the optocoupler, creating a solid logic 0 when a ring signal is present. Figure 1 depicts the schematic of the ring detector. The peripheral components around the MC34012 set trigger levels and the ringing impedance signature for FCC Part 68 compliance.

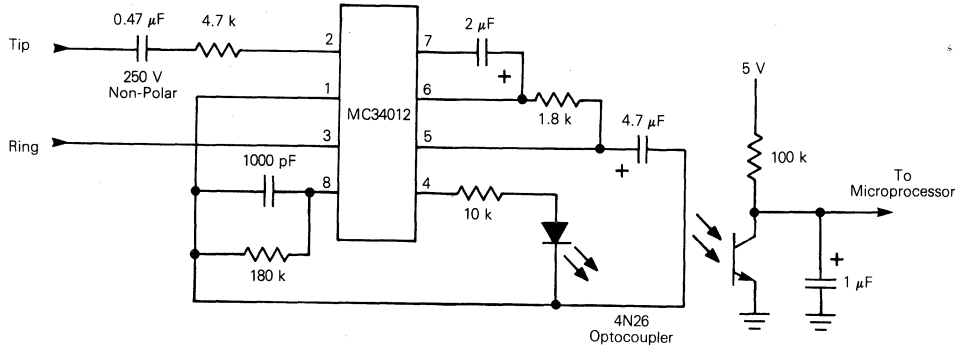


FIGURE 1 — Ring Detector Schematic

LSI for Telecommunications

a one-chip telephone

W. DAVID PACE
Motorola, Inc.
Tempe, Arizona

In recent years, a number of integrated circuits — such as DTMF dialers, speech networks, and tone ringers — have been developed for telephone applications. These products have replaced electromagnetic elements of the telephone because of performance and cost improvements achievable with integrated systems. In addition, the use of integrated circuits in telephones provides considerable freedom in the external design of telephone sets from both the practical and aesthetic points of view.

With these objectives in mind, a single-chip telephone circuit has been developed. The MC34010 Electronic Telephone Circuit (ETC) provides all the functions of a standard tone-dialing telephone. In addition, a microprocessor interface port facilitates automatic dialing features. An important characteristic of the ETC is its ability to operate with instantaneous input voltages as low as 1.4 V. Low-voltage operation is a key requirement in North American telephone networks, where parallel connections are common.

FUNCTIONAL BLOCKS OF THE MC34010 ETC

Figure 1 shows the elements of the ETC:

- **Line Voltage Regulator:** provides the dc termination of the subscriber loop and a bias voltage for the DTMF dialer and speech network.
- **DTMF Dialer:** generates the appropriate dual-tone multi-frequency (DTMF) signals for dialing.
- **MPU Interface:** allows the DTMF generator to be controlled by a separate microprocessor, which may be programmed to provide automatic dialing features.
- **Speech Network:** provides the two-wire to four-wire interface between the telephone line and the receiver and microphone of the handset.
- **Tone Ringer:** converts the ac ringing signals from the exchange into a warbled tone emitted through a piezo sound element.

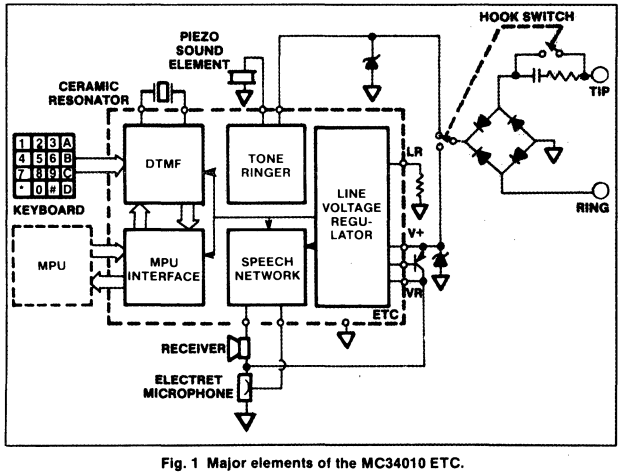


Fig. 1 Major elements of the MC34010 ETC.

Line Voltage Regulator

The line voltage regulator provides a regulated bias voltage at the VR terminal of 1.1 V to other sections of the ETC. The low saturation voltage of an external PNP pass transistor allows the line input voltage to fall within 300 mV of VR voltage without clipping signals on the line. Thus, the DTMF and speech circuits maintain specified performance with instantaneous line voltages as low as 1.4 V.

The circuit associated with the LR terminal determines the dc resistance of the telephone. At low line voltages (corresponding to operation in parallel with nonelectronic telephones), the ETC draws only 5 mA of bias current for the speech network and keypad interface circuits. When the V+ terminal voltage exceeds 3 V, excess line current flows through an external resistor at terminal LR. The 3-kV level shift from V+ to LR prevents saturation of the dc termination circuit with signals up to 2 V peak (+5 dBm) on the line.

An internal constant current sink nominally equal to the bias current of the DTMF dialer also flows through the dc termination circuit. When the DTMF dialer is activated, this current sink is disabled to reduce the line current transient and dialer clicks.

DTMF Dialer

Inexpensive telephone keypads have switches of the single pole/single throw (SPST) type that connect the row and column terminals corresponding to the selected digit. A keypad interface circuit within the ETC, consisting of input resis-

tors, comparators, and decoding logic, activates the DTMF tone generators whenever two keypad input terminals are connected.

When the keypad interface activates the DTMF generator, it also produces a mute signal for the speech network. This mute signal disables the transmit amplifier and reduces the DTMF sidetone in the receiver. Muting the receiver also suppresses clicks associated with DTMF turn-on and turn-off transients.

The row and column tone generators include a programmable counter, an encoder, and a digital-to-analog (D/A) converter. The output of the D/A converter is a stair-step approximation of a sine wave with 16-step intervals per period. Fourier analysis of such a waveform reveals that the time intervals corresponding to the positive and negative peaks (first and ninth intervals) can be shortened or lengthened with little impact on distortion. By modifying the division ratio of the programmable counter during these peak intervals, output frequency errors are reduced. The periods of the DTMF tones are adjusted to the desired value within the resolution afforded by the 500-kHz oscillator frequency.

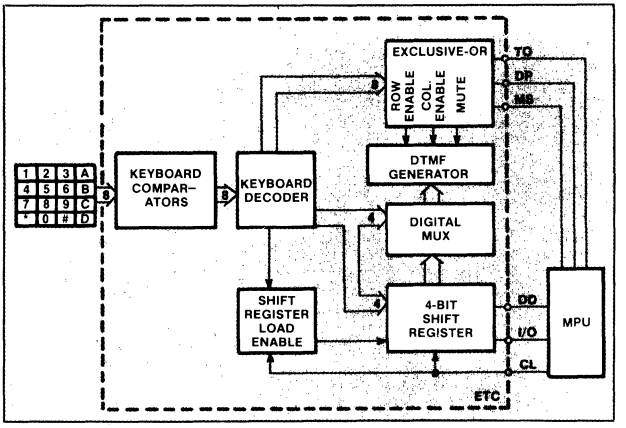


Fig. 3 The MPU interface circuit.

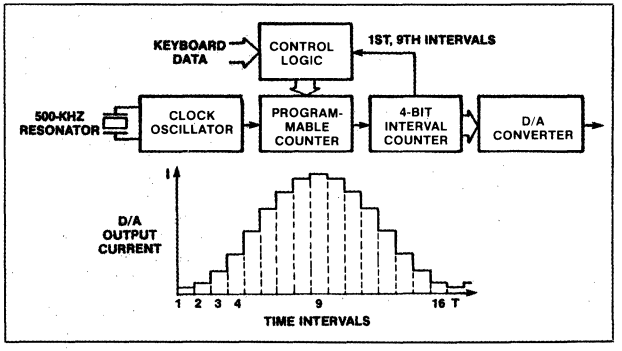


Fig. 2 The DTMF frequency synthesis technique.

Figure 2 depicts the implementation of this error reduction technique. The programmable counter divides the 500-kHz clock frequency by a number N that is loaded by the control logic at the beginning of each step. The output frequency of the programmable counter is further divided by the 4-bit interval counter. It is this counter which distinguishes the 16 waveform intervals. The output of the 4-bit counter drives the D/A converter through an encoder (not shown in **Figure 2** for simplicity).

Consider, for example, the generation of the 697-Hz Row 1 tone. For 14 of the 16 waveform intervals the control logic loads the programmable counter with a divisor of 45. For the first and the ninth intervals, however, feedback from the 4-bit interval counter causes the control logic to program the counter to divide by 44. This combination of divisors reduces the 500-kHz clock frequency to 11.14 kHz at the output of the programmable counter. The interval counter divides this signal by 16, producing a 696.4-Hz Row 1 tone. The desired frequency of 697 Hz, therefore, is synthesized with an error of only 0.09 percent.

Other DTMF tones are generated by loading the programmable counters with appropriate pairs of divisors. The worst-case frequency-division error for the eight dialing tones is 0.16 percent. Reducing the divider errors permits an inexpensive 500-kHz ceramic resonator to be used for DTMF clock generation instead of a more precise quartz crystal. In addition, the lower clock frequency allows the counter to be fabricated in a linear-compatible integrated injection logic (I^2L) technology which enhances the performance of the analog sections of the ETC.

The outputs of the row and column D/A converters are summed in the proper proportion (with a 2-dB twist) and amplified to drive the telephone line. The amplitude of the line's signal is determined by an external resistor. Feedback around the DTMF output amplifier reduces the dialing-mode output impedance to 2 kΩ to satisfy return-loss specifications.

MPU Interface

The MPU interface permits communication between the telephone keypad, the DTMF dialer, and a microprocessor. Through this port, telephone numbers may be stored in the microprocessor and later retrieved for automatic dialing. **Figure 3** shows the major blocks of the MPU interface section and the connections between the keypad, DTMF dialer, and microprocessor.

Each button of a 12- or 16-number keypad is represented by a 4-bit code. This same code controls the programmable counters to generate

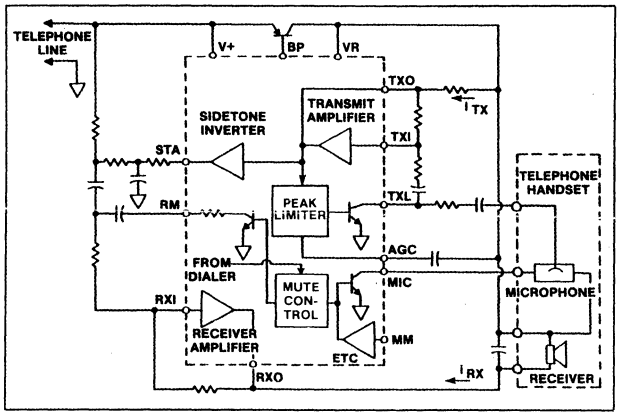


Fig. 4 Speech network block diagram.

the appropriate row and column tones. Binary words corresponding to keypad digits are transmitted serially to or from the microprocessor via the 4-bit shift register. The direction of data flow is determined by the state of the DD terminal input.

In the manual dialing mode, DD is a logic "0"; the 4-bit code from the keypad is fed to the DTMF generator and also loaded into the shift register. The microprocessor-controlled clock shifts the data through the I/O terminal on negative clock transitions. The shift register load-enable circuit cycles the register between the load and shift modes such that multiple read cycles may be provided to the microprocessor for a single key closure. Six complete clock cycles will output a 4-bit word from the ETC and reload the shift register for a second look.

In the automatic dialing mode, DD is a logic "1" and a 4-bit code is entered from the microprocessor into the ETC. The shift register load-enable circuit is disabled in this mode. Only four clock cycles are required to transfer a digit to be dialed into the ETC. A logic "1" on the TO terminal disables the DTMF output until valid data from the microprocessor is in place. Subsequently, TO is switched to a logic "0" to generate a DTMF tone pair on the line.

An exclusive OR circuit in the keypad interface logic determines if more than one key is depressed. Single tones may be initiated by depressing two keys in the same row or column. The exclusive OR circuit also generates the DP and MLS output signals. DP indicates when one and only one key is depressed, thereby signaling the microprocessor that valid data are available. MS indicates when the DTMF generator is enabled and the speech network is muted.

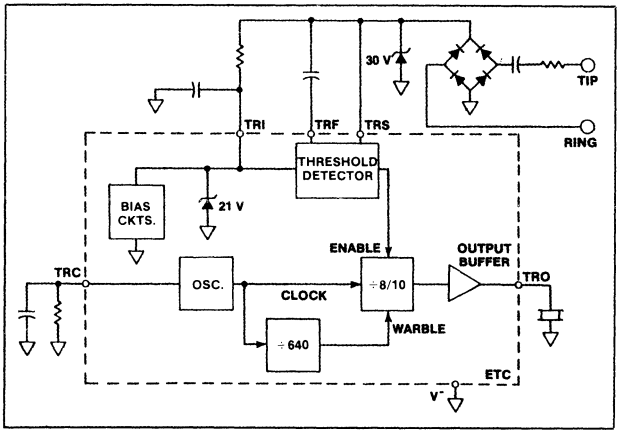


Fig. 5 Tone ringer block diagram.

Speech Network

The speech network illustrated in **Figure 4** provides the two- to four-wire interface between the telephone line and the transmit and receive transducers. The key feature of this circuit is its ability to operate with instantaneous line voltages as low as 1.4 V. Satisfactory operation has been demonstrated in parallel with a carbon microphone telephone for loop resistances of up to 2200 Ω. This corresponds to 27,000 ft of 26 AWG cable between the subscriber terminal and the local exchange.

An electret microphone biased by the VR regulator drives the transmit amplifier. The microphone is muted internally by the dialer during DTMF signaling and may be muted by the control signal on the MM terminal.

For very loud talkers, the peak limiter reduces the transmit amplifier input level to maintain low harmonic distortion. Transmit gain control is achieved by varying the saturation resistance of the transistor which drives the TXL terminal. This transistor operates as a variable resistance because its collector terminal is unbiased. The peak limiter circuit determines when the transmit amplifier output approaches the clipping level and drives the transistor at TXL to attenuate the amplifier input. The peak limiter typically provides 30-dB additional dynamic range with approximately 1 percent total distortion.

As shown in **Figure 4,** the transmit amplifier output signal is inverted at the STA terminal to provide sidetone cancellation at the receiver. The signals from the telephone line and the STA terminal are summed at the input at the receive amplifier. When transmitting, these signals are nominally 180° out of phase and the proper choice of external components will nullify the

transmitted signal in the receiver. In practice, phase shift from the transmit amplifier output to the line due to reactive line impedances limits the degree of sidetone cancellation achieved.

The receive amplifier output produces a signal current in the receive transducer that also flows through the VR regulator to the telephone line. This ac current determines the impedance of the telephone at the interface with the line. The input impedance is set by the proper choice of receive amplifier gain and receiver impedance. A 300-Ω receiver driven with a gain of one-half results in a 600-Ω input impedance and satisfactory receive sensitivity.

Tone Ringer

The tone ringer responds to large signal ac input voltages with a warbled two-tone output signal which may drive a piezo transducer or speaker. This warbled tone is produced by dividing the tone ringer oscillator frequency alternately by 8 or 10 as shown in **Figure 5.** The warble rate is the oscillator frequency divided by 640. In a typical application, an 8-kHz oscillator produces 800-Hz and 1000-Hz tones warbling at 12.5 Hz.

The tone ringer output is enabled by the threshold detector when a ringing signal greater than 35 Vrms is applied at tip and ring. The ringing signal level is measured by monitoring the voltage across the external resistor at the TRI terminal. When the average voltage across this resistor exceeds a threshold level, the output buffer commences driving the piezo element at the TRO terminal. The additional current drawn from the line to drive the piezo also flows through the external resistor at TRI. Therefore, the voltage across this resistor increases when the output is enabled. Increasing the voltage applied to the threshold detector creates hysteresis between the turn-on and turn-off levels that ensures clean on/off transitions.

DESCRIPTION

The MC34010 ETC incorporates 300 bipolar transistors and 520 I^2L gates on a 125 x 146 mil die. The chip is fabricated using a two-layer metal, Linear/I^2L process and packaged in a 40-pin plastic package. Combining a dialer, speech network, and tone ringer on a single chip represents a major step forward in the modernization and cost reduction of analog telephones. □

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AN946

Limited Distance Modem
Using the Universal Digital Loop Transceiver Chip Family

OVERVIEW

The introduction of the Universal Digital Loop Transceiver (UDLT) family of integrated circuits aids the design of a high speed Limited Distance Modem (LDM). With an external clock, the LDM will transmit asynchronous data at rates up to 80 kbps. As shown here with an internal clock, the LDM can send as much as 38.4 kbps of asynchronous full duplex data up to two kilometers on 26 AWG twisted pair wire. The data transfer is controlled by the following RS-232C handshake signals: Request to Send (RTS), Clear to Send (CTS), Data Set Ready (DSR) and Carrier Detect (CD). If the data link is operating, CTS goes active in response to RTS going active. DSR is active if the LDM is powered up. If synchronization is lost, the CD signal goes inactive. Figure 1 shows a block diagram of the LDM. Figure 10 is a photostat of the LDM Demonstration Board - front, and Figure 11 is a photostat of the LDM Demonstration Board - back. Table 1 is a parts list for the slave and master LDM.

UNIVERSAL DIGITAL LOOP TRANSCEIVER

The heart of the LDM is the UDLT master/slave chip set. This chip set transmits data at a 256 kbps burst rate using a "ping pong" approach. As shown in Figure 2, a Modified Differential Phase Shift Keyed (MDPSK) data burst is transmitted from the master to the slave. Then after a slight delay, a burst is transmitted from the slave to the master. Since an eight kHz clock is typically applied to the Master Sync Input (MSI) pin, and ten bits are sent to the master and the slave every MSI period (every 125 μs), the transceiver is effectively transmitting 80 kbps of full duplex synchronous data.

The burst's ten bits of digital data are input on three different pins of the UDLT master. The first eight bits are serially received from the Receive Data Input (Rx) pin. The ninth bit is from the Signaling Bit Input (SI1) and the tenth bit is from the SI2 pin. These ten bits are formatted together and shipped out from the chip on the LO1 and the LO2 pins (Line Driver Outputs). After being transmitted across the line and received on the LI pin of the slave UDLT, eight bits of data are serially output through the slave's Transmit Data Output (Tx) pin, one bit on the SO1 and one bit on the SO2 (Signaling Bit Output). Then the slave UDLT sends a similar burst to the master UDLT.

DLT VS. UDLT

Since the MC145418/19 Digital Loop Transceiver (DLT) chip set is very similar to the UDLT, it is not difficult to adapt

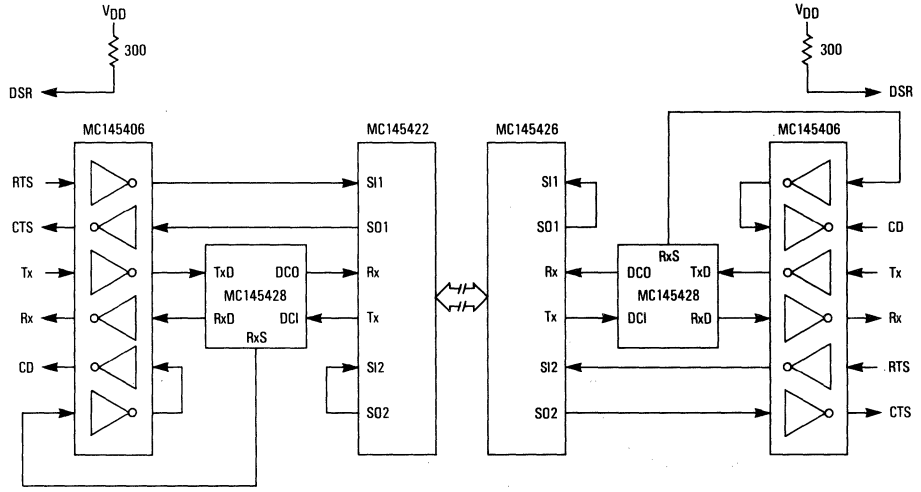

Figure 1. Limited Distance Modem Block Diagram

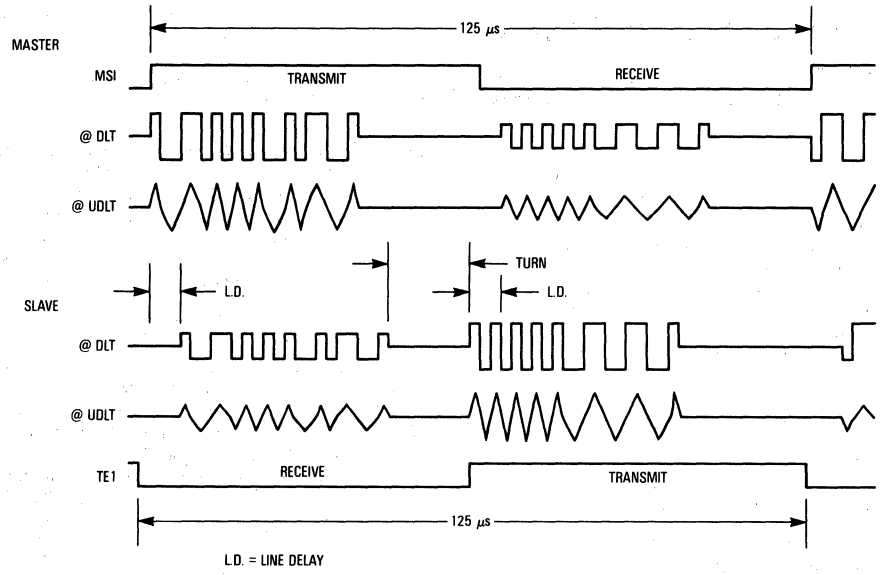

Figure 2. 80 kbps MDPSK Timing Diagram

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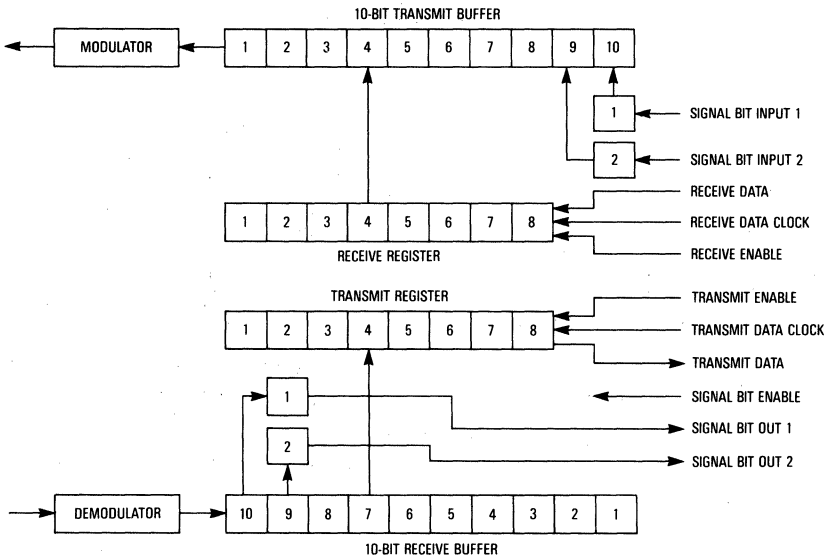


Figure 3. UDLT Receive and Transmit Registers

AA8929-1

this LDM to use the DLT. There are three main differences between the UDLT and the DLT chips. The most important difference between the chips is that the UDLT automatically adjusts the thresholds on the receive circuitry. This allows the UDLT to optimize its reception to a particular line's attenuation level. The DLTs threshold is externally set , so typically this receive optimization will not be achieved, unless some rather complex circuitry is implemented. Also, the DLT requires external drivers and transmits square waves instead of triangular waves. In conclusion, the UDLT has on board driver and threshold adjust circuitry, but the DLTs basic approach allows driver and threshold design flexibility.

SIGNALING PINS FOR RTS/CTS HANDSHAKE

This LDM uses the SI1, SI2, SO1 and SO2 pins of the master and slave for a RTS/CTS handshake. To perform this task, the signaling channels are used for transmitting the RTS/CTS handshake. The input at SI1 of the master UDLT is the RTS signal. This information is transmitted to the SO1 of the slave UDLT chip. At this point, the signal is looped around into SI1 of the slave UDLT, and it is transmitted to SO1 of the master UDLT. This signal at SO1 is the master's CTS signal. A similar configuration is used for the slave's RTS/CTS handshake on the SI2/SO2 channel. This allows the RTS/CTS handshake to verify that the communication link is operating.

DATA SET INTERFACE

Since most data from a terminal is an asynchronous format, the Data Set Interface (DSI) is needed to convert data from an asynchronous to a synchronous format and vice versa. At TxD of the DSI, the asynchronous signal should begin with a start bit (logic 0). After following with an eight or nine bit data word, the format ends with one or more stop bits (logic 1). The rate that the data is loaded into the DSI is determined by the internal bit rate generator, whose rate, if 38.4 kbps or less, is selected by BR1, BR2 and BR3 (Baud Rate Select Pins). An external bit rate generator can be used for data rates higher than 38.4 kbps.

Once in the DSI, the data is stripped of its start and stop bits and loaded in a register. Next, the data is checked for a break condition, and one of three types of words is sent, under the timing control of the DC, CM and DOE pins. If a break condition is recognized, the break flag (11111110) is transmitted. If data is in the register, it is dispatched. Finally, if no data is in the register, a synchronizing flag (01111110) is sent. However, regardless of data being in the transmit register, a synchronizing flag is also transmitted on a regular basis to verify that synchronization is intact. Furthermore, the transmit circuitry inserts a binary 0 after five continuous 1's of data, so neither pattern, (11111110) or (01111110), can be sent as data.

At DCI, DC, CM and DIE control the synchronous data's receive loading into the DSI. Once loaded, the DSI's receiver determines if the data is break or synchronizing information. If it is a break or synchronizing flag, the appropriate action is taken. If it is not, the data is loaded into a receive register. From this register, data words are taken, start and stop bits are added and the asynchronous word is output on RxD (Receive Data) at the baud rate selected by BR1, BR2 and BR3. Figure 4 is a block diagram of the DSI.

MC145428
DATA SET INTERFACE

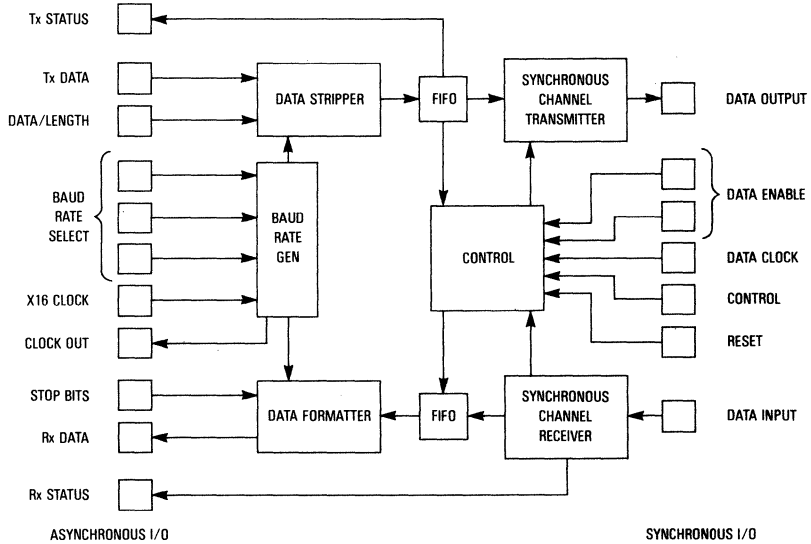


Figure 4. DSI Block Diagram

AA9544-1

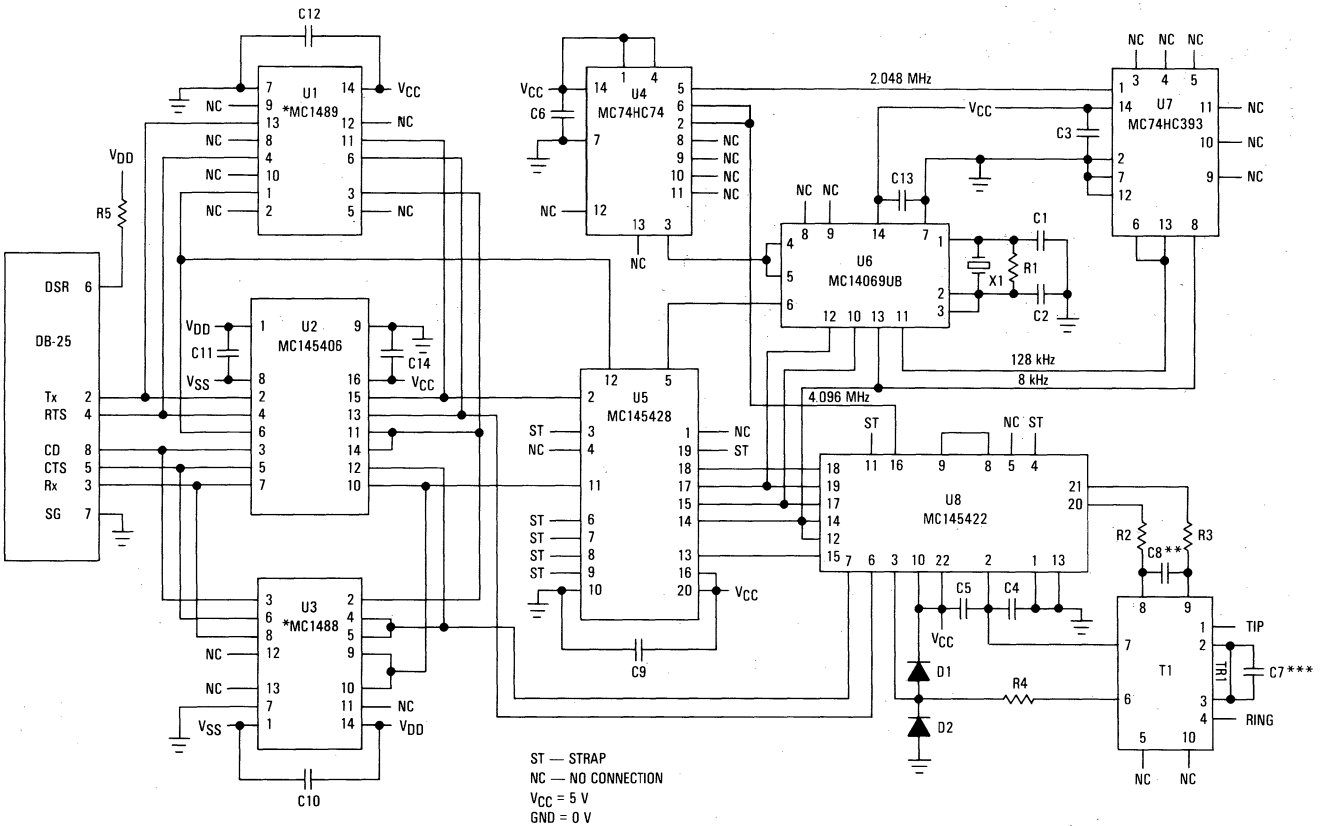
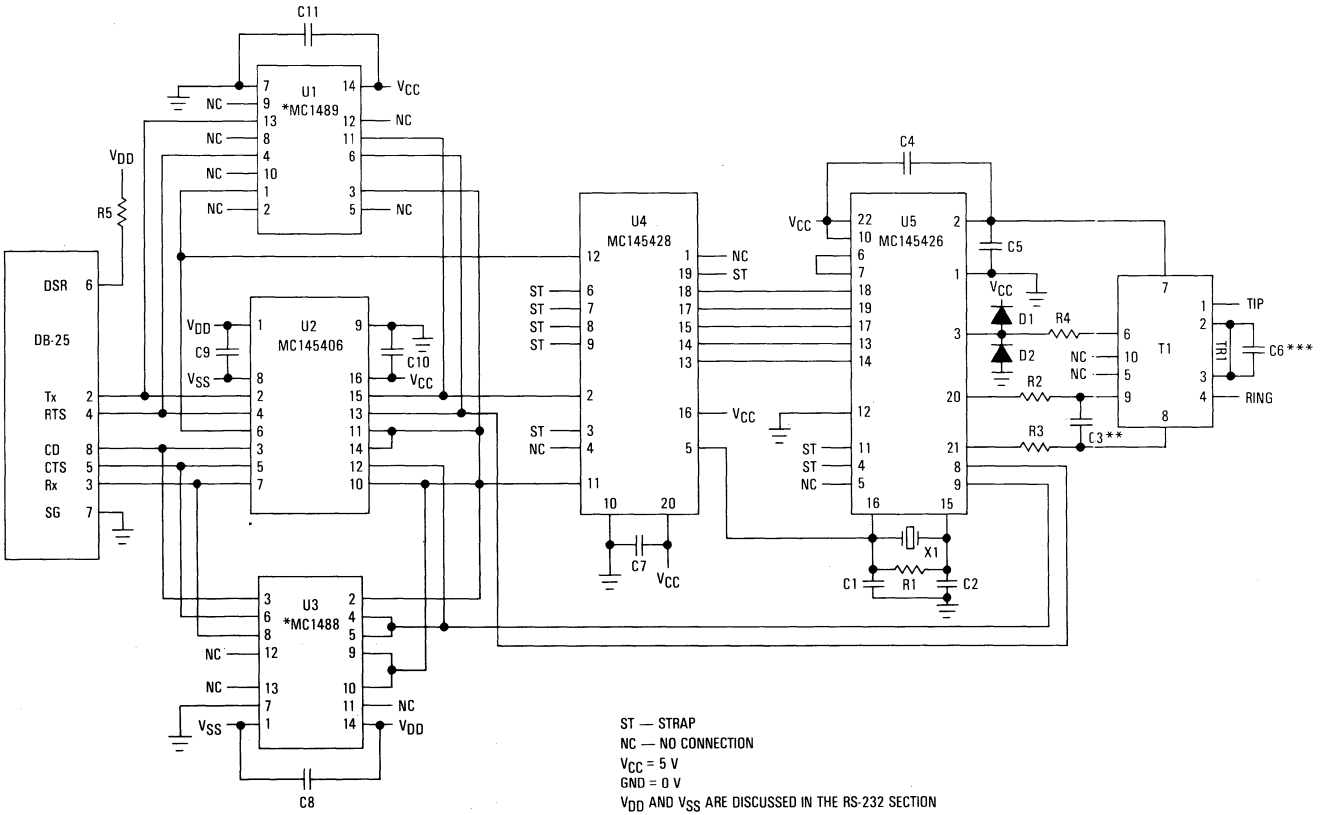


Figure 5. Master Limited Distance Modem



*MC1489 and MC1488 used when MC145406 not used
**C3 is optional filtering.
***TR1 should be cut when C6 is used

Figure 6. Slave Limited Distance Modem

RS-232C DRIVER/RECEIVER

The last integrated circuit discussed is the RS-232C interface. Either the MC145406 or the MC1488/MC1489 Driver/Receiver, which both fulfill the electrical specifications of EIA Standard RS-232C and CCITT Recommendation V.28, can be used. The receivers invert the signal and convert the RS-232 signals to standard five volt logic levels, and the drivers invert the signal and convert five volt logic levels to RS-232 voltage levels.

The MC145406 is a CMOS RS-232 chip with three drivers and three receivers. This chip operates with a five volt supply and ±5 to ±12 volt supplies. Although the MC145406 chip will work with ±5 volt supplies in most systems, the voltage supplies should be at least ±7 volts to meet the RS-232 driver specification. For full RS-232 compliance, the driver's output must be between 5 volts and 15 volts for a logical 0, and it must be between -5 volts to -15 volts for a logical 1.

The MC1488 is a quad line driver. For the MC1488 to comply with the RS-232 driver requirements, a minimum power supply of ±8 volts must be used. However, the chip will operate effectively in most systems with the positive supply voltage varying from +7 to +15 volts. The MC1489 is a five volt quad line receiver.

RS-232C CONTROL AND SIGNALS

As seen in Figure 5, the master LDM schematic, and Figure 6, the slave LDM schematic, asynchronous control and data signals enter the LDM at RS-232 voltage levels through a DB-25 connector. Figure 7 shows a DB-25 connector which is the standard computer terminal connector. Pins 2,3,4,5,6,7,8 transmit the following information:

Pin 2: Transmit Data (Tx)
Pin 3: Receive Data (Rx)
Pin 4: Request to Send (RTS)
Pin 5: Clear to Send (CTS)
Pin 6: Data Set Ready (DSR)
Pin 7: Signal Ground (GND)
Pin 8: Carrier Detect (CD)

The Tx and RTS signals are fed into the receivers, and the Rx, CTS and CD signals are outputs of the driver. For the CD signal, one of the receivers inverts the signal from the RxS pin of the DSI. When the DSI is in asynchronous status, this inversion gives the CD a logic 0. The output of that receiver is then put into a driver to obtain RS-232 voltage levels. The DSR pin is connected to the RS-232 positive power supply through a 300 ohm resistor. Therefore, DSR will go active whenever the power supply is on. The GND pin is connected to the system's ground. The remaining pins used of the DB-25 connector are routed to the RS-232 Driver/Receiver.

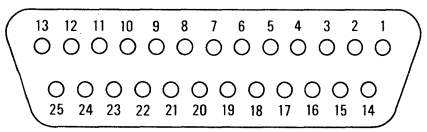


Figure 7. DB-25 Connector

TRANSFORMER INTERFACE

The transformer interface greatly affects the UDLTs capabilities. It performs the functions of impedance matching, bandwidth limiting, increasing receive voltages to required threshold levels and input protection. At 256 kHz, 26 AWG wire's characteristic impedance is 110 ohms. The source resistors from the LO1 and LO2 pins are chosen to be 220 ohms. With a transformer turns ratio of 2:1, the line side's characteristic impedance is 110 ohms. This configuration impedance matches the twisted pair.

The UDLTs minimum output voltage from the LO1 and the LO2 pins is 2.25 volts peak. Half of the voltage is lost across the 220 ohm source resistor. That voltage of 1.12 volt peak is halved again by the 2:1 turns ratio of the transformer to 0.56 volts peak. At 256 kHz, 26 AWG wire attenuates a signal level of 18 decibels-per-kilometer. After traveling a distance of two kilometers the signal will have attenuated 36 decibels. At the line side of the transformer, the minimum signal level is 8.9 millivolts peak. A turns ratio of 1:4 in the transformer windings brings the signal level up to 35.6 millivolt peak. This voltage is divided between a resistor from the transformer to the LI pin and an internal resistance. At worst case, 29 millivolt peak are at the LI pin — within the 25 millivolts peak minimum allowed signal.

The UDLTs maximum voltage output is 3.0 volts peak. Because of the voltage being halved by the source resistors and the transformer windings, the transmit signal level at the line side is 0.75 volt peak. With a short loop, the signal level drop is negligible, so the signal level at the receiving transformer is about 0.75 volts peak. With the 1:4 turns ratio at the receiving transformer, the signal level at LI will be 3.0 volts peak, which exceeds the 2.5 volt peak maximum input at LI. A signal level greater than 2.5 volts peak will inject current into the UDLTs substrate. This action will distort the modulator's output, thus creating bit errors. Consequently, protection diodes and resistors are needed to clamp the input at LI. The demonstration board's transformer configuration is shown in Figure 8. The LI pin's protection includes a 1 kilohm resistor between the LI pin and the diodes. This resistor is not on the

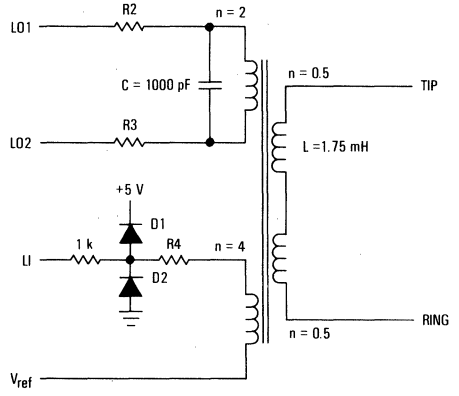


Figure 8. Transformer Configuration Used in LDM Schematic

demonstration board. Typically, the external diodes will turn on before the chip's internal diodes, so the external diodes will shunt most of the current. However, the 1 kilohm resistor will further ensure that the external diodes turn on first.

The maximum power bandwidth of the UDLT is 8 to 512 kHz, but to improve line settling, it is desirable to use a 20 to 512 kHz bandwidth. To make the lower corner of the bandwidth 20 kHz, the inductance of the transformer windings is chosen to be 1.75 millihenries. To make the upper corner of the bandwidth 512 kHz, a 0.001 microfarad capacitor is placed in parallel with the transmit tap. If battery feed is used, further input protection is advised. Figure 9 shows a more durable transformer configuration. Transformers fulfilling these specification can be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521

Part Number: P/N P-1358-A

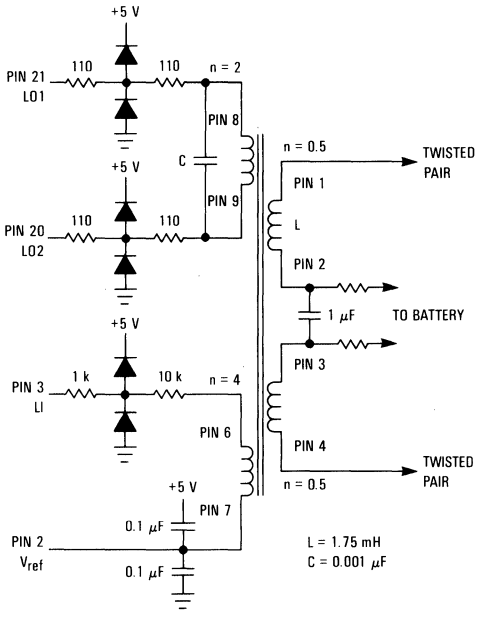


Figure 9. Battery Feed Transformer Configuration

LDM BOARD OPTIONS

A picture of the LDM demonstration board is shown in Figure 10 and 11. Many of the UDLT and DSI features are made available on the demonstration board using straps. These UDLT features include:

$\overline{LB}$: In the master, a low disconnects the LI pin from the internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator to the demodulator. In the slave, a low on the $\overline{LB}$ pin makes the incoming demodulated data going to Tx replace the incoming data on Rx.

$\overline{PD}$: A low powers down the UDLT, except for the receive circuitry.

The DSI features that can be controlled using the straps include:

SB: A low selects outputting one stop bit per data word, and a high selects outputting two stop bits.

DL: A low selects operating with eight bit data words, and a high selects operating with nine bit data words.

Reset: A low clears the internal FIFO, disables TxD, and forces TxS and RxS low.

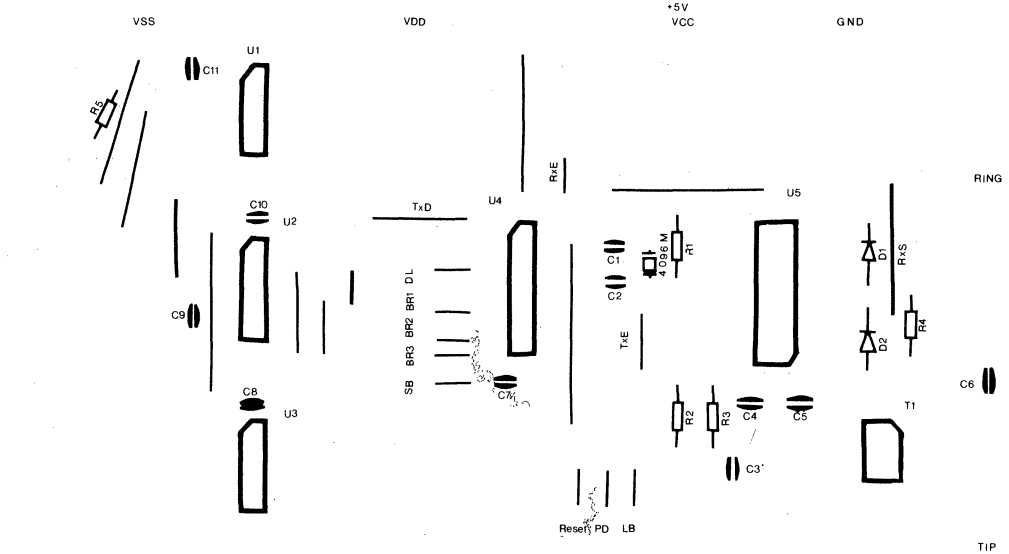
BR1, BR2, BR3: These pins select the asynchronous data rate.

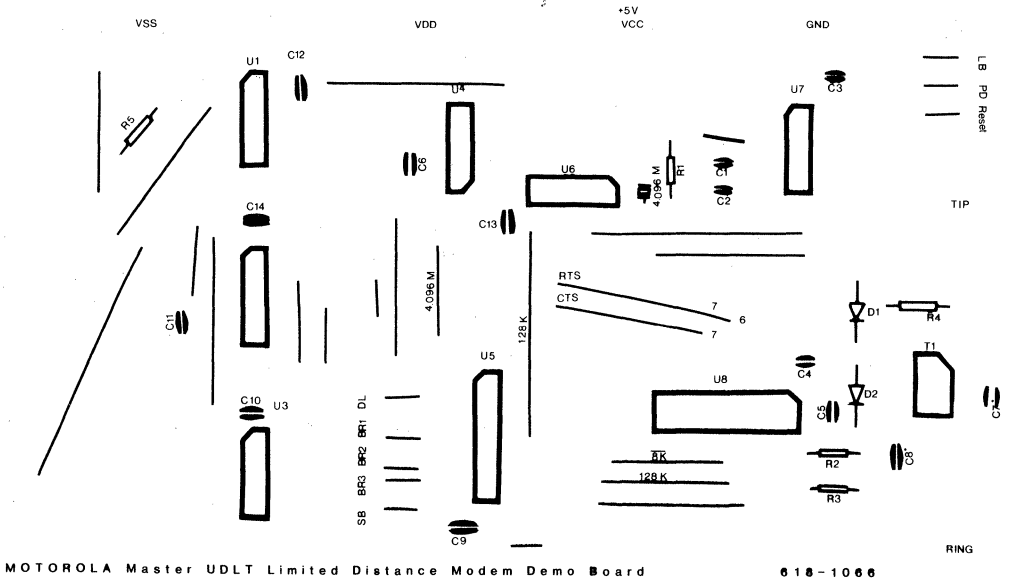
For more information, refer to the individual data sheets. The top of the LDM board shows suggested straps for these functions. These straps select one stop bit, an eight data word, an inactive Reset, a 9600 baud asynchronous data rate, an inactive loop-back and an inactive power-down.

For battery feed applications, C6 of the slave LDM and C7 of the master LDM can be inserted, and the trace between these pins should be broken. This capacitor allows ac signals to pass through the transformer, but keeps dc power across the capacitor to be fed into the system's power supply. C3 of the slave LDM and C8 of master LDM provide filtering for the upper corner of the bandwidth. If this filtering is not desired, these capacitors may be omitted, but their insertion is recommended.

CONNECTORS

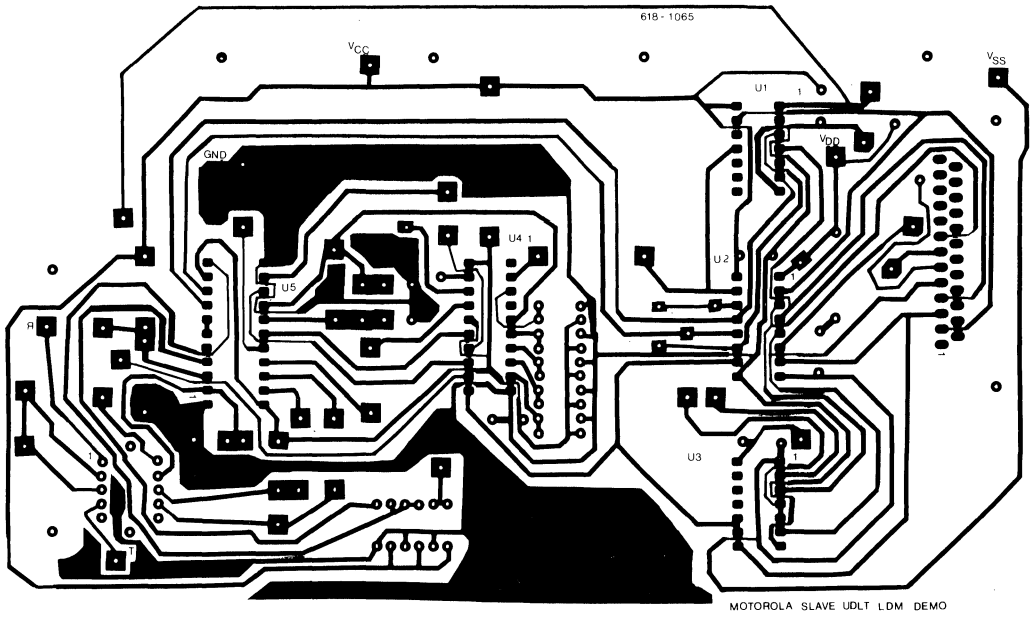
On the demonstration board, V_{SS} and V_{DD} are only used to power the RS-232 circuitry. V_{SS} is the most negative power supply, and V_{DD} is the most positive power supply. The RS-232C Driver/Receiver section explains the appropriate voltage ranges for using either the MC145406 or the MC1488/MC1489. V_{CC} is the board's five volt supply, and GND is the board's digital ground. Tip and Ring are the connections for the twisted pair wire. The 25 pins on the left side of both the slave and the master board is for the DB-25 connector.

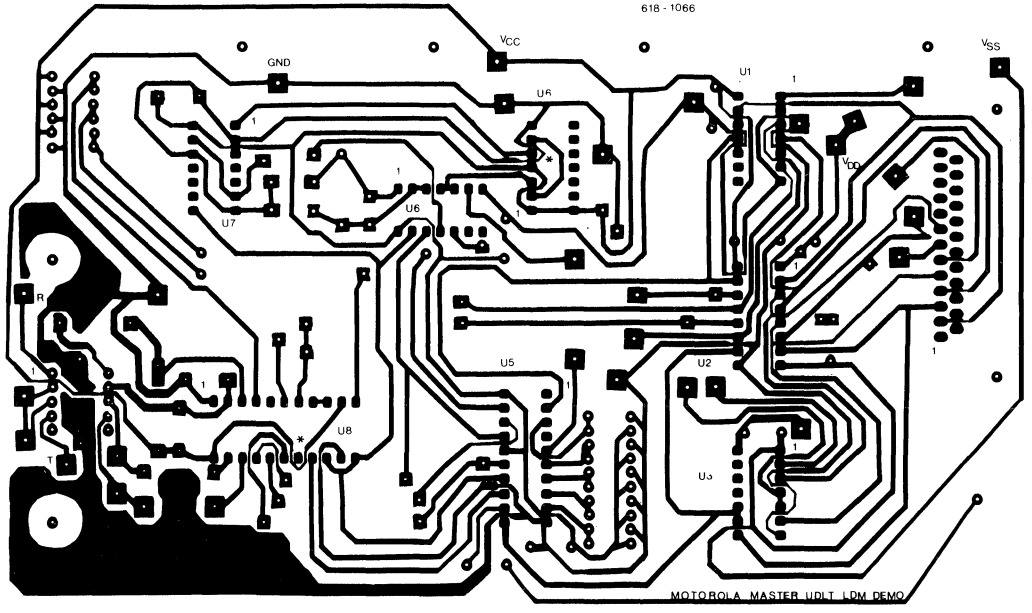




NOTE: Drawings are not actual size.

Figure 10. Photostat of LDM Demonstration Board - Front





*External to the demonstration board-back, pin 6 of the MC74HC74 should be connected to pin 16 of the MC145422

NOTE: Drawings are not actual size.

Figure 11. Photostat of LDM Demonstration Board - Back

Table 1. Limited Distance Modem Parts List

Master LDM		Slave LDM	
R1: 10 MΩ	R4: 10 kΩ	R1: 10 MΩ	R4: 10 kΩ
R2: 220 Ω	R5: 300 Ω	R2: 220 Ω	R5: 300 Ω
R3: 220 Ω		R3: 220 Ω	
C1: 20 pF	C8: 1000 pF	C1: 20 pF	C7: 0.1 μF
C2: 20 pF	C9: 0.1 μF	C2: 20 pF	C8: 0.1 μF
C3: 0.1 μF	C10: 0.1 μF	C3: 0.001 μF	C9: 0.1 μF
C4: 0.1 μF	C11: 0.1 μF	C4: 0.1 μF	C10: 0.1 μF
C5: 0.1 μF	C12: 0.1 μF	C5: 0.1 μF	C11: 0.1 μF
C6: 0.1 μF	C13: 0.1 μF	C6: 1.0 μF	
C7: 1.0 μF	C14: 0.1 μF		
D1: 1N914	D2: 1N914	D1: 1N914	D2: 1N914
X1: 4.096 MHz		X1: 4.096 MHz	
U1: MC1489		U1: MC1489	
U2: MC145406		U2: MC145406	
U3: MC1488		U3: MC1488	
U4: MC74HC74		U4: MC145428	
U5: MC145428		U5: MC145426	
U6: MC14069UB			
U7: MC74HC393			
U8: MC145422			
T1: Lepco P/N P-1358-A		T1: Lepco P/N P-1358-A	

AN948

Data Multiplexing
Using the Universal Digital Loop Transceiver and the Data Set Interface

INTRODUCTION

Data multiplexers find applications where clusters of terminals are connected to a central computer and in systems where modems are pooled at a common location. Combining the signals from the various terminals onto one multiplexed data link simplifies wiring and reduces expenses. Sharing the cost of the multiplexer among the several terminals results in a lower net cost compared to installing and maintaining individual cables for each terminal. While present day multiplexers are economical, new ICs from Motorola make possible enhanced performance multiplexers for a fraction of the cost of existing devices.

This Application Note will describe the design of a short-haul multiplexer for asynchronous data at rates up to 9600 baud. The mux combines eight full-duplex data channels along with eight end-to-end RS-232 control signals onto a single pair of telephone wire for distances up to 2 km. Motorola's Universal Digital Loop Transceivers (MC145422/26 UDLTs) master/slave high-speed synchronous data transceivers and Data Set Interface (MC145428 DSI) full-duplex asynchronous to synchronous converter form the heart of this multiplexer. A few MSI CMOS ICs complete the design.

Figure 1 illustrates a typical system with the terminals in a departmental situation multiplexed onto one high-speed data link. RS-232 control signals are passed transparently through the multiplexer so the terminals have direct access to the controls of the modems. This multiplexer system transports one control signal bidirectionally for each data channel. As will be described below, other configurations may easily be constructed with simple wiring changes.

CHARACTERISTICS OF THE UDLTs

The UDLTs are synchronous data transceivers capable of transporting 80 kbps of full-duplex data over ordinary twisted pair 26 to 19 gauge telephone wire at distances of up to 2 km. These devices utilize a 256 kilobaud MDPSK ping-pong burst modulation technique for transmission. Three logical data channels, one of 64 kbps and two of 8 kbps each are exchanged in bursts of 10 bits every 125 μs frame. MDPSK timing is shown in Figure 2. The master initiates a ping-pong frame by bursting 10 bits of data to the slave beginning on the rising edge of an externally generated Master Sync Input (MSI). The modulator's analog output signal (LO1, LO2) is shown referenced to MSI. Upon receiving the last bit from the master, the slave responds with a 10 bit burst of its own after a four baud delay. The slave's modulator output (LO1, LO2) is shown referenced to its own Transmit Enable 1 (TE1). Depending on the transmission line characteristics and length, the actual time of arrival of the slave's return burst at the master will vary due to the propagation time of the signal

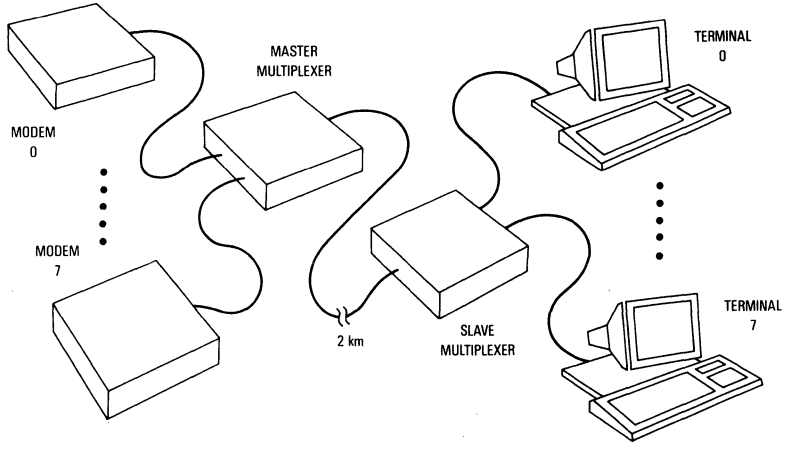


Figure 1. Typical Multiplexer Application

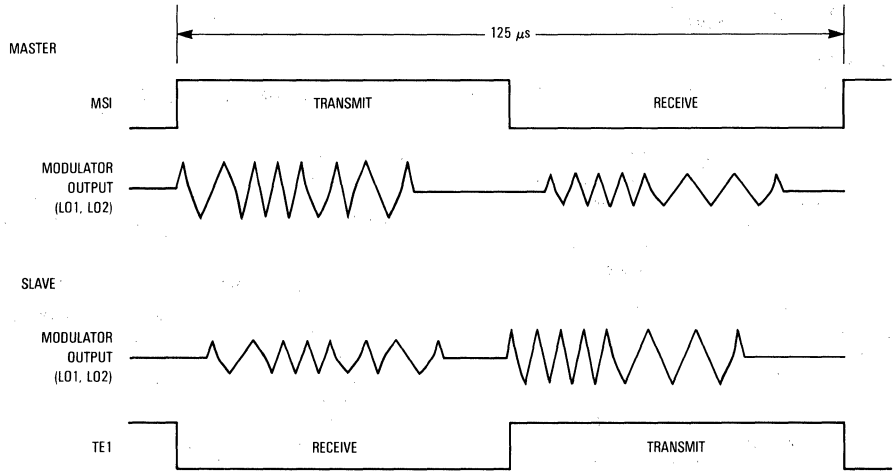


Figure 2. UDLT Timing

between UDLTs. On excessively long lines, propagation time down the transmission line results in collisions between the master and slave bursts so maximum line length is limited to 2 km with 26 gauge wire. The slave's TE1 is generated internally upon completion of demodulation of the burst from the master. TE1 remains high for eight data clock (128 kHz) periods and returns low until another burst is received. This process is repeated every 125 μs. Since both master and slave devices exchange data every frame in a half-duplex manner at a 256 kilobaud rate, an effective full-duplex rate of 80 kilobaud is accessible to the user.

The bursts of data on the transmission line use Modified DPSK signals to reduce EMI and susceptibility to crosstalk from other signals in telephone cables. The frequency spectrum consists of peaks at 128 kHz and 256 kHz and their odd harmonics. Only a small amount of energy is present in the frequency bands used by analog telephone service, so UDLT signals may be placed on adjacent pairs in cables with ordinary telephone signals with no degradation of performance. The power spectral density at 76 kHz is approximately 18 dBm and at 28 kHz the level is less than −30 dBm. Because there is no signal energy at very low frequencies, dc energy may be transported on the transmission line to power the remote multiplexer unit. Details of this feature will be described later.

The UDLTs have internal buffers to store and prepare synchronous data for transmission. Eight bits for the 64 kbps channel are serially input and output every 125 μs frame. The two 8 kbps channels each have one bit input and output every frame. The master and slave UDLTs synchronous timing is shown in Figures 3 and 4 respectively. Both figures illustrate the transmit and receive timing for the eight bit words on Tx and Rx, and the timing for the two signalling bits, both inputs (SI1, SI2) and outputs (SO1, SO2).

The master UDLT timing shown in Figure 3 requires external timing signals of 8 kHz for MSI, TE1, RE1, and 64 kHz up to 2.56 MHz may be used for the TDC/RDC pin. This application uses 128 kHz. Eight bits of the 64 kbps data channel received from the slave are output on the Tx pin on the first eight rising edges of TDC/RDC while TE1 is high. Data to be sent to the slave is input on the Rx pin on the first eight falling edges of TDC/RDC while RE1 is high. In this application TE1 and RE1 are connected together so data is input and output simultaneously. Data on the 8 kHz signalling channels are input on SI1 and SI2 pins and output on SO1 and SO2 pins on MSI's rising edge.

The slave UDLT timing (shown in Figure 4) is similar to the master except that the slave synchronizes to the master's bursts and generates its own clocks and enables. The eight bits of the 64 kbps data channel received from the master are presented on the Tx pin on the rising edges of CLK while TE1 is high. Data to be transmitted to the master is loaded in on the Rx pin on the falling edges of CLK while RE1 is high. Signalling bits on the 8 kbps channels to and from the master are input at SI1, SI2 and output at SO1, SO2 on TE1's rising edge.

The master UDLT has pin controlled Power-Down ($\overline{PD}$) and Loop-Back ($\overline{LB}$) features which can be used for system testing. Also available on the master is Signal Insert Enable (SIE) which enables the insertion and extraction of an 8 kbps channel into the LSB of the 64 kbps channel. In this application SIE is unused and held low. The signal enable pin ($\overline{SE}$) is a three-state control pin which when held high enables $\overline{PD}$, $\overline{LB}$, and the two signalling bits (SO1 and SO2) allowing these signals to be bussed to a microprocessor.

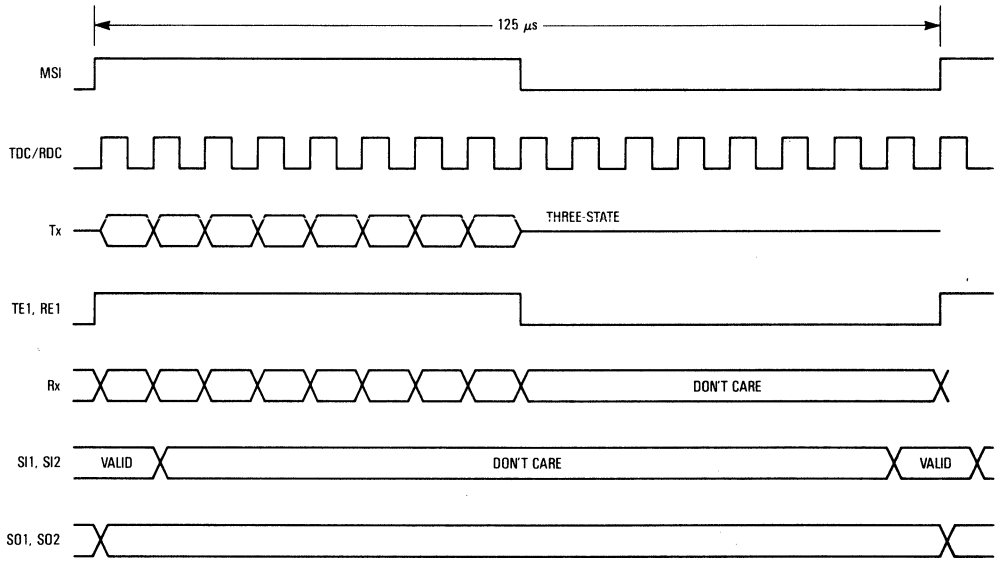


Figure 3. Master Timing

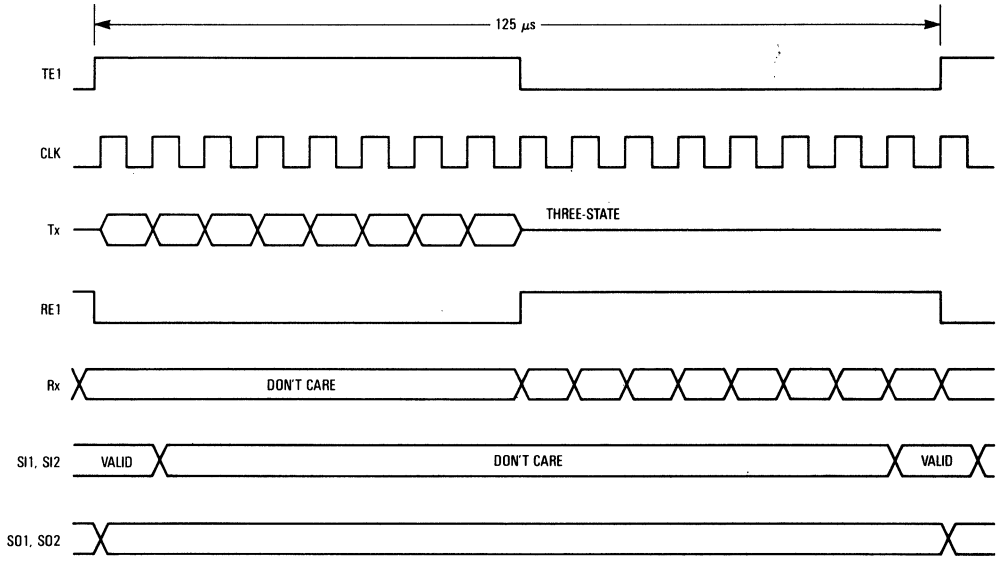


Figure 4. Slave Timing

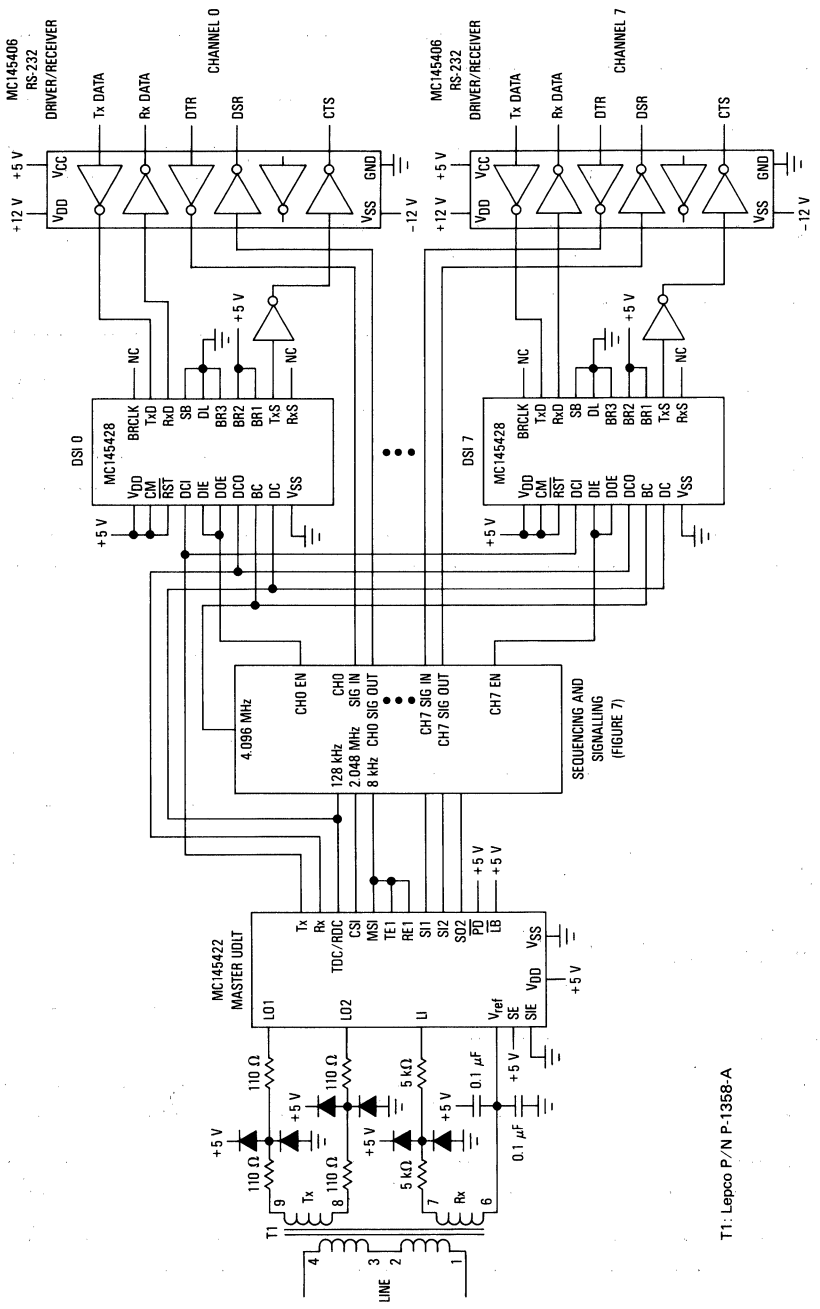


Figure 5. Master Unit Interconnect

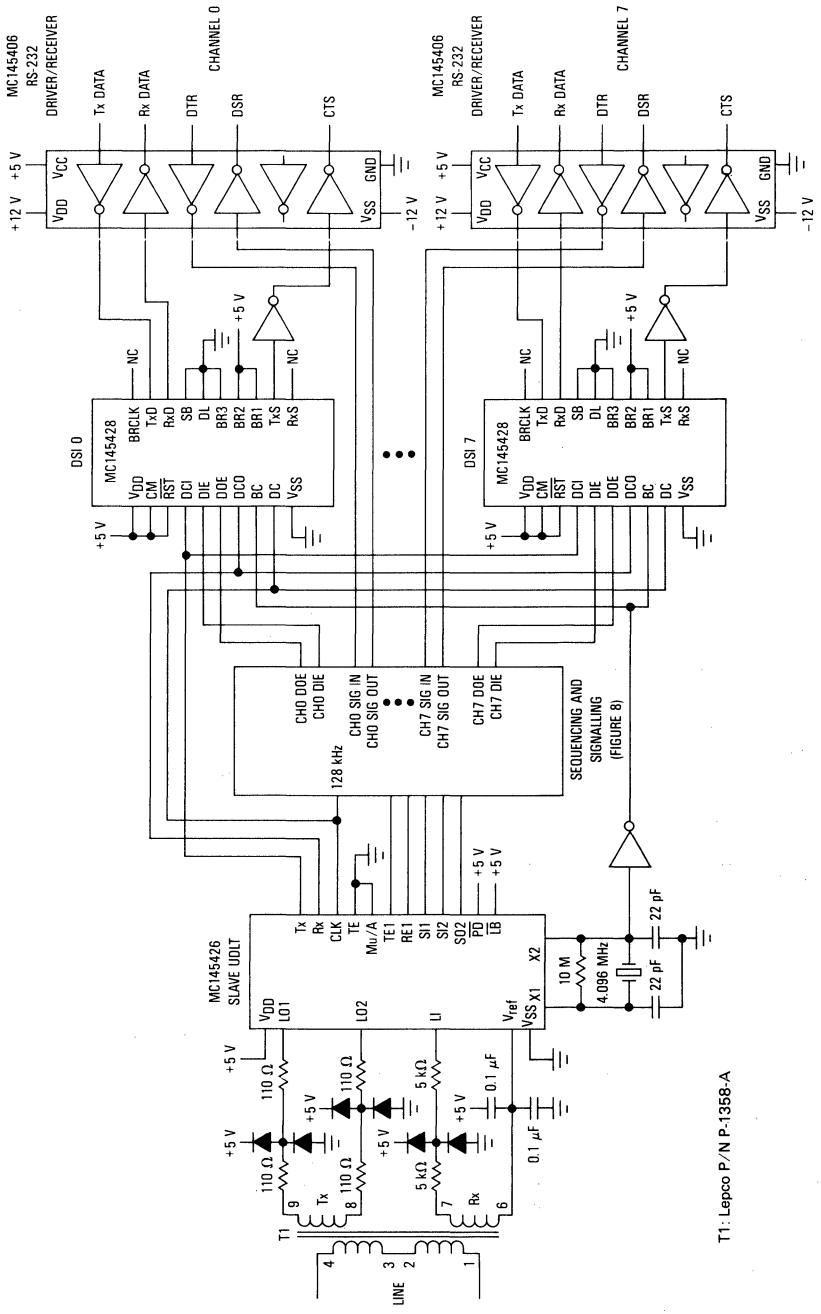


Figure 6. Slave Unit Interconnect

3

TRANSFORMER INTERFACE

The duplexer function, separating transmit and receive bursts on a single twisted pair wire is automatic with UDLTs. The receiver input is blanked while the transmitter is active so the transmitted signal is ignored by the demodulator circuits. The receiver unblanks when the transmitter finishes its burst to search for the return burst from the other end. Automatic duplexer action allows a simple transformer to be used for the interface between the transmission media and UDLTs shown in Figures 5 and 6. The transformer Tx winding and the associated padding network match the transmitter output to the impedance of the transmission line. The Rx winding steps up the signal from the far end to compensate for the loss in the matching network. The characteristic impedance of twisted pair telephone wire in the frequency range used by the UDLTs is approximately 110 ohms. Matching this impedance requires resistors of 220 ohms in each leg of the Tx winding. The impedance of 440 ohms when transformed through a 2:1 turns ratio results in a match to 110 ohms. 12 dB of loss is also introduced. The 12 dB is made up in the Rx winding which has a 4:1 step-up from line to receiver input.

Protection of the UDLTs against transients induced onto the transmission line is accomplished by adding clamp diodes to the padding networks. It is convenient to split the 220 ohm resistors into two 110 ohm resistors and place the clamps at the junction of the resistors. The same technique is used at the receiver inputs.

CHARACTERISTICS OF THE DSI

The DSI is a device which provides full-duplex asynchronous to synchronous conversion. It allows the user to select asynchronous data formats and baud rates. The synchronous port has selectable timing for easy interfacing to a variety of systems. The asynchronous port characteristics are controlled by the Stop Bit select (SB), Data Length select (DL), Baud Rate select (BR1-BR3) pins. Synchronous data is under the control of the Data Output Enable (DOE), Data Input Enable (DIE), Data Clock (DC), and Clock Mode (CM) pins. Asynchronous data is sampled at 16 times the selected baud rate. Logic circuits search the asynchronous data for a start bit, eight or nine data bits and one or two stop bits. When valid start and stop bits are found, they are removed from the character and the remaining eight or nine data bits are loaded into the transmit FIFO for transmission on the synchronous port. The Tx Status pin goes low when the transmit FIFO is more than half full. This signal may be used for a local Clear-To-Send indication to the data device on the asynchronous port. Special characters are generated and transmitted on the synchronous port to synchronize the receiver of the remote DSI to the character boundaries. At the remote DSI synchronous data is reassembled into eight or nine bit characters, start and stop bits are added and the data is transmitted out on the asynchronous port.

Since start and stop bits are removed from the asynchronous data before transmission on the synchronous port, some data compression is achieved. For example, asynchronous data at 9600 baud with eight data bits and one stop bit is compressed to 7680 baud on the synchronous channel. This makes possible the use of an 8 kbps synchronous channel to transport 9600 baud data. However, since sync and break characters consisting of data patterns 01111110 and 11111110 respectively are exchanged between DSIs every so often, the effective data compression is somewhat reduced. Zero bit insertion on the synchronous data between DSIs is used to eliminate the possibility of data imitating either of these characters (the inserted zeros are removed by the synchronous receiver). The multiplexer allocates the UDLTs 64 kbps synchronous channel to each DSI for one 125 μs ping-pong frame out of every 1 ms data frame. This results in an 8 kbps synchronous channel for each DSI. Under certain circumstances, with binary data, zero insertion may cause the transmit FIFO to overrun. If hex 'FF' characters are input to the DSI on the asynchronous port at 9600 baud with minimum time between characters, inserted zeros and sync characters cause the effective data rate to increase from 7680 baud to approximately 9400 baud. Since the synchronous channel supports only 8 kilobaud, an overrun of the Tx FIFO will occur. The TxS pin will go low approximately 5 ms before an overrun occurs and this indication may be used to stop the flow of new asynchronous data until the FIFO clears out. When ASCII data is used, only 6 characters (>(3E hex), ?(3F hex), I(7C hex), ~(7E hex), DEL(7F hex), and Blank(7D hex)) generate stuffed zeros. Fortunately, it is unlikely that these characters will be sent in large enough groups to cause FIFO overruns. In applications where ASCII data is transported, eight 9600 baud channels may be multiplexed onto this system's 64 kbps synchronous channel. If binary data is transported, a 16 kbps synchronous channel must be allocated for each DSI, resulting in a four channel multiplexer. This guarantees that even with maximum zero insertions, FIFO overruns will not occur.

OCTAL MULTIPLEXER SYSTEM DESCRIPTION

This multiplexer system fully exploits the DSI chips and the UDLT transceiver pair. The UDLTs 64 kbps channel transports the synchronous data from the DSIs. One of the UDLTs 8 kbps channels is used to synchronize the multiplexing of the eight data channels, and the other 8 kbps channel is used to transport eight RS-232 control signals.

The multiplexer system consists of two units, a master and a slave. Figure 5 illustrates the interconnection of the various devices within the master unit. The transformer interface to the twisted pair is shown with the previously described impedance matching and protection circuitry. The master UDLT is shown with the Tx, Rx lines along with the 128 kHz and the 4.096 MHz clocks bussed to the eight DSIs. The data channel enables and signalling lines are shown connecting the DSIs and the RS-232 driver/receivers to the sequencing and signalling block. Each DSI is shown configured for 9600 baud with eight bit character lengths and one stop bit which may be made switch selectable, if desired.

Figure 6 shows the complementing slave unit. Protection circuitry and the transformer interface are the same as the master unit. The slave UDLT generates its own clocks derived from an on-chip crystal oscillator circuit. An inverter is used to drive the eight clock inputs to the DSIs. Also shown is the sequencing and signalling interconnect to the DSIs and the RS-232 driver/receivers.

Circuitry in the sequencing and signalling blocks is shown in Figures 7 and 8 for the master and slave units respectively. All pertinent timing of the multiplexer system is shown in Figure 9. Master timing is shown in the top section, master and slave bursts on the twisted pair are shown on the line

labeled 'Transmission Line'. Slave timing is illustrated on the bottom half of the figure.

Clocks for the master UDLT are created by a 12-stage ripple counter (MC74HC4040) which is driven by a 4.096 MHz crystal oscillator. Taps at Q1, Q5, and Q9 create the 2.048 MHz (CCI), 128 kHz (TDC/RDC) and 8 kHz (MSI,TE1,RE1) clocks respectively. Inverters are needed on each line so the rising edges coincide. A pulse which synchronizes the master and slave data channel sequencing circuitry is generated when a count of 0 is reached by Q10, Q11, and Q12 of the ripple counter. This pulse is shifted through the enable shift register (MC14015B) to create eight non-overlapping enables for the DSIs. A latch (MC14013B) is used to delay the pulse so that it can be properly input into SI1 of the UDLT on the next rising edge of MSI. The delayed pulse on SI1 and the data channel enables (CH0-CH7 DOE, DIE) are shown on the timing diagram. RS-232 control data is routed to a latch by an addressable data selector (MC14051B). RS-232 control data received from the slave unit is written into an addressable latch (MC14051B). Notice that the first Q0 of the shift register is the enable to the DSI of data channel 1. Since the sync pulse arrives at the input of the shift register slightly after the clock, a one-channel offset is used to address the proper channel. This offset is transparent to the system.

Data input on the Rx pin of the UDLT is buffered until the next rising edge of MSI, when it is burst out on the transmission line. Data on SI1 and SI2 are latched in on the rising edge of MSI and transmitted in the burst which was initiated by that MSI edge. The bursts from the master (boxes with M) and the return bursts from the slave (boxes with S) on the twisted pair wire are illustrated on the 'Transmission Line'. The numbers indicate which channel's data is transported in that burst.

The system sync pulse arrives at the slave unit on the SO1 pin of the UDLT (Figure 8). It is shifted through a shift register (MC14015B) which is clocked by the RE1 pin. The Q's from this shift register enable the transmission of data from the DSIs to the UDLT. The sync pulse is delayed and shifted through another shift register clocked by TE1. The Q's from this shift register enable the DSIs to accept data from the UDLT. RS-232 control data is handled in the slave unit in a similar manner as the master with a data selector and an addressable latch. Simply offsetting the connections to the RS-232 driver/receivers realigns the data to the proper

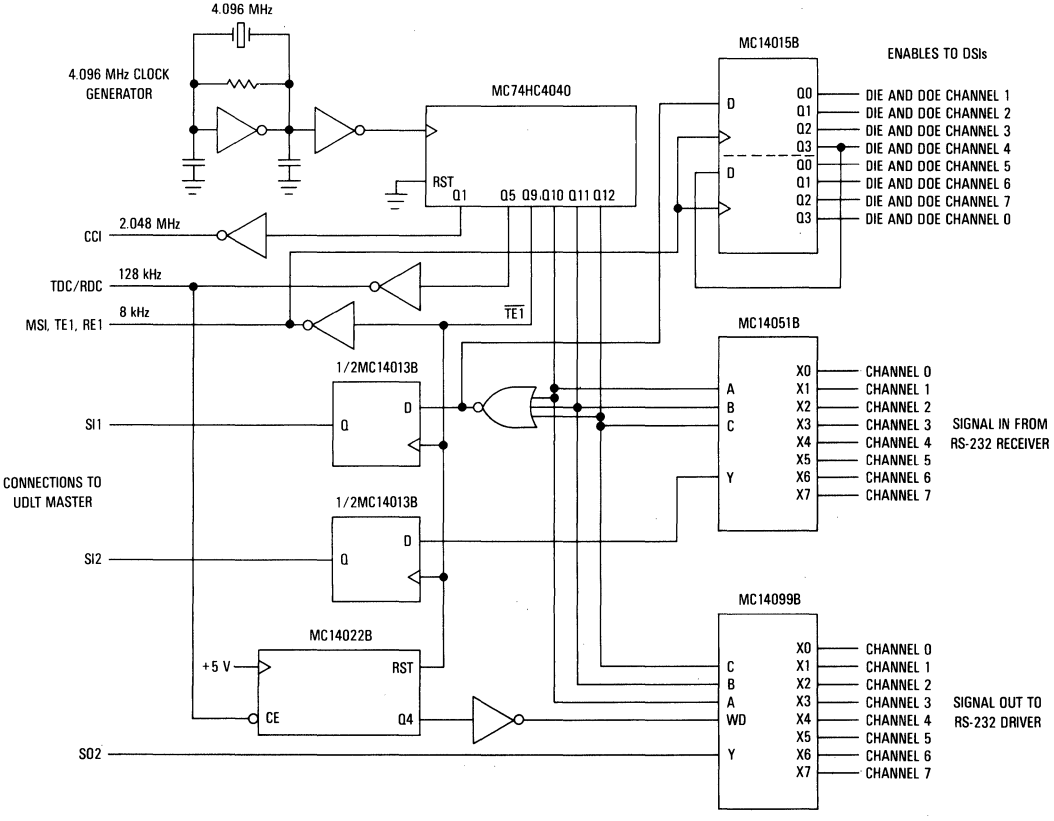


Figure 7. Master Sequencing and Signalling

channels eliminating any superfluous circuitry. Offsetting the connections to the data selector (MC14051B) similarly aligns the channels so that the data arrives at the master in the correct time slot. Following the channels on the timing diagram illustrates the concept.

ADDITIONAL CONSIDERATIONS

This multiplexer design is quite modular. If RS-232 control signalling is not desired then the circuitry can be simplified by removing the write pulse generator (MC14022B), addressable latches (MC14099B) and data selectors (MC14051B) from both units. The address generator (MC14163B) on the slave unit may also be removed. In applications where data rates of less than 9600 baud are used, the Baud Rate select pins on the DSIs need simply be reconfigured. A DIP switch can be conveniently used to set the Baud Rate, Data Length and Stop Bit pins on the DSIs. Note that the DSIs must not be set for 19.2 or 38.4 kilobaud when eight channels are multiplexed. If data rates higher than 9600 baud are desired, the individual data channels must be serviced more often by the UDLT. Because the high-speed synchronous channel between UDLTs is 64 kbps, the total bandwidth required by all of the channels must be at or below 64 kbps. The multiplexer may also be converted into a single channel limited-distance modem where data rates of up to 56 kbps can be attained.

This multiplexer, because it is all CMOS, consumes only about 175 mW per unit. One of the units may be powered by dc energy transported on the transmission line itself eliminating a power cord. The line interface transformer is designed to pass dc energy by separating the two line windings and installing a 1 μF capacitor between pins 2 and 3. Now, dc current may be passed to the twisted pair. A switching power supply may be installed in the remote unit to convert the line power to voltage levels useable by the digital circuitry. Recall that the dc resistance of 2 km of 26 AWG wire is approximately 575 ohms. This necessitates a relatively high voltage on the sending side to keep the I^2R losses in the twisted pair to a tolerable level. Usually 36 to 40 volts is satisfactory to furnish enough voltage to the remote unit. Since the transmission line is balanced, there is no ground reference between master and slave units. dc power to the twisted pair must be fed from an isolated winding on the mains transformer, so that a ground reference may be established at the remote unit. Connecting the ground references of the two units through the twisted pair will result in poor data performance due to longitudinal currents in the line.

References

Motorola Telecommunications Device Data Book DL136, 1984.

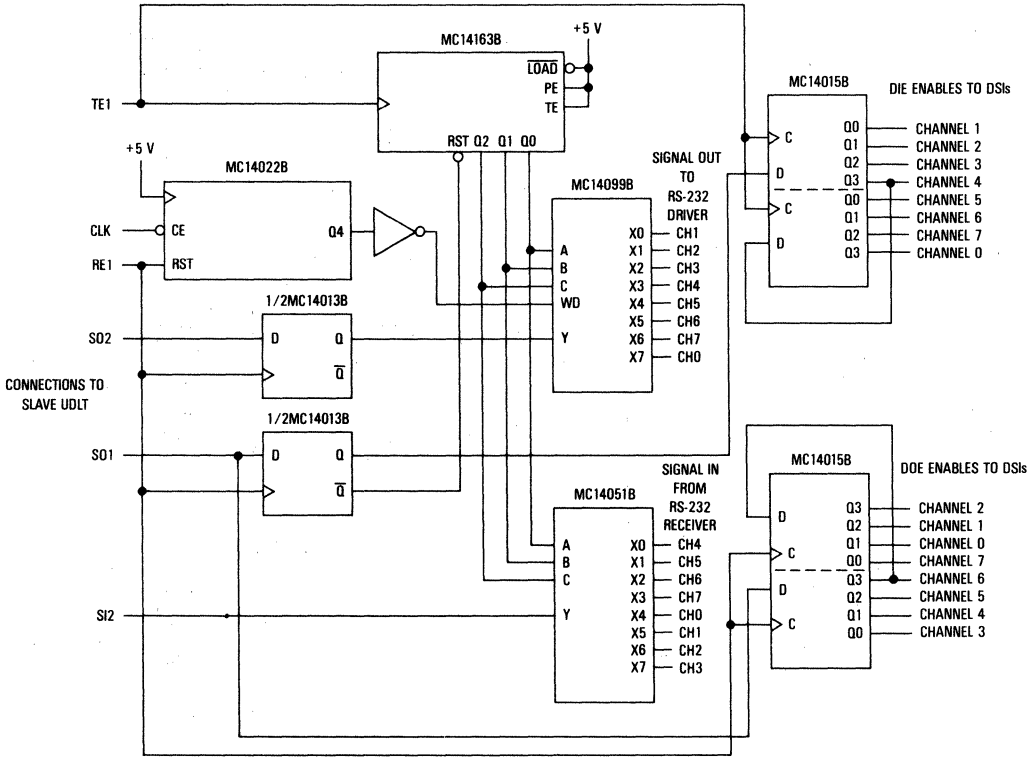


Figure 8. Slave Sequencing and Signalling

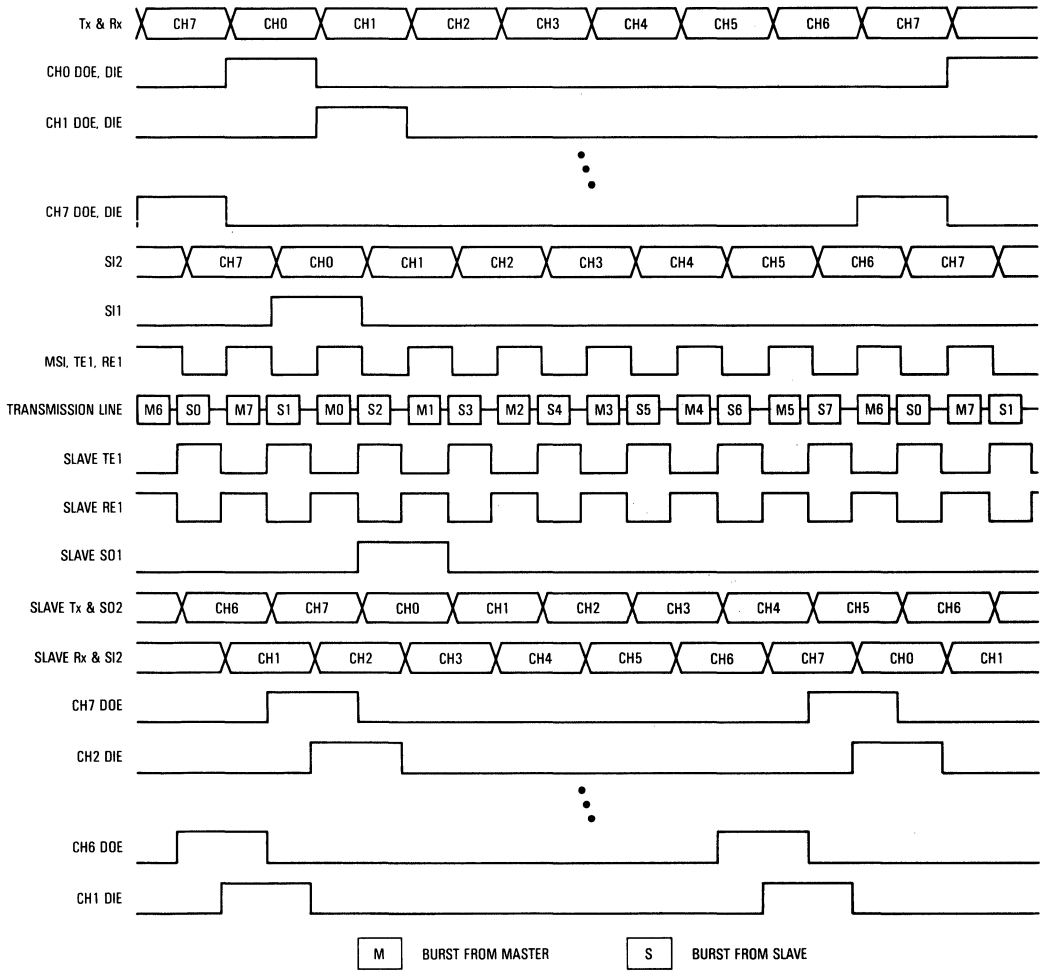


Figure 9. System Timing

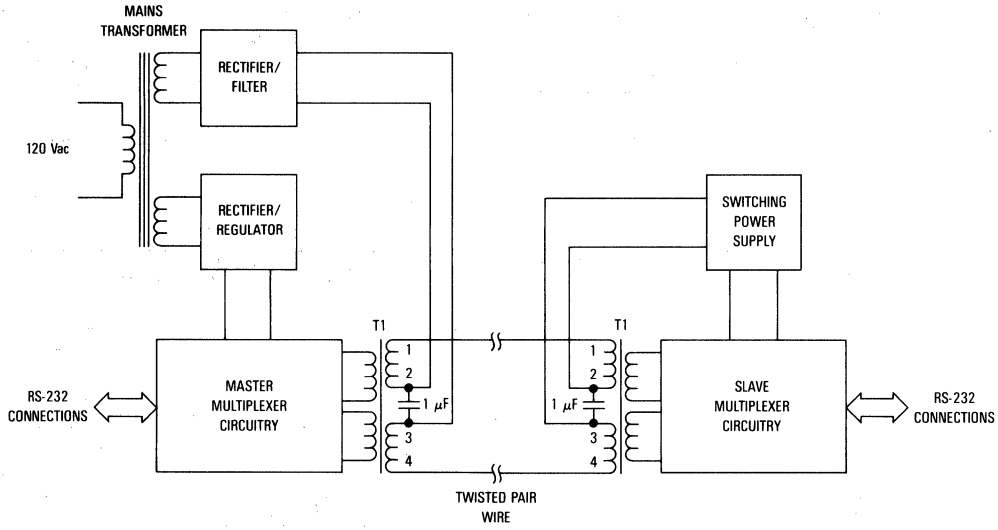


Figure 10. Powering Slave Unit From the Twisted Pair

Engineering Bulletin

By Vince Deems
Telecommunication Applications
Austin, Texas

THE APPLICATION OF A DUPLEXER

The purpose of this document is to explain the application and operation of a duplexer circuit, to show how to balance a duplexer, and to discuss the duplexer's operation analysis when used with two different transformers and with variable components.

The duplexer circuit shown in Figure 1 is a fundamental circuit that is used to help reject the transmit energy from the receive signal. The circuit in Figure 1 is set up for a standard 600 ohm system.

This circuit eliminates the transmit signal from the receiving point by sending a combination of both signals into the inputs of a differential amplifier. This tends to cancel out the transmit signal leaving only the receive signal. A signal is transmitted into Pin 3, the noninverting input, while a signal is being received across Pins 5 and 8 of the transformer, from the same line. There is a 600 ohm impedance when looking into Pins 1 and 4 of the transformer. With R1 tweaked to approximately 600 ohms, a voltage divider network is established with the 600 ohm impedance of the transformer. Thus, the signal at the noninverting input, Pin 5, is Rx + (Tx/2). The signal at the inverting input, Pin 6, is Tx/2 due to the virtual ground concept. When these inputs are added together, the transmit signal cancels leaving Rx, the receive signal, at the output Pin 7.

There are several ways of balancing or tuning duplexers but only one technique will be explained for this application. The transmit Pin 3 is grounded while a 600 ohm signal source with a predetermined level and frequency is connected to Pins 5 and 8 of the transformer. A signal with a level of − 10 dBm (0.6938 Vp-p) and a frequency of 1700 Hz was used in this circuit. R1 is then tweaked such that the voltage across Pins 5 and 8 of the transformer is half the signal voltage or until there is exactly a 6 dB loss across Pins 5 and 8, (i.e., − 16 dBm at Pins 5 and 8). Next, the 600 ohm signal source set at the same level and frequency is connected to Tx (Pin 3) across a 10 kilohm resistor. A 600 ohm resistor is connected to Pins 5 and 8 of the transformer. Then, R2 is tweaked until there is a minimum signal at Rx. Next, several different values of capacitance are tried for C1 until the smallest null is found at Rx. Once the best value of capacitance has been found, the duplexer has been balanced for that particular input signal and the best possible rejection of the transmission signal to the receive signal has been found. This is called the Transhybrid Rejection and is shown with different values of capacitance in Figure 2.

There are several noisy signals that this duplexer can not eliminate at the receive Pin 7. For instance, deflection of the transmit signal off of the transformer returns out of phase and tends to leak through onto the receive signal. For this particular circuit, curve 1 shows the best rejection over the spectrum.

It is worth noting the difference in performance of this duplexer with respect to the type of transformer used. The rejection versus frequency plot shown in Figure 2 was the result obtained when the Midcom 671-0018 was incorporated. This transformer has winding resistances of 14 ohms on the primary coil and 18 ohms on the secondary. The same test was run with a different transformer (Midcom 671-0915) and the results are shown in Figure 3. This transformer has winding resistances of 178 ohms on the primary coil and 67 ohms on the secondary coil giving it a much larger insertion loss than the Midcom 671-0018. This difference is displayed in Figure 3 as there is not as much rejection with the Midcom 671-0915 over the spectrum as with the Midcom 671-0018 (Figure 2).

It can be seen from Figures 2 and 3 that changing the capacitance changes the amount of rejection. This is due to the fact that the coil (Pins 1 and 4) not only has a resistance but also has an inductive reactance. If there is not a proper sized capacitance in parallel with this inductance, then the overall impedance of the coil increases. This impedance changes the voltage divider with R1 which in turn allows a larger Tx at Pin 5 which is slightly out of phase with the Rx + Tx/2 at Pin 6. This allows more leakage of the transmission onto the receive signal thus decreasing the rejection. This difference between the size of the capacitance and the type of transformer to use is a tradeoff which is left to the designer's judgement.

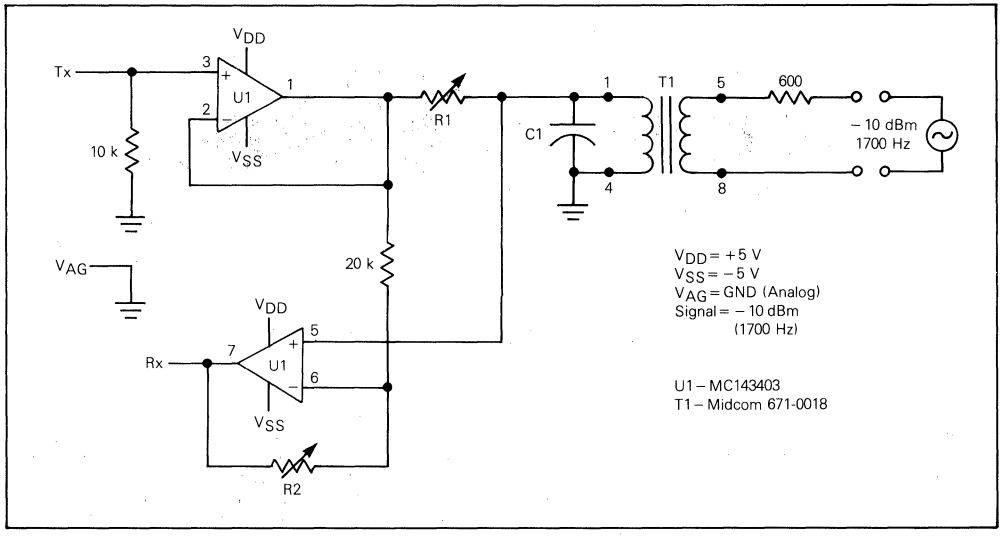


FIGURE 1 — Duplexer Circuit

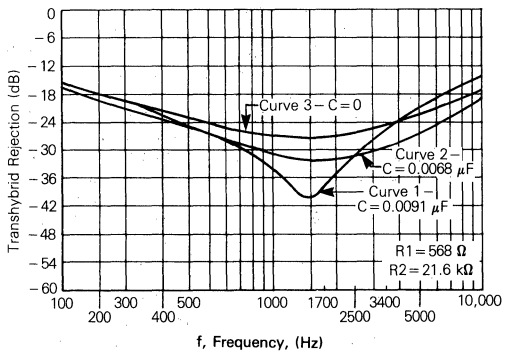


FIGURE 2 — Transhybrid Loss with Midcom 671-0018

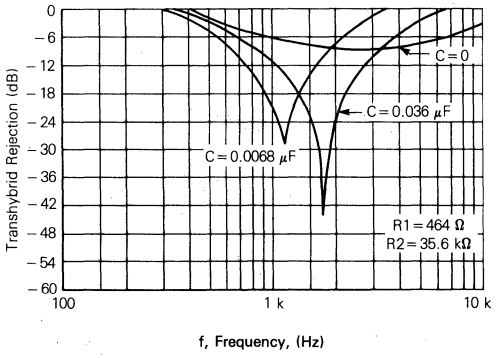


FIGURE 3 — Transhybrid Loss with Midcom 671-0915

IC trio simplifies speech synthesis

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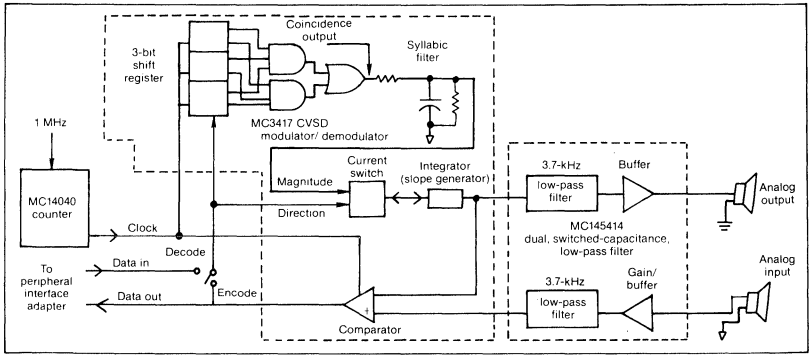
Despite the emergence of special-purpose speech chips, the details of adding voice output to a system are still foreign to most designers. However, they should be happy to learn that highly intelligible speech is possible using a low-cost microprocessor and three readily available integrated circuits.

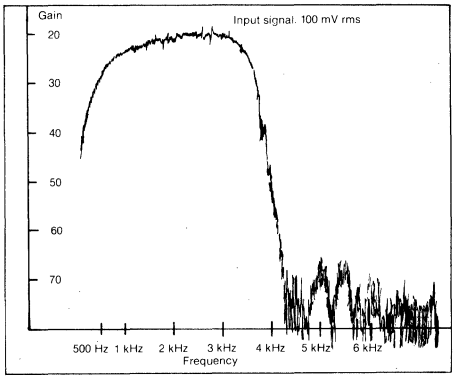
The speech peripheral, which contains an MC3417 continuously variable-slope delta modulator-demodulator, an MC145414 tunable, dual switched-capacitor, low-pass filter, and an MC14040 counter, encodes analog signals into a serial bit stream at a rate of 15,625 bits/s (Fig. 1). The bit stream is then stored in CPU memory. On demand, the peripheral will reproduce an analog signal well enough to be understood easily by an untrained listener.

Such a speech peripheral will enhance the I/O capability of industrial systems, consumer service systems, and games tremendously. Although more CPU memory is required than for linear predictive coding, stored words are easily changed than with LPC. Furthermore, no special memories or complicated calculations are required and no special-purpose synthesizer chips are needed. The encoded speech signals are simply recorded into and played out of CPU memory as any other data. Even the software is simple: words can be packed into ROM or a disk and need only be selected by the microprocessor software for output.

Since the three-IC circuit is designed for speech applications, the bandwidth ranges from 500 Hz to 3.7 kHz (Fig. 2). However, different filter time constants, data rates, and integrator designs can change the frequency range and with it the circuit's



1. At the heart of a three-chip speech peripheral is an MC3417 continuously variable-slope delta modulator-demodulator, which converts an audio waveform into a serial bit stream. The second and newest of the three is an MC145414 dual switched-capacitor low-pass filter with on-board operational amplifiers. An MC14040 12-bit binary counter completes the trio.

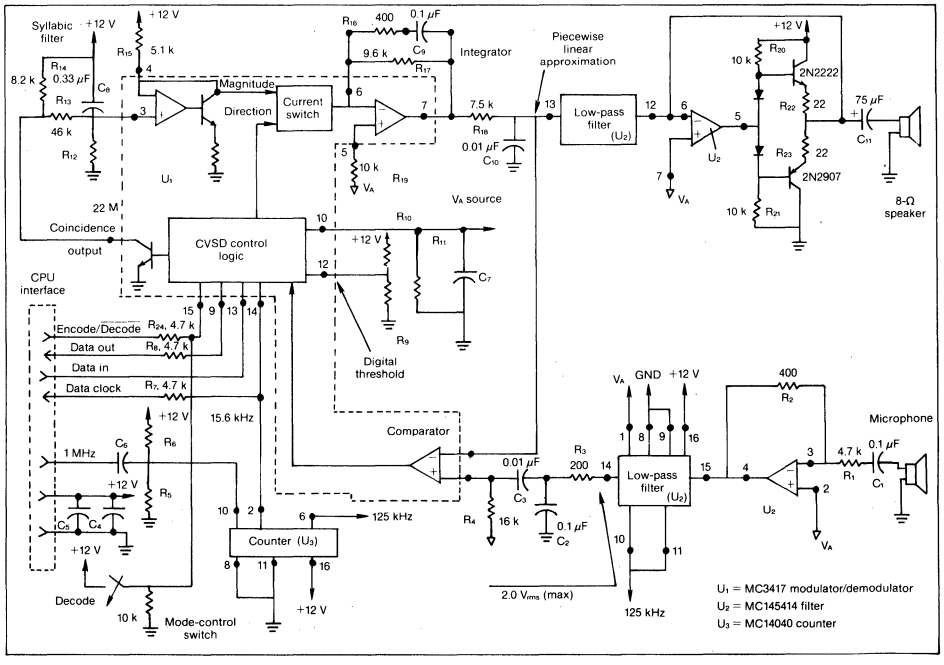


2. The switched-capacitor low-pass filter limits both input and output frequencies to about 3.7 kHz, as reflected by the system frequency response curve. Input frequencies are limited to prevent aliasing; filtering the output smooths it out. Bandwidth for the circuit ranges from 500 Hz to 3.7 kHz.

application. The tradeoffs made for this circuit make it suitable for many industrial applications as well.

About the key chip

Of the three ICs, the key one is the CVSD modulator-demodulator. On board, a current-controlled integrator generates a ramped voltage to linearly approximate the encoded analog waveform in piecewise fashion. Whenever the ramped voltage becomes greater than the input voltage, an on-board comparator switches the direction of the ramp. Digitally, an increasing slope is represented by a 1; a decreasing slope, by a 0. This process is called delta modulation because the slopes change, or delta, is detected. However, the MC3417 does more than simple delta modulation; it performs what is called continuously variable-slope delta modulation (and demodulation). Thus the slope of the ramp voltage —that is, the gain of the chip's integrator—is infinitely variable. This way, in tracking the analog input voltage, the output slope can change more quickly when changes in the analog input demand it. As a result, tracking is more accurate than with any constant-slope delta modulation scheme.



3. A continuously variable slope gives the MC3417 the accuracy to reproduce analog signals. When necessary, the syllabic filter changes the rate of integration and with it the slope. The three basic chips, a simple audio amplifier, and a microprocessor interface complete the speech peripheral circuit.

The MC145414 contains two filters and two operational amplifiers. One filter provides anti-aliasing by cutting off input frequencies above 3.7 kHz. It has a gain of 18 dB. The other filter smooths output noise, but has no inherent gain. One of the chip's on-board operational amplifiers augments the signal from a microphone to about 1 V rms to drive the MC3417's comparator input. At the output, a second op amp and several discrete components drive an 8-Ω speaker.

The MC145414 uses switched-capacitor filters, which need no precise external components for accurate, low-pass analog filtering. Both filters are five-pole, elliptic, low-pass types whose cutoff frequency depends on the sampling clock frequency.

For producing speech, the break frequency (3.7 kHz) requires a 125-kHz clock. The clock is generated by the third IC, a CMOS MC14040 divider, and a 1-MHz master clock derived from the CPU. The three ICs interface with a CPU system, in this case, through an MC6821 peripheral interface adapter (PIA).

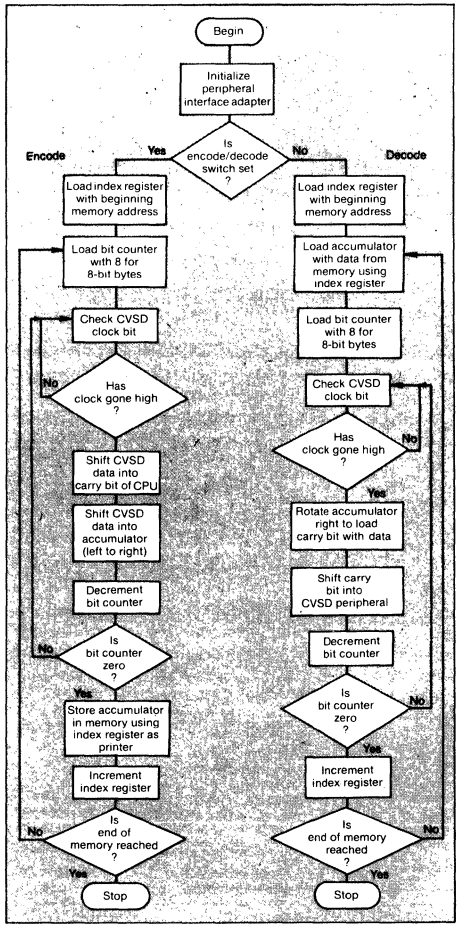
Figure 3 details the entire speech circuit and its two functions: encoding the analog signal into a serial bit stream for the CPU to record and decoding the bit stream into a reconstructed analog waveform. Switch S_1 determines which function to perform by supplying a corresponding level to both the CPU and the CVSD chip.

When switched to encode, analog signals from the microphone are amplified and filtered by one of the op amps and a low-pass filter on board the MC145414. The filtered audio is then fed to the MC3417, where the analog-to-digital conversion produces the serial bit stream. Each high bit means the integrator slope is positive, and each low signals a negative slope. Later, the stored bits are used to control the integrator, whose output approximates the audio signal. In this way, the integrator uses straight lines to reconstruct the original analog waveform.

Thus, when the circuit is set to decode—that is, to output speech—the sequence of bits that translates the serial bit stream into a linear approximation of the original audio is fed to the MC3417, which sends it to the second low-pass filter and op amp on board the MC145414 to smooth out the sequence of linear approximations and provide enough gain to drive a loud-speaker. As a result, with the CPU selecting the sequence of bits (representing words) previously stored in memory, spoken sentences are put out through the peripheral.

Since the speech quality is dramatically affected by the sampling rate, the feedback loop gain, the signal level, and the filtering, there is room to tweak and adjust the sound to suit an application. The circuit represents several tradeoffs to produce highly intelligible speech using a reasonable amount of CPU memory for speech storage, yet requires reasonably few readily available parts.

For example, the transfer function in this application has two poles—one at 160 Hz and one at 280 Hz—and a zero at 4.0 kHz. The pole at 160 Hz provides the long time constant necessary for following relatively linear portions of the original analog



4. The speech peripheral and the controlling microprocessor communicate through a peripheral interface adapter. In addition, clocking and serializing are software tasks, but since the transfer of data between the program and the peripheral is asynchronous, changing the software does not create a timing problem.

3

```
************* MC6800 SPEECH PERIPHERAL DRIVER *************
*          FOR MC145414 / MC3417 PERIPHERAL CIRCUIT.
*
* A PROGRAM TO RECORD AND PLAY SERIAL CVSD DATA.
*
* ENTER STARTING MEMORY LOCATION FOR DATA STORAGE
*  AT LOCATIONS $A000 - $A001.
*
* ENTER ENDING MEMORY LOCATIONS FOR DATA STORAGE
*  AT LOCATIONS $A002 - $A003.
*
* PIA IS LOCATED AT ADDRESSES $8004 - $8007.
*    PIA PB7, PIN 17 IS DATA FROM MC3417 PIN 9.
*    PIA PB4, PIN 14 IS LEVEL FROM ENCODE/DECODE
*                SWITCH (ENCODE = "1").
*    PIA PB0, PIN 10 IS DATA TO MC3417 PIN 13.
*    PIA CB1, PIN 18 IS DATA CLOCK FROM MC14040 PIN 2
*    PIA PIN 25 IS 1.0000 MHZ CLOCK TO MC14040 PIN 10
*    PIA PIN 20 IS +5.0 VOLTS.
*    PIA PIN 1 IS GROUND.
[illegible]
***************************************INITIALIZE PIA
[illegible]                  ACCESS DATA DIRECTION REG.
[illegible]                  BIT FOR OUTPUT.
[illegible]                  CB1 INTERRUPT ACTIVE GOING HI
[illegible]
***********************DETERMINE WHICH FUNCTION FROM SWITCH
[illegible]
**********************************************ENCODE ROUTINE
[illegible]
*********************************************DECODE ROUTINE
[illegible]                  GET STARTING ADDRESS.
[illegible]                  SET UP BIT COUNTER.
[illegible]                  GET A BYTE FROM MEMORY.
[illegible]                  CHECK FOR CLOCK TRANSITION.
[illegible]                  ROLL DATA INTO CARRY BIT.
[illegible]                  ROLL CARRY BIT OUT
[illegible]                  POINT TO NEXT BYTE.
[illegible]                  CHECK FOR END OF MEMORY BLOCK
[illegible]
```

5. Conspicuous by its small size, the program for running the speech peripheral circuit performs both encoding and decoding functions in 84 lines, including comments. The routine "reads" the encoding-decoding switch position and branches to the corresponding routine.

waveform; the pole at 280 Hz prevents instantaneous reversals of the integrator's output voltage. The latter action avoids a sawtoothlike peak at extreme values of the audio sine wave, which enables the output to follow rapid changes in the audio waveform more closely.

Finally, the zero at 4.0 kHz improves the phase margin of the MC3417's feedback loop. In a simple delta modulation-demodulation system, the slope of the output signal used to approximate the input is constant. Acceptable speech quality, however, calls for a continuously variable slope—one that increases or decreases with the input. The MC3417 performs continuously variable slope modulation and demodulation so that the slope of the approximating line segments depends on the last three bits clocked into the decoder.

To do that, the MC3417's internal 3-bit shift register monitors the serial bit stream of the comparator. If the comparator detects a series of three or more 1s or three or more 0s in a row, its coincidence pin will go active and the slope of the integrator's output line segments will be made slightly steeper. If three or more consecutive 1s or 0s are detected, a capacitor off the chip will charge up, and the control current of the integrator will be increased continuously.

When the stream of all 1s or all 0s ends, the capacitor is discharged by an external resistor (R_{17}), which, with capacitor C_9, forms a so-called syllabic filter. (Incidentally, the values of R and C are not critical and in this application, the time constant provided by the pair is 50 ms.)

Simple software

As Fig. 4 indicates, the software to record and play speech using this peripheral is simple. The assembly listing for an MC6800 system is given in Fig. 5. In this case, a switch on the CPU board selects the encoding or decoding by setting a high or low level, respectively, at pin 14 of the PIA and pin 15 of the CVSD chip. The encoding routine reads bits serially from the peripheral, performs serial-to-parallel conversion, and saves the encoded data in memory. The program operates asynchronously with the peripheral, allowing different clock rates without changing the software. The CPU simply waits for a data clock edge, then reads the data. The decoding routine works in the same way. The CPU waits for a data clock edge, then sends a bit from memory to the peripheral, which converts it into speech.□

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Turn I/O data port into speech port

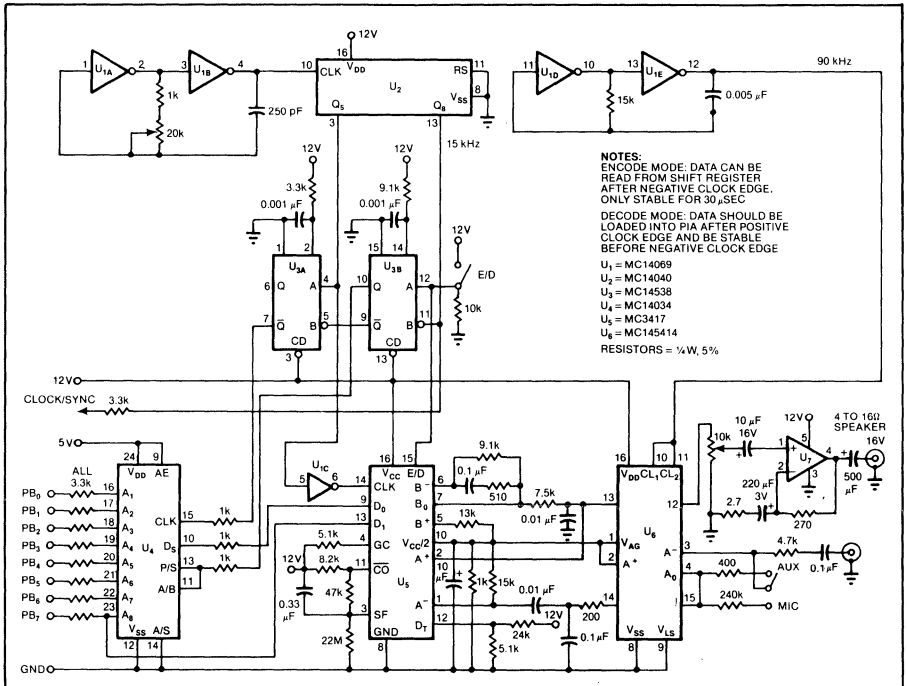
Earle West and **Al Mouton**
Motorola Inc, Austin, TX

This low-cost, low-power μP peripheral circuit (**figure**) converts an 8-bit I/O data port into a high-quality speech port, using continuously variable slope-delta (CVSD) modulation to encode and decode waveforms per μP direction. The μP can play back any segment of recorded speech; 1 sec of intelligible speech requires ~1.5k bytes of memory. You can trade off between voice quality and memory-storage requirements by adjusting the data-clock rate for the CVSD chip.

To encode speech, an MC145414 CMOS dual switched-capacitor filter/dual op amp (U_6) buffers the signal and band-limits the input to ~2.9 kHz. U_5, an MC3417 linear CVSD modulator/demodulator, encodes the CVSD word and creates a bit stream at ~12k bps. This serial bit stream loads into U_4, where the μP reads it in parallel.

For decoding and outputting speech, the μP loads the MC14014 8-bit shift register (U_4) with parallel data. U_4 shifts the data to U_5 for CVSD decoding. U_6 performs low-pass filtering and buffers the resultant voice waveform.

CMOS ICs U_1, U_2 and U_3 clock the filter and CVSD chips, and U_7 drives a loudspeaker. Four control lines connect with the μP to control data direction and synchronize data clocking. **EDN**



This 8-bit speech circuit *encodes and decodes analog waveforms. Adjust the data-clock rate to trade off between voice quality and memory overhead.*

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Glossary 4

4

Glossary of Terms and Abbreviations

The list reproduced here refers to terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Telecommunications.

A law—An European companding/encoding law commonly used in PCM systems.

A/B signaling—A special case of 8th-bit (LSB) signaling in a μ-law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (analog-to-digital) converter (ADC)—A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing noise—A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Answer back—A signal sent by receiving data-processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

Anti-aliasing filter—A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Asynchronous—A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Attenuation—A decrease in magnitude of a communication signal.

Bandwidth—The information-carrying frequencies between the limiting frequencies of a communication line or channel.

Baseband—The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process.

Baud—A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

Bit rate—The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Blocking—A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

BORS(C)HT—Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband—A transmission facility whose bandwidth is greater than that available on voice-grade facilities. (Also called wide band.)

C message—A frequency weighting that evaluates the effects of noise based on its annoyance to the "typical" subscriber of standard telephone service or the effects of noise (background and impulse) on voice-grade data service.

Carrier—An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission.

CCITT—Consultative Committee for International Telephone and Telegraph; an international standards group of European International Telecommunications Union.

Central Office (CO)—A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

Channel bank—Communication equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

CODEC—COder-DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

COFIDEC—COder-FIlter-DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common mode rejection—The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential-input terminals.

Companding—The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic.

Compandor—A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal-to-noise ratio.

Conference call—A call between three or more stations, in which each station can carry on a conversation simultaneously.

Crosspoint—The operating contacts or other low-impedance-path connection over which conversations can be routed.

Crosstalk—The undesired transfer of energy from one signal path to another.

CTS—Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

CVSD—Continuous Variable Slope Delta (modulation); a simple technique for converting an analog signal (like voice) into a serial bit stream.

D3—D3 channel bank; a specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (digital-to-analog) converter (DAC)—A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data compression—A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel)—A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$10 \times \log (P1/P2)$ for power measurements, and

$20 \times \log (V1/V2)$ for voltage measurements.

dBm—An indication of signal power. 1.0 milliwatt across 600 ohms, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

$dBm = 20 \times \log (Vrms/0.775)$, or

$dBm = [20 \times \log (Vrms)] + 2.22$.

dBmO—Signal power measured at a point in a standard test tone level at the same point.

i.e., $dBmO = dBm - dBr$

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp—Relative power expressed in dBmp. (See dBmO and dBmp.)

dBmp—Indicates dBm measurement made with a psophometric weighting filter.

dBrn—Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = −90 dBm.

dBrnC—Indicates dBrn measurement made with a C-message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

dBrnc0—Noise measured in dBrnc referenced to zero transmission level.

Decoding—A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delay distortion—Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

Delta modulation—A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation.

Demodulator—A functional section of a modem that converts received analog line signals to digital form.

Digital telephone—A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

Distortion—The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

DPSK—Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180°, and 290° to define the digital information.

DTMF—Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two nonharmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Duplex—A mode of operation permitting the simultaneous two-way independent transmission of telegraph or data signals.

Echo—A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

Echo suppressor—A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time.

Encoder (PCM)—A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalizer—An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line.

FDM—Frequency-Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

Four wire circuit—The portion of a telephone, or central office, that operates on two pairs of wires. One pair is for the transmit path (generally from the microphone), and one pair is for the receive path (generally from the receiver).

Frame—A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Full duplex—A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain—The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Gain tracking error—The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

HDLC—High-Level Data Link Control; a CCITT standard data communication line protocol.

Half duplex—A transmission system that permits communication in one direction at a time. CB ratios, with "push-to-talk" switches, and voice-activated speakerphones, are half duplex.

Handset—A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

Hookswitch—A switch that connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Idle channel noise (ICN)—The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wide-band noise measurement using a C-message weighting filter to band-limit the output noise).

Intermodulation—The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation distortion—An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

ISDN—Integrated Services Digital Network; a communication network intended to carry digitized voice and data multiplexed onto the public network.

Jitter—A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency, or phase.)

Key system—A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

μ-law—A companding law accepted as the North American standard for PCM based systems.

LAN—Local Area Network; a data-only communication network between data terminals using a standard interface to the network.

Line—The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

Line length compensation—Also referred to as loop length compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Longitudinal balance—The common-mode rejection of a telephone circuit.

Loop—The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loopback—Directing signals back toward the source at some point along a communication path.

Loop current—The dc current that flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

MCU—MicroComputer Unit (also MicroController Unit).

MPU—MicroProcessor Unit.

Mu law—A companding/encoding law commonly used in U.S. (same as μ-law).

MUX—Multiplex or multiplexer.

Modem—MOdulator-DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

Multiplex—To simultaneously transmit two or more messages on a single channel.

Off hook—The condition when the telephone is connected to the phone system, permitting loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On hook—The condition when the telephone's dc path is open, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX—Private Automatic Branch Exchange; a customer-owned, switchable telephone system providing internal and/or external station-to-station dialing.

Pair—The two associated conductors that form part of a communication channel.

Pass-band filter—A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

PBX—Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM—Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8-bit words.

Phase jitter—Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

Propagation delay—The time interval between specified reference points on the input and output voltage waveforms.

Psophometric weighting—A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing.

Pulse dialer—A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing.

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Quantizing noise—Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

REN—Ringer Equivalence Number; an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals about 8 kilohms. The Bell system typically permits a maximum of 5.0 REN (1.6 kilohms) on an individual subscriber line. A minimum REN of 0.2 (40 kilohms) is required by the Bell system.

Repeater—An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory dialer—A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Ring—One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

RTS—Request To Send; an EIA-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

Sampling rate—The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

SCU—Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Sidetone—The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Signaling—The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal-to-distortion ratio (S/D)—The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

SLIC—Subscriber Line Interface Circuit; a circuit that performs the 2-to-4 wire conversion, battery feed, line supervision, and common mode rejection at the central office (or PBX) end of the telephone line.

Speech network—A circuit that provides 2-to-4 wire conversion, i.e., connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber line—The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Switchhook—A synonym for hookswitch.

Syn (Sync)—(1) A bit character used to synchronize a time frame in a time-division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous modem—A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 carrier—A PCM system operating at 1.544 MHz and carrying 24 individual voice-frequency channels.

Tandem trunk—See trunk.

Telephone exchange—A switching center for interconnecting the lines that service a specific area.

TELETEX—A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

TELETEXT—The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

Time-division multiplex—A process that permits the transmission of two or more signals over a common path by using a different time interval for each signal.

Tip—One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone ringer—The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80-90 volts rms, 20 Hz.

Trunk—A telephone circuit or channel between two central offices or switching entities.

TSAC—Time Slot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

TSIC—Time Slot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" crosspoint switch.

Twist—The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

Two wire circuit—Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

UDLT—Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

Voice frequency—A frequency within that part of the audio range that is used for the transmission of speech of commercial quality, i.e., 300-3400 Hz.

Weighting network—A network whose loss varies with frequency in a predetermined manner.

Handling and Design Guidelines 5

5

Handling and Design Guidelines

HANDLING PRECAUTIONS

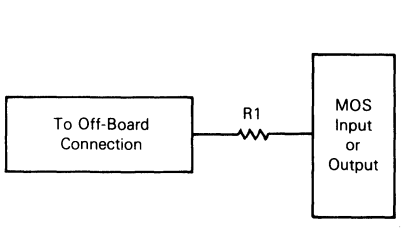
All MOS devices have an insulated gate that is subject to voltage breakdown. The gate oxide for Motorola's devices is about 800 Å thick and breaks down at a gate-source potential of about 100 V. The high-impedance gates on the devices are protected by resistor-diode networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Another effect of static damage is, often, increased leakage currents.

CMOS and NMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

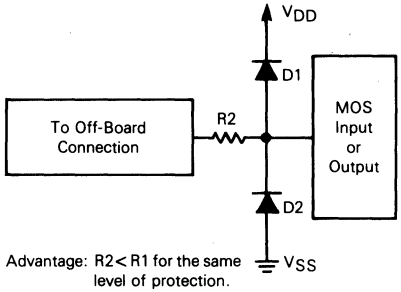
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS or NMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or NMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS or NMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS or NMOS devices should be stored or

FIGURE 1 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost

Note: These networks are useful for protecting the following:
A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 — PROPAGATION DELAY vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for the MC145040/1
k = 0.7 for other devices

EQUATION 2 — RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum rise time per data sheet in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for the MC145040/1
k = 2.3 for other devices

transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

6. All CMOS or NMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS or NMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS or NMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS or NMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.
17. Do not recycle shipping rails. Continuous use causes deterioration of their antistatic coating.

RECOMMENDED FOR READING

"Total Control of the Static in Your Business"

Available by writing to:
Static Control Systems Div.
Box ELB-3, 225-4S
3M Center
St. Paul, MN 55144

Or calling:
1-800-328-1368
1-612-733-9420 (in Minnesota)

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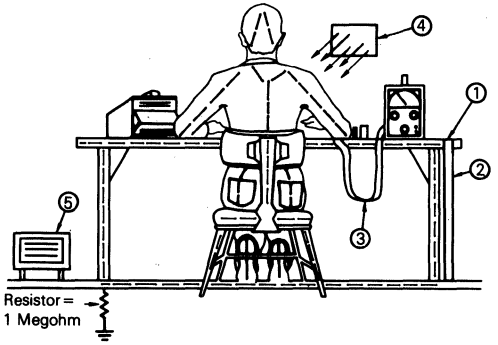
FIGURE 2 — TYPICAL MANUFACTURING WORK STATION



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than − 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:
   $-0.5 \le V_{in} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $-0.5 \le V_{out} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $|I_{in}| \le 10$ mA
   $|I_{out}| \le 10$ mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values. See Figure 1.
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of I_{in} = 10 mA. See Figure 1.
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 3 — CMOS WAFER CROSS SECTION

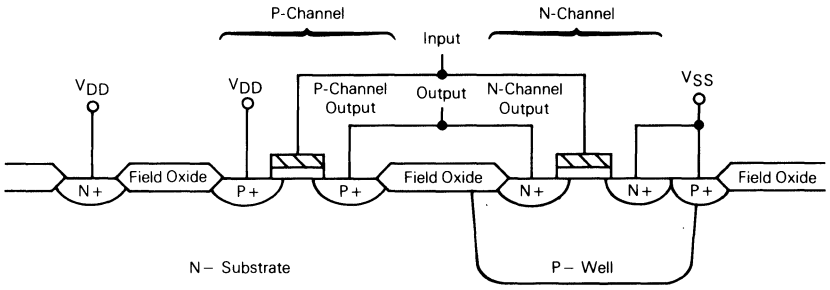
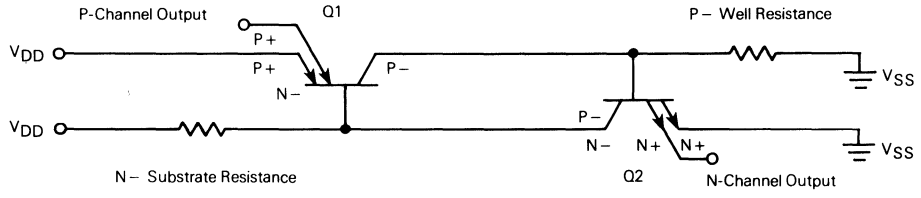


FIGURE 4 — LATCH UP CIRCUIT SCHEMATIC



Quality and Reliability 6

6

Quality in Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is its philosophy to "design in" reliability. At all development points of any new design reliability orientated guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola Incoming Inspection Specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

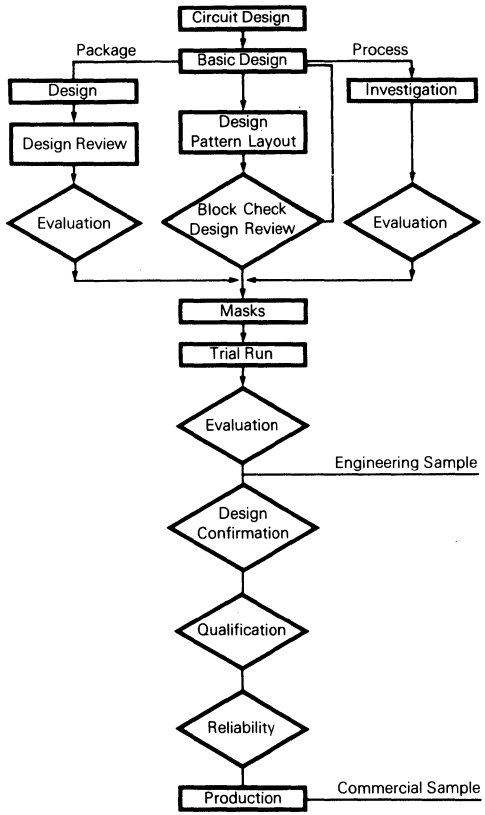
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



This basic design flow-chart omits some feedback loops for simplicity

6

The Six Sigma Challenge

Motorola's expressed objective is the achievement of "error free performance" in products and services. The high quality level of the product-line outputs, followed by stringent outgoing quality control, readily assures this objective. But error-free output from the production lines themselves is a matter that continues to demand full attention at all levels of production, design and administration. This far more stringent requirement has a two-fold goal:

1. To further improve ultimate product reliability—experience has proved that products **designed** for 100% conformance to specifications are far less subject to field failure than products **selected** to a given level of performance.
2. To reduce waste—thereby making the end-product more cost competitive.

Whether or not one-hundred percent perfection is consistently achievable remains subject to conjecture. Motorola's already low reject rates, however, warrant a high level of confidence that the goal can be met, and milestones toward this objective have been firmly established. They call for a hundred-fold performance improvement in output by 1991, and a Six Sigma Capability by 1992.

Six Sigma Capability—not yet zero defects, but 99.9999998% perfection in both product and in customer services.

Why Six Sigma?

Each process attempts to reproduce its characteristics identically from unit to unit. Inherent in each process, however, there are variations in conditions and in materials that are uncontrollable and unalterable. In all cases, therefore, the unit-to-unit output characteristics vary somewhat from the ideal (design target).

The performance of a product is determined by how much margin exists between the design specifications and the actual value of that specification. For some processes, such as those using real-time feedback to control the output, the variations can be quite small; for others they may be quite large. Many of the parametric data of a given specification tend to follow the normal distribution curve shown in Figure 1.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal deviation, defined as process width, is ±3 Sigma about the mean, representing a yield of 99.73%. But is ±3 Sigma good enough as an overall specification? Statistically, with a ±3 sigma deviation, approximately 2700 parts per million still fall outside acceptable performance limits.Clearly, for a product to be built virtually defect free it must be designed with a component yield that is significantly better than ±3 Sigma.

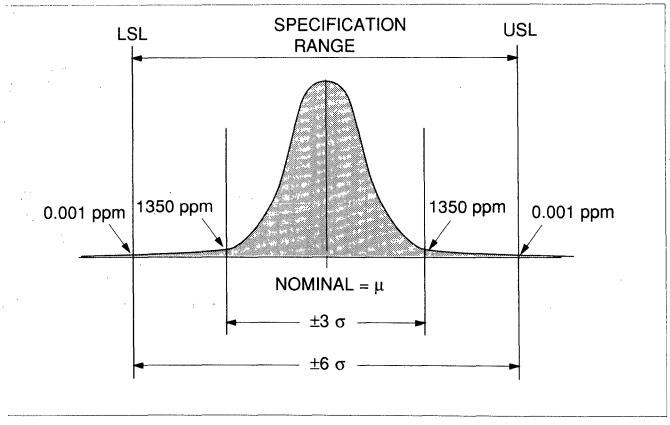
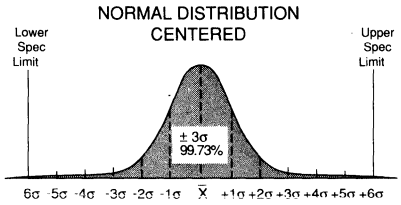


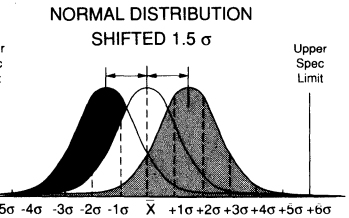
Figure 1. Standard distribution curve illustrates the Three Sigma and Six Sigma Parametric Conformance.

6



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	68.27	317300
± 2 SIGMA	95.45	45500
± 3 SIGMA	99.73	2700
± 4 SIGMA	99.9937	63
± 5 SIGMA	99.999943	0.57
± 6 SIGMA	99.9999998	.002

Figure 2. With a Centered Distribution Between Six-Sigma Limits Only 2 Devices Per Billion Fail to Meet the Specification Target.



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	30.23	697700
± 2 SIGMA	69.13	308700
± 3 SIGMA	93.32	66810
± 4 SIGMA	99.3790	6210
± 5 SIGMA	99.97670	233
± 6 SIGMA	99.999660	3.4

Figure 2a. Effects of a 1.5 Sigma Shift Where Only 3.4 ppm Fail to Meet Specification.

The Six Sigma Latitude

Product yield is a factor of two variables: Process width and design width. If a process is adequately controlled so that its output is ±3 Sigma, and if the product is so well designed that ±3 Sigma deviations still place the products well within the specified design limits, then the overall yield is increased.

The table in Figure 2 shows that a design which can accept twice the normal ±3 Sigma variation of the process (design width = ±6 Sigma)) will have a product yield of 99.9999998%, corresponding to 2.0 defective parts per billion. Even if the process mean were to shift by as much as ±1.5 Sigma from the center of the distribution, the process would be expected to have no more than 3.4 parts per million defective.

It is Motorola's goal to achieve ±6 Sigma capability in product design, manufacturing, sales and services by 1992.

The Motorola SPC Program

* Purpose * Objective * Scope

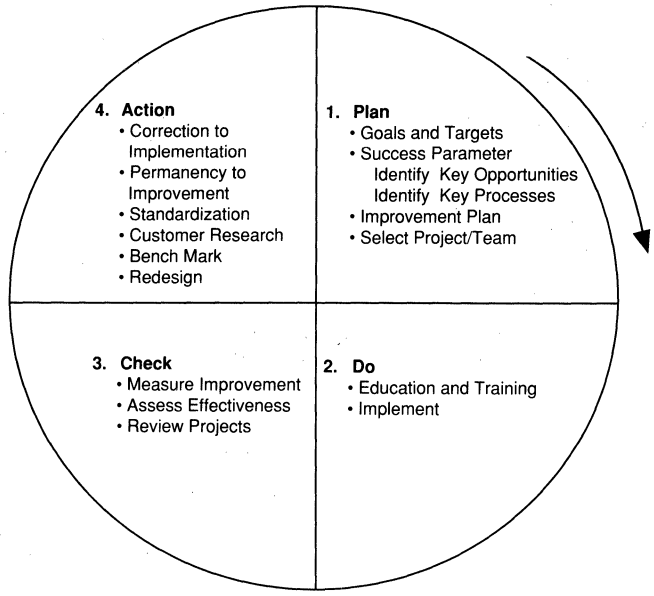
The Purpose of this program is to establish a standard approach toward continued process improvement through statistical process control.

Its Objective is to maintain all critical processes under tight statistical control in order to enhance quality and reduce scrap through identification of process variation, and through the reduction of these variations by means of real time corrective action. It is expected to establish the cultural environment and the organizational support required to achieve the Six-Sigma goal.

Its Scope encompasses a total quality improvement effort, involving design, manufacturing and management of all Motorola product groups and their suppliers as well as their support departments and vendors. It provides for the establishment of SPC teams and ensures adequate training . It serves as a liaison between teams in order to standardize and unify the approach to continuous quality improvement.

6

Continuous Improvement



Key Factors for Success

- Management Leadership
  - Top Down
  - Committed
  - Active
- Clear & Agreed-On Goals
- Breakthrough Thinking
- Project/Teamwork
- Training
- Reinforcing Successes

6

Verification of Statistical Process Control

Statistical process control programs have two specific functions:

1. as a monitor, to verify that a specific process is under control, or to indicate that a process is not in control based on interpretation of control-chart abnormalities or other indicators;
2. as a quality improvement tool, for the purpose of improving process capability.

In either case, documentation must be available that permits the utilization, verification and interpretation of process control data, or if necessary, to implement new programs for process improvement.

Evidence of Process Capability
Capability indices must be established for each critical process and there must be evidence that the upper and lower specification limits are realistic and not arbitrary. The present goal is $C_p \geq 2.0$ and $C_{pk} \geq 1.5$.
Evidence of a process capability study must be on file. Depending on the level of sophistication, the study may include a factorial experiment, a nested variance study, summation of the results and recommendation for further action. The selection of critical process points must be justified.

Measurement System Capability
Results of measurement system capability study must be on file. Precision-to-Tolerance (P/T) ratio should be less than 0.10.

Process Control Specifications
Process specifications must include procedures to be followed in the event of a process requiring corrective action.

Operator Training
The operators are normally the first to see the control charts. Incorrect interpretation will cause unnecessary and time consuming investigations or delay needed studies. Consequently, operator training is a vital function and documented operator certification must be on file.

Control Chart Accuracy and Visibility
Control charts must be current and and readily available. They shall be maintained by the production operators and upper and lower control limits must be calculated according to historical data.

Control Chart Tracking
Control charts must be tracked continuously. All out-of-control points must be highlighted and the appropriate corrective action described either on the chart or in a companion log. The objective is to view the trend, not simply to obtain a snapshot-in-time.

Supplier/Customer Relationships

Customers have no desire to control a supplier's process. Nor are they interested in the confidential details of a supplier's processes. They only want assurance (data) that a supplier has an ongoing program that supports an overall statistical process control plan. Primarily, Motorola's customers are interested in a supplier's statistical control of the critical processes, and his early warning system which keeps a process from becoming marginal. Most importantly, they are interested in what is being done for continuous improvement.

What We Offer Our Customers
It has been adequately demonstrated that a well monitored and controlled manufacturing process with minimum variations will produce a better, more useful and more reliable product at a reduced cost. In many instances, customer satisfaction now hinges not so much on a product's ability to meet specifications as on a manufacturer's ability to control his processes as evidenced by reduced variability. This is used as an indicator of both product quality and projected costs. Motorola provides detailed data and inferential statistics that allow customers to make decisions about the product they buy. In many instances, we provide a customer access to our computer data banks in order to improve communications and reduce turnaround time for product approval.

What We Expect From Our Suppliers
Improved quality of incoming material is crucial to success in achieving our Six Sigma goals. In order to accomplish this goal, we feel it necessary to reduce the number of suppliers and to work closely with those remaining as partners to resolve quality issues.

It is the responsibility of Motorola Supplier Quality Control to ensure that all suppliers maintain an adequate system of process and material controls which provides for prevention (as opposed to detection) of defects in their manufacturing processes. This includes, but is not limited to, the following:

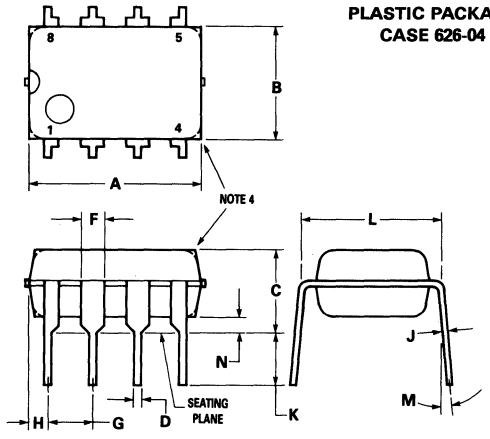
- General plan for continuous improvement
- Detailed product flow
- Process control plan
- Equipment and process capability studies
- Measurement system capabilty studies
- Specific action plan for out-of-control conditions
- Evidence of statistical process control

Mechanical Data 7

MECHANICAL DATA

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

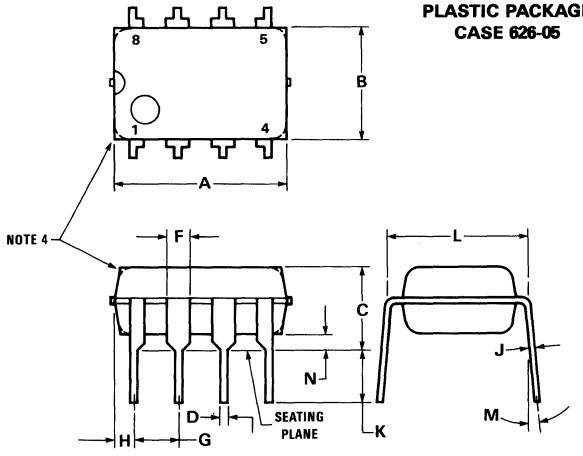
8-PIN PACKAGES



PLASTIC PACKAGE
CASE 626-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.



PLASTIC PACKAGE
CASE 626-05

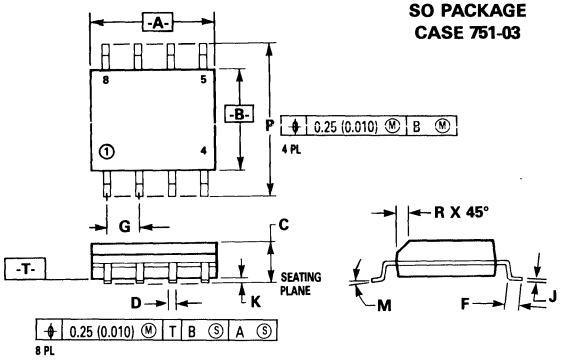
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.76	1.01	0.030	0.040

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

7

8-PIN PACKAGES (Continued)

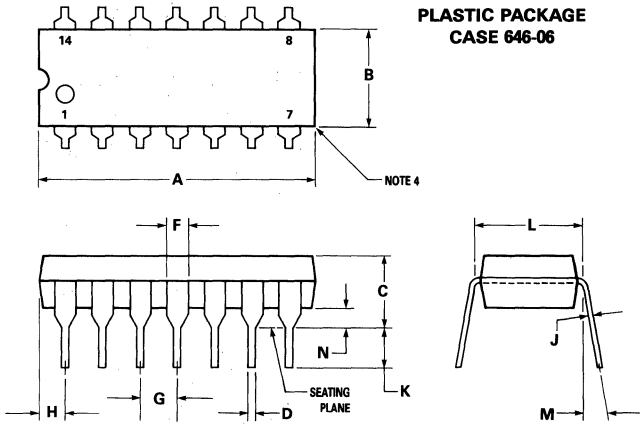
SO PACKAGE
CASE 751-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

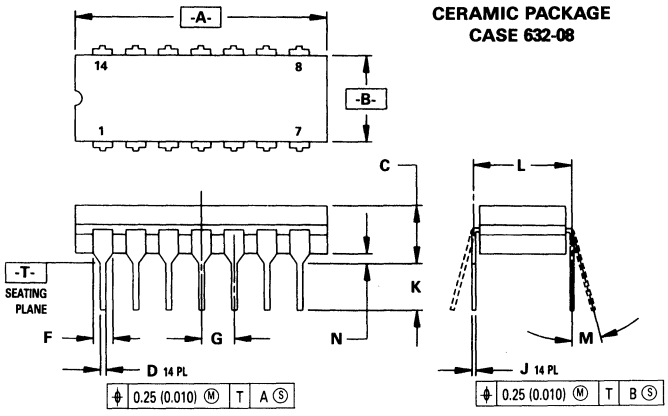
14-PIN PACKAGES



PLASTIC PACKAGE
CASE 646-06

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.



CERAMIC PACKAGE
CASE 632-08

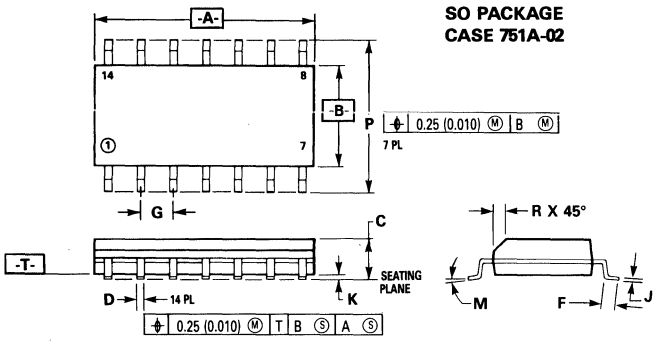
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

7

14-PIN PACKAGES (Continued)

SO PACKAGE
CASE 751A-02

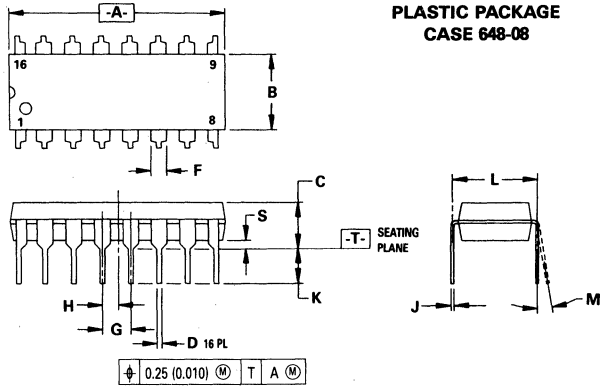


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

16-PIN PACKAGES

PLASTIC PACKAGE
CASE 648-08



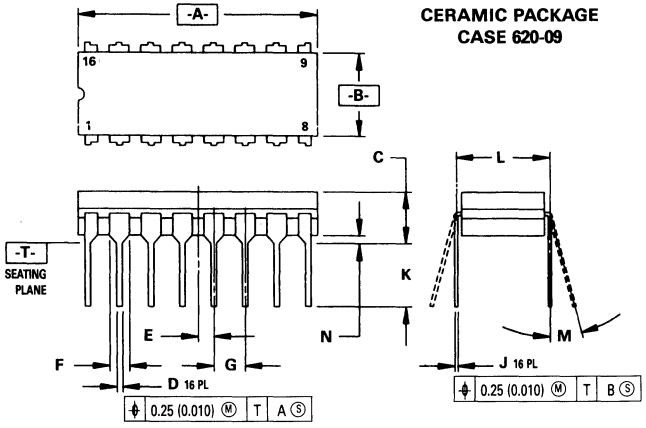
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

7

16-PIN PACKAGES (Continued)

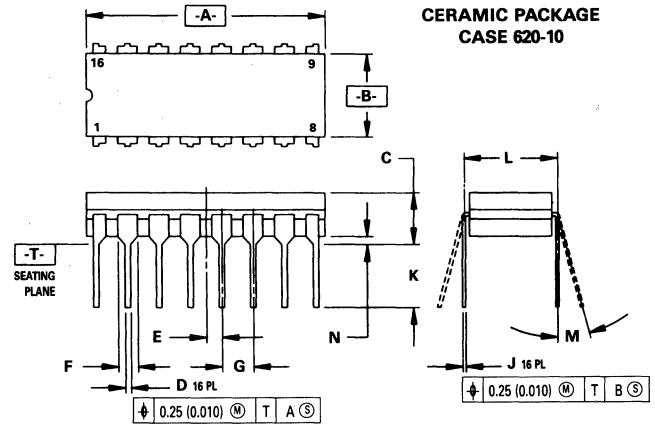
CERAMIC PACKAGE
CASE 620-09



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

CERAMIC PACKAGE
CASE 620-10

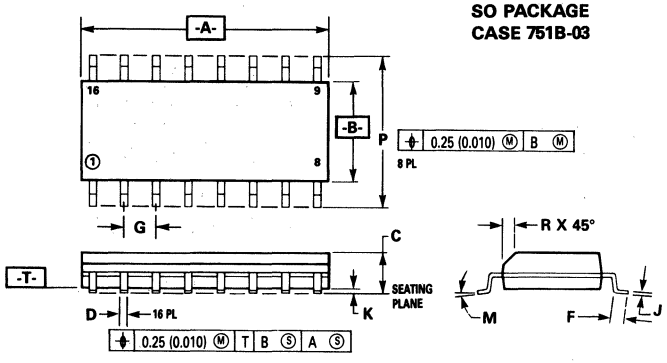


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.93	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.39	0.50	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

16-PIN PACKAGES (Continued)

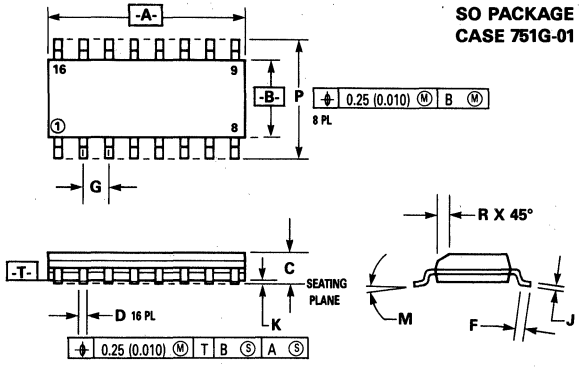
SO PACKAGE
CASE 751B-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

SO PACKAGE
CASE 751G-01

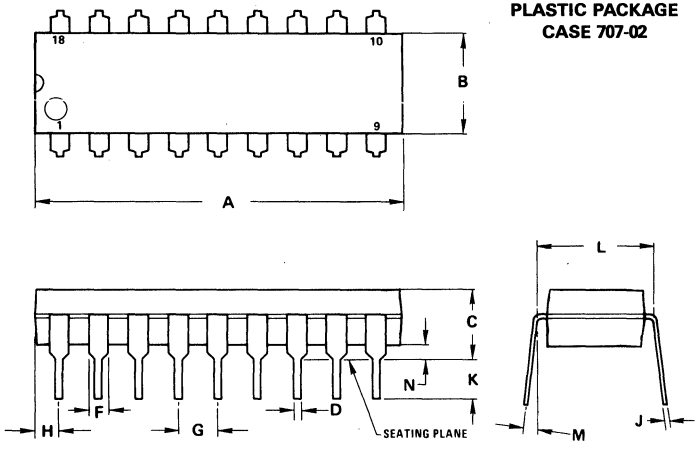


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

18-PIN PACKAGES

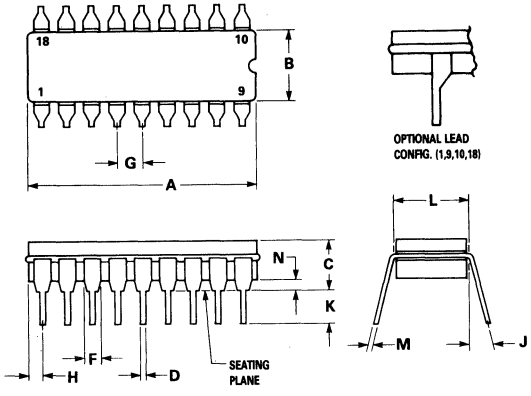
PLASTIC PACKAGE
CASE 707-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERAMIC PACKAGE
CASE 726-04

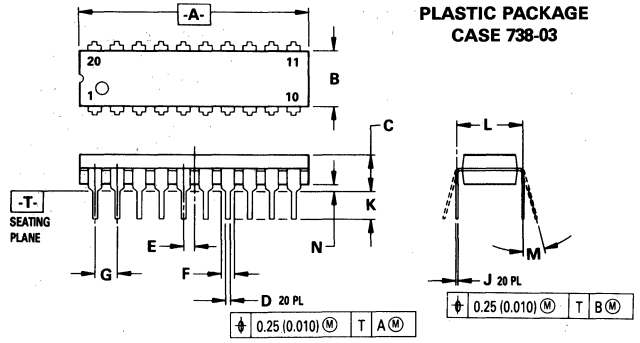


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

7

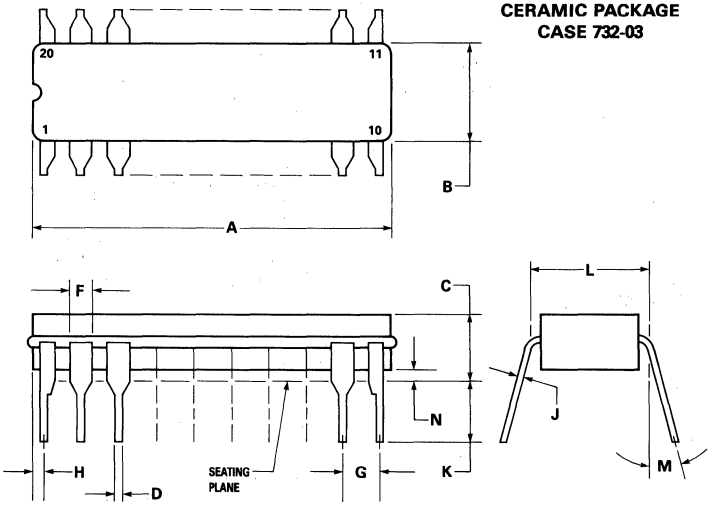
20-PIN PACKAGES



PLASTIC PACKAGE
CASE 738-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.



CERAMIC PACKAGE
CASE 732-03

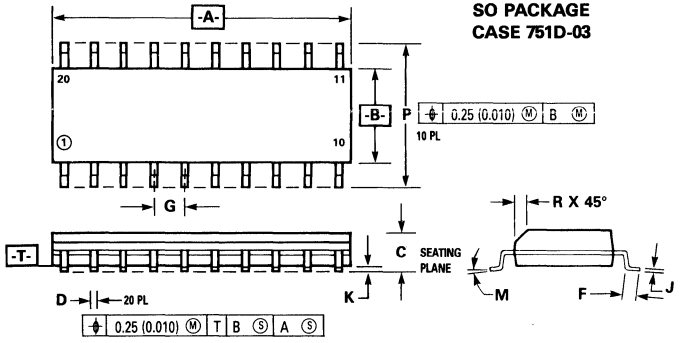
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

7

20-PIN PACKAGES (Continued)

SO PACKAGE
CASE 751D-03

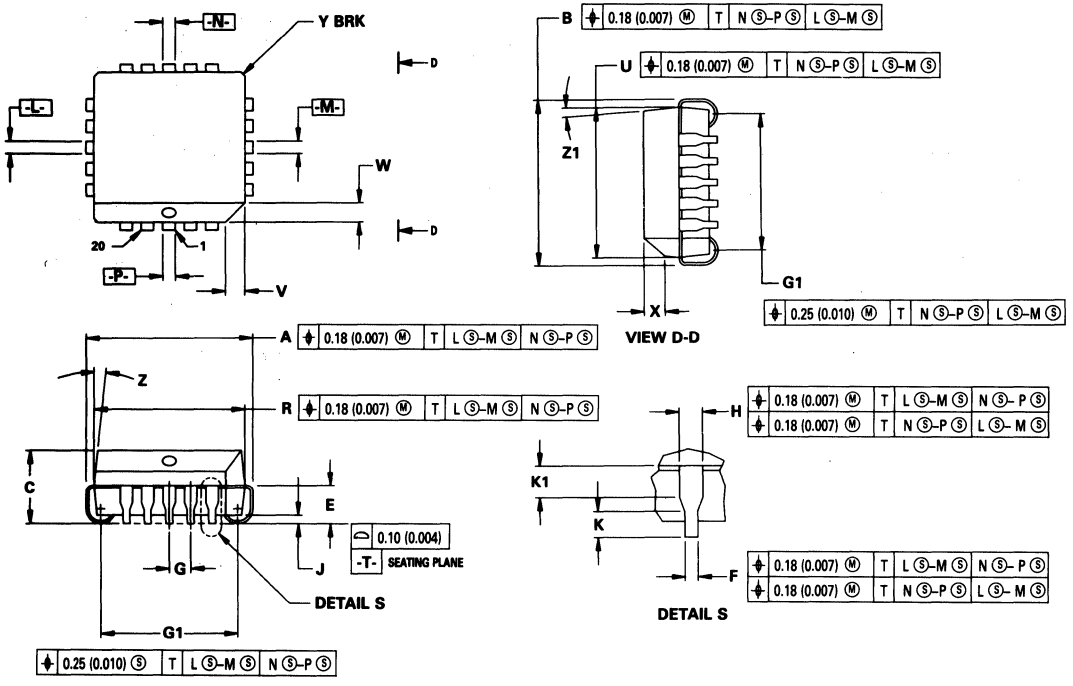


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.509
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

20-PIN PACKAGES (Continued)

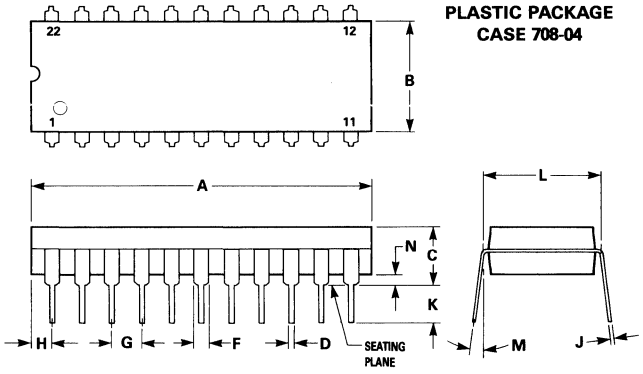
PLCC PACKAGE
CASE 775-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

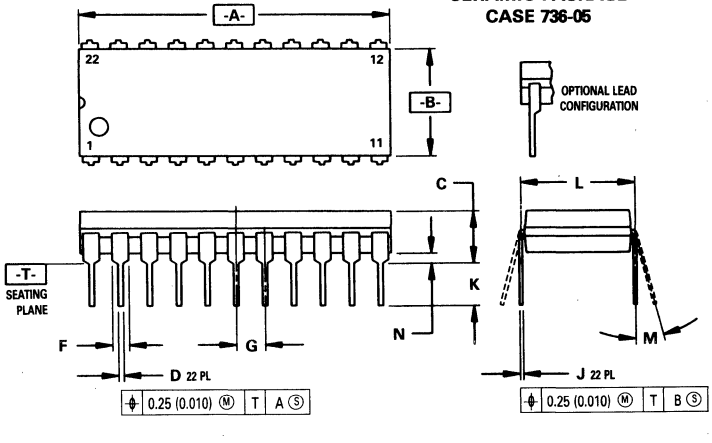
22-PIN PACKAGES



PLASTIC PACKAGE
CASE 708-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

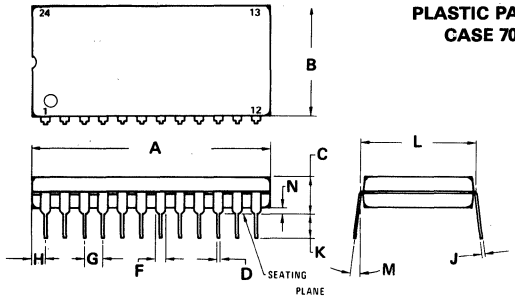


CERAMIC PACKAGE
CASE 736-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.93	27.81	1.060	1.095
B	9.15	9.90	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.39	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.39	0.008	0.015
K	3.18	4.31	0.125	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

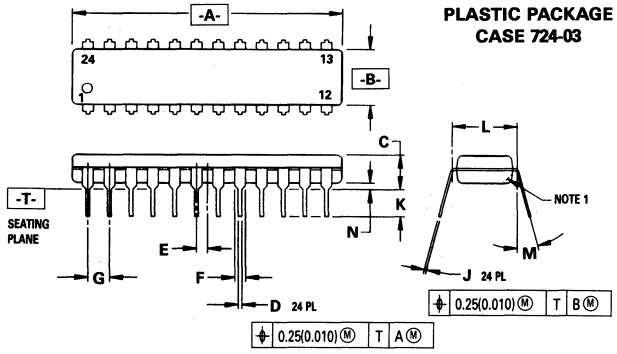
24-PIN PACKAGES



PLASTIC PACKAGE
CASE 709-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



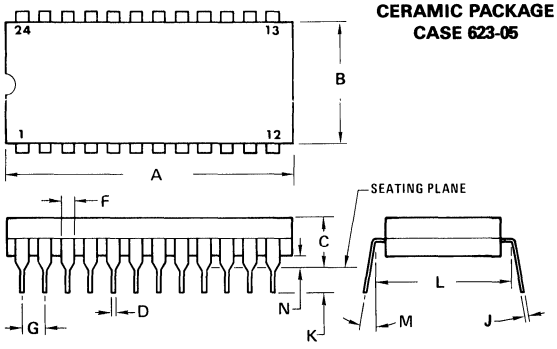
PLASTIC PACKAGE
CASE 724-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

7

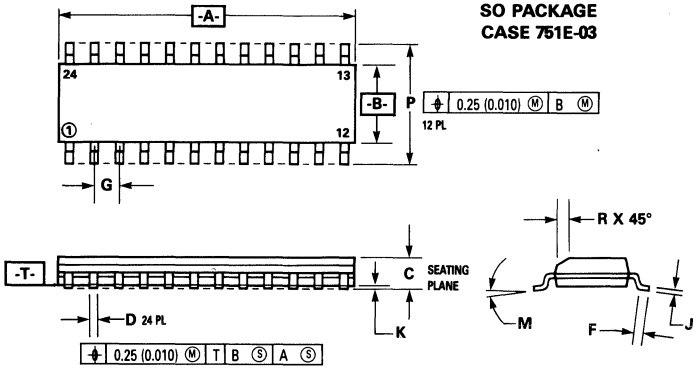
24-PIN PACKAGES (Continued)



CERAMIC PACKAGE
CASE 623-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).



SO PACKAGE
CASE 751E-03

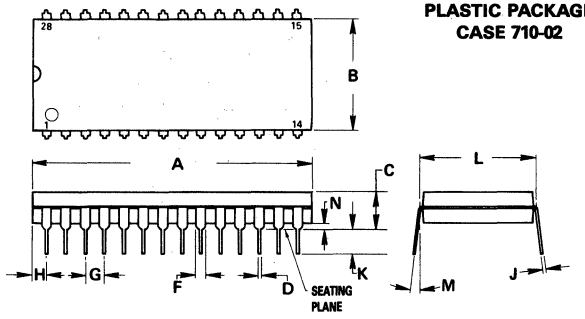
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

7

28-PIN PACKAGES

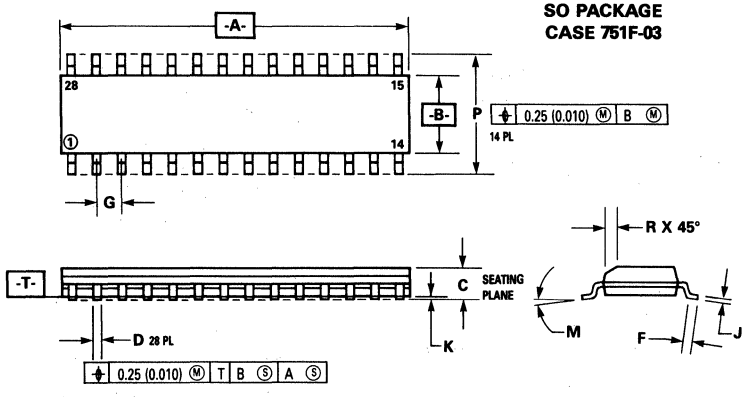
PLASTIC PACKAGE
CASE 710-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

SO PACKAGE
CASE 751F-03



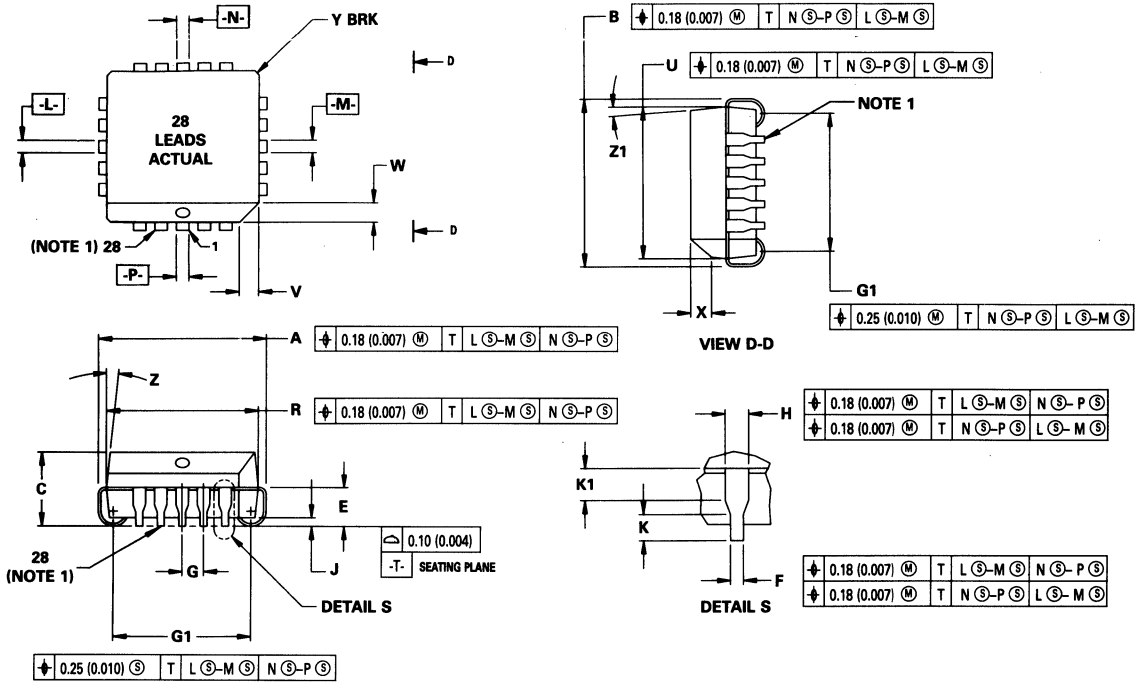
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

7

28-PIN PACKAGES (Continued)

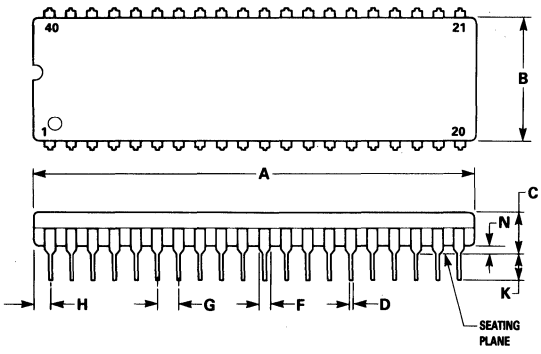
PLCC PACKAGE
CASE 776-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

40-PIN PACKAGE



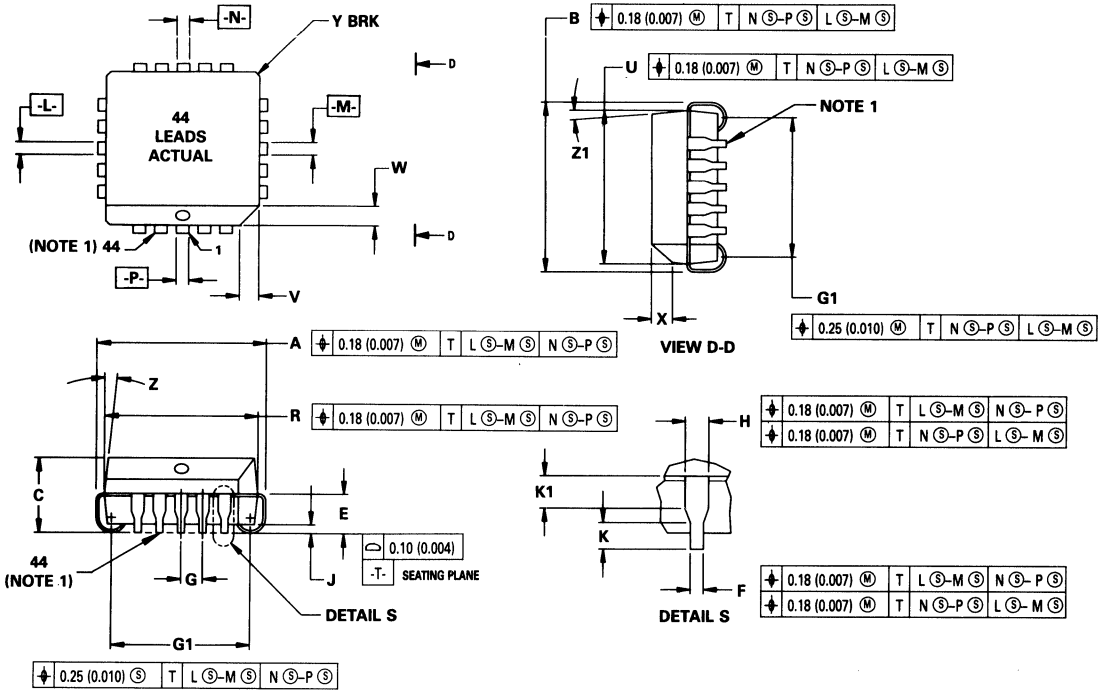
PLASTIC PACKAGE
CASE 711-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

44-LEAD PACKAGE

PLCC PACKAGE
CASE 777-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

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