DL113
REV 5

MOTOROLA

MEMORY DATA

MOTOROLA MEMORY DATA

Q2/89
DL113
REV 5

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

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MOTOROLA

MEMORIES

Prepared by
Technical Information Center

Motorola has developed a broad range of reliable memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, a selector guide is included to simplify the task of choosing the best combination of circuits for optimum system architecture.

New Motorola memories are being introduced continually. For the latest releases, and additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Series F

Printed in U.S.A.

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Selector Guide and Cross Reference

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MOS/CMOS

MOS/CMOS Dynamic RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
64K×4	MCM41464AP10 (P)	100	18
	MCM41464AP12 (P)	120	18
	MCM41464AP15 (P)	150	18
256K×1	MCM6256BP10 (P)	100	16
	MCM6256BP12 (P)	120	16
	MCM6256BP15 (P)	150	16
	MCM6257BP10 (N)	100	16
	MCM6257BP12 (N)	120	16
	MCM6257BP15 (N)	150	16
256K×4	MCM514256AP70 (P)#	70	20
	MCM514256AP80 (P)#	80	20
	MCM514256AP10 (P)#	100	20
	MCM514256AJ70 (P)#	70	20/26
	MCM514256AJ80 (P)#	80	20/26
	MCM514256AJ10 (P)#	100	20/26
	MCM514256AZ70 (P)#	70	20
	MCM514256AZ80 (P)#	80	20
	MCM514256AZ10 (P)#	100	20
	MCM514258AP70 (S)	70	20
	MCM514258AP80 (S)	80	20
	MCM514258AP10 (S)	100	20
	MCM514258AJ70 (S)	70	20/26
	MCM514258AJ80 (S)	80	20/26
	MCM514258AJ10 (S)	100	20/26
	MCM514258AZ70 (S)	70	20
	MCM514258AZ80 (S)	80	20
	MCM514258AZ10 (S)	100	20
1M×1	MCM511000AP70 (P)#	70	18
	MCM511000AP80 (P)#	80	18
	MCM511000AP10 (P)#	100	18
	MCM511000AJ70 (P)#	70	20/26
	MCM511000AJ80 (P)#	80	20/26
	MCM511000AJ10 (P)#	100	20/26
	MCM511000AZ70 (P)#	70	20
	MCM511000AZ80 (P)#	80	20
	MCM511000AZ10 (P)#	100	20
	MCM511001AP70 (N)	70	18
	MCM511001AP80 (N)	80	18
	MCM511001AP10 (N)	100	18
	MCM511001AJ70 (N)	70	20/26
	MCM511001AJ80 (N)	80	20/26
	MCM511001AJ10 (N)	100	20/26
	MCM511001AZ70 (N)	70	20
	MCM511001AZ80 (N)	80	20
	MCM511001AZ10 (N)	100	20
	MCM511002AP70 (S)	70	18
	MCM511002AP80 (S)	80	18
	MCM511002AP10 (S)	100	18
	MCM511002AJ70 (S)	70	20/26
	MCM511002AJ80 (S)	80	20/26
	MCM511002AJ10 (S)	100	20/26
	MCM511002AZ70 (S)	70	20
	MCM511002AZ80 (S)	80	20
	MCM511002AZ10 (S)	100	20

(P) Page Mode
(N) Nibble Mode
(S) Static Column

#Low power version available; order by MCM51L. . .

CMOS Dynamic RAM Modules

(+5 V, 0 to 70°C; 30-Lead SIMM Package)

Organization	Part Number	Access Time (ns max)	Pins
1M×8	MCM81000S80	80	30
	MCM81000S10	100	30
1M×9	MCM91000S80	80	30
	MCM91000S10	100	30

MOS Static RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
2K×8	MCM2018AN35	35	24
	MCM2018AN45	45	24

CMOS Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
4K×4	MCM1423P45	40	20
	IMS1423P-45	40	20
	MCM6168P45	45	20
	MCM6168P55	55	20
	MCM6168P70	70	20
	MCM6268P20	20	20
	MCM6268P25	25	20
	MCM6268P35	35	20
	MCM6268P45	45	20
	MCM6268P55	55	20
	MCM6269P25 (1)	25	20
	MCM6269P35 (1)	35	20
	MCM6270P20	20	22
	MCM6270P25	25	22
	MCM6270P35	35	22
	MCM6270J20	20	24
	MCM6270J25	25	24
	MCM6270J35	35	24
8K×8	MCM6064P10	100	28
	MCM6064P12	120	28
	MCM60L64P10	100	28
	MCM60L64P12	120	28
	MCM6164C45	45	28
	MCM6164C55	55	28
	MCM61L64C45	45	28
	MCM61L64C55	55	28
	MCM6164CC55 (2)	55	28
	MCM6164CC70 (2)	70	28
	MCM6264P25*	25	28
	MCM6264P30	30	28
	MCM6264P35	35	28
	MCM6264P45	45	28
	MCM6264P55	55	28
	MCM6264J25*	25	28
	MCM6264J30	30	28
	MCM6264J35	35	28
	MCM6264J45	35	28
	MCM6264J55	55	28

(Continued)

*To be introduced
(1) Fast chip select version
(2) Industrial temperature range, −40 to 85°C

CMOS Static RAMs (Continued)

Organization	Part Number	Access Time (ns max)	Pins
16K × 4	MCM6288P15*	15	22
	MCM6288P20*	20	22
	MCM6288P25	25	22
	MCM6288P30	30	22
	MCM6288P35	35	22
	MCM6288P45	45	22
	MCM6290P15* (3)	15	24
	MCM6290P20* (3)	20	24
	MCM6290P25 (3)	25	24
	MCM6290P30 (3)	30	24
	MCM6290P35 (3)	35	24
	MCM6290P45 (3)	45	24
	MCM6290J15* (3)	15	24
	MCM6290J20* (3)	20	24
	MCM6290J25 (3)	25	24
	MCM6290J30 (3)	30	24
	MCM6290J35 (3)	35	24
	MCM6290J45 (3)	45	24
64K × 1	MCM6287P15	15	22
	MCM6287P20	20	22
	MCM6287P25	25	22
	MCM6287P35	35	22
	MCM6287J15	15	24
	MCM6287J20	20	24
	MCM6287J25	25	24
	MCM6287J35	35	24
32K × 8	MCM60256AP85	85	28
	MCM60256AP10	100	28
	MCM60256AP12	120	28
	MCM60L256AP85	85	28
	MCM60L256AP10	100	28
	MCM60L256AP12	120	28
	MCM60256APC10 (2)	100	24
	MCM6206P20*	20	28
	MCM6206P25*	25	28
	MCM6206P35*	35	28
	MCM6206P45*	45	28
	MCM6206J20*	20	28
	MCM6206J25*	25	28
	MCM6206J35*	35	28
	MCM6206J45*	45	28
32K × 9	MCM6205P20*	20	32
	MCM6205P25*	25	32
	MCM6205J20*	20	32
	MCM6205J25*	25	32
64K × 4	MCM6208P20*	20	24
	MCM6208P25*	25	24
	MCM6208J20*	20	24
	MCM6208J25*	25	24
	MCM6209P20*	20	28
	MCM6209P25*	25	28
	MCM6209J20*	20	28
	MCM6209J25*	25	28
256K × 1	MCM6207P20*	20	24
	MCM6207P25*	25	24
	MCM6207J20*	20	24
	MCM6207J25*	25	24
128K × 8	MCM6226P30*	30	32
	MCM6226J30*	30	32
256K × 4	MCM6228P25*	25	28
	MCM6228J25*	25	28

*To be introduced
(2) Industrial temperature range, −40 to 85°C
(3) Output enable version

Synchronous Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
16K × 4	MCM6292P25*	25	28
	MCM6292P30*	30	28
	MCM6292P35*	35	28
	MCM6292J25*	25	28
	MCM6292J30*	30	28
	MCM6292J35*	35	28
	MCM6293P20*	20	28
	MCM6293P25*	25	28
	MCM6293P30*	30	28
	MCM6293J20*	20	28
	MCM6293J25*	25	28
	MCM6293J30*	30	28
	MCM6294P20*	20	28
	MCM6294P25	25	28
	MCM6294P30	30	28
	MCM6294J20*	20	28
	MCM6294J25	25	28
	MCM6294J30	30	28
	MCM6295P25	25	28
	MCM6295P30	30	28
	MCM6295P35	35	28
	MCM6295J25	25	28
	MCM6295J30	30	28
	MCM6295J35	35	28
4K × 10	MCM62963FN20*	20	44
	MCM62963FN25*	25	44
	MCM62963FN30*	30	44
	MCM62964FN20*	20	44
	MCM62964FN25*	25	44
	MCM62964FN30*	30	44
	MCM62965FN25*	25	44
	MCM62965FN30*	30	44
	MCM62965FN35*	35	44
4K × 12	MCM62973FN20*	20	44
	MCM62973FN25*	25	44
	MCM62973FN30*	30	44
	MCM62974FN20*	20	44
	MCM62974FN25*	25	44
	MCM62974FN30*	30	44
	MCM62975FN25*	25	44
	MCM62975FN30*	30	44
	MCM62975FN35*	35	44

CMOS Dual Port RAM

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
256 × 8	MCM68HC34L	240	40
	MCM68HC34P	240	40

CMOS EEPROM†

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (μs)	Pins
256 × 8	MCM2814P	3.5	8

†Available in Europe only.

SELECTOR GUIDE (Continued)

Cache Tag RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Address to Match Time (ns max)	Pins
4K×4	MCM62350P20*	20	24
	MCM62350P22*	22	24
	MCM62350P25	25	24
	MCM62350P30	30	24
	MCM62350J20*	20	24
	MCM62350J22*	22	24
	MCM62350J25	25	24
	MCM62350J30	30	24
	MCM62351P20*	20	24
	MCM62351P22*	22	24
	MCM62351P25	25	24
	MCM62351P30	30	24
	MCM62351J20*	20	24
	MCM62351J22*	22	24
	MCM62351J25	25	24
	MCM62351J30	30	24
	MCM4180P20*	20	22
	MCM4180P22*	22	22
	MCM4180P25	25	22
	MCM4180P30	30	22
	MCM5180J20*	20	24
	MCM4180J22*	22	24
	MCM4180J25	25	24
	MCM4180J30	30	24

*To be introduced

MECL

RAMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
8×2	MCM10143	15.3	24
16×4	MCM10145	15	16
16×4	MC10H145	6	16
64×1	MCM10148	15	16
128×1	MCM10147	15	16
256×1	MCM10144	26	16
256×1	MCM10152	15	16
1024×1	MCM10146	29	16

PROMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
32×8	MCM10139	20	16
256×4	MCM10149-10	10	16
256×4	MCM10149-25	25	16

CAM

(0 to 75°C)

Organization	Part Number	Associate Time (ns max)	Pins
8×2	MCM10H155	7	18

MILITARY PRODUCTS

CMOS Static RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
4K×4	6168-55/BRAJC	55	20
	6168-55/BUAJC	55	20
	6168-70/BRAJC	70	20
	6168-70/BUAJC	70	20
	6268-35/BRAJC	35	20
	6268-35/BUAJC	35	20
	6268-45/BRAJC	45	20
	6268-45/BUAJC	45	20
8K×8	6164-55/BXAJC	55	28
	6164-55/BUAJC	55	32
	6164-70/BXAJC	70	28
	6164-70/BUAJC	70	32
16K×4	6288-35/BXAJC	35	22
	6288-35/BUAJC	35	22
	6288-45/BXAJC	45	22
	6288-45/BUAJC	45	22
64K×1	6287-35/BXAJC	35	22
	6287-35/BUAJC	35	22
	6287-45/BXAJC	45	22
	6287-45/BUAJC	45	22
32K×8	6206-45/BXAJC*	45	28
	6206-55/BXAJC*	55	28
	6206-70/BXAJC*	70	28

CMOS Cache Tag RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
4K×4	4180-35/BXAJC*	35	22
	4180-45/BXAJC*	45	22

TTL RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
256K×4	93422/BWAJC	60	22
	93L422/BWAJC	75	22
	93L422A/BWAJC	55	22
1024×1	93415/BEAJC	45	16
	93415/BFAJC	45	16
	93425/BEAJC	45	16
	93425/BFAJC	45	16

*To be introduced

CROSS REFERENCE

The part numbers in the first column are arranged in alphanumeric sequence. The "Motorola Part Number" denotes what is believed to be the functional equivalent by pin function, except for differences in select/enable functions.

NOTE: The user must verify speed, power, and package interchangeability based on detailed specifications.

Motorola does not assume any liability arising out of the application or use of any product listed.

MOS Dynamic RAM Cross Reference

Competition Part Number	Motorola Part Number	Organization
AM90C255	**MCM6256B**	256K × 1
AM90C256	**MCM6256B**	256K × 1
HM50464	**MCM41464**	64K × 4
HM511000	**MCM511000A**	1M × 1
HM511001	**MCM511001A**	1M × 1
HM511002	**MCM511002A**	1M × 1
HM51256	**MCM6256B**	256K × 1
HM51256L	**MCM6256B**	256K × 1
HY51C100	**MCM511000A**	1M × 1
HY51C256	**MCM6256B**	256K × 1
HY51C464	**MCM41464**	64K × 4
HY51256L	**MCM6256B**	256K × 1
HY51464	**MCM41464**	64K × 4
KM41256A	**MCM6256B**	256K × 1
LH21256	**MCM6256B**	256K × 1
LH2464	**MCM41464**	64K × 4
LH2465	**MCM41464**	64K × 4
LH64256	**MCM514256A**	256K × 4
LH65257	**MCM514258A**	256K × 4
M41256N	**MCM6256B**	256K × 1
M41256P	**MCM6256B**	256K × 1
M441024K	**MCM514258A**	256K × 4
M441024P	**MCM514256A**	256K × 4
M5M4C1000	**MCM511000A**	1M × 1
M5M4C1001	**MCM511001A**	1M × 1
M5M4C1002	**MCM511002A**	1M × 1
M5M44C256	**MCM514256A**	256K × 4
M5M44C258	**MCM514258A**	256K × 4
M5M4464	**MCM41464**	64K × 4
MB81256	**MCM6256B**	256K × 1
MB81464	**MCM41464**	64K × 4
MN41256	**MCM6256B**	256K × 1
MSM41000	**MCM511000A**	1M × 1
MSM41001	**MCM511001A**	1M × 1
MSM41004	**MCM514256A**	256K × 4
MSM41005	**MCM514258A**	256K × 4
MSM41256	**MCM6256B**	256K × 1
MSM41464	**MCM41464**	64K × 4
MT1256	**MCM6256B**	256K × 1
MT4064	**MCM41464**	64K × 4
TC511000	**MCM511000A**	1M × 1
TC511001	**MCM511001A**	1M × 1
TC511002	**MCM511002A**	1M × 1
TMM41256	**MCM6256B**	256K × 1
TMM41464A	**MCM41464**	64K × 4

MOS DRAMs (Continued)

Competition Part Number	Motorola Part Number	Organization
TMS4256	**MCM6256B**	256K × 1
TMS4C1024	**MCM511000A**	1M × 1
TMS4C1025	**MCM511001A**	1M × 1
TMS4C1027	**MCM511002A**	1M × 1
TMS44C256	**MCM514256A**	256K × 4
TMS44C257	**MCM514258A**	256K × 4
TMS4464	**MCM41464**	64K × 4
μPD41256	**MCM6256B**	256K × 1
μPD41464	**MCM41464**	64K × 4
μPD421000	**MCM511000A**	1M × 1
μPD421001	**MCM511001A**	1M × 1
μPD421002	**MCM511002A**	1M × 1

MOS Static RAM Cross Reference

Part Number	Motorola Part Number	Organization
Am2168	**MCM1423/6268/IMS1423**	4K × 4
Am2169	**MCM6269**	4K × 4
Am9128	**MCM2018A**	2K × 8
Am99C164	**MCM6288**	16K × 4
Am99C165	**MCM6290**	16K × 4
Am99C641	**MCM6287**	64K × 1
Am99C68	**MCM1423/6268**	4K × 4
Am99C88	**MCM6164/61L64/6264**	8K × 8
Am99C88	**MCM6064/60L64**	8K × 8
Am99C88L	**MCM6164/61L64/6264**	8K × 8
Am99L68	**MCM1423/6268**	4K × 4
CDM62256	**MCM60256A/60L256A**	32K × 8
CDM6264	**MCM6064/60L64**	8K × 8
CXK5464	**MCM6288**	16K × 4
CXK5814	**MCM2018A**	2K × 8
CXK58255	**MCM6206**	32K × 8
CXK5864	**MCM6164/61L64/6264**	8K × 8
CXK5865	**MCM6164/61L64/6264**	8K × 8
CY7C128	**MCM2018A**	2K × 8
CY7C164	**MCM6288**	16K × 4
CY7C166	**MCM6290**	16K × 4
CY7C168	**MCM6268**	4K × 4
CY7C169	**MCM6269**	4K × 4
CY7C185	**MCM6264**	8K × 8
CYC7186	**MCM6164/61L64**	8K × 8

Continued

CROSS REFERENCE (Continued)

MOS SRAMs (Continued)

Part Number	Motorola Part Number	Organization
CY7C187	MCM6287	64K × 1
CY7C197	MCM6207	256K × 1
CY7C198	MCM6206	32K × 8
F1600	MCM6287	64K × 1
F1620/F1621	MCM6288	16K × 4
F1622	MCM6290	16K × 4
GM76C88	MCM6064/60L64	8K × 8
HM3-65768	MCM6268	4K × 4
HM3-65787	MCM6287	64K × 1
HM3-65788	MCM6288	16K × 4
HM6168H	MCM6268	4K × 4
HM6168HL	MCM6268	4K × 4
HM62256	MCM60256A/60L256A	32K × 8
HM6264	MCM6164/61L64/6064/6264	8K × 8
HM6264L	MCM6164/61L64/60L64/6264	8K × 8
HM6268	MCM6268	4K × 4
HM6268L	MCM6268	4K × 4
HM6287	MCM6287	64K × 1
HM6287L	MCM6287	64K × 1
HM-6516	MCM2018A	2K × 8
HM-65162	MCM2018A	2K × 8
HM-65172	MCM2018A	2K × 8
HM65681	MCM6268	4K × 4
HM65768	MCM6268	4K × 4
HM6788	MCM6288	16K × 4
HM6789	MCM6290	16K × 4
HM8832	MCM60256A	32K × 8
HY2116	MCM2018A	2K × 8
HY61C16	MCM2018A	2K × 8
HY61C68	MCM6268	4K × 4
HY61C68L	MCM6268	4K × 4
HY6116	MCM2018A	2K × 8
HY62C64	MCM6164/61L64/6264	8K × 8
HY62C87	MCM6287	64K × 1
HY62C88	MCM6288	16K × 4
HY63C256	MCM6206	32K × 8
IDT6116L	MCM2018A	2K × 8
IDT6116S	MCM2018A	2K × 8
IDT6168L	MCM6268	4K × 4
IDT6168LA	MCM6268	4K × 4
IDT6168S	MCM1423	4K × 4
IDT6168SA	MCM6268	4K × 4
IDT6169SA	MCM6269	4K × 4
IDT71256L	MCM60L256A	32K × 8
IDT71256S	MCM60256A	32K × 8
IDT7164L	MCM61L64/60L64	8K × 8
IDT7164S	MCM6164/6064/6264	8K × 8
IDT7187L	MCM6287	64K × 1
IDT7187S	MCM6287	64K × 1
IDT7188L	MCM6288	16K × 4
IDT7188S	MCM6288	16K × 4
IDT7198L	MCM6290	16K × 4
IDT7198S	MCM6290	16K × 4
IDT71256	MCM6206	32K × 8
IDT71257S	MCM6207	256K × 1
IDT8M864L	MCM60L64	8K × 8
IMS1420	MCM6268	4K × 4
IMS1420L	MCM6268	4K × 4
IMS1421	MCM6269	4K × 4
IMS1423	MCM6268	4K × 4

Part Number	Motorola Part Number	Organization
IMS1600	MCM6287	64K × 1
IMS1601	MCM6287	64K × 1
IMS1620	MCM6288	16K × 4
IMS1624	MCM6290	16K × 4
IMS1630	MCM6164/61L64/6264	8K × 8
KM6264	MCM6064	8K × 8
LH52251	MCM6207	256K × 1
MB61C71A	MCM6287	64K × 1
MB81C68	MCM6268	4K × 4
MB81C68A	MCM6268	4K × 4
MB81C68W	MCM6268	4K × 4
MB81C69A	MCM6269	4K × 4
MB81C71	MCM6287	64K × 1
MB81C74	MCM6288	16K × 4
MB81C78	MCM6164/61L64/6264	8K × 8
MB8128	MCM2018A	2K × 8
MB8168	MCM6268	4K × 4
MB8171	MCM6287	64K × 1
MB8416A	MCM2018A	2K × 8
MB8416A-L	MCM2018A	2K × 8
MB8417A	MCM2018A	2K × 8
MB8417A-L	MCM2018A	2K × 8
MB8418A	MCM2018A	2K × 8
MB8418A-L	MCM2018A	2K × 8
MB84256	MCM60256A	32K × 8
MB8464	MCM6064/60L64	8K × 8
MB8464-L	MCM60L64	8K × 8
MK41H68	MCM6268	4K × 4
MK41H69	MCM6269	4K × 4
MK41H80	MCM4180	4K × 4
MK4802	MCM2018A	2K × 8
MSM2128	MCM2018A	2K × 8
MSM5128	MCM2018A	2K × 8
MSM5165	MCM6064/60L64	8K × 8
MSM5165L	MCM6064/60L64	8K × 8
MSM5257	MCM6207	256K × 1
MS6168	MCM6268	4K × 4
MS6264	MCM6164/6IL64/6264	8K × 8
MS6264L	MCM61L64	8K × 8
MS6287	MCM6287	64K × 1
MS6288	MCM6288	16K × 4
M5M21C68	MCM6268	4K × 4
M5M5116	MCM2018A	2K × 8
M5M5117	MCM2018A	2K × 8
M5M5118	MCM2018A	2K × 8
M5M5165	MCM6164/61L64/6264	8K × 8
M5M5165-L	MCM6164/61L64/6264	8K × 8
M5M5178P	MCM6264	8K × 8
M5M5187	MCM6287	64K × 1
M5M5188	MCM6288	16K × 4
M5M5189	MCM6290	16K × 4
MT5C2561	MCM6207	256K × 1
MT5C2568	MCM6206	32K × 8
NMC2116	MCM2018A	2K × 8
NMC6164	MCM6164/61L64/6264	8K × 8
NMC6164L	MCM6164/61L64/6264	8K × 8
P4C164	MCM6264	8K × 8
P4C168	MCM6268	4K × 4
P4C187	MCM6287	64K × 1
P4C188	MCM6288	16K × 4

CROSS REFERENCE (Continued)

MOS SRAMs (Continued)

Part Number	Motorola Part Number	Organization
P4C198	**MCM6290**	16K × 4
P4C1257	**MCM6207**	256K × 1
PS6168	**MCM6268**	4K × 4
SCM21C16	**MCM2018A**	2K × 8
SCM6116	**MCM2018A**	2K × 8
SCM6116L	**MCM2018A**	2K × 8
SMJ5517	**MCM2018A**	2K × 8
SRM2016	**MCM2018A**	2K × 8
SRM20256	**MCM60256A**	32K × 8
SRM2064	**MCM6064/60L64**	8K × 8
SRM2261	**MCM6287**	64K × 1
SRM2264	**MCM6164/61L64/6064/60L64**	8K × 8
SRM2268	**MCM6268**	4K × 4
SRM2274	**MCM6288**	16K × 4
SRM2275H	**MCM6290**	16K × 4
SR16K4	**MCM6288**	4K × 4
SR64E4	**MCM6290**	16K × 4
SR64K1	**MCM6287**	64K × 1
SR64K4	**MCM6288**	16K × 4
SR64K8	**MCM6164/61L64/6264**	8K × 8
SSL4180	**MCM4180**	4K × 4
SSM6168	**MCM6268**	4K × 4
SSM6170	**MCM6270**	4K × 4
SSM7164	**MCM6264**	8K × 8
SSM7166	**MCM6290**	16K × 4
SSM7188	**MCM6288**	16K × 4
SSM7192	**MCM6292**	16K × 4
SSM7193	**MCM6293**	16K × 4
SSM7194	**MCM6294**	16K × 4
SSM7195	**MCM6295**	16K × 4
STC2168	**MCM6268**	4K × 4
STC2168L	**MCM6268**	4K × 4
STC2168M	**MCM6268**	4K × 4
STC6264	**MCM6064/60L64**	8K × 8
S6516	**MCM2018A**	2K × 8
TC5517B	**MCM2018A**	2K × 8
TC5517B-L	**MCM2018A**	2K × 8
TC5518C	**MCM2018A**	2K × 8
TC5518C-L	**MCM2018A**	2K × 8
TC55257	**MCM60256**	32K × 8
TC55257L	**MCM60L256A**	32K × 8
TC55416	**MCM6288**	16K × 4
TC55417	**MCM6290**	16K × 4
TC5561	**MCM6287**	64K × 1
TC5562	**MCM6287**	64K × 1

Part Number	Motorola Part Number	Organization
TC5565	**MCM6064/60L64**	8K × 8
TC5565-L	**MCM6064/60L64**	8K × 8
TMM2015A	**MCM2018A**	2K × 8
TMM2016	**MCM2018A**	2K × 8
TMM2016A	**MCM2018A**	2K × 8
TMM2018	**MCM2018A**	2K × 8
TMM2019	**MCM2018A**	2K × 8
TMM2063	**MCM6064/60L64**	8K × 8
TMM2064	**MCM6064/60L64**	8K × 8
TMM2068	**MCM6268**	4K × 4
TMM2088	**MCM6164/61L64/6264**	8K × 8
TMS4016	**MCM2018A**	2K × 8
UM2128	**MCM2018A**	2K × 8
UM2129	**MCM2016H**	2K × 8
UM6116	**MCM2018A**	2K × 8
UM6168	**MCM6268**	4K × 4
μPD4016	**MCM2018A**	2K × 8
μPD4168	**MCM6064**	8K × 8
μPD42832	**MCM60256A**	32K × 8
μPD4314	**MCM6268**	4K × 4
μPD43256	**MCM60256A**	32K × 8
μPD43257-L	**MCM60L256A**	32K × 8
μPD4361	**MCM6287**	64K × 1
μPD4362	**MCM6288**	16K × 4
μPD4364	**MCM6164/61L64/6264**	8K × 8
μPD4364L	**MCM6064/60L64**	8K × 8
μPD446	**MCM2018A**	2K × 8
μPD4464	**MCM6064/60L64**	8K × 8
μPD449	**MCM2018A**	2K × 8
VT20C68	**MCM6268**	4K × 4
VT20C69	**MCM6269**	4K × 4
VT64KS4	**MCM6288**	16K × 4
VT65KS4	**MCM6290**	16K × 4
V61C62	**MCM6288**	16K × 4
V61C68	**MCM6268**	4K × 4
V62C64	**MCM6164/61L64/6264**	8K × 8
51C68	**MCM6268**	4K × 4
51C69	**MCM6269**	4K × 4
8808CL	**MCM60L64**	8K × 8
8832C	**MCM60256A**	32K × 8

MOS Dynamic RAMs 2

2

MOS/CMOS Dynamic RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
64K × 4	MCM41464AP10 (P)	100	18
	MCM41464AP12 (P)	120	18
	MCM41464AP15 (P)	150	18
256K × 1	MCM6256BP10 (P)	100	16
	MCM6256BP12 (P)	120	16
	MCM6256BP15 (P)	150	16
	MCM6257BP10 (N)	100	16
	MCM6257BP12 (N)	120	16
	MCM6257BP15 (N)	150	16
256K × 4	MCM514256AP70 (P)#	70	20
	MCM514256AP80 (P)#	80	20
	MCM514256AP10 (P)#	100	20
	MCM514256AJ70 (P)#	70	20/26
	MCM514256AJ80 (P)#	80	20/26
	MCM514256AJ10 (P)#	100	20/26
	MCM514256AZ70 (P)#	70	20
	MCM514256AZ80 (P)#	80	20
	MCM514256AZ10 (P)#	100	20
	MCM514258AP70 (S)	70	20
	MCM514258AP80 (S)	80	20
	MCM514258AP10 (S)	100	20
	MCM514258AJ70 (S)	70	20/26
	MCM514258AJ80 (S)	80	20/26
	MCM514258AJ10 (S)	100	20/26
	MCM514258AZ70 (S)	70	20
	MCM514258AZ80 (S)	80	20
	MCM514258AZ10 (S)	100	20

Organization	Part Number	Access Time (ns max)	Pins
1M × 1	MCM511000AP70 (P)#	70	18
	MCM511000AP80 (P)#	80	18
	MCM511000AP10 (P)#	100	18
	MCM511000AJ70 (P)#	70	20/26
	MCM511000AJ80 (P)#	80	20/26
	MCM511000AJ10 (P)#	100	20/26
	MCM511000AZ70 (P)#	70	20
	MCM511000AZ80 (P)#	80	20
	MCM511000AZ10 (P)#	100	20
	MCM511001AP70 (N)	70	18
	MCM511001AP80 (N)	80	18
	MCM511001AP10 (N)	100	18
	MCM511001AJ70 (N)	70	20/26
	MCM511001AJ80 (N)	80	20/26
	MCM511001AJ10 (N)	100	20/26
	MCM511001AZ70 (N)	70	20
	MCM511001AZ80 (N)	80	20
	MCM511001AZ10 (N)	100	20
	MCM511002AP70 (S)	70	18
	MCM511002AP80 (S)	80	18
	MCM511002AP10 (S)	100	18
	MCM511002AJ70 (S)	70	20/26
	MCM511002AJ80 (S)	80	20/26
	MCM511002AJ10 (S)	100	20/26
	MCM511002AZ70 (S)	70	20
	MCM511002AZ80 (S)	80	20
	MCM511002AZ10 (S)	100	20

(P) Page Mode
(N) Nibble Mode
(S) Static Column

#Low power version available; order by MCM51L. . .

CMOS Dynamic RAM Modules

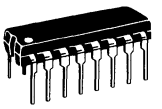
(+5 V, 0 to 70°C; 30-Lead SIMM Package)

Organization	Part Number	Access Time (ns max)	Pins
1M × 8	MCM81000S80	80	30
	MCM81000S10	100	30
1M × 9	MCM91000S80	80	30
	MCM91000S10	100	30

MCM6256B

2

256K-Bit Dynamic RAM



P PACKAGE
PLASTIC
CASE 648D

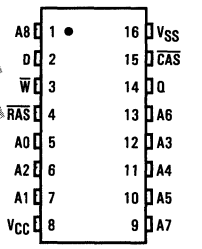
The MCM6256B is a 262,144 bit, high-speed, dynamic random access memory. Organized as 262,144 one-bit words and fabricated using N-channel silicon-gate MOS technology, this single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. All inputs and outputs are fully TTL compatible.

By multiplexing row and column address inputs, the MCM6256B requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

The MCM6256B features "page mode" which allows random column accesses of the 512 bits within the selected row.

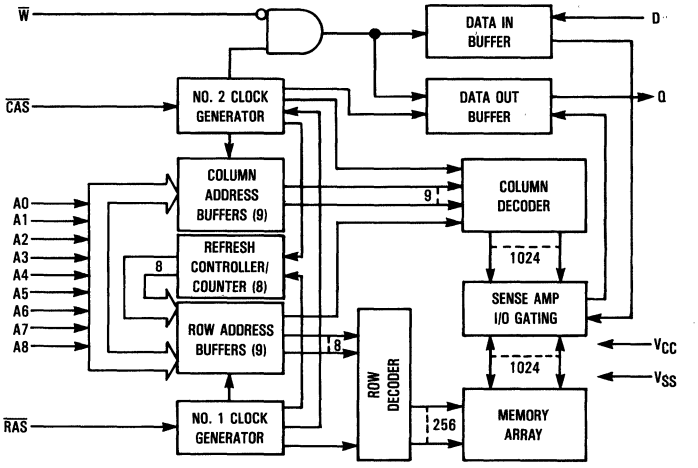
- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM6256B-10 = 100 ns
  MCM6256B-12 = 120 ns
  MCM6256B-15 = 150 ns
- Low Power Dissipation: MCM6256B-10 = 440 mW Maximum (Active)
  MCM6256B-12 = 396 mW Maximum (Active)
  MCM6256B-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- Page Mode Capability

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM6256B-10, t_{RC} = 190 ns		–	80		
MCM6256B-12, t_{RC} = 220 ns		–	72		
MCM6256B-15, t_{RC} = 260 ns		–	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM6256B-10, t_{RC} = 190 ns		–	70		
MCM6256B-12, t_{RC} = 220 ns		–	62		
MCM6256B-15, t_{RC} = 260 ns		–	55		
V_{CC} Power Supply Current During Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM6256B-10, t_{PC} = 100 ns		–	60		
MCM6256B-12, t_{PC} = 120 ns		–	55		
MCM6256B-15, t_{PC} = 145 ns		–	50		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM6256B-10, t_{RC} = 190 ns		–	70		
MCM6256B-12, t_{RC} = 220 ns		–	62		
MCM6256B-15, t_{RC} = 260 ns		–	55		
Input Leakage Current (V_{SS} < V_{in} < V_{CC})	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, V_{SS} < V_{out} < V_{CC})	$I_{lkg(O)}$	−10	10	μA	
Output Logic 1 Voltage (I_{out} = −5 mA)	V_{OH}	2.4	–	V	
Output Logic 0 Voltage (I_{out} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit	Notes
Input Capacitance	A0-A8, D	C_{in}	–	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		–	7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	–	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM6256B-10		MCM6256B-12		MCM6256B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	–	220	–	260	–	ns	4, 5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	200	–	240	–	285	–	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	220	–	260	–	310	–	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	100	–	120	–	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	50	–	60	–	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	5	25	5	30	5	35	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	–	90	–	100	–	ns	–
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	–
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	–	15	–	15	–	ns	–
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	25	–	30	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	–	85	–	105	–	ns	–
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	–
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	–	15	–	20	–	ns	11
Write Command Hold Time	t_{CELWH}	t_{WCH}	20	–	25	–	30	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	70	–	85	–	105	–	ns	–
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	25	–	30	–	ns	–
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	25	–	35	–	45	–	ns	–
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	25	–	35	–	45	–	ns	–
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	25	–	30	–	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	70	–	85	–	105	–	ns	–
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	–	60	–	75	–	ns	–
Refresh Period	t_{RVRV}	t_{RFSH}	–	4	–	4	–	4	ms	–

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

2

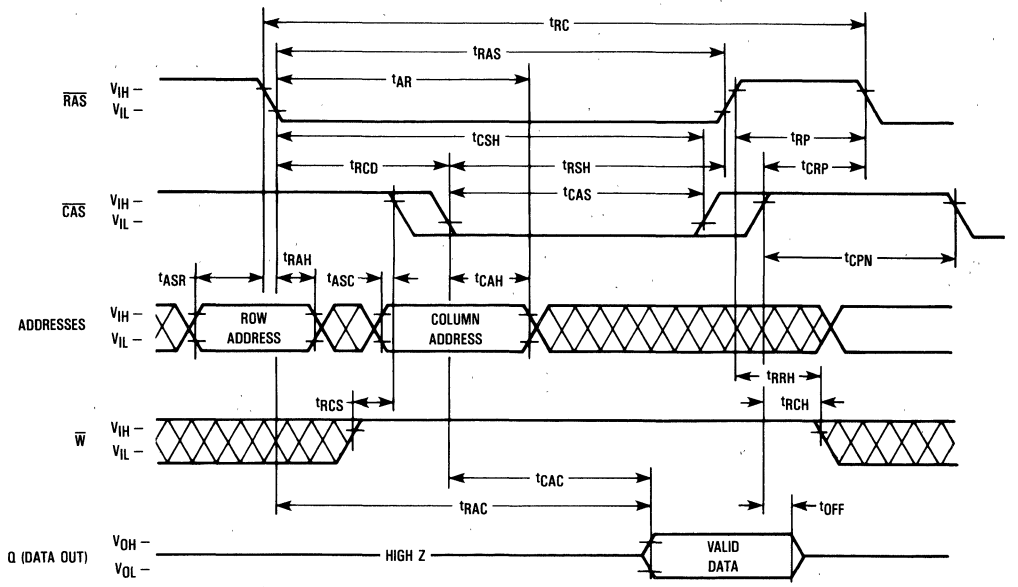
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM6256B-10		MCM6256B-12		MCM6256B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	30	–	40	–	50	–	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	–	100	–	125	–	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	20	–	25	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	40	–	50	–	60	–	ns	–
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	100	–	120	–	145	–	ns	–
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	110	–	140	–	170	–	ns	–
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRMW}	130	–	160	–	195	–	ns	–
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	–
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	50	–	60	–	ns	–

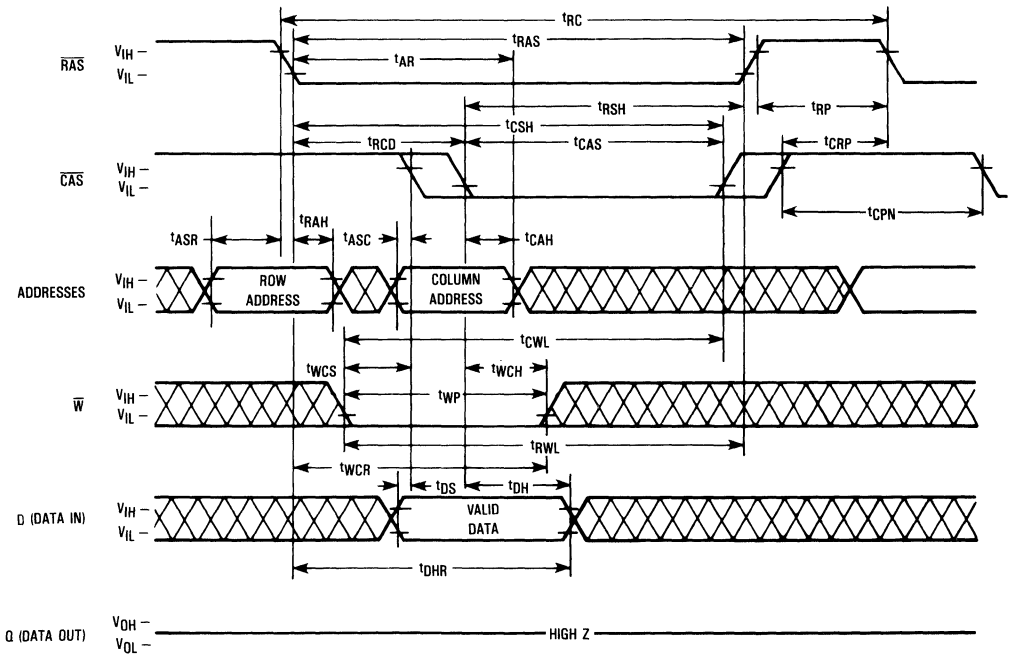
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

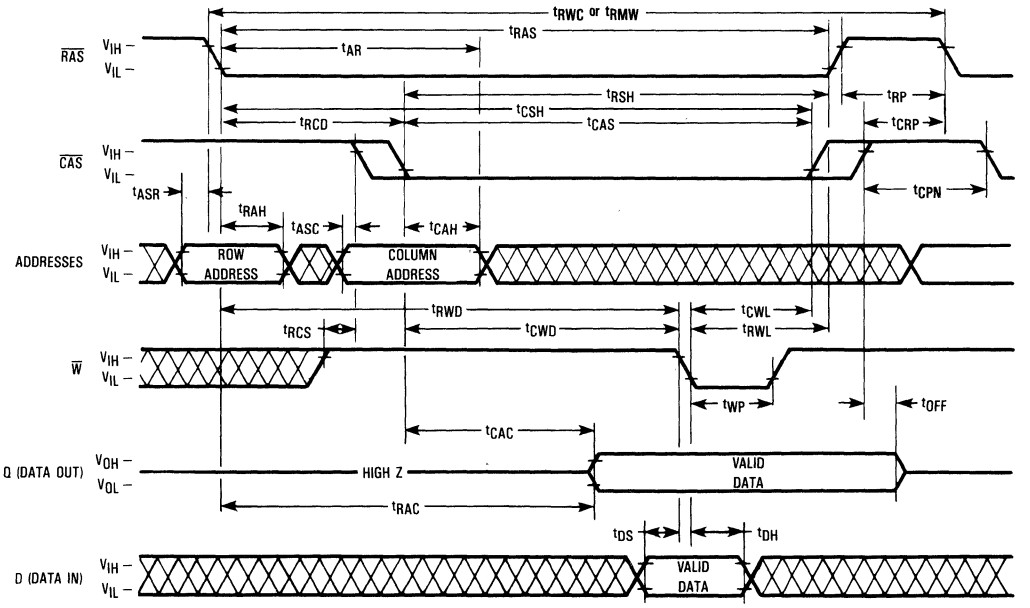
READ CYCLE TIMING



WRITE CYCLE TIMING

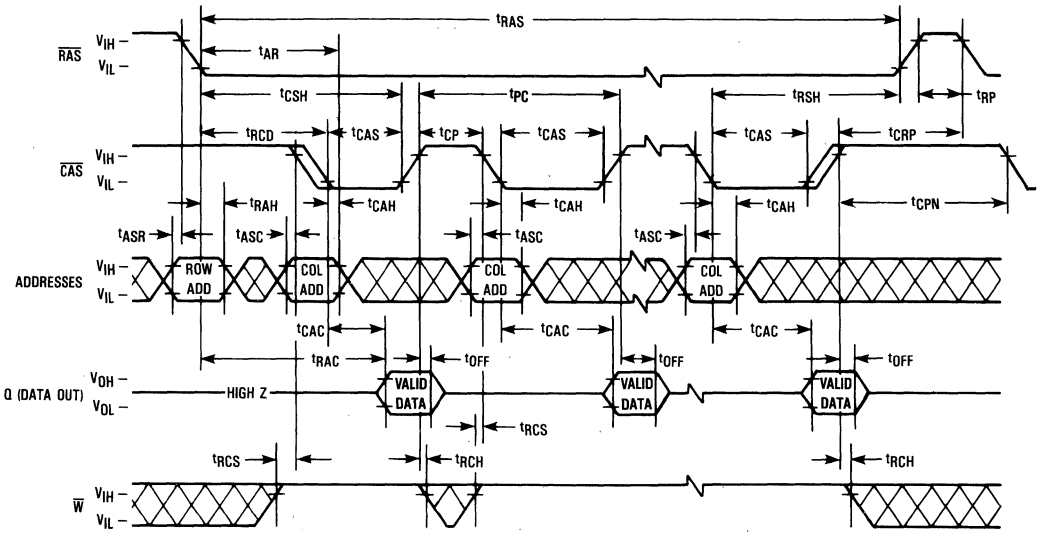


READ-WRITE/READ-MODIFY-WRITE CYCLE

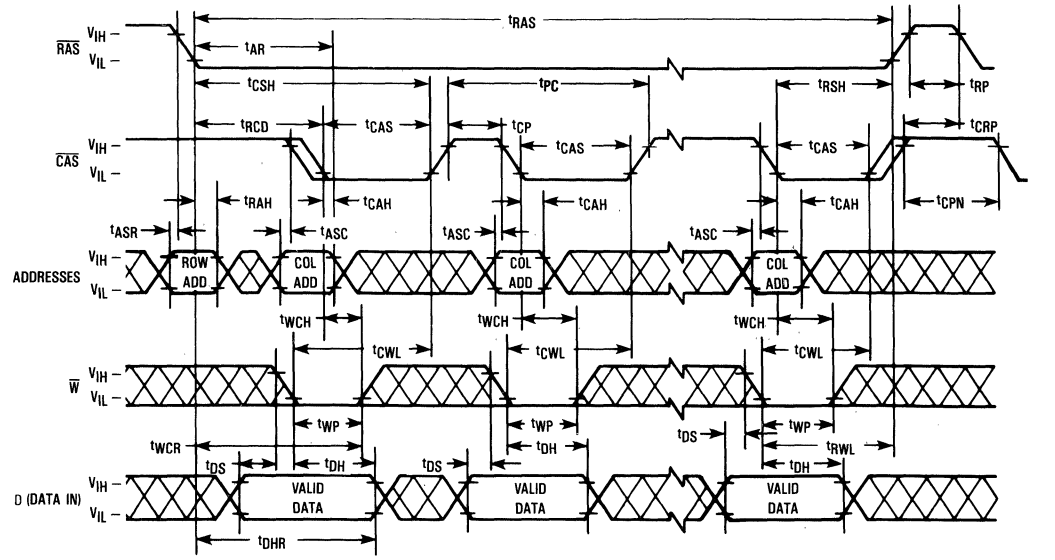


2

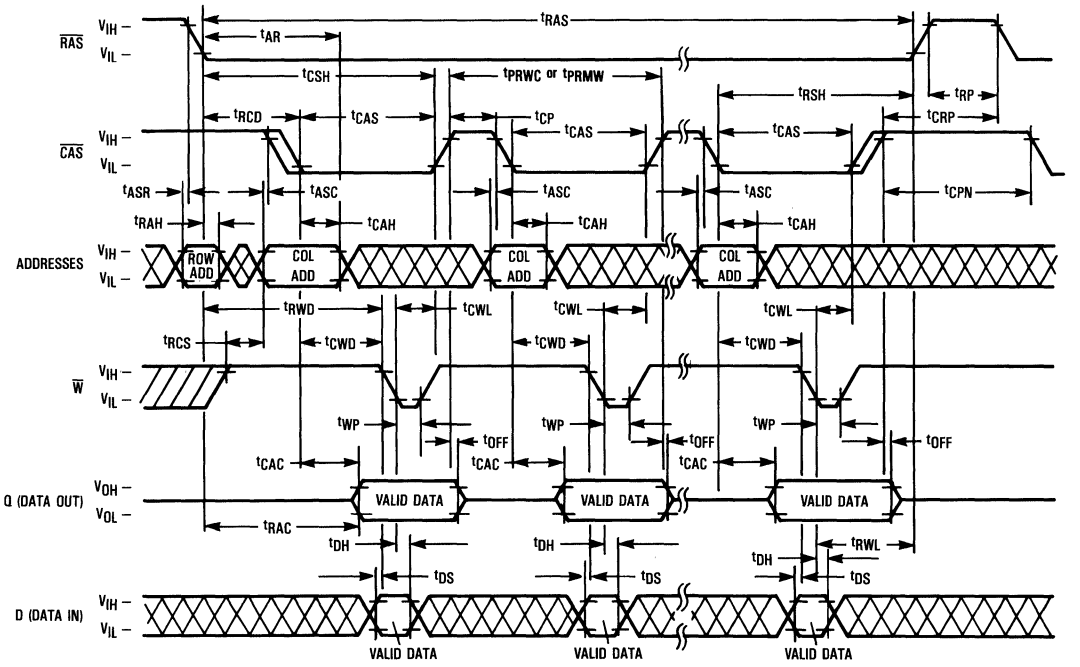
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

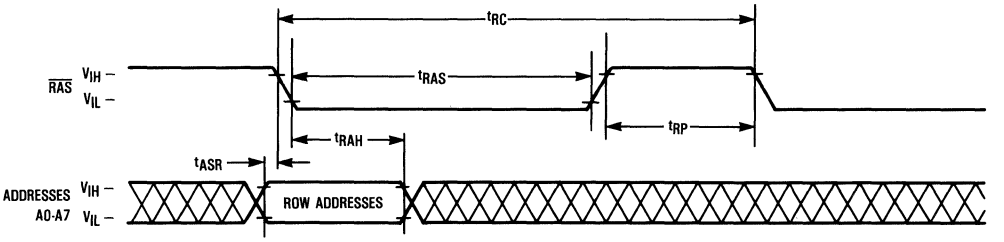


PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



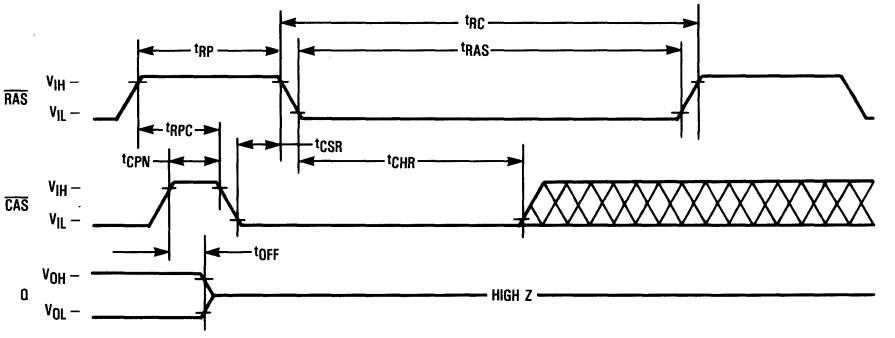
RAS-ONLY REFRESH CYCLE

(D, W, and A8 are Don't Care, CAS is High)



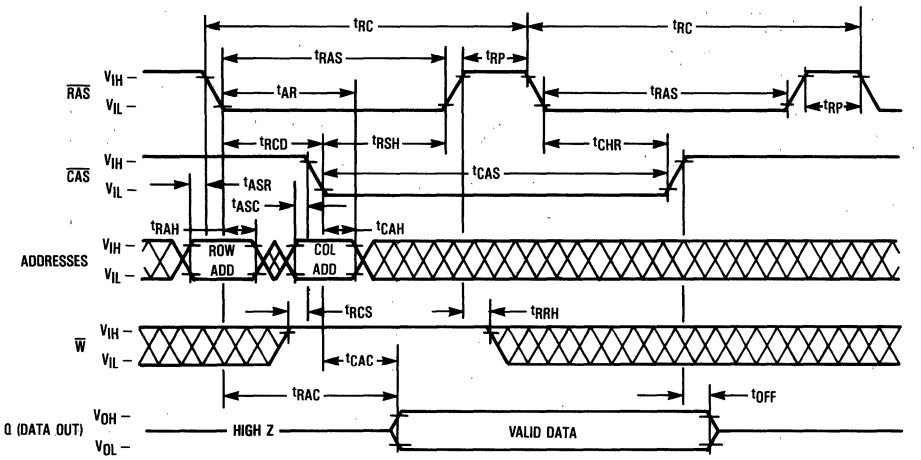
CAS-BEFORE RAS REFRESH CYCLE

(W, D, and A0-A8 are Don't Care)

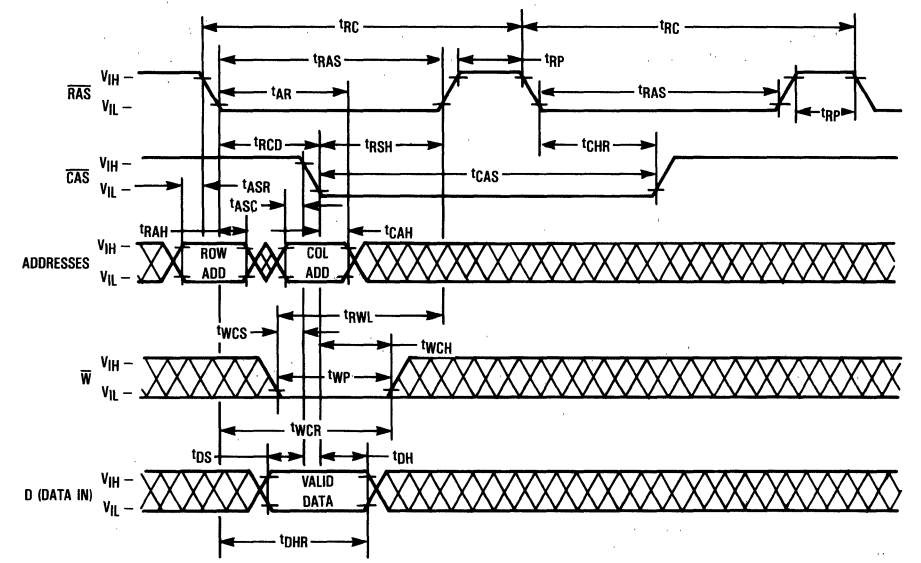


2

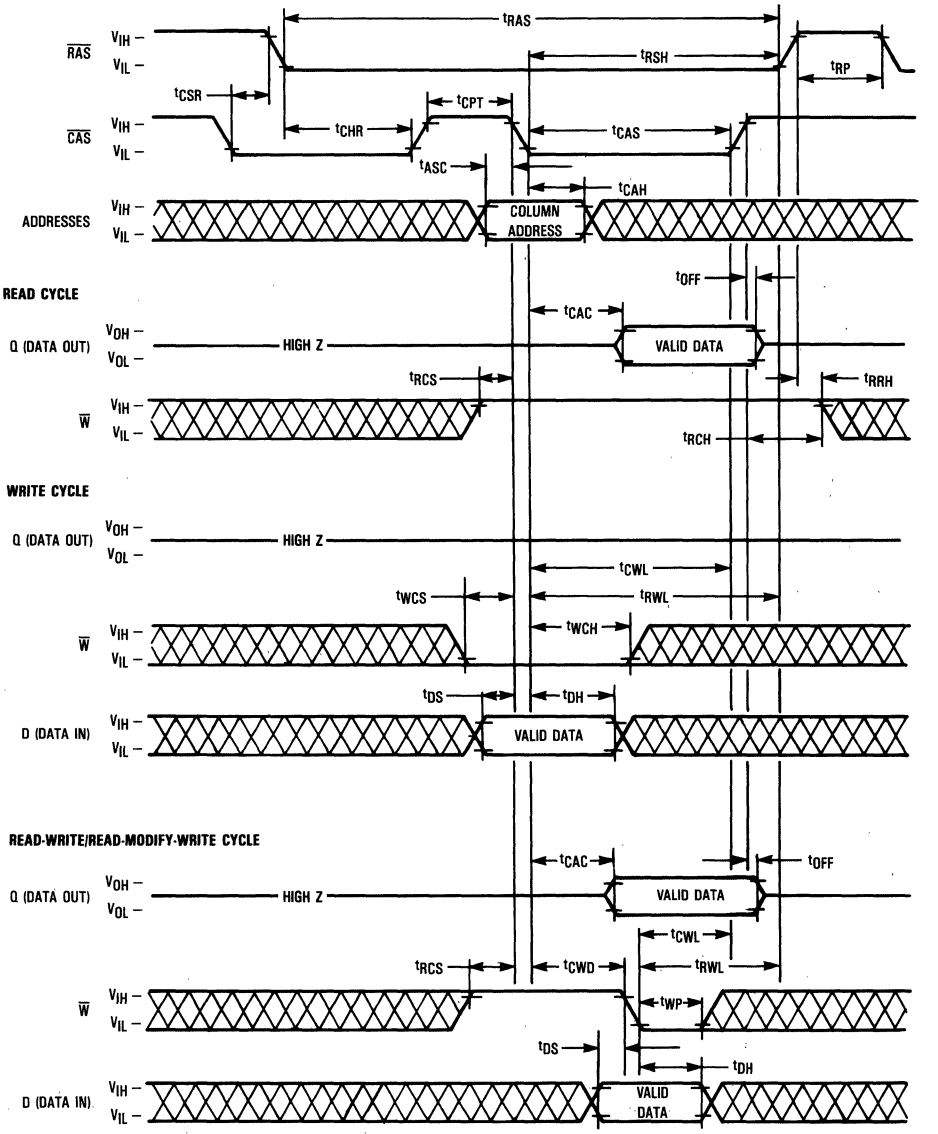
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called page mode, allows the user to column access the 512 bits within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out

occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 512 column locations on a given row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 256K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM6256B can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

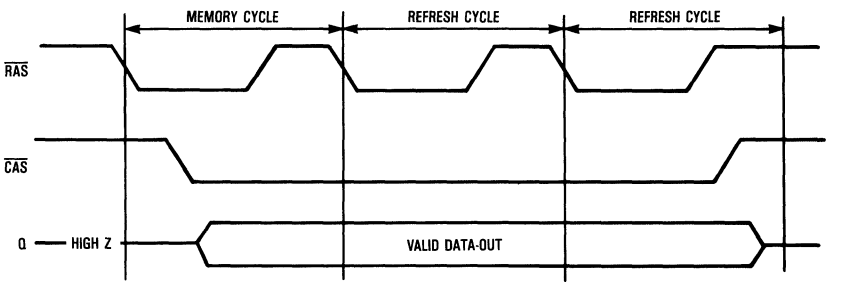
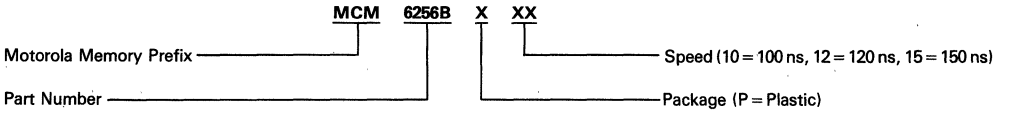


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)

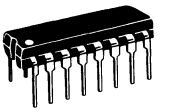


Full Part Numbers — MCM6256BP10
MCM6256BP12
MCM6256BP15

MCM6257B

2

256K x 1 Nibble Mode Dynamic RAM



P PACKAGE
PLASTIC
CASE 648D

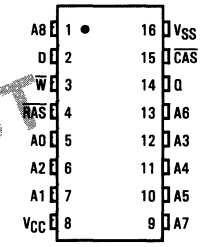
The MCM6257B is a 262,144 bit, high-speed, dynamic random access memory. Organized as 262,144 one-bit words and fabricated using N-channel silicon-gate MOS technology, this single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. All inputs and outputs are fully TTL compatible.

By multiplexing row and column address inputs, the MCM6257B requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

The MCM6257B features "nibble mode" which allows serial access of 4 bits of data at a high data rate.

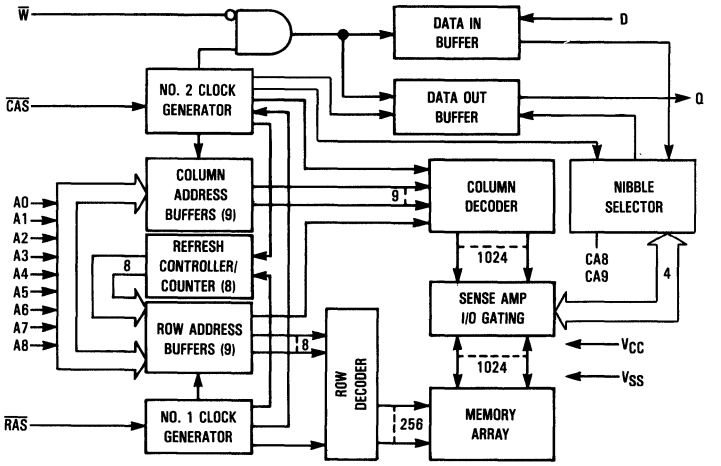
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM6257B-10 = 100 ns
  MCM6257B-12 = 120 ns
  MCM6257B-15 = 150 ns
- Low Power Dissipation: MCM6257B-10 = 440 mW Maximum (Active)
  MCM6257B-12 = 396 mW Maximum (Active)
  MCM6257B-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ and $\overline{RAS}$-Only Refresh Modes
- Hidden Refresh
- Fast Nibble Mode Access and Cycle Time (MCM6257B-10) = 25 ns Access Time
  50 ns Cycle Time

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM6257B-10, t_{RC} = 190 ns		—	80		
MCM6257B-12, t_{RC} = 220 ns		—	72		
MCM6257B-15, t_{RC} = 260 ns		—	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM6257B-10, t_{RC} = 190 ns		—	70		
MCM6257B-12, t_{RC} = 220 ns		—	62		
MCM6257B-15, t_{RC} = 260 ns		—	55		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM6257B-10, t_{NC} = 50 ns		—	50		
MCM6257B-12, t_{NC} = 60 ns		—	48		
MCM6257B-15, t_{NC} = 70 ns		—	45		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM6257B-10, t_{RC} = 190 ns		—	70		
MCM6257B-12, t_{RC} = 220 ns		—	62		
MCM6257B-15, t_{RC} = 260 ns		—	55		
Input Leakage Current (V_{SS} < V_{in} < V_{CC})	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, V_{SS} < V_{out} < V_{CC})	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit	Notes
Input Capacitance	A0-A8, D	C_{in}	—	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		—	7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	—	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM6257B-10		MCM6257B-12		MCM6257B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	–	220	–	260	–	ns	4, 5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	200	–	240	–	285	–	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	220	–	260	–	310	–	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	100	–	120	–	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	50	–	60	–	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	5	25	5	30	5	35	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	–	90	–	100	–	ns	–
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	–
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	–	15	–	15	–	ns	–
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	25	–	30	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	–	85	–	105	–	ns	–
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	–
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	–	15	–	20	–	ns	11
Write Command Hold Time	t_{CELWH}	t_{WCH}	20	–	25	–	30	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	70	–	85	–	105	–	ns	–
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	25	–	30	–	ns	–
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	25	–	35	–	45	–	ns	–
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	25	–	35	–	45	–	ns	–
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	25	–	30	–	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	70	–	85	–	105	–	ns	–
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	–	60	–	75	–	ns	–
Refresh Period	t_{RVRV}	t_{RFSH}	–	4	–	4	–	4	ms	–

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

2

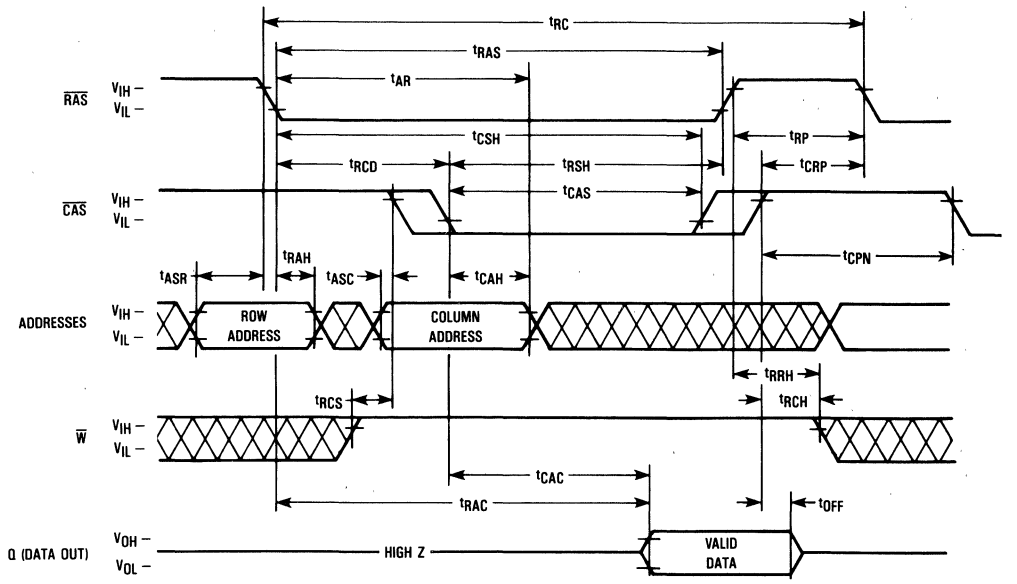
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM6257B-10		MCM6257B-12		MCM6257B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	30	–	40	–	50	–	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	–	100	–	125	–	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	20	–	25	–	ns	–
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	50	–	60	–	70	–	ns	–
Nibble Mode Read-Write/Read-Modify-Write Cycle Time	t_{CEHCEH}	t_{NRWC}	75	–	90	–	105	–	ns	–
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	25	–	30	–	40	–	ns	–
Nibble Mode $\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{NCAS}	25	–	30	–	40	–	ns	–
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	15	–	20	–	20	–	ns	–
Nibble Mode $\overline{RAS}$ Hold Time (Read)	t_{CELREH}	t_{NRRSH}	20	–	25	–	30	–	ns	–
Nibble Mode $\overline{RAS}$ Hold Time (Write)	t_{CELREH}	t_{NWRSH}	40	–	45	–	50	–	ns	–
Nibble Mode $\overline{CAS}$ to Write Delay Time	t_{CELWH}	t_{NCWD}	25	–	30	–	40	–	ns	–
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	20	–	25	–	30	–	ns	–
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	–
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	50	–	60	–	ns	–

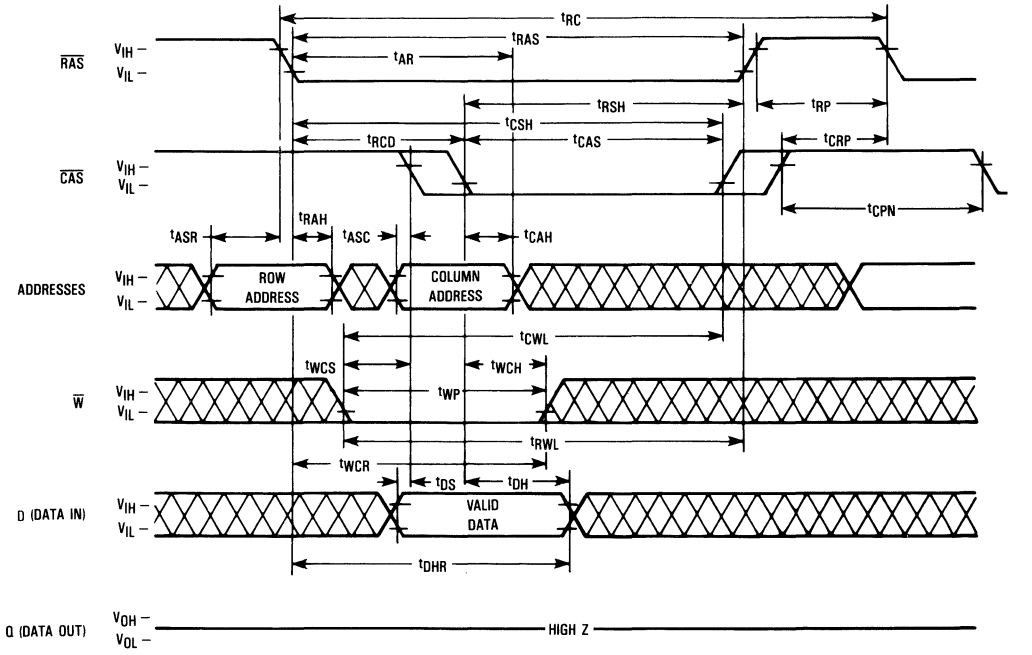
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

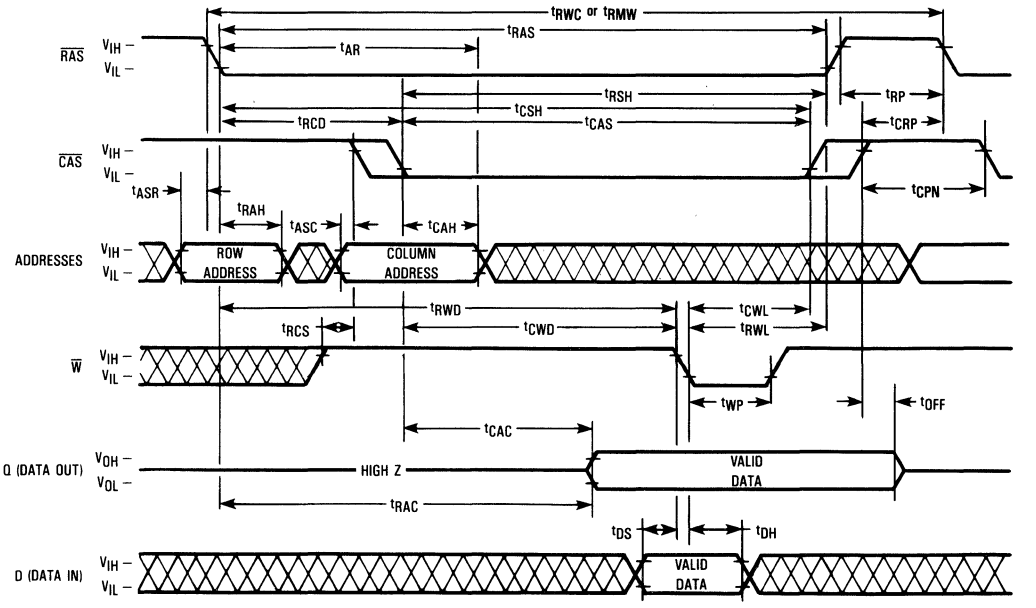
READ CYCLE TIMING



WRITE CYCLE TIMING

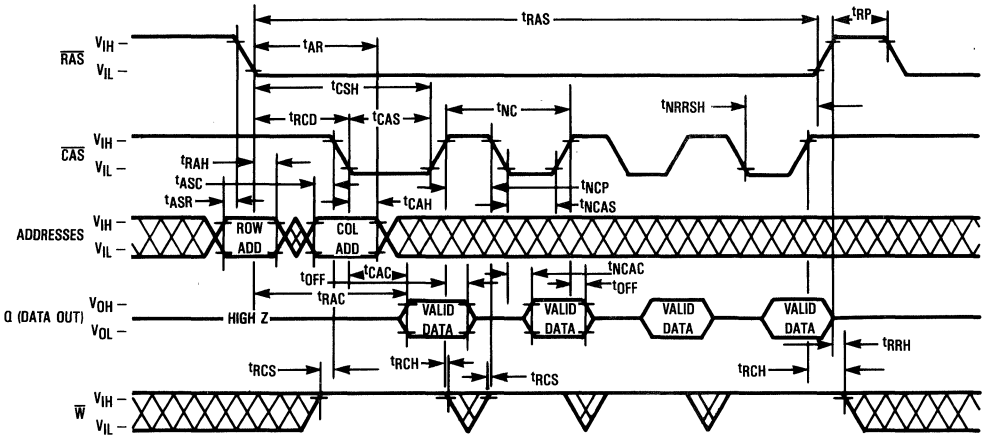


READ-WRITE/READ-MODIFY-WRITE CYCLE

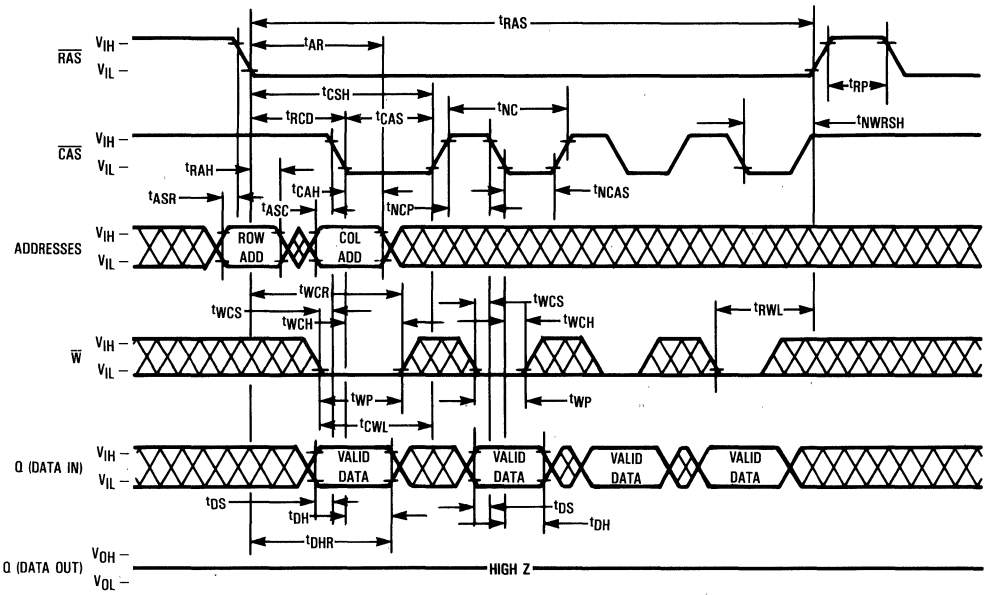


2

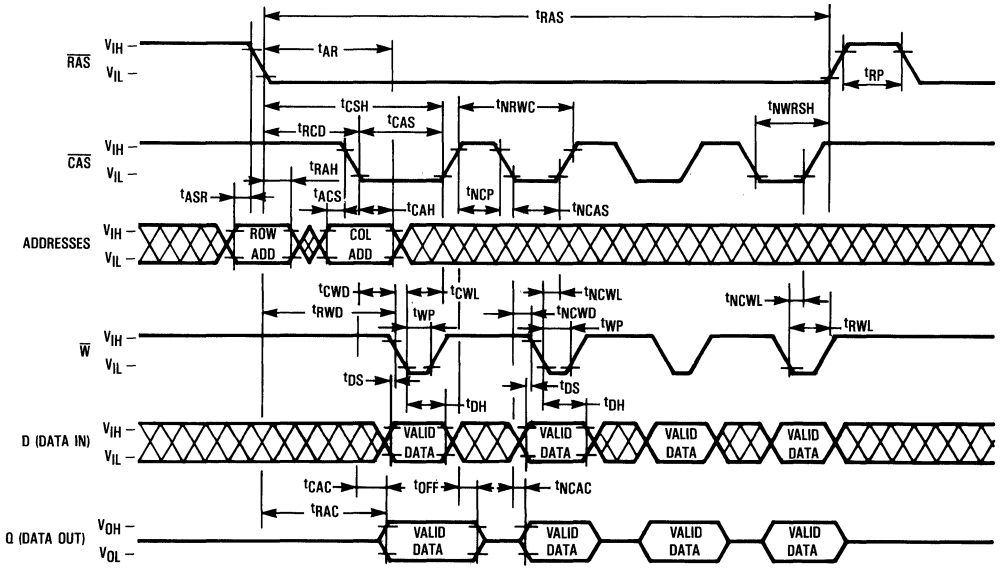
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)

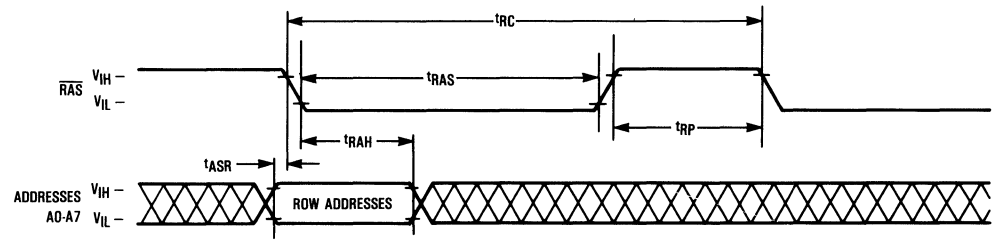


NIBBLE MODE READ-WRITE/READY-MODIFY-WRITE CYCLE



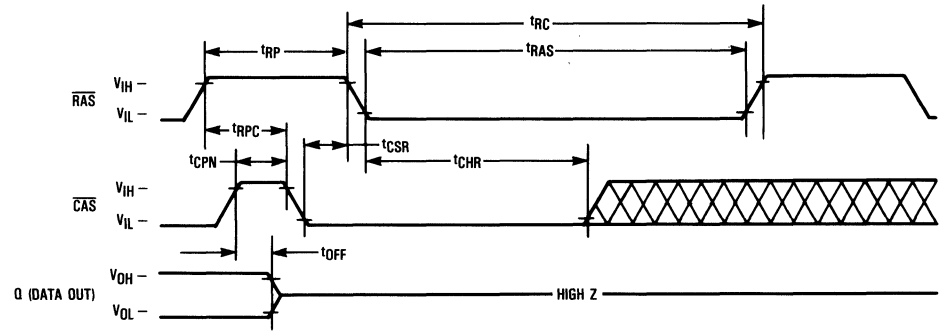
RAS-ONLY REFRESH CYCLE

(D, W, and A8 are Don't Care, CAS is High)



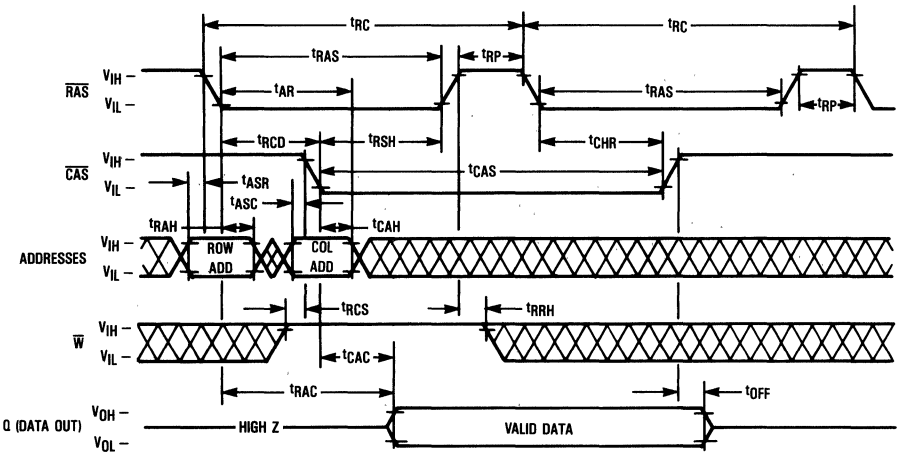
CAS-BEFORE RAS REFRESH CYCLE

(W, D, and A0-A8 are Don't Care)

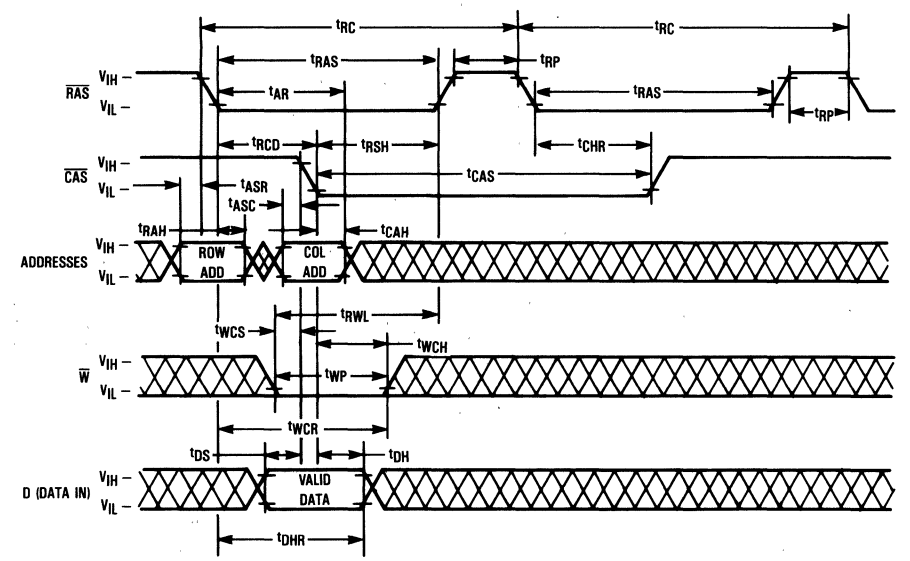


2

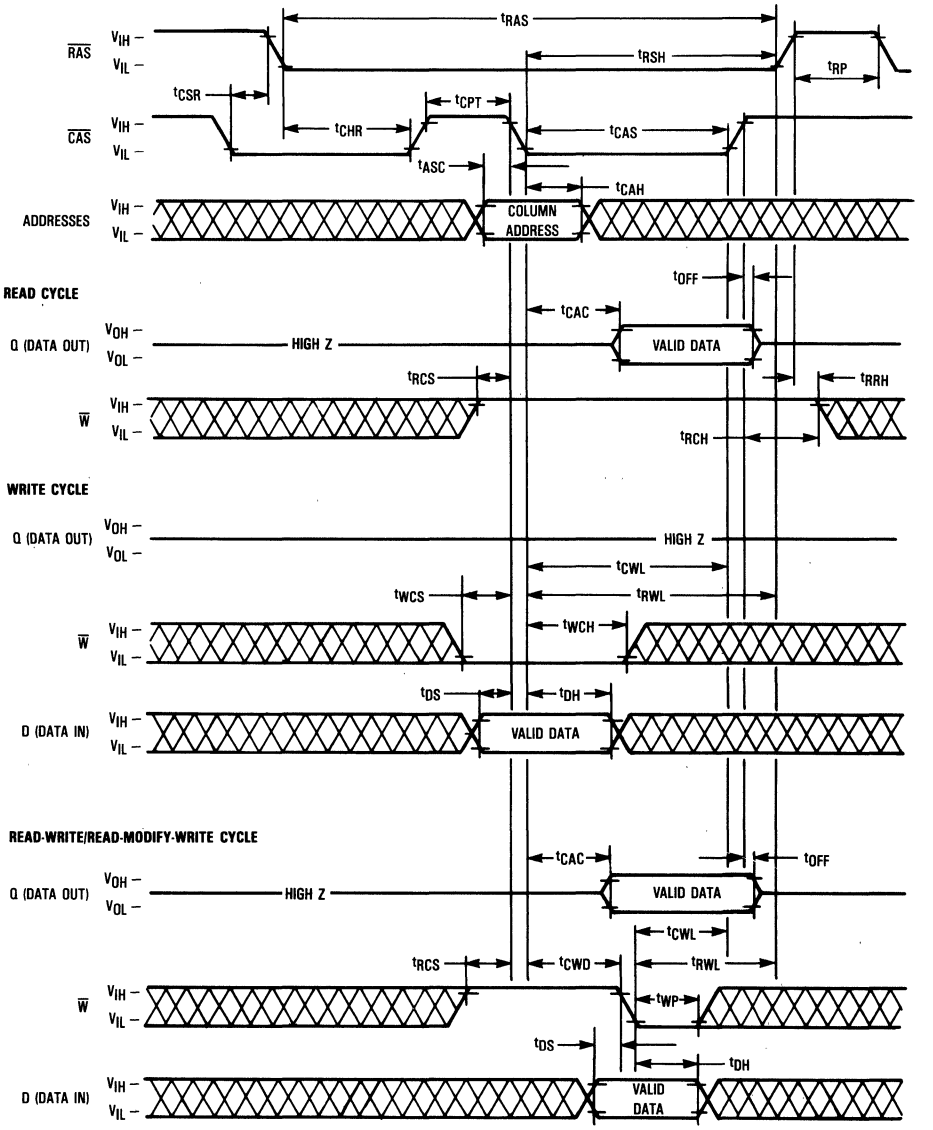
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called nibble mode, allows the user to access 4 bits serially. (See **NIBBLE MODE** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important

role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

NIBBLE MODE

Nibble mode allows high speed serial read, write, or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA8, RA8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA8 and CA8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access.

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM6257B can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

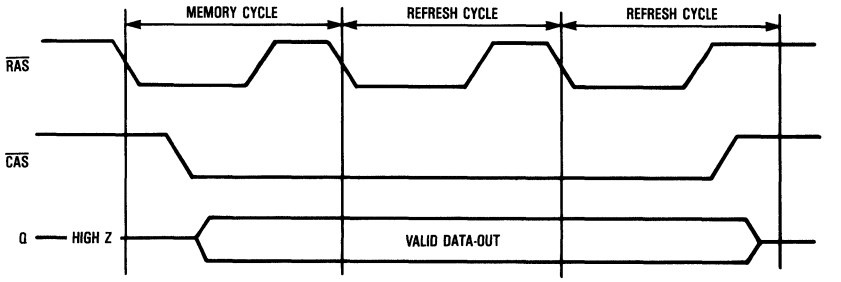
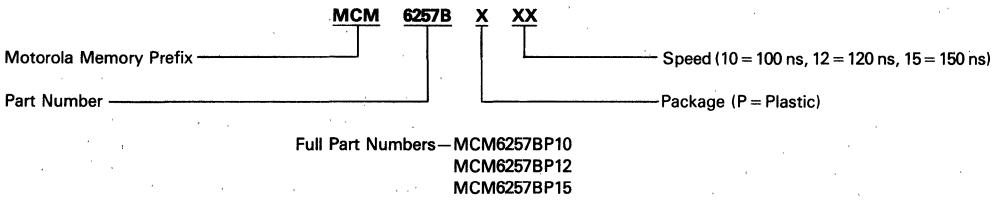


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6257BP10
MCM6257BP12
MCM6257BP15

MCM41464A

2

Advance Information

64K x 4 Dynamic RAM

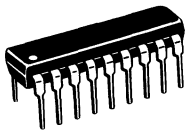
The MCM41464A is a 262,144 bit, high-speed, dynamic random access memory. Organized as 65,536 words of 4 bits, and fabricated using N-channel silicon-gate MOS technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row and column address inputs, the MCM41464A requires only eight address lines and permits packaging in standard 18-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM41464A incorporates a one transistor cell design and dynamic storage techniques.

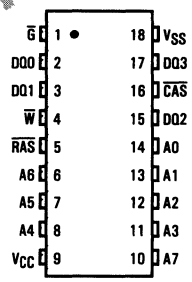
The MCM41464A features "page mode" which allows random column accesses of the 256 bits within the selected row.

- Organized as 65,536 Words of 4 Bits
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM41464A-10 = 100 ns
  MCM41464A-12 = 120 ns
  MCM41464A-15 = 150 ns
- Low Power Dissipation: MCM41464A-10 = 440 mW
  MCM41464A-12 = 396 mW Maximum (Active)
  MCM41464A-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode
- Hidden Refresh
- $\overline{RAS}$-Only Refresh Mode
- Page Mode Capability



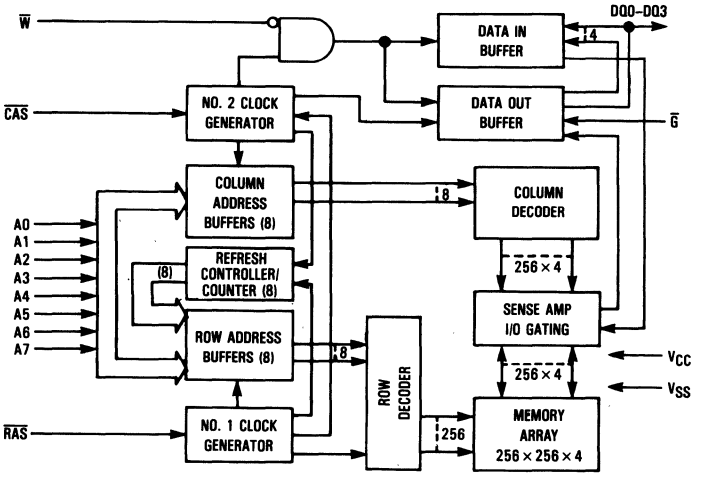
P PACKAGE
PLASTIC
CASE 707

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM41464A-10, t_{RC} = 190 ns		—	80		
MCM41464A-12, t_{RC} = 220 ns		—	72		
MCM41464A-15, t_{RC} = 260 ns		—	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	—	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM41464A-10, t_{RC} = 190 ns		—	70		
MCM41464A-12, t_{RC} = 220 ns		—	62		
MCM41464A-15, t_{RC} = 260 ns		—	55		
V_{CC} Power Supply Current During Page Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2
MCM41464A-10, t_{PC} = 100 ns		—	70		
MCM41464A-12, t_{PC} = 120 ns		—	55		
MCM41464A-15, t_{PC} = 145 ns		—	50		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM41464A-10, t_{RC} = 190 ns		—	70		
MCM41464A-12, t_{RC} = 220 ns		—	62		
MCM41464A-15, t_{RC} = 260 ns		—	55		
Input Leakage Current ($V_{SS} < V_{in} < V_{CC}$)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} < V_{out} < V_{CC}$)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A7, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM41464A-10		MCM41464A-12		MCM41464A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	–	220	–	260	–	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	260	–	300	–	355	–	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	100	–	120	–	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	50	–	60	–	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	35	0	40	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	–	90	–	100	–	ns	–
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	50	10,000	75	10,000	ns	–
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	15	–	15	–	ns	–
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	25	–	35	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	–	85	–	110	–	ns	–
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	–
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	–	15	–	20	–	ns	11
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	30	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	80	–	95	–	120	–	ns	–
Write Command Pulse Width	t_{WLWH}	t_{WP}	30	–	35	–	45	–	ns	–
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	30	–	35	–	45	–	ns	–
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	30	–	35	–	45	–	ns	–
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	30	–	35	–	45	–	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	80	–	95	–	120	–	ns	–
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	–	60	–	75	–	ns	–
Refresh Period	t_{RVRV}	t_{RFSH}	–	4	–	4	–	4	ms	–

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

2

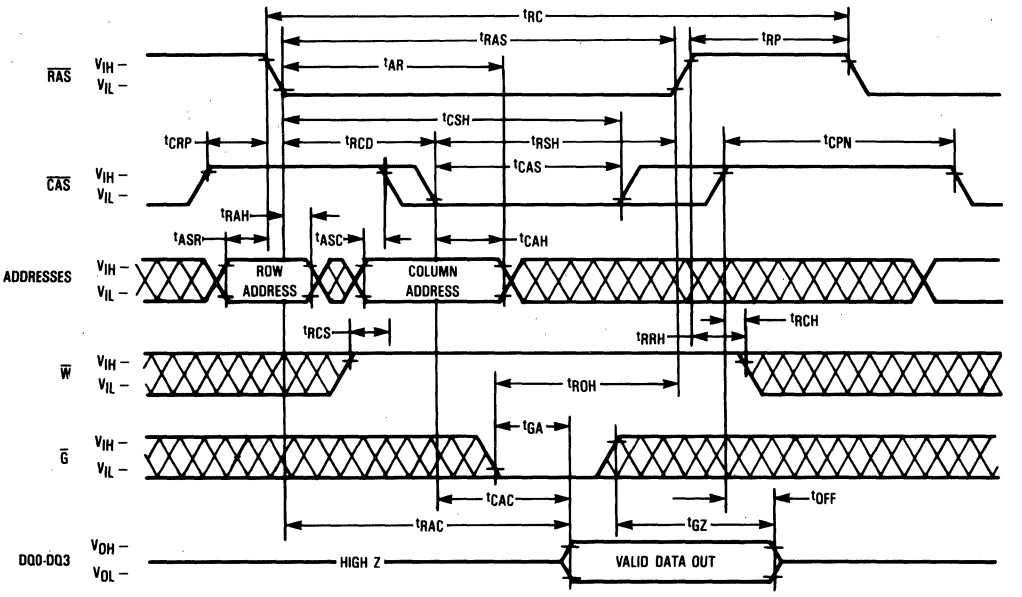
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM41464A-10		MCM41464A-12		MCM41464A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	85	–	100	–	120	–	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	135	–	160	–	195	–	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	20	–	20	–	25	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	40	–	50	–	60	–	ns	–
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	100	–	120	–	145	–	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	25	–	30	–	40	ns	–
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	25	–	30	–	40	–	ns	–
Output Buffer Turn-off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	25	0	30	0	40	ns	–
$\overline{G}$ Command Hold Time	t_{WLGH}	t_{GH}	25	–	30	–	40	–	ns	–
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	–
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	20	–	50	–	60	–	ns	–

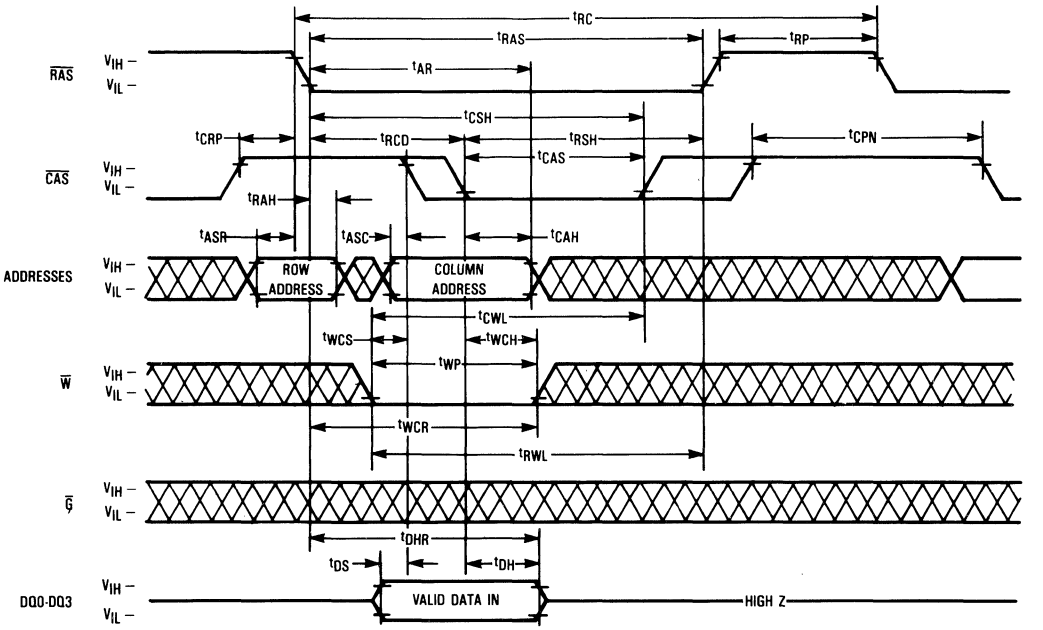
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

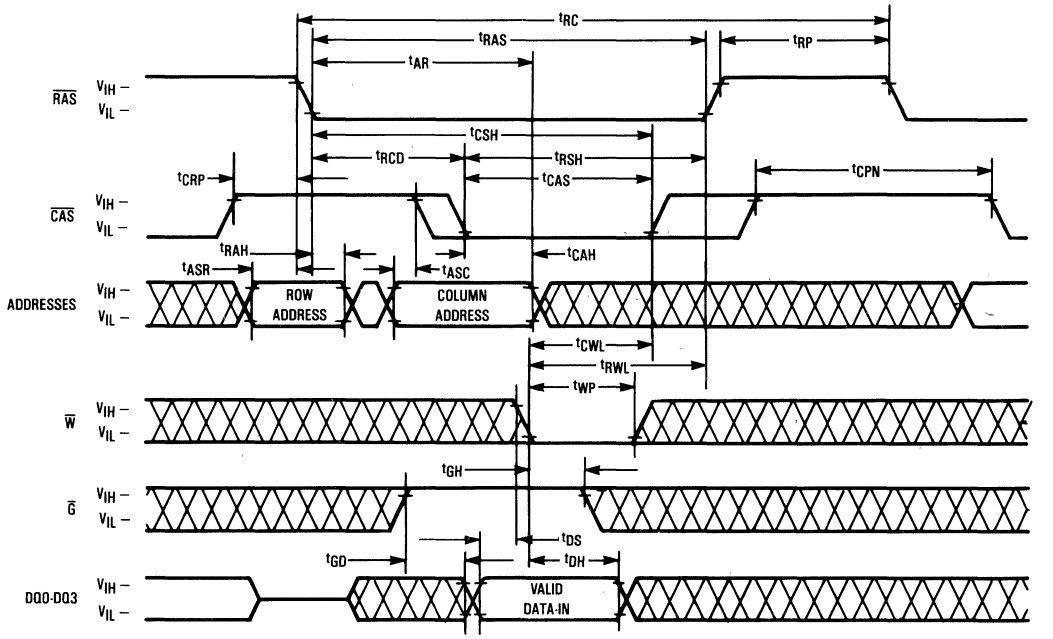
READ CYCLE



WRITE CYCLE (EARLY WRITE)

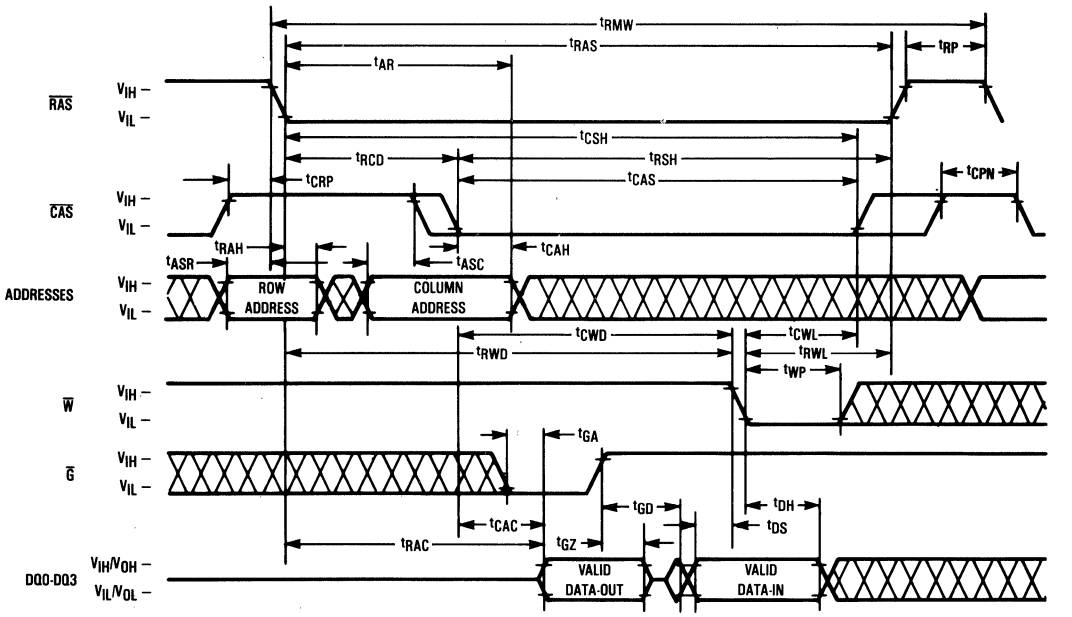


WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)

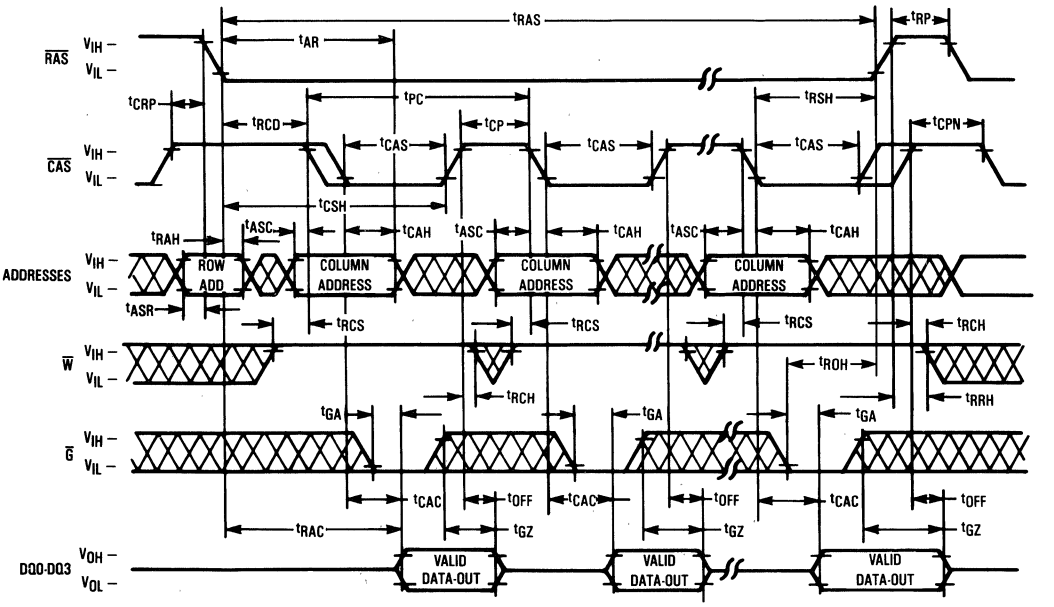


2

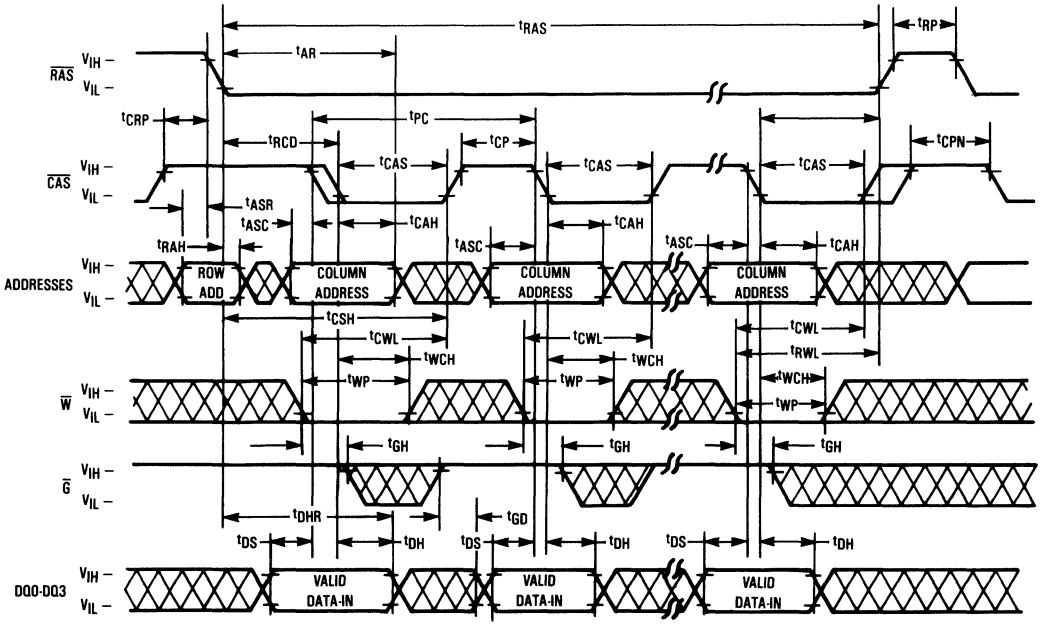
READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE

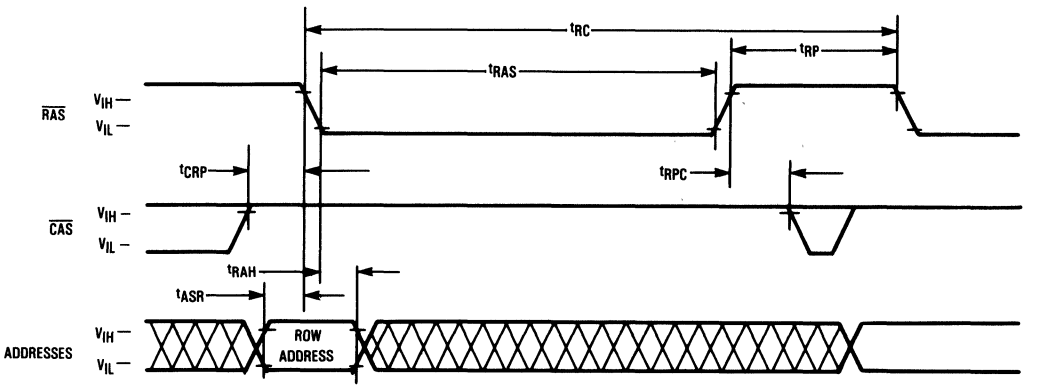


PAGE MODE WRITE CYCLE



RAS ONLY REFRESH CYCLE

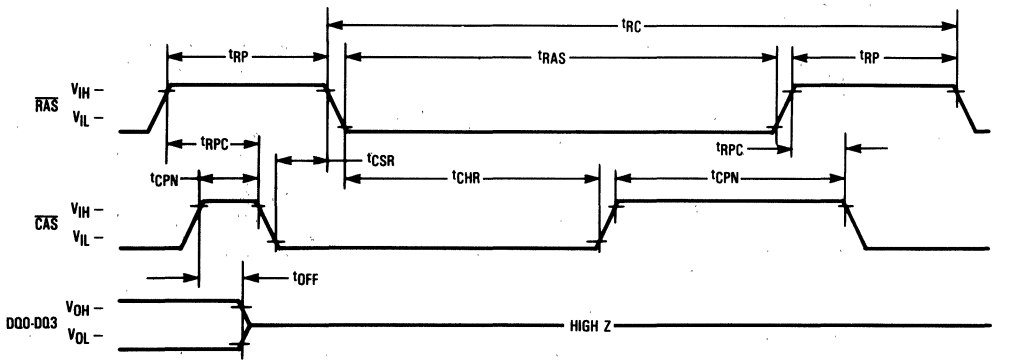
(W and G are Don't Care)



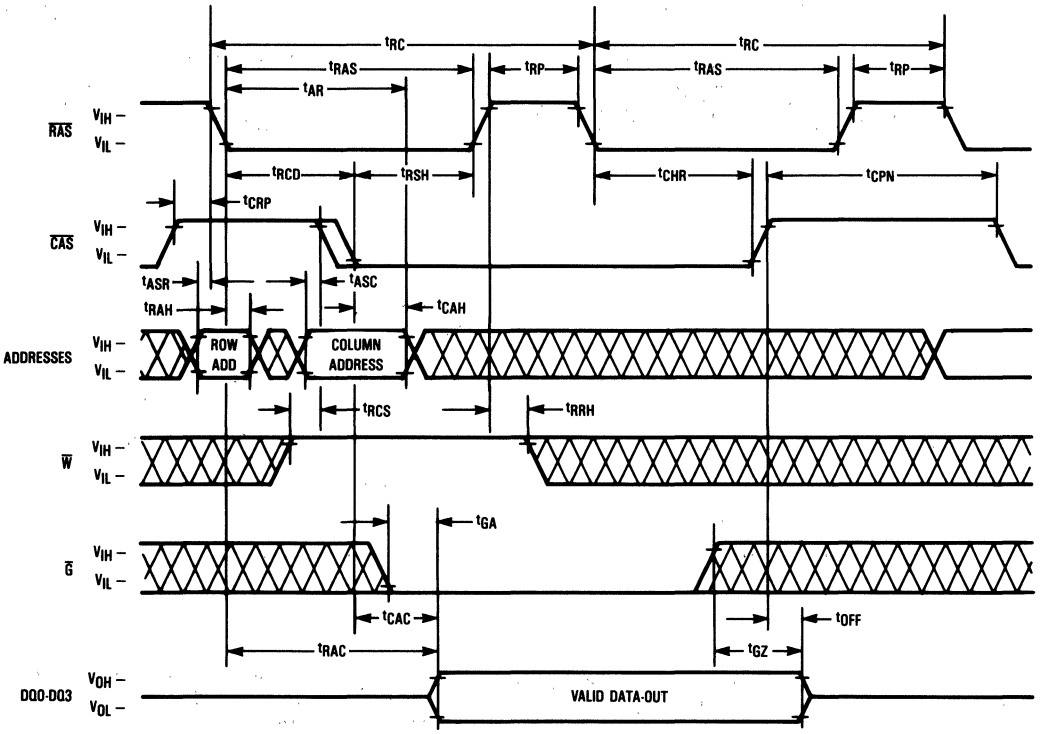
2

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

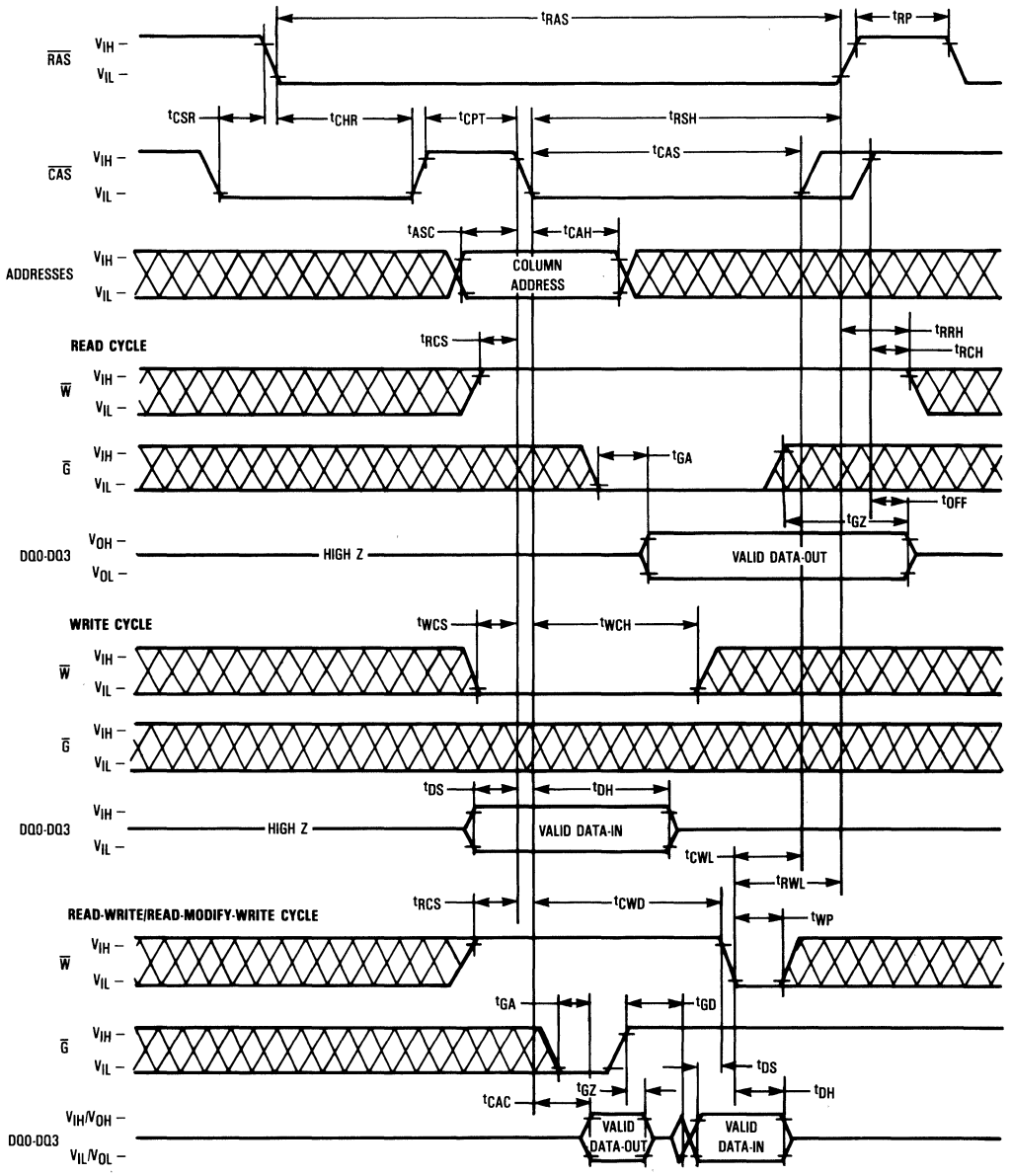
($\overline{W}$, $\overline{G}$, and A0-A7 are Don't Care)



HIDDEN REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of 16 address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CAS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called page mode allows the user to column access the 256 bits within a selected row. The refresh mode and page mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CAS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 256K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MCM41464A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM41464A is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM41464A can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

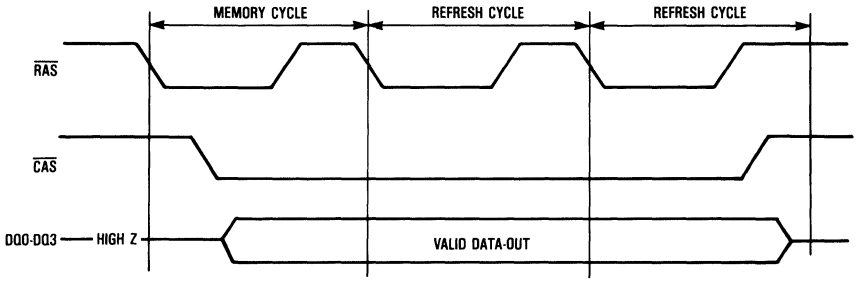
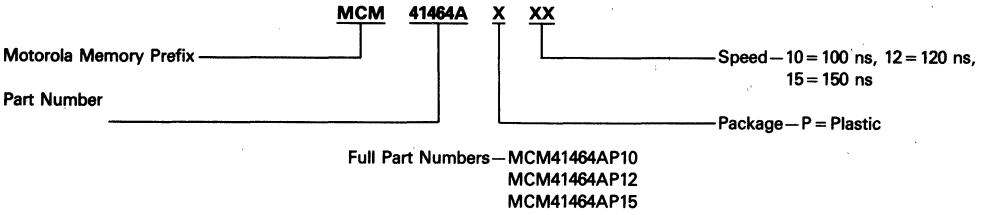


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM41464AP10
MCM41464AP12
MCM41464AP15

2

MCM511000A
MCM51L1000A

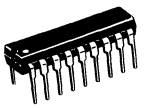
Advance Information

1M x 1 CMOS Dynamic RAM

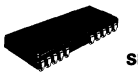
The MCM511000A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM511000A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

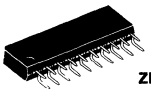
- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- Test Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: MCM511000A = 8 ms
  MCM51L1000A = 64 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  MCM511000A-70 and MCM51L1000A-70 = 70 ns (Max)
  MCM511000A-80 and MCM51L1000A-80 = 80 ns (Max)
  MCM511000A-10 and MCM51L1000A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM511000A-70 and MCM51L1000A-70 = 440 mW (Max)
  MCM511000A-80 and MCM51L1000A-80 = 385 mW (Max)
  MCM511000A-10 and MCM51L1000A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  MCM511000A and MCM51L1000A = 11 mW (Max, TTL Levels)
  MCM511000A = 5.5 mW (Max, CMOS Levels)
  MCM51L1000A = 1.1 mW (Max, CMOS Levels)



P PACKAGE
PLASTIC
CASE 707A



J PACKAGE
PLASTIC
SMALL OUTLINE
CASE 822

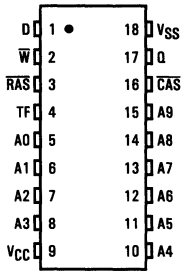


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

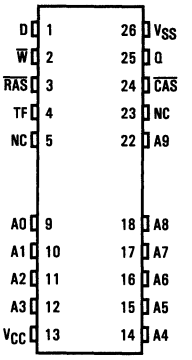
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

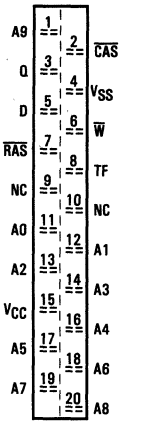
DUAL-IN-LINE



SMALL OUTLINE



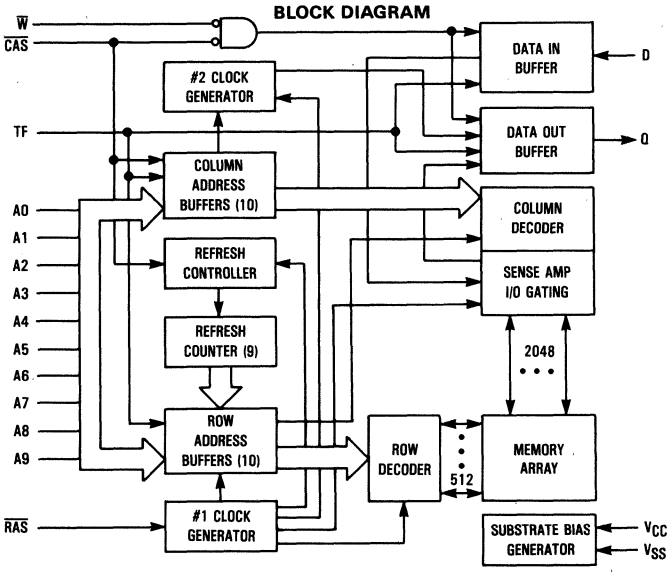
ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	–	10.5	V	1
Test Function Input Low Voltage	$V_{IL\ (TF)}$	−1.0	–	V_{CC} + 1.0	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns		–	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns		–	70		
MCM511000A-10 and MCM51L1000A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns		–	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns		–	70		
MCM511000A-10 and MCM51L1000A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{PC} = 40 ns		–	60		
MCM511000A-80 and MCM51L1000A-80, t_{PC} = 45 ns		–	50		
MCM511000A-10 and MCM51L1000A-10, t_{PC} = 55 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V) MCM511000A	I_{CC5}	–	1.0	mA	
MCM51L1000A		–	200	μA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511000A-70 and MCM51L1000A-70, t_{RC} = 130 ns		–	80		
MCM511000A-80 and MCM51L1000A-80, t_{RC} = 150 ns		–	70		
MCM511000A-10 and MCM51L1000A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current, Battery Backup Mode—MCM51L1000A only (t_{RC} = 125 μs; t_{RAS} = 1 μs min; $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0-A9, $\overline{W}$, D = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	–	200	μA	
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		MCM511000A-10 MCM51L1000A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	175	–	210	–	ns	6
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	65	–	70	–	85	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

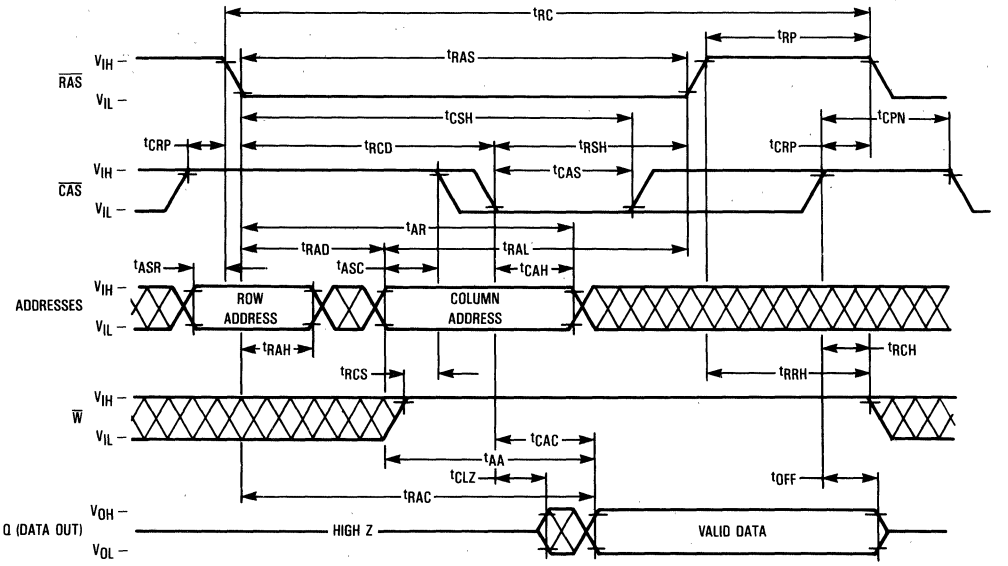
Parameter	Symbol		MCM511000A-70 MCM51L1000A-70		MCM511000A-80 MCM51L1000A-80		MCM511000A-10 MCM51L1000A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM511000A MCM51L1000A	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

NOTES:

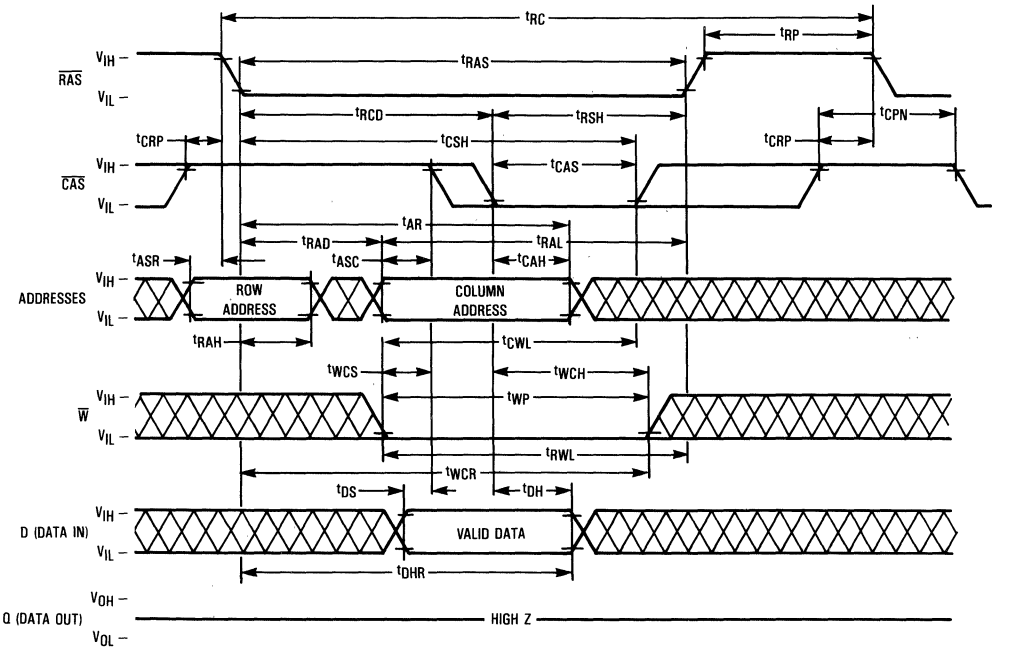
14. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

2

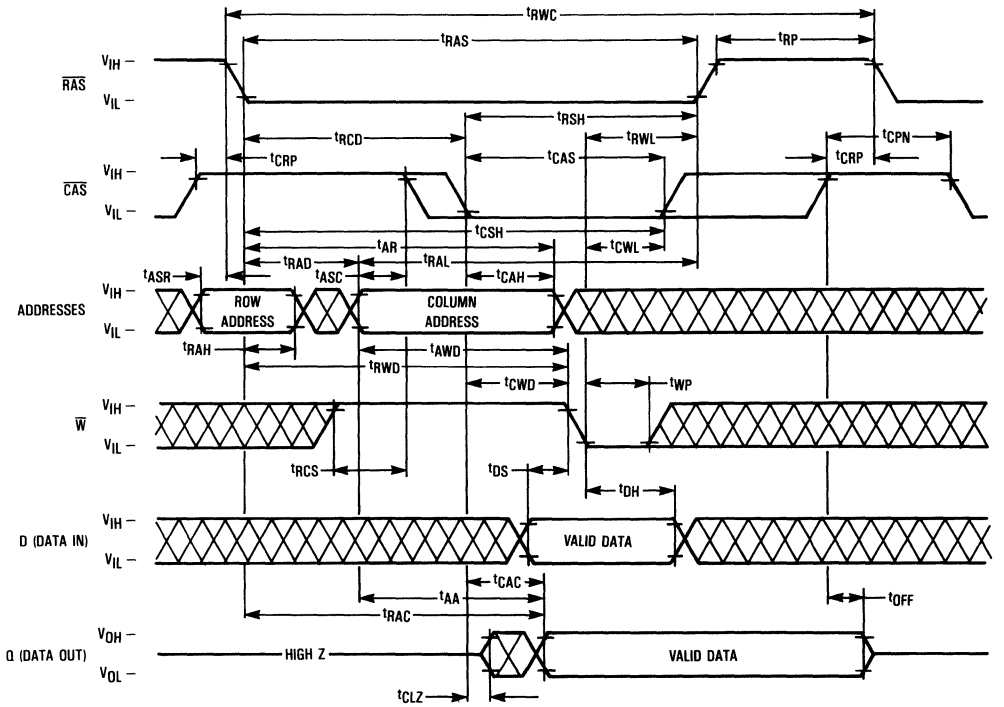
READ CYCLE



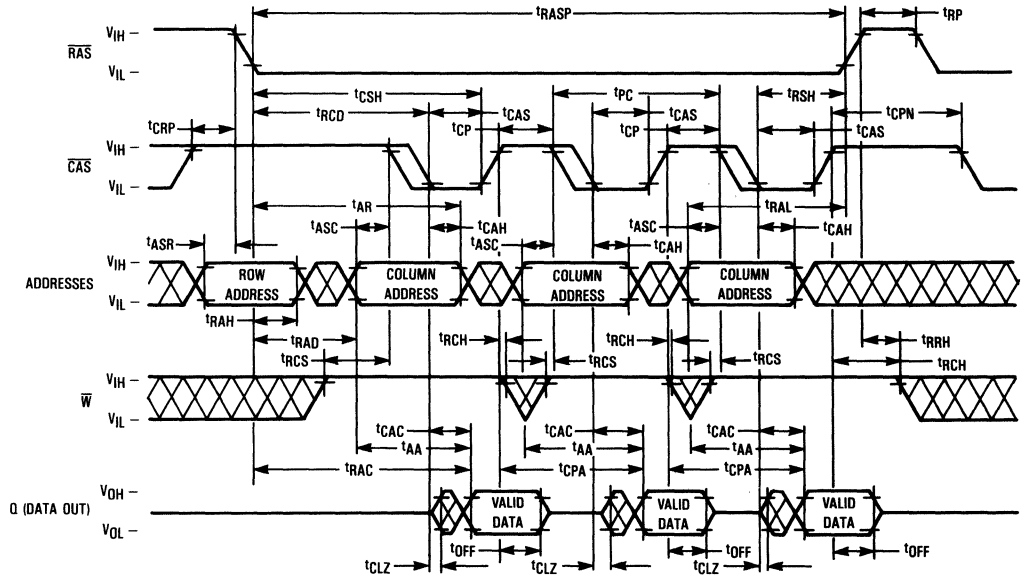
EARLY WRITE CYCLE



READ-WRITE CYCLE

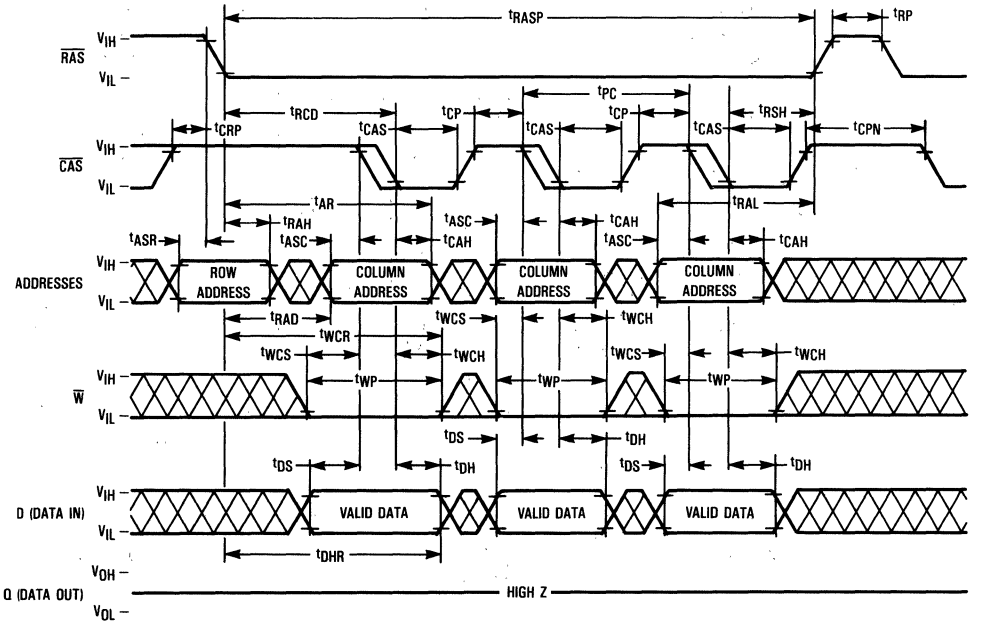


FAST PAGE MODE READ CYCLE

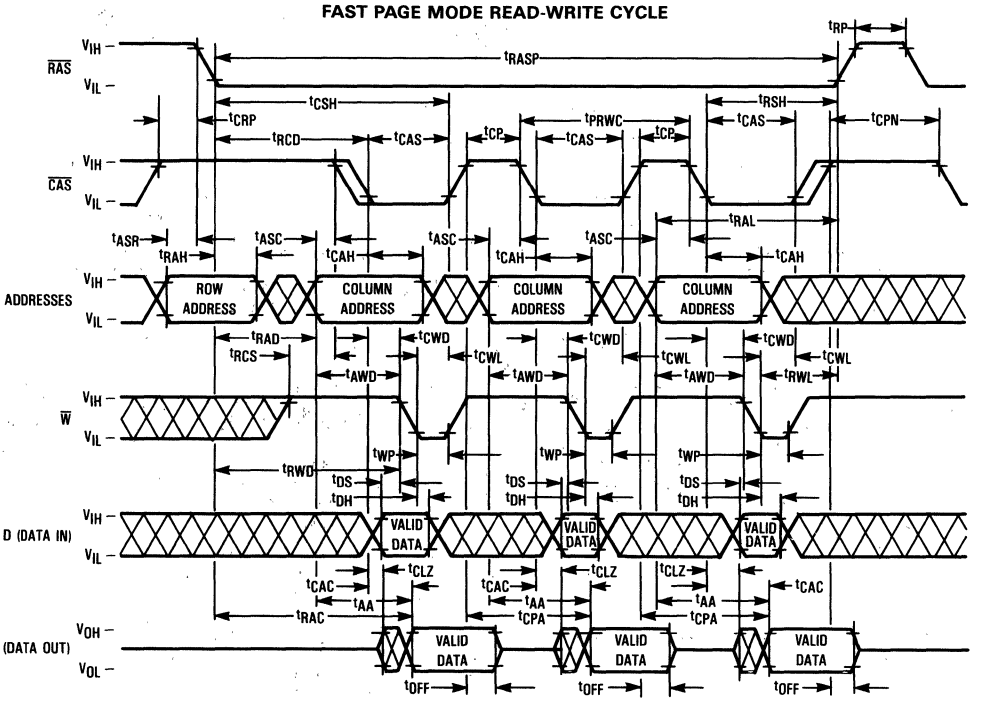


2

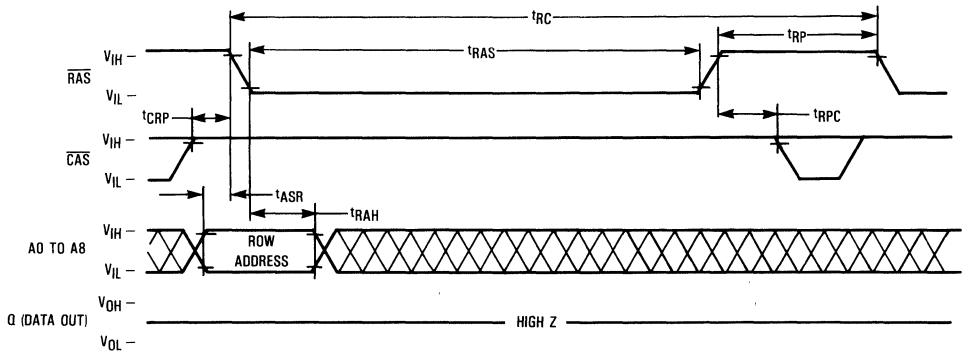
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



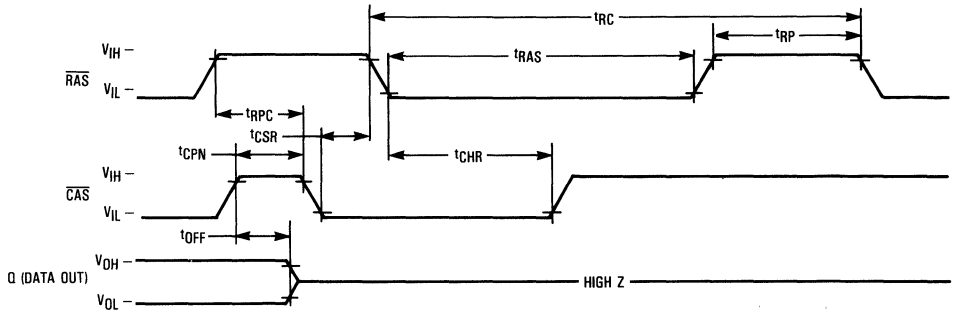
FAST PAGE MODE READ-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)

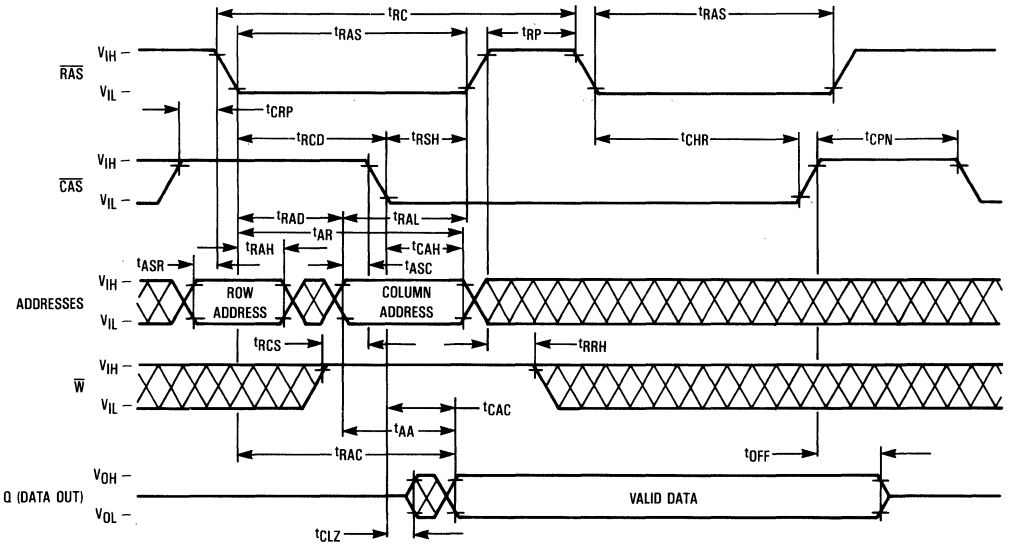


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)

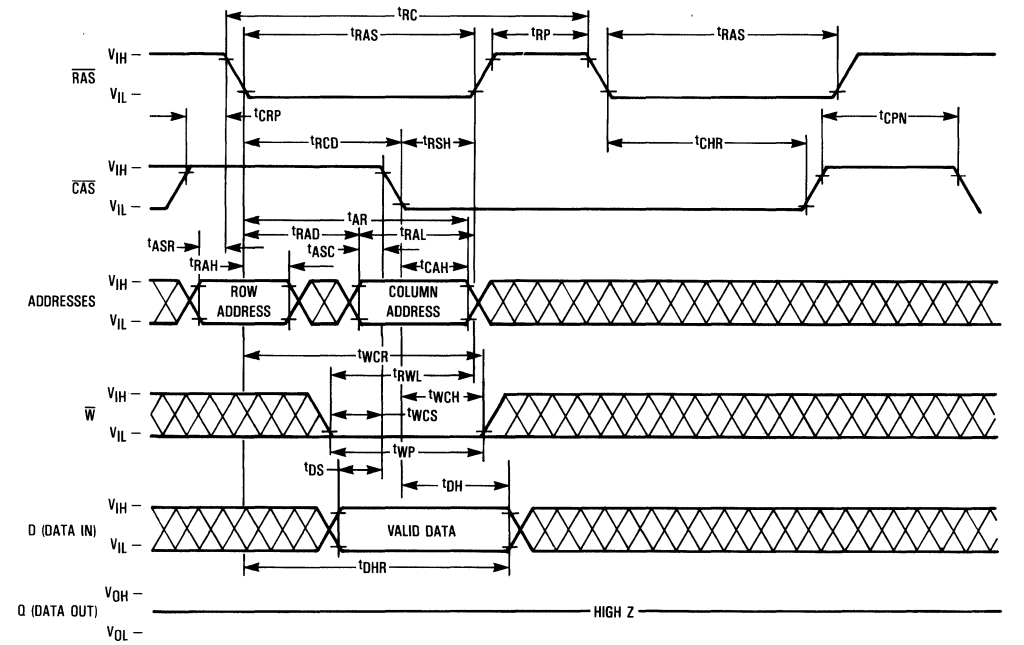


2

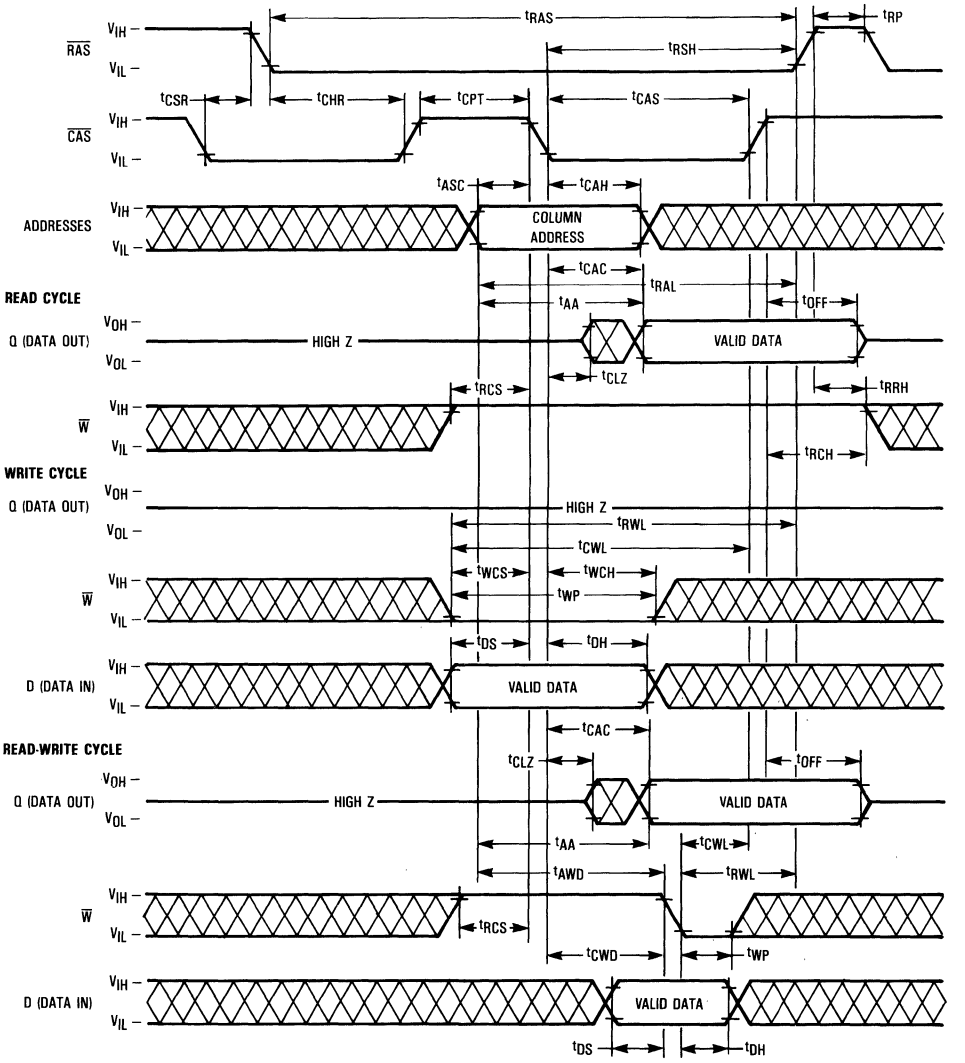
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 1,048,576 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access all 1024 bits within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL}+t_{RP}+2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out

occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at all 1024 column locations on a selected row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds for MCM511000A (64 milliseconds for MCM51L1000A). This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds for MCM511000A (64 milliseconds for MCM51L1000A), (i.e., at least one row every 15.6 microseconds for MCM511000A, or 124.8 microseconds for MCM51L1000A). A normal read or write operation to the RAM will also refresh all the bits (2048) associated with the particular row(s) decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds for MCM511000A (64 milliseconds for MCM51L1000A). The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with a read-write operation. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of 8 **$\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, read "0" out and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read "1"s (normal read mode), which were written at step 2.
4. Using the same column as in step 2, read "1" out and write "0" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s (normal read mode), which were written at step 4.
6. Repeat steps 1 to 5 using complement data.

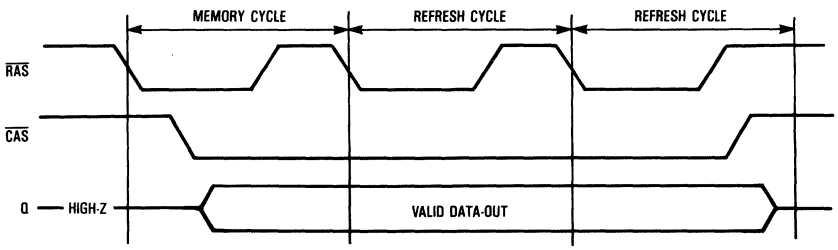


Figure 1. Hidden Refresh Cycle

2

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0-A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0-B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

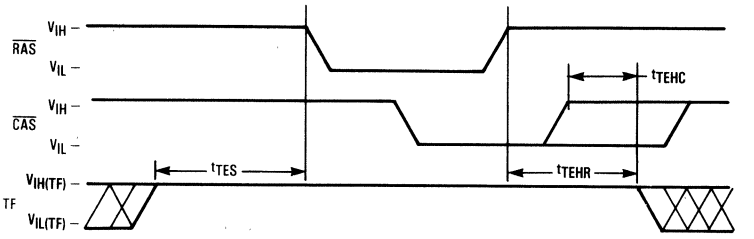
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

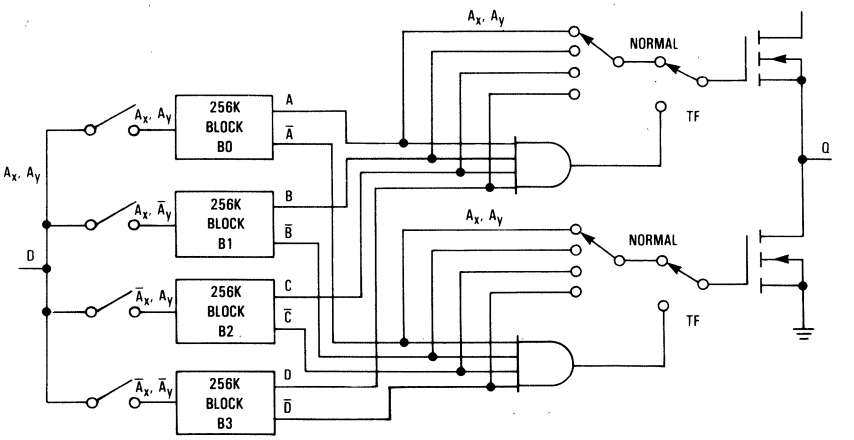
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
–	Any Other				High-Z

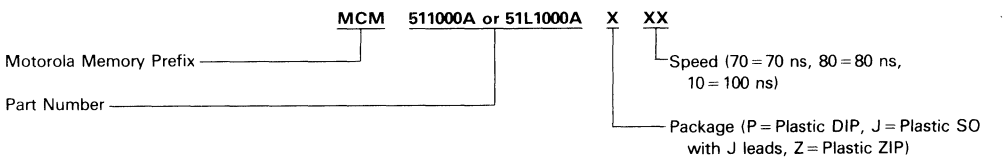
TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)



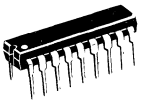
Full Part Numbers—	MCM511000AP70	MCM511000AJ70	MCM511000AZ70
	MCM511000AP80	MCM511000AJ80	MCM511000AZ80
	MCM511000AP10	MCM511000AJ10	MCM511000AZ10
	MCM51L1000AP70	MCM51L1000AJ70	MCM51L1000AZ70
	MCM51L1000AP80	MCM51L1000AJ80	MCM51L1000AZ80
	MCM51L1000AP10	MCM51L1000AJ10	MCM51L1000AZ10

2

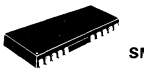
MCM511001A

Advance Information

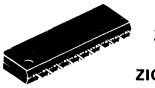
1M x 1 CMOS Dynamic RAM



P PACKAGE
PLASTIC
CASE 707A



J PACKAGE
PLASTIC
SMALL OUTLINE
CASE 822



Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

The MCM511001A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

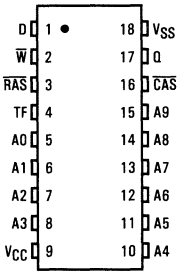
The MCM511001A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Nibble Mode Capability
- Test Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511001A-70 = 70 ns (Maximum)
  MCM511001A-80 = 80 ns (Maximum)
  MCM511001A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511001A-70 = 440 mW (Maximum)
  MCM511001A-80 = 385 mW (Maximum)
  MCM511001A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

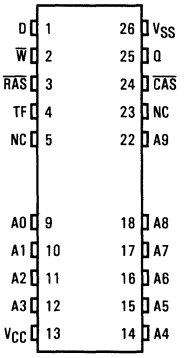
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

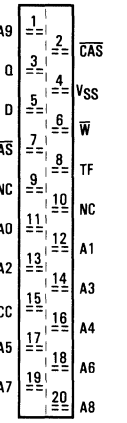
DUAL-IN-LINE



SMALL OUTLINE

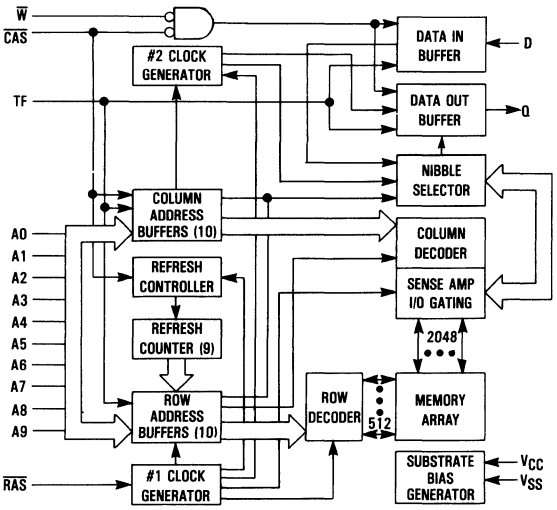


ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC}+4.5	–	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM511001A-70, t_{NC} = 35 ns		–	60		
MCM511001A-80, t_{NC} = 35 ns		–	50		
MCM511001A-10, t_{NC} = 40 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	175	–	210	–	ns	6
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	35	–	35	–	40	–	ns	
Nibble Mode Read-Write Cycle Time	t_{CEHCEH}	t_{NRMW}	55	–	55	–	65	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	–	15	–	15	–	20	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

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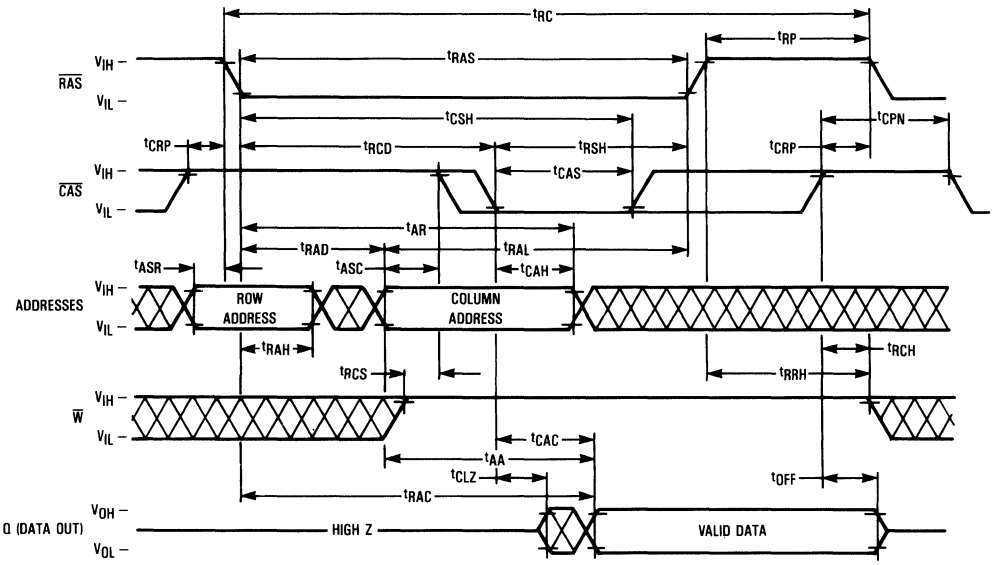
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	15	–	15	–	20	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	–	10	–	10	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NRSH}	15	–	15	–	20	–	ns	
Nibble Mode $\overline{CAS}$ to Write Delay Time	t_{CELWL}	t_{NCWD}	15	–	15	–	20	–	ns	
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{NRWL}	15	–	15	–	20	–	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	15	–	15	–	20	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

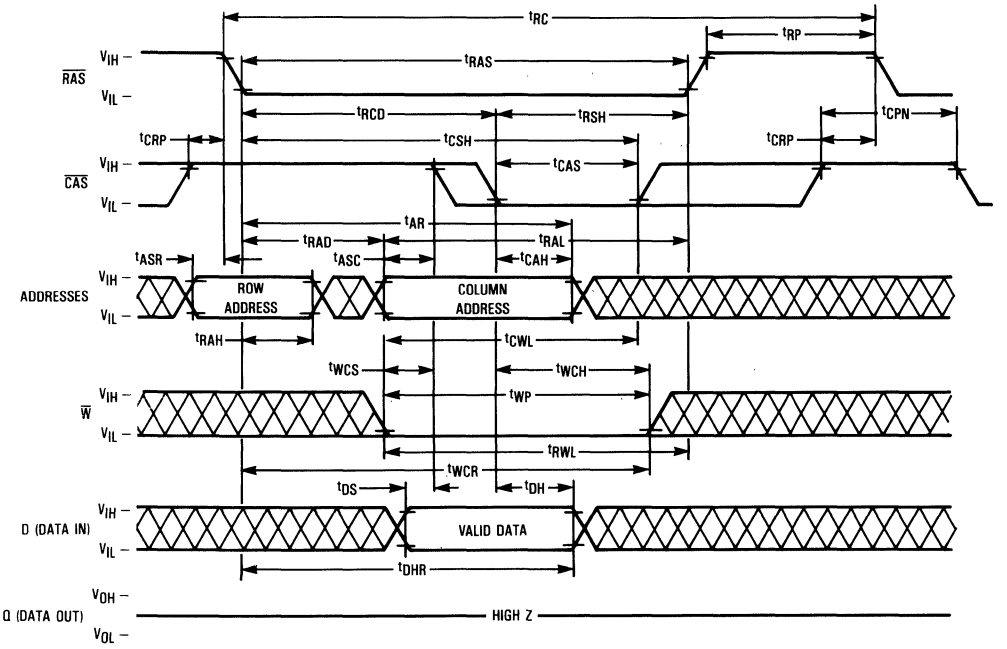
NOTES:

14. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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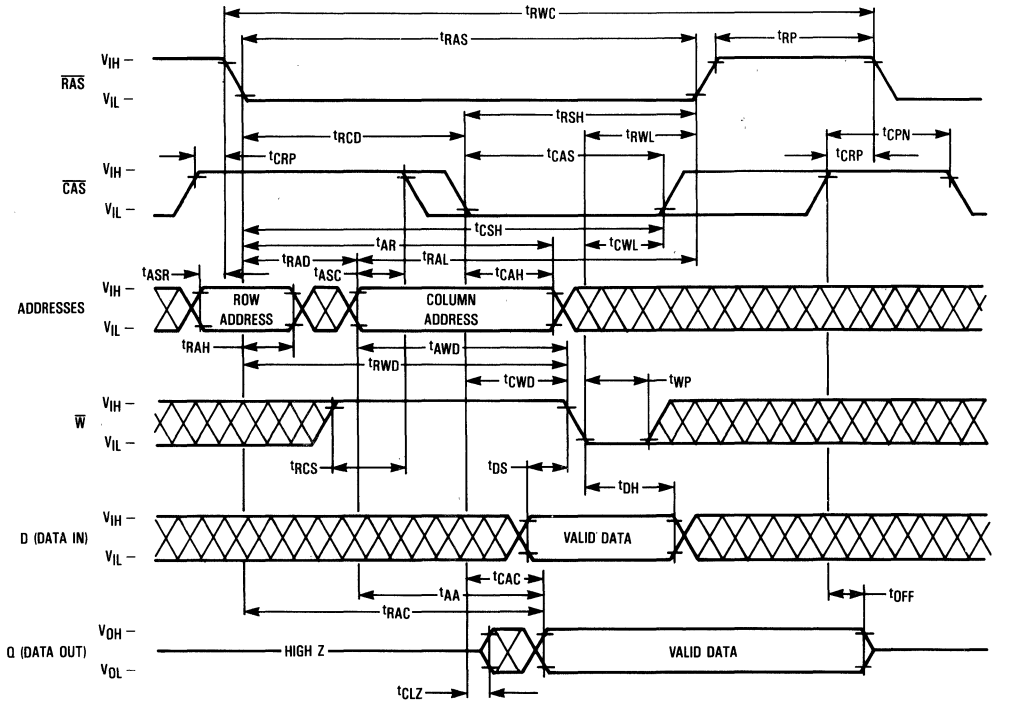
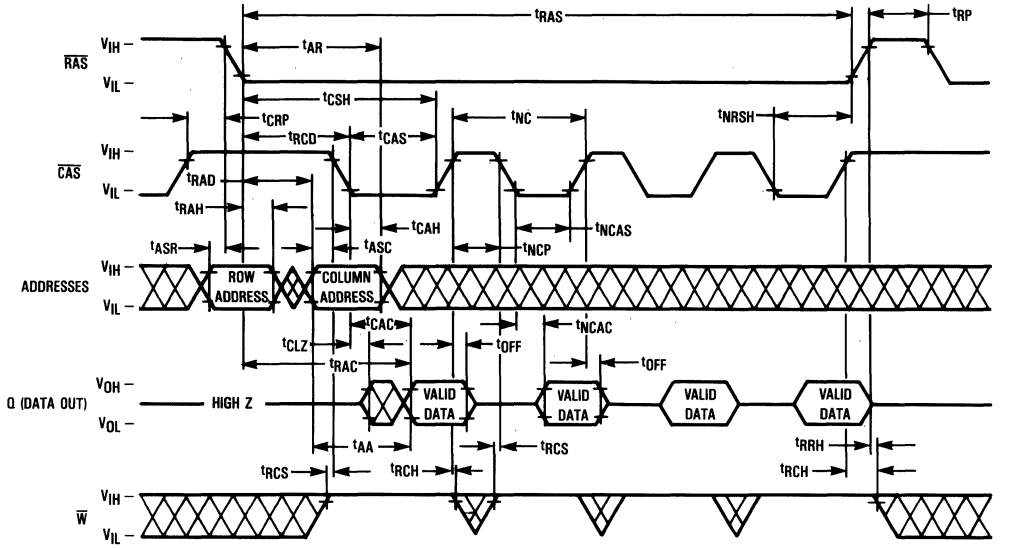
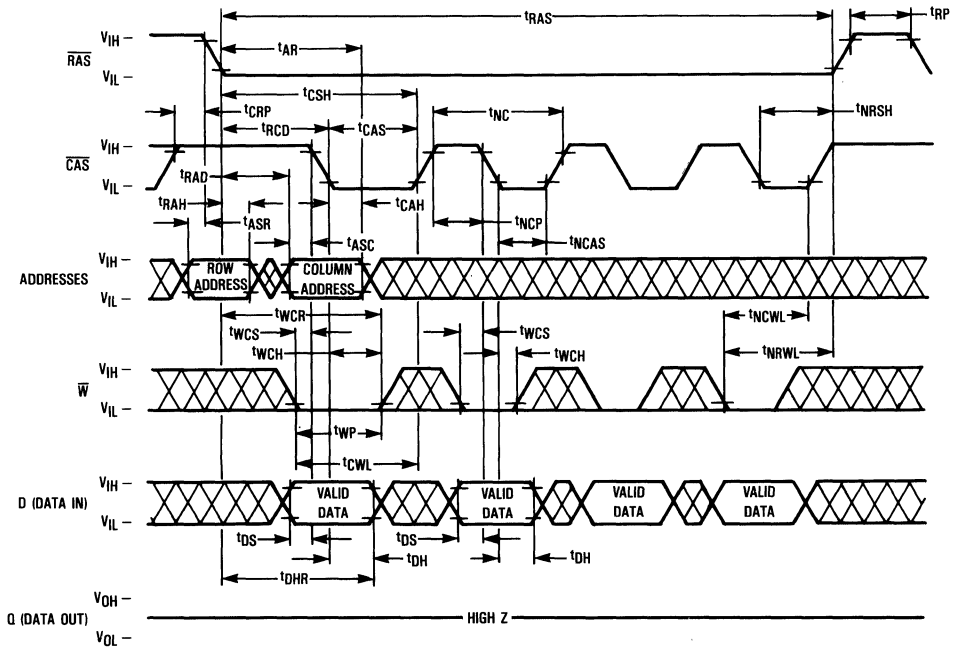
READ-WRITE CYCLE



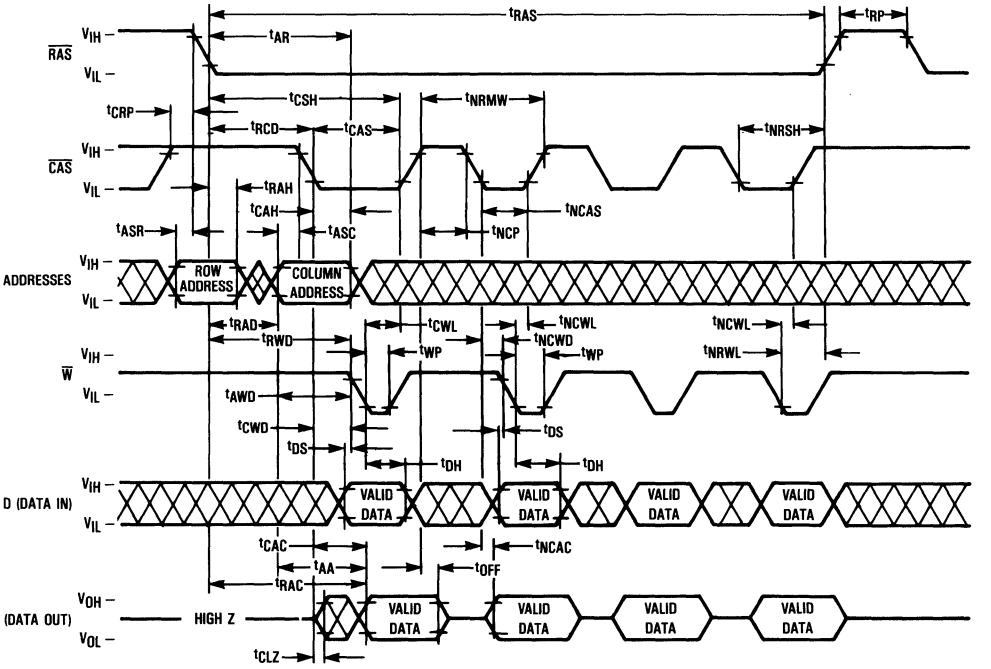
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-WRITE CYCLE



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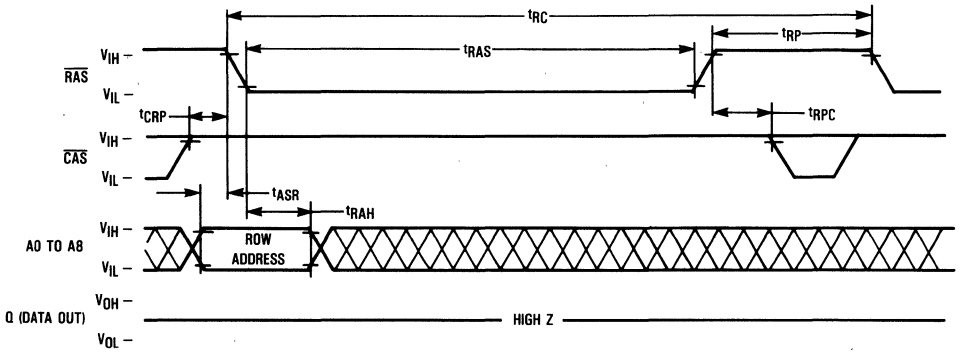
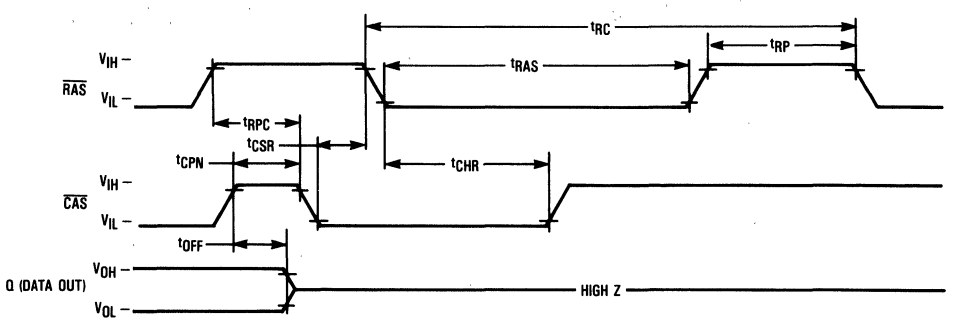
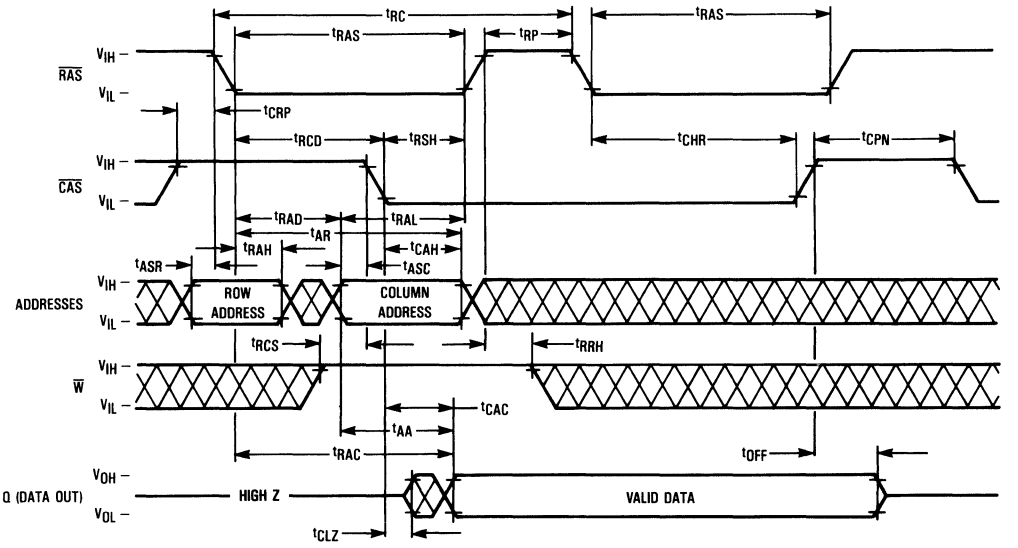
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)



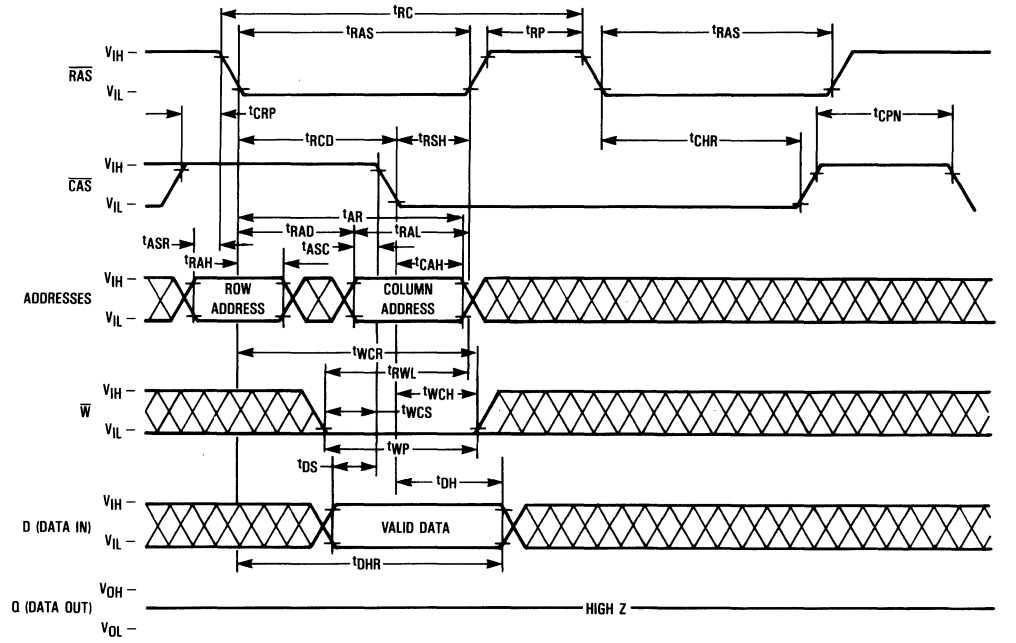
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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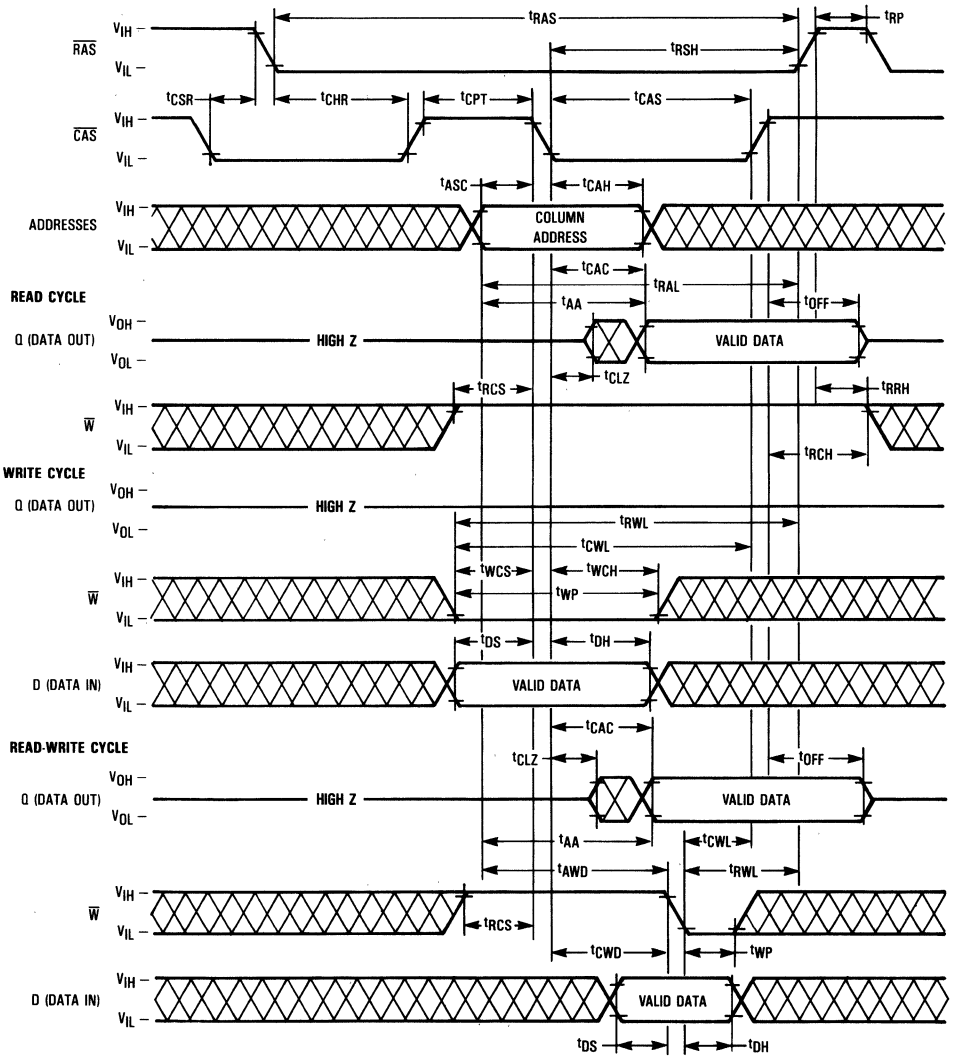
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 1,048,576 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called nibble mode, allows the user to access 4 bits serially. (See **NIBBLE MODE** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important

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role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

NIBBLE MODE

Nibble mode allows high speed serial read, write, or read-modify-write access to 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row addresses and the 9 column addresses. The 2 bits of addresses (CA9, RA9) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA9 and CA9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access.

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits (2048) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with a read-write operation. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, read "0" out and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read "1"s (normal read mode), which were written at step 2.
4. Using the same column as in step 2, read "1" out and write "0" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s (normal read mode), which were written at step 4.
6. Repeat steps 1 to 5 using complement data.

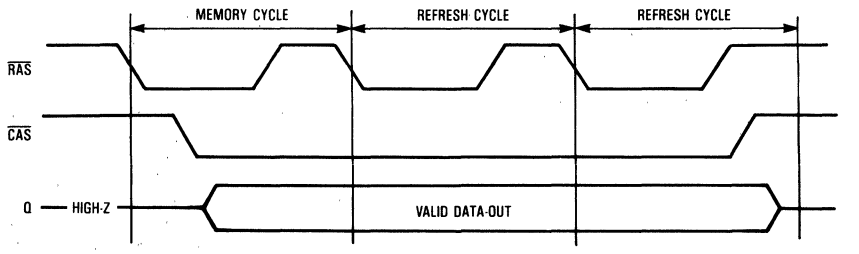


Figure 1. Hidden Refresh Cycle

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0-A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0-B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle except nibble mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

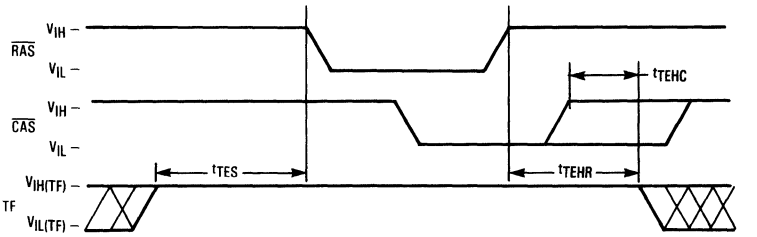
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

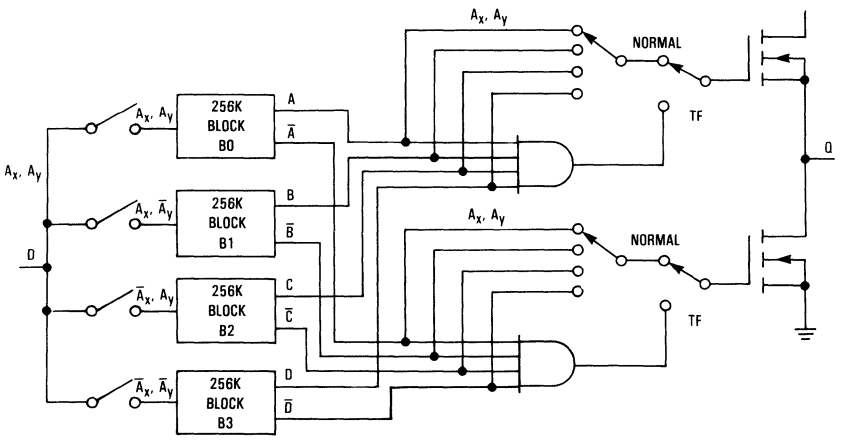
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

TEST MODE CYCLE

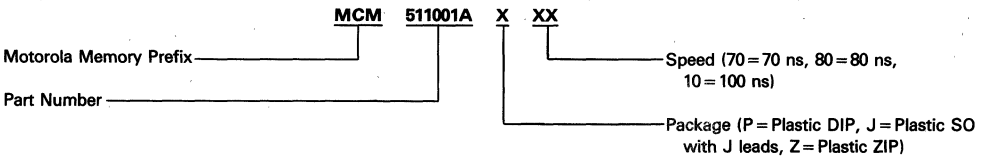


TEST FUNCTION BLOCK DIAGRAM



2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—			
	MCM511001AP70	MCM511001AJ70	MCM511001AZ70
	MCM511001AP80	MCM511001AJ80	MCM511001AZ80
	MCM511001AP10	MCM511001AJ10	MCM511001AZ10

MCM511002A

2

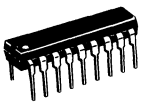
Advance Information

1M x 1 CMOS Dynamic RAM

The MCM511002A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{RAS}$ and $\overline{CS}$ are held low, similar to static RAM operation.

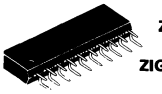
The MCM511002A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Early-Write Common I/O Capability
- Static Column Mode Capability
- Test Mode Capability
- $\overline{TTL}$-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511002A-70 = 70 ns (Maximum)
  MCM511002A-80 = 80 ns (Maximum)
  MCM511002A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511002A-70 = 440 mW (Maximum)
  MCM511002A-80 = 385 mW (Maximum)
  MCM511002A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)



P PACKAGE
PLASTIC
CASE 707A

J PACKAGE
PLASTIC
SMALL OUTLINE
CASE 822

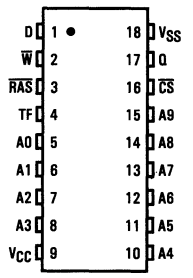


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

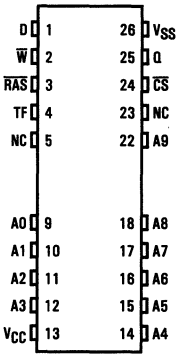
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

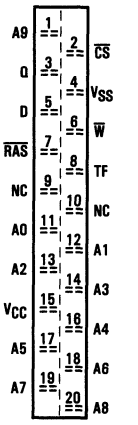
DUAL-IN-LINE



SMALL OUTLINE



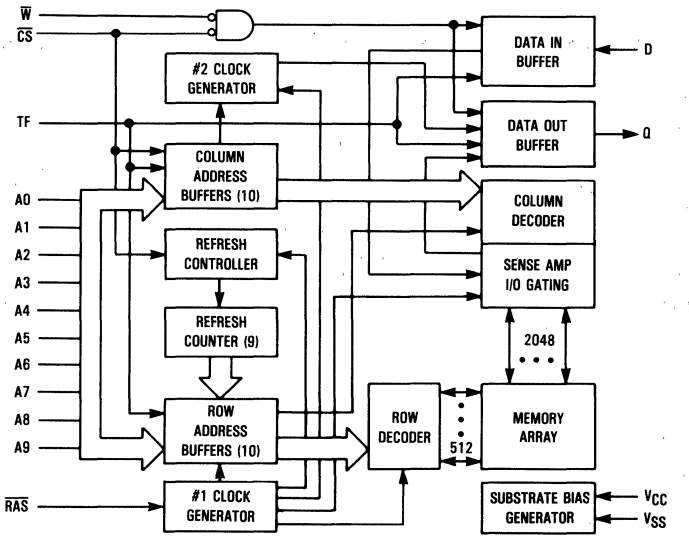
ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	–	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511002A-70, t_{RC} = 130 ns		–	80		
MCM511002A-80, t_{RC} = 150 ns		–	70		
MCM511002A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS}$ = V_{IH})	I_{CC3}			mA	2
MCM511002A-70, t_{RC} = 130 ns		–	80		
MCM511002A-80, t_{RC} = 150 ns		–	70		
MCM511002A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = $\overline{CS}$ = V_{IL})	I_{CC4}			mA	2
MCM511002A-70, t_{SC} = 40 ns		–	60		
MCM511002A-80, t_{SC} = 45 ns		–	50		
MCM511002A-10, t_{SC} = 50 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2 V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511002A-70, t_{RC} = 130 ns		–	80		
MCM511002A-80, t_{RC} = 150 ns		–	70		
MCM511002A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	155	–	210	–	ns	6
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	–	45	–	50	–	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRWC}	70	–	80	–	100	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Access Time from Last Write	t_{WLQV}	t_{ALW}	–	65	–	75	–	95	ns	7, 11
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	12
Data Out Hold from Address Change	t_{AXQX}	t_{AOH}	5	–	5	–	5	–	ns	
Data Out Enable from Write	t_{WHQV}	t_{OW}	–	20	–	20	–	25	ns	
Data Out Hold from Write	t_{WHQX}	t_{WOH}	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	20	100,000	20	100,000	25	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	13
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	14
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CS}$ Precharge Time (Static Column Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max), and/or $t_{LWAD} \geq t_{LWAD}$ (max).
11. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
12. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

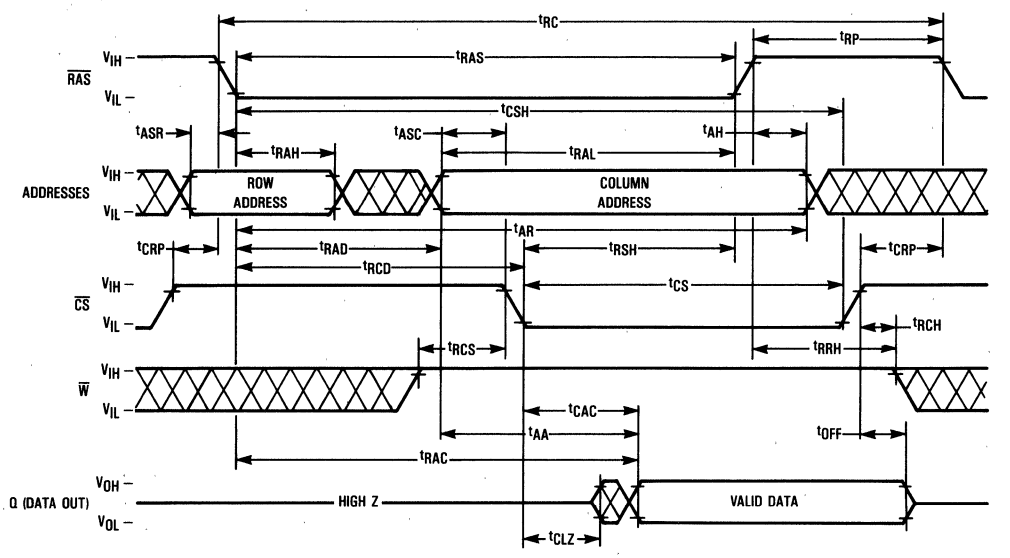
Parameter	Symbol		MCM511002A-70		MCM511002A-80		MCM511002A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	55	–	60	–	75	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	80	–	90	–	115	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$ High	t_{REHAX}	t_{AH}	5	–	5	–	10	–	ns	15
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	30	20	35	25	45	ns	16
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	65	–	75	–	95	–	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	17
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	17
Write Command Hold Time	t_{CELWX}	t_{WCH}	15	–	15	–	20	–	ns	18
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command Inactive Time	t_{WHWL}	t_{WI}	10	–	10	–	10	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	19
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	19
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	18
$\overline{CS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	18
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	18
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

NOTES:

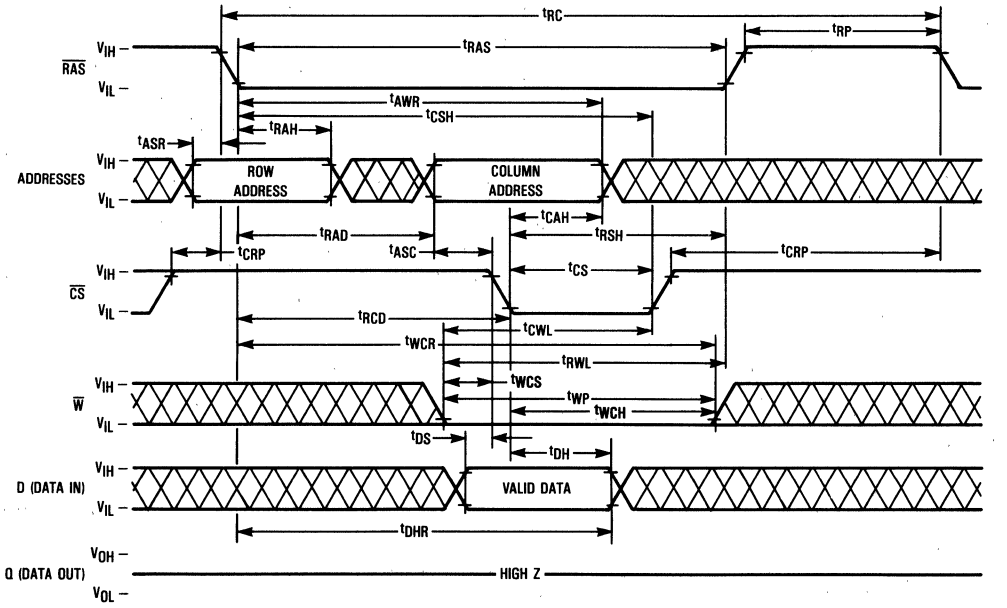
15. t_{AH} is time required to latch column address.
16. Operation within the t_{LWAD} limit ensures that t_{ALW} can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
17. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
19. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.

2

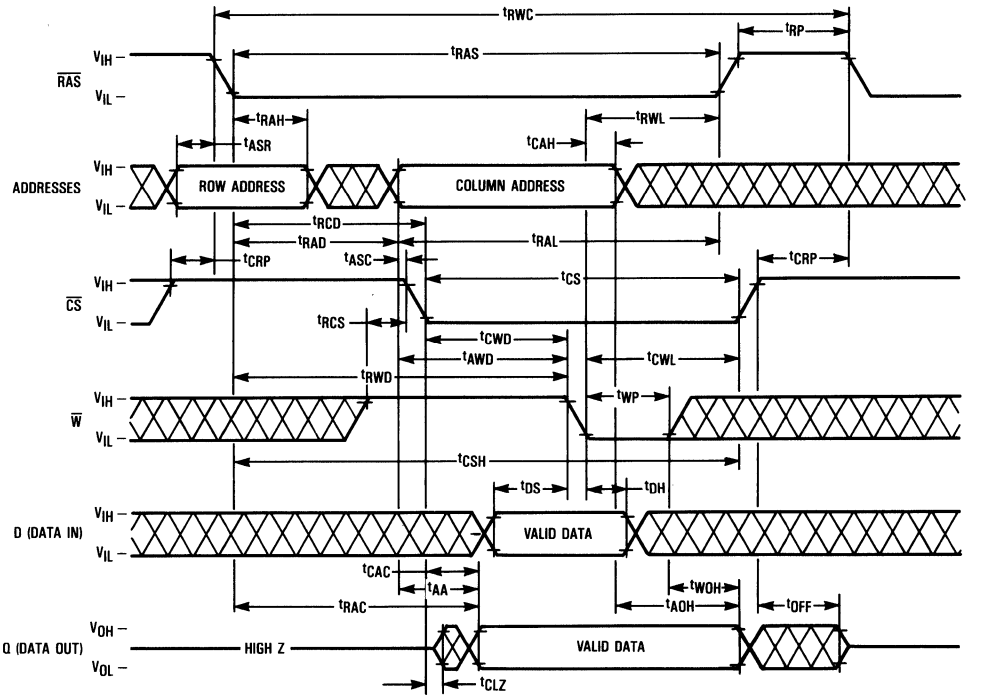
READ CYCLE



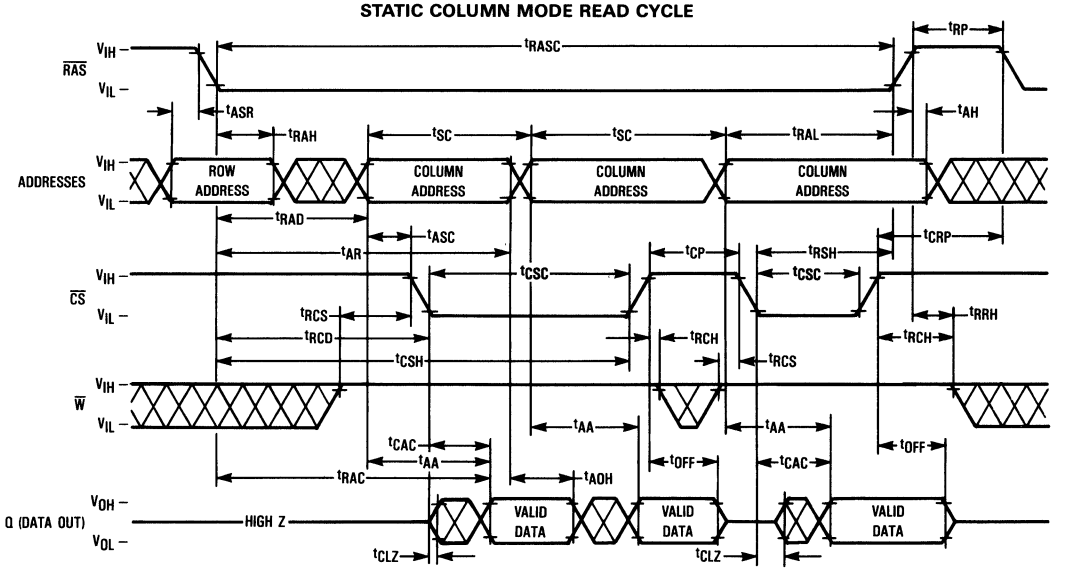
EARLY WRITE CYCLE



READ-WRITE CYCLE

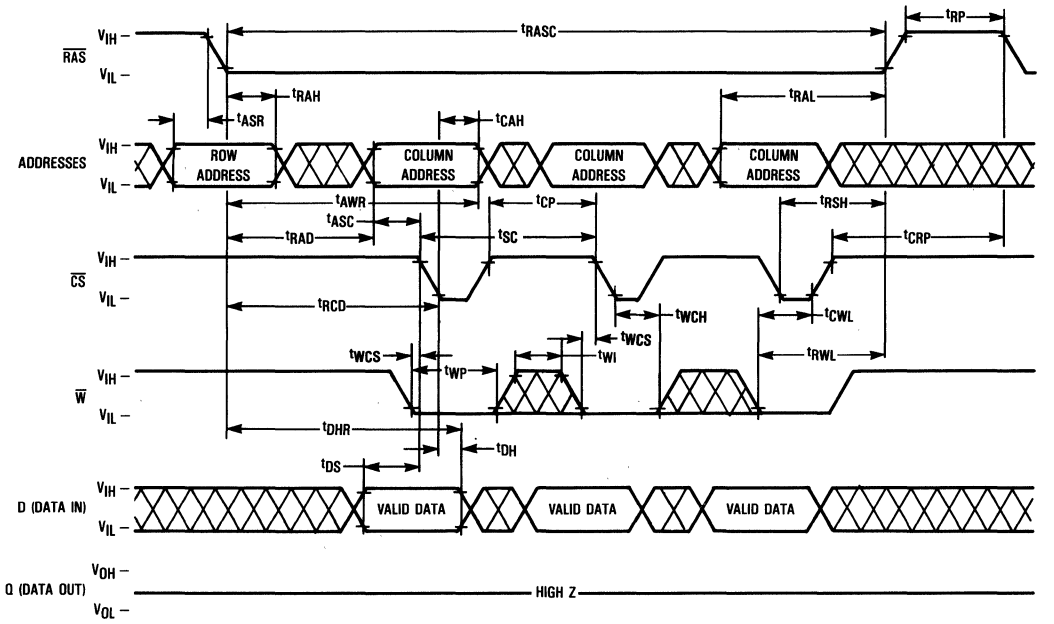


STATIC COLUMN MODE READ CYCLE

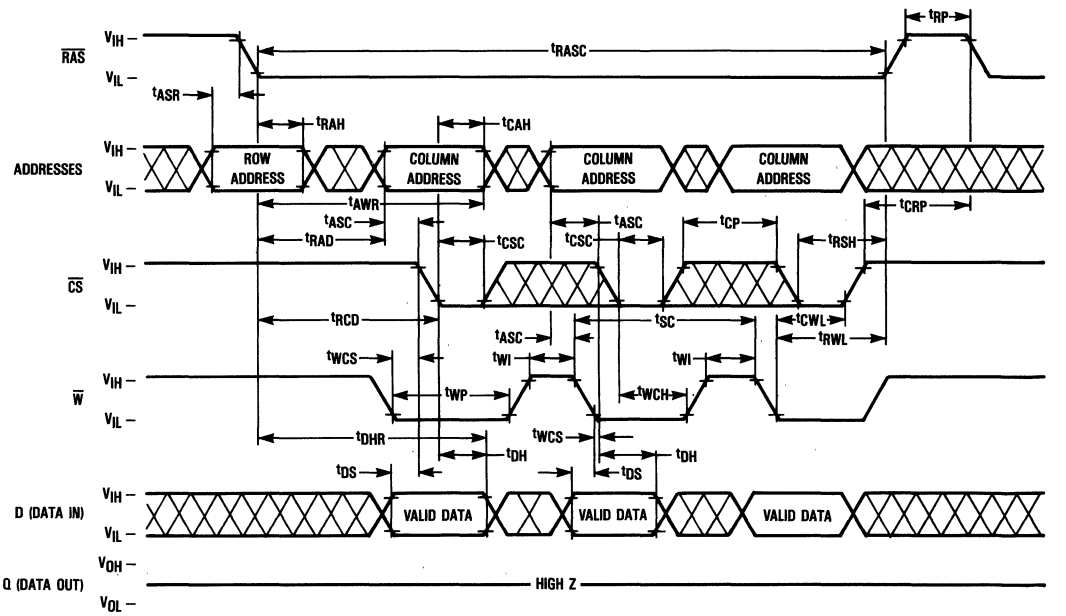


2

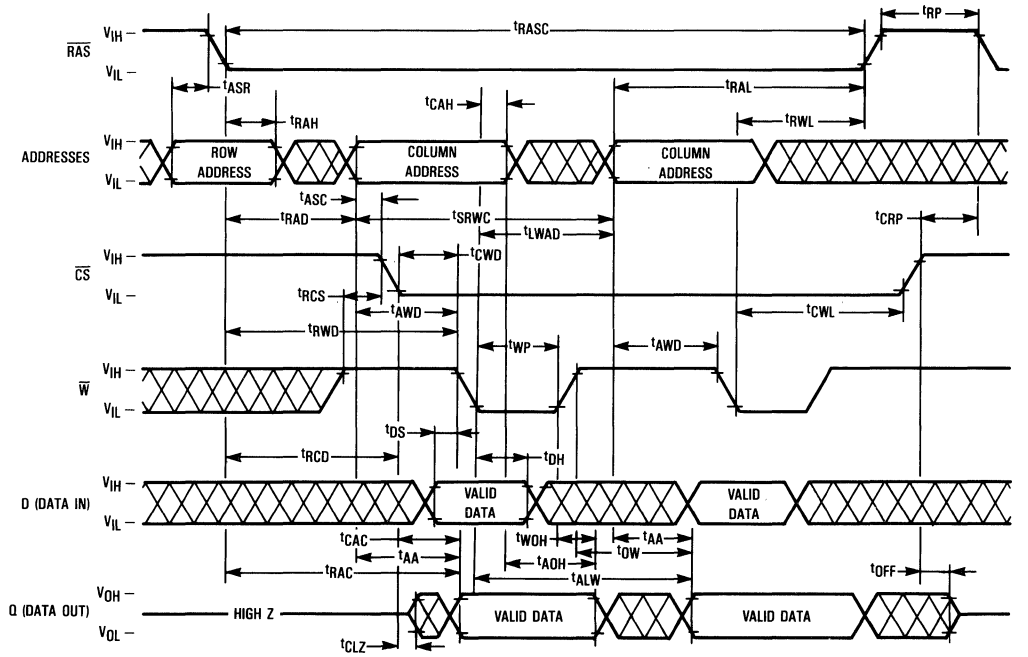
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) (A)



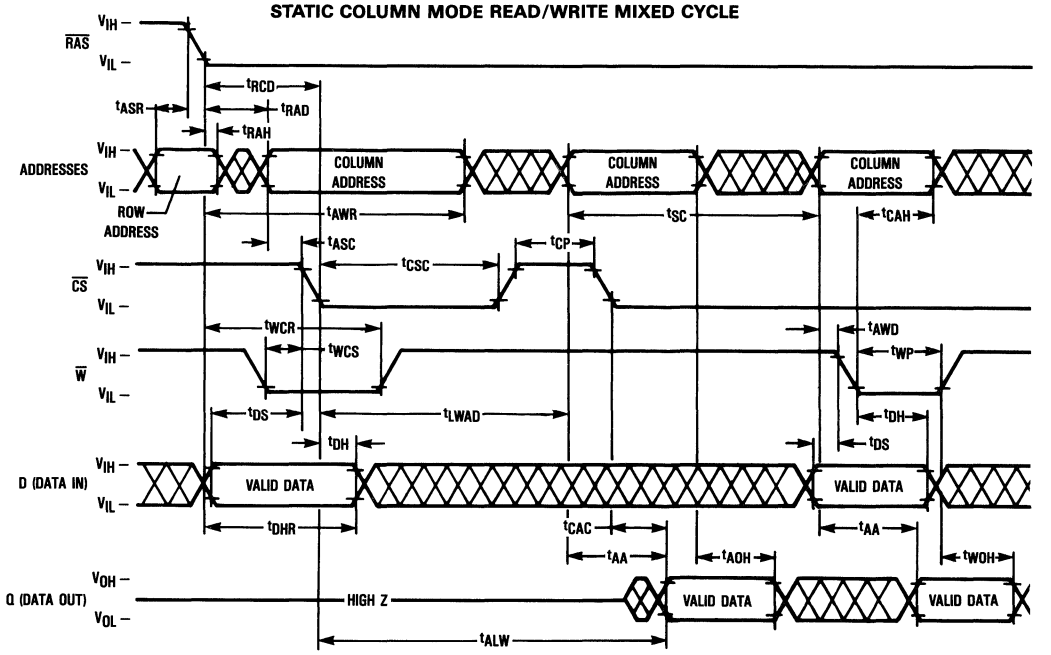
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) (B)



STATIC COLUMN MODE READ-WRITE CYCLE

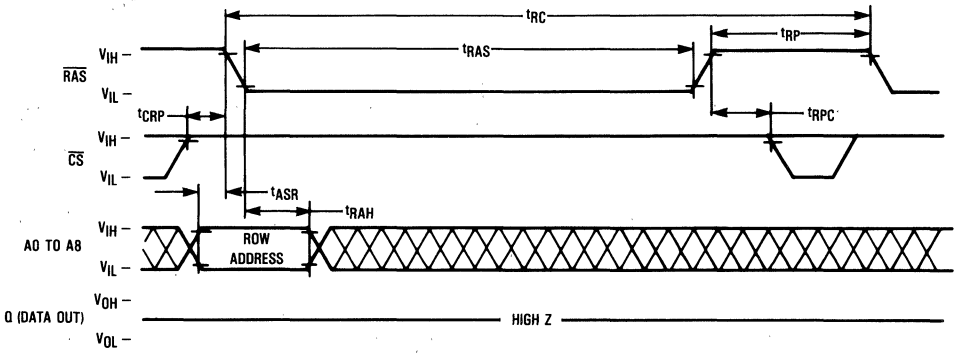


STATIC COLUMN MODE READ/WRITE MIXED CYCLE

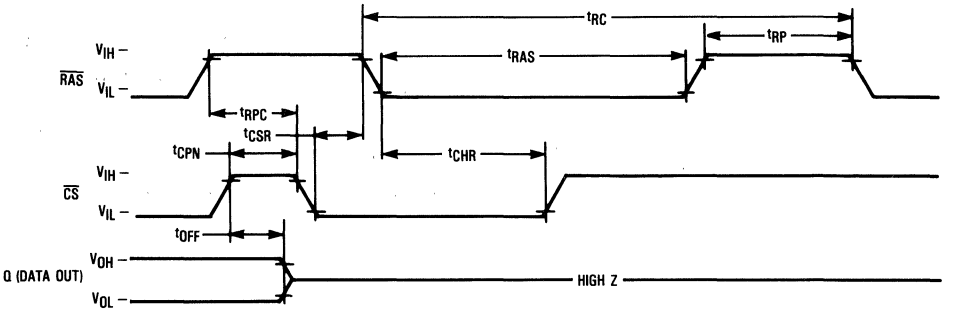


2

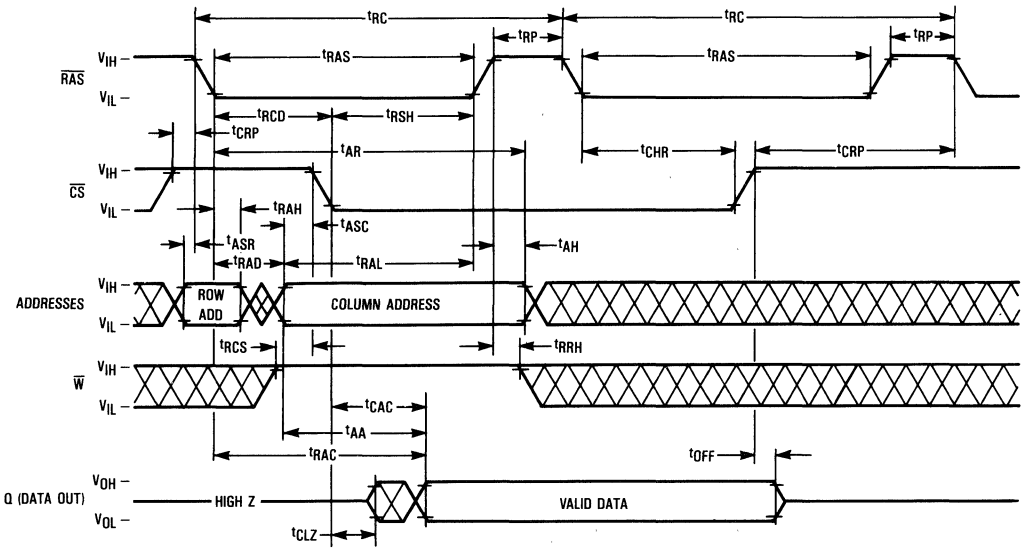
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and A9 are Don't Care)



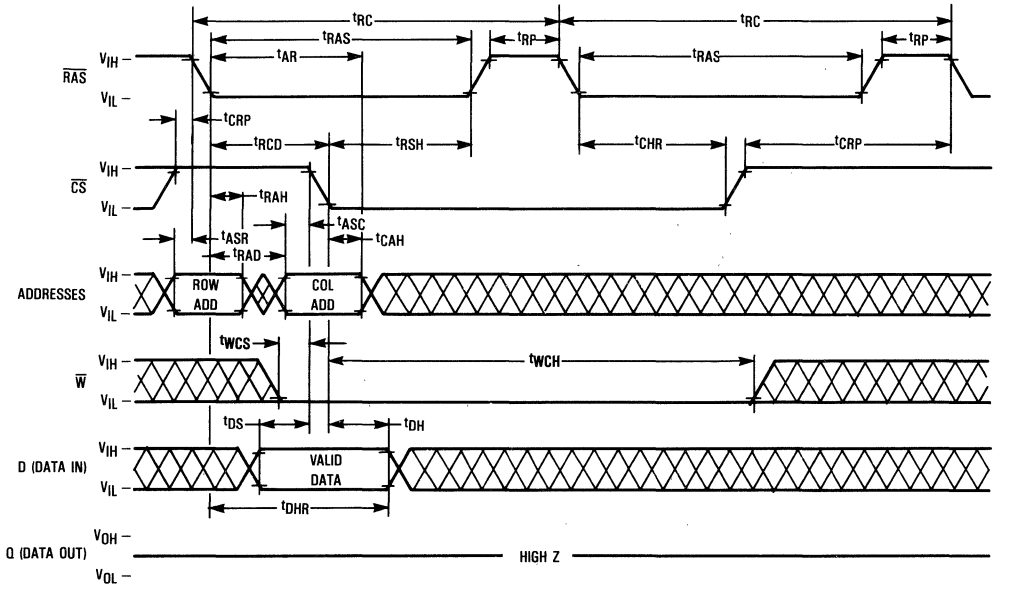
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$ and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)

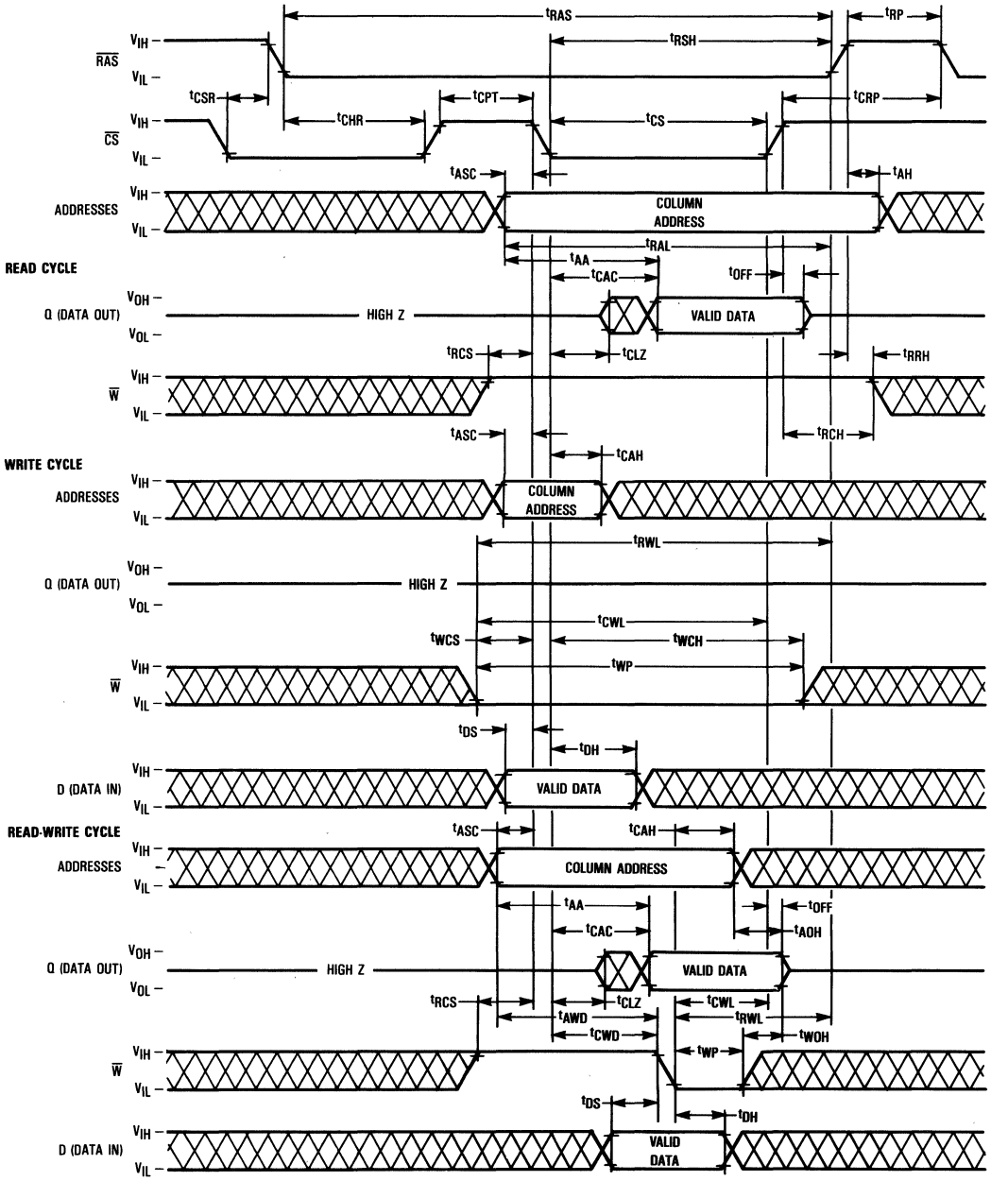


HIDDEN REFRESH CYCLE (WRITE)



2

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and chip select ($\overline{CS}$). A total of twenty address bits will decode one of the 1,048,576 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called static column mode, allows the user to column access the 1024 bits within a selected row. (See **STATIC COLUMN CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CS}$ clock active transition will determine read access time. The external $\overline{CS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CS}$ clock will allow the external $\overline{CS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CS}) period for the $\overline{CS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CS}$ clock is active; the output will switch to the three-state mode when the $\overline{CS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL}+t_{RP}+2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

2

STATIC COLUMN CYCLES

Static column operation allows fast successive data operations at the 1024 column locations within a row. Access time is typically half the regular $\overline{RAS}$ clock access (t_{RAC}). Static column operation is achieved by holding both $\overline{RAS}$ and $\overline{CS}$ low, and selecting the column location determined by the 10-bit column address field.

The static column cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by a column address and $\overline{CS}$ clock, as in a normal read or write cycle. Subsequent column addresses are accessed at a higher speed (t_{AA}, t_{ALW}, t_{OW}, or t_{CAC}, depending on the previous and intended operation), as the column address field is changed. Read, write, and read-write operations can be performed and mixed in any order when the device is in the static column mode.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the row address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with a read-write operation. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write "0"s into all memory cells (normal write mode).
2. Select a column address, read "0" out and write "1" into the cell by performing **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read "1"s (normal read mode), which were written at step 2.
4. Using the same column as in step 2, read "1" out and write "0" into the cell by performing **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s (normal read mode), which were written at step 4.
6. Repeat steps 1 to 5 using complement data.

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0-A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0-B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle, including page mode cycles. The test mode function is enabled by holding

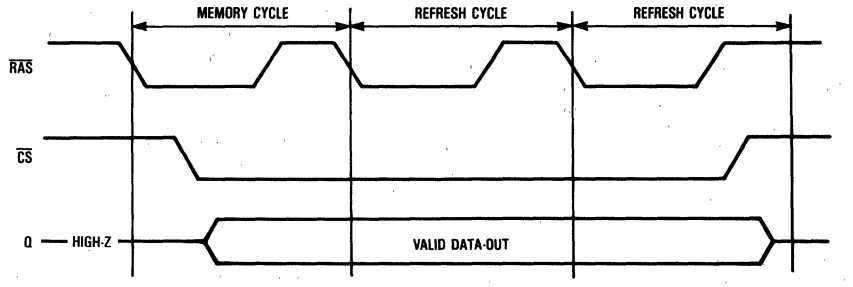


Figure 1. Hidden Refresh Cycle

the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

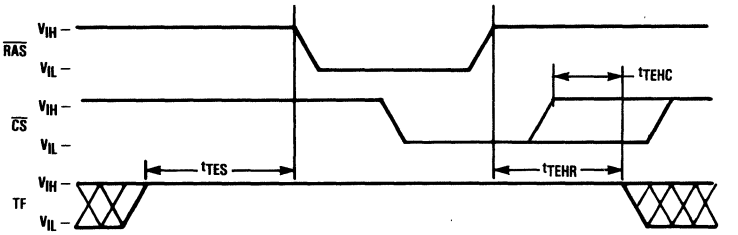
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

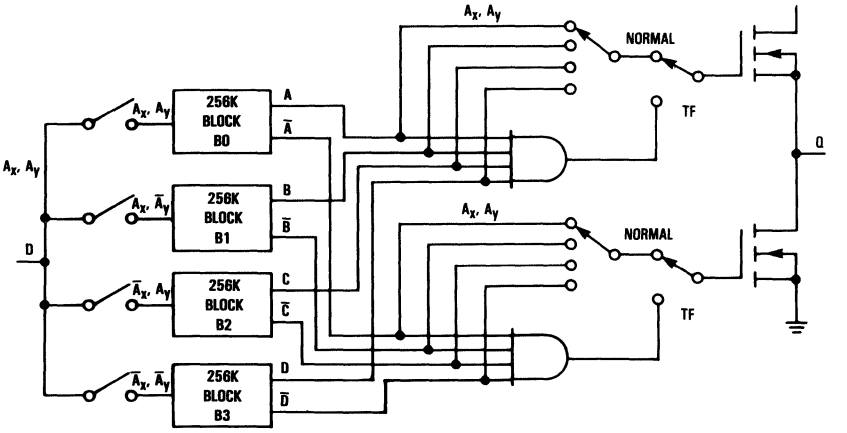
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
—	Any Other				High-Z

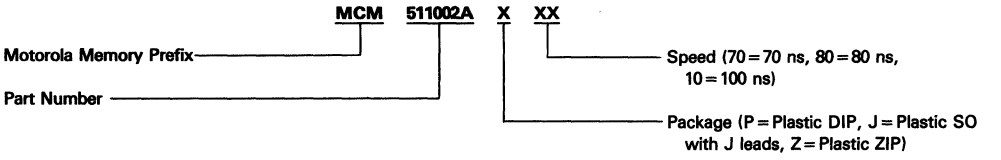
TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—			
	MCM511002AP70	MCM511002AJ70	MCM511002AZ70
	MCM511002AP80	MCM511002AJ80	MCM511002AZ80
	MCM511002AP10	MCM511002AJ10	MCM511002AZ10

2

MCM514256A
MCM51L4256A

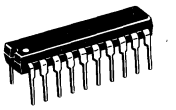
Advance Information

256K x 4 CMOS Dynamic RAM

The MCM514256A is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

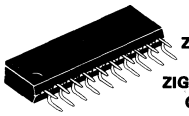
The MCM514256A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line package (DIP), a 300-mil J-lead small outline package (SOJ), and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Fast Page Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM514256A-70 and MCM51L4256A-70 = 70 ns (Max)
  - MCM514256A-80 and MCM51L4256A-80 = 80 ns (Max)
  - MCM514256A-10 and MCM51L4256A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM514256A-70 and MCM51L4256A-70 = 440 mW (Max)
  - MCM514256A-80 and MCM51L4256A-80 = 385 mW (Max)
  - MCM514256A-10 and MCM51L4256A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  - 11 mW (Max), TTL Levels
  - 5.5 mW (Max), CMOS Levels



P PACKAGE
PLASTIC
CASE 738A

J PACKAGE
SMALL OUTLINE
CASE 822

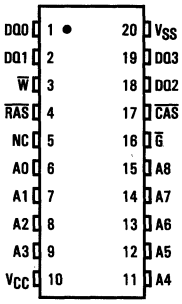


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836A

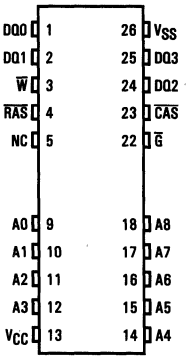
PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

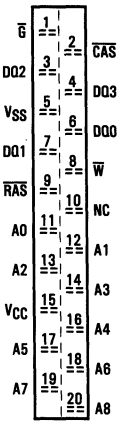
DUAL-IN-LINE



SMALL OUTLINE

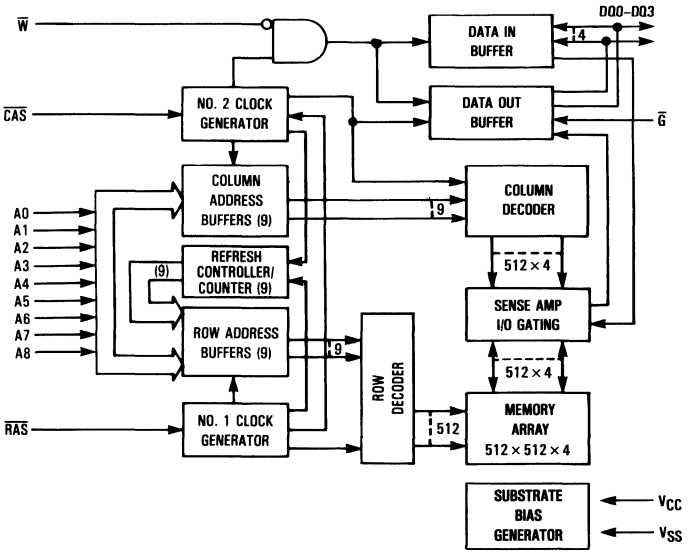


ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns		–	80		
MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns		–	70		
MCM514256A-10 and MCM51L4256A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns		–	80		
MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns		–	70		
MCM514256A-10 and MCM51L4256A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{PC} = 40 ns		–	60		
MCM514256A-80 and MCM51L4256A-80, t_{PC} = 45 ns		–	50		
MCM514256A-10 and MCM51L4256A-10, t_{PC} = 55 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V) MCM514256A	I_{CC5}	–	1.0	mA	
MCM51L4256A		–	200	µA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514256A-70 and MCM51L4256A-70, t_{RC} = 130 ns		–	80		
MCM514256A-80 and MCM51L4256A-80, t_{RC} = 150 ns		–	70		
MCM514256A-10 and MCM51L4256A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current, Battery Backup Mode—MCM51L4256A only (t_{RC} = 125 µs; t_{RAS} = 1 µs min; $\overline{CAS} = \overline{CAS}$ Before $\overline{RAS}$ Cycle or 0.2 V; A0-A8, $\overline{G}$, $\overline{W}$, DQ0-DQ3 = V_{CC} − 0.2 V or 0.2 V)	I_{CC7}	–	200	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5	pF	3
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	DQ0-DQ3	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		MCM514256A-10 MCM51L4256A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	185	–	205	–	245	–	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	–	45	–	55	–	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRMW}	95	–	100	–	115	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	35	–	40	–	50	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

2

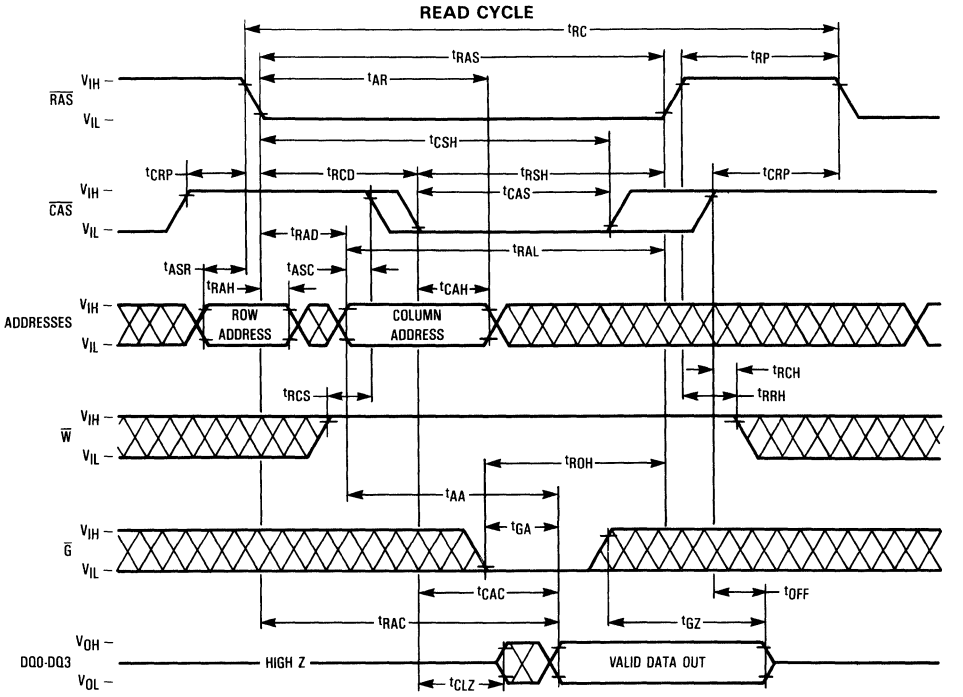
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514256A-70 MCM51L4256A-70		MCM514256A-80 MCM51L4256A-80		MCM514256A-10 MCM51L4256A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	14
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period MCM514256A MCM51L4256A	t_{RVRV}	t_{RFSH}	– –	8 64	– –	8 64	– –	8 64	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	–	50	–	60	–	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	100	–	110	–	135	–	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	–	70	–	85	–	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	10	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	20	–	20	–	25	ns	
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	–	20	–	25	–	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	10
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	–	20	–	25	–	ns	

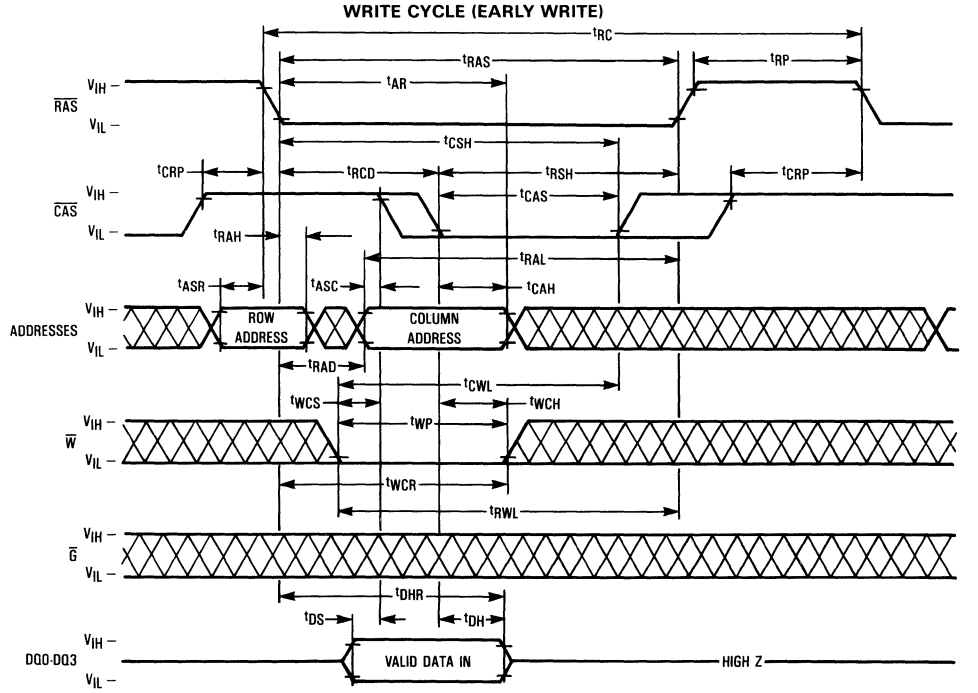
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



WRITE CYCLE (EARLY WRITE)



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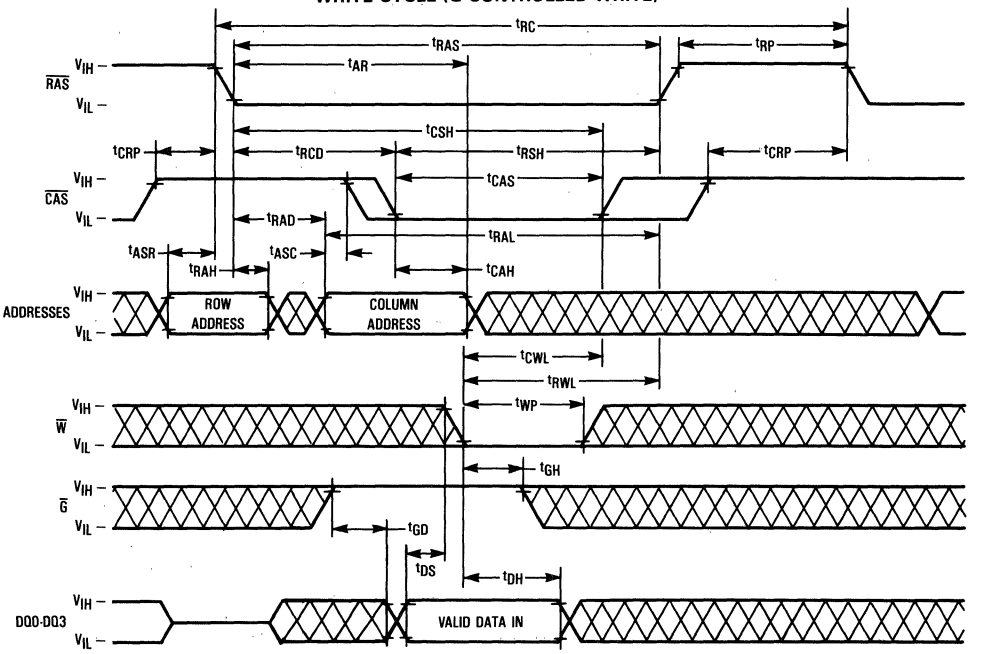
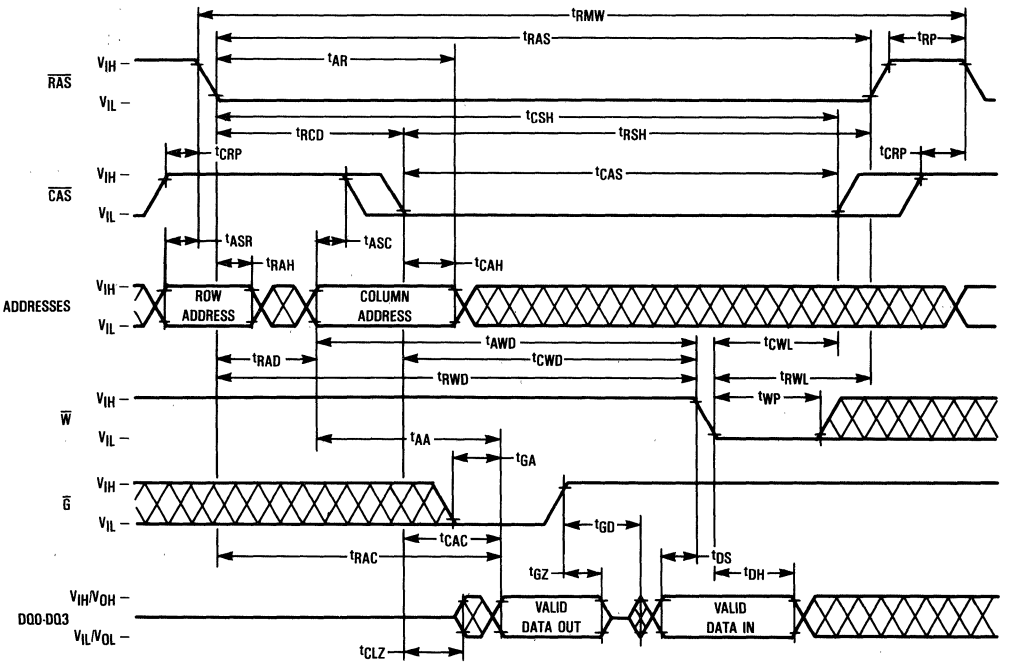
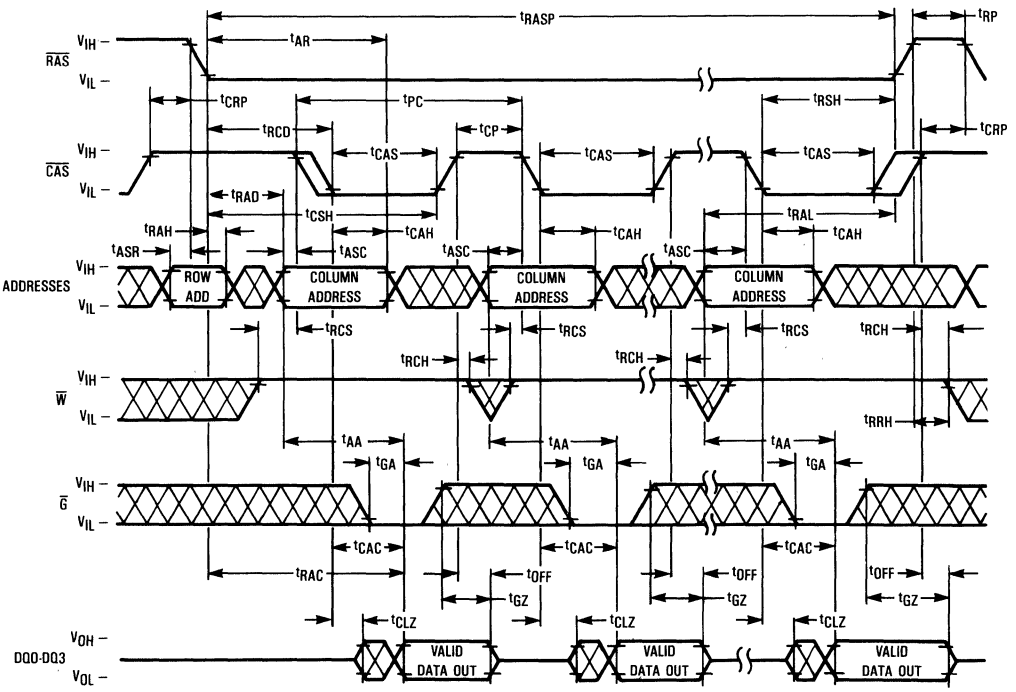
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



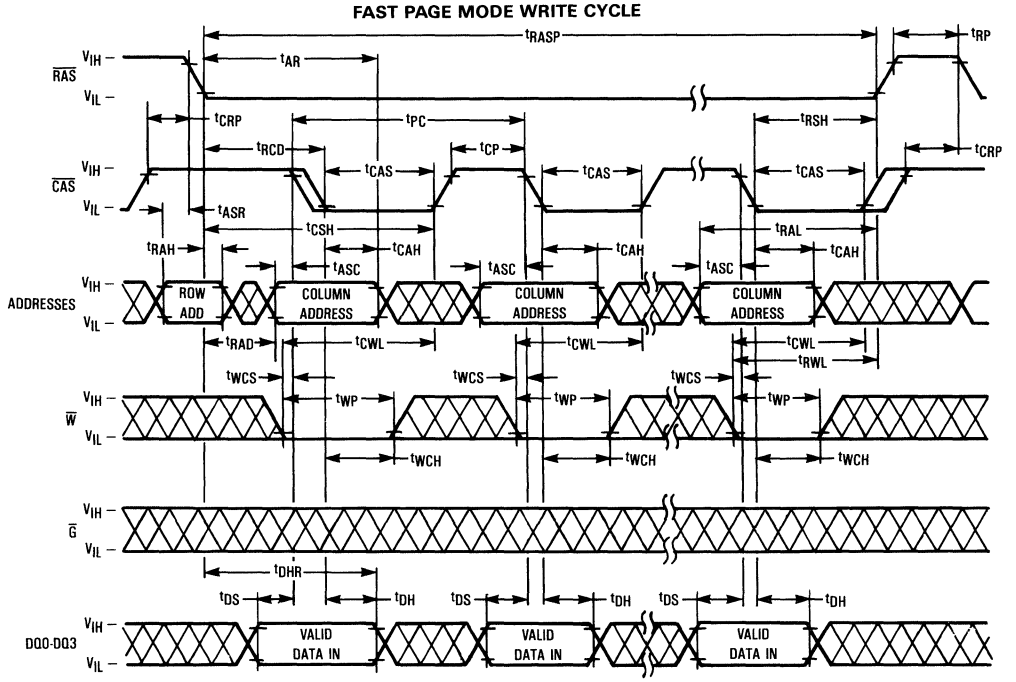
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE



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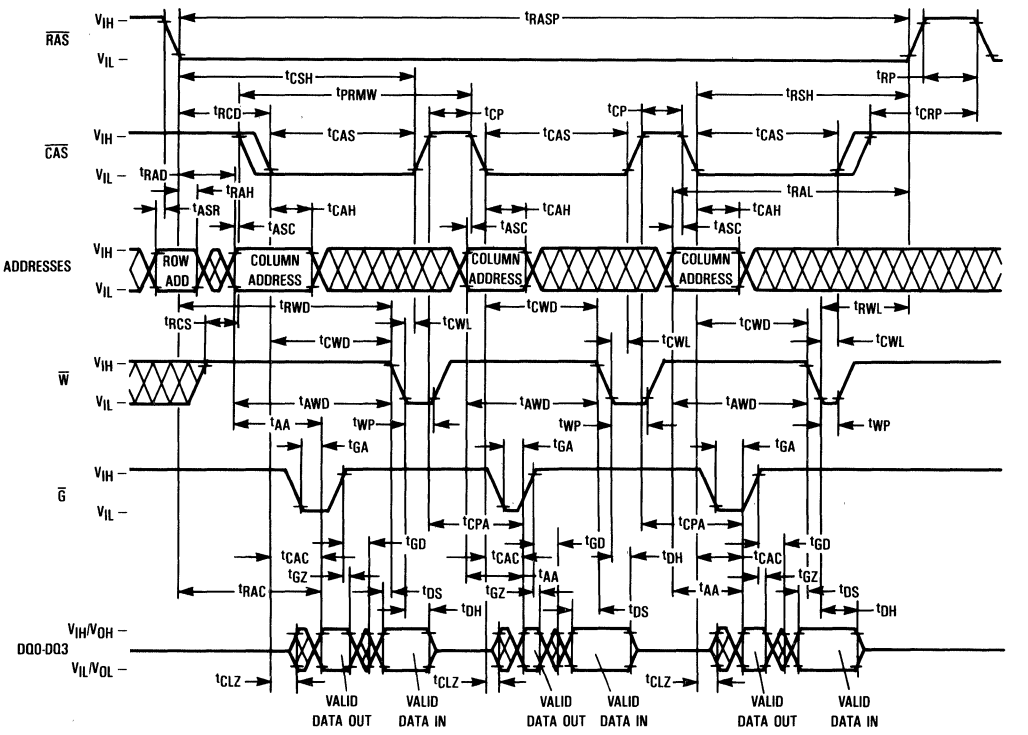
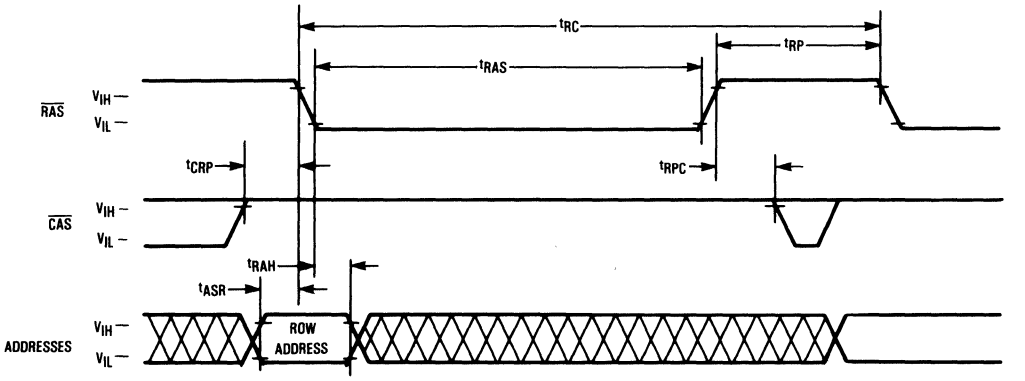
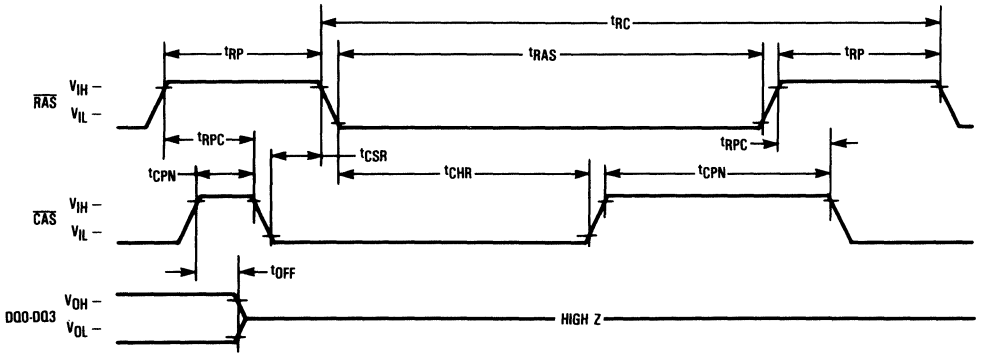
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$, $\overline{G}$, and A0-A8 are Don't Care)



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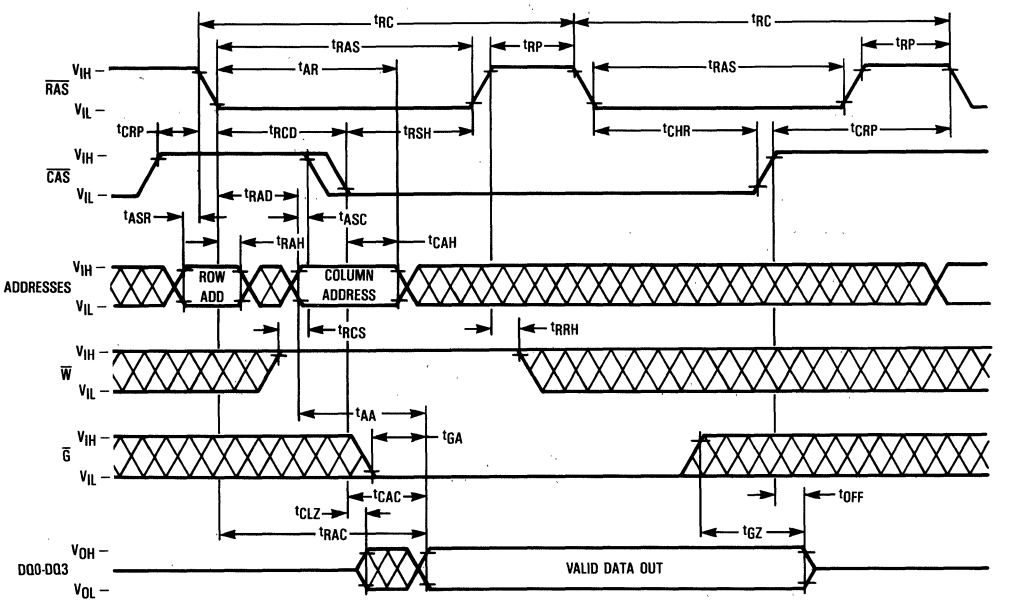
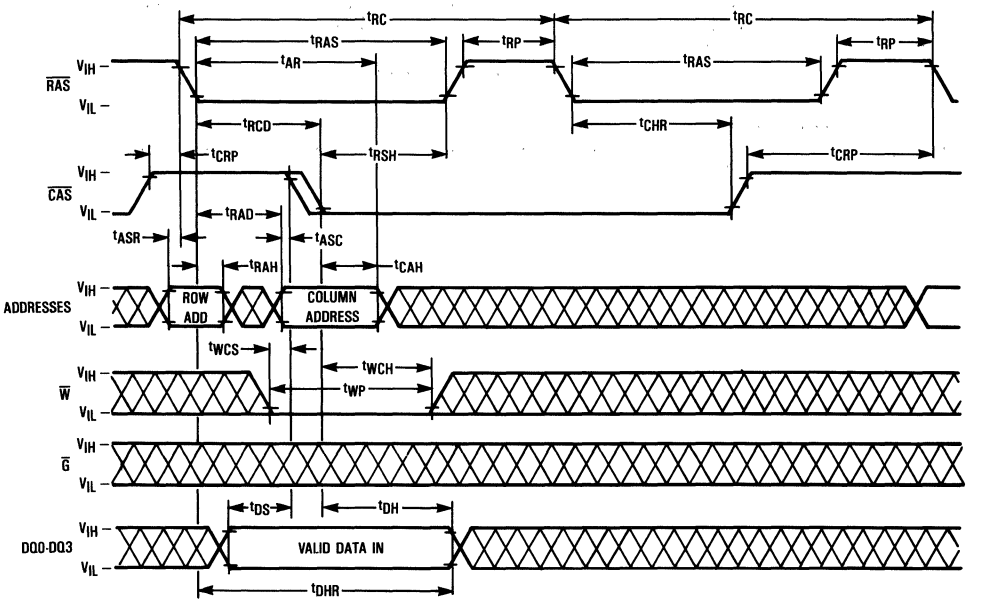
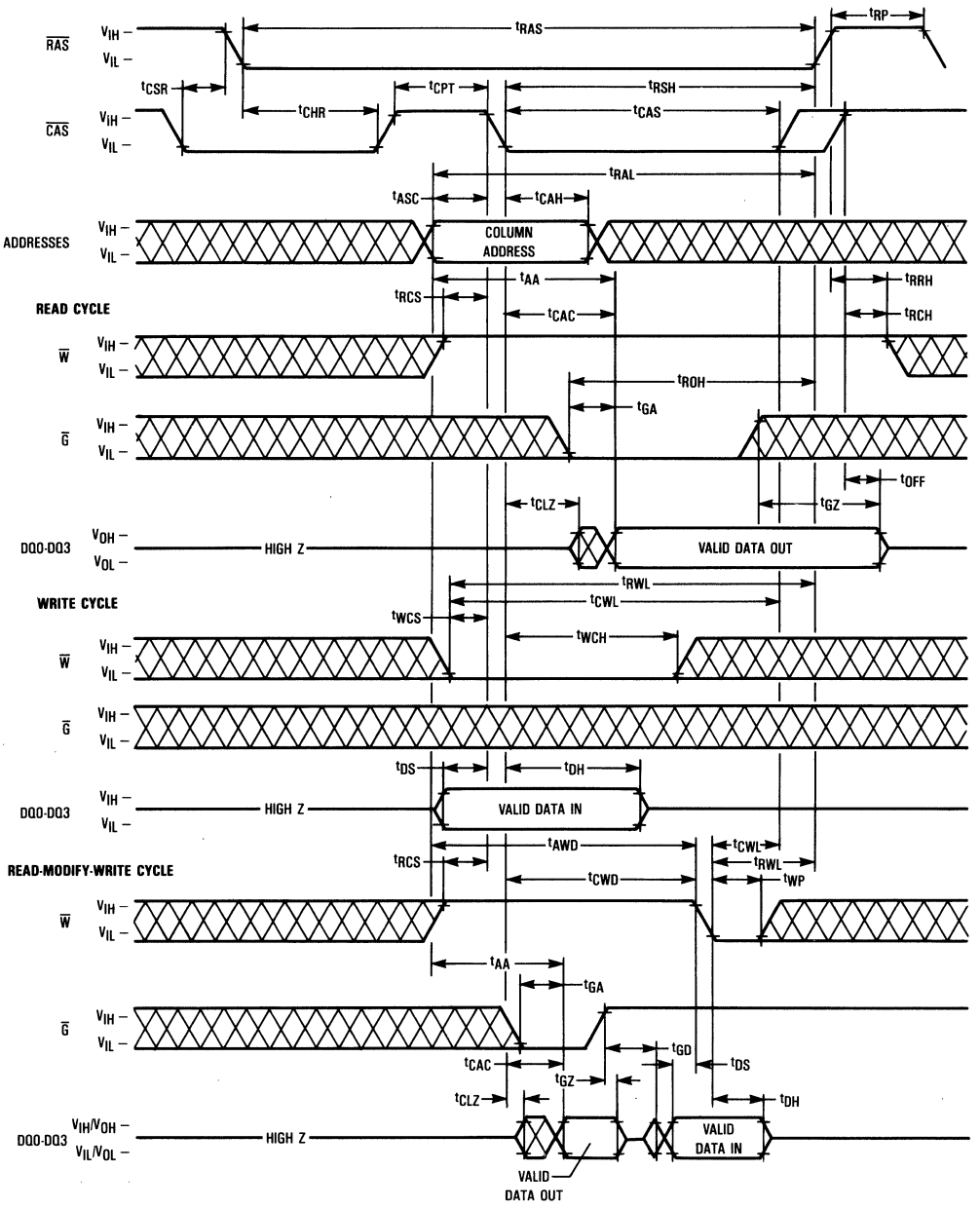
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of 18 address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CAS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called page mode allows the user to column access the 512 bits within a selected row. The refresh mode and page mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CAS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 512 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular row decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MCM514256A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM514256A is that a refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with a read-write operation. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows.

1. Write a "0"s into all memory cells (normal write mode).
2. Select a column address, read "0" out and write "1" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read "1"s (normal read mode), which were written at step 2.
4. Using the same column as in step 2, read "1" out and write "0" into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s (normal read mode), which were written at step 4.
6. Repeat steps 1 to 5 using complement data.

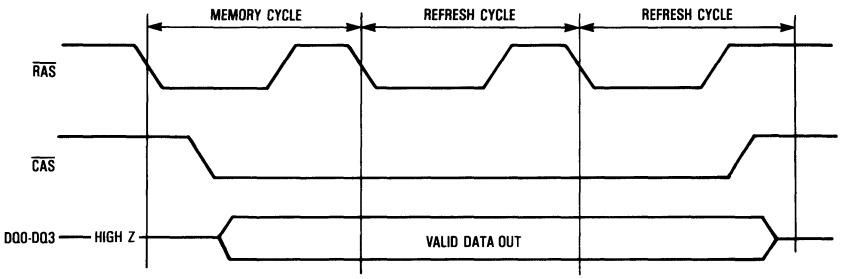
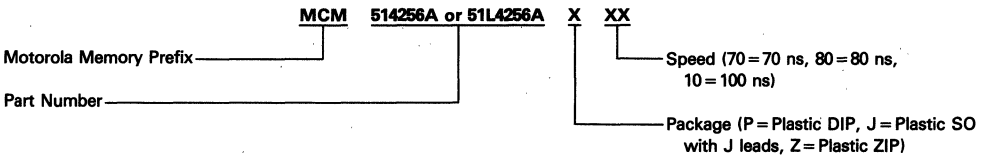


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM514256AP70	MCM514256AJ70	MCM514256AZ70
	MCM514256AP80	MCM514256AJ80	MCM514256AZ80
	MCM514256AP10	MCM514256AJ10	MCM514256AZ10
	MCM51L4256AP70	MCM51L4256AJ70	MCM51L4256AZ70
	MCM51L4256AP80	MCM51L4256AJ80	MCM51L4256AZ80
	MCM51L4256AP10	MCM51L4256AJ10	MCM51L4256AZ10

MCM514258A

2

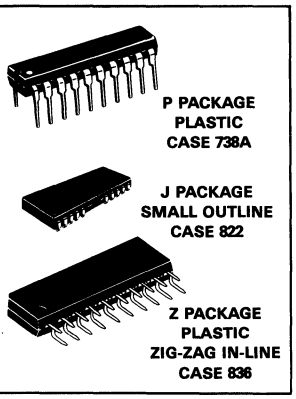
Advance Information

256K x 4 CMOS Dynamic RAM

The MCM514258A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM514258A requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line package (DIP), a 300-mil J-lead small outline package, and a 100-mil zig-zag in-line package (ZIP).

- Three-State Data Output
- Static Column Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM514258A-70 = 70 ns (Max)
  - MCM514258A-80 = 80 ns (Max)
  - MCM514258A-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM514258A-70 = 440 mW (Max)
  - MCM514258A-80 = 385 mW (Max)
  - MCM514258A-10 = 330 mW (Max)
- Low Standby Power Dissipation:
  - 11 mW (Max), TTL Levels
  - 5.5 mW (Max), CMOS Levels



P PACKAGE
PLASTIC
CASE 738A

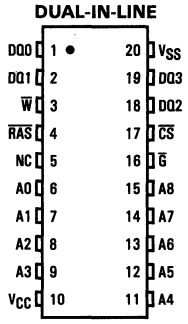
J PACKAGE
SMALL OUTLINE
CASE 822

Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

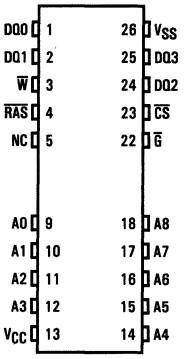
PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

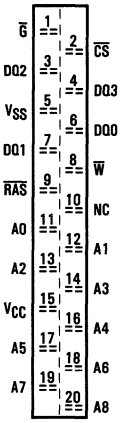
DUAL-IN-LINE



SMALL OUTLINE



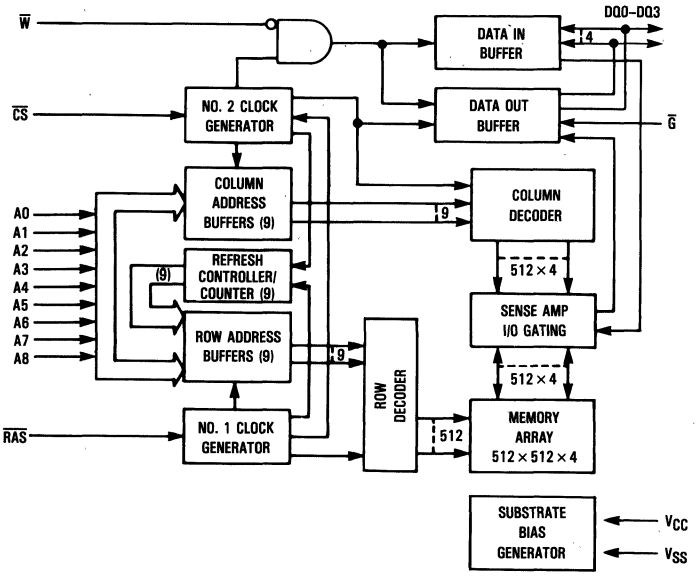
ZIG-ZAG IN-LINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514258A-70, t_{RC} = 130 ns		–	80		
MCM514258A-80, t_{RC} = 150 ns		–	70		
MCM514258A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS}$ = V_{IH})	I_{CC3}			mA	2
MCM514258A-70, t_{RC} = 130 ns		–	80		
MCM514258A-80, t_{RC} = 150 ns		–	70		
MCM514258A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM514258A-70, t_{SC} = 40 ns		–	60		
MCM514258A-80, t_{SC} = 45 ns		–	50		
MCM514258A-10, t_{SC} = 55 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2 V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514258A-70, t_{RC} = 130 ns		–	80		
MCM514258A-80, t_{RC} = 150 ns		–	70		
MCM514258A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5	pF	3
	$\overline{G}$, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CS}$ = V_{IH} to Disable Output)	DQ0-DQ3	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = IΔt/ΔV.

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514258A-70		MCM514258A-80		MCM514258A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	185	–	205	–	245	–	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	40	–	45	–	55	–	ns	
Static Column Mode Read-Modify-Write Cycle Time	t_{AVAV}	t_{SRMW}	100	–	110	–	135	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	6, 7
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	–	25	–	25	–	30	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	–	65	–	75	–	95	ns	6, 10
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	30	ns	11
Output Data Hold Time from Column Address	t_{AXQX}	t_{AOH}	5	–	5	–	5	–	ns	
Output Data Enable Time from Write	t_{WHQV}	t_{OW}	–	20	–	20	–	30	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	–	25	–	30	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	55	25	70	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	15	–	ns	
$\overline{CS}$ Precharge Time (Static Column Mode)	t_{CEHCEL}	t_{CP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	55	–	60	–	75	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	85	–	95	–	115	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

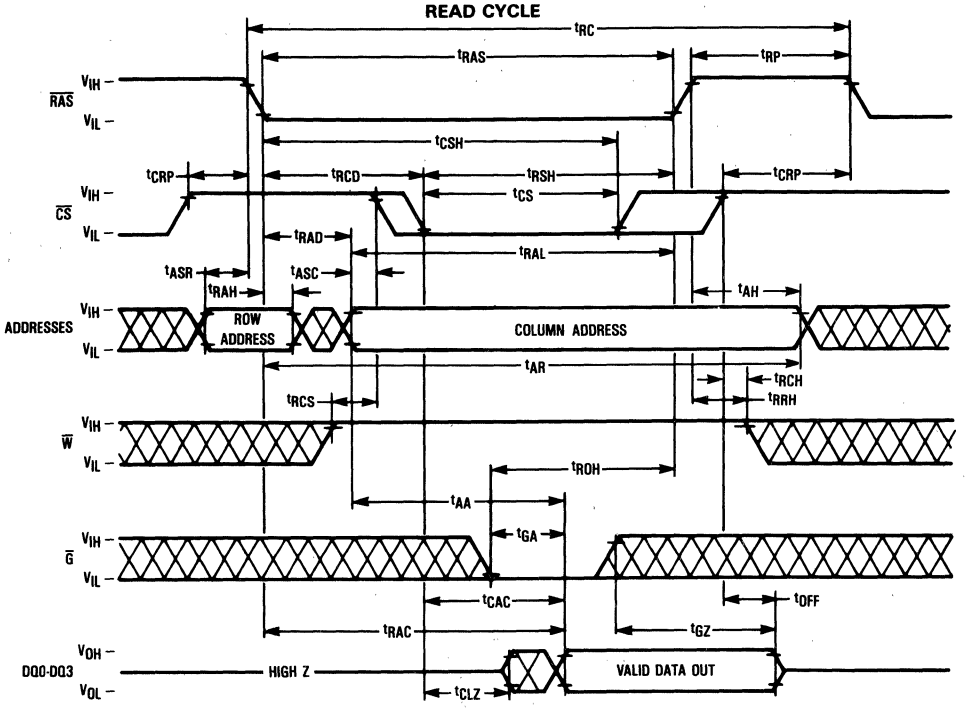
Parameter	Symbol		MCM514258A-70		MCM514258A-80		MCM514258A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Hold Time Referenced to $\overline{RAS}$	t_{REHAX}	t_{AH}	10	–	10	–	10	–	ns	14
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	20	30	20	35	25	45	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	65	–	75	–	95	–	ns	
Read Command Setup Time Referenced to $\overline{CS}$	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	16
Write Command Hold Time (Output Data Disable)	t_{CEHWH}	t_{WCH}	15	–	15	–	20	–	ns	17
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Inactive Time	t_{WHWL}	t_{WI}	10	–	10	–	10	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	18
Data in Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	18
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	17
$\overline{CS}$ to Write Delay (RMW Cycle)	t_{CELWL}	t_{CWD}	55	–	55	–	65	–	ns	17
$\overline{RAS}$ to Write Delay (RMW Cycle)	t_{RELWL}	t_{RWD}	100	–	110	–	135	–	ns	17
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	65	–	70	–	85	–	ns	17
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{CELREL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	10	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	25	–	25	–	30	ns	
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	20	–	20	–	25	–	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	11
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	20	–	20	–	25	–	ns	

NOTES:

14. t_{AH} is the condition to latch the column address when $\overline{RAS}$ transitions from low to high.
15. Operation within the specified t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. t_{WCH}, t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min) and $t_{WCH} \geq t_{WCH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
18. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.

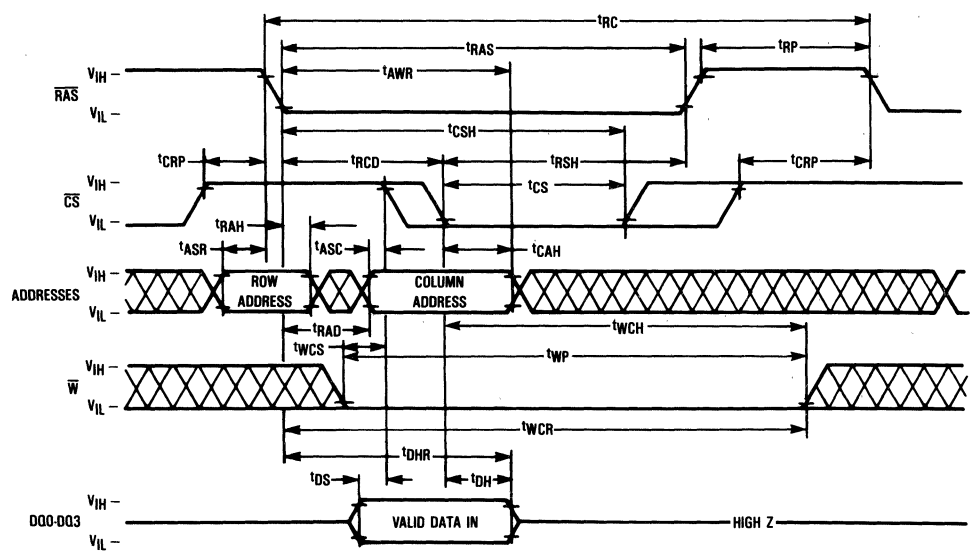
2

READ CYCLE

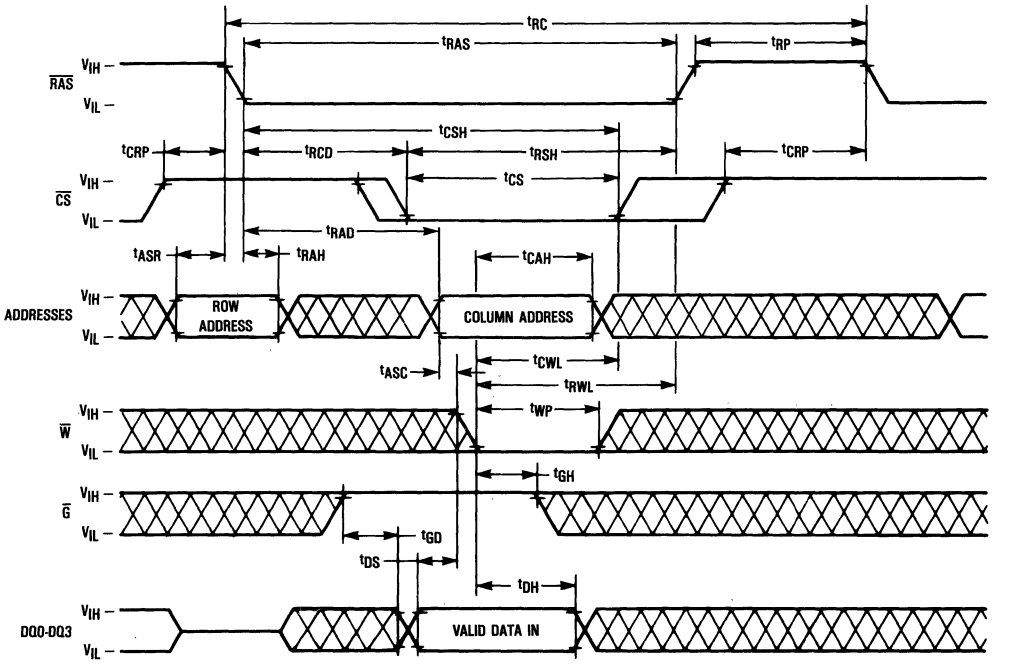


WRITE CYCLE (EARLY WRITE)

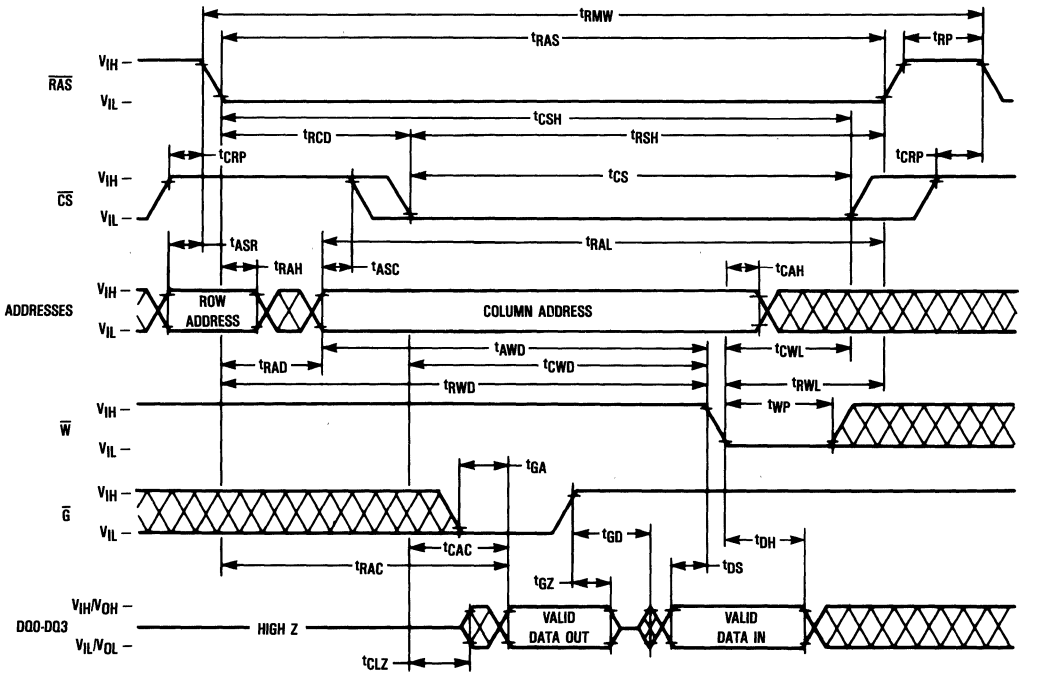
($\overline{G}$ is Don't Care)



WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)

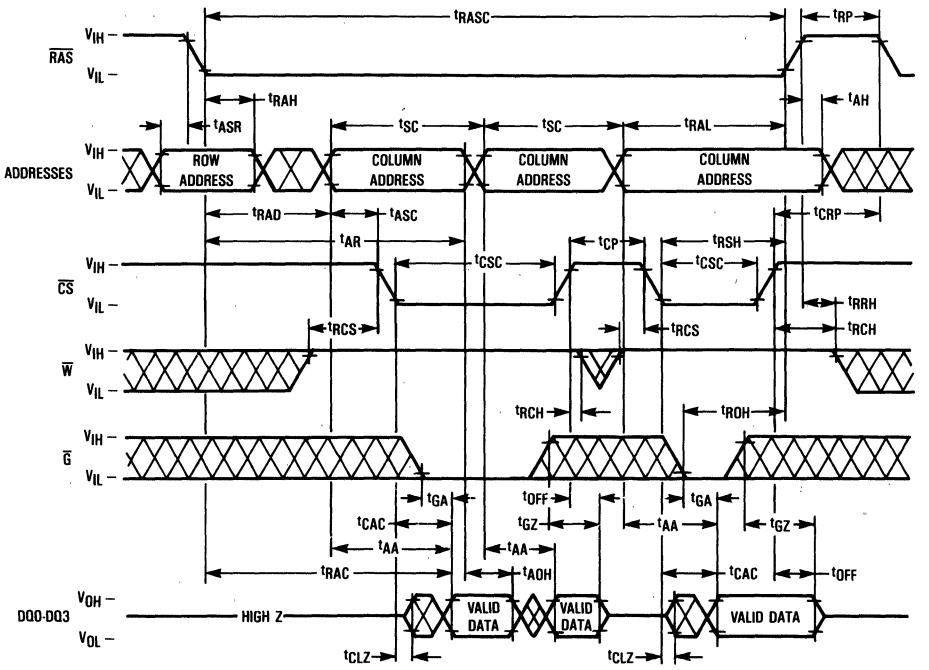


READ-MODIFY-WRITE CYCLE



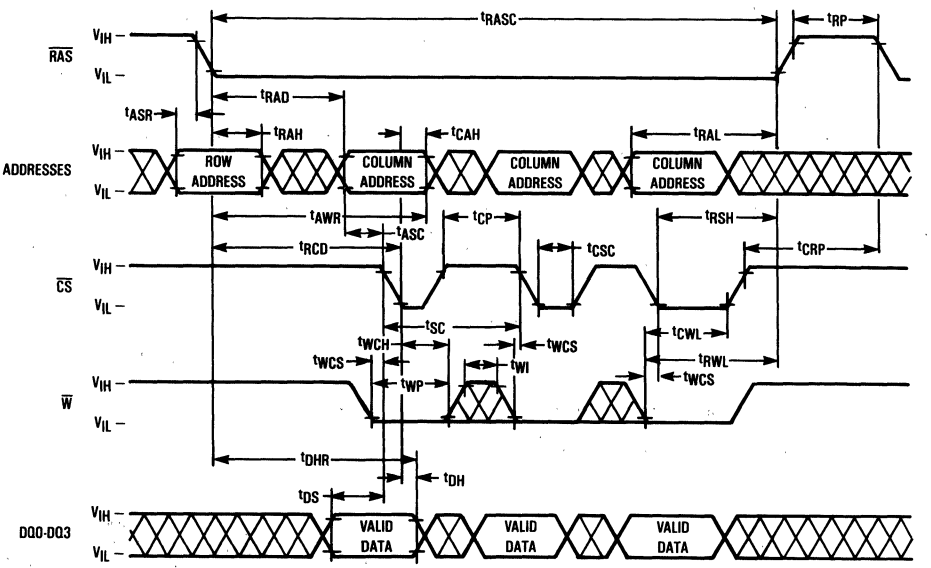
2

STATIC COLUMN MODE READ CYCLE



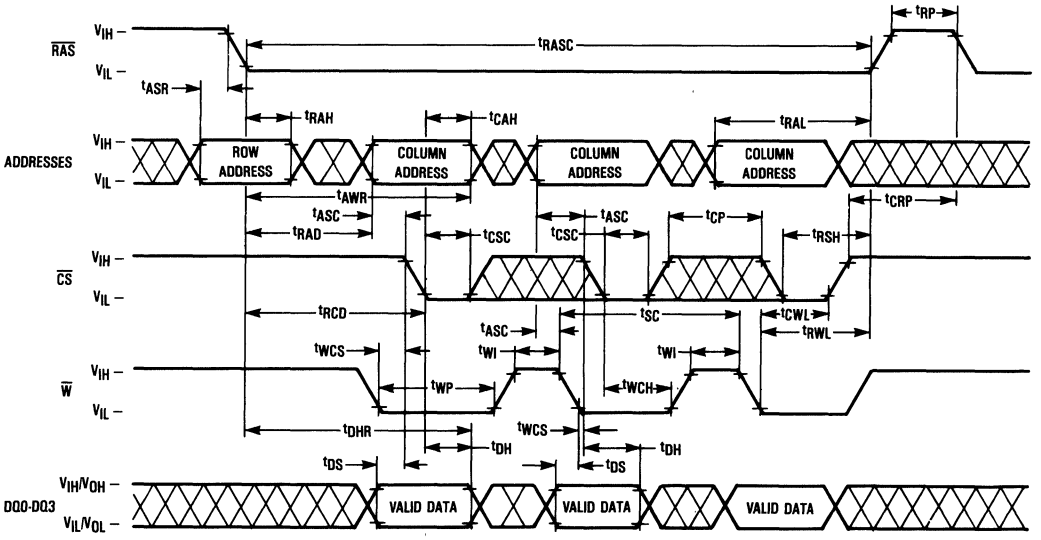
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) (A)

($\overline{G}$ is Don't Care)

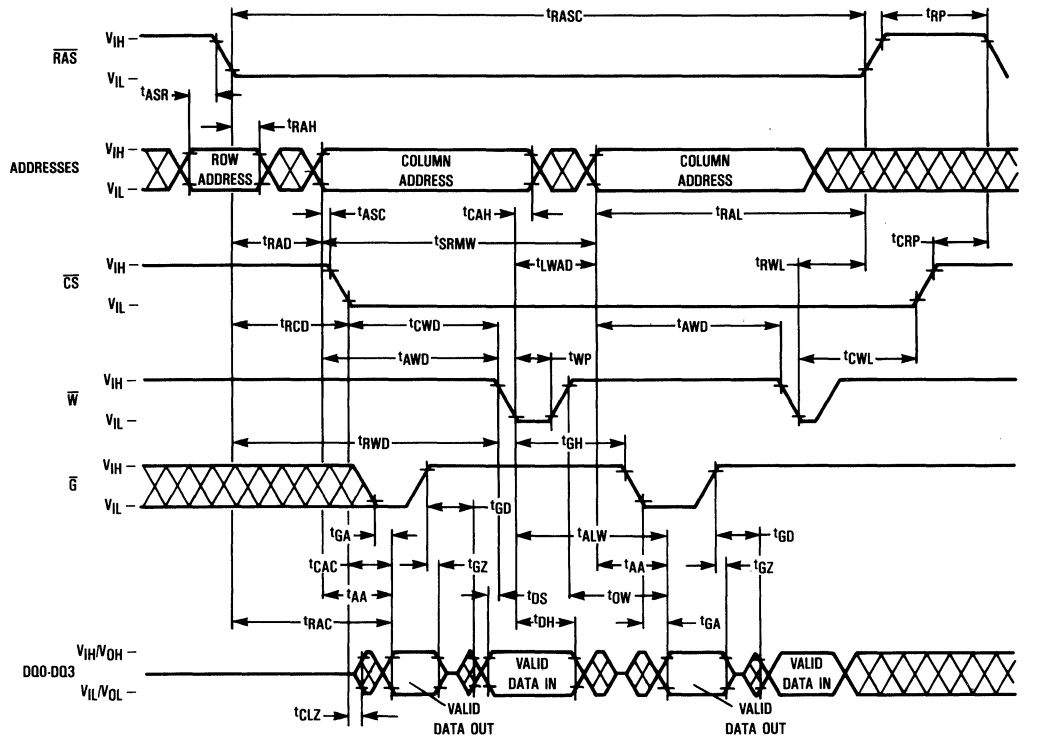


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE) (B)

($\overline{G}$ is Don't Care)



STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



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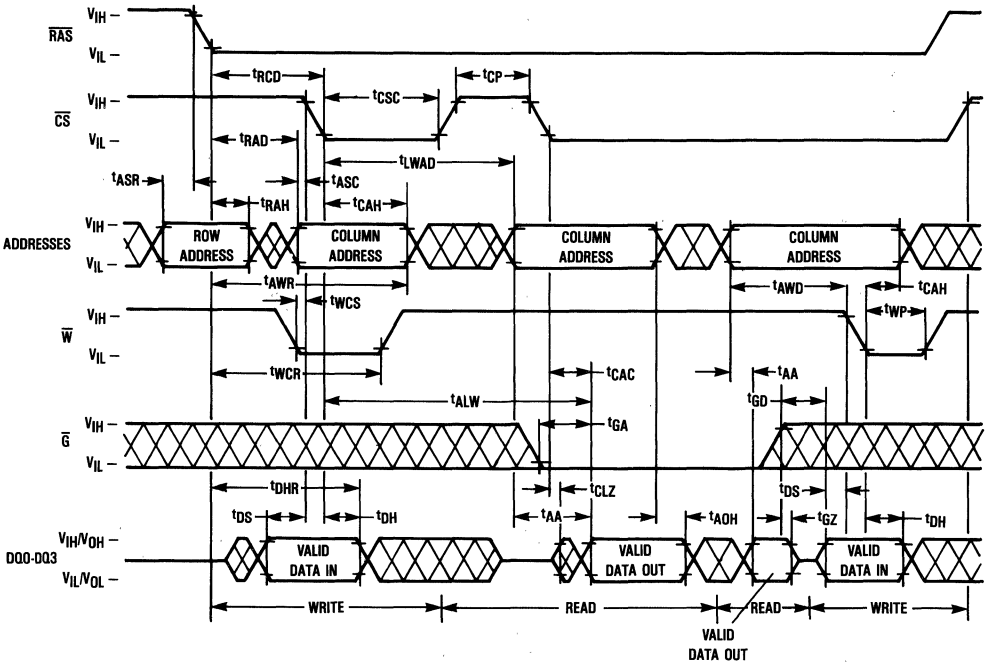
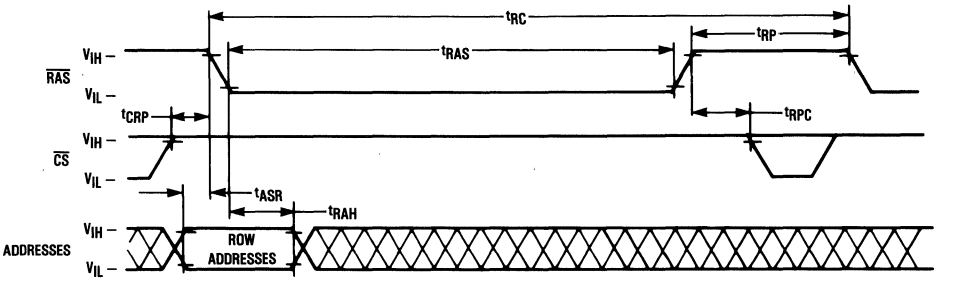
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



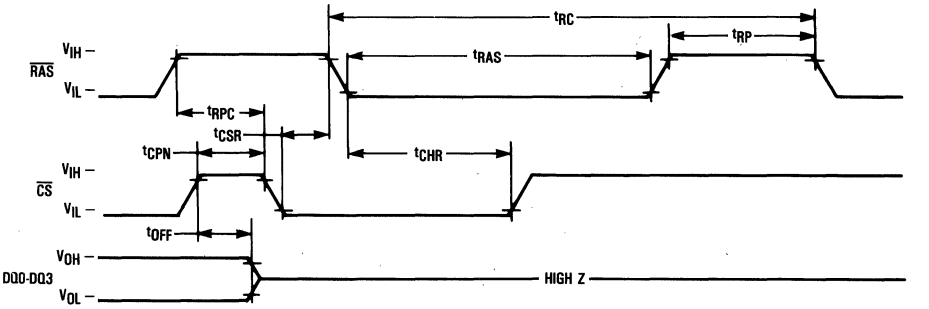
RAS ONLY REFRESH CYCLE

(W and G are Don't Care)

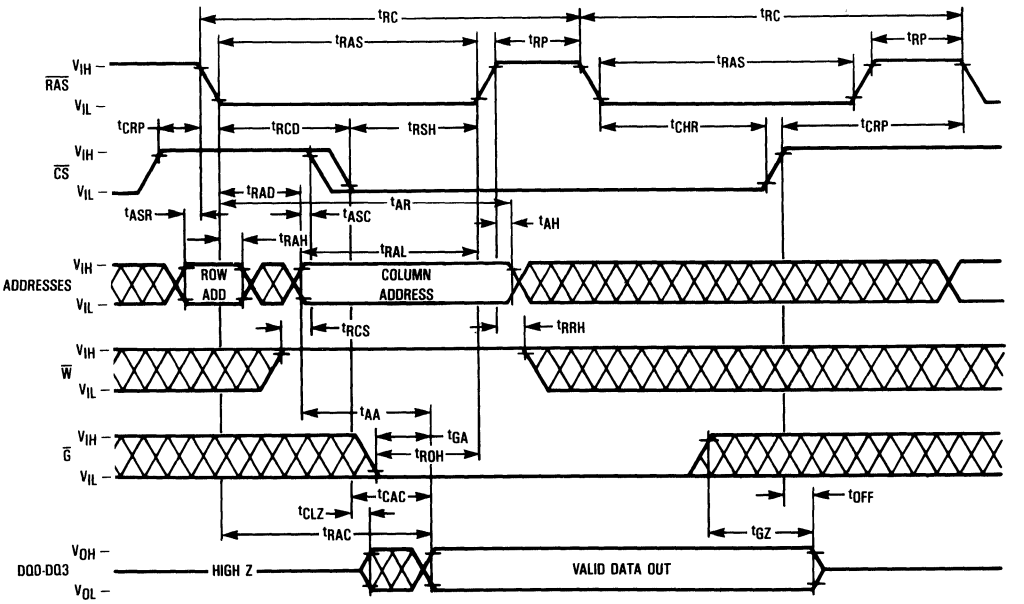


CS BEFORE RAS REFRESH CYCLE

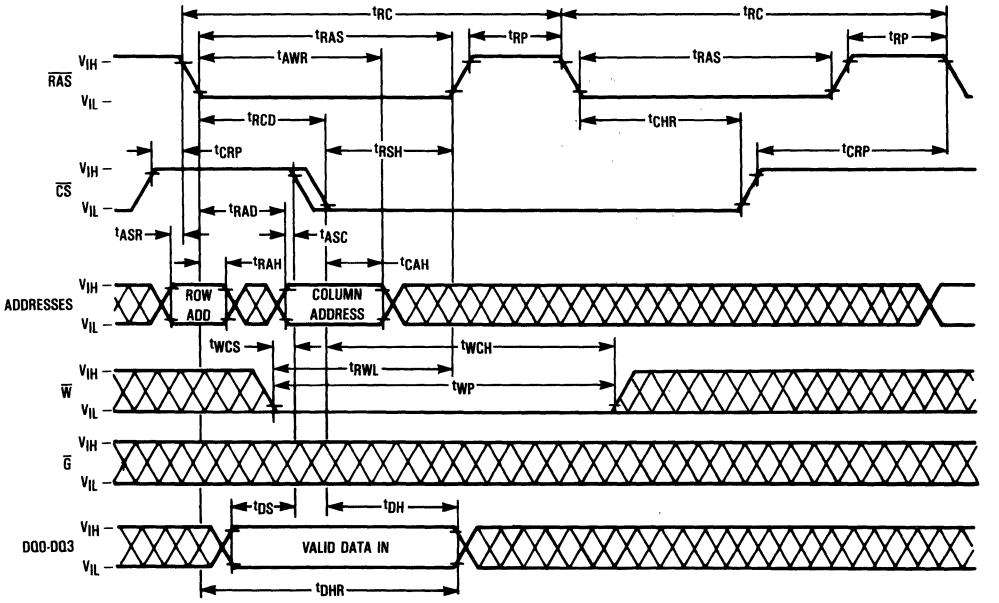
(W, G, and A0 to A8 are Don't Care)



HIDDEN REFRESH CYCLE (READ)

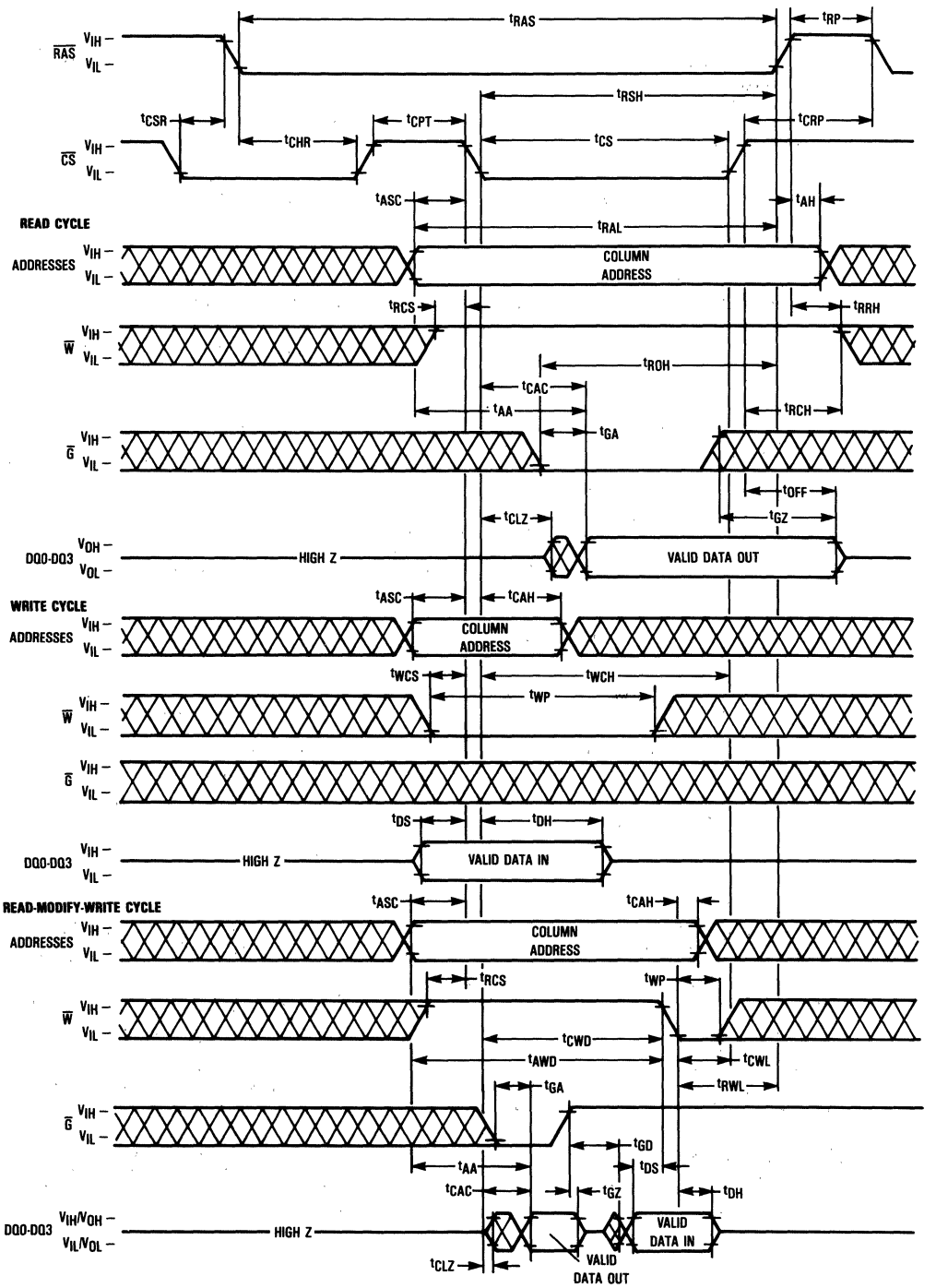


HIDDEN REFRESH CYCLE (WRITE)



2

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active low) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CS}$). A total of 18 address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called static column mode allows the user to column access the 512 bits within a selected row. The refresh mode and static column mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a static column mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CS}$ clock active transition will determine read access time. The external $\overline{CS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CS}$ clock will allow the external $\overline{CS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CS}) period for the $\overline{CS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CS}$ clock. This time could be as long as 10 microseconds—$[t_{RWL}+t_{RP}+2t_T]$.

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

2

STATIC COLUMN MODE CYCLES

Output buffers are always on when the device is in the static column mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. The static column mode allows faster access (t_{AA}) to any of the 512 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column mode operation consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. The row address is latched by the $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column mode following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained. Static column cycle time determines how fast successive bits are read.

Any combination of read, write, or read-modify-write operations can be performed in the static column mode. The conditions normal to each operation apply when the device is operated in this mode.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refreshing available on the MCM514258A offers an alternate refresh method. If $\overline{CS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM514258A is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CS}$ before $\overline{RAS}$ refresh counter test.** This refresh counter test is performed with a read-write operation. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 512 test cycles, as indicated by the check data written in each row. See **$\overline{CS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows.

1. Write a "0"s into all memory cells (normal write mode).
2. Select a column address, read "0" out and write "1" into the cell by performing **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
3. Read "1"s (normal read mode), which were written at step 2.
4. Using the same column as in step 2, read "1" out and write "0" into the cell by performing **$\overline{CS}$ before $\overline{RAS}$ refresh counter test, read-write cycle.** Repeat this operation 512 times.
5. Read "0"s (normal read mode), which were written at step 4.
6. Repeat steps 1 to 5 using complement data.

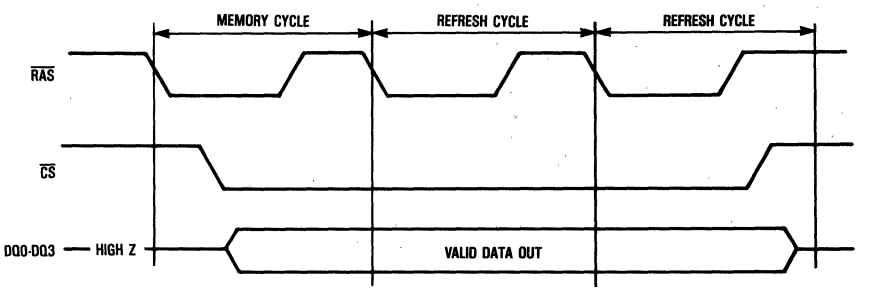
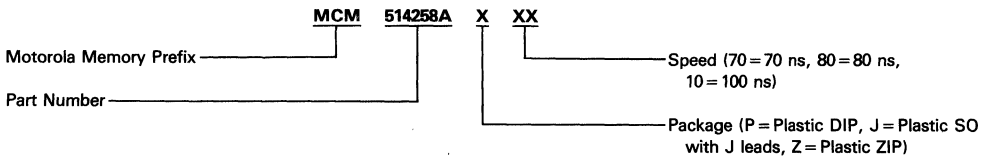


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)



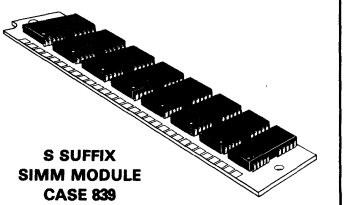
Full Part Numbers—	MCM514258AP70	MCM514258AJ70	MCM514258AZ70
	MCM514258AP80	MCM514258AJ80	MCM514258AZ80
	MCM514258AP10	MCM514258AJ10	MCM514258AZ10

2

MCM81000

Product Preview

1M x 8 Bit Dynamic Random Access Memory Module

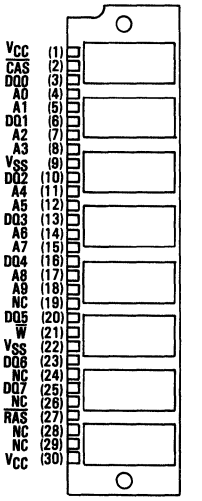


S SUFFIX
SIMM MODULE
CASE 839

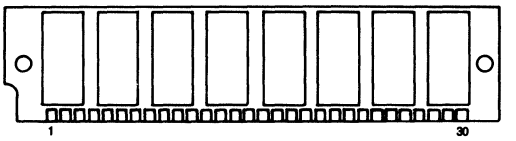
The MCM81000L and MCM81000S are 8M, dynamic random access memory (DRAM) modules organized as 1,048,576 x 8 bits. The modules are 30-lead single-in-line memory modules (SIMM) or 30-pin single-in-line packages (SIP) consisting of eight MCM511000 DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 μF decoupling capacitor mounted under each DRAM. The MCM511000 is a 1.0μ CMOS high speed, dynamic random access memory organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Consists of Eight 1M DRAMs and Eight 0.22 μF Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM81000-80 = 80 ns (Max)
  - MCM81000-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM81000-80 = 3.0 W (Max)
  - MCM81000-10 = 2.6 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 88 mW (Max)
  - CMOS Levels = 44 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- Available in Edge Connector (MCM81000S) or Pin Connector (MCM81000L)

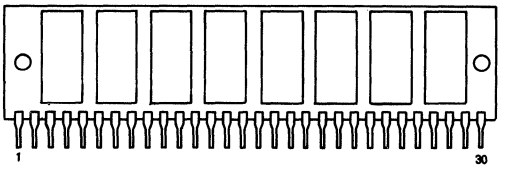
30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM81000S)



MCM81000S (SIMM)



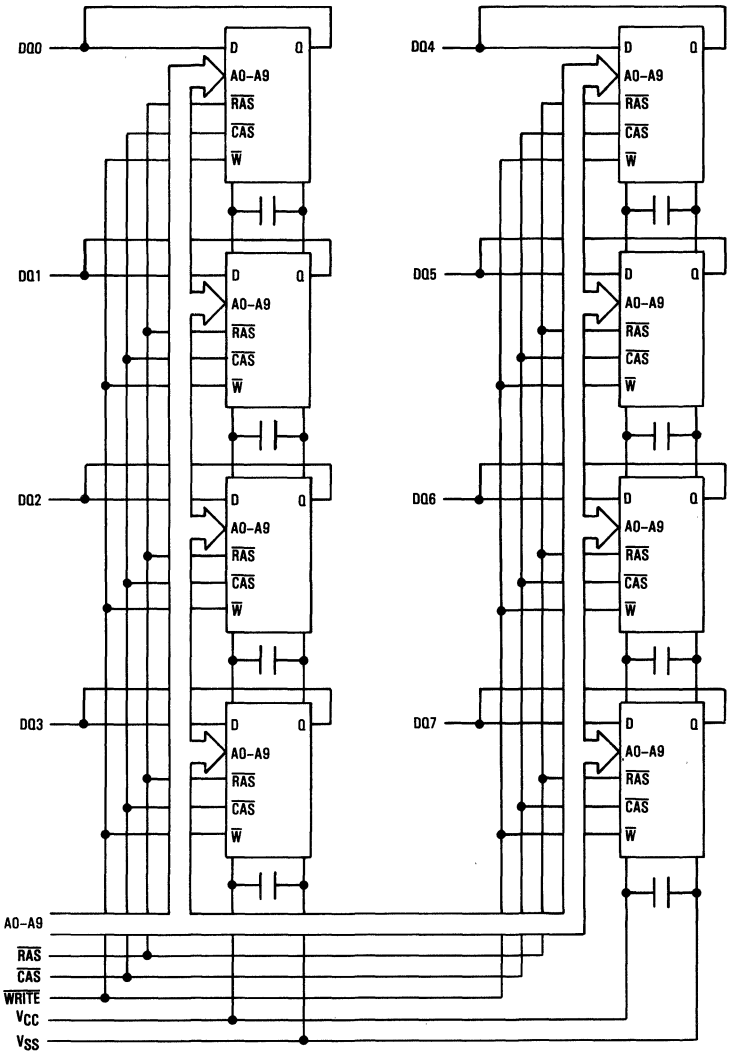
MCM81000L (SIP)



PIN NAMES	
A0-A9	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL BLOCK DIAGRAM

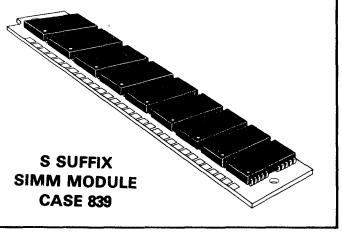


2

MCM91000

Product Preview

1M x 9 Bit Dynamic Random Access Memory Module

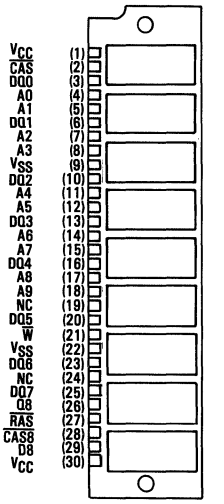


S SUFFIX
SIMM MODULE
CASE 839

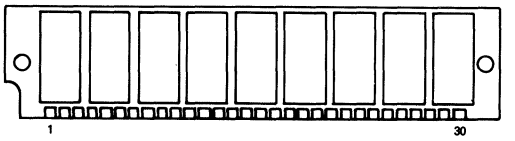
The MCM91000L and MCM91000S are 9M, dynamic random access memory (DRAM) modules organized as 1,048,576 x 9 bits. The modules are 30-lead single-in-line memory modules (SIMM) or 30-pin single-in-line packages (SIP) consisting of nine MCM511000 DRAMs housed in a 20/26 J-lead small outline package (SOJ) and mounted on a substrate along with a 0.22 μF decoupling capacitor mounted under each DRAM. The MCM511000 is a 1.0μ CMOS high speed, dynamic random access memory organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Consists of Nine 1M DRAMs and Nine 0.22 μF Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}):
  - MCM91000-80 = 80 ns (Max)
  - MCM91000-10 = 100 ns (Max)
- Low Active Power Dissipation:
  - MCM91000-80 = 3.5 W (Max)
  - MCM91000-10 = 3.0 W (Max)
- Low Standby Power Dissipation:
  - TTL Levels = 99 mW (Max)
  - CMOS Levels = 50 mW (Max)
- $\overline{CAS}$ Control for Eight Common I/O Lines
- $\overline{CAS}$ Control for Separate I/O Pair
- Available in Edge Connector (MCM91000S) or Pin Connector (MCM91000L)

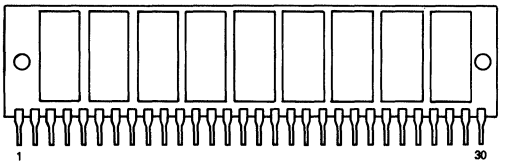
30-PIN
SINGLE IN-LINE PACKAGE
(TOP VIEW, MCM91000S)



MCM91000S (SIMM)



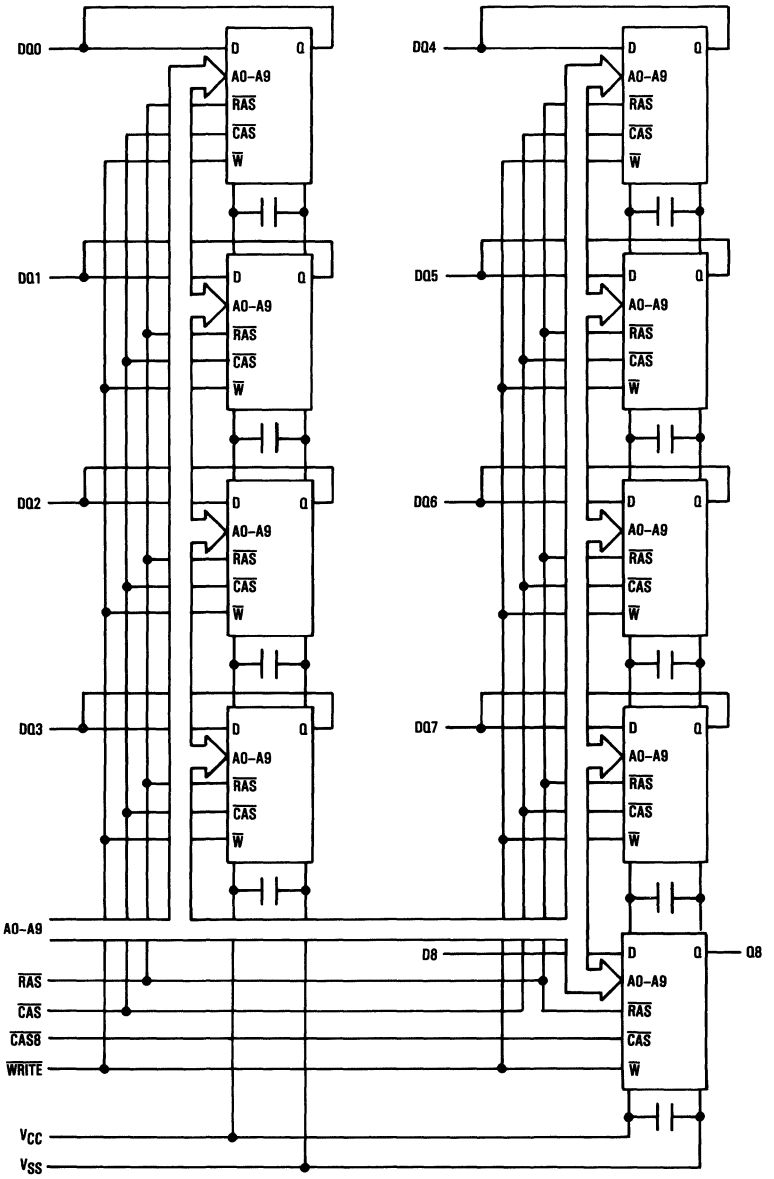
MCM91000L (SIP)



PIN NAMES	
A0-A9	Address Inputs
DQ0-DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL BLOCK DIAGRAM



General MOS Static RAMs 3

3

MOS Static RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
2K×8	MCM2018AN35	35	24
	MCM2018AN45	45	24

CMOS Static RAMs

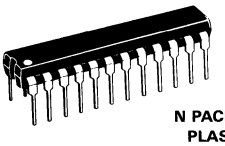
(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
8K×8	MCM6064P10	100	28
	MCM6064P12	120	28
	MCM60L64P10	100	28
	MCM60L64P12	120	28
32K×8	MCM60256AP85	85	28
	MCM60256AP10	100	28
	MCM60256AP12	120	28
	MCM60L256AP85	85	28
	MCM60L256AP10	100	28
	MCM60L256AP12	120	28
	MCM60256APC10 (2)	100	24

(2) Industrial temperature range, −40 to 85°C

MCM2018A

Fast 16K Bit Static RAM



N PACKAGE
PLASTIC
CASE 724

3

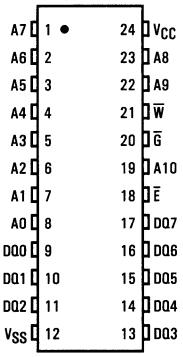
The MCM2018A is a 16,384 bit static random access memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings.

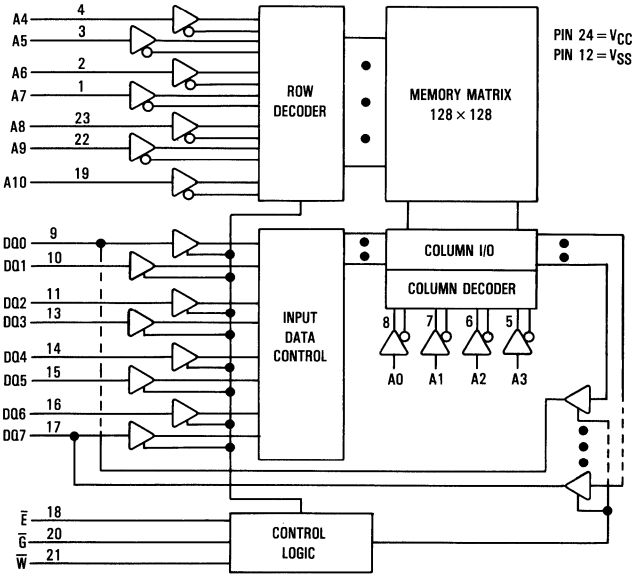
The MCM2018A is in a 24-pin dual-in-line 300 mil wide package with the industry standard JEDEC approved pinout.

- Single +5 V Operation, ±10%
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2018A-35 = 35 ns (Maximum)
  MCM2018A-45 = 45 ns (Maximum)
- Power Supply Current: 135 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

3

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle	L	X	L	I_{CC}	D

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin With Respect to V_{SS}	V_{in}, V_{out}	−0.5 to +7.0	V
DC Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.1	Watt
Temperature Under Bias	T_{bias}	−10 to +80	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$I_{lkg(I)}$	−1.0	1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC})	$I_{lkg(O)}$	−1.0	1.0	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC}	—	135	mA
Standby Power Supply Current ($\overline{E}$ = V_{IH})	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ and DQ	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

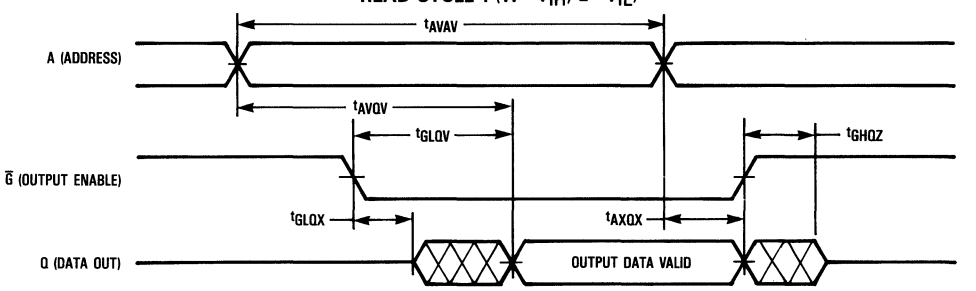
Input Pulse Levels . . . . . 0 and 3.0 V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Measurement Reference Levels . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

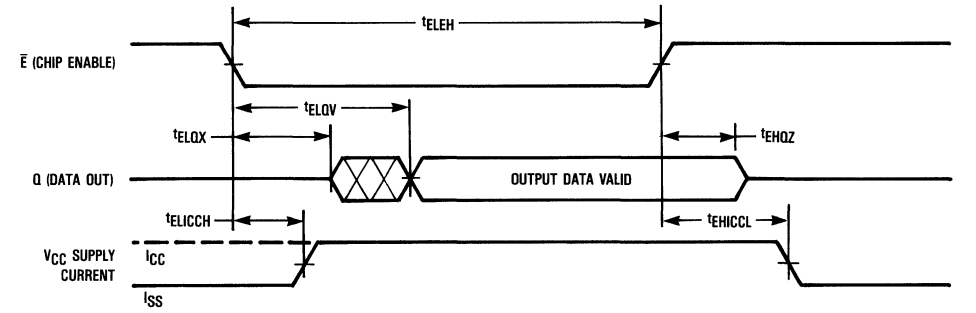
Parameter	Symbol		MCM2018A-35		MCM2018A-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	35	–	45	–	ns	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AC}	–	35	–	45	ns	
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	35	–	45	–	ns	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	35	–	45	ns	
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	–	20	–	20	ns	
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{CLZ}	5	–	5	–	ns	2
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{CHZ}	0	20	0	20	ns	2
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2
Output Enable High to Output High Z (Output Disable to Output Disable)	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	20	–	20	ns	

NOTES:
1. Transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
2. Transition is measured ±200 mV from the steady state output voltage with the output loading specified in Figure 1.
3. In read cycle 2, all addresses are valid prior to or coincident with chip enable ($\overline{E}$) transition low.

READ CYCLE 1 ($\overline{W}=V_{IH}$, $\overline{E}=V_{IL}$)



READ CYCLE 2 ($\overline{W}=V_{IH}$, $\overline{G}=V_{IL}$; See Note 3 Above)

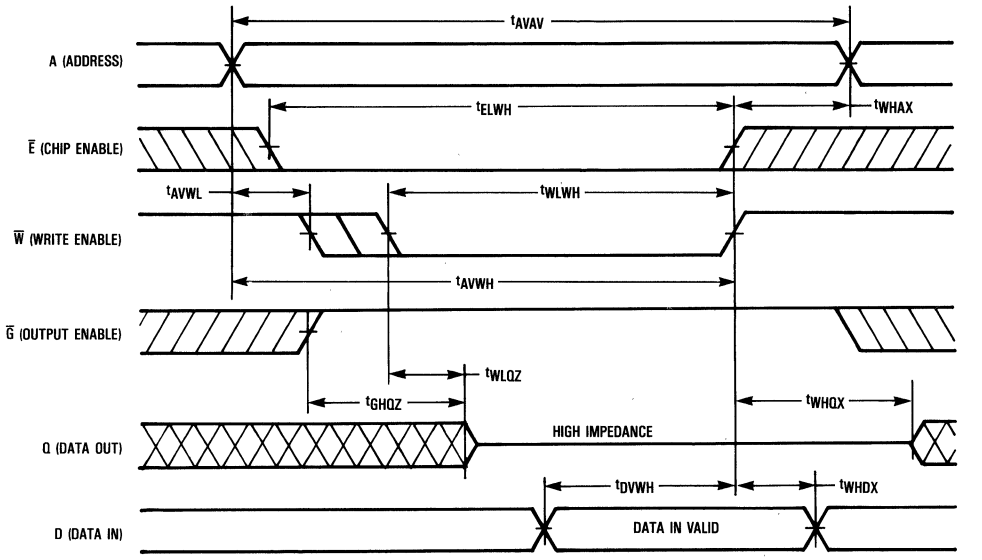


WRITE CYCLE (See Notes 1 and 2)

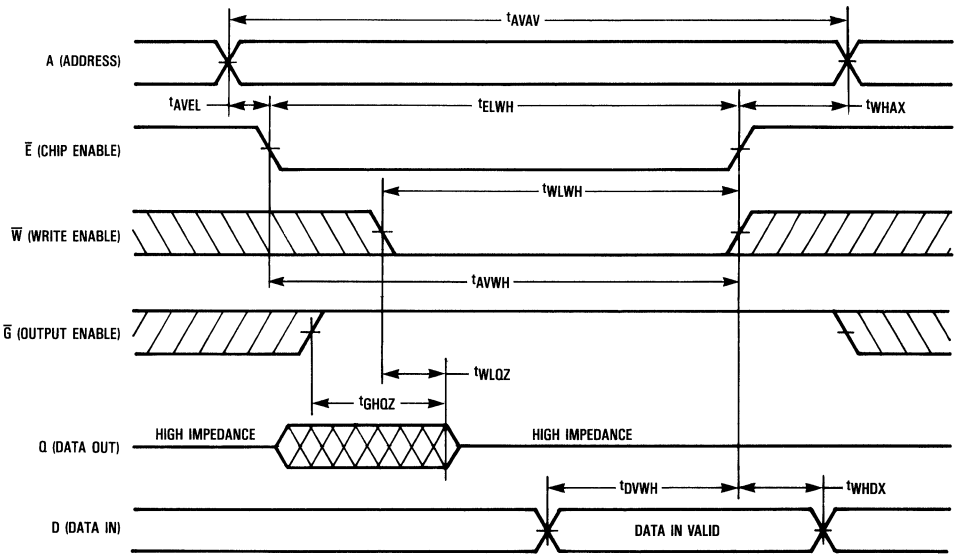
Parameter	Symbol		MCM2018A-35		MCM2018A-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	—	45	—	ns	
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	30	—	40	—	ns	
Address Valid to Chip Enable Low (Address Setup to Chip Enable)	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to Write Low (Address Setup to Write)	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to Write High	t_{AVWH}	t_{AW}	30	—	40	—	ns	3
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	30	—	35	—	ns	
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	—	0	—	ns	4
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{WLZ}	0	—	0	—	ns	5
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	5
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DS}	15	—	20	—	ns	3
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	—	0	—	ns	3, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	

NOTES:
1. Write enable ($\overline{W}$) must be high during all address transitions.
2. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
3. Both chip enable ($\overline{E}$) and write enable ($\overline{W}$) must be active (low) to write data into the memory. Either signal can terminate the write cycle by going high. Data in setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
4. t_{WHAX} is measured from the earlier of, chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
5. Output enable ($\overline{G}$) can be either low or high during a write cycle. If chip enable ($\overline{E}$) and $\overline{G}$ are both low during this period then the data input/output (DQ) pins are in the output state. Under these conditions input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



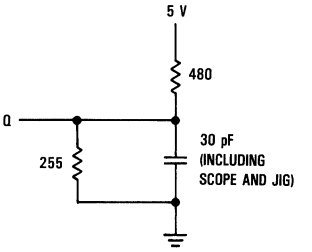
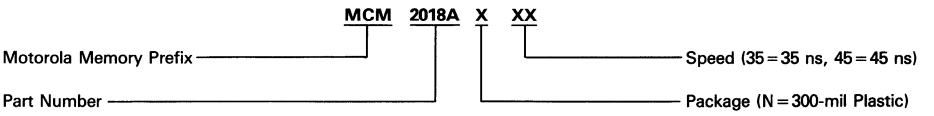


Figure 1. Output Load

ORDERING INFORMATION
(Order by Full Part Number)



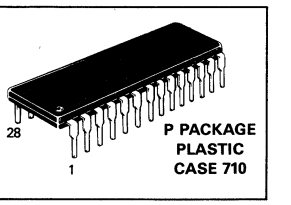
Full Part Numbers—MCM2018AN35
MCM2018AN45

MCM6064
MCM60L64

3

Advance Information

8K x 8 Bit CMOS Static Random Access Memory



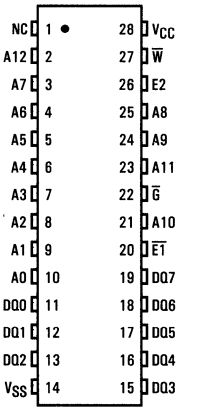
The MCM6064 is a 65,536 bit low-power static random access memory organized as 8192 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The maximum operating current is 5 mA/MHz and corresponding maximum power consumption is 27.5 mW/MHz.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. For MCM6064 typical standby current is 3 μA, with a maximum of 100 μA. For MCM60L64 typical standby current is 1 μA. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

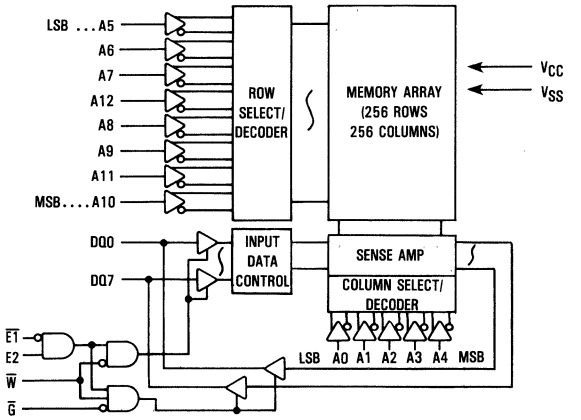
The MCM6064 is available in a 600 mil, 28 pin plastic dual-in-line package.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—248 mW (Maximum Active)
- Two Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L64)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Pin Compatible with 2764 EPROM Family
- Three State Outputs
- Fast Access Times:
  MCM6064-10 and MCM60L64-10 = 100 ns (Max)
  MCM6064-12 and MCM60L64-12 = 120 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

3

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC} + 0.5	V
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
DC Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL})	I_{CC}	–	–	10	mA
AC Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0) MCM6064-10: t_{AVAV} = 100 ns MCM6064-12: t_{AVAV} = 120 ns	I_{CCA}	 – –	 – –	 45 40	mA
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 or E2 ≤ 0.2 V) MCM6064 MCM60L64	I_{SB2}	– –	3 1	100 30	μA
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

CAPACITANCE (Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

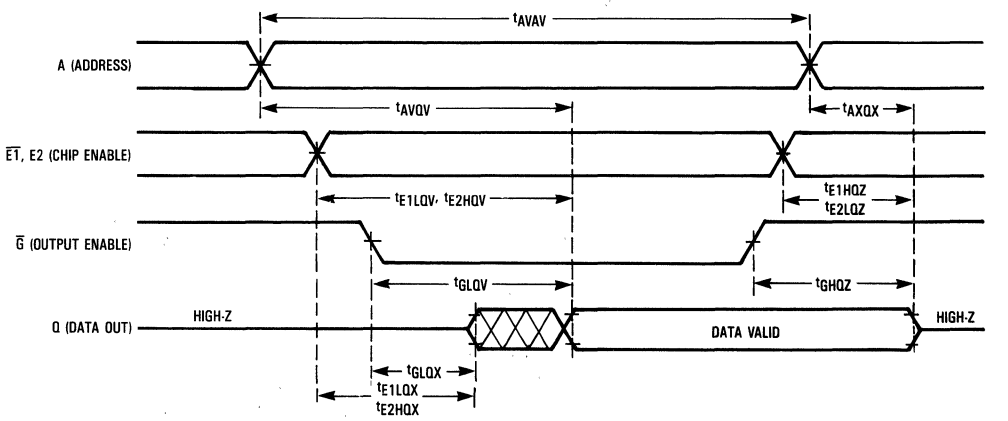
Input Pulse Levels	0.6 V, 2.4 V
Input Rise/Fall Time	5 ns
Input Timing Measurement Reference Levels	1.5 V
Output Timing Measurement Reference Levels	0.8 and 2.2 V
Output Load	See Figure 1

3

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	100	–	120	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	100	–	120	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	100	–	120	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	100	–	120	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	50	–	60	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	20	–	20	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	10	–	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	35	0	40	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	0	40	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



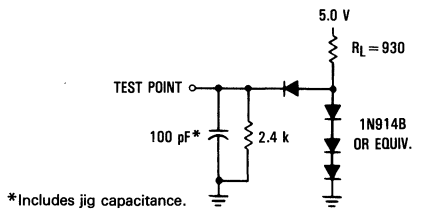
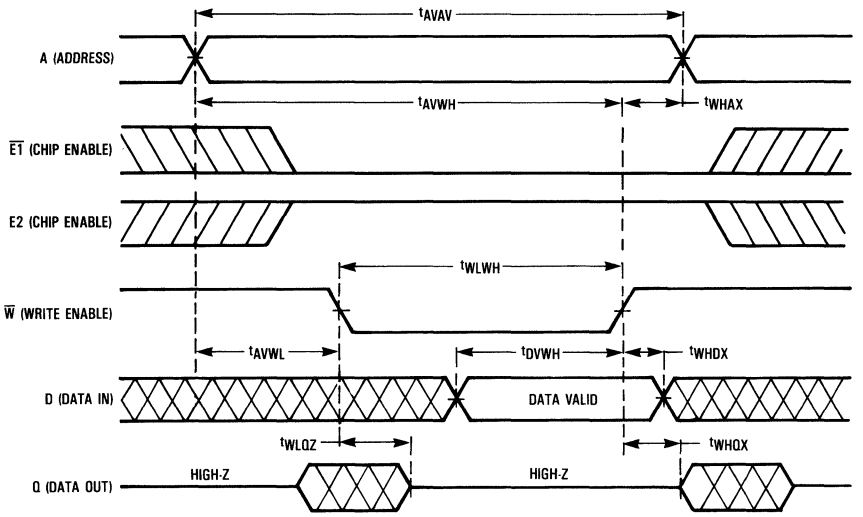


Figure 1. AC Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	120	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	80	–	85	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	40	–	50	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	35	0	40	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

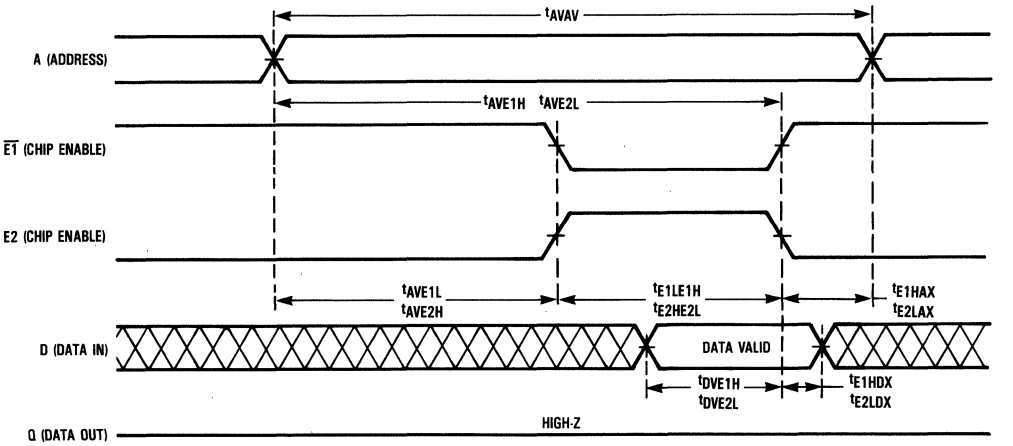
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.



WRITE CYCLE 2 ($\overline{E1}$, E2 CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	120	–	ns	–
Address Setup Time	t_{AVE1L}, t_{AVE2H}	t_{AS}	0	–	0	–	ns	2
Address Valid to End of Write	t_{AVE1H}, t_{AVE2L}	t_{AW}	80	–	85	–	ns	2
Chip Enable to End of Write	t_{E1LE1H}, t_{E2HE2L}	t_{CW}	80	–	85	–	ns	2, 3
Data Valid to End of Write	t_{DVE1H}, t_{DVE2L}	t_{DW}	40	–	50	–	ns	2
Data Hold Time	t_{E1HDX}, t_{E2LDX}	t_{DH}	0	–	0	–	ns	2, 4
Write Recovery Time	t_{E1HAX}, t_{E2LAX}	t_{WR}	0	–	0	–	ns	2, 5

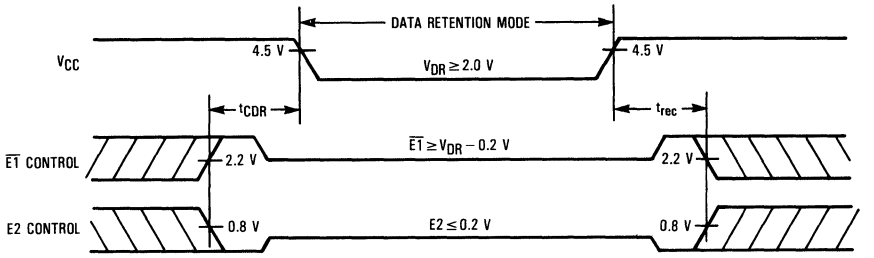
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{W}$ must be high during all address transitions.



DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V)	V_{DR}	2.0	—	5.5	V
Data Retention Current ($\overline{E1} \geq V_{CC} - 0.2$ or E2 ≤ 0.2 V)	I_{CCDR}				μA
MCM6064: V_{CC} = 3.0 V		—	—	50	
V_{CC} = 5.5 V		—	—	100	
MCM60L64: V_{CC} = 3.0 V		—	—	15	
V_{CC} = 5.5 V		—	—	30	
Chip Disable to Data Retention Time	t_{CDR}	0	—	—	ns
Operation Recovery Time	t_{rec}	t_{AVAV}*	—	—	ns

*t_{AVAV} = Read Cycle Time



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6064 or 60L64 X XX

Motorola Memory Prefix

Part Number
(With L = Low Power Version)

Speed (10 = 100 ns, 12 = 120 ns)

Package (P = Plastic)

Full Part Numbers — MCM6064P10 MCM60L64P10
MCM6064P12 MCM60L64P12

MCM60256A
MCM60L256A

3

Advance Information

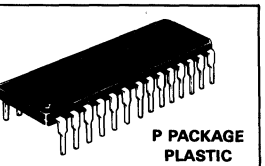
32K x 8 Bit CMOS Static Random Access Memory

The MCM60256A is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the minimum cycle time is 85 ns.

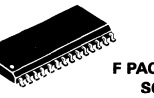
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current for MCM60L256A is 2 μA (T_A = 25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 45 ns (MCM60256A-85). Thus the MCM60256A is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The MCM60256A is offered in a 600 mil, 28 pin plastic dual-in-line package as well as the 330 mil, 28 pin plastic small outline gullwing package.

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L256A)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM60256A-85 and MCM60L256A-85 = 85 ns (Max)
  MCM60256A-10 and MCM60L256A-10 = 100 ns (Max)
  MCM60256A-12 and MCM60L256A-12 = 120 ns (Max)

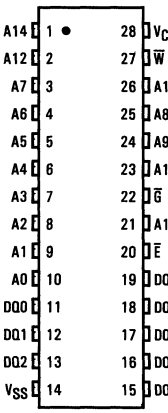


P PACKAGE
PLASTIC
CASE 710

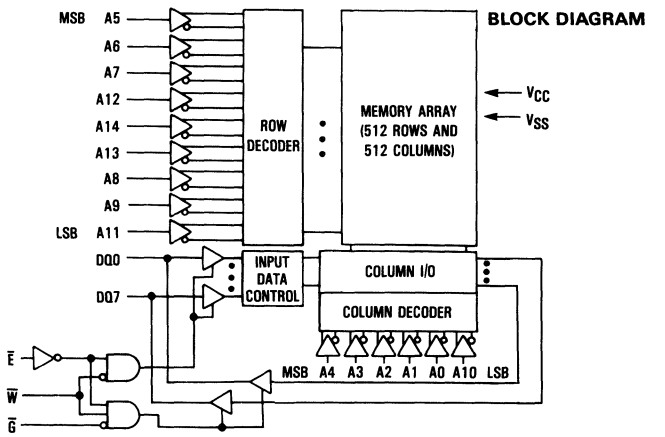


F PACKAGE
SOG
CASE 751H

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to 7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A=25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA)	I_{CCA1}				mA
MCM60256A, MCM60L256A: t_{AVAV} = 1 μs		–	10	–	
MCM60256A, MCM60L256A-85: t_{AVAV} = 85 ns		–	–	70	
MCM60256A, MCM60L256A-10: t_{AVAV} = 100 ns		–	–	70	
MCM60256A, MCM60L256A-12: t_{AVAV} = 120 ns		–	–	70	
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA)	I_{CCA2}				
MCM60256A, MCM60L256A: t_{AVAV} = 1 μs		–	5	–	
MCM60256A, MCM60L256A-85: t_{AVAV} = 85 ns		–	–	60	
MCM60256A, MCM60L256A-10: t_{AVAV} = 100 ns		–	–	60	
MCM60256A, MCM60L256A-12: t_{AVAV} = 120 ns		–	–	60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) MCM60256A	I_{SB2}	–	2	100	μA
MCM60L256A		–	–	30	
MCM60L256A (T_A = 25°C)		–	–	2	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	10	pF

3

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256A-85 MCM60L256A-85		MCM60256A-10 MCM60L256A-10		MCM60256A-12 MCM60L256A-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	85	—	100	—	120	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	85	—	100	—	120	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	85	—	100	—	120	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	45	—	50	—	60	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	10	—	10	—	ns	—
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	—	10	—	10	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	5	—	5	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	30	0	50	0	60	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	30	0	40	0	50	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

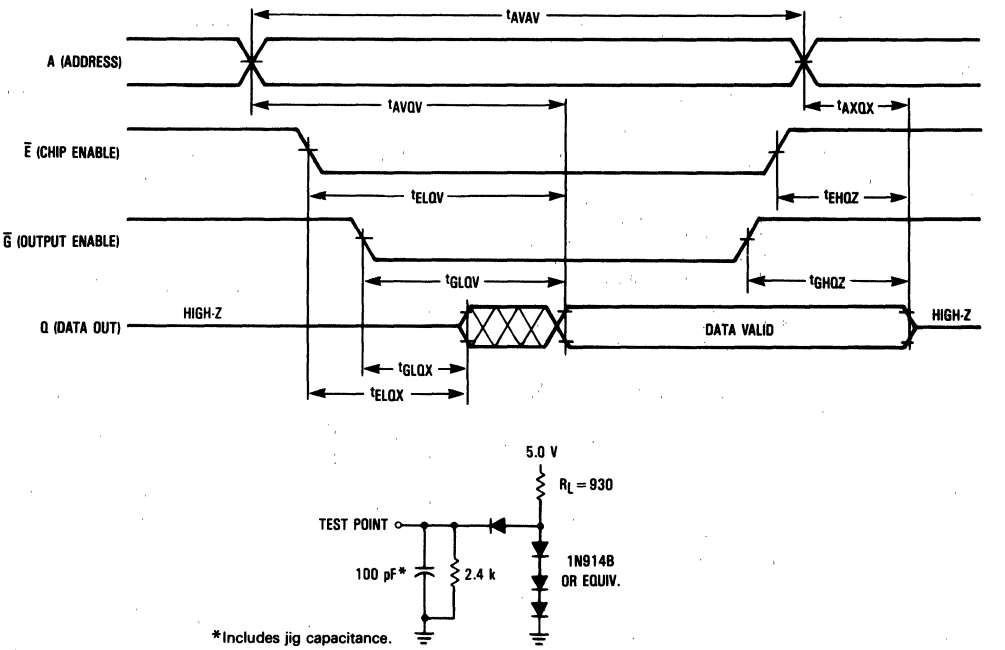


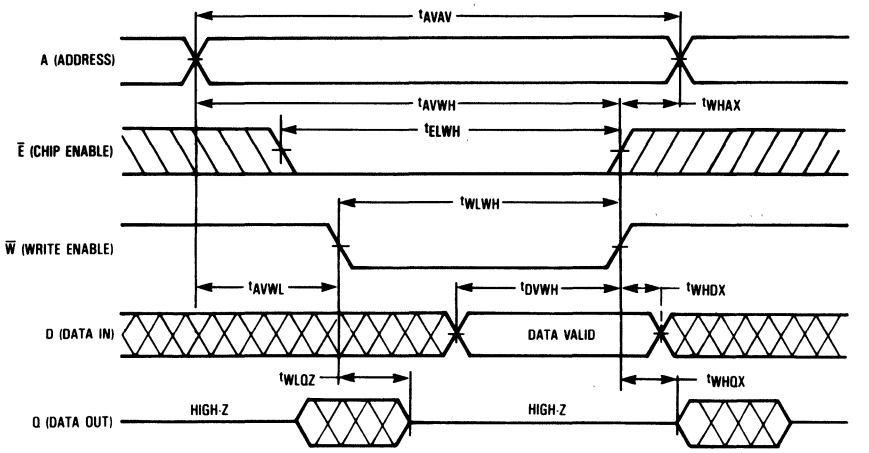
Figure 1. AC Test Load

WRITE CYCLE 1 AND 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256A-85 MCM60L256A-85		MCM60256A-10 MCM60L256A-10		MCM60256A-12 MCM60L256A-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	85	–	100	–	120	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	80	–	95	–	115	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	80	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	40	–	40	–	50	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	30	0	50	0	60	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	10	–	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	5	–	5	–	5	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	65	–	90	–	100	–	ns	–

NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



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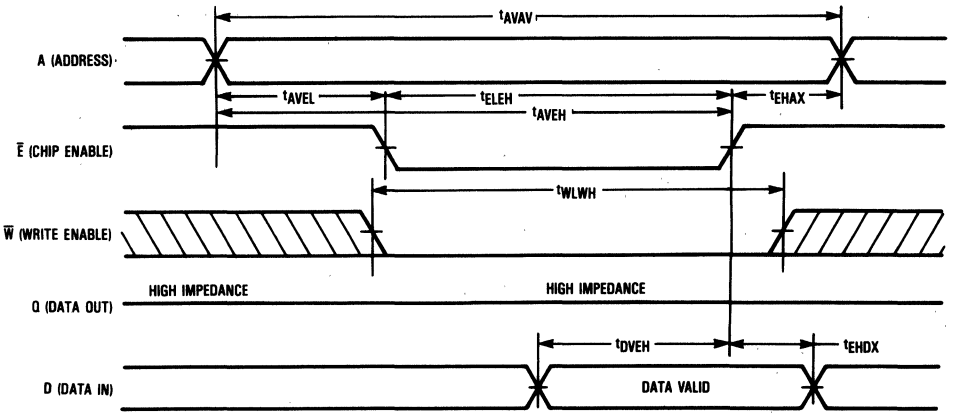
WRITE CYCLE 2 ($\overline{E}$ Controlled)

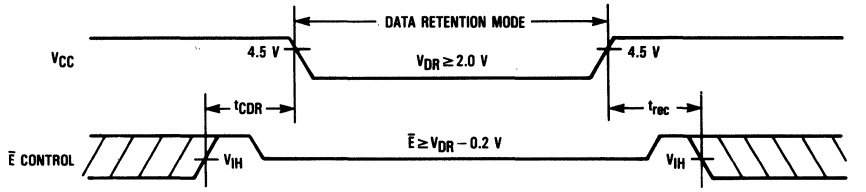


DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	MCM60256A : V_{CC} = 3.0 V	I_{CCDR}	–	–	50	μA
	V_{CC} = 5.5 V		–	–	100	
	MCM60L256A: V_{CC} = 3.0 V		–	–	20	
	V_{CC} = 5.5 V		–	–	30	
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

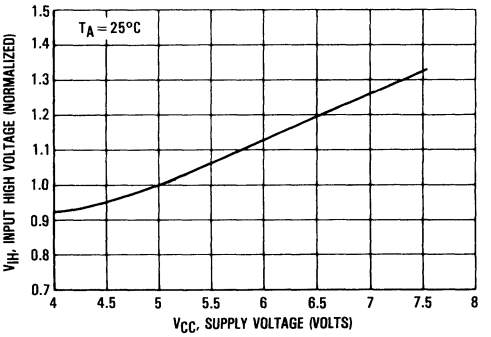


Figure 1. Input High Voltage versus Supply Voltage

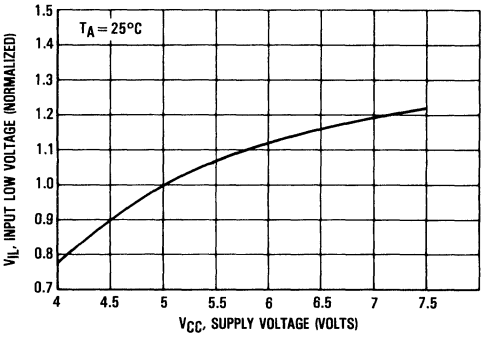


Figure 2. Input Low Voltage versus Supply Voltage

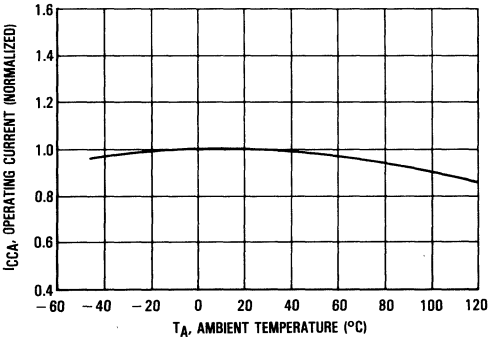


Figure 3. Operating Current versus Ambient Temperature

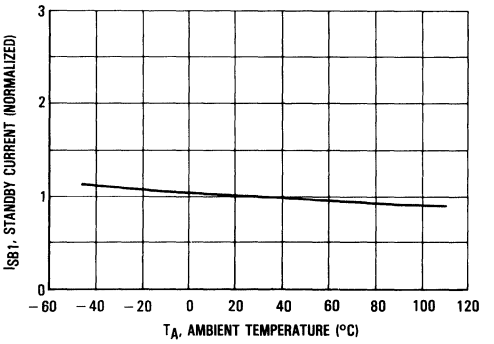


Figure 4. I_{SB1} Standby Current versus Ambient Temperature

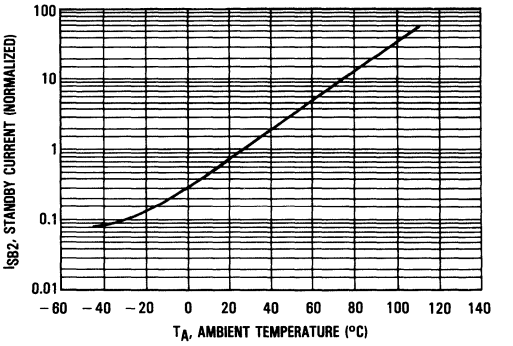


Figure 5. I_{SB2} Standby Current versus Ambient Temperature

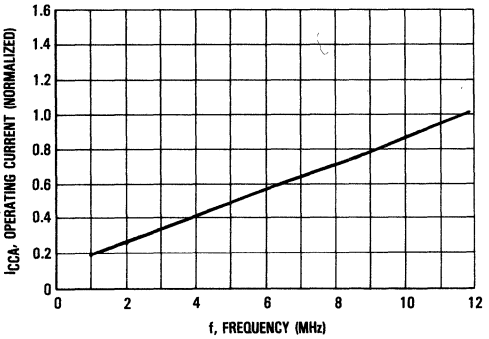


Figure 6. Operating Current versus Frequency (Read)

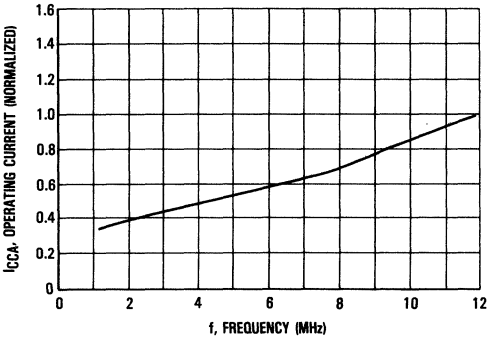


Figure 7. Operating Current versus Frequency (Write)

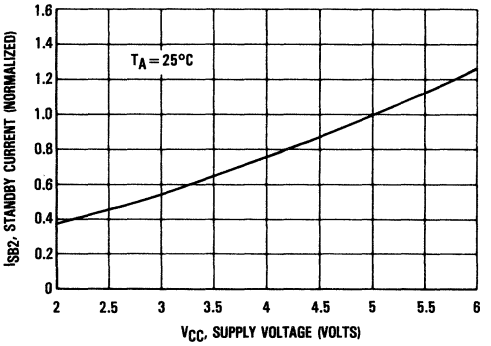


Figure 8. I_{SB2} Standby Current versus Supply Voltage

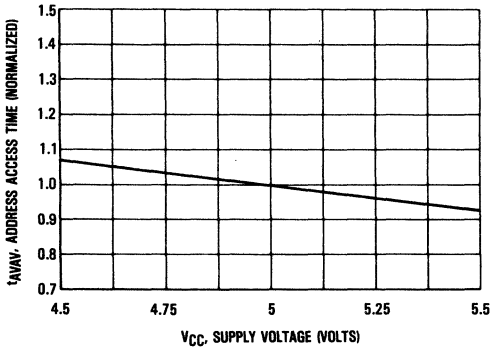


Figure 9. Access Time versus Supply Voltage

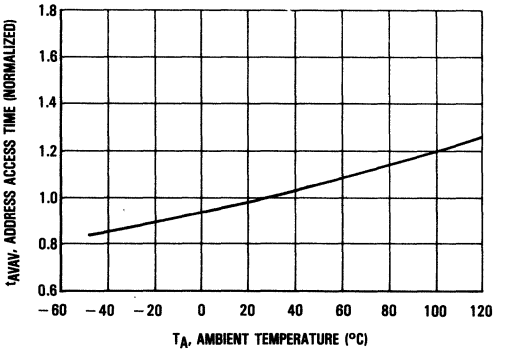
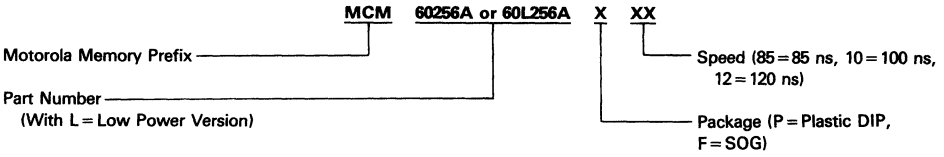


Figure 10. Access Time versus Ambient Temperature

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—		
	MCM60256AP85	MCM60L256AP85
	MCM60256AP10	MCM60L256AP10
	MCM60256AP12	MCM60L256AP12
	MCM60256AF85	MCM60L256AF85
	MCM60256AF10	MCM60L256AF10
	MCM60256AF12	MCM60L256AF12

3

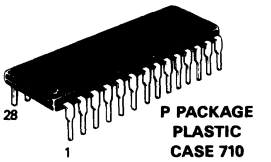
MCM60256APC

3

Advance Information

32K x 8 Bit CMOS Static Random Access Memory

Industrial Temperature Range: – 40 to 85°C



P PACKAGE
PLASTIC
CASE 710

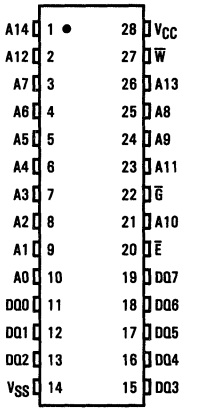
The MCM60256APC is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The maximum standby current is 2 μA (T_A = 25°C). Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 50 ns. Thus the MCM60256APC is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

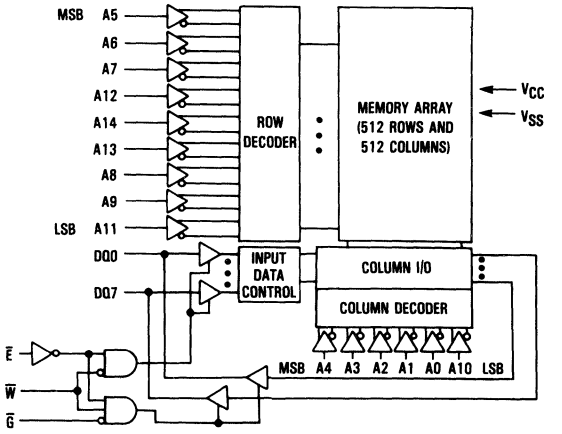
The MCM60256APC is offered in a 600 mil, 28 pin plastic dual-in-line package.

- Single 5 V Supply, ±10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current = 2 μA @ 25°C)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60256APC10 = 100 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to charige without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

3

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to 7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	−40 to 85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA) t_{AVQV} = 1 μs t_{AVQV} = 100 ns	I_{CCA1}	– –	10 –	– 70	mA
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA) t_{AVQV} = 1 μs t_{AVQV} = 100 ns	I_{CCA2}	– –	5 –	– 60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) (T_A = 25°C)	I_{SB2}	– –	2 –	100 2	μA
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	–	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	–	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

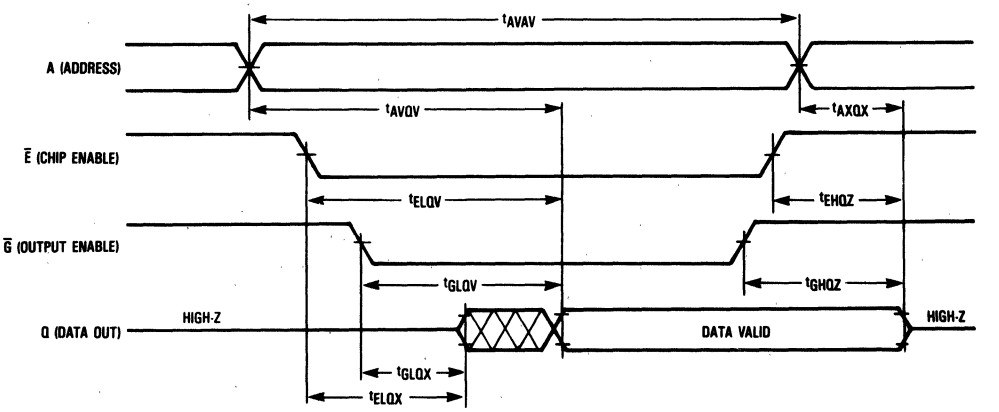
Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

3

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	t_{AVAV}	t_{RC}	100	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	100	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	100	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	50	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	10	–	ns	–
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	50	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	40	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



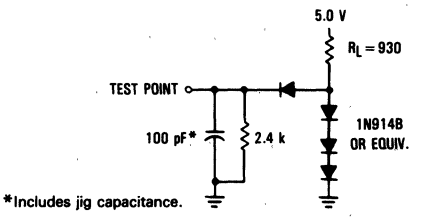


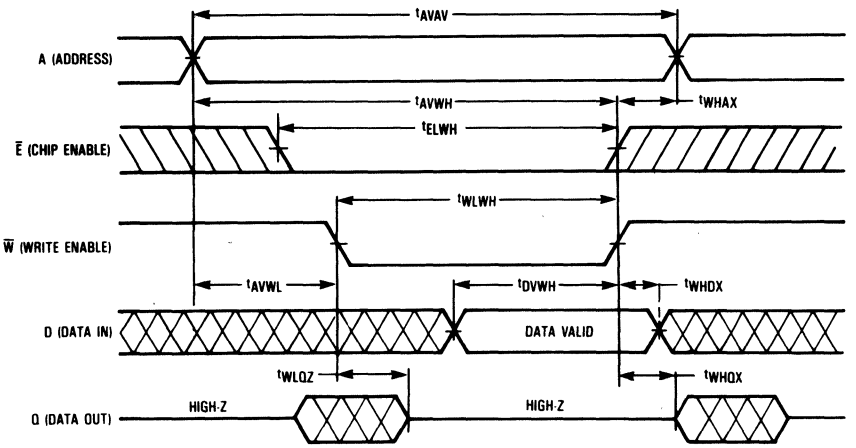
Figure 1. AC Test Load

WRITE CYCLE 1 AND 2 (See Note 1)

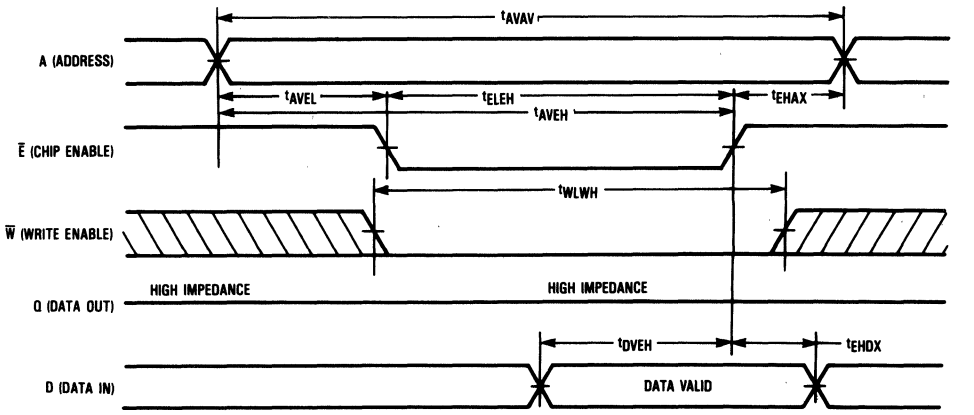
Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	100	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	95	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	70	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	40	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHDX}	t_{DH}	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	50	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	5	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	90	–	ns	–

NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ Controlled)

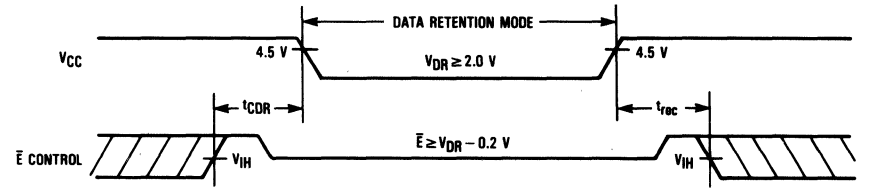


DATA RETENTION CHARACTERISTICS (T_A = −40 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	V_{CC} = 3.0 V V_{CC} = 5.5 V	I_{CCDR}	– –	– –	50 100	μA
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

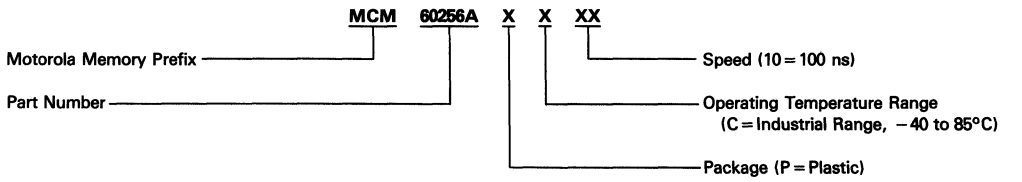
*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number—MCM60256APC10

CMOS Fast Static RAMs

4

CMOS Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
4K × 4	MCM1423P45	40	20
	IMS1423P-45	40	20
	MCM6168P45	45	20
	MCM6168P55	55	20
	MCM6168P70	70	20
	MCM6268P20	20	20
	MCM6268P25	25	20
	MCM6268P35	35	20
	MCM6268P45	45	20
	MCM6268P55	55	20
	MCM6269P25 (1)	25	20
	MCM6269P35 (1)	35	20
	MCM6270P20	20	22
	MCM6270P25	25	22
	MCM6270P35	35	22
	MCM6270J20	20	24
	MCM6270J25	25	24
	MCM6270J35	35	24
8K × 8	MCM6164C45	45	28
	MCM6164C55	55	28
	MCM61L64C45	45	28
	MCM61L64C55	55	28
	MCM6164CC55 (2)	55	28
	MCM6164CC70 (2)	70	28
	MCM6264P25*	25	28
	MCM6264P30	30	28
	MCM6264P35	35	28
	MCM6264P45	45	28
	MCM6264P55	55	28
	MCM6264J25*	25	28
	MCM6264J30	30	28
	MCM6264J35	35	28
	MCM6264J45	35	28
	MCM6264J55	55	28
16K × 4	MCM6288P15*	15	22
	MCM6288P20*	20	22
	MCM6288P25	25	22
	MCM6288P30	30	22
	MCM6288P35	35	22
	MCM6288P45	45	22
	MCM6290P15* (3)	15	24
	MCM6290P20* (3)	20	24
	MCM6290P25 (3)	25	24
	MCM6290P30 (3)	30	24
	MCM6290P35 (3)	35	24
	MCM6290P45 (3)	45	24
	MCM6290J15* (3)	15	24
	MCM6290J20* (3)	20	24
	MCM6290J25 (3)	25	24
	MCM6290J30 (3)	30	24
	MCM6290J35 (3)	35	24
	MCM6290J45 (3)	45	24

Organization	Part Number	Access Time (ns max)	Pins
64K × 1	MCM6287P15	15	22
	MCM6287P20	20	22
	MCM6287P25	25	22
	MCM6287P35	35	22
	MCM6287J15	15	24
	MCM6287J20	20	24
	MCM6287J25	25	24
	MCM6287J35	35	24
32K × 8	MCM6206P20*	20	28
	MCM6206P25*	25	28
	MCM6206P35*	35	28
	MCM6206P45*	45	28
	MCM6206J20*	20	28
	MCM6206J25*	25	28
	MCM6206J35*	35	28
	MCM6206J45*	45	28
32K × 9	MCM6205P20*	20	32
	MCM6205P25*	25	32
	MCM6205J20*	20	32
	MCM6205J25*	25	32
64K × 4	MCM6208P20*	20	24
	MCM6208P25*	25	24
	MCM6208J20*	20	24
	MCM6208J25*	25	24
	MCM6209P20*	20	28
	MCM6209P25*	25	28
	MCM6209J20*	20	28
	MCM6209J25*	25	28
256K × 1	MCM6207P20*	20	24
	MCM6207P25*	25	24
	MCM6207J20*	20	24
	MCM6207J25*	25	24
128K × 8	MCM6226P30*	30	32
	MCM6226J30*	30	32
256K × 4	MCM6228P25*	25	28
	MCM6228J25*	25	28

*To be introduced
(1) Fast chip select version
(2) Industrial temperature range, −40 to 85°C
(3) Output enable version

MCM1423*

4K x 4 Bit Static Random Access Memory

The MCM1423 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption, provides greater reliability, and provides protection against soft errors caused by alpha particles. Fast access time makes this device suitable for cache and other sub-50 ns applications, especially those requiring just a little faster address access time (40 ns).

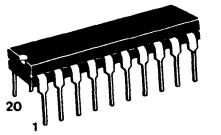
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access performance.

The MCM1423 is available in a 300 mil, 20 pin plastic dual in-line package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Protects Against Soft Errors Caused by Alpha Particles
- Fast Access Time (Maximum):

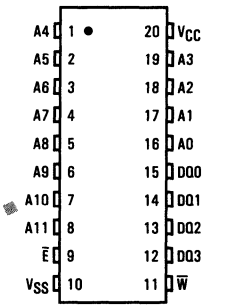
Address	Chip Enable
40 ns	45 ns

- Low Power Operation: 80 mA Max (Active)
  20 mA Max (Standby—TTL Levels)
  2 mA Max (Standby—Full Rail)

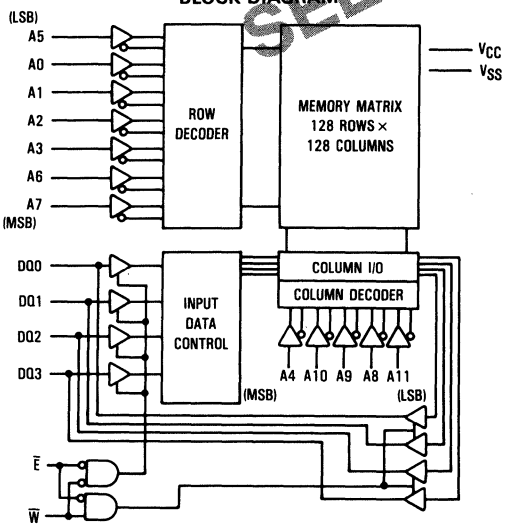


P PACKAGE
PLASTIC
CASE 738

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

*This device may also be ordered as IMS1423P-45.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	Not Selected	I_{SB}	High-Z
L	H	Read	I_{CC}	D_{out}
L	L	Write	I_{CC}	D_{in}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Power Supply Voltage (V_{CC})	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	±20	mA
Power Dissipation	1.0	W
Operating Temperature	0 to +70	°C
Storage Temperature	−55 to +125	°C
Temperature Under Bias	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage (See note below)	V_{IH}	2.0	–	V_{CC} + 0.3 V	V
Input Low Voltage (See note below)	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

NOTE: Address rise and fall times while the chip is selected are 50 ns maximum.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to 5.5 V)	I_{IL}	–	–	1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{W}$ = V_{IL}; V_{out} = 0 to V_{CC})**	I_{OL}	–	–	2.0	μA
Power Supply Current ($\overline{E}$ = V_{IL}; V_{in} = V_{IL} or V_{IH}, I_{out} = 0 mA)**	I_{CC}	–	–	80	mA
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	–	–	20	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V) (0.2 V ≥ V_{in} ≥ V_{CC} − 0.2 V)	I_{SB2}	–	–	2	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	–	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	–	–	V

**Input levels less than −0.3 V or greater than V_{CC} + 0.3 V will cause I/O and power supply currents to exceed maximum rating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	–	3	5	pF
	$\overline{E}$		–	5	7	
I/O Capacitance		$C_{I/O}$	–	5	7	pF

AC TEST LOADS

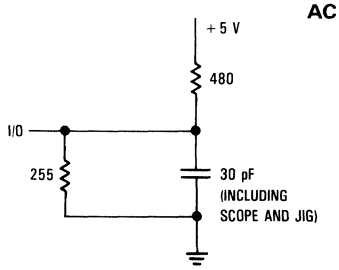


Figure 1A

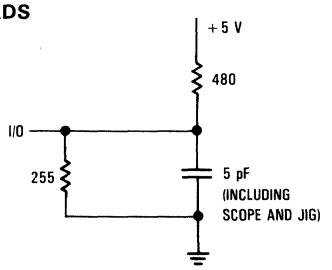


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

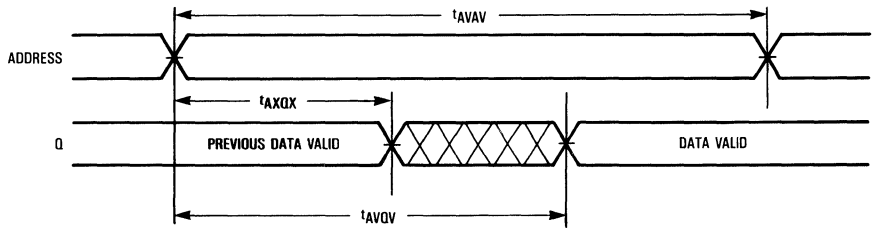
(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Mesurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

READ CYCLE 1 ($\overline{E} = V_{IL}$)

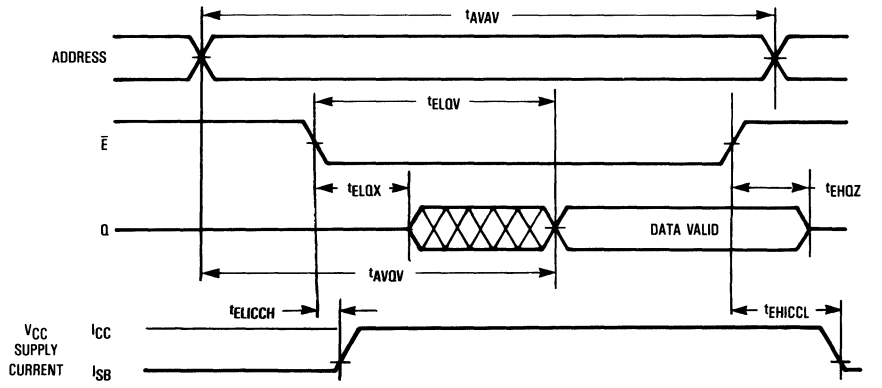
Parameter	Symbol		MCM1423P45		Unit
	Standard	Alternate	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	40	—	ns
Address Access Time	t_{AVQV}	t_{AA}	—	40	ns
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	ns



READ CYCLE 2 ($\overline{E}$ is Clocked)

Parameter	Symbol		MCM1423P45		Unit	Notes
	Standard	Alternate	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	40	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	40	ns	
$\overline{E}$ Access Time	t_{ELQV}	t_{ACS}	—	45	ns	
$\overline{E}$ Low to Output Active	t_{ELQX}	t_{LZ}	5	—	ns	1
$\overline{E}$ High to Output High-Z	t_{EHQZ}	t_{HZ}	0	20	ns	1
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	ns	
Power Up Time	t_{ELICCH}	t_{PU}	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	45	ns	

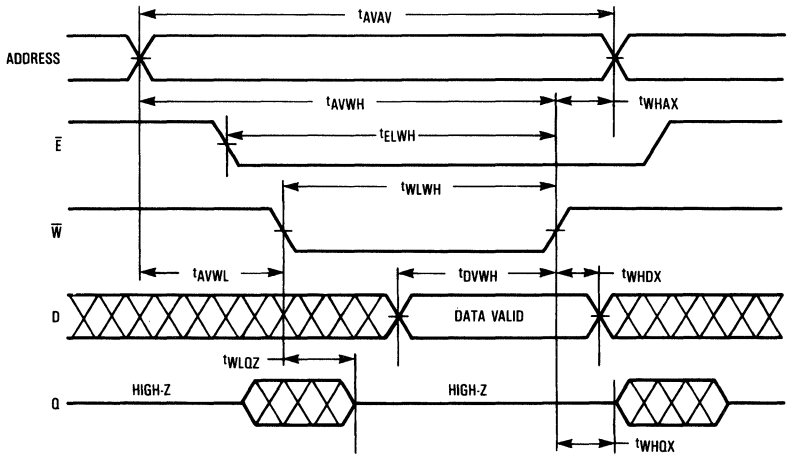
NOTE:
1. Measured with ac load of Figure 1B. Parameter is sampled and not 100% tested. Transition measured ±500 mV from steady-state voltage.



WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Note 1)

Parameter	Symbol		MCM1423P45		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	40	–	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	35	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	5	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	20	ns	2, 3
Write High to Output Active	t_{WHQX}	t_{OW}	6	–	ns	2, 3
Write Recovery Time	t_{WHAX}	t_{WR}	5	–	ns	
$\overline{E}$ Low to End of Write	t_{ELWH}	t_{CW}	35	–	ns	

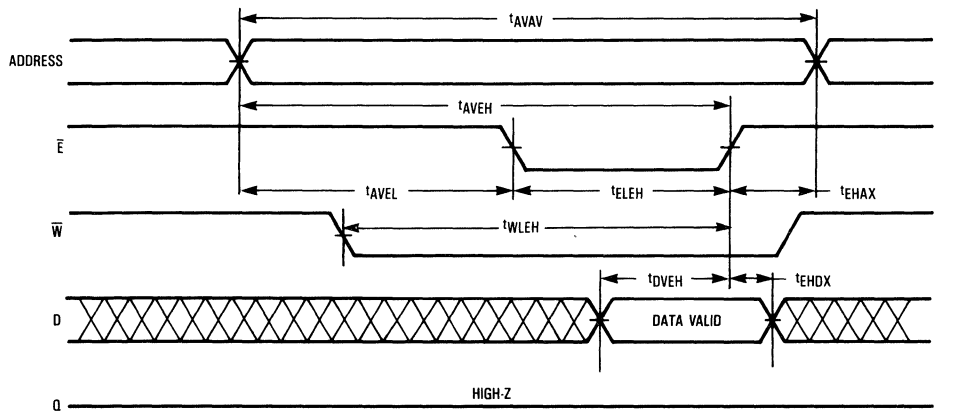
NOTES:
1. A Write occurs during the overlap of a low $\overline{W}$ and a low $\overline{E}$.
2. Measured with the ac load of Figure 1B. Parameter is sampled and not 100% tested. Transition measured ±500 mV from steady-state voltage.
3. When the outputs are active, data of opposite logic level to an output must not be applied.



WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Note 1)

Parameter	Symbol		MCM1423P45		Unit
	Standard	Alternate	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	40	—	ns
Address Setup Time	t_{AVEL}	t_{AS}	0	—	ns
Address Valid to End of Write	t_{AVEH}	t_{AW}	35	—	ns
Write Pulse Width	t_{ELEH}	t_{EW}	35	—	ns
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	ns
Data Hold Time	t_{EHDX}	t_{DH}	5	—	ns
Write Recovery Time	t_{EHAX}	t_{WR}	5	—	ns
Write Low to End of Write	t_{WLEH}	t_{WP}	35	—	ns

NOTE:
1. If $\overline{E}$ goes low coincident with or after $\overline{W}$ low, and $\overline{E}$ goes high before or coincident with $\overline{W}$ high, the I/O will remain in a high impedance condition.



TIMING PARAMETER ABBREVIATIONS

t X X X X

- signal name from which interval is defined
- transition direction for first signal
- signal name to which interval is defined
- transition direction for second signal

The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

ORDERING INFORMATION
(Order by Full Part Number)

MCM 1423 X XX

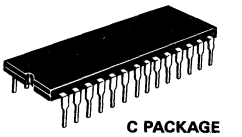
- MCM — Motorola Memory Prefix
- 1423 — Part Number
- X — Package (P = Plastic DIP)
- XX — Speed (45 = 45 ns)

Full Part Number — MCM1423P45

NOTE: This device may also be ordered as IMS1423P-45.

MCM6164
MCM61L64

8K x 8 Bit Fast Static Random Access Memory



C PACKAGE
CERAMIC
CASE 733

4

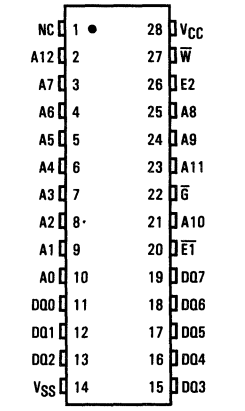
The MCM6164/MCM61L64 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

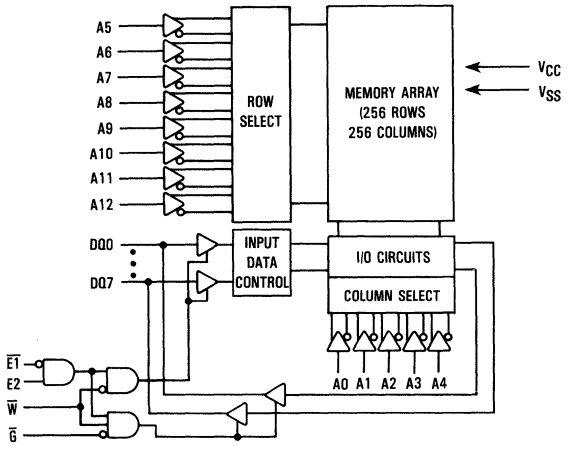
The MCM6164/MCM61L64 is available in a 600 mil, 28 pin ceramic dual-in-line package, with JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 45, 55 ns (Maximum)
- Low Power Dissipation — 495, 440 mW (Maximum, Active)
- Low Power/Data Retention Version (MCM61L64)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Industrial Temperature Range (−40 to 85°C) as MCM6164C

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	<0.01	±1.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0)	t_{AVAV} = 45 ns	I_{CC}	–	50	90	mA
	t_{AVAV} = 55 ns		–	40	80	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	–	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)	MCM6164	I_{SB2}	–	–	1.0	mA
	MCM61L64		–	5	50	μA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	3.0	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

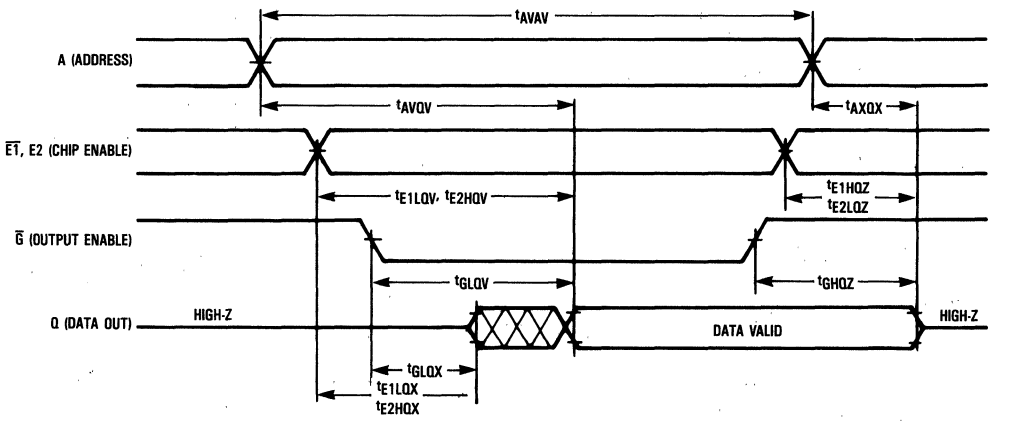
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

READ CYCLE (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	–	55	–	ns	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	45	–	55	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	45	–	55	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	45	–	55	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	20	–	25	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

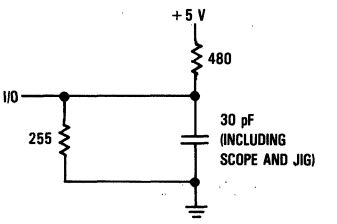
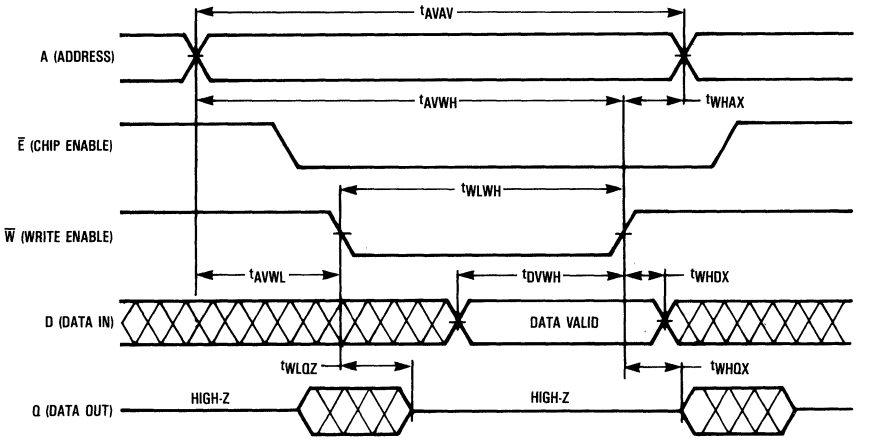


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	–	50	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	30	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.



TYPICAL CHARACTERISTICS

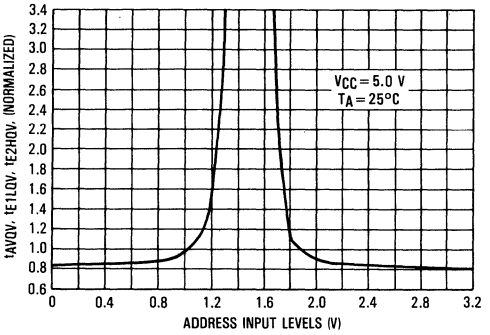
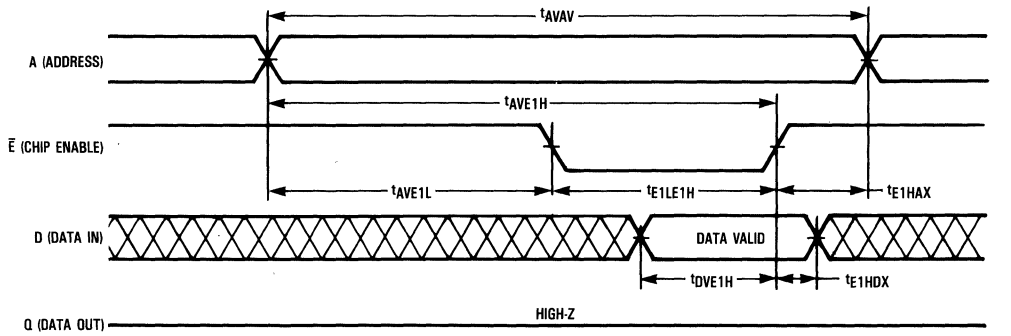


Figure 2. Access Time Versus Address Input Levels

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVE1H}	t_{AW}	40	–	50	–	ns	–
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	40	–	50	–	ns	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	ns	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	ns	–

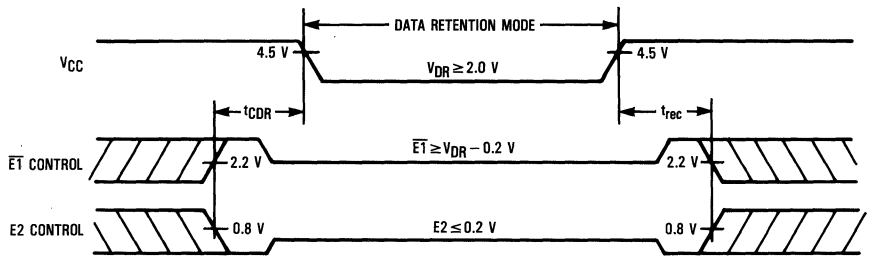
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L64 Only)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V, $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V)	V_{DR}	2.0	1.0	7.0	V
Data Retention Current (V_{CC} = 3.0 V, $\overline{E1} \geq 2.8$ V or E2 ≤ 0.2 V, $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V)	I_{CCDR}	–	10	30	μA
Chip Disable to Data Retention Time (see waveform below)	t_{CDR}	0	–	–	ns
Operation Recovery Time (see waveform below)	t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time



TYPICAL CHARACTERISTICS
(Continued)

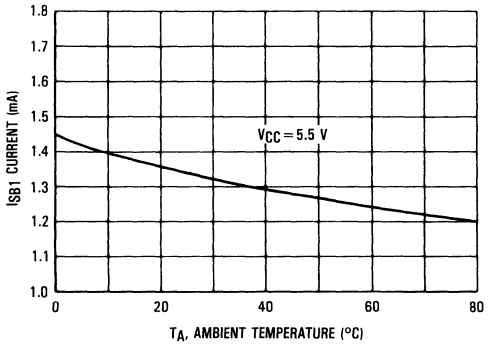


Figure 3. Standby Current Versus Temperature

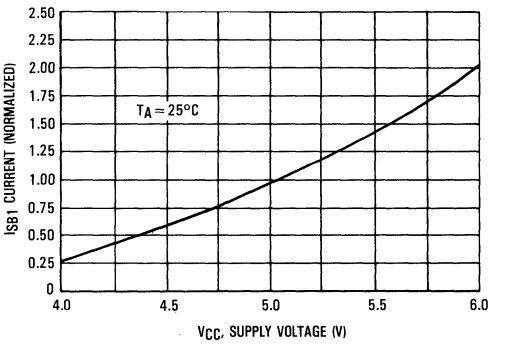


Figure 4. Standby Current Versus Supply Voltage

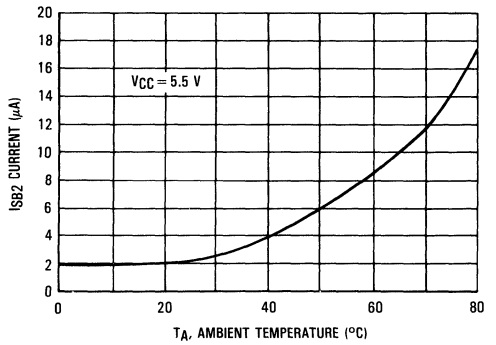


Figure 5. Standby Current Versus Temperature

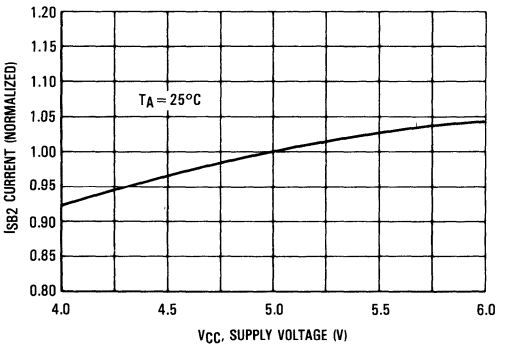


Figure 6. Standby Current Versus Supply Voltage

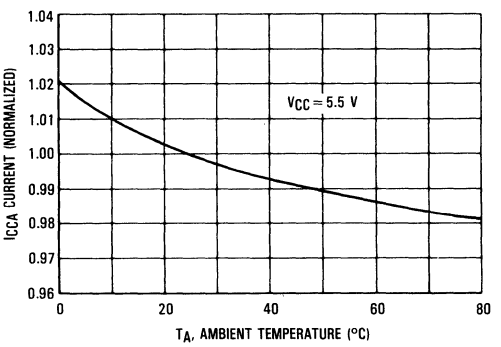


Figure 7. Supply Current Versus Temperature

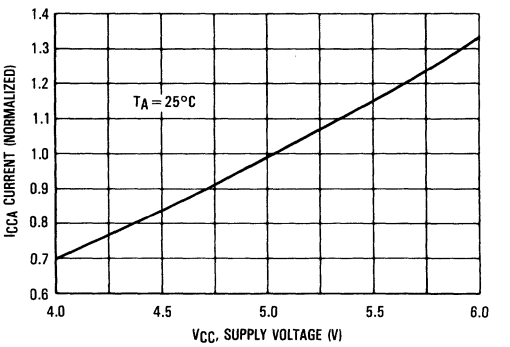


Figure 8. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

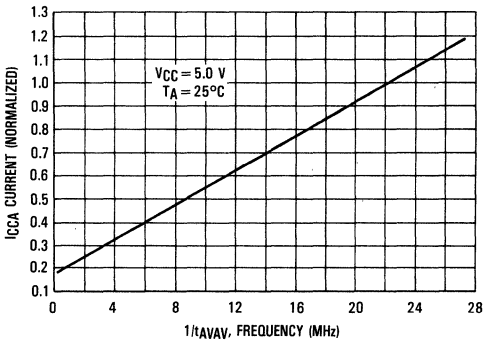


Figure 9. Supply Current Versus Frequency

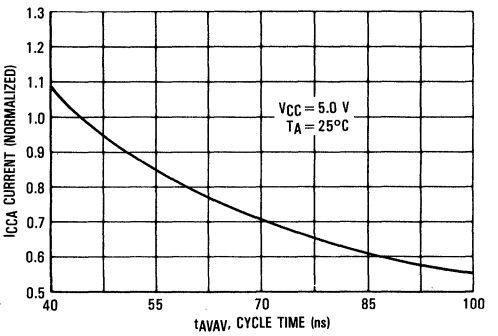


Figure 10. Supply Current Versus Cycle Time

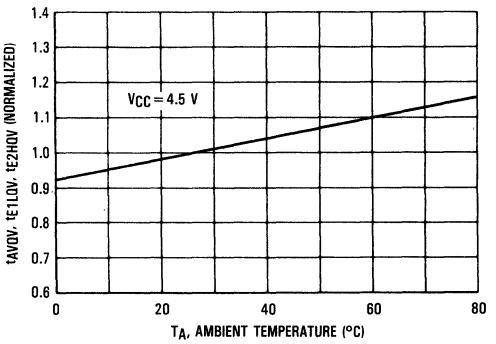


Figure 11. Access Time Versus Temperature

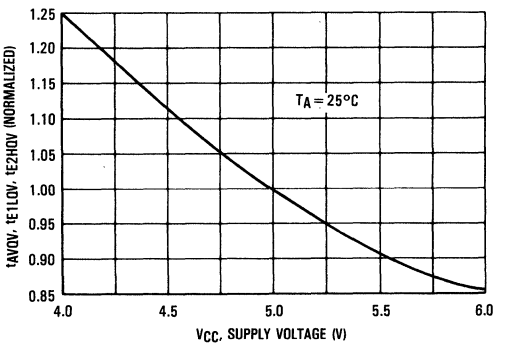


Figure 12. Access Time Versus Supply Voltage

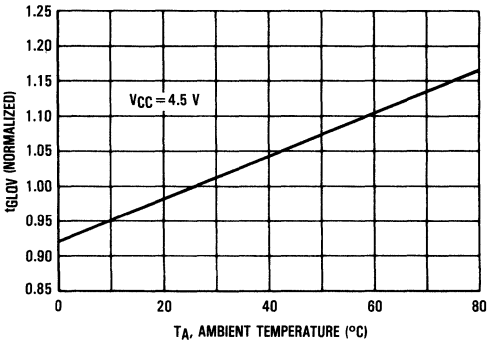


Figure 13. Access Time Versus Temperature

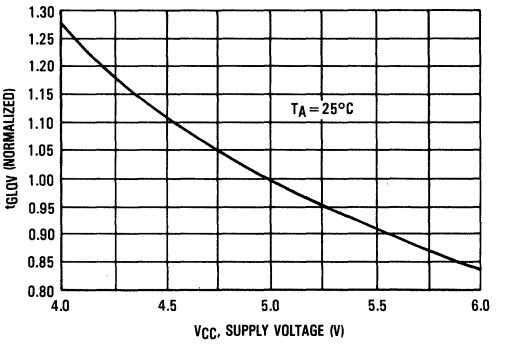
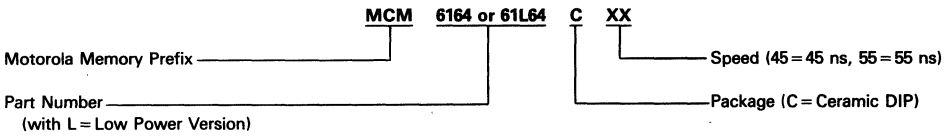


Figure 14. Access Time Versus Supply Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM6164C45 MCM6164C55 MCM61L64C45 MCM61L64C55

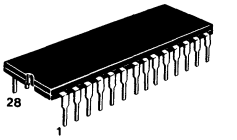
4

MCM6164C

Advance Information

8K x 8 Bit Fast Static Random Access Memory

Industrial Temperature Range: −40 to 85°C



C PACKAGE
CERAMIC
CASE 733

4

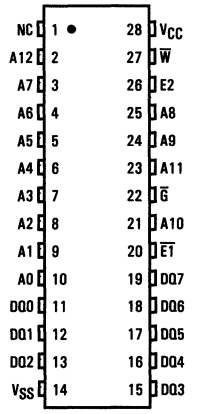
The MCM6164C is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. With its operating temperature range of −40°C to +85°C and hermetic package, the MCM6164C is ideally suited for harsh industrial type environments.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6164C is available in a 600 mil, 28 pin ceramic dual-in-line package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—55 or 70 ns (Maximum)
- Low Power Dissipation—440 or 385 mW (Maximum, Active)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Commercial Temperature Range (0 to 70°C) as MCM6164/MCM61L64

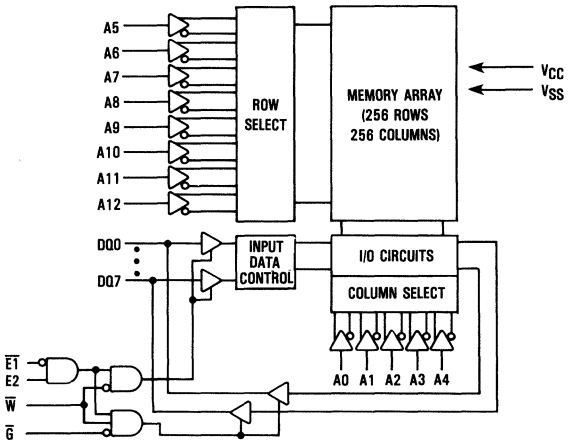
PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	<0.01	±2.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	<0.01	±2.0	μA
Power Supply Current	t_{AVAV} = 55 ns	I_{CC}	–	40	80	mA
($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0)	t_{AVAV} = 70 ns		–	35	70	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	–	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} −0.2 V or E2 ≤ 0.2 V)		I_{SB2}	–	0.005	1.0	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	3.0	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −40 to +85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

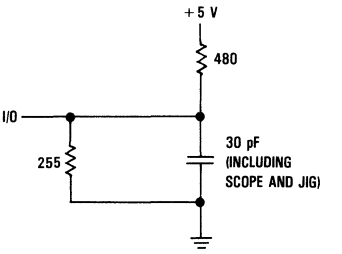


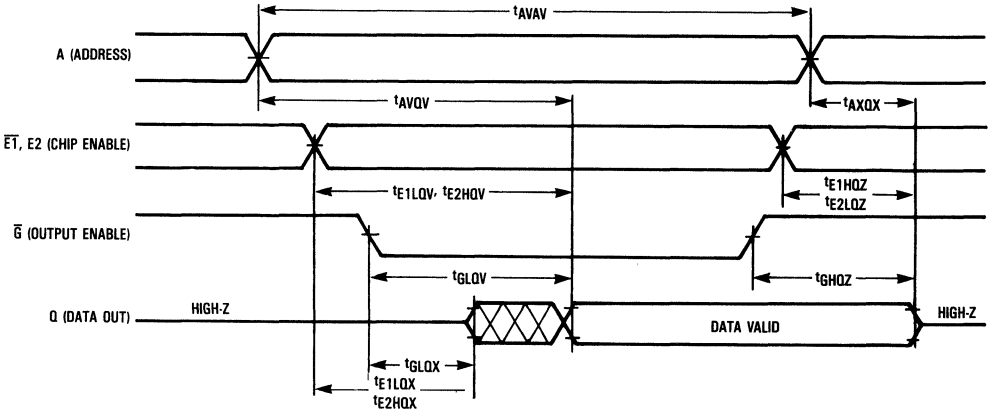
Figure 1. Test Load

4

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	55	–	70	–	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	55	–	70	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	55	–	70	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	55	–	70	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	25	–	30	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	2, 3

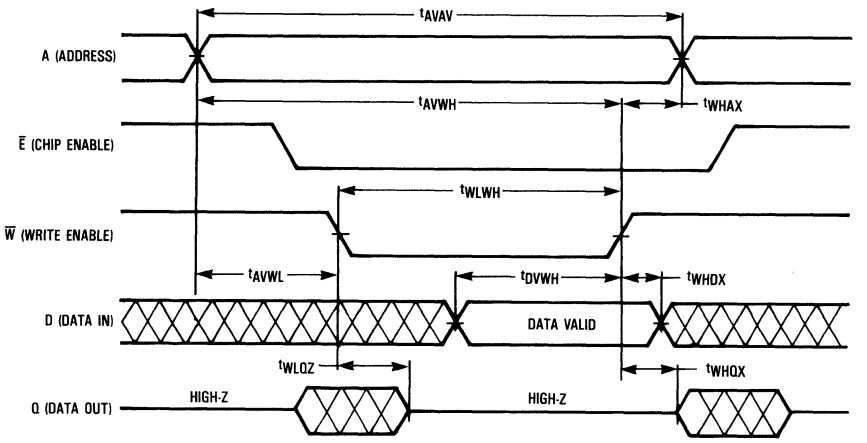
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.



WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	–	70	–	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	50	–	60	–	–
Write Pulse Width	t_{WLWH}	t_{WP}	30	–	40	–	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	25	–	30	–	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	–	5	–	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.



TIMING PARAMETER ABBREVIATIONS

t X X X X
- signal name from which interval is defined
- transition direction for first signal
- signal name to which interval is defined
- transition direction for second signal

The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

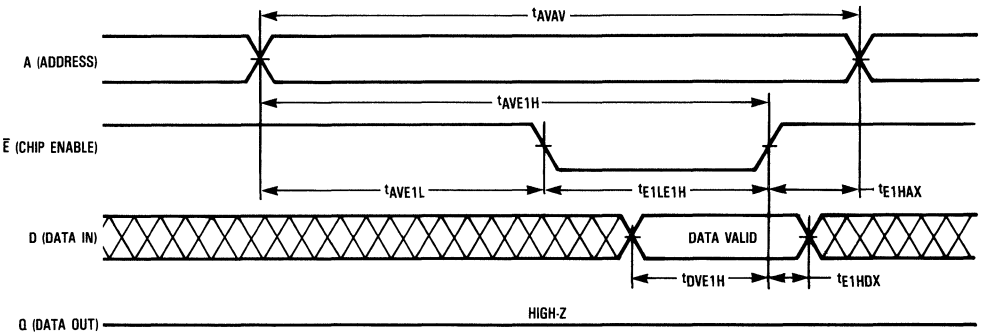
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	—
Address Setup Time	t_{AVE1L}	t_{AS}	0	—	0	—	—
Address Valid to End of Write	t_{AVE1H}	t_{AW}	50	—	60	—	—
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	50	—	60	—	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	25	—	30	—	—
Data Hold Time	t_{E1HDX}	t_{DH}	0	—	0	—	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	—	0	—	

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



TYPICAL CHARACTERISTICS

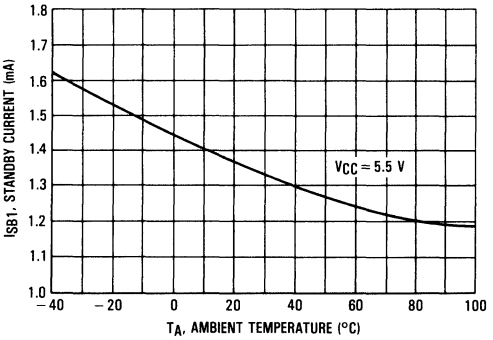


Figure 2. Standby Current Versus Temperature

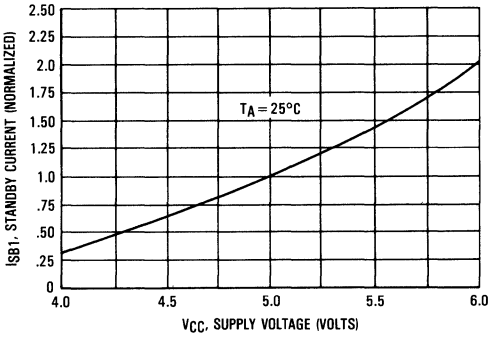


Figure 3. Standby Current Versus Supply Voltage

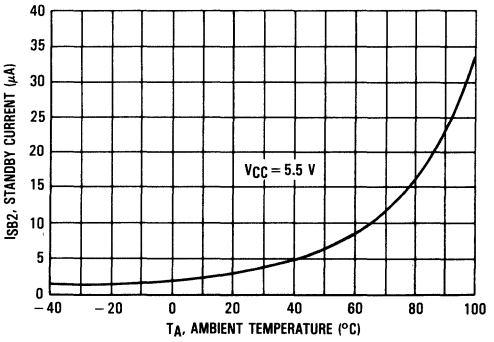


Figure 4. Standby Current Versus Temperature

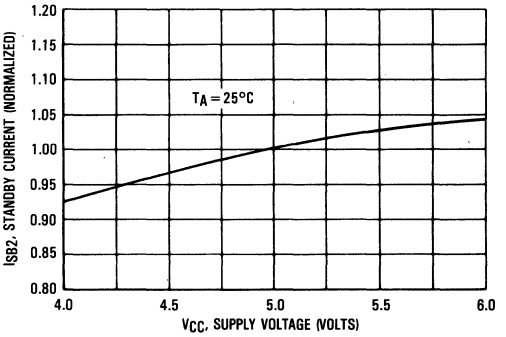


Figure 5. Standby Current Versus Supply Voltage

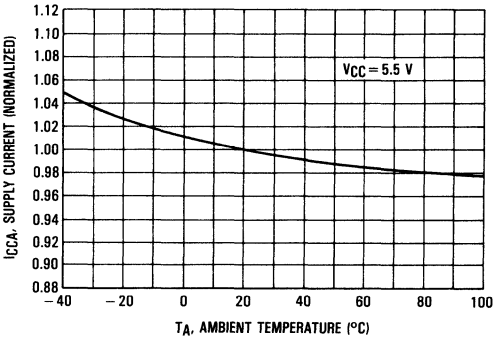


Figure 6. Supply Current Versus Temperature

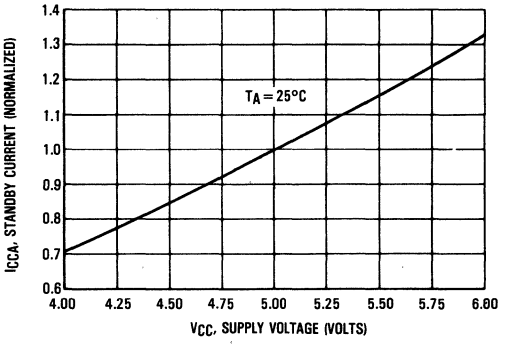


Figure 7. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

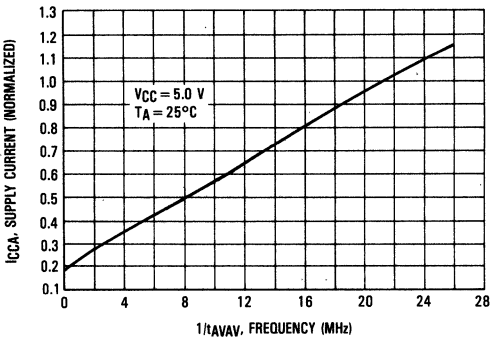


Figure 8. Supply Current Versus Frequency

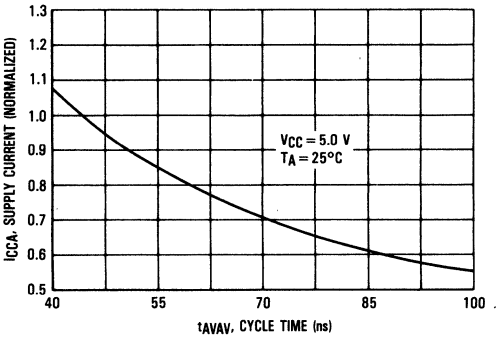


Figure 9. Supply Current Versus Cycle Time

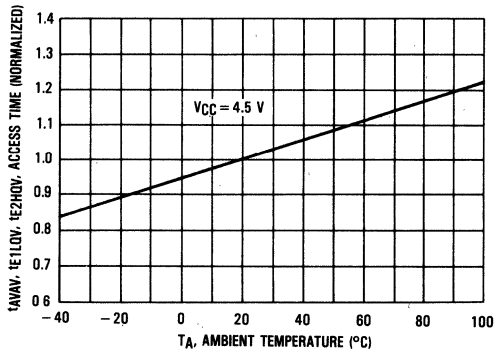


Figure 10. Access Time Versus Temperature

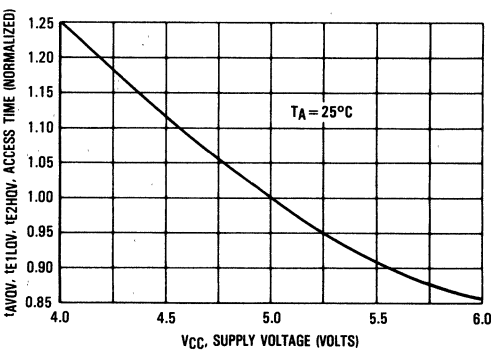


Figure 11. Access Time Versus Supply Voltage

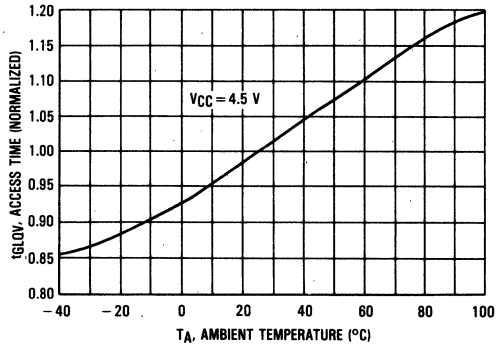


Figure 12. Access Time Versus Temperature

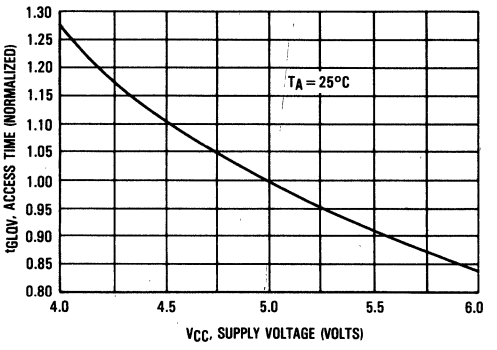
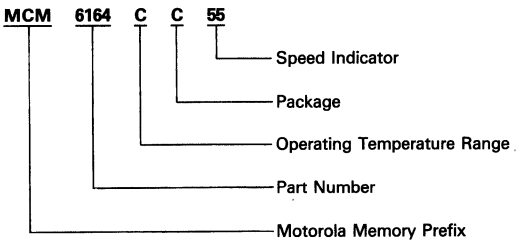


Figure 13. Access Time Versus Supply Voltage

ORDERING INFORMATION
(Order by Full Part Number)

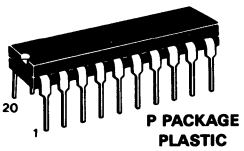


Full Part Number—MCM6164CC55 or MCM6164CC70

4

MCM6168

4K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

The MCM6168 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other high speed applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature provides reduced system power requirements without degrading access time performance.

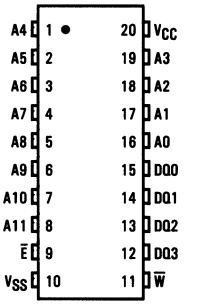
The MCM6168 is available in a 300 mil, 20 lead plastic dual-in-line package with the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fast Access Time (Maximum):

	Address	Chip Enable
MCM6168-45	45 ns	45 ns
MCM6168-55	50 ns	55 ns
MCM6168-70	60 ns	70 ns

- Low Power Operation: 80 mA Max (Active)
  20 mA Max (Standby—TTL Levels)
  2 mA Max (Standby—CMOS Levels)
- Fully TTL Compatible

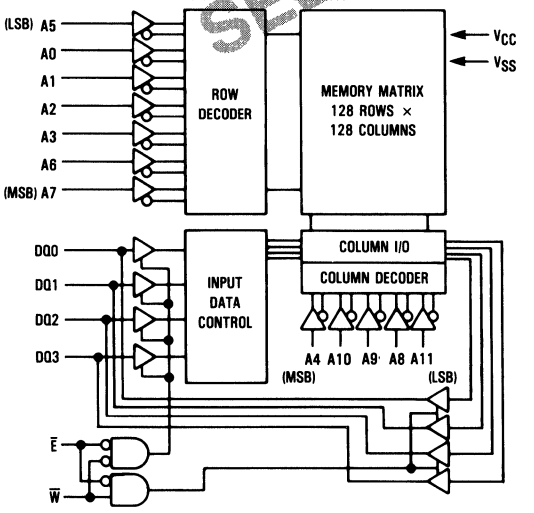
PIN ASSIGNMENT



PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin
H	X	Not Selected	ISB1, ISB2	High-Z
L	H	Read	I_{CC}	D_{out}
L	L	Write	I_{CC}	D_{in}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	−0.3	–	0.8	V	1, 2

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA	
Output Leakage Current ($\overline{E}$=V_{IH} or $\overline{W}$=V_{IL}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	–	±2.0	μA	3
Power Supply Current ($\overline{E}$=V_{IL}, I_{out}=0 mA)	I_{CC}	–	80	mA	3
TTL Standby Current ($\overline{E}$=V_{IH})	I_{SB1}	–	20	mA	
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, V_{in}≤0.2 V or ≥V_{CC}−0.2 V)	I_{SB2}	–	2	mA	
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	–	0.4	V	
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	–	V	

CAPACITANCE (f=1.0 MHz, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

NOTES:
1. Address rise and fall times while the chip is selected are 50 ns maximum.
2. V_{IL}(min)=−0.3 V dc; V_{IL}(min)=−3.0 V ac (pulse width≤20 ns).
3. Input levels less than −0.3 V or greater than V_{CC}+0.3 V will cause I/O and power supply currents to exceed maximum rating.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

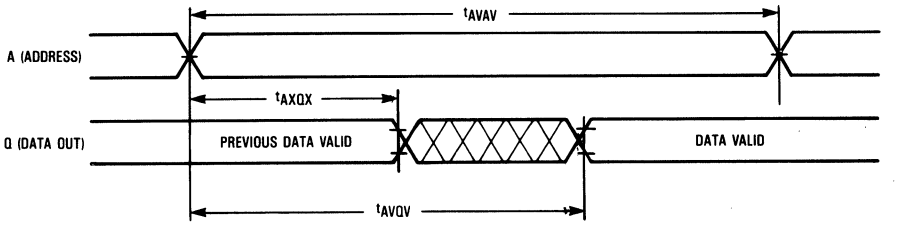
Output Timing Measurement Reference Level . . . . .0.8 and 2.0 V
Output Load. . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

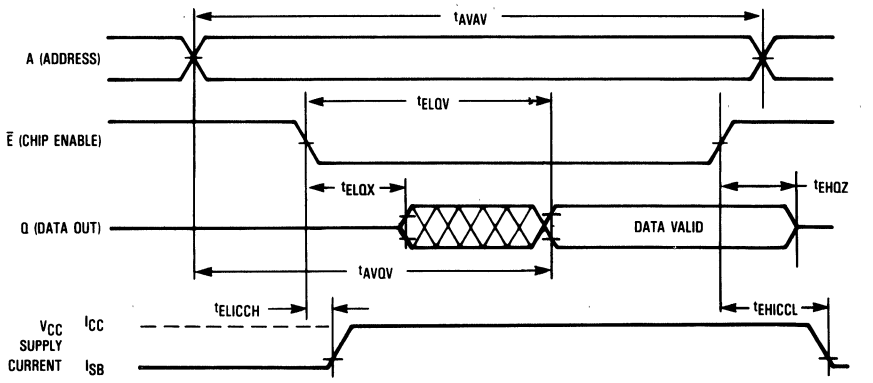
Parameter	Symbol		MCM6168-45		MCM6168-55		MCM6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	–	55	–	70	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	45	–	50	–	60	ns	
$\overline{E}$ Access Time	t_{ELQV}	t_{ACS}	–	45	–	55	–	70	ns	
$\overline{E}$ Low to Output Active	t_{ELQX}	t_{LZ}	10	–	10	–	10	–	ns	2, 3
$\overline{E}$ High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	20	0	25	ns	2, 3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	45	–	55	–	70	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
3. This parameter is sampled and not 100% tested.
4. Device is continuously selected ($\overline{E} = V_{IL}$).
5. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 4 Above)



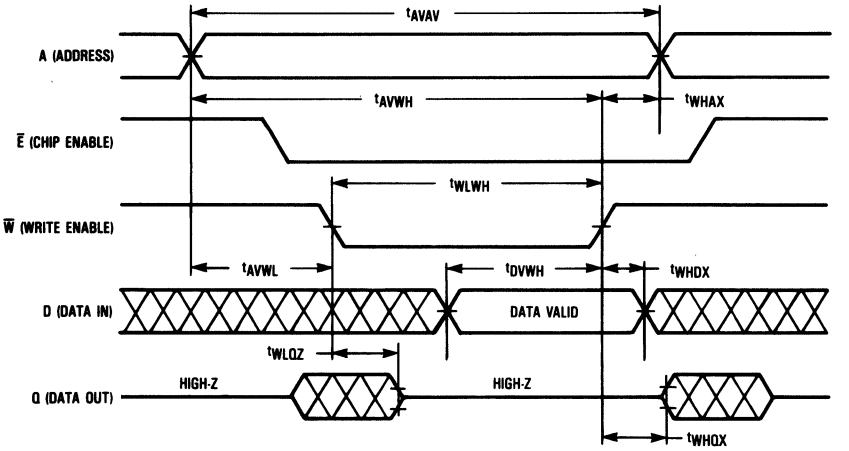
READ CYCLE 2 (See Note 5 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		MCM6168-45		MCM6168-55		MCM6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	40	–	50	–	60	–	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	35	–	45	–	55	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	–	45	–	55	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	20	–	25	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	–	3	–	3	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	20	–	25	–	30	ns	2, 3
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	ns	2, 3
Write Recovery Time	t_{WHAX}	t_{WR}	5	–	5	–	5	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
3. Parameter is sampled and not 100% tested.



AC TEST LOADS

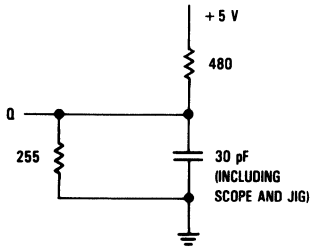


Figure 1A

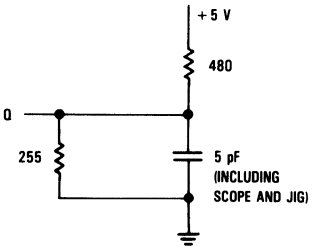


Figure 1B

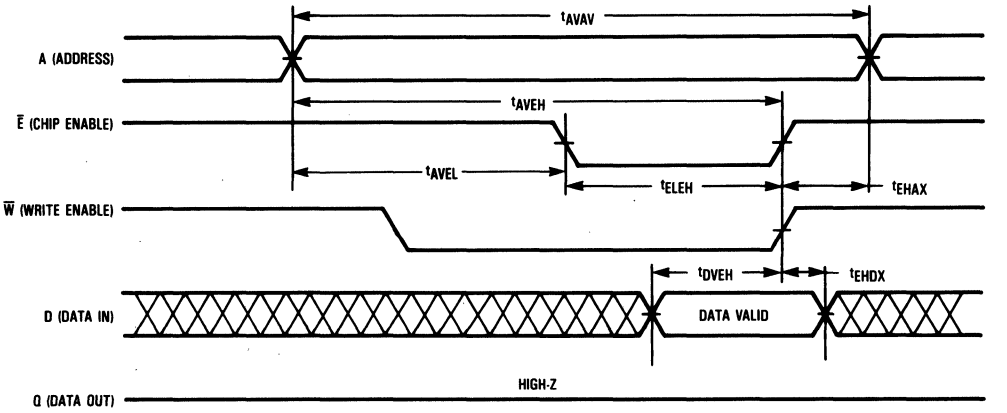
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		MCM6168-45		MCM6168-55		MCM6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	40	–	50	–	60	–	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	35	–	45	–	55	–	ns	
Write Pulse Width	t_{ELEH}	t_{CW}	35	–	45	–	55	–	ns	2, 3
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	–	20	–	25	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	–	3	–	3	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	5	–	5	–	5	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
3. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6168 X XX

- MCM: Motorola Memory Prefix
- 6168: Part Number
- X: Package (P = Plastic DIP)
- XX: Speed (45 = 45 ns, 55 = 55 ns, 70 = 70 ns)

Full Part Numbers – MCM6168P45
MCM6168P55
MCM6168P70

MCM6205-20

Product Preview

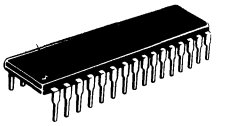
32K x 9 Bit Fast Static Random Access Memory

The MCM6205-20 is a 294,912 bit static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. This feature provides significant system-level power savings. The part will remain in standby mode until both pins are asserted true again. Another control feature, output enable ($\overline{G}$), allows access to the memory contents as fast as 10 ns (MCM6205-20).

The MCM6205-20 is packaged in a 300 mil, 32 pin plastic dual-in-line package or a 32 lead 300 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fast Access Time—20/25 ns (Maximum)
- Low Power Dissipation
- Chip Controls: Chip Enable ($\overline{E1}$, E2) for Reduced-Power Standby Mode
  Output Enable ($\overline{G}$) for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible
- High Board Density SOJ Package Available

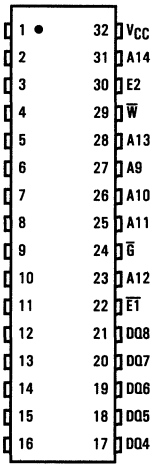


P PACKAGE
300 MIL PLASTIC
CASE TBD

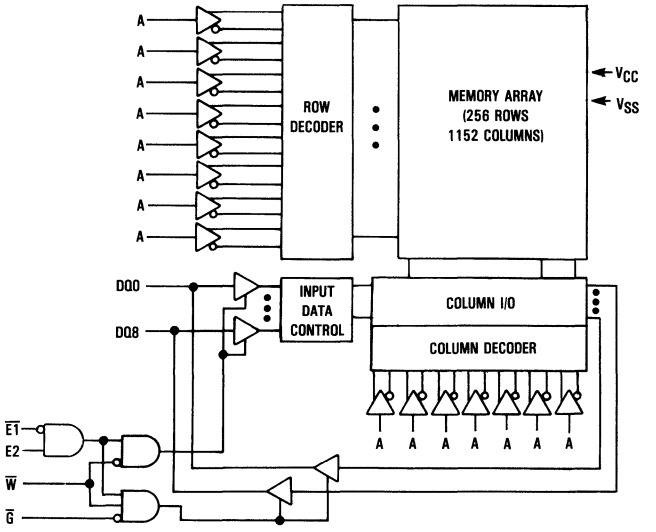
J PACKAGE
300 MIL SOJ
CASE TBD

4

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

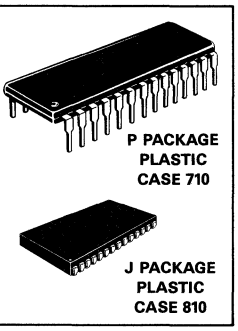
A	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ8	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM6206

Advance Information

32K x 8 Bit Fast Static Random Access Memory



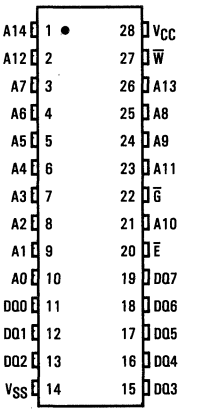
The MCM6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 15 ns (MCM6206-35).

The MCM6206 is packaged in a 600 mil, 28 pin plastic dual-in-line package or a 28 lead 400 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—35 or 45 ns (Maximum)
- Low Power Dissipation
- Two Chip Controls; $\overline{E}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible

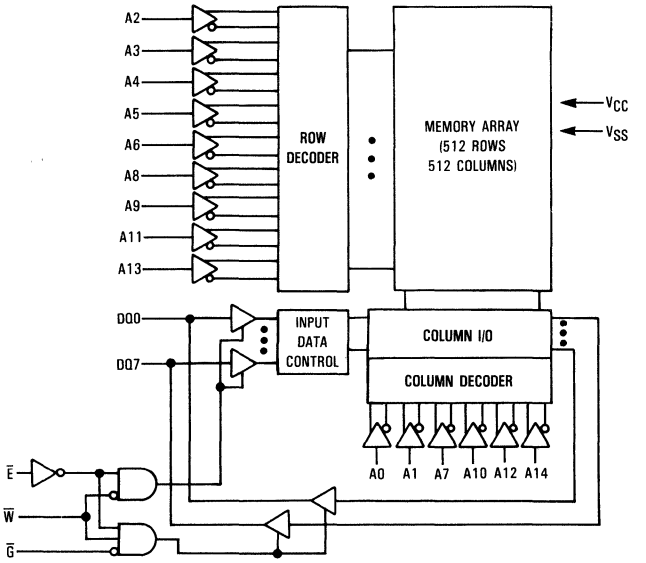
PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X—Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to 5.5 V)		$I_{lkg(O)}$	—	±1.0	μA
Power Supply Current	(t_{AVAV} = 35 ns)	I_{CC}	—	120	mA
($\overline{E}$ = V_{IL}, I_{out} = 0)	(t_{AVAV} = 45 ns)	I_{CC}	—	110	mA
Standby Current ($\overline{E}$ = V_{IH}) (TTL Levels)		I_{SB1}	—	20	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V) (CMOS Levels)		I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled and not 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

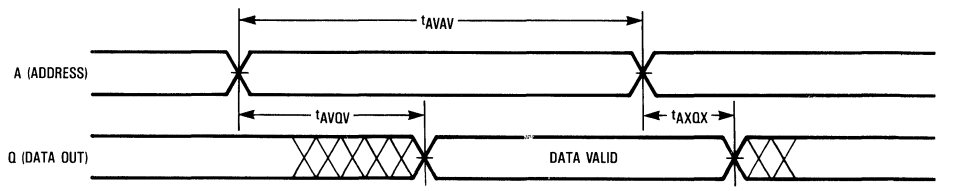
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE 1 & 2 (See Note 1)

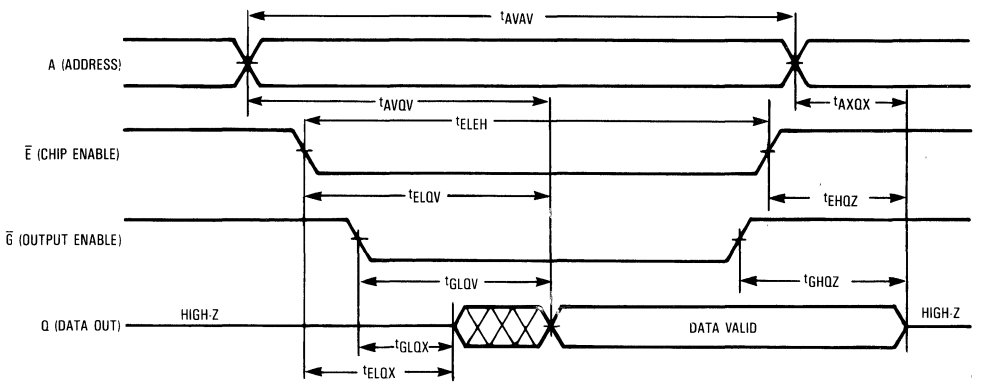
Parameter	Symbol	Alt Symbol	MCM6206-35		MCM6206-45		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	35	—	45	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	15	—	20	ns	—
Enable Low to Enable High	t_{ELEH}	t_{CW}	35	—	45	—	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	2
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	—	10	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE 1 ($\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$)



READ CYCLE 2



WRITE CYCLE 1 & 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6206-35		MCM6206-45		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	—	45	—	ns	—
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	—	0	—	ns	2
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	25	—	35	—	ns	—
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	15	—	20	—	ns	—
Data Hold From Write High Data Hold From Enable High	t_{WHDX} t_{EHDX}	t_{DH}	0	—	0	—	ns	—
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	0	—	0	—	ns	2
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	25	—	35	—	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	25	—	30	—	ns	3
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	—	5	—	ns	4, 5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E}$ or low $\overline{W}$. A write cycle ends at the earliest transition of a high $\overline{E}$ or high $\overline{W}$.
2. $\overline{W}$ must be high during all address transitions.
3. If $\overline{G}$ is enabled, allow an additional 15 ns t_{WLWH} to avoid bus contention.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.

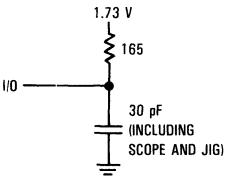
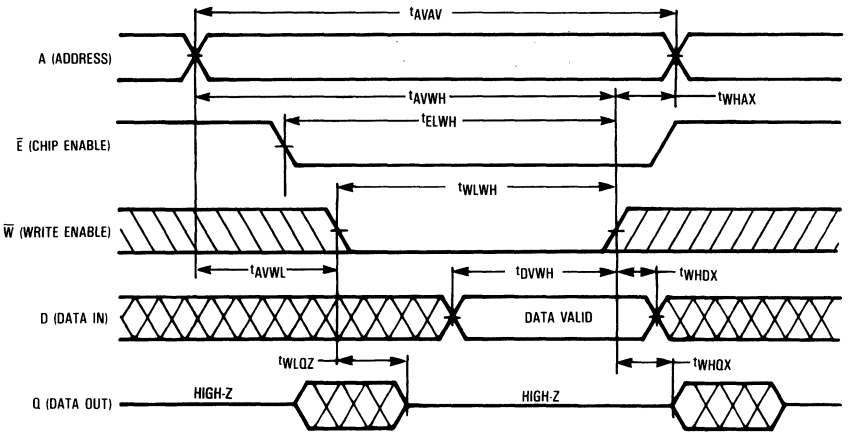
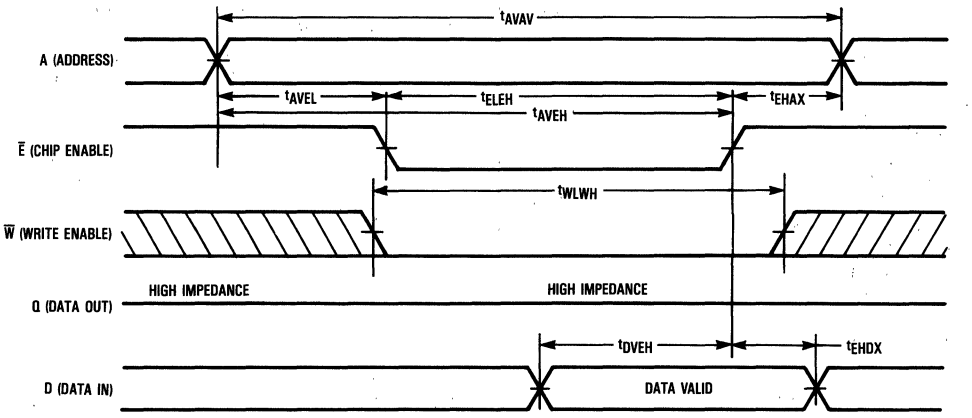


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206 X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape & Reel, Blank = Rails)
- Speed (35 = 35 ns, 45 = 45 ns)
- Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers — MCM6206P35, MCM6206P45, MCM6206J35, MCM6206J45, MCM6206J35R2, MCM6206J45R2

MCM6206-20

Product Preview

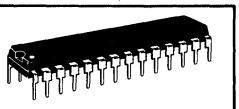
32K x 8 Bit Fast Static Random Access Memory

The MCM6206-20 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

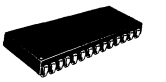
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When asserted false, the part reduces its power requirements and remains in this standby mode as long as $\overline{E}$ remains high. Another control feature, output enable ($\overline{G}$), allows access to the memory contents as fast as 8 ns (MCM6206-20).

The MCM6206-20 is packaged in a 300 mil, 28 pin plastic dual-in-line package or a 28 lead 300 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fast Access Time—20/25 ns (Maximum)
- Chip Controls: Chip Enable ($\overline{E}$) for Reduced-Power Standby Mode
  Output Enable ($\overline{G}$) for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible
- High Board Density SOJ Package Available



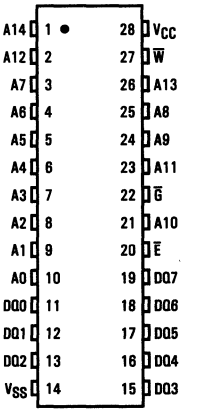
P PACKAGE
300 MIL PLASTIC
CASE 710A



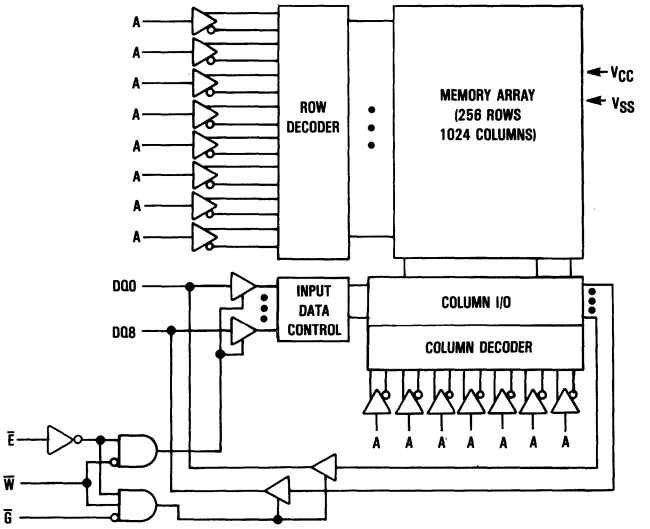
J PACKAGE
300 MIL SOJ
CASE 810B

4

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM6207

Product Preview

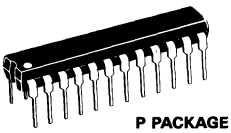
256K x 1 Bit Static Random Access Memory

The MCM6207 is a 262,144 bit static random access memory organized as 262,144 words of 1 bit, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

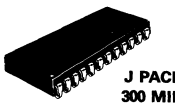
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature provides reduced system power requirements without degrading access time performance.

The MCM6207 is available in a 300 mil, 24 lead plastic DIP and in a 300 mil, surface-mount SOJ package.

- Single 5 V ±10% Power Supply
- Fast Access Time: 20/25 ns
- Equal Address and Chip Enable Access Time
- Separate Data Input and Three State Output
- Fully TTL Compatible
- Low Power Operation: 140/130 mA Maximum, Active AC
- High Board Density SOJ Package Available

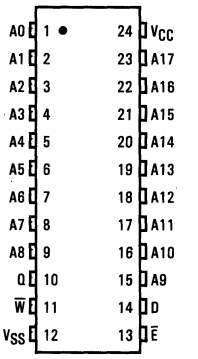


P PACKAGE
300 MIL PLASTIC
CASE 724

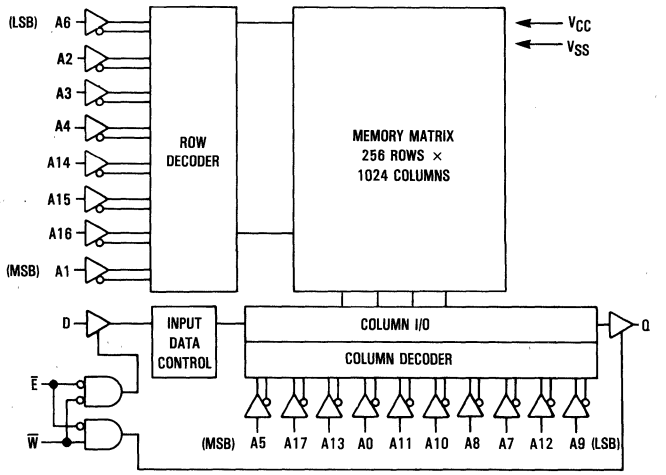


J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A17	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

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TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias (T_A=25°C)	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	**V_{CC}**	**4.5**	**5.0**	**5.5**	**V**
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6207-20: t_{AVAV}=20 ns	I_{CCA}	—	110	140	mA
	MCM6207-25: t_{AVAV}=25 ns		—	100	130	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	30	40	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	20	30	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
Output Capacitance		C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

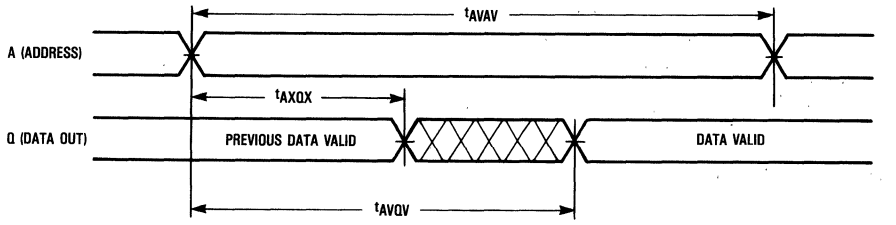
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

READ CYCLE (See Note 1)

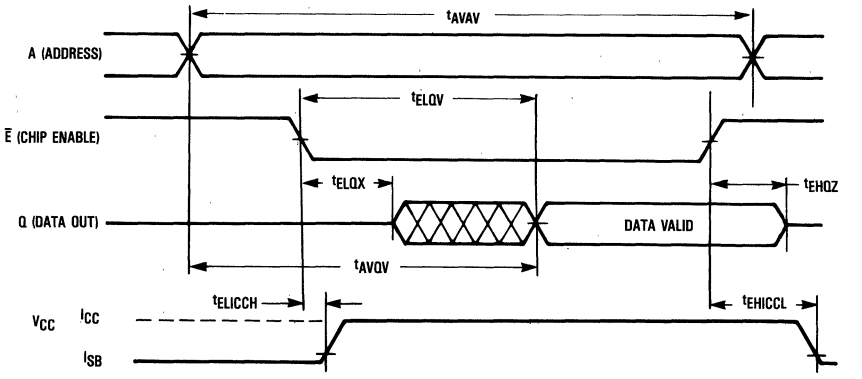
Parameter	Symbol		MCM6207-20		MCM6207-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	25	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	20	–	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	20	–	25	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	4	–	5	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	20	–	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 1 (See Note 7 Above)



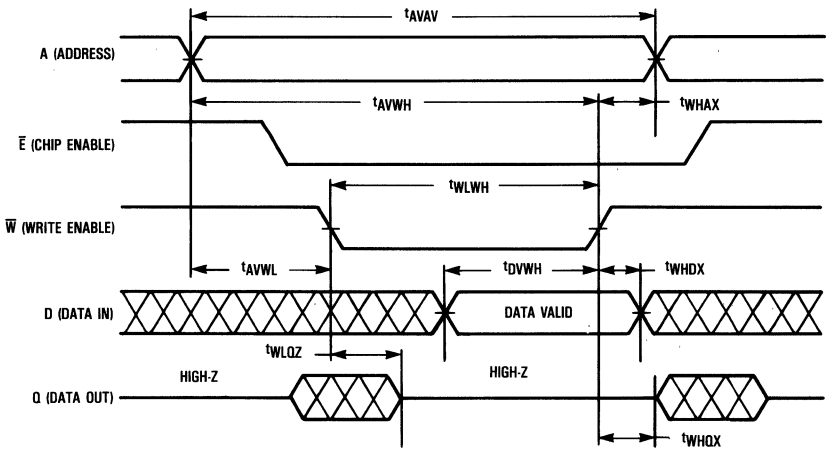
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6207-20		MCM6207-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	12	–	15	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	–	10	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	10	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

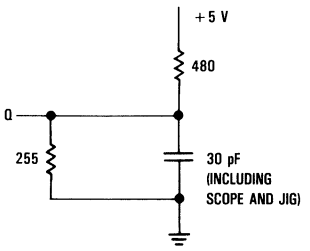


Figure 1A

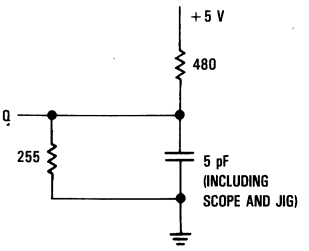


Figure 1B

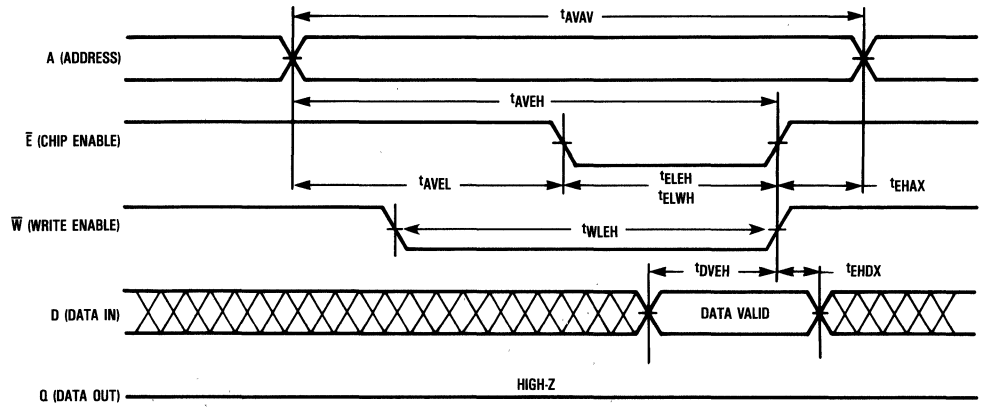
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6207-20		MCM6207-25		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	20	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	12	–	15	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	12	–	15	–	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	12	–	15	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	8	–	10	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6207 X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape & Reel, Blank = Rails)
- Speed (20 = 20 ns, 25 = 25 ns)
- Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers — MCM6207P20, MCM6207P25, MCM6207J20, MCM6207J25, MCM6207J20R2, MCM6207J25R2

MCM6208
MCM6209

Product Preview

64K × 4 Bit Static RAMs

The MCM6208 and MCM6209 are 262,144 bit static random access memories organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

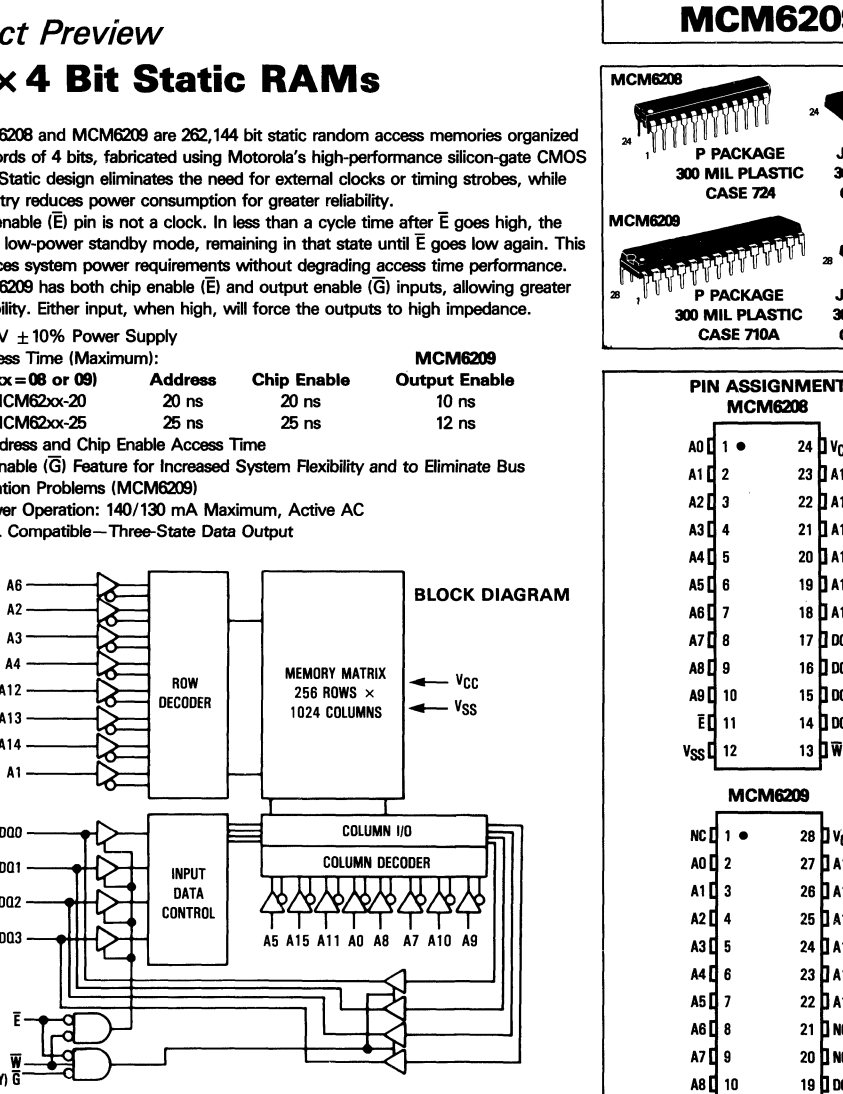
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access time performance.

The MCM6209 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

(xx = 08 or 09)	Address	Chip Enable	MCM6209 Output Enable
MCM62xx-20	20 ns	20 ns	10 ns
MCM62xx-25	25 ns	25 ns	12 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6209)
- Low Power Operation: 140/130 mA Maximum, Active AC
- Fully TTL Compatible—Three-State Data Output



4

PIN NAMES	
A0-A15 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3 . . Data Input/Output	NC . . . . . No Connection
$\overline{W}$ . . . . . Write Enable	V_{CC} . . . . +5 V Power Supply
$\overline{G}$ (MCM6209) . . Output Enable	V_{SS} . . . . . Ground

MCM6208 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6209 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

4

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	—	±1.0	μA
AC Supply Current (I_{out}=0 mA) t_{AVAV}=20 ns	I_{CCA}	—	110	140	mA
t_{AVAV}=25 ns		—	100	130	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	30	40	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	20	30	mA
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance All Inputs Except $\overline{E}$	C_{in}	4	6	pF
$\overline{E}$		5	7	
I/O Capacitance	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

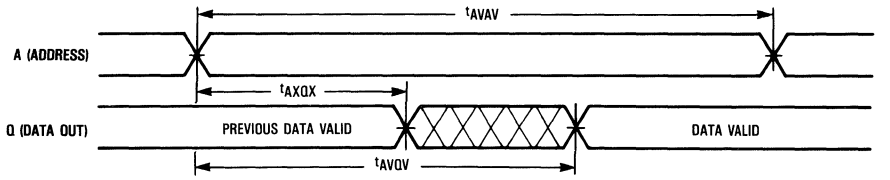
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

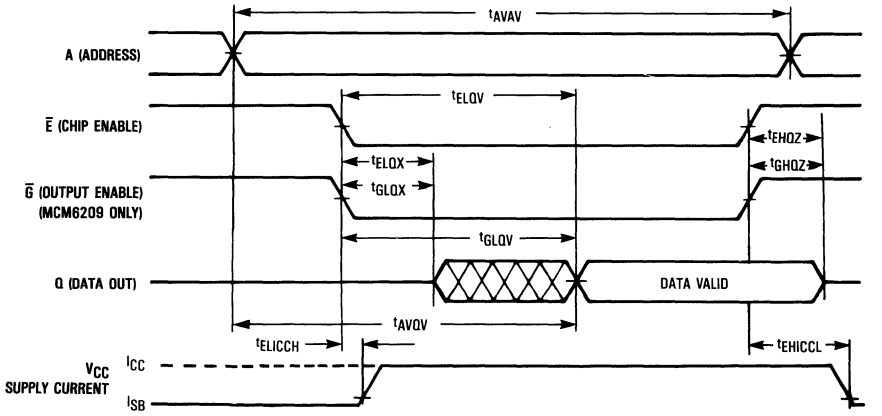
Parameter		Symbol		MCM6208-20 MCM6209-20		MCM6208-25 MCM6209-25		Units	Notes
		Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	20	—	25	—	ns	2
Address Access Time		t_{AVQV}	t_{AA}	—	20	—	25	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	—	20	—	25	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	4	—	5	—	ns	
Output Enable Access Time	MCM6209	t_{GLQV}	t_{OE}	—	10	—	12	ns	
Output Enable Low to Output Active	MCM6209	t_{GLQX}	t_{LZ}	3	—	4	—	ns	4,5,6
Output Enable High to Output High-Z	MCM6209	t_{GHQZ}	t_{HZ}	0	6	0	8	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	4	—	5	—	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	8	0	10	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time		t_{EHICCL}	t_{PD}	—	20	—	25	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}) and $\overline{G}$ = V_{IL} (MCM6209 only).

READ CYCLE 1 (See Note 7 Above)



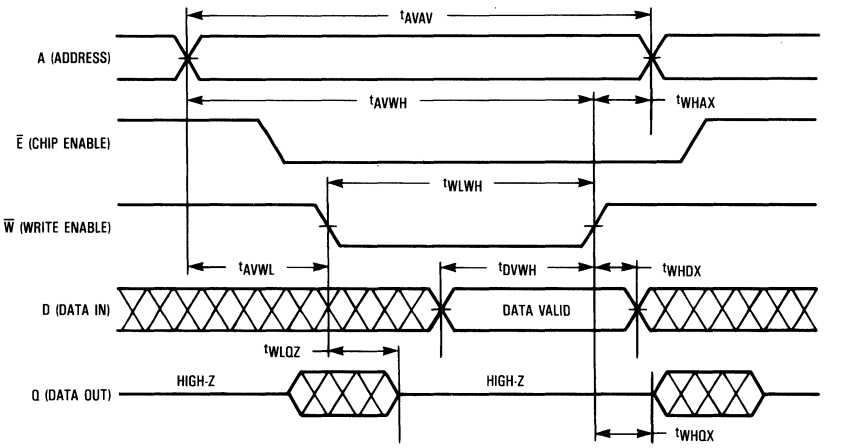
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6208-20 MCM6209-20		MCM6208-25 MCM6209-25		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	–	10	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	10	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6209, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

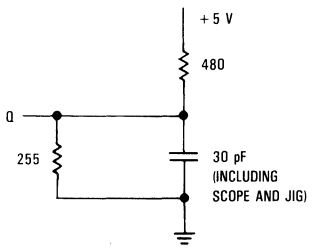


Figure 1A

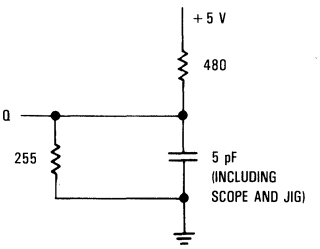
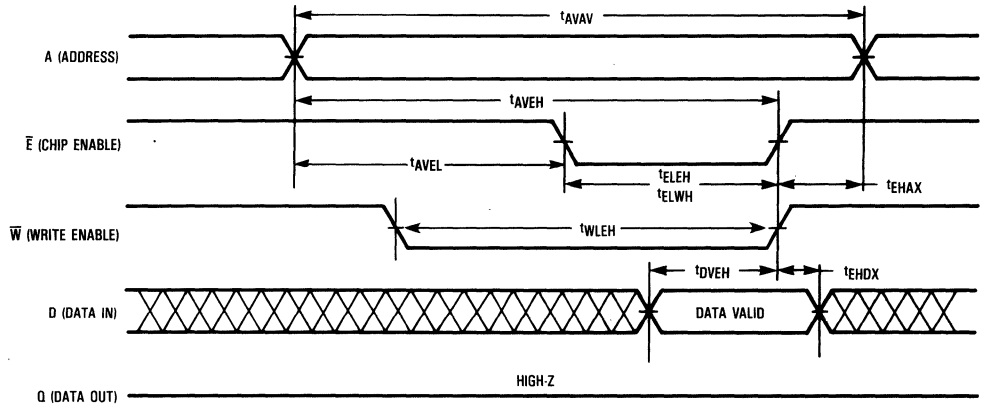


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6208-20 MCM6209-20		MCM6208-25 MCM6209-25		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	20	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	12	–	15	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	12	–	15	–	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	12	–	15	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	8	–	10	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6209, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62XX X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (20 = 20 ns, 25 = 25 ns)

Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers—			
	MCM6208P20	MCM6208J20	MCM6208J20R2
	MCM6208P25	MCM6208J25	MCM6208J25R2
	MCM6209P20	MCM6209J20	MCM6209J20R2
	MCM6209P25	MCM6209J25	MCM6209J25R2

MCM6226-30

Product Preview

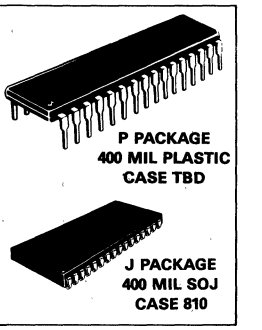
128K x 8 Bit Fast Static Random Access Memory

The MCM6226-30 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS (HCMOS) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The output enable ($\overline{G}$) feature allows fast access to the memory contents.

The MCM6226-30 is packaged in a 400 mil, 32 pin plastic dual-in-line package or a 32 lead 400 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—30 ns (Maximum)
- Low Power Dissipation—140 mA
- Three Chip Controls; $\overline{S}$ Chip Select
  S Chip Select
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible



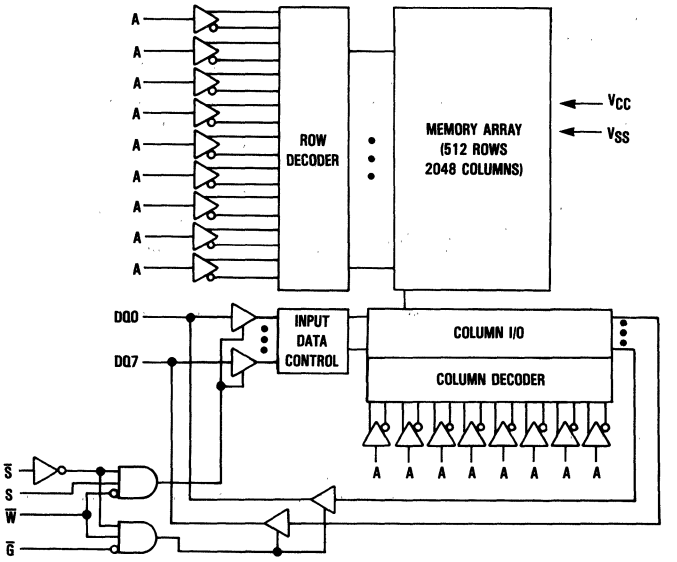
P PACKAGE
400 MIL PLASTIC
CASE TBD

J PACKAGE
400 MIL SOJ
CASE 810

PIN ASSIGNMENT

NC	1	32	V_{CC}
A	2	31	A
A	3	30	S/NC
A	4	29	$\overline{W}$
A	5	28	A
A	6	27	A
A	7	26	A
A	8	25	A
A	9	24	$\overline{G}$
A	10	23	A
A	11	22	$\overline{S}$
A	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
V_{SS}	16	17	DQ3

BLOCK DIAGRAM



PIN NAMES

A0-A16	Address
$\overline{W}$	Write Enable
$\overline{S}$	Chip Enable
S	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM6228-25

Product Preview

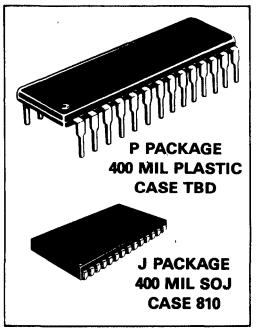
256K x 4 Bit Fast Static Random Access Memory

The MCM6228-25 is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS (HCMOS) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The output enable ($\overline{G}$) feature allows fast access to the memory contents.

The MCM6228-25 is packaged in a 400 mil, 28 pin plastic dual-in-line package or a 28 lead 400 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—25 ns (Maximum)
- Low Power Dissipation—140 mA
- Two Chip Controls; $\overline{S}$ Chip Select
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible



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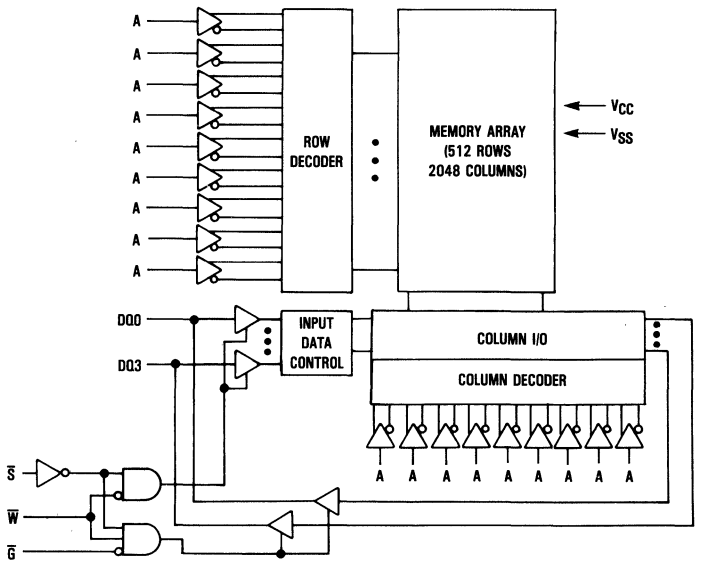
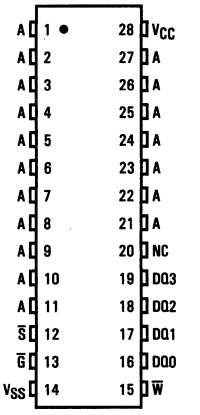
BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0-A17	Address
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM6264

8K × 8 Bit Fast Static RAM

The MCM6264 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption which provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6264 is available in 300 and 600 mil, 28 pin plastic dual-in-line packages and 300 and 400 mil, 28 pin plastic SOJ packages. All packages feature the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K × 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—30, 35, 45, 55 ns (Maximum)
- Low Power Operation—105, 100, 90, 80 mA (Maximum, Active)
- Three State Outputs
- All Inputs and Outputs are TTL Compatible
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

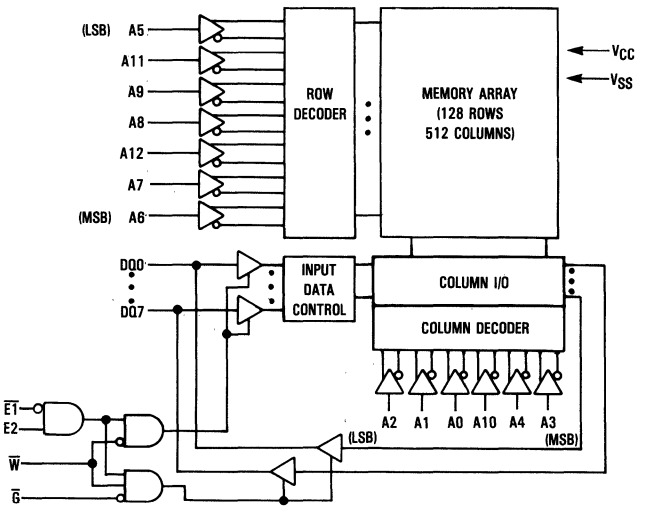
P PACKAGE
300 MIL PLASTIC
CASE 710A

WP PACKAGE
600 MIL PLASTIC
CASE TBD

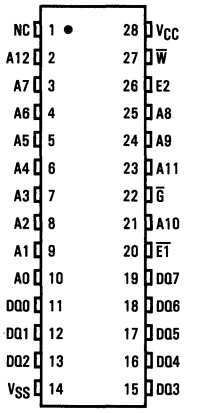
J PACKAGE
400 MIL SOJ
CASE 810

NJ PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0)	(t_{AVAV} = 30 ns)	I_{CC}	—	105	mA
	(t_{AVAV} = 35 ns)		—	100	
	(t_{AVAV} = 45 ns)		—	90	
	(t_{AVAV} = 55 ns)		—	80	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	—	10	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V, V_{in} = V_{IH} or V_{in} = V_{IL})		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
I/O Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . 0.8 and 2.0 V
Output Load . . . . . See Figure 1

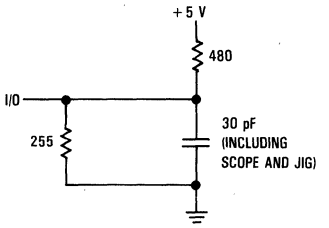


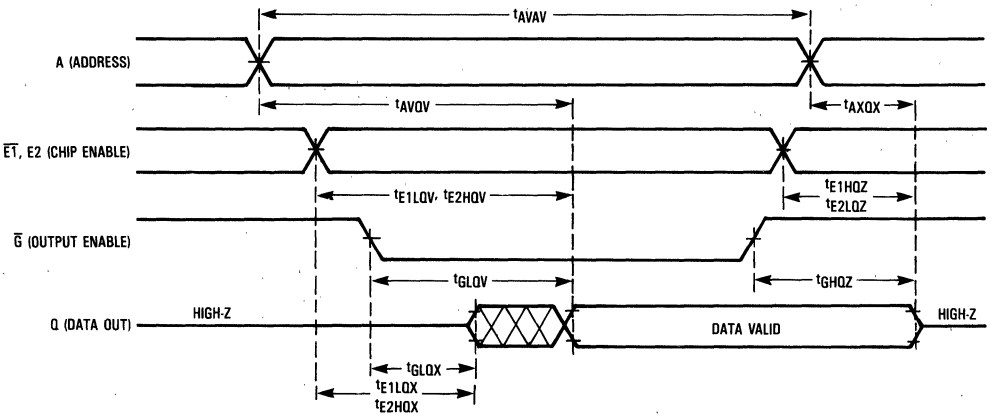
Figure 1. Test Load

4

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-30		MCM6264-35		MCM6264-45		MCM6264-55		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	30	–	35	–	45	–	55	–	ns	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	30	–	35	–	45	–	55	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	30	–	35	–	45	–	55	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	30	–	35	–	45	–	55	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	12.5	–	15	–	20	–	25	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	5	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	5	–	5	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	15	0	15	0	15	0	15	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	15	0	15	0	15	0	15	ns	2, 3

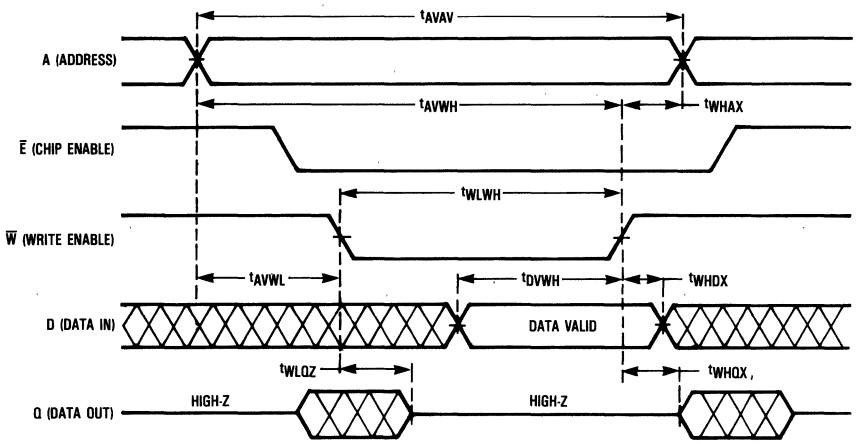
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



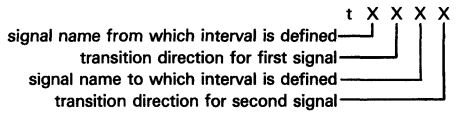
WRITE CYCLE 1 (W CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-30		MCM6264-35		MCM6264-45		MCM6264-55		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	–	35	–	45	–	55	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	22.5	–	25	–	35	–	45	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	17.5	–	20	–	25	–	30	–	ns	3
Data Valid to End of Write	t_{DVWH}	t_{DW}	12.5	–	15	–	20	–	25	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	15	0	15	0	15	0	15	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	–	5	–	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

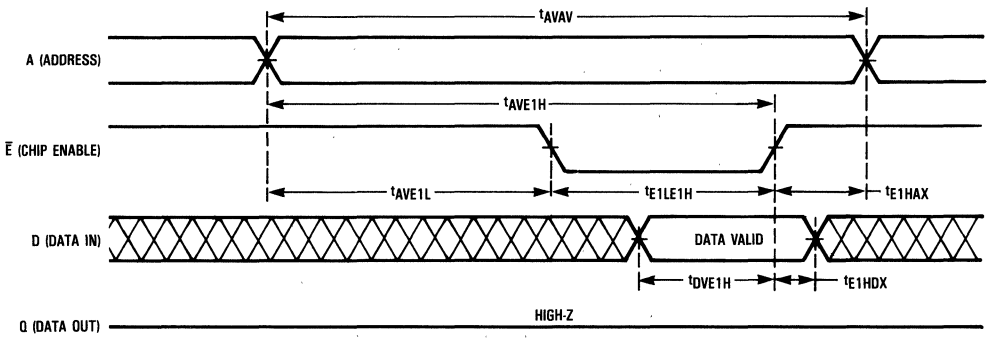
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-30		MCM6264-35		MCM6264-45		MCM6264-55		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	–	35	–	45	–	55	–	ns	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	0	–	0	–	ns	2
Address Valid to End of Write	t_{AVE1H}	t_{AW}	22.5	–	25	–	35	–	45	–	ns	2
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	22.5	–	25	–	35	–	45	–	ns	2, 3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	12.5	–	15	–	20	–	25	–	ns	2
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	2, 4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	2

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6264 X XX XX

- MCM — Motorola Memory Prefix
- 6264 — Part Number
- X — Package (P = 300 mil Plastic DIP, WP = 600 mil Plastic DIP, J = 400 mil Plastic SOJ, NJ = 300 mil Plastic SOJ)
- XX — Speed (30 = 30 ns, 35 = 35 ns, 45 = 45 ns, 55 = 55 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—

MCM6264P30	MCM6264WP30	MCM6264J30	MCM6264J30R2	MCM6264NJ30	MCM6264NJ30R2
MCM6264P35	MCM6264WP35	MCM6264J35	MCM6264J35R2	MCM6264NJ35	MCM6264NJ35R2
MCM6264P45	MCM6264WP45	MCM6264J45	MCM6264J45R2	MCM6264NJ45	MCM6264NJ45R2
MCM6264P55	MCM6264WP55	MCM6264J55	MCM6264J55R2	MCM6264NJ55	MCM6264NJ55R2

MCM6264-25

Product Preview

8K x 8 Bit Fast Static RAM

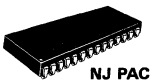
The MCM6264-25 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption which provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6264-25 is available in a 300 mil, 28 pin plastic dual-in-line package and a 300 mil, 28 pin plastic SOJ packages. All packages feature the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—25 ns (Maximum)
- Low Power Operation—110 mA (Maximum, Active)
- Three State Outputs
- All Inputs and Outputs are TTL Compatible
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

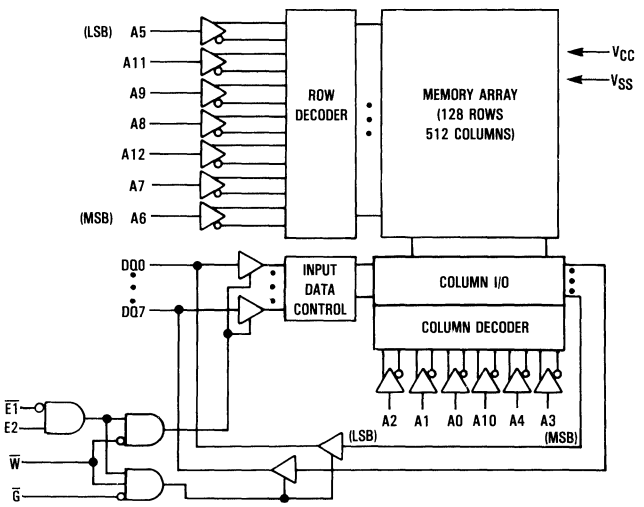
P PACKAGE
300 MIL PLASTIC
CASE 710A



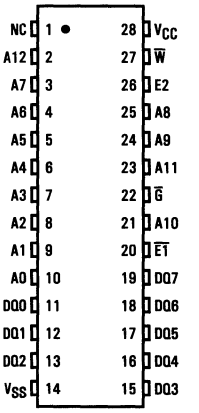
NJ PACKAGE
300 MIL SOJ
CASE 810B

4

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0, t_{AVAV} = 25 ns)	I_{CC}	–	105	mA
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	–	10	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V, V_{in} = V_{IH} or V_{in} = V_{IL})	I_{SB2}	–	5	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
I/O Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.0 V
Output Load . . . . . See Figure 1

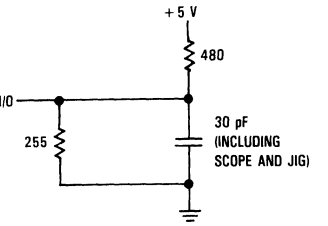
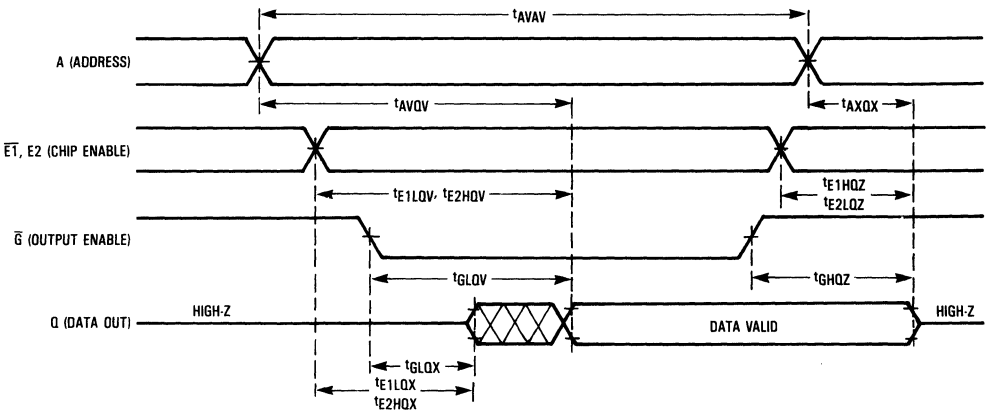


Figure 1. Test Load

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-25		Unit	Notes
			Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	ns	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	25	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	25	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	25	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	10	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	15	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	15	ns	2, 3

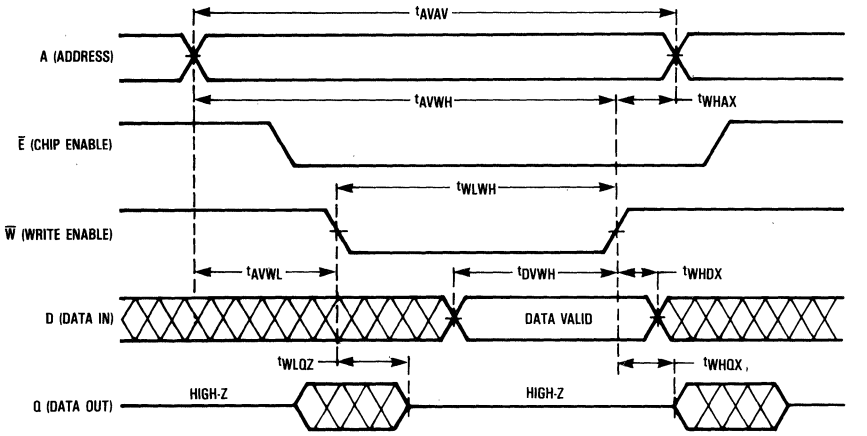
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



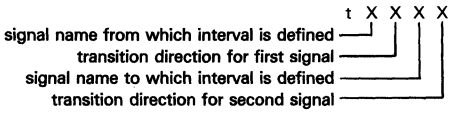
WRITE CYCLE 1 (W CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-25		Unit	Notes
			Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	ns	—
Address Setup Time	t_{AVWL}	t_{AS}	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	ns	3
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	15	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	—	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	ns	—

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

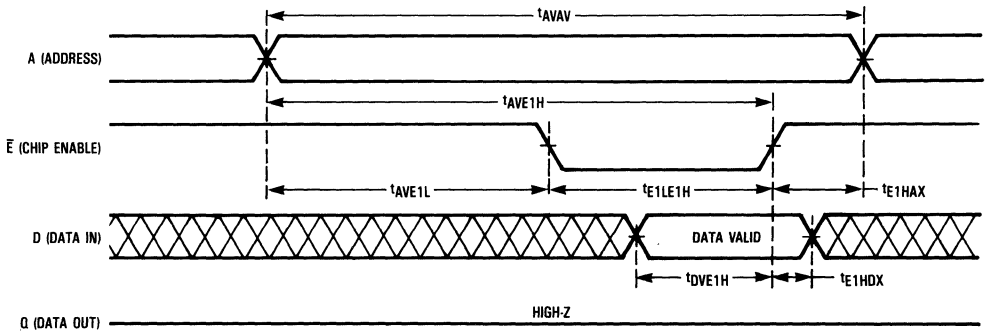
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-25		Unit	Notes
			Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	ns	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	ns	2
Address Valid to End of Write	t_{AVE1H}	t_{AW}	20	–	ns	2
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	20	–	ns	2, 3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	10	–	ns	2
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	ns	2, 4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	ns	2

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



ORDERING INFORMATION
(Order by Full Part Number)

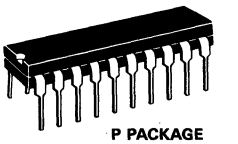
MCM 6264 X XX XX

- MCM — Motorola Memory Prefix
- 6264 — Part Number
- X — Package (P = 300 mil Plastic DIP, NJ = 300 mil Plastic SOJ)
- XX — Speed (25 = 25 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—MCM6264P25 MCM6264NJ25 MCM6264NJ25R2

MCM6268
MCM6269

4K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

The MCM6268 and MCM6269 are 16,384-bit static random access memories organized as 4096 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-50 ns applications.

The MCM6268 uses a chip enable ($\overline{E}$) function which is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

Similar in design to the Motorola MCM6268, the MCM6269 features an enhanced chip select circuit allowing access to data in as little as 12 ns.

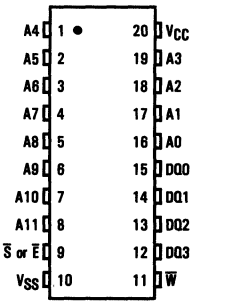
Both devices are available in a 20 lead plastic dual-in-line package and feature the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum) (xx = 68 or 69):

	Address	MCM6268 Chip Enable	MCM6269 Chip Select
MCM62xxP25	25 ns	25 ns	12 ns
MCM62xxP35	35 ns	35 ns	15 ns
MCM6268P45	45 ns	45 ns	
MCM6268P55	55 ns	55 ns	

- Low Power Operation: 110 mA Maximum, Active AC

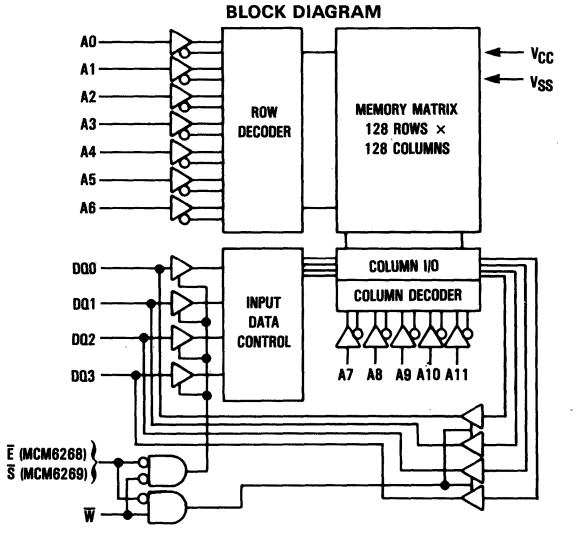
PIN ASSIGNMENT



PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$ (MCM6268)	Chip Enable
$\overline{S}$ (MCM6269)	Chip Select
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}/\overline{S}$	$\overline{W}$	Mode	V_{CC} Current (MCM6268)	V_{CC} Current (MCM6269)	I/O Pin	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	I_{CC}	High-Z	—
L	H	Read	I_{CC}	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	I_{CC}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ or $\overline{S}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6268/69-25, 35	I_{CC}	—	110	mA
	MCM6268-45, 55		—	80	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs) (MCM6268)		I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)	MCM6268-25, 35	I_{SB2}	—	15	mA
	MCM6268-45, 55		—	2	
($\overline{S}$≥V_{CC}−0.2 V, V_{in}≤0.2 V, or ≥V_{CC}−0.2 V) (MCM6269)		I_{SB}	—	15	
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$, $\overline{S}$	C_{in}	—	4	6	pF
	$\overline{E}$, $\overline{S}$		—	5	7	
I/O Capacitance		$C_{I/O}$	—	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

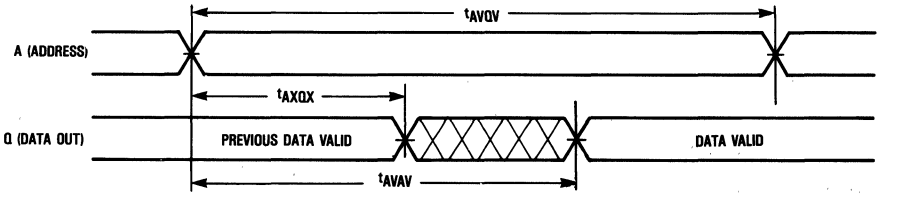
Input Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Output Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

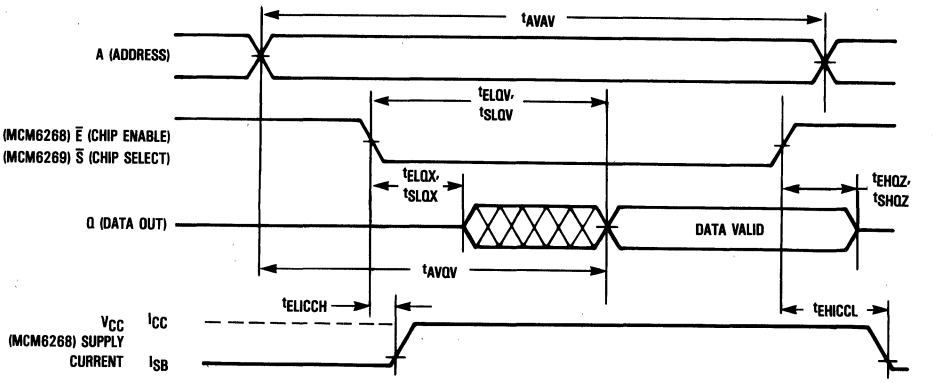
Parameter	Symbol		MCM6268P25 MCM6269P25		MCM6268P35 MCM6269P35		MCM6268P45		MCM6268P55		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	35	–	40	–	55	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	35	–	40	–	50	ns	
Enable Access Time (MCM6268)	t_{ELQV}	t_{ACS}	–	25	–	35	–	45	–	55	ns	
Select Access Time (MCM6269)	t_{SLQV}	t_{ACS}	–	12	–	15					ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	5	–	10	–	10	–	ns	3,4,5
Select Low to Output Active (MCM6269)	t_{SLQX}	t_{LZ}	5	–	5	–					ns	3,4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	10	0	15	0	15	0	20	ns	3,4,5
Select High to Output High-Z (MCM6269)	t_{SHQZ}	t_{HZ}	0	10	0	15					ns	3,4,5
Power Up Time (MCM6268)	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	0	–	ns	
Power Down Time (MCM6268)	t_{EHICCL}	t_{PD}	–	20	–	30	–	45	–	55	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} (or t_{SHQZ}) max, is less than t_{ELQX} (or t_{SLQX}) min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ or $\overline{S}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ or $\overline{S}$ going low.

READ CYCLE 1 (See Note 6 Above)



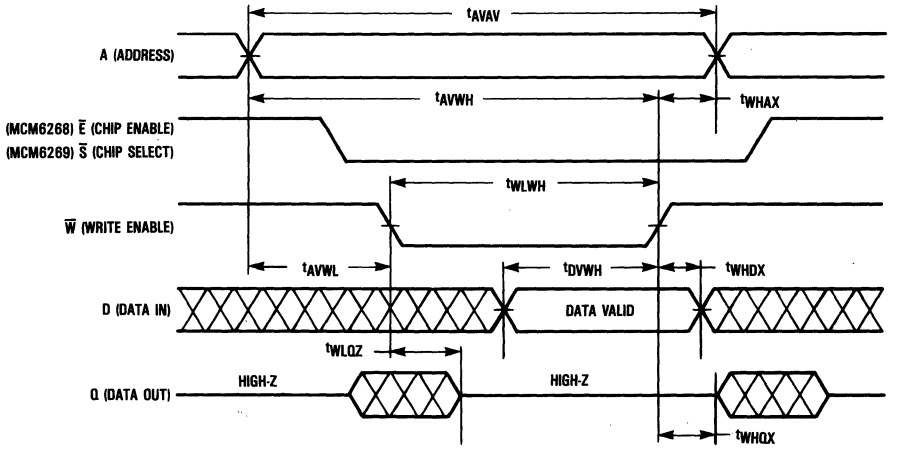
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6268P25 MCM6269P25		MCM6268P35 MCM6269P35		MCM6268P45		MCM6268P55		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	40	–	50	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	30	–	35	–	45	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	25	–	35	–	45	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	15	–	15	–	20	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	15	0	20	0	25	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	5	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ or $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

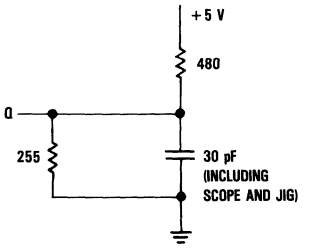


Figure 1A

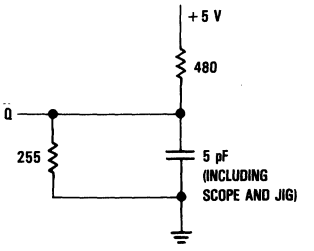


Figure 1B

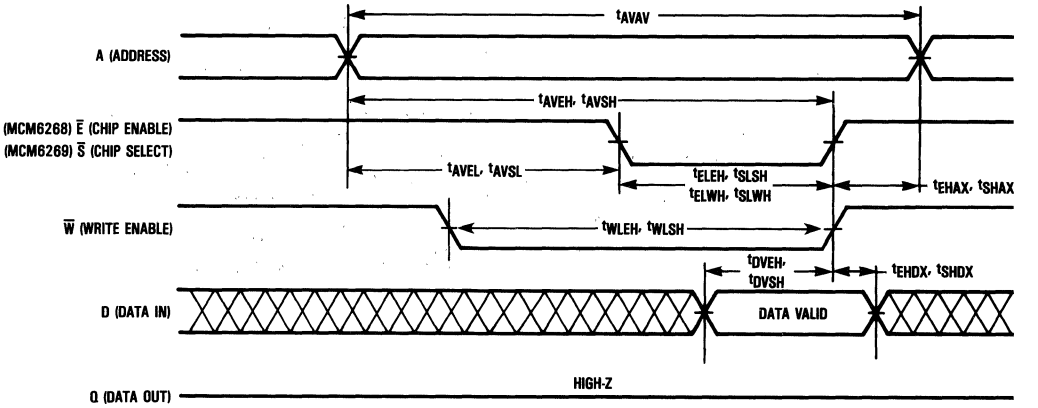
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$, $\overline{S}$ Controlled; See Note 1)

Parameter	Symbol		MCM6268P25 MCM6269P25		MCM6268P35 MCM6269P35		MCM6268P45		MCM6268P55		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	40	—	50	—	ns	2
Address Setup Time	t_{AVEL}, t_{AVSL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}, t_{AVSH}	t_{AW}	20	—	30	—	35	—	45	—	ns	
Enable to End of Write (MCM6268)	t_{ELEH}	t_{CW}	20	—	30	—	35	—	45	—	ns	3,4
Select to End of Write (MCM6269)	t_{SLSH}	t_{CW}	20	—	30	—					ns	3,4
Enable to End of Write (MCM6268)	t_{ELWH}	t_{CW}	20	—	30	—	30	—	30	—	ns	
Select to End of Write (MCM6269)	t_{SLWH}	t_{CW}	20	—	30	—					ns	
Write Pulse Width	t_{WLEH}, t_{WLSH}	t_{WP}	20	—	25	—	30	—	30	—	ns	
Data Valid to End of Write	t_{DVEH}, t_{DVSH}	t_{DW}	10	—	15	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}, t_{SHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}, t_{SHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ or $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ or $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ or $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6268 or 6269 P XX

Motorola Memory Prefix — MCM

Part Number — 6268 or 6269

Speed (25 = 25 ns, 35 = 35 ns, 45 = 45 ns, 55 = 55 ns) — XX

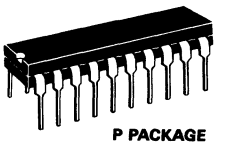
Package (P = Plastic DIP) — P

Full Part Numbers — MCM6268P25, MCM6268P35, MCM6268P45, MCM6268P55, MCM6269P25, MCM6269P35

MCM6268-20

Advance Information

4K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

The MCM6268-20 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-25 ns applications.

The chip enable ($\overline{E}$) function is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

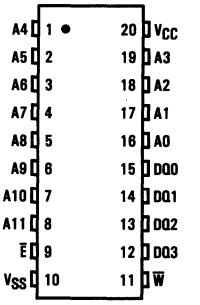
The MCM6268-20 is available in a 20 lead plastic dual-in-line package and features the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum)

	Address	Chip Enable
MCM6268P20	20 ns	20 ns

- Low Power Operation: 110 mA Maximum, Active AC

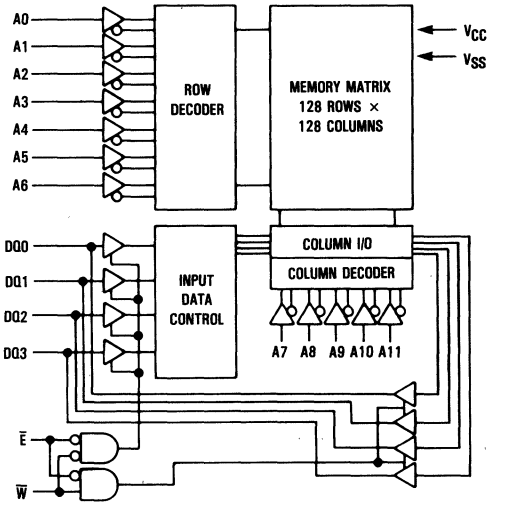
PIN ASSIGNMENT



PIN NAMES

A0-A11	Address Input
W	Write Enable
E	Chip Enable
DQ0-DQ3	Data Input/Output
VCC	+5 V Power Supply
VSS	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	I_{CC}	—	110	mA
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	4	6	pF
	$\overline{E}$		—	5	7	
I/O Capacitance		$C_{I/O}$	—	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

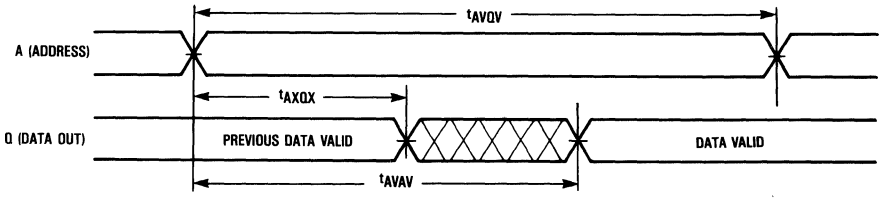
Output Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

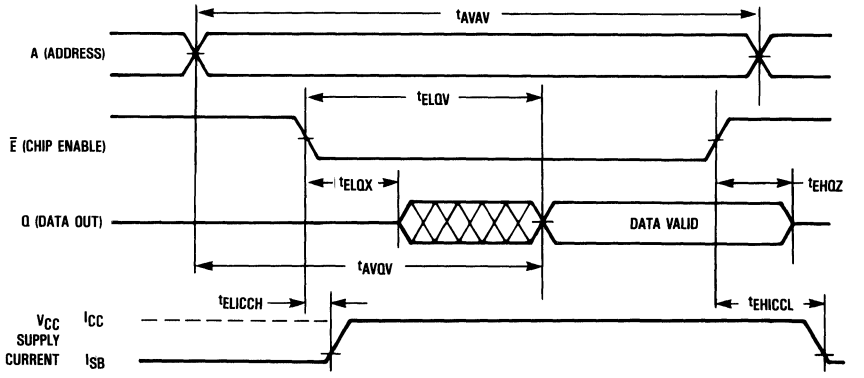
Parameter	Symbol		MCM6268P20		Unit	Notes
	Standard	Alternate	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	20	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	20	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	4	–	ns	3,4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	ns	3,4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	20	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E} = V_{IL}$).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 6 Above)



READ CYCLE 2 (See Note 7 Above)

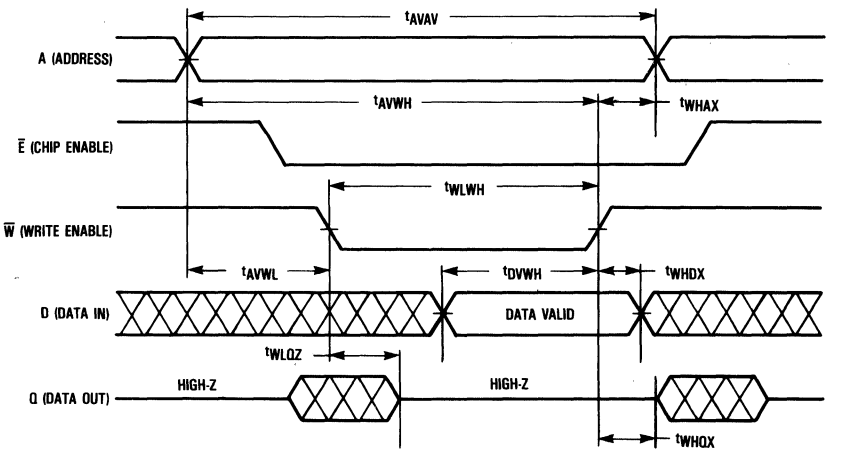


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6268P20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	ns	

4

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

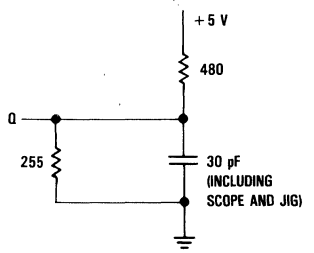


Figure 1A

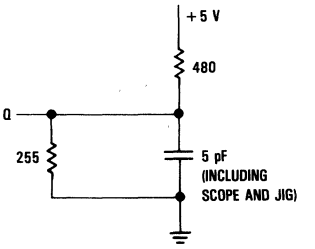


Figure 1B

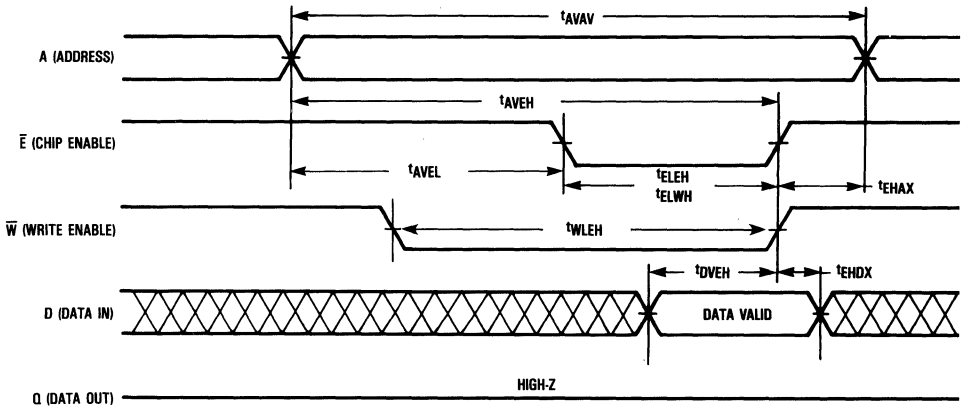
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

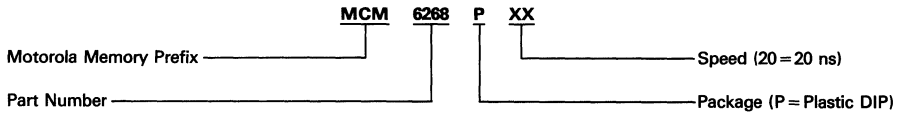
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		MCM6268P20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	15	–	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

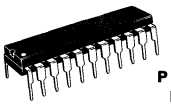


Full Part Numbers—MCM6268P20

MCM6270

Advance Information

4K x 4 Bit Static RAM



P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

The MCM6270 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The MCM6270 is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

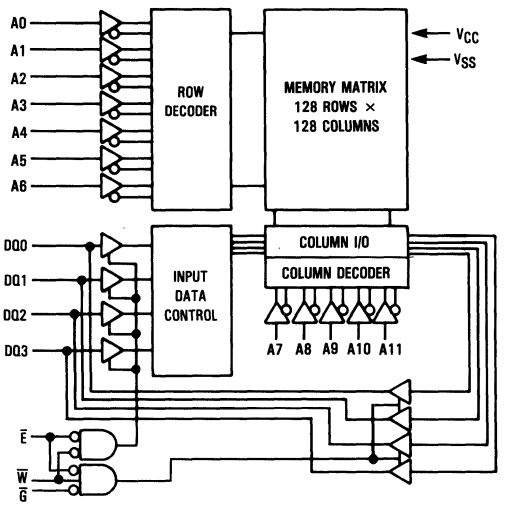
4

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Three-State Outputs
- Fully TTL Compatible
- Fast Access Time (Maximum):

	Address	Chip Enable	Output Enable
MCM6270-20	20 ns	20 ns	10 ns
MCM6270-25	25 ns	25 ns	12 ns
MCM6270-35	35 ns	35 ns	14 ns

- Low Power Operation: 110 mA Maximum, Active AC
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

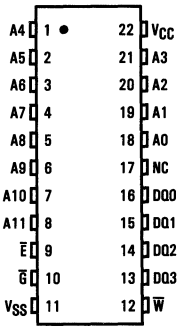
BLOCK DIAGRAM



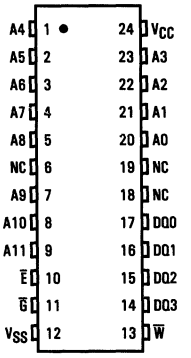
PIN NAMES	
A0-A11 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3 . Data Input/Output	V_{CC} . . . +5 V Power Supply
$\overline{W}$ . . . . . Write Enable	V_{SS} . . . . . Ground
$\overline{G}$ . . . . . Output Enable	NC . . . . . No Connection

PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC})	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (+25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	—	110	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5 V ±10%, T_A=0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

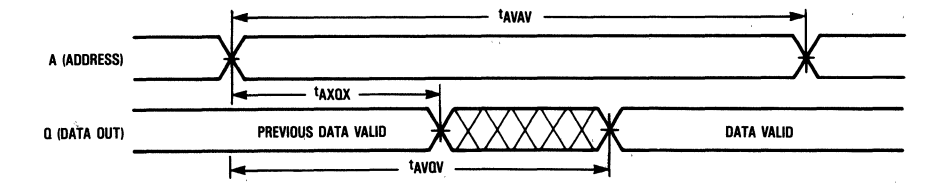
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

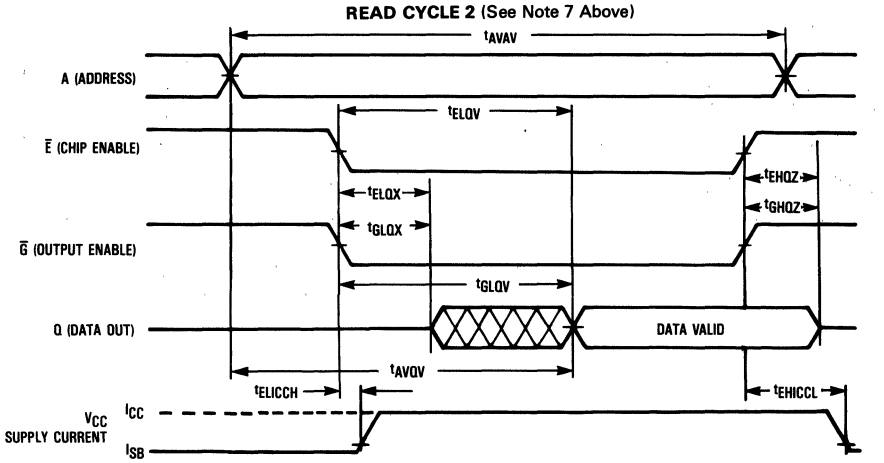
Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	20	–	25	–	35	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	–	20	–	25	–	35	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	–	10	–	12	–	14	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	–	5	–	5	–	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	4	–	5	–	5	–	ns	3,4,5
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	8	0	10	0	15	ns	3,4,5
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	–	0	–	0	–	ns	3,4,5
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	8	0	10	0	15	ns	3,4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	20	–	20	–	30	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$=V_{IL}, $\overline{G}$=V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 6 Above)



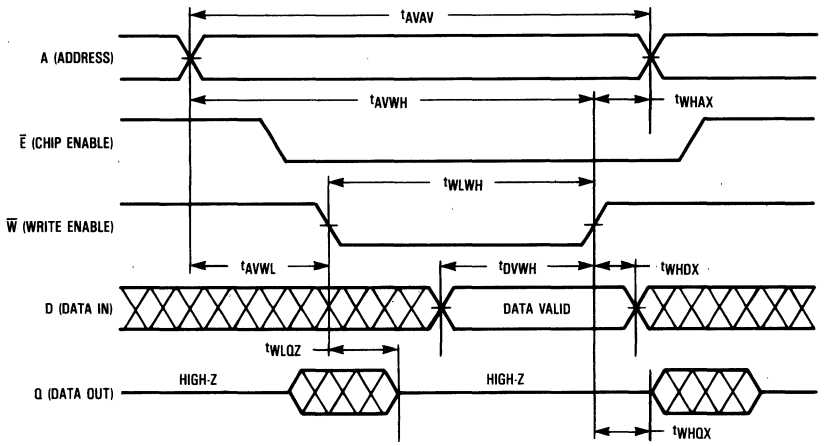
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	20	–	30	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	10	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	15	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	4	–	5	–	5	–	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

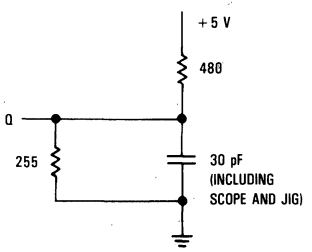


Figure 1A

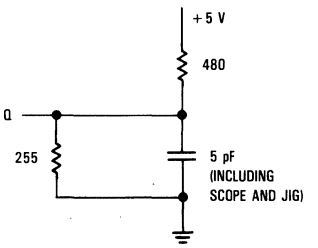
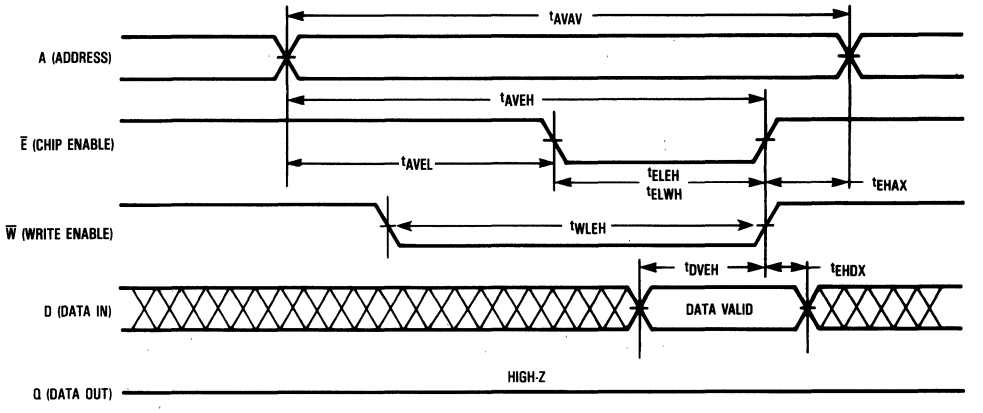


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1 and 2)

Parameter	Symbol		MCM6270-20		MCM6270-25		MCM6270-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	25	–	35	–	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	20	–	30	–	ns	
Chip Enable to End of Write	t_{ELEH}	t_{CW}	15	–	20	–	30	–	ns	4,5
Chip Enable to End of Write	t_{ELWH}	t_{CW}	15	–	20	–	30	–	ns	4,5
Write Pulse Width	t_{WLEH}	t_{WP}	15	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	10	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6270 X XX XX

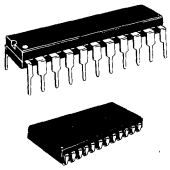
- MCM — Motorola Memory Prefix
- 6270 — Part Number
- X — Package (P = Plastic DIP, J = Plastic SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers—

MCM6270P20	MCM6270P25	MCM6270P35
MCM6270J20	MCM6270J25	MCM6270J35
MCM6270J20R2	MCM6270J25R2	MCM6270J35R2

MCM6287

64K x 1 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

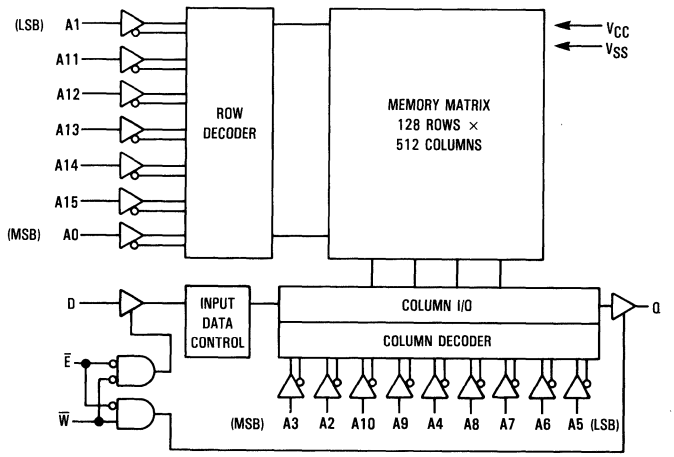
The MCM6287 is a 65,536 bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The MCM6287 is available in a 300 mil, 22 lead plastic DIP and a 24 lead, 300 mil, surface-mount SOJ package. Both feature JEDEC standard pinout.

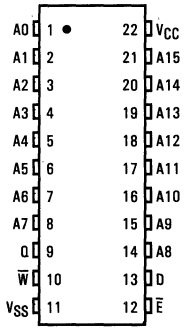
- Single 5 V ±10% Power Supply
- Fast Access Time: 25/35 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120/110 mA Maximum, Active AC
- High Board Density SOJ Available
- Three State Data Output
- Fully TTL Compatible

BLOCK DIAGRAM

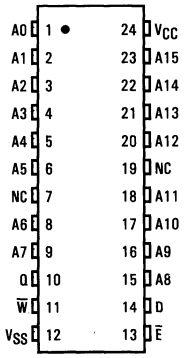


PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6287-25: t_{AVAV}=25 ns	I_{CCA}	—	120	mA
	MCM6287-35: t_{AVAV}=35 ns	I_{CCA}	—	110	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ $\overline{E}$	C_{in}	4 5	6 7	pF
Output Capacitance		C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

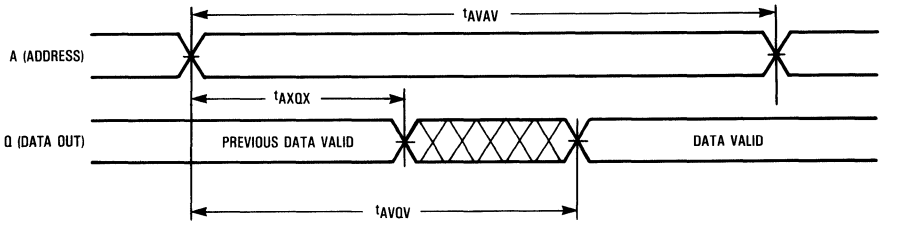
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

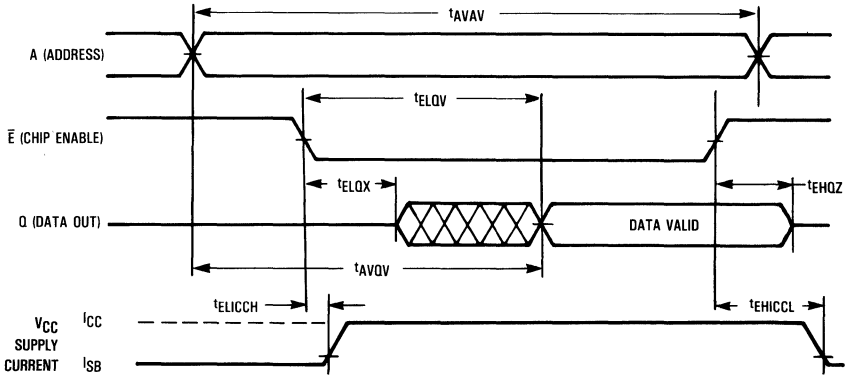
Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$).

READ CYCLE 1 (See Note 7 Above)



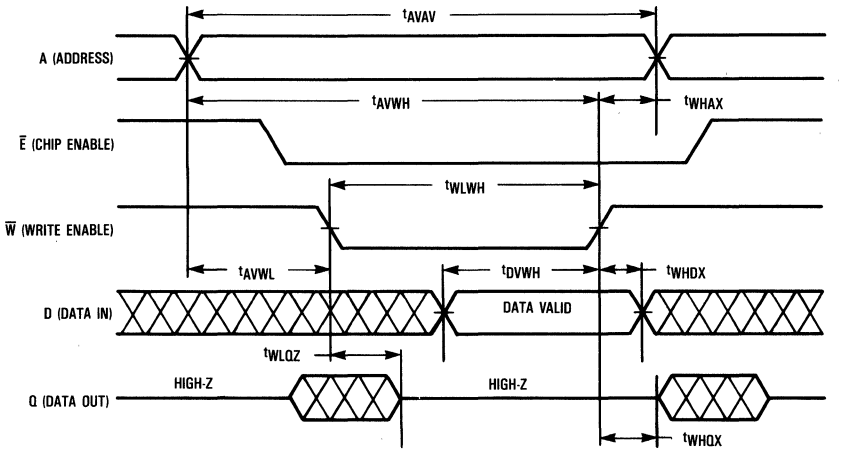
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

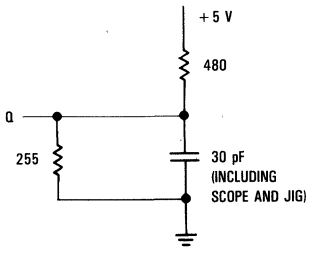


Figure 1A

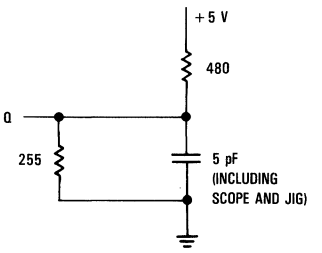


Figure 1B

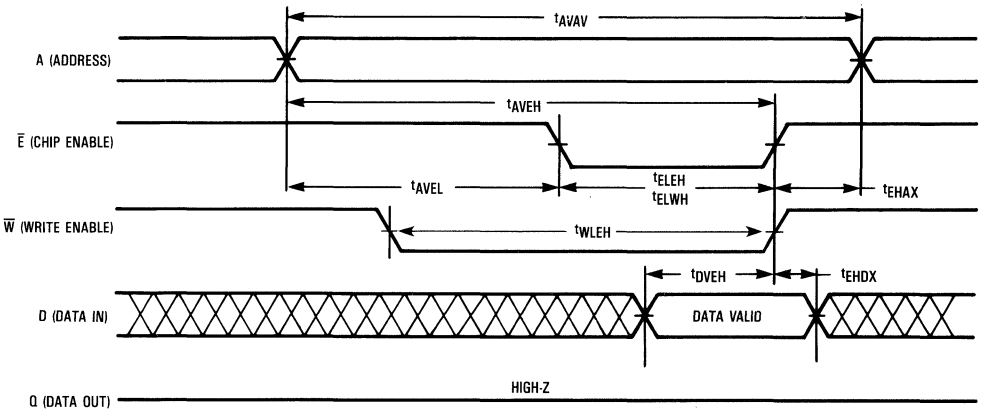
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



TYPICAL CHARACTERISTICS

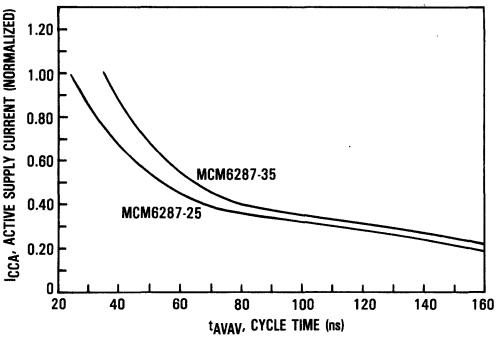


Figure 2. Relative Power versus Cycle Time

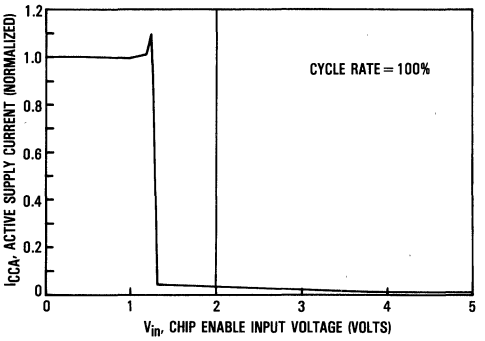


Figure 3. Active Supply Current versus Chip Enable Input Voltage

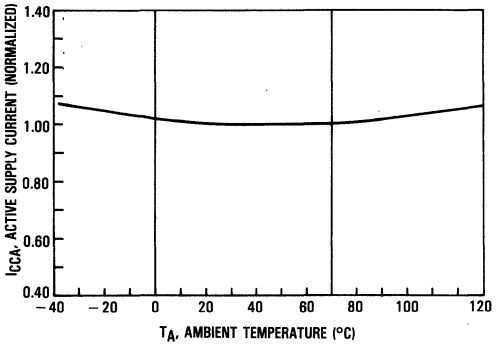


Figure 4. Active Supply Current versus Temperature

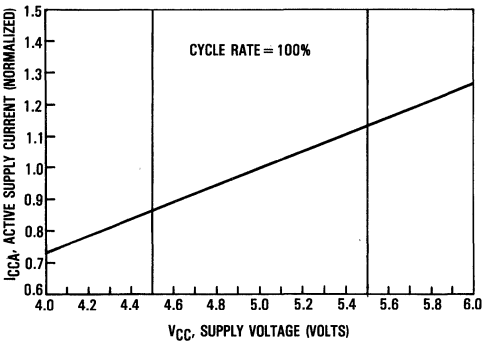


Figure 5. Active Supply Current versus Supply Voltage

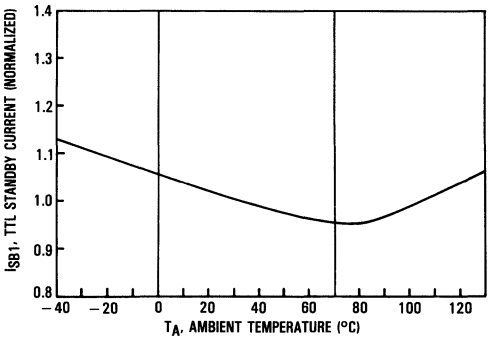


Figure 6. Standby Supply Current versus Temperature

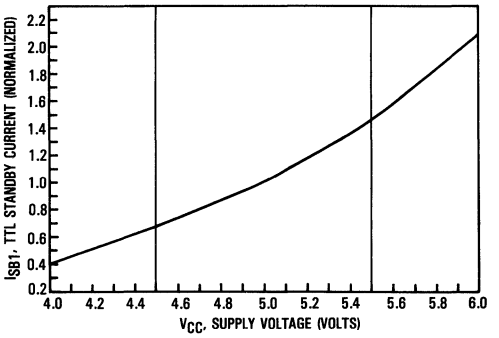


Figure 7. Standby Supply Current versus Supply Voltage

TYPICAL CHARACTERISTICS (Continued)

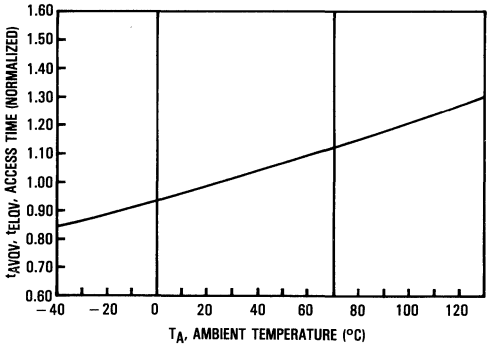


Figure 8. Address and Enable Access Times versus Temperature

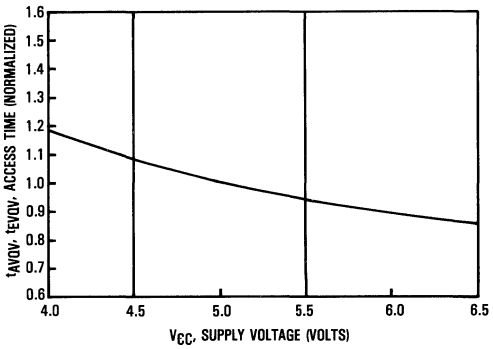


Figure 9. Address and Enable Access Times versus Supply Voltage

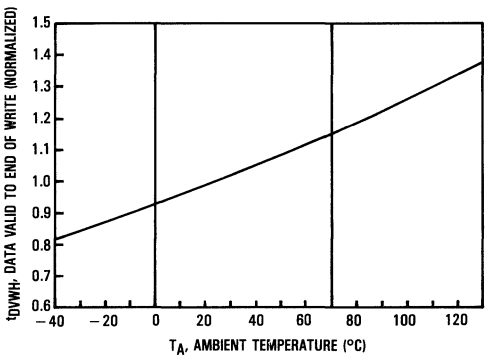


Figure 10. Data Setup Time versus Temperature

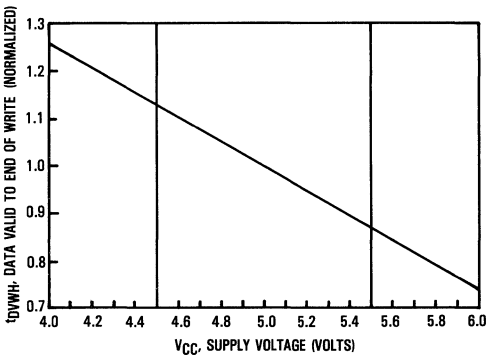


Figure 11. Data Setup Time versus Supply Voltage

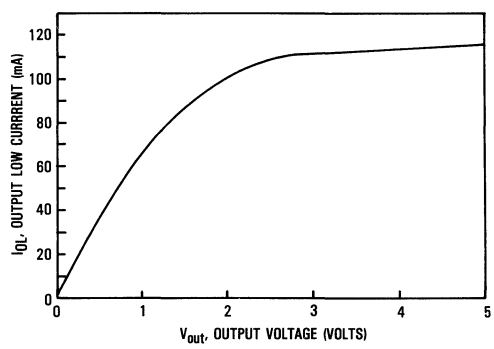


Figure 12. Output Sink Current versus Output Voltage

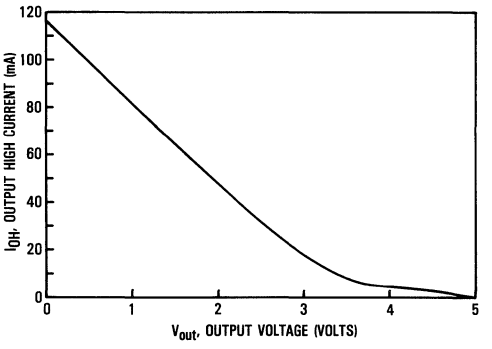
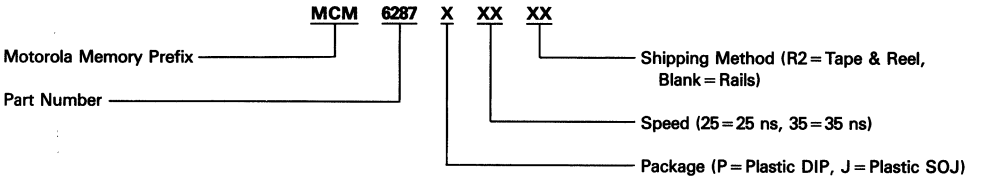


Figure 13. Output Source Current versus Output Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6287P25, MCM6287P35, MCM6287J25, MCM6287J35, MCM6287J25R2, MCM6287J35R2

4

MCM6287-15
MCM6287-20

Advance Information

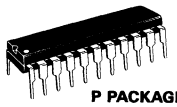
64K x 1 Bit Static Random Access Memory

The MCM6287-15/MCM6287-20 is a 65,536 bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature provides reduced system power requirements without degrading access time performance.

The MCM6287-15/MCM6287-20 is available in a 300 mil, 22 lead plastic DIP or a 24 lead, 300 mil, surface-mount SOJ package. All feature JEDEC standard pinout.

- Single 5 V ±10% Power Supply
- Fast Access Time: 15/20 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 140/130 mA Maximum, Active AC
- High Board Density SOJ
- Three State Data Output
- Fully TTL Compatible

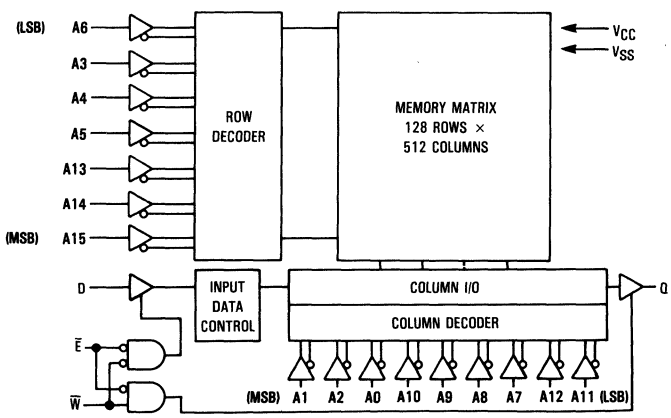


P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

4

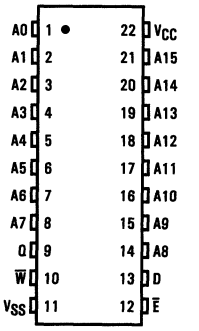
BLOCK DIAGRAM



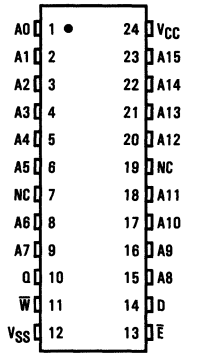
PIN NAMES	
A0-A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	MCM6287-15: t_{AVAV} = 15 ns	I_{CCA}	—	110	140	mA
	MCM6287-20: t_{AVAV} = 20 ns		—	100	130	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	30	40	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	20	30	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
Output Capacitance		C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

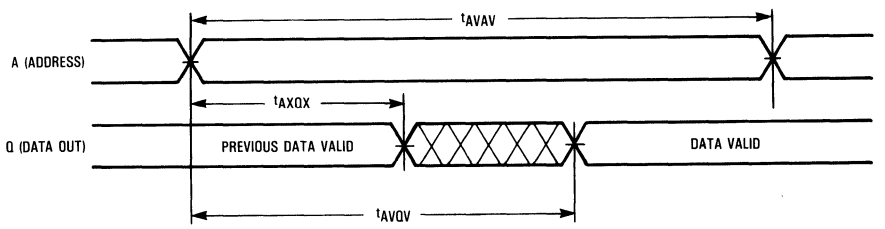
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

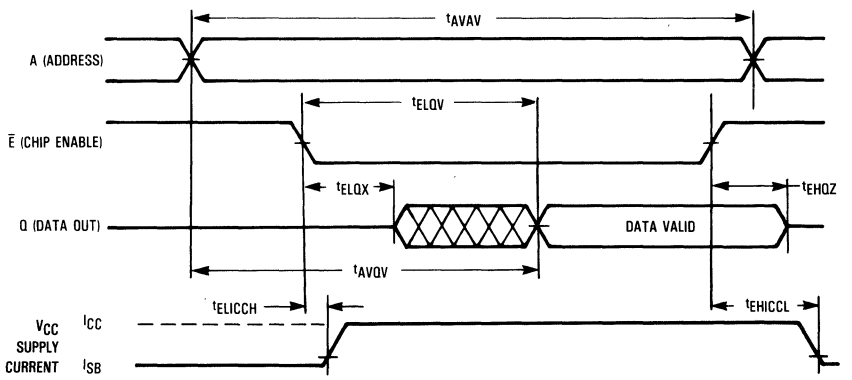
Parameter	Symbol		MCM6287-15		MCM6287-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	–	20	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	15	–	20	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	15	–	20	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	–	4	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	4	–	4	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	6	0	8	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	15	–	20	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$).

READ CYCLE 1 (See Note 7 Above)



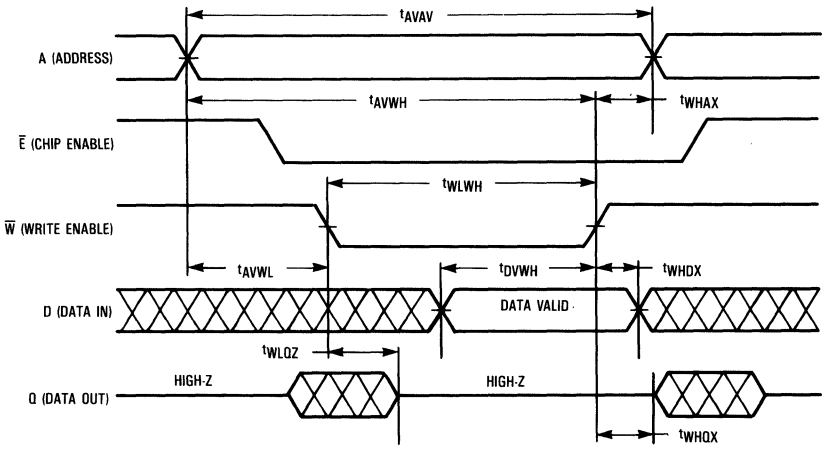
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-15		MCM6287-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	–	20	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	–	15	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	9	–	12	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	–	8	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	5	0	7	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	4	–	5	–	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

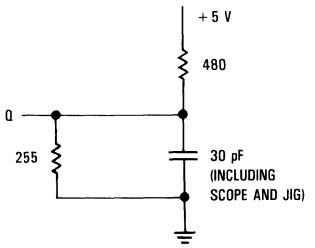


Figure 1A

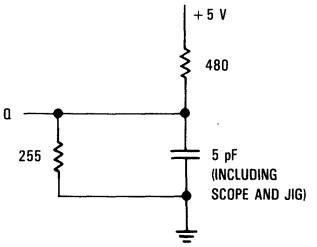


Figure 1B

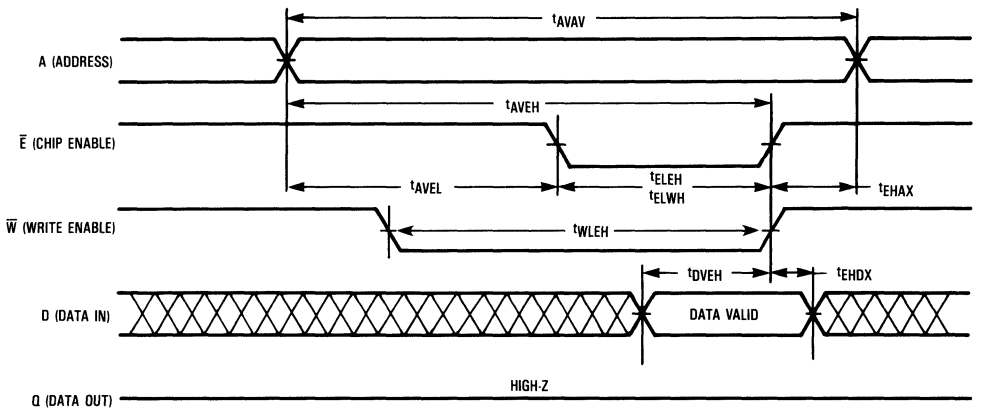
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-15		MCM6287-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	–	20	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	–	15	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	9	–	12	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	9	–	12	–	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	9	–	12	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	–	8	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6287 X XX XX

- MCM — Motorola Memory Prefix
- 6287 — Part Number
- X — Package (P = Plastic DIP, J = Plastic SOJ)
- XX — Speed (15 = 15 ns, 20 = 20 ns)
- XX — Shipping Method (R2 = Tape & Reel, Blank = Rails)

Full Part Numbers — MCM6287P15, MCM6287P20, MCM6287J15, MCM6287J20, MCM6287J15R2, MCM6287J20R2

MCM6288
MCM6290

16K x 4 Bit Static RAMs

The MCM6288 and MCM6290 are 65,536 bit static random access memories organized as 16,384 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

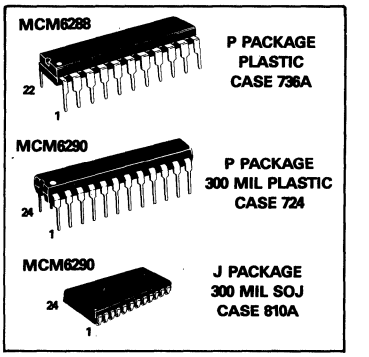
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. These devices also incorporate internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

The MCM6290 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

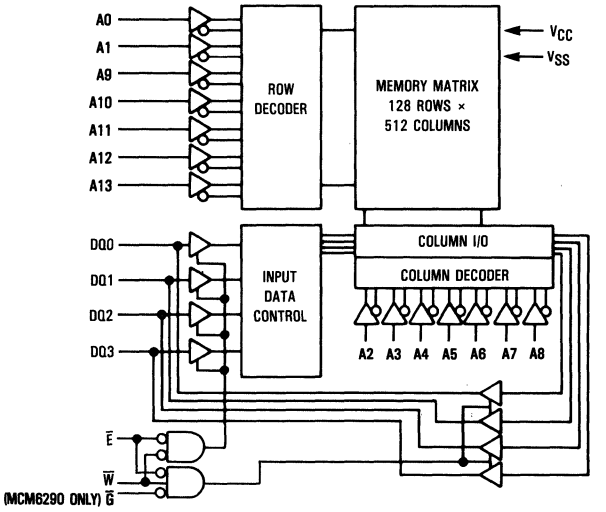
- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

(xx = 88 or 90)	Address	Chip Enable	MCM6290 Output Enable
MCM62xx-25	25 ns	25 ns	12 ns
MCM62xx-30	30 ns	30 ns	15 ns
MCM62xx-35	35 ns	35 ns	15 ns
MCM62xx-45	45 ns	45 ns	20 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6290)
- Low Power Operation: 120/110/100 mA Maximum, Active AC
- Fully TTL Compatible—Three-State Data Output



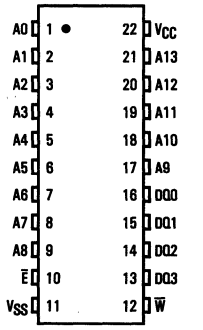
BLOCK DIAGRAM



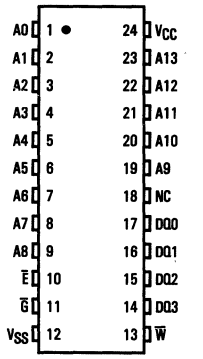
PIN NAMES	
A0-A13 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3. . Data Input/Output	NC . . . . . No Connection
$\overline{W}$. . . . . Write Enable	V_{CC}. . . . +5 V Power Supply
$\overline{G}$ (MCM6290) . . Output Enable	V_{SS}. . . . . Ground

PIN ASSIGNMENT

MCM6288



MCM6290



MCM6288 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	t_{AVAV}=25 ns	I_{CCA}	—	120	mA
	t_{AVAV}=30 ns		—	120	
	t_{AVAV}=35 ns		—	110	
	t_{AVAV}=45 ns		—	100	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

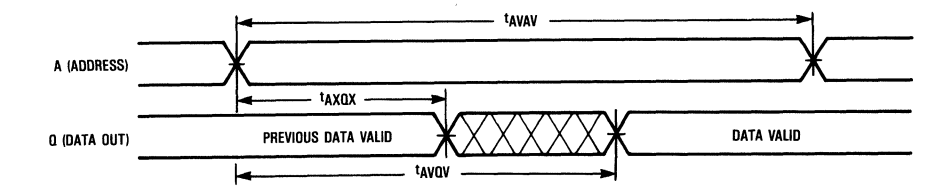
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

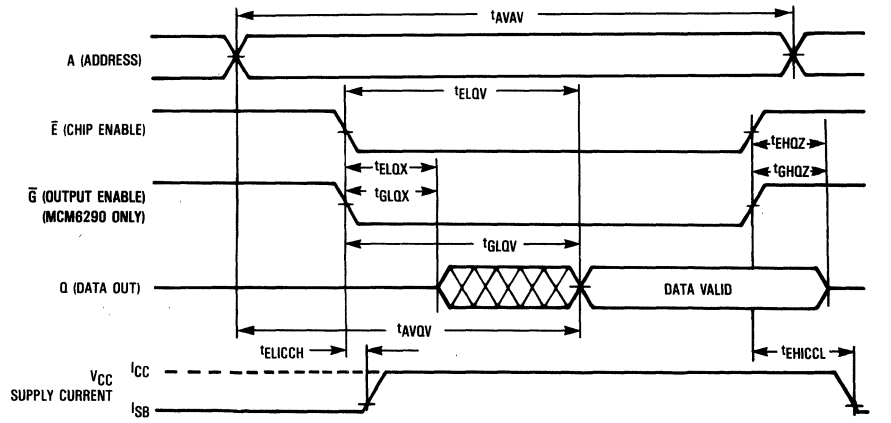
Parameter		Symbol		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		MCM6288-45 MCM6290-45		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	25	–	30	–	35	–	45	–	ns	2
Address Access Time		t_{AVQV}	t_{AA}	–	25	–	30	–	35	–	45	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	–	25	–	30	–	35	–	45	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Enable Access Time	MCM6290	t_{GLQV}	t_{OE}	–	12	–	15	–	15	–	20	ns	
Output Enable Low to Output Active	MCM6290	t_{GLQX}	t_{LZ}	0	–	0	–	0	–	0	–	ns	4,5,6
Output Enable High to Output High-Z	MCM6290	t_{GHQZ}	t_{HZ}	0	10	0	12	0	15	0	15	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	5	–	5	–	5	–	5	–	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	10	0	12	0	15	0	15	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	–	0	–	0	–	0	–	ns	
Power Down Time		t_{EHICCL}	t_{PD}	–	25	–	30	–	30	–	40	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}) and $\overline{G}$ = V_{IL} (MCM6290 only).

READ CYCLE 1 (See Note 7 Above)



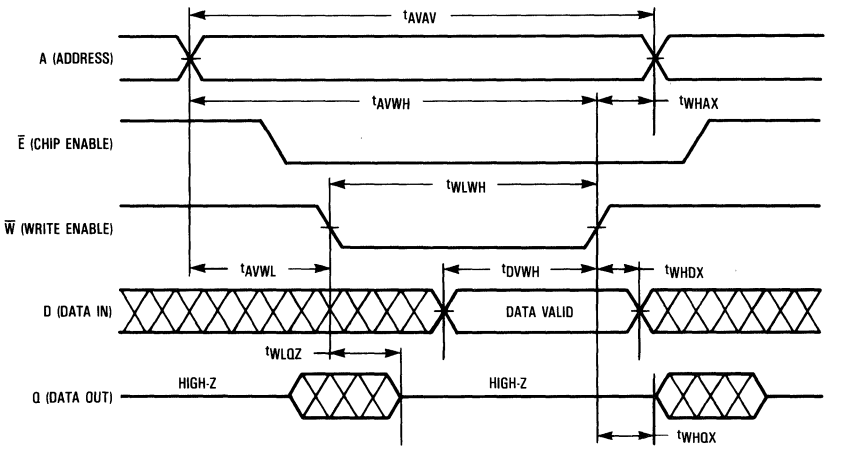
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		MCM6288-45 MCM6290-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	30	—	35	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	12	—	15	—	20	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	12	0	15	0	15	ns	3,4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6290, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

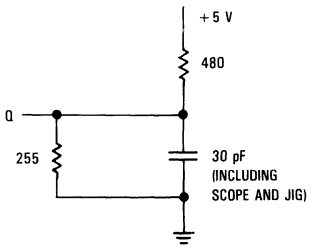


Figure 1A

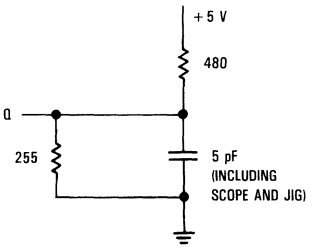
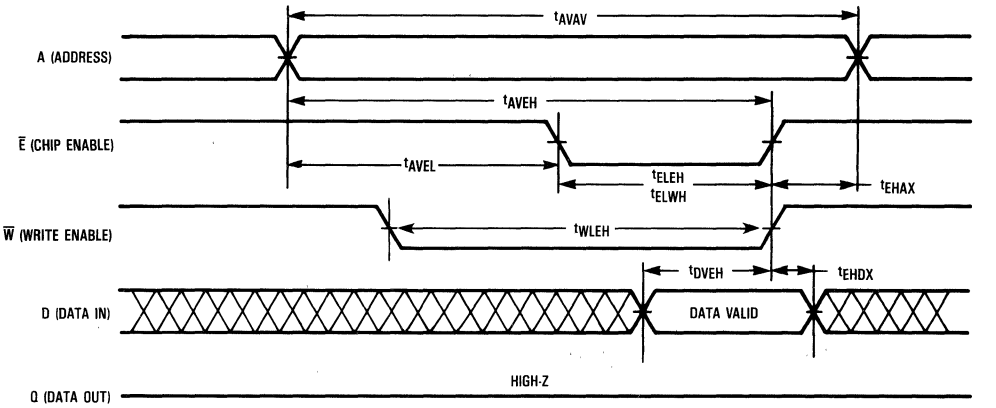


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6288-25 MCM6290-25		MCM6288-30 MCM6290-30		MCM6288-35 MCM6290-35		MCM6288-45 MCM6290-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	30	–	35	–	45	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	–	25	–	30	–	35	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	–	25	–	30	–	35	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	–	25	–	30	–	35	–	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	20	–	25	–	30	–	35	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	12	–	15	–	20	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6290, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62XX X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (25 = 25 ns, 30 = 30 ns, 35 = 35 ns, 45 = 45 ns)

Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers—				
	MCM6288P25	MCM6290P25	MCM6290J25	MCM6290J25R2
	MCM6288P30	MCM6290P30	MCM6290J30	MCM6290J30R2
	MCM6288P35	MCM6290P35	MCM6290J35	MCM6290J35R2
	MCM6288P45	MCM6290P45	MCM6290J45	MCM6290J45R2

MCM6288-15
MCM6290-15

Product Preview

16K x 4 Bit Static RAMs

The MCM6288-15 and MCM6290-15 are 65,536 bit static random access memories organized as 16,384 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

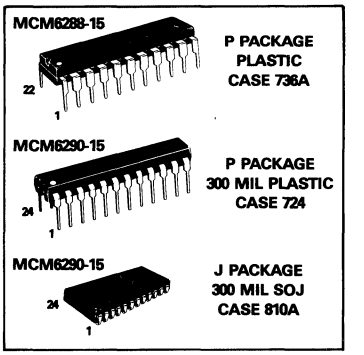
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access time performance.

The MCM6290-15 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

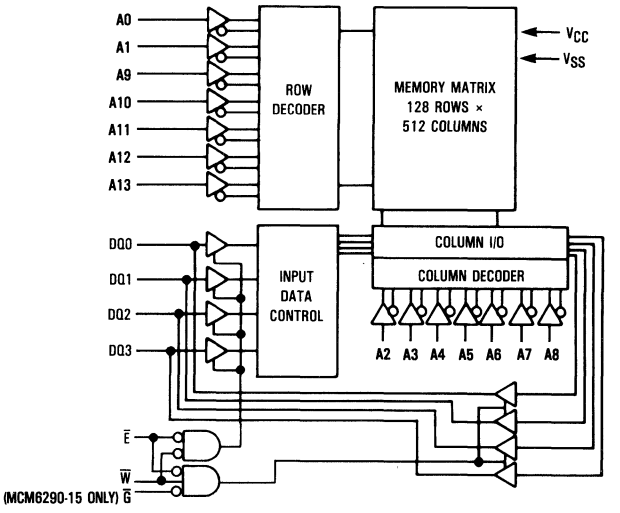
- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

(xx = 88 or 90)	Address	Chip Enable	MCM6290-15 Output Enable
MCM62xx-15	15 ns	15 ns	8 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6290-15)
- Low Power Operation: 140 mA Maximum, Active AC
- Fully TTL Compatible—Three-State Data Output



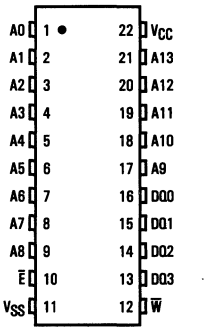
BLOCK DIAGRAM



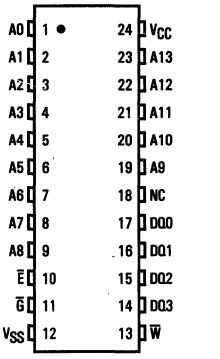
PIN NAMES	
A0-A13 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3. . Data Input/Output	NC . . . . . No Connection
$\overline{W}$. . . . . .Write Enable	V_{CC}. . . . +5 V Power Supply
$\overline{G}$ (MCM6290-15). Output Enable	V_{SS}. . . . . .Ground

PIN ASSIGNMENT

MCM6288-15



MCM6290-15



MCM6288-15 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290-15 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	—	±1.0	μA
AC Supply Current (I_{out}=0 mA) t_{AVAV}=15 ns	I_{CCA}	—	110	140	mA
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	30	40	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	20	30	mA
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

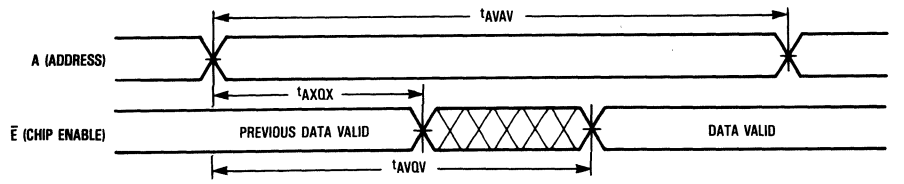
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

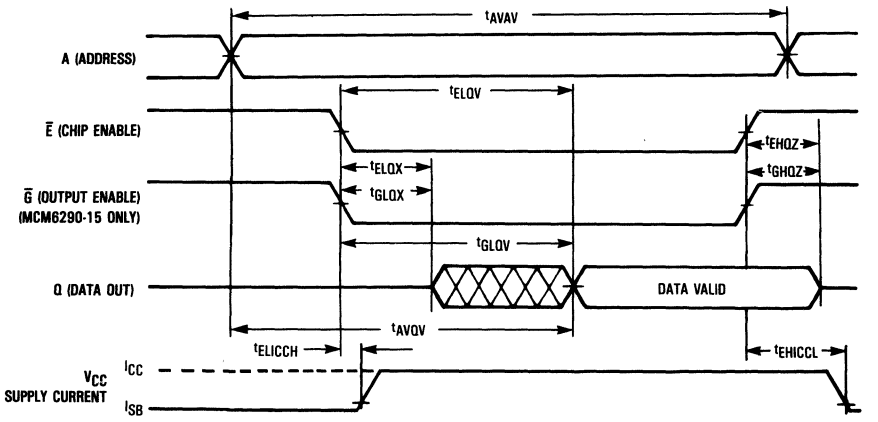
Parameter		Symbol		MCM6288-15 MCM6290-15		Units	Notes
		Standard	Alternate	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	15	–	ns	2
Address Access Time		t_{AVQV}	t_{AA}	–	15	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	–	15	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	4	–	ns	
Output Enable Access Time	MCM6290-15	t_{GLQV}	t_{OE}	–	8	ns	
Output Enable Low to Output Active	MCM6290-15	t_{GLQX}	t_{LZ}	2	–	ns	4,5,6
Output Enable High to Output High-Z	MCM6290-15	t_{GHQZ}	t_{HZ}	0	5	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	4	–	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	6	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	–	ns	
Power Down Time		t_{EHICCL}	t_{PD}	–	15	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}) and $\overline{G}$ = V_{IL} (MCM6290-15 only).

READ CYCLE 1 (See Note 7 Above)



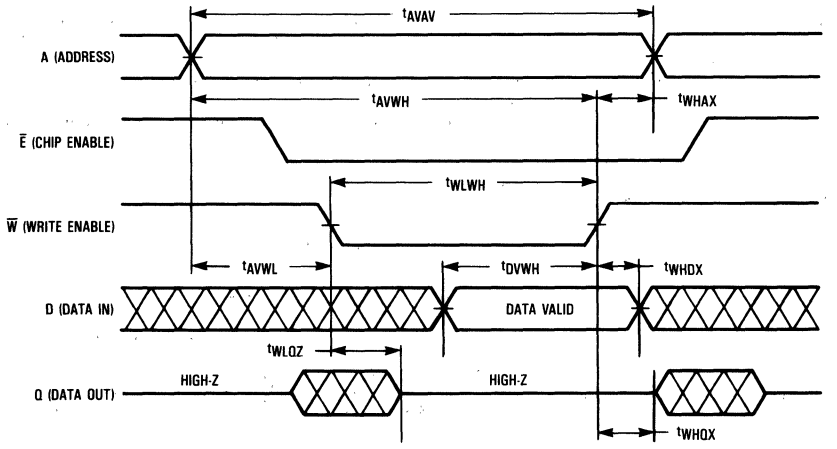
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6288-15 MCM6290-15		Units	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	5	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6290-15, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

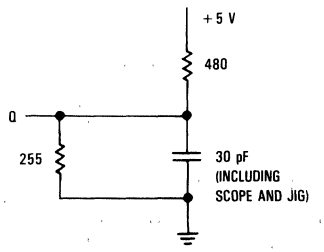


Figure 1A

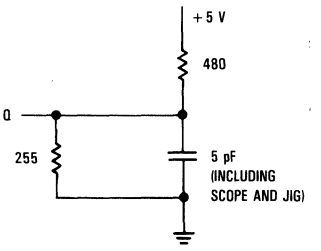
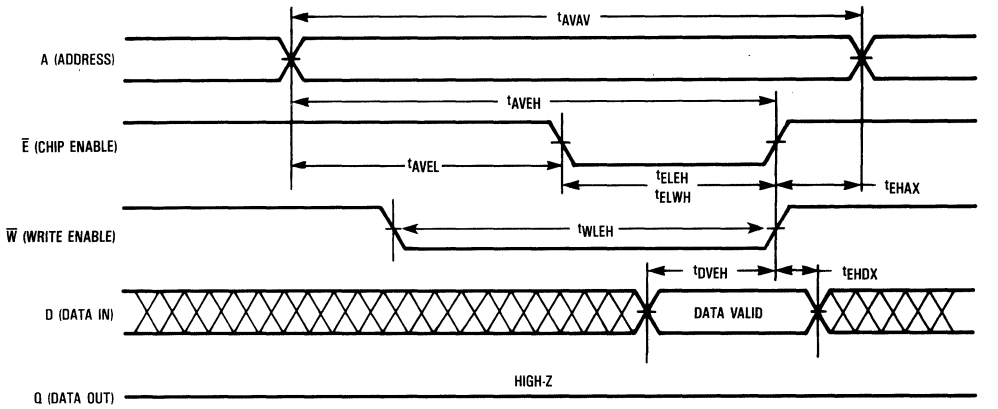


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6288-15 MCM6290-15		Units	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	9	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	9	–	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	9	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6290-15, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62XX X XX XX

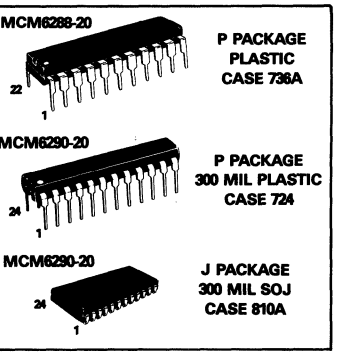
- MCM: Motorola Memory Prefix
- 62XX: Part Number
- X: Package (P = Plastic DIP, J = Plastic SOJ)
- XX: Speed (15 = 15 ns)
- XX: Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers—MCM6288P15 MCM6290P15 MCM6290J15 MCM6290J15R2

MCM6288-20
MCM6290-20

Advance Information

16K x 4 Bit Static RAMs



The MCM6288-20 and MCM6290-20 are 65,536 bit static random access memories organized as 16,384 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. These devices also incorporate internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

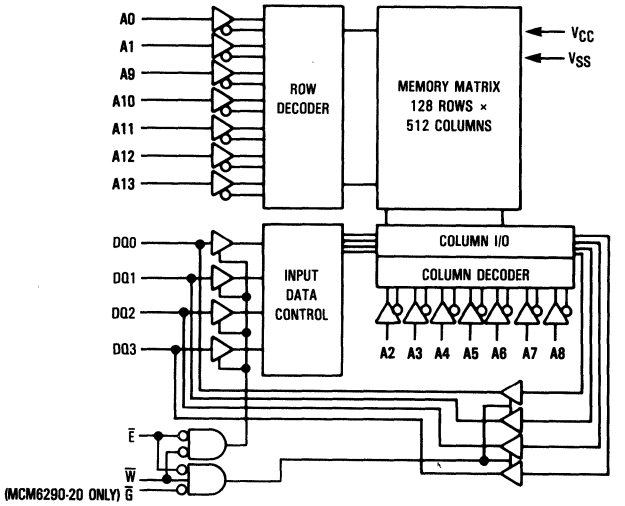
The MCM6290-20 has both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V ±10% Power Supply
- Fast Access Time (Maximum):

(xx = 88 or 90)	Address	Chip Enable	MCM6290-20 Output Enable
MCM62xx-20	20 ns	20 ns	10 ns

- Equal Address and Chip Enable Access Time
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems (MCM6290-20)
- Low Power Operation: 120 mA Maximum, Active AC
- Fully TTL Compatible—Three-State Data Output

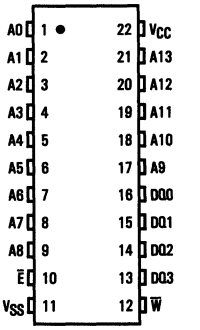
BLOCK DIAGRAM



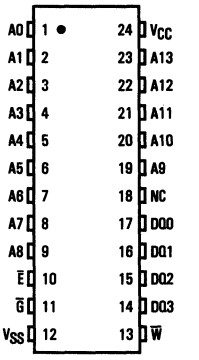
PIN NAMES	
A0-A13 . . . . . Address Input	$\overline{E}$ . . . . . Chip Enable
DQ0-DQ3. . Data Input/Output	NC . . . . . No Connection
$\overline{W}$ . . . . . Write Enable	V_{CC}. . . . +5 V Power Supply
$\overline{G}$ (MCM6290-20). Output Enable	V_{SS}. . . . . Ground

PIN ASSIGNMENT

MCM6288-20



MCM6290-20



This document contains information on a new product. Specifications and information here are subject to change without notice.

MCM6288-20 TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

MCM6290-20 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA) t_{AVAV}=20 ns	I_{CCA}	—	120	mA
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance All Inputs Except $\overline{E}$	C_{in}	4	6	pF
Input Capacitance $\overline{E}$		5	7	
I/O Capacitance	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

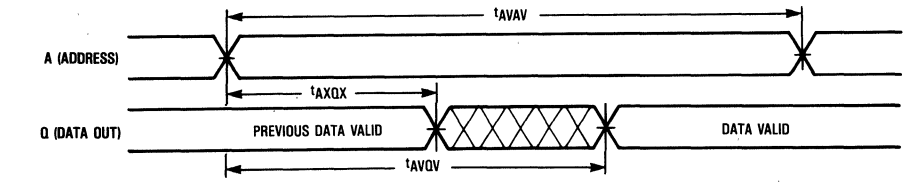
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

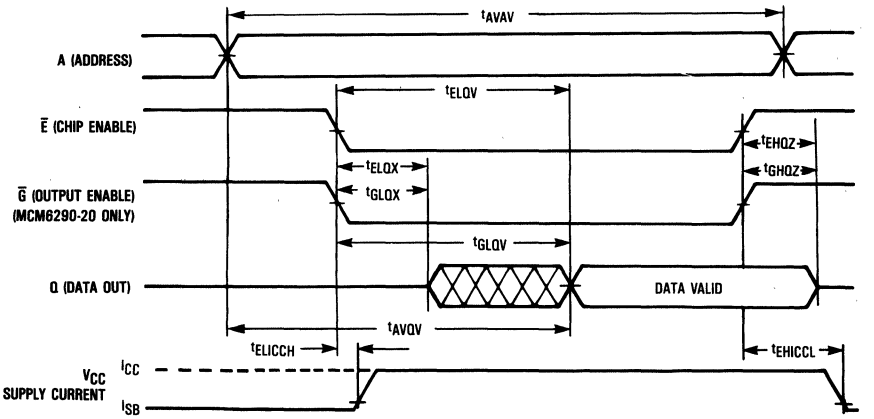
Parameter		Symbol		MCM6288-20 MCM6290-20		Units	Notes
		Standard	Alternate	Min	Max		
Read Cycle Time		t_{AVAV}	t_{RC}	20	—	ns	2
Address Access Time		t_{AVQV}	t_{AA}	—	20	ns	
Enable Access Time		t_{ELQV}	t_{ACS}	—	20	ns	3
Output Hold from Address Change		t_{AXQX}	t_{OH}	4	—	ns	
Output Enable Access Time	MCM6290-20	t_{GLQV}	t_{OE}	—	10	ns	
Output Enable Low to Output Active	MCM6290-20	t_{GLQX}	t_{LZ}	0	—	ns	4,5,6
Output Enable High to Output High-Z	MCM6290-20	t_{GHQZ}	t_{HZ}	0	8	ns	4,5,6
Enable Low to Output Active		t_{ELQX}	t_{LZ}	4	—	ns	4,5,6
Enable High to Output High-Z		t_{EHQZ}	t_{HZ}	0	8	ns	4,5,6
Power Up Time		t_{ELICCH}	t_{PU}	0	—	ns	
Power Down Time		t_{EHICCL}	t_{PD}	—	20	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}) and $\overline{G}$ = V_{IL} (MCM6290-20 only).

READ CYCLE 1 (See Note 7 Above)



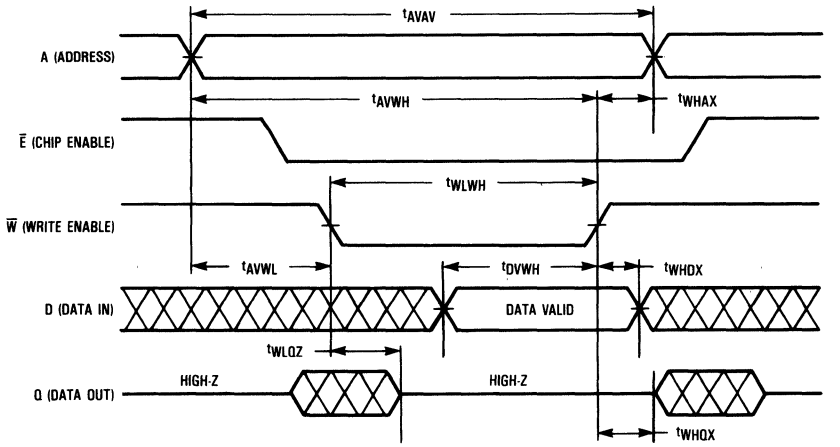
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 6)

Parameter	Symbol		MCM6288-20 MCM6290-20		Units	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	–	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
6. MCM6290-20, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



AC TEST LOADS

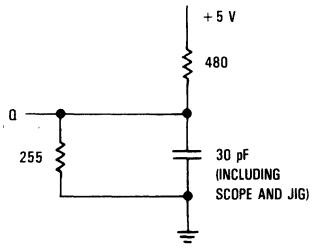


Figure 1A

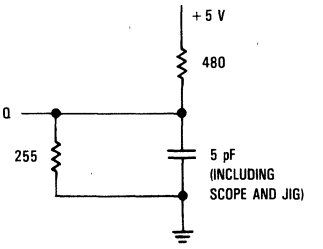
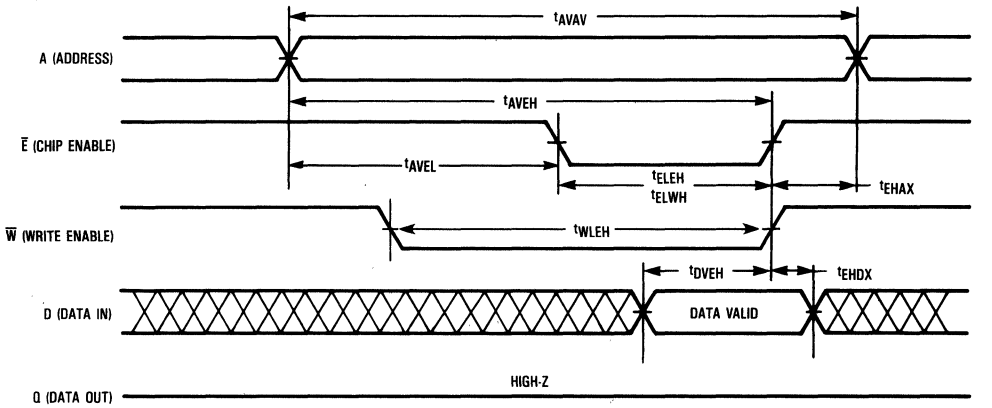


Figure 1B

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 5)

Parameter	Symbol		MCM6288-20 MCM6290-20		Units	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	15	–	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	15	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.
5. MCM6290-20, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62XX X XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (20 = 20 ns)

Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers—MCM6288P20 MCM6290P20 MCM6290J20 MCM6290J20R2

Special Application MOS Static RAMs

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Synchronous Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
16K × 4	MCM6292P25*	25	28
	MCM6292P30*	30	28
	MCM6292P35*	35	28
	MCM6292J25*	25	28
	MCM6292J30*	30	28
	MCM6292J35*	35	28
	MCM6293P20*	20	28
	MCM6293P25*	25	28
	MCM6293P30*	30	28
	MCM6293J20*	20	28
	MCM6293J25*	25	28
	MCM6293J30*	30	28
	MCM6294P20*	20	28
	MCM6294P25	25	28
	MCM6294P30	30	28
	MCM6294J20*	20	28
	MCM6294J25	25	28
	MCM6294J30	30	28
	MCM6295P25	25	28
	MCM6295P30	30	28
	MCM6295P35	35	28
	MCM6295J25	25	28
	MCM6295J30	30	28
	MCM6295J35	35	28
4K × 10	MCM62963FN20*	20	44
	MCM62963FN25*	25	44
	MCM62963FN30*	30	44
	MCM62964FN20*	20	44
	MCM62964FN25*	25	44
	MCM62964FN30*	30	44
	MCM62965FN25*	25	44
	MCM62965FN30*	30	44
	MCM62965FN35*	35	44
4K × 12	MCM62973FN20*	20	44
	MCM62973FN25*	25	44
	MCM62973FN30*	30	44
	MCM62974FN20*	20	44
	MCM62974FN25*	25	44
	MCM62974FN30*	30	44
	MCM62975FN25*	25	44
	MCM62975FN30*	30	44
	MCM62975FN35*	35	44

CMOS Dual Port RAM

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
256 × 8	MCM68HC34L	240	40
	MCM68HC34P	240	40

Cache Tag RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Address to Match Time (ns max)	Pins
4K × 4	MCM62350P20*	20	24
	MCM62350P22*	22	24
	MCM62350P25	25	24
	MCM62350P30	30	24
	MCM62350J20*	20	24
	MCM62350J22*	22	24
	MCM62350J25	25	24
	MCM62350J30	30	24
	MCM62351P20*	20	24
	MCM62351P22*	22	24
	MCM62351P25	25	24
	MCM62351P30	30	24
	MCM62351J20*	20	24
	MCM62351J22*	22	24
	MCM62351J25	25	24
	MCM62351J30	30	24
	MCM4180P20*	20	22
	MCM4180P22*	22	22
	MCM4180P25	25	22
	MCM4180P30	30	22
	MCM5180J20*	20	24
	MCM4180J22*	22	24
	MCM4180J25	25	24
	MCM4180J30	30	24

*To be introduced

MCM68HC34

Advance Information

Dual-Port RAM Memory Unit

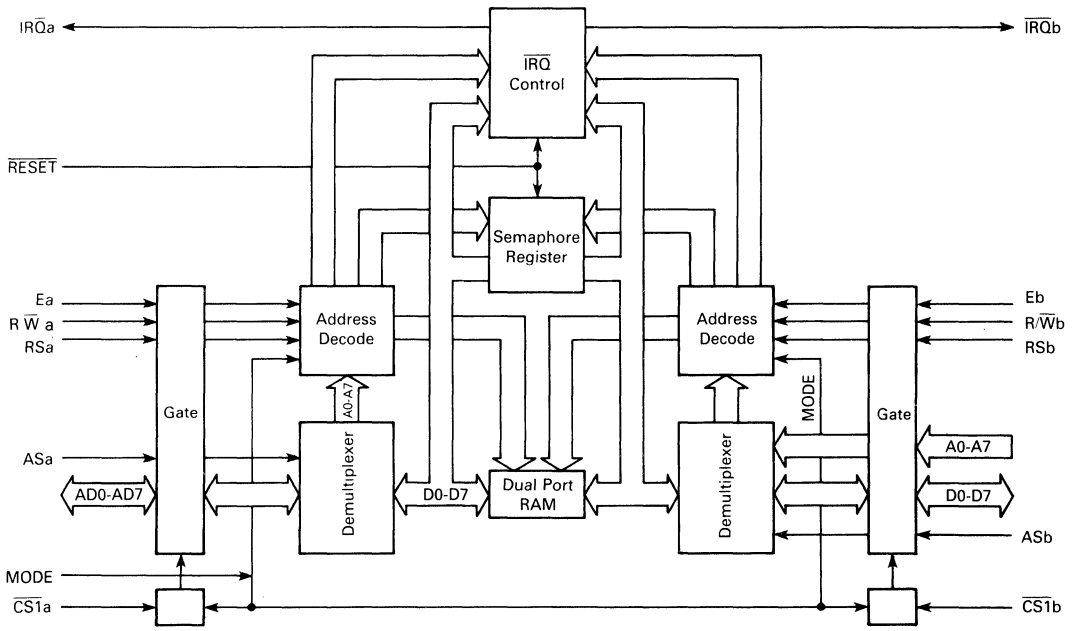
The MCM68HC34 is a dual-port RAM memory (DPM) unit which enables two processors, arbitrarily referred to a "A" and "B", operating on two separate buses to exchange data without interfering with devices on the other bus. It contains 256 bytes of dual-port RAM which is the medium actually used for the interchange of data.

The dual-port memory unit contains six semaphore registers that provide a means for controlling access to the dual-port RAM or any other shared resources. It also contains interrupt registers which provide a means for the processors to interrupt each other.

- High-Speed CMOS (HCMOS) Structure
- Six Read Write Semaphore Registers
- 256 Bytes of Dual-Port RAM
- Eight Address Lines

5

FIGURE 1 — BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

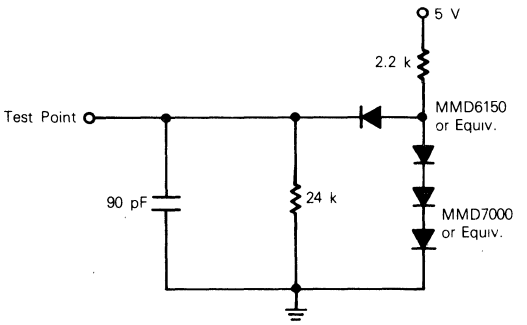
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage, All Inputs	V_{in}	V_{SS}−0.3 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		C W
Cerdip		60	
Plastic		100	
PLCC		60	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Unused inputs must be tied to an appropriate logic level (either V_{CC} or V_{SS}) to reduce leakage currents and increase reliablity.

FIGURE 2 — BUS TIMING LOAD



DC ELECTRICAL CHARACTERISTCS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Input High Voltage (see Note 1)	V_{IH}	2 0	V_{CC}+0.3	V
Input Low Voltage (see Note 2)	V_{IL}	V_{SS}−0.3	0.8	V
Input Current (V_{in} = 0 to V_{CC})	I_{in}	–	1.0	μA
Output Leakage Current	I_{OZ}	–	10.0	μA
Output High Voltage (I_{Load} = − 100 μA)	V_{OH}	2.4	–	V
(I_{Load} = < 10.0 μA)		V_{CC}−0.1	–	
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	0.4	V
(I_{Load} = < 10.0 μA)		–	0.1	
Current Drain — Outputs Unloaded Operating — Ea, Eb = 1 MHz, Both Sides Active	I_{DD}	–	30	mA
Input Capacitance	C_{in}	–	10	pF
Output Capacitance (AD0-AD7 and D0-D7)	C_{out}	–	12	pF

NOTES:
1. Input high voltage as stated is for all inputs except MODE. In the case of MODE, input high voltage is tied to V_{CC}.
2. Input low voltage as stated is for all inputs except MODE. In the case of MODE, input low voltage is tied to V_{SS} or is floating. If floating, the voltage will be internally pulled to V_{SS}.

BUS TIMING (See Notes 1 and 2 and Figure 2)

Ident Number	Characteristics	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	800	–	ns
2	Pulse Width, E Low	P_{WEL}	300	–	ns
3	Pulse Width, E High	P_{WEH}	325	–	ns
4	Input Rise and Fall Time	t_r, t_f	–	30	ns
8	Read/Write Hold Time	t_{RWH}	10	–	ns
9	Non-Multiplexed Address, RS Hold Time	t_{AH}	10	–	ns
12	Non-Multiplexed Address, RS Valid Time to Eb	t_{AV}	20	–	ns
13	R/$\overline{W}$, Chip Select Setup Time	t_{RWS}	20	–	ns
15	Chip Select Hold Time	t_{CH}	0	–	ns
18	Read Data Hold Time	t_{DHR}	20	75	ns
21	Write Data Hold Time	t_{DHW}	10	–	ns
24	Address Setup Time for Latch	t_{ASL}	20	–	ns
25	Address Hold Time for Latch	t_{AHL}	20	–	ns
26	Delay Time E to AS Rise	t_{ASD}	60	–	ns
27	Pulse Width, AS High	PW_{ASH}	110	–	ns
28	Address Strobe to E Delay	t_{ASED}	20	–	ns
30	Read Data Delay Time	t_{DDR}	–	240	ns
31	Write Data Setup Time	t_{DSW}	100	–	ns

NOTES:
1. Timing numbers relative to one side only. No numbers are intended to be cross-referenced from one side to the other.
2. Measurement points shown for ac timing are 0.8 V and 2.0 V, unless otherwise specified.

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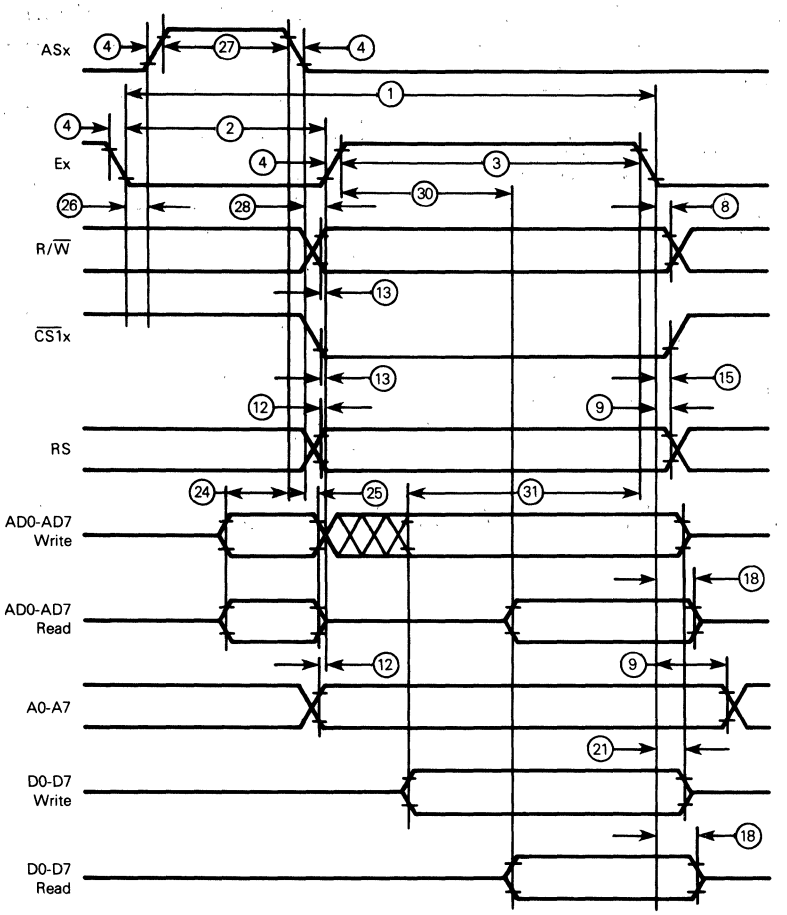
BUS TIMING DIAGRAMS



SIGNAL DESCRIPTION

The following paragraphs contain a brief description of the input and output signals.

V_{CC} AND V_{SS}

These pins supply power to the DPM. V_{CC} is +5 volts ±5% and V_{SS} is 0 volts or ground.

E CLOCK INPUTS (Ea AND Eb)

These are the input clocks from the respective processors and are positive during the latter portion of the bus cycle.

REGISTER SELECT INPUTS (RSa AND RSb)

These inputs function as register select inputs. A high on the RSa for side A or RSb for side B input allows selection of the semaphore and interrupt registers respectively for side A and side B by the lower three address bits. A low on RSa or RSb selects 256 bytes of RAM from side A or side B respectively.

CHIP SELECT INPUTS ($\overline{CS1}$a AND $\overline{CS1}$b)

These inputs function as chip select inputs for their respective sides. $\overline{CS1}$a must be low to select side A and $\overline{CS1}$b must be low to select side B. If $\overline{CS1}$a is high, side A is deselected. If $\overline{CS1}$b is high, side B is deselected.

MODE SELECT (MODE)

In normal operation, this pin should always be connected to V_{CC} (MODE = 1). Each side has three states controlled by RSa and $\overline{CS1}$a for side A and RSb and $\overline{CS1}$b for side B.

If $\overline{CS1}$a is high, side A cannot be accessed. If $\overline{CS1}$a is low, side A accesses either 256 bytes of RAM or the six semaphore registers and the two interrupt registers depending on the level of RSa. If RSa is low, 256 bytes of RAM are accessed and if RSa is high, the six semaphores and two interrupt registers are accessed.

The six semaphore and two interrupt registers are redundantly mapped in the 256 byte mode. That is, only the low order three bits select one of eight registers and the upper five bits of address are not decoded. Refer to Table 1.

TABLE 1 — SIDE A CONTROL SIGNAL OPERATION

Mode	$\overline{CS1}$a	RSa	Operation
1	0	0	Access 256 Byte RAM Side A
1	0	1	Access Semaphore/$\overline{IRQ}$ Side A on Lower Three Bits of Address
1	1	X	Side A Not Selected

The three states for side B in the 256 byte mode are controlled in the manner as side A using RSb and $\overline{CS1}$b except that side B uses separated address and data inputs. Refer to Table 2.

TABLE 2 — SIDE B CONTROL SIGNAL OPERATION

Mode	$\overline{CS1}$b	RSb	Operation
1	0	0	Access 256 Byte RAM Side B
1	0	1	Access Semaphore/$\overline{IRQ}$ Side B on Lower Three Bits of Address
1	1	X	Side B Not Selected

INTERRUPT REQUEST OUTPUTS ($\overline{IRQ}$a AND $\overline{IRQ}$b)

These pins are active low open-drain outputs. A write to address F9 from one side asserts an interrupt, if not masked on the other side. A write to address F9 sets this pin low.

B SIDE ADDRESS BUS INPUTS (A0-A7) AND B SIDE BIDIRECTIONAL DATA BUS (D0-D7)

When the B side is run from a multiplexed bus processor, the B side address pins are connected to the B side data pins, respectively (A0 to D0, A1 to D1, etc.).

SYSTEM RESET INPUT ($\overline{RESET}$)

A low level on this input causes the semaphore registers to be set to the states shown in Table 5 under **SEMAPHORE REGISTERS** and clears both bits of both $\overline{IRQ}$ registers to zeros. The RAM data is unaffected by $\overline{RESET}$.

ADDRESS STROBE INPUTS (ASa AND ASb)

The ASa input demultiplexes the eight low order address lines from the data lines on the A side. The falling edge of ASa latches the A side address within the DPM. The ASb input is used in the same manner when the B side is connected to a multiplexed bus. It must be connected to a high level when the B side is connected to a non-multiplexed bus.

A SIDE MULTIPLEXED ADDRESS/ BIDIRECTIONAL DATA BUS (AD0-AD7)

The A side can only be used with a multiplexed address/data bus. The A side addresses are on these lines during the time ASa is high. The lines are used as bidirectional data lines during the time Ea is high.

DUAL-PORT RAM

The dual-port memory unit contains 256 bytes of dual-port RAM that is accessed from either processor. It is selected in either case by eight address lines, register select, and chip select inputs. The direction of data transfer is controlled by the respective read/write (R/$\overline{W}$a or R/$\overline{W}$b) line. The dual-port RAM enables the processors to exchange data without interfering with devices on the other bus.

Simultaneous accesses by both sides of different locations of dual-port RAM will cause no ambiguities. Simultaneous reads by both sides of the same dual-port RAM location gives the proper data to both sides. On a simultaneous write and read of the same location, the data written is put into RAM but the data read is undefined. Simultaneous writes to

the same RAM location result in undefined data being stored. Thus, simultaneous writes and simultaneous write and read to the same location should be avoided. The semaphore registers provide a tool for determining when the shared RAM is available.

SEMAPHORE REGISTERS

The dual-port memory unit contains six read/write semaphore registers. Only two bits of each register are used. Bit 7 is the semaphore (SEM) bit and bit 6 is the ownership (OWN) bit. The remaining six bits will read all zeros.

Each semaphore register is able to arbitrate simultaneous accesses to it. The semaphore register bits provide a mechanism for controlling accesses to the shared RAM but there are no hardware controls of the dual-port RAM by the semaphore registers.

Table 3 is the truth table for when a semaphore register is accessed by one of the processors. When a semaphore register is written, the actual data written is disregarded but the SEM bit is set to zero. When the register is read, the resulting SEM bit is one (for the next read). The data obtained from the read is interpreted as: SEM bit equals zero — resource available, SEM bit equals one — resource not available.

TABLE 3 — ONE PROCESSOR SEMAPHORE BIT TRUTH TABLE

Original SEM Bit	R/$\overline{W}$	Data Read	Resulting SEM Bit
0	R	0*	1
1	R	1*	1
0	$\overline{W}$	—	0
1	$\overline{W}$	—	0

*0 = Resource Available
1 = Resource Not Available

Table 4 shows the truth table if both processors read or read and write the same semaphore register at the same time. The A processor always reads the actual SEM bit. The B processor reads the SEM bit except during the simultaneous read of a clear SEM bit. This ensures that during a simultaneous read, only the A processor reads a clear SEM bit and therefore has priority to the shared RAM.

TABLE 4 — SIMULTANEOUS ACCESS OF OF SEMAPHORE REGISTER TRUTH TABLE

Original	A Processor		B Processor		Resulting
SEM Bit	R/$\overline{W}$	Data Read	R/$\overline{W}$	Data Read	SEM Bit
0	R	0*	R	1*	1
1	R	1*	$\overline{W}$	—	0
1	$\overline{W}$	—	R	1*	0
1	R	1*	R	1*	1

*0 = Resource Available
1 = Resource Not Available

The ownership bit is a read-only bit that indicates which processor last set the SEM bit. The OWN bit is set to a one whenever the SEM bit is set from zero to one. The OWN bit as read by one processor is the complement of the bit read by the other processor.

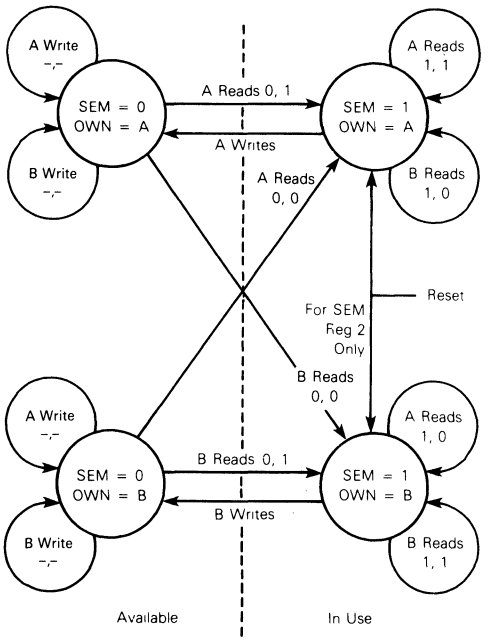
The reset state of the semaphore registers is defined in Table 5. The A processor owns all of the semaphore registers except the second semaphore register which is owned by the B processor.

TABLE 5 — RESET STATE OF SEMAPHORE REGISTERS

Semaphore Register Number	A Processor		B Processor	
	SEM Bit	OWN Bit	SEM Bit	OWN Bit
1	1	1	1	0
2	1	0	1	1
3	1	1	1	0
4	1	1	1	0
5	1	1	1	0
6	1	1	1	0

A state diagram for a semaphore register is shown in Figure 3.

FIGURE 3 — STATE DIAGRAM FOR SEMAPHORE REGISTER



NOTES:
1. Writes to a semaphore register are valid only if SEM = 1 and OWN = 1.
2. When A and B simultaneously read a semaphore register, the hardware handles it as a read by A followed by a read by B.

INTERRUPT REGISTERS

The dual-port memory unit contains two addressable locations at F8 and F9 on both sides that control the interrupt ($\overline{IRQ}$) operation between the processors. Although there is only one hardware register for each side, for purposes of explanation the register accessed at location F8 is referred to

as the IRQX status register and the register accessed at location F9 is referred to as the IRQX control register (refer to Table 6). The registers each consisting of two bits have identical bit arrangements. Bit 6 is the enable bit and bit 7 is the flag bit. The other six bits are not used and always read as zero. When $\overline{RESET}$ is asserted, both bits are cleared to zero.

Table 7 summarizes the bits involved when reading or writing to the status or control registers at F8 or F9. The enable bits on either side (A or B) track the data that is written into the status register from that side. Writes to the control register do not alter data. The actual data written is disregarded but the action sets the flag bit in the other side's register and asserts an interrupt signal if enabled.

The following describes how the B side interrupt is asserted from the A side. The A side interrupt is controlled in a similar manner.

When the enable bit in the IRQb status register is set (bit 6 = 1), a write to IRQa control register sets the flag bit in the IRQb status register (bit 7 = 1) and causes an interrupt on the B side by setting the IRQb pin low. Reading the IRQb status register reads the state of the B side enable and flag bits. Reading the IRQb control register also reads the enable and flag bits but in addition, clears the B side flag bit (bit 7 = 0) and clears the B side interrupt by removing the low condition on the IRQb pin.

The enable bit in the IRQb status register (bit 6) is changed by writing the proper data to bit 6 of the IRQb status register. If the B side enable bit is zero, interrupts are prevented on the B side. However, a write to the IRQa control register still sets the B side flag bit.

INTERNAL REGISTER ADDRESSES

Table 8 shows the address of the RAM, $\overline{IRQ}$, and semaphore registers. The addresses to these registers are the same whether accessed from the A or B side. The address and data buses are multiplexed on the A side. The B side has separate address and data buses. The B side can be used on a multiplexed bus by connecting the corresponding address and data bit pins together (A0 to D0, A1 to D1, etc.) and using the B side address strobe input pin.

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TABLE 6 — IRQ REGISTERS

Location	Register Name	Bit 7	Bit 6	Bits 5 to 0
A Side F8	IRQa Status	Flag	Enable	Not Used
A Side F9	IRQa Control	Flag	Enable	Not Used
B Side F8	IRQb Status	Flag	Enable	Not Used
B Side F9	IRQb Control	Flag	Enable	Not Used

TABLE 7 — INTERRUPT OPERATION

Operation	Action Taken
A Reads IRQa Status at F8	Read EA and FA
A Writes IRQa Status at F8	Writes to EA
A Reads IRQa Control at F9	Read EA and FA; Clear FA
A Writes IRQa Control at F9	Set FB; Assert IRQB if Enabled
B Reads IRQb Status at F8	Read EB and FB
B Writes IRQb Status at F8	Writes to EB
B Reads IRb Control at F9	Read EB and FB; Clear FB
B Writes IRQb Control at F9	Set FA; Assert IRQA if Enabled

F8 and F9 are Address Locations
EA and FA are A Side Enable and Flag Bits
EB and FB are B Side Enable and Flag Bits

TABLE 8 — REGISTER LOCATIONS

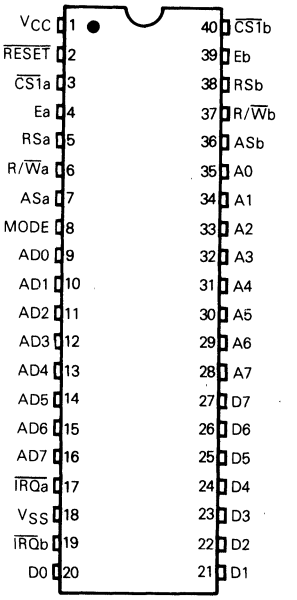
RS	Address	Register Name
0	00-FF	Dual Ported RAM
1	00-07	IRQ and Semaphore
1	08-0F	IRQ and Semaphore
1	10-17	IRQ and Semaphore
1	18-1F	IRQ and Semaphore
	•	
1	•	IRQ and Semaphore
	•	
1	E0-E7	IRQ and Semaphore
1	E8-EF	IRQ and Semaphore
1	F0-F7	IRQ and Semaphore
1	F8-FF	IRQ and Semaphore

Where:
X is 0 through F of the upper four bits of the address (note that only the lower three bits of the address are decoded):
X0 and X8 IRQa or IRQb Status
X1 and X9 IRQa or IRQb Control
X2 and XA Semaphore 1
X3 and XB Semaphore 2
X4 and XC Semaphore 3
X5 and XD Semaphore 4
X6 and XE Semaphore 5
X7 and XF Semaphore 6

ORDERING INFORMATION (T_A = 0° to 70°C)

Package Type	Order Number
Cerdip S Suffix	MCM68HC34S
Plastic P Suffix	MCM68HC34P
PLCC FN Suffix	MCM68HC34FN

PIN ASSIGNMENT



MCM4180

4K x 4 Bit Cache Address Tag Comparator

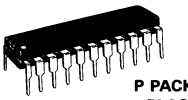
The MCM4180 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core with an on-board comparator for efficient implementation of a cache memory.

The device has a $\overline{CLR}$ pin for flash clear of the RAM, useful for system initialization.

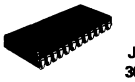
The MCM4180 compares RAM contents with current input data. The result is either an active high match level for a cache hit, or an active low level for a cache miss.

The MCM4180 is available in 22 lead plastic DIP and 24 lead SOJ packages.

- Single 5 V ±10% Power Supply
- Fast Address to Match Time: 22/25/30 ns max
- Fast Data to Match Time: 10/12/15 ns max
- Fast Read of Tag RAM Contents: 25/30/35 ns max
- Flash Clear of the Tag RAM ($\overline{CLR}$ Pin)
- Pin and Function Compatible with MK41H80

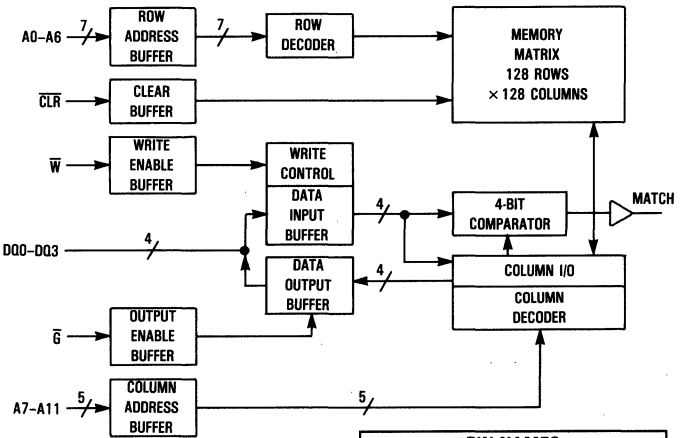


P PACKAGE
PLASTIC
CASE 736A



J PACKAGE
300 MIL SOJ
CASE 810A

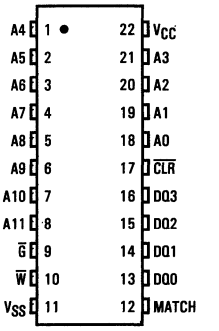
BLOCK DIAGRAM



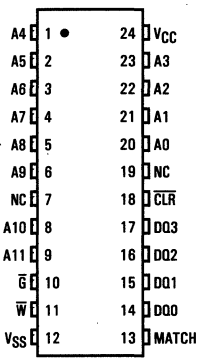
PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{CLR}$	Flash Clear Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



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TRUTH TABLE

$\overline{W}$	$\overline{G}$	$\overline{CLR}$	DQ0-DQ3	Match	Mode
H	H	H	Compare D_{in}	Valid	Compare
L	X	H	D_{in}	Assert	Write
H	L	H	D_{out}	Assert	Read
X	X	L	High-Z	Assert	Clear

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC} +0.5	V
Output Current Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current, Except Match Output ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current (I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	–	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, Match Output: I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
Match Output Capacitance	C_{match}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load (I/O Pins) . . . . . See Figure 1a
Output Load (Match Output) . . . . . See Figure 1c

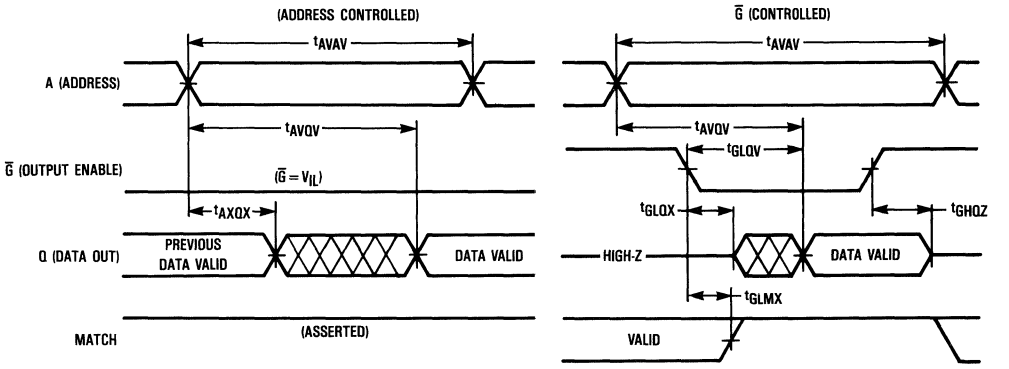
READ CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-22		MCM4180-25		MCM4180-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{OEA}	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
$\overline{G}$ Low to Output Active	t_{GLQX}	t_{OEL}	5	—	5	—	5	—	ns	2
$\overline{G}$ High to Output High-Z	t_{GHQZ}	t_{OEZ}	—	8	—	10	—	10	ns	2
$\overline{G}$ Low to Match Assert	t_{GLMX}	t_{CH}	0	10	0	12	0	15	ns	

NOTES:
1. $\overline{CLR} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

READ CYCLE



AC TEST LOADS

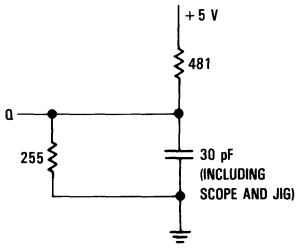


Figure 1a

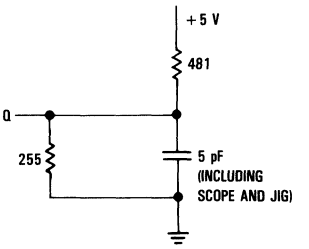


Figure 1b

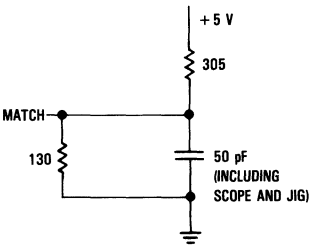


Figure 1c

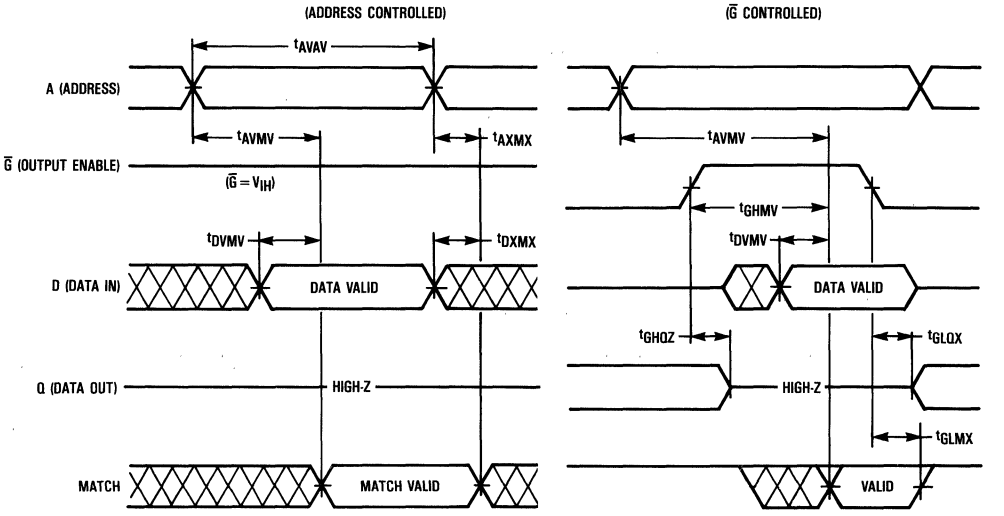
COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-22		MCM4180-25		MCM4180-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	25	–	30	–	35	–	ns	
Address Valid to Match Valid	t_{AVMV}	t_{ACA}	–	22	–	25	–	30	ns	
$\overline{G}$ High to Match Valid	t_{GHMV}	t_{GCA}	–	15	–	18	–	20	ns	
Data Valid to Match Valid	t_{DVMV}	t_{DCA}	–	10	–	12	–	15	ns	
Match Hold from $\overline{G}$ Low	t_{GLMX}	t_{CH}	0	10	0	12	0	15	ns	
Match Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	5	–	5	–	ns	
Match Hold from Data Invalid	t_{DXMX}	t_{DCH}	3	–	3	–	3	–	ns	
$\overline{G}$ Low to Output Active	t_{GLQX}	t_{LZ}	5	–	5	–	5	–	ns	2
$\overline{G}$ High to Output High-Z	t_{GHQZ}	t_{HZ}	–	8	–	10	–	10	ns	2

NOTES:
1. A compare cycle is performed when $\overline{CLR}$, $\overline{W}$, and $\overline{G}$ are all high.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

COMPARE CYCLE



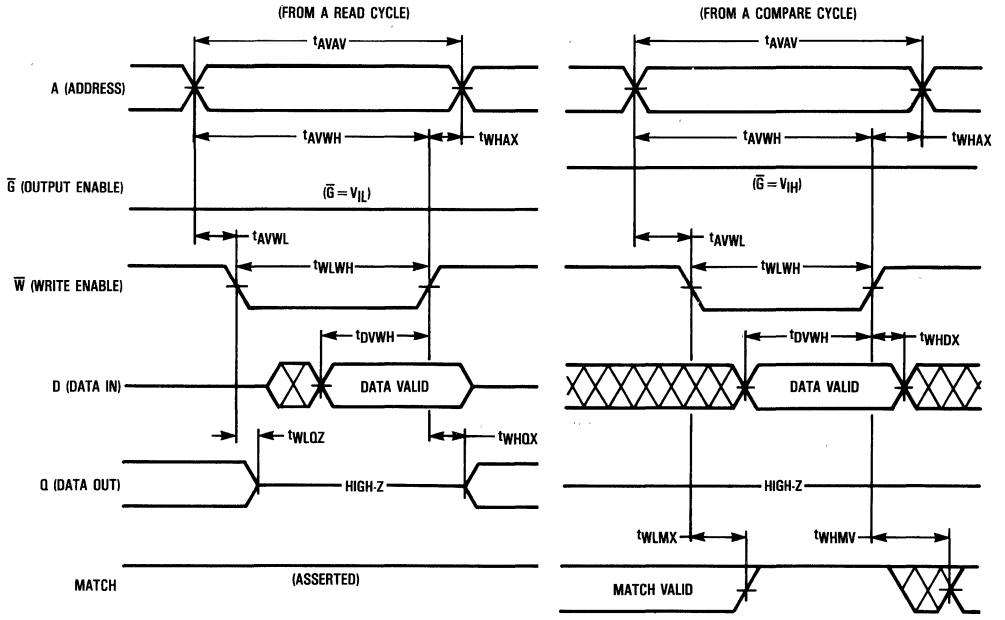
WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-22		MCM4180-25		MCM4180-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WEW}	18	—	20	—	25	—	ns	
Address Setup to Beginning of Write	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	18	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DS}	10	—	12	—	14	—	ns	
Data Hold from Write End	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{HZ}	0	9	0	10	0	12	ns	2
Address Hold from Write End	t_{WHAX}	t_{WAH}	0	—	0	—	0	—	ns	
Write Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	18	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	—	22	—	25	—	30	ns	
Write High to Output Active	t_{WHQX}	t_{LZ}	5	—	5	—	5	—	ns	2

NOTES:
1. A write occurs during the overlap of $\overline{W}$ low and $\overline{CLR}$ high.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

WRITE CYCLE



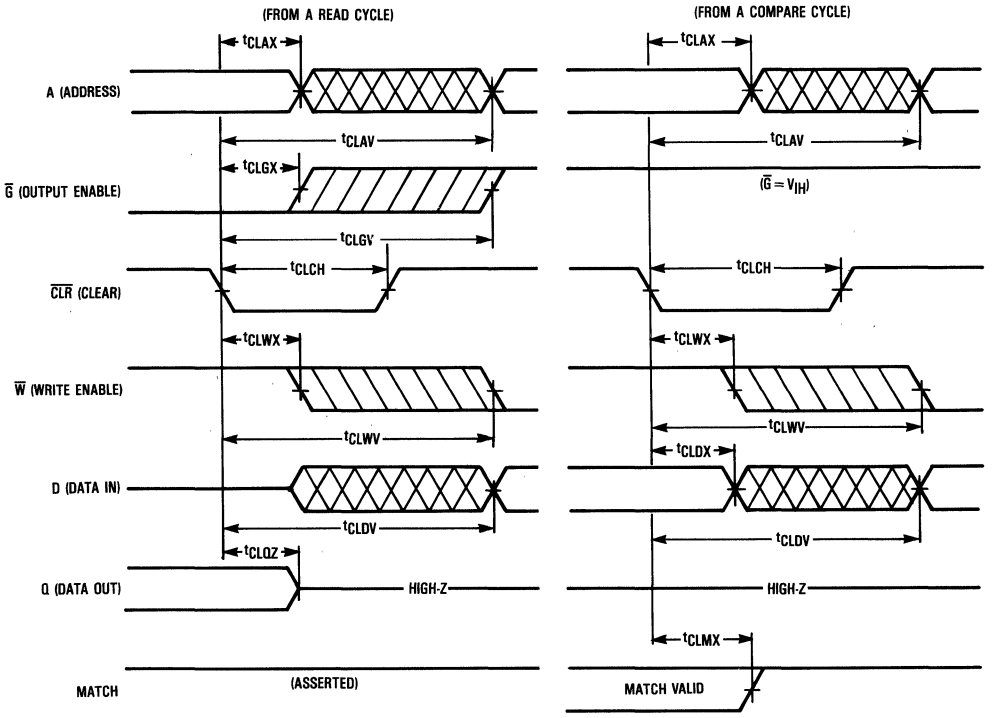
CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM4180-22		MCM4180-25		MCM4180-30		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{CLR}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{CLAV}	t_{CR}	—	70	—	70	—	70	ns	2
	$\overline{G}$	t_{CLGV}	t_{CR}								
	$\overline{W}$	t_{CLWV}	t_{CR}								
	D	t_{CLDV}	t_{CR}								
$\overline{CLR}$ Pulse Width		t_{CLCH}	t_{CLP}	25	—	30	-	35	—	ns	2
$\overline{CLR}$ Low to Inputs Don't Care	A	t_{CLAX}	t_{CX}	0	—	0	—	0	—	ns	
	$\overline{G}$	t_{CLGX}	t_{CX}								
	D	t_{CLDX}	t_{CX}								
	$\overline{W}$	t_{CLWX}	t_{CX}								
$\overline{CLR}$ Low to Match Assert		t_{CLMX}	t_{MH}	0	15	0	18	0	20	ns	
$\overline{CLR}$ Low to Output High-Z		t_{CLQZ}	t_{CZ}	—	15	—	18	—	20	ns	3

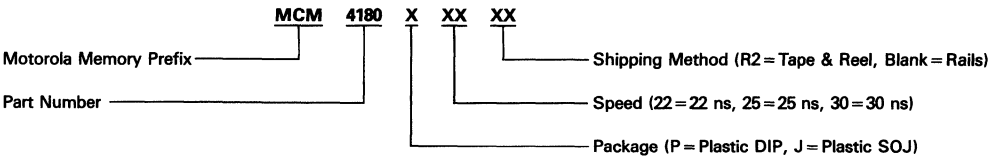
NOTES:
1. The address, data, $\overline{W}$, and $\overline{G}$ inputs are a don't care during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{CLR}$.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

CLEAR CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—

MCM4180P22	MCM4180P25	MCM4180P30
MCM4180J22	MCM4180J25	MCM4180J30
MCM4180J22R2	MCM4180J25R2	MCM4180J30R2

5

MCM4180-20

Product Preview

4K x 4 Bit Cache Address Tag Comparator

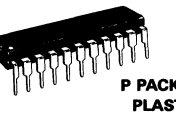
The MCM4180 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core with an on-board comparator for efficient implementation of a cache memory.

The device has a $\overline{CLR}$ pin for flash clear of the RAM, useful for system initialization.

The MCM4180 compares RAM contents with current input data. The result is either an active high match level for a cache hit, or an active low level for a cache miss.

The MCM4180 is available in 22 lead plastic DIP and 24 lead SOJ packages.

- Single 5 V ±10% Power Supply
- Fast Address to Match Time: 20 ns max
- Fast Data to Match Time: 10 ns max
- Fast Read of Tag RAM Contents: 20 ns max
- Flash Clear of the Tag RAM ($\overline{CLR}$ Pin)
- Pin and Function Compatible with MK41H80

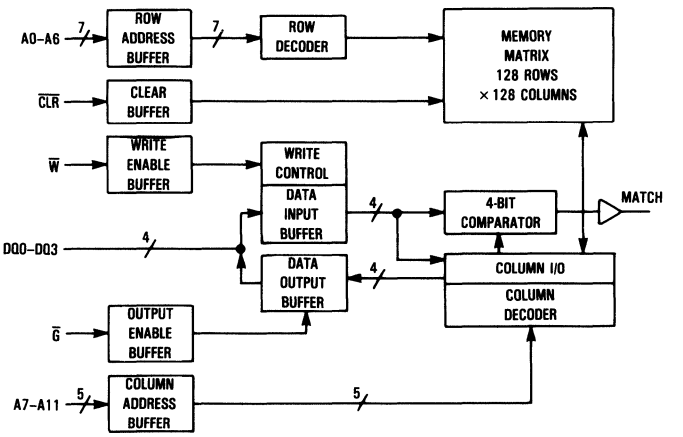


P PACKAGE
PLASTIC
CASE 736A

J PACKAGE
300 MIL SOJ
CASE 810A

5

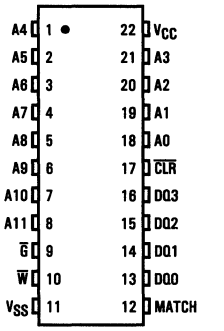
BLOCK DIAGRAM



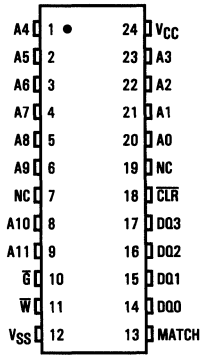
PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{CLR}$	Flash Clear Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

DUAL-IN-LINE



SMALL OUTLINE



TRUTH TABLE

$\overline{W}$	$\overline{G}$	$\overline{CLR}$	DQ0-DQ3	Match	Mode
H	H	H	Compare D_{in}	Valid	Compare
L	X	H	D_{in}	Assert	Write
H	L	H	D_{out}	Assert	Read
X	X	L	High-Z	Assert	Clear

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current — Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current, Except Match Output ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	—	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 12.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, Match Output: I_{OH} = −10.0 mA)	V_{OH}	2.4	—	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
Match Output Capacitance	C_{match}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

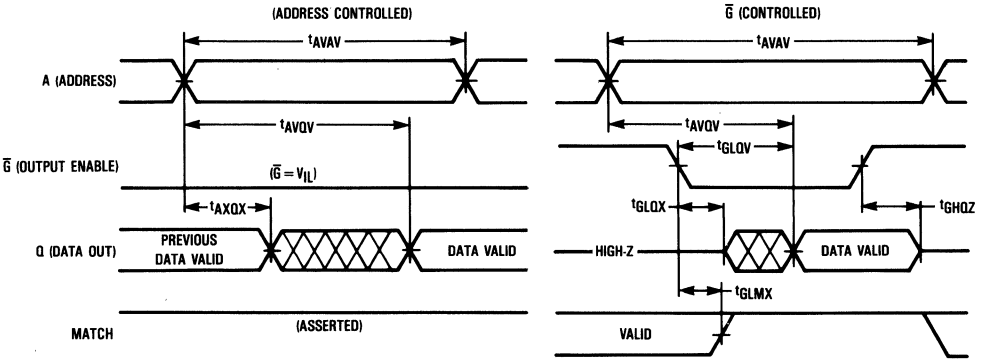
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load (I/O Pins) . . . . . See Figure 1a
Output Load (Match Output) . . . . . See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-20		Unit	Notes
	Standard	Alternate	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	20	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{OEA}	—	9	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	ns	
$\overline{G}$ Low to Output Active	t_{GLQX}	t_{OEL}	3	—	ns	2
$\overline{G}$ High to Output High-Z	t_{GHQZ}	t_{OEZ}	—	8	ns	2
$\overline{G}$ Low to Match Assert	t_{GLMX}	t_{CH}	0	15	ns	

NOTES:
1. $\overline{CLR} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

READ CYCLE



AC TEST LOADS

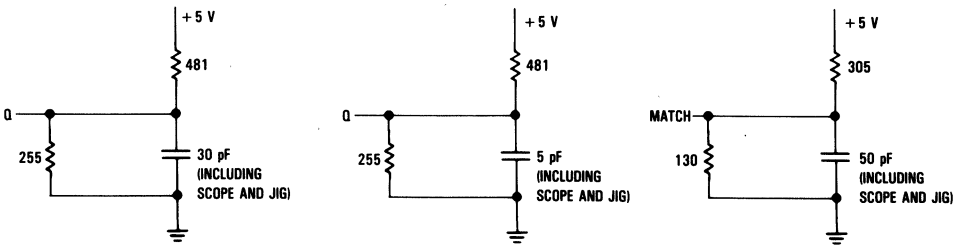


Figure 1a Figure 1b Figure 1c

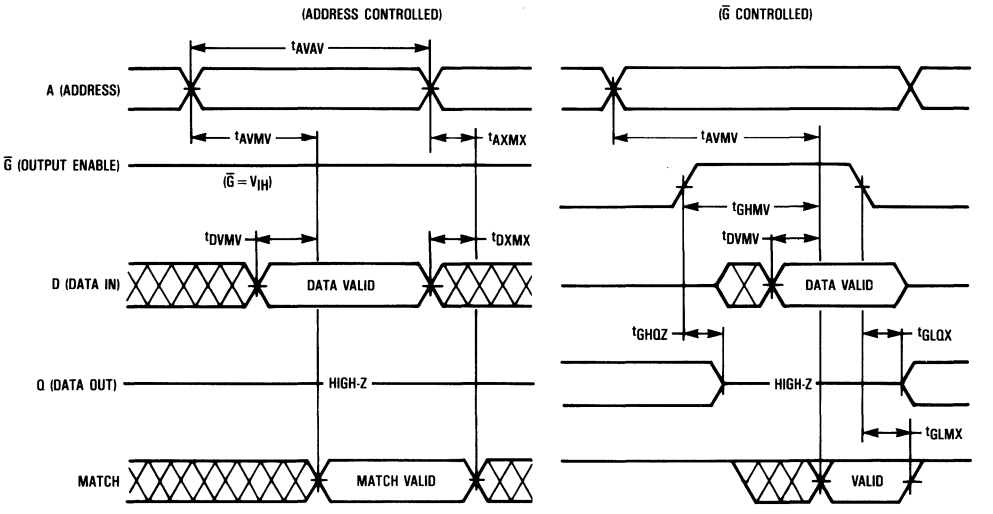
COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-20		Unit	Notes
	Standard	Alternate	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	20	—	ns	
Address Valid to Match Valid	t_{AVMV}	t_{ACA}	—	20	ns	
$\overline{G}$ High to Match Valid	t_{GHMV}	t_{GCA}	—	15	ns	
Data Valid to Match Valid	t_{DVMV}	t_{DCA}	—	10	ns	
Match Hold from $\overline{G}$ Low	t_{GLMX}	t_{CH}	0	15	ns	
Match Hold from Address Change	t_{AXMX}	t_{ACH}	5	—	ns	
Match Hold from Data Invalid	t_{DXMX}	t_{DCH}	3	—	ns	
$\overline{G}$ Low to Output Active	t_{GLQX}	t_{LZ}	3	—	ns	2
$\overline{G}$ High to Output High-Z	t_{GHQZ}	t_{HZ}	—	8	ns	2

NOTES:
1. A compare cycle is performed when $\overline{CLR}$, $\overline{W}$, and $\overline{G}$ are all high.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

COMPARE CYCLE



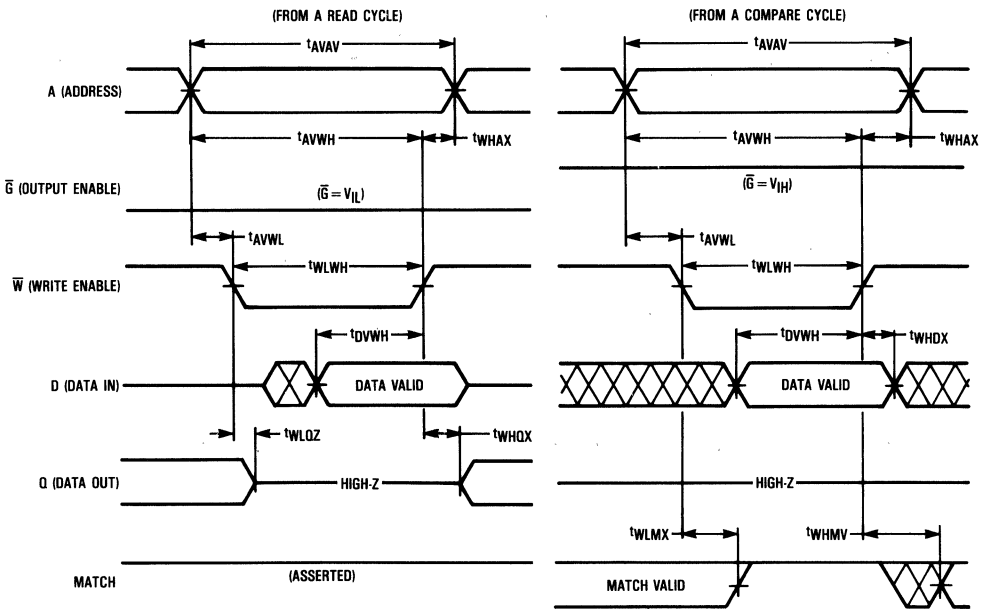
WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM4180-20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	
Write Pulse Width	t_{WLWH}	t_{WEW}	14	–	ns	
Address Setup to Beginning of Write	t_{AVWL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	16	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DS}	10	–	ns	
Data Hold from Write End	t_{WHDX}	t_{DH}	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{HZ}	0	8	ns	2
Address Hold from Write End	t_{WHAX}	t_{WAH}	0	–	ns	
Write Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	20	ns	
Write High to Output Active	t_{WHQX}	t_{LZ}	3	–	ns	2

NOTES:
1. A write occurs during the overlap of $\overline{W}$ low and $\overline{CLR}$ high.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

WRITE CYCLE



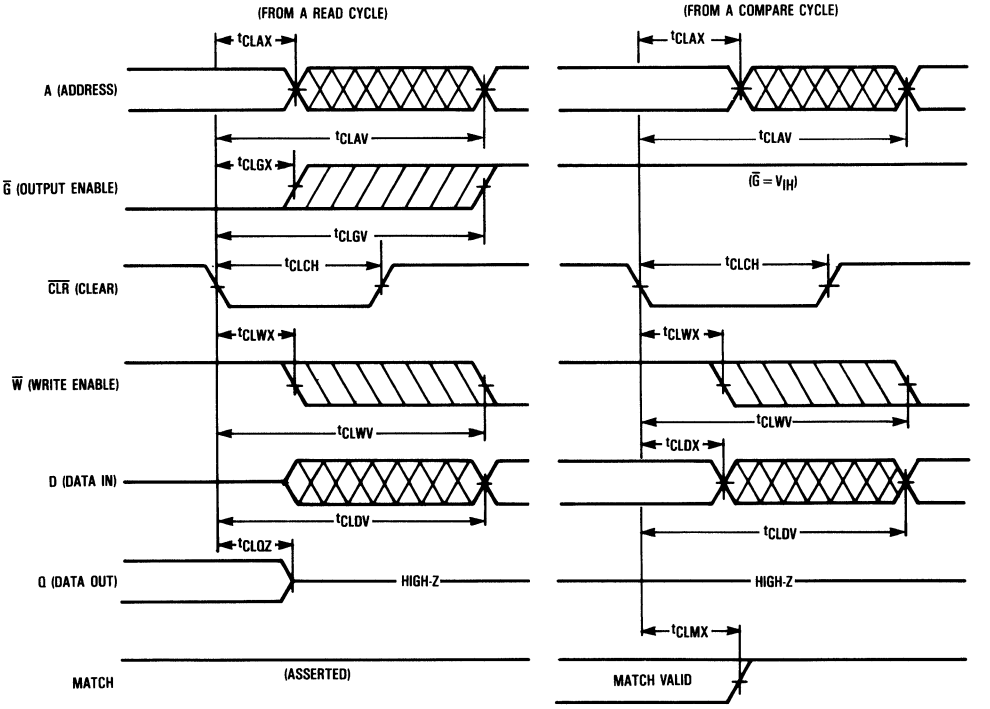
CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM4180-20		Unit	Notes
		Standard	Alternate	Min	Max		
$\overline{CLR}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{CLAV}	t_{CR}	–	70	ns	2
	$\overline{G}$	t_{CLGV}	t_{CR}				
	$\overline{W}$	t_{CLWV}	t_{CR}				
	D	t_{CLDV}	t_{CR}				
$\overline{CLR}$ Pulse Width		t_{CLCH}	t_{CLP}	20	–	ns	2
$\overline{CLR}$ Low to Inputs Don't Care	A	t_{CLAX}	t_{CX}	0	–	ns	
	$\overline{G}$	t_{CLGX}	t_{CX}				
	D	t_{CLDX}	t_{CX}				
	$\overline{W}$	t_{CLWX}	t_{CX}				
$\overline{CLR}$ Low to Match Assert		t_{CLMX}	t_{MH}	0	15	ns	
$\overline{CLR}$ Low to Output High-Z		t_{CLQZ}	t_{CZ}	–	15	ns	3

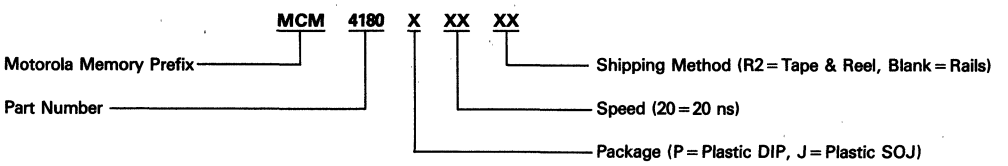
NOTES:
1. The address, data, $\overline{W}$, and $\overline{G}$ inputs are a don't care during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{CLR}$.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

CLEAR CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers— MCM4180P20
MCM4180J20
MCM4180J20R2

5

MCM6292

16K x 4 Bit Synchronous Static RAM
with Transparent Outputs

The MCM6292 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A13), data (D0–D3), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

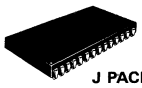
The MCM6292 provides transparent output operation when K is low for access of RAM data within the same cycle (output data is latched when K is high).

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6292 is available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

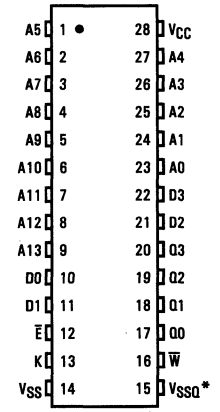
- Single 5 V ±10% Power Supply
- Fast Access and Cycle Times: 25/30/35 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

P PACKAGE
300 MIL PLASTIC
CASE 710A



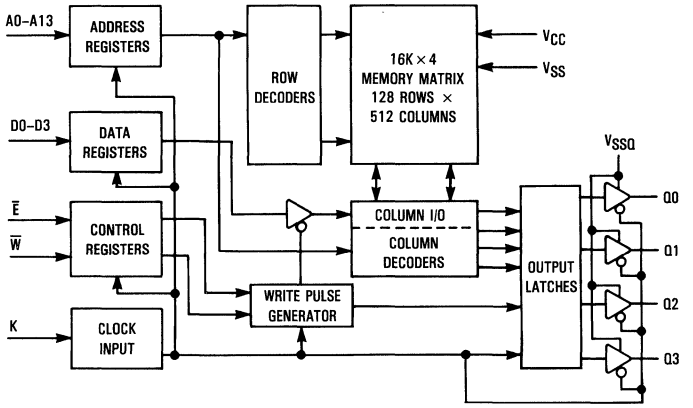
J PACKAGE
PLASTIC
CASE 810

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES	
A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

5

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q3
L	L	Write	High Z
L	H	Read	D_{out}
H	X	Not Selected	High Z

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, V_{out}=0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, I_{out}=0 mA, All Inputs=V_{IL} or V_{IH}, Cycle Time≥t_{KHKH} min)	I_{CCA}	–	140	mA
Standby Current ($\overline{E}=V_{IH}$, V_{IH}≥3.0 V, V_{IL}≤0.4 V, I_{out}=0 mA, Cycle Time≥t_{KHKH} min)	I_{SB1}	–	55	mA
Output Low Voltage (I_{OL}=12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH}=−10.0 mA)	V_{OH}	2.4	–	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter		Symbol	MCM6292-25		MCM6292-30		MCM6292-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{KHKH}	25	—	30	—	35	—	ns	2
Clock Access Time		t_{KHQV}	—	25	—	30	—	35	ns	4, 6
Data Valid from Clock Low		t_{KLQV}	—	10	—	13	—	15	ns	5, 6
Output Hold from Clock Low		t_{KLQX}	0	—	0	—	0	—	ns	3, 6
Clock Low to Q High Z ($\overline{E}=V_{IH}$)		t_{KLQZ}	—	10	—	13	—	15	ns	3, 6
Clock Low Pulse Width		t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width		t_{KHKL}	5	—	5	—	5	—	ns	
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	5	—	5	—	ns	7
	A	t_{AVKH}								
	$\overline{W}$	t_{WHKH}								
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	3	—	3	—	ns	7
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
4. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
5. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.
6. K must be at a low level for outputs to transition.
7. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

AC TEST LOADS

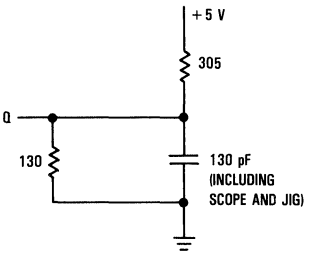


Figure 1A

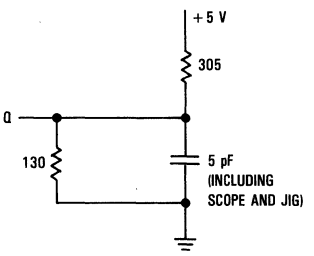
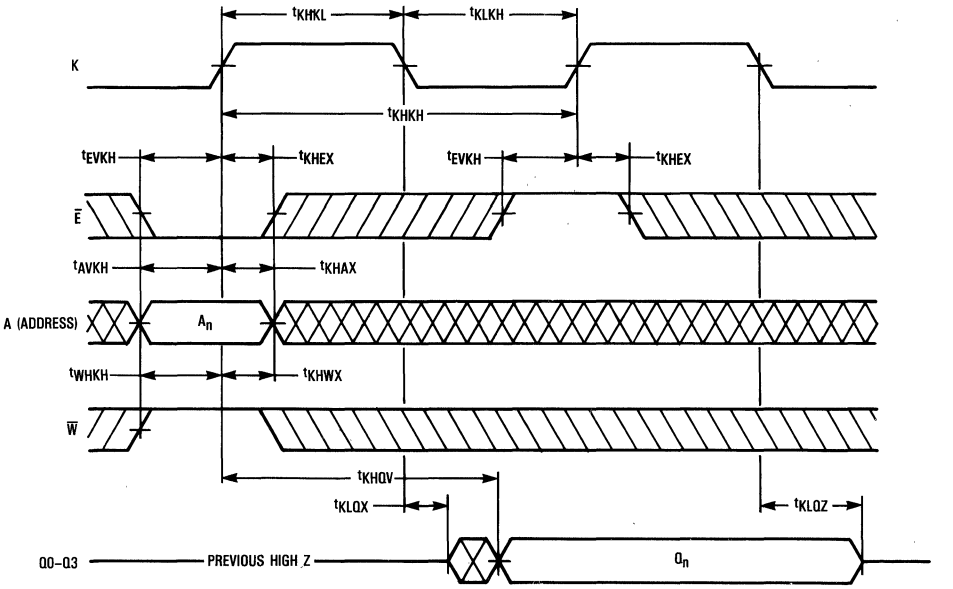
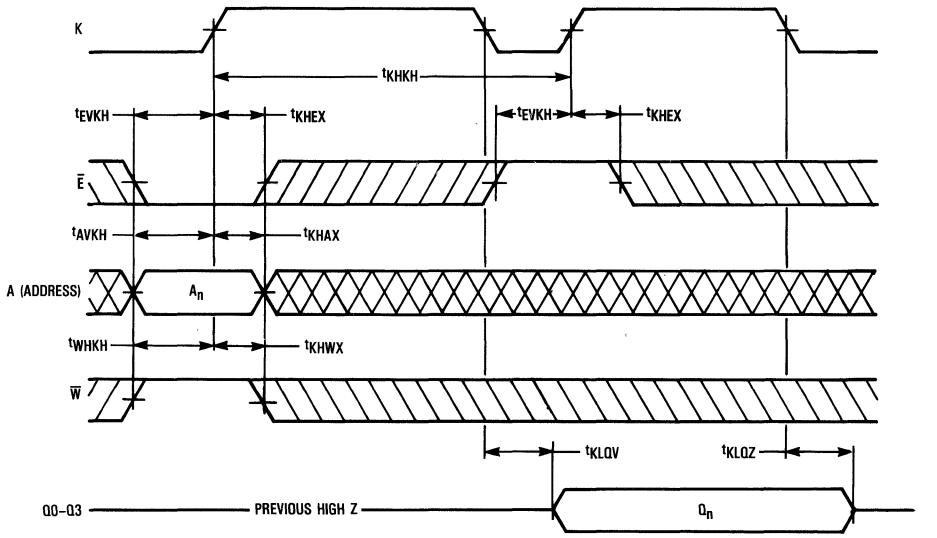


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)



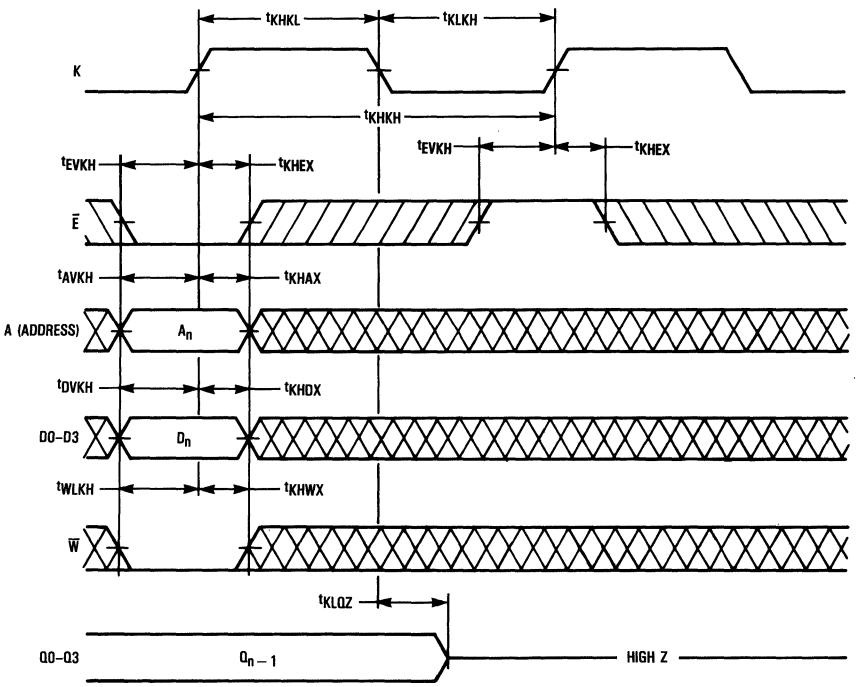
NOTES:
1. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6292-25		MCM6292-30		MCM6292-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	—	30	—	35	—	ns	2
Clock Low to Output High Z		t_{KLQZ}	—	10	—	13	—	15	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	5	—	5	—	ns	4
	A	t_{AVKH}								
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	3	—	3	—	ns	4
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. K must be at a low level for outputs to transition.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

5



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Latches on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output latches, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6292 offers transparent output operation, which allows output data access within the same t_{KHKH} cycle. This feature lends itself well to applications requiring RAM data to be set up on the system bus prior to the next rising clock edge. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next falling clock edge. When the clock (K) signal is low, the output is allowed to transition relative to the most recent rising clock (K) edge.

Figure 2 shows a typical system configuration using four MCM6292 chips. The system addresses are tied to the MCM6292s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6292. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

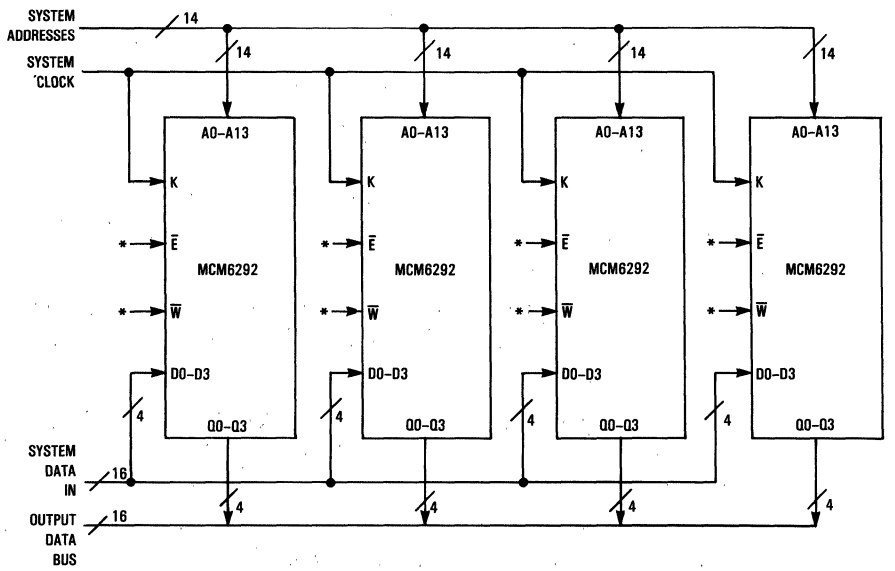
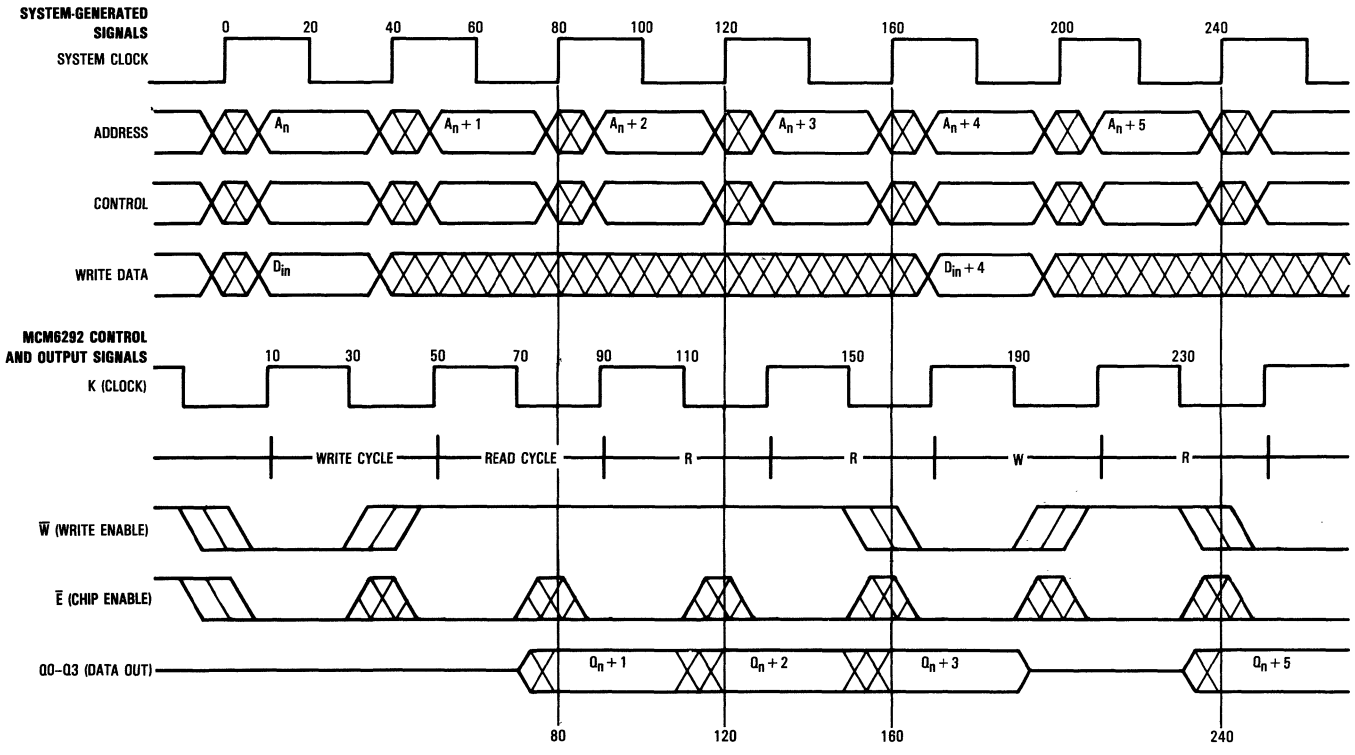


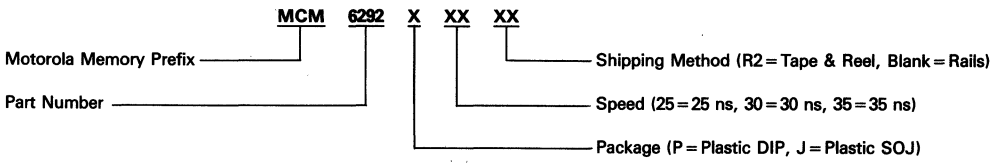
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Nonpipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)

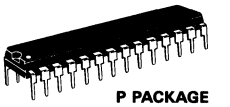


Full Part Numbers—	MCM6292P25	MCM6292J25	MCM6292J25R2
	MCM6292P30	MCM6292J30	MCM6292J30R2
	MCM6292P35	MCM6292J35	MCM6292J35R2

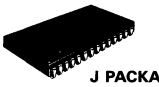
5

MCM6293

16K x 4 Bit Synchronous Static RAM
with Output Registers



P PACKAGE
300 MIL PLASTIC
CASE 710A



J PACKAGE
PLASTIC
CASE 810

The MCM6293 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

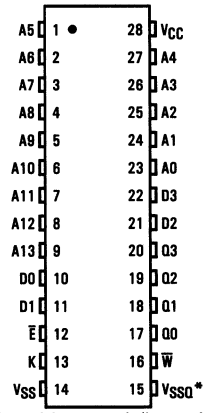
The MCM6293 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6293 is available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

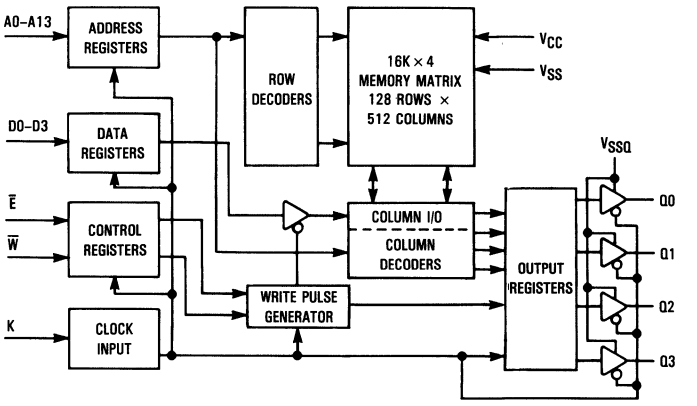
- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

5

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q3
L	L	Write	High Z
L	H	Read	D_{out}
H	X	Not Selected	High Z

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E} = V_{IL}$, I_{out} = 0 mA, All Inputs = V_{IH} or V_{IL}, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	140	mA
Standby Current ($\overline{E} = V_{IH}$, $V_{IH} \geq 3.0$ V, $V_{IL} \leq 0.4$ V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	55	mA
Output Low Voltage (I_{OL} = 12.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −10.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6293-20		MCM6293-25		MCM6293-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	ns	4
Clock High to Q High Z ($\overline{E}$=V_{IH})	t_{KHQZ}	–	10	–	10	–	13	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	–	5	–	5	–	ns	5
A	t_{AVKH}								
$\overline{W}$	t_{WHKH}								
Hold Times for: $\overline{E}$	t_{KHEX}	3	–	3	–	3	–	ns	5
A	t_{KHAX}								
$\overline{W}$	t_{KHWX}								

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

5

AC TEST LOADS

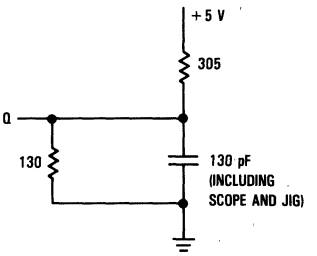


Figure 1A

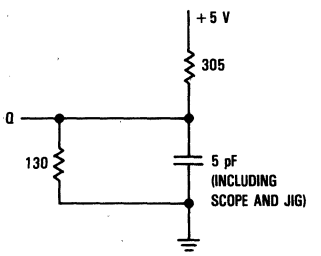
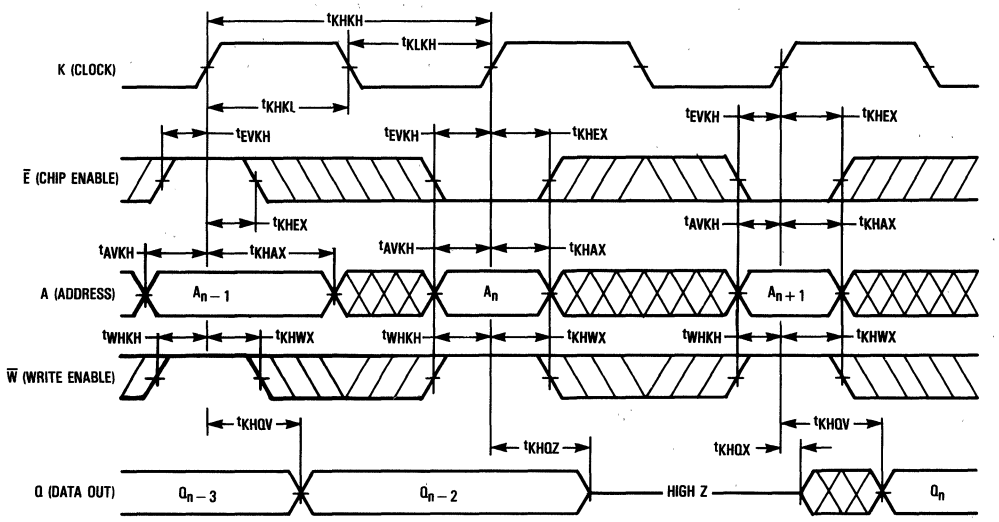
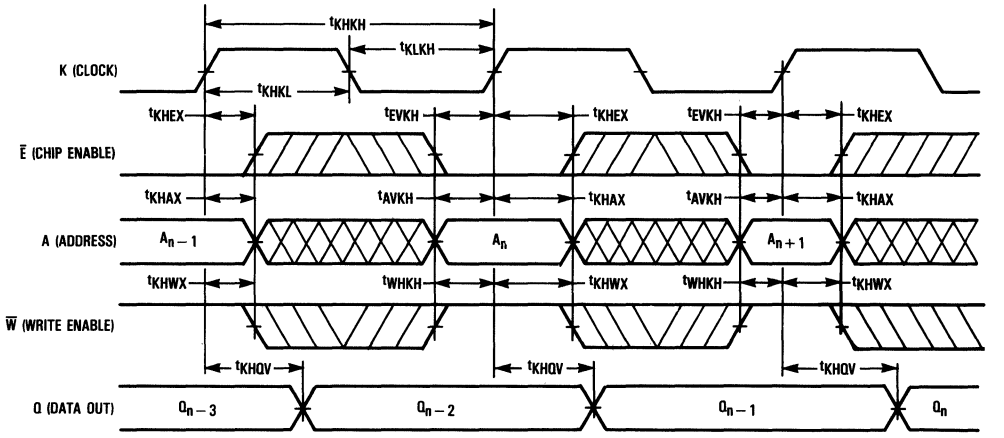


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

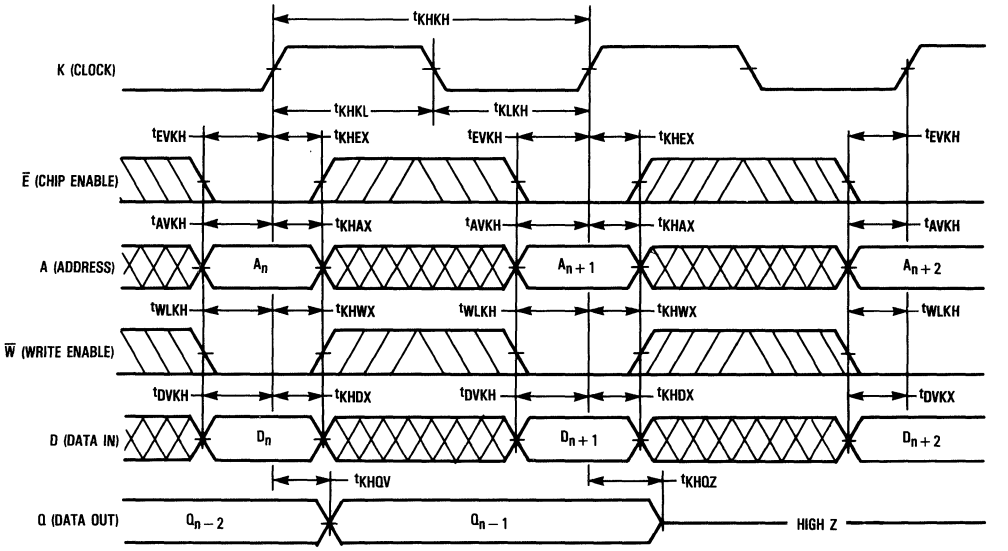
WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6293-20		MCM6293-25		MCM6293-30		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	—	25	—	30	—	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	—	10	—	10	—	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	5	—	5	—	ns	4
	A	t_{AVKH}								
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	3	—	3	—	ns	4
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

5

WRITE CYCLE



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6293 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

Figure 2 shows a typical system configuration using four MCM6293 chips. The system addresses are tied to the MCM6293s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6293. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

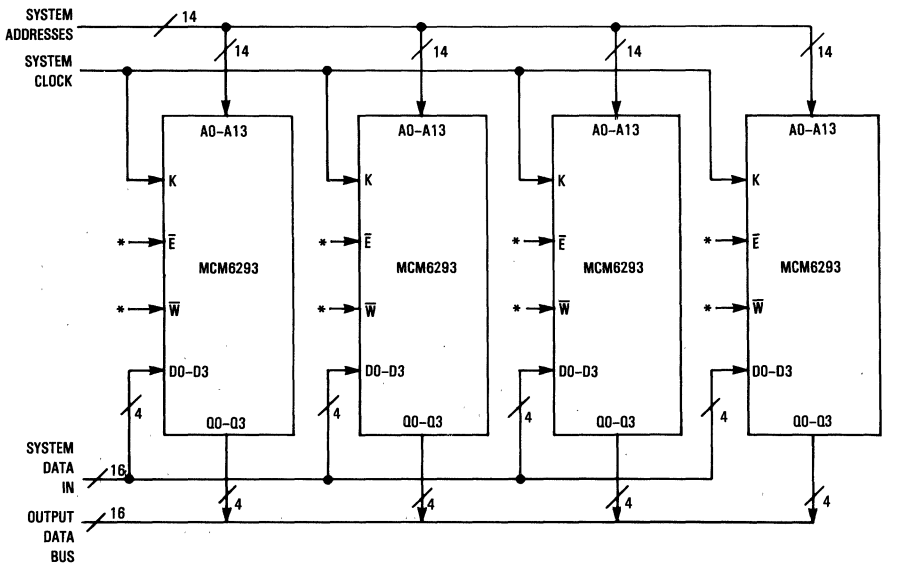
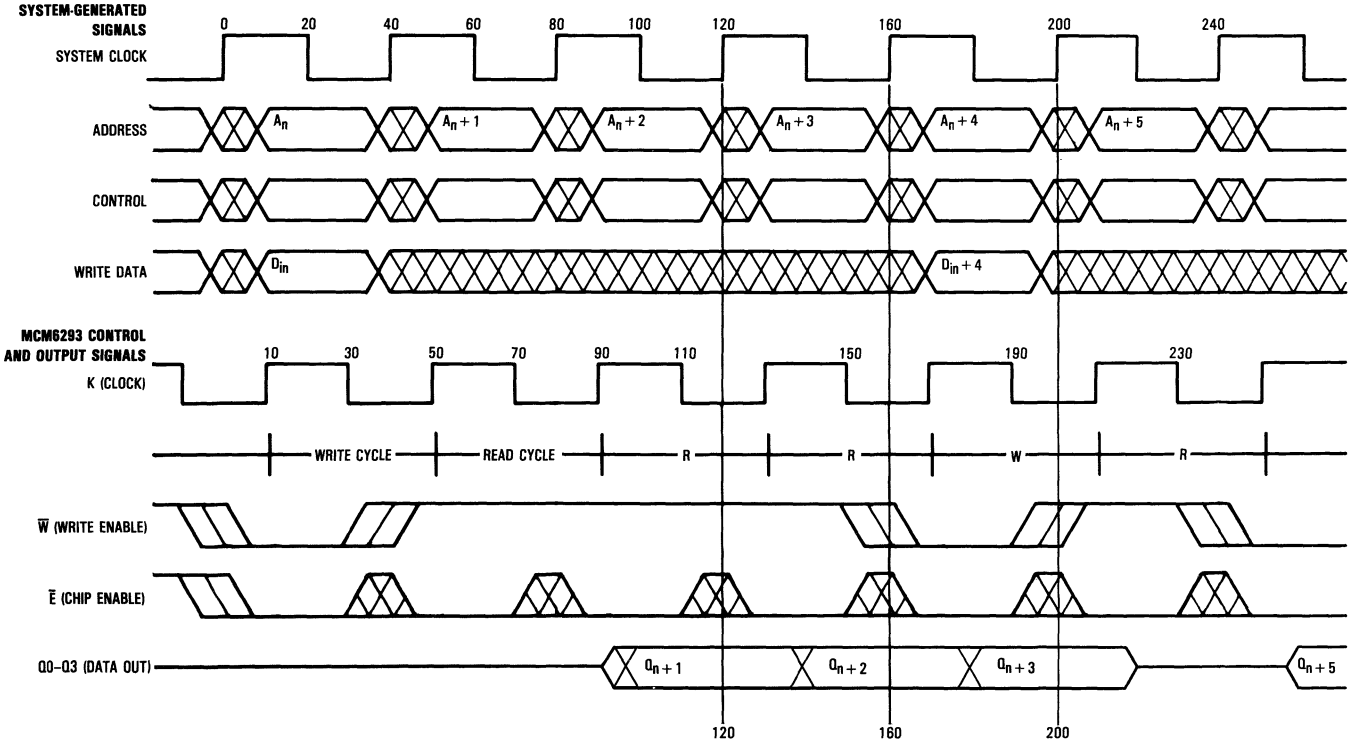


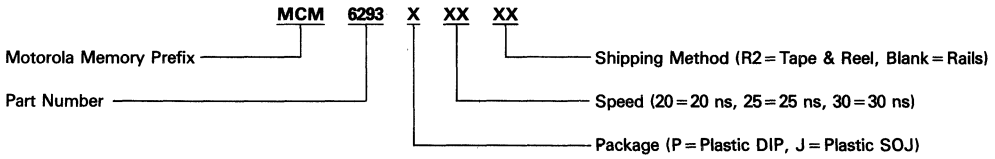
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Pipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6293P20	MCM6293J20	MCM6293J20R2
	MCM6293P25	MCM6293J25	MCM6293J25R2
	MCM6293P30	MCM6293J30	MCM6293J30R2

5

MCM6294

16K x 4 Bit Synchronous Static RAM
with Output Registers and Output Enable

The MCM6294 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MCM6294 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

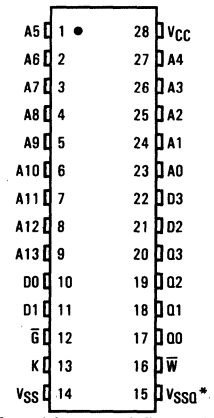
The MCM6294 is available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

P PACKAGE
300 MIL PLASTIC
CASE 710A

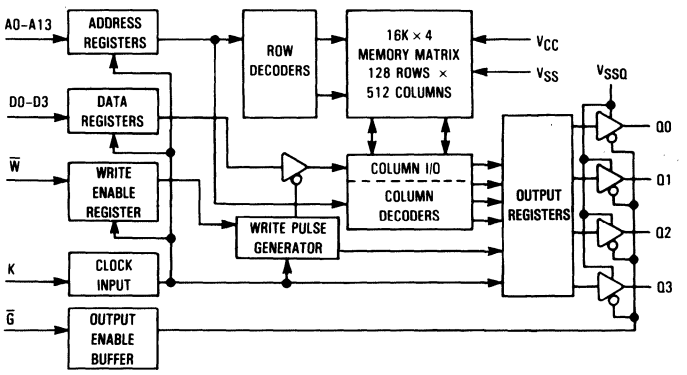
J PACKAGE
PLASTIC
CASE 810

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q3
L	Write	High Z
H	Read	D_{out}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G}=V_{IL}$, $I_{out}=0$ mA, Cycle Time = t_{KHKH} min)	I_{CCA}	–	140	mA
Output Low Voltage ($I_{OL}=12.0$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-10.0$ mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6294-20		MCM6294-25		MCM6294-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	—	25	—	30	—	ns	2
Clock Access Time	t_{KHQV}	—	10	—	10	—	13	ns	3
Output Active from Clock High	t_{KHQX}	0	—	0	—	0	—	ns	4
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	5	—	ns	
Setup Times for: A	t_{AVKH}	5	—	5	—	5	—	ns	5
Setup Times for: $\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	—	3	—	3	—	ns	5
Hold Times for: $\overline{W}$	t_{KHWX}								
$\overline{G}$ High to Q High Z	t_{GHQZ}	—	10	—	10	—	13	ns	4, 6
$\overline{G}$ Low to Q Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 6
$\overline{G}$ Low to Q Valid	t_{GLQV}	—	10	—	10	—	13	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device.

AC TEST LOADS

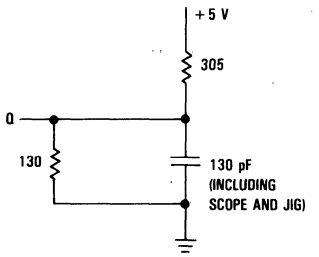


Figure 1A

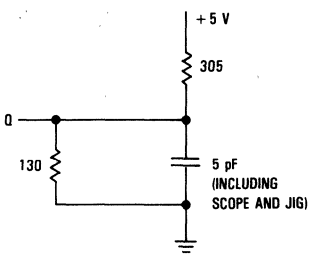
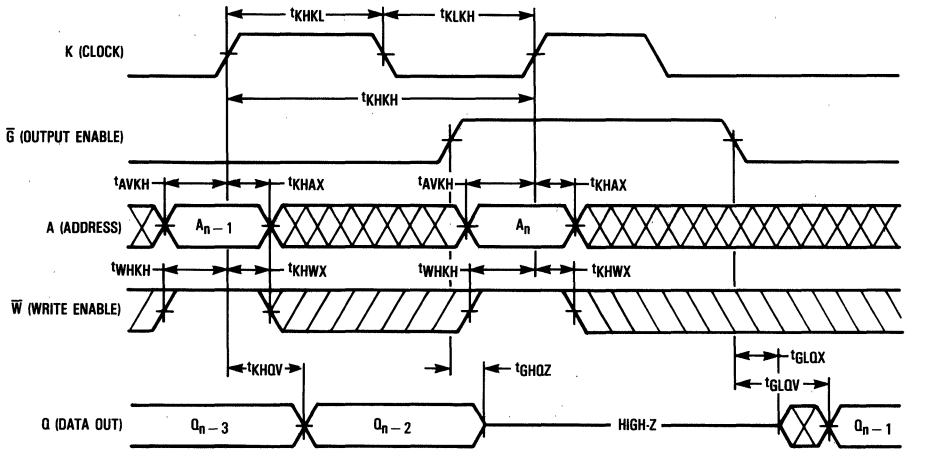
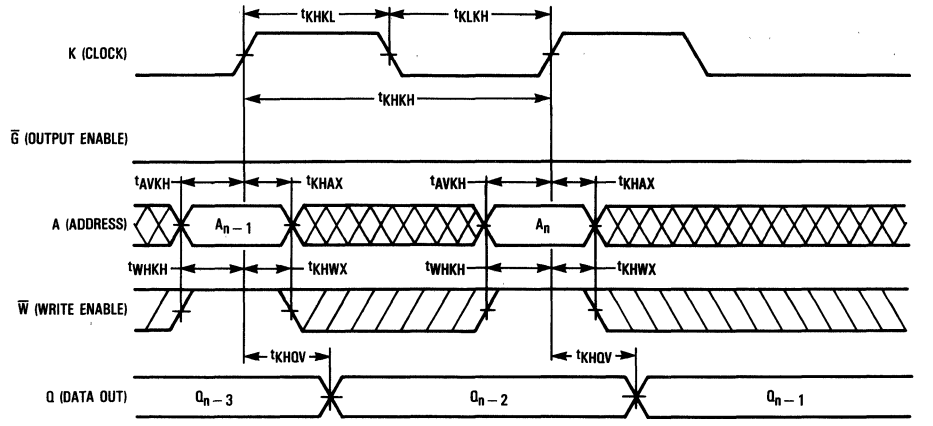


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles, where $\overline{W} = V_{IH}$ for those cycles.

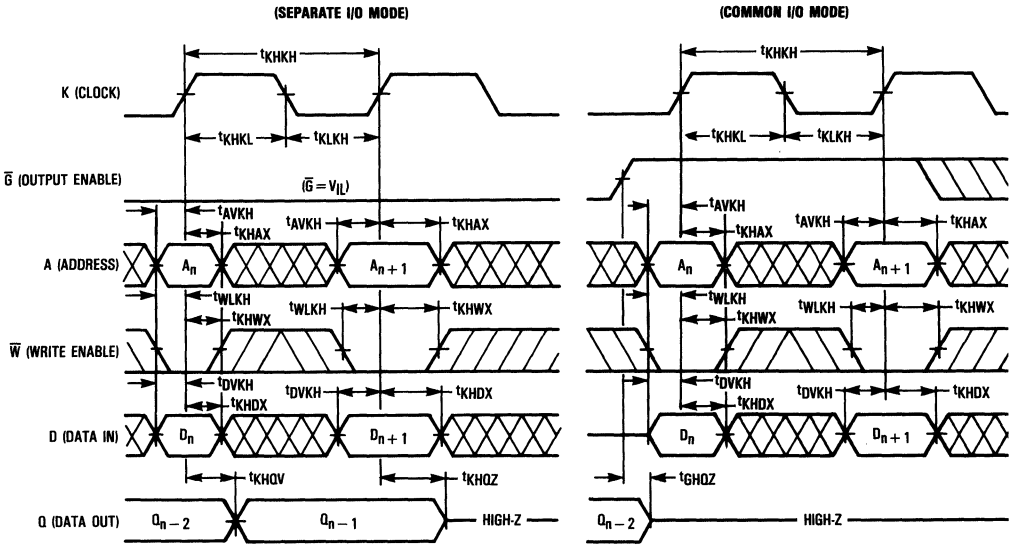
WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6294-20		MCM6294-25		MCM6294-30		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	–	25	–	30	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	–	13	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	10	–	13	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	5	–	ns	5
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	A	t_{KHAX}	3	–	3	–	3	–	ns	5
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

5

WRITE CYCLE



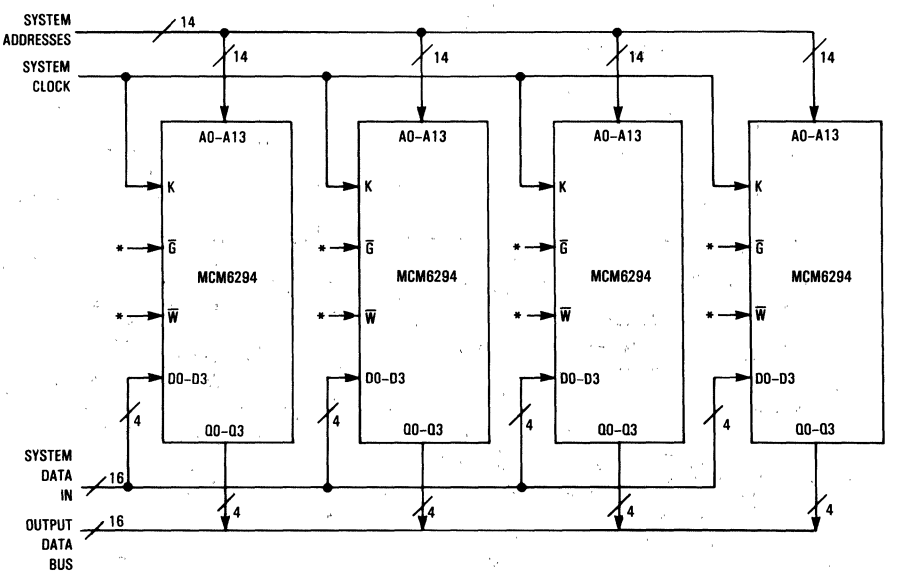
APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6294 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

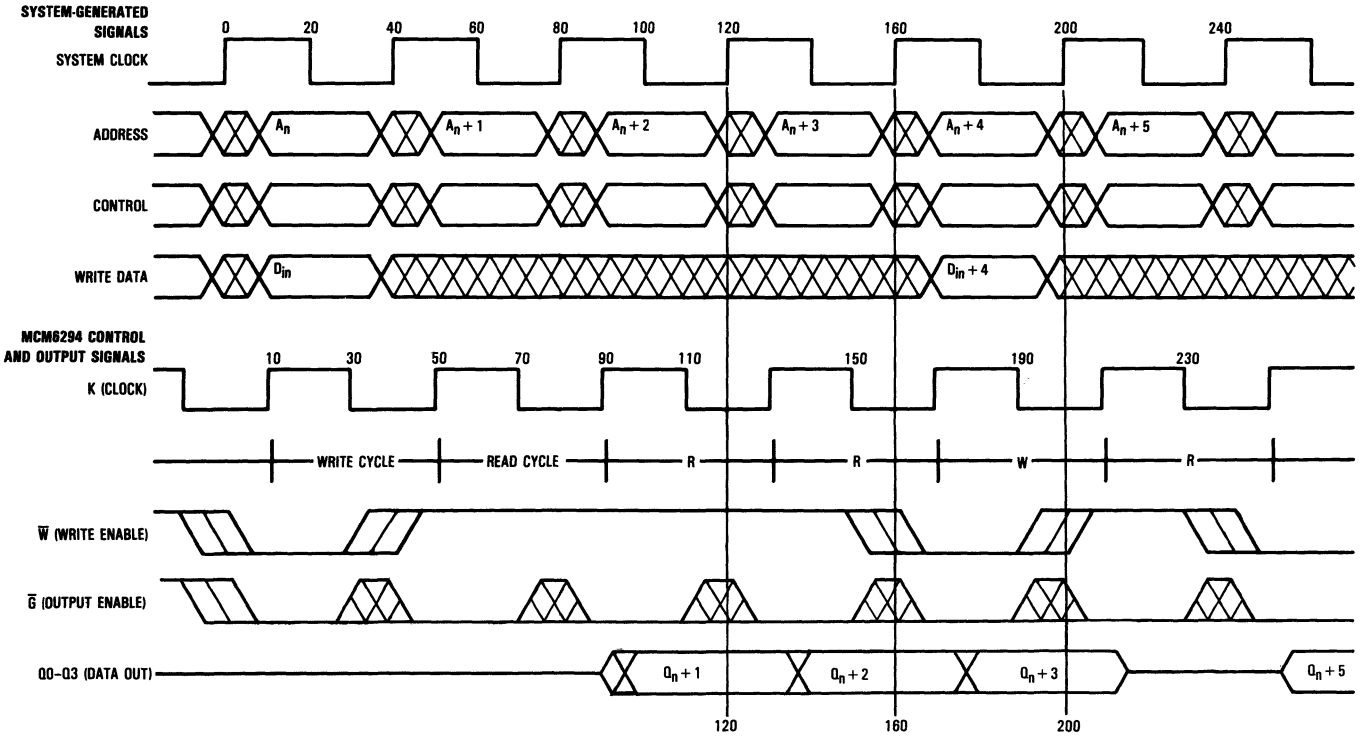
Figure 2 shows a typical system configuration using four MCM6294 chips. The system addresses are tied to the MCM6294s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6294. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.



*From read/write controller.

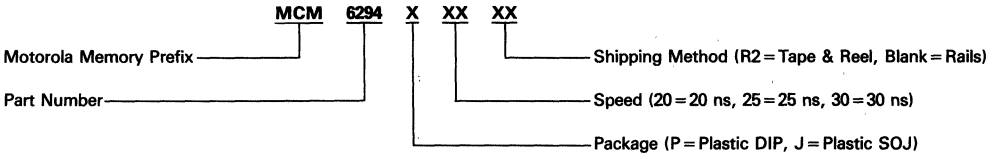
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Pipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6294P20	MCM6294J20	MCM6294J20R2
	MCM6294P25	MCM6294J25	MCM6294J25R2
	MCM6294P30	MCM6294J30	MCM6294J30R2

5

MCM6295

16K x 4 Bit Synchronous Static RAM
with Transparent Outputs and Output Enable

The MCM6295 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

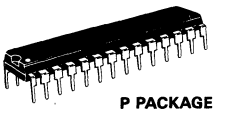
The MCM6295 provides transparent output operation when K is low for access of RAM data within the same cycle (output data is latched when K is high).

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6295 is available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

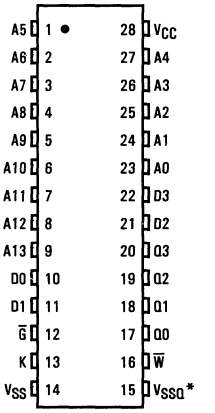
- Single 5 V ±10% Power Supply
- Fast Access and Cycle Times: 25/30/35 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag



P PACKAGE
300 MIL PLASTIC
CASE 710A

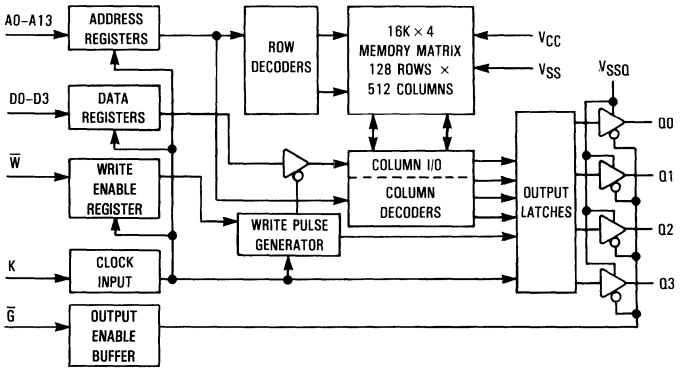
J PACKAGE
PLASTIC
CASE 810

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES	
A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q3
L	Write	High Z
H	Read	D_{out}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{S}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be in high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{G}=V_{IL}$, $I_{out}=0$ mA)	I_{CCA}	—	140	mA
Output Low Voltage ($I_{OL}=12.0$ mA)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH}=-10.0$ mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6295-25		MCM6295-30		MCM6295-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	–	30	–	35	–	ns	2
Clock Access Time	t_{KHQV}	–	25	–	30	–	35	ns	4, 6
Data Valid from Clock Low	t_{KLQV}	–	10	–	13	–	15	ns	5, 6
Output Hold from Clock Low	t_{KLQX}	0	–	0	–	0	–	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	7
Setup Times for: $\overline{W}$	t_{WHKH}	5	–	5	–	5	–	ns	7
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	7
Hold Times for: $\overline{W}$	t_{KHWX}	3	–	3	–	3	–	ns	7
$\overline{G}$ High to Q High Z	t_{GHQZ}	–	10	–	13	–	15	ns	8
$\overline{G}$ Low to Q Active	t_{GLQX}	0	–	0	–	0	–	ns	8
$\overline{G}$ Low to Q Valid	t_{GLQV}	–	10	–	13	–	15	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
4. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
5. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.
6. K must be at a low level for outputs to transition.
7. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
8. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.

AC TEST LOADS

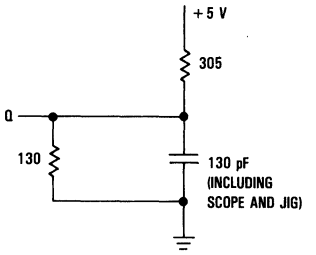


Figure 1A

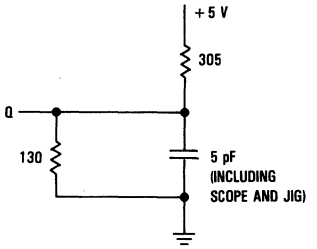
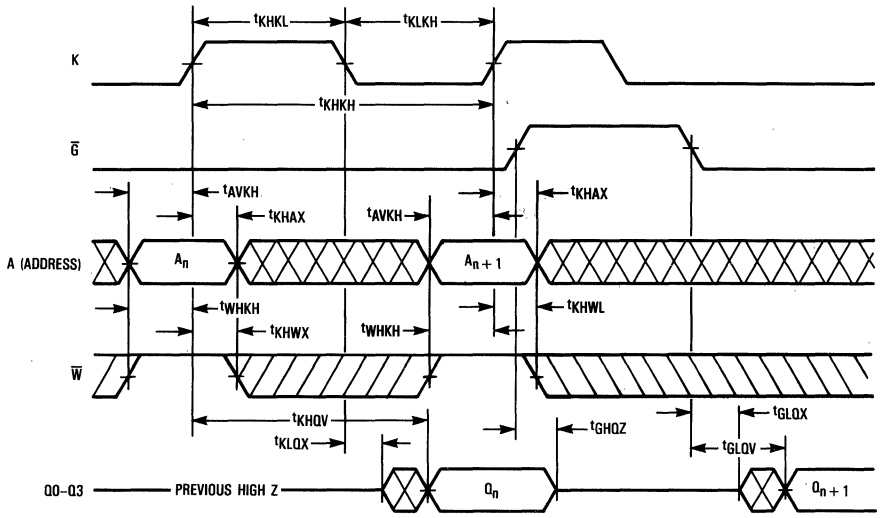
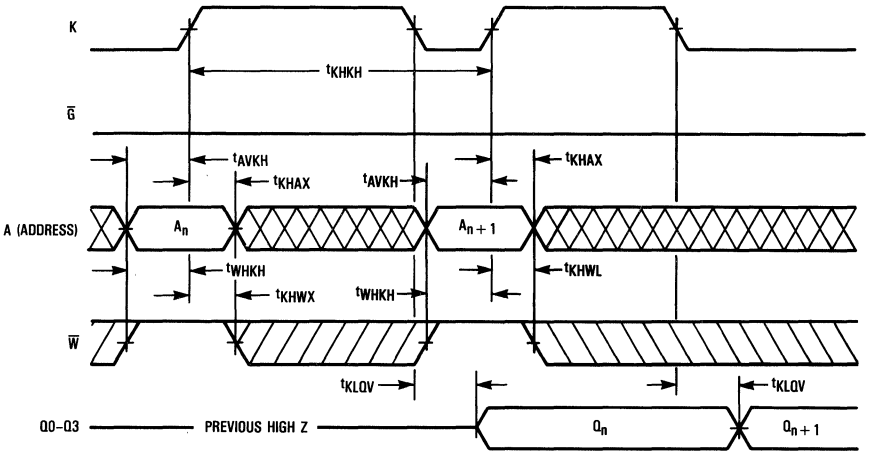


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)

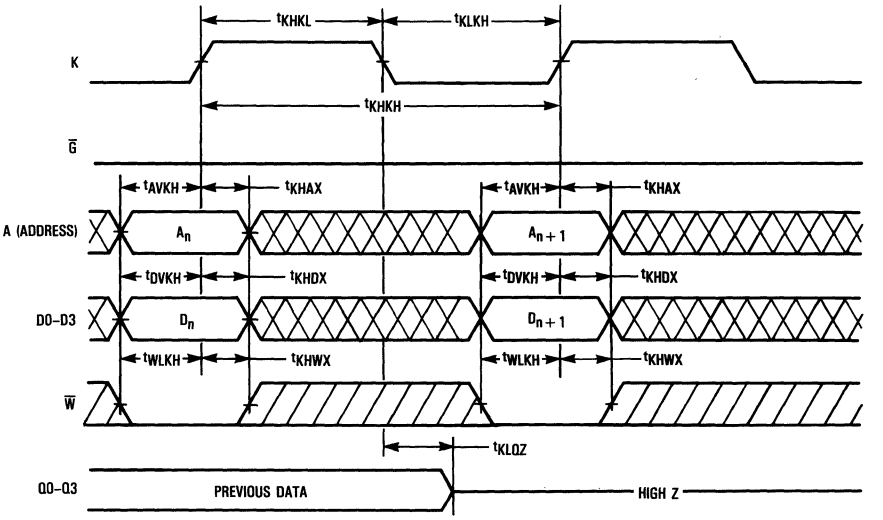


NOTES:
1. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6295-25		MCM6295-30		MCM6295-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	–	30	–	35	–	ns	2
Clock Low to Output High Z ($\overline{W}=V_{IL}$)		t_{KLQZ}	–	10	–	13	–	15	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	13	–	15	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	5	–	ns	5
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	A	t_{KHAX}	3	–	3	–	3	–	ns	5
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. K must be at a low level for outputs to transition.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Latches on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output latches, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6295 offers transparent output operation, which allows output data access within the same t_{KHKH} cycle. This feature lends itself well to applications requiring RAM data to be set up on the system bus prior to the next rising clock edge. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next falling clock edge. When the clock (K) signal is low, the output is allowed to transition relative to the most recent rising clock (K) edge.

Figure 2 shows a typical system configuration using four MCM6295 chips. The system addresses are tied to the MCM6295s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6295. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

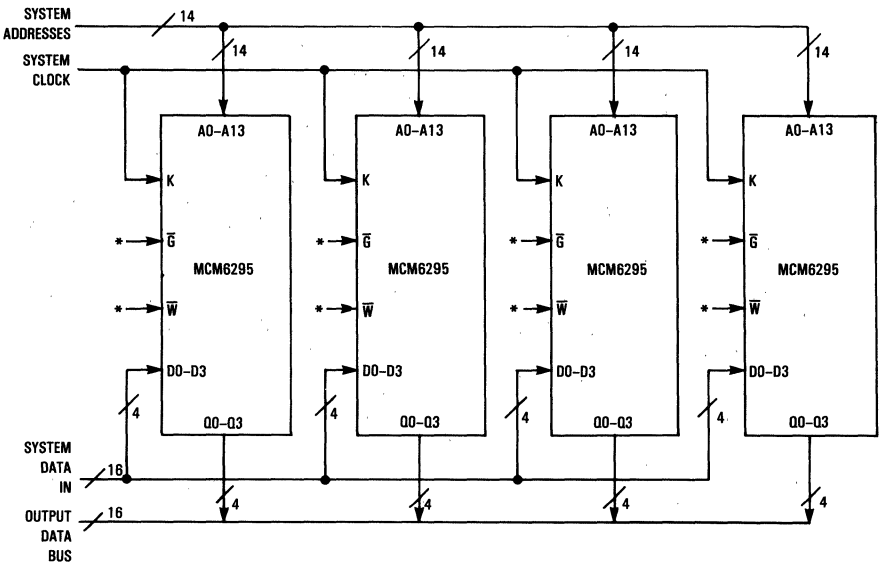
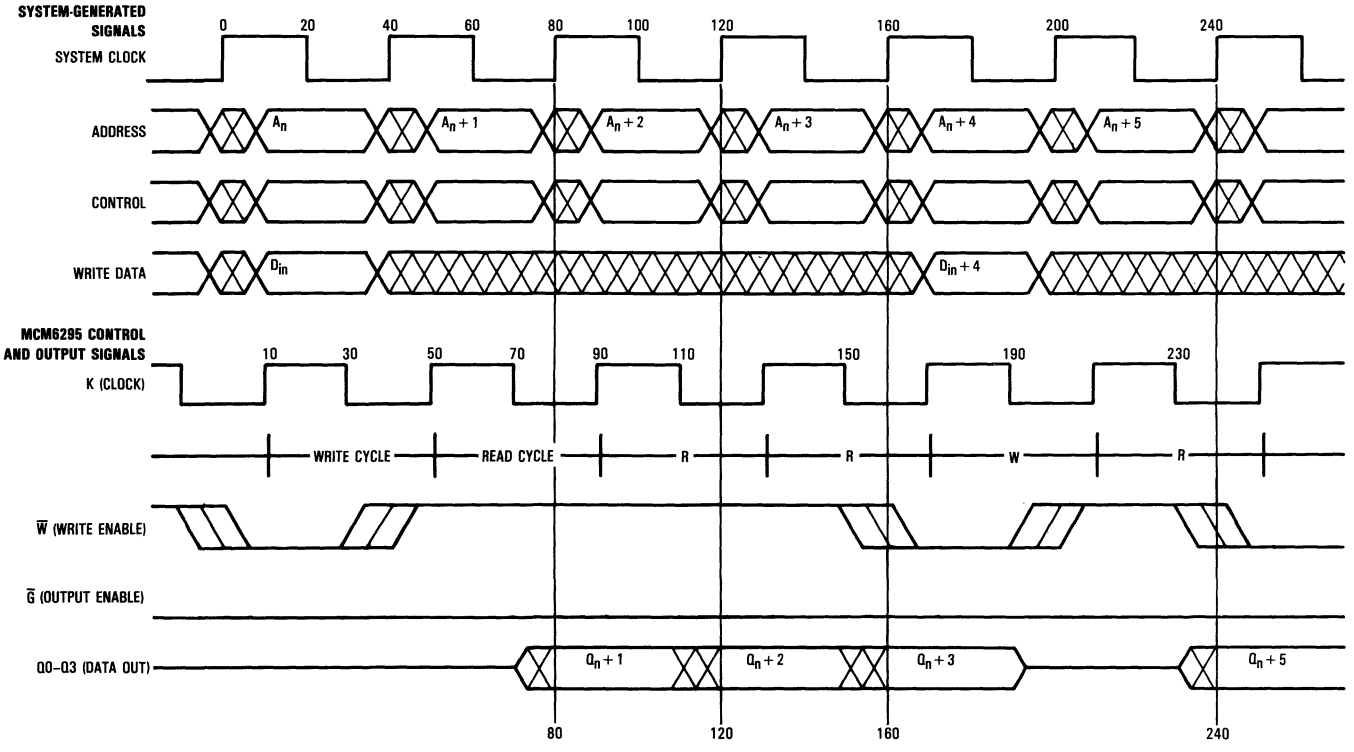


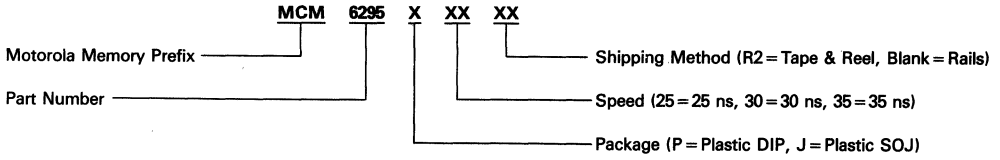
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Nonpipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6295P25	MCM6295J25	MCM6295J25R2
	MCM6295P30	MCM6295J30	MCM6295J30R2
	MCM6295P35	MCM6295J35	MCM6295J35R2

5

MCM62350

4K × 4 Bit Cache Address Tag Comparator

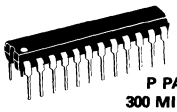
with System Status Bit Functions

The MCM62350 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K × 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required. The MCM62350 is available in 24 lead plastic DIP and SOJ packages.

The device has a reset ($\overline{R}$) pin for flash clear of the RAM within two minimum cycles. This function is useful for system initialization. Individual bits within a tag field can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

The MCM62350 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status bit applications). In addition, the match output can be programmed as true high or true low for potential logic delay savings. The configuration of these modes is accomplished by performing a write cycle with the $\overline{R}$ pin held low.

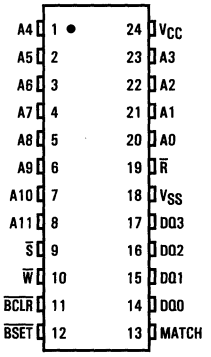
- Single 5 V ±10% Power Supply
- Fast Address to Match Time; 22/25/30 ns max
- Fast Data to Match Time; 10/12/15 ns max
- Fast Read of Tag RAM Contents; 25/30/35 ns max
- Flash Clear of the Tag RAM; 70/70/70 ns max
- Programmable Active Output Level of Match
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes: XNOR Mode for Address Tag Comparison
  AOI Mode for System Valid Bit Comparison



P PACKAGE
300 MIL PLASTIC
CASE 724

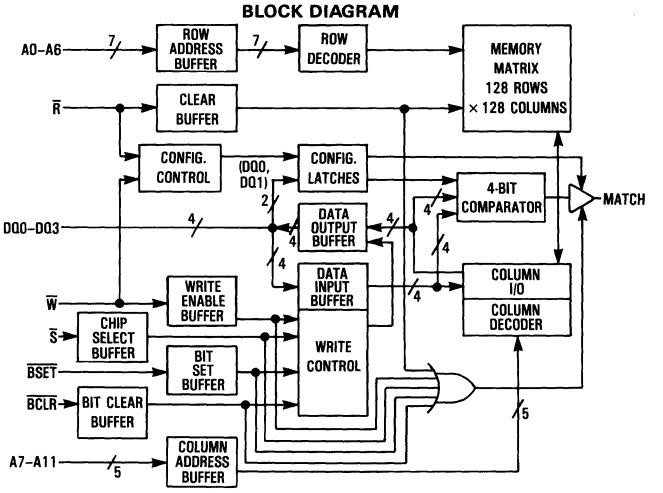
J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

A0-A11—ADDRESS INPUTS

The address lines are used for indexing into the tag RAM portion of the chip.

DQ0-DQ3—DATA INPUT/OUTPUT

The data lines are used as input for compare, write, and configuration cycles, and as output for read cycles.

$\overline{BSET}$—BIT SET CONTROL INPUT

This control signal is used for ORing data into the tag RAM during $\overline{BSET}$ write cycles. Independent bits within the tag can be set using the appropriate mask, as indicated in the bit set truth table. The $\overline{BSET}$ input can also be used to initiate a read cycle.

$\overline{BCLR}$—BIT CLEAR CONTROL INPUT

This control signal is used for ANDing the complement of data into the tag RAM during $\overline{BCLR}$ write cycles. Independent bits within the tag can be cleared using the appropriate mask, as indicated in the bit clear truth table. The $\overline{BCLR}$ input can also be used to initiate a read cycle (note that at least one of the $\overline{BSET}$/$\overline{BCLR}$ signals must be asserted to trigger a read cycle).

$\overline{R}$—RESET (FLASH CLEAR) INPUT

The reset control signal is used to initiate a clear cycle or a configuration cycle.

$\overline{S}$—CHIP SELECT

This control signal is used to chip select the device.

$\overline{W}$—WRITE ENABLE

The write enable signal is used to initiate write cycles.

MATCH—MATCH (HIT) OUTPUT

This output signal is used to indicate a match of DQ0-DQ3 inputs with the contents of the tag RAM addressed by A0—A11.

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FUNCTIONAL TRUTH TABLE

$\overline{S}$	$\overline{W}$	$\overline{BCLR}$	$\overline{BSET}$	$\overline{R}$	DQ0-DQ3	Match	Cycle
L	H	H	H	H	Compare D_{in}	Valid	Compare
L	H	L	X	H	Read D_{out}	Assert	Read
L	H	X	L	H	Read D_{out}	Assert	Read
L	L	H	H	H	Write D_{in}	Assert	Write
L	L	L	H	H	Bit Clear Mask	Assert	$\overline{BCLR}$ Write
L	L	H	L	H	Bit Set Mask	Assert	$\overline{BSET}$ Write
X	H	X	X	L	High-Z	Assert	Clear (Reset)
L	L	X	X	L	Config D_{in}*	Assert	Configuration
H	X	X	X	H	High-Z	Assert	Deselect

*DQ2 and DQ3 are don't cares during a configuration cycle.

COMPARATOR BEHAVIORAL TABLE

Type	DQ0	DQ1	DQ2	DQ3	RAMQ0	RAMQ1	RAMQ2	RAMQ3	Match
XNOR	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
XNOR	$\overline{Q0}$	Q1	Q2	Q3	Q0	Q1	Q2	Q3	0
AOI	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
AOI	L	Q1	Q2	Q3	X	Q1	Q2	Q3	1
AOI	H	Q1	Q2	Q3	L	Q1	Q2	Q3	0

L = Low
H = High
0 = False
1 = True
X = Don't Care

BIT CLEAR TRUTH TABLE (See Note)

Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	0	Bit Cleared
1	1	0	to "Zero"

BIT SET TRUTH TABLE (See Note)

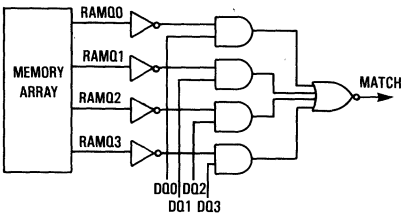
Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	1	Bit Set
1	1	1	to "One"

NOTE: These tables reflect the behavior of single bit positions. The four bits in the tag can all be set or cleared in tandem, or bits within the tag can be independently set or cleared with the appropriate mask.

CONFIGURATION TABLE

DQ0	DQ1	Comparator Type	Match True Level
L	L	XNOR	Low
L	H	XNOR	High
H	L	AOI	Low
H	H	AOI	High

AOI COMPARATOR LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

The power supply (V_{CC}) should be stable for at least 100 μs before operating the device. During this interval, the part will internally configure itself for XNOR compares, with the match output active high. In addition, the memory array of RAM bits will be cleared.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current, Except Match Output ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{S}$ = V_{IL}, I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	–	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, Match Output: I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
Match Output Capacitance	C_{match}	6	7	pF

AC TEST LOADS

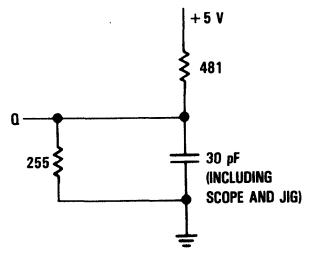


Figure 1a

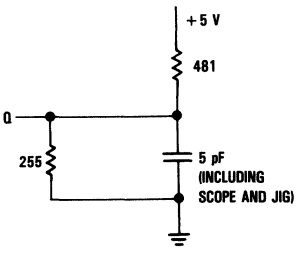


Figure 1b

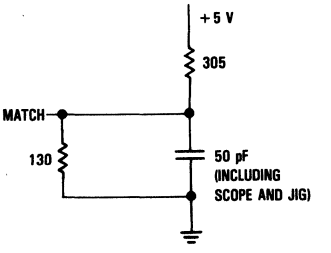


Figure 1c

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

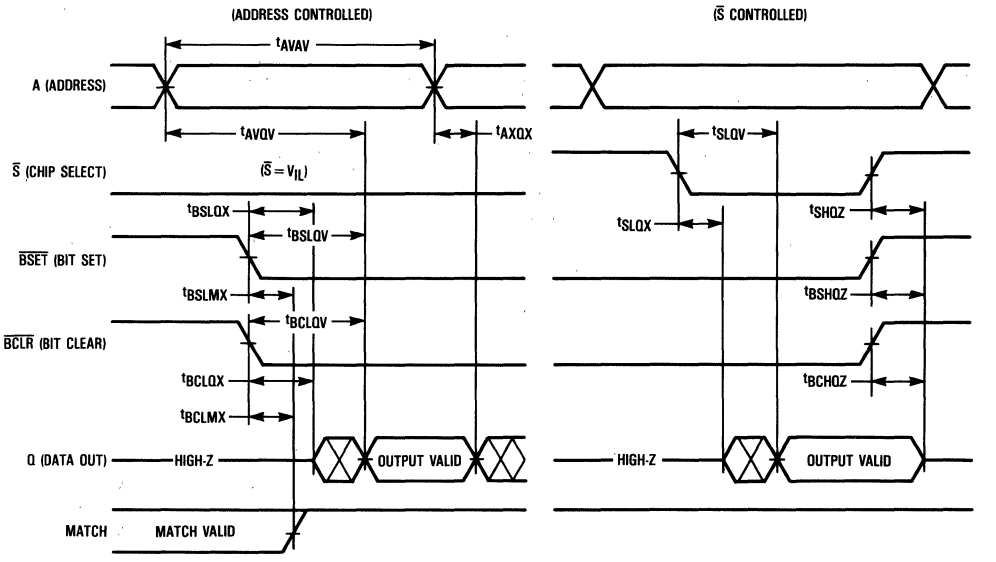
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load (I/O Pins) . . . . . See Figure 1a
Output Load (Match Output) . . . . . See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-22		MCM62350-25		MCM62350-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	30	–	35	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	30	–	35	ns	
Select Access Time	t_{SLQV}	t_{ACS}	–	12	–	15	–	15	ns	
$\overline{BCLR}$ Access Time	t_{BCLQV}	t_{ABC}	–	25	–	30	–	35	ns	2
$\overline{BSET}$ Access Time	t_{BSLQV}	t_{ABS}	–	25	–	30	–	35	ns	2
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Select Low to Output Active	t_{SLQX}	t_{CSL}	5	–	5	–	5	–	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Output Active	t_{BSLQX}/t_{BCLQX}	t_{LZ}	10	–	10	–	10	–	ns	3
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{CSZ}	–	9	–	10	–	12	ns	3
$\overline{BSET}$/$\overline{BCLR}$ High to Output High-Z	t_{BSHQZ}/t_{BCHQZ}	t_{HZ}	–	9	–	10	–	12	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Match Assert	t_{BSLMX}/t_{BCLMX}	t_{CH}	0	15	0	18	0	20	ns	

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles. One of either $\overline{BSET}$ or $\overline{BCLR}$ pins must be asserted low to activate the outputs. The match output becomes asserted when either the $\overline{BSET}$ or $\overline{BCLR}$ pin transitions low.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

READ CYCLE



COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-22		MCM62350-25		MCM62350-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	25	–	30	–	35	–	ns	
Address Valid to Match Valid	t_{AVMV}	t_{ACA}	–	22	–	25	–	30	ns	
$\overline{BCLR}$ High to Match Valid	t_{BCHMV}	t_{BCCA}	–	15	–	18	–	20	ns	2
$\overline{BSET}$ High to Match Valid	t_{BSHMV}	t_{BSCA}	–	15	–	18	–	20	ns	2
Data Valid to Match Valid	t_{DVMV}	t_{DCA}	–	10	–	12	–	15	ns	
$\overline{S}$ Low to Match Valid	t_{SLMV}	t_{CSCA}	–	15	–	18	–	20	ns	
Match Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	5	–	5	–	ns	
Match Hold from Data Change	t_{DXMX}	t_{DCH}	3	–	3	–	3	–	ns	
$\overline{S}$ High to Match Assert	t_{SHMX}	t_{CH}	0	10	0	12	0	15	ns	
$\overline{BCLR}$ High to Output High-Z	t_{BCHQZ}	t_{BCZ}	–	9	–	10	–	12	ns	3
$\overline{BSET}$ High to Output High-Z	t_{BSHQZ}	t_{BSZ}	–	9	–	10	–	12	ns	3

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during compare cycles.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

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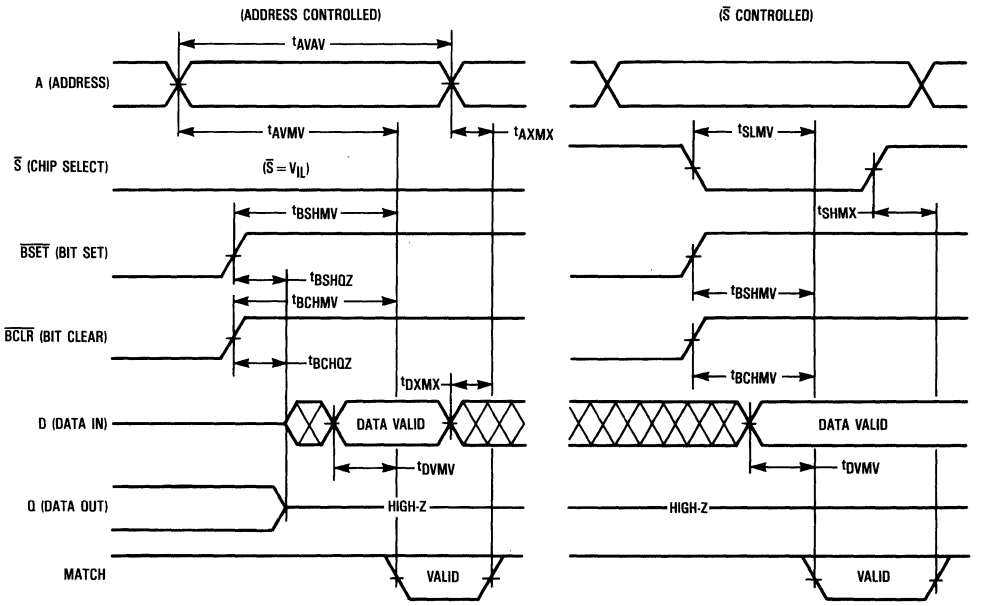
COMPARE CYCLE

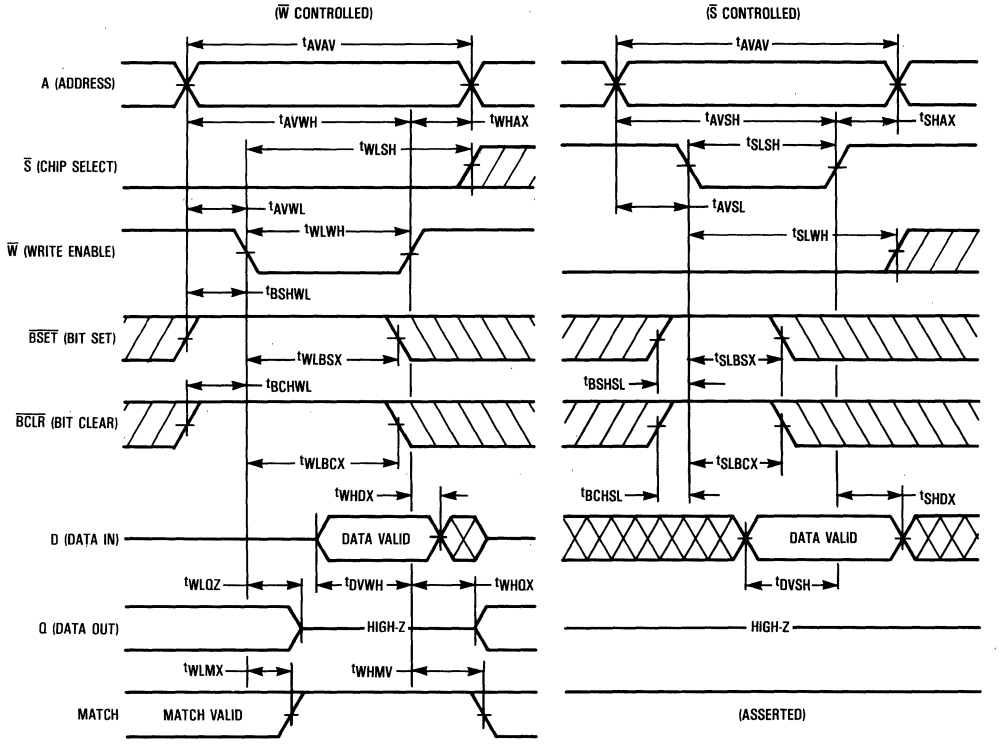


STANDARD WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-22		MCM62350-25		MCM62350-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	30	–	35	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	18	–	20	–	25	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	18	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVWH}/t_{DVSH}	t_{DW}	10	–	12	–	14	–	ns	
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	9	–	10	–	12	ns	2, 3
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	0	–	0	–	ns	
Write Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	18	ns	3
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSHWL}/t_{BSHSL} t_{BCHWL}/t_{BCHSL}	t_{BSS} t_{BCS}	−1	–	−1	–	−1	–	ns	
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	10	–	10	–	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	22	–	25	–	30	ns	3
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	ns	2, 3

NOTES:
1. A standard write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ and $\overline{BCLR}$ high. The $\overline{R}$ pin is high continuously during a write cycle.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.
3. Both the match output and Q0-Q3 are shown as valid in the $\overline{W}$ controlled cycle below to convey their timing relative to $\overline{W}$. In reality, only one of either match or Q0-Q3 can be valid at one time, as determined by $\overline{BSET}$and $\overline{BCLR}$ inputs.

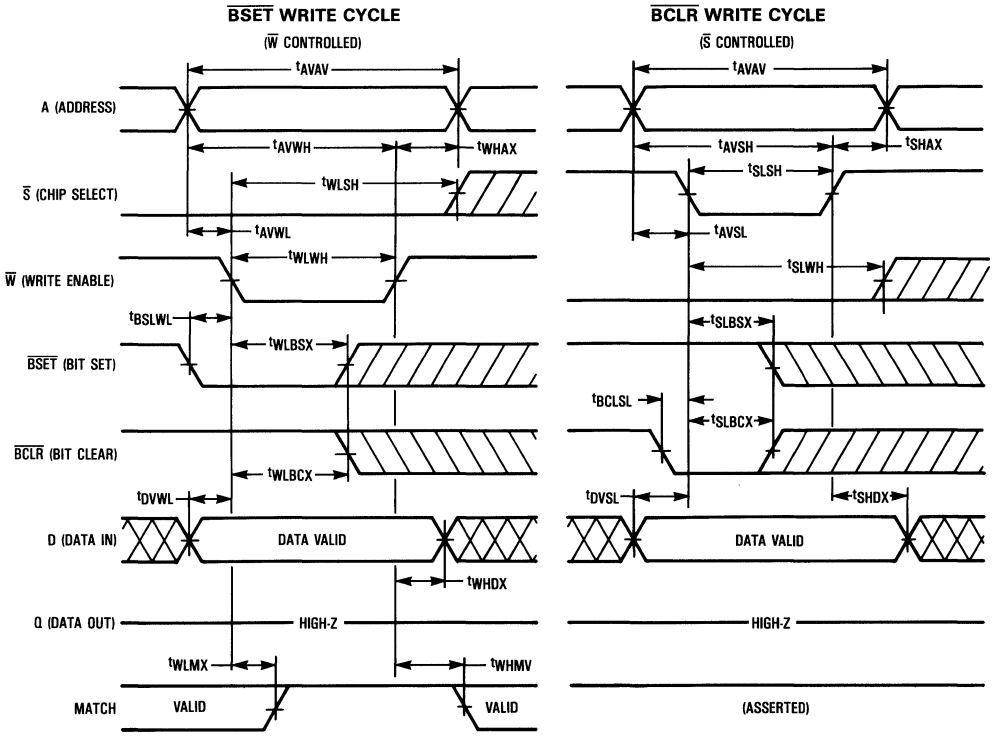
STANDARD WRITE CYCLE



$\overline{BSET}/\overline{BCLR}$ WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-22		MCM62350-25		MCM62350-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	18	—	20	—	25	—	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	18	—	20	—	25	—	ns	
Data Setup to Beginning of Write	t_{DVWL}/t_{DVSL}	t_{DS}	−1	—	−1	—	−1	—	ns	2
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	—	0	—	0	—	ns	
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	—	0	—	0	—	ns	
$\overline{W}$ Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	18	ns	
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSLWL}/t_{BSLSL} t_{BCLWL}/t_{BCLSL}	t_{BSS} t_{BCS}	−1	—	−1	—	−1	—	ns	2
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	—	10	—	10	—	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	—	22	—	25	—	30	ns	

NOTES:
1. A $\overline{BSET}/\overline{BCLR}$ write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ or $\overline{BCLR}$ low. The $\overline{R}$ pin is high continuously during a write cycle. $\overline{BSET}$ and $\overline{BCLR}$ write cycles can be $\overline{W}$ controlled or $\overline{S}$ controlled. Only two of four possible cycles are shown here for brevity.
2. Data output buffer must be in high-Z prior to start of either $\overline{BSET}$ or $\overline{BCLR}$ write cycles. Note that for $\overline{W}$ controlled cycles, the user must avoid excessive setup time of $\overline{BSET}/\overline{BCLR}$ to avoid bus contention. Data must be set up for t_{DVWL}/t_{DVSL} time to ensure the data integrity of non-modified bits during $\overline{BSET}/\overline{BCLR}$ write cycles. In the event that invalid data is presented for non-modified bits during the $\overline{BSET}/\overline{BCLR}$ write, note that it is not possible to recover the original data state by simply presenting valid data before the end of write.

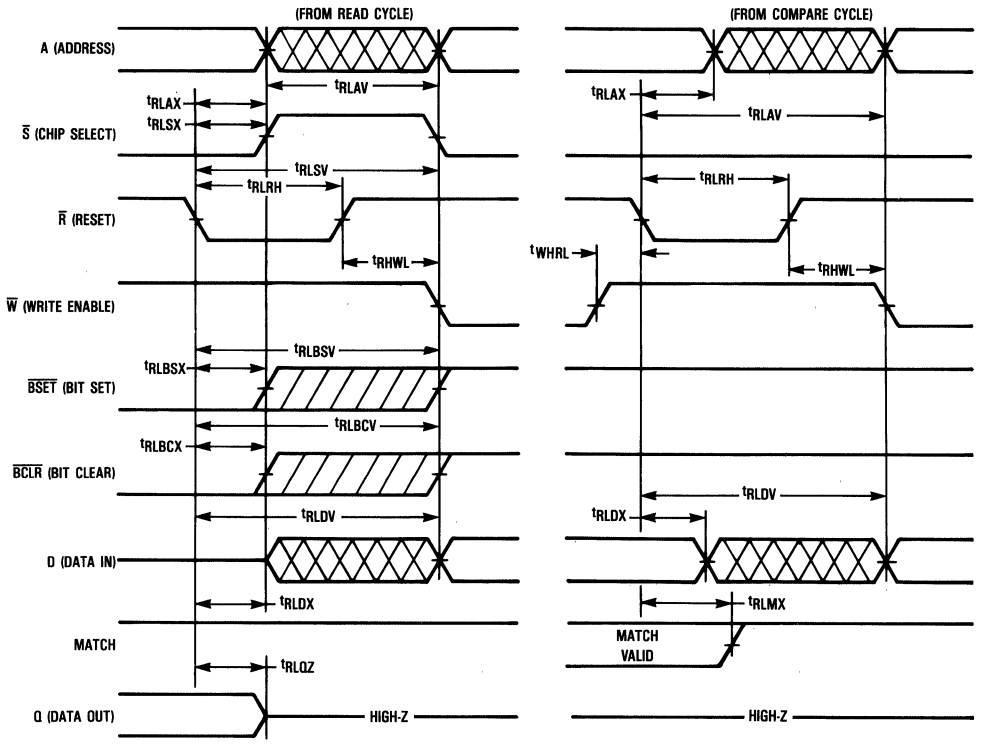


CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM62350-22		MCM62350-25		MCM62350-30		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{R}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{RLAV}	t_{CR}	–	70	–	70	–	70	ns	
	$\overline{S}$	t_{RLSV}	t_{CR}								
	$\overline{BSET}$	t_{RLBSV}	t_{CR}								
	$\overline{BCLR}$	t_{RLBCV}	t_{CR}								
	D	t_{RLDV}	t_{CR}								
$\overline{R}$ Pulse Width		t_{RLRH}	t_{CLP}	25	–	30	–	35	–	ns	
Read Setup to $\overline{R}$ Low		t_{WHRL}	t_{RS}	5	–	5	–	5	–	ns	2
Write Hold from $\overline{R}$ High		t_{RHWL}	t_{WH}	0	–	0	–	0	–	ns	2
$\overline{R}$ Low to Inputs Don't Care	A	t_{RLAX}	t_{CX}	0	–	0	–	0	–	ns	3
	$\overline{S}$	t_{RLSX}	t_{CX}								
	$\overline{BSET}$	t_{RLBSX}	t_{CX}								
	$\overline{BCLR}$	t_{RLBCX}	t_{CX}								
	D	t_{RLDX}	t_{CX}								
$\overline{R}$ Low to Match Assert		t_{RLMX}	t_{MH}	0	15	0	18	0	20	ns	
$\overline{R}$ Low to Output High-Z		t_{RLQZ}	t_{CZ}	–	15	–	18	–	20	ns	4

NOTES:
1. The address, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{R}$. The t_{WHRL} and t_{RHWL} parameters must be satisfied to prevent an undesired configuration cycle.
3. "Inputs" for this parameter refers to all inputs except $\overline{W}$.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE

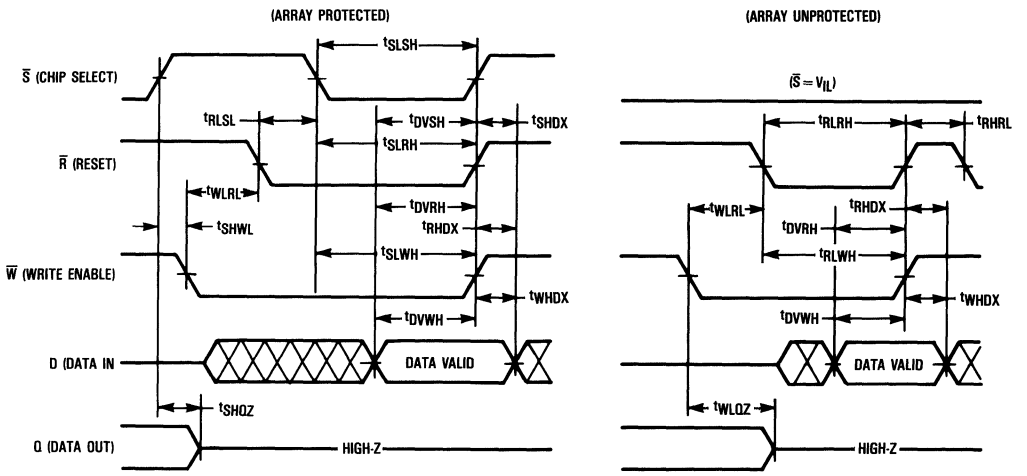


CONFIGURATION CYCLE (See Notes 1 and 2)

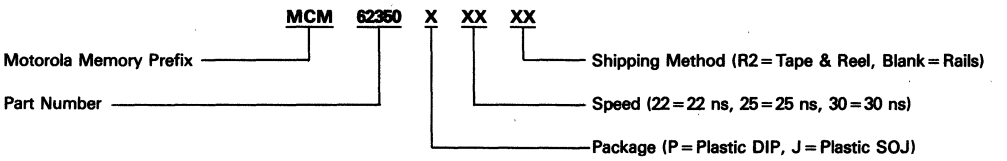
Characteristic		Symbol		MCM62350-22		MCM62350-25		MCM62350-30		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
Configuration Control Pulse Width	$\overline{S}$	t_{SLSH}	t_{SP}	20	—	25	—	30	—	ns	3
	$\overline{R}$	t_{RLRH}	t_{SP}								
Data Setup to End of Configuration Cycle	$\overline{S}$	t_{DVSH}	t_{DS}	10	—	12	—	14	—	ns	
	$\overline{R}$	t_{DVRH}	t_{DS}								
	$\overline{W}$	t_{DVWH}	t_{DS}								
Data Hold from End of Configuration Cycle	$\overline{S}$	t_{SHDX}	t_{DH}	0	—	0	—	0	—	ns	
	$\overline{R}$	t_{RHDX}	t_{DH}								
	$\overline{W}$	t_{WHDX}	t_{DH}								
$\overline{R}$ High Pulse Width		t_{RHRL}	t_{CP}	5	—	5	—	5	—	ns	
Write Setup to $\overline{R}$ Low		t_{WLRL}	t_{WS}	5	—	5	—	5	—	ns	
$\overline{S}$ Setup to End of Configuration		t_{SLWH}	t_{SWS}	20	—	25	—	30	—	ns	4
		t_{SLRH}	t_{SCS}								
$\overline{R}$ Setup to End of Configuration		t_{RLWH}	t_{SR}	20	—	25	—	30	—	ns	
$\overline{R}$ Setup to $\overline{S}$ Low		t_{RLSL}	t_{CSS}	5	—	5	—	5	—	ns	3
$\overline{S}$ Setup to Beginning of Write		t_{SHWL}	t_{WSS}	0	—	0	—	0	—	ns	
$\overline{S}$ High to Output High-Z		t_{SHQZ}	t_{HZ}	—	9	—	10	—	12	ns	5
$\overline{W}$ Low to Output High-Z		t_{WLQZ}	t_{HZ}	—	9	—	10	—	12	ns	5

NOTES:
1. A configuration cycle is performed during the overlap of $\overline{W}$ low, $\overline{R}$ low, and $\overline{S}$ low. Address, DQ2, DQ3, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during configuration cycles.
2. To ensure proper configuration of the device during power up, chip select must be equal to or greater than V_{IH}.
3. A valid configuration can be performed with $\overline{S}$ asserted prior to $\overline{R}$ and $\overline{W}$ low transitions. Be aware, however, that array data may be altered under this condition.
4. Note that terminating the cycle with $\overline{R}$ while leaving $\overline{W}$ and $\overline{S}$ asserted may cause array data to be altered.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CONFIGURATION CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM62350P22	MCM62350P25	MCM62350P30
	MCM62350J22	MCM62350J25	MCM62350J30
	MCM62350J22R2	MCM62350J25R2	MCM62350J30R2

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MCM62350-20

Product Preview

4K x 4 Bit Cache Address Tag Comparator

with System Status Bit Functions

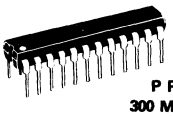
The MCM62350 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required. The MCM62350 is available in 24 lead plastic DIP and SOJ packages.

The device has a reset ($\overline{R}$) pin for flash clear of the RAM. This function is useful for system initialization. Individual bits within a tag field can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

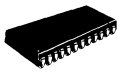
The MCM62350 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status bit applications). In addition, the match output can be programmed as true high or true low for potential logic delay savings. The configuration of these modes is accomplished by performing a write cycle with the $\overline{R}$ pin held low.

The MCM62350 is available in a 24 lead plastic or sidebrazed DIP, as well as a 24 lead plastic SOJ package.

- Single 5 V ±10% Power Supply
- Fast Address to Match Time; 20 ns max
- Fast Data to Match Time; 10 ns max
- Fast Read of Tag RAM Contents; 20 ns max
- Flash Clear of the Tag RAM; 70 ns max
- Programmable Active Output Level of Match
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes:
  - XNOR Mode for Address Tag Comparison
  - AOI Mode for System Valid Bit Comparison

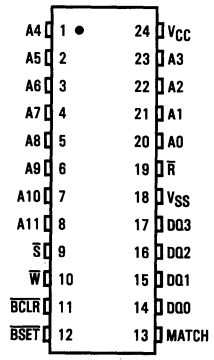


P PACKAGE
300 MIL PLASTIC
CASE 724

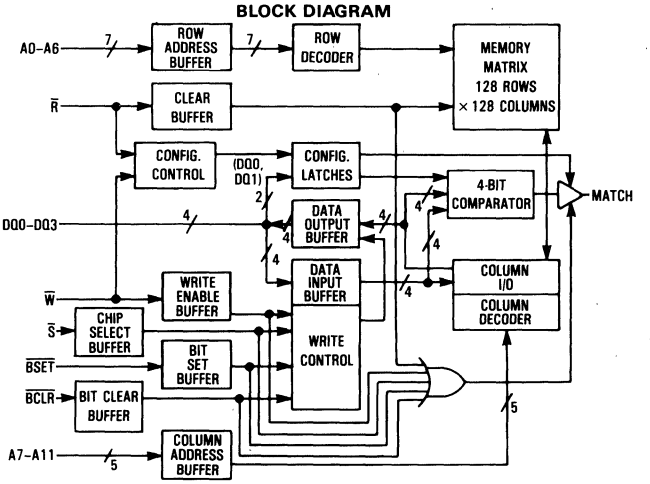


J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

SIGNAL DESCRIPTIONS

A0-A11—ADDRESS INPUTS

The address lines are used for indexing into the tag RAM portion of the chip.

DQ0-DQ3—DATA INPUT/OUTPUT

The data lines are used as input for compare, write, and configuration cycles, and as output for read cycles.

$\overline{BSET}$—BIT SET CONTROL INPUT

This control signal is used for ORing data into the tag RAM during $\overline{BSET}$ write cycles. Independent bits within the tag can be set using the appropriate mask, as indicated in the bit set truth table. The $\overline{BSET}$ input can also be used to initiate a read cycle.

$\overline{BCLR}$—BIT CLEAR CONTROL INPUT

This control signal is used for ANDing the complement of data into the tag RAM during $\overline{BCLR}$ write cycles. Independent bits within the tag can be cleared using the appropriate mask, as indicated in the bit clear truth table. The $\overline{BCLR}$ input can also be used to initiate a read cycle (note that at least one of the $\overline{BSET}$/$\overline{BCLR}$ signals must be asserted to trigger a read cycle).

$\overline{R}$—RESET (FLASH CLEAR) INPUT

The reset control signal is used to initiate a clear cycle or a configuration cycle.

$\overline{S}$—CHIP SELECT

This control signal is used to chip select the device.

$\overline{W}$—WRITE ENABLE

The write enable signal is used to initiate write cycles.

MATCH—MATCH (HIT) OUTPUT

This output signal is used to indicate a match of DQ0-DQ3 inputs with the contents of the tag RAM addressed by A0—A11.

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FUNCTIONAL TRUTH TABLE

$\overline{S}$	$\overline{W}$	$\overline{BCLR}$	$\overline{BSET}$	$\overline{R}$	DQ0-DQ3	Match	Cycle
L	H	H	H	H	Compare D_{in}	Valid	Compare
L	H	L	X	H	Read D_{out}	Assert	Read
L	H	X	L	H	Read D_{out}	Assert	Read
L	L	H	H	H	Write D_{in}	Assert	Write
L	L	L	H	H	Bit Clear Mask	Assert	$\overline{BCLR}$ Write
L	L	H	L	H	Bit Set Mask	Assert	$\overline{BSET}$ Write
X	H	X	X	L	High-Z	Assert	Clear (Reset)
L	L	X	X	L	Config D_{in}*	Assert	Configuration
H	X	X	X	H	High-Z	Assert	Deselect

*DQ2 and DQ3 are don't cares during a configuration cycle.

COMPARATOR BEHAVIORAL TABLE

Type	DQ0	DQ1	DQ2	DQ3	RAMQ0	RAMQ1	RAMQ2	RAMQ3	Match
XNOR	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
XNOR	$\overline{Q0}$	Q1	Q2	Q3	Q0	Q1	Q2	Q3	0
AOI	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
AOI	L	Q1	Q2	Q3	X	Q1	Q2	Q3	1
AOI	H	Q1	Q2	Q3	L	Q1	Q2	Q3	0

L = Low
H = High
0 = False
1 = True
X = Don't Care

BIT CLEAR TRUTH TABLE (See Note)

Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	0	Bit Cleared
1	1	0	to "Zero"

BIT SET TRUTH TABLE (See Note)

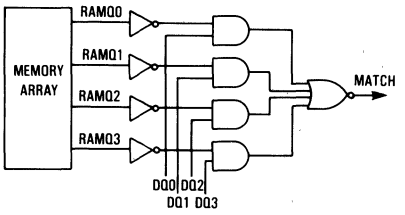
Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	1	Bit Set
1	1	1	to "One"

NOTE: These tables reflect the behavior of single bit positions. The four bits in the tag can all be set or cleared in tandem, or bits within the tag can be independently set or cleared with the appropriate mask.

CONFIGURATION TABLE

DQ0	DQ1	Comparator Type	Match True Level
L	L	XNOR	Low
L	H	XNOR	High
H	L	AOI	Low
H	H	AOI	High

AOI COMPARATOR LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The power supply (V_{CC}) should be stable for at least 100 μs before operating the device. During this interval, the part will internally configure itself for XNOR compares. In addition, the memory array of RAM bits will be cleared.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current, Except Match Output ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{S}$ = V_{IL}, I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	–	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 12.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, Match Output: I_{OH} = −10.0 mA)	V_{OH}	2.4	–	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
Match Output Capacitance	C_{match}	6	7	pF

AC TEST LOADS

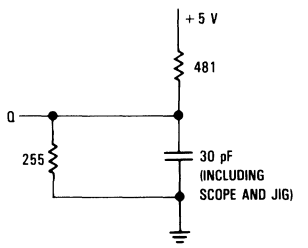


Figure 1a

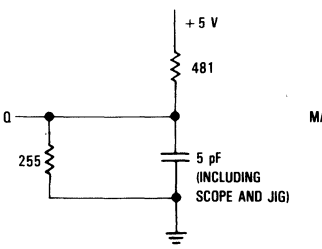


Figure 1b

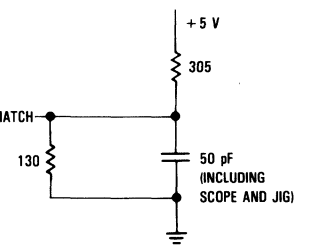


Figure 1c

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

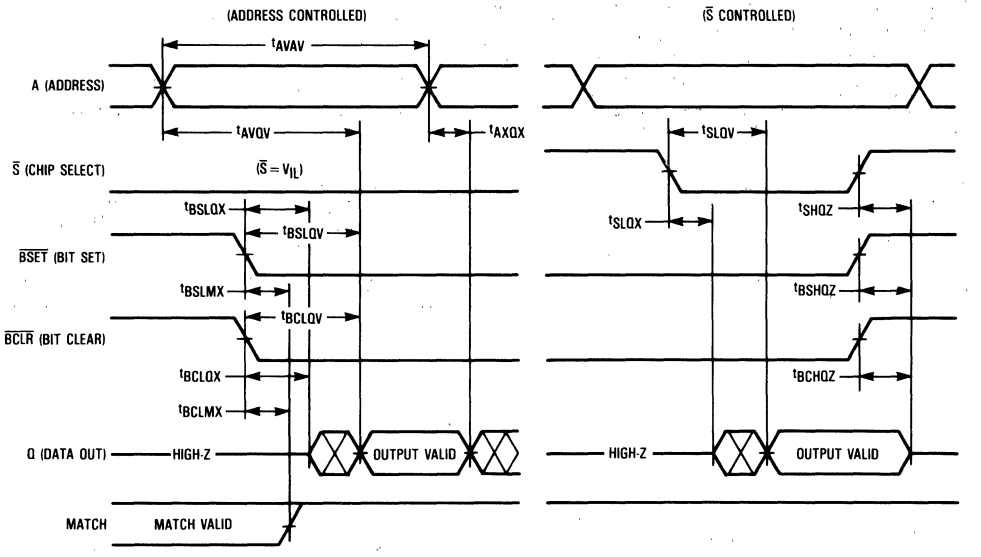
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load (I/O Pins) . . . . . See Figure 1a
Output Load (Match Output) . . . . . See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-20		Unit	Notes
	Standard	Alternate	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	20	ns	
Select Access Time	t_{SLQV}	t_{ACS}	–	11	ns	
$\overline{BCLR}$ Access Time	t_{BCLQV}	t_{ABC}	–	20	ns	2
$\overline{BSET}$ Access Time	t_{BSLQV}	t_{ABS}	–	20	ns	2
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	ns	
Select Low to Output Active	t_{SLQX}	t_{CSL}	5	–	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Output Active	t_{BSLQX}/t_{BCLQX}	t_{LZ}	7	–	ns	3
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{CSZ}	–	8	ns	3
$\overline{BSET}$/$\overline{BCLR}$ High to Output High-Z	t_{BSHQZ}/t_{BCHQZ}	t_{HZ}	–	8	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Match Assert	t_{BSLMX}/t_{BCLMX}	t_{CH}	0	15	ns	

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles. One of either $\overline{BSET}$ or $\overline{BCLR}$ pins must be asserted low to activate the outputs. The match output becomes asserted when either the $\overline{BSET}$ or $\overline{BCLR}$ pin transitions low.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

READ CYCLE



COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-20		Unit	Notes
	Standard	Alternate	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	20	–	ns	
Address Valid to Match Valid	t_{AVMV}	t_{ACA}	–	20	ns	
$\overline{BCLR}$ High to Match Valid	t_{BCHMV}	t_{BCCA}	–	15	ns	2
$\overline{BSET}$ High to Match Valid	t_{BSHMV}	t_{BSCA}	–	15	ns	2
Data Valid to Match Valid	t_{DVMV}	t_{DCA}	–	10	ns	
$\overline{S}$ Low to Match Valid	t_{SLMV}	t_{CSCA}	–	12	ns	
Match Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	ns	
Match Hold from Data Change	t_{DXMX}	t_{DCH}	3	–	ns	
$\overline{S}$ High to Match Assert	t_{SHMX}	t_{CH}	0	10	ns	
$\overline{BCLR}$ High to Output High-Z	t_{BCHQZ}	t_{BCZ}	–	8	ns	3
$\overline{BSET}$ High to Output High-Z	t_{BSHQZ}	t_{BSZ}	–	8	ns	3

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during compare cycles.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

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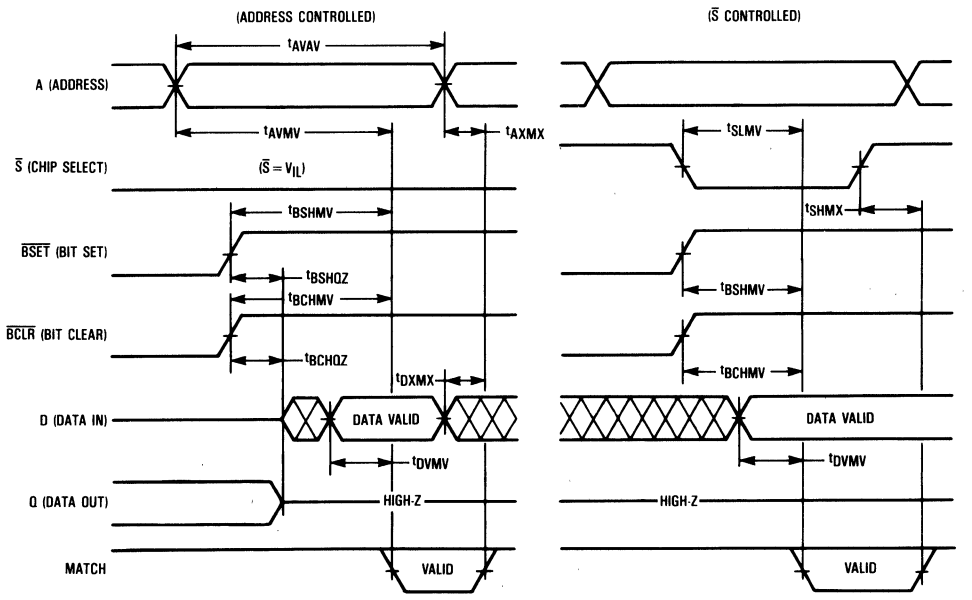
COMPARE CYCLE

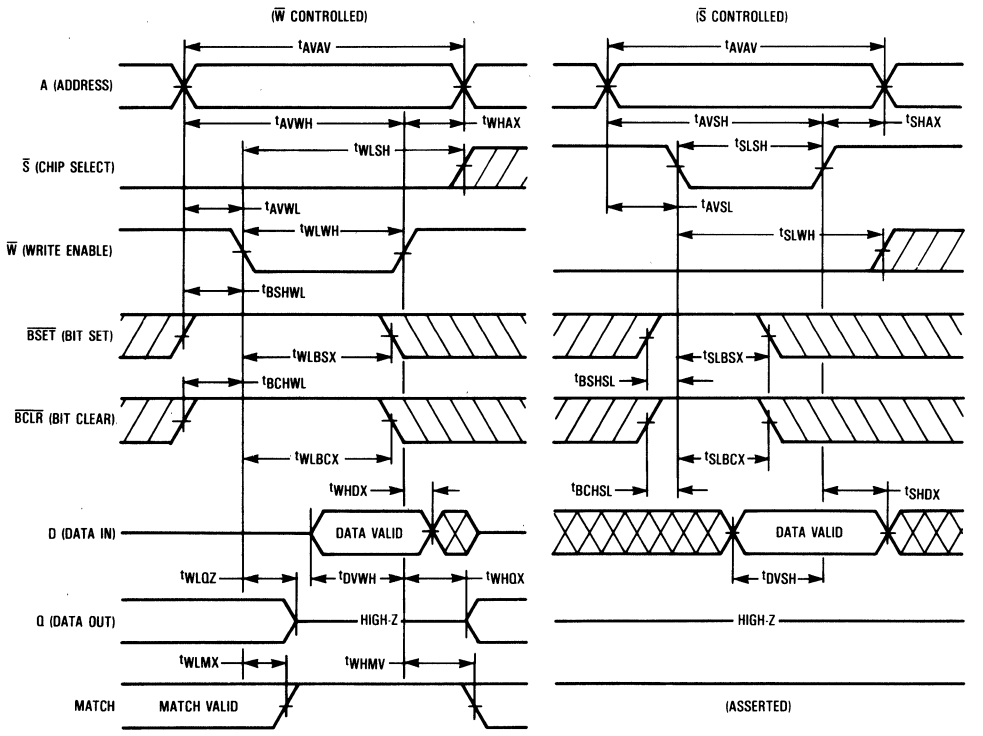


STANDARD WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	16	–	ns	
Data Valid to End of Write	t_{DVWH}/t_{DVSH}	t_{DW}	10	–	ns	
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	8	ns	2, 3
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	ns	
Write Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	ns	3
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSHWL}/t_{BSHSL} t_{BCHWL}/t_{BCHSL}	t_{BSS} t_{BCS}	−1	–	ns	
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	20	ns	3
Write High to Output Active	t_{WHQX}	t_{OW}	3	–	ns	2, 3

NOTES:
1. A standard write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ and $\overline{BCLR}$ high. The $\overline{R}$ pin is high continuously during a write cycle.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.
3. Both the match output and Q0-Q3 are shown as valid in the $\overline{W}$ controlled cycle below to convey their timing relative to $\overline{W}$. In reality, only one of either match or Q0-Q3 can be valid at one time, as determined by $\overline{BSET}$and $\overline{BCLR}$ inputs.

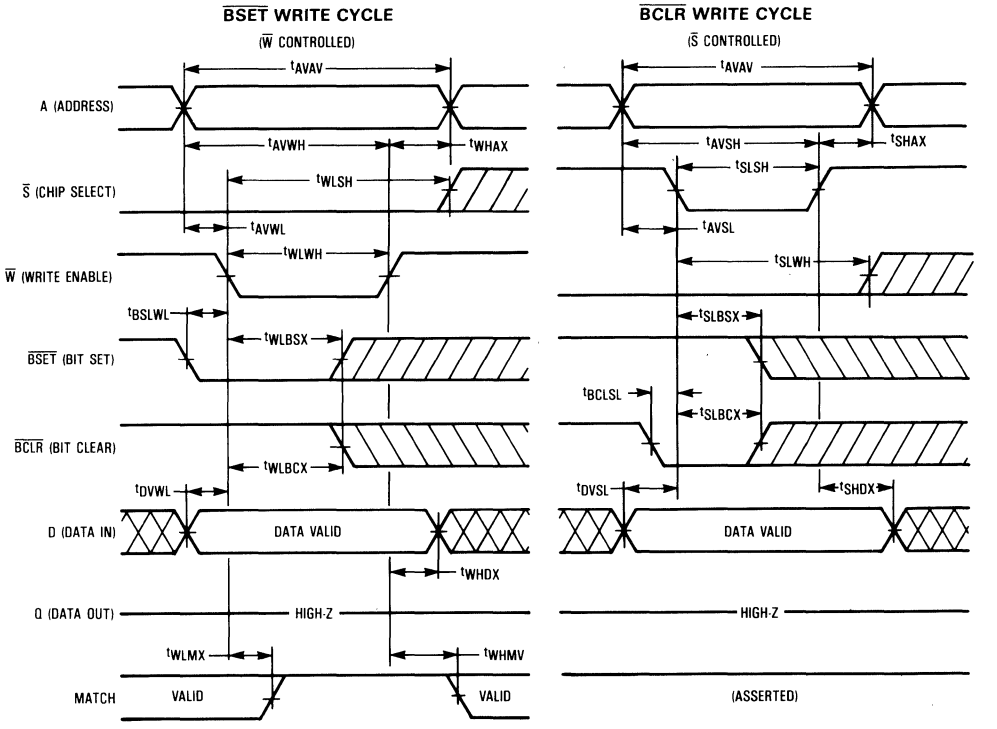
STANDARD WRITE CYCLE



$\overline{\text{BSET}}/\overline{\text{BCLR}}$ WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62350-20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	14	–	ns	
Data Setup to Beginning of Write	t_{DVWL}/t_{DVSL}	t_{DS}	0	–	ns	2
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	ns	
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	ns	
$\overline{\text{W}}$ Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	ns	
$\overline{\text{BSET}}/\overline{\text{BCLR}}$ Setup to Beginning of Write	t_{BSLWL}/t_{BSLSL} t_{BCLWL}/t_{BCLSL}	t_{BSS} t_{BCS}	−1	–	ns	2
$\overline{\text{BSET}}/\overline{\text{BCLR}}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	20	ns	

NOTES:
1. A $\overline{\text{BSET}}/\overline{\text{BCLR}}$ write occurs during the overlap of $\overline{\text{W}}$ and $\overline{\text{S}}$ low and $\overline{\text{BSET}}$ or $\overline{\text{BCLR}}$ low. The $\overline{\text{R}}$ pin is high continuously during a write cycle. $\overline{\text{BSET}}$ and $\overline{\text{BCLR}}$ write cycles can be $\overline{\text{W}}$ controlled or $\overline{\text{S}}$ controlled. Only two of four possible cycles are shown here for brevity.
2. Data output buffer must be in high-Z prior to start of either $\overline{\text{BSET}}$ or $\overline{\text{BCLR}}$ write cycles. Note that for $\overline{\text{W}}$ controlled cycles, the user must avoid excessive setup time of $\overline{\text{BSET}}/\overline{\text{BCLR}}$ to avoid bus contention. Data must be set up for t_{DVWL}/t_{DVSL} time to ensure the data integrity of non-modified bits during $\overline{\text{BSET}}/\overline{\text{BCLR}}$ write cycles. In the event that invalid data is presented for non-modified bits during the $\overline{\text{BSET}}/\overline{\text{BCLR}}$ write, note that it is not possible to recover the original data state by simply presenting valid data before the end of write.



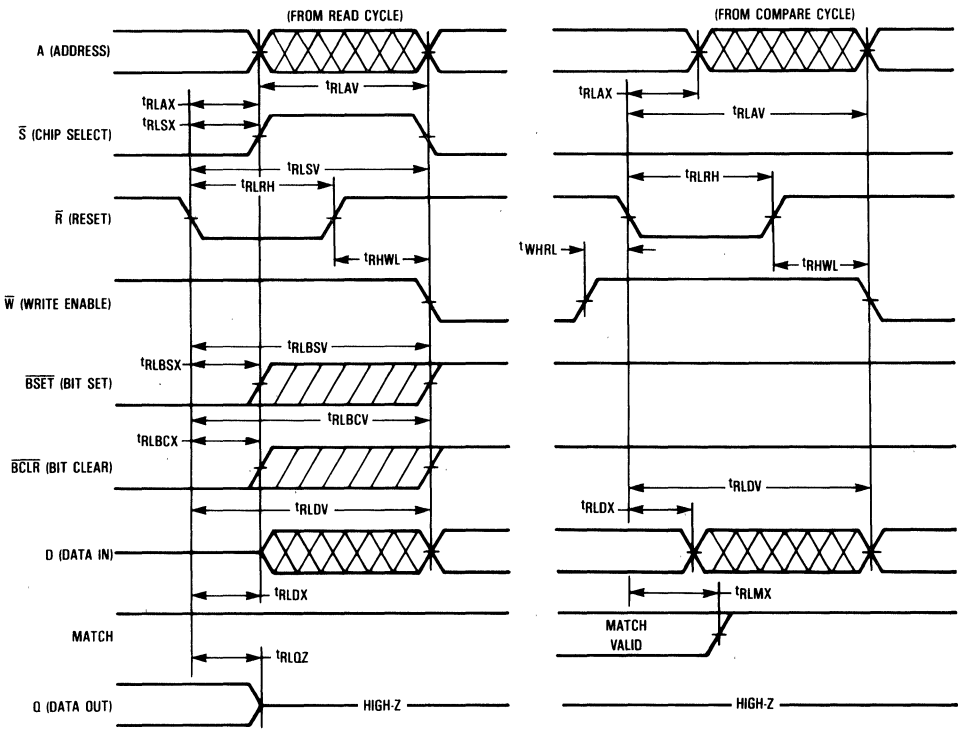
CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM62350-20		Unit	Notes
		Standard	Alternate	Min	Max		
$\overline{R}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{RLAV}	t_{CR}	–	70	ns	
	$\overline{S}$	t_{RLSV}	t_{CR}				
	$\overline{BSET}$	t_{RLBSV}	t_{CR}				
	$\overline{BCLR}$	t_{RLBCV}	t_{CR}				
	D	t_{RLDV}	t_{CR}				
$\overline{R}$ Pulse Width		t_{RLRH}	t_{CLP}	20	–	ns	
Read Setup to $\overline{R}$ Low		t_{WHRL}	t_{RS}	5	–	ns	2
Write Hold from $\overline{R}$ High		t_{RHWL}	t_{WH}	0	–	ns	2
$\overline{R}$ Low to Inputs Don't Care	A	t_{RLAX}	t_{CX}	0	–	ns	3
	$\overline{S}$	t_{RLSX}	t_{CX}				
	$\overline{BSET}$	t_{RLBSX}	t_{CX}				
	$\overline{BCLR}$	t_{RLBCX}	t_{CX}				
	D	t_{RLDX}	t_{CX}				
$\overline{R}$ Low to Match Assert		t_{RLMX}	t_{MH}	0	15	ns	
$\overline{R}$ Low to Output High-Z		t_{RLQZ}	t_{CZ}	–	15	ns	4

5

NOTES:
1. The address, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{R}$. The t_{WHRL} and t_{RHWL} parameters must be satisfied to prevent an undesired configuration cycle.
3. "Inputs" for this parameter refers to all inputs except $\overline{W}$.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE

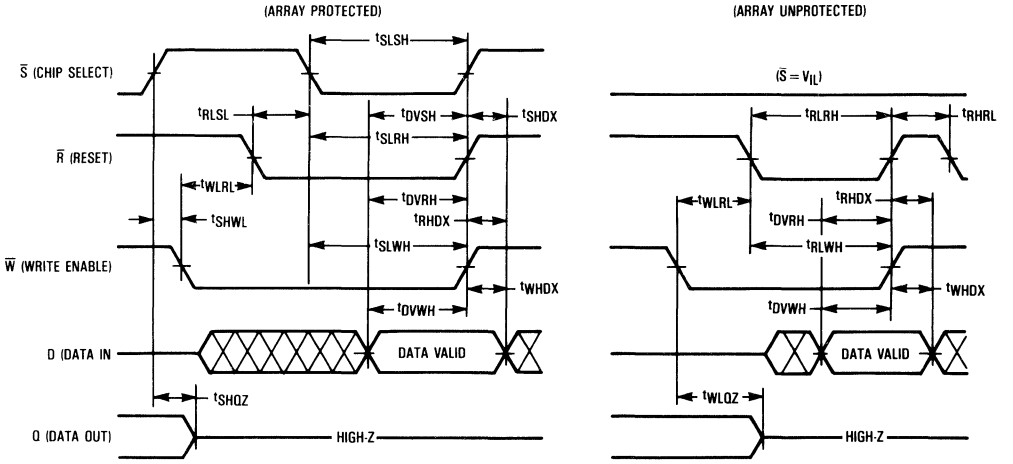


CONFIGURATION CYCLE (See Notes 1 and 2)

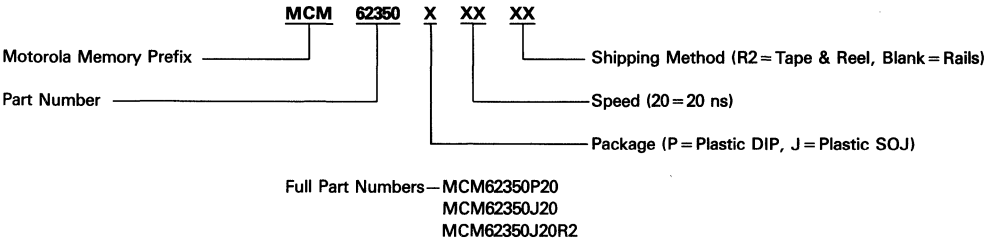
Characteristic		Symbol		MCM62350-20		Unit	Notes
		Standard	Alternate	Min	Max		
Configuration Control Pulse Width	$\overline{S}$ $\overline{R}$	t_{SLSH} t_{RLRH}	t_{SP} t_{SP}	20	–	ns	3
Data Setup to End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{DVSH} t_{DVRH} t_{DVWH}	t_{DS} t_{DS} t_{DS}	10	–	ns	
Data Hold from End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{SHDX} t_{RHDX} t_{WHDX}	t_{DH} t_{DH} t_{DH}	0	–	ns	
$\overline{R}$ High Pulse Width		t_{RHRL}	t_{CP}	5	–	ns	
Write Setup to $\overline{R}$ Low		t_{WLRL}	t_{WS}	5	–	ns	
$\overline{S}$ Setup to End of Configuration		t_{SLWH} t_{SLRH}	t_{SWS} t_{SCS}	20	–	ns	4
$\overline{R}$ Setup to End of Configuration		t_{RLWH}	t_{SR}	20	–	ns	
$\overline{R}$ Setup to $\overline{S}$ Low		t_{RLSL}	t_{CSS}	5	–	ns	3
$\overline{S}$ Setup to Beginning of Write		t_{SHWL}	t_{WSS}	0	–	ns	
$\overline{S}$ High to Output High-Z		t_{SHQZ}	t_{HZ}	–	9	ns	5
$\overline{W}$ Low to Output High-Z		t_{WLQZ}	t_{HZ}	–	9	ns	5

NOTES:
1. A configuration cycle is performed during the overlap of $\overline{W}$ low, $\overline{R}$ low, and $\overline{S}$ low. Address, DQ2, DQ3, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during configuration cycles.
2. To ensure proper configuration of the device during power up, chip select must be equal to or greater than V_{IH}.
3. A valid configuration can be performed with $\overline{S}$ asserted prior to $\overline{R}$ and $\overline{W}$ low transitions. Be aware, however, that array data may be altered under this condition.
4. Note that terminating the cycle with $\overline{R}$ while leaving $\overline{W}$ and $\overline{S}$ asserted may cause array data to be altered.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CONFIGURATION CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM62350P20
MCM62350J20
MCM62350J20R2

5

MCM62351

4K x 4 Bit Cache Address Tag Comparator

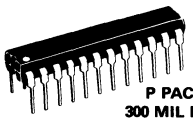
with System Status Bit Functions

The MCM62351 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required.

The device has a reset ($\overline{R}$) pin for flash clear of the RAM, which is useful for system initialization. Individual bits within a tag can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

The MCM62351 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status applications). The configuration of the comparator is accomplished by performing a write cycle with the $\overline{R}$ pin held low. The match output is open drain, allowing efficient combination of multiple match outputs using a wired-OR connection.

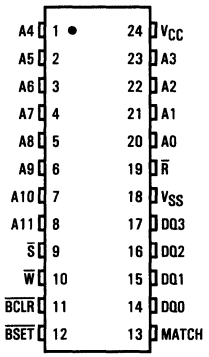
- Single 5 V ±10% Power Supply
- Fast Address to Match Time; 22/25/30 ns max
- Fast Data to Match Time; 10/12/15 ns max
- Fast Read of Tag RAM Contents; 25/30/35 ns max
- Flash Clear of the Tag RAM; 70/70/70 ns max
- Open Drain Match Output
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes:
  - XNOR Mode for Address Tag Comparison
  - AOI Mode for System Valid Bit Comparison
- High Board Density SOJ Package Available



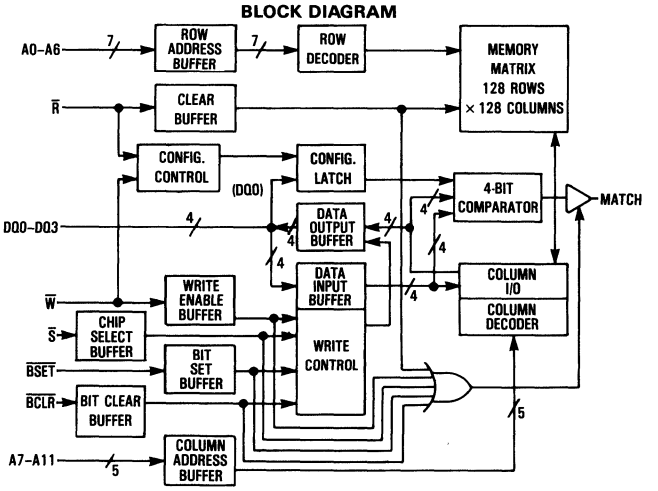
P PACKAGE
300 MIL PLASTIC
CASE 724

J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

5

SIGNAL DESCRIPTIONS

A0-A11—ADDRESS INPUTS

The address lines are used for indexing into the tag RAM portion of the chip.

DQ0-DQ3—DATA INPUT/OUTPUT

The data lines are used as input for compare, write, and configuration cycles, and as output for read cycles.

$\overline{BSET}$—BIT SET CONTROL INPUT

This control signal is used for ORing data into the tag RAM during $\overline{BSET}$ write cycles. Independent bits within the tag can be set using the appropriate mask, as indicated in the bit set truth table. The $\overline{BSET}$ input can also be used to initiate a read cycle.

$\overline{BCLR}$—BIT CLEAR CONTROL INPUT

This control signal is used for ANDing the complement of data into the tag RAM during $\overline{BCLR}$ write cycles. Independent bits within the tag can be cleared using the appropriate mask, as indicated in the bit clear truth table. The $\overline{BCLR}$ input can also be used to initiate a read cycle (note that at least one of the $\overline{BSET}$/$\overline{BCLR}$ signals must be asserted to trigger a read cycle).

$\overline{R}$—RESET (FLASH CLEAR) INPUT

The reset control signal is used to initiate a clear cycle or a configuration cycle.

$\overline{S}$—CHIP SELECT

This control signal is used to chip select the device.

$\overline{W}$—WRITE ENABLE

The write enable signal is used to initiate write cycles.

MATCH—MATCH (HIT) OUTPUT

This output signal is used to indicate a match of DQ0-DQ3 inputs with the contents of the tag RAM addressed by A0—A11.

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FUNCTIONAL TRUTH TABLE

$\overline{S}$	$\overline{W}$	$\overline{BCLR}$	$\overline{BSET}$	$\overline{R}$	DQ0-DQ3	Match	Cycle
L	H	H	H	H	Compare D_{in}	Valid	Compare
L	H	L	X	H	Read D_{out}	Assert	Read
L	H	X	L	H	Read D_{out}	Assert	Read
L	L	H	H	H	Write D_{in}	Assert	Write
L	L	L	H	H	Bit Clear Mask	Assert	$\overline{BCLR}$ Write
L	L	H	L	H	Bit Set Mask	Assert	$\overline{BSET}$ Write
X	H	X	X	L	High-Z	Assert	Clear (Reset)
L	L	X	X	L	Config D_{in}*	Assert	Configuration
H	X	X	X	H	High-Z	Assert	Deselect

*DQ1, DQ2, and DQ3 are don't cares during a configuration cycle.

COMPARATOR TRUTH TABLE

Type	DQ0	DQ1	DQ2	DQ3	RAMQ0	RAMQ1	RAMQ2	RAMQ3	Match
XNOR	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
XNOR	$\overline{Q0}$	Q1	Q2	Q3	Q0	Q1	Q2	Q3	0
AOI	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
AOI	L	Q1	Q2	Q3	X	Q1	Q2	Q3	1
AOI	H	Q1	Q2	Q3	L	Q1	Q2	Q3	0

L = Low
H = High
0 = False
1 = True
X = Don't Care

BIT CLEAR TRUTH TABLE (See Note)

Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	0	Bit Cleared
1	1	0	to "Zero"

BIT SET TRUTH TABLE (See Note)

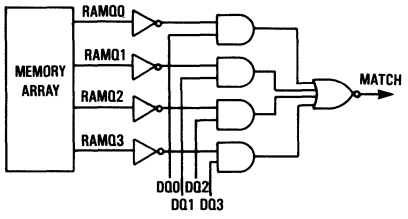
Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	1	Bit Set
1	1	1	to "One"

NOTE: These tables reflect the behavior of single bit positions. The four bits in the tag can all be set or cleared in tandem, or bits within the tag can be independently set or cleared with the appropriate mask.

CONFIGURATION TABLE

DQ0	Comparator Type
L	XNOR
H	AOI

AOI COMPARATOR LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC}+0.5	V
Output Current — Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

The power supply (V_{CC}) should be stable for at least 100 μs before operating the device. During this interval, the part will internally configure itself for XNOR compares. In addition, the memory array of RAM bits will be cleared.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
Match Output Leakage Current (Match Asserted)	$I_{lkg(M)}$	—	±2.0	μA
AC Supply Current ($\overline{S}$ = V_{IL}, I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	—	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 23.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I/O Pins: I_{OH} = 4.0 mA)	V_{OH}	2.4	—	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
Match Output Capacitance	C_{match}	6	7	pF

AC TEST LOADS

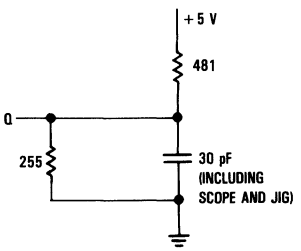


Figure 1a

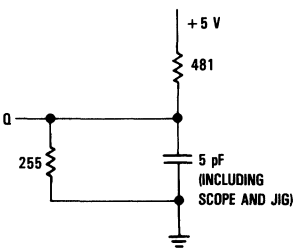


Figure 1b

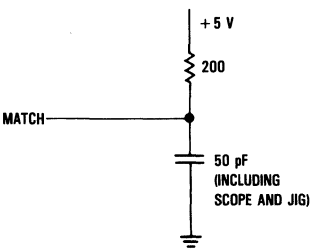


Figure 1c

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

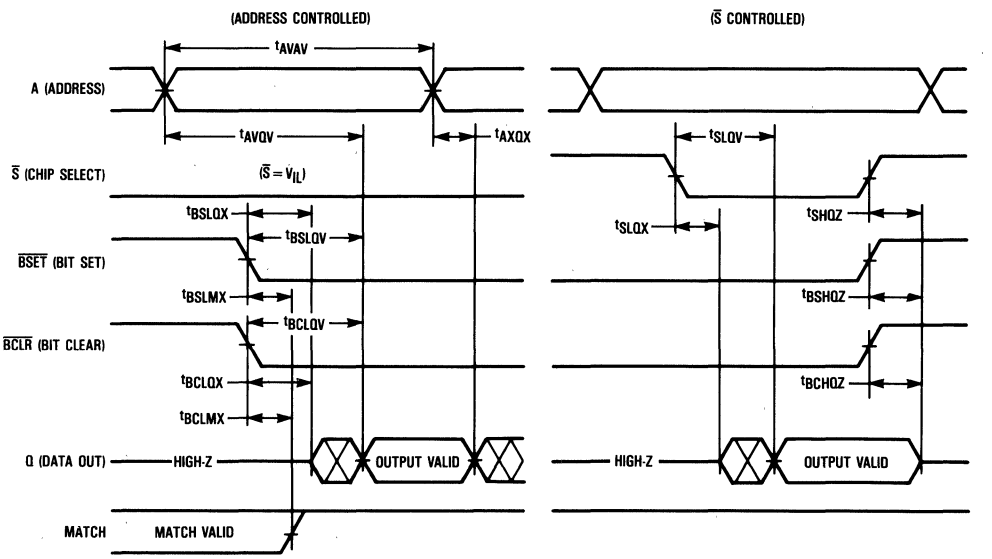
Input Timing Measurement Reference Level	1.5 V
Input Pulse Levels	0 to 3.0 V
Input Rise/Fall Time	5 ns
Output Timing Measurement Reference Level	1.5 V
Output Load (I/O Pins)	See Figure 1a
Output Load (Match Output)	See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-22		MCM62351-25		MCM62351-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	30	–	35	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	30	–	35	ns	
Select Access Time	t_{SLQV}	t_{ACS}	–	12	–	15	–	15	ns	
$\overline{BCLR}$ Access Time	t_{BCLQV}	t_{ABC}	–	25	–	30	–	35	ns	2
$\overline{BSET}$ Access Time	t_{BSLQV}	t_{ABS}	–	25	–	30	–	35	ns	2
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Select Low to Output Active	t_{SLQX}	t_{CSL}	5	–	5	–	5	–	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Output Active	t_{BSLQX}/t_{BCLQX}	t_{LZ}	10	–	10	–	10	–	ns	3
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{CSZ}	–	9	–	10	–	12	ns	3
$\overline{BSET}$/$\overline{BCLR}$ High to Output High-Z	t_{BSHQZ}/t_{BCHQZ}	t_{HZ}	–	9	–	10	–	12	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Match Assert	t_{BSLMX}/t_{BCLMX}	t_{CH}	0	15	0	18	0	20	ns	

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles. One of either $\overline{BSET}$ or $\overline{BCLR}$ pins must be asserted low to activate the outputs. The match output becomes asserted when either the $\overline{BSET}$ or $\overline{BCLR}$ pin transitions low.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

READ CYCLE



COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-22		MCM62351-25		MCM62351-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	25	–	30	–	35	–	ns	
Address Valid to Match Valid	t_{AVMV}	t_{ACA}	–	22	–	25	–	30	ns	
$\overline{BCLR}$ High to Match Valid	t_{BCHMV}	t_{BCCA}	–	15	–	18	–	20	ns	2
$\overline{BSET}$ High to Match Valid	t_{BSHMV}	t_{BSCA}	–	15	–	18	–	20	ns	2
Data Valid to Match Valid	t_{DVMV}	t_{DCA}	–	10	–	12	–	15	ns	
$\overline{S}$ Low to Match Valid	t_{SLMV}	t_{CSCA}	–	15	–	18	–	20	ns	
Match Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	5	–	5	–	ns	
Match Hold from Data Change	t_{DXMX}	t_{DCH}	3	–	3	–	3	–	ns	
$\overline{S}$ High to Match Assert	t_{SHMX}	t_{CH}	0	10	0	12	0	15	ns	
$\overline{BCLR}$ High to Output High-Z	t_{BCHOZ}	t_{BCZ}	–	9	–	10	–	12	ns	3
$\overline{BSET}$ High to Output High-Z	t_{BSHOZ}	t_{BSZ}	–	9	–	10	–	12	ns	3

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during compare cycles.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

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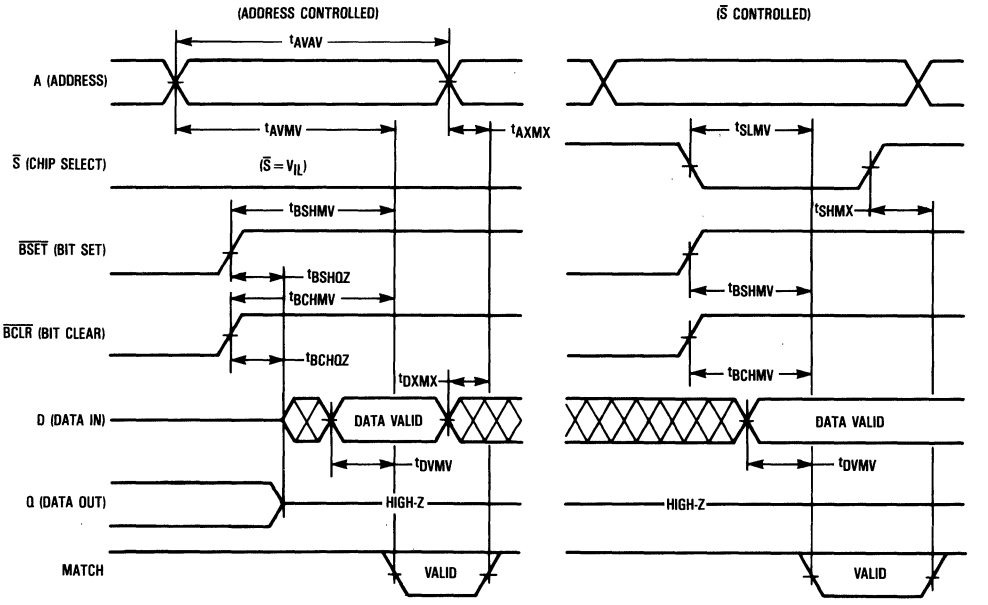
COMPARE CYCLE

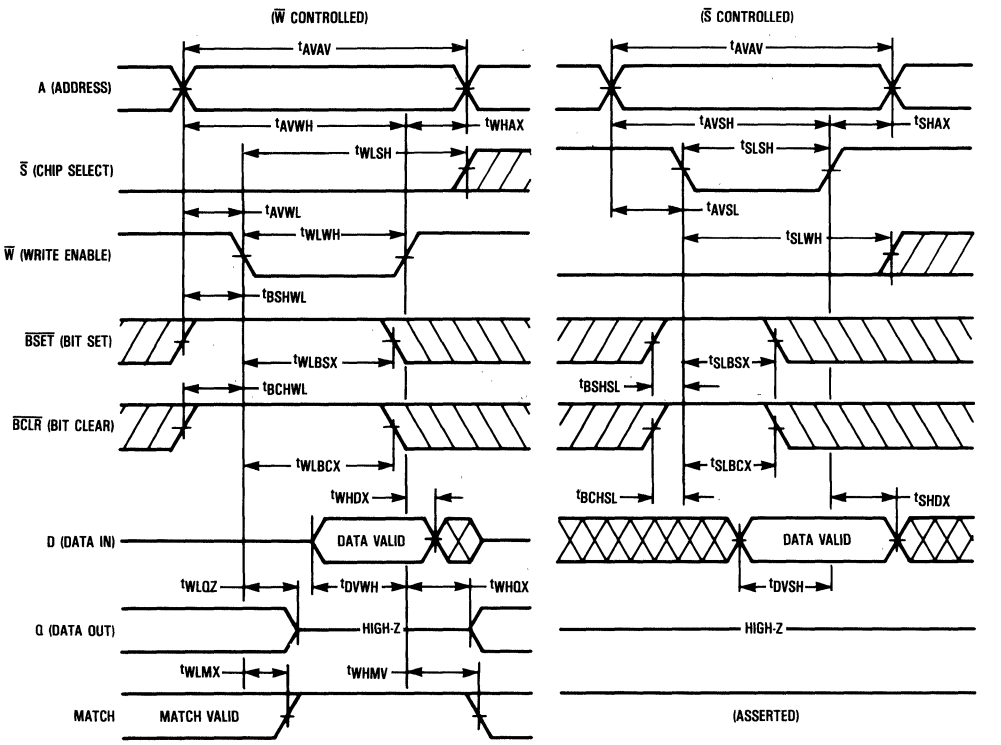


STANDARD WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-22		MCM62351-25		MCM62351-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	30	–	35	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	18	–	20	–	25	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	18	–	20	–	25	–	ns	
Data Valid to End of Write	t_{DVWH}/t_{DVSH}	t_{DW}	10	–	12	–	14	–	ns	
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	9	–	10	–	12	ns	2, 3
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	0	–	0	–	ns	
Write Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	18	ns	3
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSHWL}/t_{BSHSL} t_{BCHWL}/t_{BCHSL}	t_{BSS} t_{BCS}	−1	–	−1	–	−1	–	ns	
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	10	–	10	–	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	22	–	25	–	30	ns	3
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	ns	2, 3

NOTES:
1. A standard write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ and $\overline{BCLR}$ high. The $\overline{R}$ pin is high continuously during a write cycle.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.
3. Both the match output and Q0-Q3 are shown as valid in the $\overline{W}$ controlled cycle below to convey their timing relative to $\overline{W}$. In reality, only one of either match or Q0-Q3 can be valid at one time, as determined by $\overline{BSET}$and $\overline{BCLR}$ inputs.

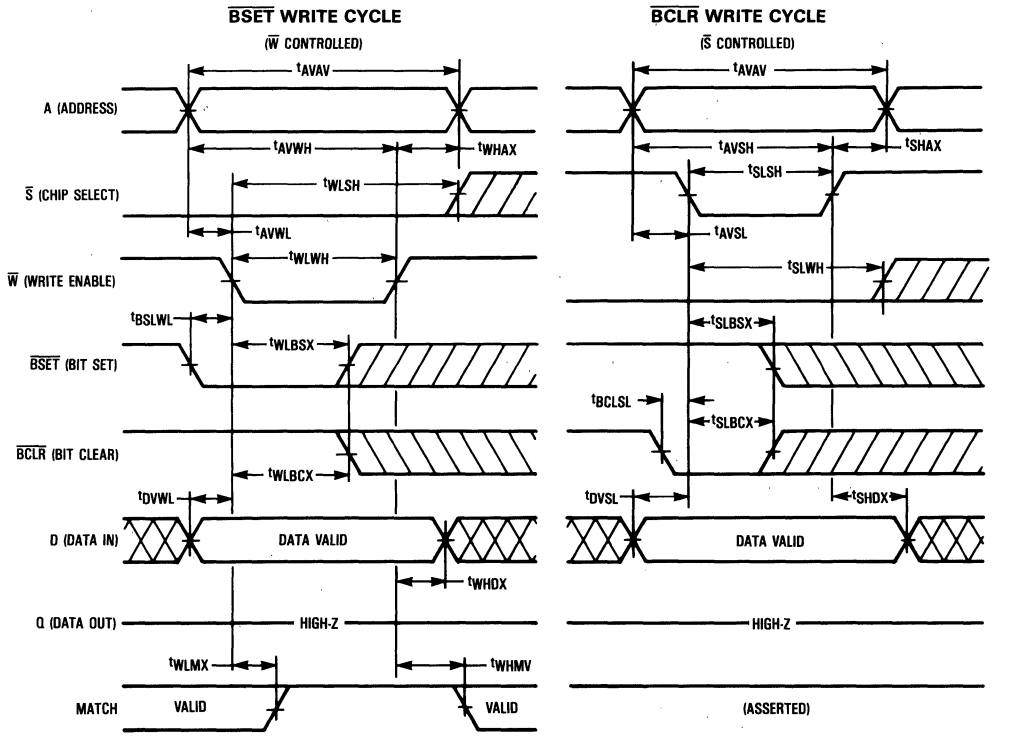
STANDARD WRITE CYCLE



$\overline{BSET}/\overline{BCLR}$ WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-22		MCM62351-25		MCM62351-30		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	18	—	20	—	25	—	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	18	—	20	—	25	—	ns	
Data Setup to Beginning of Write	t_{DVWL}/t_{DVSL}	t_{DS}	−1	—	−1	—	−1	—	ns	2
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	—	0	—	0	—	ns	
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	—	0	—	0	—	ns	
$\overline{W}$ Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	0	15	0	18	ns	
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSLWL}/t_{BSLSL} t_{BCLWL}/t_{BCLSL}	t_{BSS} t_{BCS}	−1	—	−1	—	−1	—	ns	2
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	—	10	—	10	—	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	—	22	—	25	—	30	ns	

NOTES:
1. A $\overline{BSET}/\overline{BCLR}$ write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ or $\overline{BCLR}$ low. The $\overline{R}$ pin is high continuously during a write cycle. $\overline{BSET}$ and $\overline{BCLR}$ write cycles can be $\overline{W}$ controlled or $\overline{S}$ controlled. Only two of four possible cycles are shown here for brevity.
2. Data output buffer must be in high-Z prior to start of either $\overline{BSET}$ or $\overline{BCLR}$ write cycles. Note that for $\overline{W}$ controlled cycles, the user must avoid excessive setup time of $\overline{BSET}/\overline{BCLR}$ to avoid bus contention. Data must be set up for t_{DVWL}/t_{DVSL} time to ensure the data integrity of non-modified bits during $\overline{BSET}/\overline{BCLR}$ write cycles. In the event that invalid data is presented for non-modified bits during the $\overline{BSET}/\overline{BCLR}$ write, note that it is not possible to recover the original data state by simply presenting valid data before the end of write.

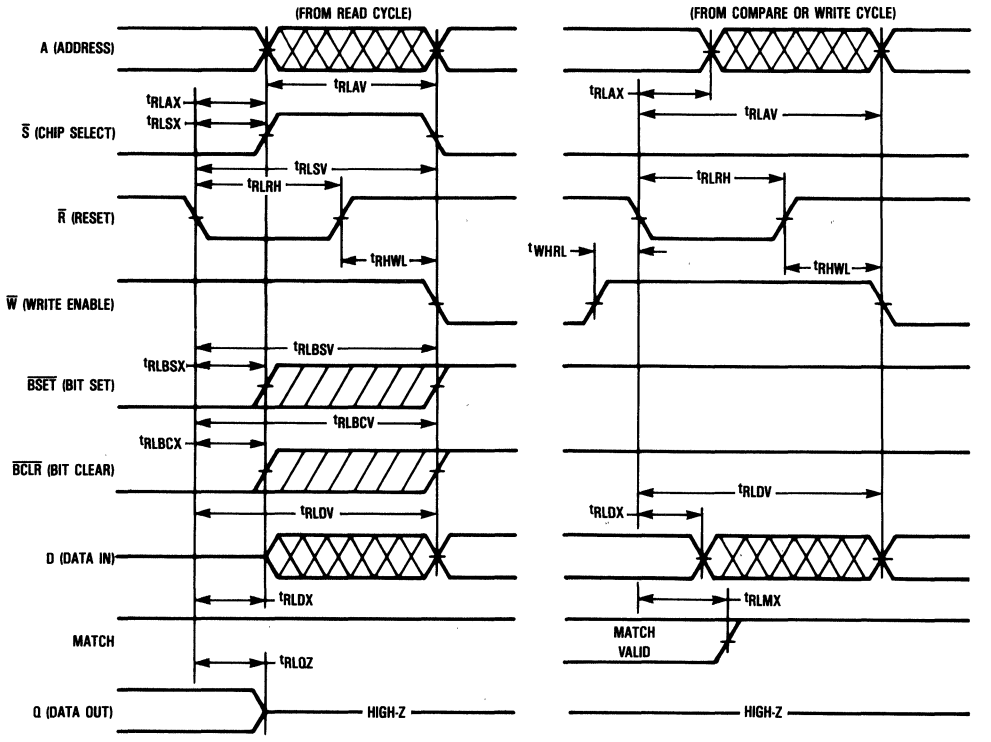


CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM62351-22		MCM62351-25		MCM62351-30		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
$\overline{R}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{RLAV}	t_{CR}	–	70	–	70	–	70	ns	
	$\overline{S}$	t_{RLSV}	t_{CR}								
	$\overline{BSET}$	t_{RLBSV}	t_{CR}								
	$\overline{BCLR}$	t_{RLBCV}	t_{CR}								
	D	t_{RLDV}	t_{CR}								
$\overline{R}$ Pulse Width		t_{RLRH}	t_{CLP}	25	–	30	–	35	–	ns	
Read Setup to $\overline{R}$ Low		t_{WHRL}	t_{RS}	5	–	5	–	5	–	ns	2
Write Hold from $\overline{R}$ High		t_{RHWL}	t_{WH}	0	–	0	–	0	–	ns	2
$\overline{R}$ Low to Inputs Don't Care	A	t_{RLAX}	t_{CX}	0	–	0	–	0	–	ns	3
	$\overline{S}$	t_{RLSX}	t_{CX}								
	$\overline{BSET}$	t_{RLBSX}	t_{CX}								
	$\overline{BCLR}$	t_{RLBCX}	t_{CX}								
	D	t_{RLDX}	t_{CX}								
$\overline{R}$ Low to Match Assert		t_{RLMX}	t_{MH}	0	15	0	18	0	20	ns	
$\overline{R}$ Low to Output High-Z		t_{RLQZ}	t_{CZ}	–	15	–	18	–	20	ns	4

NOTES:
1. The address, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{R}$. The t_{WHRL} and t_{RHWL} parameters must be satisfied to prevent an undesired configuration cycle.
3. "Inputs" for this parameter refers to all inputs except $\overline{W}$.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE

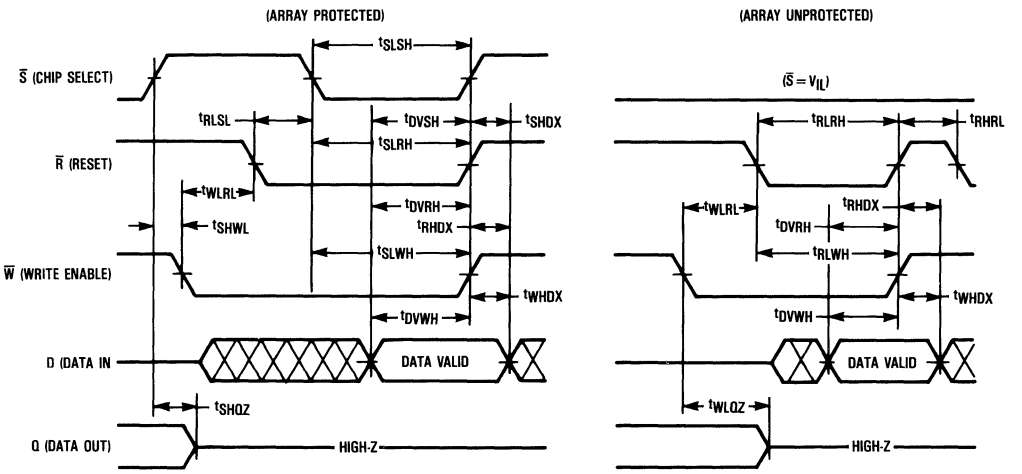


CONFIGURATION CYCLE (See Notes 1 and 2)

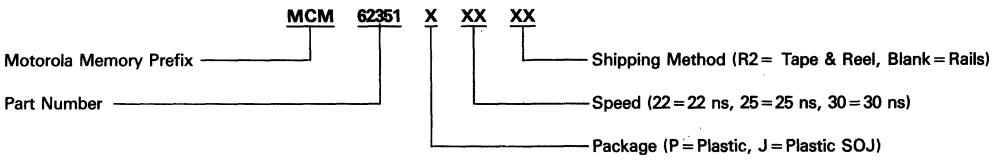
Characteristic		Symbol		MCM62351-22		MCM62351-25		MCM62351-30		Unit	Notes
		Standard	Alternate	Min	Max	Min	Max	Min	Max		
Configuration Control Pulse Width	$\overline{S}$ $\overline{R}$	t_{SLSH} t_{RLRH}	t_{SP} t_{SP}	20	—	25	—	30	—	ns	3
Data Setup to End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{DVSH} t_{DVRH} t_{DVWH}	t_{DS} t_{DS} t_{DS}	10	—	12	—	14	—	ns	
Data Hold from End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{SHDX} t_{RHDX} t_{WHDX}	t_{DH} t_{DH} t_{DH}	0	—	0	—	0	—	ns	
$\overline{R}$ High Pulse Width		t_{RHRL}	t_{CP}	5	—	5	—	5	—	ns	
Write Setup to $\overline{R}$ Low		t_{WLRL}	t_{WS}	5	—	5	—	5	—	ns	
$\overline{S}$ Setup to End of Configuration		t_{SLWH} t_{SLRH}	t_{SWS} t_{SCS}	20	—	25	—	30	—	ns	4
$\overline{R}$ Setup to End of Configuration		t_{RLWH}	t_{SR}	20	—	25	—	30	—	ns	
$\overline{R}$ Setup to $\overline{S}$ Low		t_{RLSL}	t_{CSS}	5	—	5	—	5	—	ns	3
$\overline{S}$ Setup to Beginning of Write		t_{SHWL}	t_{WSS}	0	—	0	—	0	—	ns	
$\overline{S}$ High to Output High-Z		t_{SHQZ}	t_{HZ}	—	9	—	10	—	12	ns	5
$\overline{W}$ Low to Output High-Z		t_{WLQZ}	t_{HZ}	—	9	—	10	—	12	ns	5

NOTES:
1. A configuration cycle is performed during the overlap of $\overline{W}$ low, $\overline{R}$ low, and $\overline{S}$ low. Address, DQ1, DQ2, DQ3, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during configuration cycles.
2. To ensure proper configuration of the device during power up, chip select must be equal to or greater than V_{IH}.
3. A valid configuration can be performed with $\overline{S}$ asserted prior to $\overline{R}$ and $\overline{W}$ low transitions. Be aware, however, that array data may be altered under this condition.
4. Note that terminating the cycle with $\overline{R}$ while leaving $\overline{W}$ and $\overline{S}$ asserted may cause array data to be altered.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CONFIGURATION CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM62351P22	MCM62351P25	MCM62351P30
	MCM62351J22	MCM62351J25	MCM62351J30
	MCM62351J22R2	MCM62351J25R2	MCM62351J30R2

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MCM62351-20

Product Preview

4K x 4 Bit Cache Address Tag Comparator

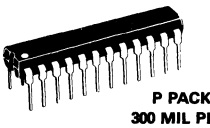
with System Status Bit Functions

The MCM62351 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 4K x 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required.

The device has a reset ($\overline{R}$) pin for flash clear of the RAM, which is useful for system initialization. Individual bits within a tag can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

The MCM62351 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status applications). The configuration of the comparator is accomplished by performing a write cycle with the $\overline{R}$ pin held low. The match output is open drain, allowing efficient combination of multiple match outputs using a wired-OR connection.

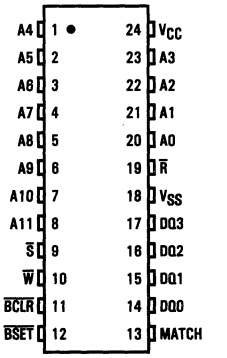
- Single 5 V ±10% Power Supply
- Fast Address to Match Time; 20 ns max
- Fast Data to Match Time; 10 ns max
- Fast Read of Tag RAM Contents; 20 ns max
- Flash Clear of the Tag RAM; 70 ns max
- Open Drain Match Output
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes: XNOR Mode for Address Tag Comparison
  AOI Mode for System Valid Bit Comparison



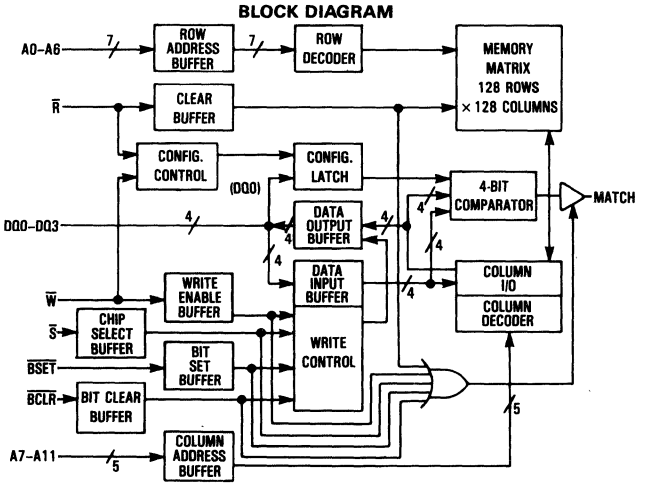
P PACKAGE
300 MIL PLASTIC
CASE 724

J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

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SIGNAL DESCRIPTIONS

A0-A11—ADDRESS INPUTS

The address lines are used for indexing into the tag RAM portion of the chip.

DQ0-DQ3—DATA INPUT/OUTPUT

The data lines are used as input for compare, write, and configuration cycles, and as output for read cycles.

$\overline{BSET}$—BIT SET CONTROL INPUT

This control signal is used for ORing data into the tag RAM during $\overline{BSET}$ write cycles. Independent bits within the tag can be set using the appropriate mask, as indicated in the bit set truth table. The $\overline{BSET}$ input can also be used to initiate a read cycle.

$\overline{BCLR}$—BIT CLEAR CONTROL INPUT

This control signal is used for ANDing the complement of data into the tag RAM during $\overline{BCLR}$ write cycles. Independent bits within the tag can be cleared using the appropriate mask, as indicated in the bit clear truth table. The $\overline{BCLR}$ input can also be used to initiate a read cycle (note that at least one of the $\overline{BSET}$/$\overline{BCLR}$ signals must be asserted to trigger a read cycle).

$\overline{R}$—RESET (FLASH CLEAR) INPUT

The reset control signal is used to initiate a clear cycle or a configuration cycle.

$\overline{S}$—CHIP SELECT

This control signal is used to chip select the device.

$\overline{W}$—WRITE ENABLE

The write enable signal is used to initiate write cycles.

MATCH—MATCH (HIT) OUTPUT

This output signal is used to indicate a match of DQ0-DQ3 inputs with the contents of the tag RAM addressed by A0—A11.

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FUNCTIONAL TRUTH TABLE

$\overline{S}$	$\overline{W}$	$\overline{BCLR}$	$\overline{BSET}$	$\overline{R}$	DQ0-DQ3	Match	Cycle
L	H	H	H	H	Compare D_{in}	Valid	Compare
L	H	L	X	H	Read D_{out}	Assert	Read
L	H	X	L	H	Read D_{out}	Assert	Read
L	L	H	H	H	Write D_{in}	Assert	Write
L	L	L	H	H	Bit Clear Mask	Assert	$\overline{BCLR}$ Write
L	L	H	L	H	Bit Set Mask	Assert	$\overline{BSET}$ Write
X	H	X	X	L	High-Z	Assert	Clear (Reset)
L	L	X	X	L	Config D_{in}*	Assert	Configuration
H	X	X	X	H	High-Z	Assert	Deselect

*DQ1, DQ2, and DQ3 are don't cares during a configuration cycle.

COMPARATOR TRUTH TABLE

Type	DQ0	DQ1	DQ2	DQ3	RAMQ0	RAMQ1	RAMQ2	RAMQ3	Match
XNOR	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
XNOR	$\overline{Q0}$	Q1	Q2	Q3	Q0	Q1	Q2	Q3	0
AOI	Q0	Q1	Q2	Q3	Q0	Q1	Q2	Q3	1
AOI	L	Q1	Q2	Q3	X	Q1	Q2	Q3	1
AOI	H	Q1	Q2	Q3	L	Q1	Q2	Q3	0

L = Low
H = High
0 = False
1 = True
X = Don't Care

BIT CLEAR TRUTH TABLE (See Note)

Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	0	Bit Cleared
1	1	0	to "Zero"

BIT SET TRUTH TABLE (See Note)

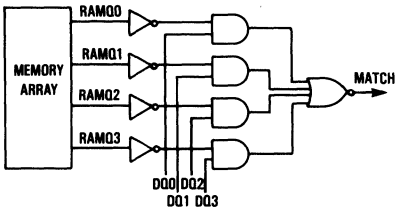
Data In	Initial Stored Data	Final Stored Data	
0	0	0	Bit
0	1	1	Unchanged
1	0	1	Bit Set
1	1	1	to "One"

NOTE: These tables reflect the behavior of single bit positions. The four bits in the tag can all be set or cleared in tandem, or bits within the tag can be independently set or cleared with the appropriate mask.

CONFIGURATION TABLE

DQ0	Comparator Type
L	XNOR
H	AOI

AOI COMPARATOR LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC} +0.5	V
Output Current Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

The power supply (V_{CC}) should be stable for at least 100 μs before operating the device. During this interval, the part will internally configure itself for XNOR compares. In addition, the memory array of RAM bits will be cleared.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} min = −0.5 V dc; V_{IL} min = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
Match Output Leakage Current (Match Asserted)	$I_{lkg(M)}$	–	±2.0	μA
AC Supply Current ($\overline{S}$ = V_{IL}, I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	–	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 23.0 mA)	V_{OL}	–	0.4	V
Output High Voltage (I/O Pins: I_{OH} = 4.0 mA)	V_{OH}	2.4	–	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	5	pF
I/O Capacitance	C_{out}	5	7	pF
Match Output Capacitance	C_{match}	6	7	pF

AC TEST LOADS

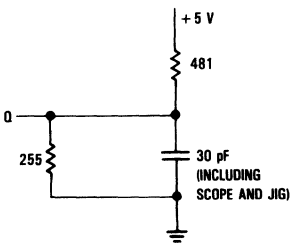


Figure 1a

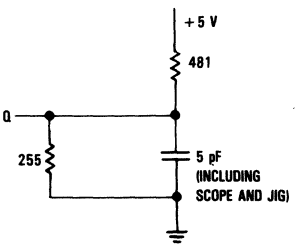


Figure 1b

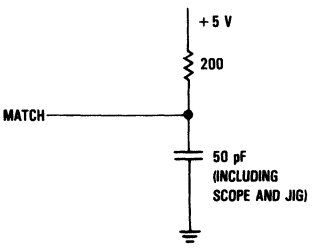


Figure 1c

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

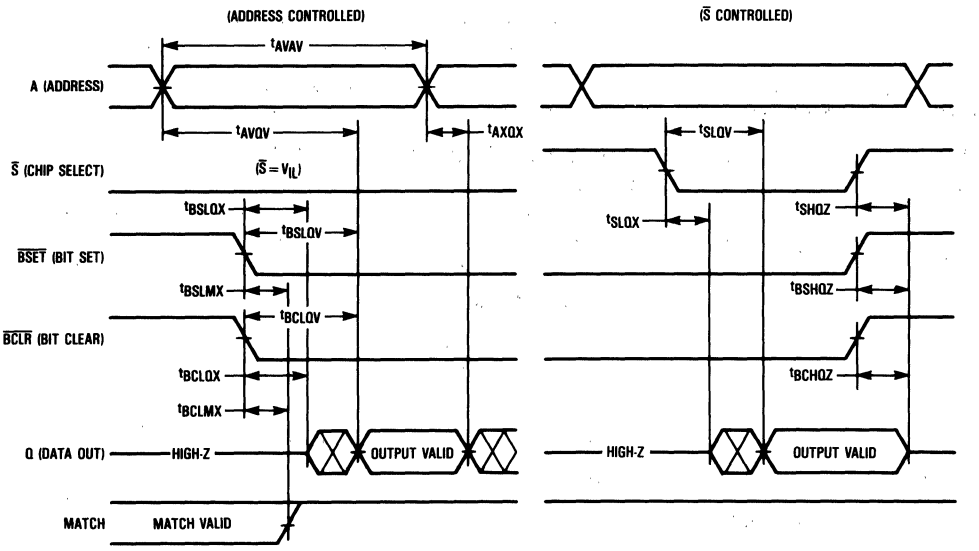
Input Timing Measurement Reference Level . . . . . 1.5 V	Output Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V	Output Load (I/O Pins) . . . . . See Figure 1a
Input Rise/Fall Time . . . . . 5 ns	Output Load (Match Output) . . . . . See Figure 1c

READ CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		Unit	Notes
	Standard	Alternate	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	20	ns	
Select Access Time	t_{SLQV}	t_{ACS}	—	11	ns	
$\overline{BCLR}$ Access Time	t_{BCLQV}	t_{ABC}	—	20	ns	2
$\overline{BSET}$ Access Time	t_{BSLQV}	t_{ABS}	—	20	ns	2
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	ns	
Select Low to Output Active	t_{SLQX}	t_{CSL}	5	—	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Output Active	t_{BSLQX}/t_{BCLQX}	t_{LZ}	7	—	ns	3
$\overline{S}$ High to Output High-Z	t_{SHQZ}	t_{CSZ}	—	8	ns	3
$\overline{BSET}$/$\overline{BCLR}$ High to Output High-Z	t_{BSHQZ}/t_{BCHQZ}	t_{HZ}	—	8	ns	3
$\overline{BSET}$/$\overline{BCLR}$ Low to Match Assert	t_{BSLMX}/t_{BCLMX}	t_{CH}	0	15	ns	

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during read cycles. One of either $\overline{BSET}$ or $\overline{BCLR}$ pins must be asserted low to activate the outputs. The match output becomes asserted when either the $\overline{BSET}$ or $\overline{BCLR}$ pin transitions low.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

READ CYCLE



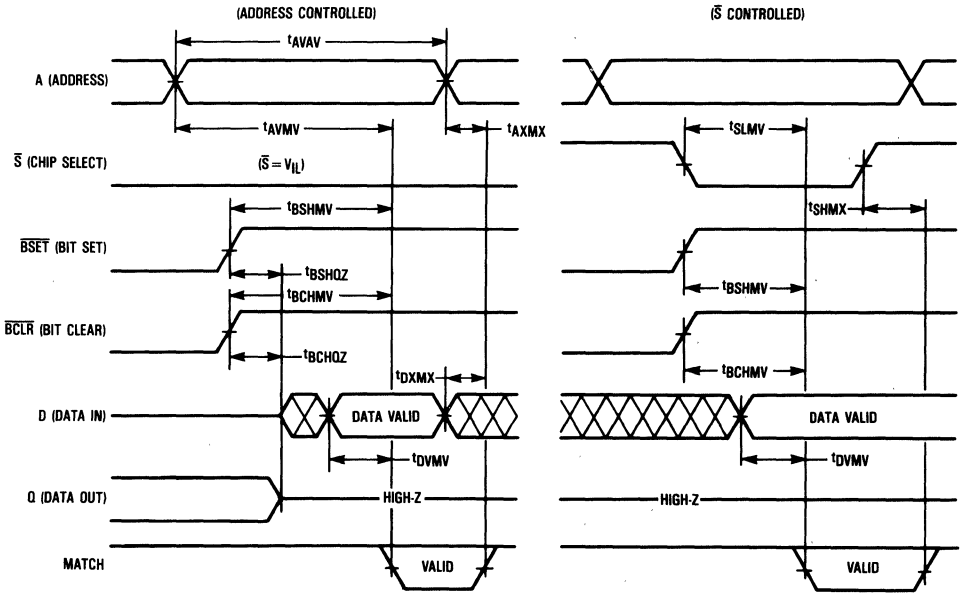
COMPARE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		Unit	Notes
	Standard	Alternate	Min	Max		
Compare Cycle Time	t_{AVAV}	t_C	20	–	ns	
Address Valid to Match Valid	t_{AVMV}	t_{ACA}	–	20	ns	
$\overline{BCLR}$ High to Match Valid	t_{BCHMV}	t_{BCCA}	–	15	ns	2
$\overline{BSET}$ High to Match Valid	t_{BSHMV}	t_{BSCA}	–	15	ns	2
Data Valid to Match Valid	t_{DVMV}	t_{DCA}	–	10	ns	
$\overline{S}$ Low to Match Valid	t_{SLMV}	t_{CSCA}	–	12	ns	
Match Hold from Address Change	t_{AXMX}	t_{ACH}	5	–	ns	
Match Hold from Data Change	t_{DXMX}	t_{DCH}	3	–	ns	
$\overline{S}$ High to Match Assert	t_{SHMX}	t_{CH}	0	10	ns	
$\overline{BCLR}$ High to Output High-Z	t_{BCHQZ}	t_{BCZ}	–	8	ns	3
$\overline{BSET}$ High to Output High-Z	t_{BSHQZ}	t_{BSZ}	–	8	ns	3

NOTES:
1. $\overline{R} = V_{IH}$, $\overline{W} = V_{IH}$ continuously during compare cycles.
2. For brevity in signal names, BC is used to represent $\overline{BCLR}$ transitions, while BS is used to represent $\overline{BSET}$ transitions.
3. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

5

COMPARE CYCLE

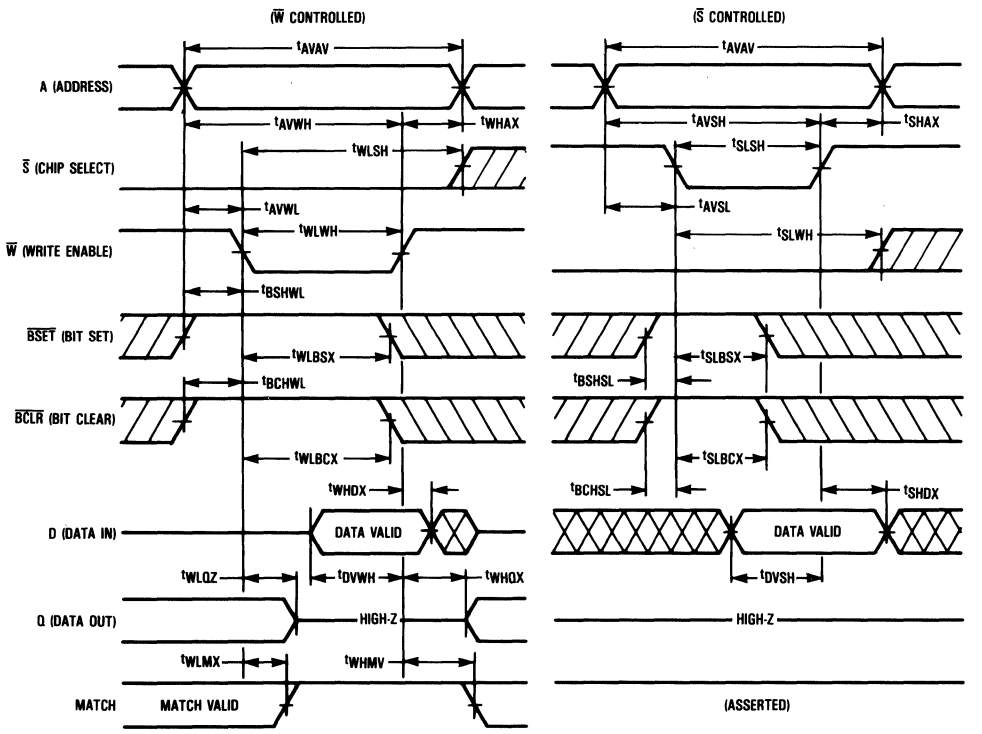


STANDARD WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	16	–	ns	
Data Valid to End of Write	t_{DVWH}/t_{DVSH}	t_{DW}	10	–	ns	
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	8	ns	2, 3
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	ns	
Write Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	ns	3
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSHWL}/t_{BSHSL} t_{BCHWL}/t_{BCHSL}	t_{BSS} t_{BCS}	−1	–	ns	
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	20	ns	3
Write High to Output Active	t_{WHQX}	t_{OW}	3	–	ns	2, 3

NOTES:
1. A standard write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ and $\overline{BCLR}$ high. The $\overline{R}$ pin is high continuously during a write cycle.
2. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.
3. Both the match output and Q0–Q3 are shown as valid in the $\overline{W}$ controlled cycle below to convey their timing relative to $\overline{W}$. In reality, only one of either match or Q0–Q3 can be valid at one time, as determined by $\overline{BSET}$ and $\overline{BCLR}$ inputs.

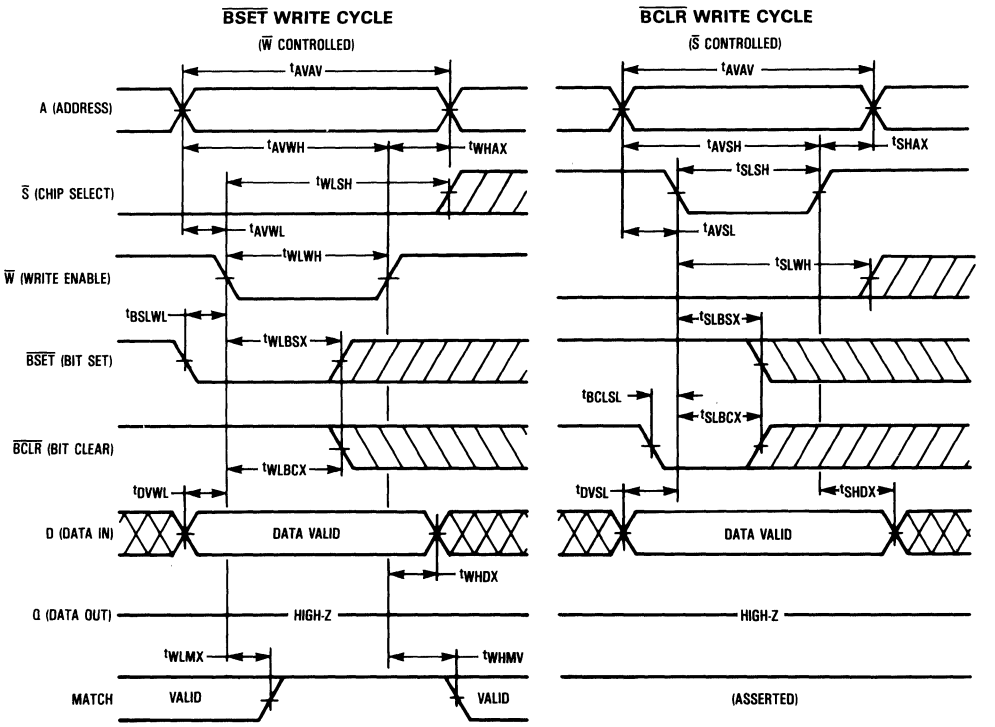
STANDARD WRITE CYCLE



$\overline{BSET}/\overline{BCLR}$ WRITE CYCLE (See Note 1)

Characteristic	Symbol		MCM62351-20		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	–	ns	
Write Pulse Width	t_{WLWH}/t_{SLSH} t_{WLSH}/t_{SLWH}	t_{WP} t_{WP}	14	–	ns	
Address Setup to Beginning of Write	t_{AVWL}/t_{AVSL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}/t_{AVSH}	t_{AW}	14	–	ns	
Data Setup to Beginning of Write	t_{DVWL}/t_{DVSL}	t_{DS}	0	–	ns	2
Data Hold from Write End	t_{WHDX}/t_{SHDX}	t_{DH}	0	–	ns	
Address Hold from Write End	t_{WHAX}/t_{SHAX}	t_{WR}	0	–	ns	
$\overline{W}$ Low to Match Assert	t_{WLMX}	t_{WCH}	0	15	ns	
$\overline{BSET}/\overline{BCLR}$ Setup to Beginning of Write	t_{BSLWL}/t_{BSLSL} t_{BCLWL}/t_{BCLSL}	t_{BSS} t_{BCS}	−1	–	ns	2
$\overline{BSET}/\overline{BCLR}$ Hold Time from Write Start	t_{WLBSX}/t_{SLBSX} t_{WLBCX}/t_{SLBCX}	t_{BSH} t_{BCH}	10	–	ns	
Write High to Match Valid	t_{WHMV}	t_{WCA}	–	20	ns	

NOTES:
1. A $\overline{BSET}/\overline{BCLR}$ write occurs during the overlap of $\overline{W}$ and $\overline{S}$ low and $\overline{BSET}$ or $\overline{BCLR}$ low. The $\overline{R}$ pin is high continuously during a write cycle. $\overline{BSET}$ and $\overline{BCLR}$ write cycles can be $\overline{W}$ controlled or $\overline{S}$ controlled. Only two of four possible cycles are shown here for brevity.
2. Data output buffer must be in high-Z prior to start of either $\overline{BSET}$ or $\overline{BCLR}$ write cycles. Note that for $\overline{W}$ controlled cycles, the user must avoid excessive setup time of $\overline{BSET}/\overline{BCLR}$ to avoid bus contention. Data must be set up for t_{DVWL}/t_{DVSL} time to ensure the data integrity of non-modified bits during $\overline{BSET}/\overline{BCLR}$ write cycles. In the event that invalid data is presented for non-modified bits during the $\overline{BSET}/\overline{BCLR}$ write, note that it is not possible to recover the original data state by simply presenting valid data before the end of write.



CLEAR CYCLE (See Note 1)

Characteristic		Symbol		MCM62351-20		Unit	Notes
		Standard	Alternate	Min	Max		
$\overline{R}$ Low to Inputs Recognized (Clear Cycle Time)	A	t_{RLAV}	t_{CR}	–	70	ns	
	$\overline{S}$	t_{RLSV}	t_{CR}				
	$\overline{BSET}$	t_{RLBSV}	t_{CR}				
	$\overline{BCLR}$	t_{RLBCV}	t_{CR}				
	D	t_{RLDV}	t_{CR}				
$\overline{R}$ Pulse Width		t_{RLRH}	t_{CLP}	20	–	ns	
Read Setup to $\overline{R}$ Low		t_{WHRL}	t_{RS}	5	–	ns	2
Write Hold from $\overline{R}$ High		t_{RHWL}	t_{WH}	0	–	ns	2
$\overline{R}$ Low to Inputs Don't Care	A	t_{RLAX}	t_{CX}	0	–	ns	3
	$\overline{S}$	t_{RLSX}	t_{CX}				
	$\overline{BSET}$	t_{RLBSX}	t_{CX}				
	$\overline{BCLR}$	t_{RLBCX}	t_{CX}				
	D	t_{RLDX}	t_{CX}				
$\overline{R}$ Low to Match Assert		t_{RLMX}	t_{MH}	0	15	ns	
$\overline{R}$ Low to Output High-Z		t_{RLQZ}	t_{CZ}	–	15	ns	4

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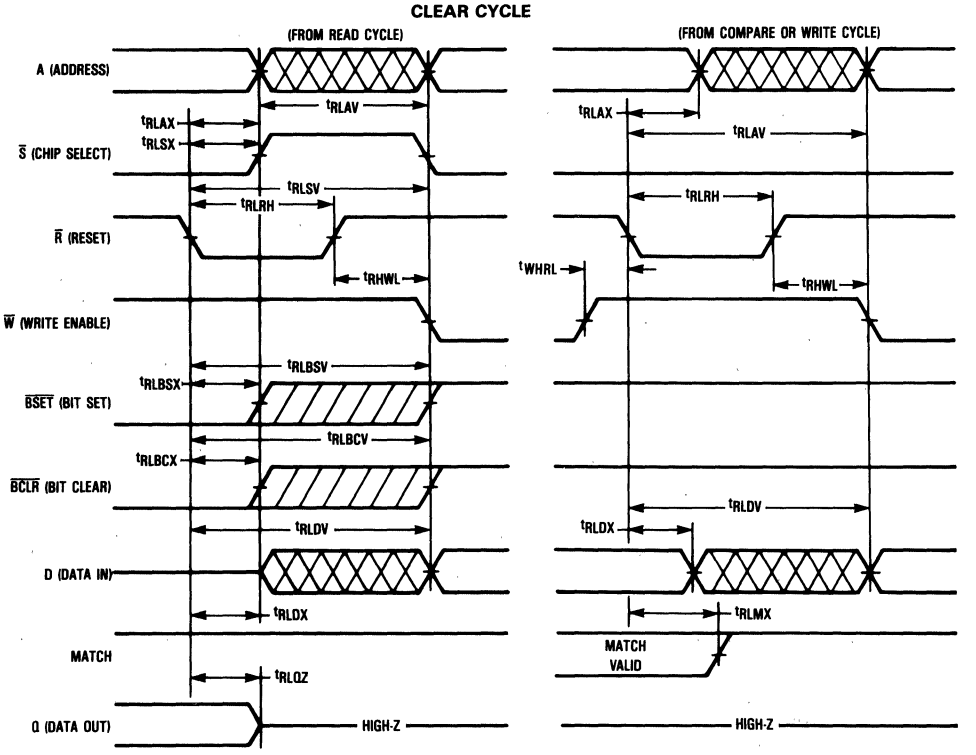
NOTES:
1. The address, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during a clear cycle.
2. The clear cycle is initiated at the falling edge of $\overline{R}$. The t_{WHRL} and t_{RHWL} parameters must be satisfied to prevent an undesired configuration cycle.
3. "Inputs" for this parameter refers to all inputs except $\overline{W}$.
4. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CLEAR CYCLE

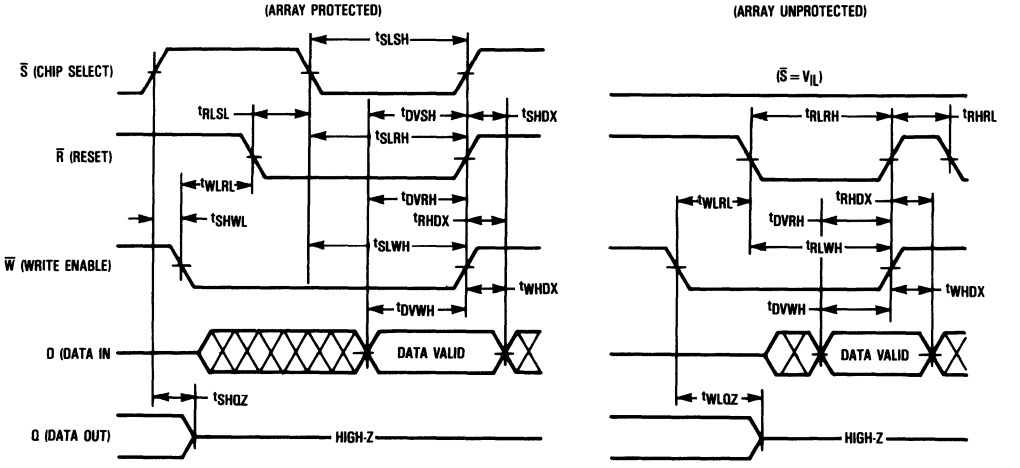


CONFIGURATION CYCLE (See Notes 1 and 2)

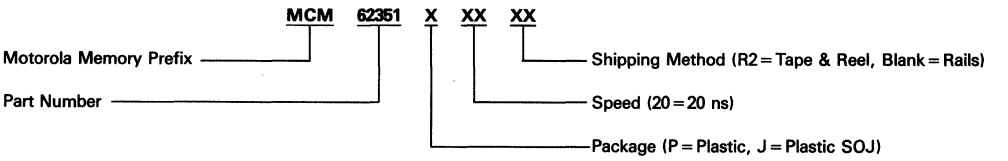
Characteristic		Symbol		MCM62351-20		Unit	Notes
		Standard	Alternate	Min	Max		
Configuration Control Pulse Width	$\overline{S}$ $\overline{R}$	t_{SLSH} t_{RLRH}	t_{SP} t_{SP}	20	–	ns	3
Data Setup to End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{DVSH} t_{DVRH} t_{DVWH}	t_{DS} t_{DS} t_{DS}	10	–	ns	
Data Hold from End of Configuration Cycle	$\overline{S}$ $\overline{R}$ $\overline{W}$	t_{SHDX} t_{RHDX} t_{WHDX}	t_{DH} t_{DH} t_{DH}	0	–	ns	
$\overline{R}$ High Pulse Width		t_{RHRL}	t_{CP}	5	–	ns	
Write Setup to $\overline{R}$ Low		t_{WLRL}	t_{WS}	5	–	ns	
$\overline{S}$ Setup to End of Configuration		t_{SLWH} t_{SLRH}	t_{SWS} t_{SCS}	20	–	ns	4
$\overline{R}$ Setup to End of Configuration		t_{RLWH}	t_{SR}	20	–	ns	
$\overline{R}$ Setup to $\overline{S}$ Low		t_{RLSL}	t_{CSS}	5	–	ns	3
$\overline{S}$ Setup to Beginning of Write		t_{SHWL}	t_{WSS}	0	–	ns	
$\overline{S}$ High to Output High-Z		t_{SHQZ}	t_{HZ}	–	9	ns	5
$\overline{W}$ Low to Output High-Z		t_{WLQZ}	t_{HZ}	–	9	ns	5

NOTES:
1. A configuration cycle is performed during the overlap of $\overline{W}$ low, $\overline{R}$ low, and $\overline{S}$ low. Address, DQ1, DQ2, DQ3, $\overline{BSET}$, and $\overline{BCLR}$ inputs are don't cares during configuration cycles.
2. To ensure proper configuration of the device during power up, chip select must be equal to or greater than V_{IH}.
3. A valid configuration can be performed with $\overline{S}$ asserted prior to $\overline{R}$ and $\overline{W}$ low transitions. Be aware, however, that array data may be altered under this condition.
4. Note that terminating the cycle with $\overline{R}$ while leaving $\overline{W}$ and $\overline{S}$ asserted may cause array data to be altered.
5. Transition is measured ±500 mV from steady state voltage with load of Figure 1b. This parameter is sampled and not 100% tested.

CONFIGURATION CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM62351P20
MCM62351J20
MCM62351J20R2

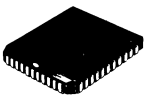
5

MCM62963

Product Preview

4K x 10 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62963 is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit. This allows reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D9), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

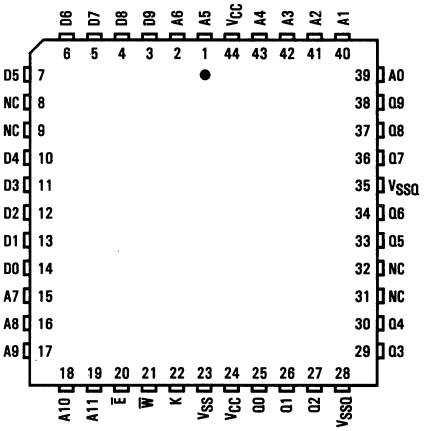
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62963 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

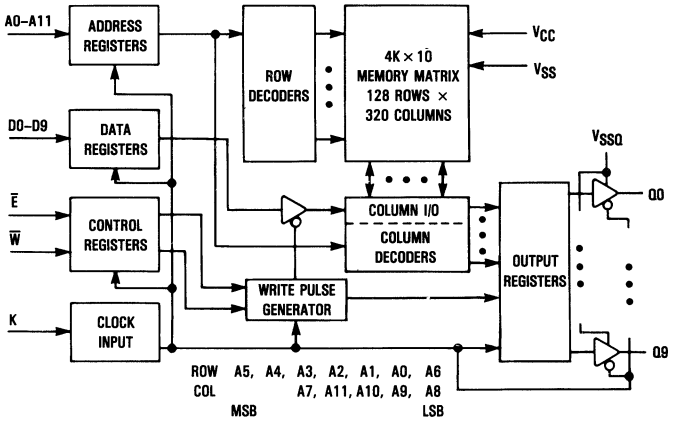
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/13 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q9	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62963-20: $t_{KHKH}=20$ ns		–	170	
MCM62963-25: $t_{KHKH}=25$ ns		–	170	
MCM62963-30: $t_{KHKH}=30$ ns		–	150	
Standby Current ($\overline{E}=V_{IH}$, $V_{IH}\geq3.0$ V, $V_{IL}\leq0.4$ V, $I_{out}=0$ mA, Cycle Time ≥ = t_{KHKH} min)	I_{SB}	–	30	mA
Output Low Voltage ($I_{OL}=12.7$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-1.8$ mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter		Symbol	MCM62963-20		MCM62963-25		MCM62963-30		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{KHKH}	20	–	25	–	30	–	ns	2
Clock Access Time		t_{KHQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High		t_{KHQX}	3	–	3	–	3	–	ns	4
Clock High to Q High Z ($\overline{E}=V_{IH}$)		t_{KHQZ}	–	10	–	10	–	13	ns	4
Clock Low Pulse Width		t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width		t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for:	$\overline{E}$	t_{EVKH}	5	–	5	–	5	–	ns	5
	A	t_{AVKH}								
	$\overline{W}$	t_{WHKH}								
Hold Times for:	$\overline{E}$	t_{KHEX}	3	–	3	–	3	–	ns	5
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

5

AC TEST LOADS

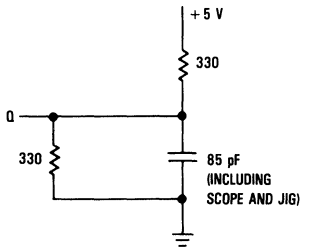


Figure 1A

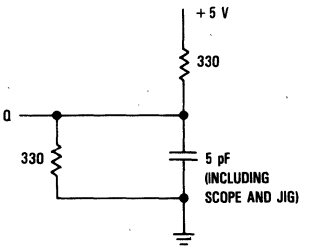
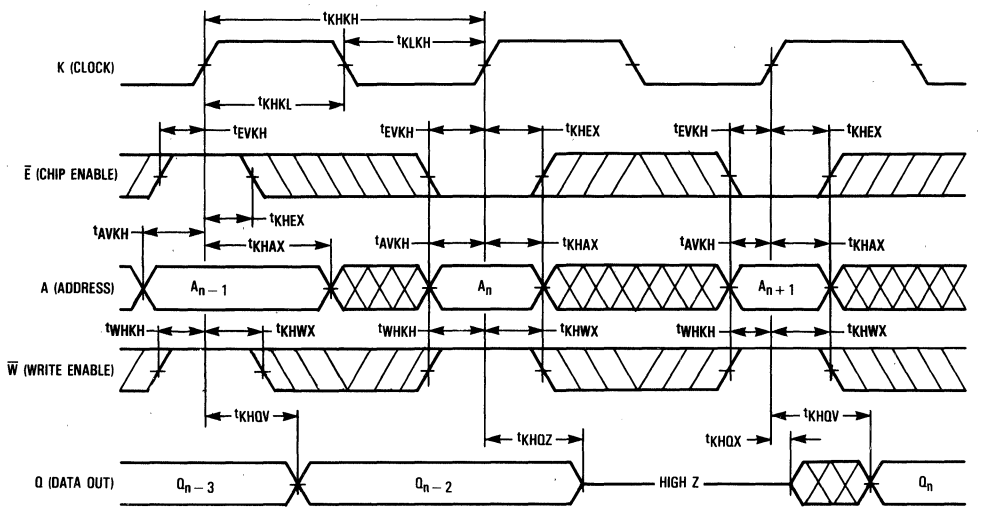
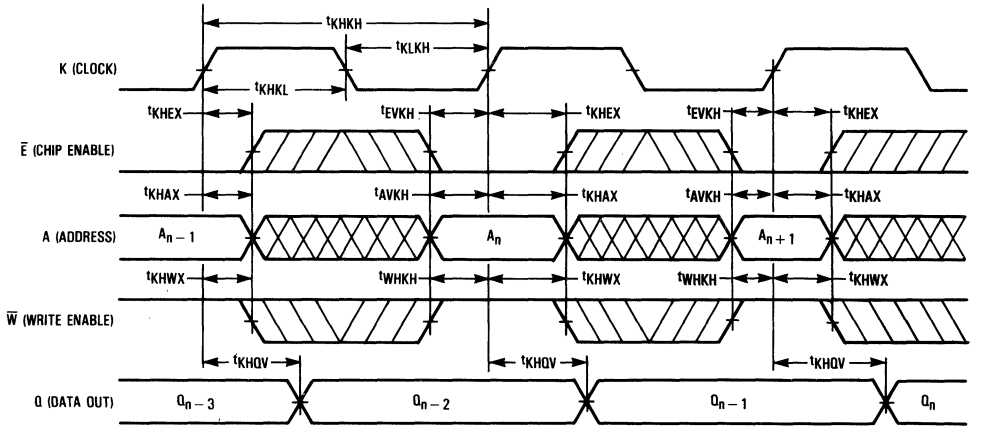


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM62963-20		MCM62963-25		MCM62963-30		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	–	25	–	30	–	ns	2
Clock High to Q High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	–	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	–	5	–	5	–	ns	4
	A	t_{AVKH}								
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	$\overline{E}$	t_{KHEX}	3	–	3	–	3	–	ns	4
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

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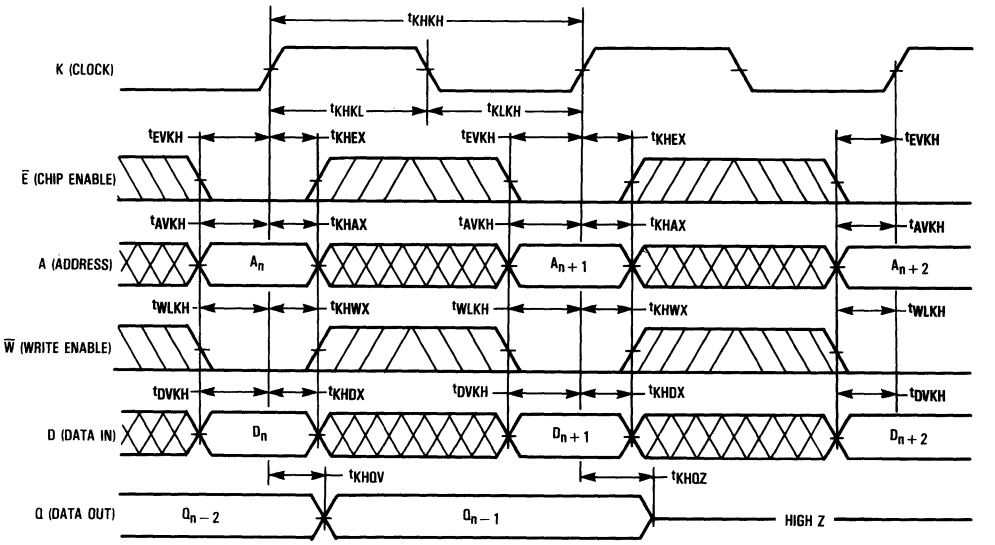
WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62963 X XX

- MCM — Motorola Memory Prefix
- 62963 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

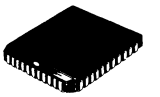
Full Part Numbers — MCM62963FN20 MCM62963FN25 MCM62963FN30

MCM62964

Product Preview

4K x 10 Bit Synchronous Static RAM

with Output Registers and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62964 is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D9), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

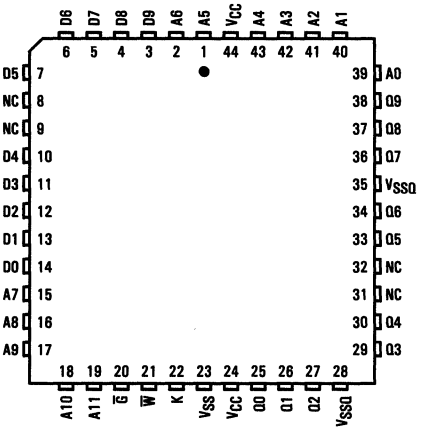
The MCM62964 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

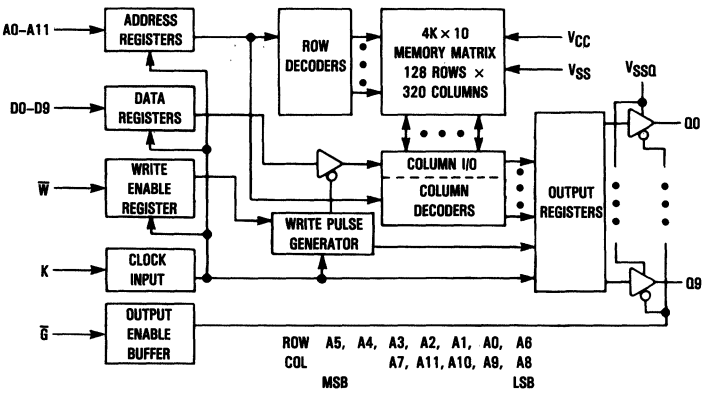
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/13 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q9	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G}=V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62964-20: $t_{KHKH}=20$ ns		–	170	
MCM62964-25: $t_{KHKH}=25$ ns		–	170	
MCM62964-30: $t_{KHKH}=30$ ns		–	150	
Output Low Voltage ($I_{OL}=12.7$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-1.8$ mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62964-20		MCM62964-25		MCM62964-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	1, 3
Write Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	2, 3
Clock High Access Time	t_{KHQV}	–	10	–	10	–	13	ns	3, 4
$\overline{G}$ Low to Output Valid	t_{GLQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	–	0	–	0	–	ns	
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	1, 2, 5
D	t_{DVKH}								
$\overline{W}$	t_{WVKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	1, 2, 5
D	t_{KHDX}								
$\overline{W}$	t_{KHWX}								
Clock High to Output High Z ($\overline{W}$ = V_{IL})	t_{KHQZ}	0	10	0	10	0	13	ns	3, 6
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	10	0	13	ns	3, 6, 7

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Valid data from K high will be the data stored at the address of the last valid read cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
7. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

AC TEST LOADS

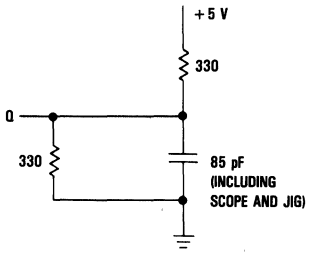


Figure 1A

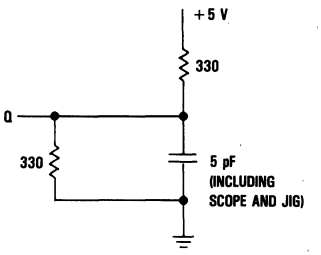
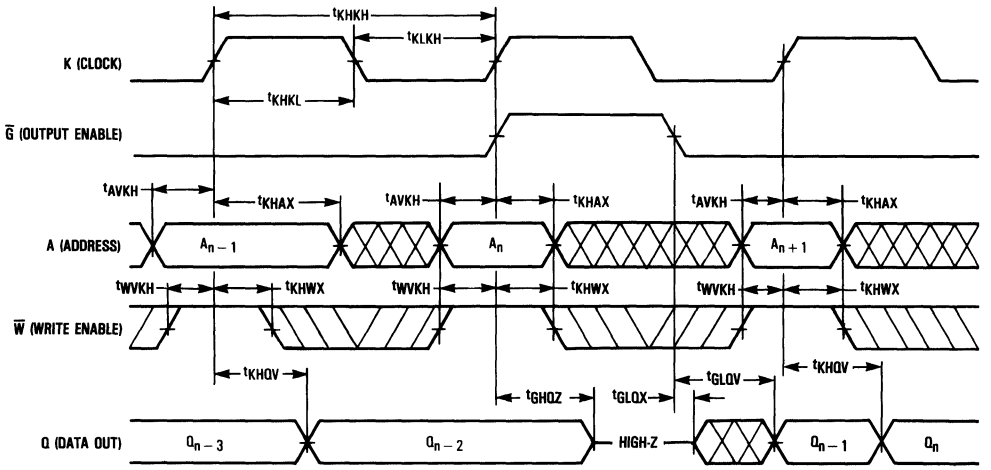
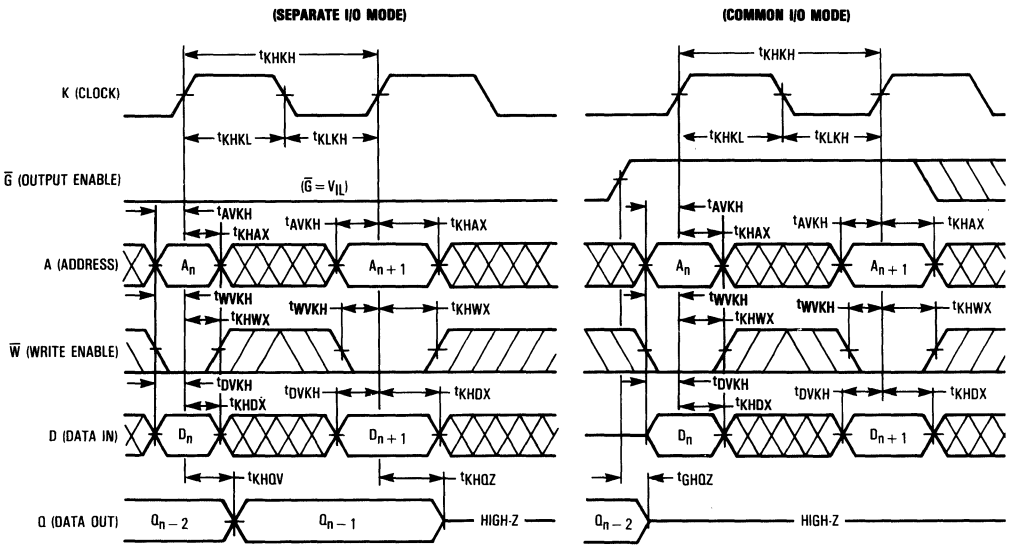


Figure 1B

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62964 X XX

- MCM — Motorola Memory Prefix
- 62964 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

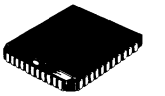
Full Part Numbers — MCM62964FN20 MCM62964FN25 MCM62964FN30

MCM62965

Product Preview

4K x 10 Bit Synchronous Static RAM

with Transparent Outputs and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62965 is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D9), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

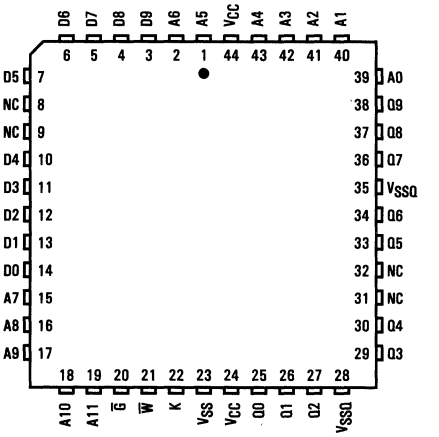
The MCM62965 provides transparent output operation when clock (K) is low for access of RAM data within the same cycle (output data is latched when clock (K) is high).

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

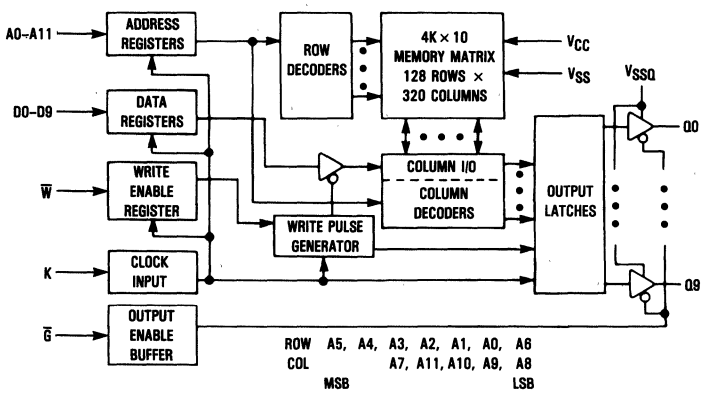
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 25/30/35 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q9	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62965-25: t_{KHKH} = 25 ns		–	170	
MCM62965-30: t_{KHKH} = 30 ns		–	170	
MCM62965-35: t_{KHKH} = 35 ns		–	150	
Output Low Voltage (I_{OL} = 12.7 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −1.8 mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62965-25		MCM62965-30		MCM62965-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	–	30	–	35	–	ns	1, 3
Write Cycle Time	t_{KHKH}	25	–	30	–	35	–	ns	2, 3
Clock High Access Time	t_{KHQV}	–	25	–	30	–	35	ns	3, 4, 5
Clock Low to Output Valid	t_{KLQV}	–	10	–	13	–	15	ns	3, 4, 5
$\overline{G}$ Low to Output Valid	t_{GLQV}	–	10	–	13	–	15	ns	3
Output Active from Clock Low	t_{KLQX}	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	–	0	–	0	–	ns	
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	1, 2, 6
D	t_{DVKH}								
$\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	1, 2, 6
D	t_{KHDX}								
$\overline{W}$	t_{KHWX}								
Clock Low to Output High Z ($\overline{W}=V_{IL}$)	t_{KLQZ}	0	10	0	13	0	15	ns	5, 7
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	13	0	15	ns	3, 7, 8

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Access time is controlled by t_{KLQV} if the clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$; otherwise it is controlled by t_{KHQV}.
5. K must be low for the outputs to transition.
6. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
7. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
8. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

AC TEST LOADS

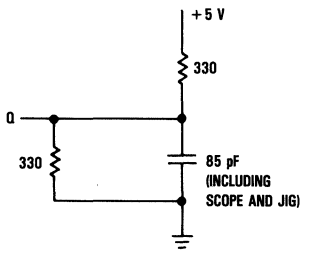


Figure 1A

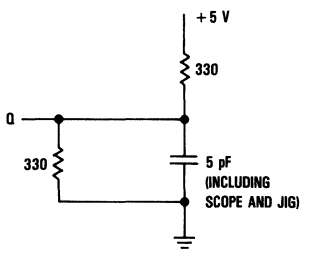
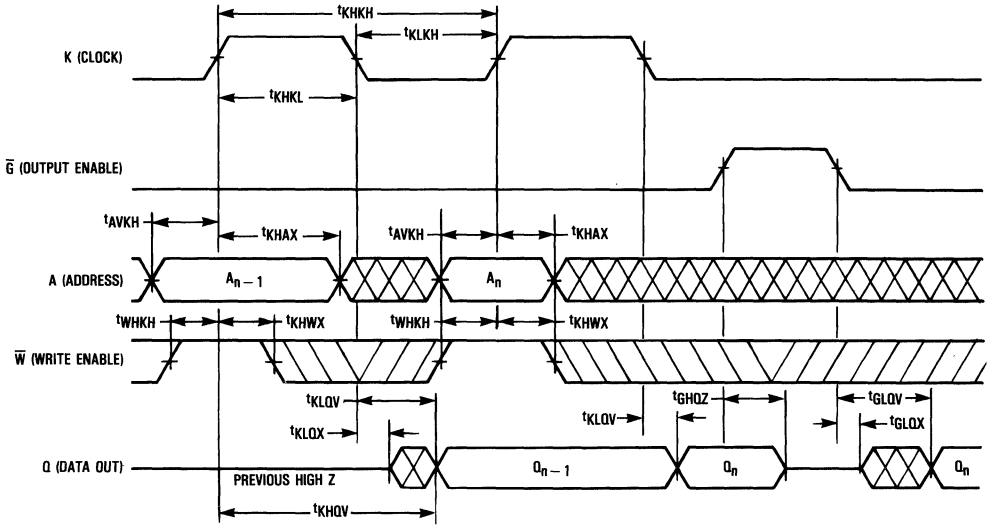
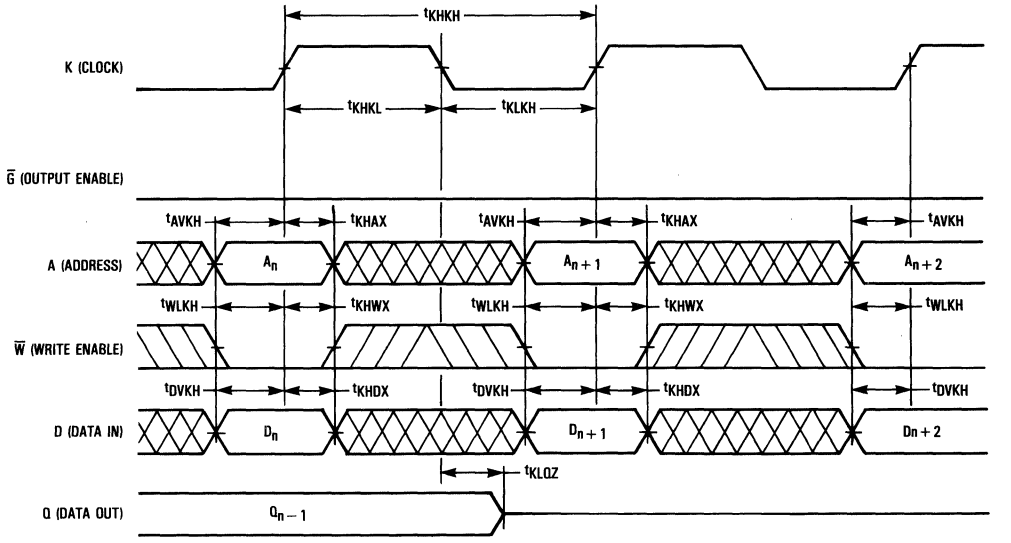


Figure 1B

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62965 X XX

- MCM — Motorola Memory Prefix
- 62965 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (25 = 25 ns, 30 = 30 ns, 35 = 35 ns)

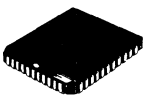
Full Part Numbers — MCM62965FN25 MCM62965FN30 MCM62965FN35

MCM62973

Product Preview

4K x 12 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62973 is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D11), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

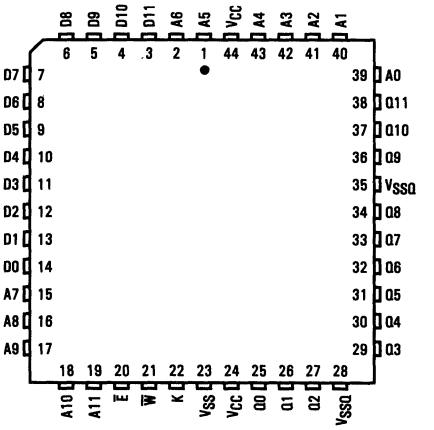
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62973 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

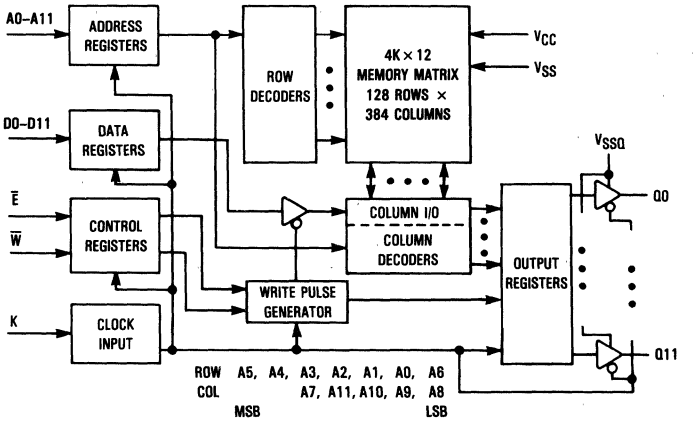
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/13 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q11	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A=25°C$)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of the clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be in High Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62973-20: $t_{KHKH}=20$ ns		—	170	
MCM62973-25: $t_{KHKH}=25$ ns		—	170	
MCM62973-30: $t_{KHKH}=30$ ns		—	150	
Standby Current ($\overline{E}=V_{IH}$, $V_{IH}\geq3.0$ V, $V_{IL}\leq0.4$ V, $I_{out}=0$ mA, Cycle Time ≥ = t_{KHKH} min)	I_{SB}	—	30	mA
Output Low Voltage ($I_{OL}=12.7$ mA)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH}=-1.8$ mA)	V_{OH}	2.8	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62973-20		MCM62973-25		MCM62973-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	3	–	3	–	3	–	ns	4
Clock High to Q High Z ($\overline{E}=V_{IH}$)	t_{KHQZ}	–	10	–	10	–	13	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	–	5	–	5	–	ns	5
A	t_{AVKH}								
$\overline{W}$	t_{WHKH}								
Hold Times for: $\overline{E}$	t_{KHEX}	3	–	3	–	3	–	ns	5
A	t_{KHAX}								
$\overline{W}$	t_{KHWX}								

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

AC TEST LOADS

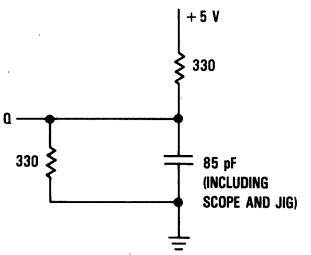


Figure 1A

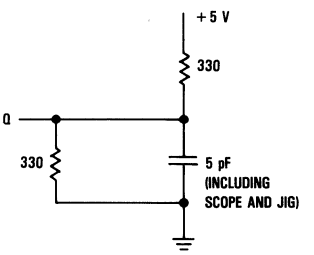
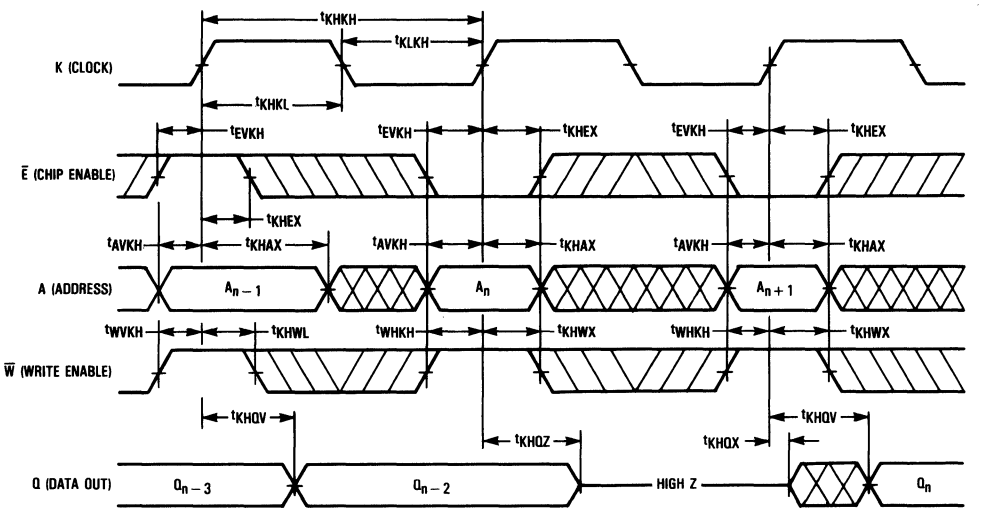
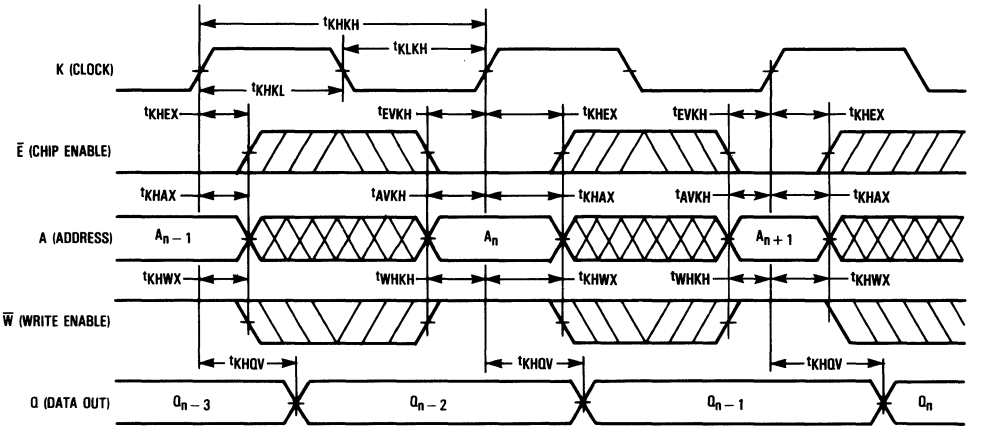


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM62973-20		MCM62973-25		MCM62973-30		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	20	–	25	–	30	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	–	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	–	5	–	5	–	ns	4
	A	t_{AVKH}								
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	$\overline{E}$	t_{KHEX}	3	–	3	–	3	–	ns	4
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

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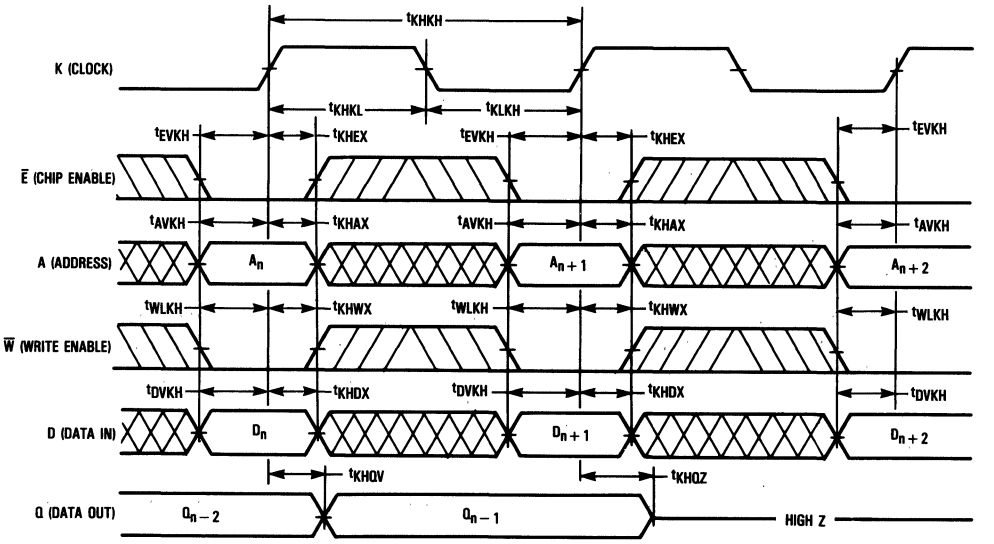
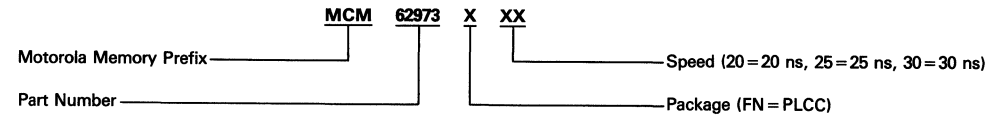
WRITE CYCLE





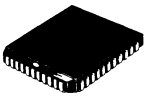
Full Part Numbers—MCM62973FN20 MCM62973FN25 MCM62973FN30

MCM62974

Product Preview

4K x 12 Bit Synchronous Static RAM

with Output Registers and Output Enable



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62974 is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D11), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

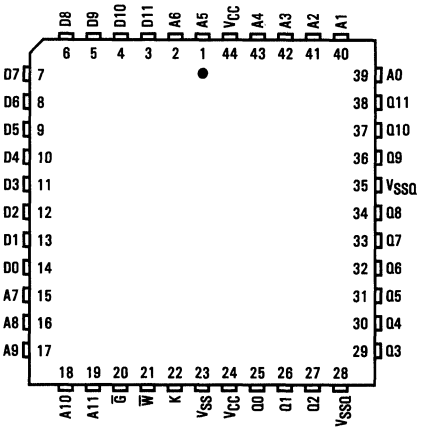
The MCM62974 provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

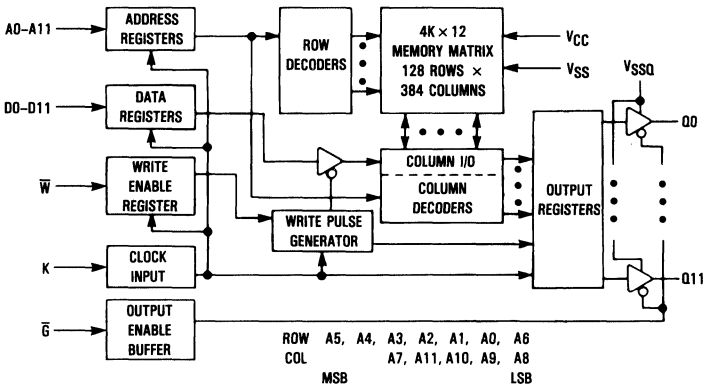
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 20/25/30 ns Max
- Fast Clock (K) Access Times: 10/10/13 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0–Q9	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{G} = V_{IH}$, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62974-20: t_{KHKH} = 20 ns		—	170	
MCM62974-25: t_{KHKH} = 25 ns		—	170	
MCM62974-30: t_{KHKH} = 30 ns		—	150	
Output Low Voltage (I_{OL} = 12.7 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −1.8 mA)	V_{OH}	2.8	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62974-20		MCM62974-25		MCM62974-30		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	1, 3
Write Cycle Time	t_{KHKH}	20	–	25	–	30	–	ns	2, 3
Clock High Access Time	t_{KHQV}	–	10	–	10	–	13	ns	3, 4
$\overline{G}$ Low to Output Valid	t_{GLQV}	–	10	–	10	–	13	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	–	0	–	0	–	ns	
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	1, 2, 5
D	t_{DVKH}								
$\overline{W}$	t_{WVKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	1, 2, 5
D	t_{KHDX}								
$\overline{W}$	t_{KHWX}								
Clock High to Output High Z ($\overline{W}$ = V_{IL})	t_{KHQZ}	0	10	0	10	0	13	ns	3, 6
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	10	0	13	ns	3, 6, 7

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Valid data from K high will be the data stored at the address of the last valid read cycle.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
7. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

AC TEST LOADS

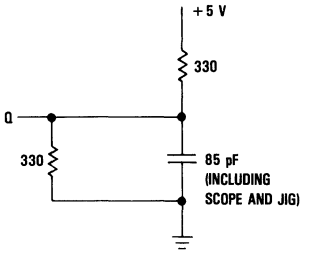


Figure 1A

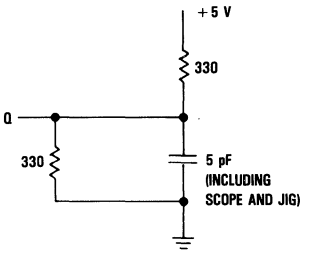
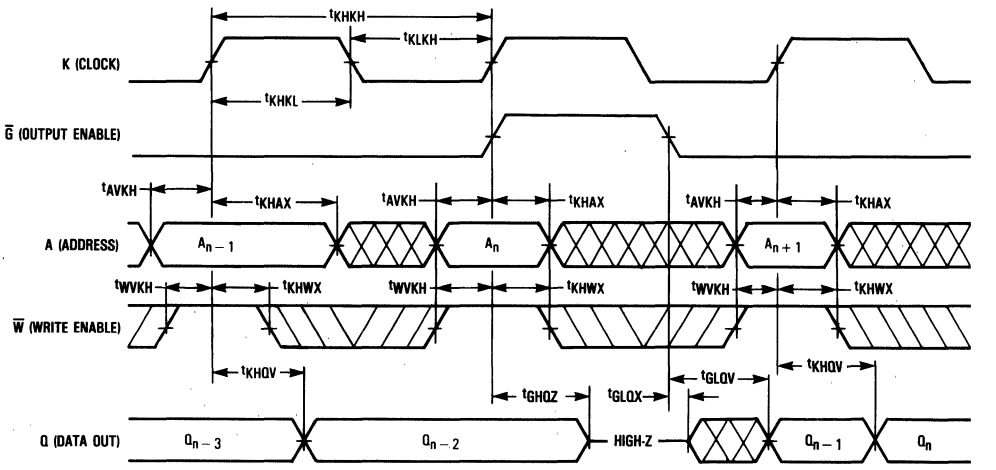


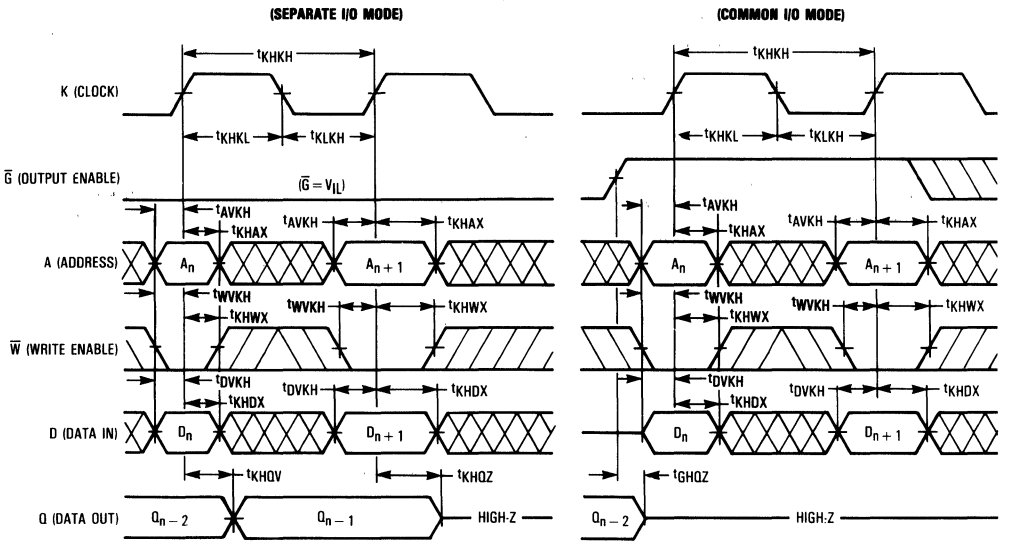
Figure 1B

5

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62974 X XX

- MCM — Motorola Memory Prefix
- 62974 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 30 = 30 ns)

Full Part Numbers — MCM62974FN20 MCM62974FN25 MCM62974FN30

MCM62975

Product Preview

4K x 12 Bit Synchronous Static RAM

with Transparent Outputs and Output Enable

FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62975 is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0–A11), data (D0–D11), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

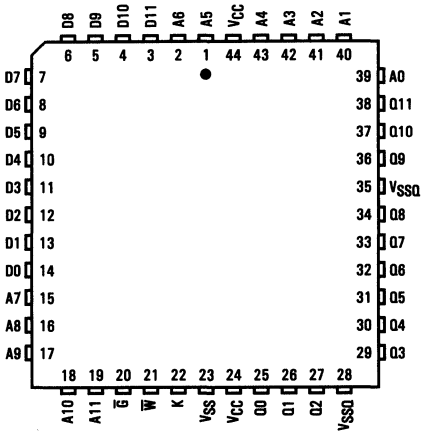
The MCM62975 provides transparent output operation when clock (K) is low for access of RAM data within the same cycle (output data is latched when clock (K) is high).

The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

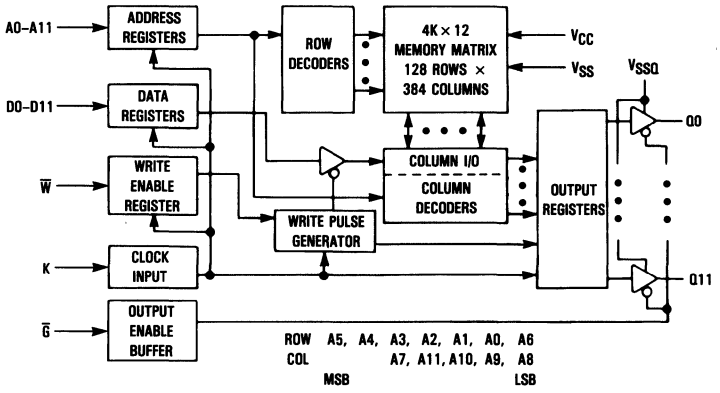
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 25/30/35 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q11	Current
L	Write	High Z	I_{CCA}
H	Read	D_{out}	I_{CCA}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{G}$ = V_{IL}, All Inputs = V_{IL} or V_{IH}, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}			mA
MCM62975-25: t_{KHKH} = 25 ns		–	170	
MCM62975-30: t_{KHKH} = 30 ns		–	170	
MCM62975-35: t_{KHKH} = 35 ns		–	150	
Output Low Voltage (I_{OL} = 12.7 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −1.8 mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE

Parameter	Symbol	MCM62975-25		MCM62975-30		MCM62975-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	—	30	—	35	—	ns	1, 3
Write Cycle Time	t_{KHKH}	25	—	30	—	35	—	ns	2, 3
Clock High Access Time	t_{KHQV}	—	25	—	30	—	35	ns	3, 4, 5
Clock Low to Output Valid	t_{KLQV}	—	10	—	13	—	15	ns	3, 4, 5
$\overline{G}$ Low to Output Valid	t_{GLQV}	—	10	—	13	—	15	ns	3
Output Active from Clock Low	t_{KLQX}	0	—	0	—	0	—	ns	
Output Active from $\overline{G}$ Low	t_{GLQX}	0	—	0	—	0	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	5	—	ns	
Setup Times for: A	t_{AVKH}	5	—	5	—	5	—	ns	1, 2, 6
D	t_{DVKH}								
$\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	—	3	—	3	—	ns	1, 2, 6
D	t_{KHDX}								
$\overline{W}$	t_{KHWX}								
Clock Low to Output High Z ($\overline{W}=V_{IL}$)	t_{KLQZ}	0	10	0	13	0	15	ns	5, 7
$\overline{G}$ High to Output High Z	t_{GHQZ}	0	10	0	13	0	15	ns	3, 7, 8

NOTES:
1. A read is defined by $\overline{W}$ high for the specified setup and hold times.
2. A write is defined by $\overline{W}$ low for the specified setup and hold times.
3. All read and write cycle timing is referenced from K or from $\overline{G}$.
4. Access time is controlled by t_{KLQV} if the clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$; otherwise it is controlled by t_{KHQV}.
5. K must be low for the outputs to transition.
6. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.
7. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min and t_{GHQZ} max is less than t_{GLQX} min for a given device.
8. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

AC TEST LOADS

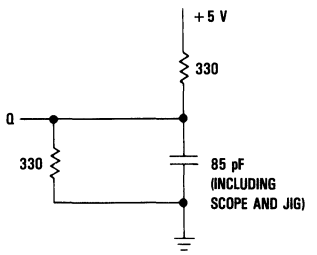


Figure 1A

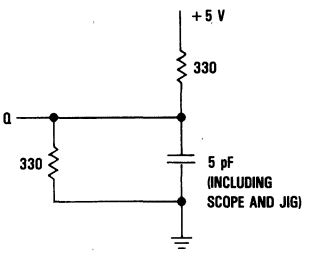
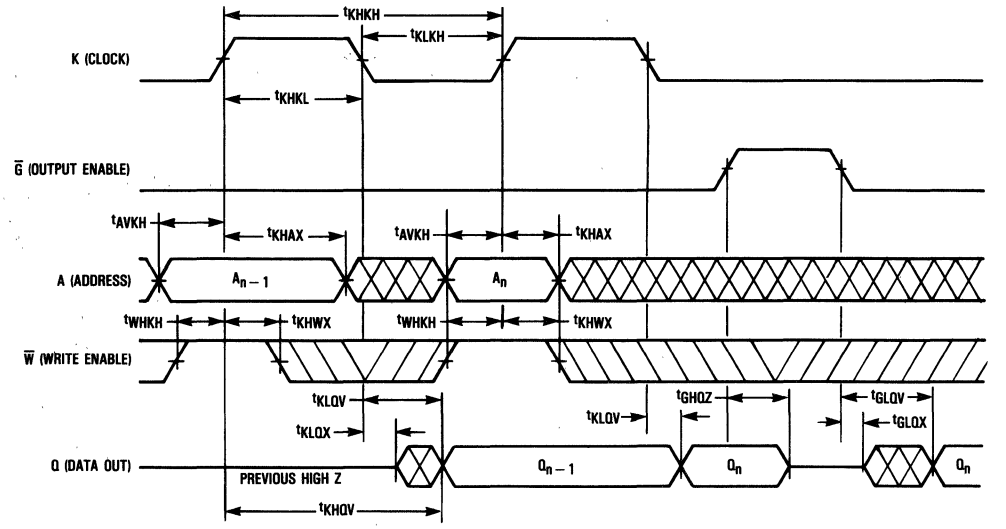


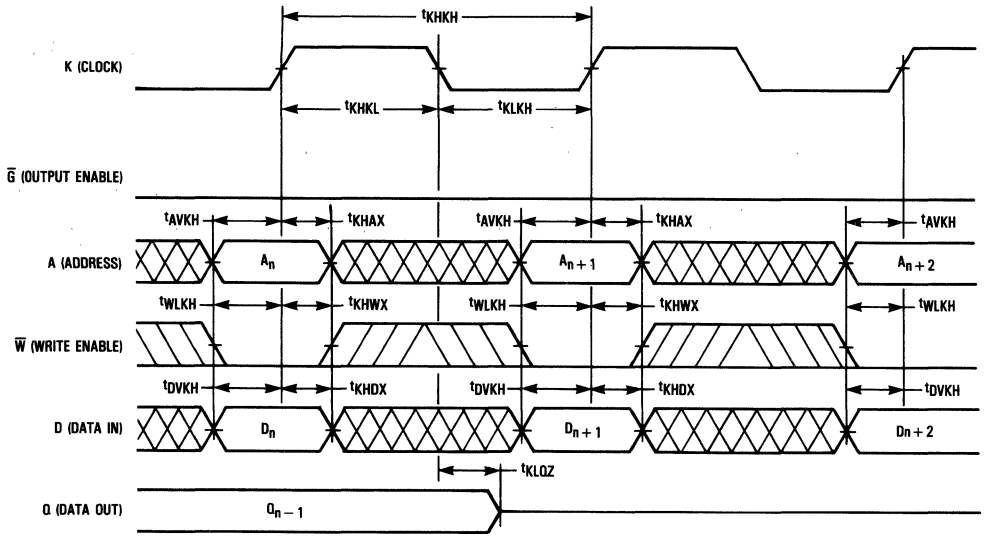
Figure 1B

5

READ CYCLE



WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62975 X XX

Motorola Memory Prefix

Part Number

Speed (25 = 25 ns, 30 = 30 ns, 35 = 35 ns)

Package (FN = PLCC)

Full Part Numbers—MCM62975FN25 MCM62975FN30 MCM62975FN35

MOS EEPROM 6

6

CMOS EEPROM†

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (μs)	Pins
256 x 8	MCM2814P	3.5	8

†Available in Europe only.

MCM2814

Advance Information

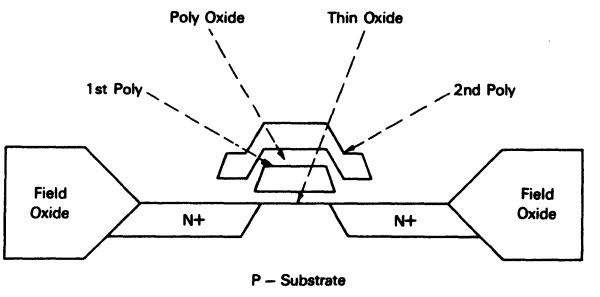
256x8 BIT SERIAL EEPROM

The MCM2814 is a 2048-bit serial electrically erasable PROM. Designed for handling data in applications requiring both non-volatile memory and in-system information updates.

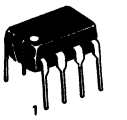
The MCM2814 is fabricated in an 8-pin DIL package using floating-gate HCMOS EEPROM technology.

Features:
- 8-pin DIP, in HCMOS for low consumption.
- 2048 bits organised as 256 bytes.
- Byte programmable.
- 3 – 6 V supply during read operations.
- On-chip Programming Voltage Generator.
- Two programming modes: two-wire serial access, M-bus/four-wire serial access SPI.
- Data protection of ¼, ½, or ¾ array with EEPROM bits.
- Simultaneous programming of 1 to 4 bytes.
- Automatic byte address increment in Read mode.
- Chip selection with separate pin.
- Single 4.5 V to 6 V supply during programming.
- Digital filtering on Clock and Data inputs.
- Bit program operation: no byte erase necessary.
- Data protection after Reset.
- Write/Erase endurance: 10000 cycles.
- Data retention: 10 years.

FETMOS
(Floating-Gate Electron Tunnelling MOS)

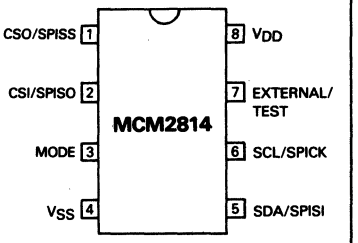


HCMOS
(FLOATING-GATE TECHNOLOGY)
256 x 8 BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 626-04

PIN ASSIGNMENT



PIN DESCRIPTION

V_{DD}:	Power Supply
V_{SS}:	Ground (Ref)
External/ Test	Connected to on-chip Voltage Multiplier output
Mode =	0 M-bus
CS0	Chip Select (Hardwired)
CS1	Chip Select (Hardwired)
SDA	Serial Date I/O
SCL	Serial Clock Input
Mode =	1 SPI
SPISS	Slave Select Input
SPISO	Serial Data Output
SPISI	Serial Data Input
SPICK	Serial Clock Input

6

SECTION 1. PIN DESCRIPTION

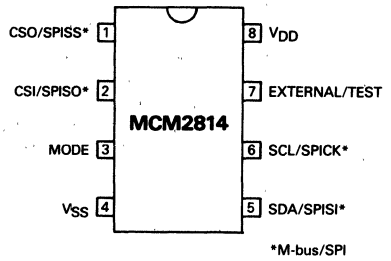


Figure 1 Pinout

1.1 V_{SS}/V_{DD} (Pins 4/8)

V_{DD} and V_{SS} are used to power the circuit. In read mode this supply voltage must be comprised in the V_{DDR} range. (See **5.2 Electrical Characteristics**). In program mode this supply range is limited to V_{DDP}.

1.2 External/Test (Pin 7)

This pin is used for testing the on-chip voltage multiplier that generates the programming voltage required for a program operation, and should be left open for 5 Volt only operation.
An external capacitor (Low leakage) on this pin might have a positive impact on the programming endurance, as the V_{PP} rise time will be increased.
Recommendations will be issued after the characterisation. As this on-chip generator has a high impedance, an external supply can be connected to this pin. This also allows to block any inadvertant programming by maintaining this pin at V_{DD}.

1.3 Mode (Pin 3)

This pin is used to select one of two modes of operation: M-bus mode at the low logic level or SPI mode at high level.
This pin is usually hardwired to V_{SS} or V_{DD}. It should only be changed if the circuit is internally in a standby state. This pin is high impedance when V_{DD} is at V_{SS} level.

1.4 CS1 / SPISO (Pin 2)

In M-bus mode, this pin is used for selecting multiple identical chips on the same serial bus. The chip address is formed by 5 bits predefined for this chip, followed by 2 additional chip select bits. These last two bits must correspond to the CS1 / CS0 code for proper chip selection. Up to four MCM 2814 can be connected on the same SCL and SDA lines. (See **Figure 4**).

In SPI mode this pin is a push-pull slave data output (SPISO). It will shift-out byte addresses and data as described in Section 4.
This pin is usually connected to the data input pin of a SPI master (MISO).
This pin can not be pulled higher than 0.5 V above V_{DD}, even if V_{DD} is at V_{SS} level.

1.5 CSO / SPISS (Pin 1)

In M-bus mode this pin is used in conjunction with CS1 for chip selection. (See **above**).

In SPI mode this pin is a Slave Select input. In this mode the serial access is deselected when the SPISS input is high, and the SPISO data output pin is forced high impedance. Multiple chips using the same SPICK, SPISI and SPISO lines, can be selected via this pin as described in Figure 10.
After powering up the device, a falling edge of the SPISS line is required to start the SPI serial access.

This pin is high impedance when V_{DD} is at V_{SS} level.

1.6 SCL / SPICK (Pin 6)

The serial clock is supplied on pin SCL / SPICK. This pin is an input only, therefore the chip can only operate as a slave under the control of a serial bus master.
The clock input rising edge is used to shift in data present on the SDA/SPISI pin, and the falling edge is used to shift out data on the SDA or SPISO pin.

This pin is high impedance when V_{DD} is at V_{SS} level.

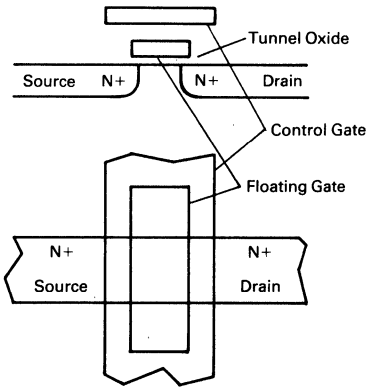
1.7 SDA / SPISI (Pin 5)

In M-bus mode, SDA pin is used to transmit data serially in the memory (Receiver) or from the memory (Transmitter). Data transmitted via this pin includes chip addresses, byte addresses, byte data, Read/Write and acknowledge bits. When SDA is in output, it operates as a pull-down only device (Open-drain). The protocol of this transmission is described in Figures 5 and 6.

In SPI mode, this pin is a Slave data Input (SPISI) only and is used to receive opcodes, byte addresses and byte data. It is usually connected to the data output pin of a SPI master. (MOSI).

This pin is high impedance when V_{DD} is at V_{SS} level.

SECTION 2. EEPROM



	CG	D	S
READ	0V	VDD	0V
PROG 1	0V	VPP	OPEN
PROG 0	VPP	0V	0V

Figure 2 EEPROM Transistor

256 Bytes of EEPROM memory are implemented in a floating gate double poly-silicon process. A Byte Address register is used to select one of the bytes. Three basic state of operation can be distinguished :

- Standby state.
- Read state
- Program state

2.1 EEPROM Operation

2.1.1 Standby State

In this state, neither a programming, nor a serial transmission occurs, and the power consumption is minimum. (See **3.4.1** and **4.5**).

2.1.2 Read State

In read state the data of the selected byte is transferred from the memory array to the data shift register used for the serial transmission. This state is active during a serial transmission.

2.1.3 Program State

In this state, a programming voltage higher than V_{DD} is necessary. This voltage is generated by the on-chip voltage multiplier or can be supplied externally. During programming V_{DD} must be within the V_{DDP} range. (See **5.2**).

In M-bus mode, the programming starts at the end of a write command, when a STOP or a new START condition occurs. The programming is enabled at this time, as well as the on-chip voltage multiplier. If there is a capacitive load on the V_{PP} pin, the V_{PP} rise time should be added to the minimum program time t_{PROG}.

In SPI mode, programming could start when a write serial transmission is ended with an SPISS rising edge. Actual programming will only happen if enabled by a V_{PP} enable serial command. This command can be transmitted before or after the write sequence.

2.2 EEPROM Data Protection

Some circuitry has been included to prevent unwanted modification of EEPROM data, and is described below. However, a noisy serial link is very often the cause of bad data or data written to the wrong address. Besides measures to reduce this noise on the board, the serial clock and data inputs (SCL/SDA) have Schmitt triggers and digital filters to reject some of the noise.

2.2.1 Power Up Reset

Immediately after power is applied, programming is inhibited to prevent EEPROM data loss during the system power up.

In both modes this condition is removed when a READ is performed.
In M-bus mode, the read bit with a valid chip address gives the control to the MCM2814. Therefore another 8 bits read without master acknowledge is necessary to stop the read sequence.
In SPI mode, it is sufficient to send the READ opcode before a new V_{PP} enable command and the write sequence.

At Reset the following circuitry is initialised:

- The circuit is in standby state.
- In M-bus mode, it is waiting for a start condition.
- In SPI mode, it is waiting for a high to low SPISS transition.
- The data outputs are high impedance (SDA, SPISO).
- The programming is disabled.
- The on-chip Vpp generator is off.
- The byte address register is cleared ($00).

2.2.2 Programming Voltage Enable

In SPI mode only, an internal programming voltage enable flip-flop can be set or cleared with two separate opcodes, thus reducing the risk of unwanted EEPROM programming.

2.2.3 Array Write Protect

In both modes, byte address 255 ($FF) contains EEPROM bits with a special function. When one or two bits of this address are programmed at once, the programming of EEPROM sections is inhibited according to the following table:

Data at ADDR $FF		Protected Addresses	No. of Bytes Protected
XXXX	00XX	No Write Prot.	-
XXXX	01XX	$C0 – $FB	60
XXXX	10XX	$80 – $FB	124
XXXX	11XX	$40 – $FB	188

X = Don't care

Table 1 EEPROM Write Protect

This protection is reversible as address 255 ($FF) can be modified at any time.

2.3 EEPROM Properties

NO ERASE : Unlike most EEPROM's it is not necessary to erase a byte before writing new data to it.
The program operation takes t_{PROG} and must be externally timed.

CUMULATIVE : As the programming operation is under external control, it can be done at once or at various time frames as long as the total programming time exceeds the specified minimum t_{PROG} value.
t_{PROG} is defined with Vpp at its programming level.

SELF LIMITING : Excess pogramming has no positive effect, as programmed EEPROM thresholds will asymptotically reach their nominal values. Programming durations above the recommended maximum t_{PROG} have negative impacts on the EEPROM programming endurance.

2.4 EEPROM Reliability

Reliability figures are statistical in nature. Therefore no minimum or maximum specifications can be applied. The result of reliability tests will be published instead. These tests are conducted on a regular basis during the production life of a circuit and reports are available upon request.

2.4.1 Data Retention

Typical data retention should exceed 10 years for the specified operating temperature range. Data retention is usually tested with the device under bias, but without accessing the EEPROM array.

2.4.2 Read Stress

Unlike some non-volatile memories, there should be no disturbance of the stored data under continuous read of EEPROM bytes. The life limit under continuous read condition should therefore be similar to the normal operating life of the device.

2.4.3 Program Endurance

As for all EEPROM's, there is a wearout mechanism associated with the programming mechanism of the non volatile memory. More than 10,000 programming cycles should be possible per memory bit, for the specified operating temperature range. A programming cycle is defined as a 0 to 1 to 0 programming. Unlike most EEPROM's where the whole byte is erased before being re-programmed, if just one bit is modified in a byte, only this bit will see the programming stress.
Some endurance experiments have shown that the number of programming cycles can be increased if the Vpp rise time is increased. This can be achieved with an external capacitor on Vpp when the on-chip Vpp generator is used. In SPI mode, the Vpp should be enabled after the write command has been transmitted.
If an external Vpp is provided, it should be ramped up only after the write command is transmitted. In this case, a Vpp above the maximum value has also a neagtive impact on the endurance.

2.5 Vpp Voltage Multiplier

In M-bus mode, the on-chip Vpp generator is turned on or off automatically during a program sequence.

In SPI mode, it is switched on only after a serial Vpp enable command has been issued, independently of write or read commands.

SECTION 3. M-BUS OPERATING MODE

The MODE pin can be hardwired to V_{DD} or V_{SS} to select two different modes of operation. Differences are at the serial transmission level and in the EEPROM operation. They are called M-bus mode and SPI mode.

3.1 M-bus Mode

Only two wires are needed to control the device operation. The serial transmission of this mode is similar to the IIC (*) serial communication standard. It features :

- Up to 4 identical chips on the same 2 wire bus.
- CS1 / CS0 pins for chip selection.
- SCL clock line, input only.
- SDA line used as Input and Output.
- Data acknowledge bit generated.
- Auto programming after reception of new data.
- Programming time under external control.
- Write inhibit after reset.

*IIC is a trademark of Philips

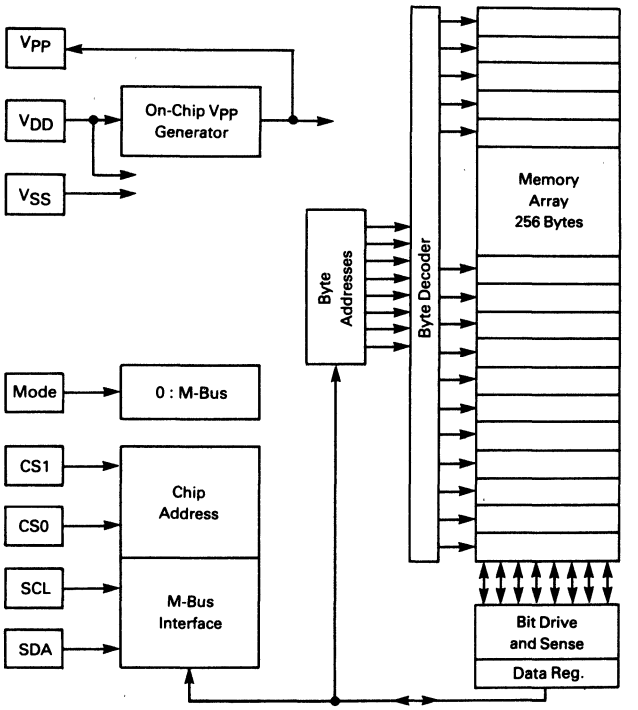


Figure 3 M-bus Block Diagram

3.2 Lexicon

This lexicon will describe some terms used in this serial interface description.

MASTER : The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. This memory can never function as a master.

SLAVE : This memory always operates as a slave.

TRANSMITTER : The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open-Drain connection.

RECEIVER : A device that has been properly selected by a chip address followed by a write bit is a receiver, and will

shift data present on the SDA pin in internal registers.

MSB : The Most Significant Bit is the first bit transmitted and received.

START CONDITION : The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the R/W bit. All devices connected on the same bus receive this data to check if they are addressed.

STOP CONDITION : The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.
A STOP after a serial read sequence will put the device in standby state.

CHIP ADDRESS : The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7 bit chip address is formed of 5 fixed bits followed by 2 chip select bits.
Fixed bits are 1010X for this device (X is a don't care bit).

The 2 chip select bits must correspond to the 2 chip select inputs for proper chip selection. By this means, up to 4 identical chips can be connected on the same SDA / SCL lines, in order to form a memory bank of up to 8 KBits.

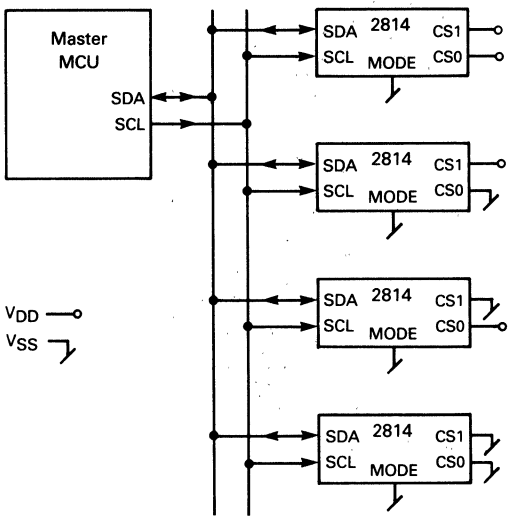
READ/WRITE BIT : The 8th bit transmitted by the master after the 7 bit chip address will indicate the direction of transfer for the next bytes. (Until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the MCM 2814.

BYTE ADDRESS : The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

ACKNOWLEDGE BIT : This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

3.3 Chip Selection

The 2 chip select bits transmitted in the chip address must match the status of CS1 and CS0 inputs.



Pin Status			Chip Address Transmitted
Mode	CS1	CS0	
0	1	1	1010 X11
0	1	0	1010 X10
0	0	1	1010 X01
0	0	0	1010 X00

X = Don't care

Figure 4 M-bus Chip Selection

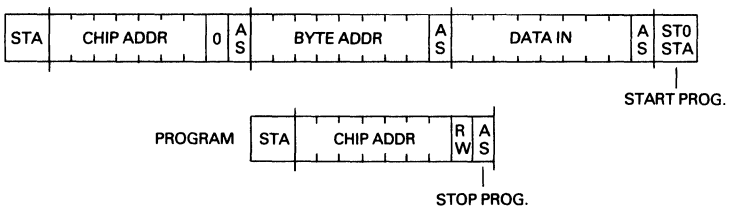
3.4 Protocol

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

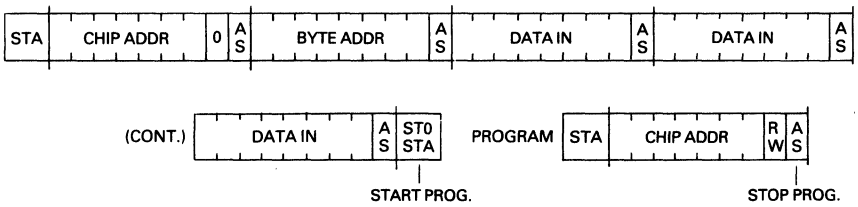
3.4.1 Standby State

When no serial transmission and no programming are made, the circuit is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the circuit in standby. A new START condition will wake up the device, to get the chip address. If the chip address is not valid, the device will return in standby.
The power consumption is minimum in standby.

Write One Byte



Write up to 4 Bytes



STA: Start Condition
STO: Stop Condition
R/W BIT: 1 = Read/0 = Write
INC: Increment Byte Address
AS: Slave Acknowledge (2814)
AM: Master Acknowledge

Figure 5 M-bus Write Protocol

3.4.2 Write Sequence

The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop or a new start condition, the programming sequence is initiated.

Programming is under control of the master. It is initiated by the write sequence just described, and stopped by any new valid selection of the chip.
Therefore, the t_{PROG} time is defined as the time between these two operations, and is defined by the master.

Bad chip addresses or chip addresses for other chips on the same bus do not suspend the programming.

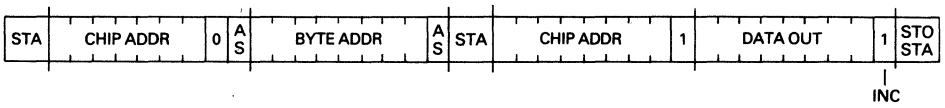
The on-chip V_{PP} generator is automatically turned on or off when needed. If an external V_{PP} is applied, the programming voltage is only allowed into the array during the above defined t_{PROG} time.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

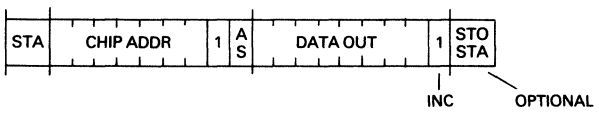
3.4.3 Read Sequence

Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read this step can be skipped.
The byte address is automatically incremented after each data byte transmitted.
This is also valid after the last byte of a transmission.
Therefore, the next read sequence without any byte address specified, will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case the SDA output driver will switch off and the circuit will go to standby.

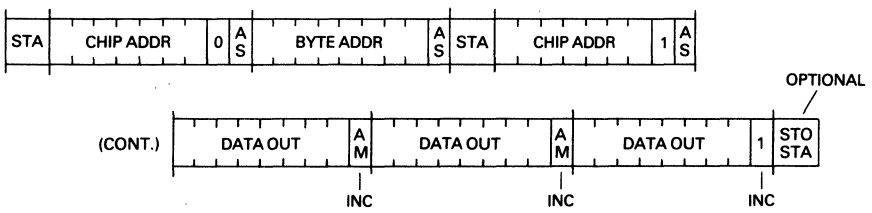
Read One Byte. (Inc. Write Byte Address)



Read One More Byte. (Byte Address Defined)



Read Many Bytes



STA: Start Condition R/W BIT: 1 = Read/0 = Write AS: Slave Acknowledge (2814)
STO: Stop Condition INC: Increment Byte Address AM: Master Acknowledge

Figure 6 M-bus Read Protocol

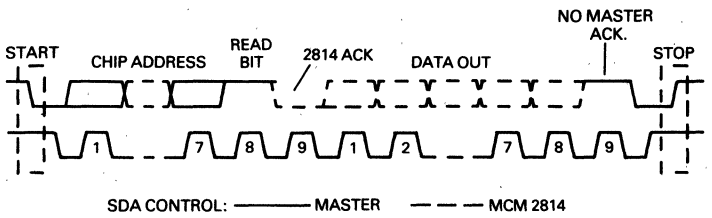


Figure 7 M-bus Read Detail

3.4.4 Signal Levels

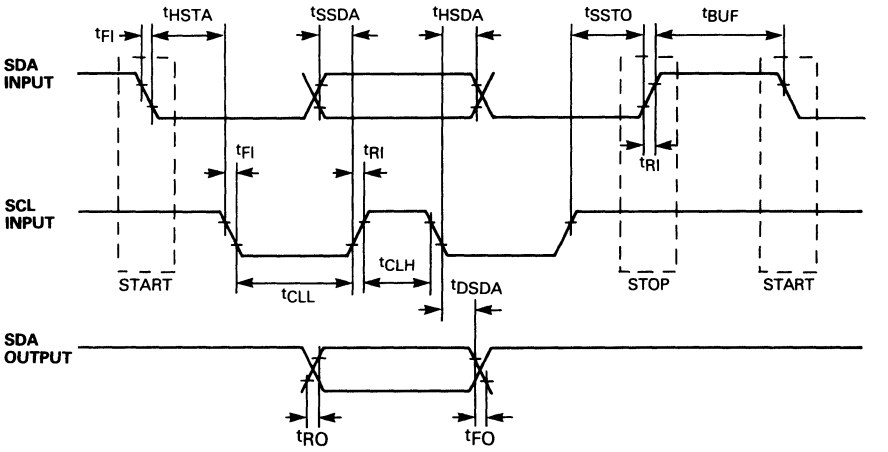


Figure 8 M-bus Timings

Electrical and switching characteristics are described in Section 5.
During a transmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognised as a START condition, the positive transition as a STOP condition.

The acknowledge bit is provided by the device receiving data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.
As this memory has an open drain SDA output, an external pull-up resistor to V_{DD} should be included on SDA line.

SECTION 4. SPI OPERATING MODE

The serial transmission of this mode requires 4 wires to control the device operation. It features:

- Multiple chips on same 3 wire bus with separate chip select lines.
- SPISS chip selection.
- SPICK clock line, Input only.
- SPISI line used as Input only.
- SPISO line used as Output only.
- No acknowledge bit.
- Programming under control of the master via serial opcodes.
- Programming time under external control.
- Write inhibit after reset.
- Write enable/disable via serial opcodes.
- Byte address output for transparency.

This SPI mode can be used with the SPI of Motorola Microprocessor MC6805S2/S3, MC6805K2/L3/L8, MC68HC05C4 and MC68HC11.

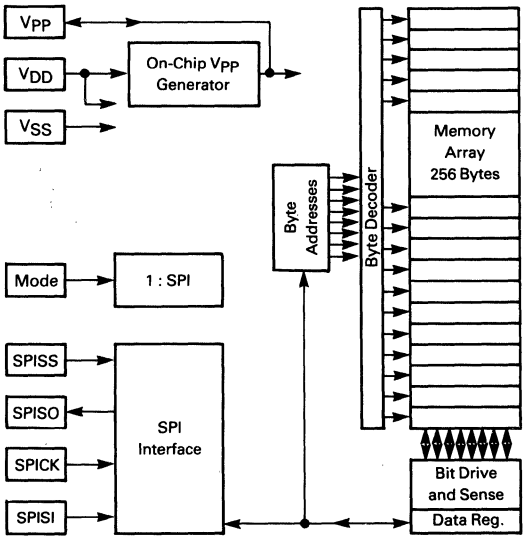


Figure 9 SPI Block Diagram

6

4.1 SPI Serial Interface

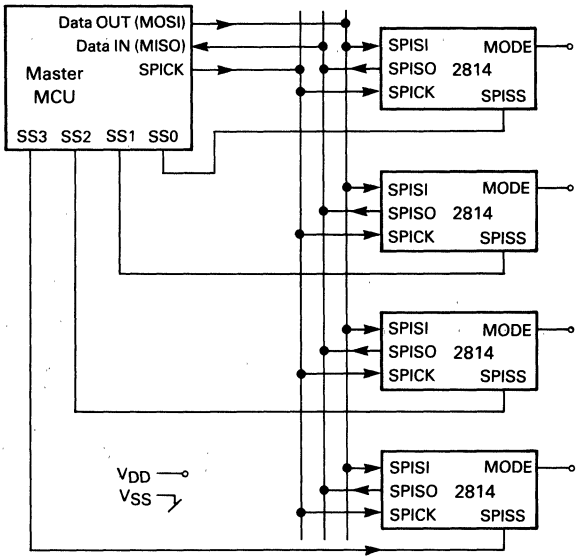


Figure 10 SPI Chip Selection

The serial interface via pins SPICL, SPISI and SPISO is compatible with the SPI standard when the MODE pin is high.

4.2 Lexicon

This lexicon will describe some terms used in this serial interface description.

MASTER : The device that generates the serial clock on SPICK is designated as master. This memory can never function as a master.

SLAVE : This memory always operate as a slave as the SPICK pin is always an input.

TRANSMITTER / RECEIVER : This device has separate pins for data transmission (SPISO) and reception (SPISI). Simultaneous data input and output can therefore occur when the chip is selected with SPISS and is clocked (SPICK).

MSB : The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT : The chip is selected when pin SPISS is low. When the chip is not selected, no data will be input from pin SPISI, and output pin SPISO is high impedance.

4.3 Serial Op-Code

The first byte transmitted after the chip is selected with SPISS going low, contains the opcode that defines the operation to be performed.

Data Transmitted	Operation
1010 0111	Read byte address followed by data.
1010 0110	Program enable. V_{PP} generator ON.
1010 0100	Program disable. V_{PP} generator OFF.
1010 0010	Write (Program) data.

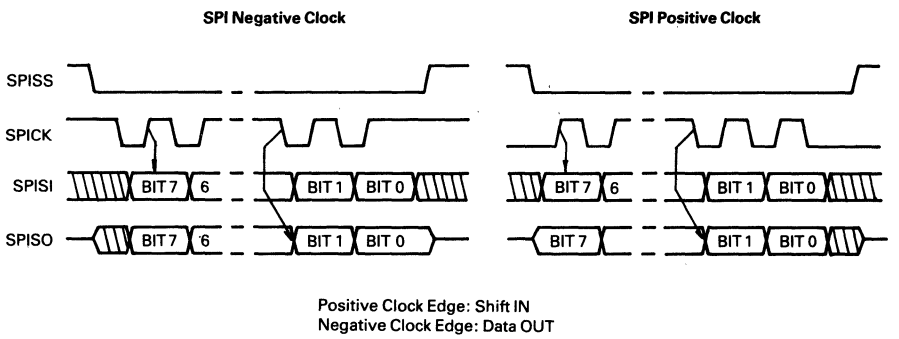
Table 2 SPI Opcodes

All other codes are invalid. After an invalid code is received, no data is shifted in the MCM 2814 and the SPISO data output is high impedance until a new SPISS falling edge re-initialises the serial communication.

4.4 Protocol

The MCM2814 SPI interface accepts both a negative or positive clock.
The SPI protocol for this device defines the bytes transmitted on the SPISI and SPISO data lines for proper chip operation.

6



Positive Clock Edge: Shift IN
Negative Clock Edge: Data OUT

Figure 11 SPI Clock Phase and Polarity

4.5 Standby State

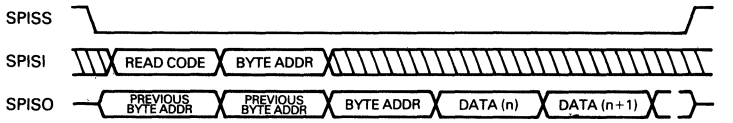
The circuit is in standby when no serial transmission takes place, when no write is waiting for the V_{PP} enable command and when the V_{PP} generator is off.
When SPISS is high, standby state will follow:

- A power up reset.
- A V_{PP} disable command.
- A Read, providing no V_{PP} enable command has been issued previously.

The power consumption is minimum in standby.

4.6 Read Sequence

Read One or More Bytes



Invalid Opcodes

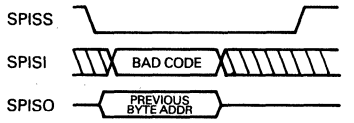


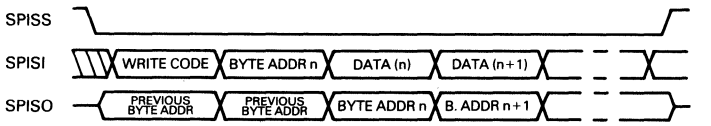
Figure 12 SPI Read

Reading the memory via the serial SPI link requires the following sequence. The SPISS line is pulled low to select the device. The read opcode is transmitted on the SPISI line followed by the byte address. When this is done, data on the SPISI line has no more influence on the memory. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte address. The new byte address is then transmitted followed by corresponding data. If just one byte is read, SPISS can be pulled back to the high level. It is possible to continue the read sequence, as the byte address is automatically incremented. The byte address is shifted out only once, in the beginning of a transmission.

6

4.7 Program Sequence

Write One to Four Bytes



Vpp Enable/Disable

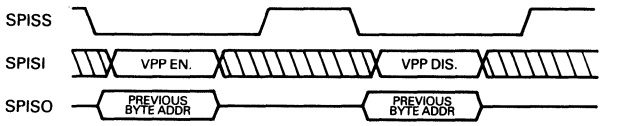


Figure 13 SPI Program

To program a byte, two separate conditions must be simultaneously present. The program must be enabled via the Vpp enable command, and a serial write must be done. The Vpp enable will also turn on the on-chip Vpp generator. At this time, the chip is obviously not in standby, even if SPISS is high. The program disable command will stop the on-chip Vpp supply and protect the EEPROM data against unwanted modifications. An external Vpp supply will also oe internally enabled or disabled by this mechanism.
A write serial sequence includes an SPISS high to low transition, followed by the write code on the SPISI line. The byte address followed by the corresponding data to be written are then shifted through the SPISI pin. At the

beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte to be programmed. The new byte address is also echoed for possible checking by the master. If Vpp is enabled, the programming will start after the SPISS line goes back to a high level. It is also possible to issue the Vpp enable command after the write sequence.
If the Vpp enable command is issued after the serial write, no Read or invalid code should be transmitted in between as this would clear the programming latch containing the data to be programmed.
The programming is suspended when a new chip selection with SPISS low occurs. It is then possible to send a new write command to program new data. A Vpp enable or a Read command will stop the programming.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

4.8 Signal Levels

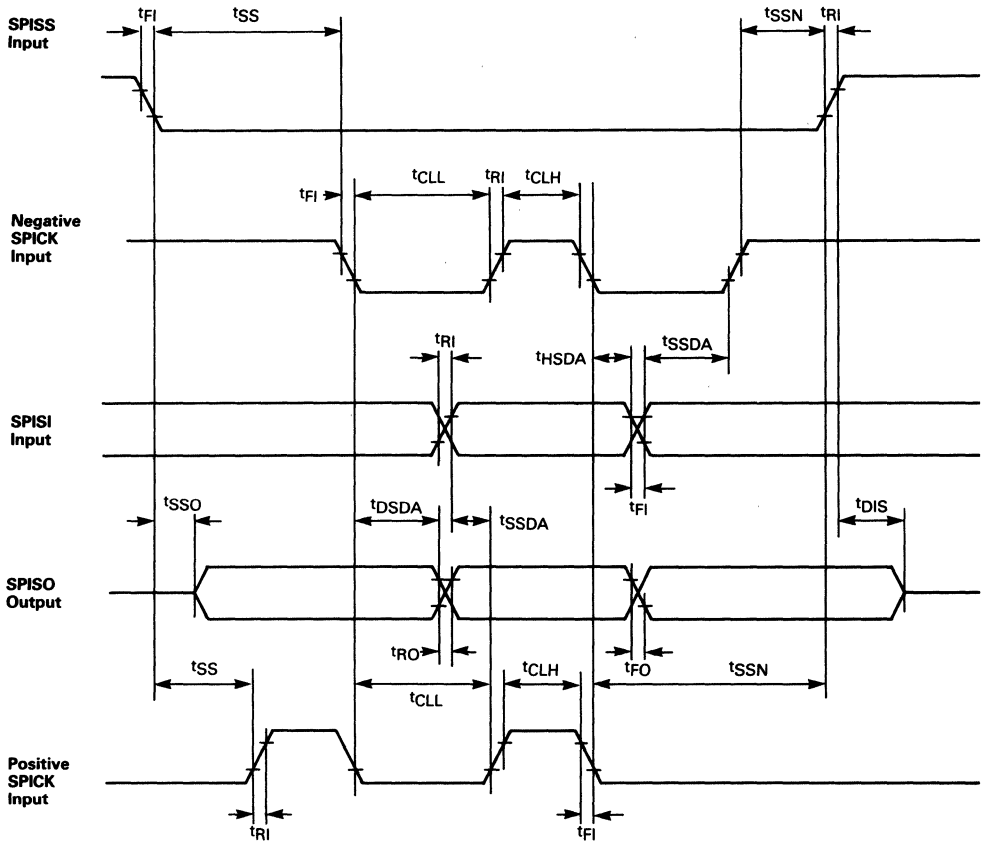


Figure 14 SPI Timings

Electrical and switching characteristics are described in **Section 5.**

SECTION 5. CHARACTERISTICS

V_{SS} = 0 V

5.1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	Vdc
Input voltage pins 1, 3, 5, 6	V_{in}	−0.3 to +7.0	Vdc
Input voltage pin 2	V_{in}	−0.3 to V_{DD} +0.3	Vdc
Current on any Input	I_{in}	0.1	mA
Sink current SDA	ISDAL	10	mA
Sink current SPISO	ISOL	10	mA
Source current SPISO	ISOH	10	mA
Operating temperature	T_A	0 to 70*	°C
Storage temperature	T_S	−55 to 125**	°C
Junction Temperature	T_j	150**	°C
Thermal resistance	Th_{ja}	200	°C/W

*Specification over the temperature range, −40 to +85°C to be determined.

Stresses above those listed under 'Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum operating conditions for extended periods may affect reliability.

**In particular, continuous high temperature application may cause leakage of stored charge in EEPROM, resulting in data loss.

5.2 Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage STANDBY	V_{DDS}	-	-	6.0	Vdc
Supply current STANDBY*	I_{DDS}	-	1	TBD	μA
Supply voltage READ	V_{DDR}	3.0	-	6.0	Vdc
Supply current READ*	I_{DDR}	-	0.3	1.5	mA
Supply voltage PROG	V_{DDP}	4.5**	-	6.0	Vdc
Supply current PROG*	I_{DDP}	-	0.5	3.0	mA

*Inputs at V_{SS} or V_{DD}.
**Programmability at 3 V V_{DDP} (min) is still to be determined.

5.3 Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SCL, SDA, SPISS, SPISI Inputs					
Input low voltage	V_{IL}	−0.3	-	$0.3*V_{DD}$	Vdc
Input high voltage	V_{IH}	$0.7*V_{DD}$	-	$V_{DD}+0.3$	Vdc
Input leakage	I_{IN}	-	-	±10	μA
SDA/SPISO Pull down Outputs					
Output low I_{OL} <10μA	V_{OL}	-	-	0.1	Vdc
Output high leakage	I_{OH}	-	-	±10	μA
Output low I_{OL} = 3 mA V_{DD} = 5 V	V_{OL}	-	-	0.4	Vdc
Output low I_{OL} = 1 mA V_{DD} = 3 V	V_{OL}	-	-	0.4	Vdc
SPISO Pull up Output					
Output high I_{OH} = 1.6 mA V_{DD} = 5 V	V_{OH}	$V_{DD}-0.8$	-	-	Vdc
Output high I_{OH} = 0.4 mA V_{DD} = 3 V	V_{OH}	$V_{DD}-0.3$	-	-	Vdc
MODE, CS1, CS0 Inputs					
Input low voltage	V_{ILV}	−0.3	-	$0.3*V_{DD}$	Vdc
Input high voltage	V_{IH}	$0.7*V_{DD}$	-	$V_{DD}+0.3$	Vdc
Input leakage	I_{IN}	-	-	±10	μA
Input capacitance	C_{IN}	-	10	-	pF

5.4 SWITCHING PARAMETERS

5.4.1 General

Characteristic	Symbol	Min	Typ	Max	Unit
Programming time 1 byte	t_{PROG}	10	-	t_{BD}	mS
Programming time 4 bytes	t_{PROG}	20	-	t_{BD}	mS

6

5.4.2 Serial Bus Input

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISI, SCL/SPICK, SPISS Inputs					
Clock frequency	F_{SCL}	0.0	-	125	kHz
Clock High time	t_{CLH}	4.0	-	-	µS
Clock Low time	t_{CLL}	4.0	-	-	µS
Stop to Start delay	t_{BUF}	4.0	-	-	µS
Start hold time	t_{HSTA}	4.0	-	-	µS
Data hold time	t_{HSDA}	0.0	-	-	µS
Data set-up time	t_{SSDA}	250	-	-	nS
Input Rise time	t_{RI}	-	-	1.0	µS
Input Fall time	t_{FI}	-	-	300	nS
Stop set-up time	t_{SSTO}	4.0	-	-	µS
SPISS Lead time	t_{SS}	4.0	-	-	µS
SPISS Lag time	t_{SSN}	4.0	-	-	µS

All values refer to V_{IH} and V_{IL} levels.

5.4.3 Serial Bus Output

V_{DD} = 5 Vdc ±10%. T_A = 0 to 70°C. C_L = 200 pF.

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs					
Data delay	t_{DSDA}	-	1.5	3.5	µS
Rise time SDA	t_{RO}	-	-	*	nS
Rise time SPISO	t_{RO}	-	-	100	nS
Fall time	t_{FO}	-	-	100	nS
SPI select time	t_{SSO}	-	-	1.2	µS
Disable time	t_{DIS}	-	1.5	3.5	µS

V_{DD} = 3.3 Vdc ± 10%. T_A = 0 to 70°C. C_L = 200 pF.

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs					
Data delay	t_{DSDA}	-	2.0	3.5	µS
Rise time SDA	t_{RO}	-	-	*	nS
Rise time SPISO	t_{RO}	-	-	200	nS
Fall time	t_{FO}	-	-	200	nS
SPI select time	t_{SSO}	-	-	1.5	µS
Disable time	t_{DIS}	-	2.0	3.5	µS

All values referred to V_{IH} and V_{IL} levels.
*Depends on external pull-up resistor value.

MECL Memories

7

RAMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
8×2	MCM10143	15.3	24
16×4	MCM10145	15	16
16×4	MC10H145	6	16
64×1	MCM10148	15	16
128×1	MCM10147	15	16
256×1	MCM10144	26	16
256×1	MCM10152	15	16
1024×1	MCM10146	29	16

PROMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
32×8	MCM10139	20	16
256×4	MCM10149-10	10	16
256×4	MCM10149-25	25	16

CAM

(0 to 75°C)

Organization	Part Number	Associate Time (ns max)	Pins
8×2	MCM10H155	7	18

7

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MC10H145

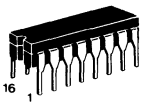
Advance Information

16 x 4 BIT REGISTER FILE

The MC10H145 is a 16 x 4 bit register file. The active-low chip select allows easy expansion.

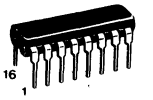
The operating mode of the register file is controlled by the $\overline{WE}$ input. When $\overline{WE}$ is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address, when $\overline{WE}$ is "high," the device is in the read mode — the data state at the selected location is present at the Q_n outputs.

- Address Access Time, 3.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



FN SUFFIX
PLCC
CASE 775

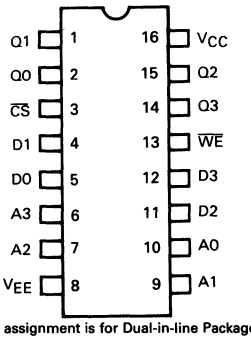
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

Q-State of Addressed Cell

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	165	—	150	—	165	mA
Input Current High	I_{inH}	—	375	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

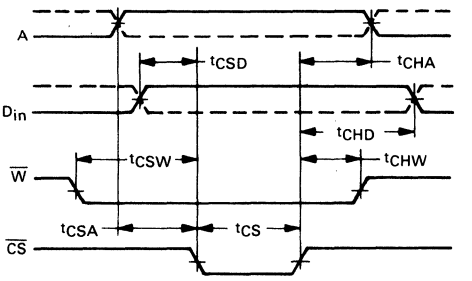
7

AC PARAMETERS

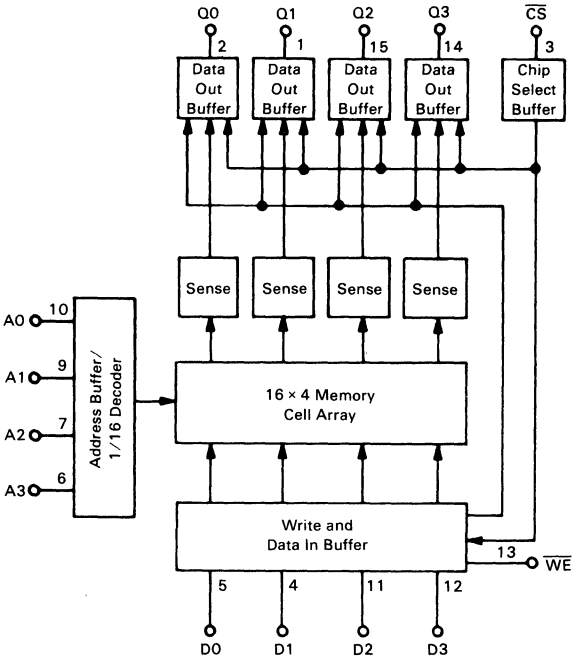
Characteristics	Symbol	MC10H145 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5% Min	Max	Unit	Conditions
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	0	4.0		
Chip Select Recovery Time	t_{RCS}	0	4.0		
Address Access Time	t_{AA}	0	6.0		
Write Mode				ns	t_{WSA} = 3.5 ns Measured at 50% of input to 50% of output. t_W = 6.0 ns.
Write Pulse Width	t_W	6.0	—		
Data Setup Time Prior to Write	t_{WSD}	0	—		
Data Hold Time After Write	t_{WHD}	1.5	—		
Address Setup Time Prior to Write	t_{WSA}	3.5	—		
Address Hold Time After Write	t_{WHA}	1.5	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	—		
Chip Select Hold Time After Write	t_{WHCS}	1.5	—		
Write Disable Time	t_{WS}	1.0	4.0		
Write Recovery Time	t_{WR}	1.0	4.0		
Chip Enable Strobe Mode				ns	Guaranteed but not tested on standard product. See Figure 1.
Data Setup Prior to Chip Select	t_{CSD}	0	—		
Write Enable Setup Prior to Chip Select	t_{CSW}	0	—		
Address Setup Prior to Chip Select	t_{CSA}	0	—		
Data Hold Time After Chip Select	t_{CHD}	1.0	—		
Write Enable Hold Time After Chip Select	t_{CHW}	0	—		
Address Hold Time After Chip Select	t_{CHA}	2.0	—		
Chip Select Minimum Pulse Width	t_{CS}	4.0	—		
Rise and Fall Time	t_r, t_f			ns	Measured between 20% and 80% points.
Address to Output		0.6	2.5		
CS to Output		0.6	2.5		
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	6.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MC10H145. $C_L \leq$ 5.0 pF (including jig and Stray Capacitance) Delay should be derated 30 ps/pF for capacitive loads up to 50 pF
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

FIGURE 1 — CHIP ENABLE STROBE MODE



BLOCK DIAGRAM



7

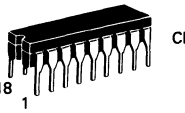
MC10H155

Advance Information

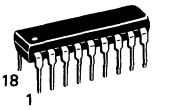
CONTENT ADDRESSABLE MEMORY

The MC10H155 is a 16-bit ECL Content Addressable Memory (CAM). The device is organized as an array of 8 words by 2 bits with each cell of the array containing an exclusive-OR comparator, a D-type latch as well as control logic. The modes of operation possible with the MC10H155 are reading, writing, associate, masked associate and the hybrid mode.

- Associate Time 7.0 ns Max
- Single Bit Masking
- Open Emitter Match Lines for Easy Bit Expansion
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

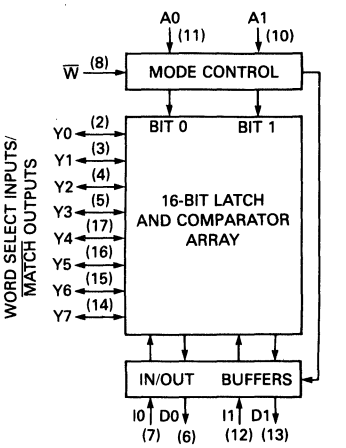


L SUFFIX
CERAMIC PACKAGE
CASE 726-04

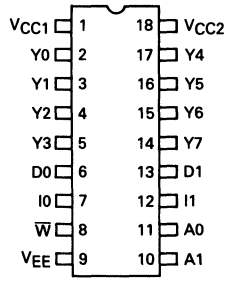


P SUFFIX
PLASTIC PACKAGE
CASE 707-02

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	−8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	−55 to +150 −55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V ±5%) (See Note)

		0°C		25°C		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	135	—	125	—	135	mA
Input Current High Pins 2,3,4,5,7, 12,14,15,16,17 Pins 10,11 Pin 8	I_{inH}	 — — —	 380 435 400	 — — —	 240 270 250	 — — —	 240 270 250	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	Vdc
Low Output Voltage	V_{OL}	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	Vdc
High Input Voltage	V_{IH}	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	Vdc
Low Input Voltage	V_{IL}	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	Vdc

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to −2.0 volts.

This document contains information on a new product. Specifications and information herein is subject to change without notice.

AC PARAMETERS

Characteristic			0°		25°		75°C		Unit
			Min	Max	Min	Max	Min	Max	
Associate Time	(I to Y)	TA1	—	6.0	—	6.0	—	7.0	ns
	(A to Y)	TA2	—	6.0	—	6.0	—	7.0	
Disable Time	(A to Y)	TD1	—	6.0	—	6.0	—	7.0	ns
	(A to D)	TD2	—	4.0	—	4.0	—	5.0	
	(Y to D)	TD3	—	7.5	—	7.5	—	8.0	
Setup Time	(A to $\overline{W}$)	TS2	—	8.0	—	8.0	—	9.0	ns
	(Y to $\overline{W}$)	TS3	—	3.0	—	3.0	—	4.0	
	(I to $\overline{W}$)	TS4	—	4.0	—	4.0	—	5.0	
Write Pulse Width		TW	—	8.0	—	8.0	—	9.0	ns
Write Access Time TS4 ≥ TW	($\overline{W}$ to D)	TA3	—	8.0	—	8.0	—	9.0	
TS4 ≥ TW	(I to D)	TA4	—	6.0	—	6.0	—	7.0	
Hold Time	($\overline{W}$ to A)	TH1	—	1.0	—	1.0	—	1.5	ns
	($\overline{W}$ to Y)	TH2	—	3.0	—	3.0	—	4.0	
	($\overline{W}$ to I)	TH3	—	3.0	—	3.0	—	4.0	
Read Access Time TS4 ≥ TW	(Y to D)	TA5	—	6.0	—	6.0	—	6.0	ns
TS4 ≥ TW	(A to D)	TA6	—	4.0	—	4.0	—	5.0	
Cycle Time, CP Rate			40	—	40	—	35	—	MHz

TRUTH TABLE

Mode	A0	A1	I0	I1	$\overline{W}$	D0	D1	Qn0	Qn1	Yn
Associate[1]	1	1	1/0	1/0	X	0	0	Qn0	Qn1	Qn0 ⊕ I0 + Qn1 ⊕ I1
Associate[1,2] (Masked)	1	0	1/0	X	1	0	D1	Qn0	Qn1	Qn0 ⊕ I0
Associate[1,2] (Masked)	0	1	X	1/0	1	D0	0	Qn0	Qn1	Qn1 ⊕ I1
Read[2,3]	0	0	X	X	1	D0	D1	Qn0	Qn1	0 (Selected Address)
Write[3,4]	0	0	1/0	1/0	0	I0	I1	I0	I1	0 (Selected Address)
Hybrid[5]	1	0	1/0	1/0	0	0	I1	Qn0	I1•$\overline{Y}$n	Qn0 ⊕ I0
Hybrid[5]	0	1	1/0	1/0	0	I0	0	I0•$\overline{Y}$n	Qn1	Qn1 ⊕ I1

X = Don't Care
Qn0 = Contents of Address n, Bit 0 (n = 0 to 7)
Qn1 = Contents of Address n, Bit 1

NOTES:
1. 1 (High) = Mismatch of Qn ⊕I, 0 (Low) = Match of Qn ⊕I
2. D0 = Q00 • $\overline{Y}$0 + Q10 • $\overline{Y}$1 + ••• + Q70 • $\overline{Y}$7
   D1 = Q01 • $\overline{Y}$0 + Q11 • $\overline{Y}$1 + ••• + Q71 • $\overline{Y}$7
3. Under normal operation, only one Y address is selected for read or write.
4. The write is transparent.
5. At all "matched" addresses there exists a simultaneous Associate and Write.

7

DESCRIPTION OF MODES OF OPERATION

The MC10H155 can be operated in any of the following modes: Read, Write, Associate, Masked Associate and Hybrid. Lines Y0–Y7 can be used as either inputs (a linear word select in the read/write mode) or as outputs (indicating match/mismatch in the associate mode).

Associate

Data present on the I0 and I1 inputs are compared with the latch outputs (Qn0, Qn1) of each cell. If the data input is at the same state as the latch output of a particular Y location, that Y-line goes low. Because these Y outputs are open emitters, expansion in multiples of 2 bits is obtained by tying additional MC10H155's to the Y-bus lines.

Masked Associate

This mode allows only the comparison of a single bit which is selected by bringing the corresponding A0- or A1-line high. The other bit is inhibited by holding the corresponding A0- or A1-line low.

Read

The particular cell output to be read is selected by bringing the associated Y-input low. Under normal operation only one cell is selected to be read, all Y-inputs of deselected cells must be held high. The state of the selected cell appears on outputs D0 and D1. In the case where more than one cell is selected, the outputs of these cells are OR-ed together and appear on the D0-, D1-outputs.

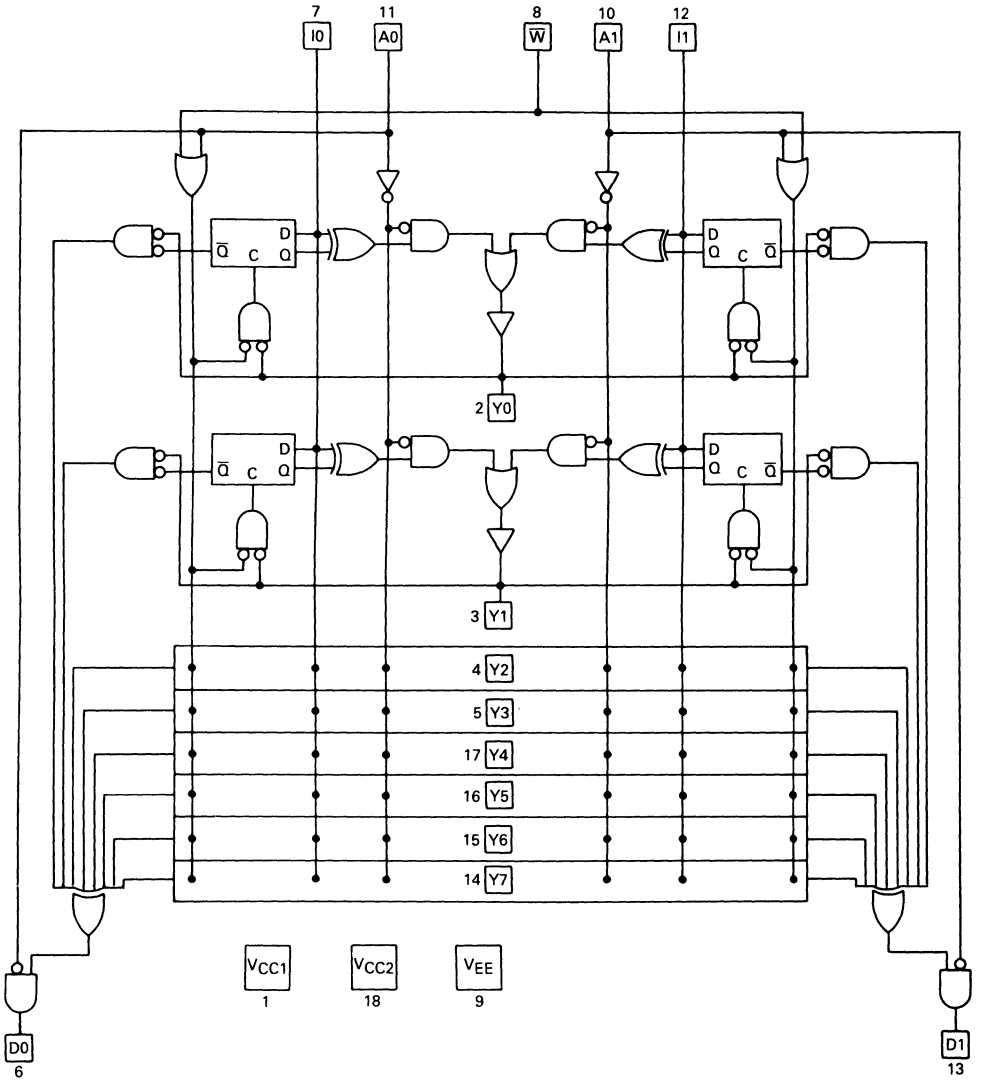
Write

In this mode data present at the I0-, I1-inputs is transferred to the latch outputs. Since the D0-, D1-outputs are transparent, they follow the state of these I0-, I1-inputs. The particular cells to be written into are selected by taking their respective Y-inputs low. All deselected cells, Y-inputs must be held high.

Hybrid

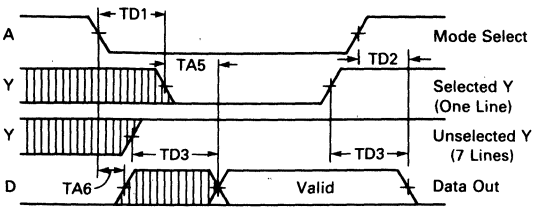
In this mode, only one of the I0- or I1-data inputs are associated with their respective latch outputs, Qn0 or Qn1. If a match exists, the corresponding Yn-line(s) will go low. As the Y-line goes low, this will address the other half of the memory for writing new data. Thus, when I0 matches Qn0, it is possible to write I1 in Qn1 or vice versa.

LOGIC DIAGRAM

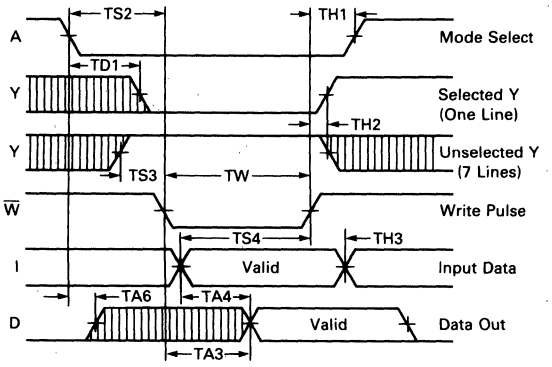


TIMING DIAGRAMS

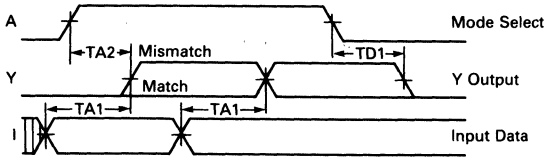
READ CYCLE



WRITE CYCLE



ASSOCIATE CYCLE



7

MCM10139

MECL

32 X 8 BIT PROGRAMMABLE READ-ONLY MEMORY

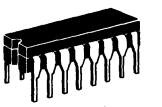
256-BIT PROGRAMMABLE READ ONLY MEMORY (PROM)

The MCM10139 is a 256-bit programmable read only memory (PROM). The circuit is organized as 32 words of 8 bits. Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The MCM10139 has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

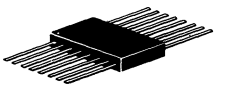
The MCM10139 is fully compatible with the MECL 10,000 logic family. It is designed for use in microprogramming, code conversion, logic simulation, and look-up table storage.

P_D = 520 mW typ/pkg (No Load)

t_{Access} = 15 ns typ (Address Inputs)

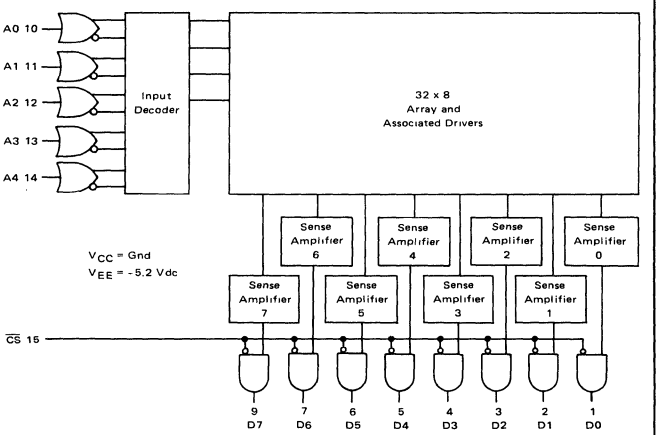


L SUFFIX
CERAMIC PACKAGE
CASE 620

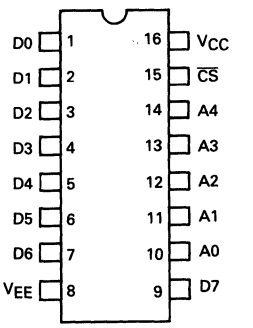


F SUFFIX
CERAMIC PACKAGE
CASE 650

LOGIC DIAGRAM



PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

	DC Test Voltage Values (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

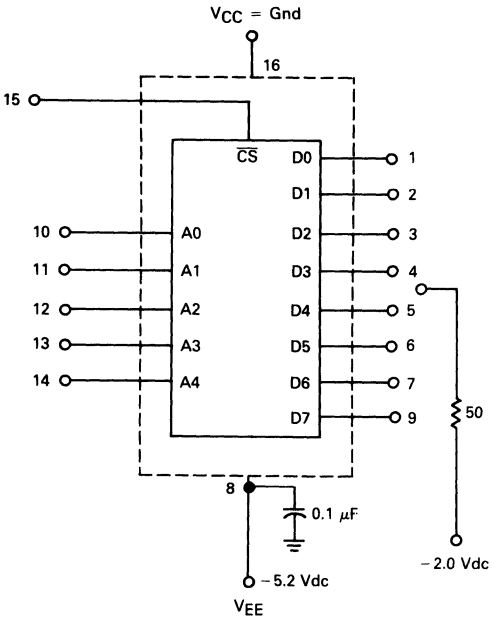
		MCM10139 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	150	—	145	—	140	mAdc	Typ I_{EE} @ 25°C = 100 mA. All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	—	265	—	265	—	265	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V.
Logic "0" Output Voltage	V_{OL}	-2,010	-1.665	-1.990	-1.650	-1.970	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	$V_{in} = V_{ILH}$ or V_{ILA}. Load 50 Ω to -2.0 V.

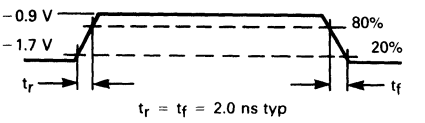
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ±5%; Output Load—See Figure 1 and Note 1)

		Test Limits				
Characteristic	Symbol	Min	Typ	Max	Unit	Conditions
Chip Select Access Time	t_{ACS}	—	10	15	ns	See Figures 2 and 3.
Chip Select Recovery Time	t_{RCS}	—	10	15	ns	Measured from 50% of input to 50%
Address Access Time	t_{AA}	—	15	20	ns	of output. See Note 2.
Output Rise and Fall Time	t_r, t_f	—	3.0	—	ns	Measured between 20% and 80% points.
Input Capacitance	C_{in}	—	4.0	5.0	pF	
Output Capacitance	C_{out}	—	7.0	8.0	pF	

Notes: 1. Contact your Motorola Sales Representative for details if extended temperature operation is desired.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the memory.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels.
All outputs loaded 50 ohms to −2.0 Vdc.

FIGURE 2 – CHIP SELECT ACCESS TIME

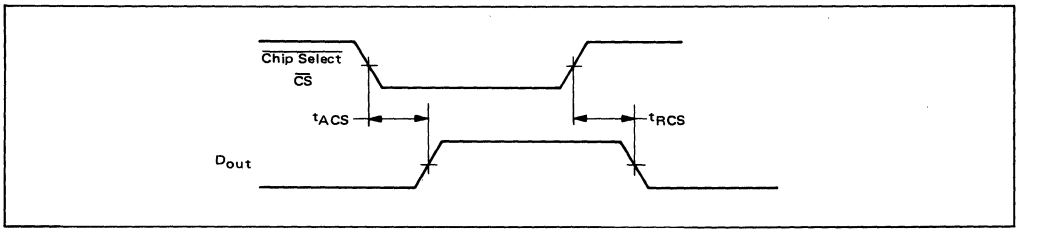
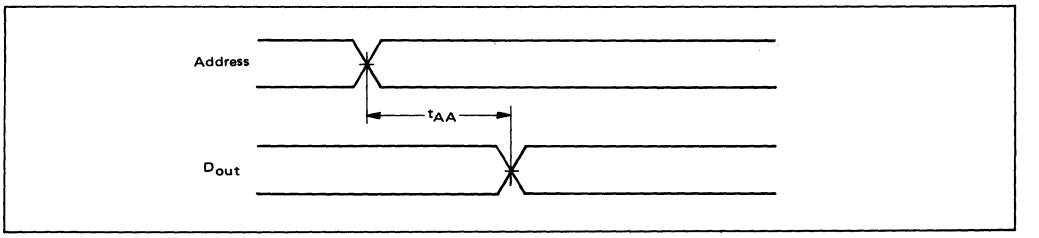


FIGURE 3 – ADDRESS ACCESS TIME



RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 4)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 5)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

7

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	—	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	—	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	—	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	—	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	—	—	—	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	—	1.0	ms	
Output Pulse Rise Time	—	—	—	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	—	1.0	ms	
Between Output Pulses	t_d1	0.01	—	1.0	ms	

NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

FIGURE 4 – MANUAL PROGRAMMING CIRCUIT

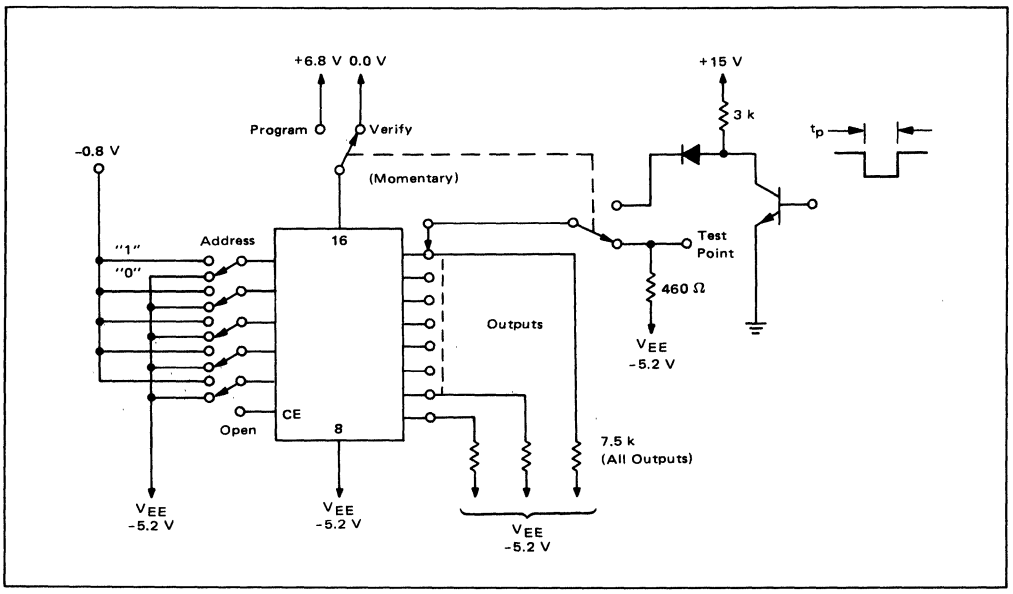
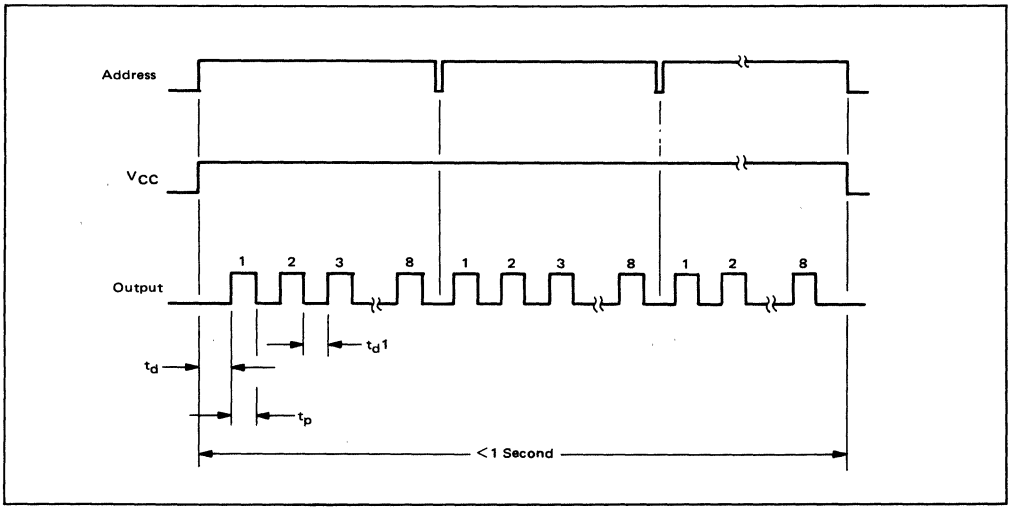


FIGURE 5 – AUTOMATIC PROGRAMMING CIRCUIT



7

MCM10143

MECL

8 x 2 MULTIPORT REGISTER FILE (RAM)

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MC10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

A write occurs on the positive to negative transition of the clock. Data is enabled by having the write enable (of each bit to be written) low when the clock transition is made. The written information is seen at the output on the negative to positive clock transition provided the read enable (of each bit) is at a low level. To inhibit a bit from being written, the write enable of that bit must be at a high level when the clock goes to a low state and must remain high until clock goes high. The operation of the clock and write enables can be reversed. While the clock is low, a positive to negative transition of the write enable will write into the bit addressed by A_0–A_2. The data is seen at the output on the negative to positive transition of the clock, provided the read enable is low.

READ

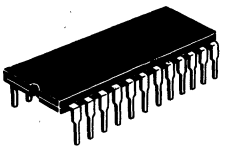
When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

t_{pd}:
CLock to Data out = 5 ns (typ)
(Read Selected)
Address to Data out = 10 ns (typ)
(Clock High)
Read Enable to Data out = 2.8 ns (typ)
(Clock high, Addresses present)
P_D = 610 mW/pkg (typ no load)

TRUTH TABLE

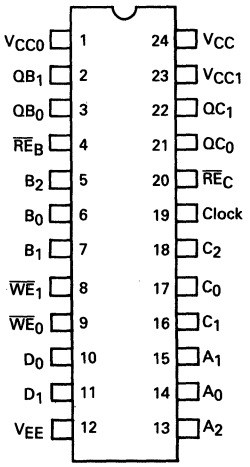
*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	H→L	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	L→H→L	H	H	ϕ	ϕ	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	L	H	L	H

**Note: Clock occurs sequentially through Truth Table
*Note. A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.
ϕ = Don't Care



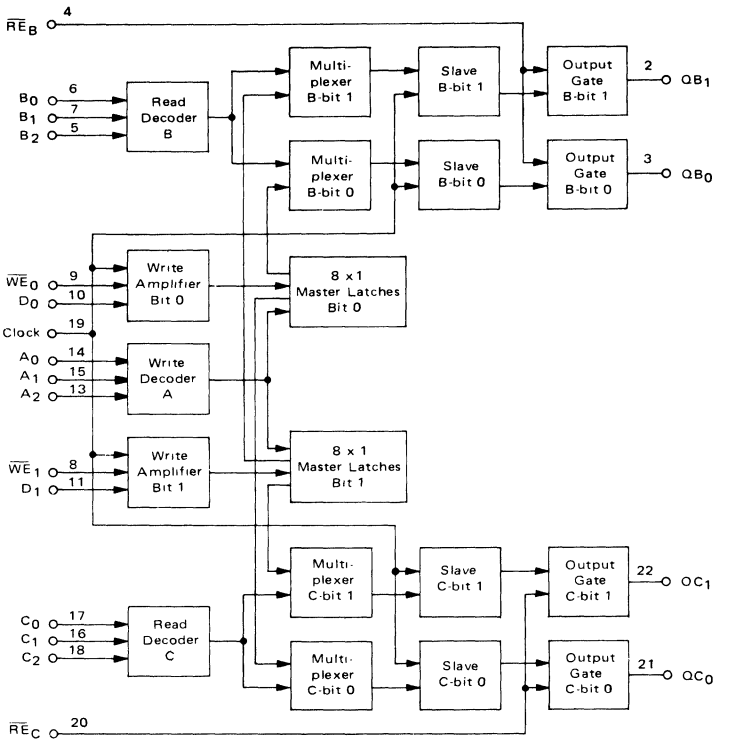
L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENT



7

BLOCK DIAGRAM



7

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ± 5%)

Characteristics	Symbol	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	–	150	–	118	150	–	150	mAdc
Input Current	I_{inH}								μAdc
Pins 10, 11, 19		–	245	–	–	245	–	245	
All other pins		–	200	–	–	200	–	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
Read Enable	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	–	–	8.5	5.5	–	–	–	
Hold									
Address	$t_{hold(Clock-B+)}$	–	–	-1.5	-4.5	–	–	–	
Write Mode									
Setup									
Write Enable	$t_{setup(\overline{WE}-Clock+)}$	–	–	7.0	4.0	–	–	–	
Write Disable	$t_{setup(\overline{WE}+Clock-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{setup(A-Clock+)}$	–	–	8.0	5.0	–	–	–	
Data	$t_{setup(D-Clock+)}$	–	–	5.0	2.0	–	–	–	
Hold									
Write Enable	$t_{hold(Clock-\overline{WE}+)}$	–	–	5.5	2.5	–	–	–	
Write Disable	$t_{hold(Clock+\overline{WE}-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{hold(Clock+A+)}$	–	–	1.0	-3.0	–	–	–	
Data	$t_{hold(Clock+D+)}$	–	–	1.0	-2.0	–	–	–	
Write Pulse Width	$PW_{\overline{WE}}$	–	–	8.0	5.0	–	–	–	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

①AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS

Access (Clock High)

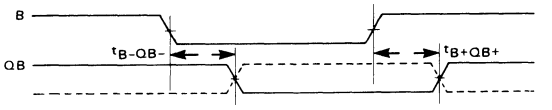


FIGURE 1

Enable

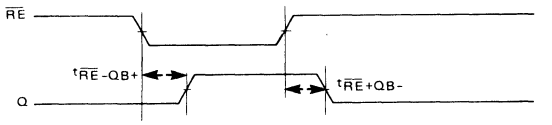


FIGURE 2

Data (Address Selected)

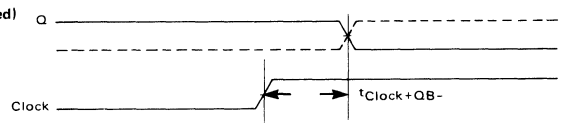


FIGURE 3

Setup and Hold

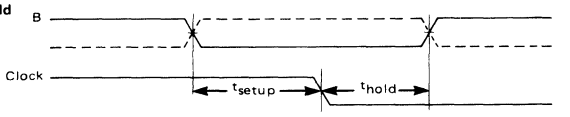


FIGURE 4

WRITE TIMING DIAGRAM

Enable Setup

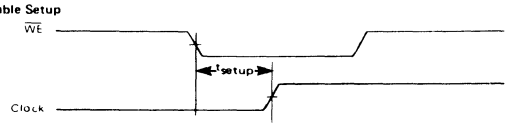


FIGURE 5

Enable Hold

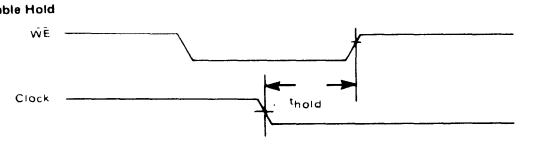


FIGURE 6

Disable

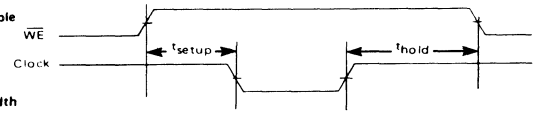


FIGURE 7

Pulse Width

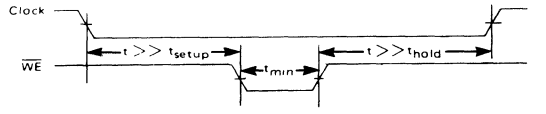


FIGURE 8

Address

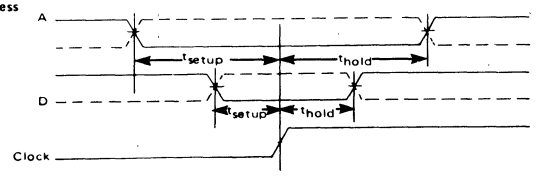


FIGURE 9

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MCM10144

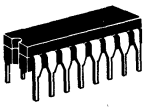
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10144 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 17 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Pin-for-Pin Replacement for F10410

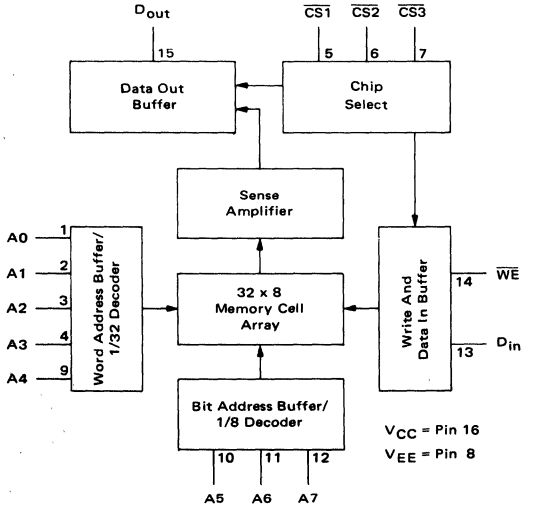
MECL

256 X 1-BIT RANDOM ACCESS MEMORY

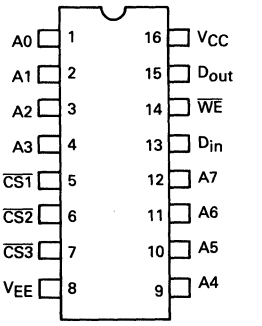


L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10144 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

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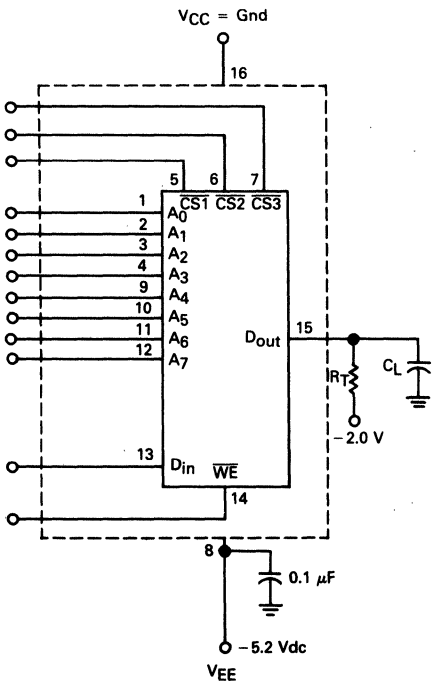
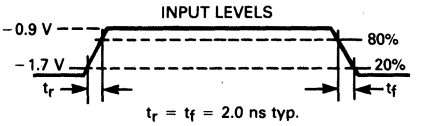
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	10	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	10	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	17	26	ns	
Write Mode						
Write Pulse Width	t_W	25	6.0	–	ns	t_{WSA} = 8.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-3.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	0.0	-4.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	10	ns	
Write Recovery Time	t_{WR}	2.5	5.0	10	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	7.0	ns	When driven from Address inputs.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f$ = 2.0 ns typ.

All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

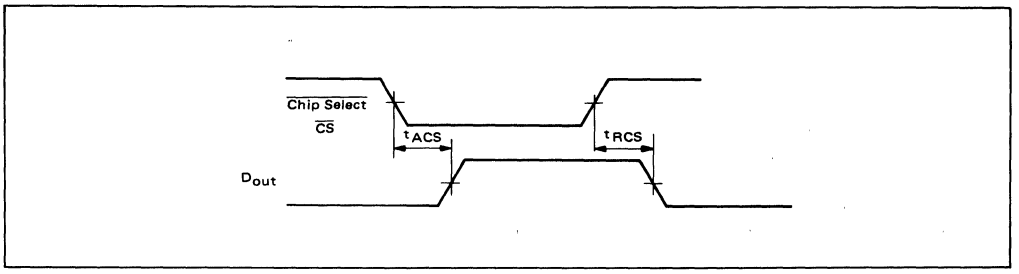


FIGURE 3 – ADDRESS ACCESS TIME

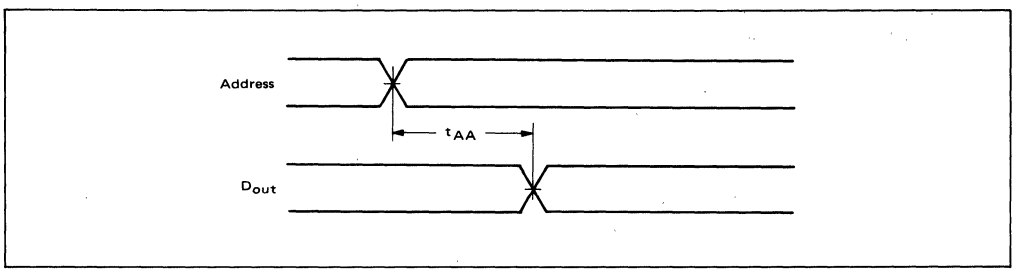
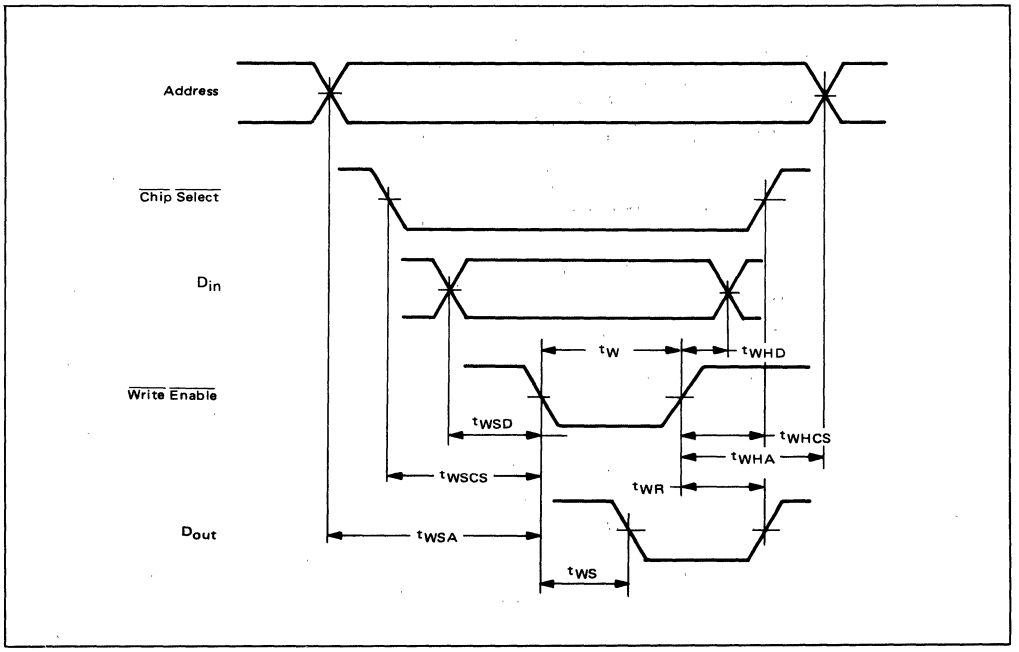


FIGURE 4 – WRITE MODE



7

MCM10145

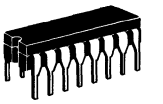
64-BIT REGISTER FILE (RAM)

The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MCM10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Select input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Select, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- Operating Temperature Range = 0° to +75°C
- 50 kΩ Pulldown Resistors on All Inputs
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the F10145

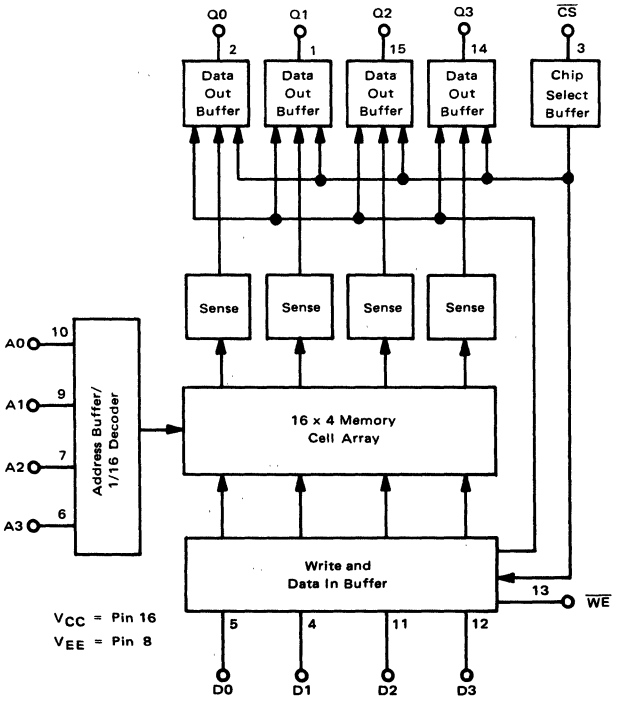
MECL

64-BIT REGISTER FILE (RAM)

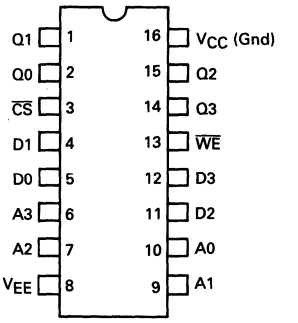


L SUFFIX
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A3	Address Inputs
D0 thru D3	Data Inputs
Q0 thru Q3	Data Outputs
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	CS	WE	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 thru A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DC Characteristics	Symbol	MCM10145 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	-	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

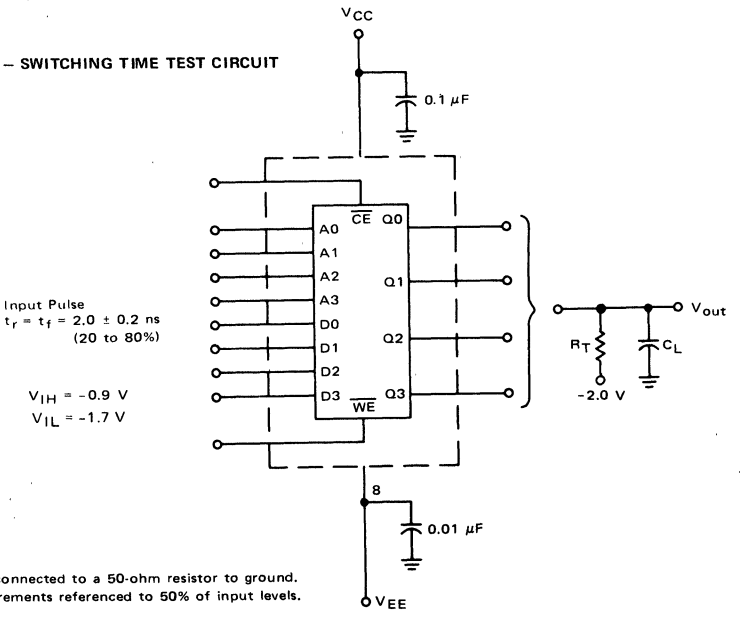
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ±5°; Output Load see Figure 1; see Note 2.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.5	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 1.
Address Access Time	t_{AA}	4.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	–	–	ns	t_{WSA} = 5 ns
Data Setup Time Prior to Write	t_{WSD}	0	-6.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	3.0	0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	1.0	–	ns	t_W = 8 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	1.0	-3.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	0	-6.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	
Chip Enable Strobe Mode						
Data Setup Prior to Chip Select	t_{CSD}	0	-6.0	–	ns	Guaranteed but not tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	-3.0	–	ns	product. See Figure 5.
Address Setup Prior to Chip Select	t_{CSA}	0	-3.0	–	ns	
Data Hold Time After Chip Select	t_{CHD}	2.0	-1.0	–	ns	
Write Enable Hold Time After Chip Select	t_{CHW}	0	-6.0	–	ns	
Address Hold Time After Chip Select	t_{CHA}	4.0	-1.0	–	ns	
Chip Select Minimum Pulse Width	t_{CS}	18	12	–	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Address to Output	t_r, t_f	1.5	3.0	7.0	ns	
$\overline{CS}$ to Output	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	6.0	pF	
Output Capacitance	C_{out}	–	5.0	8.0	pF	

Notes:
1. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
2. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

7

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



Unused outputs connected to a 50-ohm resistor to ground.
All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (Including Jig and Stray Capacitance)
Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

FIGURE 2 – CHIP SELECT ACCESS TIME

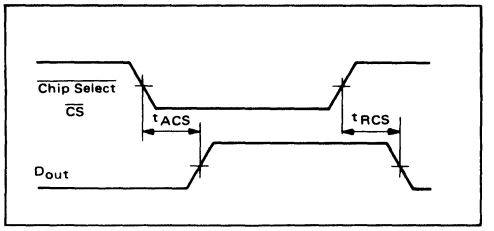


FIGURE 3 – ADDRESS ACCESS TIME

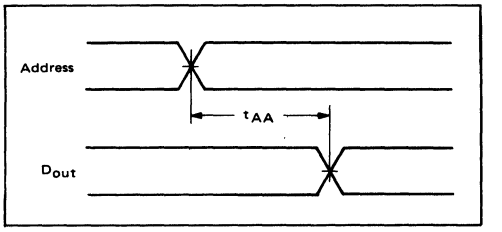


FIGURE 4 – WRITE MODE

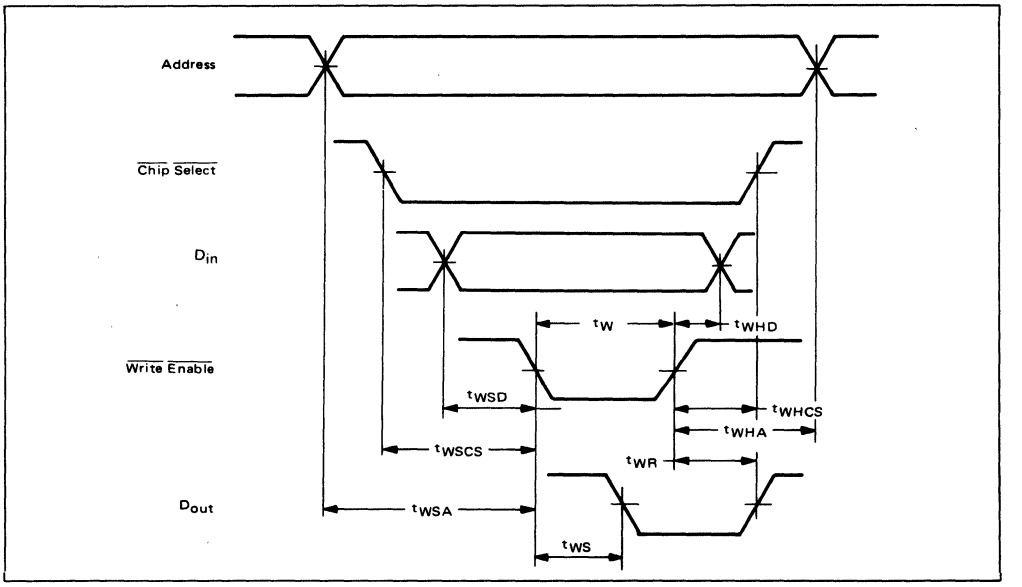
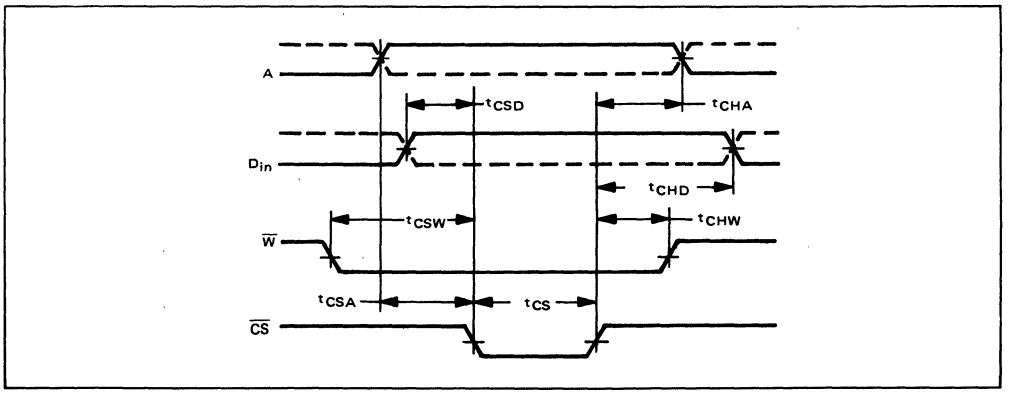


FIGURE 5 – CHIP ENABLE STROBE MODE



7

MCM10146

1024 x 1-BIT RANDOM ACCESS MEMORY

The MCM10146 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

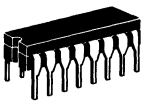
- Fully Compatible with MECL 10,000
- Temperature Range of 0° to 75°C (see note 1)
- Emitter-Follower Output Permits Full Wire-ORing (see note 3)
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns

PIN DESIGNATION

$\overline{CS}$	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
$\overline{WE}$	Write Enable Input

MECL

1024 X 1-BIT RANDOM ACCESS MEMORY



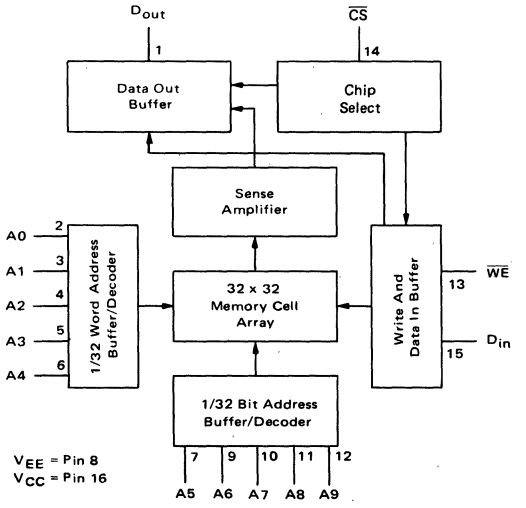
L SUFFIX
CERAMIC PACKAGE
CASE 620

ORDERING INFORMATION

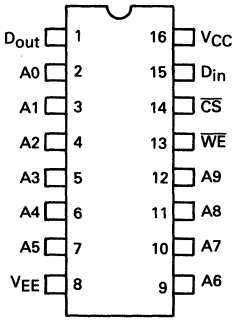
Suffix Denotes

MCM10146 – L Ceramic Dual-In-Line Package
– F Ceramic Flat Package

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

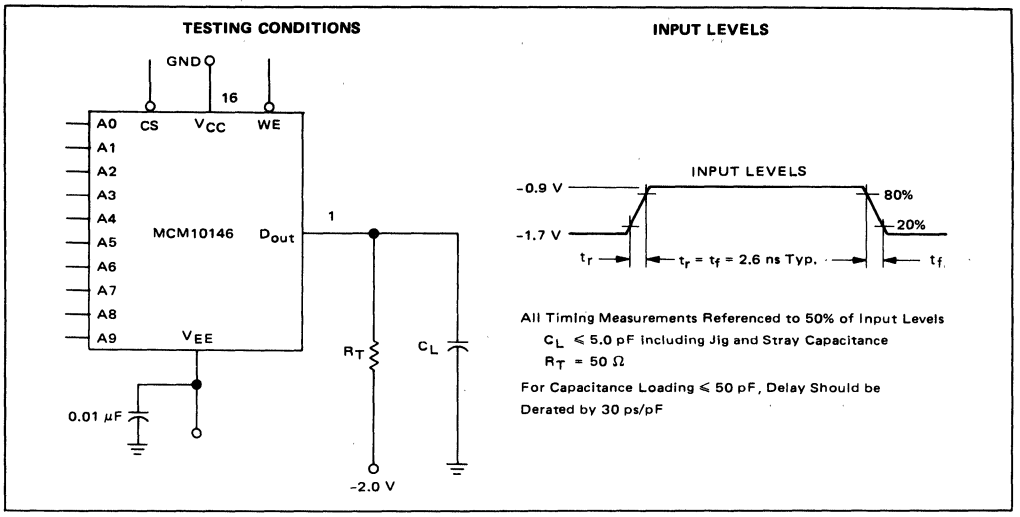
	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10146 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	150	–	145	–	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10146 Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.0	ns	See Note 2.
Address Access Time	t_{AA}	8.0	24	29	ns	
Write Mode						See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	20	–	ns	t_{WSA} = 8.0 ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns
Address Hold Time After Write	t_{WHA}	2.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	0	–	ns	
Write Disable Time	t_{WS}	2.8	5.0	7.0	ns	
Write Recovery Time	t_{WR}	2.8	5.0	7.0	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	2.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	8.0	ns	When driven from Address inputs.
Capacitance						Measured with a pulse technique.
Input Lead Capacitance	C_{in}	–	4.0	5.0	pF	
Output Lead Capacitance	C_{out}	–	7.0	8.0	pF	

Notes:

(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

(4) Typical limits are at V_{EE} = -5.2 Vdc, T_A = 25°C and standard loading.

FIGURE 2 – CHIP SELECT ACCESS TIME

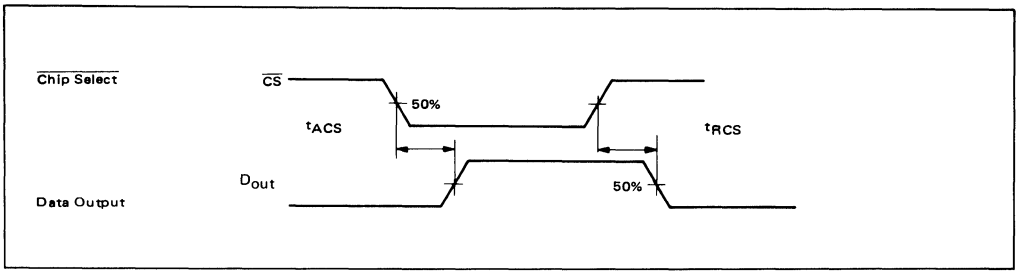


FIGURE 3 – ADDRESS ACCESS TIME

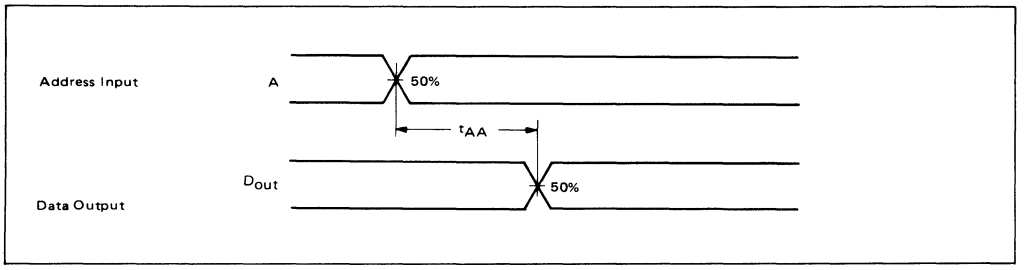
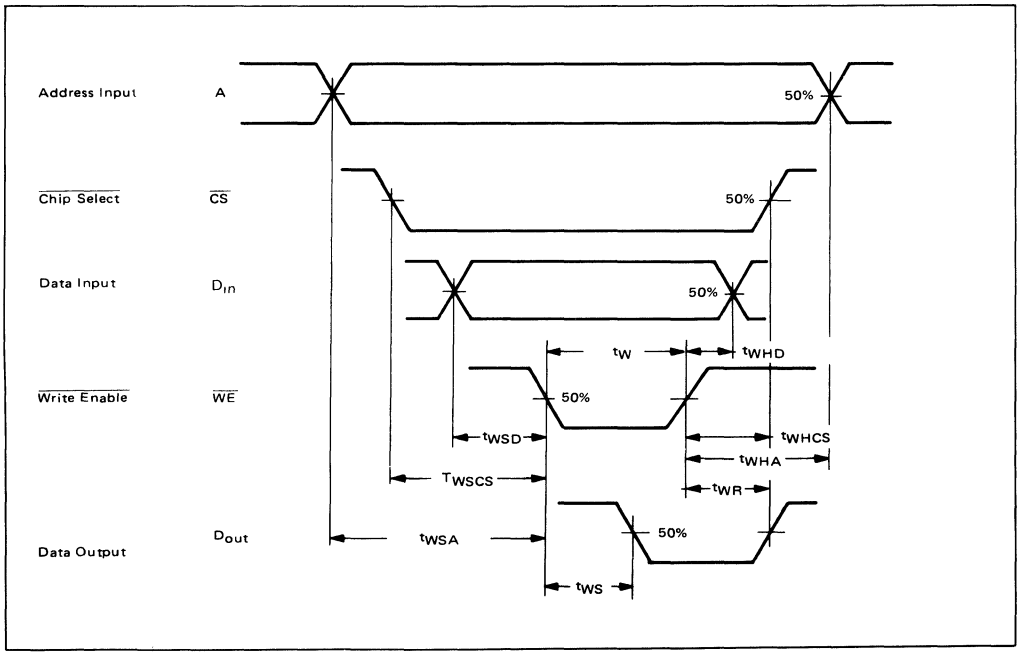


FIGURE 4 – WRITE STROBE MODE



7

MCM10147

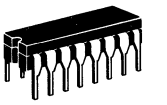
128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10147 is a 128-word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of a 7-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 2 active-low chip select lines. It has a typical access time of 10 ns and is designed for high-speed scratch pads, control, cache, and buffer storage applications.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 5.0 ns
- Operating Temperature Range = 0^{o} to $+75^{o}C$
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Similar to F10405.

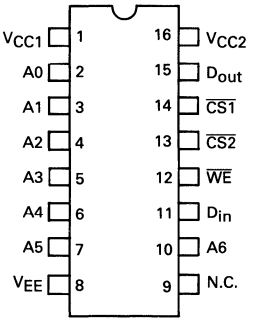
MECL

128-BIT RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620

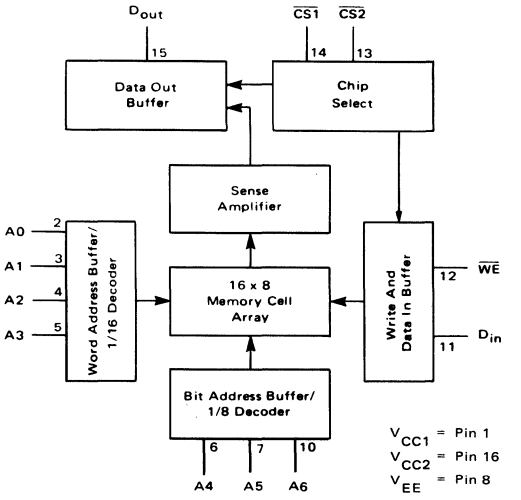
PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A6	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

BLOCK DIAGRAM



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM 10147 is a 128 word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address A0 thru A6.

The active-low chip select allows memory expansion up to 512 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	105	–	100	–	95	mAdc	Typ I_{EE} @ 25°C = 80 mA All outputs and inputs open. Measure pin 8.
Input Current High	I_{inH}	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	I_{inL}	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

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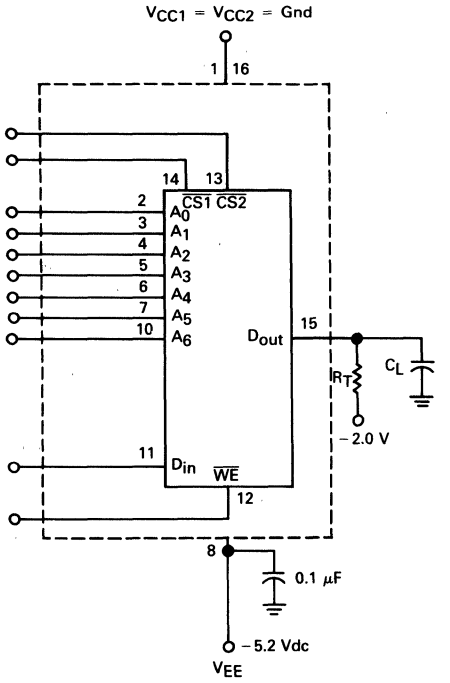
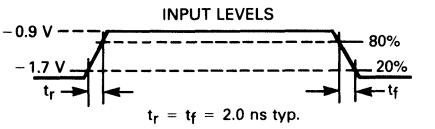
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	5.0	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 2.
Address Access Time	t_{AA}	5.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	6.0	–	ns	t_{WSA} = 4.0 ns
Data Setup Time Prior to Write	t_{WSD}	1.0	-5.0	–	ns	
Data Hold Time After Write	t_{WHD}	3.0	-2.0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	4.0	0	–	ns	t_W = 8.0 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	1.0	-5.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	Measured at 50% of input to 50%
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	of output.
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f$ = 2.0 ns typ.

All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

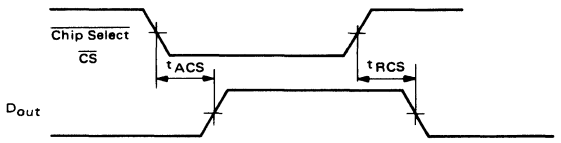


FIGURE 3 – ADDRESS ACCESS TIME

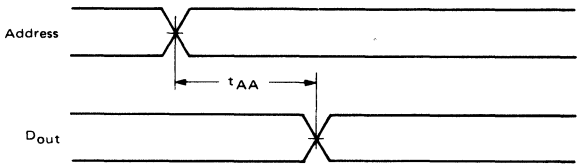
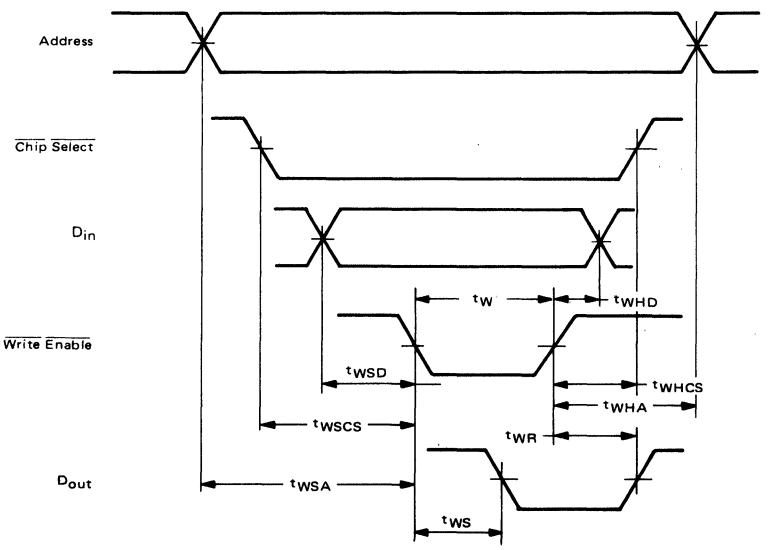


FIGURE 4 – WRITE MODE



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MCM10148

64 X 1 BIT RANDOM ACCESS MEMORY

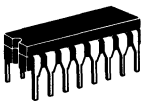
The MCM10148 is a fast 64-word X 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance. The operating mode (CS inputs low) is controlled by the WE input. With WE low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With WE high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- 50 kΩ Input Pulldown Resistors (420 mW typ) on All Inputs

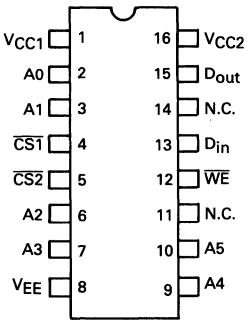
MECL

64 X 1-BIT
RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620

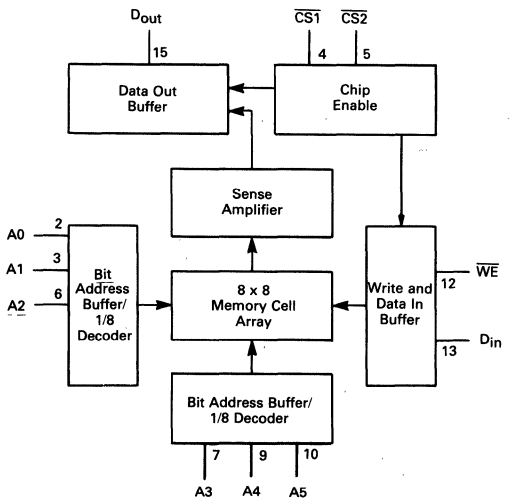
PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A6	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

BLOCK DIAGRAM



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	X	X
Disabled	H	X	X	L

*$\overline{CS}$ = $\overline{CS1}$ + $\overline{CS2}$
X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	—	105	—	100	—	95	mAdc
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10148 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5%		Unit	Conditions
		Min	Max		
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	—	7.5		
Chip Select Recovery Time	t_{RCS}	—	7.5		
Address Access time	t_{AA}	—	15		
Write Mode				ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	—		
Data Setup Time Prior to Write	t_{WSD}	3.0	—		
Data Hold Time After Write	t_{WHD}	2.0	—		
Address Setup Time Prior to Write	t_{WSA}	5.0	—		
Address Hold Time After Write	t_{WHA}	3.0	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	—		
Chip Select Hold Time After Write	t_{WHCS}	0	—		
Write Disable Time	t_{WS}	2.0	7.5		
Write Recovery Time	t_{WR}	2.0	7.5		
Rise and Fall Time	t_r, t_f	1.5	5.0	ns	Measured between 20% and 80% points.
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50Ω, MCM10148.
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

7

MCM10149*10

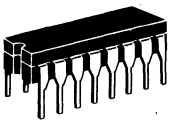
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 7.0 ns
- Typical Chip Select Access Time of 2.5 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (740 mW typ @ 25°C) Decreases with Increasing Temperature

MECL

1024-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620

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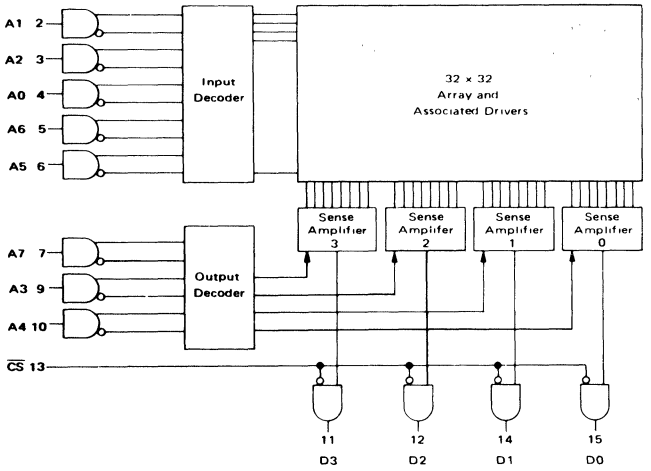
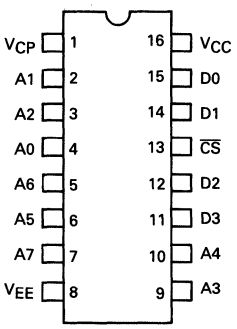


PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS①

Characteristic	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	175	–	170	–	165	mAdc
Input Current High	I_{inH}	–	265	–	265	–	265	μAdc

Forcing Function	Parameter	0°C	25°C②	75°C②
V_{IHmax} =	V_{OHmax}	−0.840	−0.810	−0.720
	V_{OHmin}	−1.000	−0.960	−0.900
	V_{OHAmin}	−1.020	−0.980	−0.920
V_{IHAmin}		−1.130	−1.105	−1.045
V_{ILAmax}		−1.490	−1.475	−1.450
	V_{OLAmax}	−1.645	−1.630	−1.605
	V_{OLmax}	−1.665	−1.650	−1.625
V_{ILmin} =	V_{OLmin}	−1.870	−1.850	−1.830
V_{ILmin}	I_{NLmin}	0.5	0.5	0.3

NOTES: ① The MCM10149*10 is designed to meet the dc specifications in the electrical characteristics tables after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear FPM is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.
② 0–75°C temperature range, 50 Ω to −2.0 V.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	T_A = 0 to 75°C, V_{EE} = −5.2 Vdc ±5%			Unit	Conditions
		Min	Typ	Max		
Read Mode					ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	1.0	3.0	5.0		
Chip Select Recovery Time	t_{RCS}	1.0	3.0	5.0		
Address Access Time	t_{AA}	3.0	7.0	10		
Rise and Fall Time	t_r, t_f	1.0	2.0	5.0	ns	Measured between 20% and 80% points.
Capacitance					pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	—	5.0		
Output Capacitance	C_{out}	—	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. V_{CP} = V_{CC} = Gnd for normal operation.

PROGRAMMING THE MCM10149*10

During programming of the MCM10149*10, input Pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input Pins 2, 3, 4, 5, and 6 are addressed with 0 V $\leq V_{IH} \leq$ +0.25 V and $V_{EE} \leq V_{IL} \leq$ −3.0 V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with V_{CP} = V_{CC} = 0 V and V_{EE} = −5.2 V ±5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to +10 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 15.2 V, +10 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at +10 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ±5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of +2.85 V ±5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to −2.0 V. Current into the selected output is 5 mA maximum.

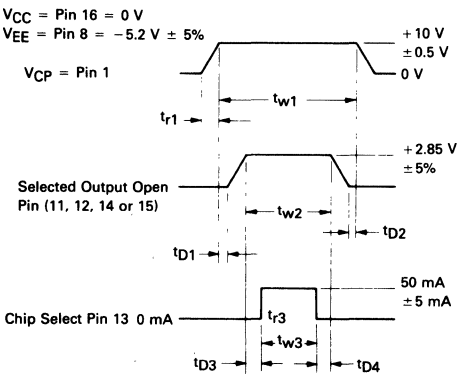
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ±5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned to 0 mA, the bit select pulse is returned to its initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149*10.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ⩽ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	⩾ 1 μs
t_{w1}	Pulse Width, Programming Voltage	⩾ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	⩾ 0
t_{w2}	Pulse Width, Bit Select	⩾ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	⩾ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	⩾ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	⩾ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	⩾ 1 μs

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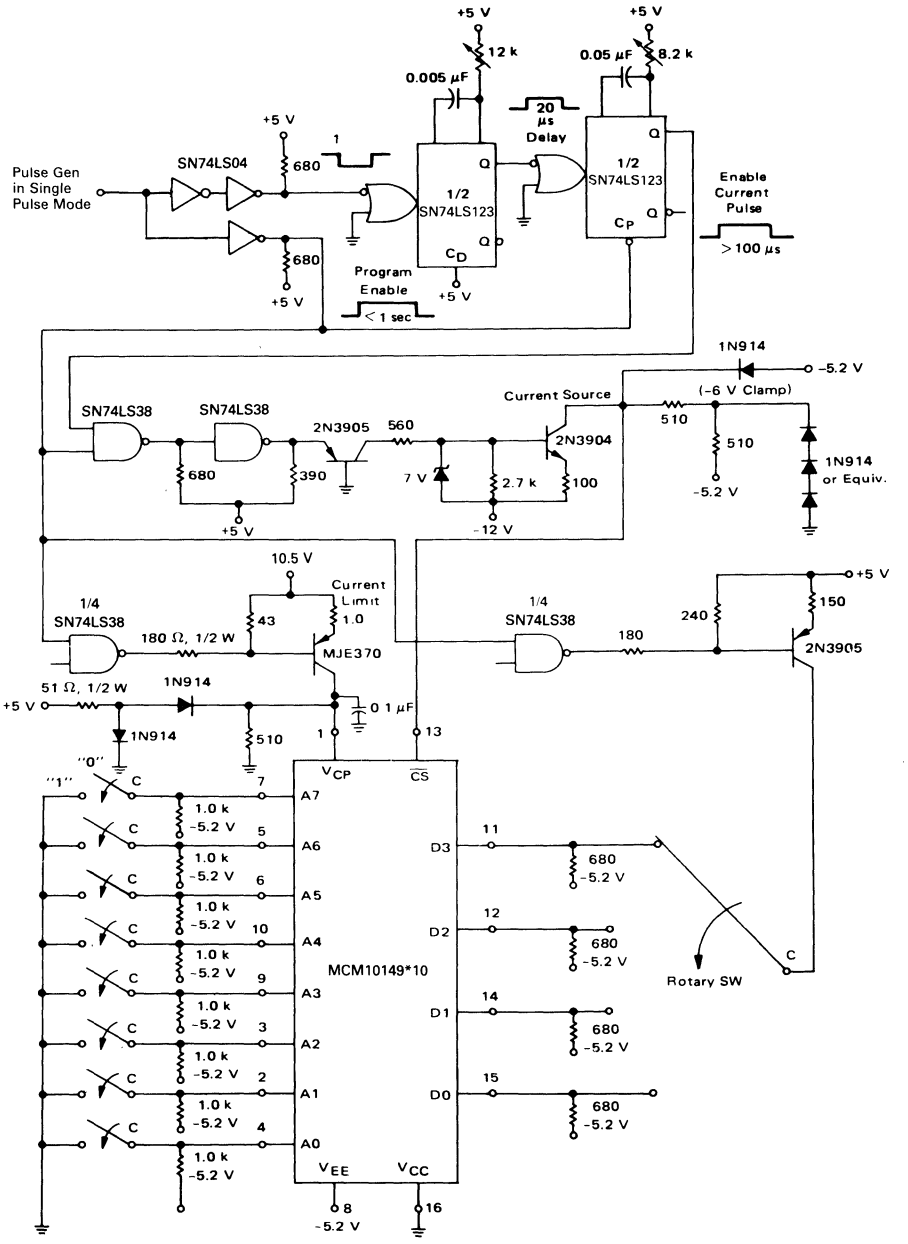
MANUAL PROGRAMMING CIRCUIT



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MCM10149*25

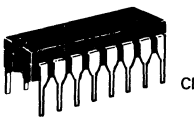
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature

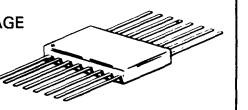
MECL

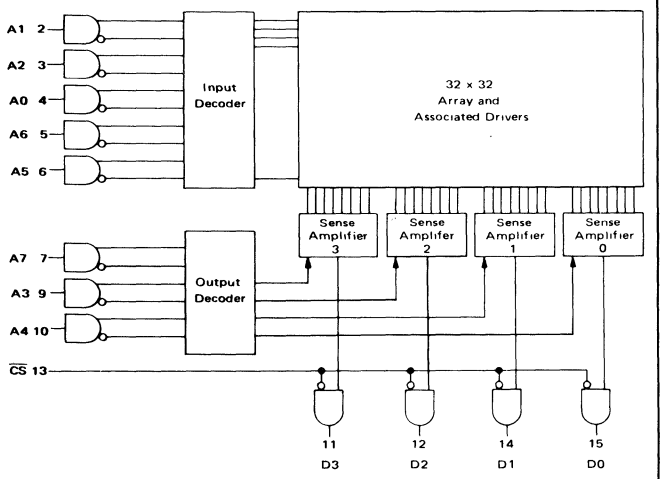
1024-BIT PROGRAMMABLE READ-ONLY MEMORY



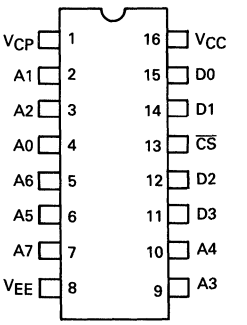
L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650





PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	mAdc
Input Current High	I_{inH}	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only

Forcing Function		Parameter	0°C	25°C①	75°C①
V_{IHmax}	=	V_{OHmax}	−0.840	−0.810	−0.720
		V_{OHmin}	−1.000	−0.960	−0.900
		V_{OHAmin}	−1.020	−0.980	−0.920
V_{IHAmin}			−1.130	−1.105	−1.045
V_{ILAmax}			−1.490	−1.475	−1.450
		V_{OLAmax}	−1.645	−1.630	−1.605
		V_{OLmax}	−1.665	−1.650	−1.625
V_{ILmin}	=	V_{OLmin}	−1.870	−1.850	−1.830
V_{ILmin}		I_{NLmin}	0.5	0.5	0.3

NOTES: ① 0–75°C temperature range, 50Ω to -2.0V.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149*25 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max		
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10		
Address Access Time	t_{AA}	7.0	25		
Rise and Fall Time	t_r, t_f	1.5	7.0	ns	Measured between 20% and 80% points.
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149;
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined, contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 V \leq V_{IH} \leq +0.25$ V and $V_{EE} \leq V_{IL} \leq -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC} =$ 0 V and $V_{EE} = -5.2$ V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of – 5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of + 2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to – 2.0 into the selected

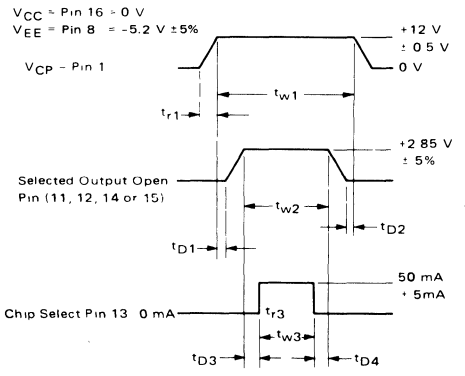
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be – 6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to – 2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ⩽ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	⩾ 1 μs
t_{w1}	Pulse Width, Programming Voltage	⩾ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	⩾ 0
t_{w2}	Pulse Width, Bit Select	⩾ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	⩾ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	⩾ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	⩾ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	⩾ 1 μs

FOR MANUAL PROGRAMMING CIRCUIT, SEE MCM10149*10

MCM10152

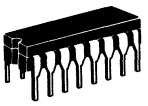
MECL

256 X 1-BIT RANDOM ACCESS MEMORY

256 x 1-BIT RANDOM ACCESS MEMORY

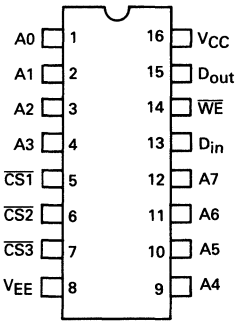
The MCM10152 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 11 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0^{o} to $+75^{o}C$
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family



L SUFFIX
CERAMIC PACKAGE
CASE 620

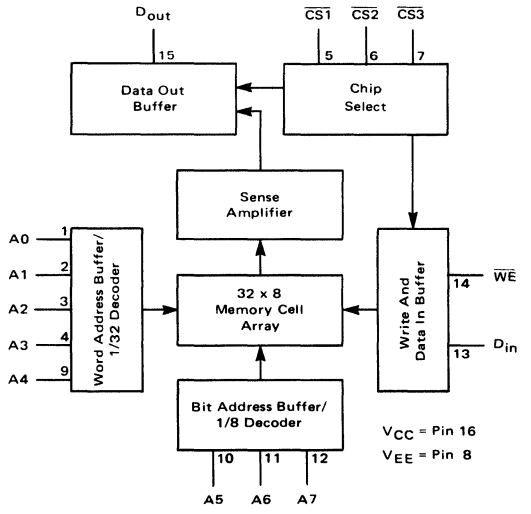
PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

BLOCK DIAGRAM



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

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FUNCTIONAL DESCRIPTION:

The MCM10152 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

		MCM10152 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	mAdc	Typ I_{EE} @ 25°C = 110 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

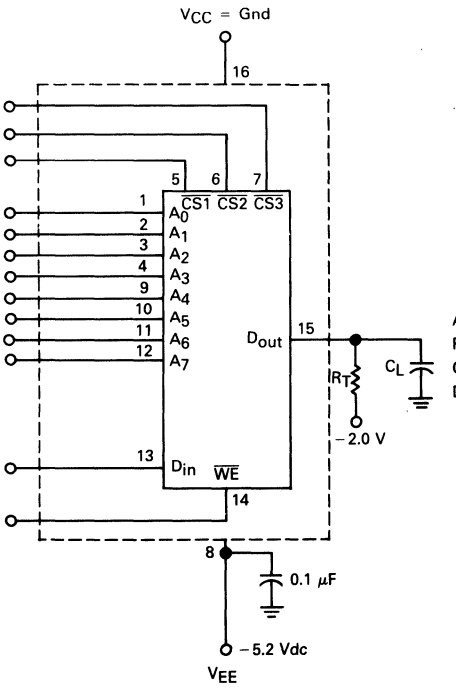
Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.5	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.5	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	11	15	ns	
Write Mode						
Write Pulse Width	t_W	10	6.0	–	ns	t_{WSA} = 5.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-2.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	3.0	–	ns	t_W = 10 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	7.5	ns	
Write Recovery Time	t_{WR}	2.5	5.0	7.5	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

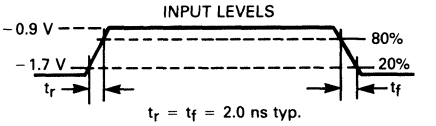
Notes. (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels.

R_T = 50 Ω

$C_L \leq$ 5.0 pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

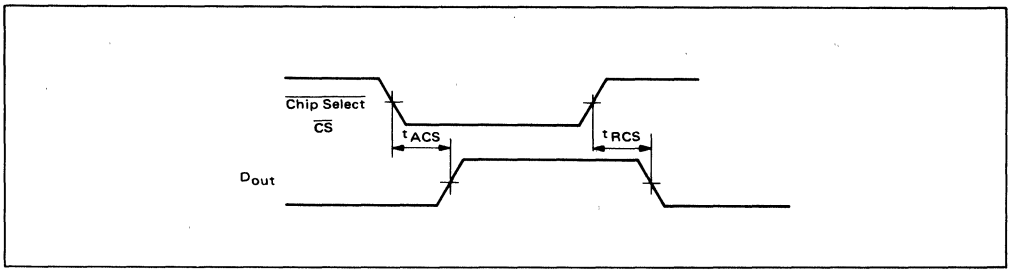


FIGURE 3 – ADDRESS ACCESS TIME

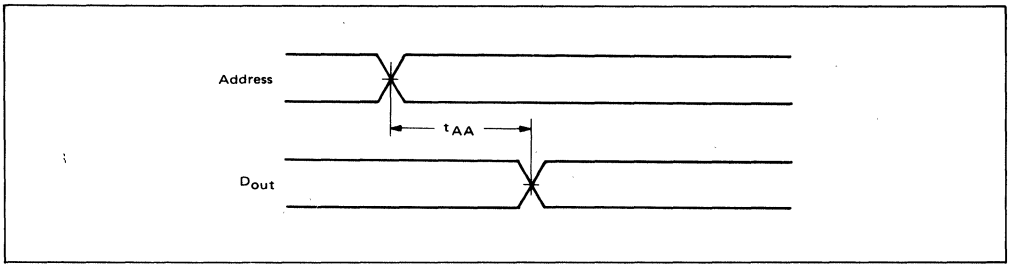
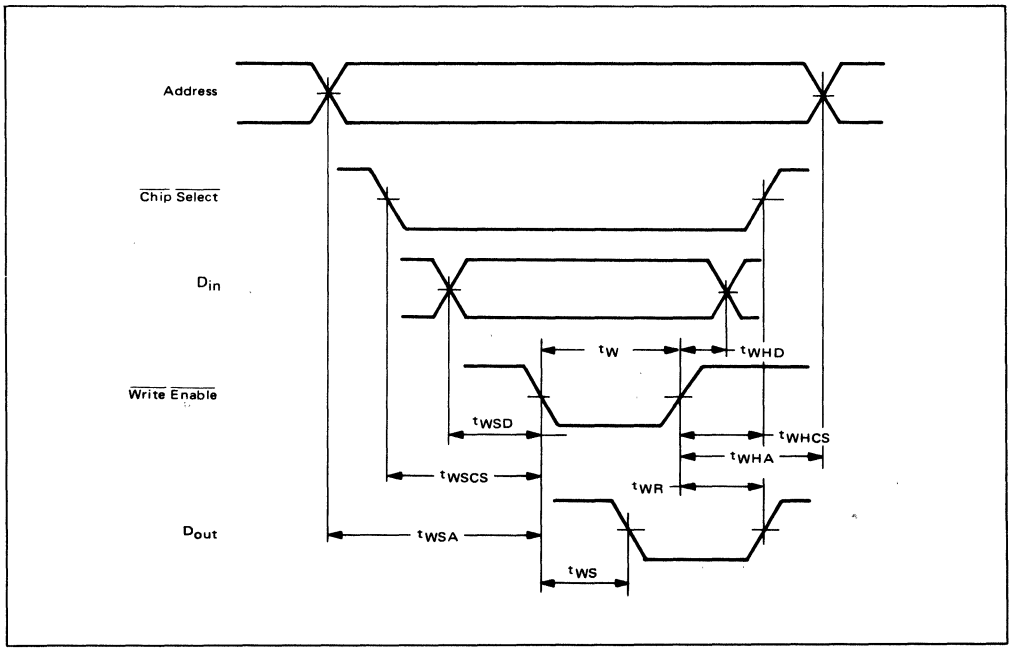


FIGURE 4 – WRITE MODE



7

Military Products 8

CMOS Static RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
4K×4	6168-55/BRAJC	55	20
	6168-55/BUAJC	55	20
	6168-70/BRAJC	70	20
	6168-70/BUAJC	70	20
	6268-35/BRAJC	35	20
	6268-35/BUAJC	35	20
	6268-45/BRAJC	45	20
	6268-45/BUAJC	45	20
8K×8	6164-55/BXAJC	55	28
	6164-55/BUAJC	55	32
	6164-70/BXAJC	70	28
	6164-70/BUAJC	70	32
16K×4	6288-35/BXAJC	35	22
	6288-35/BUAJC	35	22
	6288-45/BXAJC	45	22
	6288-45/BUAJC	45	22
64K×1	6287-35/BXAJC	35	22
	6287-35/BUAJC	35	22
	6287-45/BXAJC	45	22
	6287-45/BUAJC	45	22
32K×8	6206-45/BXAJC*	45	28
	6206-55/BXAJC*	55	28
	6206-70/BXAJC*	70	28

CMOS Cache Tag RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
4K×4	4180-35/BXAJC*	35	22
	4180-45/BXAJC*	45	22

*To be introduced

TTL RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
256K×4	93422/BWAJC	60	22
	93L422/BWAJC	75	22
	93L422A/BWAJC	55	22
1024×1	93415/BEAJC	45	16
	93415/BFAJC	45	16
	93425/BEAJC	45	16
	93425/BFAJC	45	16

*To be introduced

8

Military 4180

Advance Information

4K x 4 Bit Cache Address Tag Comparator

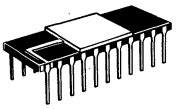
The 4180 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's second generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates a 4K x 4 SRAM core with an on-board comparator for efficient implementation of a cache memory.

The device has a $\overline{CLR}$ pin for flash clear of the RAM, useful for system initialization.

The 4180 compares RAM contents with current input data. The result is either an active high match level for a cache hit, or an active low level for a cache miss.

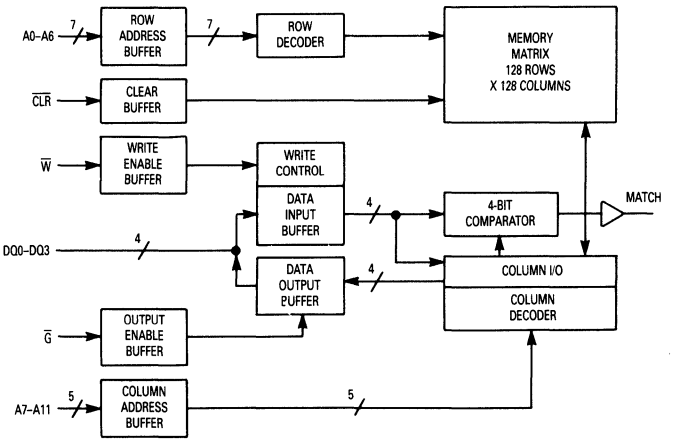
The 4180 is available in 22 lead sidebraze packages.

- Single 5.0 V ±10% Supply
- Fast Address to Match Time: 35/45 ns Max
- Fast Data to Match Time: 15/20 ns Max
- Fast Read of Tag RAM Contents: 35/45 ns Max
- Flash Clear of the Tag RAM ($\overline{CLR}$ Pin)
- Pin and Function Compatible with MK41H80

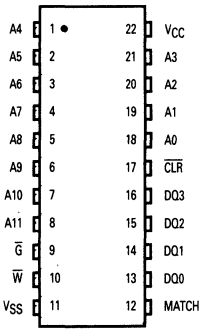


CASE 677-06
CERAMIC

BLOCK DIAGRAM



PIN ASSIGNMENT
SIDEBRAZE



PIN NAMES

A0–A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{CLR}$	Flash Clear Input
MATCH	Match (Hit) Output
DQ0–DQ3	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground
NC	No Connection

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{W}$	$\overline{G}$	$\overline{CLR}$	DQ0–DQ3	Match	Mode
H	H	H	Compare D_{in}	Valid	Compare
L	X	H	D_{in}	Assert	Write
H	L	H	D_{out}	Assert	Read
X	X	L	High-Z	Assert	Clear

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}/V_{out}	−0.5 to V_{CC} +0.5	V
Output Current — Match Output I/O Pins, Per I/O	I_{out}	40 20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Temperature Under Bias	T_{bias}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −55° to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3.0 Vac (pulse width ≤ 20 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg}(I)$	—	±1.0	μA
Output Leakage Current, Except Match Output ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg}(O)$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA, t_{AVAV} = t_{AVQV} max)	I_{CCA}	—	140*	mA
Output Low Voltage (I/O Pins: I_{OL} = 8.0 mA, Match Output: I_{OL} = 12 mA)	V_{OL}	—	0.4	V
Output High Voltage (I/O Pins: I_{OH} = −4.0 mA, Match Output: I_{OH} = −10 mA)	V_{OH}	2.4	—	V

*I_{CC} active current for the clear cycle exceeds this specification. However, this is a transient phenomenon and will not affect the power dissipation of the device. Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4.0	5.0	pF
I/O Capacitance	C_{out}	5.0	7.0	pF
Match Output Capacitance	C_{match}	6.0	7.0	pF

Military 6164

8K x 8-Bit Fast Static Random Access Memory

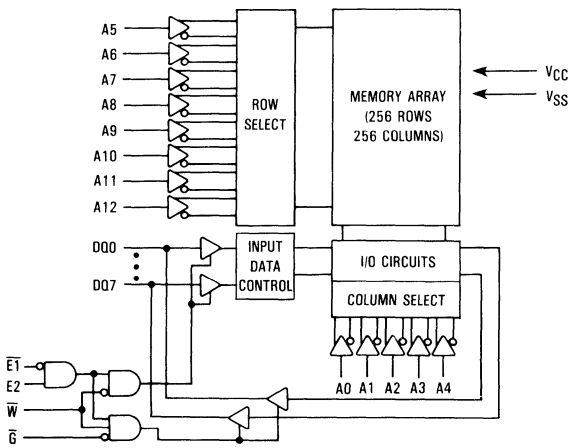
The 6164 is a 65,536-bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

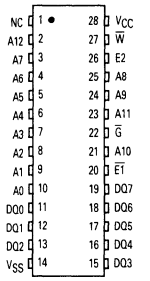
The 6164 is available in a 600 mil, 28-pin ceramic dual-in-line package, and a 32-terminal ceramic LCCC with JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 55, 70 ns (Maximum)
- Low Power Dissipation — 660, 495 mW (Maximum, Active)
- Fully TTL Compatible
- Three-State Data Outputs
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

BLOCK DIAGRAM

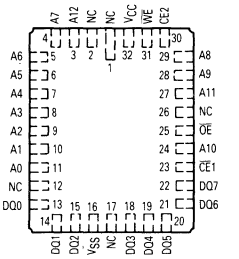


PIN ASSIGNMENT



CASE 733-04
CERAMIC

CHIP CARRIER



CASE 766A-01
CERAMIC

PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

8

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	IIL	—	2	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	IOZL	—	2	μA
Operating Supply Current Cycle = Min, Duty = 100% +25, +125°C −55°C	I_{CCA}	— —	90 120	mA
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	2	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)	I_{SB2}	—	0.9	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	—	5	10	pF
Input/Output Capacitance	DQ	$C_{I/O}$	—	6	12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

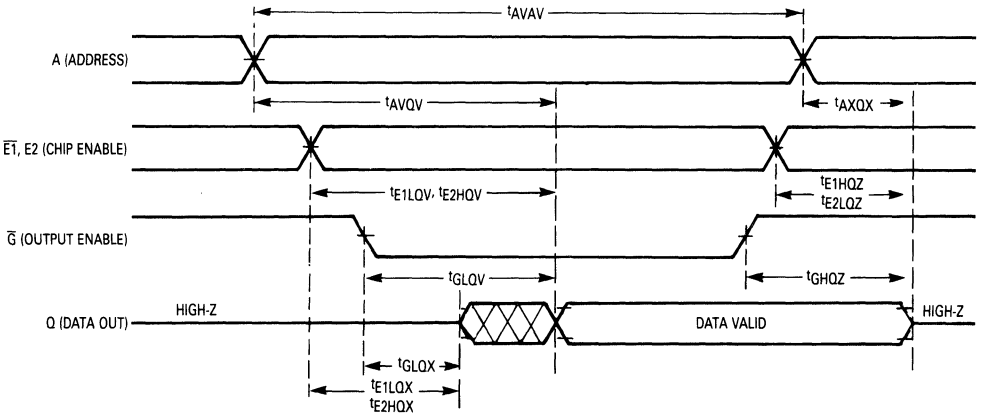
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1

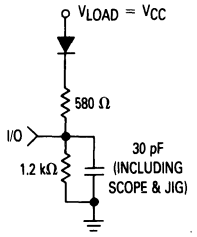
READ CYCLE (See Note 1)

Characteristic	Symbol	Alt Symbol	6164-55		6164-70		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	55	—	70	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	55	—	70	ns	
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	55	—	70	ns	
E2 Access Time	t_{E2HQV}	t_{AC2}	—	55	—	70	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	50	—	50	ns	
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	10	—	10	—	ns	2
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	5	—	ns	2
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	—	35	—	35	ns	2,3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	—	35	—	35	ns	2,3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. This parameter is sampled and not 100% tested.

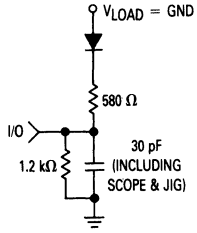


AC TEST LOADS



(Used for all propagation delay tests except for high to high Z transitions.)

Figure 1a.



(Used only for propagation tests involving high to high Z transitions or vice versa.)

Figure 1b.

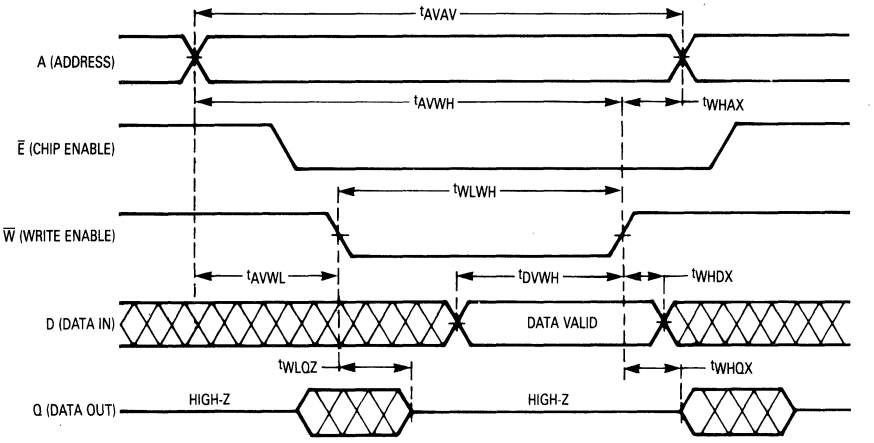
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Characteristic	Symbol	Alt Symbol	6164-55		6164-70		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	15	—	15	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	50	—	70	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	45	—	60	—	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	30	—	40	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	10	—	10	—	ns	3
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	—	5	—	ns	4

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.



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TYPICAL CHARACTERISTICS

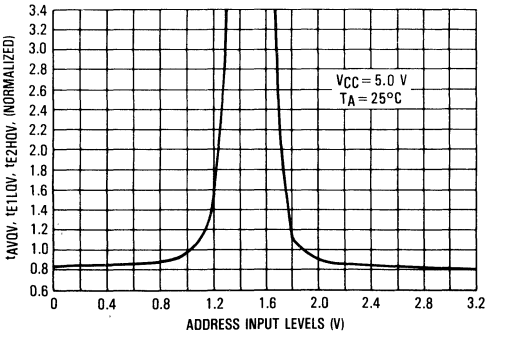
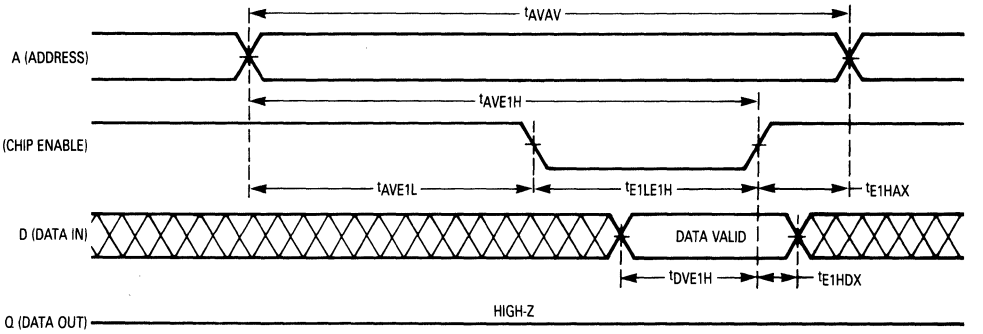


Figure 2. Access Time versus Address Input Levels

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Characteristic	Symbol	Alt Symbol	6164-55		6164-70		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	ns	
Address Setup Time	t_{AVE1L}	t_{AS}	0	—	0	—	ns	

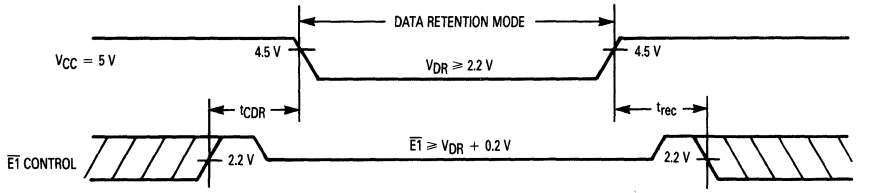
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low $\underline{E2}$.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.



LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55 to +125°C)

Characteristic		Symbol	Min	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq 2.2$ V, $V_{in} \geq 2.2$ V)		V_{DR}	2.2	5.5	V
Data Retention Current (V_{CC} = 2 V, $\overline{E1} \geq 2.2$ V, $V_{in} \geq 2.2$ V)	+25, −55°C +125°C	I_{CCDR}	— —	40 200	μA
Chip Disable to Data Retention Time (see waveform below)		t_{CDR}	0	—	ns
Operation Recovery Time (see waveform below)		t_{rec}	t_{AVAV}*	—	ns

*t_{AVAV} = Read Cycle Time



ORDERING INFORMATION
(Order by Full Part Number)

6164-55 / BXAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages in All Speeds
55 ns	X C-DIP 28 pin
70 ns	U LCCC 32 terminal

8

Military 6168

4K x 4-Bit Fast Static Random Access Memory

The 6168 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other high speed applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature provides reduced system power requirements without degrading access time performance.

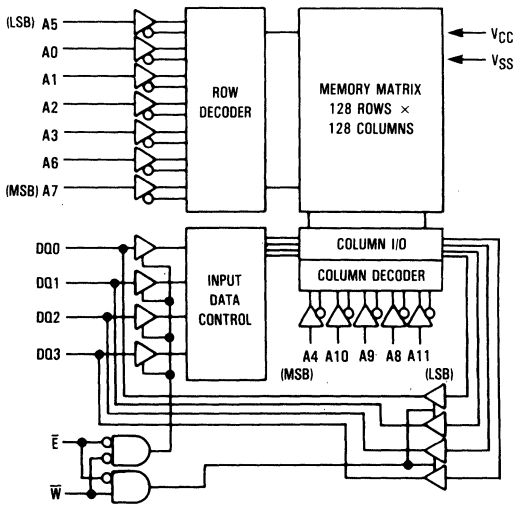
The 6168 is available in a 300 mil, 20 lead ceramic dual-in-line, 20 terminal, and rectangular ceramic LCC packages with the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Three State Output
- Fast Access Time (Maximum):

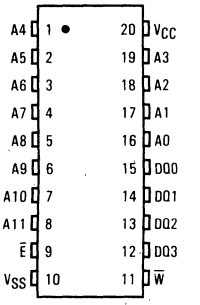
	Address	Chip Enable
6168-55	55 ns	55 ns
6168-70	70 ns	70 ns

- Low Power Operation @ 25°C: 120 mA Max (Active)
  20 mA Max (Standby — TTL Levels)
  0.9 mA Max (Standby — CMOS Levels)
- Fully TTL Compatible

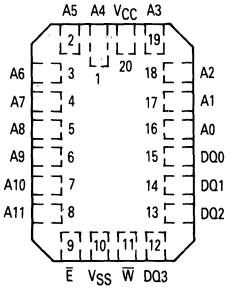
BLOCK DIAGRAM



PIN ASSIGNMENT



CASE 732-03
CERAMIC



CASE 756C-01
CERAMIC

PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

8

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin
H	X	Not Selected	ISB1, ISB2	High-Z
L	H	Read	I_{CC}	D_{out}
L	L	Write	I_{CC}	D_{in}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V	
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V	1
Input Low Voltage	V_{IL}	−0.3	0.8	V	1, 2

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	IIL	—	±2.0	μA	
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	IOZL	—	±2.0	μA	3
AC Supply Current (I_{out} = 0 mA, Cycle = Min, Duty = 100%)	I_{CCA}	—	90	mA	3
TTL Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	20	mA	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ 0.2 V or ≥ V_{CC} − 0.2 V)	I_{SB2}	—	5.0	mA	
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V	

CAPACITANCE (f = 1 MHz, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

NOTES:
1. Address rise and fall times while the chip is selected are 50 ns maximum.
2. V_{IL}(min) = −0.3 V dc; V_{IL}(min) = −3.0 V ac (pulse width ≤ 20 ns).
3. Input levels less than −0.3 V or greater than V_{CC} + 0.3 V will cause I/O and power supply currents to exceed maximum rating.

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

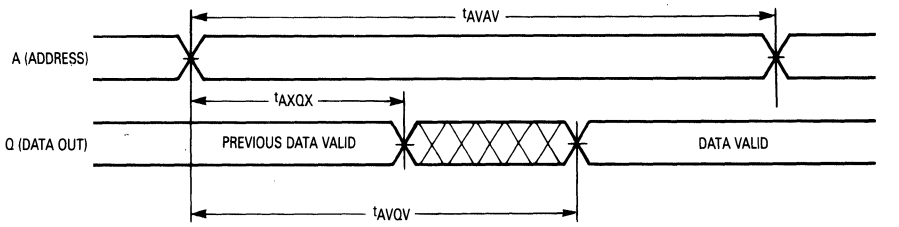
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

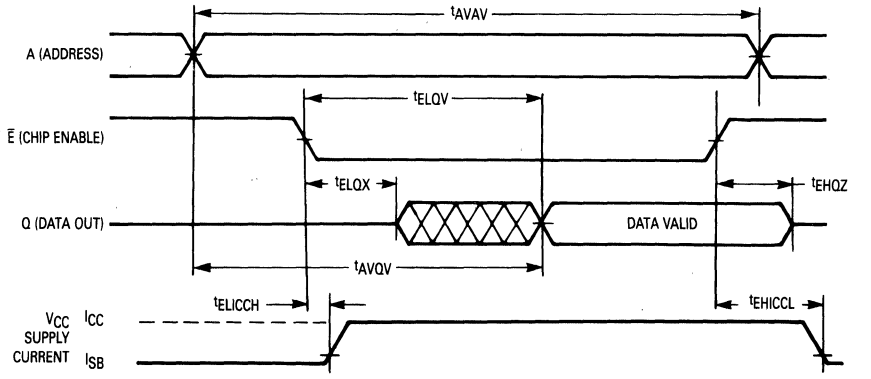
Parameter	Symbol		6168-55		6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	55	—	70	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	55	—	70	ns	
$\overline{E}$ Access Time	t_{ELQV}	t_{ACS}	—	55	—	70	ns	
$\overline{E}$ Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	2
$\overline{E}$ High to Output High-Z	t_{EHQZ}	t_{HZ}	0	25	0	30	ns	2,5
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	5
Power Down Time	t_{EHICCL}	t_{PD}	—	55	—	70	ns	5

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
3. Device is continuously selected ($\overline{E}$ = V_{IL}).
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. This test is sampled and not 100% tested.

READ CYCLE 1 (See Note 3 Above)



READ CYCLE 2 (See Note 4 Above)



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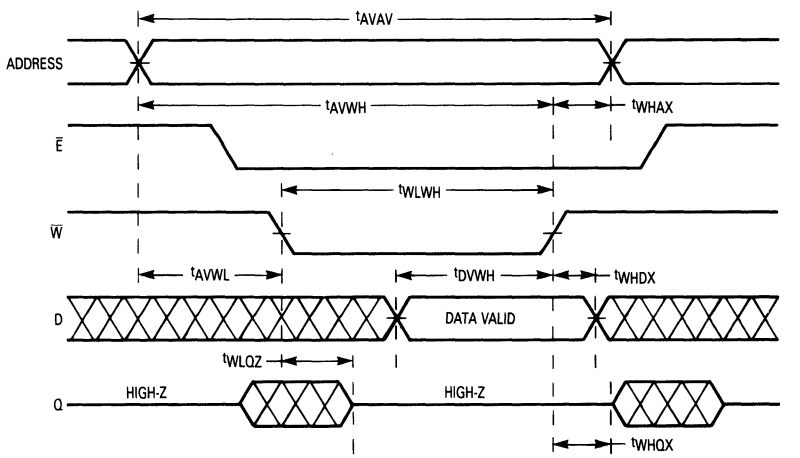
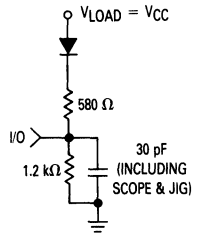
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6168-55		6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	50	—	60	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	—	60	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	40	—	60	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	25	—	30	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	—	3	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	—	25	—	30	ns	2,3
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	2,3
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
3. This parameter is sampled and not 100% tested.

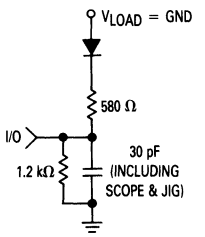


AC TEST LOADS



(Used for all propagation delay tests except for high to high Z transitions.)

Figure 1a.



(Used only for propagation tests involving high to high Z transitions or vice versa.)

Figure 1b.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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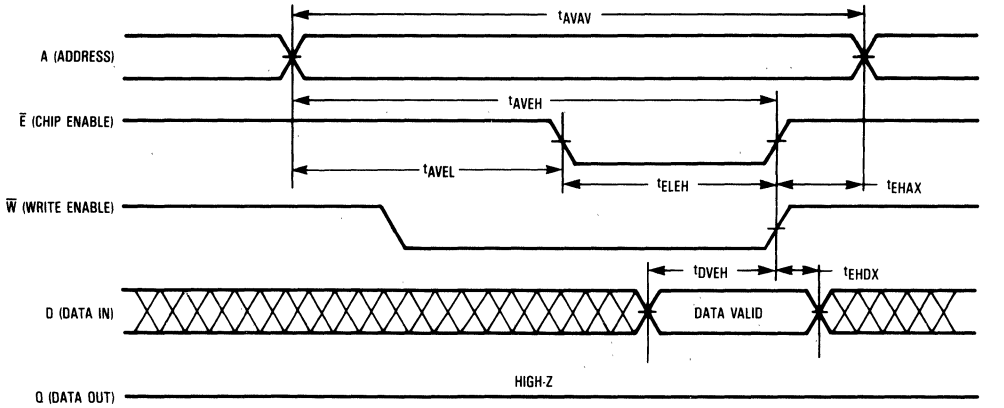
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6168-55		6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	50	—	60	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	40	—	60	—	ns	
Write Pulse Width	t_{ELEH}	t_{CW}	45	—	60	—	ns	2, 3
Data Valid to End of Write	t_{DVEH}	t_{DW}	25	—	30	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	—	3	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
3. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



8

ORDERING INFORMATION
(Order by Full Part Number)

6168-55 / BRAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages in All Speeds		
55 ns	R	C-DIP	20 pin
70 ns	U	LCCC	20 terminal

Military 6206

Advance Information

32K x 8 Bit Fast Static Random Access Memory

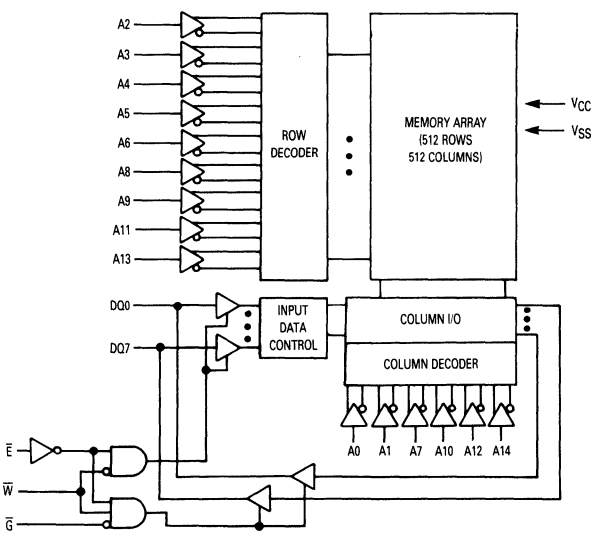
The 6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

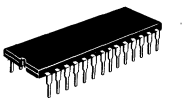
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 15 ns (6206-45).

The 6206 is packaged in a 600 mil, 28 pin ceramic dual-in-line package.

- Single 5.0 V Supply, ±10%
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 45 or 55 or 70 ns or 100 ns (Maximum)
- Low Power Dissipation
- Two Chip Controls; $\overline{E}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible
- Order as Part Number: 6206-45/BXAJC

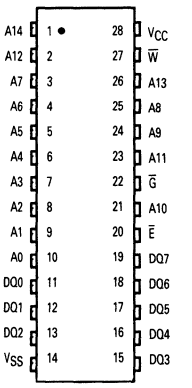
BLOCK DIAGRAM





CASE 733-04
CERAMIC

PIN ASSIGNMENT



PIN NAMES

A0–A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0–DQ7	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground

8

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X — Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature — Plastic	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 ±10%, T_A = −55° to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 Vdc; V_{IL} (min) = −3.0 Vac (pulse width ≤ 20 ns)

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DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg}(I)$	—	±2.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to 5.5 V)		$I_{lkg}(O)$	—	±2.0	μA
Power Supply Current ($\overline{E}$ = V_{IL}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0)	(t_{AVAV} = 35 ns)	I_{CC}	—	120	mA
	(t_{AVAV} = 45 ns)	I_{CC}	—	110	
Standby Current ($\overline{E}$ = V_{IH}) (TTL Levels)		I_{SB1}	—	20	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V) (CMOS Levels)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled and not 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	6.0	pF
I/O Capacitance	$C_{I/O}$	8.0	pF

Military 6268

4K x 4-Bit Fast Static Random Access Memory

The 6268 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-50 ns applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

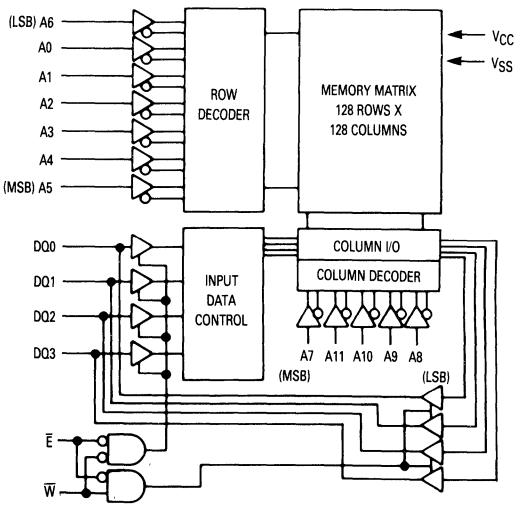
The 6268 is available in a 20-lead ceramic dual-in-line and 20-terminal ceramic LCCC package and features the standard JEDEC pinout.

- Single 5 V Supply, ± 10%
- 4K x 4 Bit Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum):

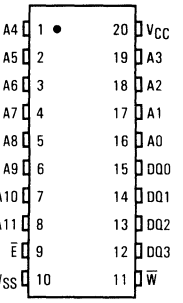
	Address	Chip Enable
6268-35	35 ns	35 ns
6268-45	45 ns	45 ns

- Low Power Operation: 120 mA Maximum, Active AC
  20 mA Maximum, Standby (TTL Levels)
  0.9 mA Maximum, Standby (Full Rail)

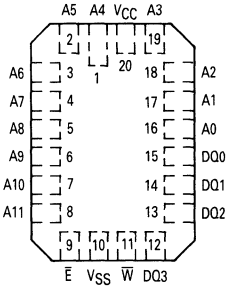
BLOCK DIAGRAM



PIN ASSIGNMENT



CASE 732-03
CERAMIC



CASE 756C-01
CERAMIC

PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

8

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

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DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	IIL	—	2	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	IOZL	—	2	μA
AC Supply Current (I_{out} = 0 mA, Cycle = Min, Duty = 100%)	I_{CCA}	—	120	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	5.0	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	3	6	pF
	$\overline{E}$		—	5	6	
I/O Capacitance		$C_{I/O}$	—	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

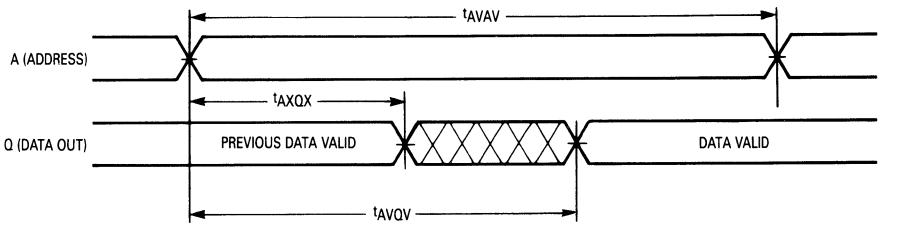
Output Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

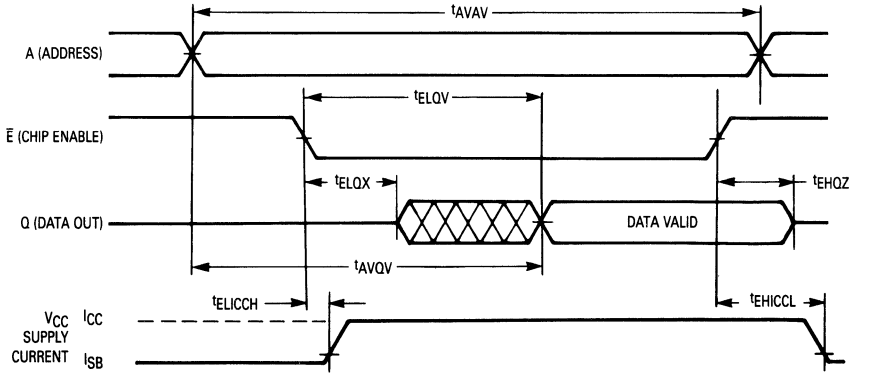
Parameter	Symbol		6268-35		6268-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	3,4
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	20	ns	3,4,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	7
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	ns	7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. Device is continuously selected ($\overline{E}$ = V_{IL}).
6. Addresses valid prior to or coincident with $\overline{E}$ going low.
7. This parameter is sampled and not 100% tested.

READ CYCLE 1 (See Note 5 Above)



READ CYCLE 2 (See Note 6 Above)



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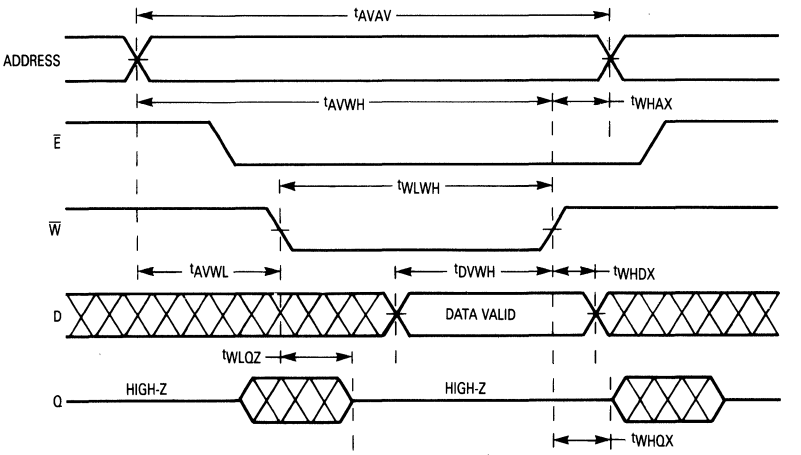
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6268-35		6268-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	—	20	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	—	3	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	20	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.
5. This parameter is sampled and not 100% tested.



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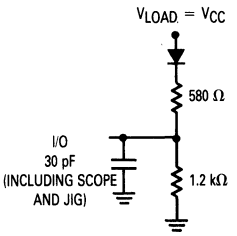
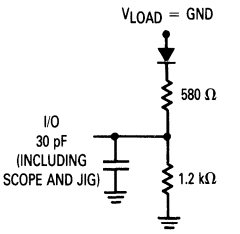
AC TEST LOADS



Test circuit used for propagation delay tests except for V_{OH} to high-Z transitions.

Figure 1a.



Use only for V_{OH} to high-Z and high-Z to V_{OH} transitions.

Figure 1b.

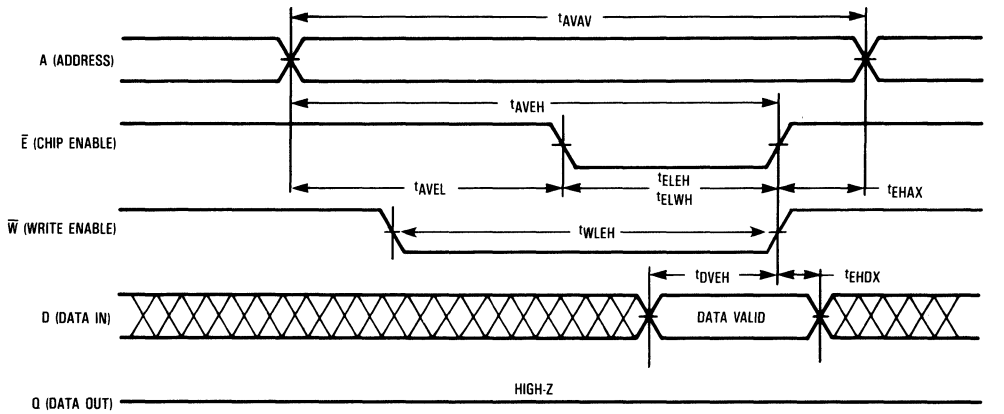
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6268-35		6268-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	30	—	35	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	30	—	35	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	20	—	20	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	—	3	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



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ORDERING INFORMATION
(Order by Full Part Number)

6268-35 / BRAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages in All Speeds		
35 ns	R	C-DIP	20 pin
45 ns	U	LCCC	20 terminal

Military 6287

64K x 1-Bit Fast Static Random Access Memory

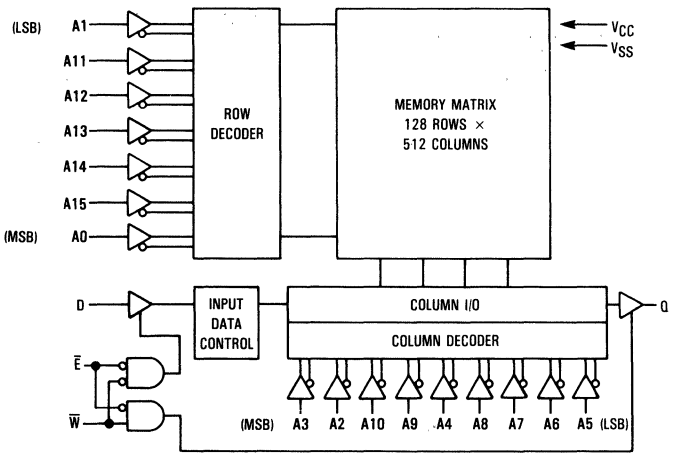
The 6287 is a 65,536-bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The 6287 is available in a 300 mil, 22-pin sidebraze, and a 22-terminal ceramic leadless chip carrier measuring 290 x 490 mils. All feature JEDEC standard pinouts.

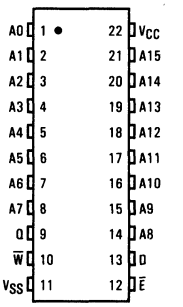
- Single 5 V ±10% Power Supply
- Fast Access Time: 35/45 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 70 mA Maximum, Active AC
  5 mA Maximum, Standby (TTL Levels)
  2 mA Maximum, Standby (Full Rail)
- Fully TTL Compatible
- Three-State Data Output
- Low Power, Battery Backup Operation with 2 V Data Retention

BLOCK DIAGRAM



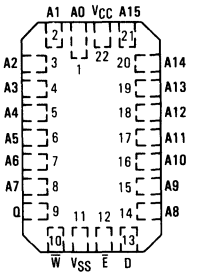
PIN ASSIGNMENT

SIDEBRAZE



CASE 677-06
CERAMIC

CHIP CARRIER



CASE 800-02
CERAMIC

PIN NAMES	
A0–A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

8

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature—Ceramic	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2 V	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	IIL	—	±2	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	IOZL	—	±2	μA
AC Supply Current (I_{out} = 0 mA, Cycle = Min, Duty = 100%)	I_{CCA}	—	70	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	4	8	pF
Output Capacitance		C_{out}	—	5	10	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

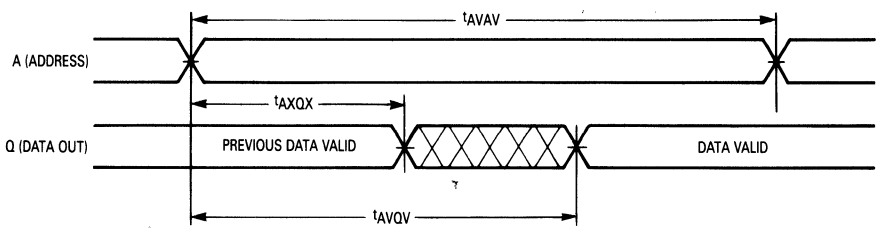
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

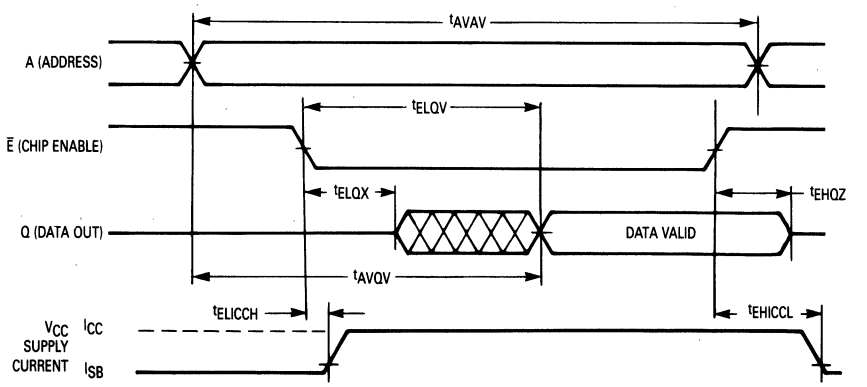
Parameter	Symbol		6287-35		6287-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	25	0	30	ns	4,5,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	7
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	ns	7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. Device is continuously selected ($\overline{E}$ = V_{IL}).
7. This parameter is sampled and not 100% tested.

READ CYCLE 1 (See Note 6 Above)



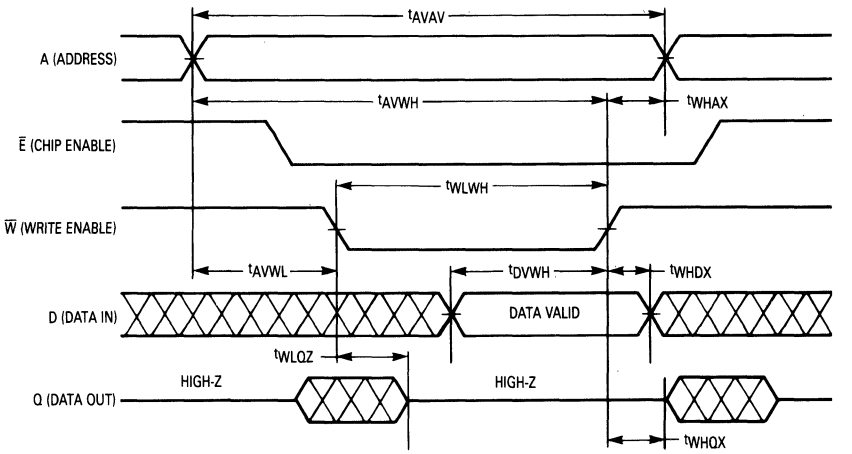
READ CYCLE 2 (See Note 3 Above)



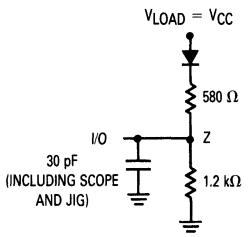
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6287-35		6287-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	—	40	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	40	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	5	—	5	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	20	0	30	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. This parameter is sampled and not 100% tested.

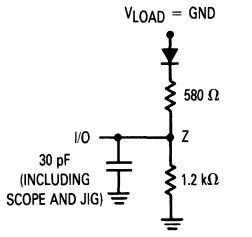


AC TEST LOADS



Test circuit used for propagation delay tests except for V_{OH} to high-Z transitions.

Figure 1a.



Use only for V_{OH} to high-Z and high-Z to V_{OH} transitions.

Figure 1b.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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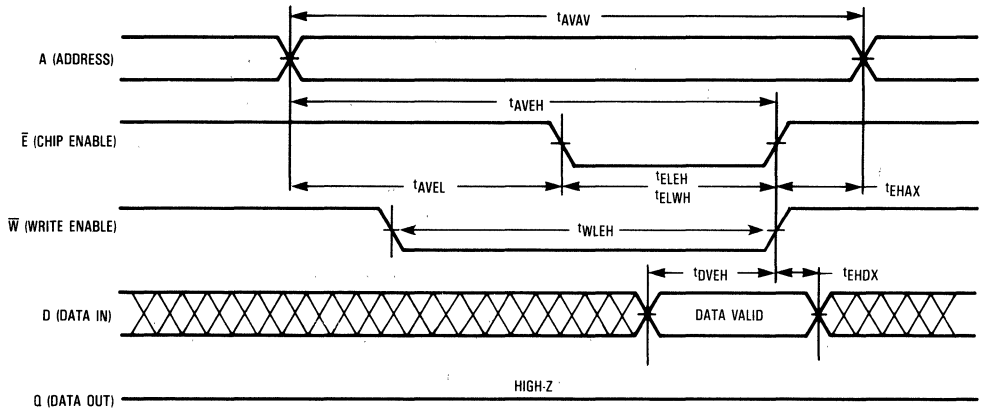
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6287-35		6287-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	30	—	35	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	30	—	40	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	30	—	40	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	5	—	5	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



8

ORDERING INFORMATION
(Order by Full Part Number)

6287-35 / BXAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages in all Speeds		
35 ns	X	Sidebraze	22 pin
45 ns	U	LCCC	22 terminal

Military 6288

16K x 4-Bit Fast Static Random Access Memory

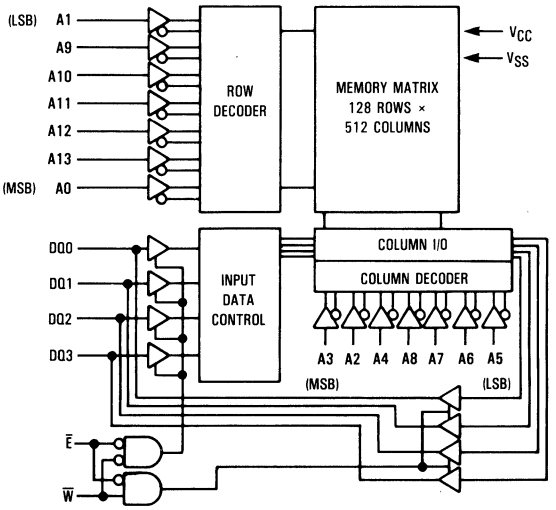
The 6288 is a 65,536-bit static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

The 6288 is available in a 300 mil, 22-pin sidebraze, and a 22-terminal ceramic leadless chip carrier measuring 290 x 490 mils. All feature JEDEC standard pinouts.

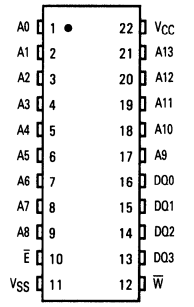
- Single 5 V ±10% Power Supply
- Fast Access Time: 35/45 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120 mA Maximum, Active AC
  5 mA Maximum, Standby (TTL Levels)
  2 mA Maximum, Standby (Full Rail)
- Fully TTL Compatible
- Three-State Data Output

BLOCK DIAGRAM



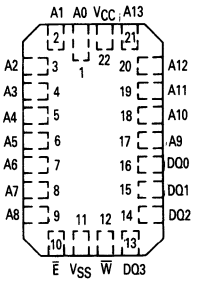
PIN ASSIGNMENT

SIDEBRAZE



CASE 677-06
CERAMIC

CHIP CARRIER



CASE 800-02
CERAMIC

PIN NAMES	
A0–A13	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0–DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

8

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	IIL	—	2	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	IOZL	—	2	μA
AC Supply Current (I_{out} = 0 mA, Cycle = Min, Duty = 100%)	I_{CCA}	—	90	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	4	8	pF
I/O Capacitance		$C_{I/O}$	—	5	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

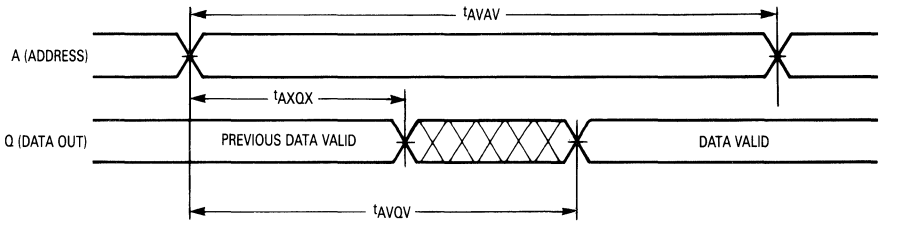
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

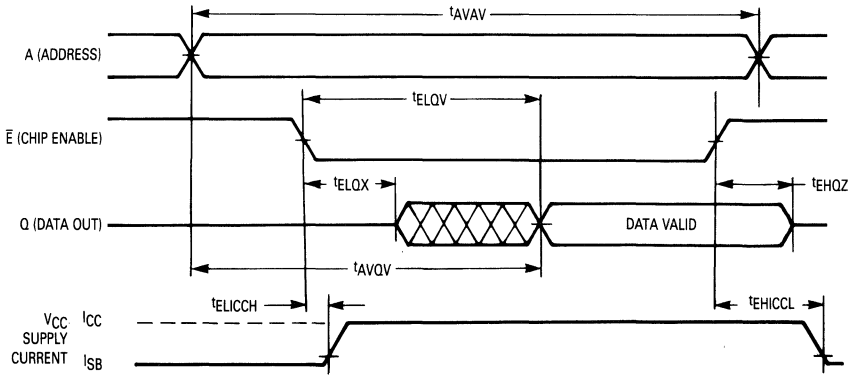
Parameter	Symbol		6288-35		6288-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	3	—	3	—	ns	4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	30	0	30	ns	4,5,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	7
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	ns	7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. Device is continuously selected ($\overline{E}$ = V_{IL}).
7. This parameter is sampled and not 100% tested.

READ CYCLE 1 (See Note 6 Above)



READ CYCLE 2 (See Note 3 Above)



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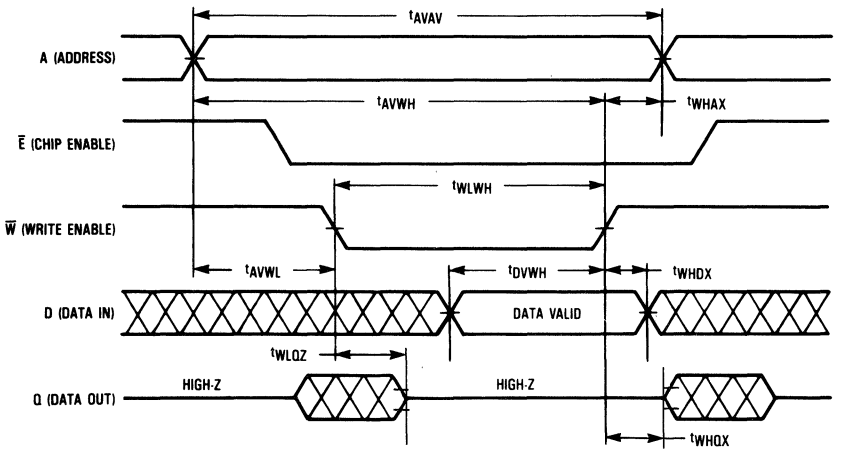
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6288-35		6288-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	—	40	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	40	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	—	20	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	20	0	20	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.
5. Parameter is sampled and not 100% tested.



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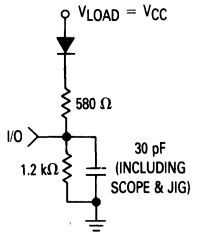
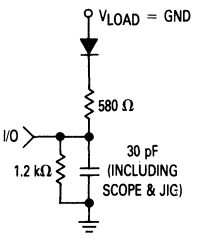
AC TEST LOADS



(Used for all propagation delay tests except for high to high Z transitions.)

Figure 1a.



(Used only for propagation tests involving high to high Z transitions or vice versa.)

Figure 1b.

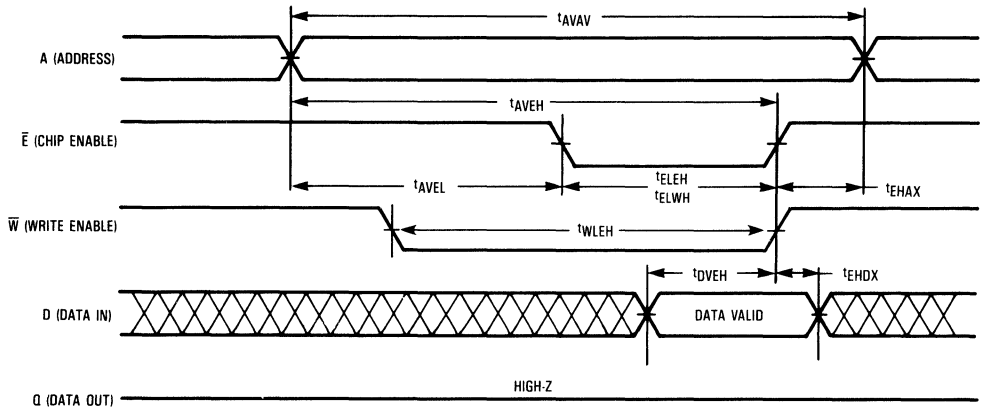
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6288-35		6288-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	30	—	40	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	30	—	35	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	30	—	40	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



8

ORDERING INFORMATION
(Order by Full Part Number)

6288-35 / BXAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages in All Speeds		
35 ns	X	Sidebraze	22 pin
45 ns	U	LCCC	22 terminal

Military 93415

TTL 1024 x 1-Bit Random Access Memory

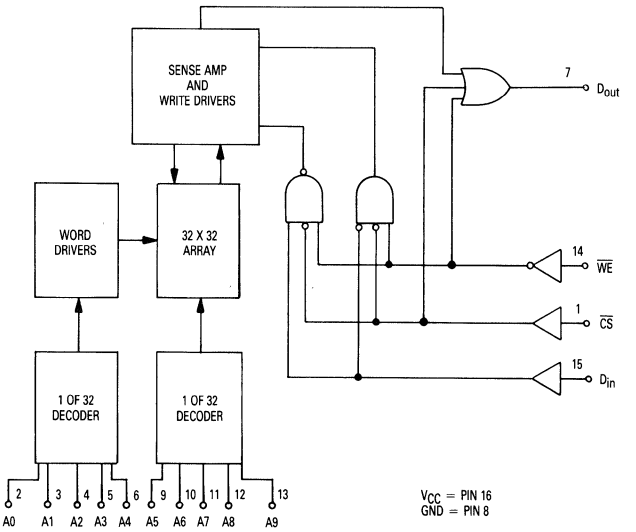
The 93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

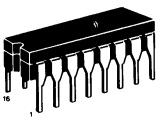
The 93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

The 93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

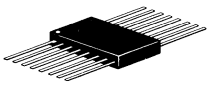
- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed —
  - Access Time — 35 ns Typical
  - Chip Select — 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words x 1 Bit
- Order as: 93415/BEAJC = Dual-In-Line
  93415/BFAJC = Flat Pack

BLOCK DIAGRAM



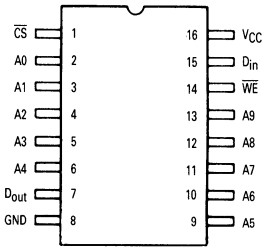


CASE 620-09
CERAMIC DUAL-IN-LINE



CASE 650-05
FLAT PACK

PIN ASSIGNMENT



PIN NAMES	
$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

8

FUNCTIONAL DESCRIPTION

The 93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Min)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature Ceramic Package (E and F Suffix)	−55°C to +165°C
Operating Junction Temperature, T_J Ceramic Package (E and F Suffix)	<165°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

GUARANTEED OPERATING RANGES (Note 2)

Supply Voltage (V_{CC})			
Min	Nom	Max	Ambient Temperature (T_A)
4.5 V	5.0 V	5.5 V	−55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature range unless otherwise noted)

Symbol	Characteristic	Limits Min	Limits Max	Unit	Conditions	
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		−400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
I_{CEX}	Output Leakage Current		100	μAdc	V_{CC} = Max, V_{out} = 5.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.5	Vdc	V_{CC} = Max, I_{in} = −12 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = +125°C	V_{CC} = 5.5 V, All Inputs Grounded
			155	mAdc	T_A = 25°C	
			170	mAdc	T_A = −55°C	

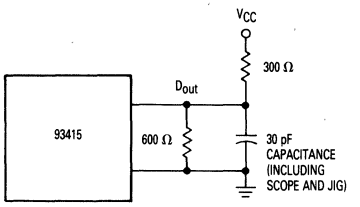
8

AC OPERATING CONDITIONS AND CHARACTERISTICS

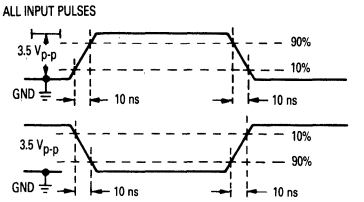
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

LOADING CONDITION



INPUT PULSES

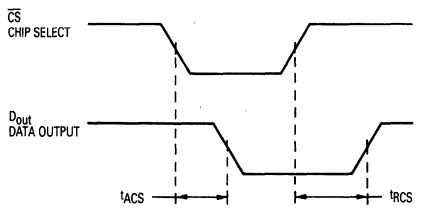


Symbol	Characteristic (Notes 2, 3)	93415/BE/BF Min	93415/BE/BF Max	Unit	Conditions
READ MODE	DELAY TIMES			ns	
t_{ACS}	Chip Select Time		45		See Test Circuit
t_{RCS}	Chip Select Recovery Time		50		and Waveforms
t_{AA}	Address Access Time		60		
WRITE MODE	DELAY TIMES			ns	
t_{WS}	Write Disable Time		45		See Test Circuit
t_{WR}	Write Recovery Time		50		and Waveforms
	INPUT TIMING REQUIREMENTS			ns	
t_W	Write Pulse Width (to guarantee write)	40			
t_{WSD}	Data Setup Time Prior to Write	5.0			
t_{WHD}	Data Hold Time After Write	5.0			See Test Circuit
t_{WSA}	Address Setup Time (at t_W = Min)	15			and Waveforms
t_{WHA}	Address Hold Time	10			
t_{WSCS}	Chip Select Setup Time	5.0			
t_{WHCS}	Chip Select Hold Time	5.0			

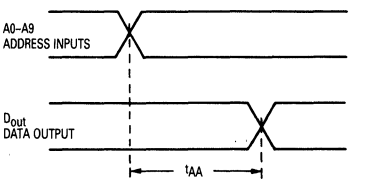
8

READ OPERATION TIMING DIAGRAM

PROPAGATION DELAY FROM CHIP SELECT

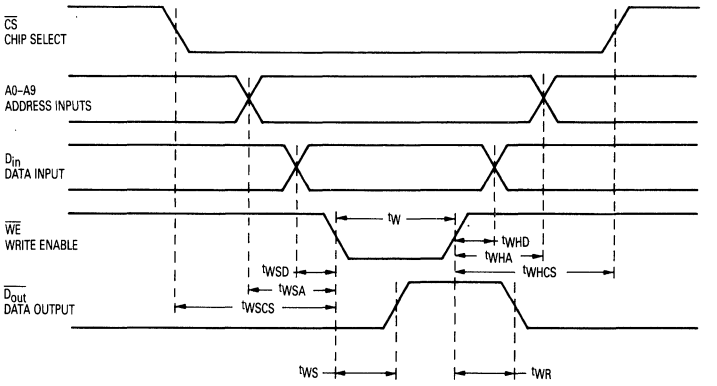


PROPAGATION DELAY FROM ADDRESS INPUTS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE CYCLE TIMING



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
E Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W

NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

8

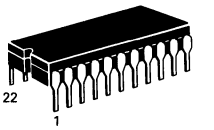
Military 93422 93L422,A

TTL 256 x 4-Bit Random Access Memory

The 93422 Series are 1024-bit Read/Write RAMs, organized 256 words by 4 bits, designed for high performance main memory and control storage applications.

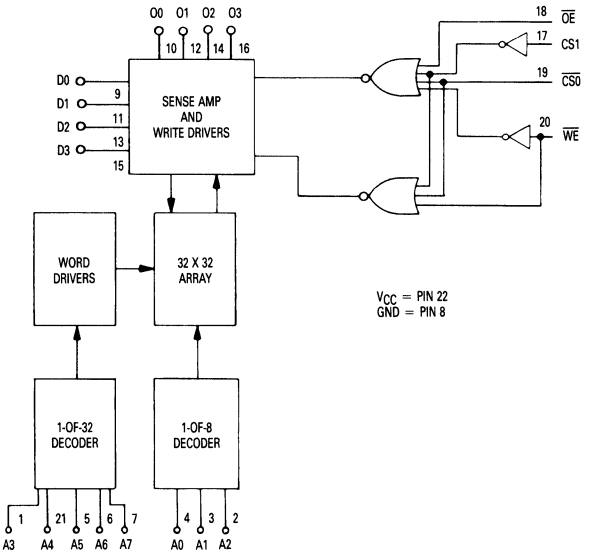
They have full decoding on-chip, separate data input and data output lines, an active low-output enable, write enable, and two chip selects, one active high, one active low. These memories are fully compatible with standard TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Outputs
- Non-Inverting Data Outputs
- Power Dissipation — 0.26 mW/Bit Typical
- Standard 22-Pin, 400 Mil Wide Package
- Power Dissipation Decreases with Increasing Temperature
- Organized 256 Words x 4 Bits
- Two Chip Select Lines for Memory Expansion
- Address Access Time: 93422 — 60 ns Max
  93L422A — 55 ns Max
  93L422 — 75 ns Max

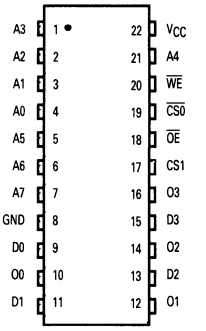


W SUFFIX
CASE 736-05
CERAMIC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

$\overline{CS0}$, CS1	Chip Selects
A0–A7	Address Inputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
D0–D3	Data Inputs
O0–O3	Data Outputs

8

FUNCTIONAL DESCRIPTION

The 93422 Series are fully decoded 1024-bit random access memories organized 256 words by 4 bits. Word selections are achieved by means of an 8-bit address, A0–A7.

The Chip Select (CS0 and CS1) inputs provide for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable (WE, Pin 20). With WE and CS0 held low and the CS1 held high, the data at D_n is written into the addressed location. To read, WE and CS1 are held high and CS0 is held low. Data in the specified location is presented at the output (O0–O2) and is non-inverted.

The three-state outputs provide drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in a high-impedance state.

GUARANTEED OPERATING RANGES

Part Number	Supply Voltage (V_{CC}) Min	Nom	Max	Ambient Temp. (T_A)
93422/BWAJC 93L422/BWAJC 93L422A/BWAJC	4.5 V	5.0 V	5.5 V	−55°C to +125°C

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature Ceramic Package (W Suffix)	−65°C to +150°C
Operating Junction Temperature, T_J Ceramic Package (W Suffix)	<165°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

*Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs					Output	
$\overline{OE}$	$\overline{CS0}$	CS1	$\overline{WE}$	D0–D3	O0–O3	Mode
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	X	X	X	X	High Z	Output Disabled
L	L	H	H	X	O0–O3	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range)

Symbol	Characteristic		Limits Min	Max	Units	Conditions
V_{OL}	Output Low Voltage		—	0.45	Vdc	V_{CC} = Min, I_{OL} = 8.0 mA
V_{IH}	Input High Voltage		2.1	—	Vdc	Guaranteed Input High Voltage for All Inputs
V_{IL}	Input Low Voltage		—	0.8	Vdc	Guaranteed Input Low Voltage for All Inputs
I_{IL}	Input Low Current		−0.01	−300	μAdc	V_{CC} = Max, V_{in} = 0.45 V
I_{IH}	Input High Current		—	40	μAdc	V_{CC} = Max, V_{in} = 5.5 V
I_{off}	Output Current (High Z)		— —	50 −50	μAdc	V_{CC} = Max, V_{out} = 2.4 V V_{CC} = Max, V_{out} = 0.45 V
I_{OS}	Output Current Short Circuit to Ground		−10	−70	mAdc	V_{CC} = Max (Note 1)
V_{OH}	Output High Voltage		2.4	—	Vdc	V_{CC} = Min, I_{OH} = −5.2 mA
V_{IK}	Input Diode Clamp Voltage		—	−1.5	Vdc	V_{CC} = Max, I_{in} = −10 mA
I_{CC}	Power Supply Current	93422	—	130	mAdc	T_A = +125°C; V_{CC} = 5.5 V, All Inputs Grounded
			—	155	mAdc	T_A = +25°C
			—	170	mAdc	T_A = −55°C
		93L422A 93L422	—	70	mAdc	T_A = +125°C
			—	80	mAdc	T_A = +25°C
			—	90	mAdc	T_A = −55°C

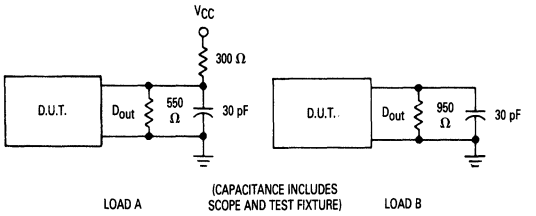
8

AC OPERATING CONDITIONS AND CHARACTERISTICS

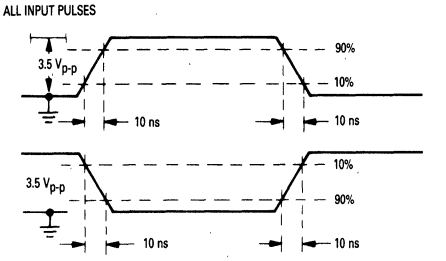
(Full operating voltage and temperature range)

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT PULSES



Symbol	Characteristic (Notes 1, 2, 3, 4, 5)	93422/BWAJC Min	93422/BWAJC Max	93L422/BWAJC Min	93L422/BWAJC Max	93L422A/BWAJC Min	93L422A/BWAJC Max	Unit
READ MODE	DELAY TIMES							ns
t_{ACS}	Chip Select Time	—	45	—	45	—	40	
t_{ZRCS}	Chip Select to High Z	—	45	—	45	—	40	
t_{AOS}	Output Enable Time	—	45	—	45	—	40	
t_{ZROS}	Output Enable to High Z	—	45	—	45	—	40	
t_{AA}	Address Access Time	—	60	—	75	—	55	
WRITE MODE	DELAY TIMES							ns
t_{ZWS}	Write Disable to High Z	—	45	—	45	—	45	
t_{WR}	Write Recovery Time	—	50	—	50	—	45	
	INPUT TIMING REQUIREMENTS							ns
t_W	Write Pulse Width (to guarantee write)	30	—	30	—	40	—	
t_{WSD}	Data Setup Time Prior to Write	5.0	—	5.0	—	5.0	—	
t_{WHD}	Data Hold Time After Write	5.0	—	5.0	—	5.0	—	
t_{WSA}	Address Setup Time (at t_W = Min)	10	—	10	—	10	—	
t_{WHA}	Address Hold Time	10	—	10	—	5.0	—	
t_{WSCS}	Chip Select Setup Time	5.0	—	5.0	—	5.0	—	
t_{WHCS}	Chip Select Hold Time	5.0	—	5.0	—	5.0	—	

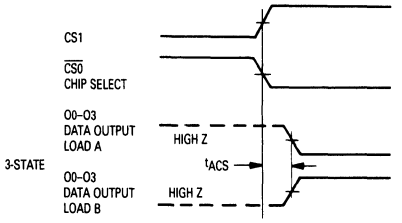
NOTES:
1. Output short circuit conditions must not exceed 1.0 second duration.
2. The maximum address access time is guaranteed to be the worst-case bit in the memory.
3. Load A used to measure transitions between logic levels and from High Z state to logic Low state.
   Load B used to measure transitions between High Z state to logic High state.
   Load C used to measure transitions from either logic High or Low state to High Z state.
4. All time measurements are referenced to +1.5 Vdc except transitions into the High Z state where outputs are referenced to a delta of 0.5 Vdc from the logic level using Load C.
5. See test circuit and waveforms.

8

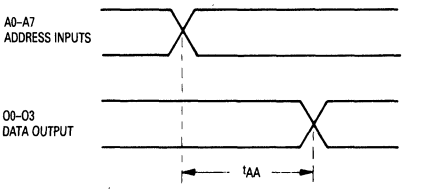
READ OPERATION TIMING DIAGRAM

(All Time Measurements Referenced to 1.5 V)

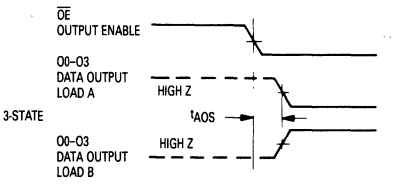
PROPAGATION DELAY FROM CHIP SELECT



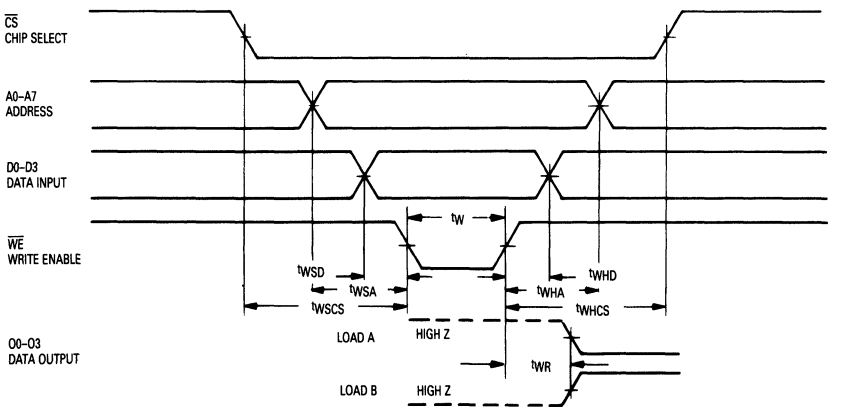
PROPAGATION DELAY FROM ADDRESS INPUTS



PROPAGATION DELAY FROM OUTPUT ENABLE



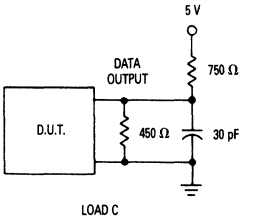
WRITE CYCLE TIMING

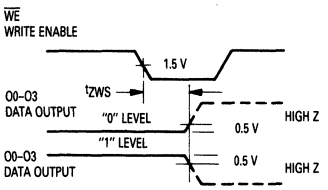


(ALL ABOVE MEASUREMENTS REFERENCE TO 1.5 V)

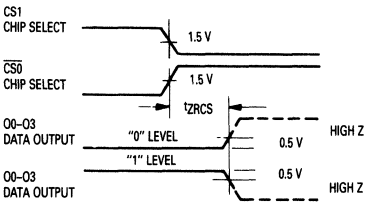
8

WRITE ENABLE TO HIGH Z DELAY

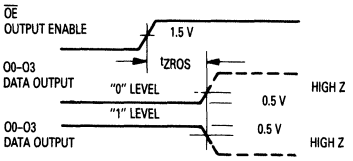




PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



PROPAGATION DELAY FROM OUTPUT ENABLE TO HIGH Z



(ALL t_{ZXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5 V FROM THE LOGIC LEVEL AND USING LOAD C.)

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown*	Still	
W Suffix	50°C/W	75°C/W	15°C/W

*500 linear ft. per minute blown air.

8

Military 93425

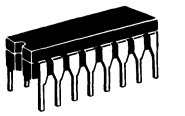
TTL 1024 x 1-Bit Random Access Memory

The 93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

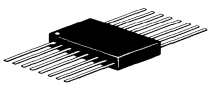
The 93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

The 93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed —
  Access Time — 35 ns Typical
  Chip Select — 15 ns Typical
- Power Dissipation — 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature
- Order as Part Number: 93425/BEAJC = Dual-In-Line
  93425/BFAJC = Flat Pack

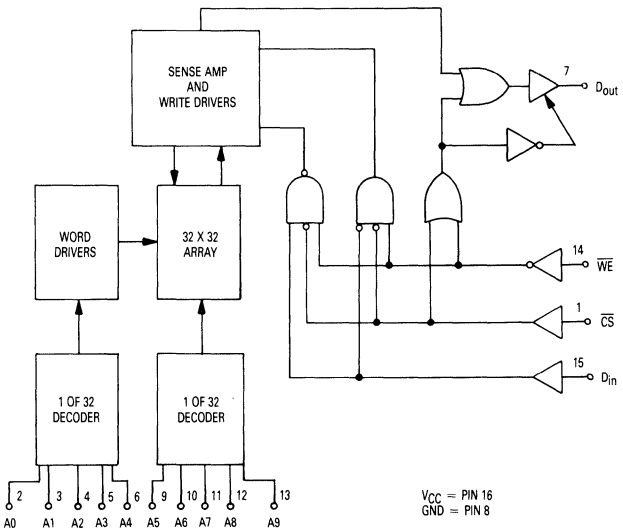


CASE 620-09
CERAMIC DUAL-IN-LINE



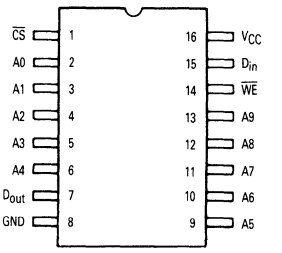
CASE 650-05
FLAT PACK

BLOCK DIAGRAM



NOTE: Logic driving sense amp/write drivers depicts negative-only write used on C4m.

PIN ASSIGNMENT



PIN NAMES

$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

8

FUNCTIONAL DESCRIPTION

The 93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0–A9.

The Chip Select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and $\overline{CS}$ held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature Ceramic Package (E and F Suffix)	−55°C to +165°C
Operating Junction Temperature, T_J Ceramic Package (E and F Suffix)	<165°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

GUARANTEED OPERATING RANGES (Notes 2 and 3)

Supply Voltage (V_{CC})			
Min	Nom	Max	Ambient Temperature (T_A)
4.5 V	5.0 V	5.5 V	−55°C to +125°C

8

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

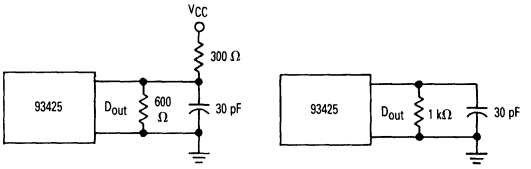
Symbol	Characteristic	Limits Min	Limits Max	Units	Conditions	
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltge	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		−400	μAdc	V_{CC} = Max, V_{in} = 0.45 V	
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 5.5 V	
I_{off}	Output Current (High Z)		50	μAdc	V_{CC} = Max, V_{out} = 4.5 V	
			−50		V_{CC} = Max, V_{out} = 0.45 V	
I_{OS}	Output Current Short Circuit to Ground	−20	−100	mAdc	V_{CC} = Max	
V_{OH}	Output High Voltage	2.4		Vdc	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage		−1.5	Vdc	V_{CC} = Max, I_{in} = −12 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = +125°C	V_{CC} = 5.5 V, All Inputs Grounded
			155	mAdc	T_A = 25°C	
			170	mAdc	T_A = −55°C	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

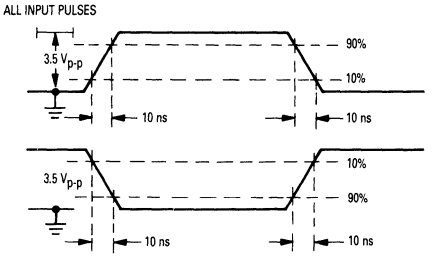
AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



LOAD A LOAD B

INPUT PULSES



Symbol	Characteristic (Notes 2, 4)	93425/BE/BF Min	93425/BE/BF Max	Units	Conditions
READ MODE	DELAY TIMES			ns	
t_{ACS}	Chip Select Time		45		See Test Circuit
t_{ZRCS}	Chip Select to High Z		50		and Waveforms
t_{AA}	Address Access Time		60		
WRITE MODE	DELAY TIMES			ns	
t_{WS}	Write Disable to High Z		45		See Test Circuit
t_{WR}	Write Recovery Time		50		and Waveforms
	INPUT TIMING REQUIREMENTS			ns	
t_W	Write Pulse Width (to guarantee write)	40			
t_{WSD}	Data Setup Time Prior to Write	5.0			
t_{WHD}	Data Hold Time After Write	5.0			See Test Circuit
t_{WSA}	Address Setup Time (at t_W = Min)	15			and Waveforms
t_{WHA}	Address Hold Time	10			
t_{WSCS}	Chip Select Setup Time	5.0			
t_{WHCS}	Chip Select Hold Time	5.0			

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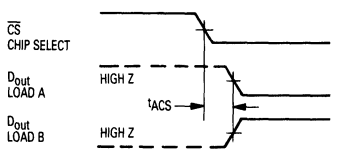
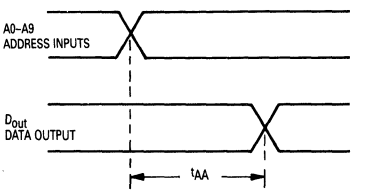
READ OPERATION TIMING DIAGRAM

PROPAGATION DELAY FROM CHIP SELECT

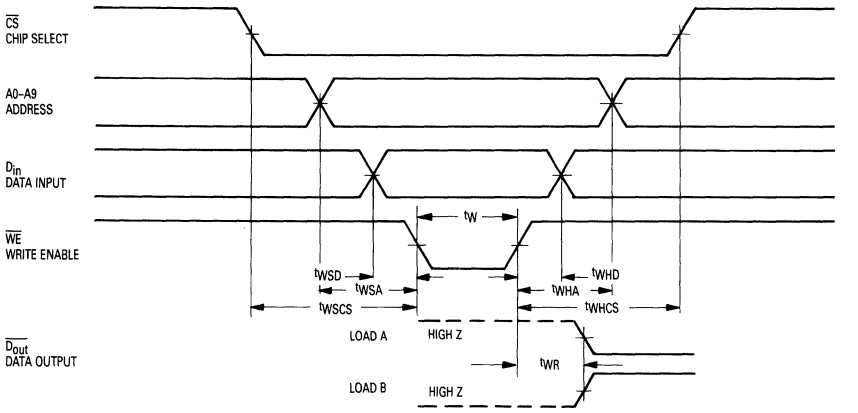


PROPAGATION DELAY FROM ADDRESS INPUTS



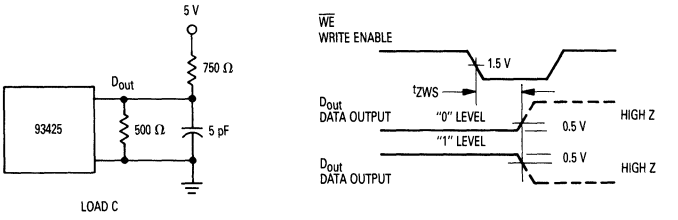
(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE CYCLE TIMING



(ALL ABOVE MEASUREMENTS REFERENCE TO 1.5 V)

WRITE ENABLE TO HIGH Z DELAY



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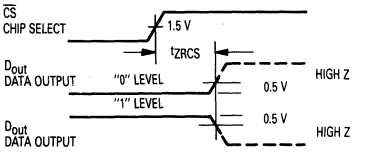
PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(ALL t_{ZXX} PARAMETERS ARE MEASURED AT A DELTA OF 0.5 V FROM THE LOGIC LEVEL AND USING LOAD C)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
E Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W

NOTE 3: Output short circuit conditions must not exceed 1 second duration.
NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

Reliability Information 9

MOTOROLA CORPORATE QUALITY GOAL

IMPROVE PRODUCT AND SERVICES QUALITY TEN TIMES BY 1989
AND AT LEAST ONE HUNDRED FOLD BY 1991.

ACHIEVE SIX SIGMA CAPABILITY BY 1992.

With a deep sense of urgency, spread dedication to quality to every facet of the corporation and achieve a culture of continual improvement to ASSURE TOTAL CUSTOMER SATISFACTION. There is only one ultimate goal: zero defects in everything we do.

signed:

BOB GALVIN
Chairman

BILL WEISZ
Vice Chairman

JOHN MITCHELL
President

GEORGE FISHER
Deputy to Chief
Executive Office

GARY TOOKER
Chief to Corporate
Staff Officer

JACK GERMAIN
Motorola Director
of Quality

JIM LINCICOME
Government Electronics
Group

CARL LINDHOLM
International
Operations

LEVY KATZIR
New Enterprises

JIM NORLING
Semiconductor Products
Sector

STEVE LEVY
Japanese Operations

DON JONES
Chief Financial
Officer

JIM DONNELLY
Personnel

RAY FARMER
Communications Sector

ED STAIANO
General Systems
Group

GERHARD SCHULMEYER
Automotive & Industrial
Electronics Group

DIVISION QUALITY STATEMENT

MOTOROLA MOS MEMORY PRODUCTS DIVISION

COMMITMENT TO SIX SIGMA
WORLD CLASS

The Memory Products Division staff are pleased to announce our commitment to be a World Class MOS Memory supplier. This means more bullet proof designs which can tolerate handling, processes at the limit and beyond, and outstanding control of the manufacturing processes such that a product design which is marginal will still yield consistent quality performance.

The Memory Products Division fully endorses the Motorola Corporate goal of improving product and service quality ten times by 1989 and one hundred fold by 1991.

Through our quality improvement process using SIX SIGMA methodology we can and will accomplish being the best memory supplier through WORLD CLASS product margins and services in their truest sense.

ENDORSEMENTS:

Jim George | Bud Broeker | Bill Bowers | Jim Eachus

Weldon Knape | Roger Kung | Bill Pfaff

9

OUR SIX SIGMA CHALLENGE

WHAT IS SIX SIGMA?

Six Sigma is the required capability level to approach the Standard. The Standard is Zero Defects. Our goal is to be best-in-class in Product, Sales, and Service.

WHY SIX SIGMA?

The performance of a product is determined by how much margin exists between the process characteristics required by the design, and the actual value of those characteristics. These characteristics are produced by processes in the factory, and at the suppliers.

Each process attempts to reproduce its characteristics identically from unit to unit, but within each process some variation does occur. For some processes, such as those which use real-time feedback to control the outcome, the variation is quite small, and for others it may be quite large.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal variation, defined as process width, is ±3 Sigma about the mean.

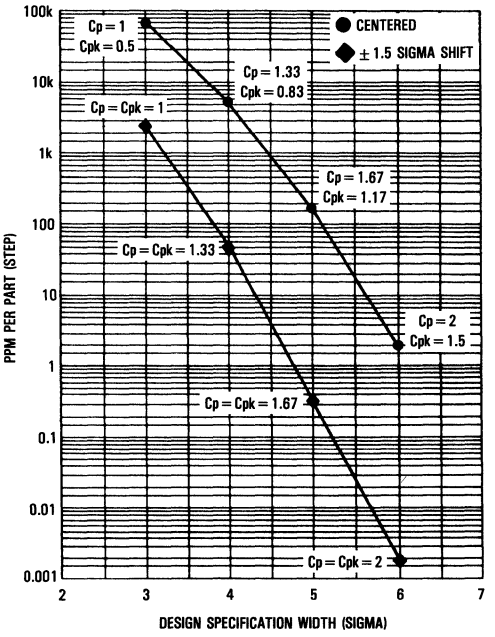


Figure 1. Standard Deviations from Mean

Approximately 2,700 parts per million parts/steps will fall outside the normal variation of ±3 Sigma, see Figure 1. This, by itself, does not appear disconcerting. However, when we build a product containing 1,200 parts/steps, we can expect 3.24 defects per unit (1200 × 0.0027), on an average. This would result in a rolled yield of less than 4%, which means fewer than 4 units out of every hundred would go through the entire manufacturing process without a defect, see Table 1.

Thus, we can see that for a product to be built virtually defect-free, it must be designed to accept characteristics that are significantly more than ±3 Sigma away from the Mean.

It can be shown that a design that can accept **twice the normal variation** of the process, or ±6 Sigma, can be expected to have no more than 3.4 parts per million defective for each characteristic, even if the process mean were to shift by as much as ±1.5 Sigma, see Figure 1. To quantify this, Capability Index (Cp) is used, where:

$$Cp = \frac{\text{design specification width}}{\text{process width}}$$

Table 1. Rolled Yield

TOTAL DEFECTS PER UNIT	ROLLED THROUGHPUT YIELD (%)
5.3	0.5
4.6	1.0
3.9	2.0
3.5	3.0
3.2	4.0
3.0	5.0
2.3	10
1.9	15
1.6	20
1.4	25
1.2	30
1.0	37
0.9	40
0.8	45
0.7	50
0.6	55
0.51	60
0.43	65
0.36	70
0.29	75
0.22	80
0.16	85
0.10	90
0.05	95
0.00	100

ROLLED THROUGHPUT YIELD (%) = $100\ e^{-d/u}$

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A design specification width of ±6 Sigma and a process width of ±3 Sigma yields a Cp of 12/6=2. However, as shown in Figure 2, the process mean can shift. When the process mean is shifted with respect to the design target mean, the Capability Index is adjusted with a factor k, and becomes Cpk. Cpk = Cp(1 − k), where:

$$k = \frac{\text{process shift}}{\text{design specification width/2}}$$

The k factor for ±6 Sigma design with a 1.5 Sigma process shift = 1.5/(12/2) = 0.25, and the Cpk = 2(1 − 0.25) = 1.5.

In the same case of a product containing 1,200 parts/steps, we would now expect only 0.0041 defects per unit (1200 × 0.0000034). This would mean that 996 units out of 1,000 would go through the entire manufacturing process without a defect (see Table 2).

It is our five year goal to achieve ±6 Sigma capability in Product, Sales, and Service.

Table 2. Overall Yield vs Sigma (Distribution Shifted ±1.5 σ)

NUMBER OF PARTS (STEPS)	±3 σ (%)	±4 σ (%)	±5 σ (%)	±6 σ (%)
1	93.32	99.379	99.9767	99.99966
7	61.63	95.733	99.839	99.9976
10	50.08	93.96	99.768	99.9966
20	25.08	88.29	99.536	99.9932
40	6.29	77.94	99.074	99.9864
60	1.58	68.81	98.614	99.9796
80	0.40	60.75	98.156	99.9728
100	0.10	53.64	97.70	99.966
150	–	39.38	96.61	99.949
200	–	28.77	95.45	99.932
300	–	15.43	93.26	99.898
400	–	8.28	91.11	99.864
500	–	4.44	89.02	99.830
600	–	2.38	86.97	99.796
700	–	1.28	84.97	99.762
800	–	0.69	83.02	99.729
900	–	0.37	81.11	99.695
1000	–	0.20	79.24	99.661
1200	–	0.06	75.88	99.593
3000	–	–	50.15	98.985
17000	–	–	0.02	94.384
38000	–	–	–	87.880
70000	–	–	–	78.820
150000	–	–	–	60.000

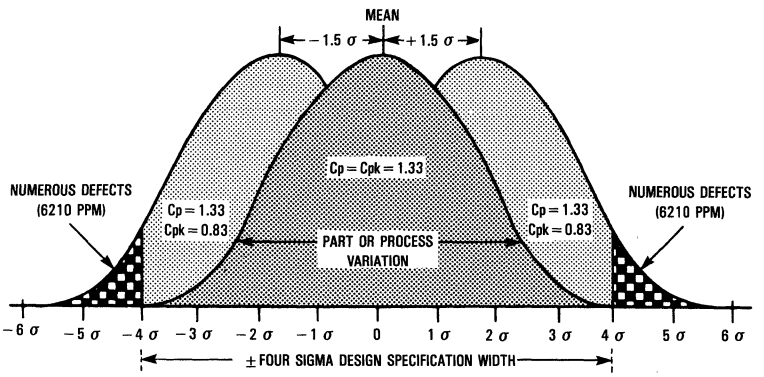

Figure 2a. Four Sigma Capability

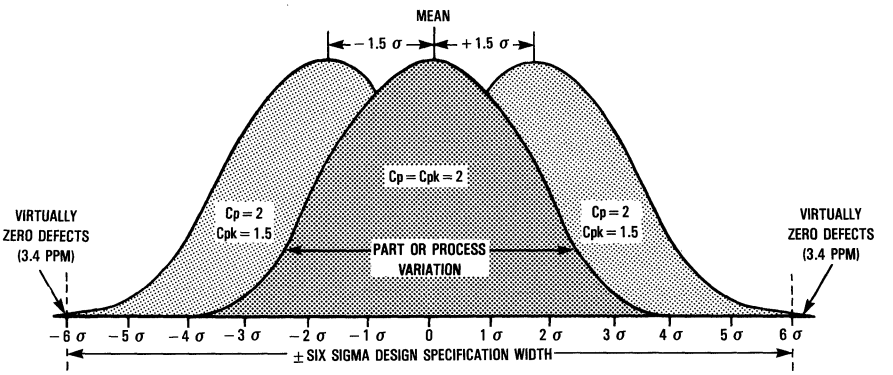

Figure 2b. Six Sigma Capability

9

QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero defects. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY (AOQ) CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \cdot (\text{Lot Acceptance Rate}) \cdot (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices}^*}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \cdot \text{Lot Size}$$

$$\text{Total Number of Devices} = \text{Sum of all the units in each submitted lot}$$

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

10^6 = Conversion to parts per million (PPM)

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235° to 260°C solder dip and microscope inspection of the leads.

RELIABILITY MONITORING

Motorola recognizes the need to monitor established MOS Memory products to maintain the level of quality and reliability demonstrated through the internal and joint qualification processes. Motorola maintains a system of monitor programs that provide monthly feedback on the extensive matrix of Motorola fabrication, assembly, and testing technologies that produce our products. As with qualification activity, great care is taken to assure the accuracy and quality of the data generated.

*All rejects: visual, mechanical, and electrical (dc, ac, and high/low temperature).

RELIABILITY STRESS TESTS

The following summary gives brief descriptions of the various reliability tests included in both reliability qualification and monitor programs. Not all of the tests listed are performed by each program and other tests can be performed when appropriate. Refer to Table 3.

Table 3. Stresses and Typical Stress Conditions

Stress	Typical Stress Condition
High Temperature Operating Life, Dynamic or Static	125°C, 6.0 V
Temperature Cycle	−65°C to +150°C Air to Air
Thermal Shock	−65°C to +150°C Liquid to Liquid
Temperature Humidity Bias	85°C, 85% RH, 5.0 V
Autoclave	121°C, 100% RH, 15 psig
Pressure Temperature Humidity Bias	148°C, 90% RH, 44 psig, 5.0 V
Low Temperature Operating Life	0°C/25°C, 6.0 V

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms that are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in a static bias configuration.

TEMPERATURE CYCLE

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing—to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress in that

the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle.

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H^{3}TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization.

AUTOCLAVE

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test.

PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. The test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions usually employed during the test are a temperature of 148°C, pressure of 44 psig or greater, a relative humidity of 90%, and a bias level which is the nominal rating of the device.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate hot carrier injection effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or other parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. The typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulses = 5.

VARIABLE FREQUENCY VIBRATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. The typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

QUALITY SYSTEMS

A Global Quality System is key to achieving our goal of "Best In Class". Quality systems are implemented in wafer fabrication, assembly, final test, and distribution world wide. Figure 3 depicts Quality Assurance involvement and the techniques applied in the general flow of product and Figure 4 shows Memory Manufacturing locations world wide.

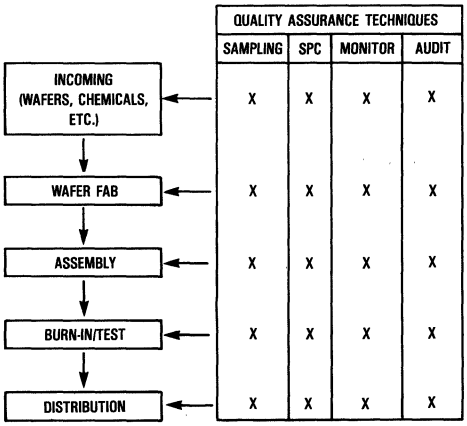

Figure 3. General Product Flow

Direct Customer interaction ensures the receipt of product that meets all of their requirements 100% of the time. In fact, the MOS Memories Reliability and Quality Assurance department has devised a customer advocate list that assigns key Reliability and Quality Assurance personnel to specific customers in order to facilitate any inquiry regarding quality, reliability, or any other issue they may want to discuss.

All processes and procedures that relate to the manufacturing of MOS Memories are fully documented, and regular audits are performed to ensure continuous adherence to proper procedures. We are always striving to produce and reproduce the highest quality product available throughout the world.

MOS Memory Products Division promotes the concept of statistical process controls throughout the entire manufacturing process. This is exemplified by our commitment to in-depth statistical process control training programs for everyone—from the line operator to upper management. Favorable results have already been realized from the initial phases of implementation, with much more to follow.

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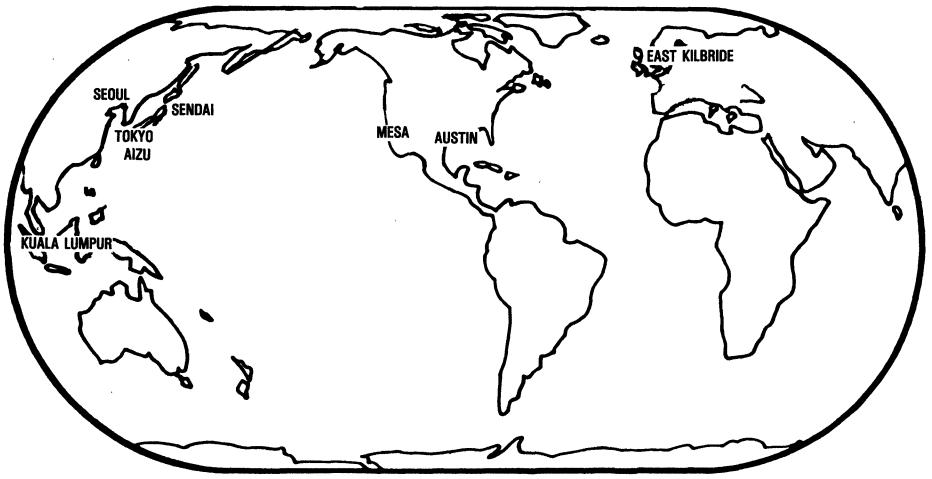

Figure 4. Wafer Fab/Assembly/Final Test Locations

The MOS Memory Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on a timely basis. The MOS Memory Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that the MOS Memory Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all MOS Memory devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proven accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to these criteria and the use of control devices insure that the test results are valid and meaningful.

New MOS Memory devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, design, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola MOS Memory products, our customers can benefit from joint qualification activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend the qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

HISTORICAL PERFORMANCE

Over the course of the last five years, significant achievements have been made on quality and delivery performance. The Six Sigma methodology will assist the MOS Memory Products Division in pursuit of our standard of zero defects and 100% on time delivery.

Figure 5 indicates the product Average Outgoing Quality performance as measured in parts per million.

As of October 1988 our average outgoing quality was below 50 parts per million. We are striving to reach Six Sigma.

1988 MALCOLM BALDRIGE NATIONAL QUALITY AWARD

Motorola won the first Malcolm Baldrige National Quality Award. The award recognizes the achievements of U.S. manufacturing and service companies. The award was established in 1987 to promote quality awareness, recognize the achievements of U.S. companies, and publicize successful quality strategies. Our quality process was examined for corporate quality leadership, information and analysis, planning, human resource utilization, quality assurance, quality improvement results, and Customer Satisfaction. Our fundamental objective—Everyone's overriding responsibility is Total Customer Satisfaction. Six Sigma Quality is a key initiative for the achievement of our fundamental objective.

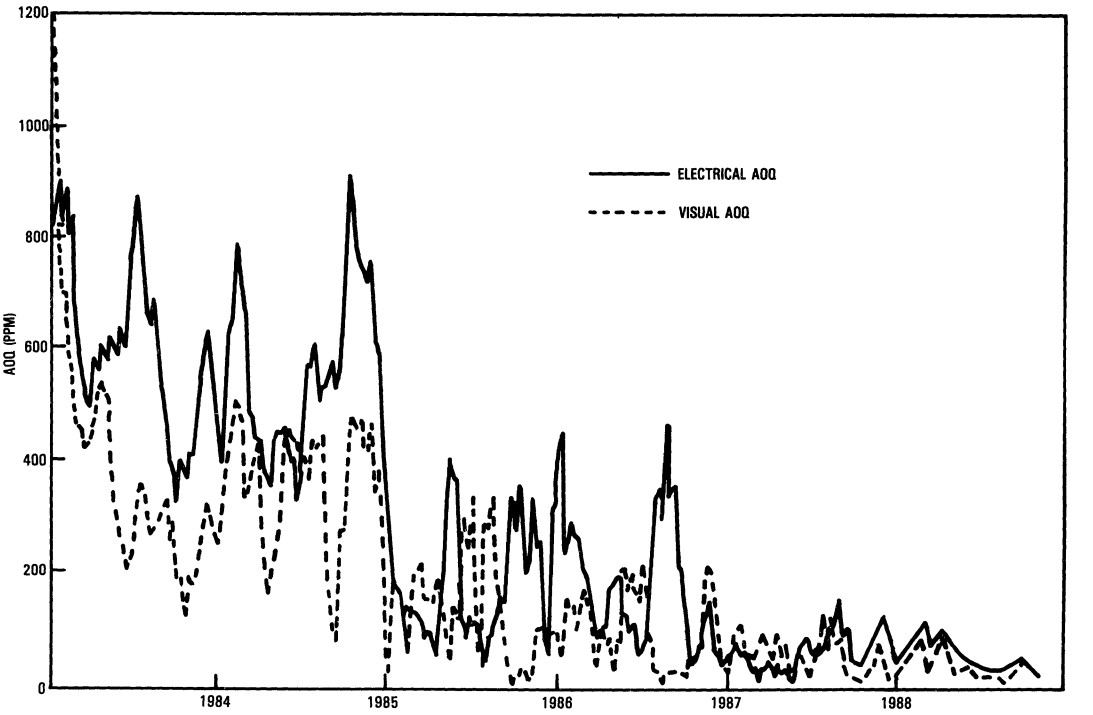

Figure 5. Motorola MOS Memory Products Division Average Outgoing Quality—4 Week Average World Memory

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Applications Information 10

AN987

DRAM Refresh Modes

DRAMs offer the lowest cost per bit of any memory, and for that reason are enormously popular in a wide range of applications. This low cost per bit is achieved with a very simple bit cell design, among other things, but rooted in this simplicity are some inherent drawbacks. One major limitation is the need to refresh each memory bit at regular intervals. This note discusses what refresh is, the reasons refresh is required for DRAM operation, and the various types of refresh available on the Motorola 1M × 1 and 256K × 4 DRAMs. Specific comments refer to the 1M × 1 85-ns DRAM. Refer to specific device data sheets for analogous information on other devices.

The heart of any memory device is the bit cell. A 1M DRAM has 1,048,576 of these cells in the memory array. Each cell holds a single bit of information in the form of a high or low voltage, where high voltage = a binary "1" and low voltage = a binary "0". The DRAM bit cell consists of one transistor and one capacitor. The transistor acts as a switch, regulating when the capacitor will charge and discharge, while the capacitor stores a high or low voltage charge.

All capacitors leak over time, slowly losing the charge stored in them, regardless of how carefully they are constructed. Junction and dielectric leakage are two capacitor discharge paths that are characteristic of the DRAM bit cell, and both are affected by temperature. The capacitor in the bit cell can hold a small charge, on the order of 35–125 fF (fF = 1×10^{-15} farads). As this charge dissipates through leakage paths, the small difference between a "1" and a "0" diminishes. If nothing is done to restore the charge on the capacitor to its initial value, the sensing circuitry on the DRAM will eventually be unable to detect a charge difference and will read the cell as a "0".

Thus, all the capacitors in the memory array must be periodically recharged, or refreshed. Refresh is accomplished by accessing each row in the array, one row at a time. When a row is accessed, it is turned on, and voltage is applied to the row, recharging each capacitor on the row to its initial value. Specified refresh time on the 1M × 1 DRAM is 8 milliseconds; every row must be recharged every 8 milliseconds. This is a vast improvement over refresh times required for earlier generations of DRAMs. The 16K × 1 DRAM required refresh every 2 milliseconds, the 256K × 1 DRAM requires a refresh every 4 milliseconds. Longer refresh times mean more time available for access to memory, and less time required to refresh the device.

Design and operation of the DRAM allow only one row to be refreshed at a time; 512 refresh cycles are required to refresh the entire 1M × 1 memory array. The array is actually 1024 rows by 1024 columns, but it operates electrically like two half arrays of 512 rows by 1024 columns. During refresh, every row is treated as if it runs through both halves of the array, refreshing 2048 column locations (bit cells) per row. This design results in fewer refresh cycles required to recharge the entire array, since only 512 rows need to be accessed, rather than 1024.

Refresh can be performed in either a single **burst** of 512 consecutive refresh cycles (one cycle per row) every 8 milliseconds, or **distributed** over time, one refresh cycle every 15 microseconds (8 milliseconds per 512 rows = 15.6 microseconds per row) on average, or some combination of these two extremes. As long as every row is refreshed within 8 milliseconds, the actual method used is best determined by system use of the DRAM. The burst takes 84 microseconds to complete (165 nanoseconds per row × 512 rows for 85 nanoseconds per device). During this burst refresh time, no memory operations can be performed on the device. Distributed refresh disables memory access for 165 nanoseconds every 15 microseconds.

The 1M × 1 DRAM can be refreshed in three ways: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and hidden refresh. In addition, any normal read or write refreshes all 2048 bit cells on the row accessed. Regardless of the refresh method used, the time required to refresh one row is the random read or write ($\overline{RAS}$) cycle time (t_{RC}). When operating the device in page, nibble, or static column mode, only the row being accessed is refreshed. The device must be in normal random mode to utilize any of these specific refresh methods.

$\overline{RAS}$ only refresh requires external row counters, to ensure all rows are refreshed within the specified time, and externally-supplied row addresses. $\overline{CAS}$ before $\overline{RAS}$ relies on internal row counters and internally generates the address of the next row to be refreshed. Hidden refresh is a variation on $\overline{CAS}$ before $\overline{RAS}$ refresh that holds valid data at the output while refresh is occurring. Whenever the device is in a refresh cycle, neither a read nor a write operation can be performed. Hidden refresh allows the device to be read ahead of refresh, then holds the valid data at the output while refresh cycles are in progress. It appears that the refresh is hidden among data cycles because valid data is maintained at the output.

$\overline{RAS}$ only refresh is performed by supplying row addresses A0–A8 and completing a $\overline{RAS}$ cycle (t_{RC}); switching $\overline{RAS}$ from inactive (high) to active (low), holding $\overline{RAS}$ low (t_{RAS}), then switching back to high, and holding $\overline{RAS}$ high (t_{RP}). A9 is ignored during $\overline{RAS}$ only refresh, since this address normally determines which half of the array is to be accessed. $\overline{CAS}$ must be held high through this $\overline{RAS}$ cycle, hence the name $\overline{RAS}$ only refresh. An external row counter is required for this refresh method. See Figure 1.

$\overline{CAS}$ before $\overline{RAS}$ refresh is performed by switching $\overline{CAS}$ from high to low while $\overline{RAS}$ is high, then switching $\overline{RAS}$ low (t_{CSR}). This reversal of the usual clock order activates an internal row counter that generates addresses to be refreshed; external addresses are ignored in this cycle. $\overline{CAS}$ must be held low (t_{CHR}) after $\overline{RAS}$ transitions to low. After that time it can either be held low or switched to high. See Figure 2. The $\overline{CAS}$ before $\overline{RAS}$ refresh counter test, specified on all DRAM data sheets that offer this type of refresh, is used to check for proper operation of the internal row counters and correct address generation.

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Hidden refresh is a $\overline{CAS}$ before $\overline{RAS}$ refresh that has been initiated during a read or write operation. At the end of a typical read cycle, $\overline{CAS}$ would be switched to high before $\overline{RAS}$, turning off the output. In a hidden refresh cycle, $\overline{RAS}$ is switched to high, concluding the $\overline{RAS}$ cycle (t_{RC}), while $\overline{CAS}$ is held low. $\overline{RAS}$ is held high (t_{RP}), then switched low, beginning another $\overline{RAS}$ cycle. As long as $\overline{CAS}$ is held low, data is valid at the output, resulting in a long read cycle. Since data can be read while the device is being refreshed, the refresh operation(s) appears to be hidden by the read cycle. The same refresh can be performed after a write cycle is initiated. This method of refresh allows refresh cycles to be mixed within read and write cycles. During the refresh cycle, a write operation cannot be performed. See Figure 3.

Refresh is an integral and necessary part of DRAM operation. Substantial improvement has been made in increasing the time between refresh cycles, but as long as the bit cell design utilizes a capacitor, periodic recharging will be required. Three methods of refresh are available on the 1M × 1 DRAM: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and hidden refresh. The Motorola 1M × 1 and 256K × 4 will work in virtually all systems as a result of flexibility provided by this assortment of refresh methods.

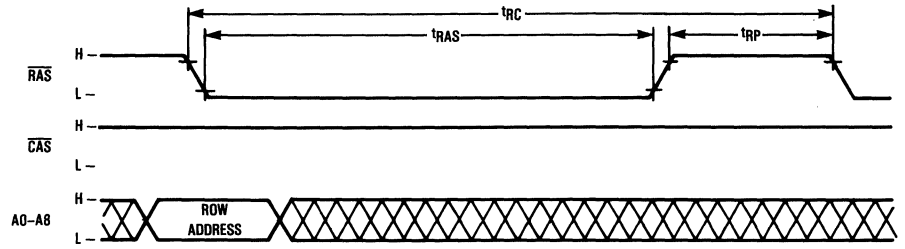

Figure 1. $\overline{RAS}$ Only Refresh Cycle

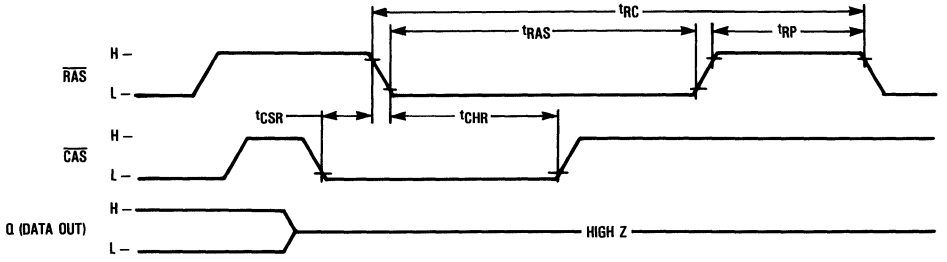

Figure 2. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

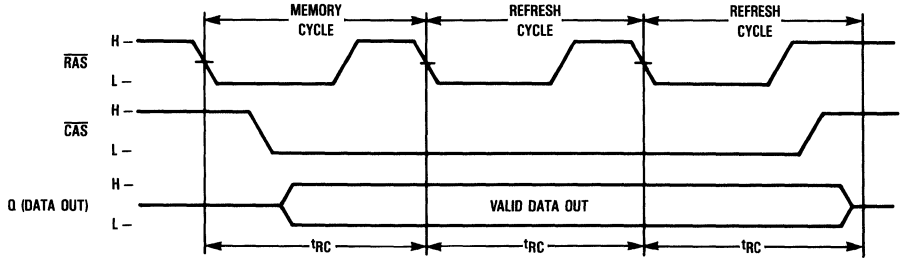

Figure 3. Hidden Refresh Cycle

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AN986

Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit + DRAMs

The 1M-bit and higher density DRAMs offered by Motorola, in addition to operating in a standard mode at advertised access times, have special operating modes that will significantly decrease access time. These are page, nibble, and static column modes. All three modes are available in the 1M × 1 configuration; page and static column modes are also available on the 256K × 4 configuration. Read, write, and read-write operations can be mixed and performed in any order while these devices are operating in either random or special mode.

The comments that follow refer specifically to successive read operations for page, nibble, and static column modes on the 1M × 1 device. The read operation is chosen for sake of simplicity in illustrating these special operating modes. However, decreased access times will occur for all operations, performed in any order, when the device is operated in any of these modes. General operating comments apply to the 256K × 4 device as well.

All of these special operating modes are useful in applications that require high-speed serial access. Typical examples include video bit map graphics monitors or RAM disks. Page mode is the standard, available since the days of the 16K × 1 DRAM. Static column is the latest mode to be made available on DRAMs, and nibble mode first appeared somewhere in between. Page and static column offer the same column location access, but operate somewhat differently. Nibble is unlike either of the other modes, but faster than both in its niche. All modes are initiated after a standard read or write is performed.

Page and static column modes allow access to any of 1024 column locations on a specific row, while nibble allows access to a maximum of four bits. The location of the first bit in nibble mode determines the other bits to be accessed. Nibble mode allows the fastest access of the three devices (t_{NCAC}), all other parameters held equal, at about 1/4 the standard (t_{RAC}) rate. Page and static column access times (t_{CAC}, t_{AA}) are, respectively, about 1/3 and 1/2 the standard rate.

Cycle time is a better indicator of relative speed improvement, since it measures the minimum time between any two successive reads. Cycle time is approximately 1/4 for nibble and 1/3 for page and static column modes, with respect to a

Table 1. Operating Characteristic Comparison

Parameter		Page	Nibble	Static Column	Random
Access Time (ns)*	t_{CAC}	25	—	—	—
	t_{NCAC}	—	20	—	—
	t_{AA}	—	—	45	—
	t_{RAC}	—	—	—	85
Cycle Time (ns)*	t_{PC}	50	—	—	—
	t_{NC}	—	40	—	—
	t_{SC}	—	—	50	—
	t_{RC}	—	—	—	165
Accessible Bits		1024	4	1024	All
Order of Accessible Bits		Random	Fixed	Random	Random
Conditions	$\overline{RAS}$	Active	Active	Active	Cycle
	$\overline{CAS}$ or $\overline{CS}$**	Cycle	Cycle	Active	Cycle
	Addresses	Cycle	N/A	Cycle	Cycle
	Outputs	Cycle	Cycle	Active	Cycle
Time to Read 4 Bits (ns)*		235	205	235	660
Time to Read 1024 Unique Bits (ns)*		51,235	70,400	51,235	168,960

*Values for a 1M × 1 85-ns device.

**$\overline{CS}$ on Static Column.

Page:
4 bit read = $t_{RAC} + 3t_{PC}$
1024 bit read = $t_{RAC} + 1023t_{PC}$

Nibble:
4 bit read = $t_{RAC} + 3t_{NC}$
1024 bit read = $256 \cdot (t_{RAC} + 3t_{NC} + t_{RP})$

Static Column:
4 bit read = $t_{RAC} + 3t_{SC}$
1024 bit read = $t_{RAC} + 1023t_{SC}$

Random:
4 bit read = $4t_{RC}$
1024 bit read = $1024t_{RC}$

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random cycle time of 165 nanoseconds. When operated in these high-speed modes, users will typically access most or all of the bits available to that mode, once the mode has been initiated. Thus the best measure of speed for nibble mode is the rate at which four bits are read, while the rate at which 1024 bits are read is the best measure of page or static column mode. When the actual operating conditions are considered, as described elsewhere, the difference between t_{CAC}, t_{NCAC}, and t_{AA} measurements hold relatively little significance.

Page mode is slightly more difficult to interface in a system than static column mode due to extra $\overline{CAS}$ pulses that are required in page mode. Static column generates less noise than page mode, because output buffers and $\overline{CS}$ are always active in this mode. Noise transients, generated every time $\overline{CAS}$ is cycled from inactive to active, are thus eliminated in the static column mode.

PAGE MODE

Page mode allows faster access to any of the 1024 column locations on a given row, typically at one third the standard (t_{RAC}) rate for randomly-performed operations. Page mode consists of cycling the $\overline{CAS}$ clock from active (low) to inactive (high) and back, and providing a column address, while holding the $\overline{RAS}$ clock active (low). A new column location can be accessed with each $\overline{CAS}$ cycle (t_{PC}).

Page mode is initiated with a standard read or write operation. Row address is latched by the $\overline{RAS}$ clock transition to active, followed by column address and $\overline{CAS}$ clock active. Performing a $\overline{CAS}$ cycle (t_{PC}) and supplying a column address while $\overline{RAS}$ clock remains active constitutes the first page mode cycle. Subsequent page mode cycles can be performed as long as $\overline{RAS}$ clock is active. The first access (data valid) occurs at the standard rate (t_{RAC}). All of the read operations in page mode following the initial operation are measured at the faster rate (t_{CAC}), provided all other timing minimums are maintained (see Figure 1a). Page mode cycle time determines how fast successive bits are read (see Figure 1b).

NIBBLE MODE

Nibble mode allows serial access to two, three, or four bits of data at a much higher rate than random operations (t_{RAC}). Nibble mode consists of cycling the $\overline{CAS}$ clock while holding the $\overline{RAS}$ clock active, like page mode. Internal row and column address counters increment at each $\overline{CAS}$ cycle, thus no external column addresses are required (unlike page or static column modes). After cycling $\overline{CAS}$ three times in nibble mode, the address sequence repeats and the same four bits are accessed again, in serial order, upon subsequent cycles of $\overline{CAS}$:

00, 01, 10, 11, 00, 01, 10, 11, . . .

Nibble mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CAS}$ clock. Performing a $\overline{CAS}$ cycle (t_{NC}) while $\overline{RAS}$ clock remains active constitutes the first nibble mode cycle. Subsequent nibble mode cycles can be performed as long as the $\overline{RAS}$ clock is held active. The first access (data out) occurs at the standard rate (t_{RAC}). All of the read operations in nibble mode following the initial operation are measured at the faster rate (t_{NCAC}), provided all other timing minimums are maintained (see Figure 2a). Nibble mode cycle time determines how fast successive bits are read (see Figure 2b).

STATIC COLUMN MODE

This mode is useful in applications that require less noise than page mode. Output buffers are always on when the device is in this mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. It allows faster access to any of the 1024 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained (see Figure 3a). Static column cycle time determines how fast successive bits are read (see Figure 3b).

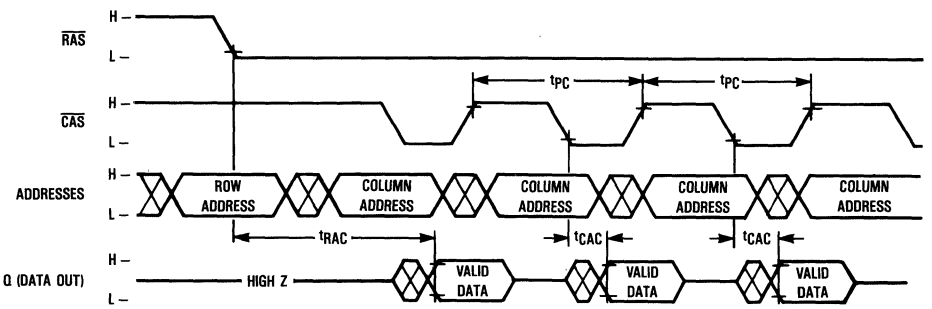

Figure 1a. Page Mode Read Cycle

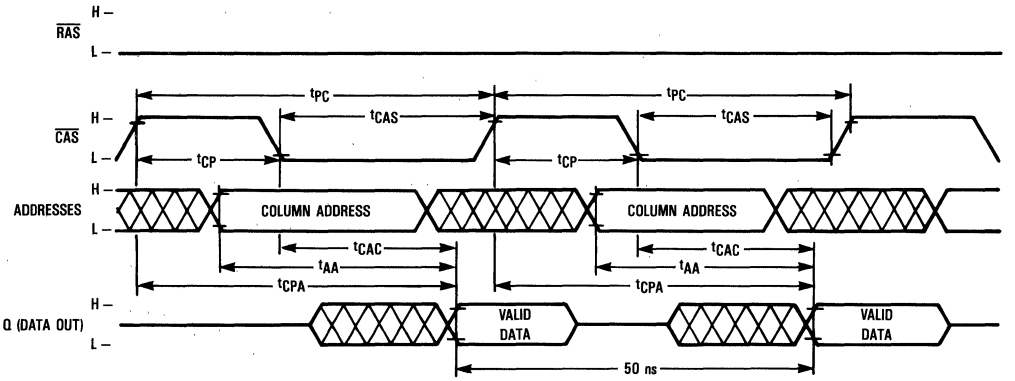

Figure 1b. Page Mode Cycle Minimum Timing

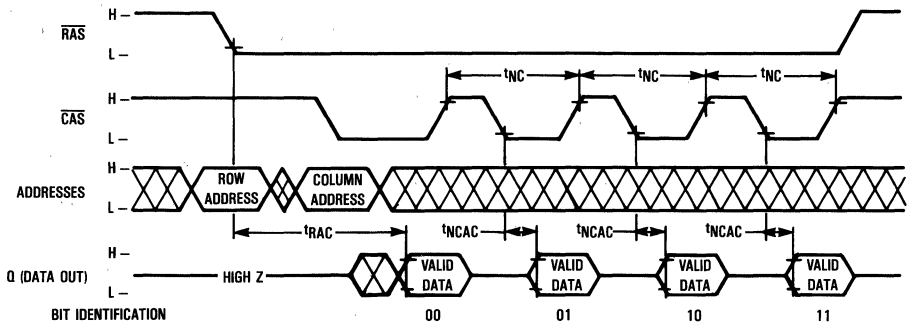

Figure 2a. Nibble Mode Read Cycle

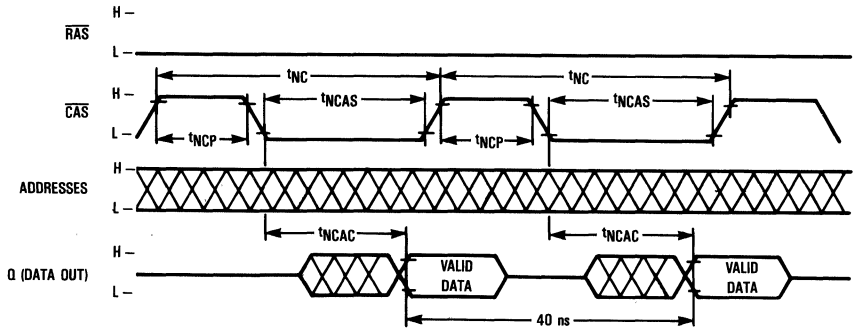

Figure 2b. Nibble Mode Cycle Minimum Timing

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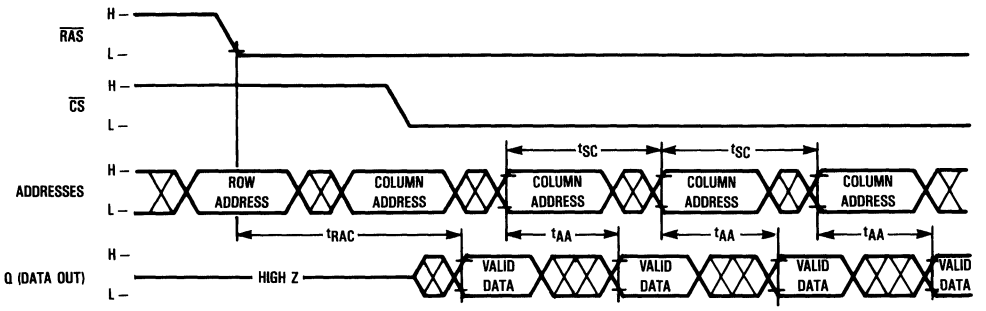

Figure 3a. Static Column Mode Read Cycle

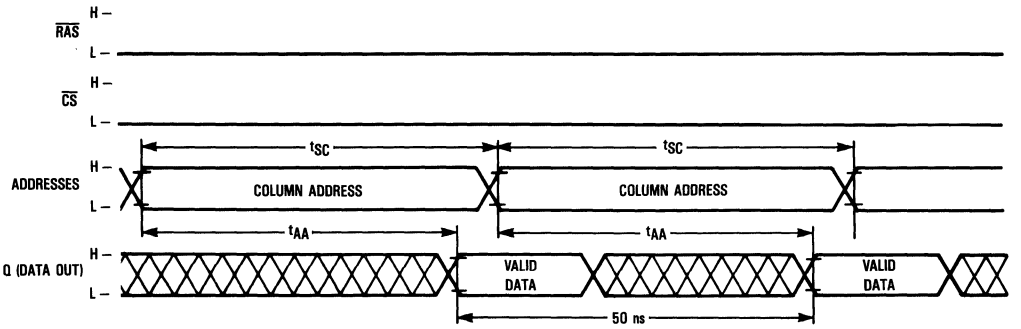

Figure 3b. Static Column Mode Cycle Minimum Timing

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Avoiding Bus Contention in Fast Access RAM Designs

INTRODUCTION

When designing a bus oriented system, the possibility of bus contention must be taken into consideration. Bus contention occurs when two or more devices try to output opposite logic levels on the same common bus line.

This application note points out common causes of bus contention when designing with fast static random access memories and describes ways to eliminate or reduce contention.

WHAT CAUSES BUS CONTENTION?

The most common form of bus contention occurs when one device has not completely turned off (output in a high-impedance state) before another device is turned on (output active). Basically, contention is a timing overlap problem that results in large, transient current spikes. These large current spikes not only generate system noise, but can also affect the long term reliability of the devices on the bus (see Figure 1).

BUS CONTENTION AND FAST STATIC RAMs

Since memory devices are primarily used in bus oriented systems, care must be taken to avoid bus contention in memory designs. Fast static RAMs with common I/O data lines (or any high frequency device with common I/O pins) are the most likely candidates to encounter bus contention. This is due to the tight timing requirements that are needed to achieve high-speed operation. If timing control is not well maintained, bus contention will occur. The most common form of bus contention for memories occurs when switching from a read mode to a write mode or vice versa.

SWITCHING FROM A READ TO WRITE MODE

With $\overline{E}$ low (device selected), on the falling edge of $\overline{W}$ (write asserted) the RAM output driver begins to turn off (high-impedance state). Depending on the input and output logic levels, if sufficient time is not allowed for the output to fully turn off before an input driver turns on, bus contention will occur (see Figure 2a).

Figure 2a shows an example of a RAM trying to drive a bus line low while an input driver is trying to drive the line high. If the situation were reversed (RAM output high and the input driver low), bus contention would still exist.

Of course the obvious way to avoid this type of bus contention is to make sure that the input buffer is not enabled until the write low to output high-impedance (t_{WLQZ}) time is satisfied (see Figure 2b). This specification is usually given on most manufacturers' data sheets.

Another method to eliminate bus contention would be to use $\overline{E}$ to deselect the RAM before asserting $\overline{W}$ (low). This allows the RAM output extra time to go into high-impedance state before the input driver is enabled. $\overline{E}$ and $\overline{W}$ are later asserted low to begin a write cycle (see Figure 2c).

SWITCHING FROM A WRITE TO A READ MODE

With $\overline{E}$ set low (device selected), on the rising edge of $\overline{W}$ (write terminated) the address or data-in changes before the device has had a chance to terminate the write mode. If this should occur, and depending on the input and output logic levels, a bus contention situation could exist (see Figure 3). To avoid address changing type bus contention requires that the address not change till the write recovery specification (t_{WHAX}) is satisfied. To avoid bus contention caused by data changing requires that the data-in remains stable for the duration of the data hold specification (t_{WHDX}). Most of

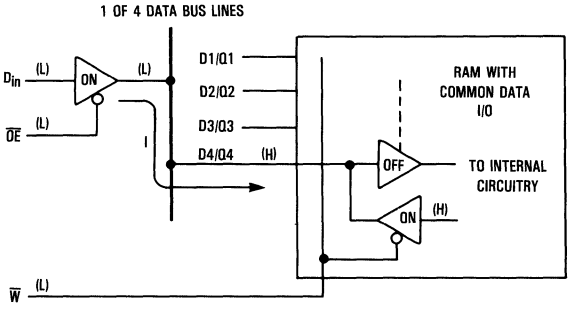

Figure 1. Common I/O Bus Contention

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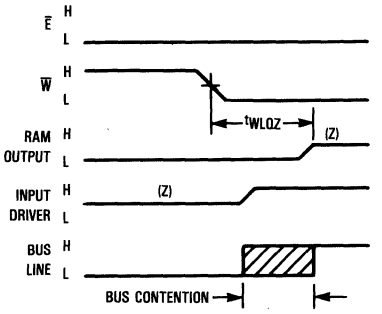

Figure 2a. Input Driver Enabled Prior to Disabling RAM Output

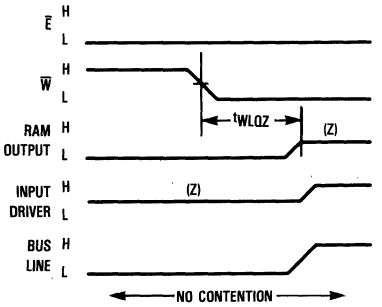

Figure 2b. Input Driver Disabled Prior to Enabling RAM Output

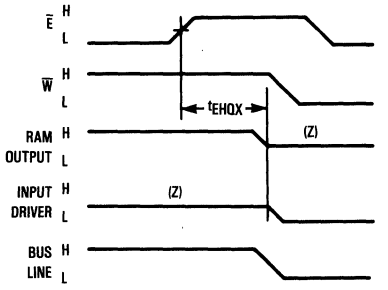

Figure 2c. Using Ē to Avoid Bus Contention

Motorola's fast static RAMs specify write recovery and data hold times of 0 ns. However, it is always a good practice to allow some margin to take care of possible race conditions.

Both of these types of contention could also be avoided by taking Ē high prior to taking W̄ high. This will give the RAM output driver time to go to a high-impedance state before W̄ goes high. In this case Ē is used to terminate the write cycle instead of W̄ (see Figure 3c).

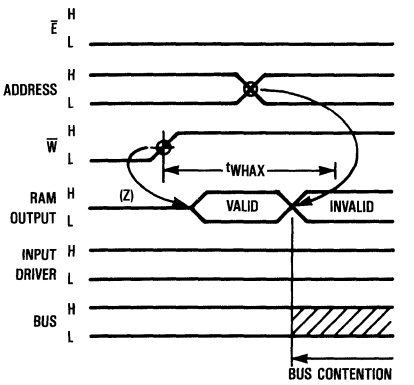

Figure 3a. Data Setup Time Violation

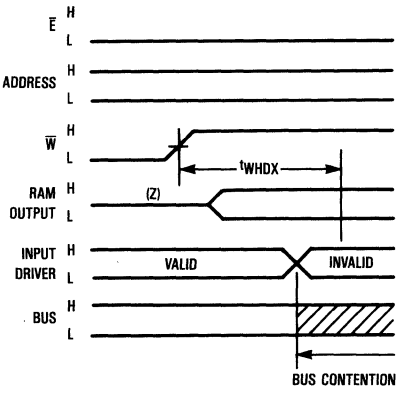

Figure 3b. Data Hold Time Violation

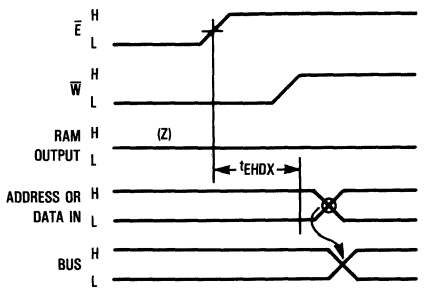

Figure 3c. Using Ē to Avoid Bus Contention

OTHER WAYS TO ELIMINATE BUS CONTENTION

If the RAM has an output enable pin (G̅), synchronizing schemes can be incorporated to help eliminate bus contention. Taking G̅ high will ensure that even when the RAM is in a read mode the output will be in a high-impedance state. This will allow the input driver to be enabled longer.

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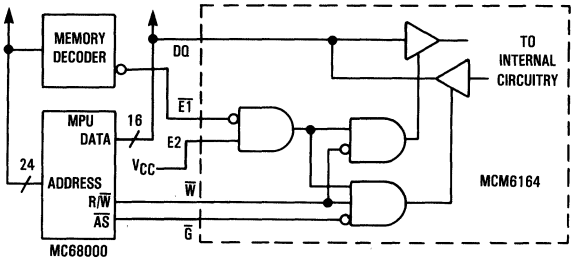

Figure 4a. Using $\overline{G}$ to Avoid Bus Contention

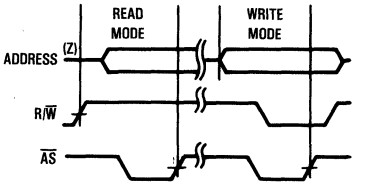

Figure 4b. Timing Diagram of the MC68000

Most advanced microprocessors, such as the MC68000 and MC68020, have asynchronous bus control signals that take advantage of fast memory devices with output enable pins. Figure 4 shows one way to avoid bus contention using a Motorola MC68000 interfaced to a Motorola 45-ns MCM6164.

A more obvious way to eliminate bus contention is to use slow memory devices. Slow memories have loose timing requirements that allow devices to fully turn off before another device turns on. Of course this defeats the whole purpose of fast static memory devices.

Another obvious way to eliminate bus contention is to use memory devices that have separate data I/O pins. In this way the R/$\overline{W}$ signal from the microprocessor can control a buffer device to eliminate bus contention (see Figure 5). However, the industry is demanding RAM with common I/O because these devices cost less and save system real estate.

Common I/O devices reduce package size since fewer pins are needed. Smaller packages result in less PCB space requirement. Common I/O devices also eliminate the need for an extra buffer with its associated expense and space requirement. In general fast static RAMs configured greater than a X1 will have common data I/O pins.

Another popular way to reduce bus contention is to put a current limiting series resistor on each bus line (see Figure 6). The series resistor does not eliminate bus contention, but it helps reduce the large transient currents associated with bus contention. However, series resistors increase access time as well as increasing component count. The added access time depends on the total bus capacitance (including the capacitance of the devices on the bus) and the total bus resistance. The added delay should be added on to the point at which bus contention ceases. The following formulas can be used to determine the added access delay.

$$t_{HL} = R_L \cdot C_L \cdot \ln \frac{V_{in}(initial) - V_{in}(final)}{V_{IL}(max) - V_{in}(final)}$$

$$t_{LH} = R_L \cdot C_L \cdot \ln \frac{V_{in}(final) - V_{in}(initial)}{V_{in}(final) - V_{IH}(min)}$$

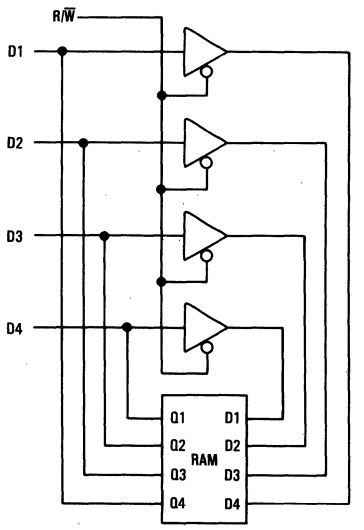

Figure 5. Separate I/O Buffer

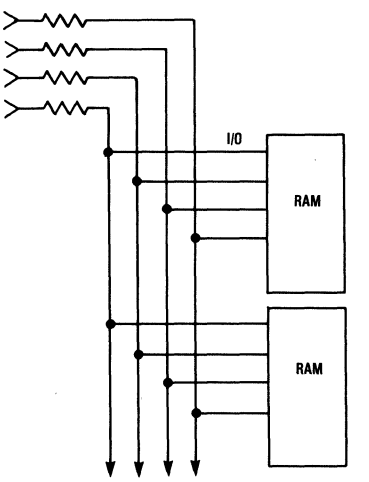

Figure 6. Using Series Terminating Resistors

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Generally the value of the resistor should be around 100 ohms. The larger the resistor the less the transient current generated, but the greater the delay. Using a 150-ohm resistor will limit the current flow to less than 20 milliamperes while adding approximately 3 nanoseconds extra access time. However, note that even with series resistors bus contention duty cycle must be minimized to reduce EMI and bus ringing.

Although it is very important to reduce bus contention, CMOS memories can tolerate more bus noise generated by bus contention than can bipolar memories, due to the excellent noise immunity advantage of CMOS over bipolar technology. However, even when using CMOS memories, large destructive transient currents generated by bus contention can still occur.

CONCLUSION

Bus contention must be taken into consideration in most bus-oriented system design. The occurrence of bus contention generates large transient currents that produce system noise and could also affect the system's long term reliability.

Fast random access memories with common data I/O pins are very susceptible to bus contention due to tight timing requirements. Although it is almost impossible to totally eliminate bus contention, it must be the goal of the system designer to minimize bus contention.

AN973

Avoiding Data Errors with Fast Static RAMs

Microprocessors are now capable of 20–25 MHz. This places a great demand on SRAMs to supply super-fast access times. Today's sub-100-nanosecond SRAMs in production are rapidly moving to sub-50 nanoseconds as yesterday's prototypes ramp into production, and sub-25 nanoseconds is just on the horizon. This need for high-speed SRAMs is amplified by the fact that setup, hold times, and cycle edge accuracies do not usually improve at the same rate as the clock frequency. There is help on the way in terms of application specific SRAMs that put on chip some of the "glue" features that eliminate gate delays caused by decoders, drivers, or clock signals; but for now, the main burden will fall upon SRAM designers to make up for the "lost time" in the shorter cycles. Some of the tools of the SRAM designer are improved processes, tighter design rules, and improved circuit techniques such as address transition detection. When you combine all of these features into a high performance SRAM, you no longer have the bistable flip-flop of yesterday but a highly tuned circuit that is more closely related to a DRAM. This is where the system designer can help. Although SRAM designers are doing everything possible to make the devices stable and noise immune, there is no substitute for a good solid system layout and design. The following discussion gives system designers some insight into potential trouble areas from a component engineering viewpoint.

CHARACTERISTICS OF HIGH-SPEED BUSES

When data is transmitted over long distances, the line on which the data travels has to be considered a transmission line. A long distance is relative to the rate at which data is being toggled. Address and data buses associated with high-throughput microprocessors (e.g., M68000 family) must also be thought of as transmission lines, since it is not uncommon for these processors to run bus cycles of 40-nanosecond periods or less.

Other features of high-end microprocessor buses are that they tend to operate in harsh, noisy-type environments, and most of these buses are unterminated. A high-impedance, unterminated bus line acts just like an antenna. It not only radiates EMI, it can also receive EMI. This can result in bus ringing, crosstalk, and various other noise associated problems. The more transmission lines a bus has, the more antennas to pick up and radiate noise. Of course, the best way to reduce this EMI is to ensure that the bus is properly terminated into a low-impedance load. This low-impedance load could be in the form of a pull-up or pull-down resistor tied to each bus line. Ideally, the termination resistor should be equal to the characteristic impedance of the bus line. A transmission line terminated into its own characteristic impedance has the best incident wave switching as well as the least amount of reflection.

Since an unterminated bus looks almost entirely like a capacitive load, the larger the resistor value the slower the rate at which data can be presented to the receiving device. This is due to the time it takes to charge and discharge this capacitive line through the termination resistor. If a small value resistor is used, the charging/discharging time delay can be minimized (t = RC). However, the smaller the resistor the greater the power consumption through the resistor. Also, if the resistor value is too small, its value will approach that of the source resistance of the transmitting device, which could lead to a degradation of noise margin to the receiving devices. A resistor value between 1 kilohm and 10 kilohms is usually adequate. The actual value should be optimized through experimentation (see Figure 1).

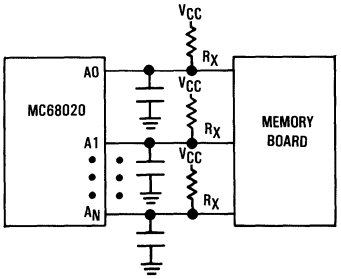

Figure 1. Microprocessor Address Bus with Pull-Up Resistors

HIGH SPEED SRAM DESIGN TECHNIQUES

In order to speed up access times of high-speed RAMs, many new design techniques have surfaced. One of the most innovative techniques to emerge is known as address transition detection (ATD) circuitry. Since row address access times are typically slower than column address access times, this circuitry originally used the row addresses to trigger a clocking sequence that restored bit lines, shorted data lines, equalized sense amplifiers, and threestated the output as the output buffers were equalized. This meant that many of the internal transistions could be completed by the time that the signals were decoded and propagated through the device seeking the proper cell and outputting data. This then made row and column access times much more equal and eliminated one of the speed bottlenecks. This scheme also has the added advantage of reducing power consumption because the static bit line loads can be reduced in size by utilizing a parallel equalization that is also generated at the ATD initiation and used to pull up the bit line 0 before selection of the new word line. Since

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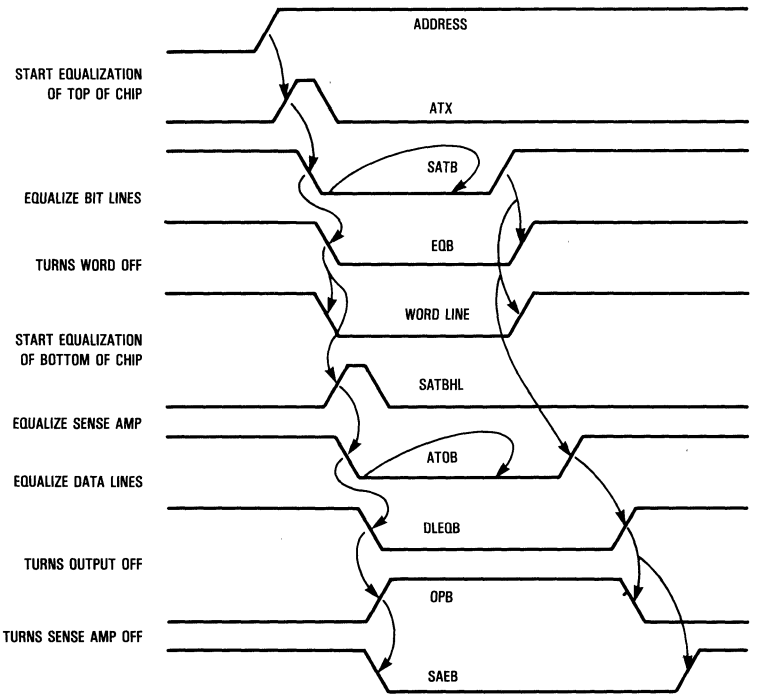

Figure 2. Address Transition Detection Timing Chain

its inception, ATD has been expanded and is now activated by all addresses and chip select pins instead of just row addresses. A typical timing chain, as shown in Figure 2, applies to Motorola's MCM6164 8K×8 SRAM and exemplifies the clock sequence dependency.

ATD has been shown to be very effective as a performance enhancer and will remain a valuable tool for designers, but it can be seen that we now essentially have a clock-activated part. What happens if addresses are floated or oscillate at a frequency greater than the ATD response? What happens if addresses are skewed, thereby getting successive ATD initiations? There is also the case of signals being gated from numerous sources, in which the address may start in one direction and then reverse several times before it finally seeks a valid high or low level. Circuit designers believe that these potential problems have been resolved over the last few years as testing techniques and circuit simulations have wrung out the infinite number of application variations. However, there is a simple, foolproof way that system designers can eliminate any potential for this type of a problem. Deselect the device during address transitions (see Figure 3).

Since new design techniques have made chip select access times equal to address access times, system designers can take advantage of this and improve reliabilty of their system by increasing overall immunity to a noisy environment. This can cover a host of potential board-induced problems from oscillating multiplexer or driver units, to spurious address glitches put out by MPUs.

Another design improvement is related to rise and fall times on the output levels, known by circuit designers as di/dt. This is the inductance associated with the changing current as loads are charging and discharging. This inductance is coupled back to the device, and through connections and bus resistance can cause the power supply or ground to change drastically. This is pushed to the limits as output drivers become more powerful, and is especially aggravated by multiple I/O devices like byte-wide SRAMs which may have all eight data lines switch from all 0s to all 1s or vice versa. These spurious noise spikes on the power lines can affect the data contents of the device, as well as any other device sharing the same power and ground buses (see Figure 4). Circuit designers have developed circuitry that has a feedback loop that controls the rise and fall time just enough to minimize overshoot, undershoot, and ringing. This di/dt is the inherent reason why byte-wide SRAMs are typically 4–5 nanoseconds slower than single output devices.

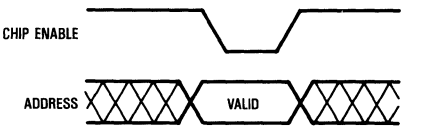

Figure 3. Deselection of Device During Address Transition

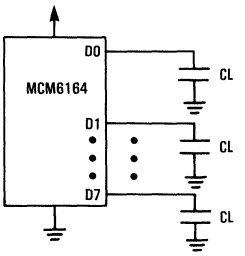

Figure 4a. MCM6164C Data Bus

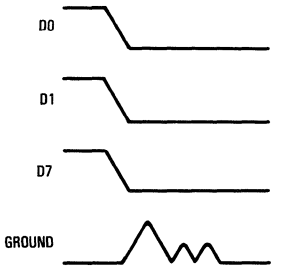

Figure 4b. Ground Bounce When Data Switches from All 1s to All 0s

PCB POWER FEED CONSIDERATIONS

Another source of noise can be inadequate power feeds and power supply decoupling. Large ground planes should be used to reduce both inductances and resistances. The resistances of the power supply lines should be less than 0.1 ohm. If the inductances or resistances of the power supply lines become significant, V_{CC} or ground bounce can occur. Since all inputs are referenced to ground, gate input thresholds could be exceeded, causing data errors to be generated. An excellent PCB design is one that incorporates a multilayer board. One layer should be entirely devoted to a ground plane.

The use of good-quality decoupling capacitors can help to keep noise off the power lines. A value between 0.01 microfarad and 0.1 microfarad (use 0.1 microfarad for ×8 organizations) should be used for each RAM. This capacitor should be located as close to the RAM power pins as possible. When using IC sockets, it is recommended that sockets with gold-plated copper contacts and built-in decoupling capacitors be used.

A large value capacitor (≥1 microfarad) should be used on each V_{CC} line. The purpose of this capacitor is to provide for sudden current demand (current surges) from the power supply.

Figure 5 illustrates a typical memory board design.

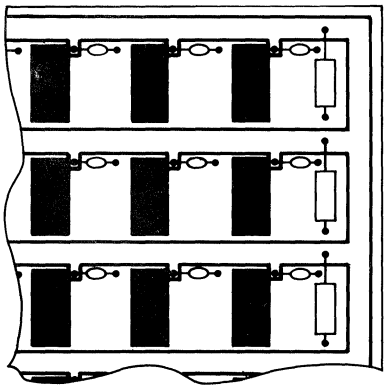

Figure 5. Typical Memory Board

SUMMARY

Digital transmission line theory must be taken into account when designing high-frequency buses. A high-impedance, unterminated bus behaves much like an antenna, receiving as well as transmitting EMI. The use of termination resistors on these buses can reduce EMI. Many innovative designs have evolved to speed up access times of fast static RAMs. One of the more innovative designs is that of address transition detection circuitry. Most high-speed RAMs today use this technique to decrease access time. Good PCB power feed design, as well as the judicious use of decoupling capacitors, is essential for optimum performance from fast static RAMs.

Much of the time, the problems caused by a marginal device, system layout, or pushing for the last nanosecond is an intermittent random type of problem that could result in either destroyed data or access time push-out. If you are having a problem, call Motorola MOS Memories in Austin, Texas, (512) 928-SRAM (928-7726). We are on your design team!

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AN984

25 MHz Logical Cache for an MC68020

Prepared by:
Motorola — East Kilbride, Scotland

INTRODUCTION

As the speed of the MC68020 processor increases it becomes more difficult and more expensive to provide large amounts of no-wait states memory. The addition of a logical cache in a memory management based system then becomes a more viable alternative to the problem. For a typical 25 MHz MC68020 system the incorporation of a no-wait states cache is one of the most economical ways in which the true performance attainable from this particular processor can be achieved.

CACHE DESCRIPTION

The cache described in this application note is a 32K byte (8K long words) direct mapped logical cache. The cache is organized such that both supervisor and user, program and data accesses are stored. The entries are tagged appropriately with the function code lines. To avoid any stale data problems that may occur with the data the cache update logic includes a 'write through' mechanism that forces any data writes to update both the memory and the cache. The cache operates with no wait states with a 25 MHz MC68020.

BLOCK DIAGRAM DESCRIPTION

The cache can be broken down into several functional parts as follows:

- tag RAMs
- data RAMs
- control logic
- entry update mechanism

The cache is organized as 8K long word entries (see Figure 1) which are referenced by a 22 bit TAG field. This TAG is made up of the upper address lines (TA15–TA31), the function codes (TFC0-2) and the size pins (TSIZE0-1). By incorporating the size pins into the TAG field means that the data entry can be validated even if it were referenced as a misaligned data transfer. The function codes allow the entries to be referenced separately with respect to user/supervisor and program and data entries.

The cache mechanism will begin operation as soon as an address becomes valid on the logical address bus. This address accesses the TAG RAM within the cache and the corresponding entry is compared with the relevant section of the logical address bus (LA15-LA31) and the control bus (FC0-2, SIZE0-1).

If this comparison is valid then this gives an indication to the comparator logic that a valid entry may be present within the cache data RAMs.

To determine whether this data entry is indeed valid a simultaneous access is made to the VALID bit RAM with the lower section of the logical address bus (LA2-LA14). If the entry in this VALID RAM is a logic 0 then this indicates that the corresponding data entry at that cache address (LA2-LA14) is a valid entry.

Access to that data item can then be made on the condition of several control signals (e.g. R/W*, CACHE-E*, etc.) and the data buffers to the system data bus will be enabled. This is termed as a CACHE HIT.

Conversely, if the entry in the VALID bit RAM was a logic 1 then this would indicate that the corresponding data item was not a valid cache entry and so the isolation data buffers would not be enabled to the system bus. This is termed as a CACHE MISS.

When the cache detects a HIT then the bus cycle is completed from the data RAMs and the system operates with no wait states.

If on the other hand the cache detects a MISS then the processor has to fetch its data from external memory which by its nature will be slower and will incur wait states.

To facilitate the data fetch from external memory the cache mechanism forces the processor to do a RETRY of the MISSed bus cycle. This retried bus cycle will then go out to external memory and fetches the relevant data item which will be latched by the processor and also used to update the cache. Subsequent accesses to this address will then find the data resident in the cache.

To preserve data integrity a CACHE MISS is also generated by a data write cycle. On writing to an address the cache forces a MISS such that the data item will be written to the cache in addition to the external memory. Subsequent data reads at this location will find that the data item is resident and is the most recent version.

Forced CACHE MISSes are also generated when the logical

address is detected as being a peripheral access (e.g. serial I/O device) or when the processor is executing a CPU space cycle (e.g. interrupt acknowledge).

CACHE CONTROL MECHANISM

The cache hit signal (CHIT*) is generated as a result of the comparison of the TAG data, the VALID bit and various control signals. When the logical address from the processor becomes valid the cache TAG RAMs are enabled and the TAG data is produced for comparison.

These TAG RAMs are addressed as an 8K long word bank and so logical address lines LA2 to LA14 are used.

The TAG RAM itself contains information relating to the bus status of the cached item. This bus status consists of a section of the logical address bus (LA15-LA31) and some control signals (FC0-2, SIZE0-1). When these TAG RAMs are accessed this previous bus status is compared with the existing bus to detect if there is a match.

Comparators U215, U216 and U217 (see Figure 4) are used to compare this information and if there is a match the outputs Oa=b (pin 19) will be asserted.

The assertion of these three comparator outputs is then conditioned by various other factors to determine whether a cache hit signal should be generated.

While the TAG RAMs are being accessed by logical address lines LA2-LA14 a VALID bit RAM is also accessed. The information contained in this VALID bit determines whether or not the cache data is valid. When the cache is enabled all the entries in the VALID RAM are set to logic 1 to indicate that there are no valid entries in the cache.

Subsequent memory accesses then cause a cache miss which results in a cache entry being made. When this cache entry is made the status of the bus (LA15-31, FC0-2, SIZE0-1) is saved in the TAG RAM at the location pointed to by the cache index (LA2-14). The information on the data bus is then saved in the data RAMs at address with cache index LA2-14 and the corresponding VALID bit entry is also set (i.e. the cache entry is marked as being valid).

Subsequent accesses to that address will then cause the TAG address comparators to assert their outputs and the VALID bit to be set. The assertion of the cache hit signal (CHIT*) is then dependent upon the status of several other control signals such as cache enable (CACHE-E*), CPU space and peripheral access (IOEN*). Accesses to CPU space are not cached because of the problems that might arise when servicing interrupts or accessing coprocessors. In addition access to peripheral devices (indicated by the signal IOEN*) are not cached because of the read write nature of some peripheral device registers.

When these signals are taken into account the resultant assertion of the cache hit signal (CHIT*) will then cause the processor to complete the bus cycle with no wait states.

Control of the cache is facilitated by three hardware primitives: Cache Enable, Cache Disable and Cache Clear. These primitives are initiated by accessing a specific address within CPU space which is not used for any other CPU space functions.

On requesting a cache enable function the mechanism causes the VALID bit RAM to be set to logic 1's, indicating no valid cache entries, and then assert the CACHE-E* signal to the rest of the system.

The cache disable function simply negates this CACHE-E* signal.

The cache clear function is included to allow the support of multi-tasking software. On initiation of the cache clear function all entries in the VALID bit RAM are cleared so emptying the cache. This is useful where the software has to perform a context switch.

CACHE CONTROL LOGIC

The Cache control logic allows the software programmer to enable the cache, disable the cache and to clear the cache contents. Accesses to the control logic can only be done under CPU space. This prevents accidentally writing to the control logic during normal operation (the SFC and DFC registers are programmed for CPU space with the MOVEC instruction, and the MOVES is used in writing to the control logic). Hence only the supervisor mode of operation can control the cache.

The address lines LA24-LA26 are used to decode the cache control functions, these being inputs fed to an 74LS138 U241 (see Figure 3). In addition to these addresses in CPU space, the programmer should also select an area of memory that will not cause contention with the normal MC68020 CPU functions.

An example decode could be $1070000 ($ is used to represent a hexadecimal number) for clear cache, $2070000 for disable cache and $4070000 for enable cache.

Cache Enable

The cache is enabled by accessing to a CPU address similar to the one given above, the data being irrelevant. On enabling the cache all entries are made invalid. This ensures that no stale data problems are created from accesses when the cache was previously enabled.

The output from U118D (see Figure 3) is used to enable a sequencer consisting of three 4-bit binary counters: U246, U247 and U248. These counters are used to increment the address bus to set the valid bits to all 1's (entry is invalid). The addresses are presented to the valid RAM U259 via the latches U249 and U250, the outputs from these being enabled at the same time as a write to enable the cache. Also during this sequence the logical address bus to this RAM is tri-stated from the RAM's address bus by U243 and U244.

Under normal operation the latches U243 and U244 are enabled and U249, U250 are disabled allowing the valid RAM to be addressed from the logical address bus. The 12-bit sequence clears 4 K entries in the cache (each entry is a long word).

The sequence is repeated twice to clear the whole 8 K entry cache. The two D-type flip flops U251B and U251A are used to write first to the upper 4 K then the lower 4 K entries.

At the end of the cache clear sequence the cache is enabled via the S-R flip flop U257D and U118C. The CACHE.E* is then used in the comparator logic to indicate that the cache is enabled. In addition the DSACK0* and DSACK1* is returned to the MC68020.

As far as the processor is concerned the cache clear mechanism can be thought of as a long instruction. The valid

RAM latches data with respect to the sequencer clock (40 MHz for 25 ns SRAM's) and a logic 1 is latched on each falling edge of this clock.

A logic 1 is written into the valid RAM when: the sequencer is enabled; it is the falling edge of the 40 MHz clock and the WRITEN* signal from the entry update mechanism is high (U258C, U263A and U219D). This logic is also used to write a logic 0 into the valid RAM during normal operation.

To prevent external bus contention when the cache is being written to, a signal ADDBUFDIS* is generated which can be used to disable external address buffers. The CMISS signal should be used to disable the external address buffers during a cache hit.

Cache Clear

The cache clear mechanism is used to allow the operating system to perform a context switch. A cache clear command will produce the same output as the enable cache command.

Using the 40 MHz clock gives a context switch time of approximately 0.025 x 1024 x 8 = 205 us. If this is unacceptable the mechanism can be speeded up by using several valid bit RAMs of lower density in parallel, or using a RAM with a clear feature.

Cache Disable

This command produces an input into U240B to set the S-R flip flop to cache disable (CACHE.E* set to a logic 1). The reset signal is also fed into U240B to ensure that the cache is always disabled at reset.

ENTRY UPDATE MECHANISM

This section of logic (see Figure 2) is used to control the cache mechanism for updating entries in the cache. In addition, the logic will produce control signals used to latch data into the Tag and Data RAMs and control the isolation data buffers for the cache (U236 - U239 in Figure 5).

The mechanism used to update the entries in the cache is only enabled on a read cycle (R/W* signal into U261D) and when the cache is enabled (CACHE.E* signal into U261C).

The control logic is required to perform three distinct operations:

- On a write cycle the WRITEN* signal should be asserted to latch data into the RAMs to perform a write through operation. When the address is next accessed it will reside in the cache.
- On a read cycle that does not generate a cache hit, the logic needs to initiate a retry operation to enable the cache to latch the data which is being read by the MC68020.
- Thirdly, on a read cycle, which causes a cache hit, the bus cycle needs to be terminated to allow zero wait state operation at 25 MHz from the cache.

Write Cycles

Assuming the cache is enabled then on a write cycle the output from U240D produces logic 0 (the output from U261C will be logic 0). This output produces a signal INHIBIT* which prevents the cache returning DSACK0*, DSACK1*, HALT* and BERR* (U256A, B, C, D), used for read cycles (see Figure 2).

A signal FORCEW* is also generated via U258B and U219C to control the output enable of the cache isolation buffers to allow data to be routed to the cache data RAMs (see Figure 5).

The WRITEN* signal is finally generated from U258A to produce the W* enable for the TAG and DATA RAMs. WRITEN* is also used to enable the buffers: U212 - U214, to route the current logical address, function codes and size lines into the TAG RAMs (see Figure 4).

Two banks of RAMs are used to obtain an 8 K entry long word cache; the lower bank of RAMs are enabled with LA14* from U255C and the upper bank is enabled by LA14. This is needed to allow 25 MHz operation (25 ns SRAM - MCM6268-25 -are used as shown in Figure 4).

On the assertion of DSACK0*, DSACK1* from the external physical memory the two D-type flip-flops U235A and U253B (see Figure 2) are used to negate the WRITEN* just after the falling edge of the processor clock S4 (just after the MC68020 latches data). On the negation of WRITEN*, tag data is written into the tag field.

The information on the data bus is latched into the cache data RAM and the tag buffers and data isolation buffers isolate the cache from the system busses. This section together with the whole entry update mechanism must operate logically very quickly hence FAST logic is used throughout.

Read Cycle with a Cache Miss

Timing diagram 1 shows the cache sequence when a cache miss occurs. From this diagram it can be seen that the addresses on the address bus do not become stable until 5 ns into S1 worst case. At this point it will take 25 ns to obtain information from the TAG data RAMs (the RAMs are permanently enabled).

In addition to this there is a delay through two levels of comparator (U215 - U218). This gives an absolute maximum propagation delay time of 46 ns after the address bus is stable before a valid CHIT* signal is generated. With the above conditions a valid cache hit signal (CHIT*) should be asserted in the middle of S3 for a TAG match. The entry update mechanism uses this information to determine if there is going to be a cache miss or a cache hit.

In the case of a cache miss the following sequence of events are executed: DSACK0* and DSACK1* are asserted by the assertion of the MC68020 AS* (U255B) by U256A and U256B as shown in Figure 2. The INHIBIT is set to a logic 1 by U261C, U261D and U262A. U252A is then used to bring U252B out of RESET on the falling edge of S2. This D-type is then used to sample the CHIT* signal in the middle of S3. In the case of a cache miss the D input will still remain high, forcing the cache miss signal CMISS to go high. This is used to enable external data buffers for the MC68020. This causes the BERR* and HALT* signal to be asserted simultaneously to request a retry cycle (via U261B, U256C and U256D). This takes advantage of the MC68020's ability to recognize a late retry if spec 27A is satisfied. (Note that

68020 inserts an additional 3 clock cycles after S5 of this cycle).

On the termination of this bus cycle all signals are negated as shown in the timing diagram, with the exception of the INHIBIT. This is because on the rising edge of LAS* the output from Q* of U269A is fed back to the input to produce a low INHIBIT signal for the following retry cycle This low INHIBIT signal prevents the DSACK0*, DSACK1*, BERR* and HALT* lines from being asserted by the cache during the retry cycle.

Timing diagram 2 shows the retry cycle. The length of this cycle is determined by the actual physical device being read so it is shown as an unknown number of wait states. The same cycle is repeated as above, however, during this cycle INHIBIT has been asserted causing FORCEW* (force a write to the RAMs) and WRITEN* to be asserted. This has the effect of updating the cache on the read cycle by forcing the cache to latch the addresses, function code and size signals to the TAG RAM and the DATA bus contents into the data RAMs.

The buffers U236 - U239 are enabled by (CHIT*) ANDed with (FORCEW*) and the direction is controlled by CHIT*. In this case CHIT* is a logic 1 causing data to be written into the RAMs. The buffers U212 - U214 are enabled by the WRITEN* signal.

On return of the DSACK0*, DSACK1* from the physical system, the WRITEN* signal is negated (via U257A, U255C, U253A, U253B, U219B and U258A) to latch data into the RAMs just after the falling edge of S4.

In addition to this all the signals are negated at the end of the cycle and the INHIBIT signal returns to a logic 1 level on the negation of LAS* (U262A and U240D).

Read Cycle with a Cache Hit

When a read cycle occurs at an address which has a corresponding input in the cache, a cache hit will occur. This cycle is similar to the one above except the CHIT* signal from the comparators U215 - U218 is asserted by the middle of S3, setting CMISS inactive (output from Q of U252B is set to a logic low) and forcing the external data buffers to be disabled preventing data bus contention. The BERR* and HALT* are also prevented from being asserted by U261B so no late retry cycle is signalled to the MC68020.

Finally, the cache data RAM isolation buffers U236 - U239 are enabled and the direction is selected to be output from the RAMs to the data bus. As there is no bus activity which stops the recognition of DSACK0* and DSACK1*, this read cycle by the MC68020 from the cache is performed in zero wait states at 25 MHz.

At the end of the cycle all the signals are negated for the next bus cycle.

CONCLUSION

The design of a 25 MHz logical data cache to interface between the processor and an MMU involves the use of very fast logic and static RAMs for zero wait state operation. The RAM access speed required in this application is 25 nS to allow no wait states operation.

The control logic has been designed discretely with FAST Schottky TTL since the use of PLAs would have a serious effect on gate propagation delay times.

The MC68020 supports a late retry cycle recognition and this is used in the design to take corrective action in the case of a cache miss.

As greater performance is required from the MC68020 the move towards high frequency zero-wait state operation becomes a more important requirement. If an MMU is placed between the processor and memory this will have an effect on zero-wait operation at the higher frequencies.

If the logical data cache can be made large enough, so that a high hit rate can be achieved, then slower physical memory could be tolerated in the system.

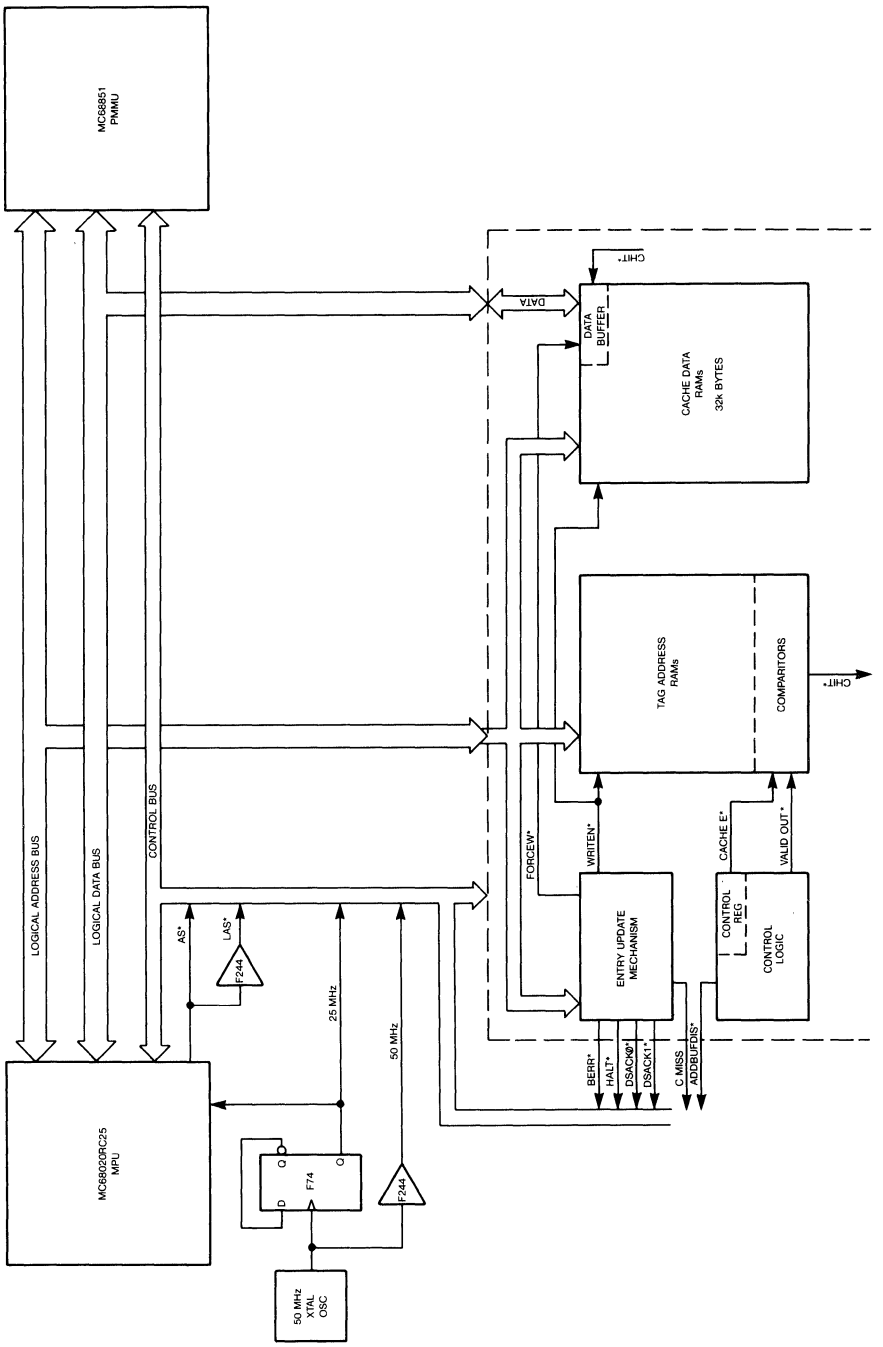

Figure 1: Block Diagram

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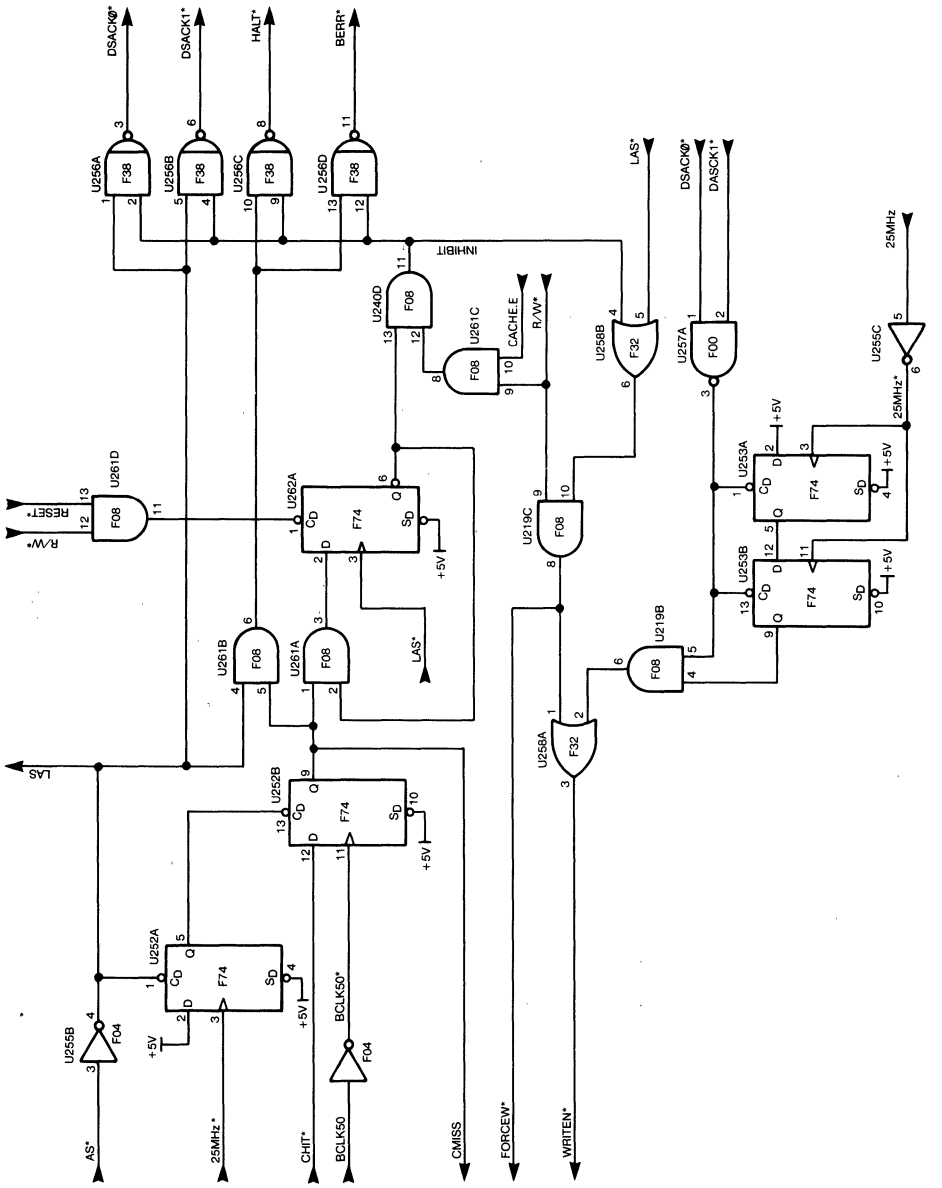

Figure 2: Entry Update Mechanism

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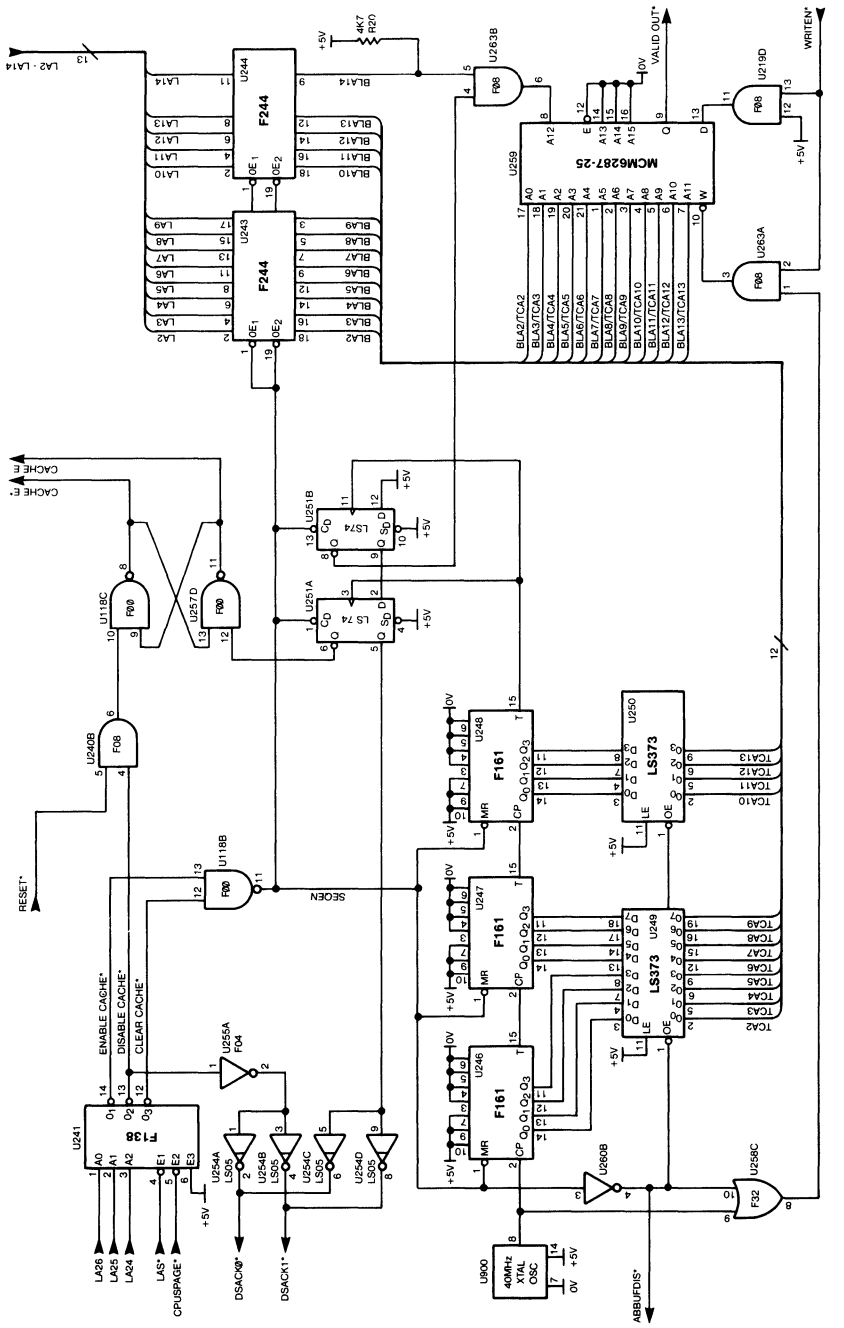

Figure 3: Control Logic

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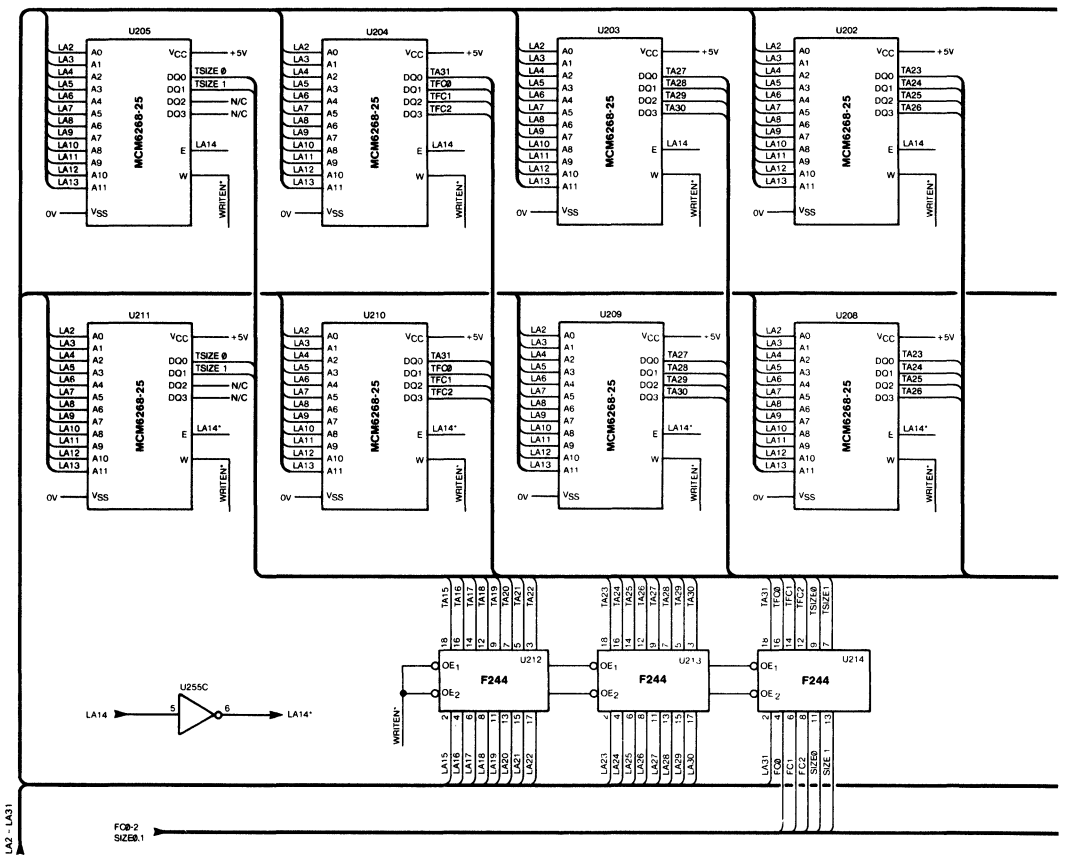

Figure 4: TAG Address RAMs

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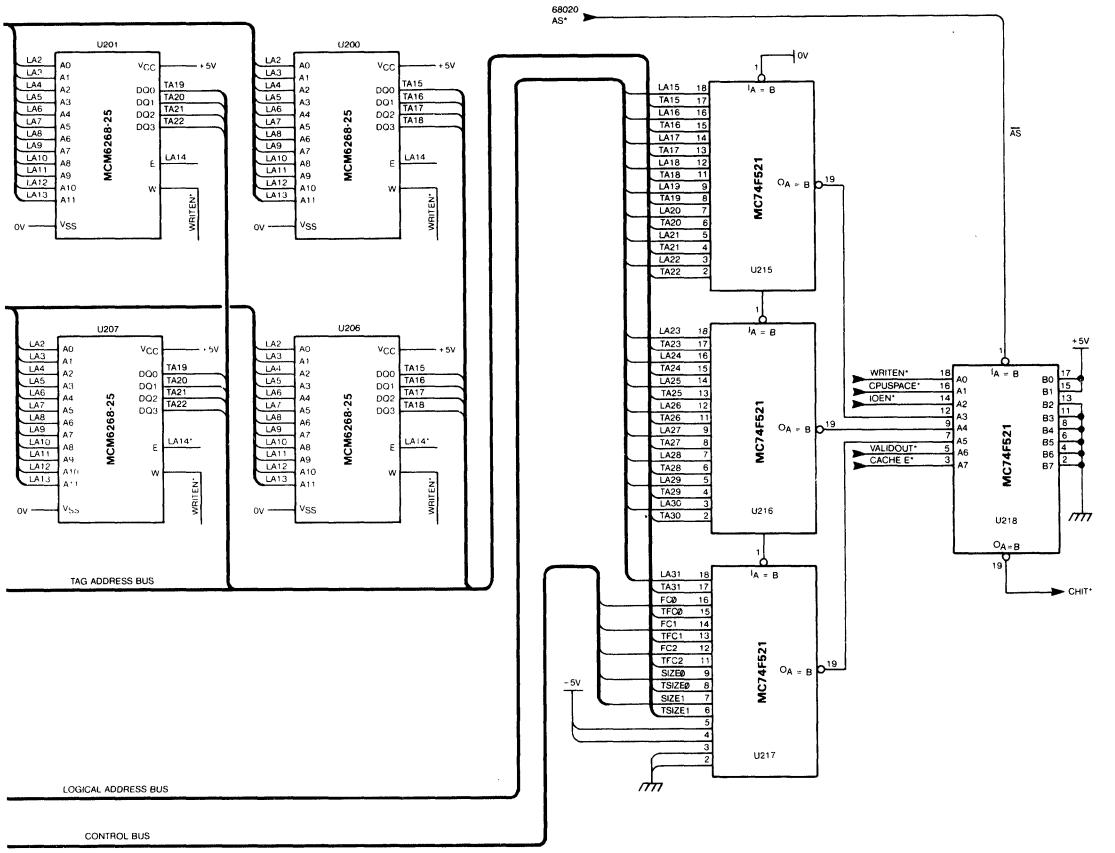
68020
AS*
U201
U200
U207
U206
MCM6268-25
+5V
0V
WRITEN*
TAG ADDRESS BUS
U215
U216
U217
U218
MC74F521
WRITEN*
CPUSPACE*
IOEN*
VALIDOUT*
CACHE E*
CHIT*
LOGICAL ADDRESS BUS
CONTROL BUS

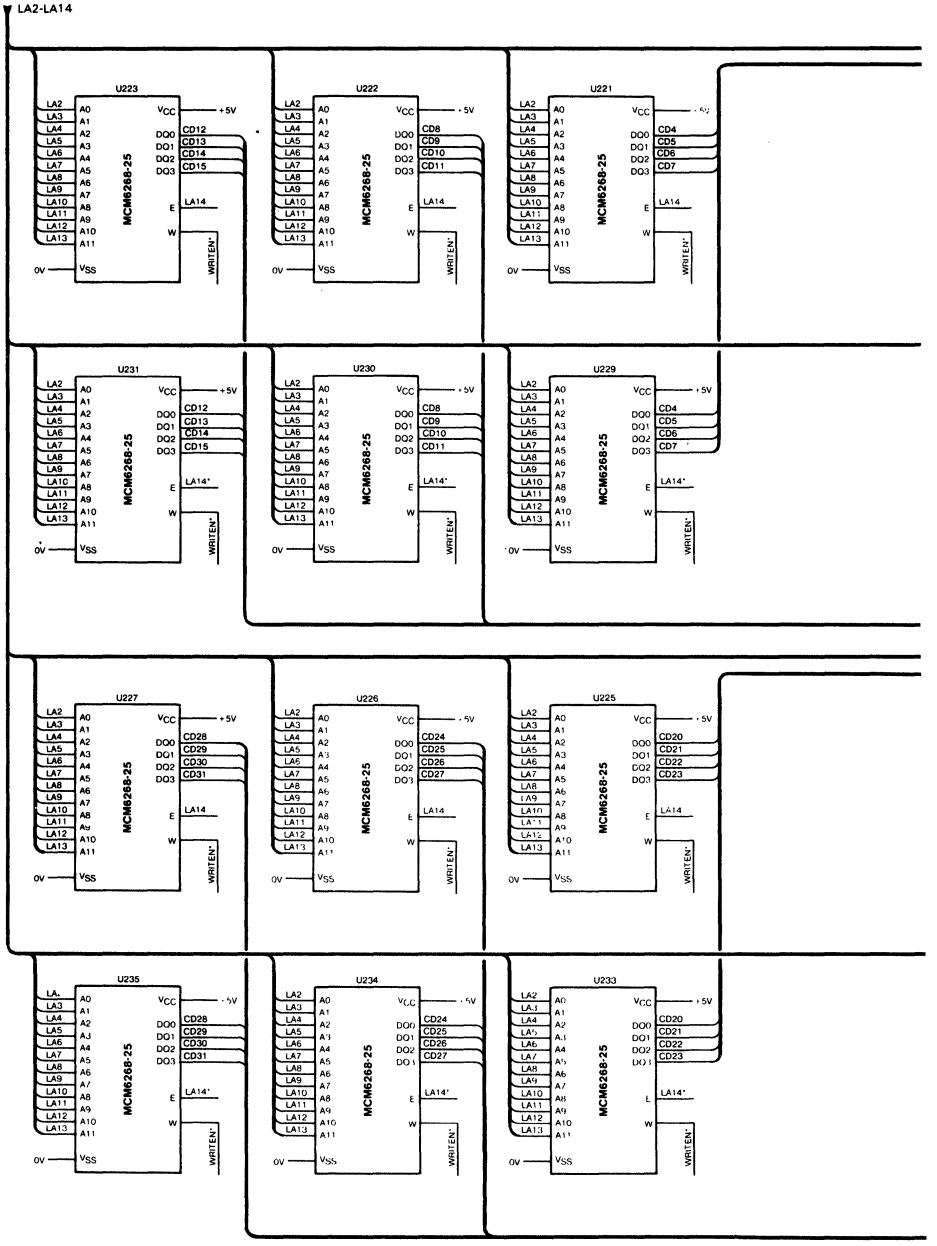

Figure 5: Cache Data RAMS

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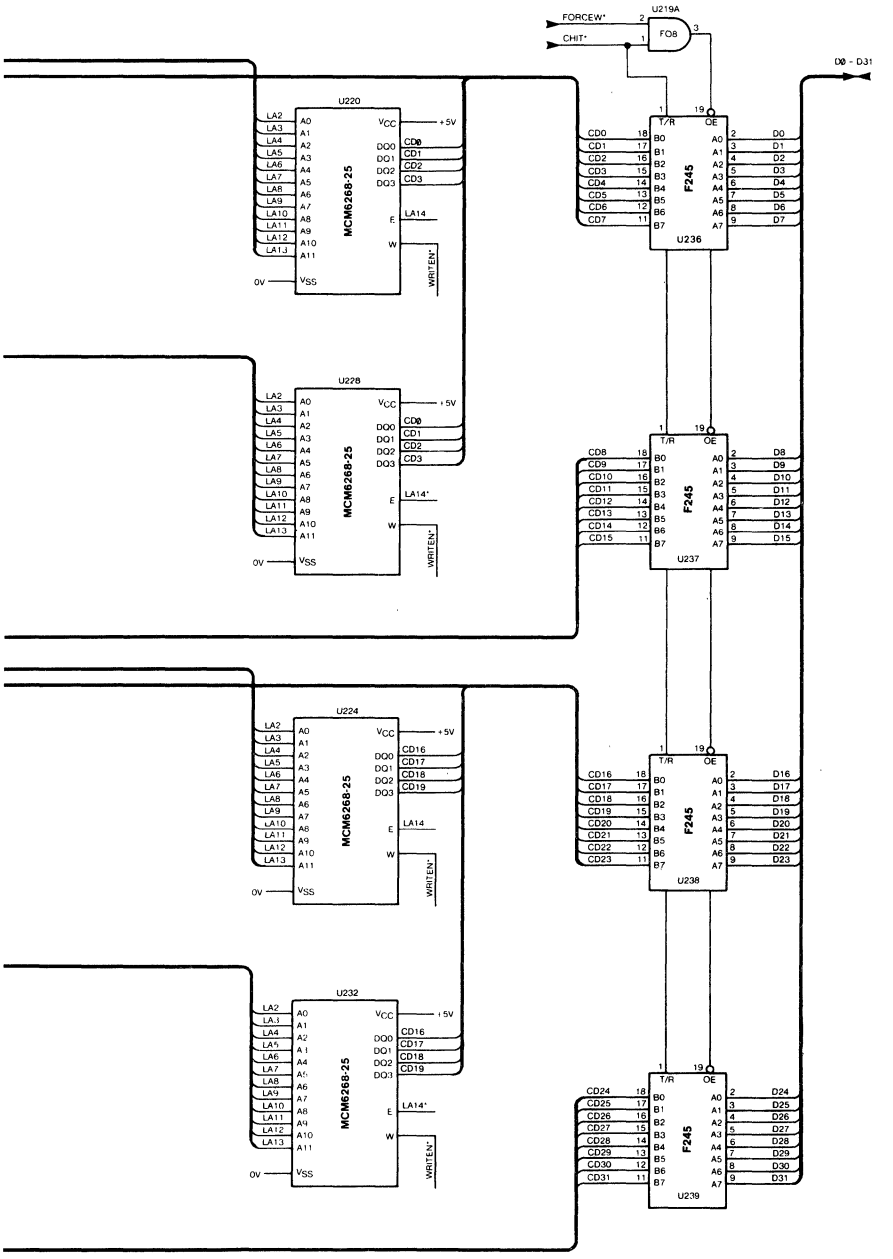
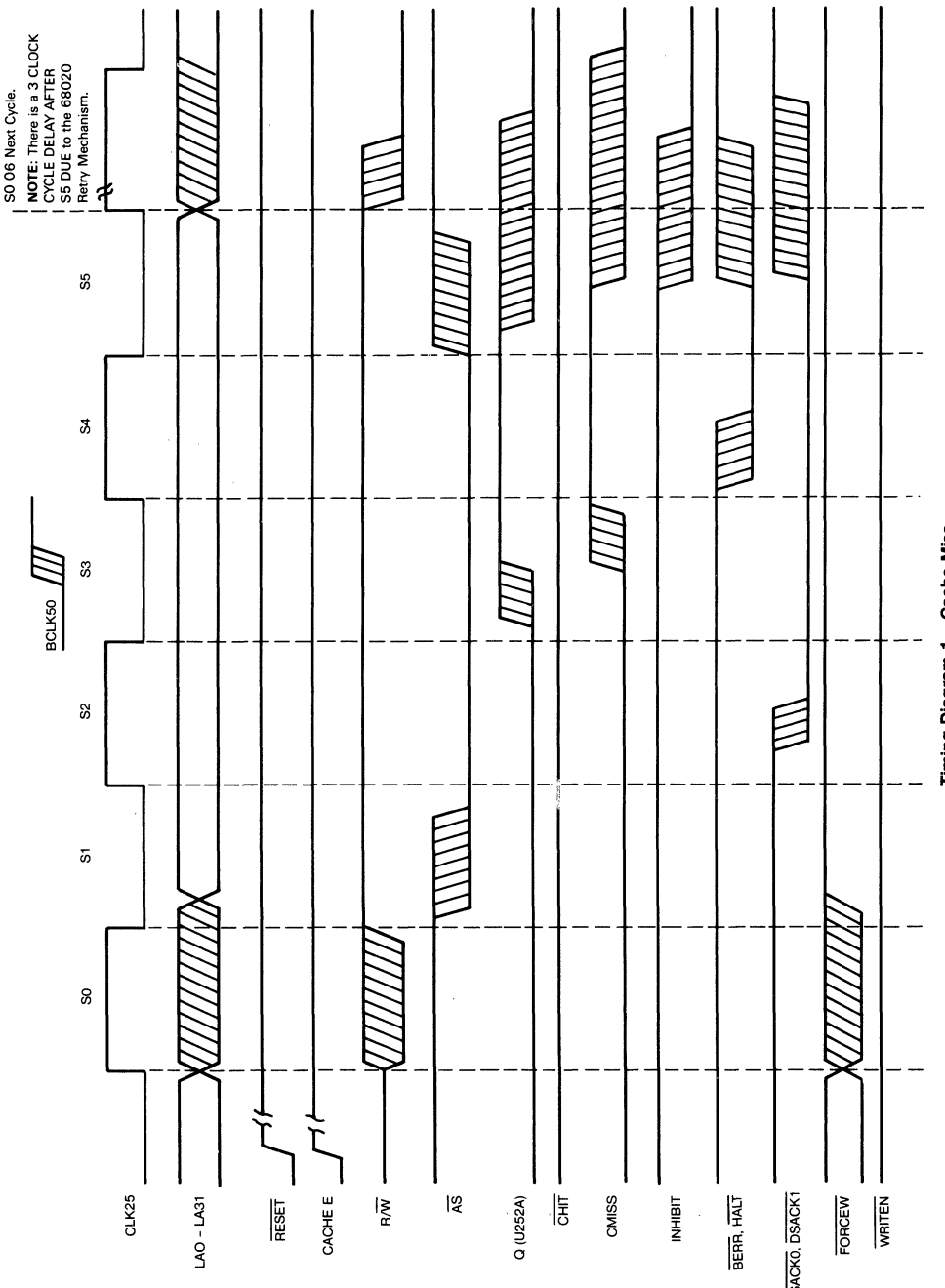

FORCEW*
CHIT*
U219A
FOB
D0 - D31
U220
U228
U224
U232
MCM6268-25
F245
U236
U237
U238
U239
WRITEN*
LA14
LA14*
+5V
0V



Timing Diagram 1 - Cache Miss

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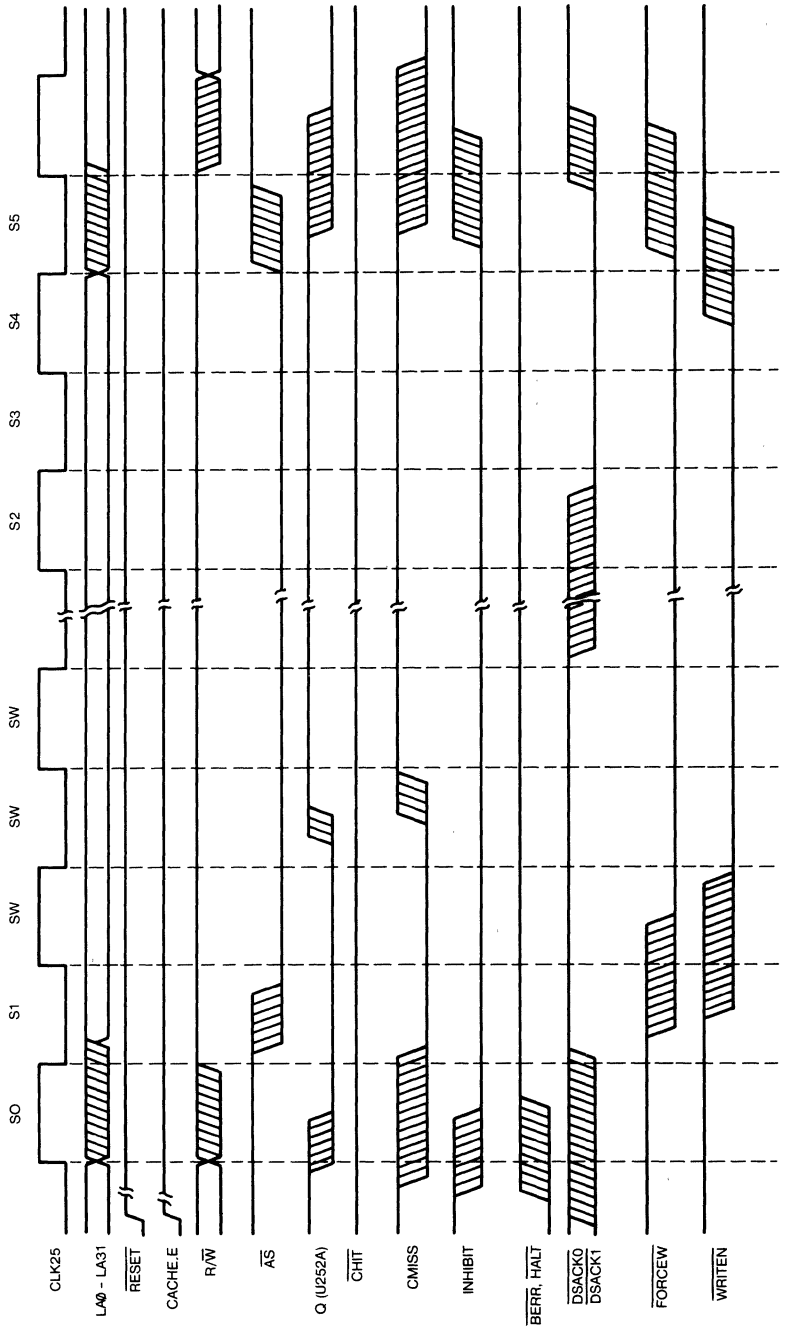

Timing Diagram 2 – Retry of the Cache Miss Cycle

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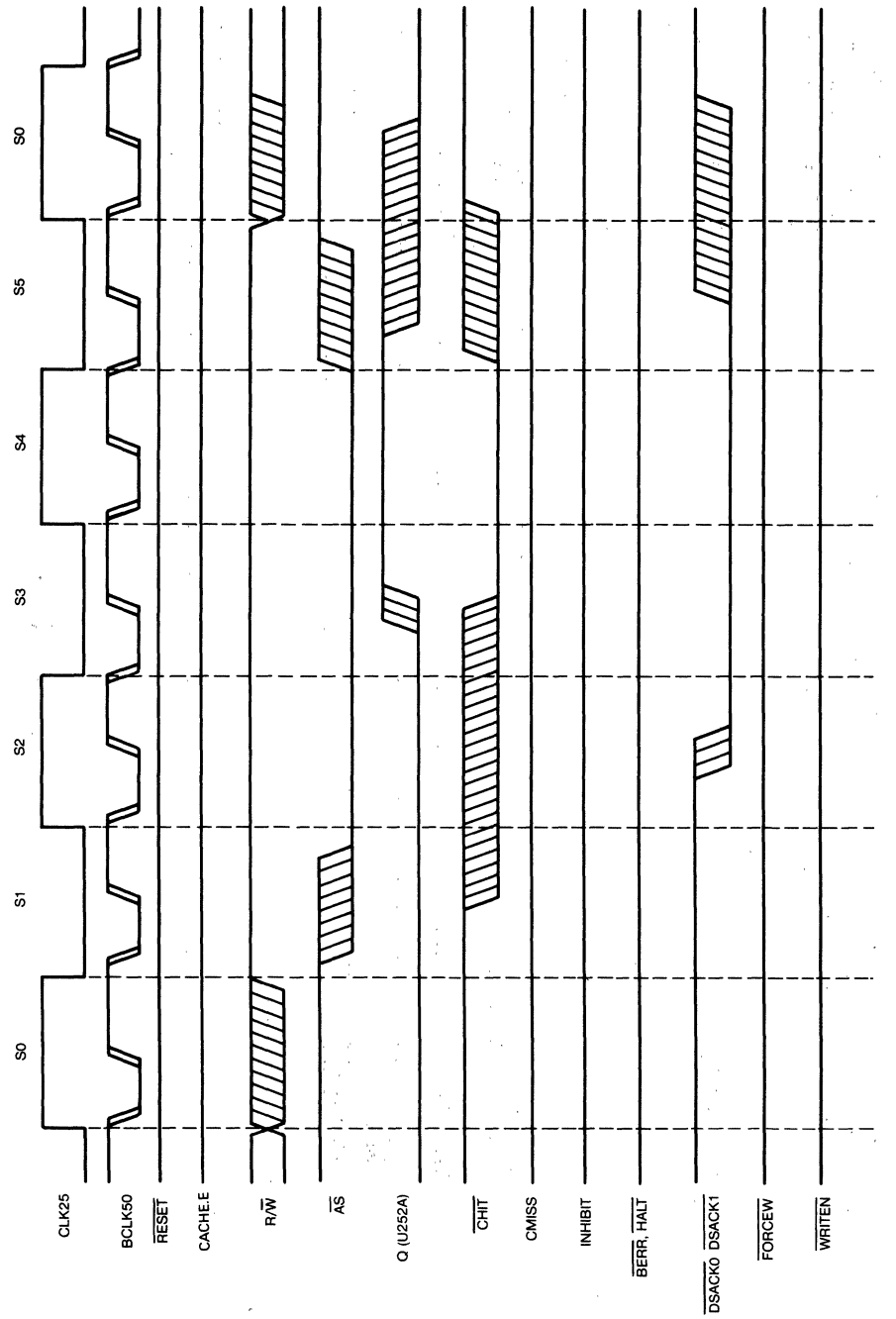

Timing Diagram 3 – Cache Hit

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DESIGN APPLICATIONS

DESIGNING A CACHE FOR A FAST PROCESSOR

COMPARATOR CHIPS HELP CREATE A HIGH-SPEED CACHE FOR THE MC68030

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To wring the best performance from the new breed of superfast microprocessors, system designers frequently turn to external caches. Direct mapped and set-associative caches offer advantages, compared with fully associative caches. In designing an address-tag-and-comparator system for a direct-mapped or set-associative cache, engineers must consider issues such as the speed of the hit, the address-bus loading, and the data-block size *(see "What's the Cache?")*.

Issues relating to the specific high-speed microprocessor also crop up. For instance, a system built around the MC68030 microprocessor must support two-cycle reads and writes related to the address-tag-comparator timing. Designers must also resolve questions of whether or not and how to support a burst mode. To support this mode, they must decide on address-tag and cache-data-RAM requirements unique to the mode, such as automatically incrementing addresses for the address tags and the cache-data RAM. They must also consider the data setup and hold timing requirements at the processor.

CACHE TAG RAMS

Matching the speed of the MC68030 microprocessor, the cache-tag comparators in the MCM4180, MCM62350, and MCM62351, organized to handle 4 kwords by 4 bits, compare data in the cache RAM with an external 4-bit-wide data field. The comparison results appear on the devices' Match pins. Each of the cache-tag devices is bulk clearable and has read and write functions. Of all the cache-system configurations possible with this MCM family of RAMS, for a 32-bit-by-16-kword system, a block of four MCM4180s as tag valid-bits comparators and four MCM62350s provide the fastest hardware arrangement, least bus loading, and lowest cost *(Fig. 1)*.

The MCM4180 includes an Exclusive-Nor (XNOR) comparator, which matches each bit position with the stored data for a true result. This type of comparator requires that every bit position match the stored data for the result to be true.

The MCM62350 and MCM62351 supply a user-configurable comparator offering the conventional XNOR mode and an And-Or-Invert (AOI) mode. Unlike the XNOR mode, the AOI comparator treats zeros in any bit position as don't-care bits during the compare operation. The AOI option is extremely useful for comparing status bits often stored with each address tag. The status bits can represent validating entry bits, which allow storing multiple data entries with each address-tag entry (block size = n), as well as individual so-called dirty bits needed for copy-back caching schemes.

The MCM62350 and MCM62351 RAMs also feature bit-set and bit-clear write cycles, which allow individual bits to be unconditionally set or cleared through a mask. Thus, any combination of the four bits in any particular location can be set or cleared without having to read the RAM, modify the data, and write it back as in a conventional SRAM. This feature is useful with the AOI com-

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DESIGN APPLICATIONS

CACHE SYSTEMS

parator for storing status bits. Also, both the MCM62350 and the MCM62351 have ground pins positioned to achieve minimum self-inductance in both DIP and small-outline J-type packages.

The MCM62350 differs from the MCM62351 in that it offers a user-configurable Match-output active level. The MCM62351 has an active high open-drain Match output. Wire-ORed connections of separate Match pins allow the comparison width to expand efficiently.

The design of external caches for the MC68030 involves two major timing problem areas—in the address-tag-comparator and in the data cache. Since the synchronous bus protocol makes it possible to use short bus cycles and supports burst-mode accessing, the prudent designer will also choose to use it for external cache interfacing to the MC68030 *(see "A Synchronous Bus Protocol").*

The primary challenge with timing the address-tag comparator is to avoid wait states when the processor runs at a high frequency. Generally, only a hit in any given bus cycle should assert the Synchronous Termination Handshake (/STERM) signal. The first order of business, then, is how to generate /STERM.

To avoid a wait state, the MC68030 asserts the worst-case Address Strobe (/AS) signal at the same time that the /STERM signal is activated. As a result, cache designs for this processor cannot generally use the /AS to signal the cache that a bus cycle is starting.

Nevertheless, the address-tag comparison must be qualified based on valid addresses that /AS announces. Fortunately, a signal called External Cycle Start (/ECS) is valid slightly earlier than the addresses. Whenever the processor needs an instruction or data, it therefore asserts

WHAT'S THE CACHE?

With a cache, when a processor executes a new task, it fetches from the system's main dynamic memory the first instruction and corresponding data, plus the instructions and data for several subsequent operations at adjacent memory addresses.

The cache's SRAM memory fetches the instructions and data from the adjacent main-memory addresses because they have a high probability of being used in the operations that follow. Most programs contain loops, and if the cache is large enough, the needed information will be present in the fast cache, shortening the average memory-access time.

That's a cache hit. If the cache doesn't contain the information, a miss occurs. In this case, the main memory again responds, and the cache receives updated instructions and data.

A cache controller circuit sequences the necessary functional steps. For normal program operation, the system doesn't directly address the cache. The cache subsystem stores both the information and its corresponding main-memory address. The controller compares the stored address in the cache, called the address tag, with the address the processor provides to determine whether the cache contains the requested data.

Cache types are usually delineated by their placement policy, or mapping algorithm, which determines where new information is stored in the cache. Most caches are either associatively content addressable or directly mapped, random-accessible types.

Whereas in a straight RAM, the processor directly accesses the information, in a content-addressable memory a match with a stored address of the information's original main-memory location causes the contents-addressable portion of the cache to respond with a pointer *(see the figure, opposite, left).* The pointer, or address, then specifies the data's location in a random-access-memory portion of the cache system. This fully associative memory cache copies the information in any main-memory location into any location in the cache.

A directly mapped cache, on the other hand, uses random-access memories to store both an address tag and the information's image *(see the figure, opposite, right).* The low-order bits of the address from the processor provide an index into the address-tag-store portion of the cache system, which stores the high-order address bits. To determine whether the requested information resides in the cache, the system compares the high-order address bits from the processor's bus with the contents of the address-tag-store RAM. If they're the same, the cache contains the requested information. Unlike in a fully associative cache, in a directly mapped cache, a memory-address location has its information copied into only one unique location.

The fully associative content-addressable memory cache can have a higher hit rate than any other cache type of the same size *m*. But it's very expensive, compared with a directly mapped random-access cache memory of comparable size.

When *n* directly mapped caches operate in parallel, the cache is designated as an *n*-way set-associative type. Nevertheless, system designers may consider both directly mapped and fully associative types as set-associative caches. A directly mapped cache is simply a one-way set-associative type, and a fully associative one is an *m*-way set-associative type.

A four-way set-associative cache yields about the same hit

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DESIGN APPLICATIONS

CACHE SYSTEMS

/ECS during the clock's high phase when the new addresses appear. Should the processor find what it needs in its internal caches, it would not assert /AS and an external bus cycle would not run. If /STERM activates when no bus cycle runs, the processor ignores it.

The timing diagram of the synchronous bus shows that after addresses are valid, /STERM must be activated within just a half clock period minus the clock-rise time to avoid wait states. Operating at 25 MHz, that leaves only 15 ns to check for a cache hit and assert /STERM if wait states are to be avoided.

The circuit must furnish an extra gate for the results of the tag comparator to be ANDed with a qualifier—a latched /ECS signal. A 74F64 AOI gate can AND the Match signals from the tag comparators to this qualifier. Unfortunately, this gate adds a 5.5-ns delay to the circuit. Consequently, the tag comparators must perform their comparison in 9.5 ns.

Since TTL-compatible tag comparators aren't that fast, this technique isn't feasible. Two options remain: Always assert /STERM after /ECS, and if the cache misses assert /BERR and /HALT retry, or insert a wait state. With retries, at 25 MHz, the tag comparator has 35 ns to perform its function and generate /STERM. At 33 MHz, it has just 28 ns. For the wait-state option, 34.5 ns is available to generate /STERM after the addresses are valid.

Retries, however, can run into trouble. After requesting a retry, the processor must disable the cache to prevent a system deadlock condition when the bus cycle reruns. Also, before the bus cycle can rerun, a two-clock-cycle delay occurs. As a result, the penalty incurred when the external cache misses might be greater than it would be if the processor asserted /STERM only on a cache hit.

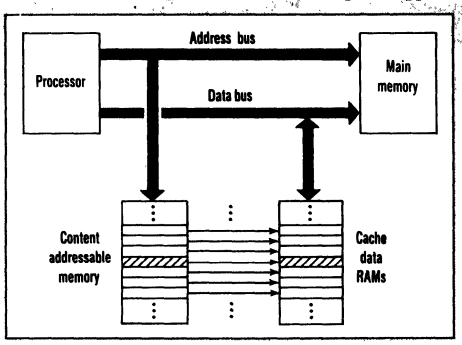
rate as a fully associative one-way cache of the same size. In an *n*-way set-associative cache, any particular address location maps data in *n* locations in the cache.

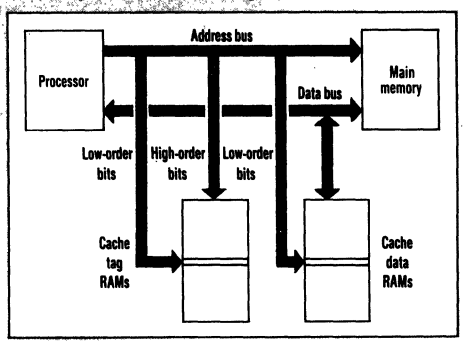
Consider the issues involved in designing the address-tag store and comparator of a directly mapped cache. For maximum performance, the time taken to bus load the addresses should be minimum. Thus, one component should both store and compare the address tags to minimize delays resulting from off-chip signal propagation. For a 16-kword by 32-bit cache operating on a 32-bit address bus, the part must store a 16-bit-wide address-tag field, plus a 17th bit to indicate that the address tag is a valid entry. Consequently, the storage of only one cache data item for each address-tag entry—a block size equal to one—requires an address-tag storage capability of 16 kwords by 17 bits.

When storing *n* data items with each address tag entry, the block size equals *n*. Keeping the cache size constant reduces the depth of the address-tag store by a factor of *n*.

Having only one validating bit for each address tag, however, requires either an *n*-by-32-bit main-memory data-bus width or running *n* 32-bit bus cycles to fill the cache line in the event of a miss. Another event could also transfer the *n* by 32 bits. A less restrictive way to support *n* entries per address tag is to have *n* validating bits stored along with the address tag. Then when the system records a miss, the controller updates the address tag and sends only the validating bit corresponding to the transferred data item. This procedure requires only a 32-bit data bus and one main-memory cycle to allocate a new cache line.

An increased block size would mean that designers need fewer memory components to build the address-tag store and comparator. A large block size with fewer components not only saves board space and shrinks cost, but also reduces address-bus loading, which then, of course, will result in faster performance.





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Therefore a no-wait-state cache with a low hit rate can perform worse than a cache with a wait state.

A secondary difficulty with tag comparators in MC68030 cache designs is supporting burst-mode accesses. The address-tag-comparator timing is clearly a limiting factor in the design of external caches for the MC68030. Because the burst-mode cycles furnish only a first address for the four desired long words, the circuit must provide autoincrementing addressing to the address-tag comparator and the cache-data RAMs. This requirement, coupled with the fact that burst transfers can occur in single clock cycles, implies that incrementing the addresses into the address-tag comparator will not be fast enough to support one-cycle bursting.

Organizing the cache with a block size of four is a viable one-cycle bursting solution. Storing a valid bit for each long word per tag, then, requires only checking the valid bit on the fly during the bursting portion of the burst-mode transfer.

This approach can exploit the fast timing of the compare port in an MCM62350 or MCM62351 to store the valid bits. It also allows the AOI comparator option for the valid-bit comparisons to operate effectively *(Fig. 2)*.

A PAL POINTER

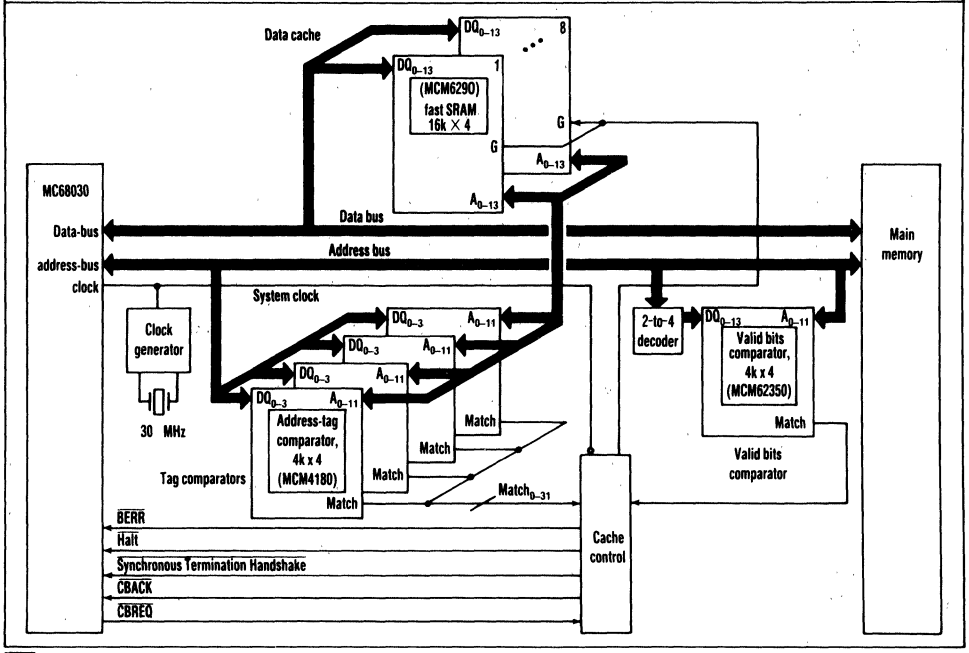
The open-drain Match pins of the MCM62351s permit wire-ORing of the four address-tag outputs to the matching circuit and thereby the elimination of a fan-in gate. A PAL device makes possible a simple, fast input to this circuit by providing a pointer for checking only the relevant long word while bursting. The address tag still needs comparison, but only on the initial access.

The PAL should contain a decoder to decode addresses A2 and A3 from the processor. The resulting one-of-four outputs then enter a shift register, also built into the PAL. In this way, the four outputs from the PAL provide the compare port of the status-bit comparator with a rotating pointer. In the AOI comparator, a single valid bit compares when only one of the four compare inputs is at a logic-one level. The other three valid bits become don't cares.

A block size of four not only allows single-cycle bursting to work, but it also saves components. Furthermore, because address-line loading is reduced, the processor can drive its address bus more quickly. The result is fast hardware.

The main data-RAM issues relate to burst mode. They include address autoincrementing and data setup

NO WAIT-STATE CACHE FOR FAST RAMS



1. A CACHE SYSTEM with four XNOR-configured comparators and one AOI configured comparator—each with a depth of 4-kword entries, a 16-kword-by-32-bit cache, and a block size of four—has the lowest cost, reduced bus loading, and fast hardware.

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DESIGN APPLICATIONS

CACHE SYSTEMS

A SYNCHRONOUS BUS PROTOCOL

The MC68030 adds a new bus protocol—the synchronous bus cycle—to the MC68XXX family of processors. Like its predecessors, the MC68030 supports the standard asynchronous bus protocol. Unlike the asynchronous bus on the MC68020, the 60830's synchronous bus doesn't support dynamic bus sizing. As a result, all synchronous bus cycles issue from a 32-bit port.

The minimum length of the MC68030's synchronous bus cycle is two clock periods, whereas the MC68020 has a minimum bus cycle of three clock periods. Also, the MC68030 has on-chip memory-management functions; the MC68020 does not. Since an MC68851 memory-management unit requires a clock cycle to translate logical addresses to physical addresses, the minimum physical bus-cycle length of an MC68020-MC68851 combination requires four clock periods. The MC68030 bus can therefore operate twice as fast as an equivalent MC68020-MC68851 system at any given clock frequency.

Another feature added to the MC68030 bus, the burst-mode protocol runs only in synchronous mode. The MC68030 has two internal caches—an instruction cache and a data cache. Both have 16 lines with a block size of four (four 32-bit words per address tag). When either internal cache of the MC68030 records a line miss from a cachable area of main memory, the system attempts to burst four long 32-bit words to fill the new line.

The processor places the address of the first long word on the bus and expects the return of the corresponding data, plus three additional long words, in as little as three clock cycles. The processor doesn't change the address on the bus during these subsequent transfers. Rather, it assumes that the external memory increments address lines A2 and A3 in a modulo-four fashion, as if the the bus were operating in nibble mode. Thus, with no wait states, the MC68030 receives as many as four long words in just five clock cycles by using the burst-mode protocol. Because the application's characteristics affect the type of code the system runs, the decision of whether or not to use the burst mode is very important. System designers would do well to study the matter in depth.

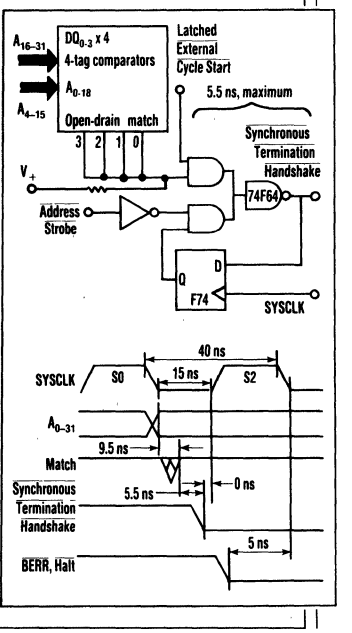
A knowledge of the timing requirements of no-wait-state operation is crucial to understanding how the MC68030's synchronous bus operates *(see the figure)*. When a new bus cycle starts, the processor delivers memory addresses during a system-clock high time, but the addresses are guaranteed valid only at the end of the clock high time.

To avoid wait states, the Synchronous Termination Handshake signal, /STERM, must assert 0 ns before the rising edge of the next system-clock pulse. If this condition is met, the processor latches the data on the next falling edge of the clock. The processor needs a 5-ns setup time for the data with respect to the falling edge of the clock.

If the processor requires wait states, /STERM can be delayed relative to the clock rising edge to allow the use of slow memories in the synchronous mode. This feature applies also to burst-mode cycles. But when the processor recognizes /STERM on a clock rising edge, data latches on the next falling edge, subject, of course, to adequate setup and hold times.

When the processor runs a burst cycle, it can accept new data with the same setup time to the clock on the clock's next three falling edges. The processor also needs an 8-ns data hold time after the clock falls when operating at 25 MHz. Accordingly, if the processor runs burst cycles at 25 MHz, the data must be valid during the bursting portion of the cycle for 13 ns of the 40-ns clock period to meet the processor's setup and hold time requirements.

Like its predecessors, the MC68030 microprocessor supports bus retries and reruns. If the bus-termination handshake STERM/, or DSACKx/, is asserted with proper setup time relative to a rising clock edge, activating BERR/ and HALT/ with a 5-ns setup relative to the next falling edge of the clock aborts and reruns the current bus cycle. But this action results in two dead clocks on the bus before the bus cycle restarts. Nevertheless, no wait-state caches designed for the MC68030 use this technique to prevent the processor from latching bad data when an external cache records a miss.



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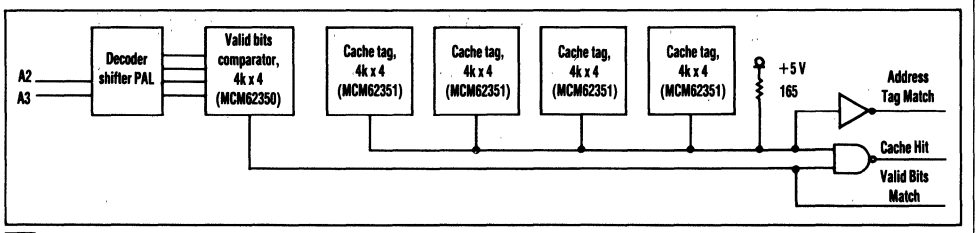
DESIGN APPLICATIONS

CACHE SYSTEMS



2. ORGANIZING THE CACHE with a block size of four is a viable single-cycle burst-mode solution. This approach can exploit the fast timing of the compare port in an MCM62350 or MCM62351 to store the valid bits and make it possible to effectively apply the AOI comparator option for the valid-bit comparisons. The open-drain Match pins of the MCM62351 permit the wire-ORing of the four address-tag outputs to the matching circuit, thereby eliminating a fan-in gate.

and hold timing to the processor. At issue is whether burst mode supports two-cycle write timing.

If a synchronous bus cycle is run, the data must set up at the processor without delay (in 5 ns), before the first falling edge of the clock after the processor recognizes the STERM signal. If the cycle is two clock periods, then the time available to access the cache-data RAM equals a clock period. For a 25-MHz clock, the time available would be 35-ns. A 33-MHz clock would yield a 25-ns interval.

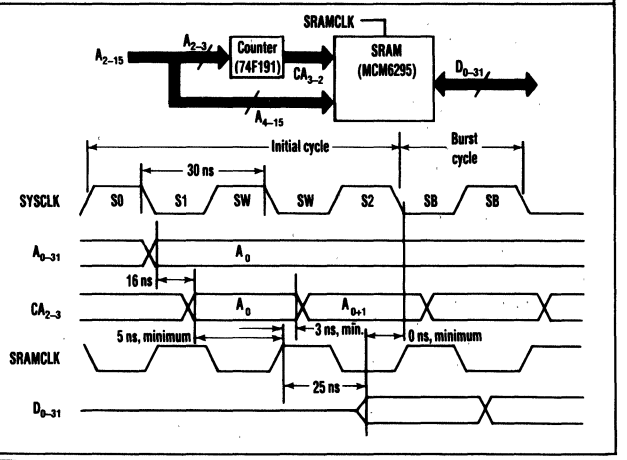
For single-clock burst cycles, also, 35 ns is available for RAM accesses at 25 MHz. But the data hold time after a clock low at 25 MHz is merely 15 ns. That short time interval calls for very fast output-enable SRAMs, such as the MCM6290.

To support the burst mode, a 74F191 counter, inserted in series with A2 and A3 address pins, gives two incremental addresses to the cache-data run for autoincrement addressing. Unfortunately, the processor's data-hold-time requirements prevent this scheme from working. Besides, the counter's latency in a parallel-load mode requires a RAM faster than 35 ns.

A MCM6295 synchronous SRAM as the cache-data RAM, with one 74F191 counter, readily supports single-cycle bursting *(Fig. 3)*. Latching the data outputs when the synchronous SRAM clock is low resolves the issue of data-hold time. Furthermore, once the synchronous SRAM clock drives high, the addresses into the device are registered and can be changed for the next access in the burst sequence.

When the MC68030 performs a two-clock write cycle, the data and address sent to the RAMs are simultaneously valid for only a half clock period. For clock frequencies over 25 MHz, this time isn't adequate to complete a write cycle in typical fast static RAMs. In that case, it's necessary to insert a wait state.□

A THREE-CYCLE BURST READ



3. AN MCM6295 SYNCHRONOUS SRAM, a cache-data RAM with one 74F191 counter, readily supports single-cycle bursts.

Richard Crisp led the design team for the Motorola cache-tag comparators. He has helped design several microprocessors, including the MC69000, MC658020, and the Intel P7CP. Crisp, who holds a BS from Texas A&M University, has four U.S. patents.

Brian Branson received a BS from Colorado State University. At Motorola, he designs application-specific static and dynamic RAMs. He has one patent pending.

Ron Hanson holds a BS from Rose-Hulman Institute of Technology and an MBA from Indiana University, in Bloomington. Hanson is a product marketing engineer for fast static RAMs at Motorola.

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AR260/D

ENHANCING SYSTEM PERFORMANCE USING SYNCHRONOUS SRAMs

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INTRODUCTION TO SYNCHRONOUS SRAM ARCHITECTURE

Fast static RAMs (FSRAMs) are commanding a lot of attention from today's high performance system designers who frequently find that the speed of their system is limited by the performance of FSRAMs on the market. As 32-bit microprocessor-based systems become faster and more prevalent, the demand for sub 25 ns FSRAMs will grow even more.

FSRAMs are the driving force behind semiconductor technology today: they have the smallest circuit features—as low as 0.8 micron from some manufacturers—and use special processes like double-level metal and BIMOS. The Fast SRAM has come a long way from its slower ancestors like the 1K × 4 Model 2114. The ease of use and dependable performance that resulted from the asynchronous performance of SRAMs have been replaced by the raw speed which is pacing today's demand; however, FSRAMs are still expected to meet the basic SRAM specifications for pure asynchronous performance. This dichotomy has caused problems as chip designers come up with more innovative ways to speed up their circuits. Address transition-detection circuitry, for example, caused a number of problems when first introduced in 2K × 8 FSRAMs under certain system conditions. With such advanced technology being used and the cost of manufacturing these chips so high, Motorola has developed an alternative to a high-tech 15 ns access SRAM that uses conventional technology.

Motorola's newest SRAMs are the first to fully embrace the primary purpose of Fast SRAMs. They totally abandon the previous definition of asynchronous SRAMs. They have the requirement of a clock signal, and are, therefore, Synchronous SRAMs. They have separate pins for input and output data, and do not specify standby power.

Motorola offers four different 65,536-bit Synchronous SRAM family members organized as 16K × 4: Models MCM6292, MCM6293, MCM6294, and MCM6295. The technology used for their implementation is the fast, low power-consuming, and noise-immune HCMOS III, which uses a silicon gate for its fabrication. One of the main advantages to using these devices is that they can be designed into system cache-memory or writeable control-store applications with fewer interfacing glue-type parts than the standard SRAM memory. Among the reasons for this are the integrated input and output latches that are capable of driving loads up to 130 pF. Due to the increased operating speed of the device and the additional output-buffer loads, an extra ground pin has been placed on the chip.

Four different devices have been specified so that all combinations of the output-latching and output-enable features are in the offering. The MCM6292 comes equipped with latches that are edge triggered on the inputs but transparent on the outputs. To support systems with pipelined data, the MCM6293 is offered with edge-triggered latches on both the inputs and outputs. The MCM6295 and MCM6294 are output-enable versions of the two basic parts. All of the Synchronous SRAMs come with separate data-in and data-out pins; however, some systems specify a more conventional common I/O mode, and the asynchronous output-enable control ($\overline{G}$) which replaced the $\overline{S}$ signal on these parts can be helpful in such a case.

In many designs using SRAMs, there is actually extra time during the cycle that is being wasted. In more critical applications, the Synchronous SRAM offers an alternative to the conventional SRAM. An external clock input (K) can be used to precisely control the cycle by directing the operation of the on-chip latches.

The designer of small personal computer systems can use the Synchronous SRAM in a number of storage areas. One of the primary applications, cache memory, is high-speed memory that resides between the central processing unit (CPU) and the main memory of the system. Accesses to this fast cache typically require 60 ns versus the 200 ns needed to perform an access to main memory. One way the cache is used is to store data or instructions from main memory that are frequently called for by an application. As an example of this, higher-level languages often use repetitive loops: by storing the data necessary for these repeated operations and instructions in the cache, accesses to the main memory can be avoided.

A typical system is illustrated in Figure 1. It is configured as a cache memory residing between the CPU and the system bus. The system bus links the main memory and I/O devices to the CPU by way of the cache.

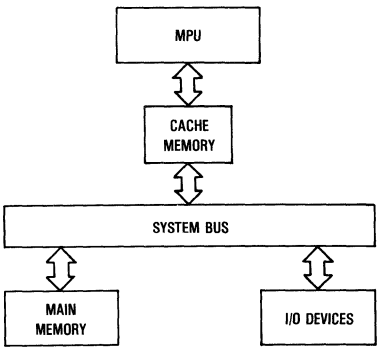

Figure 1. A primary synchronous SRAM application is high-speed cache memory residing between the CPU and the main memory of a personal computer system. Accesses to the cache typically require 50 ns, whereas main memory takes 200 ns.

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In operation, there is one set of locations in which data is stored and another set of locations containing a cache tag for each word in the cache. The cache tag identifies the main memory location with which the data is associated. A comparison is made between the cache tags, which are located in the cache memory, and the address, which is generated by the microprocessor at the beginning of a cycle. If a cache tag and the address match, there is no access made to main memory, but instead the read or write cycle is executed on the corresponding byte of data stored in the cache. When the address does not find a match, a miss occurs, and new locations must be read into the cache from main memory.

A cache miss is the result of a mismatch between the cache tag and the desired address to be accessed by the CPU. When this occurs, the system logic is allowed to perform a retry of the previous access. The appropriate address is accessed from main memory. Following an update of the cache, the data is then available for processing.

The cache hit rate is the actual percentage of accesses made to the cache in which the requested address is resident. In order to keep the hit rate as high as possible, a variety of software routines are used. The function of these routines is to keep the cache as full as possible with the most frequently used data. In so doing, the cache hit rate for both the data and instruction caches will be maximized, increasing overall information throughput.

The Harvard architecture, an efficient method used in many current day applications, is characteristic of a configuration which supports parallelism throughout a system. Synchronous SRAMs can be organized as relatively small external caches connected to the data buses and instruction paths located between the CPU and main memory. This will allow simultaneous instruction execution and data prefetches. The external cache demonstrates another system speed enhancement capability of these devices.

ADDRESSING CONSIDERATIONS FOR READ/WRITE CYCLES

To better understand the Synchronous SRAM's addressing capabilities in regard to read and write cycles, refer to Figure 2. In this illustration, there are four MCM6292 synchronous SRAM devices configured to operate on a 16-bit data bus. Each memory has four data inputs and four data outputs to allow the transfer to data. The address bus consists of 14 address bits, A0-A13. These 14 bits are required to decode and access the 65,536 memory locations of each device. The memory matrix is configured as 128 rows by 512 columns. The system clock is connected to the (K) input of each memory and used to latch all inputs, outputs, write enable, and chip select.

In Figure 3, there are two different read-cycle timings being represented for the MCM6292 (transparent output latches). Both are examples of systems that use the rising edge of (K) to latch all inputs to the memory device. The states of the outputs are then held until the clock makes its transition to the low state. With this Synchronous SRAM, however, it is possible to have different memory access times, depending upon the condition of the clock (K). If the clock pulse is high for less than the 25 ns access time of the memory device, the total access time is rated at t_{KHQV} or 25 ns (Read Cycle 1). On the other hand, if the high portion of the clock cycle lasts longer than 25 ns, the total access time becomes t_{KLQV} (10 ns maximum) plus the length of the clock high (Read Cycle 2).

Figure 4 has been included to show the timing of a write cycle. The timing of a write operation is similar to that of the previously discussed read cycle. One point to consider is that to generate a write pulse, there is no requirement for complex external interfacing chips. This is accomplished through the self-timing mechanism which samples both the write enable and input data when (K) rises. A high-impedance state is entered when the clock returns low.

MPU AND MEMORY SPEED CONSIDERATIONS AT A SYSTEM LEVEL

One consideration worth mentioning is that many memories are not able to keep up with very high-speed MPU control devices. This has been a problem with DRAM technology for a number of years. MPUs operating at clock speeds of over 20 MHz are common in both business and engineering systems

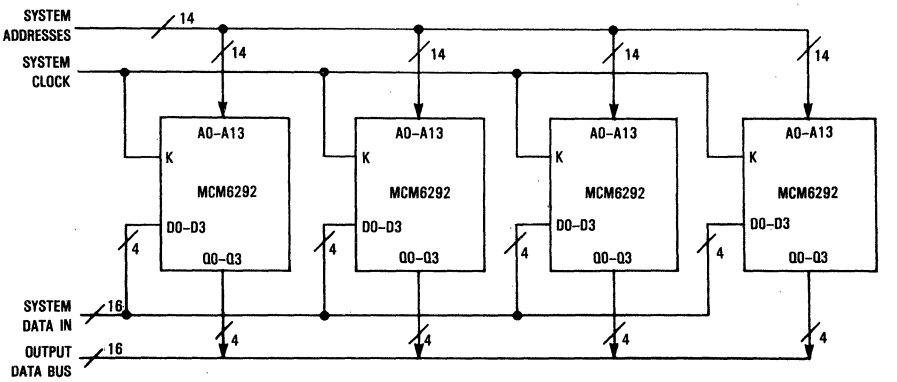
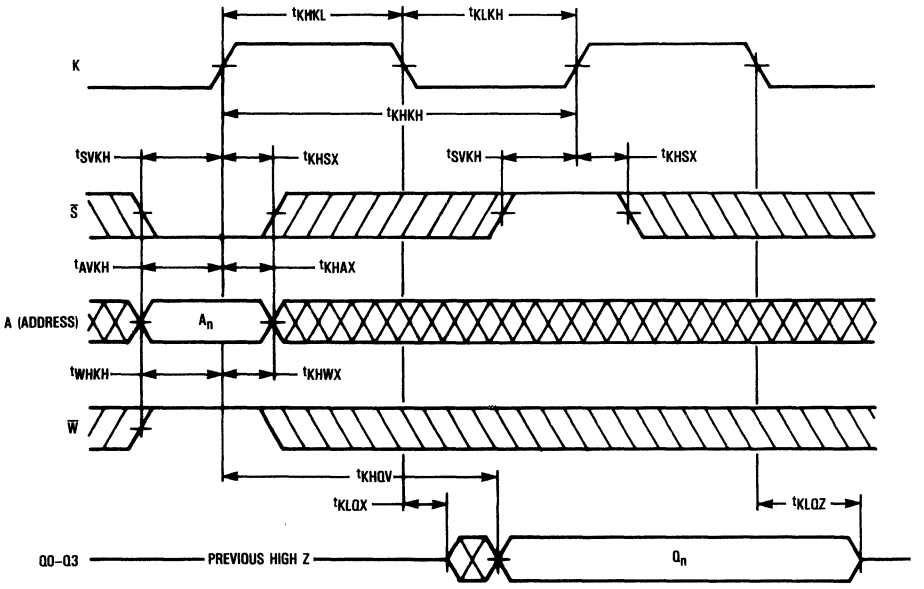
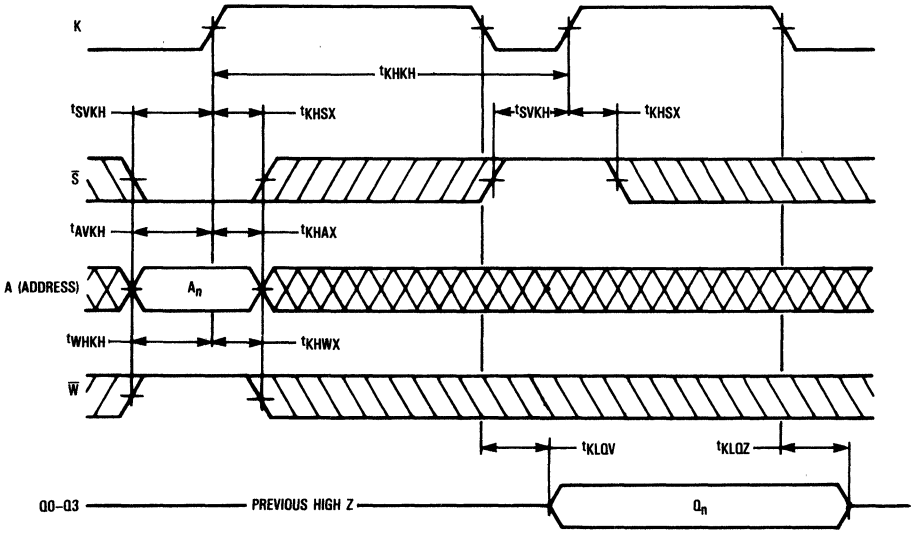


Figure 2. An array of synchronous SRAMs is configured for a 16-bit data bus. Each MCM6292 has four data inputs, four data outputs, and fourteen address lines.

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)



NOTES:
1. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.

Figure 3. If the system's clock high, t_{KHKL}, is shorter than the MCM6292's 25 ns access time, then the total access time will be 25 ns. However, if t_{KHKL} is longer than 25 ns, total access time is increased.

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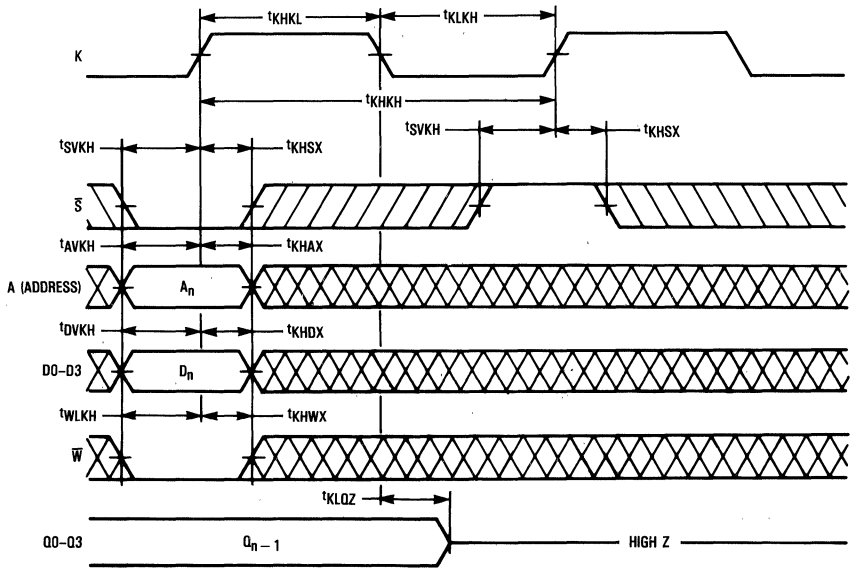

Figure 4. In a write cycle, the self-timing mechanism of the MCM6292 samples both the write enable and the input data when the clock signal, K, rises.

in use today; therefore, 25 ns Synchronous SRAMs are ideal to operate with zero wait states.

Wait states are implemented with slower SRAMs and most DRAMs to freeze the state of the microprocessor address and data bus for a clock cycle. As long as the signal controlling wait states is asserted, more wait-state periods will be generated. The microprocessor resumes operation when the wait-state signal is negated.

The alternative to implementing a wait state to halt the microprocessor for a slow memory device is to use the much faster Synchronous SRAM. Its timing parameters can be more exactly controlled, making the system operate more efficiently. Faster data throughput plus an improvement in overall system performance make the Synchronous SRAM cache a very cost-effective solution in a microprocessor-based system.

When performing read and write operations in a personal computer system, the timing relationship between a high-speed microprocessor's system clock and a typical Synchronous SRAM's cycle time constraints is very critical. These operations could be as simple as inputting console information for CRT display outputs or as complex as supporting multitasking environments or concurrent execution of operations.

High-performance microprocessor systems with operating frequencies of 20-25 MHz are a realistic timing example being offered today. For microprocessors capable of operating at these speeds, a 25 ns Synchronous SRAM is ideally suited. These devices not only provide precise clocked timing control, but also will support applications requiring system clocks running at over 30 MHz. This can be accomplished without incurring any degradation of the processor by inserting wait states.

WHAT'S TO COME FROM SYNCHRONOUS SRAMs

Very high cache hit rates can be attained from a relatively small cache store. The high-rate efficiency is primarily due to the fact that the cache is located external to the CPU rather than actually being an on-chip cache, as is the case with some high-performance microprocessors.

In addition to the popular high-speed cache-memory applications, Synchronous SRAMs are also ideal for writeable control store environments. Data can be downloaded into a Synchronous SRAM array, and the information can be accessed at very high speeds—much faster than from a DRAM array.

Memories are taking on new roles. Because of this, they are being used in a wide variety of application areas and operating to support functions previously not possible. Future Synchronous SRAM devices will be even more complex and some will very likely contain higher degrees of intelligence. Many will be designed with special system functions in mind. Higher-speed operation working from lower voltage sources is just one example. There will be enhancements allowing the designer more flexibility and enabling him to reach supercomputer performance.

Current-day static memories support numerous applications. The synchronous SRAMs discussed above will be offered in 300-mil, 28-lead CERDIP and 400-mil, 28-lead plastic SOJ packages. These configurations satisfy the requirements of most systems presently. As chip integration and sophistication continue to advance, the packaging technology will also need to advance to promote future innovations within the industry.

For more information on MCM6292-series synchronous SRAMs, contact Memory Marketing at Motorola, Inc., MOS Memory Products Div., P.O. Box 6000, Austin, TX 78762. (512) 928-6700.

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AR258

HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMs

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INTRODUCTION

The market for semiconductor memory products suitable for today's high speed cache applications is changing dramatically as the demand for higher performance super mini, ASIC, and microprocessor based computers rapidly increases. This development has put heavy pressure on MOS memory suppliers for faster and faster static RAMs to support shorter and shorter processor cycle times. To utilize their full system performance, fast SRAMs require precise system control, long address hold times, and have tight write pulse requirements. They provide short data valid time, cause common I/O data contention, and offer low drive capability. Todays high performance processors themselves have similar I/O requirements. Therefore system designers have many concerns when designing a fast memory subsystem. They must use additional logic (latches, drivers, pulse generators, etc.) to allow the memory subsystem to interact efficiently with the processor at the fastest system cycle times.

A solution to get the memory and the processor to work well together at fast cycle and access times lies not only in faster components, but in minimizing the need for external glue logic and its associated delays. The Synchronous Static RAM is defined as having on chip latches for all its inputs and outputs, added drive capability, and a self timed write cycle all under the control of the system clock. This eliminates the need for most external logic chips and allows the memory to run at higher system speeds than standard SRAMs with comparable access times.

This paper outlines the basic architecture of a Synchronous SRAM that Motorola plans to introduce in the first half of 1988. We will highlight its advantages over standard SRAMs in high frequency computer system operation. This is followed by an application example for a MC68030 cache subsystem.

ARCHITECTURE AND OPERATION

ARCHITECTURE

A block diagram of the 16K × 4 Synchronous SRAM is shown in Figure 1. This diagram shows all inputs, outputs, and control signals ($\overline{W}$, $\overline{S}$, and K) to the part; addresses (A0-A13), data in (D0-D3), data out (Q0-Q3), clock (K), chip select ($\overline{S}$), and write enable ($\overline{W}$). All inputs, outputs, write enable, and chip select are latched by the clock.

The latches are one of two types, either positive edge triggered or transparent. The positive edge triggered latches are latched by the rising edge of clock (K). The transparent latches are frozen when the clock is in the high state and open when it is in the low state. Our parts feature two of the possible combinations of input and output latches. The first part, the MCM6292, features edge triggered latches on the inputs and transparent latches on the outputs. Our second part, the MCM6293, has edge triggered latches on both inputs and outputs, to aid in pipelining data.

The output buffers on all of our parts are capable of driving 130 pF loads. The output buffers were designed to drive this load because in some systems the latches that they replace would be required to drive a comparable size load. Due to the size of load that the output buffers must drive, and the speed at which the part operates, we have added an extra ground pin (V_{SSQ}). This pin is the ground connection for all of our output drivers, and allows us to drive our outputs harder and also gives us noise immunity on the ground bus.

For systems that require a common I/O configuration we expect to offer the MCM6295 and the MCM6294, which are the MCM6292 and the MCM6293 with an asynchronous output enable ($\overline{G}$) option. These parts, the MCM6294 and the MCM6295, replace the chip select ($\overline{S}$) buffer with an asynchronous output enable ($\overline{G}$) buffer.

OPERATION

The operation of these parts is much the same as a standard 16K × 4 SRAM except for the fact that the inputs and outputs are latched and the cycle begins with the low to high transition of the clock. The following examples will concentrate on a read and write cycle for both the MCM6292 and the MCM6293. The MCM6294 and MCM6295 read and write cycles are the same as the MCM6292 and the MCM6293 except that the outputs can be put into a high impedance state at any time by using output enable ($\overline{G}$).

During a read, see Figure 2, all inputs are latched into the part at the rising edge of the clock (K) in both the MCM6292 and the MCM6293. For the MCM6292, when clock goes high, the outputs become latched and are held in that state until the clock falls low. Since the output latches are transparent, during clock low time, there are two possible access times, t_{KHQV} and t_{KLQV}. These access times are dependent upon the high pulse width of the clock. If the high pulse width is less than the access time of the memory array the longer t_{KHQV} spec is the clock access time. However if the clock high pulse is longer than the memory array access time, the clock access time becomes t_{KLQV}. For the MCM6293 the

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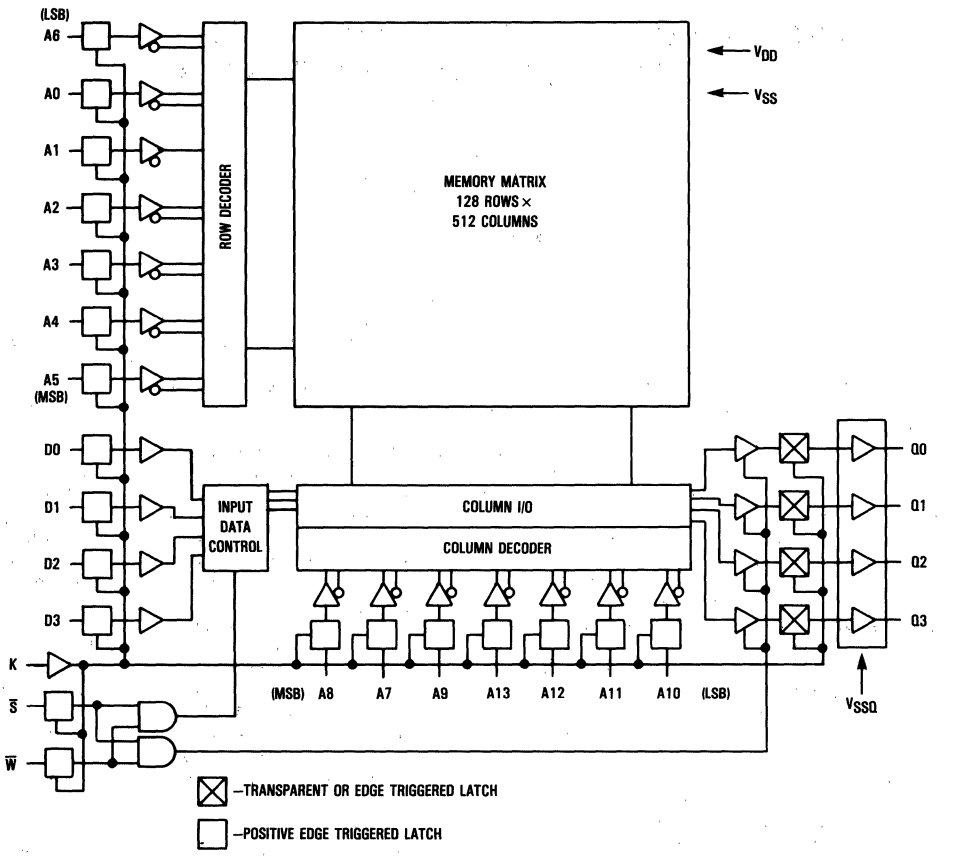

Figure 1. Synchronous SRAM Block Diagram

outputs transition only when the clock switches from low to high. The output data that is latched during the low to high transition of the clock is the data from the previous read cycle.

For the write cycle, see Figure 3, all inputs are handled in the same manner as in the read. Since both write enable and the input data are sampled on the rising edge of the clock the write becomes self timed. This eliminates the need for complex off chip write pulse generating circuitry. The outputs are put in a high impedance state t_{KLOZ} after the clock falls low for the MCM6292. In the MCM6293 the output buffers will not go into a high impedance state until the low to high transition of the clock at the beginning of the next cycle. The MCM6294 and the MCM6295 allow the user to put the output buffers into a high impedance state asynchronously by using the output enable input. This allows the user to put the output buffers into a high impedance state earlier in the cycle, which eases the data contention problem when the part is used in a common I/O system configuration.

SYSTEM ADVANTAGES (SRAM vs SSRAM)

SYSTEM DESCRIPTION AND TIMING

Figure 7 shows two examples of a 16K x 32 bit memory using standard parts. The systems shown require eighteen parts each, ten latches and eight 16K x 4 SRAMs, to implement the same function as eight synchronous SRAMs and no glue logic.

The functional equivalent of a MCM6292 is the standard 16K x 4 SRAM with edge triggered latches on the inputs and transparent latches on the outputs, as shown at the top of Figure 7. The parts used in this example are six 'F374 octal D-type flip flops, four 'F373 octal transparent latches, and eight 6288 16K x 4 SRAMs. The predicted timing diagram for the system is shown in Figure 4. This timing diagram compares the predicted system access with that of the MCM6292. In the timing diagrams an approximate skew of 5 ns was added to the address timing to allow for some propagation delay from the MPU or CPU. For the purpose of comparison, three timing

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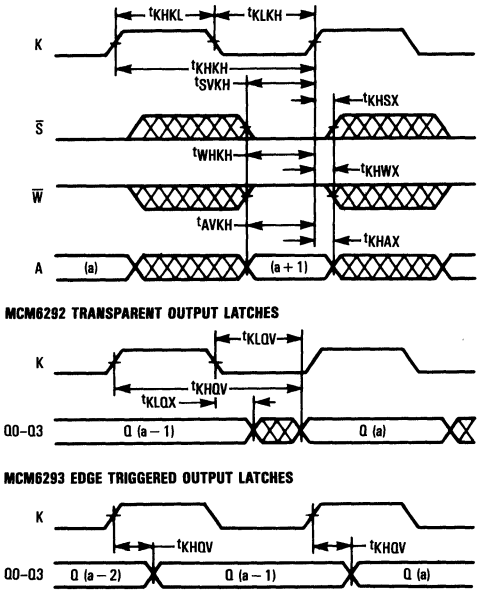
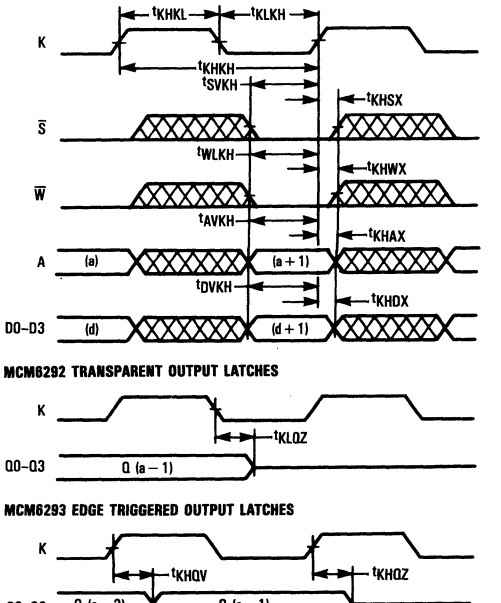


NOTE: Both MCM6292 and MCM6293 are available with an asynchronous $\overline{G}$ option.

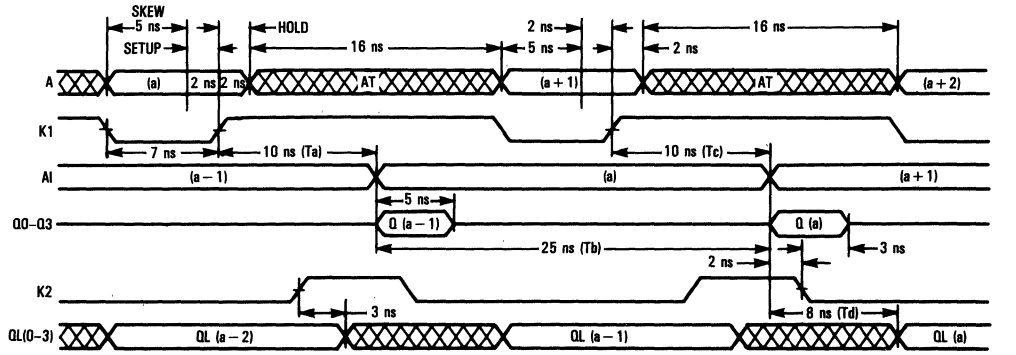
Figure 2. Read Cycle Comparison



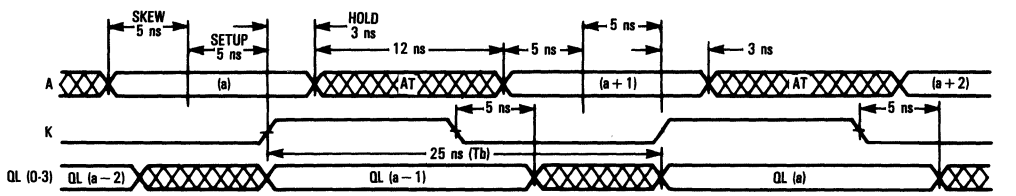
NOTE: Both MCM6292 and MCM6293 are available with an asynchronous $\overline{G}$ option.

Figure 3. Write Cycle Comparison

STANDARD SRAM WITH EDGE TRIGGERED LATCHES ON INPUTS AND TRANSPARENT LATCHES ON OUTPUTS (t_{AVQV} = 50 ns, t_{CYC} = 25 ns)



MCM6292 SYNCHRONOUS SRAM (t_{AVQV} = 35 ns, t_{CYC} = 25 ns)



NOTE: AT—Address generation and transition time.

Figure 4. Standard SRAM vs MCM6292 Timing Diagram

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parameters were calculated, t_{CYC} (cycle time), t_{AVQV} (address valid to data out valid time), and t_{KQV} (address clock valid to data out valid time). The equations used to calculate each of the timing parameters for the standard SRAMs are as follows:

$$t_{CYC} = Ta + Tb - Tc$$
$$t_{KQV} = Ta + Tb + Td$$
$$t_{AVQV} = skew + setup + Ta + Tb + Td \ .$$

The equivalent timing parameters for the MCM6292 can be determined as follows:

$$t_{CYC} = Tb$$
$$t_{KQV} = Tb$$
$$t_{AVQV} = skew + setup + Tb \ .$$

The equivalent circuit for the MCM6293, as shown at the bottom of Figure 7, is a 16K × 4 SRAM with positive edge triggered latches on both inputs and outputs. For this example the parts used are, eight 6288 16K × 4 SRAMs and ten 'F374 octal D-type flip flops. The timing diagrams for this example are shown in Figure 5. The equations for calculating the timing parameters are as follows:

Standard SRAMs:

$$t_{CYC} = Ta + Tb - Tc$$
$$t_{KQV} = Ta + Tb + Td + Te$$
$$t_{AVQV} = skew + setup + Ta + Tb + Td + Te$$

MCM6293:

$$t_{CYC} = Tb$$
$$t_{KQV} = Tb + Te$$
$$t_{AVQV} = skew + setup + Tb + Te$$

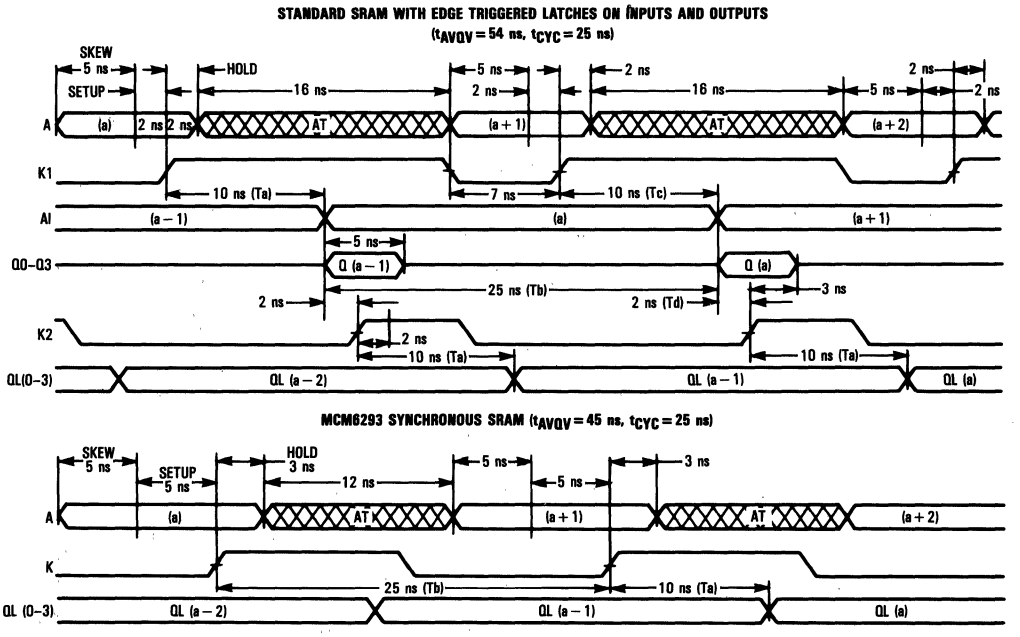
SYSTEM COMPARISONS

The timing parameters for the 25 ns 16K × 4 synchronous SRAMs and the equivalent circuits using 25 ns SRAMs are in Table 1. Also in Table 1 are timing parameters for other systems using progressively faster and more expensive SRAMs. From this table it can be determined that if either t_{AVQV} or t_{KQV} were the most important timing constraints a much faster SRAM would be needed to match the performance of the synchronous SRAM. For the performance of the system built with standard parts to match the performance of the 25 ns MCM6292, it would be necessary to use a 10 ns SRAM. Similarly, if the system used 25 ns MCM6293s the equivalent system made from standard parts would require 15 ns SRAMs.

Another important advantage of the synchronous parts over standard parts is the board level chip count; 18 parts are necessary when using standard SRAMs while only 8 parts are needed for the synchronous SRAM implementation. This is critical when board space is an important factor. Also, the fact that data and write enable are sampled on the rising edge of the clock, eliminates the need for complex write pulse generating circuitry. Finally, in order to get the high speed performance out of standard SRAMs, it requires precise timing and phase control of two clock signals (K1 and K2), while in the synchronous part only one clock (K) is needed.

APPLICATION: MC68030 CACHE SUBSYSTEM

The Synchronous SRAM combined with the Motorola MC68030 microprocessor illustrates the potential of this advanced memory architecture. The high frequency performance of microprocessors like the MC68030 can be impaired by having



NOTE: AT—Address generation and transition time.

Figure 5. Standard SRAM vs MCM6293 Timing Diagram

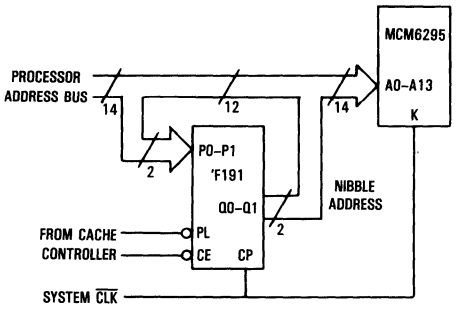


Figure 6. MC68030 Burst Read Addressing

to wait for slow memory to respond. For this example we will use a 16K by 32-bit cache system running at frequencies of up to 33-1/3 MHz. This does not mean that you can purchase MC68030 processors today at this speed, only that our 25 ns SSRAM will support this processor up to that speed. The MC68030 timings used for this example are extrapolated from the current 16.67 and 20 MHz specifications that exist today and are not intended to be the official specifications.

We will exploit the processor's burst read cycle which supports burst filling of its on-chip instruction and data caches, adding to the overall system performance. The on-chip caches are organized with a block size of four long words, so that there is only one tag for the four long words in a block. Since locality of reference is present to some degree in most programs, filling of all four entries when a single entry misses can be advantageous, especially if the time spent filling the additional entries is minimal. When the caches are burst-filled, data can be latched by the processor in as little as one clock for each 32 bits.[1]

The timing diagram shown in Figure 8 shows a burst read cycle (four 32-bit words read) in a 3-1-1-1 clock cycle configuration. The first word is read in 3 clock cycles and the remaining three words are read in one clock cycle each. The burst read cycle begins with a cache burst request ($\overline{\text{CBREQ}}$) from the processor followed by a cache burst acknowledge ($\overline{\text{CBACK}}$) from the memory controller. This means the processor is requesting a burst cycle and the accessed memory can comply. During the burst cycle the processor supplies the starting address in the normal synchronous fashion and holds it valid until all four long words are read. It does not provide the next three addresses required to complete the burst fill, so they must be generated off chip. For this example we used a 'F191 counter whose control signals, PL and $\overline{\text{CE}}$, are generated in a cache controller. The clock input, CP ($\overline{\text{CLK}}$), is the opposite phase of the system clock. The SSRAM operates with the same inverted system clock ($\overline{\text{CLK}}$) and receives its addresses from two sources; A2–A13 are supplied from the processor's address bus, and A0–A1 are supplied from the 'F191 counter to allow nibble counting as shown in Figure 6.

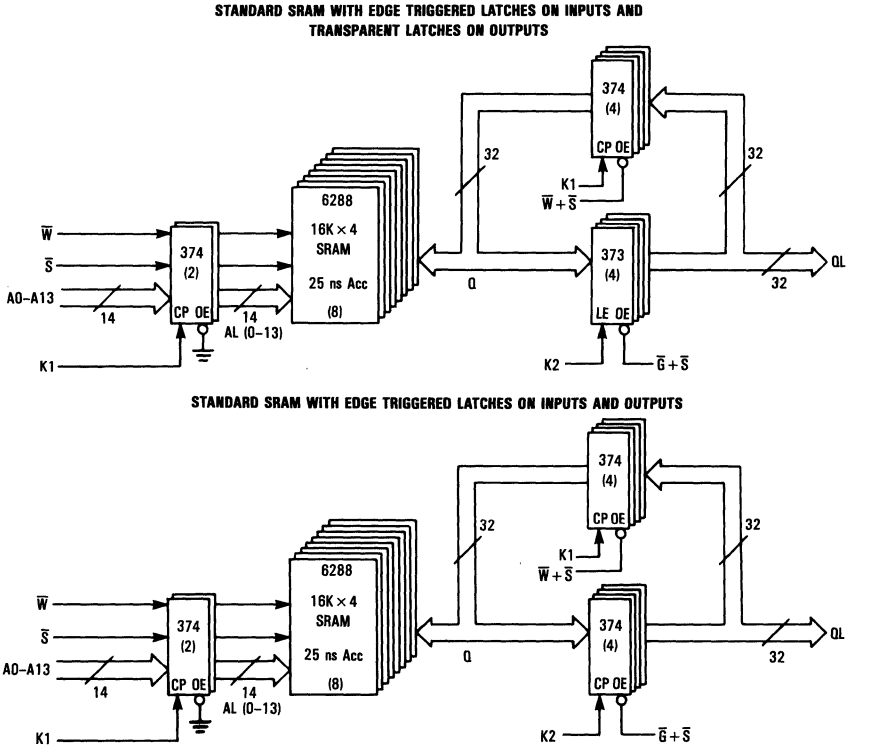


Figure 7. Standard SRAM Implementations

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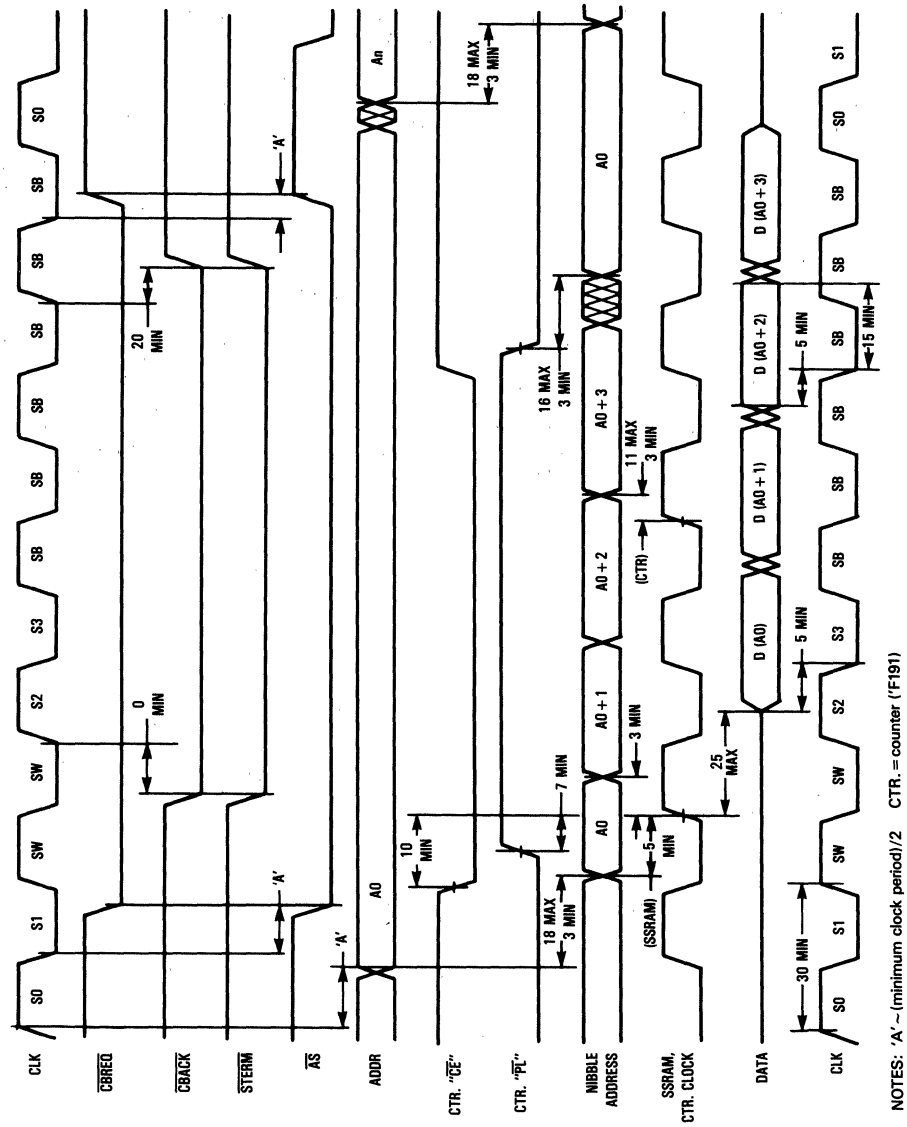

NOTES: 'A' ~ (minimum clock period)/2 CTR. = counter ('F191)

Figure 8. MC68030 Burst Fill Timing

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Table 1. Timing Comparisons Between SSRAMs and SRAMs

Timings	25 ns SSRAM		25 ns SRAM		20 ns SRAM		15 ns SRAM		10 ns SRAM	
	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output
t_{CYC}	25 ns	25 ns	25 ns	25 ns	20 ns	20 ns	15 ns	15 ns	10 ns	10 ns
t_{AVQV}	35 ns	45 ns	50 ns	54 ns	45 ns	49 ns	40 ns	44 ns	35 ns	39 ns
t_{KQV}	25 ns	35 ns	43 ns	43 ns	38 ns	38 ns	33 ns	33 ns	28 ns	28 ns

The timing begins with the request, the acknowledgment and the generation of the first address. This address is used to access one of the four long words. Two low order address signals from this address must also be loaded into the counter. At the beginning of the cycle the parallel load signal for the counter is enabled, the address is then loaded in and the PL signal can be disabled. The counter will provide the memory this first address a propagation delay later and then increment it on successive clock edges to supply the memory with the remaining three needed addresses. After receiving all four 32-bit words the processor is free to continue.

A similar system built using standard MCM6288 (16K × 4) type SRAMs would require the use of off-chip input and output latches ('F373 or 'F374 type) in addition to the counter. It would require four chips to perform the latching function for 32-bit data in, and four chips to latch the 32-bit data out, for a total of eight additional 20 pin packages added to the memory PC board. This standard SRAM cache system would also require additional logic in the cache controller to support the write pulse, associated write enable and data in timing for write cycles, and the generation of a second clock (LE or CP) to separately control the input and output latches. To attain the cache system speed of 33-1/3 MHz would require a SRAM access time of approximately one bin faster than the SSRAM. In addition the external glue logic would have to be faster than what is currently offered in the 74F series logic.

SUMMARY

There are many applications for high-speed Synchronous Static RAMs. The integration of latches, self timed writes, bus drive capability, and clock control greatly simplifies system level implementation and ease of use. These features will allow SSRAMs to continue to support higher frequency system operation. Depending on the application, Synchronous Static RAMs can provide up to a 10 to 15 ns improvement in system access time over SRAMs that spec the same chip speeds. They save precious board space by reducing the chip count, and simplify controller design for latch control and write cycles.

ACKNOWLEDGMENTS

The authors would like to thank Brian Branson and Bill Martino for their inputs and comments that helped complete this paper. And special thanks to Richard Crisp for his MC68030 cache system timing analysis.

REFERENCES

1. Motorola Semiconductor Technical Data: "Technical Summary: Second Generation 32-Bit Enhanced Microprocessor", 1986.
2. Motorola Semiconductor Technical Data: "Fast and LS TTL Data", 1986.

Motorola Inc. can provide the usual promotional and technical literature associated with the Synchronous Static RAM family.

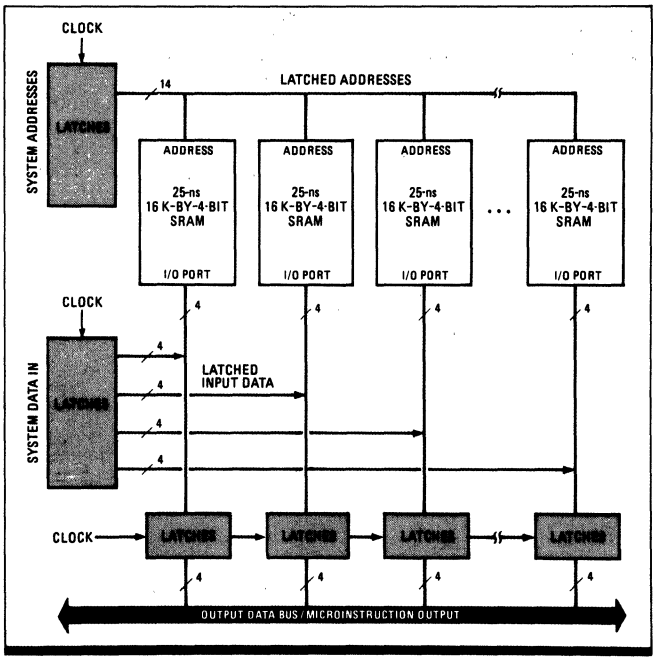
MOTOROLA'S RADICAL SRAM DESIGN SPEEDS SYSTEMS 40%

Key to higher throughput is a synchronous clocked architecture and on-chip I/O latches; the combination cuts interconnection delay by up to 20 ns

by Bernard C. Cole

Engineers at Motorola Inc.'s MOS Memory Products Division are taking a radically different approach from the current asynchronous architecture for static random-access memories. They are developing a synchronous architecture the company claims will improve system throughput by as much as 40% and will reduce system component count by as much as 50%.

The keys to the Austin, Texas, division's new architecture are: replacing the traditional self-clocked address-transition-detection circuitry, found in conventional asynchronous SRAMs, with a synchronous clocked architecture, and adding critical input and output latches on-chip. The combination of these features eliminates as much as 8 to 10 ns of interconnection delay on input and on output, says William Martino, the division's design manager for specialized memories. It also eliminates circuitry often required to make asynchronous devices appear synchronous in high-performance cache-memory systems, which depend heavily on the synchronization of critical timing parameters. Also incorporated on the chip are drive transistors capable of driving buses with capacitive loads of up to 130 pF without additional external circuitry. Motorola designers also enlarged the geometries to increase the inherent drive capability of the devices.



1. ASYNCHRONOUS. Using asynchronous SRAMs, designers of high-performance synchronous systems must incorporate latches on the inputs and outputs, adding 15 to 20 ns of delay.

The new architecture has been incorporated into four initial products that are members of a new family of 16-Kbit-by-4-bit SRAMs with cycle times ranging from 25 to 35 ns and access times in the 10 to 35 ns range. This equals that of comparably sized asynchronous SRAMs fabricated with the same 1.5-μm double-metal CMOS process [*Electronics*, Aug. 7, 1986, p. 81], says Frank Miller, synchronous SRAM project leader at the division. But Miller emphasizes that the elimination of as much as 20 ns of interconnection delay can almost double system-level performance.

Motorola expects to offer samples of the four clocked synchronous SRAM parts within about a month and plans to be in volume production by the end of the fourth quarter. Two of the devices, the MCM6292 and 6295, incorporate level-sensitive transparent latches,

whereas the MCM6293 and 6294 use positive-edge-triggered latches. Also the 6294 and 6295 each have an output enable pin that allows the user asynchronous control of the output buffers, allowing the parts to be used in common I/O at the board level. All the devices feature an active ac power dissipation of 600 mW and an active dc power of only 100 mW.

The advantages of Motorola's new family of synchronous SRAMs outweigh the advantages of asynchronous devices, Martino says. In asynchronous devices, great reliance is placed on address-transition detection, a self-clocking scheme that uses the address-signal transition, or edge, as a reference to synchronizing all operations on the chip to that signal. Martino says that asynchronous SRAMs are widely used because they allow and recognize address changes at any time. As a result, no external global clock is necessary to access data, making them easy to use. Also, compared with dynamic RAMs, asynchronous SRAMs take much less external circuitry, says Miller. Because they are free-running, the addresses can be changed whenever needed, and they are very easy to control.

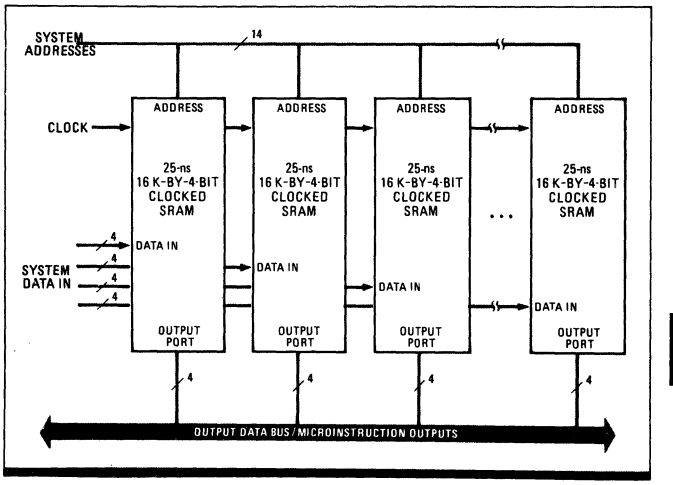
Although they are easy to use, asynchronous SRAMs must be surrounded by considerable external logic (see fig. 1) in many applications in high-performance processor systems such as writable control stores, data caches, and cache-tag memories [*Electronics*, June 11, 1987, p. 78] that require synchronous operation. The extra circuitry imposes a considerable performance penalty, and that can be a problem in cache applications in particular, says Martino, where the speed of memory typically must be at least an order of magnitude faster than main memory. Also, for a cache to work properly, critical timing relationships must be preserved so that a variety of simultaneous operations can be coordinated, such as searching the tag store, getting data out of cache, and replacing proper entries in the cache. The added delay of the external logic can make it difficult to preserve these relationships.

When system speeds were in the 200-ns range, Miller says, the additional 10-to-20-ns penalty of this external logic could be tolerated. "But with processor speeds improving so dramatically, now pushing below 100 ns toward 50 ns, this is a penalty that is critical, especially since the speed of the external logic has not kept pace with the improvements in speed at the chip level."

Depending on the type of register involved and the process used, the delay time, even with high-performance logic families, can be reduced to no more than 7 to 10 ns, says Martino. As a result, most speed improvements have come by pushing the speed of the memory chips themselves. But, as processors speed up, memories with sufficiently low access times are getting harder and harder to produce inexpensively, Martino says. Current 25-to-35-ns asynchronous SRAMs are barely adequate, he says. And newer processors will require a system throughput of no more than 35 to 40 ns. For such throughputs, SRAMs must be pushed to below 10 ns, only achievable now with bipolar and BiCMOS circuits, but at much higher power. "However, even if parts are pushed down to 1 ns and under, there is still that 10 ns on the input and another 10 ns on the output to deal with," says Martino.

The most important element in Motorola's new SRAM architecture (see fig. 2) is the incorporation of the external input and output latches necessary for synchronous operation on board. This design considerably simplifies system design and reduces interconnection delay. "By pulling all of that glue logic on board, it is no longer necessary to drive a large bus to TTL levels," says Martino. "It is now done on-chip, reducing the 10-ns delay down to picosecond levels. This allows the use of a 25-ns part for a 25-to-30-ns bus, rather than using more expensive, power-hungry 10- and 15-ns parts for the same chore."

The Motorola architecture uses address-input latches to hold the addresses so that the processor does not have to hold the addresses valid for the entire cycle. A similar function is served by the data latches on the input. The latches on the output, however, serve a dual function. First, they provide a longer setup and hold time over which the data is valid on the bus, necessary in most processing systems. With a



2. SYNCHRONOUS. By incorporating latches and drivers on-chip, Motorola's synchronous SRAM reduces chip count by more than 50% and reduces interconnection delay.

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standard SRAM at minimum cycle time, that time is about 5 ns without any external latching. This is not enough time for most systems, which require the data to be on the bus for at least 15 to 20 ns, for the processor to receive the valid data. The other function of the latches is to provide the extra drive needed to drive the buses with capacitive loads of up to 130 pF.

The designers of the new SRAMs have eliminated the address-detection-transition circuitry; now they use on-chip clock input for a synchronous clocking scheme

Also incorporated on-chip to support the synchronous operation of the latches is a clock input that controls when the latches are transparent and when they are brought into play. Usually this clock input is a derivative of the system clock; that is, the latches are controlled by the edge of the system clock.

The Motorola designers have eliminated the address-detection-transition circuitry in the new SRAMs. Instead, they use the on-chip clock input to incorporate a synchronous clocking scheme in which the necessary address, data, chip-select, and write-enable information previously brought on board the chip by the address-detection-transition circuitry is now accessed at the beginning of the cycle in reference to the external clock, rather than to the address edge as in the asynchronous scheme. The technique, says Martino, is similar to how a DRAM brings in its addresses with setup and hold times in relation to a read-access or column-access signal input. "Since this device employs a clock with a high-going edge at the beginning of each cycle, it is no longer necessary to detect address- transitions," he says. "The system will tell the chip when to supply the necessary information by providing the clock at the appropriate time."

To eliminate the external drive circuitry, the inherent drive capability of the devices was increased fourfold, says Miller. So Motorola designers enlarged the geometries used to fabricate the pull-up and pull-down transistors, typically on the order of 1,500 μm wide, compared with 400- to 600-μm widths on the standard 30-pF devices, and as small as 6 μm in the memory array and 80 μm in the peripheral circuitry. Moreover, to achieve higher speed in spite of the higher drive currents, n-channel devices, which are only output devices, were used rather than the slower p-channel devices. Furthermore, these output devices were speeded up by incorporating a separate ground-supply pin for the output drivers. "This allowed us to burn more current in the output drivers without corrupting the operation of the rest of the circuit," Miller says.

Although this required a substantial increase in the area devoted to the drive circuitry, the chip size, 146 by 404 mils, is not substantially larger than comparable 64-Kbit asynchronous SRAMs. The extra area required for the larger drivers and for the internal clocking circuitry is offset by the area eliminated by removal of the address-transition-detection circuitry required on asynchronous parts, Martino says. □

INGENIOUS SRAM DESIGN WAS DONE IN REMARKABLY SHORT TIME

For a memory device of such complexity and ingenious design, Motorola's new clocked synchronous static random-access-memory design was completed in a remarkably short time—only 12 months. Moreover, most of the work was done by a four-person design team: William Martino, design manager for specialized memories; Frank Miller, synchronous SRAM project leader; chip designer Scott Remington; and layout engineer Richard Southerland.

One reason for the fast turnaround was that the array and much of the peripheral circuitry is identical to what was used in the company's family of asynchronous 64-Kbit SRAMs, says Miller. "All we had to do was strip off those portions of the circuit relating to the asynchronous operation and replace them with new synchronous elements."

The team drew from two sources for the features incorporated into the synchronous design—including their cumulative design experience. Miller has seven years' experience in memory design. Remington, an eight-year Motorola veteran, worked on the company's 64-Kbit and 1- Mbit DRAMs. Southerland, a five-year Texas Instruments veteran, worked on most of Motorola's asynchronous SRAMs in his two years with the company.

EXPERTS. Miller, Southerland, and Remington, from left, are old hands at memory design.

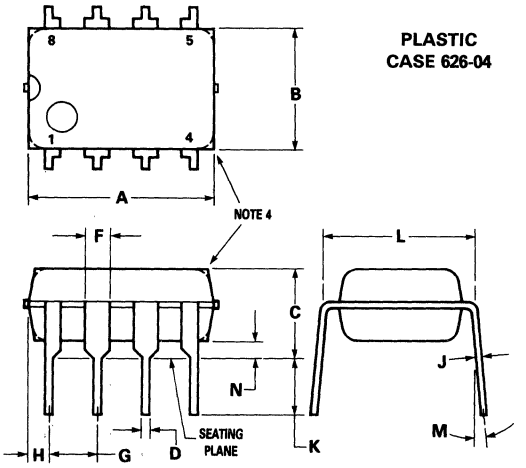
The other source was extensive input from Motorola's customers. "We spent several months defining a variety of special-application memory devices, from dual-port SRAMs and video DRAMs to content-addressable memories," says Miller. "But when we started taking these designs around to customers for input, we found they were most concerned with ways to make standard parts work better. For designers of high-performance systems using cache architectures, one of the largest common denominators was complaints that they had to surround the asynchronous parts with a variety of glue logic to operate appropriately in a synchronous environment.

"The key is listening to the customers, finding out what their specific complaints are, and coming up with parts that satisfy those needs."

Mechanical Data 11

Package availability and ordering information are given on the individual data sheets.

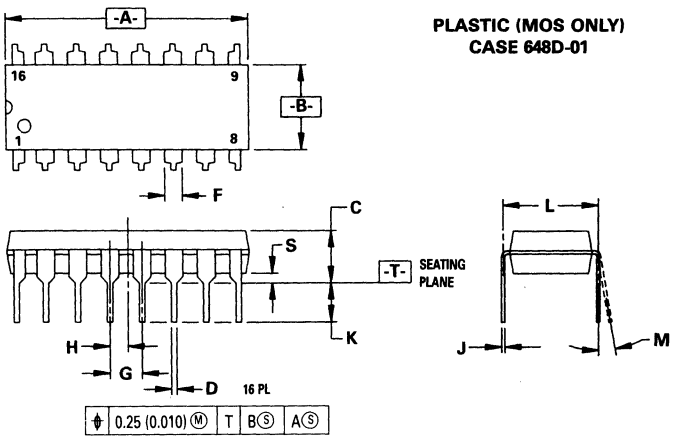
8-PIN PACKAGE



PLASTIC
CASE 626-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

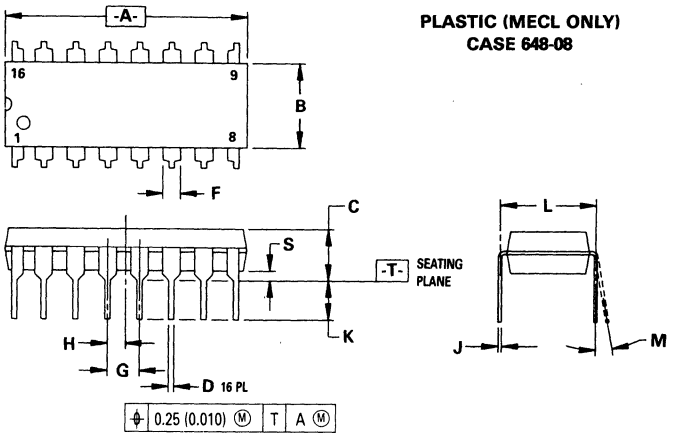
NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ϕ 0.13 (0.005) Ⓜ T A Ⓜ B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.



PLASTIC (MOS ONLY)
CASE 648D-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.30	0.740	0.760
B	6.23	6.60	0.245	0.260
C	3.69	4.19	0.145	0.165
D	0.39	0.53	0.015	0.021
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	3.05	3.55	0.120	0.140
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.39	0.88	0.015	0.035

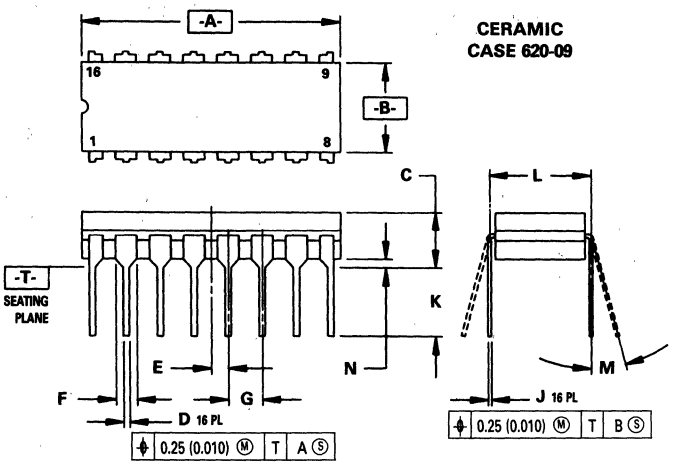
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONS "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNERS OPTIONAL.



PLASTIC (MECL ONLY)
CASE 648-08

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

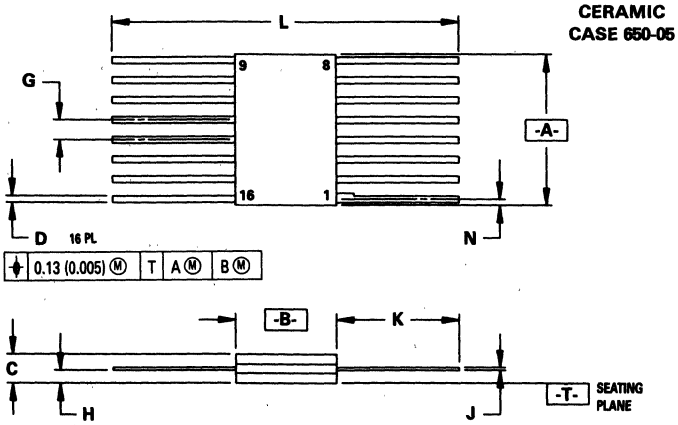
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.



CERAMIC
CASE 620-09

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

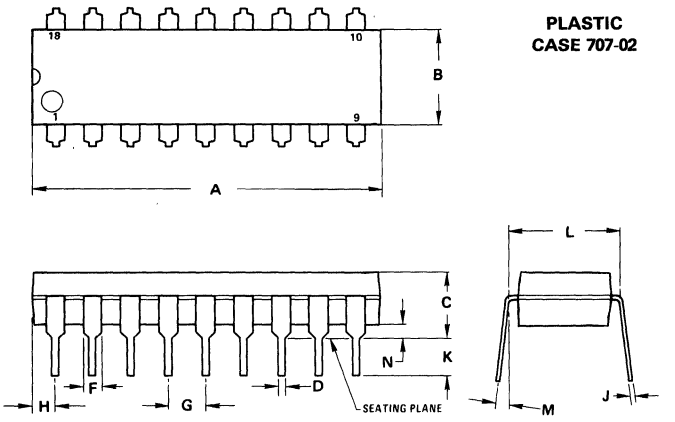


CERAMIC
CASE 650-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	1.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

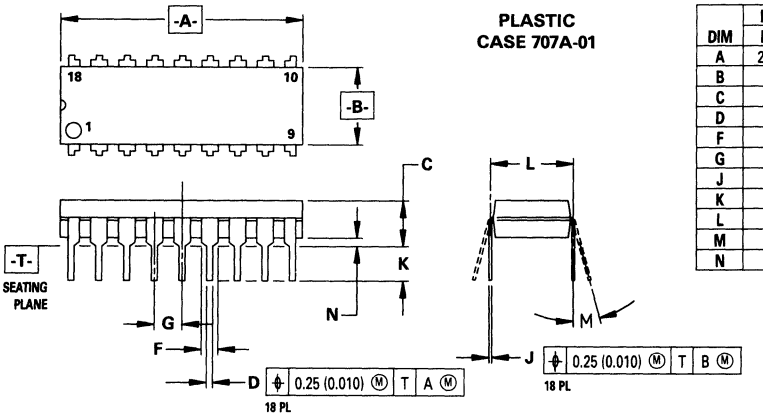
11



PLASTIC
CASE 707-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



PLASTIC
CASE 707A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.85	22.35	0.860	0.880
B	7.12	7.49	0.280	0.295
C	3.56	4.57	0.140	0.180
D	0.36	0.55	0.014	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	2.93	3.42	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

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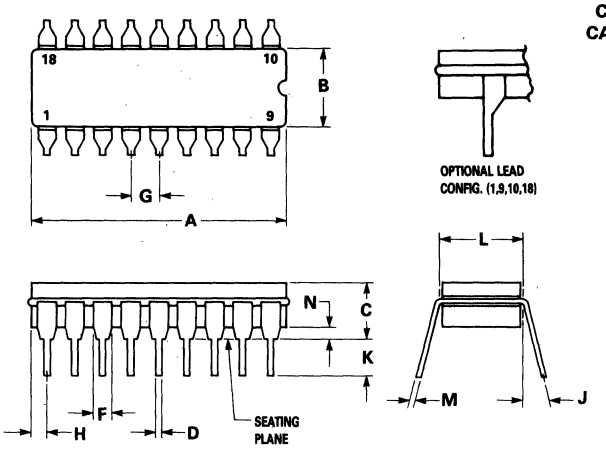
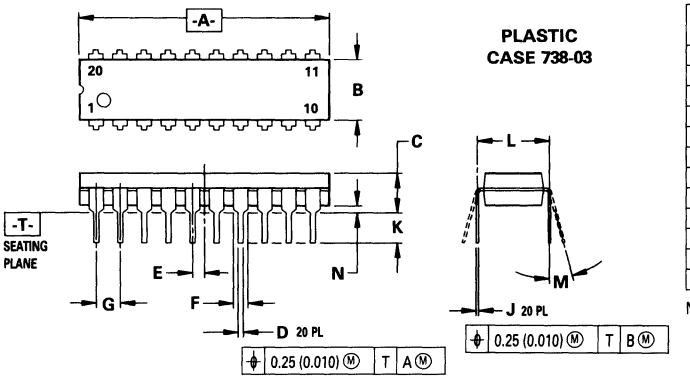
CERAMIC
CASE 726-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

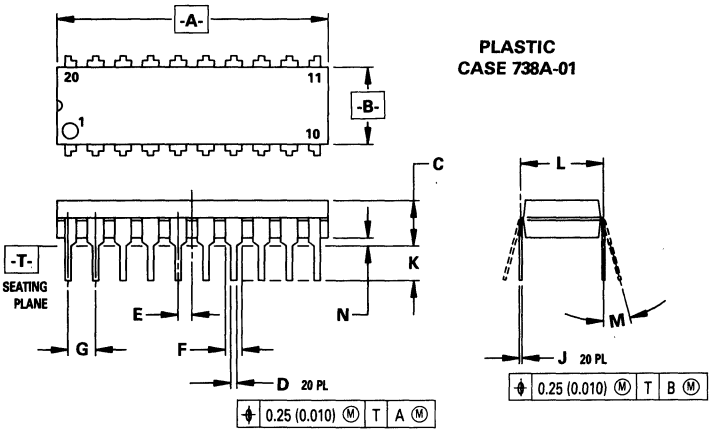
11



PLASTIC
CASE 738-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.



PLASTIC
CASE 738A-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.39	24.89	0.960	0.980
B	7.12	7.49	0.280	0.295
C	3.69	4.44	0.145	0.175
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

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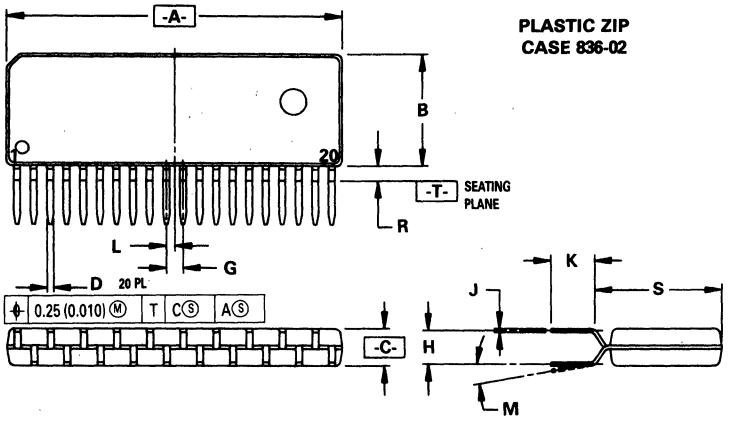
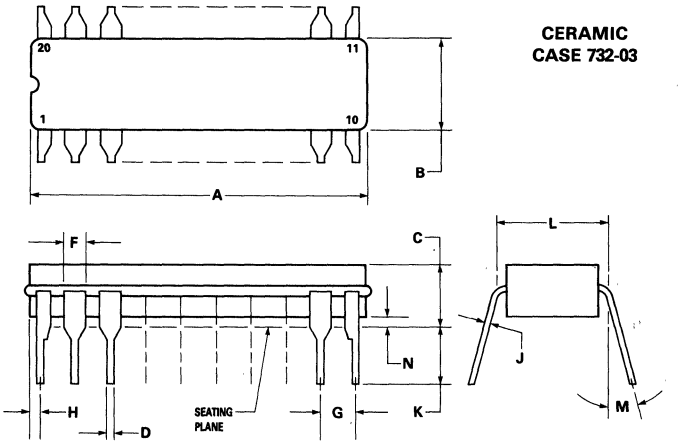


PLASTIC ZIP
CASE 836-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.53	25.90	1.005	1.020
B	8.59	8.89	0.338	0.350
C	2.75	2.94	0.108	0.116
D	0.45	0.55	0.018	0.022
G	1.27 BSC		0.050 BSC	
H	2.44	2.64	0.097	0.103
J	0.23	0.33	0.009	0.013
K	3.18	3.55	0.125	0.140
L	0.64 BSC		0.025 BSC	
M	0°	4°	0°	4°
R	0.89	1.39	0.035	0.055
S	9.66	10.16	0.380	0.400

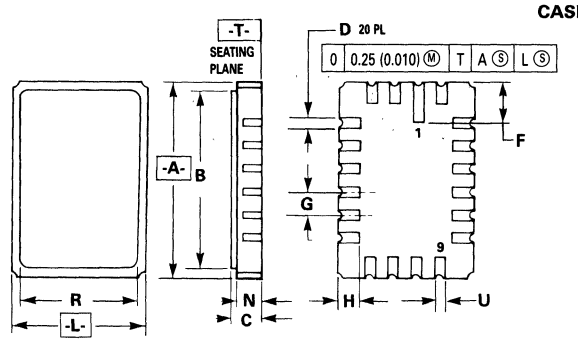
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "H" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS "A", "B", AND "S" DO NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010).



CERAMIC
CASE 732-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

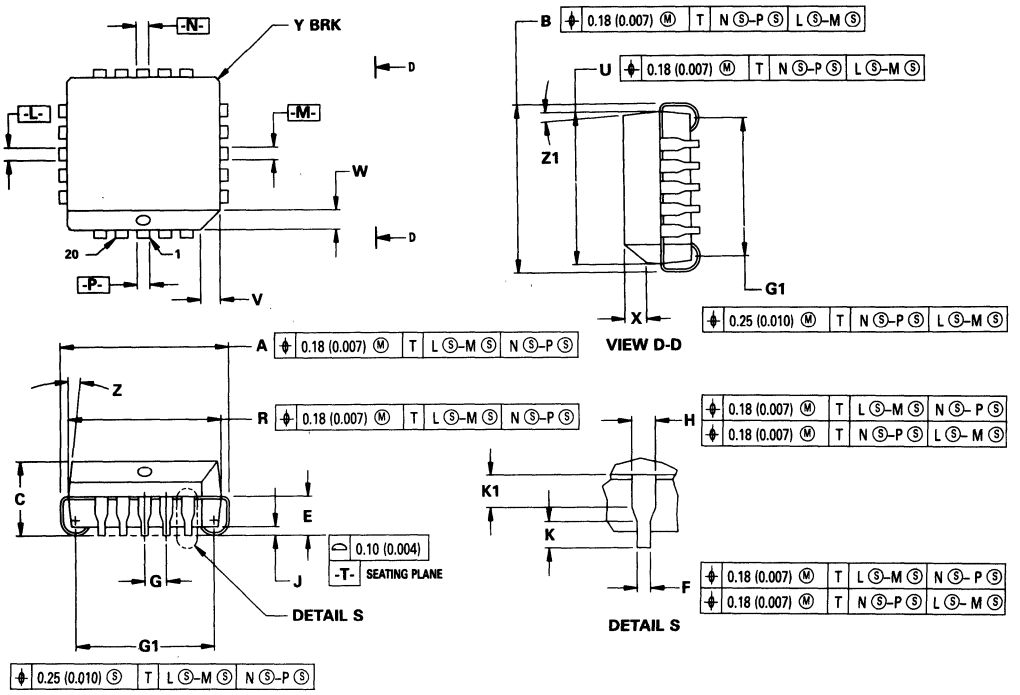


CERAMIC
CASE 756C-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.67	10.92	0.420	0.430
B	10.09	10.41	0.400	0.410
C	1.68	1.98	0.066	0.078
D	0.56	0.71	0.022	0.028
F	2.11	2.46	0.083	0.097
G	1.27 BSC		0.050 BSC	
H	1.07	1.21	0.042	0.048
L	7.24	7.49	0.285	0.295
N	1.40	1.65	0.055	0.065
R	6.61	6.85	0.260	0.270
U	0.28	0.53	0.011	0.021

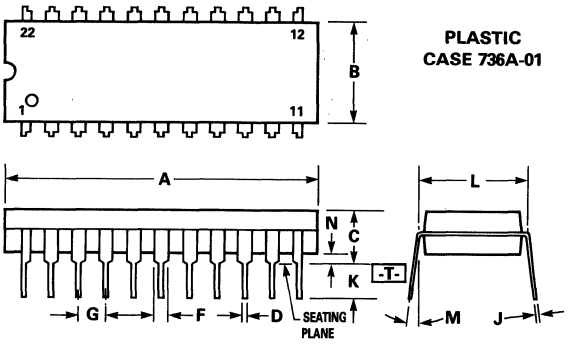
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

PLASTIC CHIP CARRIER
CASE 775-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

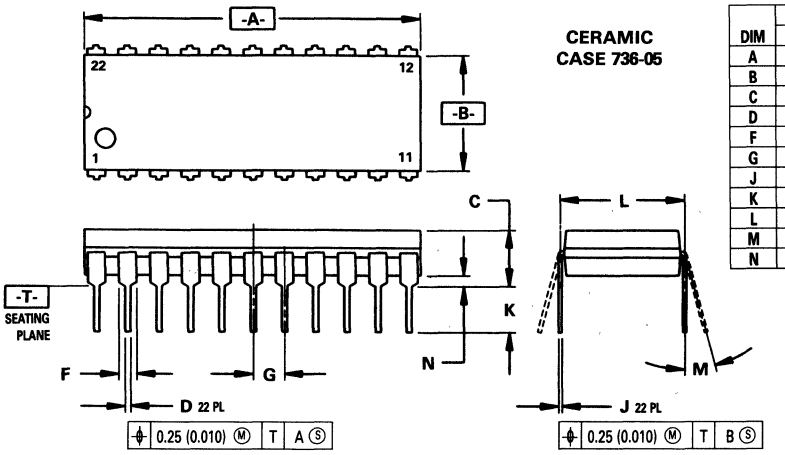
NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.



PLASTIC
CASE 736A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.65	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.74	4.57	0.155	0.180
D	0.38	0.55	0.015	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSION A IS A DATUM. T IS BOTH A DATUM AND A SEATING PLANE.
2. POSITIONAL TOLERANCE FOR D DIMENSION; 22 PL:
   ⌖ | 0.25 (0.010) Ⓜ | -T- | A Ⓜ
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONING AND TOLERANCING PER Y14.5 M, 1982.
5. CONTROLLING DIMENSION: INCH.

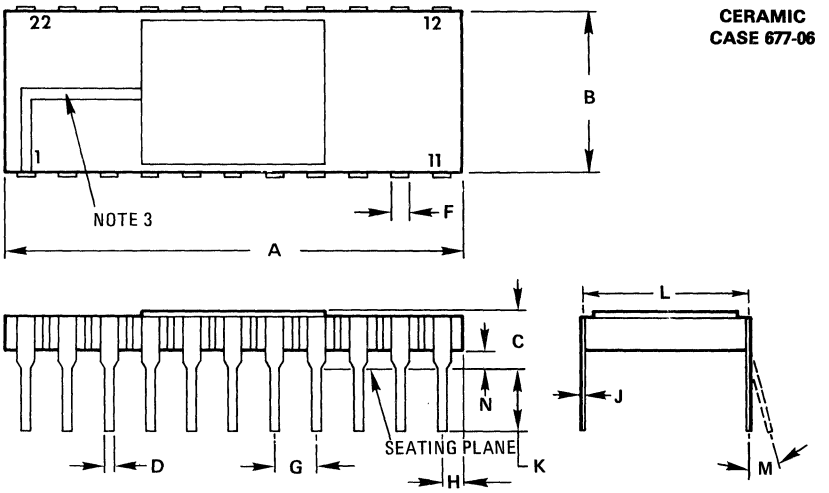


CERAMIC
CASE 736-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.93	27.81	1.060	1.095
B	9.15	9.90	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.39	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.39	0.008	0.015
K	3.18	4.31	0.125	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

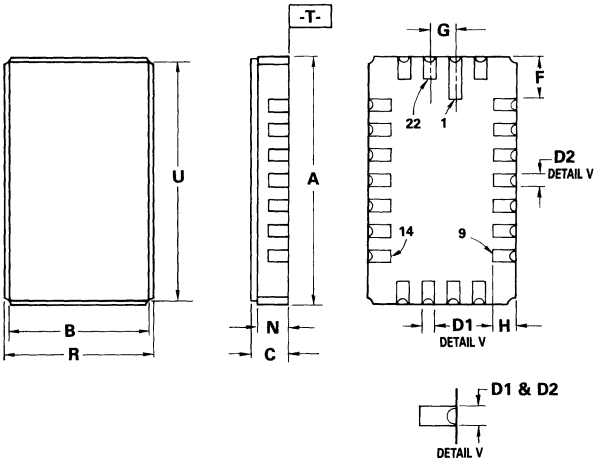
CERAMIC
CASE 677-06



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.15	27.71	1.069	1.091
B	9.65	10.29	0.380	0.405
C	2.67	4.11	0.105	0.162
D	0.38	0.58	0.015	0.023
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	1.52	0.020	0.060
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	9.91	10.41	0.390	0.410
M	–	10°	–	10°
N	0.64	1.27	0.025	0.050

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. EXPOSED CONTACT TO LEAD 1, OPTIONAL.

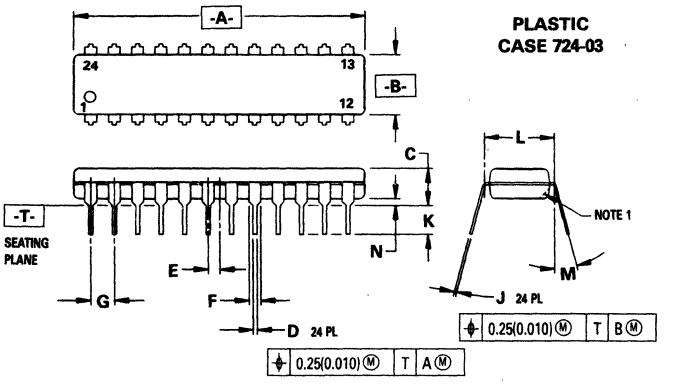
CERAMIC CHIP CARRIER
CASE 800-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.27	12.62	0.483	0.497
B	6.68	7.03	0.263	0.277
C	1.63	1.98	0.064	0.078
D	0.51	0.76	0.020	0.030
F	1.98	2.33	0.078	0.092
G	1.27 BSC		0.050 BSC	
H	0.97	1.32	0.038	0.052
N	1.27	1.62	0.050	0.064
R	7.19	7.54	0.283	0.297
U	11.76	12.11	0.463	0.477

NOTES:
1. DIMENSIONS A AND R ARE DATUMS AND T IS A GAUGE PLANE.
2. POSITIONAL TOLERANCE FOR TERMINALS D_2, 14 PLACES:
   ⌖ | 0.25 (0.010) Ⓜ | T | R Ⓢ | U Ⓢ
   TERMINALS D_1, 8 PLACES:
   ⌖ | 0.25 (0.010) Ⓜ | T | U Ⓢ | R Ⓢ
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIM: INCH.

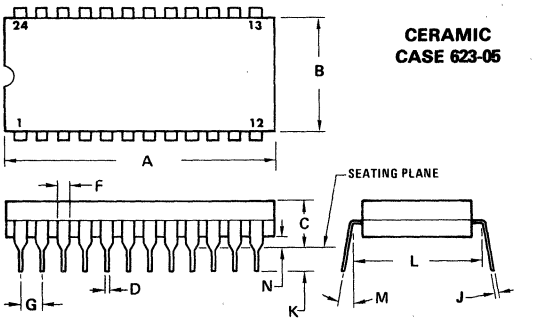
11



PLASTIC
CASE 724-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.



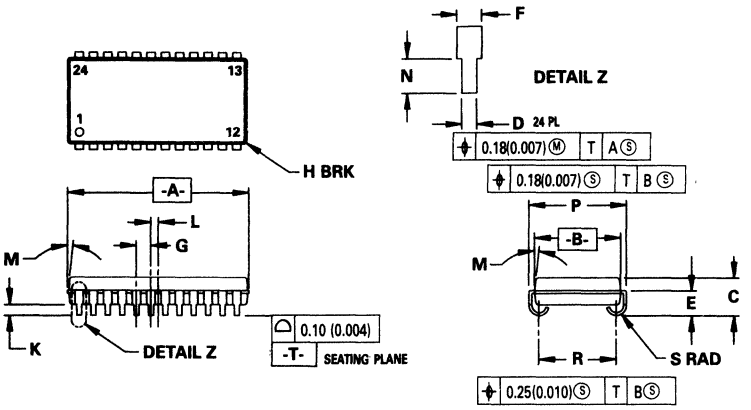
CERAMIC
CASE 623-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

11

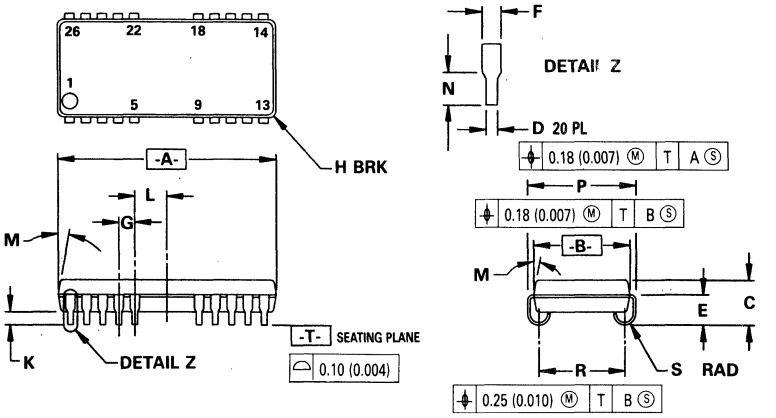
PLASTIC SOJ
CASE 810A-01



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.00	0.620	0.630
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	8.51	8.76	0.335	0.345
R	6.61	7.11	0.260	0.280
S	0.77	1.01	0.030	0.040

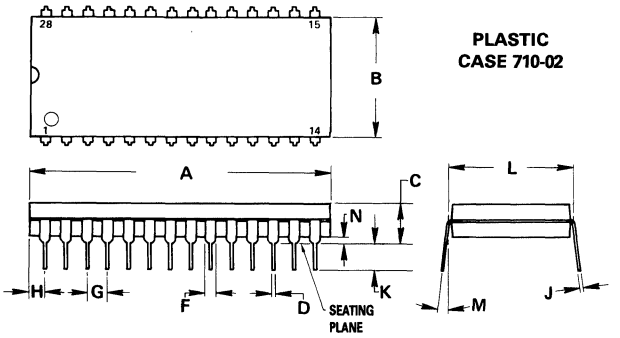
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM "R" TO BE DETERMINED AT DATUM -T-.

PLASTIC SOJ
CASE 822-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	2.54 BSC		0.100 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.39	8.63	0.330	0.340
R	6.61	6.98	0.260	0.275
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.

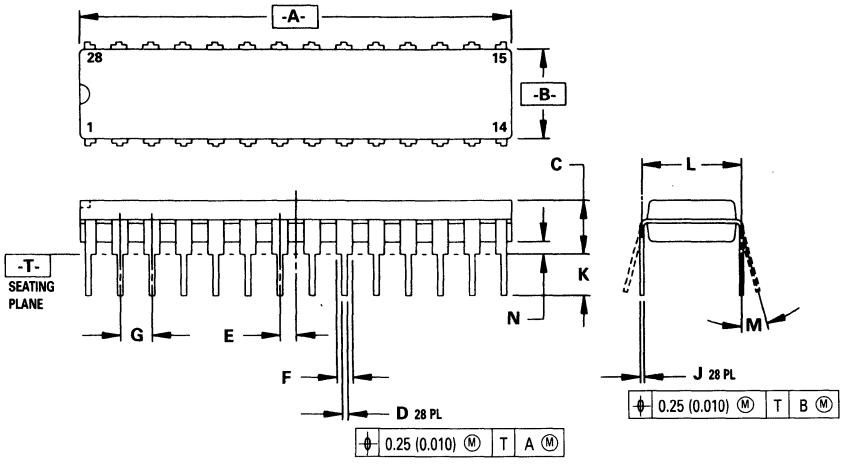


PLASTIC
CASE 710-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

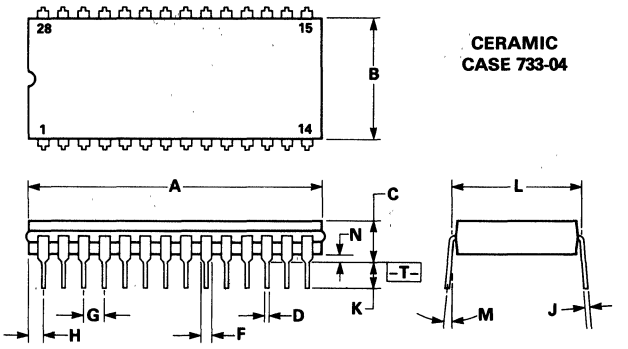
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

PLASTIC
CASE 710A-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	34.17	34.29	1.345	1.350
B	6.86	7.36	0.270	0.290
C	—	4.31	—	0.170
D	0.41	0.50	0.016	0.020
E	1.27 BSC		0.050 BSC	
F	1.15	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	3.42	0.125	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	—	0.015	—

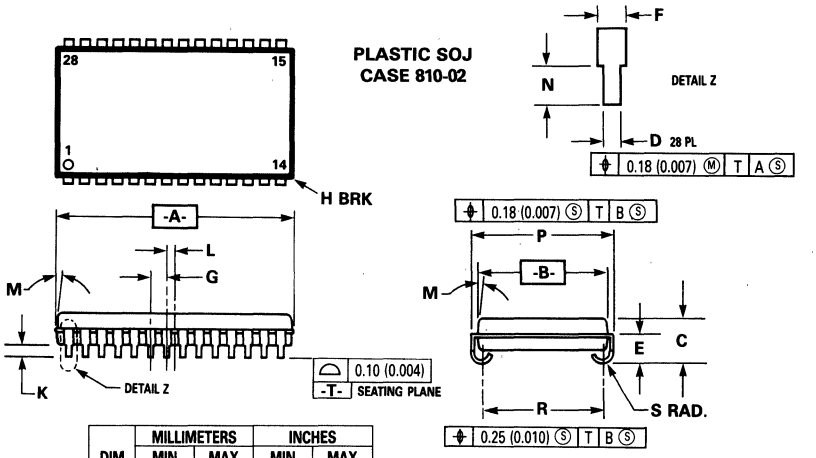
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



CERAMIC
CASE 733-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING & TOLERANCING PER Y14.5, 1982.
7. CONTROLLING DIM: INCH.



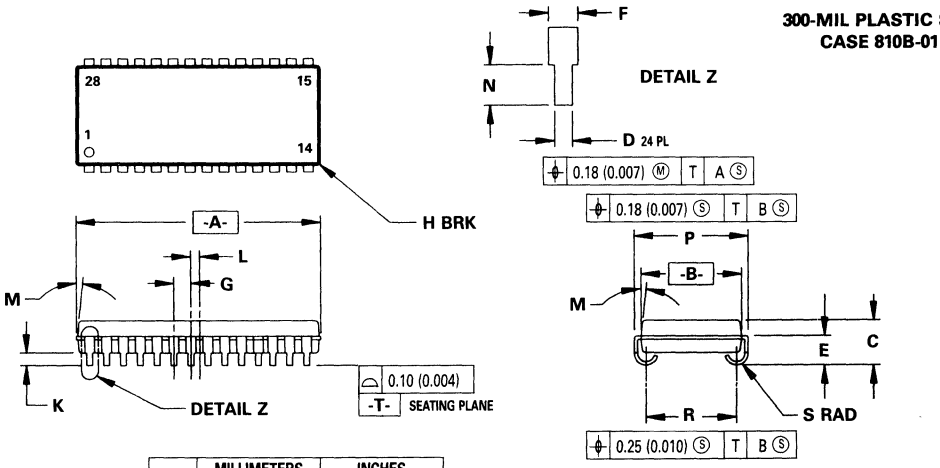
PLASTIC SOJ
CASE 810-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM "R" TO BE DETERMINED AT DATUM -T-.

11

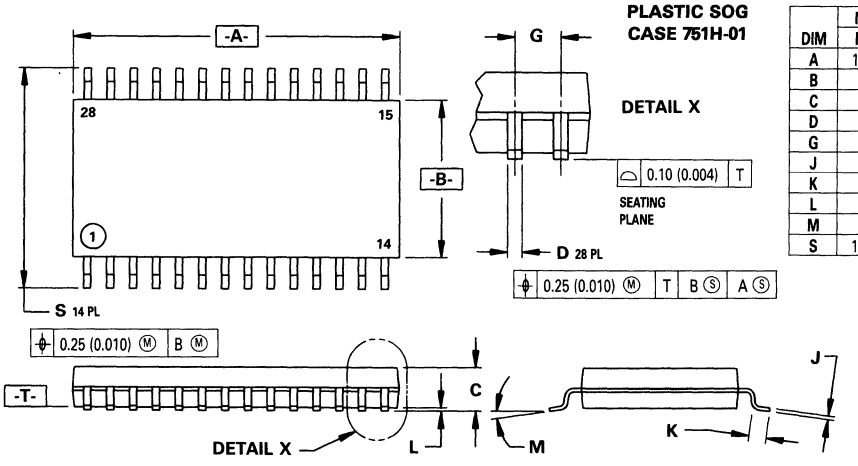
300-MIL PLASTIC SOJ
CASE 810B-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.51	8.76	0.335	0.345
R	6.61	7.11	0.260	0.280
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

PLASTIC SOG
CASE 751H-01

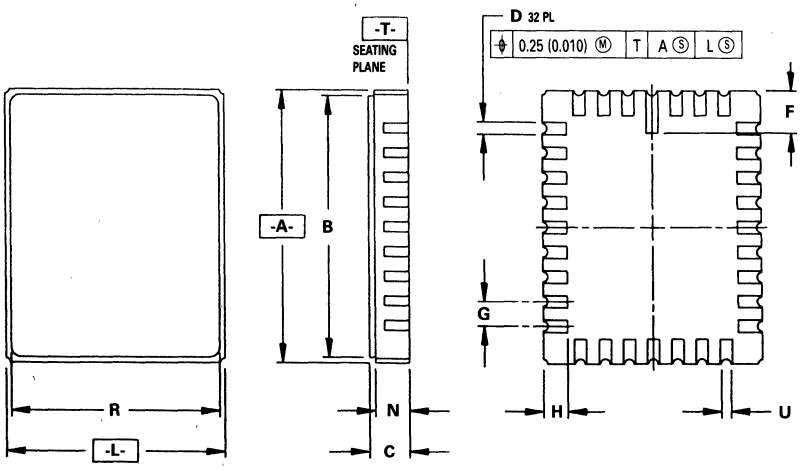


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.70	18.50	0.697	0.728
B	8.23	8.90	0.324	0.350
C	2.04	2.54	0.080	0.100
D	0.35	0.50	0.014	0.020
G	1.27 BSC		0.050 BSC	
J	0.14	0.32	0.0060	0.0125
K	0.40	1.27	0.016	0.050
L	0.05	0.35	0.002	0.014
M	0°	8°	0°	8°
S	11.50	12.70	0.453	0.500

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIM: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

11

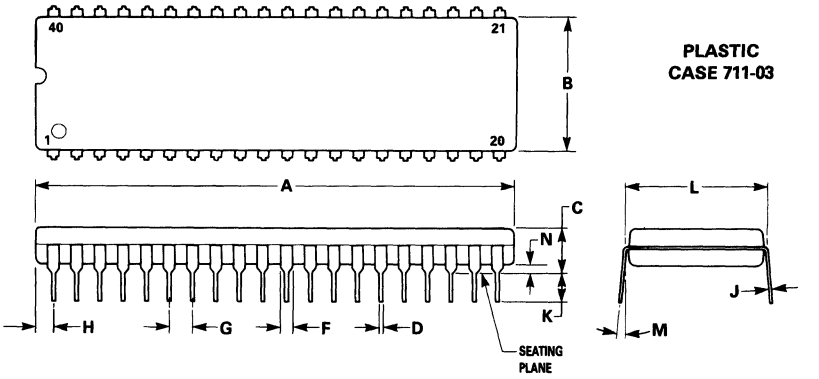
CERAMIC
CASE 766A-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.85	14.22	0.545	0.560
B	13.34	13.58	0.525	0.535
C	1.91	2.26	0.075	0.089
D	0.56	0.71	0.022	0.028
F	1.91	2.41	0.075	0.095
G	1.27 BSC		0.050 BSC	
H	1.07	1.47	0.042	0.058
L	11.31	11.63	0.445	0.458
N	1.63	1.93	0.064	0.076
R	10.80	11.04	0.425	0.435
U	—	0.50	—	0.020

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

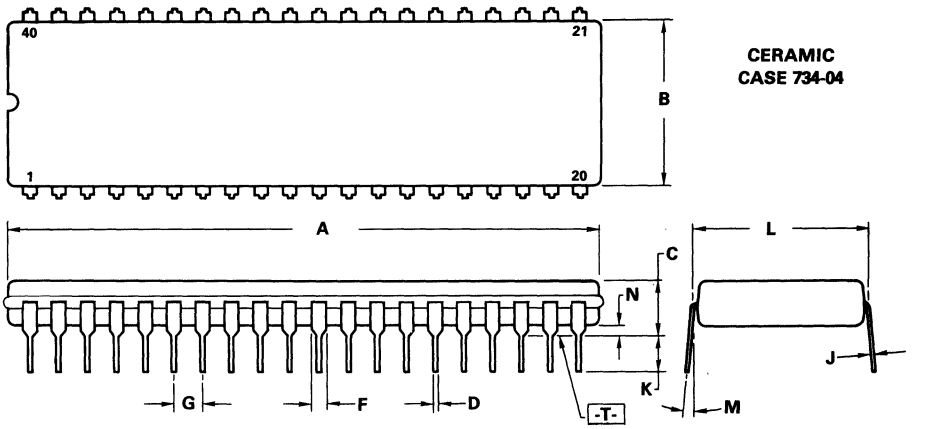
11



PLASTIC
CASE 711-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

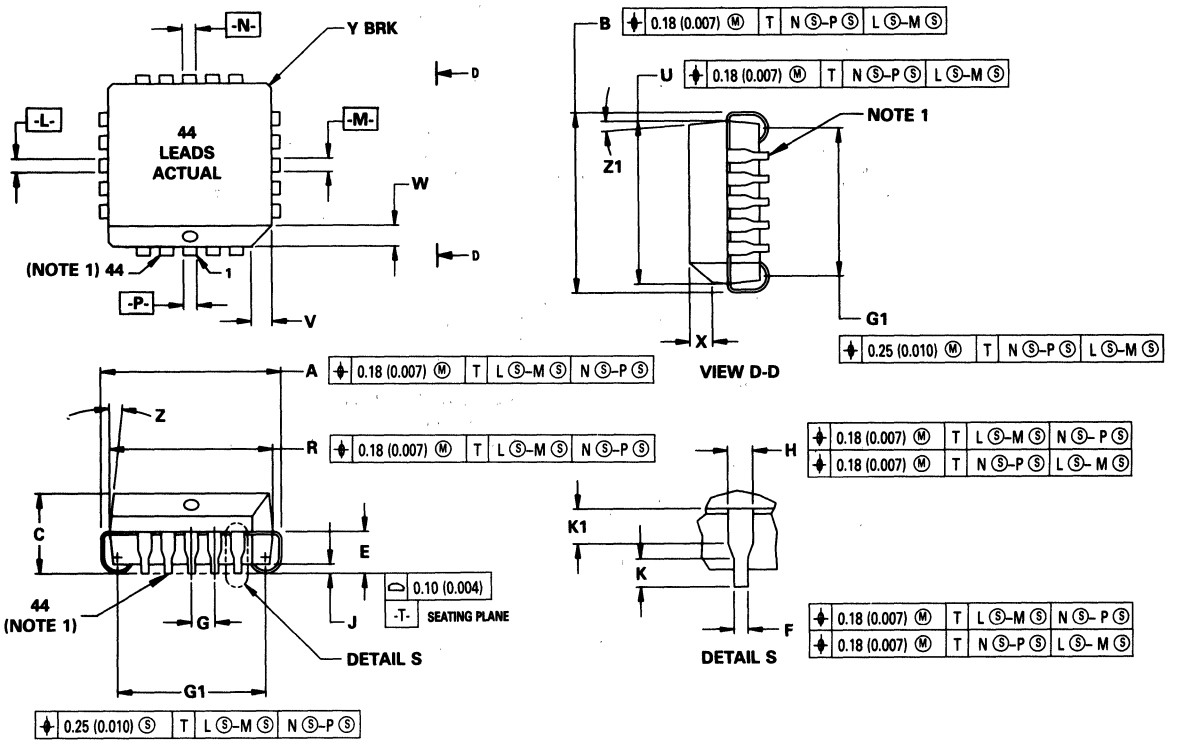


CERAMIC
CASE 734-04

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS A DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

PLASTIC CHIP CARRIER
CASE 777-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

Embossed Tape and Reel

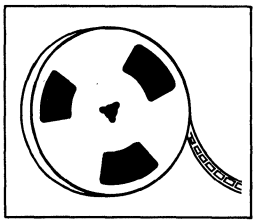
Tape and Reel Data for MOS Memory Surface Mount Devices

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel-back" cover tape.

- 13-Inch Reel
- Used For Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA-481
- SOJ-24, SOJ-28, SOJ-20/26

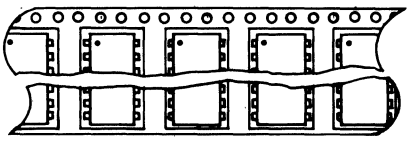
PACKAGES

SOJ-24
SOJ-28
SOJ-20/26



Ordering Information

Use the standard device title and add the required suffix R2. Note that the individual reels have 1000 devices per reel. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.



DIRECTION OF FEED

Package	Tape Width (mm)	Device per Reel	Reel Size (inch)	Tape & Reel Lot Size (Min)	Device Suffix
SOJ-24	24	1,000	13	1,000	R2
SOJ-28	24	1,000	13	1,000	R2
SOJ-20/26	24	1,000	13	1,000	R2

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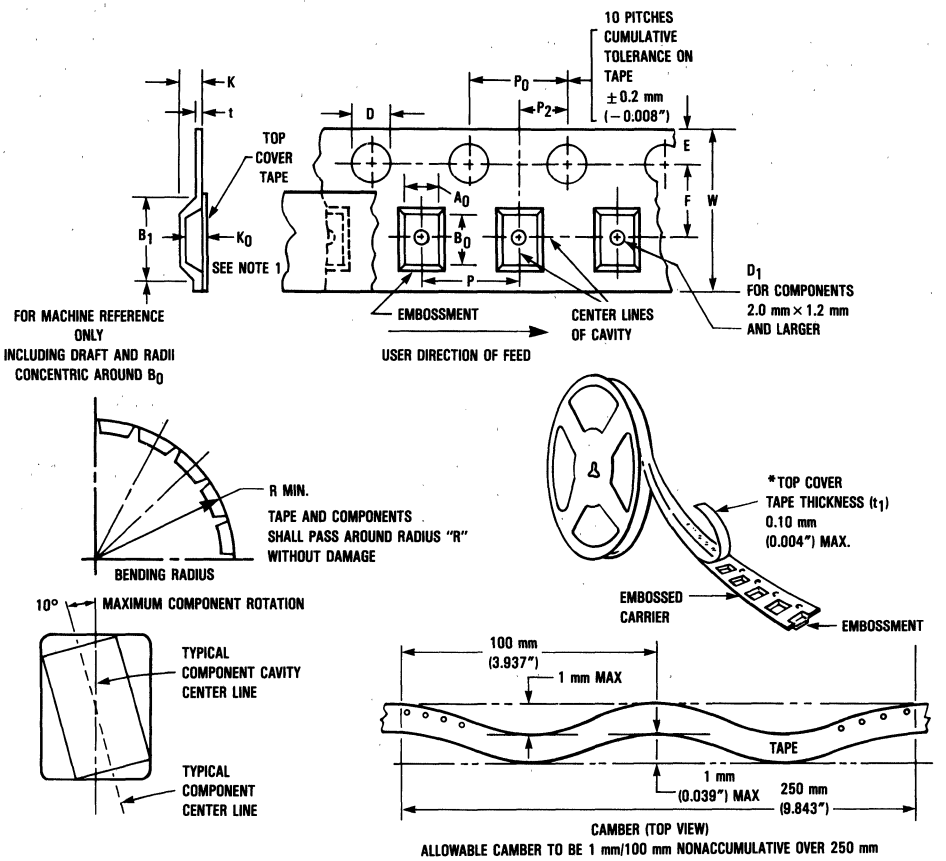
CARRIER TAPE SPECIFICATIONS



DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R Min	T Max	W
24 mm	19.4 mm (0.764")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75±0.1 mm (0.069±0.004")	11.5±0.1 mm (0.453±0.004")	4.0 mm (0.157")	12.0±0.10 mm (0.472±0.004")	4.0±0.1 mm (0.157±0.004")	2.0±0.05 mm (0.079±0.002")	50 mm (1.968")	0.400 mm (0.016")	24±0.2 mm (0.945±0.008")

Metric Dimensions Govern—English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.

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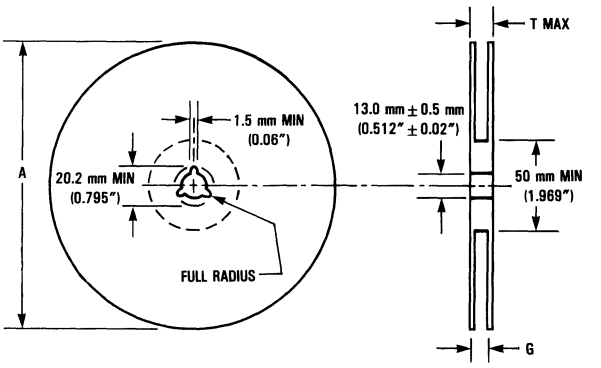
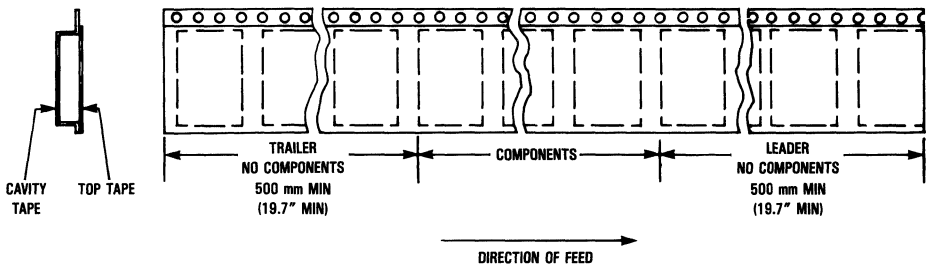
REEL DIMENSIONS

Metric Dimensions Govern—English are in Parentheses for Reference only.



Size	A Max	G	T MAX
24 mm	330 mm (12.992")	24.400 mm, +2.0 mm, −0.0 (0.961", +0.079", −0.00)	30.4 mm (1.197")

TAPE ENDS



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