MOTOROLA

DL140/D
REV 2

High Performance ECL Data
ECLinPS and ECLinPS Lite

Logic Integrated Circuits Division

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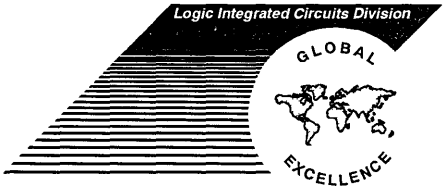
High Performance ECL Data

ECLinPS and ECLinPS Lite



Suggested References:

The user is referred to the following for general information on the MECL and 100K ECL families:

Motorola MECL Device Data Book, Motorola Inc., 1987. Stock code DL122/D.

F100K ECL Data Book, Fairchild Camera and Instrument Corp.

Motorola MECL System Design Handbook, second edition. Motorola Inc., 1983. Stock code HB205R1/D.

Signetics ECL 10K/100K Data Manual.

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High Performance ECL Data
ECLinPS and ECLinPS Lite

This databook contains device specifications for Motorola's ECLinPS advanced ECL logic family.

ECLinPS (ECL in picoseconds) was developed in response to the need for an even higher performance ECL family of standard logic functions, particularly in the Computer, Automated Test, Instrumentation and Communications industries. Family general features as well as specific functions were developed in close consultation with ECL systems design engineers.

ECLinPS offers the user a single gate delay of 500ps max., including package delay, and a flip-flop toggle frequency of 1100MHz.

ECLinPS is compatible with two different ECL standards. Each function is available with either MECL 10H compatibility (MC10Exxx series) or 100K compatibility (MC100Exxx series).

ECLinPS is offered in the 28-lead plastic leaded chip carrier (PLCC), a J-lead surface mount IC package. This package was selected for high performance, reduced parasitics and good thermal handling in a low cost, standard package, and reflects an industry trend towards surface mount assembly.

Printed in U.S A.

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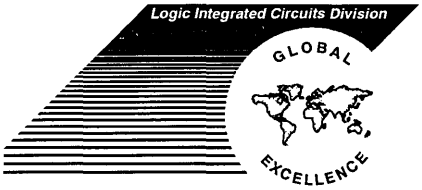

This section contains a numerical listing of LinPS and ECLinPS Lite family functions, a hnical overview of the ECLinPS Lite families as 'l as an outline of their electrical characteristics. addition, this section outlines the procedures l philosophies used to AC test the families. C10E/EL series devices are compatible with MECL 10H family. MC100E/EL series are npatible with 100K ECL.)

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* Available in 10EL version only.
† Available in 100ELT version only.

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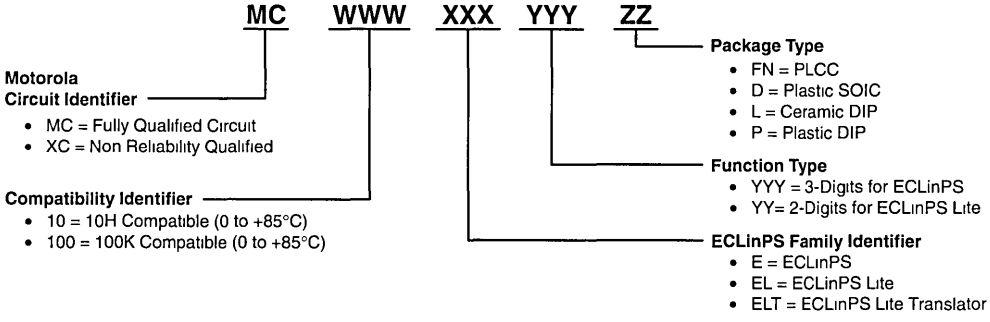
Device Nomenclature

ECLinPS, ECLinPS Lite



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* Available in 10E or 10EL Version Only.

† Available in 100ELT Version Only

SECTION 4
Family Overview

Introduction

Recent advances in bipolar processes have led to a proliferation of very high speed LSI and VLSI gate arrays in high end computer applications. The advent of these high speed arrays has created a need for a high speed logic family to tie or "glue" them together. Because arrays have a finite amount of circuitry and I/O pins, glue functions which are sensitive to either of these parameters may be better performed off of the array. In addition glue functions which require very tight skew control may be difficult to perform on an array due to the inherent skew of the large packages associated with large gate arrays. Therefore although the trend is to push more and more of the logic onto the array, there are design constraints which make performing some of the logic, such as clock distribution, multiplexing, decoding, latching, memory addressing and translating, in glue an attractive alternative.

The high end computer segment is not the only market segment pushing for higher performance logic parts. ATE, instrumentation and communication designs can have data rate requirements ranging from 300MHz to as high as 2.5GHz. Because large high speed arrays do not always lend themselves to passing high frequency signals on and off chip, portions of the designs must be realized with discrete logic. The current bipolar logic families are not capable of operating at these high frequencies.

To answer the call for a very high speed bipolar logic family Motorola has designed and produced the ECLinPS (ECL in Pico Seconds) logic family. The family was designed to meet the most stringent of system requirements in speed, skew and board density as well as maintaining compatibility to existing ECL families.

ECL Design Benefits

The speed benefits of an ECL design over those of alternative logic technologies are well documented, however there are a number of other important features that make ECL an attractive technology for system designs. The ECLinPS logic family, as with other ECL families, affords the following advantages:

Complimentary Outputs

Complimentary outputs are available on many functions with equal propagation delays between the two paths. This alleviates the need for external inverters and saves system power and board space while maintaining exceptional system timing.

Transmission Line Drive Capability

The low output impedance, high input impedance and high current drive capability of ECL makes it an ideal technology for driving transmission lines. Regardless of the technology, as system speeds increase, interconnect becomes more of a transmission line phenomenon. With ECL no special line driving devices are necessary, as all ECL devices are line drivers.

Constant Power Supply Current Drain

Because of the differential amplifier design used for ECL circuits, the current is not switched on and off but rather simply steered between two paths. Thus the current drain of an ECL device is independent of the logic state and the frequency of operation. This current stability greatly simplifies system power supply design.

Input Pulldown Resistors

ECL inputs have 50KΩ – 75KΩ internal pulldown resistors which pull the input to V_{EE} (logic LOW) when left open. This allows unused inputs to be left open and greatly simplifies logic design.

Differential Drive Capability

Because of the presence of high current drive complimentary outputs, ECL circuits are ideally suited for driving twisted pair lines or cables over long distances. With common mode noise rejection of 1V or more, ECL line receivers are less susceptible to common mode noise. In addition, their differential inputs need only a few hundred millivolt voltage differences to correctly interpret the logic.

High Speed Design Philosophy

Today a truly high speed logic family needs more than simply short propagation delays. The minimization of all types of skew, as well as a level of logic density which affords a smaller amount of board space for an equivalent function, are also necessities of a high speed family. The following summary will outline the steps taken by Motorola to achieve these goals in the development of the ECLinPS logic family.

Fast Propagation Delays

The ECLinPS family boasts 500ps maximum packaged gate delays and typical flip-flop toggle frequencies of 1.4GHz. Simple gate functions show typical propagation delays of 360ps at 25mW of power for a speed power

product of only 9pJ. For higher density devices internal gates run at 100ps with 5mW of power for a speed power product of only 0.5pJ.

Internal Differential Interconnect

The propagation delay window size, skew between rising and falling inputs and susceptibility to noise are all phenomenon which are exacerbated by V_{BB} switching reference variation. By extensively using differential interconnects internal to the chip, the ECLinPS family has been able to achieve superior performance in these areas.

Propagation Delay Temperature Insensitivity

The variation of propagation delay through an ECLinPS device across temperature is typically less than 50ps. This stability allows for faster designs due to tighter delay windows across temperature.

Input Impedance and Loading Capacitance

The input structures of the ECLinPS family show a positive real impedance across the applicable input frequency range. This ensures that the system will remain stable and operate as designed over a wide range of input frequencies. The input loading capacitance typically measures only 1.5pF and is virtually independent of input fanout as the device capacitance is less than 5% of the total. Because the propagation delay of a signal down a transmission line is adversely affected by loading capacitance, the overall system speed is enhanced.

Input Buffers

To minimize propagation delays in a system environment, inputs with a large internal fanout are buffered to minimize the loading capacitance on the transmission line.

High Level of Integration

28-pin designs allow for the design of 9-bit functions for implementation in byte plus parity applications. Full byte plus parity implementation reduces total package count and saves expensive board space.

Space Efficient Package

Surface mount PLCC package affords a high level of integration with a minimum amount of required board space. Quad layout of the package equalizes pin lengths thus minimizing the skew between similar internal paths.

Flow Through Pin Assignment

Input and output pins have been laid out in a flow through pattern with the inputs on one side of the package and the outputs on the other. This flow through pattern helps to simplify the PC board layout operation.

Multiple V_{CCO} pins

To minimize the noise generated in simultaneous switching situations, a minimum of three single-ended outputs per V_{CCO} has been employed in the family. Optimum placement of these V_{CCO}s also results in superior output-to-output skew.

Advanced Bipolar Processing

The ECLinPS logic family is fabricated using Motorola's MOSAIC III process, a process which is two generations ahead of the process used in the development of the 10H family. The small geometries and feature sizes of the MOSAIC III process enable the ECLinPS logic family to boast of a nearly three-fold improvement in speed at less than half the power of existing ECL logic families.

The MOSAIC III process is a double polysilicon process which uses a unique self-alignment scheme for device electrode and isolation definition. The process features self aligned submicron emitters as well as polysilicon base, collector and emitter electrodes. In addition, polysilicon resistors, diodes and capacitors are available to minimize the parasitic capacitance of an ECL gate. Figure 1.1 shows a cross section for an NPN device using the MOSAIC III process.

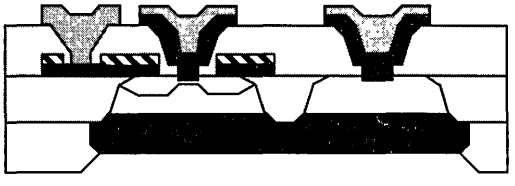


Figure 1.1. MOSAIC III Cross Section

By incorporating the use of polysilicon contacts and resistors through the MOSAIC III process, the parasitic capacitances of an ECLinPS gate are minimized, thus minimizing the time constants which comprise the switching delays of the gate. The resultant gates show delays of 100ps for internal gates and 200ps for output gates capable of driving 50Ω loads. The small geometries of the process, nearly 350% reduction in device area compared to a 10H device, allow these internal gate delays to be achieved at only 800μA of current.

Universal Compatibility

Each member of the ECLinPS family is available in both of the existing ECL standards: 10E series devices are compatible with the MECL 10H family; 100E series devices are compatible with ECL 100K. In addition, to maintain compatibility with temperature-compensated, three-level series-gated gate arrays, the 100E devices are guaranteed to operate without degradation to a V_{EE} of – 5.46V.

The section below presents a comparison between the two standards in the new context of the ECLinPS family.

The user is also referred to the Electrical Characteristics section of this book as well as appropriate family data books and other literature for descriptive information on the earlier ECL families.

Because no supplier previous to Motorola has offered both ECL standards on an identical process, comparison of existing 10H and 100K style devices has some limitations. Comparison of the two standards fabricated with two different processes has sometimes led to the erroneous conclusion that there are inherent AC performance differences between them. In reality this is not the case. The only inherent difference between the two standards is the difference in the behavior of the DC characteristics with temperature.

AC Performance

From an IC design standpoint the only differences between a 10E device and a 100E device in the ECLinPS family is a small temperature compensation network in the 100E output gate, and very minimal differences in the two bias generator networks. Therefore one would expect that from an AC stand-point the performance of the two standards in the ECLinPS family should be nearly identical; measurements prove this to be the case. There is no significant measurable difference in the rise/fall times, propagation delays or toggle frequencies when comparing a 10E and 100E device. The minor difference between previous 10H and 100K designs is due to the fact that the two are fabricated on different processes, and in some cases are designed for operation at different power levels.

Summary

Summarizing the above information, in general, the two ECL design standards, although differing somewhat in DC parameters, are nearly identical when one compares the AC performance for a given device. There may be very small differences in the AC measurements due to the slightly smaller output swing of the 100E device. However, these differences are negligible when compared to the absolute value of the measurements. Therefore, from an AC stand-point, there is no real advantage in using one standard over the other, thus removing AC performance as a decision variable in high-speed system design.

Packaging

During the definition phase of the ECLinPS family, much attention was placed on the identification of a suitable package for the family. The package had to meet the criteria of minimum parasitics and propagation delays along with an attractive I/O vs board space relationship. Although the DIP package offered a level of familiarity and convenience, the performance of the package with a very high speed logic family was inadequate. In addition to the obvious parasitics and board space problems, the propagation delays through the DIP package were nearly twice as long as the delay through the silicon.

The 28-pin PLCC package emerged as the clear favorite both internally and with the high speed market in general. The package offers a quad layout to minimize both lead lengths and lead length differences. As a result, the parasitics and delays of the package are very well suited for a high speed logic family. In addition, the nearly matched lead lengths allow for tighter skew among similar paths through the chip.

The board density potential of the PLCC is also attractive in that it allows for a nearly 100% reduction in board space when compared to the DIP alternative. The package is approximately a half inch square with 50 mil spaced J-bend leads. More detailed measurements can be found in the package section of this data book. The J-bend leads provide a smaller footprint than a gull wing package and propose fewer temperature expansion coefficient mismatch problems than the leadless alternative.

Thermally, the standard PLCC exhibits a Θ_{JA} of 43.5°C per watt at 500lfpm air flow. With this thermal resistance most 28-pin functions can be implemented with the MOSAIC III process without encountering any severe thermal problems. For more details on thermal issues of the ECLinPS family refer to the thermal section of this data book.

Abbreviation Definitions

The following is a list of abbreviations found in this data book and a brief definition of each.

Current

I_{CC}	Total power supply current drawn from the positive supply by an ECLinPS unit under test.
I_{EE}	Total power supply current drawn from an ECLinPS device under test by the negative supply.
I_{IL}	Current drawn by the input of an ECLinPS device with a specified low level (V_{IL} min) forced on the input.
I_{INH}	Current drawn by the input of an ECLinPS device with a specified high level (V_{IH} max) forced on the input.
I_{OUT}	The current sourced by an output under specified load conditions.

Voltage

V_{BB}	The switching reference voltage.
V_{BE}	Base-to-emitter voltage drop of a transistor at specified collector and base currents.
V_{CB}	Collector-to-base voltage drop of a transistor at specified collector and base currents.

Family Overview

V_{CC} The most positive supply voltage to an ECLinPS device.

V_{CCO} Power supply connection to the output emitter follower of an ECLinPS gate. For the ECLinPS logic family V_{CC} and V_{CCO} are common nodes.

V_{EE} The most negative supply voltage to an ECLinPS device.

V_{IH} Nominal input logic HIGH voltage level.

V_{IH} max Maximum (most positive) logic HIGH voltage level for which all parametric specifications hold.

V_{IH} min Minimum (least positive) logic HIGH voltage level for which all parametric specifications hold.

V_{IL} Nominal input logic LOW voltage.

V_{IL} max Maximum (most positive) logic LOW voltage level for which all parametric specifications hold.

V_{IL} min Minimum (least positive) logic HIGH voltage level for which all parametric specifications hold.

V_{OH} Output logic HIGH voltage level for the specified load condition.

V_{OHA} Output logic HIGH voltage level with the inputs biased at V_{IH} min or V_{OL} max.

V_{OH} max Maximum (most positive) logic HIGH output voltage level.

V_{OH} min Minimum (least positive) logic HIGH output voltage level.

V_{OL} Output logic LOW voltage level for the specified load condition.

V_{OLA} Output logic LOW voltage level with the inputs biased at V_{IH} min or V_{OL} max.

V_{OL} max Maximum (most positive) logic LOW output voltage level.

V_{OL} min Minimum (least positive) logic LOW output voltage level.

V_{TT} Output termination voltage for ECLinPS open emitter follower outputs.

V_{PP} Minimum peak-to-peak input voltage for differential input devices.

V_{CMR} The voltage range in which the logic HIGH voltage level of a differential input signal must fall for a differential input device.

V_{CUT} The logic LOW voltage level for ECL BUS outputs which attain cutoff of the output emitter follower.

V_{SUP} The maximum voltage difference between V_{EE} and V_{CC} for the E1651 comparator.

Timing Parameters

t_R Waveform rise time of an output signal measured from the 20% to 80% levels of the signal.

t_F Waveform fall time of an output signal measured from the 20% to 80% levels of the signal.

$T_{PD\pm\pm}$ Propagation delay of a signal measured for a rising/falling input to a rising/falling output.

xpt The crossing point of a differential input or output signal. The reference point for which differential delays are measured.

T_{PLH} The propagation delay for an output transitioning from a logic LOW level to a logic HIGH level.

T_{PHL} The propagation delay for an output transitioning from a logic HIGH level to a logic LOW level.

f_{MAX} Maximum input frequency for which an ECLinPS flip flop will function correctly.

f_{COUNT} Maximum input frequency for which an ECLinPS counter will function properly.

f_{SHIFT} Maximum input frequency for which an ECLinPS shift register will function properly.

t_{SKEW} The maximum delay difference between similar paths on a single ECLinPS device.

t_S Setup time: the minimum amount of time an input must transition before a clock transition to ensure proper function of the device.

t_H Hold time: the minimum amount of time an input must remain asserted after a clock transition to ensure proper operation of the device.

t_{RR} Release time or Reset Recovery Time: the minimum amount of time after a signal is de-asserted that a different input must wait before assertion to ensure proper functionality of the device.

t_W min Minimum pulse width of a signal necessary to ensure proper functionality of a device.

Temperature

T_{STG}	The maximum temperature at which a device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit package.
Θ_{JA}	Thermal resistance of an integrated circuit package between the junction and the ambient.
Θ_{JC}	Thermal resistance of an integrated circuit package between the junction and the case.
Θ_{CA}	Thermal resistance of an integrated circuit package between the case and the ambient.
lfpm	Linear feet per minute.

Miscellaneous

DUT	Device under test.
C_{IN}	Input capacitance of a device.
Z_{IN}	Input impedance of a device.
C_{OUT}	Output capacitance of a device.
Z_{OUT}	Output impedance of a device.
P_D	The total dc power applied to a device, not including any power delivered from the device to the load.
R_L	Load resistance.
R_T	Transmission line termination resistor.
R_P	An input pull-down resistor.
PUT	Pin under test.
SMA	Industry standard PCB connector.

SECTION 5
Electrical Characteristics

DC Characteristics

ECLinPS Transfer Curves

As mentioned in the previous section, except for the E1651, E1652 and E197 all ECLinPS devices are offered in either 10E or 100E versions to be compatible with 10H or 100K ECL logic respectively. The following information will overview the DC characteristics of the two versions of ECLinPS devices, for more detailed discussions the reader is referred to the MECL and F100K data books.

Both 10E and 100E devices produce ≈ 800mV output swings into a specified 50Ω to – 2.0V load. However, because of the low output impedance (Figure 2.1) of both standards, neither is limited to 50Ω loads. Larger load resistances can be used to reduce the system power without sacrificing the speed of the device. Of course the overall system speed will be reduced due to the increased delays of the interconnect traces. In addition, to better drive high capacitive lines, smaller resistances, down to 25Ω, can be used without violating the 50mA max output current specification. It is however recommended that for lines of less than 35Ω, specialized 25Ω driver circuits or "ganged" output schemes should be used to ensure optimum long term reliability of the device.

The 10E devices are voltage compensated but not temperature compensated, therefore, although the output voltage levels are insensitive to variations in V_{EE}, they do vary with temperature. The transfer curves in Figure 2.2 pictorially illustrate the behavior of the 10E outputs. In order to maintain noise margins over temperature, it is important that the V_{BB} switching reference tracks with temperature in such a way as to remain centered between the V_{OH} and V_{OL} levels. As shown in Table 2.1, the temperature tracking rates of the V_{OH} and V_{OL} for a 10E device are not equal. Therefore, it is necessary to design the V_{BB} reference such that it tracks at a rate equal to the average rate of the difference between the

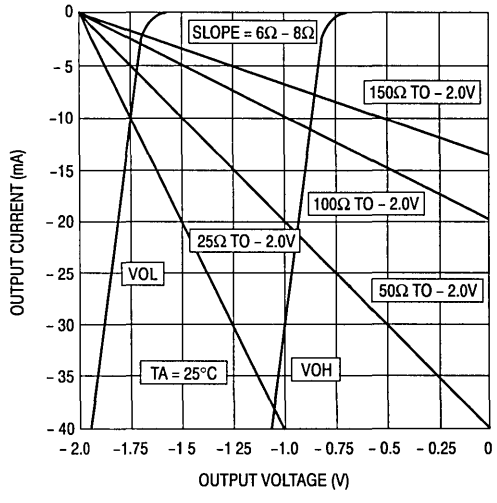


Figure 2.1. Output Characteristics vs Load

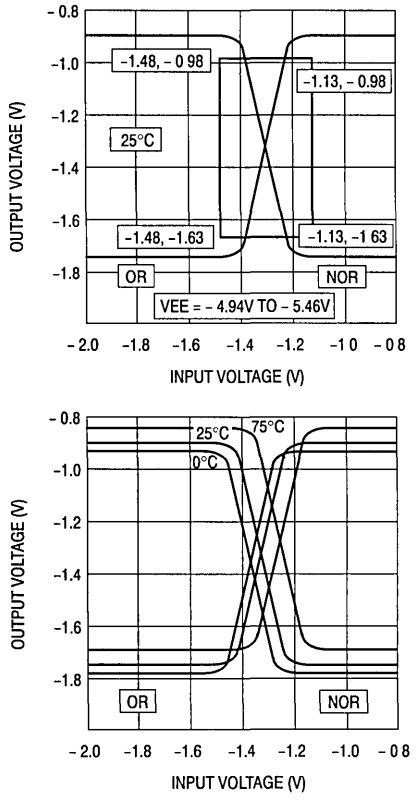


Figure 2.2. ECLinPS 10E Transfer Curves

high and low output level tracking rates. Table 2.1 also outlines the temperature tracking behavior of a 10E V_{BB} switching reference.

10E	min	typ	max
$\Delta V_{OH}/\Delta T$ (mV/°C)	1.1	1.2	1.4
$\Delta V_{OL}/\Delta T$ (mV/°C)	0	0.4	0.6
$\Delta V_{BB}/\Delta T$ (mV/°C)	0.6	0.8	1.0
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	0	5	20
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	0	10	30
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	0	5	20
100E	**min**	**typ**	**max**
$\Delta V_{OH}/\Delta T$ (mV/°C)	– 0.15	0	0.15
$\Delta V_{OL}/\Delta T$ (mV/°C)	– 0.30	0	0.30
$\Delta V_{BB}/\Delta T$ (mV/°C)	– 0.20	0	0.20
$\Delta V_{OH}/\Delta V_{EE}$ (mV/V)	0	5	20
$\Delta V_{OL}/\Delta V_{EE}$ (mV/V)	0	10	30
$\Delta V_{BB}/\Delta V_{EE}$ (mV/V)	0	5	20

Table 2.1. ECLinPS Voltage Level Tracking Rates

The 100E devices, on the other hand, are temperature and voltage compensated, therefore, the output levels remain fairly constant over variations in both V_{EE} and temperature. Figure 2.3 shows the transfer characteristics for a 100E device. The associated tracking rates are illustrated in Table 2.1. Notice that in this case the V_{BB} switching reference is designed to remain constant over temperature to maintain an optimum position within the output swing of the device. This flat temperature tracking of the internal reference levels leads to a phenomena particular to the 100E devices.

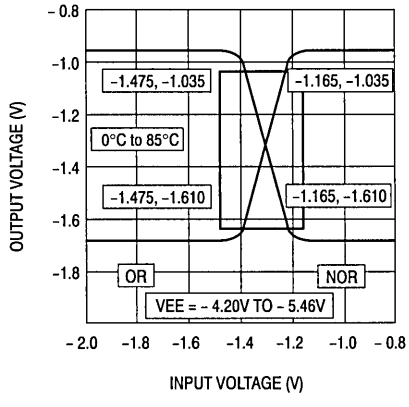


Figure 2.3. ECLinPS 100E Transfer Characteristics

Since the V_{BE}s of the current source transistor reduce with temperature, if the current source reference remains constant, as is the case for 100E devices, the I_{EE} of the device will vary with temperature. Careful scrutiny of the data sheets will reveal that the worst case I_{EE} for a function is higher for the 100E version than the 10E version of that device. As a result, from a power standpoint a 100E device operating at 85°C with a – 4.5V V_{EE} will be nearly identical to a 10E device operating with a – 5.2V V_{EE} under identical temperature conditions.

Although differing somewhat in many DC parameters, 10E and 100E devices do share a couple of the same DC characteristics. Both designs show superior I_{EE} vs V_{EE} tracking rates due to the design of the voltage regulator. With a tracking rate of <3%/V, this variation can effectively be ignored during system design. The output level and reference level variation with V_{EE} are also outstanding as can be seen in Table 2.1.

Noise Margin

The noise margin of a device is a measure of a device's resistance to undesirable switching. For ECLinPS, as well as all ECL devices, noise margin is a DC specification. The noise margin is defined as the difference between the voltage level of an output of the sending device and the required voltage level of the input of the receiving device. Therefore a worst case noise margin can be calculated from the ECLinPS data sheets by simply subtracting the V_{IL} max or V_{IH} min from the V_{OL} min or V_{OH} max respectively. Table 2.2 below illustrates the worst case and typical noise margins for both 10E and 100E ECLinPS devices. Notice that the typical noise margins are approximately 100mV larger than the worst case.

	10E		100E	
	min	typ	min	typ
NM_{HIGH} (mV)	150	240	140	210
NM_{LOW} (mV)	150	280	145	230

Table 2.2. DC Noise Margins

As mentioned above, the noise margins of a device are a DC measurement and thus can lead to some false impressions of the noise immunity of a system. For instance, from the chart the worst case noise margin is 140mV for a high level of a 100E device. This would suggest that an undershoot on this line of greater than 140mV could cause an error in the system. This however is not necessarily the case as the determination as to whether or not an AC noise signal is propagated is dependent on line impedances, output impedances and propagation delays as well as noise margins.

Electrical Characteristics

AC Characteristics

Parameter Definitions

The device data sheets in Section 3 contain specifications for the propagation delays and rise/fall times for each of the devices in the ECLinPS family. In addition, where applicable, skew, setup/hold, maximum toggle frequencies (f_{MAX}), reset recovery and minimum pulse width specifications are included. The waveforms and terminologies used in describing the propagation delays and rise/fall times of the ECLinPS family are depicted in Figure 2.4 below.

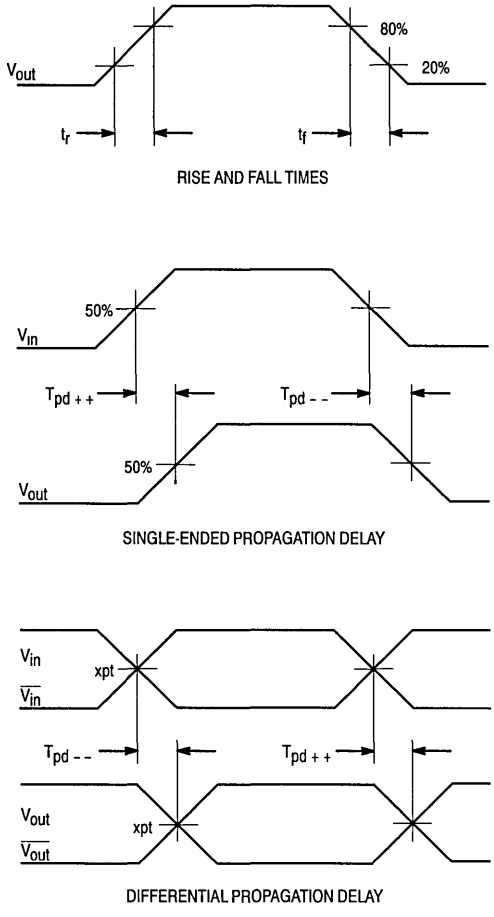


Figure 2.4. ECLinPS T_{PD} Measurement Waveforms

Propagation delays and rise/fall times are generally well understood parameters, however, there is sometimes confusion surrounding the definitions of more specialized AC parameters such as skew, setup/hold times, release times, and maximum frequency. The following few paragraphs will outline the ways in which Motorola defines these parameters.

Skew Times

In the design of high speed systems skew plays nearly as important a role as propagation delay. The majority of the devices in the ECLinPS family have the skew between outputs specified. This skew specification represents the typical difference between the delays of similar paths on a single chip. No maximum value for skew is specified due to the difficulty in the production testing of this parameter. The user is encouraged to contact an ECLinPS application engineer to obtain actual evaluation data if this parameter is critical in their designs.

Set-Up and Hold Times

Motorola defines the setup time of a device as the minimum time, prior to the transition of the clock, that an input must be stable to ensure that the device operates properly. The hold time, on the other hand, is defined as the minimum time that an input must remain stable after the transition of the clock to ensure that the device operates properly. Figure 2.5 illustrates the way in which Motorola defines setup and hold times.

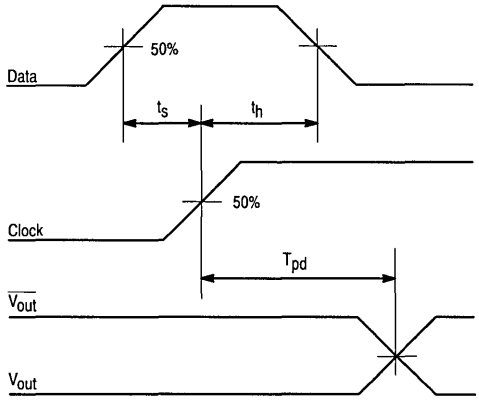


Figure 2.5. Set-Up and Hold Waveforms

Release Times

Release times are defined as the minimum amount of time an input must wait to be clocked after an enable, master reset or set signal is deactivated to ensure proper operation. Because more times than not this specification is in reference to a master reset operation, this parameter is often called reset recovery time. Figure 2.6 illustrates the definition of release time in the Motorola data sheets.

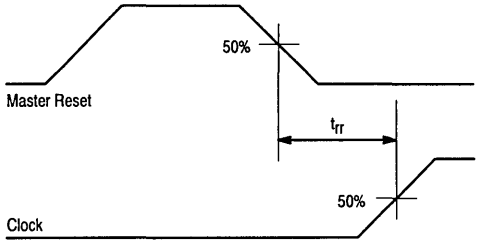


Figure 2.6. ECLinPS Release Time Waveforms

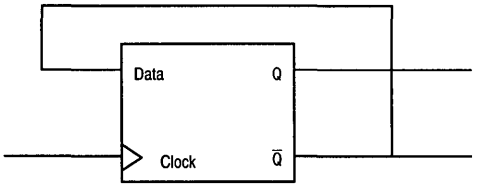


Figure 2.7. f_{MAX} Measurement

f_{MAX} Measurement

In general f_{MAX} is measured in the manner shown in Figure 2.7 with the fail criterion being either a swing of 600mV or less, or a miscount. However, in some cases, the feedback method of testing can lead to a pessimistic value of f_{MAX} because the feedback path delay is such that the setup times of the device are violated. If this is the case, it is necessary to have two free running signal generators to ensure that the setup times are observed. This parameter, along with f_{SHIFT} and f_{COUNT}, represents the maximum frequency at which a particular flip flop, shift register or counter can be clocked with the divide, shift or count operation guaranteed. This number is generated from worst case operating conditions, thus, under nominal operating conditions, the maximum toggle frequency is higher.

AC Testing ECLinPS Devices

The introduction of the ECLinPS family raised the performance of silicon to a new domain. As the propagation delays of logic devices become ever faster the task of correlating between test setups becomes increasingly challenging. To obtain test results which correlate with Motorola, various testing techniques must be adhered to. A typical schematic for an ECLinPS test setup is illustrated in Figure 2.8.

A solid ground plane is a must in the test setup, as the two power supplies are bypassed to this ground plane. A 20µF capacitor from the two power supplies to ground is used to dampen any supply variations. An RF quality 0.01µF capacitor from each power pin to ground is used to decouple the fixture. These 0.01µF capacitors should be located as close to the power pins of the package as possible. In addition, in order to minimize the inductance of the power pins, all of the power leads should be kept as short as possible. The power supplies are shifted by +2.0V so that the load comprises only the precision 50Ω input impedance of the oscilloscope. Use of this technique will assure that the customer and Motorola are terminating devices into equivalent loads and will improve test correlation.

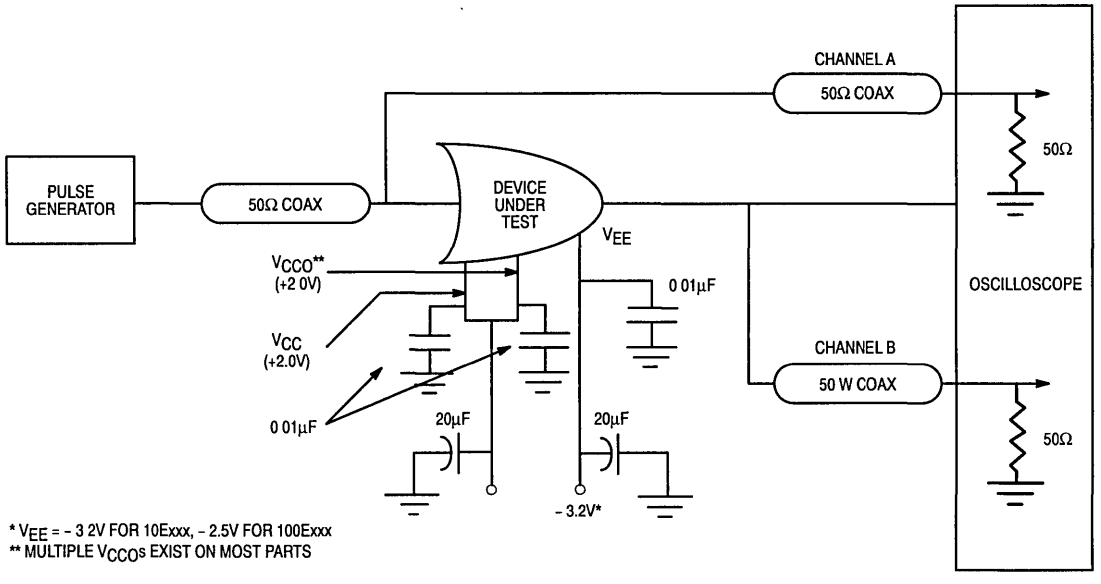


Figure 2.8. Typical ECLinPS Test Setup

To further standardize testing, any unused outputs should be loaded with 50Ω to ground.

Because the power supplies are shifted, the input levels must also be shifted by an equal amount. Table 2.3 gives the typical input levels for the ECLinPS family and their corresponding +2.0V shifted levels.

10Exxx	Typical	Shifted
V_{IL}	–1.75V	+ 0.25V
V_{IH}	– 0.90V	+1.10V
100Exxx	**Typical**	**Shifted**
V_{IL}	–1.70V	+ 0.30V
V_{IH}	– 0.95V	+1.05V

Table 2.3. ECL Levels after Translating by +2.0V

The test fixture should be in a controlled impedance 50Ω environment, with any non-50Ω interconnects, or stubs, kept as short as possible (<1/4″). This controlled impedance environment will help to minimize overshoot and ringing, two phenomena which can lead to inaccuracies in AC measurements. To minimize degradation of the input and output edge rates, a 50Ω coaxial cable with a teflon dielectric is recommended, however any other cable with a bandwidth of >5.0GHz is adequate. In addition, the cables from the device under test (DUT) to the inputs of the scope should be matched in length to prevent any errors due to different path lengths from the DUT to the scope. The interconnect fittings should be 50Ω SMA straight or SMA launchers to minimize impedance mismatches at the interface of the coax and test PC board. Although a teflon laminate board is preferable, an FR4 laminate board is acceptable as long as the signal traces are kept to five inches or less. Longer traces will result in significant edge rate degradation of the input and output signals.

To make the board useful for incoming inspection or other volume testing, the board needs to be fitted with a socket. Although not suitable for AC testing due to different pin lengths and large parasitics, there are through hole sockets which are adequate for DC testing of ECLinPS devices. For AC testing purposes a 28-pin PLCC surface mount socket is recommended.

To ease the correlation issue, Motorola has developed a universal AC test board which is now available to customers. The board is fitted with a PLCC socket and comes with instructions on how it can be configured for the different device types in the family. For ordering information see the description on the following page.

Finally, to ensure correlation between Motorola and the customer, high-performance, state-of-the-art measuring equipment should be used. The pulse generator must be capable of producing the required input levels with rise and fall times of 500ps. In addition, if f_{MAX} is going to be tested, a frequency of up to 1.5GHz may be needed. The oscilloscope should also be of the utmost in performance with a minimum bandwidth of 5.0 GHz.

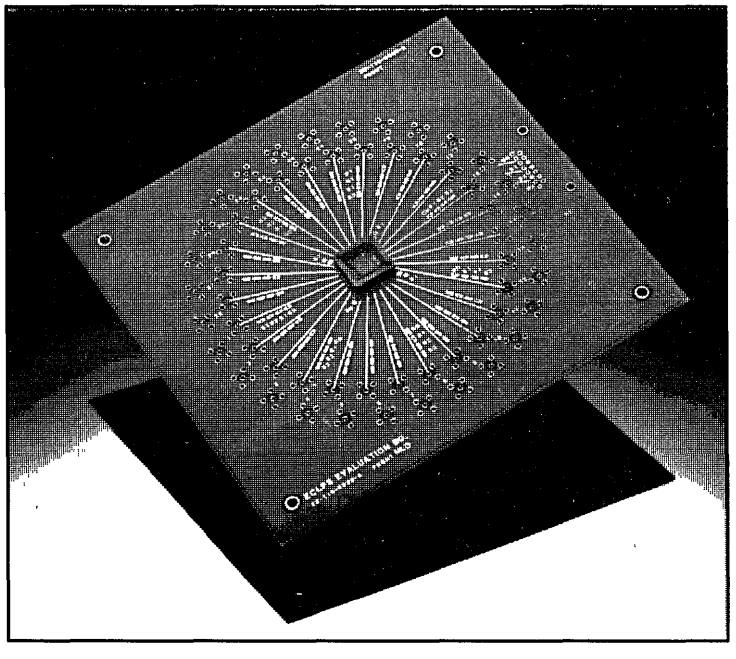


Figure 2.9. ECLinPS AC Test Board

SECTION 6
Engineering Evaluation Board for 28-Pin ECL Devices in the PLCC Package

Part # ECLPSBD28

DESCRIPTION

This board is designed to provide a low cost characterization tool for evaluating ECL devices in the ECLinPS Product Family. The board provides a high bandwidth 50Ω controlled impedance environment. The board is universal and can be configured by the user for any of the 28-pin PLCC devices in the family depending on the input, output, and power pinout layout of the device. The table below indicates common input/output/power devices.

Group	Base Device	Pin Compatible Devices
CONF1	E196	E195
CONF2	E142	E016,E141,E143,E241
CONF3	E337	E336
CONF4	E212	E104,E107,E150,E151
CONF5	E156	E155,E167,E171,E256
CONF6	E158	E116,E122,E175,E416
CONF7	E154	E452
CONF8	E101	E131,E157,E404
CONF9	E112	
CONF10	E431	E457
CONF11	E111	
CONF12	E164	E160
CONF13	E451	
CONF14	E163	E166
CONF15	E193	

Table 1. Cross Reference of Board Configurations

The board is designed to test devices using the fly-by (Kelvin contact) test method, therefore one input force trace and one input sense trace exist for each input pin. This allows termination of the input and output signals into the highly accurate 50 ohm impedance of an oscilloscope. The layout is engineered to have equal length traces from the device under test (DUT) socket to the sense outputs which simplifies the calibration requirements for accurate AC measurements.

The kit provides a printed circuit board with an attached surface mount socket as well as assembly instructions. For superior impedance control from the cable to the board, Motorola recommends the use of SMA coaxial connectors.

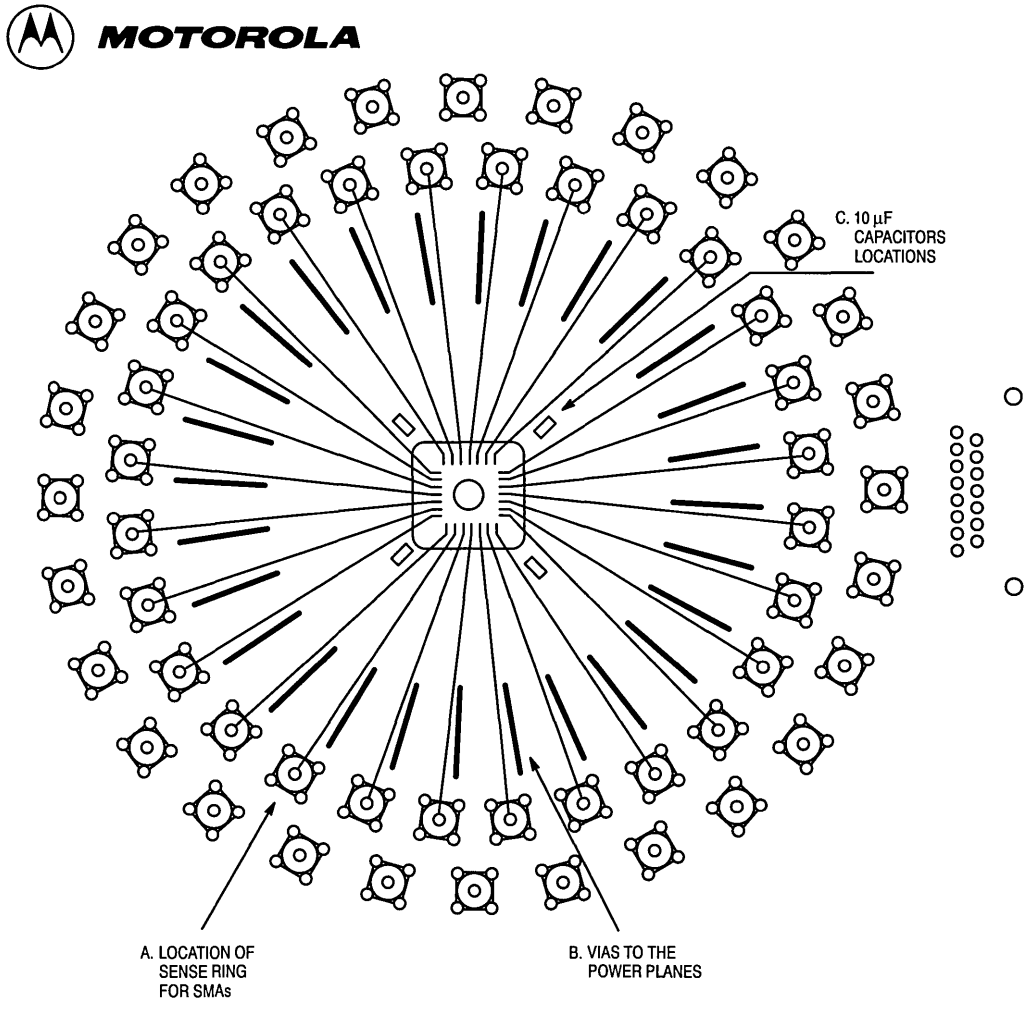


Figure 1. Front View of ECLinPS Evaluation Board

Table 2. Pin Cross Reference

Group	Part(s)	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14
CONF1	E196	V_{EE}	I	I	VB	NC	NC	I	I	I	O	O	V_{CC}	O	O
CONF2	E142	V_{EE}	I	I	I	I	I	I	V_{CC}	O	O	O	O	O	V_{CC}
CONF3	E337	V_{EE}	I	I	I	I	I	I	V_{CC}	I	NC	O	NC	I	V_{CC}
CONF4	E212	V_{EE}	I	I	I	I	V_{CC}	O	O	O	O	V_{CC}	O	O	O
CONF5	E156	V_{EE}	I	I	I	I	I	I	I	I	V_{CC}	O	O	V_{CC}	O
CONF6	E158	V_{EE}	I/VB	I	I	I	I	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	O
CONF7	E154	V_{EE}	I/VB	I	I	I	I	I	I	V_{CC}	O	O	O	O	O
CONF8	E101	V_{EE}	I	I	I	I	I	I	I	I	I	V_{CC}	O	O	O
CONF9	E112	V_{EE}	I	I	I	NC	V_{CC}	O	O	O	O	V_{CC}	O	O	O
CONF10	E431	V_{EE}	I/VB	I	I	I	I	I	I/VB	I	I	V_{CC}	O	O	O
CONF11	E111	V_{CC}	I	VB	NC	O	O	O	V_{CC}	O	O	O	O	O	O
CONF12	E164	V_{EE}	I	I	I	I	I	I	I	I	I	I	I	V_{CC}	O
CONF13	E451	V_{EE}	I	NC	I	I	I	I	I	I	V_{CC}	O	O	O	V_{CC}
CONF14	E163	V_{EE}	I	I	I	I	I	I	I	I	I	I	O	O	V_{CC}
CONF15	E193	V_{EE}	I	I	I	I	I	I	I	V_{CC}	O	O	O	O	V_{CC}

Table 2. Pin Cross Reference (continued)

Part(s) (cont'd)	P15	P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	# of Connec-tors
E196	V_{CC}	V_{CC}	NC	I	NC	I	I	I	I	I	I	I	I	I	35
E142	O	V_{CC}	O	O	O	V_{CC}	I	I	I	I	I	I	I	I	37
E337	O	V_{CC}	I	NC	O	V_{CC}	I	I	I	I	I	I	I	I	37
E212	O	V_{CC}	O	O	O	O	V_{CC}	O	I	I	I	I	I	I	33
E156	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	40
E158	O	V_{CC}	O	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	32
E154	O	V_{CC}	O	O	O	O	V_{CC}	I	I	I	I	I	I	I	38
E101	O	V_{CC}	O	O	O	O	V_{CC}	I	I	I	I	I	I	I	40
E112	O	V_{CC}	O	O	O	O	V_{CC}	O	O	O	O	V_{CC}	I	I	26
E431	O	V_{CC}	O	O	I	I	I	I/VB	I	I	I/VB	I	I	I	44
E111	V_{CC}	O	O	O	O	O	O	V_{CC}	O	O	O	V_{EE}	I	I	25
E164	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	44
E451	O	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	VB	I	37
E163	NC	V_{CC}	O	O	V_{CC}	I	I	I	I	I	I	I	I	I	42
E193	O	V_{CC}	O	O	O	V_{CC}	I	I	I	I	I	I	I	I	38

KEY:
- I designates an input
- O designates an output
- V_{EE} designates the lower voltage rail
- V_{CC} designates the upper voltage rail
- NC designates a no connect
- VB designates V_{BB} output which should not be terminated into 50 ohms

Egineering Evaluation Board

ASSEMBLING THE ECLinPS EVALUATION BOARD

The evaluation board is designed for characterizing devices in a laboratory environment using high bandwidth sampling oscilloscopes such as the Hewlett Packard 54120T, the Tektronix 11800 Series, or the Tektronix 7854. The board is designed using Kelvin contact (fly-by) techniques to present the input signals to the DUT. Each pin on the board has two traces, one force and one sense. Input pins use one force and one sense line, while outputs need only a sense line. This means that input signals are terminated through the sense line into the 50 ohm input of a sampling oscilloscope instead of at the input to the DUT. Please refer to the AC Testing section of the ECLinPS Data Book for further information and a simplified figure of the test setup.

The first step in building a board is determining which input/output/power configuration is necessary for the device of interest. Table 1 on the first page of the Applications Information shows all the board configurations. For example, if the devices of interest were the E104 and the E151, then CONF2 would be selected. Table 2 is a pin cross reference for each configuration.

1

I. Installing the SMA Connectors

Table 2 indicates the number of SMA connectors needed to populate an evaluation board for a given configuration. Depending on the device and the parameters of interest, it may not be necessary to install the full complement of SMA connectors. For example, some devices have two clock inputs or common clocks and individual clocks. Figure 1 is the frontview of the ECLinPS evaluation board. Item A points to the inner ring which connects to the sense traces of the DUT. The outer ring connects to the force traces. An input requires one SMA connector for the force and one SMA connector for the sense, while an output only requires a connection to the sense trace. Insert all the SMA connectors into the board and solder to the board. A simple assembly technique is to place a stiff piece of cardboard (8″×7″ or larger) on top of all the connectors and hold the board and cardboard together. Invert the board, place on a level surface, and all the connectors will be seated properly and can be soldered in place.

II. Connecting Power Planes to DUT Socket

There are four voltage planes on the ECLPSBD28. One is dedicated to ground and the other three, B1, B2, B3, are uncommitted. These planes are accessible through a power connection and sets of four vias that are adjacent to each sense trace. This is identified as Item B in Figure 1. For standard parts, B1 can be assigned V_{CC}, B2 can be assigned to V_{EE}, and B3 can be assigned to ground. Table 2 indicates which pins need to be connected to the various supply voltages. On the front side of the board, solder a jumper wire from the closest V_{EE} or V_{CC} via to the sense trace for each V_{CC}, V_{CCO}, and V_{EE} pin. Near the DUT there are sets of ground/bias plane vias that accommodate power supply decoupling capacitors. These are identified as Item C. On the front side of the board install 10 μF capacitors and on the back side install a 0.01 μF high frequency capacitor in parallel to decouple the V_{EE} and V_{CC} planes.

III. Cutting Force Traces for Outputs

Because of the design of the board, all force traces for output pins will appear as transmission line stubs connected to the output pin. On the back side of the board, cut the force traces associated with the outputs using a razor blade knife. It is important to cut the trace very close to the DUT area to minimize the stub length. Also cut the force traces that are connected to V_{CC}, V_{CCO}, and V_{EE} pins.

IV. Installing the Chip Capacitors for the V_{CC}/V_{CCO} Pins

In the kit are 0.01 μF chip capacitors for use in decoupling the V_{CC} and V_{CCO} pins to the ground plane. This is critical because the power pins are not directly connected to the V_{CC} plane as in an actual board layout. On the back side of the board beneath the DUT socket are pads for each pin which allow connection of chip capacitors to the center island (GND) for each V_{CC} and V_{CCO} pin. Stand the chip capacitors on edge when soldering them in place so that adjacent pins are not shorted together.

V. Final Assembly

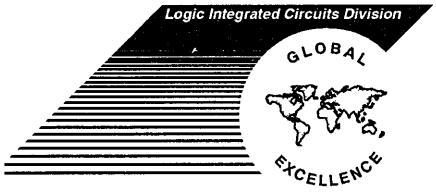
The board power plane interface is designed to accommodate a 15-pin right angle D connector. This can be used directly, or wires can be inserted into the vias to connect to the power planes that were connected to the DUT in part II. Attach standoffs into the four 0.25 inch holes at the corners of the board. This completes the assembly of the evaluation board and it should be ready to test.

VI. SMA Connector Suppliers

Below are two suppliers who manufacture PC Mount SMA connectors which interface to the evaluation board. Motorola has used these two connectors before, but there are other vendors who manufacture similar products.

EF Johnson 299 Johnson Ave. P.O. Box 1249 Waseca, Minnesota 56093 (800) 247-8343 or (507) 835-6222	0.200″ PC Mount SMA Jack Receptacle 142-0701-201
MACOM Omni Spectra 140 Fourth Avenue Waltham, Massachusetts 02254 (617) 890-4750	0.200″ PC Mount SMA Straight Jack 2062-0000-00

ligh Performance ECL Data
CLinPS and ECLinPS Lite



This section contains AC & DC specifications r each ECLinPS device type. Specifications ›mmon to all device types can be found in the ·st part of this section. While specifications ıique to a particular device can be found in the dividual data sheets following the family ›ecifications.

ECLinPS Family Specifications & Device Data Sheets

2

ata Sheet Classification

dvance Information — product in the sampling or pre-production stage at the time of publication.

roduct Preview — product in the design stage at the time of publication.

ECLinPS Family Specifications

Absolute Maximum Ratings

Beyond which device life maybe impaired.[1]

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	– 8 to 0	Vdc
Input Voltage (V_{CC} = 0V)	V_I	0 to – 6V	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range 10E Series 100E Series	T_A	 0 to + 85 0 to + 85	°C
Operating Range[2]	V_{EE}	– 5.7 to – 4.2	V

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at: 100E series: – 4 2V to – 5.46V
   10E series: – 4.94V to – 5.46V

10E Series DC Characteristics

V_{EE} = – 5.2V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Characteristic	0°C		25°C		75°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	–1020	– 840	– 980	– 810	– 920	–735	– 910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1630	–1950	–1630	–1950	–1600	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	– 840	–1130	– 810	–1070	–735	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1480	–1950	–1480	–1950	–1450	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5		0.5		0.3		0.3		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0 volts, except bus outputs which, where specified, are terminated into 25Ω.

100E Series DC Characteristics

V_{EE} = – 4.2V to – 5.46V; V_{CC} = V_{CCO} = GND; T_A = 0°C to + 85°C

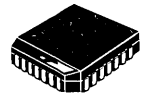
Symbol	Characteristic	Min	Typ	Max	Unit	Conditions	
V_{OH}	Output HIGH Voltage	–1025	– 955	– 880	mV	V_{IN} = V_{IH}(max)	Loading with 50Ω to – 2.0V
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV	or V_{IL}(min)	
V_{OHA}	Output HIGH Voltage	–1035			mV	V_{IN} = V_{IH}(min)	
V_{OLA}	Output LOW Voltage			–1610	mV	or V_{IL}(max)	
V_{IH}	Input HIGH Voltage	–1165		– 880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810		–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			µA	V_{IN} = V_{IL}(min)	

This table replaces the three tables at different supply voltages in the previous edition and in ECL 100K literature. The same DC parametric values at V_{EE} = – 4.5V now apply across the full V_{EE} range of – 4.2 to – 5.46V.

8-Bit Synchronous Binary Up Counter

MC10E016
MC100E016

8-BIT SYNCHRONOUS BINARY UP COUNTER



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

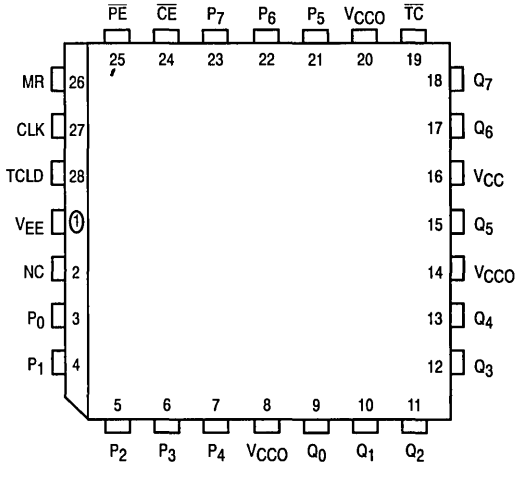
2

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10H family, extended to 8-bits, as shown in the logic symbol.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter. The Q_n outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

- 700MHz Min. Count Frequency
- 1000ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

FUNCTION TABLE

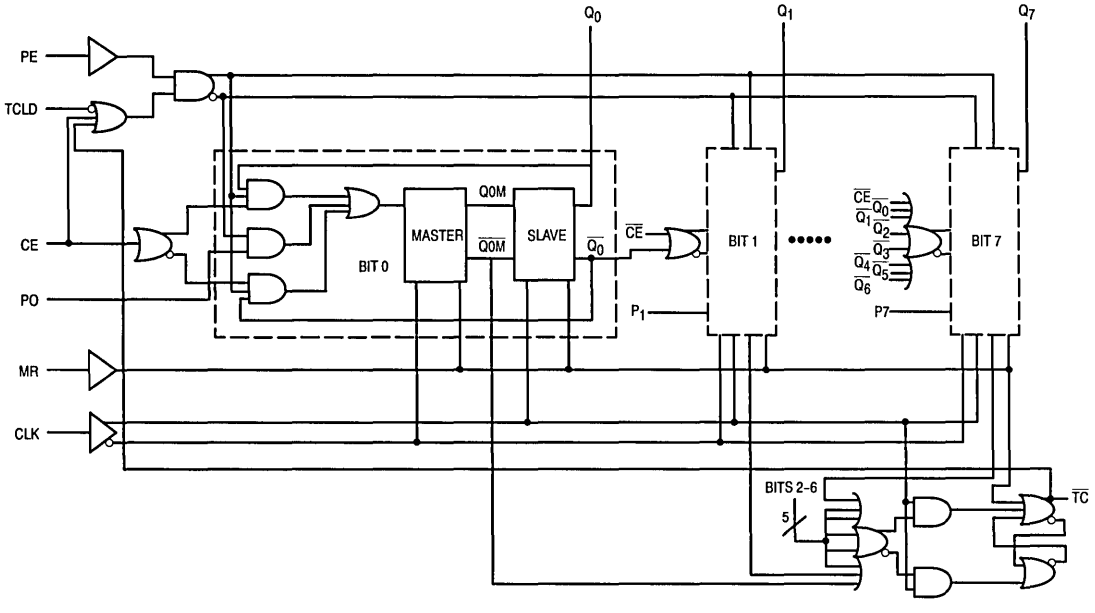
CE	PE	TCLD	MR	CLK	Function
X	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Q_n : = LOW, $\overline{TC}$: = HIGH)

Z = clock pulse (low to high);
ZZ = clock pulse (high to low)

PIN NAMES

Pin	Function
$P0 - P_7$	Parallel Data (Preset) Inputs
$Q_0 - Q_7$	Data Outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC-Load Control Input

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		151	181		151	181		151	181		
	100E		151	181		151	181		174	208		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
f_{COUNT}	Max. Count Frequency	700	900		700	900		700	900		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	CLK to Q	600	725	1000	600	725	1000	600	725	1000		
	MR to Q	600	775	1000	600	775	1000	600	775	1000		
	CLK to $\overline{TC}$	550	775	900	550	775	900	550	775	1050		
	MR to $\overline{TC}$	625	775	1000	625	775	1000	625	775	1000		
t_s	Setup Time										ps	
	Pn	150	– 30		150	– 30		150	– 30			
	$\overline{CE}$	600	400		600	400		600	400			
	$\overline{PE}$	600	400		600	400		600	400			
	TCLD	500	300		500	300		500	300			
t_h	Hold Time											
	Pn	350	100		350	100		350	100			
	$\overline{CE}$	0	– 400		0	– 400		0	– 400			
	$\overline{PE}$	0	– 400		0	– 400		0	– 400			
	TCLD	100	– 300		100	– 300		100	– 300			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	510	800	300	510	800	300	510			

2

FUNCTION TABLE

Function	PE	CE	MR	TCLD	CLK	P7-P4	P3	P2	P1	P0	Q7-Q4	Q3	Q2	Q1	Q0	TC
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

Applications Information

Cascading Multiple E016 Devices

2

For applications which call for larger than 8-bit counters multiple E016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of E016 devices. Two E016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 1 below pictorially illustrates the cascading of 4 E016s to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an E016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary setup time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 1 shows EL01 gates used to control the count enable inputs, however, if the frequency of operation is lower a slower, ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is 500MHz and that for a 16-bit counter is 625MHz.

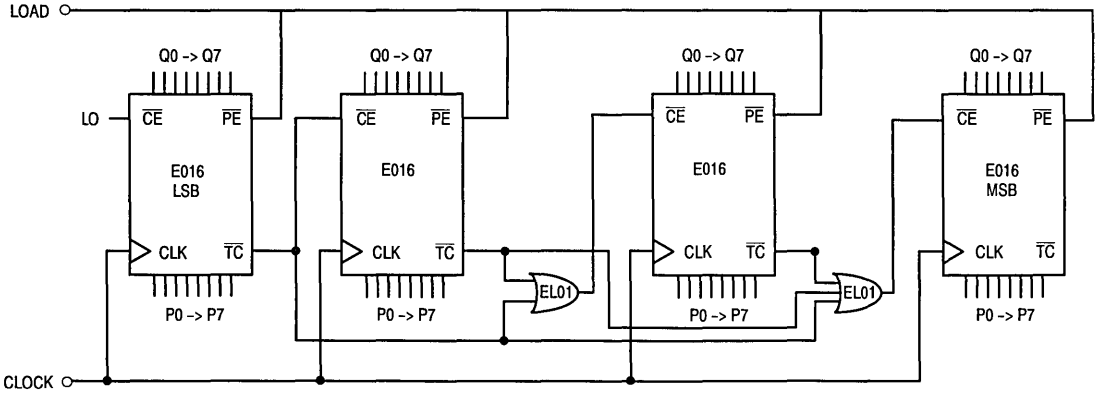


Figure 1. 32-Bit Cascaded E016 Counter

Applications Information (continued)

Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 2 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

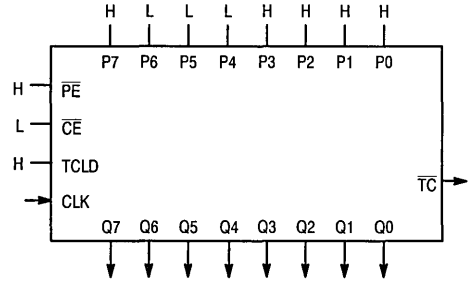


Figure 2. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = 256 – 113 = $8F_{16}$ = 1000 1111

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 2 will result in the waveforms of Figure 3. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the E016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 1. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single E016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple E016 divider chains.

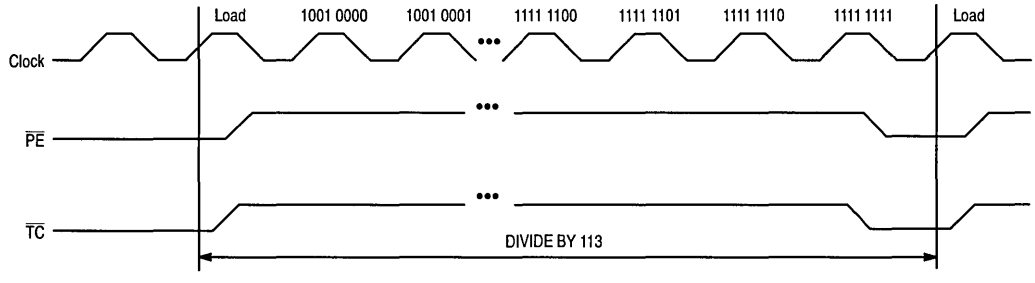


Figure 3. Divide by 113 E016 Programmable Divider Waveforms

Applications Information (continued)

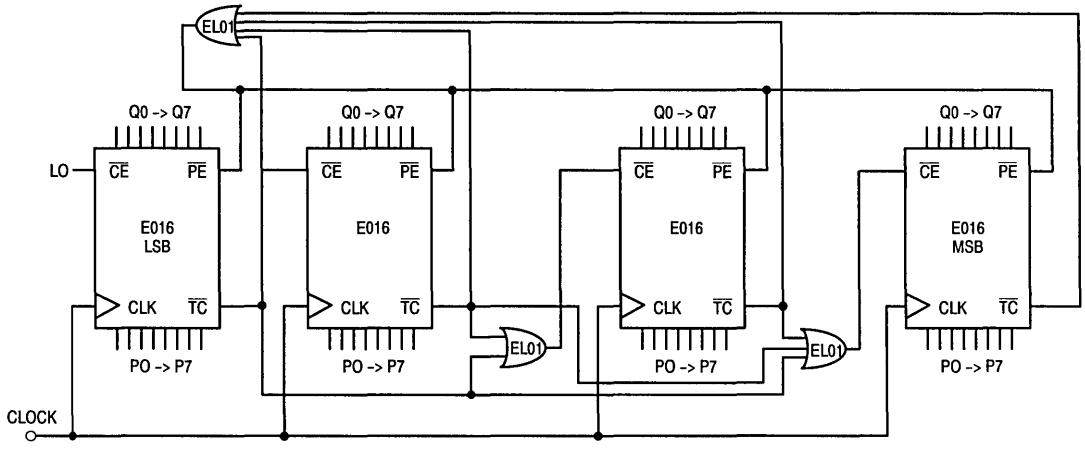


Figure 4. 32-Bit Cascaded E016 Programmable Divider

2

Figure 4 on the following page shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EL01 OR gates were used. For lower frequency applications a slower OR gate could replace the EL01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant E016 must also feed the $\overline{CE}$ input of the most significant E016. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Maximizing E016 Count Frequency

The E016 device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

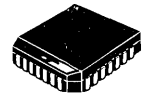
Quad 4-Input OR/NOR Gate

MC10E101
MC100E101

The MC10E/100E101 is a quad 4-input OR/NOR gate.

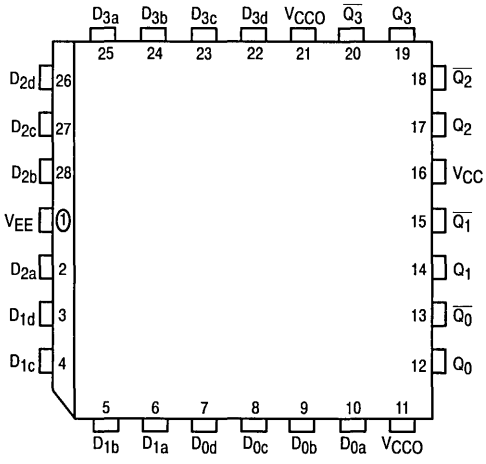
- 500ps Max. Propagation Delay
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

QUAD 4-INPUT OR/NOR GATE



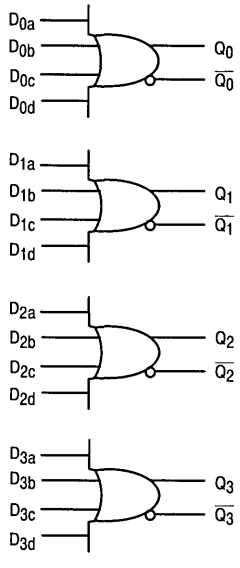
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_{0a} - D_{3d}$	Data Inputs
$Q_0 - Q3$	True Outputs
$\overline{Q_0} - \overline{Q_3}$	Inverting Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		30	36		30	36		30	36		
	100E		30	36		30	36		35	42		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	200	350	500	200	350	500	200	350	500	ps	
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_{SKEW}	Within-Gate Skew		25			25			25			2
t_r t_f	Rise/Fall Time 20 - 80%	300	380	575	300	380	575	300	380	575	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.

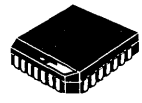
Quint 2-Input AND/NAND Gate

MC10E104
MC100E104

The MC10E/100E104 is a quint 2-input AND/NAND gate. The function output F is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

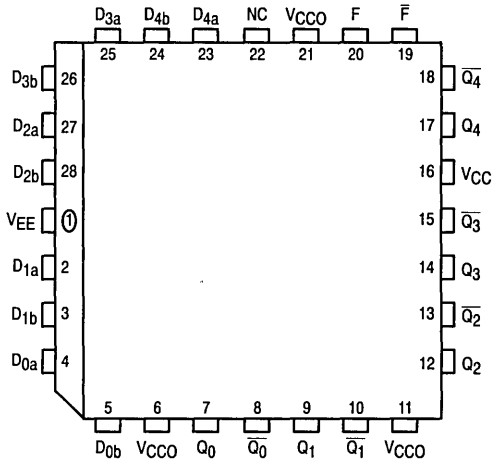
- 600ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

QUINT 2-INPUT AND/NAND GATE



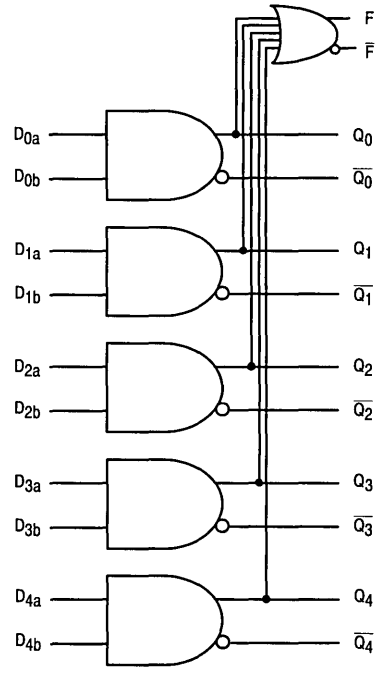
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_{0a} - D_{4b}$	Data Inputs
$Q_0 - Q_4$	AND Outputs
$\overline{Q_0} - \overline{Q_4}$	NAND Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$F = (D_{0a} \bullet D_{0b}) + (D_{1a} \bullet D_{1b}) + (D_{2a} \bullet D_{2b}) + (D_{3a} \bullet D_{3b}) + (D_{4a} \bullet D_{4b})$

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		38	46		38	46		38	46		
	100E		38	46		38	46		44	53		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to Q	225	385	600	225	385	600	225	385	600		
	D to F	500	725	1000	500	725	1000	500	725	1000		
t_{SKEW}	Within-Device Skew										ps	
	D to Q		75			75			75			1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%											
	Q	275	425	700	275	425	700	275	425	700		
	F	300	475	700	300	475	700	300	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device.

Quint 2-Input XOR/XNOR Gate

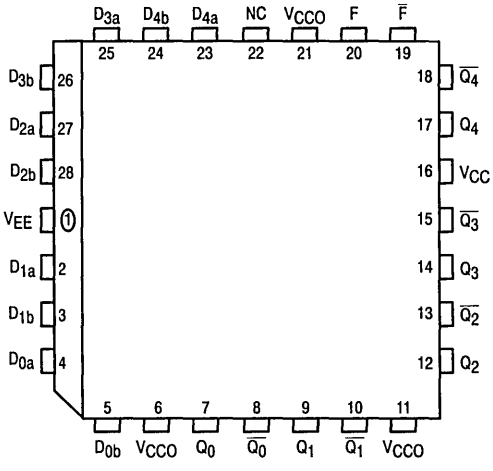
MC10E107
MC100E107

The MC10E/100E107 is a quint 2-input XOR/XNOR gate. The function output F is the OR of all five XOR outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

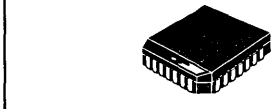
- 600ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

QUINT 2-INPUT
XOR/XNOR GATE

Pinout: 28-Lead PLCC (Top View)

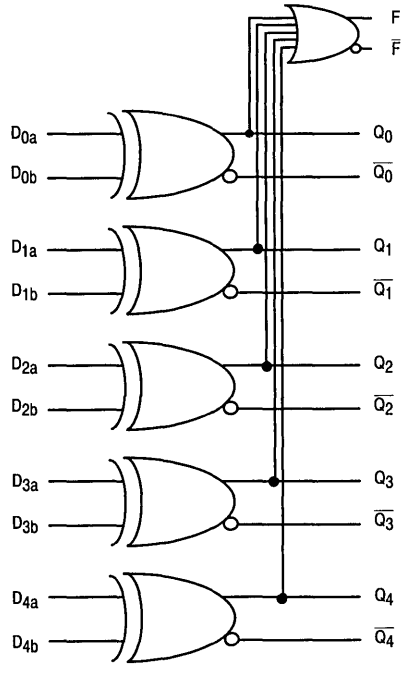


* All V_{CC} and V_{CCO} pins are tied together on the die.



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_{0a} - D_{4b}$	Data Inputs
$Q_0 - Q_4$	XOR Outputs
$\overline{Q_0} - \overline{Q_4}$	XNOR Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \oplus D_{0b}) + (D_{1a} \oplus D_{1b})\,(D_{2a} \oplus D_{2b}) + (D_{3a} \oplus D_{3b}) + (D_{4a} \oplus D_{4b})$$

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		42	50		42	50		42	50		
	100E		42	50		42	50		48	58		

AC CHARACTERISTICS (V_{EE} =V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to Q	250	410	600	250	410	600	250	410	600		
	D to F	500	725	1000	500	725	100	500	725	1000		
t_{SKEW}	Within-Device Skew										ps	
	D to Q		75			75			75			1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%											
	Q	275	450	700	275	450	700	275	450	700		
	F	300	475	700	300	475	700	300	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device.

1:9 Differential Clock Driver

MC10E111
MC100E111

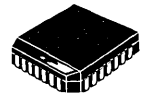
1:9 DIFFERENTIAL CLOCK DRIVER

The MC10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

- Low Skew
- Guarateed Skew Spec
- Differential Design
- V_{BB} Output
- Enable
- Extended 100E V_{EE} Range of –4.2 to –5.46V
- 75kΩ Input Pulldown Resistors

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.



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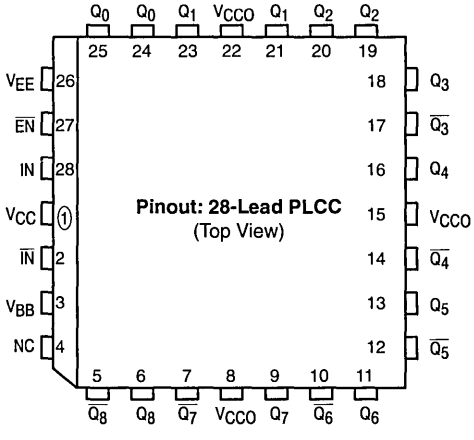
CASE 776-02

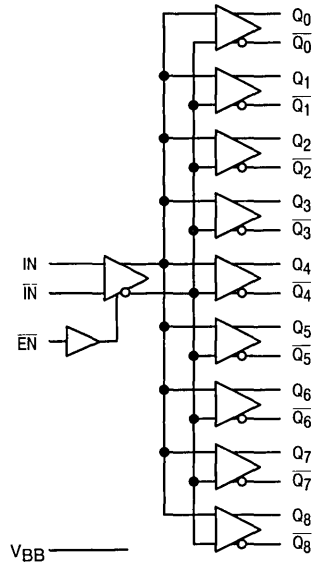
PIN NAMES

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
$\overline{EN}$	Enable
Q_0, $\overline{Q_0}$–Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Output



Pinout: 28-Lead PLCC
(Top View)

LOGIC SYMBOL



DC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage 10E	−1.43		−1.30	−1.38		−1.27	−1.35		−1.25	−1.31		−1.19	V	
	100E	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	−1 38		−1.26		
I_{IH}	Input HIGH Current			150			150			150			150	µA	
I_{EE}	Power Supply Current 10E		48	60		48	60		48	60		48	60	mA	
	100E		48	60		48	60		48	60		55	69		
$V_{PP(DC)}$	Input Sensitivity	50			50			50			50			mV	1
V_{CMR}	Commom Mode Range	−1.6		−0.4	−1.6		−0 4	−1.6		−0 4	−1.6		−0.4	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP(min)}$.

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (Diff)	380		680	460		560	480		580	510		610	ps	1
	IN (SE)	280		780	410		610	430		630	460		660		2
	Enable	400		900	450		850	450		850	450		850		3
	Disable	400		900	450		850	450		850	450		850		3
t_S	Setup Time $\overline{EN}$ to IN	250	0		200	0		200	0		200	0		ps	5
t_H	Hold Time IN to $\overline{EN}$	50	−200		0	−200		0	−200		0	−200		ps	6
t_R	Release Time $\overline{EN}$ to IN	350	100		300	100		300	100		300	100		ps	7
t_{skew}	Within-Device Skew		25	75		25	50		25	50		25	50	ps	4
$V_{PP(AC)}$	Minimum Input Swing	250			250			250			250			mV	8
t_r, t_f	Rise/Fall Time	250	450	650	275	375	600	275	375	600	275	375	600	ps	

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. (See *Definitions and Testing of ECLinPS AC Parameters* in this publication.)
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. (See *Definitions and Testing of ECLinPS AC Parameters* in this publication.)
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on $\overline{EN}$ to the 50% point of a **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from the 50% point of a **positive** transition on $\overline{EN}$ to the 50% point of a **negative** transition on Q (or a positive transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. $V_{PP(min)}$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay The $V_{PP(min)}$ is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.

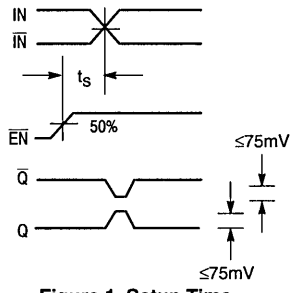


Figure 1. Setup Time

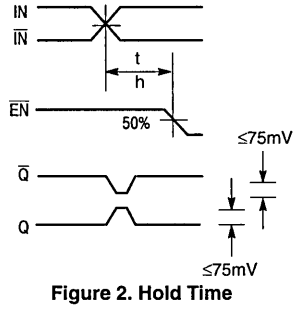


Figure 2. Hold Time

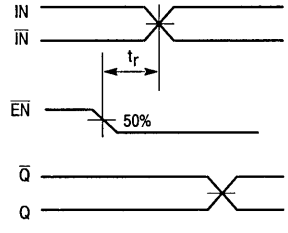


Figure 3. Release Time

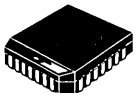
Quad Driver

MC10E112
MC100E112

QUAD DRIVER

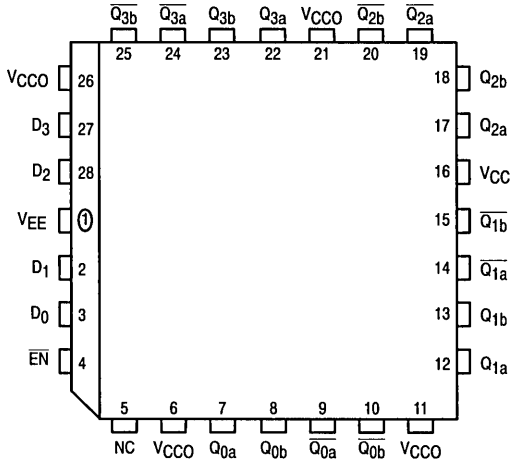
The MC10E/100E112 is a quad driver with two pairs of OR/NOR outputs from each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the MC10E/100E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the E212 device.

- 600ps Max. Propagation Delay
- Common Enable Input
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



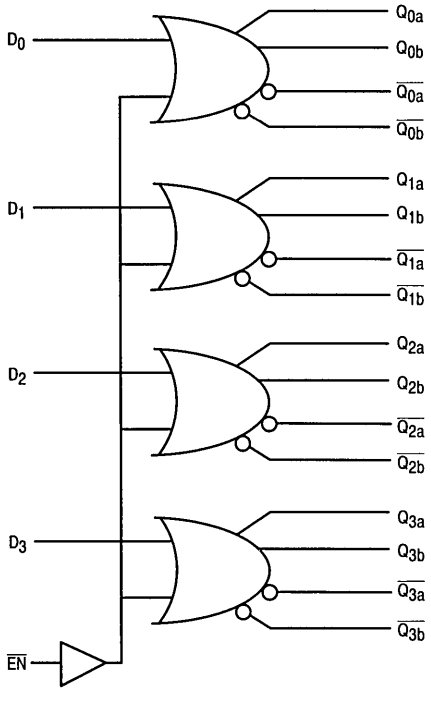
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_3$	Data Inputs
$\overline{EN}$	Enable Input
Q_{na}, Q_{nb}	True Outputs
$\overline{Q_{na}}$, $\overline{Q_{nb}}$	Inverting Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current										μA	
	D			200			200			200		
	$\overline{EN}$			200			200			200		
I_{EE}	Power Supply Current										mA	
	10E		47	56		47	56		47	56		
	100E		47	56		47	56		54	65		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	200	400	600	200	400	600	200	400	600		
	$\overline{EN}$	275	450	675	275	450	675	275	450	675		
t_{SKEW}	Within-Device Skew										ps	
	Dn to Qn, $\overline{Qn}$		80			80			80			1
	Qna to Qnb		40			40			40			2
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	425	700	275	425	700	275	425	700		

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

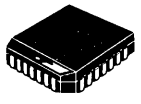
Quint Differential Line Receiver

MC10E116
MC100E116

QUINT DIFFERENTIAL LINE RECEIVER

The MC10E/100E116 is a quint differential line receiver with emitter-follower outputs. An internally generated reference supply (V_{BB}) is available for single-ended reception.

- 500ps Max. Propagation Delay
- V_{BB} Supply Output
- Dedicated V_{CCO} Pin for Each Receiver
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Active current sources plus a deep collector feature of the MOSAIC III process provide the receivers with excellent common-mode noise rejection. Each receiver has a dedicated V_{CCO} supply lead, providing optimum symmetry and stability.

The receiver design features clamp circuitry to cause a defined state if both the inverting and non-inverting inputs are left open; in this case the Q output goes LOW, while the $\overline{Q}$ output goes HIGH. This feature makes the device ideal for twisted pair applications.

If both inverting and non-inverting inputs are at an equal potential of > –2.5V, the receiver does *not* go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW, or the device may even oscillate.

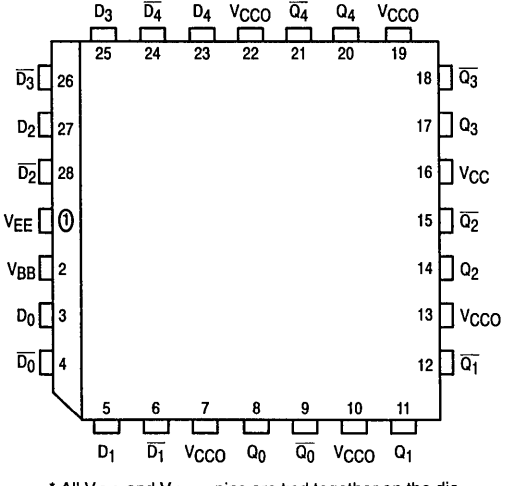
The device V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01μF capacitor. Please refer to the interface section of the design guide for information on using the E116 in specialized applications.

The E116 features input pull-down resistors, as does the rest of the ECLinPS family. For applications which require bandwidths greater than that of the E116, the E416 device may be of interest.

PIN NAMES

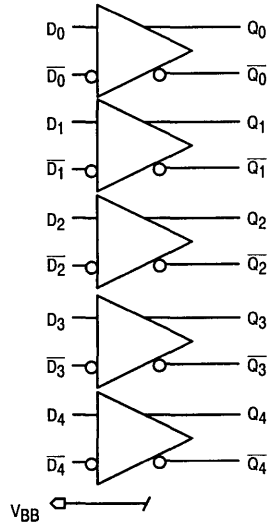
Pin	Function
D_0, $\overline{D_0}$ – D_4, $\overline{D_4}$	Differential Input Pairs
Q_0, $\overline{Q_0}$ – Q_4, $\overline{Q_4}$	Differential Output Pairs
V_{BB}	Reference Voltage Output.

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage 10E	−1.43		−1.30	−1.38		−1.27	−1.35		−1 25	−1.31		−1.19	V	
	100E	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26		
I_{IH}	Input HIGH Current			200			200			200			200	µA	
I_{EE}	Power Supply Current 10E		29	35		29	35		29	35		29	35	mA	
	100E		29	35		29	35		29	35		29	40		
V_{PP}(DC)	Input Sensitivity	150			150			150			150			mV	1
V_{CMR}	Commom Mode Range	−2.0		−0.6	−2.0		−0.6	−2.0		−0.6	−2.0		−0 6	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			0°C to 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D (Differential)	150	300	500	200	300	450	ps	
	D (Single-Ended)	150	300	550	150	300	500		
t_{skew}	Within-Device Skew		50			50		ps	1
t_{skew}	Duty Cycle Skew $t_{PLH} - t_{PHL}$		±10			±10		ps	2
V_{PP}(AC)	Minimum Input Swing	150			150			mV	3
t_r/t_f	Rise/Fall Time	250	375	625	275	375	575	ps	20–80%

1. Within-device skew is defined as identical transitions on similar paths through a device
2. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed.

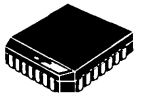
9-Bit Buffer

MC10E122
MC100E122

9-BIT BUFFER

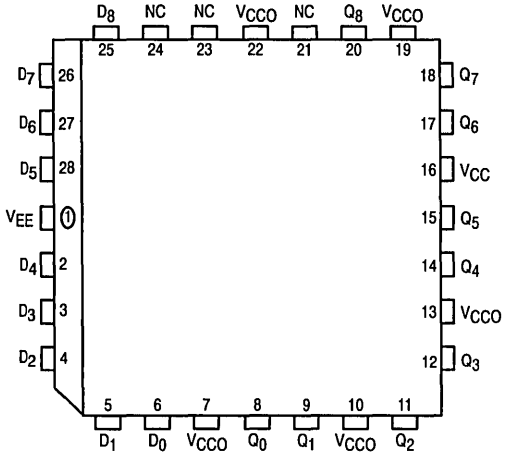
The MC10E/100E122 is a 9-bit buffer. The device contains nine non-inverting buffer gates.

- 500ps Max. Propagation Delay
- Extended 100E V_{EE} Range of – 4.2V to – 5.46 V
- 75kΩ Input Pulldown Resistors



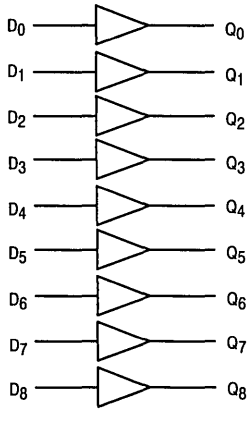
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_8$	Data Inputs
$Q_0 - Q_8$	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			200			200			200	µA	
I_{EE}	Power Supply Current										mA	
	10E		41	49		41	49		41	49		
	100E		41	49		41	49		47	57		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	150	350	500	150	350	500	150	350	500	ps	
t_{SKEW}	Within-Device Skew D to Q		75			75			75		ps	1
t_r t_f	Rise/Fall Times 20 - 80%	300	425	800	300	425	800	300	425	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

2

4-Bit D Flip-Flop

MC10E131
MC100E131

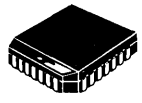
4-BIT
D FLIP-FLOP

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

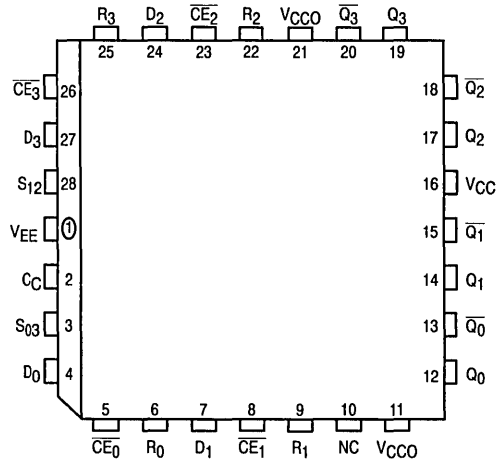
Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

- 1100MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)

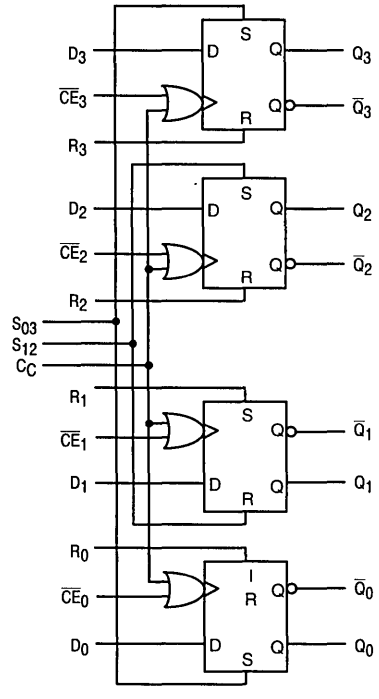


* All V_{CC} and V_{CCO} pins are tied together on the die.

PIN NAMES

Pin	Function
$D_0 - D_3$	Data Inputs
$\overline{CE}_0 - \overline{CE}_3$	Clock Enables (Individual)
$R_0 - R_3$	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (paired)
$Q_0 - Q_3$	True Outputs
$\overline{Q}_0 - \overline{Q}_3$	Inverting Outputs

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit	Cond
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current	C_C			350			350			350			350	µA	
		S			450			450			450			450		
		R, $\overline{CE}$			300			300			300			300		
		D			150			150			150			150		
I_{IEE}	Power Supply Current	10E		58	70		58	70		58	70		58	70	mA	
		100E		58	70		58	70		58	70		67	81		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

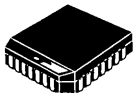
Symbol	Characteristic		–40°C			0°C to 85°C			Unit	Condition
			Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency		1000	1400		1100	1400		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output	$\overline{CE}$	310	600	750	360	500	700	ps	
		C_C	275	600	725	325	500	675		
		R	300	625	775	350	550	725		
		S	300	550	775	350	550	725		
t_S	Setup Time	D	200	20		150	20		ps	1
t_H	Hold Time	D	225	–20		175	–20		ps	1
t_{RR}	Reset Recovery Time		450	150		400	150		ps	
t_{PW}	Minimum Pulse Width	CLK	400			400			ps	
		R, S	400			400				
t_{SKEW}	Within-Device Skew			60			60		ps	2
t_r/t_f	Rise/Fall Time		275	460	725	300	480	675	ps	20–80%

1. Setup/hold times guaranteed for both C_C and $\overline{CE}$.
2. Within-device skew is defined as identical transitions on similar paths through a device.

6-Bit Universal Up/Down Counter

MC10E136
MC100E136

6-BIT UNIVERSAL UP/DOWN COUNTER



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. The device generates a look-ahead-carry output and accepts a look-ahead-carry input. These two features allow for the cacading of multiple E136's for wider bit width counters that operate at very nearly the same frequency as the stand alone counter.

- 550 MHz Count Frequency
- Fully Synchronous Up and Down Counting
- Internal 75 kΩ Input Pulldown Resistors
- Look-Ahead-Carry Input and Output
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of –4.2 V to –5.46 V

2

The $\overline{CLOUT}$ output will pulse LOW for one clock cycle one count before the E136 reaches terminal count. The $\overline{COUT}$ output will pulse LOW for one clock cycle when the counter reaches terminal count. For more information on utilizing the look-ahead-carry features of the device please refer to the applications section of this data sheet. The differential COUT output facilitates the E136's use in programmable divider and self-stopping counter applications.

Unlike the H136 and other similar universal counter designs the E136 carry out and look-ahead-carry out signals are registered on chip. This design alleviates the glitch problem seen on many counters where the carry out signals are merely gated. Because of this architecture there are some minor functional differences between the E136 and H136 counters. The user, regardless of familiarity with the H136, should read this data sheet carefully. Note specifically (see logic diagram) the operation of the carry out outputs and the look-ahead-carry in input when utilizing the master reset.

When left open all of the input pins will be pulled LOW via an input pulldown resistor. The master reset is an asynchronous signal which when asserted will force the Q outputs LOW.

The Q outputs need not be terminated for the E136 to function properly, in fact if these outputs will not be used in a system it is recommended to save power and minimize noise that they be left open. This practice will minimize switching noise which can reduce the maximum count frequency of the device or significantly reduce margins against other noise in the system.

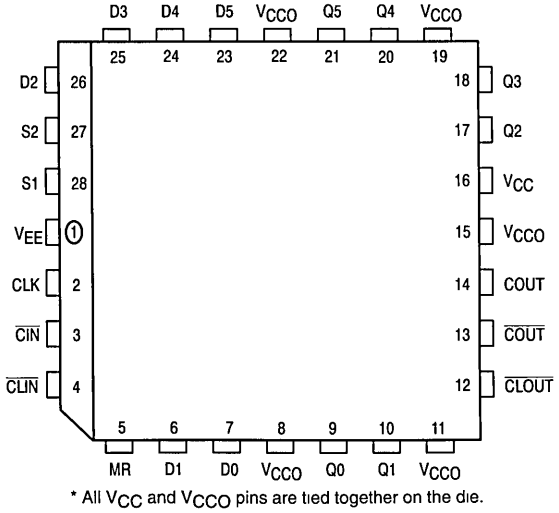
PIN NAMES

Pin	Function
$D_0 - D_5$	Preset Data Inputs
$Q_0 - Q_5$	Data Inputs
S1, S2	Mode Control Pins
MR	Master Reset
CLK	Clock Input
$\overline{COUT}$, COUT	Carry-Out Output (Active LOW)
$\overline{CLOUT}$	Look-Ahead-Carry Out (Active LOW)
$\overline{CIN}$	Carry-In Input (Active LOW)
$\overline{CLIN}$	Look-Ahead-Carry In Input (Active LOW)

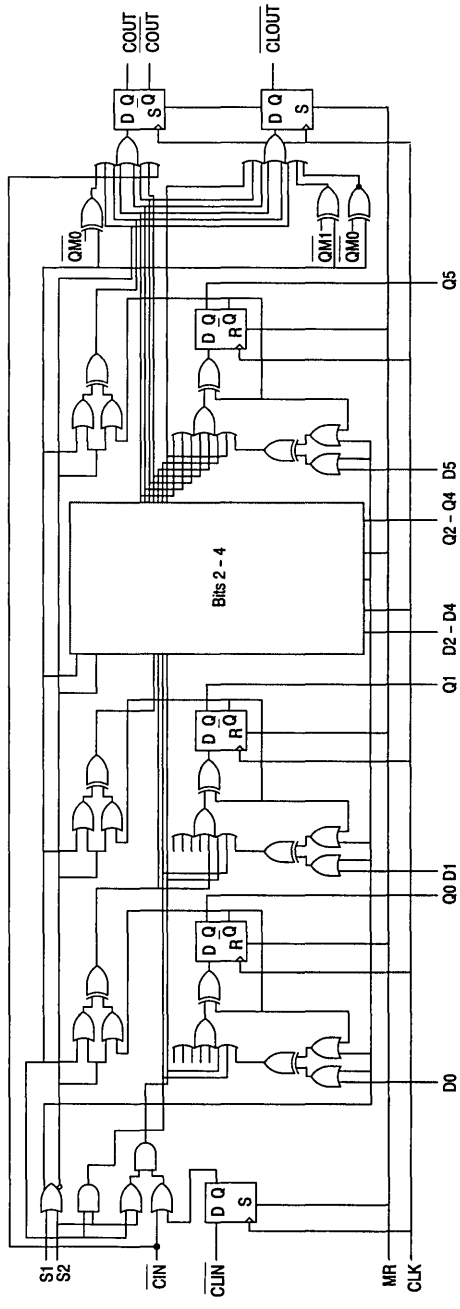
FUNCTION TABLE (Expanded truth table on page 2-29)

S1	S2	CIN	MR	CLK	Function
L	L	X	L	Z	Preset Parallel Data
L	H	L	L	Z	Increment (Count Up)
L	H	H	L	Z	Hold Count
H	L	L	L	Z	Decrement (Count Down)
H	L	H	L	Z	Hold Count
H	H	X	L	Z	Hold Count
X	X	X	H	X	Reset (Qn = LOW)

Pinout: 28-lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

E136 Universal Up/Down Counter Logic Diagram

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input HIGH Current	I_{IH}	—	—	150	—	—	150	—	—	150	µA	
Power Supply Current	I_{EE}										mA	
10E		—	125	150	—	125	150	—	125	150		
100E		—	125	150	—	125	150	—	140	170		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Count Frequency	f_{COUNT}	550	650	—	550	650	—	550	650	—	MHz	
Propagation Delay to Output	t_{PLH}										ps	
CLK to Q	t_{PHL}	850	1150	1450	850	1150	1450	850	1150	1450		
MR to Q		850	1150	1450	850	1150	1450	850	1150	1450		
CLK to $\overline{COUT}$		800	1150	1300	800	1150	1300	800	1150	1300		
CLK to $\overline{CLOUT}$		825	1150	1400	825	1150	1400	825	1150	1400		
Setup Time	t_s										ps	
S1, S2		1000	650	—	1000	650	—	1000	650	—		
D		800	400	—	800	400	—	800	400	—		
$\overline{CLIN}$		150	0	—	150	0	—	150	0	—		
$\overline{CIN}$		800	400	—	800	400	—	800	400	—		
Hold Time	t_h										ps	
S1, S2		150	−200	—	150	−200	—	150	−200	—		
D		150	−250	—	150	−250	—	150	−250	—		
$\overline{CLIN}$		300	0	—	300	0	—	300	0	—		
$\overline{CIN}$		150	−250	—	150	−250	—	150	−250	—		
Reset Recovery Time	t_{RR}	1000	700	—	1000	700	—	1000	700	—	ps	
Minimum Pulse Width	t_{PW}										ps	
CLK, MR		700	400	—	700	400	—	700	400	—		
Rise/Fall Times	t_r										ps	
$\overline{COUT}$	t_f	275	—	600	275	—	600	275	—	600		20% - 80%
Other		300	—	700	300	—	700	300	—	700		

EXPANDED TRUTH TABLE

Function	S1	S2	MR	$\overline{CIN}$	$\overline{CLIN}$	CLK	D5	D4	D3	D2	D1	D0	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{COUT}$	$\overline{CLOUT}$
Preset	L	L	L	X	X	Z	L	L	L	L	H	H	L	L	L	L	H	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Hold	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
Hold	H	L	L	L	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
	L	H	L	H	H	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Hold	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	H	H	H
Reset	X	X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	H	H

Z = Low to High Transition

APPLICATIONS INFORMATION

Overview

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. Using the S1 and S2 control pins the user can select between preset, count up, count down and hold count. The master reset pin will reset the internal counter, and set the $\overline{COUT}$, $\overline{CLOUT}$, and $\overline{CLIN}$ flip-flops. Unlike previous 136 type counters the carry out outputs will go to a high state during the preset operation. In addition since the carry out outputs are registered they will not go low if terminal count is loaded into the register. The look-ahead-carry out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry out functions. This architecture not only reduces the carry out delay, but is essential to incorporate the registered carry out functions. In addition to being faster, because these functions are registered the resulting carry out signals are stable and glitch free.

Cascading Multiple E136 Devices

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past cascading several 136 type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture it is minor compared to the impact of the ripple propagate designs. As a result the E016 type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

Motorola has incorporated several improvements to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.

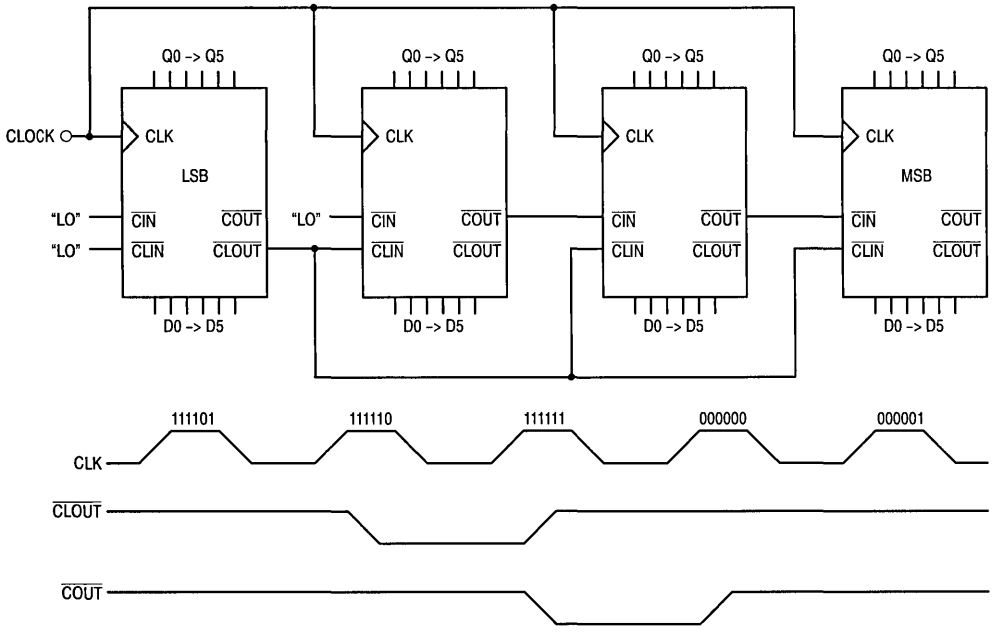


Figure 1. 24-bit Cascaded E136 Counter

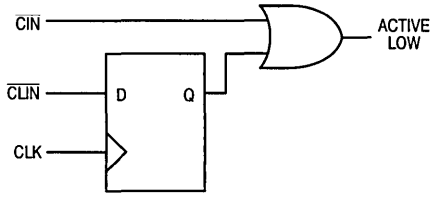


Figure 2. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ($\overline{CLOUT}$) pulses low one clock pulse before the counter reaches terminal count. Also note that both $\overline{CLOUT}$ and the carry out pin ($\overline{COUT}$) of the device pulse low for only one clock period. The input structure for look-ahead-carry in ($\overline{CLIN}$) and carry in ($\overline{CIN}$) is pictured in Figure 2.

The $\overline{CLIN}$ input is registered and then ORed with the $\overline{CIN}$ input. From the truth table one can see that both the $\overline{CIN}$ and the $\overline{CLIN}$ inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The $\overline{CLIN}$ inputs are driven by the $\overline{CLOUT}$ output of the lowest order E136 and therefore are only asserted for a single clock period. Since the $\overline{CLIN}$ input is registered it must be asserted one clock period prior to the $\overline{CIN}$ input.

If the counter previous to a given counter is at terminal count its $\overline{COUT}$ output and thus the $\overline{CIN}$ input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The $\overline{CLOUT}$ output of the LSC will pulse low one clock period before it reaches terminal count. This $\overline{CLOUT}$ signal will be clocked into the $\overline{CLIN}$ input of the higher order counters on the following positive clock transition. Since both $\overline{CIN}$ and $\overline{CLIN}$ are in the LOW state the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by their $\overline{CIN}$ inputs, to count by one.

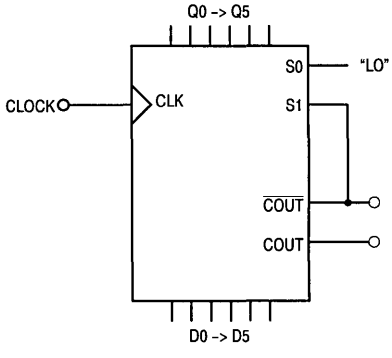


Figure 3. 6-bit Programmable Divider

During the clock pulse in which the higher order counter is counting by one the $\overline{CLIN}$ is clocking in the high signal presented by the $\overline{CLOUT}$ of the LSC. The $\overline{CIN}$'s in the higher order counter will ripple propagate through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has 2^6-1 or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the setup time of the $\overline{CLIN}$ input. This limit will consist of the CLK to $\overline{CLOUT}$ delay of the E136 plus the $\overline{CLIN}$ setup time plus any path length differences between the $\overline{CLOUT}$ output and the clock.

Programmable Divider

Using external feedback of the $\overline{COUT}$ pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count down programmable divider. If for some reason a count up divider is preferred the $\overline{COUT}$ signal is simply fed back to S2 rather than S1. Examination of the truth table for the E136 shows that when both S1 and S2 are LOW the counter will parallel load on the next positive transition of the clock. If the S2 input is low and the S1 input is high the counter will be in the count down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the $\overline{COUT}$ output it becomes a trivial matter to build programmable dividers.

For a programmable divider one wants to load a predesignated number into the counter and count to terminal count. Upon terminal count the counter should automatically reload the divide number. With the architecture shown in Figure 3 when the counter reaches terminal count the $\overline{COUT}$ output and thus the S1 input will go LOW, this combined with the low on S2 will cause the counter to load the inputs present on D0-D5. Upon loading the divide value into the counter $\overline{COUT}$ will go HIGH as the counter is no longer at terminal count thereby placing the counter back into the count mode.

Table 1. Preset Inputs Versus Divide Ratio

Divide Ratio	Preset Data Inputs					
	D5	D4	D3	D2	D1	D0
2	L	L	L	L	L	H
3	L	L	L	L	H	L
4	L	L	L	L	H	H
5	L	L	L	H	L	L
•	•	•	•	•	•	•
•	•	•	•	•	•	•
36	H	L	L	L	H	H
37	H	L	L	H	L	L
38	H	L	L	H	L	H
•	•	•	•	•	•	•
•	•	•	•	•	•	•
62	H	H	H	H	L	H
63	H	H	H	H	H	L
64	H	H	H	H	H	H

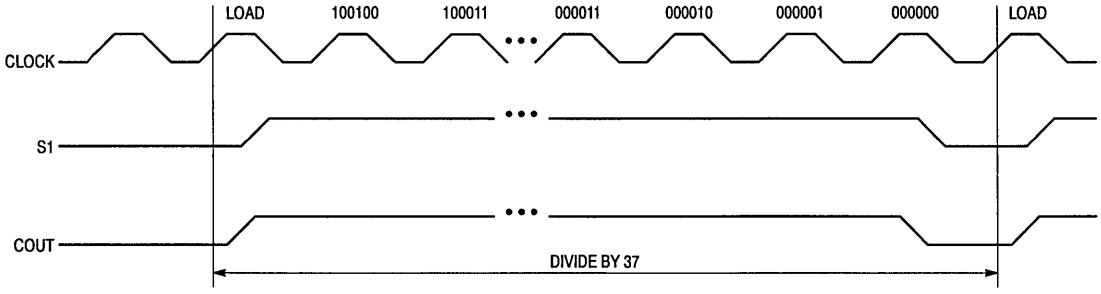


Figure 4. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N–1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64 inclusive, Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complimentary output $\overline{\text{COUT}}$ allows the user to choose the polarity of the divide by output.

For single device programmable counters the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter, this not only simplifies board design but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits the superiority of the E016 diminishes, and in fact for very wide dividers the E136 will provide the capability of a faster count frequency. This potential is a result of the cascading features mentioned previously in this document. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However the final decision as to what device to use for the external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.

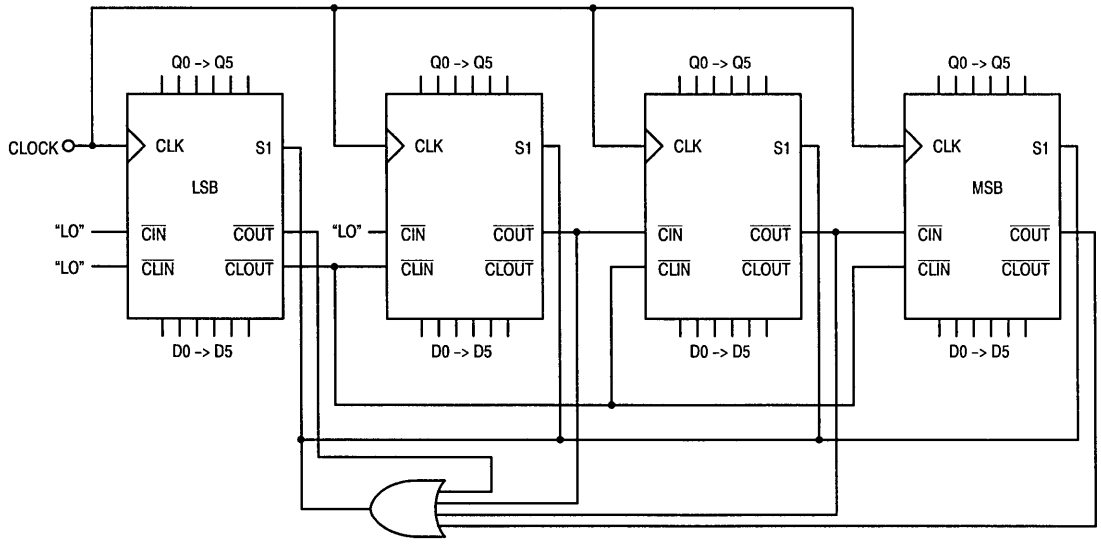


Figure 5. 24-bit Programmable Divider Architecture

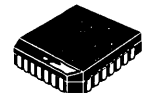
8-Bit Ripple Counter

MC10E137
MC100E137

8-BIT RIPPLE COUNTER

The MC10E/100E137 is a very high speed binary ripple counter. The two least significant bits were designed with very fast edge rates while the more significant bits maintain standard ECLinPS™ output edge rates. This allows the counter to operate at very high frequencies while maintaining a moderate power dissipation level.

- 1.8GHz Minimum Count Frequency
- Differential Clock Input and Data Output Pins
- V_{BB} Output for Single-Ended Use
- Internal 75kΩ Input Pulldown Resistors
- Synchronous and Asynchronous Enable Pins
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of –4.2V to –5.46V



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The device is ideally suited for multiple frequency clock generation as well as a counter in a high performance ATE time measurement board.

Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted enables the counter while overriding any synchronous enable signals. The E137 features XORed enable inputs, EN1 and EN2, which are synchronous to the CLK input. When only one synchronous enable is asserted the counter becomes disabled on the next CLK transition; all outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. If EN1 (or EN2) and CLK edges are coincident, sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip flop setup time) to insure that the synchronous enable signal is clocked correctly, hence, the counter is disabled.

The E137 can also be driven single-endedly utilizing the V_{BB} output supply as the voltage reference for the CLK input signal. If a single-ended signal is to be used the V_{BB} pin should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01μF capacitor. V_{BB} can only source/sink 0.5mA, therefore it should be used as a switching reference for the E137 only.

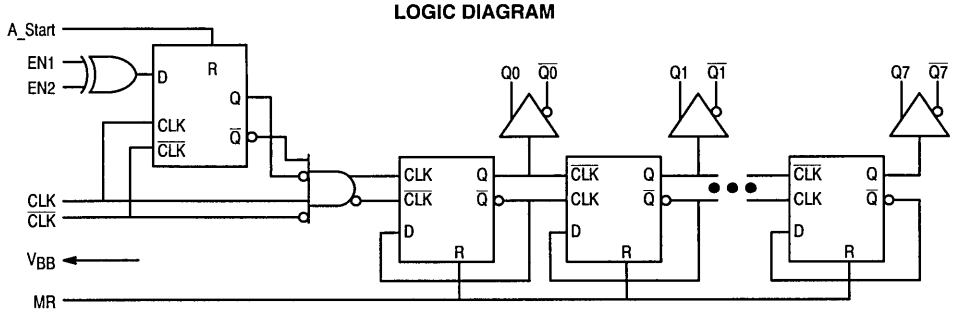
PIN NAMES

PIN	FUNCTION
CLK, $\overline{CLK}$	Differential Clock Inputs
Q0-Q7, $\overline{Q0}$-$\overline{Q7}$	Differential Q Outputs
A_Start	Asynchronous Enable Input
EN1, EN2	Synchronous Enable Inputs
MR	Asynchronous Master Reset
V_{BB}	Switching Refernce Output

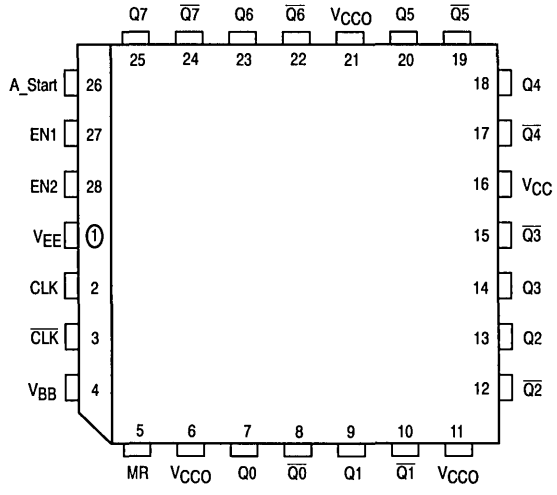
All input pins left open will be pulled LOW via an input pulldown resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

LOGIC DIAGRAM



Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

2

SEQUENTIAL TRUTH TABLE

Function	EN1	EN2	A_Start	MR	CLK	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L
Count	L	L	L	L	Z	L	L	L	L	L	L	L	H
	L	L	L	L	Z	L	L	L	L	L	L	H	L
	L	L	L	L	Z	L	L	L	L	L	L	H	H
Stop	H	L	L	L	Z	L	L	L	L	L	L	H	H
	H	L	L	L	Z	L	L	L	L	L	L	H	H
Asynch Start	H	L	H	L	Z	L	L	L	L	L	H	L	L
	H	L	H	L	Z	L	L	L	L	L	H	L	H
	L	L	H	L	Z	L	L	L	L	L	H	H	L
Count	L	L	L	L	Z	L	L	L	L	L	H	H	H
	L	L	L	L	Z	L	L	L	L	H	L	L	L
	L	L	L	L	Z	L	L	L	L	H	L	L	H
Stop	L	H	L	L	Z	L	L	L	L	H	L	L	H
	L	H	L	L	Z	L	L	L	L	H	L	L	H
Synch Start	H	H	L	L	Z	L	L	L	L	H	L	H	L
	H	H	L	L	Z	L	L	L	L	H	L	H	H
	H	H	L	L	Z	L	L	L	L	H	H	L	L
Stop	H	L	L	L	Z	L	L	L	L	H	H	L	L
	H	L	L	L	Z	L	L	L	L	H	H	L	L
Count	L	L	L	L	Z	L	L	L	L	H	H	L	H
	L	L	L	L	Z	L	L	L	L	H	H	H	L
	L	L	L	L	Z	L	L	L	L	H	H	H	H
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L

Z = Low to High Transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage										V	
	10E	−1 38		−1.27	−1.35		−1 25	−1 31		−1.19		
	100E	−1.38		−1.27	−1.38		−1 26	−1 38		−1.26		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		121	145		121	145		121	145		
	100E		121	145		121	145		139	167		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{COUNT}	Maximum Count Frequency	1800	2200		1800	2200		1800	2200		MHz	
t_{PLH} / t_{PHL}	Propagation Delay to Output										ps	
	CLK to Q0	1300	1700	2150	1300	1700	2150	1350	1750	2200		
	CLK to Q1	1600	2025	2500	1600	2050	2500	1650	2100	2550		
	CLK to Q2	1950	2425	2925	1950	2450	2925	2025	2500	3000		
	CLK to Q3	2275	2750	3350	2275	2775	3350	2350	2850	3425		
	CLK to Q4	2625	3125	3750	2625	3150	3750	2700	3225	3825		
	CLK to Q5	2950	3450	4150	2950	3475	4150	3050	3550	4250		
	CLK to Q6	3250	3775	4450	3250	3800	4450	3375	3925	4600		
	CLK to Q7	3575	4075	4800	3575	4125	4800	3700	4250	4950		
	A_Start to Q0	950	1325	1700	950	1325	1700	950	1325	1700		
	MR to Q0	700	1000	1300	700	1000	1300	700	1000	1300		
t_s	Setup Time (EN1, EN2)	0	−150		0	−150		0	−150		ps	
t_h	Hold Time (EN1, EN2)	300	150		300	150		300	150		ps	
t_{RR}	Reset Recovery Time										ps	
	MR, A_Start	400	200		400	200		400	200			
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR, A_Start	400			400			400				
V_{PP}	Minimum Input Swing (CLK)	0.25		1.0	0.25		1.0	0.25		1.0	V	1
V_{CMR}	Com Mode Range (CLK)	−0 4		−2.0	−0.4		−2.0	−0.4		−2.0	V	
t_r / t_f	Rise/Fall Times										ps	20%–80%
	Q0,Q1	150		400	150		400	150		400		
	Q2 to Q7	275		600	275		600	275		600		

1 Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

8-Bit Shift Register

MC10E141
MC100E141

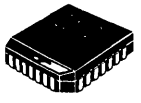
8-BIT SHIFT REGISTER

The MC10E/100E141 is an 8-bit full-function shift register. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs $D_0 - D_7$ accept parallel input data, while DL/DR accept serial input data for left/right shifting. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.

- 700MHz Min. Shift Frequency
- 8-Bit
- Full-Function, Bi-Directional
- Asynchronous Master Reset
- Pin-Compatible with E241
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

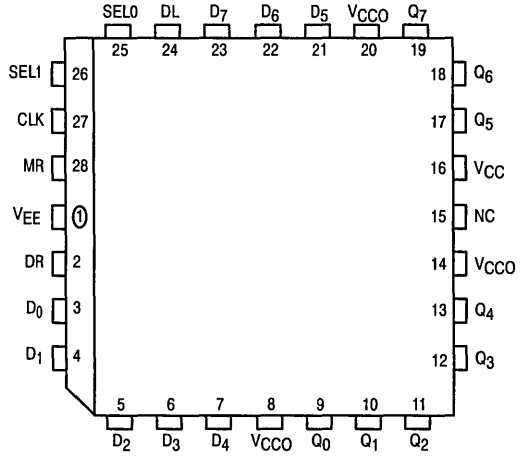
The select pins, SEL0 and SEL1, select one of four modes of operation: Load, Hold, Shift Left, Shift Right, according to the Function Table.

Input data is accepted a set-up time before the positive clock edge. A HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

FUNCTION TABLE

SEL0	SEL1	Function
L	L	Load
L	H	Shift Right (D_n to D_{n+1})
H	L	Shift Left (D_n to D_{n-1})
H	H	Hold

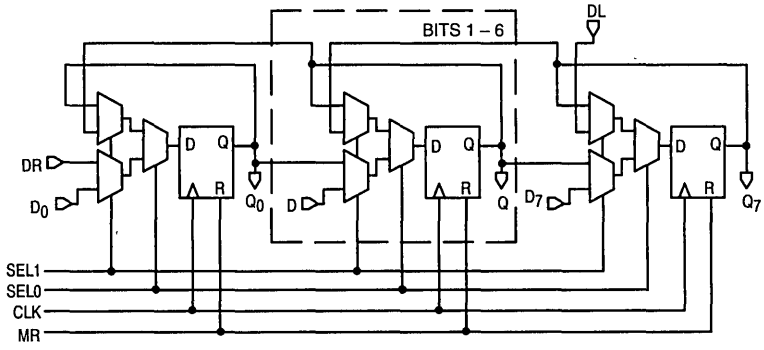
PIN NAMES

Pin	Function
$D_0 - D_7$	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL0, SEL1	Mode Select In Inputs
CLK	Clock
$Q_0 - Q_7$	Data Outputs
MR	Master Reset

EXPANDED FUNCTION TABLE

Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		131	157		131	157		131	157		
	100E		131	157		131	157		151	157		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

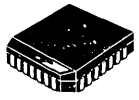
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz	
t_{PLH} t_{PHL}	Propagation Delay To Output										ps	
	Clk	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_s	Setup Time										ps	
	D	175	25		175	25		175	25			
	SEL0	350	200		350	200		350	200			
	SEL1	300	150		300	150		300	150			
t_h	Hold Time										ps	
	D	200	– 25		200	– 25		200	– 25			
	SEL0	100	– 200		100	– 200		100	– 200			
	SEL1	100	–150		100	–150		100	–150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r t_f	Rise/Fall Times										ps	
	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device

9-Bit Shift Register

MC10E142
MC100E142

9-BIT SHIFT REGISTER



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

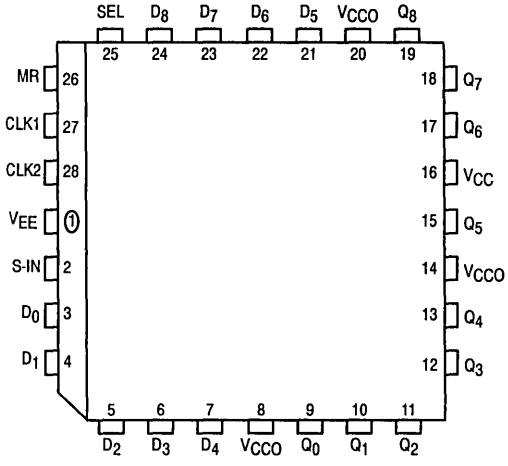
The MC10E/100E142 is a 9-bit shift register, designed with byte-parity applications in mind. The E142 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D0 – D8 accept parallel input data, while S-IN accepts serial input data. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.

- 700MHz Min. Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

The SEL (Select) input pin is used to switch between the two modes of operation — SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the resisters to zero.

2

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

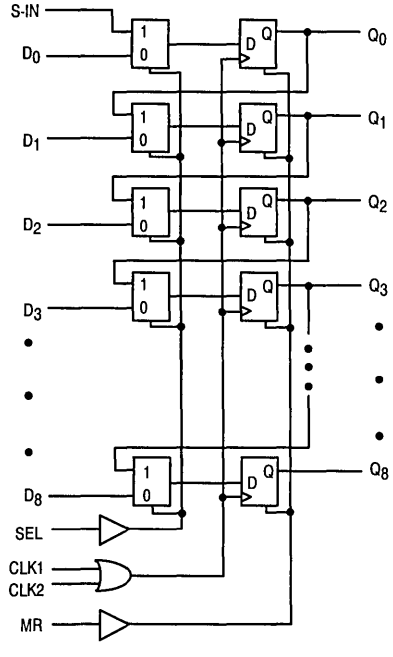
PIN NAMES

Pin	Function
$D_0 - D_8$	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
$Q_0 - Q_8$	Data Outputs

FUNCTIONS

SEL	Mode
L	Load
H	Shift

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		120	145		120	145		120	145		
	100E		120	145		120	145		138	165		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Setup Time										ps	
	D	50	−100		50	−100		50	−100			
	SEL	300	150		300	150		300	150			
t_h	Hold Time										ps	
	D	300	100		300	100		300	100			
	SEL	75	−150		75	−150		75	−150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

9-Bit Hold Register

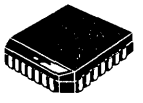
MC10E143
MC100E143

The MC10E/100E143 is a 9-bit holding register, designed with byte-parity applications in mind. The E143 holds current data or loads new data, with the nine inputs D0 – D8 accepting parallel input data.

- 700MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

9-BIT HOLD REGISTER

The SEL (Select) input pin is used to switch between the two modes of operation — HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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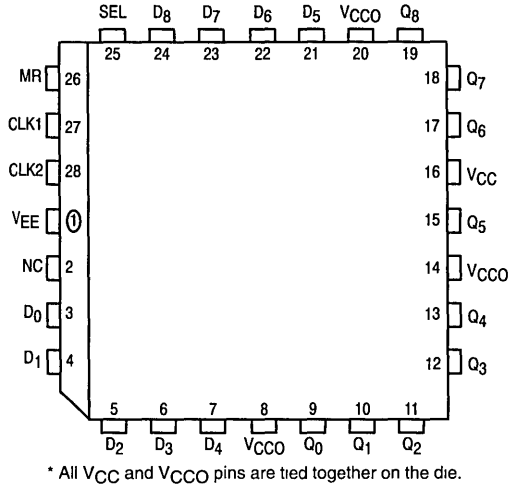
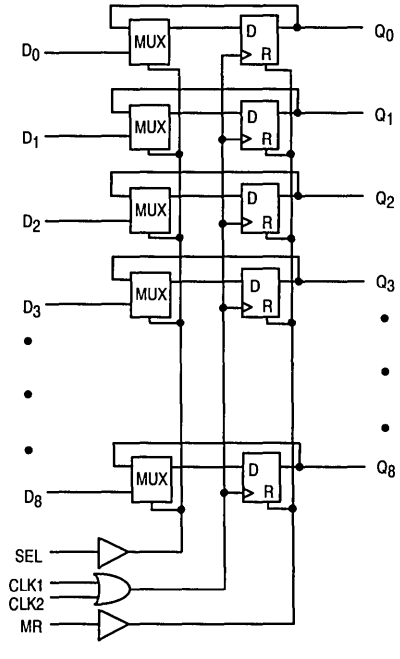
Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_8$	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
$Q_0 - Q_8$	Data Outputs
NC	No Connection

FUNCTIONS

SEL	Mode
L	Load
H	Hold

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		120	145		120	145		120	145		
	100E		120	145		120	145		138	165		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
f_{MAX}	Max. Toggle Frequency	700	900		700	900		700	900		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Setup Time										ps	
	D	50	–100		50	–100		50	–100			
	SEL	300	150		300	150		300	150			
t_h	Hold Time										ps	
	D	300	100		300	100		300	100			
	SEL	75	–150		75	–150		75	–150			
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

2

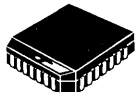
6-Bit D Latch

MC10E150
MC100E150

6-BIT D LATCH

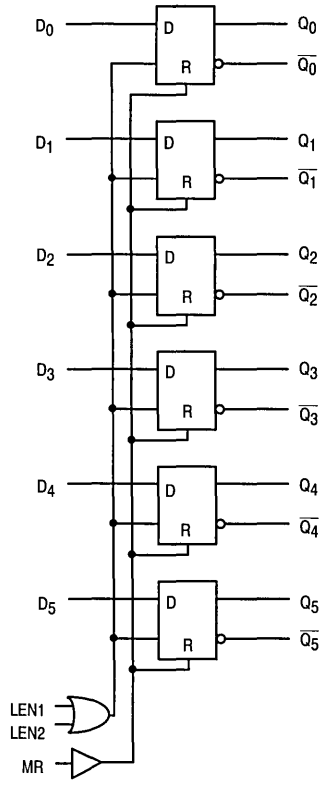
The MC10E/100E150 contains six D-type latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent and input data transitions propagate through to the output. A logic HIGH on either LEN1 or LEN2 (or both) latches the data. The Master Reset (MR) overrides all other controls to set the Q outputs low.

- 800ps Max. Propagation Delay
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

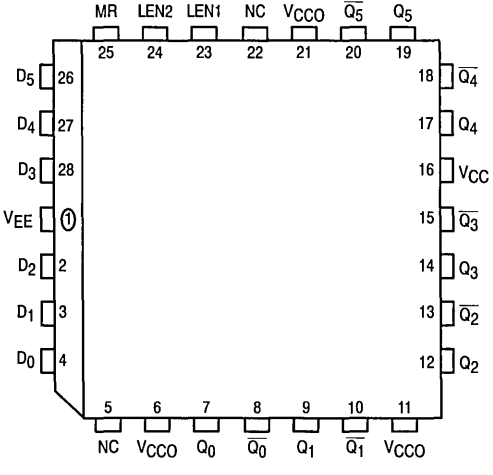
LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_5$	Data Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
$Q_0 - Q_5$	True Outputs
$\overline{Q_0} - \overline{Q_5}$	Inverting Outputs

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current										μA	
	D			200			200			200		
	LEN, MR			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		52	62		52	62		52	62		
	100E		52	62		52	62		60	72		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	250	375	550	250	375	550	250	375	550		
	LEN	375	500	700	375	500	700	375	500	700		
	MR	450	625	750	450	625	750	450	625	750		
t_S	Setup Time										ps	
	D	200	50		200	50		200	50			
t_h	Hold Time										ps	
	D	200	−50		200	−50		200	−50			
t_{RR}	Reset Recovery Time	750	650		750	650		750	650		ps	ps
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	450	650	300	450	650	300	450	650		

1. Within-device skew is defined as identical transitions on similar paths through a device.

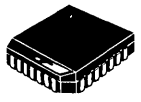
6-Bit D Register

MC10E151
MC100E151

6-BIT D REGISTER

The MC10E/100E151 contains 6 D-type, edge-triggered, master-slave flip-flops with differential outputs. Data enters the master when both CLK1 and CLK2 are LOW, and is transferred to the slave when CLK1 or CLK2 (or both) go HIGH. The asynchronous Master Reset (MR) makes all Q outputs go LOW.

- 1100MHz Min. Toggle Frequency
- Differential Outputs
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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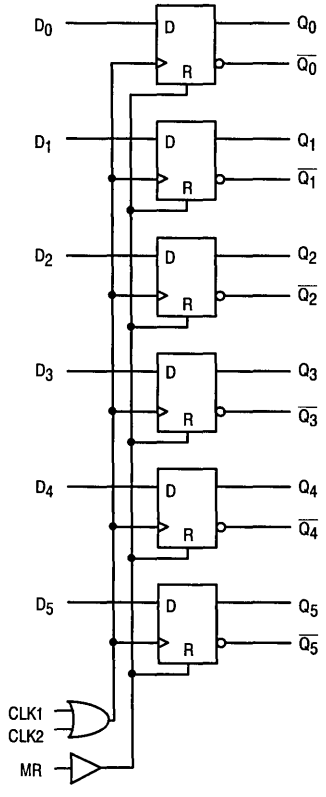
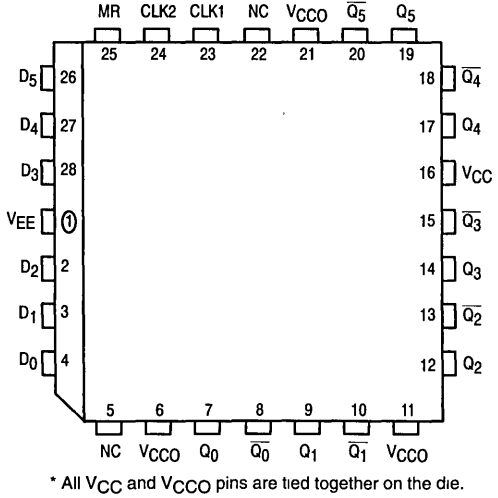
LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_5$	Data Inputs
CLK1, CLK2	Clock Inputs
MR	Master Reset
$Q_0 - Q_5$	True Outputs
$\overline{Q_0} - \overline{Q_5}$	Inverted Outputs

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		65	78		65	78		65	78		
	100E		65	78		65	78		75	90		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
f_{MAX}	Max. Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk	475	650	800	475	650	800	475	650	800		
	MR	475	650	850	475	650	850	475	650	850		
t_s	Setup Time										ps	
	D	0	–175		0	–175		0	–175			
t_h	Hold Time										ps	
	D	350	175		350	175		350	175			
t_{RR}	Reset Recovery Time	750	550		750	550		750	550			ps
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_{SKEW}	Within-Device Skew		65			65			65		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	450	700	300	450	700	300	450	700		

1. Within-device skew is defined as identical transitions on similar paths through a device.

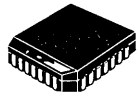
5-Bit 2:1 Mux-Latch

MC10E154
MC100E154

5-BIT 2:1
MUX-LATCH

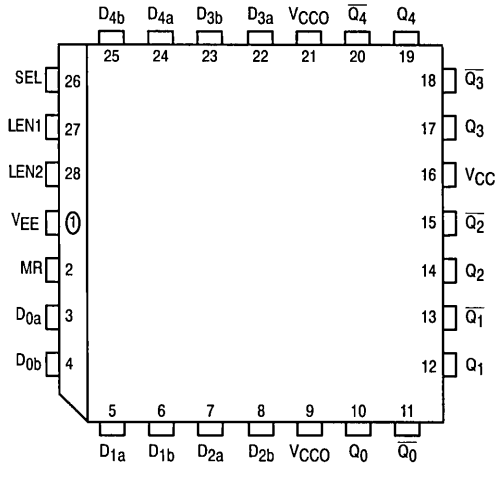
The MC10E/100E154 contains five 2:1 multiplexers followed by transparent latches with differential outputs When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

- 850ps Max. LEN to Output
- 825ps Max. D to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



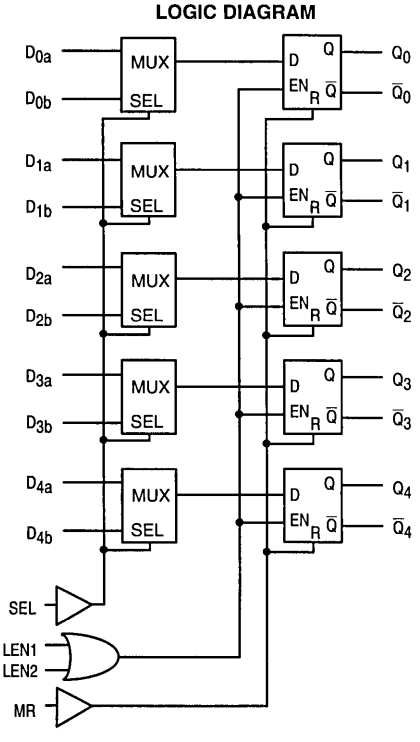
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_{0a} - D_{4a}$	Input Data a
$D_{0b} - D_{4b}$	Input Data b
SEL	Data Select Input
LEN1, LEN2	Latch Enables
MR	Master Reset
$Q_0 - Q_4$	True Outputs
$\overline{Q_0} - \overline{Q_4}$	Inverted Outputs

TRUTH TABLE

SEL	Data
H	a
L	b

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		76	91		76	91		76	91		
	100E		76	91		76	91		87	105		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	325	500	700	325	500	700	325	500	700		
	SEL	475	650	925	475	650	925	475	650	925		
	LEN	350	500	750	350	500	750	350	500	750		
	MR	450	600	800	450	600	800	450	600	800		
t_s	Setup Time										ps	
	D	300	100		300	100		300	100			
	SEL	500	250		500	250		500	250			
t_h	Hold Time										ps	
	D	300	−100		300	−100		300	−100			
	SEL	200	− 250		200	− 250		200	− 250			
t_{RR}	Reset Recovery Time	800	600		800	600		800	600			ps
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	475	800	300	475	800	300	475	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

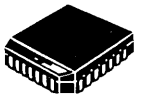
6-Bit 2:1 Mux-Latch

MC10E155
MC100E155

6-BIT 2:1
MUX-LATCH

The MC10E/100E155 contains six 2:1 multiplexers followed by transparent latches with single-ended outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

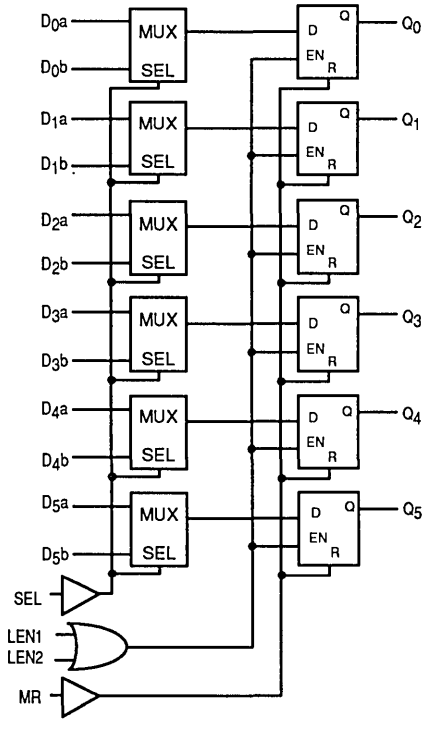
- 850ps Max. LEN to Output
- 825ps Max. D to Output
- Single-Ended Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



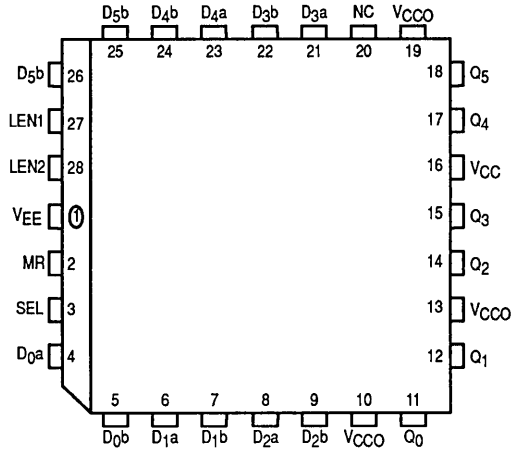
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

2

LOGIC DIAGRAM



Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

2

PIN NAMES

Pin	Function
$D_0a - D_04$	Input Data a
$D_0b - D_4b$	Input Data b
SEL	Data Select Input
LEN1, LEN2	Latch Enables
MR	Master Reset
$Q_0 - Q_4$	Outputs

TRUTH TABLE

SEL	Data
H	a
L	b

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		85	102		85	102		85	102		
	100E		85	102		85	102		98	117		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	325	500	700	325	500	700	325	500	700		
	SEL	475	675	925	475	675	925	475	675	925		
	LEN	350	500	750	350	500	750	350	500	750		
	MR	450	600	850	450	600	850	450	600	850		
t_s	Setup Time										ps	
	D	300	100		300	100		300	100			
	SEL	500	250		500	250		500	250			
t_h	Hold TIme										ps	
	D	300	−100		300	−100		300	−100			
	SEL	0	− 250		0	− 250		0	− 250			
t_{RR}	Reset Recovery Time	800	650		800	650		800	650		ps	
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	450	800	300	450	800	300	450	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

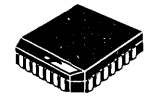
3-Bit 4:1 Mux-Latch

MC10E156
MC100E156

3-BIT 4:1
MUX-LATCH

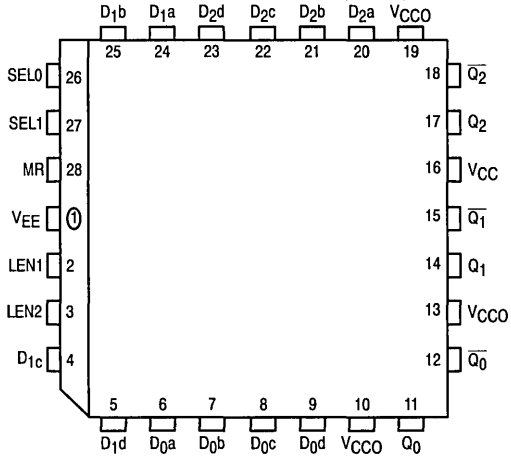
The MC10E/100E156 contains three 4:1 multiplexers followed by transparent latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output date is controlled by the multiplexer select controls (SEL0, SEL1). A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

- 950ps Max. D to Output
- 850ps Max. LEN to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



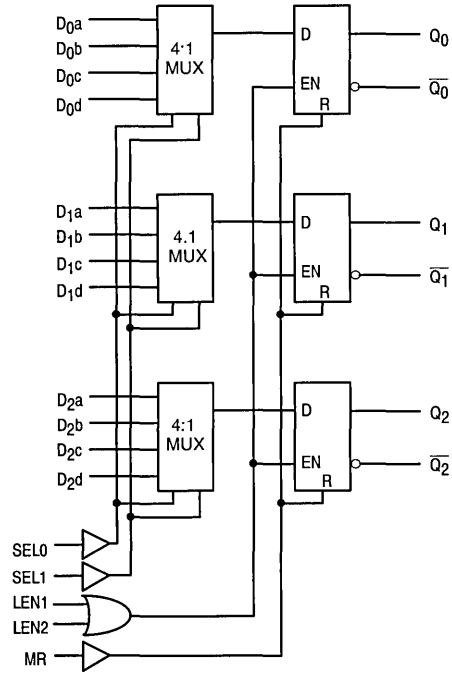
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0x - D_3x$	Input Data
SEL0, SEL1	Select Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
$Q_0 - Q_2$	True Outputs
$\overline{Q_0} - \overline{Q_2}$	Inverted Outputs

FUNCTION TABLE

SEL0	SEL1	Data
L	L	a
L	H	b
H	L	c
H	H	d

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		75	90		75	90		75	90		
	100E		75	90		75	90		86	103		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	400	600	900	400	600	900	400	600	900		
	SEL0	550	775	1050	550	775	1050	550	775	1050		
	SEL1	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	800		
	MR	350	600	825	350	600	825	350	600	825		
t_s	Setup Time										ps	
	D	400	275		400	275		400	275			
	SEL0	700	300		700	300		700	300			
	SEL1	600	400		600	400		600	400			
t_h	Hold Time										ps	
	D	300	−275		300	−275		300	−275			
	SEL0	100	−300		100	−300		100	−300			
	SEL1	200	−400		200	−400		200	−400			
t_{RR}	Reset Recovery Time	800	600		800	600		800	600			ps
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	475	700	275	475	700	275	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device.

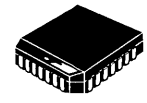
Quad 2:1 Multiplexer

MC10E157
MC100E157

QUAD 2:1 MULTIPLEXER

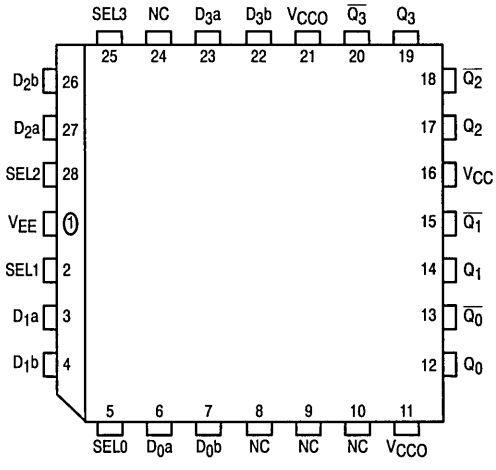
The MC10E/100E157 contains four 2:1 multiplexers with differential outputs. The output data are controlled by the individual Select (SEL) inputs. The individual select control makes the devices well suited for random logic designs.

- Individual Select Controls
- 550ps Max. D to Output
- 800ps Max. SEL to Output
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- Internal 75kΩ Input Pulldown Resistors



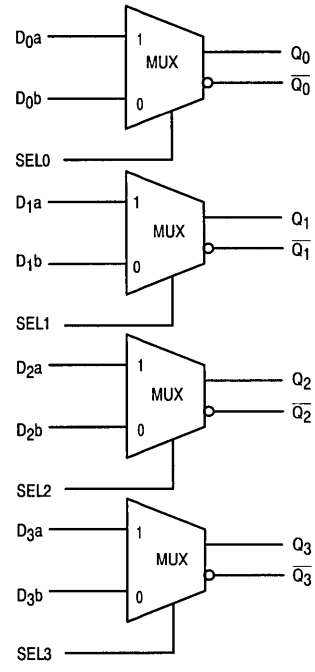
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0a - D_3a$	Input Data a
$D_0b - D_3b$	Input Data b
SEL0 – SEL3	Select Inputs
$Q_0 - Q_3$	True Outputs
$\overline{Q_0} - \overline{Q_3}$	Inverted Outputs

TRUTH TABLE

SEL	Data
H	a
L	b

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current										μA	
	D			200			200			200		
	SEL			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		32	38		32	38		32	38		
	100E		32	38		32	38		37	44		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	220	380	550	220	380	550	220	380	550		
	SEL	425	600	800	425	600	800	425	600	800		
t_{SKEW}	Within-Device Skew		70			70			70		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	400	650	275	400	650	275	400	650		

1. Within-device skew is defined as identical transitions on similar paths through a device.

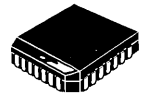
5-Bit 2:1 Multiplexer

MC10E158
MC100E158

The MC10E/100E158 contains five 2:1 multiplexers with differential outputs. The output data are controlled by the Select input (SEL).

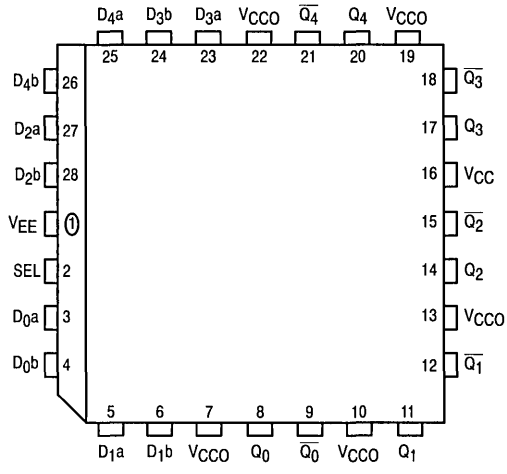
- 600ps Max. D to Output
- 800ps Max. SEL to Output
- Differential Outputs
- One V_{CCO} Pin Per Output Pair
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

5-BIT 2:1 MULTIPLEXER



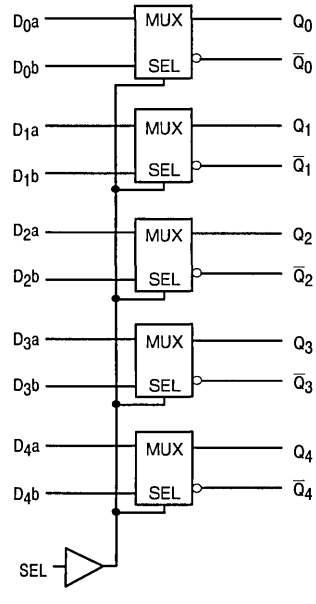
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0a - D_4a$	Input Data a
$D_0b - D_4b$	Input Data b
SEL	Select Input
$Q_0 - Q_4$	True Outputs
$\overline{Q}_0 - \overline{Q}_4$	Inverted Outputs

FUNCTION TABLE

SEL	Data
H	a
L	b

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current										µA	
	D			200			200			200		
	SEL			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		33	40		33	40		33	40		
	100E		33	40		33	40		38	46		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	225	385	550	225	385	550	225	385	550		
	SEL	400	600	775	400	600	775	400	600	775		
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r	Rise/Fall Time										ps	
t_f	20 - 80%	275	425	650	275	425	650	275	425	650		

1. Within-device skew is defined as identical transitions on similar paths through a device.

12-Bit Parity Generator/Checker

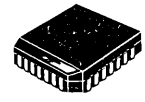
MC10E160
MC100E160

12-BIT PARITY GENERATOR/CHECKER

The MC10E/100E160 is a 12-bit parity generator/checker. The Q output is HIGH when an odd number of inputs are HIGH. A HIGH on the Enable input ($\overline{EN}$) forces the Q output LOW.

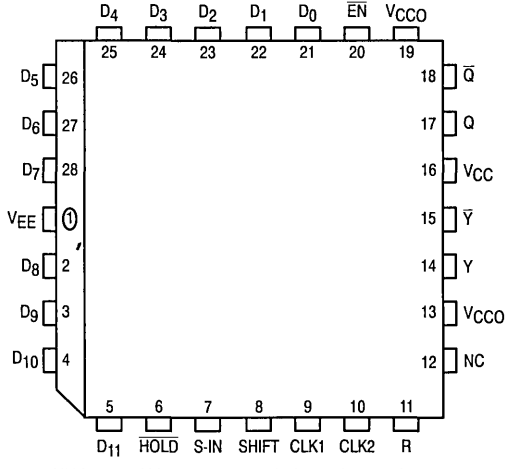
The E160 also features an output register. Multiplexers direct the register input, giving the option of holding present data by asserting $\overline{HOLD}$ LOW, or of shifting data in through the S-IN pin by asserting SHIFT HIGH. The output register itself is clocked by a positive edge on CLK1 or CLK2 (or both). A HIGH on the reset pin (R) overrides to force the Y output LOW.

- Provides Odd-HIGH Parity of 12 Inputs
- Shiftable Output Register with Hold
- 900ps Max. D to Q/$\overline{Q}$ Output
- Enable
- Asynchronous Register Reset
- Dual Clocks
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



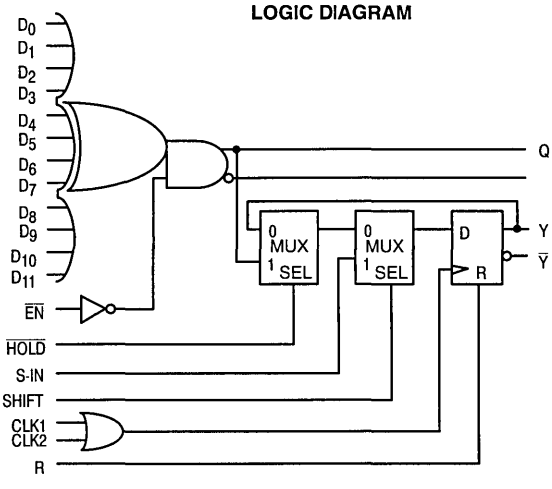
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_{11}$	Data Inputs
S-IN	Serial Data Input
$\overline{EN}$	Enable, active LOW
$\overline{HOLD}$	Hold, active LOW
SHIFT	Shift, active HIGH
CLK1, CLK2	Clock Inputs
R	Reset Inputs
Q, $\overline{Q}$	Direct Output
Y, $\overline{Y}$	Register Output

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current										µA	
	CLK1, CLK2			200			200			200		
	R			300			300			300		
	All Other Inputs			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		82	98		82	98		82	98		
	100E		82	98		82	98		94	113		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to Q	400	650	950	400	650	950	400	650	950		
	$\overline{En}$ to Q	300	550	750	300	550	750	300	550	750		
	CLK to Y	275	500	700	275	500	700	275	500	700		
	R to Y	275	500	725	275	500	725	275	500	725		
t_s	Setup Time										ps	
	D	1200	900		1200	900		1200	900			
	$\overline{HOLD}$	600	300		600	300		600	300			
	S-IN	350	150		350	150		350	150			
	SHIFT	500	250		500	250		500	250			
t_h	Hold Time										ps	
	D	– 400	– 900		– 400	– 900		– 400	– 900			
	$\overline{HOLD}$	100	– 300		100	– 300		100	– 300			
	S-IN	300	–150		300	–150		300	–150			
	SHIFT	200	– 250		200	– 250		200	– 250			
t_r	Rise/Fall Time										ps	
t_f	20 - 80%	300	450	650	300	450	650	300	450	650		

1. Within a device skew is guaranteed for identical transitions on similar paths through a device.

2-Bit 8:1 Multiplexer

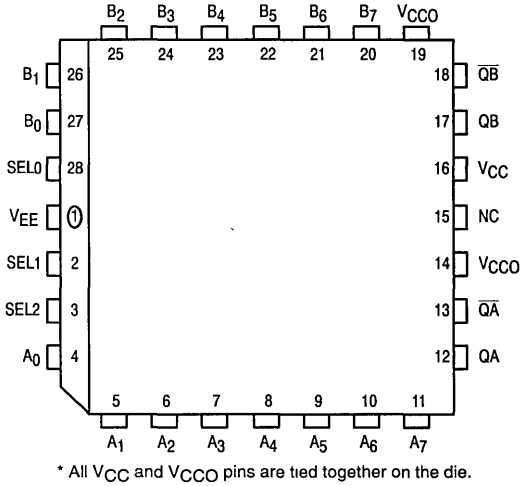
MC10E163
MC100E163

2-BIT
8:1 MULTIPLEXER

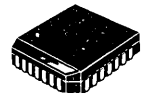
The MC10E/100E163 contains two 8:1 multiplexers with differential outputs and common select inputs. The select inputs (SEL0, 1, 2) control which one of the eight data inputs ($A_0 - A_7$, $B_0 - B_7$) is propagated to the output.

- 850ps Max. D to Output
- Differential Outputs
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



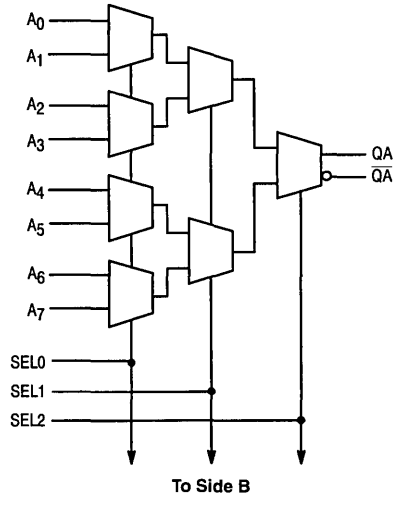
* All V_{CC} and V_{CCO} pins are tied together on the die.



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

2

LOGIC DIAGRAM



FUNCTION TABLE

SEL2	SEL1	SEL0	A/B Data
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

PIN NAMES

Pin	Function
$A_0 - A_7$	A Data Inputs
$B_0 - B_7$	B Data Inputs
SEL0, 1, 2	Select Inputs
QA, QB	True Outputs
$\overline{QA}$, $\overline{QB}$	Inverting Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		73	88		73	88		73	88		
	100E		73	88		73	88		83	100		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output											ps
t_{PHL}	D	400	550	800	400	550	800	400	550	800		
	SEL0	525	725	950	525	725	950	525	725	950		
	SEL1	425	625	850	425	625	850	425	625	850		
	SEL2	350	525	725	350	525	725	350	525	725		
t_{SKEW}	Within-Device Skew										ps	1
	An, Bn to Q		40			40			40			
	An, Am to QA		30			30			30			
	Bn, Bm to QB		30			30			30			
t_r	Rise/Fall Time										ps	
t_f	20 - 80%	275	375	575	275	375	575	275	375	575		

1. Within-device skew is defined as identical transitions on similar paths through a device; n = 0-7, m n, m = 0-7.

16:1 Multiplexer

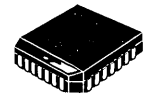
MC10E164
MC100E164

16:1 MULTIPLEXER

The MC10E/100E164 is a 16:1 multiplexer with a differential output. The select inputs (SEL0, 1, 2, 3) control which one of the sixteen data inputs (A0 – A15) is propagated to the output.

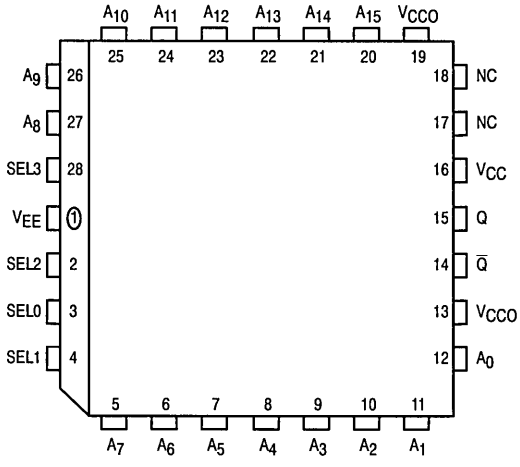
Special attention to the design layout results in a typical skew between the 16 inputs of only 50ps.

- 850ps Data Input to Output
- Differential Output
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- Internal 75kΩ Input Pulldown Resistors



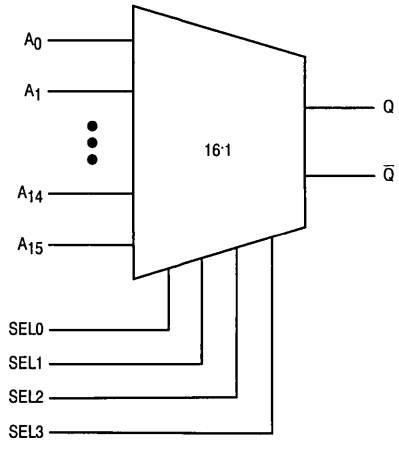
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$A_0 - A_{15}$	Data Inputs
SEL[0:3]	Select Inputs
Q, $\overline{Q}$	Output

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		59	71		59	71		59	71		
	100E		59	71		59	71		68	81		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	A Input	350	600	850	350	600	850	350	600	850		
	SEL0	500	700	900	500	700	900	500	700	900		
	SEL1	400	675	900	400	675	900	400	675	900		
	SEL2	400	675	900	400	675	900	400	675	900		
	SEL3	400	550	700	400	550	700	400	550	700		
t_{SKEW}	Within Device Skew		50			50			50		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	400	550	275	400	550	275	400	550		

1. Within Device skew is defined as the difference in the A to Q delay between the 16 different A inputs.

FUNCTION TABLE

SEL3	SEL2	SEL1	SEL0	Data
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	L	L	L	A8
H	L	L	H	A9
H	L	H	L	A10
H	L	H	H	A11
H	H	L	L	A12
H	H	L	H	A13
H	H	H	L	A14
H	H	H	H	A15

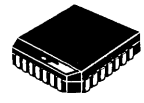
9-Bit Magnitude Comparator

MC10E166
MC100E166

The MC10E/100E166 is a 9-bit magnitude comparator which compares the binary value of two 9-bit words and indicates whether one word is greater than, or equal to, the other.

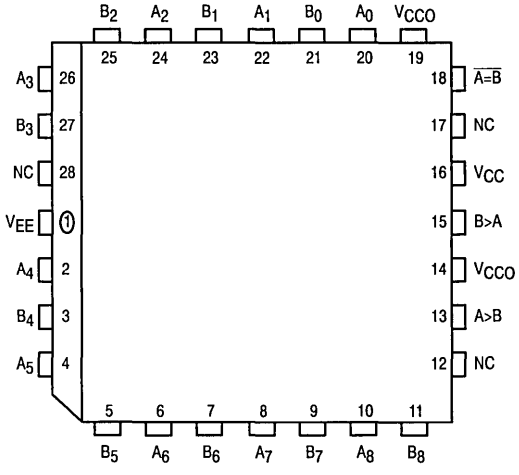
- 1100ps Max. $\overline{A=B}$
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

9-BIT MAGNITUDE COMPARATOR



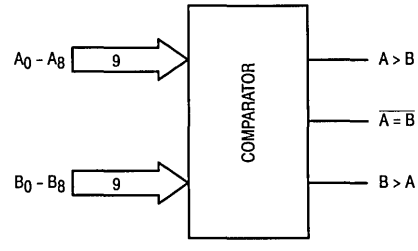
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$A_0 - A_8$	A Data Inputs
$B_0 - B_8$	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A = B}$	A Equal to B Output (active-LOW)

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		113	136		113	136		113	136		
	100E		113	136		113	136		130	136		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to A = B	500	750	1100	500	750	1100	500	750	1100		
	D to A < B, A > B	500	850	1400	500	850	1400	500	850	1400		
t_r	Rise/Fall Time										ps	
t_f	20 - 80%	300	450	800	300	450	800	300	450	800		

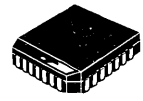
6-Bit 2:1 Mux-Register

MC10E167
MC100E167

6-BIT 2:1
MUX-REGISTER

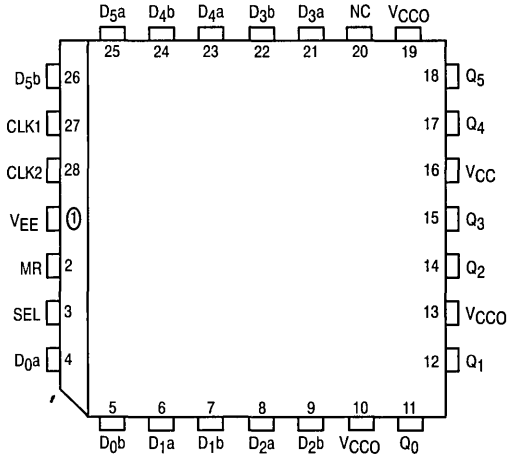
The MC10E/100E167 contains six 2:1 multiplexers followed by D flip-flops with single-ended outputs. Input data are selected by the Select control, SEL. The selected data are transferred to the flip-flop outputs by a positive edge on CLK1 or CLK2 (or both). A HIGH on the Master Reset (MR) pin asynchronously forces all Q outputs LOW.

- 1000MHz Min. Operating Frequency
- 800ps Max. Clock to Output
- Single-Ended Outputs
- Asynchronous Master Resets
- Dual Clocks
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



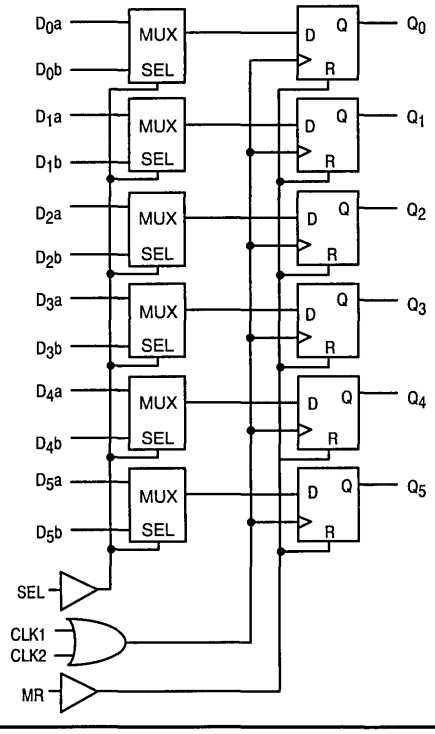
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0a - D_5a$	Input Data a
$D_0b - D_5b$	Input Data b
SEL	Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
$Q_0 - Q_5$	Data Outputs

FUNCTIONS

SEL	Data
H	a
L	b

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		94	113		94	113		94	113		
	100E		94	113		94	113		108	130		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	min	typ	max	min	typ	max	min	typ	max	Unit	Condition
f_{MAX}	Max. Toggle Frequency	1000	1400		1000	1400		1000	1400		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk	450	650	800	450	650	800	450	650	800		
	MR	450	650	850	450	650	850	450	650	850		
t_s	Setup Time										ps	
	D	100	– 50		100	– 50		100	– 50			
	SEL	275	125		275	125		275	125			
t_h	Hold Time										ps	
	D	300	50		300	50		300	50			
	SEL	75	–125		75	–125		75	–125			
t_{RR}	Reset Recovery Time	750	550		750	550		750	550		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		75			75			75		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	450	800	300	450	800	300	450	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

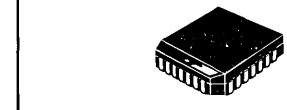
3-Bit 4:1 Multiplexer

MC10E171
MC100E171

3-BIT 4:1 MULTIPLEXER

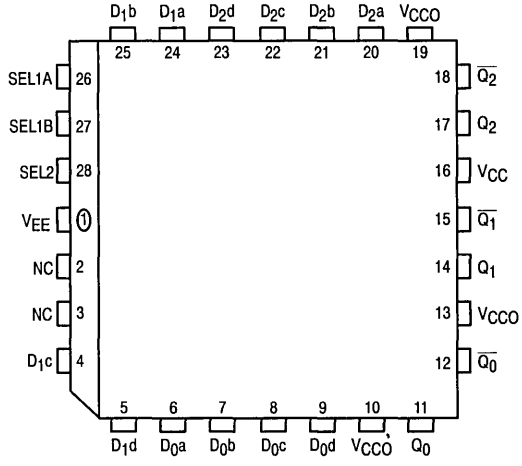
The MC10E/100E171 contains three 4:1 multiplexers with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol). The three Select inputs control which one of the four data inputs in each case is propagated to the corresponding output.

- 725ps Max. D to Output
- Split Select
- Differential Outputs
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



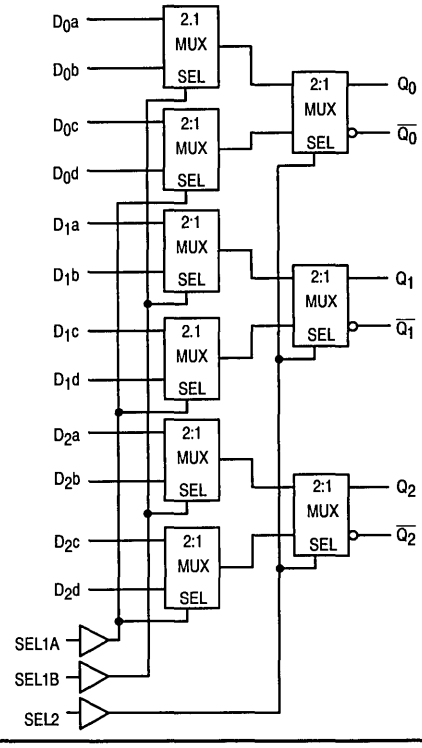
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0x - D_2x$	Data Inputs
SEL1A, SEL1B	First-stage Select Inputs
SEL2	Second-stage Select Input
$Q_0 - Q_2$	True Output
$\overline{Q}_0 - \overline{Q}_2$	Inverted Output

FUNCTION TABLE

Pin	State	Operation
SEL2	H	Output c/d data
SEL1A	H	Input d data
SEL1B	H	Input b data

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		56	67		56	67		56	67		
	100E		56	67		56	67		65	77		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	275	480	650	275	480	650	275	480	650		
	SEL1	450	650	850	450	650	850	450	650	850		
	SEL2	350	550	700	350	550	700	350	550	700		
t_{SKEW}	Within-Device Skew										ps	1
	Dnm, Dnm to Qn		60			60			60			
	Da, Db, Dc, Dd to Q		40			40			40			
t_r	Rise/Fall Time										ps	
t_f	20 - 80%	300	475	650	300	475	650	300	475	650		

1. Within-device skew is defined as identical transitions on similar paths through a device; n = 0,1,2 m = a,b,c,d

9-Bit Latch With Parity

MC10E175
MC100E175

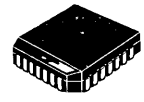
9-BIT LATCH WITH PARITY

The MC10E/100E175 is a 9-bit latch. It also features a tenth latched output, ODDPAR, which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

The E175 can also be used to generate byte parity by using D8 as the parity-type select (L = even parity, H = odd parity), and using ODDPAR as the byte parity output.

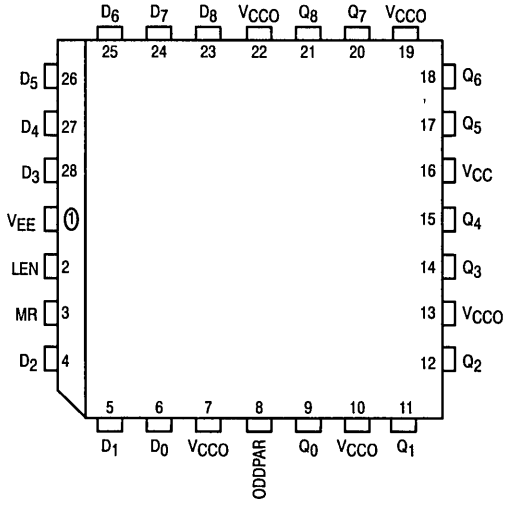
The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

- 9-Bit Latch
- Parity Detection/Generation
- 800ps Max. D to Output
- Reset
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- Internal 75kΩ Input Pulldown Resistors



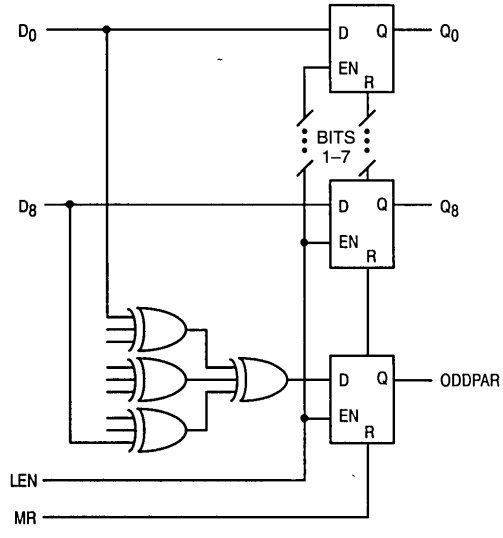
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_8$	Data Inputs
LEN	Latch Enable
MR	Master Reset
$Q_0 - Q_8$	Data Outputs
ODDPAR	Parity Output

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Cond
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		110	132		110	132		110	132		
	100E		110	132		110	132		127	152		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Cond
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D to Q	450	600	800	450	600	800	450	600	800		
	D to ODDPAR	850	1150	1450	850	1150	1450	850	1150	1450		
	LEN to Q	525	700	900	525	700	900	525	700	900		
	LEN to ODDPAR	525	700	900	525	700	900	525	700	900		
	MR to Q(t_{PHL})	525	700	900	525	700	900	525	700	900		
	MR to ODDPAR(t_{PHL})	525	700	900	525	700	900	525	700	900		
t_s	Setup Time										ps	
	D (Q)	275	100		275			275				
	D (ODDPAR)	900	700		900			900				
t_h	Hold Time										ps	
	D (Q)	175	–100		175			175				
	D (ODDPAR)	– 300	– 70		– 300			– 300				
t_{RR}	Reset Recovery Time	850	600		850	600		850	600		ps	
t_{SKEW}	Within-Device Skew										ps	1
	LEN, MR		75			75			75			
	D to Q		75			75			75			
	D to ODDPAR		200			200			200			
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	500	800	300	500	800	300	500	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

FUNCTION TABLE

D	EN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of Dn HIGH
L	L	L	L	H if odd no. of Dn HIGH
X	H	L	Q_0	Q_0
X	X	H	L	L

Error Detection/Correction Circuit

MC10E193
MC100E193

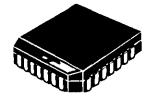
ERROR DETECTION/ CORRECTION CIRCUIT

The MC10E/100E193 is an error detection and correction (EDAC) circuit. Modified Hamming parity codes are generated on an 8-bit word according to the pattern shown in the logic symbol. The P5 output gives the parity of the whole word. The word parity is also provided at the PGEN pin, after Odd/Even parity control and gating with the BPAR input. This output also feeds to a 1-bit shiftable register, for use as part of a scan ring.

The combinatorial part of the device generates the same code pattern as the MC10193, a member of the MECL 10K family. The user is referred to the 10193 data sheet in the *MECL Device Data Book* for an expanded description of pattern expansion to long words, along with check bit generation and decoding schemes.

Used in conjunction with 12-bit parity generators such as the E160, a SECDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

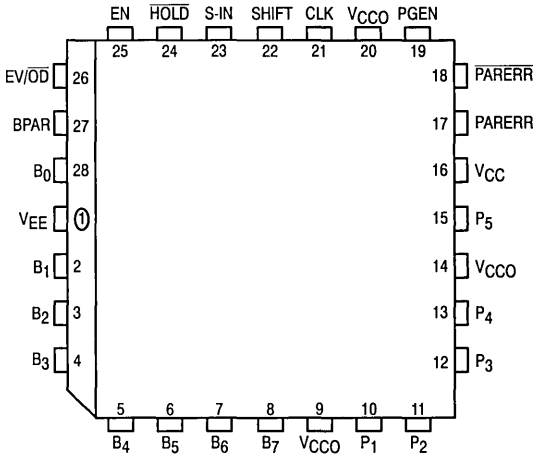
- Hamming Code Generation
- 8-Bit Word, Expandable
- Provides Parity of Whole Word
- Scannable Parity Register
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

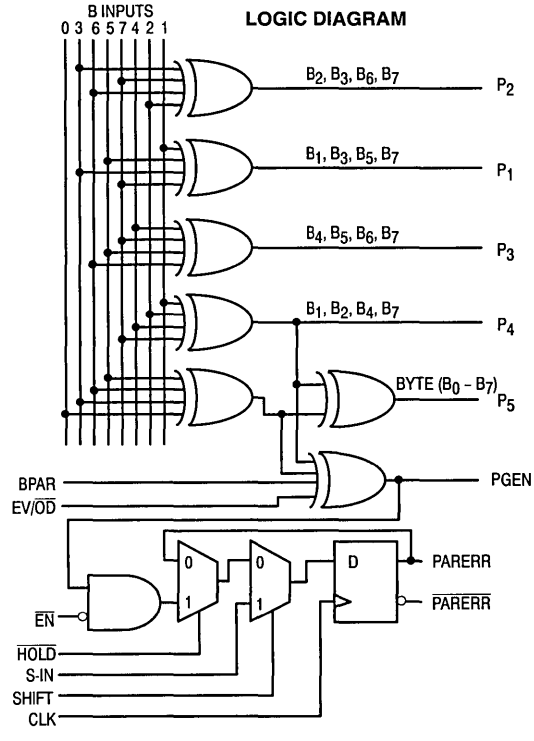
2

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		112	134		112	134		112	134		
	100E		112	134		112	134		129	155		

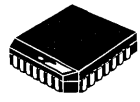
AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	B to P1, P2, P3, P4	350	700	1000	350	700	1000	350	700	1000		
	B to P5	400	775	1150	400	775	1150	400	775	1150		
	EV/$\overline{OD}$, BPAR to PGEN	350	650	850	350	650	850	350	650	850		
	B to PGEN	600	1000	1450	600	1000	1450	600	1000	1450		
	CLK to PARERR	300	550	850	300	550	850	300	550	850		
t_S	Setup Time										ps	
	SHIFT	400	150		400	150		400	150			
	S-IN	300	50		300	50		300	50			
	$\overline{HOLD}$	750	350		750	350		750	350			
	$\overline{EN}$	500	250		500	250		500	250			
	EV/$\overline{OD}$	1300	850		1300	850		1300	850			
	BPAR	1300	850		1300	850		1300	850			
	B	1700	1100		1700	1100		1700	1100			
t_h	Hold Time										ps	
	SHIFT	200	−150		200	−150		200	−150			
	S-IN	300	− 50		300	− 50		300	− 50			
	$\overline{HOLD}$	100	− 350		100	− 350		100	− 350			
	$\overline{EN}$	100	− 250		100	− 250		100	− 250			
	EV/$\overline{OD}$	− 200	− 850		− 200	− 850		− 200	− 850			
	BPAR	− 200	− 850		− 200	− 850		− 200	− 850			
	B	− 300	−1100		− 300	−1100		− 300	−1100			
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	700	1100	300	700	1100	300	700	1100		

Programmable Delay Chip

MC10E195
MC100E195

PROGRAMMABLE DELAY CHIP



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E/100E195 is a programmable delay chip (PDC) designed primarily for clock de-skewing and timing adjustment. It provides variable delay of a differential ECL input transition.

The delay section consists of a chain of gates organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the E195 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

Because the delay programmability of the E195 is achieved by purely differential ECL gate delays the device will operate at frequencies of >1.0 GHz while maintaining over 600 mV of output swing.

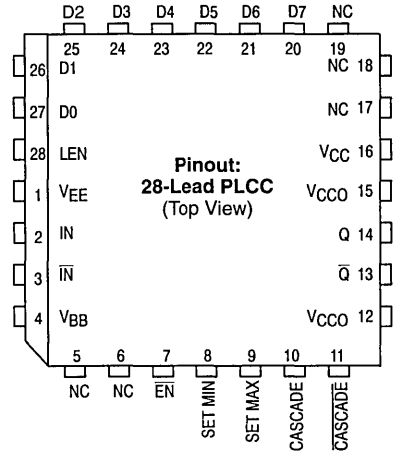
The E195 thus offers very fine resolution, at very high frequencies, that is selectable entirely from a digital input allowing for very accurate system clock timing.

An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

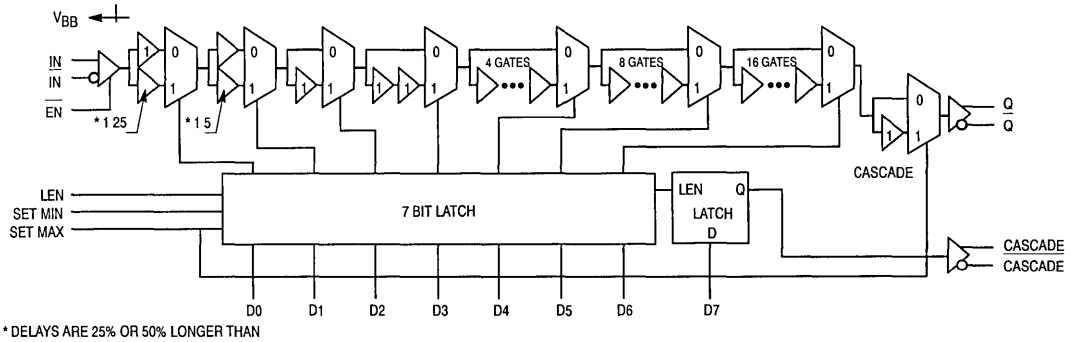
- 2.0ns Worst Case Delay Range
- ≈20ps/Delay Step Resolution
- >1.0GHz Bandwidth
- On Chip Cascade Circuitry
- Extended 100E V_{EE} Range of –4.2 to –5.46V
- 75KΩ Input Pulldown Resistors

PIN NAMES

Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Min Delay Set
SET MAX	Max Delay Set
CASCADE	Cascade Signal



LOGIC DIAGRAM – SIMPLIFIED



* DELAYS ARE 25% OR 50% LONGER THAN STANDARD (STANDARD ≈ 80 PS)

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		130	156		130	156		130	156		
	100E		130	156		130	156		150	179		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay										ps	
	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765		
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range										ps	
	t_{PD} (max) – t_{PD} (min)	2000	2175		2050	2240		2375	2580			
Δt	Step Delay										ps	6
	D0 High		17			17.5			21			
	D1 High		34			35			42			
	D2 High	55	68	105	55	70	105	65	84	120		
	D3 High	115	136	180	115	140	180	140	168	205		
	D4 High	250	272	325	250	280	325	305	336	380		
	D5 High	505	544	620	515	560	620	620	672	740		
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D1	D0		D1	D0		D1	D0			7
t_{SKEW}	Duty Cycle Skew										ps	
	t_{PHL}–t_{PLH}		±30			±30			±30			1
t_s	Setup Time										ps	
	D to LEN	200	0		200	0		200	0			
	D to IN	800			800			800				2
	$\overline{EN}$ to IN	200			200			200				3
t_h	Hold Time										ps	
	LEN to D	500	250		500	250		500	250			
	IN to $\overline{EN}$	0			0			0				4
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300			300			300				5
	SET MAX to LEN	800			800			800				
	SET MIN to LEN	800			800			800				
t_{jit}	Jitter		<5.0			<5.0			<5.0		ps	8
t_r t_f	Output Rise/Fall Time										ps	
	20–80% (Q)	125	225	325	125	225	325	125	225	325		
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650		

1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
2. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set
3. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i e. increasing delay steps for increasing binary counts on the control inputs Dn) Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques

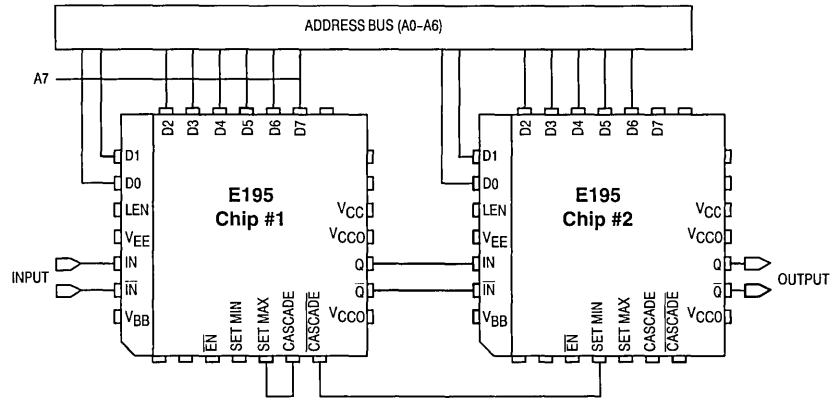


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E195's

To increase the programmable range of the E195 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195's without the need for any external gating. Furthermore this capability requires only one more address line per added E195. Obviously cascading multiple PDC's will result in a larger programmable range however this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195's. As can be seen, this scheme can easily be expanded for larger E195 chains. The D7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A0–A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E195 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0–A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0–A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices one simply needs to connect the D7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

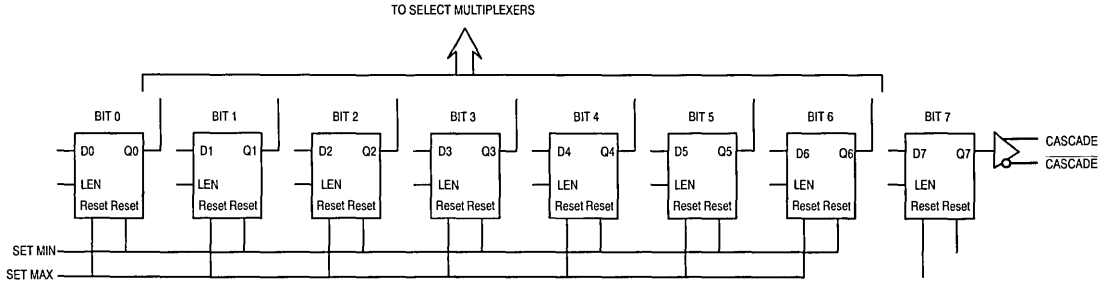


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

Programmable Delay Chip

MC10E196
MC100E196

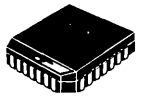
PROGRAMMABLE DELAY CHIP

The MC10E/100E196 is a programmable delay chip (PDC) designed primarily for very accurate differential ECL input edge placement applications.

The delay section consists of a chain of gates and a linear ramp delay adjust organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the E196 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

The FTUNE input takes an analog voltage and applies it to an internal linear ramp for reducing the 20 ps resolution still further. The FTUNE input is what differentiates the E196 from the E195.

An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.



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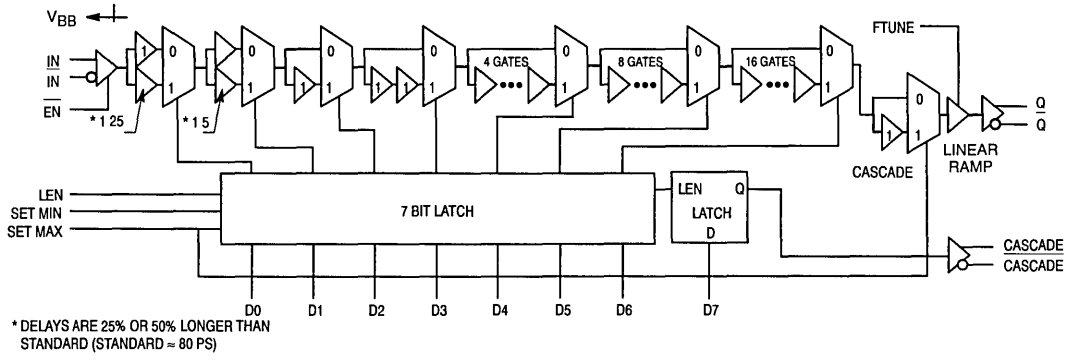
2

- 2.0ns Worst Case Delay Range
- ≈20ps/Delay Step Resolution
- Linear Input for Tighter Resolution
- >1.0GHz Bandwidth
- On Chip Cascade Circuitry
- Extended 100E V_{EE} Range of –4.2 to –5.46V
- 75KΩ Input Pulldown Resistors

PIN NAMES

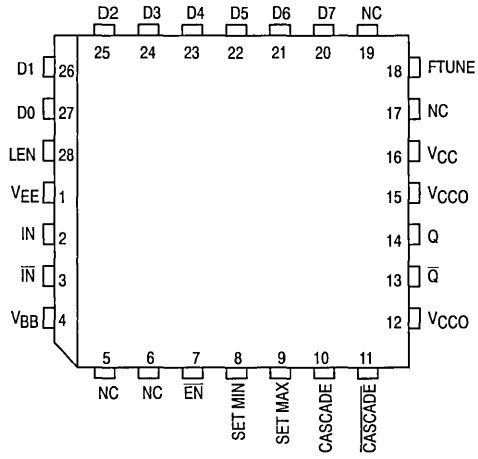
Pin	Function
IN/$\overline{IN}$	Signal Input
$\overline{EN}$	Input Enable
D[0:7]	Mux Select Inputs
Q/$\overline{Q}$	Signal Output
LEN	Latch Enable
SET MIN	Min Delay Set
SET MAX	Max Delay Set
CASCADE	Cascade Signal
FTUNE	Linear Voltage Input

LOGIC DIAGRAM – SIMPLIFIED



* DELAYS ARE 25% OR 50% LONGER THAN STANDARD (STANDARD ≈ 80 PS)

Pinout: 28-Lead PLCC (Top View)



2

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		130	156		130	156		130	156		
	100E		130	156		130	156		150	179		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Notes
t_{PLH} t_{PHL}	Propagation Delay										ps	
	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765		
	IN to Q, Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720		
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950		
	D7 to CASCADE	300	450	700	300	450	700	300	450	700		
t_{RANGE}	Programmable Range										ps	
	t_{PD} (max) – t_{PD} (min)	2000	2175		2050	2240		2375	2580			
Δt	Step Delay										ps	6
	D0 High		17			17.5			21			
	D1 High		34			35			42			
	D2 High	55	68	105	55	70	105	65	84	120		
	D3 High	115	136	180	115	140	180	140	168	205		
	D4 High	250	272	325	250	280	325	305	336	380		
	D5 High	505	544	620	515	560	620	620	672	740		
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450		
Lin	Linearity	D1	D0		D1	D0		D1	D0			7
t_{SKEW}	Duty Cycle Skew										ps	
	t_{PHL}–t_{PLH}		±30			±30			±30			1

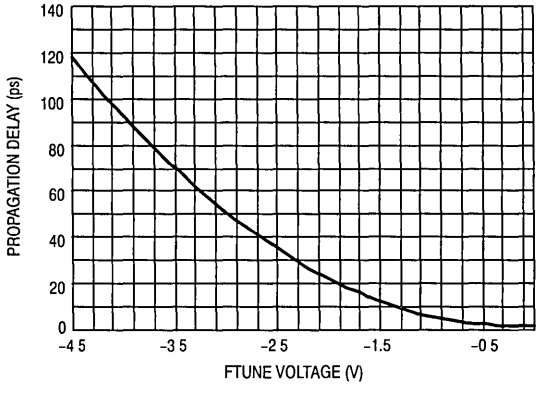
AC CHARACTERISTICS (continued) (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_S	Setup Time										ps	
	D to LEN	200	0		200	0		200	0			
	D to IN	800			800			800				2
	$\overline{EN}$ to IN	200			200			200				3
t_H	Hold Time										ps	
	LEN to D	500	250		500	250		500	250			
	IN to $\overline{EN}$	0			0			0				4
t_R	Release Time										ps	
	$\overline{EN}$ to IN	300			300			300				5
	SET MAX to LEN	800			800			800				
	SET MIN to LEN	800			800			800				
t_{jit}	Jitter		<5.0			<5 0			<5.0		ps	8
t_r	Output Rise/Fall Time										ps	
t_f	20–80% (Q)	125	225	325	125	225	325	125	225	325		
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650		

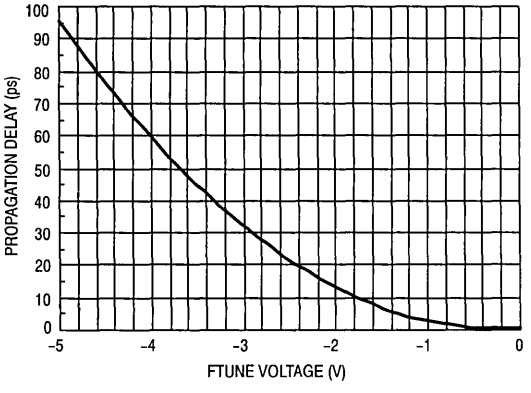
1. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output
2. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set
3. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition
4. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/IN transition.
5. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
6. Specification limits represent the amount of delay added with the assertion of each individual delay control pin The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
7. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation
8. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

ANALOG INPUT CHARACTERISTICS

Ftune = V_{CC} to V_{EE}



Propagation Delay versus Ftune Voltage (100E196)



Propagation Delay versus Ftune Voltage (10E196)

USING THE FTUNE ANALOG INPUT

The analog FTUNE pin on the E196 device is intended to enhance the 20 ps resolution capabilities of the fully digital E195. The level of resolution obtained is dependent on the number of increments applied to the appropriate range on the FTUNE pin.

To provide another level of resolution the FTUNE pin must be capable of adjusting the delay by greater than the 20 ps digital resolution. From the provided graphs one sees that this requirement is easily achieved as over the entire FTUNE voltage range a 100 ps delay can be achieved. This extra analog range ensures that the FTUNE pin will be capable even under worst case conditions of covering the digital resolution.Typically the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, the graphs provided should be used. As an example if a range of 40 ps is selected to cover worst case conditions and ensure coverage of the digital range, from the 100E196 graph a voltage range of –3.25 V to –4.0 V would be necessary on the FTUNE pin. Obviously there are numerous voltage ranges which can be used to cover a given delay range, users are given the flexibility to determine which one best fits their designs.

Cascading Multiple E196's

To increase the programmable range of the E195 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195's without the need for any external gating. Furthermore this capability requires only one more address line per added E195. Obviously cascading multiple PDC's will result in a larger programmable range, however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195's. As can be seen, this scheme can easily be expanded for larger E195 chains. The D7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A0–A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E195 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0–A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0–A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E195.

When cascading multiple PDC's it will prove more cost effective to use a single E196 for the MSB of the chain while using E195 for the lower order bits. This is due to the fact that only one fine tune input is needed to further reduce the delay step resolution.

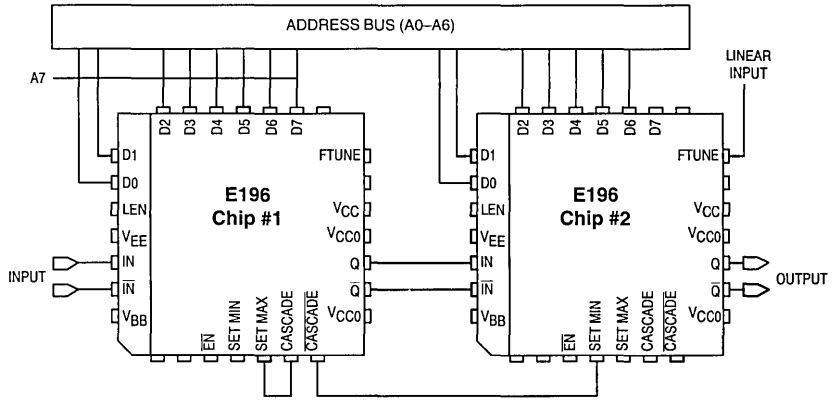


Figure 1. Cascading Interconnect Architecture

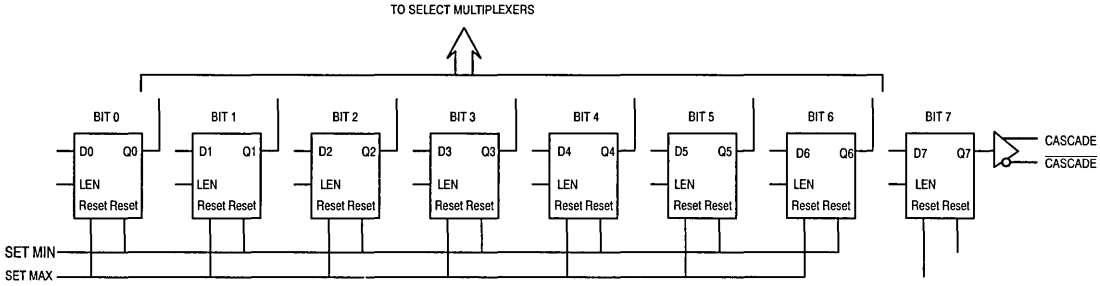


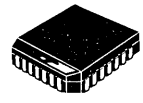
Figure 2. Expansion of the Latch Section of the E195 Block Diagram

Advanced Information

Data Separator

MC10E197

DATA SEPARATOR



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E197 is an integrated data separator designed for use in high speed hard disk drive applications. With data rate capabilities of up to 50Mb/s the device is ideally suited for today's and future state-of-the-art hard disk designs.

The E197 is typically driven by a pulse detector which reads the magnetic information from the storage disk and changes it into ECL pulses. The device is capable of operating on both 2:7 and 1:7 RLL coding schemes. Note that the E197 does not do any decoding but rather prepares the disk data for decoding by another device.

For applications with higher data rate needs, such as tape drive systems, the device accepts an external VCO. The frequency capability of the integrated VCO is the factor which limits the device to 50Mb/s.

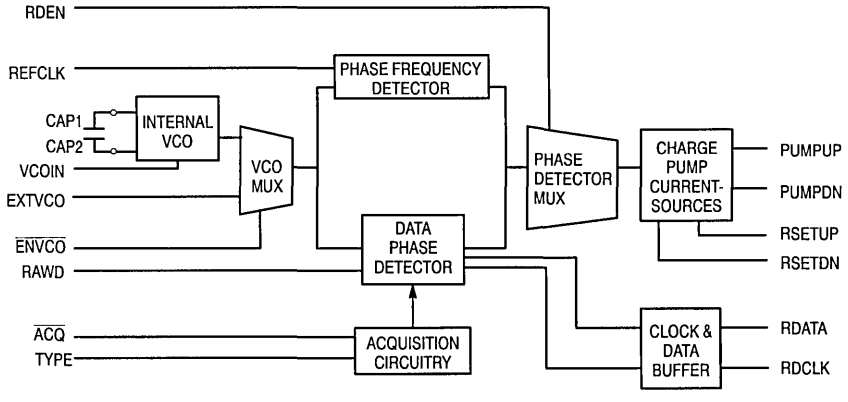
A special anti-equivocation circuit has been employed to ensure timely lock-up when the arriving data and VCO edges are coincident.

Unlike the majority of the devices in the ECLinPS family, the E197 is available in only 10H compatible ECL. The device is available in the standard 28-lead PLCC.

Since the E197 contains both analog and digital circuitry, separate supply and ground pins have been provided to minimize noise coupling inside the device. The device can operate on either standard negative ECL supplies or, as is more common, on positive voltage supplies.

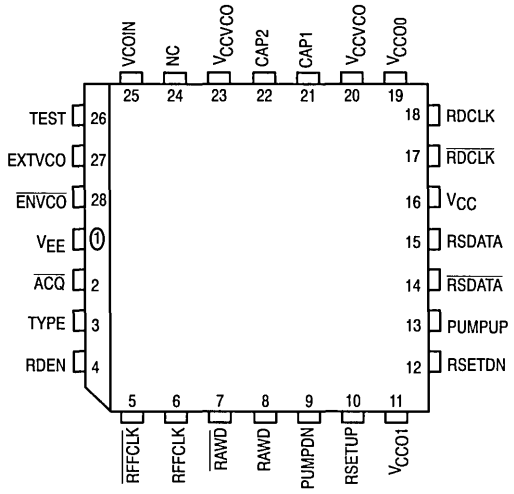
- 2:7 and 1:7 RLL Format Compatible
- Fully Integrated VCO for 50Mb/s Operation
- External VCO Input for Higher Operating Frequency
- Anti-equivocation Circuitry to Ensure PLL Lock

LOGIC DIAGRAM



This document contains information on a new product Specifications and information herein are subject to change without notice.

Pinout: 28-Lead PLCC (Top View)



2

PIN DESCRIPTIONS

REFCLK	Reference clock equivalent to one clock cycle per decoding window.
RDEN	Enable data synchronizer when HIGH When LOW enable the phase/frequency detector steered by REFCLK
RAWD	Data Input to Synchronizer logic.
VCOIN	VCO control voltage input
CAP1/CAP2	VCO frequency controlling capacitor inputs
ENVCO	VCO select pin. LOW selects the internal VCO and HIGH selects the external VCO input. Pin floats LOW when left open.
EXTVCO	External VCO pin selected when ENVCO is HIGH
ACQ	Acquisition circuitry select pin. This pin must be driven HIGH at the end of the data sync field for some sync field types.
TYPE	Selects between the two types of commonly used sync fields. When LOW it selects a sync field interspersed with 3 zeroes (2:7 RLL code). When HIGH it selects a sync field interspersed with 2 zeroes (1:7 RLL code).
TEST	Input included to initialize the clock flip-flop for test purposes only. Pin should be left open (LOW) in actual application.
PUMPUP	Open collector charge pump output for the signal pump
PUMPDN	Open collector charge pump output for the reference pump
RSETUP	Current setting resistor for the signal pump
RSETDN	Current setting resistor for the reference pump
RDATA	Synchronized data output
RDCLK	Synchronized clock output
V_{CC}, V_{CCO}, V_{CCVCO}	Most positive supply rails. Digital and analog supplies are independent on chip
V_{EE}, V_{EEVCO}	Most negative supply rails. Digital and analog supplies are independent on chip

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND or V_{CC} = 4.75V to 5.25V; V_{EE} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	1
I_{IL}	Input LOW Current	0.5			0.5			0 5			µA	1
I_{EE}	Power Supply Current	90	150	180	90	150	180	90	150	180	mA	
I_{SET}	Charge Pump Bias Current	0 5		5	0.5		5	0.5		5	mA	2
I_{OUT}	Charge Pump Output Leakage Current			1			1			1	µA	3
V_{ACT}	PUMPUP/PUMPDN Active Voltage Range	V_{CC} – 2.5		V_{CC}	V_{CC} – 2 5		V_{CC}	V_{CC} – 2.5		V_{CC}	V	

10H LOGIC LEVELS

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} + V_{CCO1} = V_{CCVCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{OH}	Output HIGH Voltage	–1020		– 840	– 980		– 810	– 910		– 720	mV	
V_{OL}	Output LOW Voltage	–1950		–1630	–1950		–1630	–1950		–1595	mV	
V_{IH}	Input HIGH Voltage	–1170		– 840	–1130		– 810	–1060		– 720	mV	
V_{IL}	Input LOW Voltage	–1950		–1480	–1950		–1480	–1950		–1445	mV	

POSITIVE EMITTER COUPLED LOGIC LEVELS

DC CHARACTERISTICS (V_{EE} = V_{EEVCO} = GND; V_{CC} = V_{CCO1} = V_{CCVCO} = +5 volts*)

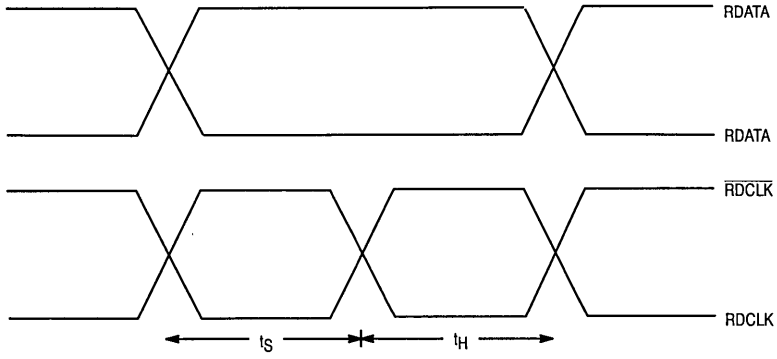
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{OH}	Output HIGH Voltage	3980		4160	4020		4190	4090		4280	mV	
V_{OL}	Output LOW Voltage	3050		3370	3050		3370	3050		3405	mV	
V_{IH}	Input HIGH Voltage	3830		4160	3870		4190	3940		4280	mV	
V_{IL}	Input LOW Voltage	3050		3520	3050		3050	3050		3555	mV	

*V_{OH} and V_{OL} levels will vary 1 1 with V_{CC}

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND or V_{CC} = 4.75V to 5.25V; V_{EE} = GND)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		min	max	min	max	min	max		
t_S	Time from RDATA Valid to Rising Edge of RDCLK	T_{VCO} – 550		T_{VCO} – 500		T_{VCO} – 500		ps	4,7
t_H	Time from Rising Edge of RDCLK to RDATA invalid	T_{VCO}		T_{VCO}		T_{VCO}		ps	4,7
t_{SKEW}	Skew Between RDATA and $\overline{RDATA}$		300		300		300	ps	
f_{VCO}	Frequency of the VCO	150		150		150		MHz	5
	Tuning Ratio	1.53	1.87	1.53	1 87	1.53	1 87		6

1. Applies to the input current for each input except VCOIN
2. For a nominal set current of 3.72mA, the resistor values for RSETUP and RSETDN should be 130Ω(0 1%) Assuming no variation between these two resistors, the current match between the PUMPUP and PUMPDN output signals should be within ±3% I_{SET} is calculated as (V_{EE}+ 1 3v – V_{BE})/R, where R is RSETUP or RSETDN and a nominal value for V_{BE} is 0 85 volts
3. Output leakage current of the PUMPUP or PUMPDN output signals when at a LOW level
4. T_{VCO} is the period of the VCO.
5. The VCO frequency determined with VCOIN = V_{EE} + 0 5 volts and using a 10pF tuning capacitor
6. The tuning ratio is defined as the ratio of f_{VCOMAX} to F_{VCOMIN} where f_{VCOMAX} is measured at VCOIN = 1 3V + V_{EE} and f_{VCOMAX} is measured at VCOIN = 2 6V + V_{EE}



SETUP AND HOLD TIMING DIAGRAMS

APPLICATIONS INFORMATION

General Operation

2

Operation

The E197 is a phase-locked loop circuit consisting of an internal VCO, a Data Phase detector with associated acquisition circuitry, and a Phase/Frequency detector (Figure 1). In addition, an enable pin(ENVCO) is provided to disable the internal VCO and enable the external VCO input. Hence, the user has the option of supplying the VCO signal.

The E197 contains two phase detectors: a data phase detector for synchronizing to the non-periodic pulses in the read data stream during the data read mode of operation, and a phase/frequency detector for frequency (and phase) locking to an external reference clock during the "idle" mode of operation. The read enable (RDEN) pin muxes between these two detectors.

Data Read Mode

The data pins (RAWD) are enabled when the RDEN pin is placed at a logic high level, thus enabling the Data Phase detector (Figure1) and initiating the data read mode. In this mode, the loop is servoed by the timing information taken from the positive edges of the input data pulses. This phase detector samples positive edges from the RAWD signal and generates both a pump up and pump down pulse from any edge of the input data pulse. The leading edge of the pump up pulse is time modulated by the leading edge of the data signal, whereas the rising edge of the pump up pulse is generated synchronous to the VCO clock. The falling edge of the pump down pulse is synchronous to the falling edge of the VCO clock and the rising edge of the pump down signal is synchronous to the rising edge of the VCO clock. Since both edges of the VCO are used the internal clock a duty cycle of 50%. This pulse width modulation technique is used to generate the servoing signal which drives the VCO. The pump down signal is a reference pulse which is included to provide an evenly balanced differential system, thereby allowing the synthesis of a VCO input control signal after appropriate signal processing by the loop filter.

By using suitable external filter circuitry, a control signal for input into the VCO can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when the data edges lead the clock by a half clock cycle. If the data edges are advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a negative polarity; whereas if the VCO is advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a positive polarity. If there is no data edge present at the RAWD input, the corresponding pump up and pump down outputs are not generated and the resulting control output is zero.

Acquisition Circuitry

The acquisition circuitry is provided to assist the data phase detector in phase locking to the sync field that precedes the data. For the case in which lock-up is attempted when the data edges are coincident with the VCO edges, the pump down signal may enter an indeterminate state for an unacceptably long period due to the violation of internal set up and hold times. After an initial pump down pulse, the circuit blocks successive pump down pulses, and inserts extra pump up pulses, during portions of the sync field that are known to contain zeros. Thus, the data phase detector is forced to have a nonzero output during the lock-up period, and the restoring force ensures correction of the loop within an acceptable time. Hence, this circuitry provides a quasi-deterministic pump down output signal, under the condition of coincident data and VCO edges, allowing lock-up to occur with excessive delays.

The $\overline{ACQ}$ line is provided to disable (disable = HIGH) the acquisition circuit during the data portion of a sector block. Typically, this circuit is enabled at the beginning of the sync field by a one-shot timer to ensure a timely lock-up.

The TYPE line allows the choice between two sync field preamble types; transitions interspersed with two zeros

between transitions. These types of sync fields are used with the 1:7 and 2:7 coding schemes, respectively.

Idle Mode

In the absence of data or when the drive is writing to the disk, PLL servoing is accomplished by pulling the read enable line (RDEN) low and providing a reference clock via the REFCLK pins. The condition whereby RDEN is low selects the Phase/Frequency detector (Figure 1) and the 10E197 is said to be operating in the "idle mode". In order to function as a frequency detector the input waveform must be periodic. The pump up and pump down pulses from the Phase/Frequency detector will have the same frequency, phase and pulse width only when the two clocks that are being compared have their positive edges aligned and are of the same frequency.

As with the data phase detector, by using suitable external filter circuitry, a VCO input control signal can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when all positive edges of both clocks are coincident. For the case in which the frequencies of the two clocks are the same but the clock edges of the reference clock are slightly advanced with respect to the VCO clock, the control clock is defined to have a positive polarity. A control signal with negative polarity occurs when the edges of the reference clock are delayed with respect to those of the VCO. If the frequencies of the two clocks are different, the clock with the most edges per unit time will initiate the most pulses and the polarity of the detector will reflect the frequency error. Thus, when the reference clock is high in frequency than the VCO clock the polarity of the control signal is positive; whereas a control signal with negative polarity occurs when the frequency of the reference clock is lower than the VCO clock.

Phase-Lock Loop Theory

2

Introduction

Phase lock loop (PLL) circuits are fundamentally feedback systems used to synchronize the frequency of an oscillator to an incoming signal. In addition to frequency synchronization, the PLL circuitry is designed to minimize the phase difference between the system input and output signals. A block diagram of a feedback control system is shown in Figure 1.

where:

A(s) is the product of the feed-forward transfer functions.

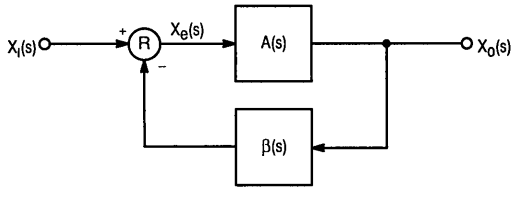


Figure 1. Feedback System

β(s) is the product of the feedback transfer functions.

The transfer function for this closed loop system is

$$\frac{X_O(s)}{X_i(s)} = \frac{A(s)}{1 + A(s)\beta(s)}$$

Typically, phase lock loops are modeled as feedback systems connected in a unity feedback configuration (β(s)=1) with a phase detector, a VCO (voltage controlled oscillator), and a loop filter in the feed-forward path, A(s). Figure 2 illustrates a phase lock loop as a feedback control system in block diagram form.

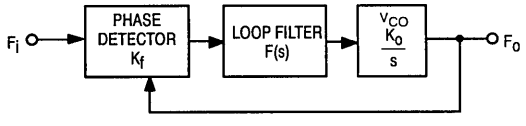


Figure 2. Phase Lock Loop Block Diagram

The closed loop transfer function is:

$$\frac{X_O(s)}{X_i(s)} = \frac{K_\phi \frac{K_O}{s} F(s)}{1 + K_\phi \frac{K_O}{s} F(s)}$$

where:

K_ϕ= the phase detector gain.
K_O= the VCO gain. Since the VCO introduces a pole at the origin of the s-plane, K_O is divided by s.
F(s) = the transfer function of the loop filter.

The 10E197 is designed to implement the phase detector and VCO functions in a unity feedback loop, while allowing the user to select the desired filter function.

Gain Constants

As mentioned, each of the three sections in the phase lock loop block diagram has an associated open loop gain constant. Further, the gain constant of the filter circuitry is composed of the product of three gain constants, one for each filter subsection. The open loop gain constant of the feed-forward path is given by

$$K_{ol} = K_\phi * K_o * K_1 * K_l * K_d$$

eqt. 1

and obtained by performing a root locus analysis.

Phase Detector Gain Constant

The gain of the phase detector is a function of the operating mode and the data pattern. The 10E197 provides data separation for signals encoded in 2:7 or 1:7 RLL encoding schemes; hence, Tables 1 and 2 are coding tables for these schemes. Table 3 lists nominal phase detector gains for both 2:7 and 1:7 sync fields.

NRZ Data Sequence	Code Sequence
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Table 1. 2:7 RLL Encoding Table

NRZ Data Sequence	Code Sequence
00	X01
01	010
10	X00
1100	010001
1101	X00000
1110	X00001
1111	010000

An X in the leading bit of a code sequence is assigned the complement of the bit

Table 2. 1:7 RLL Encoding Table

Sync Pattern	Read Mode	Idle Mode
2:7	121 mV/radian	484 mV/radian
1:7	161 mV/radian	483 mV/radian

Table 3. Phase Detector Gain Constants

VCO Gain Constant

The gain of the VCO is a function of the tuning capacitor. For a value of 10pF a nominal value of the gain, K_o, is 20MHz per volt.

Filter Circuitry Gain Constant(s)

The open loop gain constant of the filter circuitry is given by:

$$K_{fc} = K_1 * K_l * K_d \qquad \text{eqt. 2}$$

The individual gain constants are defined in the appropriate subsections of this document.

Loop Filter

The two major functions of the loop filter are to remove any noise or high frequency components present in the phase detector output signal and, more importantly, to control the characteristics which determine the dynamic response of the phase lock loop; i.e. capture range, loop bandwidth, capture time, and transient response.

Although a variety of loop filter configurations exist, this section will only describe a filter capable of performing the signal processing as described in the Data Read Mode and the Idle Mode sections. The loop filter consists of a differential summing amplifier cascaded with an augmenting integrator which drives the VCOIN input to the 10E197 through a resistor divider network (Figure 3).

The transfer function and the element values for the loop filter are derived by dividing the filter into three cascaded subsections: filter input, augmenting integrator, and the voltage divider network (Figure4).

Loop Filter Transfer Function

The open loop transfer function of the phase lock loop is the product of each individual filter subsection, as well as the phase detector and VCO. Thus, the open loop filter transfer function is:

$$F_o(s) = K_\phi * \frac{K_o}{s} * F_1(s) * F_l(s) * F_d(s)$$

where:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{01})\, s + \omega_{01}^2]}$$

$$F_l(s) = K_l * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{02})\, s + \omega_{02}^2]}$$

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

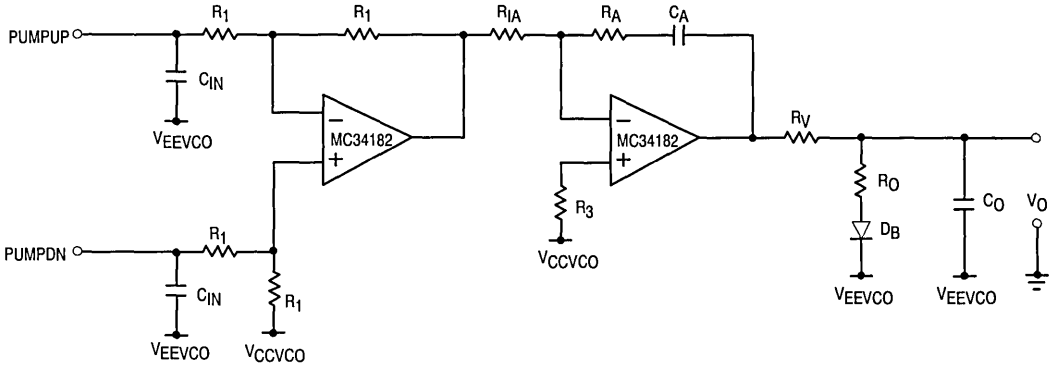


Figure 3. Loop Filter Circuitry

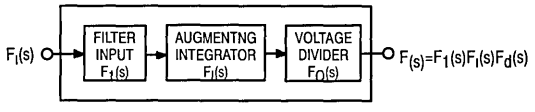


Figure 4. Loop Filter Block Diagram

A root locus analysis is performed on the open loop transfer function to determine the final pole-zero locations and the open loop gain constant for the phase lock loop. Note that the open loop gain constant impacts the crossover frequency and that a lower frequency crossover point means a much more efficient filter. Once these positions and constants are determined the component values may be calculated.

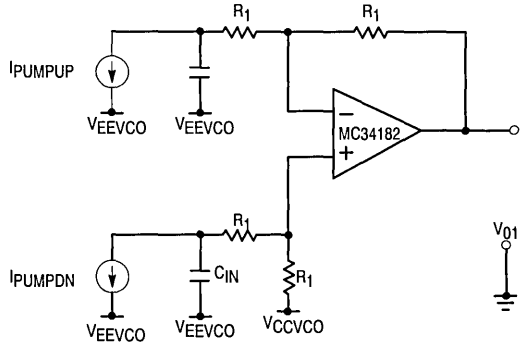


Figure 5. Filter Input Sunsection

Filter Input

The primary function of the filter input subsection is to convert the output of the phase detector into a single ended signal for subsequent processing by the integrator circuitry. This subsection consists of the 10E197 charge pump current sinks, two shunt capacitors, and a differential summing amplifier (Figure 5).

Hence, this portion of the filter circuit contributes a real pole and two complex poles to the overall loop transfer function F(s). Before these pole locations are selected, appropriate values for the current setting resistors (RSETUP and RSETDN) must be ascertained. The goal in choosing these resistor values is to maximize the gain of the filter input subsection while ensuring the charge pump output transistors operate in the active mode. The filter input gain is maximized for a charge pump current of 1.1mA; a value of 464Ω for both RSETUP and RSETDN yields a nominal charge pump current of 1.1mA.

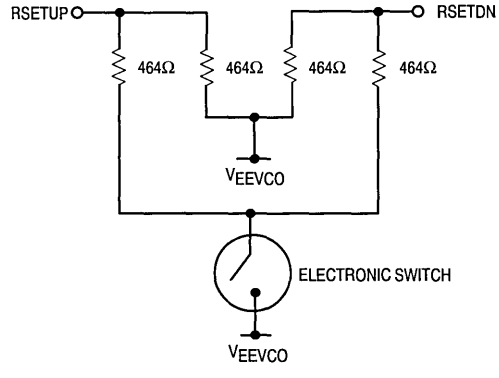


Figure 6. Dual Bandwidth Current Source Implementation

It should be noted that a dual bandwidth implementation of the phase lock loop may be achieved by modifying the current setting resistors such that an electronic switch enables one of two resistor configurations. Figure 6 shows a circuit configuration capable of providing this dual bandwidth function. Analysis of the filter input circuitry yields the transfer function:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{01})\, s + \omega_{01}^2]}$$

The gain constant is defined as:

$$K_1 = A_1 * \frac{1}{C_{IN}} \qquad \text{eqt. 3}$$

where:

A_1= op-amp gain constant for the selected pole positions.

C_{IN} = phase detector shunt capacitor.

The real pole is a function of the input resistance to the op-amp and the shunt capacitors connected to the phase detector output. For stability the real pole must be placed beyond the unity gain frequency; hence, this pole is typically placed midway between the unity crossover and phase detector sampling frequency, which should be about ten times greater.

The second order pole set arises from the two pole model for an op-amp. The open loop gain and the first open loop pole for the op-amp are obtained from the data sheets. Typically, op-amp manufacturers do not provide information on the location of the second open loop pole; however, it can be approximated by measuring the roll off of the op-amp in the open loop configuration. The second pole is located where the gain begins to decrease at a rate of 40dB per decade. The inclusion of both poles in the differential summing amplifier transfer function becomes important when closing the feedback path around the op-amp because the poles migrate; and this migration must be accounted for to accurately determine the phase lock loop transient performance.

Typically the op-amp poles can be approximated by a pole pair occurring as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane. Two constraints on the selection of the op-amp pole pair are that the poles lie beyond the crossover frequency and they are positioned for near unity gain operation. Performing a root locus analysis on the op-amp open loop configuration and adhering to the two constraints yields the pole positions contributed by the op-amp.

Determination of Element Values

Since the difference amplifier is configured to operate as a differential summer the resistor values associated with the amplifier are of equal value. Further, the typical input resistance to the summing amplifier is 1kΩ; thus, the op-amp resistors are set at 1 kΩ. Having set the input resistance to the op-amp and selected the position of the real pole, the value of the shunt capacitors is determined using the following relationship:

$$|p_1| = \frac{1}{2\pi R_1 C_{IN}} \qquad \text{eqt. 4}$$

Augmenting Integrator

The augmenting integrator consists of an active filter with a lag-lead network in the feedback path (Figure 7).

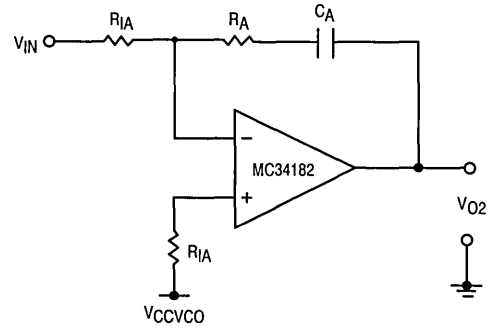


Figure 7. Integrator Subsection

Analysis of this portion of the filter circuit yields the transfer function:

$$F_1(s) = K_I * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{02})\, s + \omega_{02}^2]}$$

The gain constant is defined as:

$$K_I = A_I * \frac{R_A}{R_{IA}} \qquad \text{eqt. 5}$$

where:

A_I = op-amp gain constant for selected pole positions.

R_A = integrator feedback resistor.

R_{IA} = integrator input resistor.

The integrator circuit introduces a zero, a pole at the origin, and a second order pole set as described by the two pole model for an op-amp. As in the case of the differential summing amplifier, we assume the op-amp pole pair occur as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane; are positioned for near unity gain operation; and are located beyond the crossover frequency. Since both the summing and integrating op-amps are realized by the same type of op-amp (MC34182D), the open loop pole positions for both amplifiers will be the same.

Further, the loop transfer function contains two poles located at the origin, one introduced by the integrator and the other by the VCO; hence a zero is necessary to compensate for the phase shift produced by these poles and ensure loop stability. The op-amp will be stable if the crossover point occurs before the transfer function phase angle becomes 180°. The zero should be positioned much less than one decade before the unity gain frequency.

As in the case of the filter input circuitry, the poles and zero from this analysis will be used as open loop poles and a zero when performing the root locus analysis for the complete system.

Determination of Element Values

The location of the zero is used to determine the element values for the augmenting integrator. The value of the capacitor, C_A, is selected to provide adequate charge storage when the loop is not sampling data. A value of 0.1μF is sufficient for most applications; this value may be increased when the RDCLK frequency is much lower than 4 MHz. The value of R_A is governed by:

$$|z| = \frac{1}{2\pi R_A C_A} \qquad \text{eqt. 6}$$

For unity gain operation of the integrating op-amp the value of RIA is selected such that:

$$R_{IA} = R_A \qquad \text{eqt. 7}$$

It should be noted that although the zero can be tuned by varying either R_A or C_A, caution must be exercised when adjusting the zero by varying C_A because the integrator gain is also a function of C_A. Further, the gain of the loop filter can be adjusted by changing the integrator input resistor R_{IA}.

Voltage Divider

The input range to the VCOIN input is from 1.3V + V_{EE} to 2.6V + V_{EE}; hence, the output from the augmenting amplifier section must be attenuated to meet the VCOIN constraints. A simple voltage divider network provides the necessary attenuation (Figure 8).

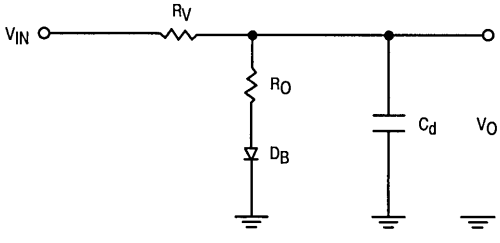


Figure 8. Voltage Divider Subsection

In addition, a shunt filter capacitor connected between the VCOIN input pin and V_{EE} provides the voltage divider subsection with a single time constant transfer function that adds a pole to the overall loop filter. The transfer function for the voltage divider network is:

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

The gain constant, K_d, is defined as:

$$K_d = \frac{1}{R_V C_d} \qquad \text{eqt. 9}$$

The value of K_d is easily extracted by rearranging Equation 1:

$$K_d = \frac{K_{OI}}{K_\phi * K_O * K_1 * K_I} \qquad \text{eqt. 10}$$

The gain constant K_d is set such that the output from the integrator circuit is within the range 1.3V +V_{EE} to 2.6V +V_{EE}. The pole for the voltage divider network should be positioned an octave beyond that for the filter input.

Determination of Element Values

Once the pole location and the gain constant K_d are established the resistor values for the voltage divider network are determined using the design guidelines mentioned above and from the following relationship:

$$\frac{K_d}{2\pi|p_2|} = \frac{R_O}{R_O + R_V}$$

Having determined the resistor values, the filter capacitor is calculated by rearranging Equation 9:

$$C_d = \frac{1}{R_V K_d} \qquad \text{eqt. 9a}$$

Finally, a bias diode is included in the voltage divider network to provide temperature compensation. The finite resistance of this diode is neglected for these calculations.

Calculations For a 2:7 Coding Scheme

Introduction

The circuit component values are calculated for a 2:7 coding scheme employing a data rate of 23Mbit/sec. Since the number of bits is doubled when the data is encoded, the data clock is at half the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 46MHz. Further, the pole and zero positions are a function of the data rate; hence, the component values derived by these calculations must be scaled if a different operating frequency is used. Finally, it should be noted that the values are optimized for settling time.

The analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning. Dynamic poles and zeros are those which the designer may position, to yield the desired dynamic response, through the judicious choice of element values. Static poles are not directly controlled by the choice of component values.

2

Static Poles

Each op-amp introduces a pair of "static" complex conjugate poles which must lie beyond the crossover frequency. As obtained from the data sheets and laboratory measurements, the two open loop poles for the MC34182D are:

$$P^*_{1a} = -0.1\text{Hz}$$

$$P^*_{1b} = -11.2\text{Hz}$$

Performing a root locus analysis and following the two guidelines previously stated, an acceptable pole set is:

$$P_{1a} = -5.65 + j5.65\text{MHz}$$

$$P_{1b} = -5.65 - j5.65\text{MHz}$$

Both op-amps introduce a set of static complex conjugate poles at these positions for a total of four poles. Further, the loop gain for each op-amp associated with these pole positions is determined from the root locus analysis to be:

$$A_1 = A_2 = 2.48\ e15\frac{V}{V}$$

In addition to the op-amps, the integrator and the VCO each contribute a static pole at the origin. Thus, there are a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.24\text{MHz}$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus the open loop voltage divider pole position is picked to be:

$$P^*_2 = -2.57\text{MHz}$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311\text{Hz}$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -573\text{kHz}$$

$$P_2 = -3.06\text{MHz}$$

$$z = -311\text{Hz}$$

Filter Input Subsection

Rearranging Equation 4:

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 573 kHz for the pole position and 1 kΩ for the resistor value yields:

$$C_{IN} = 278\text{ pF}$$

Augmenting Integrator Subsection

Rearranging Equation 6:

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311Hz for the zero position and 0.1μF for the capacitor value yields:

$$R_A = 5.11k\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11k\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3V + V_{EE} to 2.6V + V_{EE}.
Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.585\ e51 \frac{V}{mA\ sec^3}$$

From Equation 3

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1 is:

$$K_1 = 8.90\ e21 \frac{V}{mA\ sec}$$

From Equation 5

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant K_I is:

$$K_I = 2.48\ e15 \frac{V}{V}$$

Having determined the gain constant K_d, the value of R_V, is selected such that the constraints $R_V > R_O$ and:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_O}{R_O + R_V}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -3.06MHz$$

Hence, R_V is selected to be:

$$R_V = 2.15k\Omega$$

and R_O is calculated to be:

$$R_O = 700\Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_V K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is:

$$C_d = 98pF$$

Note that the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 23 Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations are provided to facilitate scaling and were derived with the assumptions that a 2:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock.

$$C_{IN} = 278 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 11}$$

$$C_d = 98 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 12}$$

where f is the RDCLK frequency in MHz.

Example for an 11 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 2:7 code are used but the data rate is 11Mbit/sec. The dynamic pole positions, and therefore the bandwidth of the loop filter, are a function of the data rate. Thus a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 11 the value of C_{IN} is:

$$C_{IN} = 581pF$$

and from Equation 12 the value of C_d is:

$$C_d = 205pF$$

Thus the element values for the filter are:

Filter Input Subsection:

$$C_{IN} = 581pF$$

$$R_1 = 1k\Omega$$

Integrator Subsection:

$$C_A = 0.1\mu F$$

$$R_A = 5.11k\Omega$$

$$R_{IA} = 5.11k\Omega$$

Voltage Divider Subsection:

$$C_d = 205pF$$

$$R_V = 2.15k\Omega$$

$$R_O = 700k\Omega$$

Note, the poles P_1 and P_2 are now located at:

$$P_1 = -274kHz$$

$$P_2 = -1.47MHz$$

And, the open loop filter unity crossover point is at 300kHz. The gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic 2 performance of the filter.

Calculations For a 1:7 Coding Scheme

Introduction

The circuit component values are calculated for a 1:7 coding scheme employing a data rate of 20Mbit/sec. Since the number of bits increases from two to three when the data is encoded, the data clock is at two-thirds the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 30MHz. As in the case of the 2:7 coding scheme the pole and zero positions are a function of the data rate, hence the component values derived by these calculations must be scaled if a different operating frequency is used.

Again, the analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning.

Static Poles

As in the 2:7 coding example, an MC34182D op-amp is employed, hence the pole set is:

$$P_{1a} = -5.65 + j5.65MHz$$

$$P_{1b} = -5.65 - j5.65MHz$$

and the open loop gain is:

$$A_I = A_2 = 2.48\ e15\ \frac{V}{V}$$

Since the op-amps introduce a set of complex conjugate poles, a total of four poles are introduced by the op-amp. In addition, the integrator and the VCO each contribute a pole at the origin for a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.1MHz$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus, the open loop voltage divider pole position is selected as:

$$P^*_2 = -2.28MHz$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311Hz$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -541kHz$$

$$P_2 = -2.73MHz$$

$$z = -311Hz$$

Filter Input Subsection

Rearranging Equation 4

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 541kHz for the pole position and 1.0kΩ for the resistor value yields:

$$C_{IN} = 294\ pF$$

Augmenting Integrator Subsection

Rearranging Equation 6

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311Hz for the zero position and 0.1μF for the capacitor value yields:

$$R_A = 5.11k\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11k\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3V + V_{EE} to 2.6V + V_{EE}.
Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.258\ e51 \frac{V}{\frac{MA}{SEC^3}}$$

From Equation 3:

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1:

$$K_1 = 8.42\ e21 \frac{V}{mA\ sec}$$

From Equation 5:

$$K_I = A_I * \frac{R_A}{R_{IA}}$$

and the gain constant K_I is:

$$K_I = 2.48\ e15 \frac{V}{V}$$

$$K_d = 2.98\ e6\ sec^{-1}$$

Having determined the gain constant K_d, the value of R_v, is selected such that the constraints $R_v > R_o$ and:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_o}{R_o + R_v}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -2.73MHz$$

Hence, R_v is selected to be:

$$R_v = 2.15k\Omega$$

and R_o is calculated to be:

$$R_o = 453\Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is calculated to be:

$$C_d = 156pF$$

Again, note the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 20Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations provided are to facilitate scaling and were derived with the assumptions that a 1:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock:

$$C_{IN} = 294 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 13}$$

$$C_d = 156 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 14}$$

where f is the RDCLK frequency in MHz.

Example for an 10 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 1:7 code are used but the data rate is 10Mbit/sec. The dynamic pole positions and, therefore, the bandwidth of the loop filter, are a function of the data rate. Thus, a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 13 the value of C_{IN} is:

$$C_{IN} = 588pF$$

and from Equation 14 the value of C_d is:

$$C_d = 312pF$$

Thus, the element values for the filter are:

Filter Input Subsection:

$$C_{IN} = 588pF$$

$$R_1 = 1.0k\Omega$$

Integrator Subsection:

$$C_A = 0.1\mu F$$

$$R_A = 5.11k\Omega$$

$$R_{IA} = 5.11k\Omega$$

Voltage Divider Subsection:

$C_d = 312pF$

$R_V = 2.15k\Omega$

$R_O = 453k\Omega$

Note, the poles P_1 and P_2 are now located at:

$P_1 = -271kHz$

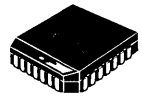
$P_2 = -1.36MHz$

And, the open loop filter unity crossover point is at 300kHz. As in the case of the 2:7 coding scheme, the gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic performance of the filter.

1:6 Differential Clock Distribution Chip

MC10E211
MC100E211

1:6 DIFFERENTIAL CLOCK DISTRIBUTION CHIP



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E/100E211 is a low skew 1:6 fanout device designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal (PECL is an acronym for Positive ECL, PECL levels are ECL levels referenced to +5V rather than ground). If a single-ended input is to be used the V_{BB} pin should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} supply is designed to act as the switching reference for the input of the E211 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

- Guaranteed Low Skew Specification
- Synchronous Enabling/Disabling
- Multiplexed Clock Inputs
- V_{BB} Output for Single-Ended Use
- Internal 75kΩ Input Pulldown Resistors
- Common and Individual Enable/Disable Control
- High Bandwidth Output Transistors
- Extended 100E V_{EE} Range of –4.2V to –5.46V

2

The E211 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open in which case it will be pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

Both a common enable and individual output enables are provided. When asserted the positive output will go LOW on the next negative transition of the CLK (or SCLK) input. The enabling function is synchronous so that the outputs will only be enabled/disabled when the outputs are already in the LOW state. In this way the problem of runt pulse generation during the disable operation is avoided. Note that the internal flip flop is clocked on the falling edge of the input clock edge, therefore all associated specifications are referenced to the negative edge of the CLK input.

The output transitions of the E211 are faster than the standard ECLinPS™ edge rates. This feature provides a means of distributing higher frequency signals than capable with the E111 device. Because of these edge rates and the tight skew limits guaranteed in the specification, there are certain termination guidelines which must be followed. For more details on the recommended termination schemes please refer to the applications information section of this data sheet.

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{ENx}$	Q
H/L	X	L	L	CLK
X	H/L	H	L	SCLK
Z*	Z*	X	H	L

* Z = Negative transition of CLK or SCLK

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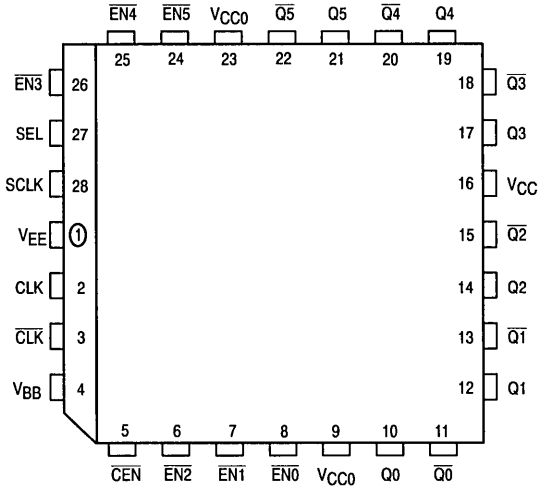
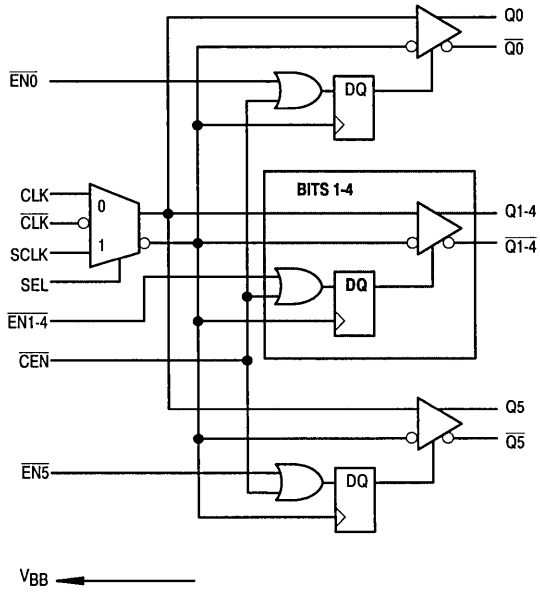


Pinout: 28-Lead PLCC (Top View)



Logic Diagram

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Output Reference Voltage	V_{BB}										V	
10E		–1.38		–1.27	–1.35		–1.25	–1.31		–1.19		
100E		–1.38		–1.26	–1.38		–1.26	–1.38		–1 26		
Input High Current	I_{IH}			150			150			150	µA	
Power Supply Current	I_{EE}										mA	
10E			119	142		119	142		119	142		
100E			119	142		119	142		137	164		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Characteristic	Symbol	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Propagation Delay to Output	t_{PLH}										ps	
CLK to Q (Diff)	t_{PHL}	795	930	1065	805	940	1075	825	960	1095		
CLK to Q (SE)		745	930	1115	755	940	1125	775	960	1145		
SCLK to Q		715	900	1085	725	910	1095	745	930	1115		
SEL to Q		745	970	1195	755	980	1205	775	1000	1225		
Disable Time	t_{PHL}										ps	
CLK or SCLK to Q			600	800		600	800		600	800		2
Part–to–Part Skew	t_{skew}										ps	
CLK (Diff) to Q				270			270			270		
CLK (SE), SCLK to Q				370			370			370		
Within-Device Skew			50	75		50	75			75		1
Setup Time	t_s										ps	
$\overline{EN}$x to CLK		100	–100		100	–100		100	–100			
$\overline{CEN}$ to CLK		200	0		200	0		200	0			2
Hold Time	t_h										ps	
CLK to $\overline{EN}$x, $\overline{CEN}$		300	100		300	100		300	100			2
Minimum Input Swing (CLK)	V_{PP}	0.25		1.0	0.25		1.0	0.25		1.0	V	3
Com. Mode Range (CLK)	V_{CMR}	–0.4		Note	–0.4		Note	–0.4		Note	V	4
Rise/Fall Times	t_r										ps	
20 – 80%	t_f	150		400	150		400	150		400		

1. Within-Device skew is defined for identical transitions on similar paths through a device.
2. Setup, Hold and Disable times are all relative to a falling edge on CLK or SCLK.
3 Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.
4. The range in which the high level of the input swing must fall while meeting the V_{PP} spec. The lower end of the range is V_{EE} dependant and can be calculated as V_{EE} + 2.4V.

2

APPLICATIONS INFORMATION

General Description

The MC10E/100E211 is a 1:6 fanout tree designed explicitly for low skew high speed clock distribution. The device was targeted to work in conjunction with the E111 device to provide another level of flexibility in the design and implementation of clock distribution trees. The individual synchronous enable controls and multiplexed clock inputs make the device ideal as the first level distribution unit in a distribution tree. The device provides the ability to distribute a lower speed scan or test clock along with the high speed system clock to ease the design of system diagnostics and self test procedures. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Because of lower fanout and larger skews the E211 will not likely be used as an alternative to the E111 for the bulk of the clock fanout generation. Figure 1 shows a typical application combining the two devices to take advantage of the strengths of each.

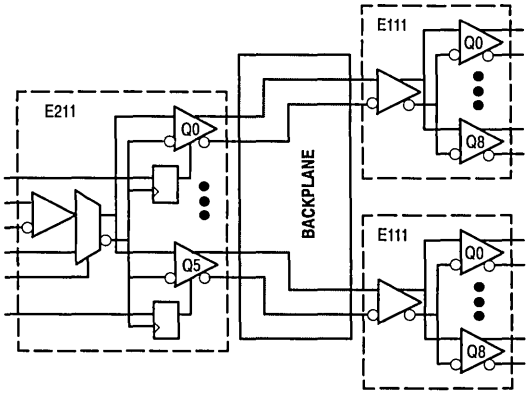


Figure 1. Standard E211 Application

Using the E211 in PECL Designs

The E211 device can be utilized very effectively in designs utilizing only a +5V power supply. Since the internal switching reference levels are biased off of the V_{CC} supply the input thresholds for the single-ended inputs will vary with V_{CC}. As a result the single-ended inputs should be driven by a device on the same board as the E211. Driving these inputs across a backplane where significant differences between the V_{CC}'s of the transmitter and receiver can occur can lead to AC performance and/or significant noise margin degradations. Because the differential I/O does not use a switching reference, and due to the CMR range of the E211, even under worst case V_{CC} situations between cards there will be no AC performance or noise margin loss for the differential CLK inputs.

For situations where TTL clocks are required the E211 can be interfaced with the H641 or H643 ECL to TTL Clock Distribution Chips from Motorola. The H641 is a single supply 1:9 PECL to TTL device while the H643 is a 1:8 dual supply standard ECL to TTL device. By combining the superior skew performance of the E211, or E111, with the low skew translating capabilities of the H641 and H643 very low skew TTL clock distribution networks can be realized.

Handling Open Inputs and Outputs

All of the input pins of the E211 have a 50kΩ to 75kΩ pulldown resistor to pull the input to V_{EE} when left open. This feature can cause a problem if the differential clock inputs are left open as the input gate current source transistor will become saturated. Under these conditions the outputs of the CLK input buffer will go to an undefined state. It is recommended, if possible,that the SCLK input should be selected any time the differential CLK inputs are allowed to float. The SCLK buffer, under open input conditions, will maintain a defined output state and thus the Q outputs of the device will be in a defined state (Q = LOW). Note that if all of the inputs are left open the differential CLK input will be selected and the state of the Q outputs will be undefined.

With the simultaneous switching characteristics and the tight skew specifications of the E211 the handling of the unused outputs becomes critical. To minimize the noise generated on the die all outputs should be terminated in pairs, ie. both the true and compliment outputs should be terminated even if only one of the outputs will be used in the system. With both complimentary pairs terminated the current in the V_{CC} pins will remain essentially constant and thus inductance induced voltage glitches on V_{CC} will not occur. V_{CC} glitches will result in distorted output waveforms and degradations in the skew performance of the device.

The package parasitics of the 28-lead PLCC cause the signals on a given pin to be influenced by signals on adjacent pins. The E211 is characterized and tested with all of the outputs switching, therefore the numbers in the data book are guaranteed only for this situation. If all of the outputs of the E211 are not needed and there is a desire to save power the unused output pairs can be left unterminated. Unterminated outputs can influence the propagation delay on adjacent pins by 15ps - 20ps. Therefore under these conditions this 15ps - 20ps needs to be added to the overall skew of the device. Pins which are separated by a package corner are not considered adjacent pins in the context of propagation delay influence. Therefore as long as all of the outputs on a single side of the package are terminated the specification limits in the data sheet will apply.

APPLICATIONS INFORMATION

Differential versus Single-Ended Use

As can be seen from the data sheet, to minimize the skew of the E211 the device must be used in the differential mode. In the single-ended mode the propagation delays are dependent on the relative position of the V_{BB} switching reference. Any V_{BB} offset from the center of the input swing will add delay to either the T_{PLH} or T_{PHL} and subtract delay from the other. This increase and decrease in delay will lead to an increase in the duty cycle skew and thus part-to-part skew. The within-device skew will be independent of the V_{BB} and therefore will be the same regardless of whether the device is driven differentially or single-endedly.

For applications where part-to-part skew or duty cycle skew are not important the advantages of single-ended clock distribution may lead to its use. Using single-ended interconnect will reduce the number of signal traces to be routed, but remember that all of the complimentary outputs still need to be terminated therefore there will be no reduction in the termination components required. To use the E211 with a single-ended input the arrangement pictured in Figure 2b should be used. If the input to the differential CLK inputs are AC coupled as pictured in Figure 2a the dependence on a centered V_{BB} reference is removed. The situation pictured will ensure that the input is centered around the bias set by the V_{BB}. As a result when AC coupled the AC specification limits for a differential input can be used. For more information on AC coupling please refer to the interfacing section of the design guide in the ECLinPS data book.

Using the Enable Pins

Both the common enable ($\overline{CEN}$) and the individual enables ($\overline{ENx}$) are synchronous to the CLK or SCLK input depending on which is selected. The active low signals are clocked into the enable flip flops on the negative edges of the E211 clock inputs. In this way the devices will only be disabled when the outputs are already in the LOW state. The internal propagation delays are such that the delay to the output through the distribution buffers is less than that through the enable flip flops. This will ensure that the disabling of the device will not slice any time off the clock pulse. On initial power up the enable flip flops will randomly attain a stable state, therefore precautions should be taken on initial power up to ensure the E211 is in the desired state.

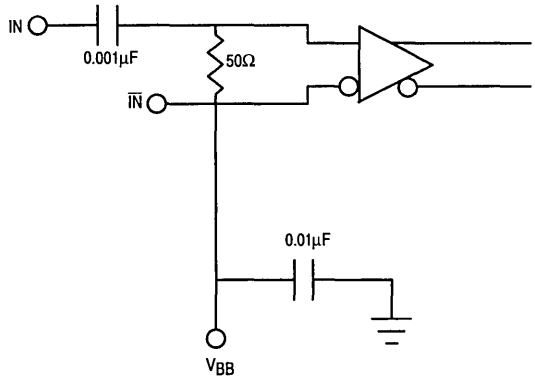


Figure 2a. AC Coupled Input

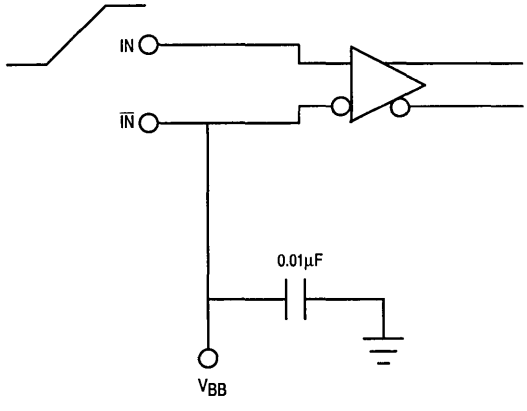


Figure 2b. Single-Ended Input

3-Bit Scannable Registered Address Driver

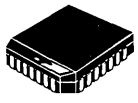
MC10E212
MC100E212

3-BIT SCANNABLE REGISTERED ADDRESS DRIVER

The MC10E/100E212 is a scannable registered ECL driver typically used as a fan-out memory address driver for ECL cache driving. In a VLSI array based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

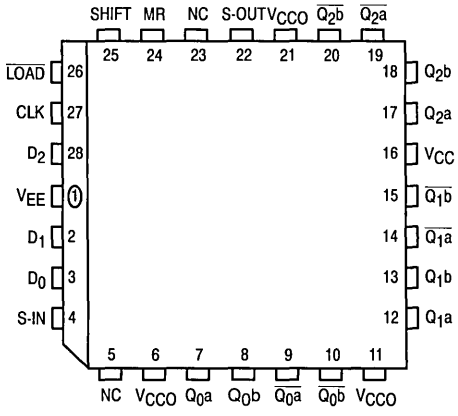
- Scannable Version E112 Driver
- 1025ps Max. CLK to Output
- Dual Differential Outputs
- Master Reset
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- Internal 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

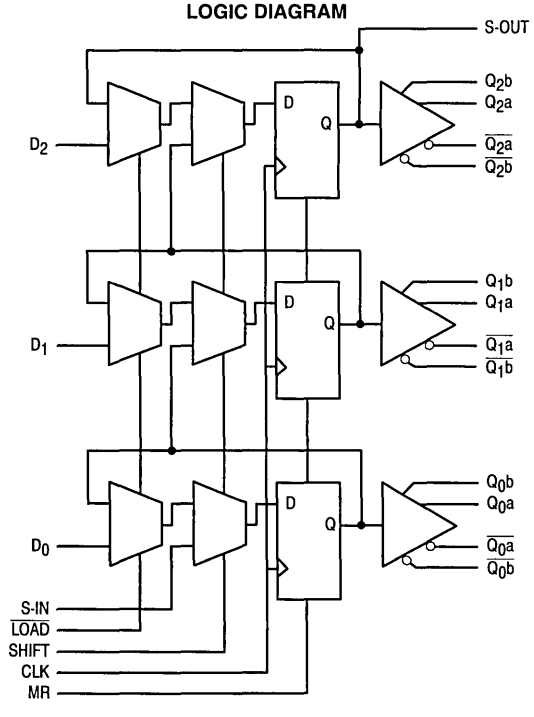
2

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_2$	Data Inputs
S-IN	Scan Input
$\overline{LOAD}$	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Reset
S-OUT	Scan Output
Q[0 2]a, Q[0:2]b	True Outputs
$\overline{Q}$[0.2]a, $\overline{Q}$[0:2]b	Inverting Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		80	96		80	96		80	96		
	100E		80	96		80	96		92	110		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	CLK	575	800	1025	575	800	1025	575	800	1025		
	MR	575	800	1025	575	800	1025	575	800	1025		
	CLK to S-OUT	575	800	1025	575	800	1025	575	800	1025		
t_S	Setup Time										ps	
	D	175	25		175	25		175	25			
	SHIFT	150	– 50		150	– 50		150	– 50			
	$\overline{LOAD}$	225	50		225	50		225	50			
	S-IN	150	– 50		150	– 50		150	– 50			
t_h	Hold Time										ps	
	D	250	25		250	25		250	25			
	SHIFT	300	100		300	100		300	100			
	$\overline{LOAD}$	225	0		225	0		225	0			
	S-IN	300	100		300	100		300	100			
t_{RR}	Reset Recovery	600	350		600	350		600	350		ps	
t_{SKEW}	Within-Device Skew		100			100			100		ps	1
t_{SKEW}	Within-Gate Skew		50			50			50		ps	2
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	425	650	275	425	650	275	425	650		

1. Within-device skew is defined as identical transitions on similar paths through a device
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input

FUNCTION TABLE

$\overline{LOAD}$	SHIFT	MR	MODE
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

8-Bit Scannable Register

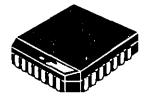
MC10E241
MC100E241

8-BIT SCANNABLE REGISTER

The MC10E/100E241 is an 8-bit shiftable register. Unlike a standard universal shift register such as the E141, the E241 features internal data feedback organized so that the SHIFT control overrides the HOLD/$\overline{\text{LOAD}}$ control. This enables the normal operations of HOLD and LOAD to be toggled with a single control line without the need for external gating. It also enables switching to scan mode with the single SHIFT control line.

The eight inputs $D_0 - D_7$ accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the positive-going edge of CLK; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

- SHIFT overrides HOLD/$\overline{\text{LOAD}}$ Control
- 1000ps Max. CLK to Q
- Asynchronous Master Reset
- Pin-Compatible with E141
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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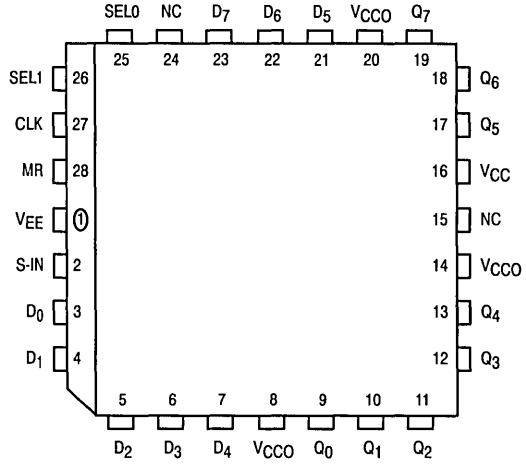
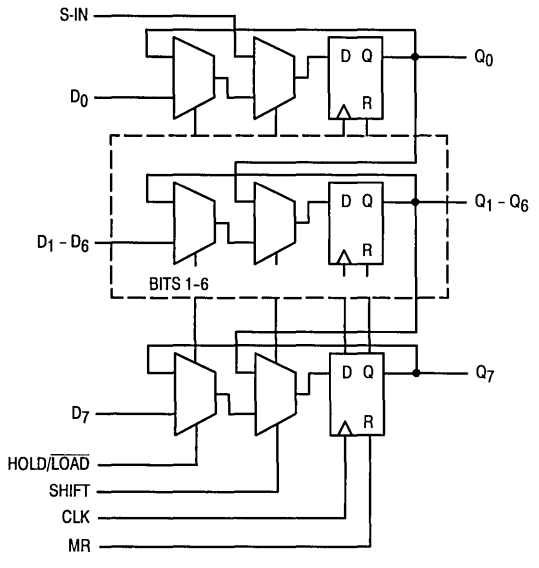
Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_7$	Parallel Date Inputs
S-IN	Serial Data Inputs
SEL0	SHIFT Control
SEL1	HOLD/$\overline{\text{LOAD}}$ Control
CLK	Clock
MR	Master Reset
$Q_0 - Q_7$	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										MA	
	10E		125	150		125	150		125	150		
	100E		125	150		125	150		144	173		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk	625	750	975	625	750	975	625	750	975		
	MR	600	725	975	600	725	975	600	725	975		
t_s	Setup Time										ps	
	D	175	25		175	25		175	25			
	SEL0 (SHIFT)	350	200		350	200		350	200			
	SEL1 (HOLD/$\overline{LOAD}$)	400	250		400	250		400	250			
	S-IN	125	–100		125	–100		125	–100			
t_h	Hold Time										ps	
	D	200	– 25		200	– 25		200	– 25			
	SEL0 (SHIFT)	100	– 200		100	– 200		100	– 200			
	SEL1 (HOLD/$\overline{LOAD}$)	50	– 250		50	– 250		50	– 250			
	S-IN	300	100		300	100		300	100			
t_{RR}	Reset Recovery Time	900	600		900	600		900	600		ps	
t_{PW}	Minimum Pulse Width										ps	
	Clk, MR	400			400			400				
t_{SKEW}	Within-Device Skew		60			60			60		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	300	525	800	300	525	800	300	525	800		

1. Within-device skew is defined as identical transitions on similar paths through a device.

2

3-Bit 4:1 Mux-Latch

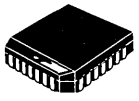
MC10E256
MC100E256

3-BIT 4:1
MUX-LATCH

The MC10E/100E256 contains three 4:1 multiplexers followed by transparent latches with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol).

When the Latch Enable (LEN) is LOW, the latch is transparent, and output data is controlled by the multiplexer select controls. A logic HIGH on LEN latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

- 950ps Max. D to Output
- 850ps Max. LEN to Output
- Split Select
- Differential Outputs
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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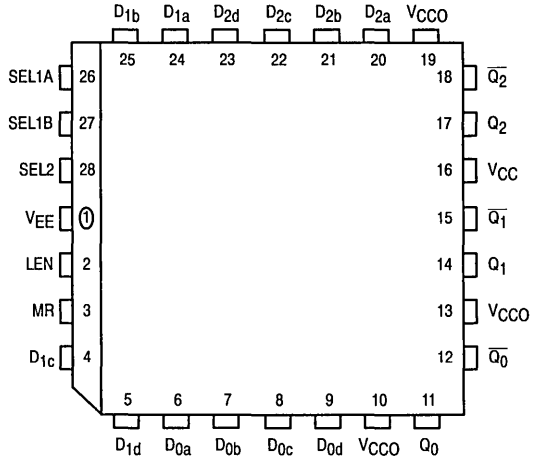
Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

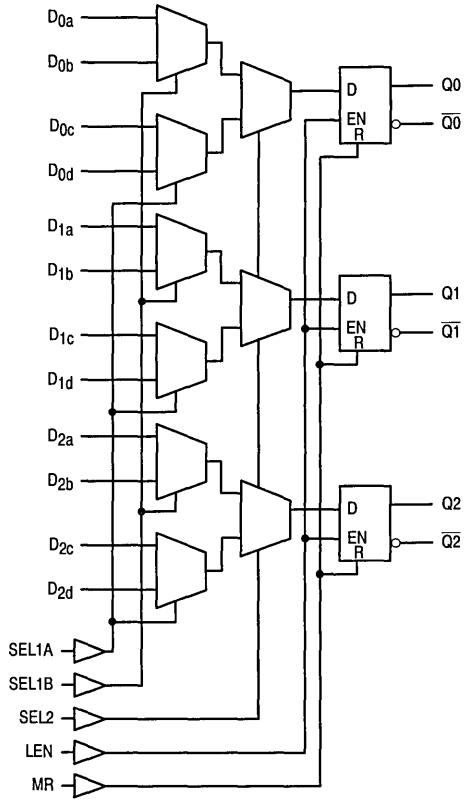
FUNCTION TABLE

Pin	State	Operation
SEL2	H	Output c/d Data
SEL1A	H	Input d Data
SEL1B	H	Input b Data

PIN NAMES

Pin	Function
$D_{0x} - D_{2x}$	Data Inputs
SEL1A, SEL1B	First-stage Select Inputs
SEL2	Second-stage Select input
LEN	Latch Enable
MR	Master Reset
$Q_0, \overline{Q_0} - Q_2, \overline{Q_2}$	Data Outputs

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		69	83		69	83		69	83		
	100E		69	83		69	83		79	96		

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**	**Condition**
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	D	400	600	900	400	600	900	400	600	900		
	SEL1	550	775	1050	550	775	1050	550	775	1050		
	SEL2	450	650	900	450	650	900	450	650	900		
	LEN	350	500	800	350	500	800	350	500	800		
	MR	350	600	825	350	600	825	350	600	825		
t_S	Setup Time										ps	
	D	400	275		400	275		400	275			
	SEL1	600	300		600	300		600	300			
	SEL2	500	250		500	250		500	250			
t_h	Hold Time										ps	
	D	300	−275		300	−275		300	−275			
	SEL1	100	−300		100	−300		100	−300			
	SEL2	200	−250		200	−250		200	−250			
t_{RR}	Reset Recovery Time	700	600		700	600		700	600		ps	
t_{PW}	Minimum Pulse Width										ps	
	MR	400			400			400				
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	475	700	275	475	700	275	475	700		

1. Within-device skew is defined as identical transitions on similar paths through a device.

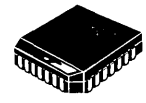
3-Bit Registered Bus Transceiver

MC10E336
MC100E336

3-BIT REGISTERED BUS TRANSCEIVER

The MC10E/MC100E336 contains three bus transceivers with both transmit and receive registers. The bus outputs ($\overline{BUS0}$–$\overline{BUS2}$) are specified for driving a 25Ω bus; the receive outputs (Q0 – Q2) are specified for 50Ω. The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to –2.0V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

- 25Ω Cutoff Bus Outputs
- 50Ω Receiver Outputs
- Transmit and Receive Registers
- 1500ps Max. Clock to Bus
- 1000ps Max. Clock to Q
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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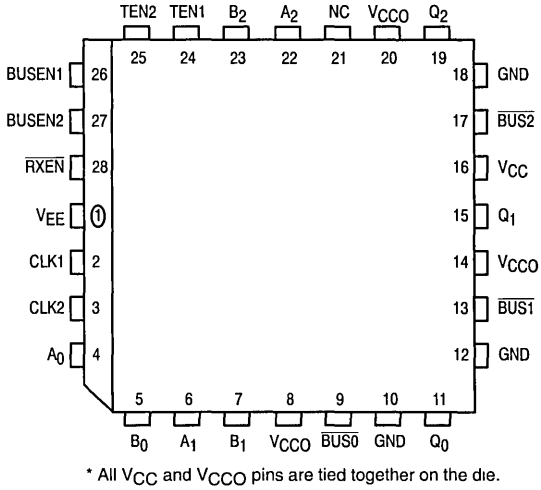
The Transmit Enable pins (TEN) control whether current data is held in the transmit register, or new data is loaded from the A/B inputs. A LOW on both of the Bus Enable inputs (BUSEN), when clocked through the register, disables the bus outputs to –2.0V.

The receiver section clocks bus data into the receive registers, after gating with the Receive Enable ($\overline{RXEN}$) input.

All registers are clocked by a positive transition of CLK1 or CLK2 (or both).

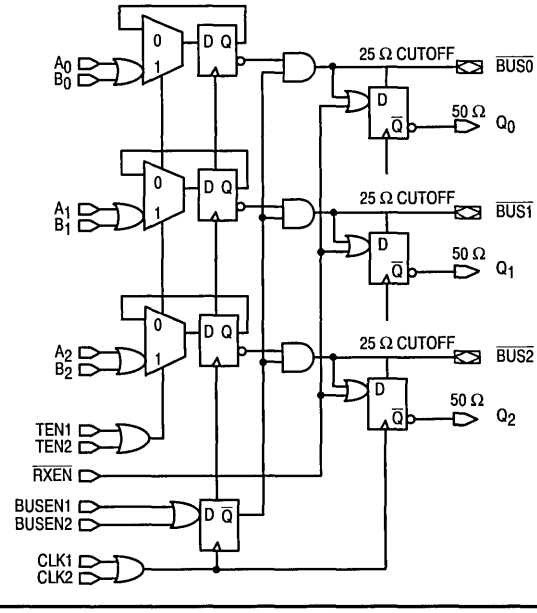
Additional leadframe grounding is provided through the Ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{CUT}	*Cut-off Output Voltage	– 2.10		– 2.03	– 2.10		– 2.03	– 2.10		– 2.03	V	
I_{IH}	Input HIGH Current										µA	
	$\overline{RXEN}$			225			225			225		
	All Other Inputs			150			150			150		
I_{EE}	Power Supply Current										mA	
	10E		125	150		125	150		125	150		
	100E		125	150		125	150		144	173		

*measured with V_{TT} = – 2.10V

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Clk to Q	500	700	100	500	700	1000	500	700	1000		
	Clk to $\overline{BUS}$	825	1250	1800	825	1250	1800	825	1250	1800		
t_S	Setup Time										ps	
	$\overline{BUS}$, $\overline{RXEN}$	150	–150		150	–150		150	–150			
	BUSEN	100	– 200		100	– 200		100	– 200			
	A, B Data	300	– 50		300	– 50		300	– 50			
	TEN	450	150		450	150		450	150			
t_h	Hold Time										ps	
	$\overline{BUS}$, $\overline{RXEN}$	450	150		450	150		450	150			
	BUSEN	500	200		500	200		500	200			
	A, B Data	350	50		350	50		350	50			
	TEN	200	–150		200	–150		200	–150			
t_{PW}	Minimum Pulse Width										ps	
	Clk	400			400			400				
t_r	Rise/Fall Times										ps	
t_f	20 - 80% (Qn)	300	450	700	300	450	700	300	450	700		
	20 - 80% ($\overline{BUSn}$ Rise)	500	800	1000	500	800	1000	500	800	1000		
	20 - 80% ($\overline{BUSn}$ Fall)	300	500	800	300	500	800	300	500	800		

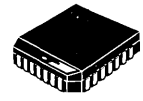
3-Bit Scannable Registered Bus Transceiver

MC10E337
MC100E337

3-BIT SCANNABLE REGISTERED BUS TRANSCEIVER

The MC10E/100E337 is a 3-bit registered bus transceiver with scan. The bus outputs (BUS0–BUS2) are specified for driving a 25Ω bus; the receive outputs (Q0 – Q2) are specified for 50Ω. The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to – 2.0V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

- Scannable Version of E336
- 25Ω Cutoff Bus Outputs
- 50Ω Receiver Outputs
- Scannable Registers
- Sync. and Async. Bus Enables
- Non-inverting Data Path
- 1500ps Max. Clock to Bus (Data Transmit)
- 1000ps Max. Clock to Q (Data Receive)
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

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Both drive and receive sides feature the same logic, including a loopback path to hold data. The HOLD/$\overline{\text{LOAD}}$ function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides respectively, with a HIGH selecting LOAD. Note that the implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable ($\overline{\text{ABUSDIS}}$) disables the bus immediately for scan mode.

The $\overline{\text{SYNCEN}}$ input is provided for flexibility when re-enabling the bus after disabling with $\overline{\text{ABUSDIS}}$, allowing either synchronous or asynchronous re-enabling. An alternative use is asynchronous-only operation with $\overline{\text{ABUSDIS}}$, in which case $\overline{\text{SYNCEN}}$ is tied LOW, or left open. $\overline{\text{SYNCEN}}$ is implemented as an overriding SET control (active-LOW) to the enable flip-flop.

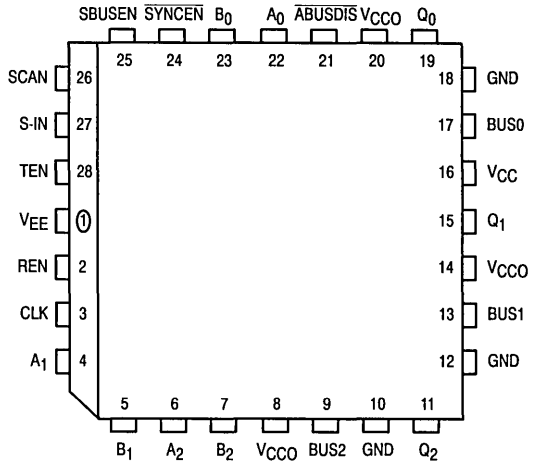
Scan mode is selected by a HIGH at the SCAN input. Scan input data is shifted in through S_IN and output data appears at the Q2 output.

All registers are clocked on the positive transition of CLK. Additional lead-frame grounding is provided through the Ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

PIN NAMES

Pin	Function
$A_0 - A_2$	Data Inputs A
$B_0 - B_2$	Data Inputs B
S-IN	Serial (Scan) Data Input
TEN, REN	HOLD/$\overline{\text{LOAD}}$ Controls
SCAN	Scan Control
$\overline{\text{ABUSDIS}}$	Asynchronous Bus Disable
SBUSEN	Synchronous Bus Enable
$\overline{\text{SYNCEN}}$	Synchronous Enable Control
CLK	Clock
BUS0 – BUS2	25Ω Cutoff Bus Outputs
$Q_0 - Q_2$	Receive Data Outputs (Q2 serves as SCAN_OUT in scan mode)

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

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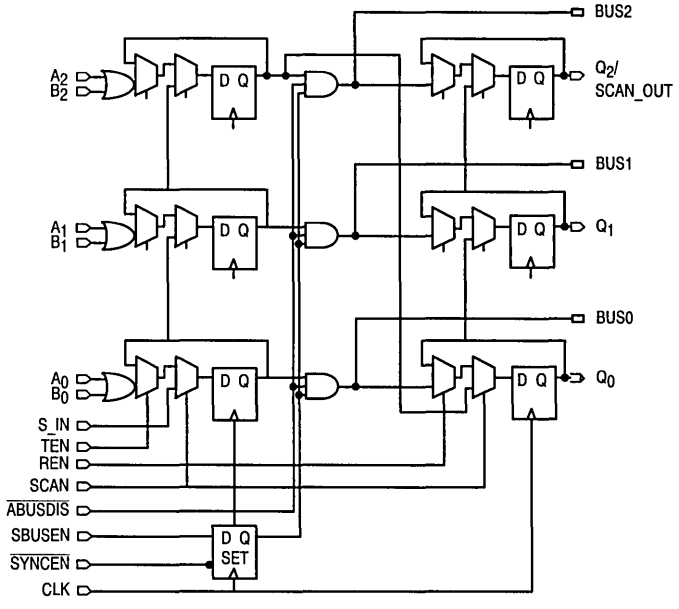
LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{CUT}	*Cut-off Output Voltage	– 2.10		– 2.03	– 2.10		– 2.03	– 2.10		– 2.03	V	
I_{IH}	Input HIGH Current All Other Inputs			150			150			150	µA	
I_{EE}	Power Supply Current 10E 100E		145 145	174 174		145 145	174 174		145 167	174 200	mA	

*measured with V_{TT} = –2.10V

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

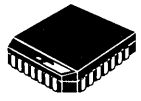
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output Clk to Q Clk to BUS $\overline{ABUSDIS}$ $\overline{SYNCEN}$	450 800 500 800		1000 1800 1500 1800	450 800 500 800		1000 1800 1500 1800	450 800 500 800		1000 1800 1500 1800	ps	
t_S	Setup Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 100 400 550			350 100 400 550			350 100 400 550			ps	
t_h	Hold TIme BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 500 350 200			350 500 350 200			350 500 350 200			ps	
t_{PW}	Minimum Pulse Width CLk	400			400			400			ps	
t_r t_f	Rise/Fall Times 20 - 80% (Qn) 20 - 80% (BUSn Rise) 20 - 80% (BUSn Fall)	300 500 300		800 1000 800	300 500 300		800 1000 800	300 500 300		800 1000 800	ps	

2

Quad Differential AND/NAND

MC10E404
MC100E404

QUAD DIFFERENTIAL AND/NAND



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E404/100E404 is a 4-bit differential AND/NAND device. The differential operation of the device makes it ideal for pulse shaping applications where duty cycle skew is critical. Special design techniques were incorporated to minimize the skew between the upper and lower level gate inputs.

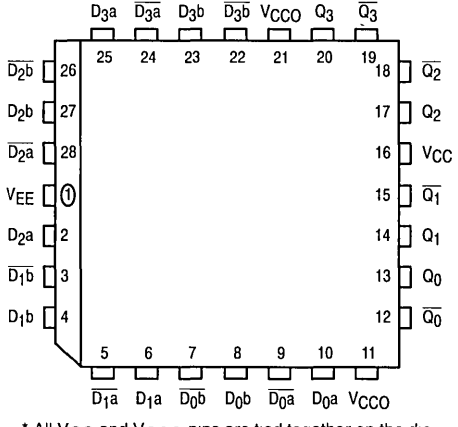
Because a negative 2-input NAND function is equivalent to a 2-input OR function, the differential inputs and outputs of the device also allow for its use as a fully differential 2 input OR/NOR function.

The output RISE/FALL times of this device are significantly faster than most other standard ECLinPS devices resulting in an increased bandwidth.

The differential inputs have clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5V below V_{CC}.

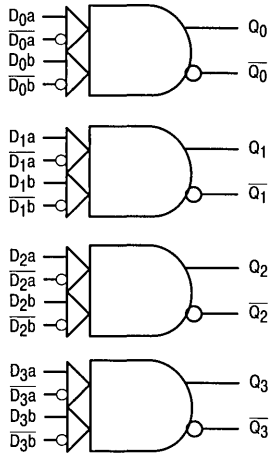
- Differential D and Q
- 700ps Max. Propagation Delay
- High Frequency Outputs
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- Internal 75kΩ Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die

LOGIC DIAGRAM



PIN NAMES

Pin	Function
D[0:4], $\overline{D}$[0.4]	Differential Data Inputs
Q[0:4], $\overline{Q}$[0·4]	Differential Data Outputs

FUNCTION TABLE

Da	Db	Q	$\overline{Da}$	$\overline{Db}$	$\overline{Q}$
L	L	L	L	L	L
L	H	L	L	H	H
H	L	L	H	L	H
H	H	H	H	H	H

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		106	127		106	127		106	127		
	100E		106	127		106	127		122	146		
V_{PP}(DC)	Input Sensitivity	50			50			50			mV	1
V_{CMR}	Common Mode Range	–1.5		0	–1.5		0	–1.5		0	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than $V_{PP\ MIN}$ and < 1.0V.

AC CHARACTERISTICS (V_{EE}= V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	Da (Diff)	350	475	650	350	475	650	350	475	650		
	Da (SE)	300	475	700	300	475	700	300	475	700		
	Db (Diff)	375	500	675	375	500	675	375	500	675		
	Db (SE)	325	500	725	325	500	725	325	500	725		
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
V_{PP}(AC)	Minimum Input Swing	150			150			150			mV	2
t_r	Rise/Fall Time											
t_f	20 - 80%	150		400	150		400	150		400	ps	

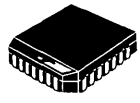
1 Within-device skew is defined as identical transitions on similar paths through a device.
2. Minimum input swing for which AC parameters are guaranteed.

2

Quint Differential Line Receiver

MC10E416
MC100E416

QUINT DIFFERENTIAL LINE RECEIVER



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

The MC10E416/100E416 is a 5-bit differential line receiving device. The 2.0GHz of bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

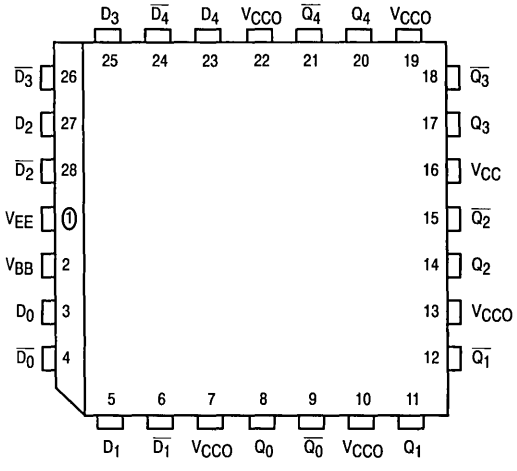
A V_{BB} pin is available to AC couple an input signal to the device. More information on AC coupling can be found in the design handbook section of this data book.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5V below V_{CC}.

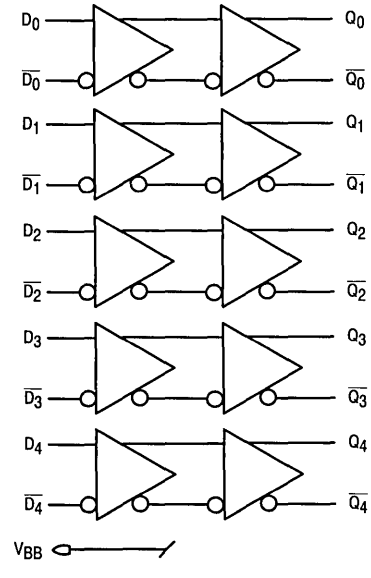
- Differential D and Q; V_{BB} available
- 600ps Max. Propagation Delay
- High Frequency Outputs
- 2 Stages of Gain
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- Internal 75kΩ Input Pulldown Resistors

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
D[0:4], $\overline{D}$[0:4]	Differential Data Inputs
Q[0:4], $\overline{Q}$[0.4]	Differential Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{BB}	Output Reference Voltage										V	
	10E	−1.38		−1.27	−1.35		−1.25	−1.31		−1.19		
	100E	−1.38		−1 26	−1.38		−1.26	−1.38		−1.26		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		135	162		135	162		135	162		
	100E		135	162		135	162		155	186		
V_{PP}(DC)	Input Sensitivity	50			50			50			mV	1
V_{CMR}	Common Mode Range	−1.5		0	−1.5		0	−1.5		0	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signal are within the V_{CMR} range and the input swing is greater than $V_{PP\ MIN}$ and < 1.0V

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	d(Diff)	250	350	500	250	350	500	250	350	500		
	D(SE)	200	350	550	200	350	550	200	350	550		
t_{SKEW}	Within-Device Skew		50			50			50		ps	1
t_{SKEW}	Duty Cycle Skew											
	t_{PLH}-t_{PHL}		±10			±10			±10		ps	2
V_{PP}(AC)	Minimum Input Swing	150			150			150			mV	3
t_r	Rise/Fall Time											
t_f	20 - 80%	100	200	350	100	200	350	100	200	350	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed.

3-Bit Differential Flip-Flop

MC10E431
MC100E431

3-BIT DIFFERENTIAL FLIP-FLOP

The MC10E/100E431 is a 3-bit flip-flop with differential clock, data input and data output.

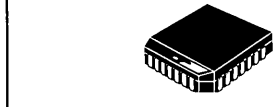
The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge, without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduce the metastability susceptibility window.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5V below V_{CC}.

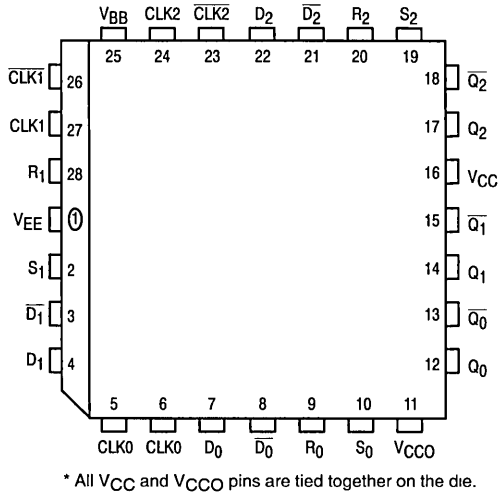
2

- Edge-Triggered Asynchronous Set and Reset
- Differential D, CLK and Q; V_{BB} Reference Available
- 1100MHz Min. Toggle Frequency
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V



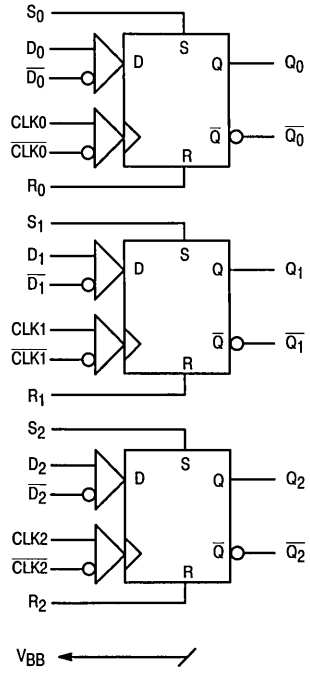
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
D[0:2], $\overline{D}$[0:2]	Differential Data Inputs
CLK[0:2], $\overline{CLK}$[0.2]	Differential Clock
S[0:2]	Edge Triggered Set Inputs
R[0:2]	Edge Triggered Reset Input
V_{BB}	V_{BB} Reference Output
Q[0:2], $\overline{Q}$[0:2]	Differential Data Outputs

FUNCTION TABLE

Dn	CLKn	Rn	Sn	Qn
L	Z	L	L	L
H	Z	L	L	H
X	L	Z	L	L
X	L	L	Z	H

Z = Low to high transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage 10E	–1.43		–1.30	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V	
	100E	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1 26		
I_{IH}	Input HIGH Current			150			150			150	150			µA	
I_{EE}	Power Supply Current 10E		110	132	110	132		110	132		110	132		mA	
	100E		110	132	110	132		110	132		127	152			
V_{CMR}	Common Mode Range	–1.5		0	–1.5		0	–1.5		0	–1.5		0	V	1

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal specified operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP}

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic		–40°C			0°C to 85°C			Unit	Condition
			Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency		1000	1400		1100	1400		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK (Diff)	410	600	790	450	600	750	ps	
		CLK (SE)	460	600	840	400	600	800		
		R	500	725	975	550	725	925		
		S	500	725	975	550	725	925		
t_S	Setup Time	D	250	0		200	0		ps	
		R	1100	700		1000	700			1
		S	1100	700		1000	700			1
t_H	Hold Time	D	250	0		200	0		ps	
t_{PW}	Minimum Pulse Width	CLK	400			400			ps	
t_{skew}	Within-Device Skew			50			50		ps	2
V_{PP}	Minimum Input Swing		150			150			mV	3
t_r/t_f	Rise/Fall Times		250	450	700	275	450	650	ps	20–80%

1. These setup times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Minimum input swing for which AC parameters are guaranteed.

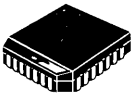
4-Bit Serial/Parallel Converter

MC10E445
MC100E445

4-BIT SERIAL/ PARALLEL CONVERTER

The MC10/100E445 is an integrated 4-bit serial to parallel data converter. The device is designed to operate for NRZ data rates of up to 2.0Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q0, the second to Q1 etc.

- On-Chip Clock ÷4 and ÷8
- 2.0Gb/s Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-Ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8-Bits
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E V_{EE} Range of –4.2V to –5.46V



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel to serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse applied asynchronously for at least two input clock cycles shifts the start bit for conversion from Qn to Qn–1. For each additional shift required an additional pulse must be applied to the SYNC input. Asserting the SYNC input will force the internal clock dividers to "swallow" a clock pulse, effectively shifting a bit from the Qn to the Qn–1 output (see Timing Diagram B).

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the data on the output will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E445's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 2.0Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E445.

For lower data rate applications a V_{BB} reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz differential input signals are recommended. For single-ended inputs the V_{BB} pin is tied to the inverting differential input and bypassed via a 0.01μF capacitor. The V_{BB} provides the switching reference for the input differential amplifier. The V_{BB} can also be used to AC couple an input signal, for more information on AC coupling refer to the interfacing section of the design guide in the ECLinPS™ data book.

Upon power-up the internal flip-flops will attain a random state. To synchronize multiple E445's in a system the master reset must be asserted.

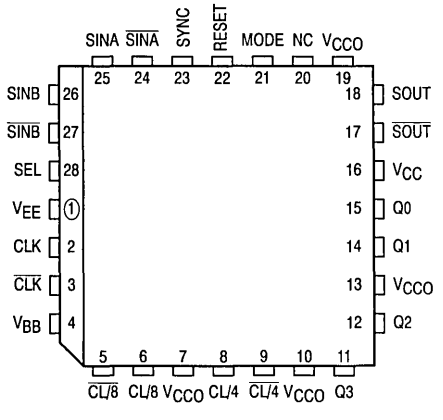
PIN NAMES

Pin	Function
SINA, $\overline{\text{SINA}}$	Differential Serial Data Input A
SINB, $\overline{\text{SINB}}$	Differential Serial Data Input B
SEL	Serial Input Selector Pin
Q0–Q3	Parallel Data Outputs
CLK, $\overline{\text{CLK}}$	Differential Clock Inputs
CL/4, $\overline{\text{CL/4}}$	Differential ÷4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Differential ÷8 Clock Output
MODE	Conversion Mode 4-Bit/8-Bit
SYNCH	Conversion Synchronizing Input

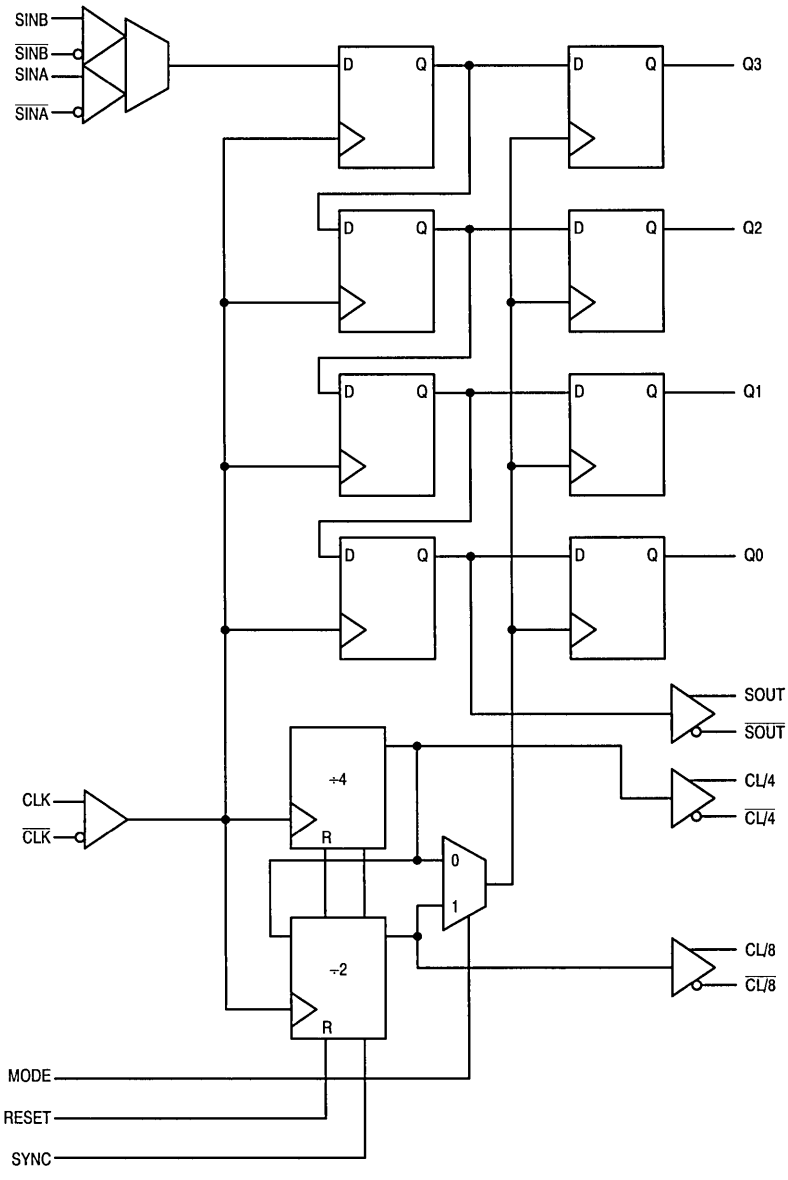
FUNCTION TABLES

Mode	Conversion	SEL	Serial Input
L	4-Bit	H	A
H	8-Bit	L	B

Pinout: 28-Lead PLCC (Top View)



LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

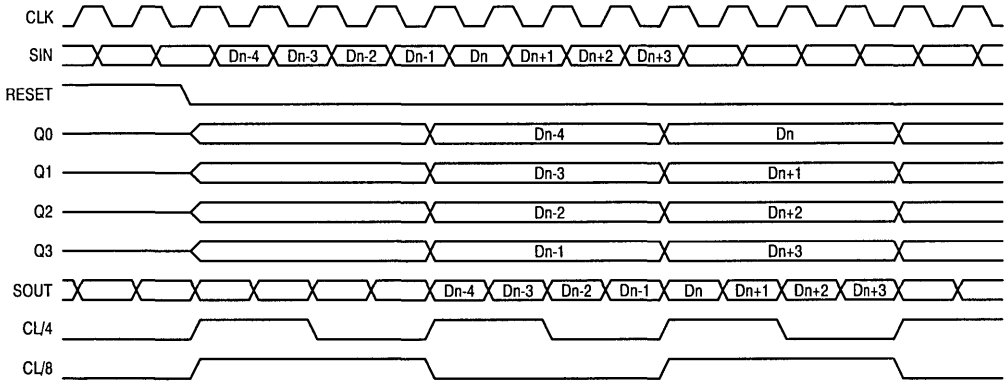
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	µA	
V_{OH}	Ouput HIGH Current										V	
	10E (SOUT Only)	–1020		–790	–980		–760	–910		–670		1
	100E (SOUT Only)	–1025		–830	–1025		–830	–1025		–830		1
V_{BB}	Output Reference Voltage										V	
	10E	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19		
	100E	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26		
I_{EE}	Power Supply Current										mA	
	10E		154	185		154	185		154	185		
	100E		154	185		154	185		177	212		

1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

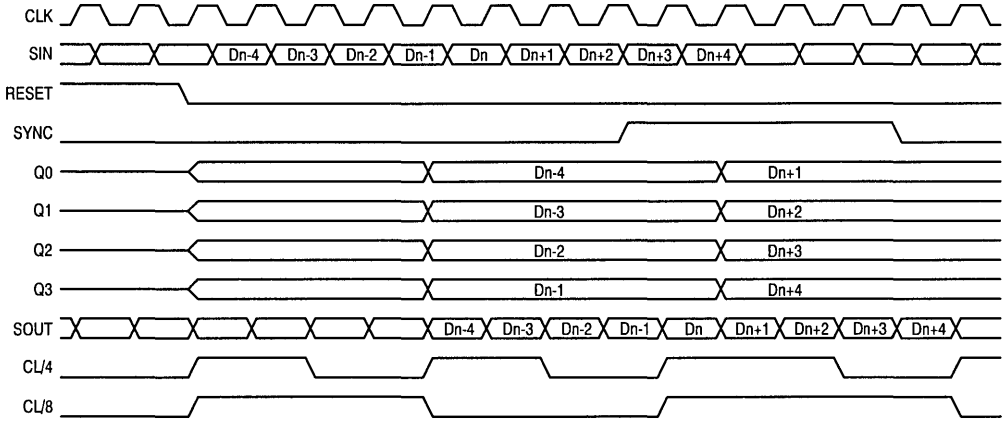
AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Conversion Frequency	2.0			2.0			2.0			Gb/s NRZ	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to Q	1500	1800	2100	1500	1800	2100	1500	1800	2100		
	CLK to SOUT	800	975	1150	800	975	1150	800	975	1150		
	CLK to CL/4	1100	1325	1550	1100	1325	1550	1100	1325	1550		
	CLK to CL/8	1100	1325	1550	1100	1325	1550	1100	1325	1550		
t_S	Setup Time										ps	
	SINA, SINB	–100	–250		–100	–250		–100	–250			
	SEL	0	–200		0	–200		0	–200			
t_h	Hold Time										ps	
	SINA, SINB, SEL	450	300		450	300		450	300			
t_{RR}	Reset Recovery Time	500	300		500	300		500	300		ps	
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_r t_f	Rise/Fall Times										ps	20%–80%
	SOUT	100	225	350	100	225	350	100	225	350		
	Other	200	425	650	200	425	650	200	425	650		

TIMING DIAGRAMS



Timing Diagram A. 1:4 Serial to Parallel Conversion



Timing Diagram B. 1:4 Serial to Parallel Conversion With SYNC Pulse

APPLICATIONS INFORMATION

The MC10E/100E445 is an integrated 1:4 serial to parallel converter. The chip is designed to work with the E446 device to provide both transmission and receiving of a high speed serial data path. The E445, can convert up to a 2.0Gb/s NRZ data stream into 4-bit parallel data. The device also provides a divide by four clock output to be used to synchronize the parallel data with the rest of the system.

The E445 features multiplexed dual serial inputs to provide test loop capability when used in conjunction with the E446. Figure 1 illustrates the loop test architecture. The architecture allows for the electrical testing of the link without requiring actual transmission over the serial data path medium. The SINA serial input of the E445 has an extra buffer delay and thus should be used as the loop back serial input.

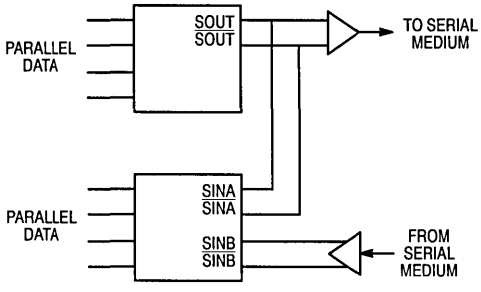


Figure 1. Loopback Test Architecture

The E445 features a differential serial output and a divide by 8 clock output to facilitate the cascading of two devices to build a 1:8 demultiplexer. Figure 2 illustrates the architecture for a 1:8 demultiplexer using two E445's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1150ps and tS for SIN = –100ps, yields a minimum period of 1050ps or a clock frequency of 950MHz.

The clock frequency is significantly lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E445. By delaying the clock feeding the second E445 relative to the clock of the first E445 the frequency of operation can be increased. The delay between the two clocks can be increased until the minimum delay of clock to serial out would potentially cause a serial bit to be swallowed (Figure 3).

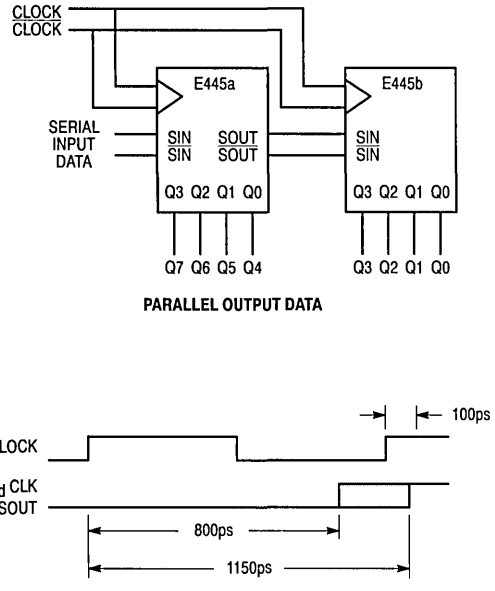


Figure 2. Cascaded 1:8 Converter Architecture

With a minimum delay of 800ps on this output the clock for the lower order E445 cannot be delayed more than 800ps relative to the clock of the first E445 without potentially missing a bit of information. Because the setup time on the serial input pin is negative coincident excursions on the data and clock inputs of the E445 will result in correct operation.

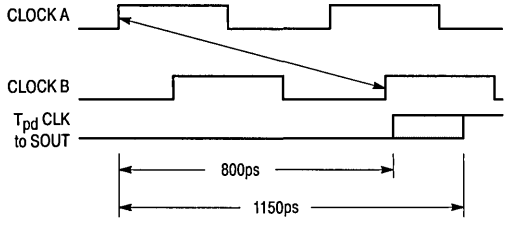


Figure 3. Cascade Frequency Limitation

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E445. By connecting the clock for the second E445 to the complimentary clock input pin the device will clock a half a clock period after the first E445 (Figure 4). Utilizing this simple technique will raise the potential conversion frequency up to 1.4GHz. The divide by eight clock of the second E445 should be used to synchronize the parallel data to the rest of the system as the parallel data of the two E445's will no longer be synchronized. This skew problem between the outputs can be worked around as the parallel information will be static for eight more clock pulses.

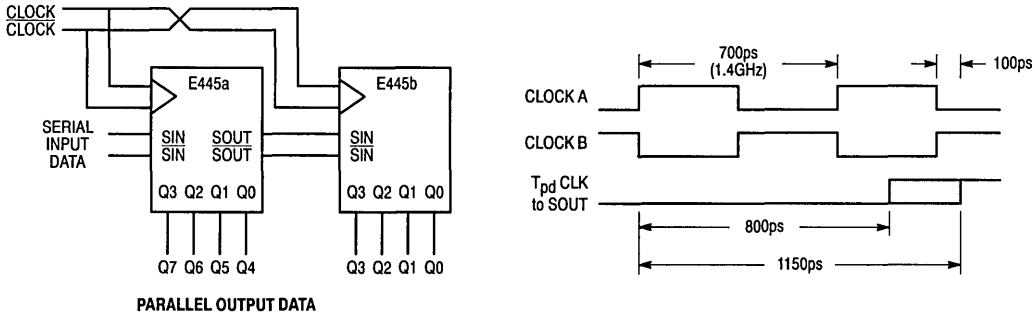
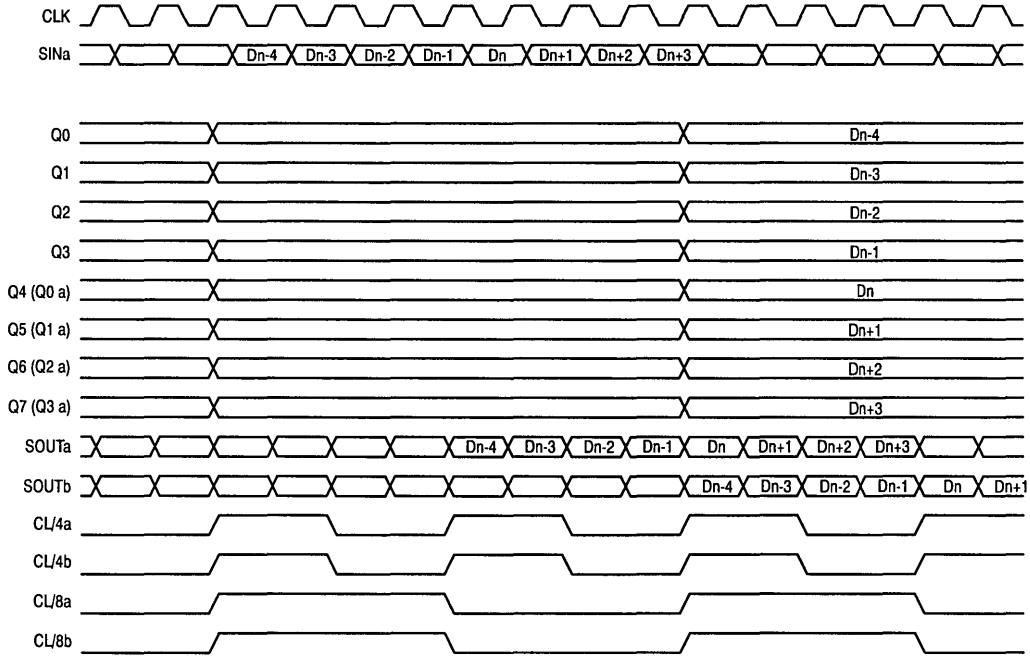


Figure 4. Extended Frequency 1:8 Demultiplexer

2



Timing Diagram A. 1:8 Serial to Parallel Conversion

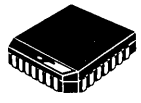
4-Bit Parallel/Serial Converter

MC10E446
MC100E446

4-BIT PARALLEL/ SERIAL CONVERTER

The MC10E/100E446 is an integrated 4-bit parallel to serial data converter. The device is designed to operate for NRZ data rates of up to 1.3Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8 bit conversion applications. Note that the serial output data clocks off of the negative input clock transition.

- On Chip Clock ÷4 and ÷8
- 1.5 Gb/s Typical Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8 Bits
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E V_{EE} Range of -4.2V to -5.46V



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2

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and thus select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the internal load clock will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E446's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 1.3Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

For lower data rate applications a V_{BB} reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz differential input signals are recommended. For single-ended inputs the V_{BB} pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The V_{BB} provides the switching reference for the input differential amplifier. The V_{BB} can also be used to AC couple an input signal, for more information on AC coupling refer to the interfacing section of the design guide in the ECLinPS™ data book.

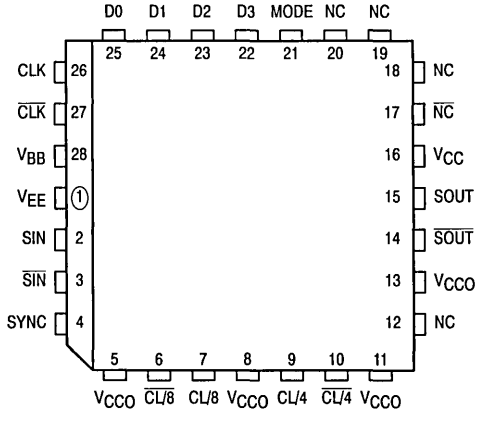
PIN NAMES

Pin	Function
SIN	Differential Serial Data Input
D0 – D3	Parallel Data Inputs
SOUT, $\overline{\text{SOUT}}$	Differential Serial Data Output
CLK, $\overline{\text{CLK}}$	Differential Clock Inputs
CL/4, $\overline{\text{CL/4}}$	Differential ÷4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Differential ÷8 Clock Output
MODE	Conversion Mode 4-Bit/8-Bit
SYNC	Conversion Synchronizing Input

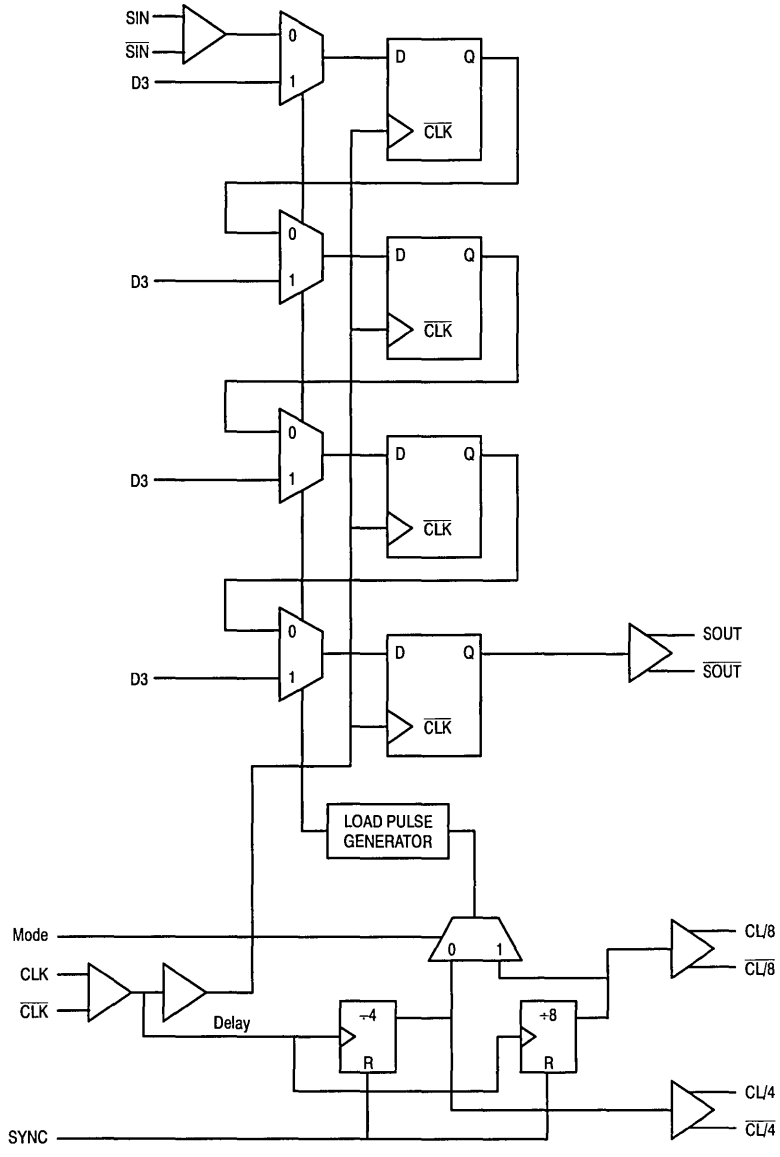
FUNCTION TABLES

Mode	Conversion
L	4-Bit
H	8-Bit

Pinout: 28-Lead PLCC (Top View)



LOGIC DIAGRAM



DC CHARACTERISTICS (V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$; V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	µA	
V_{OH}	Output HIGH Voltage										V	
	10E (SOUT Only)	–1020		–790	–980		–760	–910		–670		1
	100E (SOUT Only)	–1025		–830	–1025		–830	–1025		–830		1
V_{BB}	Output Reference Voltage 10E	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V	
	100E	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26		
I_{EE}	Power Supply Current 10E		126	151		126	151		126	151	mA	
	100E		126	151		126	151		145	174		

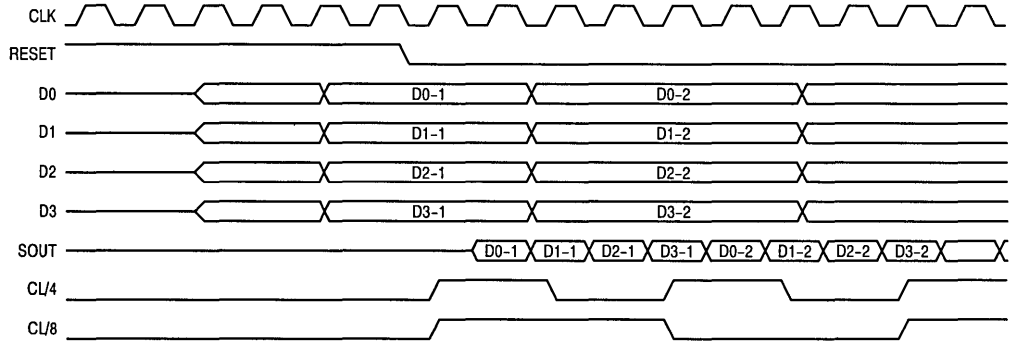
1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

AC CHARACTERISTICS (V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$; V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
F_{MAX}	Max Conversion Frequency	1.3	1.6		1.3	1.6		1.3	1.6		Gb/s NRZ	
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	
	CLK to SOUT[1]	1020	1200	1480	1020	1200	1480	1020	1200	1480		
	CLK to CL/4	650	850	1050	650	850	1050	650	850	1050		
	CLK to CL/8	800	1050	1300	800	1050	1300	800	1050	1300		
	SYNC to CL/4, CL/8	650	850	1100	650	850	1100	650	850	1100		
t_S	Setup Time[2] SIN, Dn	-200	-450		-200	–450		–200	–450		ps	
t_h	Hold Time[2] SIN, Dn	900	650		900	650		900	650		ps	
t_{RR}	Reset Recovery Time SYNC	500	300		500	300		500	300		ps	
t_{PW}	Min Pulse Width CLK, MR	300			300			300			ps	
t_r	Rise/Fall Times SOUT	100	225	350	100	225	350	100	225	350	ps	20% - 80%
t_f	Other	200	425	650	200	425	650	200	425	650		

1. Propagation delays measured from negative going clock edge.
2. Relative to negative clock edge.

Timing Diagrams



Timing Diagram A. 4:1 Parallel to Serial Conversion

Applications Information

The MC10E/100E446 is an integrated 4:1 parallel to serial converter. The chip is designed to work with the E445 device to provide both transmission and receiving of a high speed serial data path. The E446 can convert 4 bits of data into a 1.3Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see timing diagram A).

The E446 features a differential serial input and internal divide by 8 circuitry to facilitate the cascading of two devices to build a 8:1 multiplexer. Figure 1 illustrates the architecture for a 8:1 multiplexer using two E446's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1480ps and tS for SIN = –200ps, yields a minimum period of 1280ps or a clock frequency of 780MHz.

The clock frequency is somewhat lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E446. By delaying the clock feeding E446A relative to the clock of E446B the frequency of operation can be increased.

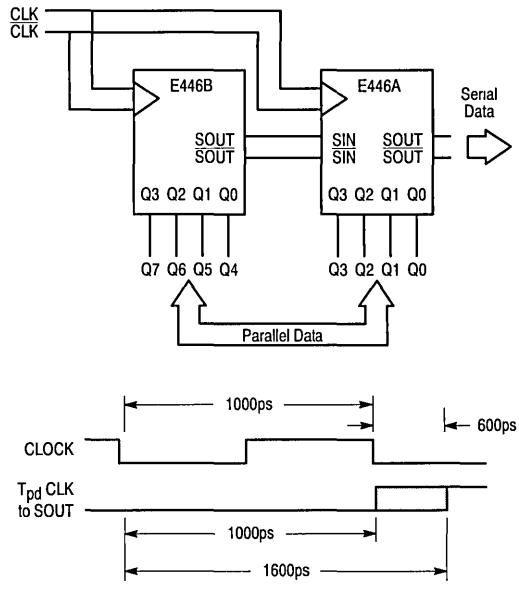
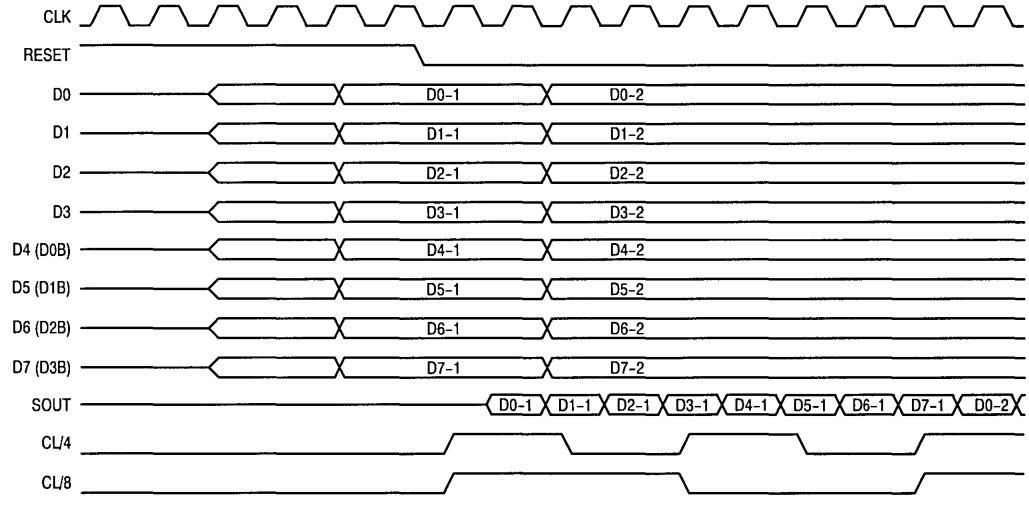


Figure 1. Cascaded 8:1 Converter Architecture



Timing Diagram B. 8:1 Parallel to Serial Conversion

6-Bit D Register Differential Data and Clock

MC10E451
MC100E451

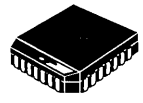
6-BIT D REGISTER DIFFERENTIAL DATA AND CLOCK

The MC10E/100E451 contains six D-type flip-flops with single-ended outputs and differential data inputs. The common clock input is also differential. The registers are triggered by a positive transition of the positive clock (CLK) input.

A HIGH on the Master Reset (MR) input resets all Q outputs to LOW. The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01μF capacitor.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5V below V_{CC}.

- Differential Inputs: Data and Clock
- V_{BB} Output
- 1100MHz Min. Toggle Frequency
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors



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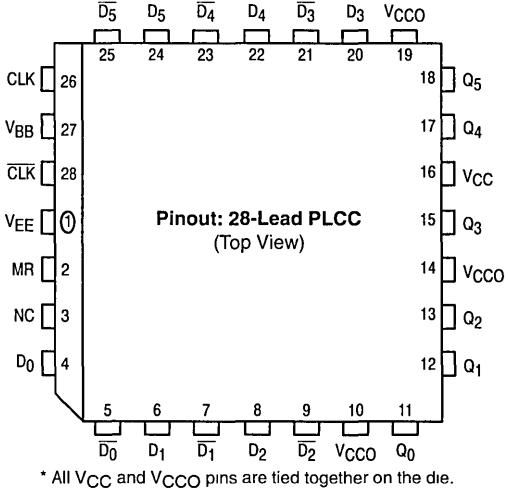
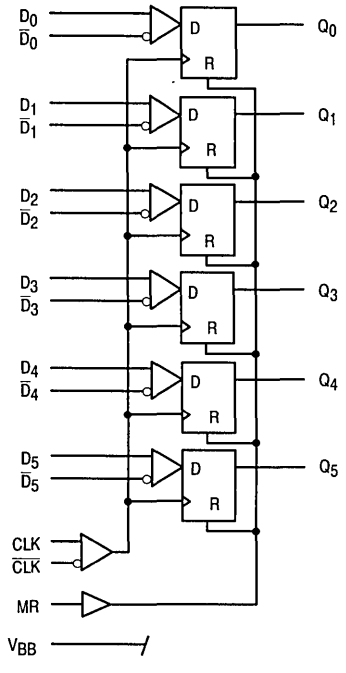


Pinout: 28-Lead PLCC
(Top View)

* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
$D_0 - D_5$	+Data Input
$\overline{D_0} - \overline{D_5}$	– Data Input
CLK	+Clock Input
$\overline{CLK}$	– Clock Input
MR	Master Reset Input
V_{BB}	V_{BB} Output
$Q_0 - Q_5$	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{BB}	Output Reference Voltage										V	
	10E	−1.3		−1.2	−1.3		−1.2	−1.3		−1.1		
		8		7	5		5	1		9		
	100E	−1.3		−1.2	−1.3		−1.2	−1.3		−1.2		
		8		6	8		6	8		6		
I_{IH}	Input HIGH Current			150			150			150	µA	
I_{EE}	Power Supply Current										mA	
	10E		84	101		84	101		84	101		
	100E		84	101		84	101		97	116		
V_{CMR}	Common Mode Range	−2.0		−0.4	−2.0		−0.4	−2.0		−0.4	V	2

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than $V_{PP\ MIN}$ and < 1.0V.

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
f_{MAX}	Max, Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz	
t_{PLH}	Propagation Delay to Output										ps	
t_{PHL}	CLK (Diff)	475	650	800	475	650	800	475	650	800		
	CLK (SE)	425	650	850	425	650	850	425	650	850		
	MR	425	600	850	425	600	850	425	600	850		
t_s	Setup Time										ps	
	D	150	−100		150	−100		150	−100			
t_h	Hold Time										ps	
	D	250	100		250	100		250	100			
$V_{PP(AC)}$	Minimum Input Swing	150			150			159			mV	1
t_{RR}	Reset Recovery Time	750	600		750	600		750	600		ps	
t_{PW}	Minimum Pulse Width										ps	
	CLK, MR	400			400			400				
t_{SKEW}	Within-Device Skew		100			100			100		ps	2
t_r	Rise/Fall Times										ps	
t_f	20 - 80%	275	450	800	275	450	800	275	450	800		

1. Minimum input voltage for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.

5-Bit Differential Register

MC10E452
MC100E452

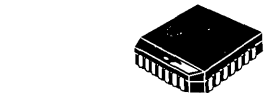
5-BIT DIFFERENTIAL REGISTER

The MC10E/100E452 is a 5-bit differential register with differential data (inputs and outputs) and clock. The registers are triggered by a positive transition of the positive clock (CLK) input. A high on the Master Reset (MR) asynchronously resets all registers so that the Q outputs go LOW.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5V below V_{CC}.

The fully differential design of the device makes it ideal for very high frequency applications where a registered data path is necessary.

- Differential D, CLK and Q; V_{BB} Reference Available
- 1100MHz Min. Toggle Frequency
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V



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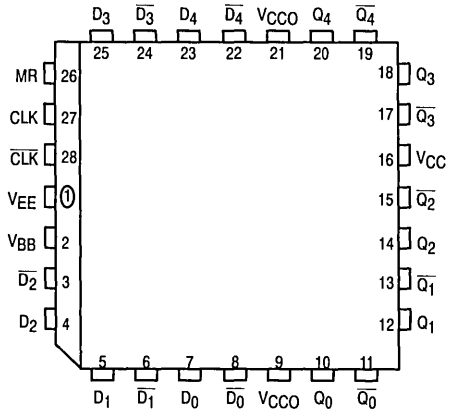
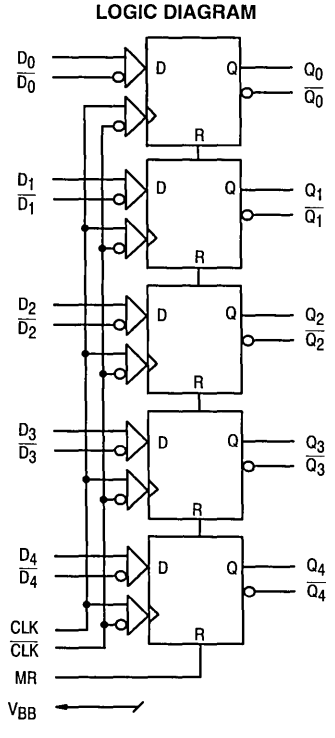
Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



PIN NAMES

Pin	Function
D[0 4], $\overline{D}$[0:4]	Differential Data Inputs
MR	Master Reset Input
CLK, $\overline{CLK}$	Differential Clock Input
VBB	VBB Reference Output
Q[0:4], $\overline{Q}$[0 4]	Differential Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit	Cond
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{BB}	Output Reference Voltage	10E	–1.43		–1.30	–1 38		–1.27	–1.35		–1 25	–1 31		–1.19	V	
		100E	–1.38		–1 26	–1.38		–1 26	–1.38		–1.26	–1.38		–1.26		
I_{IH}	Input HIGH Current				150			150			150			150	µA	
I_{EE}	Power Supply Current	10E		74	89		74	89		74	89		74	89	mA	
		100E		74	89		74	89		74	89		85	102		
V_{CMR}	Common Mode Range		–2.0		–0.4	–2.0		–0.4	–2 0		–0.4	–2.0		–0 4	V	1

1. V_{CMR} is referenced to the most positive side of the differential input signal Normal specified operation is obtained when the input signals are within the V_{CMR} range and the input swing is greater than V_{PP}.

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic		–40°C			0°C to 85°C			Unit	Condition
			Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Toggle Frequency		1000	1400		1100	1400		MHz	
t_{PLH}	Propagation Delay to Output	CLK (Diff)	425	600	850	475	600	800	ps	
t_{PHL}		CLK (SE)	375	600	900	425	600	850		
		MR	375	625	900	425	625	850		
t_S	Setup Time	D	175	–50		150	–50		ps	
t_H	Hold Time	D	225	50		200	50		ps	
t_{RR}	Reset Recovery Time		750	450		700	450			
t_{PW}	Minimum Pulse Width	CLK	400			400			ps	
		MR	400			400				
t_{skew}	Within-Device Skew			50			50		ps	1
V_{PP}	Minimum Input Swing		150			150			mV	2
t_r/t_f	Rise/Fall Times		250	475	725	275	475	675	ps	20–80%

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Minimum input swing for which AC parameters are guaranteed.

Triple Differential 2:1 Multiplexer

MC10E457
MC100E457

TRIPLE DIFFERENTIAL 2:1 MULTIPLEXER

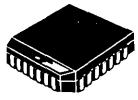
The MC10E457/100E457 is a 3-bit differential 2:1 multiplexer. The fully differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided to ease AC coupling input signals.

The higher frequency outputs provide the device with a >1.0GHz bandwidth to meet the needs of the most demanding system clock.

Both, separate selects and a common select, are provided to make the device well suited for both data path and random logic applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5V below V_{CC}.

- Differential D and Q; V_{BB} available
- 700ps Max. Propagation Delay
- High Frequency Outputs
- Separate and Common Select
- Extended 100E V_{EE} Range of –4.2V to –5.46V
- Internal 75kΩ Input Pulldown Resistors



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

2

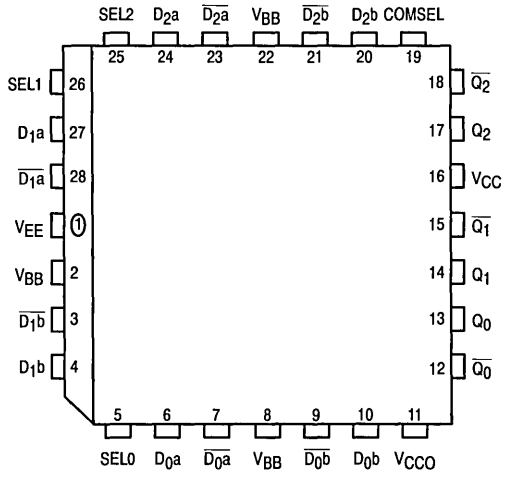
PIN NAMES

Pin	Function
Dn[0:2]; $\overline{Dn}$[0.2]	Differential Data Inputs
SEL	Individual Select Input
COMSEL	Common Select Input
V_{BB}	V_{BB} Reference Output
Q[0:2], $\overline{Q}$[0.2]	Differential Data Outputs

FUNCTION TABLE

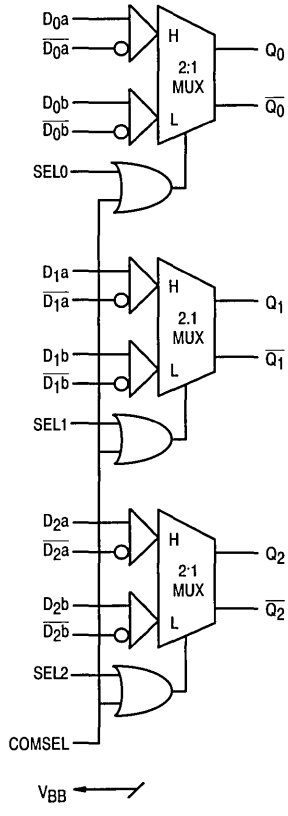
SEL	Data
H	a
L	b

Pinout: 28-Lead PLCC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



2

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

		–40°C			0°C			25°C			85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Cond**
V_{BB}	Output Reference Voltage 10E	–1.43		–1.30	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V	
	100E	–1.38		–1.26	–1.38		–1.26	–1 38		–1.26	–1.38		–1.26		
I_{IH}	Input HIGH Current			150			150			150			150	µA	
I_{EE}	Power Supply Current 10E		92	110		92	110		92	110		92	110	mA	
	100E		92	110		92	110		92	110		106	127		
V_{PP}(DC)	Input Sensitivity	50			50			50			50			mV	1
V_{CMR}	Commom Mode Range	–1.5		0	–1.5		0	–1.5		0	–1.5		0	V	2

1. Differential input voltage required to obtain a full ECL swing on the outputs
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			0°C to 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output							ps	
	D (Differential)	325	475	700	375	475	650		
	D (Single-Ended)	275	475	750	325	475	700		
	SEL	300	500	775	350	500	725		
	COMSEL	325	525	800	375	525	750		
t_{skew}	Within-Device Skew		40			40		ps	1
t_{skew}	Duty Cycle Skew $t_{PLH} - t_{PHL}$		±10			±10		ps	2
V_{PP}(AC)	Minimum Input Swing	150			150			mV	3
t_r/t_f	Rise/Fall Time	125	275	500	150	275	450	ps	20–80%

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
3. Minimum input swing for which AC parameters are guaranteed.

2

Dual ECL Output Comparator With Latch

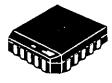
MC10E1651

DUAL ECL OUTPUT COMPARATOR WITH LATCH

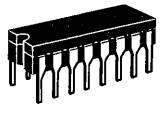
The MC10E1651 is functionally and pin-for-pin compatible with the MC1651 in the MECL III family, but is fabricated using Motorola's advanced MOSAIC III process. The MC10E1651 incorporates a fixed level of input hysteresis as well as output compatibility with 10KH logic devices. In addition, a latch is available allowing a sample and hold function to be performed. The device is available in both a 16-pin DIP and a 20-pin surface mount package.

The latch enable ($\overline{LEN_a}$ and $\overline{LEN_b}$) input pins operate from standard ECL 10KH logic levels. When the latch enable is at a logic high level the MC10E1651 acts as a comparator, hence Q will be at a logic high level if V1 > V2 (V1 is more positive than V2). $\overline{Q}$ is the complement of Q. When the latch enable input goes to a low logic level, the outputs are latched in their present state providing the latch enable setup and hold time constraints are met.

- Typ. 3.0 dB Bandwidth > 1.0 GHz
- Typ. V to Q Propagation Delay of 775 ps
- Typ. Output Rise/Fall of 350 ps
- Common Mode Range –2.0 V to +3.0 V
- Individual Latch Enables
- Differential Outputs
- 28 mV Input Hysteresis

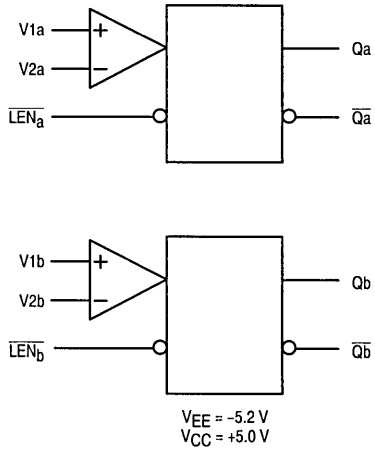


FN SUFFIX
PLASTIC PACKAGE
CASE 775-02



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

LOGIC DIAGRAM

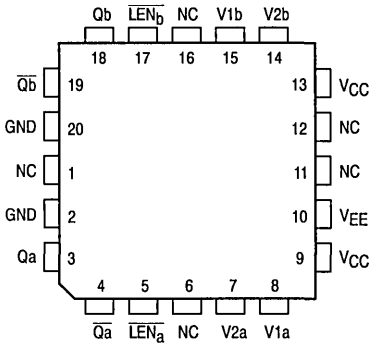


FUNCTION TABLE

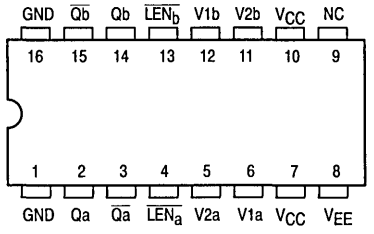
$\overline{LEN}$	V1, V2	Function
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

2

Pinout: 20-Lead PLCC (Top View)



Pinout: 16-Pin Ceramic DIP (Top View)



2

ABSOLUTE MAXIMUM RATINGS (Beyond which device life may be impaired)

Symbol	Characteristic	Min	Typ	Max	Unit
VSUP	Total Supply Voltage $\|V_{EE}\| + \|V_{CC}\|$			12.0	V
VPP	Differential Input Voltage |V1 – V2|			3.7	V

DC CHARACTERISTICS (V_{EE} = –5.2 V ±5%; V_{CC} = +5.0 V ±5%)

		0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1020		–840	–980		–810	–920		–735	mV	
V_{OL}	Output Low Voltage	–1950		–1630	–1950		–1630	–1950		–1600	mV	
II I_{IH}	Input Current (V1, V2) Input HIGH Current ($\overline{LEN}$)			65 150			65 150			65 150	µA	
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current			50 –55			50 –55			50 –55	mA	
VCMR	Common Mode Range	–2.0		3.0	–2 0		3.0	–2.0		3 0	V	
Hys	Hysteresis		27			27			30		mV	
V_{skew}	Hysteresis Skew		–1.0			–1.0			0		mV	1
C_{in}	Input Capacitance DIP PLCC			 3 2			 3 2			 3 2	pF	

Note:

1. Hysteresis skew (V_{skew}) is provided to indicate the offset of the hysteresis window. For example, at 25°C the nominal hysteresis value is 27 mV and the V_{skew} value indicates that the hysteresis was skewed from the reference level by 1 mV in the negative direction. Hence the hysteresis window ranged from 14 mV below the reference level to 13 mV above the reference level. All hysteresis measurements were determined using a reference voltage of 0 mV.

AC CHARACTERISTICS (V_{EE} = –5.2 V ±5%; V_{CC} = +5 0 V ±5%)

		0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay to Output V to Q $\overline{LEN}$ to Q	 600 400	 750 575	 900 750	 625 400	 775 575	 925 750	 700 500	 850 650	 1050 850	ps	1
t_s	Setup Time V	 450	 300		 450	 300		 550	 350		ps	
t_h	Enable Hold Time V	 –50	 –250		 –50	 –250		 –100	 –250		ps	
t_{pw}	Minimum Pulse Width $\overline{LEN}$	 400			 400			 400			ps	
t_{skew}	Within Device Skew		15			15			15		ps	2
T_{DE}	Delay Dispersion (ECL Levels)					 100 60					ps	 3, 4 3, 5
T_{DL}	Delay Dispersion (TTL Levels)					 350 100					ps	 6, 7 5, 6
t_r t_f	Rise/Fall Times 20-80%	 225	 325	 475	 225	 325	 475	 250	 375	 500	ps	

Notes:

1. The propagation delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals. For propagation delay measurements the threshold level (V_{THR}) is centered about an 850 mV input logic swing with a slew rate of 0 75 V/NS. There is an insignificant change in the propagation delay over the input common mode range
2. t_{skew} is the propagation delay skew between comparator A and comparator B for a particular part under identical input conditions.
3. Refer to figure 4 and note that the input is at 850 mV ECL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals
4. The slew rate is 0 25 V/NS for input rising edges.
5. The slew rate is 0 75 V/NS for input rising edges.
6. Refer to Figure 5 and note that the input is at 2 5 V TTL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals.
7. The slew rate is 0 3 V/NS for input rising edges.

APPLICATIONS INFORMATION

The timing diagram (Figure 3) is presented to illustrate the MC10E1651's compare and latch features. When the signal on the $\overline{LEN}$ pin is at a logic high level, the device is operating in the "compare mode," and the signal on the input arrives at the output after a nominal propagation delay (t_{PHL}, t_{PLH}). The input signal must be asserted for a time, t_s, prior to the negative going transition on $\overline{LEN}$ and held for a time, t_h, after the LEN transition. After time t_h, the latch is operating in the "latch mode," thus transitions on the input do not appear at the output. The device continues to operate in the "latch mode" until the latch is asserted once again. Moreover, the $\overline{LEN}$ pulse must meet the minimum pulse width (t_{pw}) requirement to effect the correct input-output relationship. Note that the $\overline{LEN}$ waveform in Figure 3 shows the $\overline{LEN}$ signal swinging around a reference labeled VBB_{INT}; this waveform emphasizes the requirement that $\overline{LEN}$ follow typical ECL 10KH logic levels because VBB_{INT} is the internally generated reference level, hence is nominally at the ECL VBB level.

Finally, V_{OD} is the input voltage overdrive and represents the voltage level beyond the threshold level (V_{THR}) to which the input is driven. As an example, if the threshold level is set on one of the comparator inputs as 80 mV and the input signal swing on the complementary input is from zero to 100 mV, the positive going overdrive would be 20 mV and the negative going overdrive would be 80 mV. The result of differing overdrive levels is that the devices have shorter propagation delays with greater overdrive because the threshold level is crossed sooner than the case of lower overdrive levels. Typically, semiconductor manufactures refer to the threshold voltage as the input offset voltage (VOS) since the threshold voltage is the sum of the externally supplied reference voltage and inherent device offset voltage.

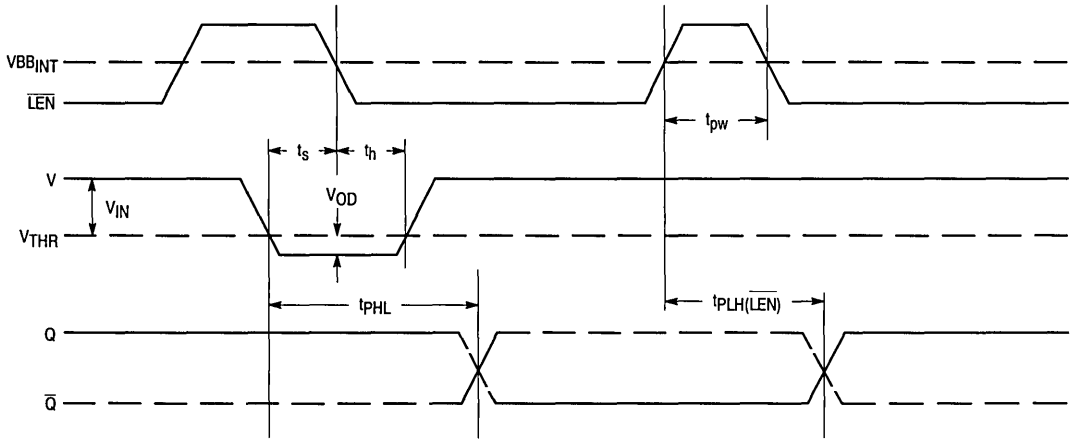


Figure 3. Input/Output Timing Diagram

2

DELAY DISPERSION

Under a constant set of input conditions comparators have a specified nominal propagation delay. However, since propagation delay is a function of input slew rate and input voltage overdrive the delay dispersion parameters, T_{DE} and T_{DT}, are provided to allow the user to adjust for these variables (where T_{DE} and T_{DT} apply to inputs with standard ECL and TTL levels, respectively).

Figure 4 and Figure 5 define a range of input conditions which incorporate varying input slew rates and input voltage overdrive. For input parameters that adhere to these constraints the propagation delay can be described as:

$T_{NOM} \pm T_{DE}$ (or T_{DT})

where T_{NOM} is the nominal propagation delay. T_{NOM} accounts for nonuniformity introduced by temperature and voltage variability, whereas the delay dispersion parameter takes into consideration input slew rate and input voltage overdrive variability. Thus a modified propagation delay can be approximated to account for the effects of input conditions that differ from those under which the parts where tested. For example, an application may specify an ECL input with a slew rate of 0.25 V/NS, an overdrive of 17 mV and a temperature of 25°C, the delay dispersion parameter would be 100 ps. The modified propagation delay would be

775ps ± 100ps

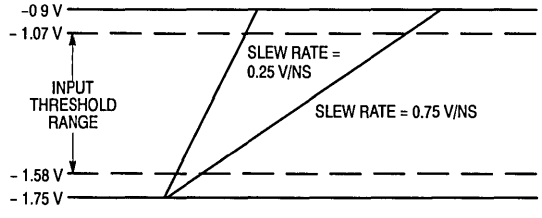


Figure 4. ECL Dispersion Test Input Conditions

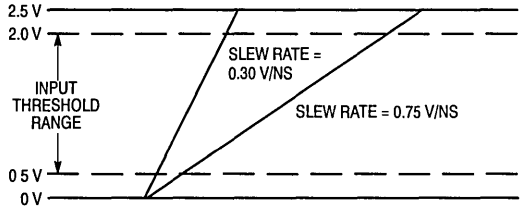


Figure 5. TTL Dispersion Test Input Conditions

Dual ECL Output Comparator With Latch

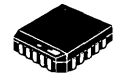
MC10E1652

DUAL ECL OUTPUT COMPARATOR WITH LATCH

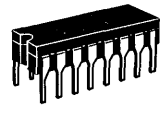
The MC10E1652 is functionally and pin-for-pin compatible with the MC10E1651 and thus the MC1651 in the MECL III™ family, but is fabricated using Motorola's advanced MOSAIC III™ process and is output compatible with 10H logic devices. In addition, the device is available in both a 16-pin DIP and a 20-pin surface mount package. However, the MC10E1652 provides user programmable hysteresis.

The latch enable ($\overline{LEN_a}$ and $\overline{LEN_b}$) input pins operate from standard ECL 10H™ logic levels. When the latch enable is at a logic high level the MC10E1652 acts as a comparator, hence Q will be at a logic high level if V1 > V2 (V1 is more positive than V2). $\overline{Q}$ is the complement of Q. When the latch enable input goes to a low logic level, the outputs are latched in their present state, providing the latch enable setup and hold time constraints are met. The level of input hysteresis is controlled by applying a bias voltage to the HYS pin.

- Typical 3.0 dB Bandwidth > 1.0 GHz
- Typical V to Q Propagation Delay of 775 ps
- Typical Output Rise/Fall of 350 ps
- Common Mode Range –2.0 V to +3.0 V
- Individual Latch Enables
- Differential Outputs
- Programmable Input Hysteresis

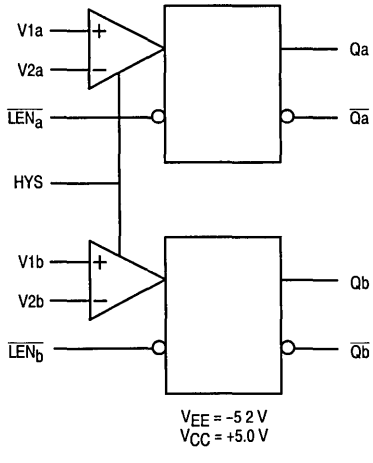


FN SUFFIX
PLASTIC PACKAGE
CASE 775-02



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

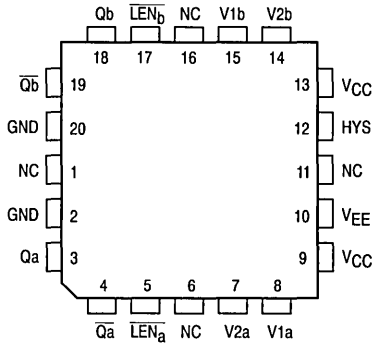
LOGIC DIAGRAM



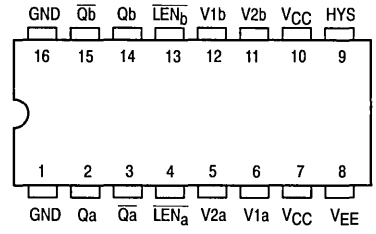
FUNCTION TABLE

$\overline{LEN}$	V1, V2	Function
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

Pinout: 20-Lead PLCC (Top View)



Pinout: 16-Pin Ceramic DIP (Top View)



ABSOLUTE MAXIMUM RATINGS (Beyond which device life may be impaired)

Symbol	Characteristic	Min	Typ	Max	Unit
VSUP	Total Supply Voltage $\|V_{EE}\| + \|V_{CC}\|$			12.0	V
VPP	Differential Input Voltage |V1 – V2|			3.7	V

DC CHARACTERISTICS (V_{EE} = –5.2 V ±5%; V_{CC} = +5.0 V ±5%)

		0°C			25°C			85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1020		–840	–980		–810	–920		–735	mV	
V_{OL}	Output Low Voltage	–1950		–1630	–1950		–1630	–1950		–1600	mV	
II I_{IH}	Input Current (V1, V2) Input HIGH Current ($\overline{LEN}$)			65 150			65 150			65 150	µA	
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current			50 –55			50 –55			50 –55	mA	
VCMR	Common Mode Range	–2.0		3.0	–2.0		3.0	–2.0		3.0	V	
Hys	Hysteresis		27			27			30		mV	1
V_{skew}	Hysteresis Skew		–1.0			–1.0			0		mV	2
C_{in}	Input Capacitance DIP PLCC			 3 2			 3 2			 3 2	pF	

1 The HYS pin programming characterization information is shown in Figure 2, The hysteresis values indicated in the data sheet are for the condition in which the voltage on the HYS pin is set to V_{EE}

2. Hysteresis skew (V_{skew}) is provided to indicate the offset of the hysteresis window For example, at 25°C the nominal hysteresis value is 27 mV and the V_{skew} value indicates that the hysteresis was skewed from the reference level by 1 mV in the negative direction Hence the hysteresis window ranged from 14 mV below the reference level to 13 mV above the reference level. All hysteresis measurements were determined using a reference voltage of 0 mV The hysteresis skew values apply over the programming range shown in Figure 2.

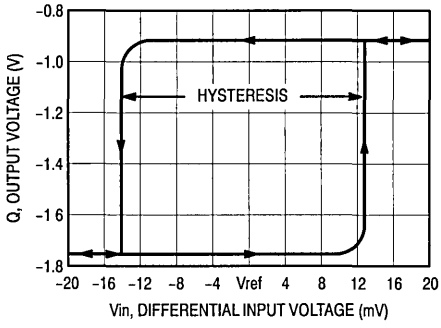


Figure 1. Typical Hysteresis Curve

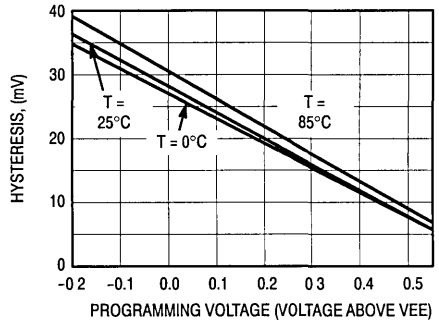


Figure 2. Hysteresis Programming Voltage

AC CHARACTERISTICS (V_{EE} = –5.2 V ±5%; V_{CC} = +5.0 V ±5%)

		0°C			25°C			85°C				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay to Output V to Q $\overline{LEN}$ to Q	 600 400	 750 575	 900 750	 625 400	 775 575	 925 750	 700 500	 850 650	 1050 850	ps	1
t_s	Setup Time V	 450	 300		 450	 300		 550	 350		ps	
t_h	Enable Hold Time V	 –50	 –250		 –50	 –250		 –100	 –250		ps	
t_{pw}	Minimum Pulse Width $\overline{LEN}$	 400			 400			 400			ps	
t_{skew}	Within Device Skew		15			15			15		ps	2
T_{DE}	Delay Dispersion (ECL Levels)					 100 60					ps	 3, 4 3, 5
T_{DL}	Delay Dispersion (TTL Levels)					 350 100					ps	 6, 7 5, 6
t_r t_f	Rise/Fall Times 20-80%	 225	 325	 475	 225	 325	 475	 250	 375	 500	ps	

Notes:

1. The propagation delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals For propagation delay measurements the threshold level (V_{THR}) is centered about an 850 mV input logic swing with a slew rate of 0 75 V/NS There is an insignificant change in the propagation delay over the input common mode range
2. t_{skew} is the propagation delay skew between comparator A and comparator B for a particular part under identical input conditions
3. Refer to Figure 4 and note that the input is at 850 mV ECL levels with the input threshold range between the 20% and 80% points The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals.
4. The slew rate is 0.25 V/NS for input rising edges
5. The slew rate is 0 75 V/NS for input rising edges
6. Refer to Figure 5 and note that the input is at 2 5 V TTL levels with the input threshold range between the 20% and 80% points The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals
7. The slew rate is 0 3 V/NS for input rising edges.

APPLICATIONS INFORMATION

The timing diagram (Figure 3) is presented to illustrate the MC10E1652's compare and latch features. When the signal on the $\overline{LEN}$ pin is at a logic high level, the device is operating in the "compare mode," and the signal on the input arrives at the output after a nominal propagation delay (t_{PHL}, t_{PLH}). The input signal must be asserted for a time, t_s, prior to the negative going transition on $\overline{LEN}$ and held for a time, t_h, after the LEN transition. After time t_h, the latch is operating in the "latch mode," thus transitions on the input do not appear at the output. The device continues to operate in the "latch mode" until the latch is asserted once again. Moreover, the $\overline{LEN}$ pulse must meet the minimum pulse width (t_{pw}) requirement to effect the correct input-output relationship. Note that the $\overline{LEN}$ waveform in Figure 3 shows the $\overline{LEN}$

signal swinging around a reference labeled VBB_{INT}; this waveform emphasizes the requirement that $\overline{LEN}$ follow typical ECL 10KH logic levels because VBB_{INT} is the internally generated reference level, hence is nominally at the ECL VBB level.

Finally, V_{OD} is the input voltage overdrive and represents the voltage level beyond the threshold level (V_{THR}) to which the input is driven. As an example, if the threshold level is set on one of the comparator inputs as 80 mV and the input signal swing on the complementary input is from zero to 100 mV, the positive going overdrive would be 20 mV and the negative going overdrive would be 80 mV. The result of differing overdrive levels is that the devices have shorter propagation delays with greater overdrive because the threshold level is crossed sooner than the case of lower overdrive levels. Typically, semiconductor manufactures refer to the threshold voltage as the input offset voltage (VOS) since the threshold voltage is the sum of the externally supplied reference voltage and inherent device offset voltage.

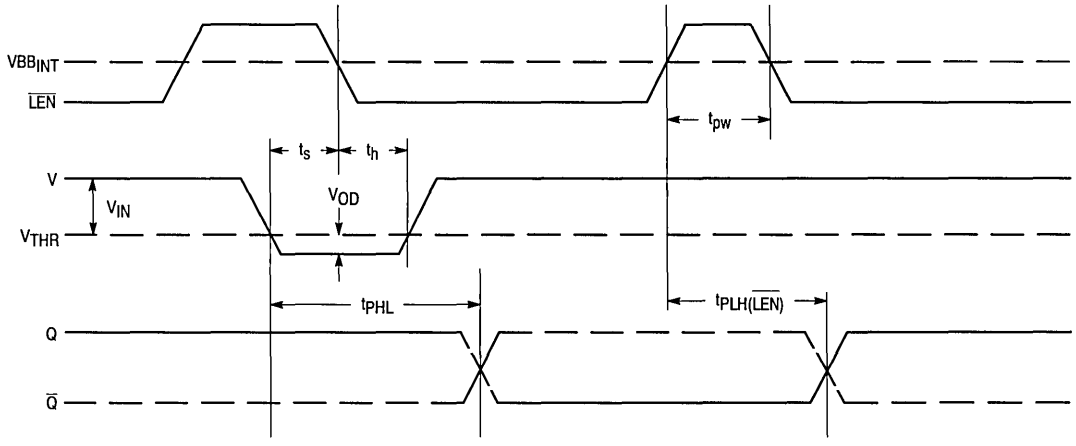


Figure 3. Input/Output Timing Diagram

DELAY DISPERSION

Under a constant set of input conditions comparators have a specified nominal propagation delay. However, since propagation delay is a function of input slew rate and input voltage overdrive the delay dispersion parameters, T_{DE} and T_{DT}, are provided to allow the user to adjust for these variables (where T_{DE} and T_{DT} apply to inputs with standard ECL and TTL levels, respectively).

Figure 4 and Figure 5 define a range of input conditions which incorporate varying input slew rates and input voltage overdrive. For input parameters that adhere to these constraints the propagation delay can be described as:

$T_{NOM} \pm T_{DE}$ (or T_{DT})

where T_{NOM} is the nominal propagation delay. T_{NOM} accounts for nonuniformity introduced by temperature and voltage variability, whereas the delay dispersion parameter takes into consideration input slew rate and input voltage overdrive variability. Thus a modified propagation delay can be approximated to account for the effects of input conditions that differ from those under which the parts where tested. For example, an application may specify an ECL input with a slew rate of 0.25 V/NS, an overdrive of 17 mV and a temperature of 25°C, the delay dispersion parameter would be 100 ps. The modified propagation delay would be

775ps ± 100ps

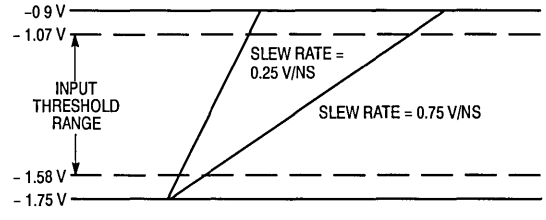


Figure 4. ECL Dispersion Test Input Conditions

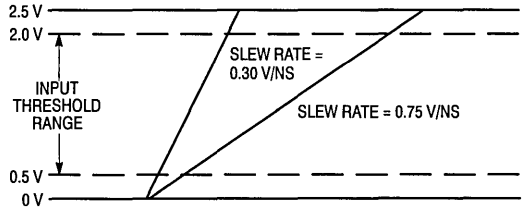
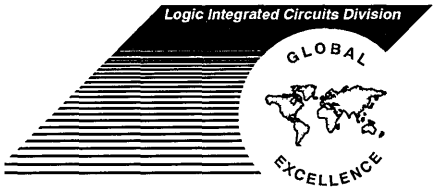


Figure 5. TTL Dispersion Test Input Conditions

ligh Performance ECL Data
CLinPS and ECLinPS Lite



This section contains AC & DC specifications r each ECLinPS Lite device type. Specifications ommon to all device types can be found in the st part of this section. While specifications nique to a particular device can be found in the ndividual data sheets following the family ecifications.

ECLinPS Lite Family Specifications & Device Data Sheets

3

)ata Sheet Classification

Advance Information — product in the sampling or pre-production stage at the time of publication.

Product Preview — product in the design stage at the time of publication.

ECLinPS *Lite* Family Specifications

Absolute Maximum Ratings

Beyond which device life maybe impaired.[1]

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	–8.0 to 0	VDC
Input Voltage (V_{CC} = 0V)	V_I	0 to –6.0	VDC
Output Current Continuous Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	–40 to +85	°C
Operating Range[1,2]	V_{EE}	–5.7 to –4 2	V

1 Unless otherwise specified on an individual data sheet.
2 Parametric values specified at: 100EL Series: –4.20V to –5.50V
10EL Series: –4.94V to –5.50V

10EL Series DC Characteristics

V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1]

		–40°C		0°C		25°C		85°C		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltge	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

1 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

100EL Series DC Characteristics

V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1]

		–40°C			0°C to 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(max)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(min)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltge	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(max)

1 This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

Applications Information

Introduction

The ECLinPS Lite family of products is very similar in design and performance as the multi-gate ECLinPS family. As a result the design guide and application notes written in support of the ECLinPS family are equally applicable to the new ECLinPS Lite family. The reader is encouraged to read through the ECLinPS Data Book to answer any general questions they may have concerning the ECLinPS Lite family. The following paragraphs will be used to describe behavior that is unique to the ECLinPS Lite family or which has not been thoroughly documented in the existing literature.

Maximum Frequency/Bandwidth

One of the goals of the ECLinPS Lite family was to provide means for using ECL in even higher frequency applications. Much effort was placed in the reduction of the output transition times as these were the limiting factors of the frequency capability of the original ECLinPS family. With a nearly 50% reduction in output edge rates the ECLinPS Lite family's frequency capability is nearly twice that of the ECLinPS devices.

The data sheets for the flip-flop devices state maximum toggle frequencies of 2.2GHz, although impressive these values tend to underestimate the useful bandwidth of the device. Similarly the buffer devices have a 3db bandwidth (600mV output swing) of about 1.4GHz, however the devices can be useful to frequencies well above 2GHz. The trick to using the ECLinPS Lite devices to their fullest capabilities is to take advantage of the differential I/O functions. From the data sheets for the differential devices the minimum input swing is 150mV, a value significantly lower than the somewhat arbitrary 600mV output chosen as the FMAX fail criteria. Figure 1 illustrates several ECLinPS Lite devices' output eye voltage versus input frequency; note for the buffer type devices the outputs produce a 150mV eye pattern for frequencies well over 3GHz.

Traditionalist may argue that 150mV input swings leave no noise margins for the design, when analyzed further this is not the case. For single-ended interconnect the worst case noise margins are ≈150mV with no common mode noise rejection capabilities. For a 150mV differential input the same 150mV of noise margin exists, however in this case the interface also has common mode noise rejection capability and thus may provide a safer environment than a standard single-ended interface.

The purpose of this discussion is to illustrate the potential of using ECLinPS Lite devices at frequencies well above the stated maximum limits. The criteria for establishing the maximum frequency of a device was determined with single-ended interfaces in mind, however in the 1GHz+ realm of designs differential interconnect is predominant. For differential interconnect systems the criteria for FMAX needs to be redefined to better describe the reliable operating frequency range of a device. Under this new set of criteria the ECLinPS Lite family can be pushed well above 2.5GHz and thus provide a cost effective means for processing very high speed signals.

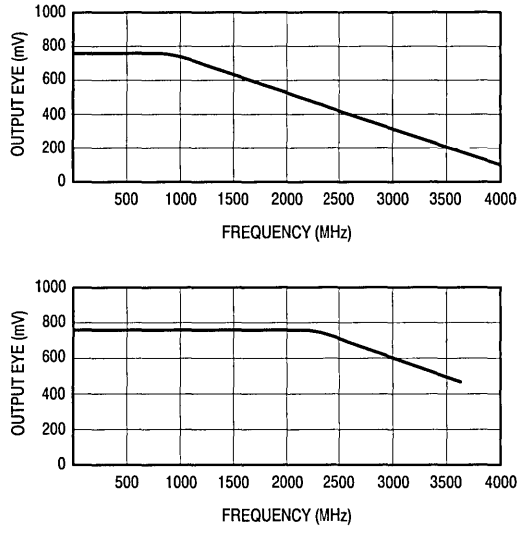


Figure 1. Eye Pattern versus Frequency

Using ECLinPS Lite in PECL Designs

PECL is an acronym for Positive ECL and simply represents using standard ECL devices in a +5.0V environment. All of the ECLinPS Lite devices, as with the majority of all ECL devices, will operate as specified when positive power supplies are used. The reason for the use of negative power supplies with ECL is due to the fact that the output levels and internal bias levels are V_{CC} rail referenced. Because ground is simpler to keep quiet than a power supply, it was the natural choice for the V_{CC} bias. Because the output levels vary 1:1 with V_{CC}, differences in power supply levels between transmitter and receiver can be problematic. These problems can be eliminated if differential interconnect is used. A thorough discussion on this subject can be found in the PECL application note (Designing With PECL – AN1406/D) available from a Motorola representative.

With its small size and low power the ECLinPS Lite family of products will naturally find applications in PECL form in otherwise TTL or CMOS systems. Many of these applications will be in the area of clock distribution. Because minimizing skew is the most important aspect of clock distribution differential interconnect should be used. This not only minimizes skew, but as previously mentioned, it also eliminates problems due to V_{CC} variation in PECL designs. Again, refer to the Motorola application note (ECL Clock Distribution Techniques – AN1405/D) dealing with using ECL in clock distribution applications for a more detailed discussion.

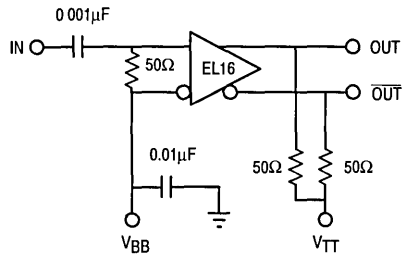


Figure 2. AC Coupling Architecture

An important aspect of using ECLinPS Lite in clock distribution schemes is in the interface to the clock source. By taking advantage of the AC coupling capability of the EL16, or any other differential input device which also features a V_{BB} output, ECLinPS Lite products can be interfaced to clock sources which generate other than ECL compatible outputs. Probably the most cost efficient and simplest oscillators to choose are sinusoidal oscillators. By using the architecture of Figure 2 a sinusoidal oscillators can be used to drive ECLinPS Lite devices. The only criteria is that the amplitude of the oscillator input not exceed the upper or lower end of the CMR range when centered on the V_{BB} reference. A larger amplitude oscillator output can be used if a lower DC bias is used or if the output of the oscillator is voltage divided prior to being coupled into the EL16.

Input Clamp Circuitry and CMR Range

To maintain stability during open input situations all of the differential input devices employ input clamping circuitry. Because all of the inputs of ECLinPS Lite devices have internal input pulldown resistors when left open the inputs will pull down to V_{EE}. A clamp voltage will take control of the input buffer when both inputs pull lower than the clamp voltage. This clamp voltage does place a lower bound on the CMR range of a device. In the ECLinPS Lite family the internal clamp voltage is referenced to the V_{EE} power rail, as a result if a larger CMR range is necessary the V_{EE} of a device can be lowered. Each incremental lowering of V_{EE} will increase the CMR range by an equivalent amount.

Package Information

The package chosen for the ECLinPS Lite family is the standard 8-lead SOIC package. The 8-lead SOIC is a plastic surface mount package with gull wing, 50mil pitch leads. Figure 3 illustrates the recommended PCB solder pads for the 8-lead SOIC and Figure 5 on the following page outlines the various package dimensions.

Because the SOIC is a plastic package the long term reliability of a device is going to be dependent on the operating junction temperature. As the junction temperature of the device increases an intermetallic is formed between the gold bond wire and the aluminum bonding pad. This intermetallic eventually causes a void to develop and the affected pin to become an open circuit. For a more detailed discussion on the subject refer to the Package and Thermal section of the ECLinPS data book.

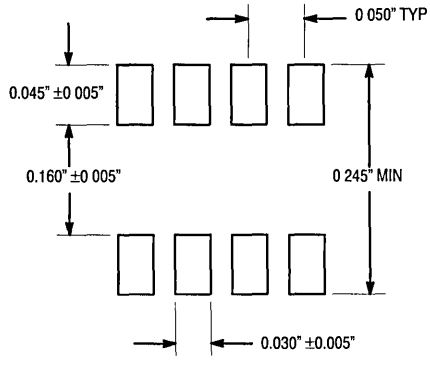


Figure 3. 8-Lead SOIC Solder Pad Dimensions

The 8-lead SOIC exhibits a thermal resistance as pictured in Figure 5. With this information as well as the power dissipation of the device in question (calculated as shown in the thermal section of the ECLinPS Data Book) the approximate junction temperature and thus theoretical lifetime can be estimated. ECLinPS Lite devices are designed with chip power levels that permit acceptable reliability levels, in most systems, under the conventional 500lfpm (2.5m/s) airflow. In fact, for all systems but those that operate at the maximum allowed ambient temperatures ECLinPS Lite devices will prove reliable with little or no cooling airflow.

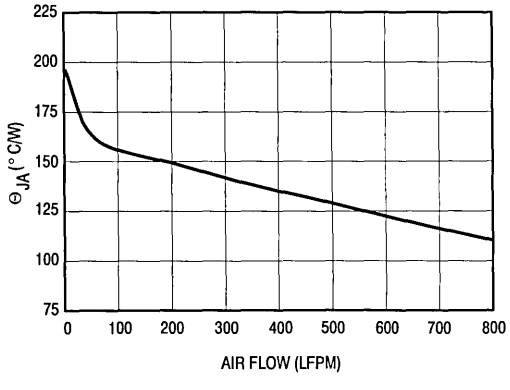


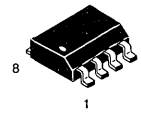
Figure 4. 8-Lead SOIC Thermal Resistance

4-Input OR/NOR

MC10EL01
MC100EL01

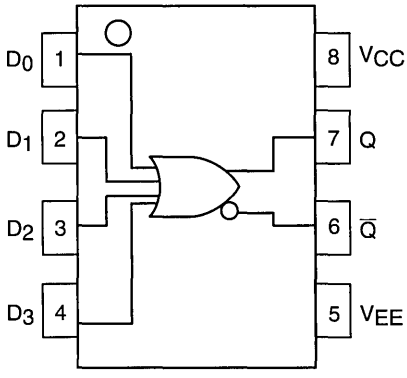
The MC10EL/100EL01 is a 4-input OR/NOR gate. The device is functionally equivalent to the E101 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E101 the EL01 is ideally suited for those applications which require the ultimate in AC performance.

- 230ps Propagation Delay
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0–D3	Data Inputs
Q	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		14		11	14	17	11	14	17	11	14	17	mA
		100EL		14		11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		100EL	–4.20	–4.5	–5 5	–4 20	–4 5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5 5	
I_{IH}	Input HIGH Current				150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

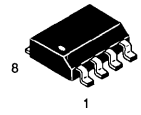
Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output		220		120	220	320	130	230	330	150	250	350	ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

2-Input AND/NAND

MC10EL04
MC100EL04

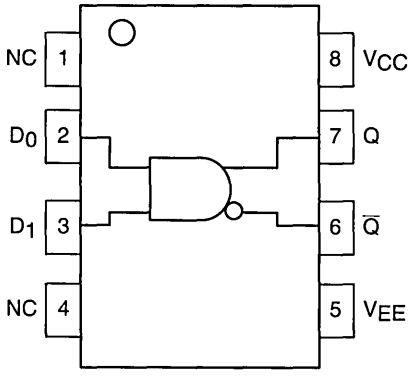
The MC10EL/100EL04 is a 2-input AND/NAND gate. The device is functionally equivalent to the E104 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E104 the EL04 is ideally suited for those applications which require the ultimate in AC performance.

- 240ps Propagation Delay
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	Data Inputs
Q	Data Outputs

3

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current 10EL		14		11	14	17	11	14	17	11	14	17	mA
	100EL		14		11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage 10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.75	–5.2	–5 5	–4.75	–5 2	–5.5	V
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4 5	–5.5	
I_{IH}	Input HIGH Current D0			250			250			250			250	µA
	D1			150			150			150			150	

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output		235		120	235	360	130	240	370	155	265	395	ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

2-Input Differential AND/NAND

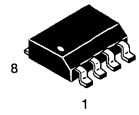
MC10EL05
MC100EL05

The MC10EL/100EL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the E404 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E404 the EL05 is ideally suited for those applications which require the ultimate in AC performance.

Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the EL05 to also be used as a 2-input differential OR/NOR gate.

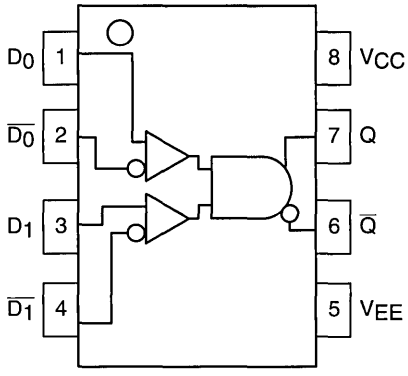
The differential inputs employ clamp circuitry so that under open input conditions (pulled down to V_{EE}) the input to the AND gate will be HIGH. In this way, if one set of inputs is open, the gate will remain active to the other input.

- 275ps Propagation Delay
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	Data Inputs
Q	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		-40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current													
	10EL		18		14	18	22	14	18	22	14	18	22	
	100EL		18		14	18	22	14	18	22	16	21	25	mA
V_{EE}	Power Supply Voltage													
	10EL	-4.75	-5.2	-5.5	-4.75	-5.2	-5.5	-4.75	-5.2	-5 5	-4 75	-5 2	-5 5	
	100EL	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4.5	-5.5	-4.20	-4 5	-5.5	V
I_{IH}	Input HIGH Current			150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{PLH} t_{PHL}	Propagation Delay to Output		260		185	275	390	185	275	390	215	305	420	ps
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
V_{CMR}	Common Mode Range[2]	–0.4		See[2]	–0.4		See[2]	–0 4		See[2]	–0.4		See[2]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

1 Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

2 The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

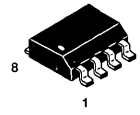
3

2-Input XOR/XNOR

MC10EL07
MC100EL07

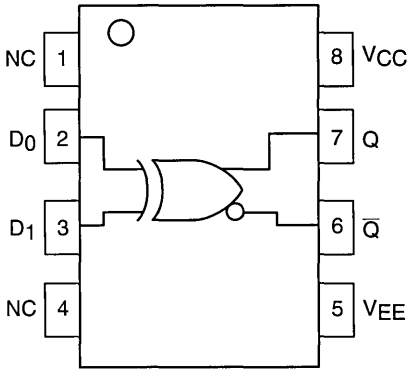
The MC10EL/100EL07 is a 2-input XOR/XNOR gate. The device is functionally equivalent to the E107 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E107 the EL07 is ideally suited for those applications which require the ultimate in AC performance.

- 260ps Propagation Delay
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	Data Inputs
Q	Data Outputs

3

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current 10EL		14		11	14	17	11	14	17	11	14	17	mA
	100EL		14		11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage 10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
	100EL	–4.20	–4 5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current D0			250			250			250			250	µA
	D1			150			150			150			150	

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output		250		140	250	385	150	260	395	170	280	415	ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

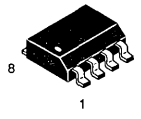
1:2 Differential Fanout Buffer

MC10EL11
MC100EL11

The MC10EL/100EL11 is a differential 1:2 fanout gate. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the EL11 is ideally suited for those applications which require the ultimate in AC performance.

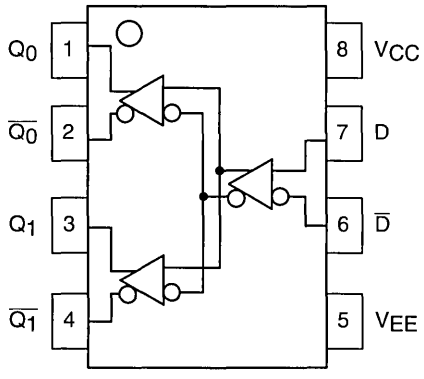
The differential inputs of the EL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}) the Q outputs will go LOW.

- 265ps Propagation Delay
- 5ps Skew Between Outputs
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D	Data Inputs
Q0, Q1	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current													mA
	10EL		26		21	26	31	21	26	31	21	26	31	
	100EL		26		21	26	31	21	26	31	24	30	36	
V_{EE}	Power Supply Voltage													V
	10EL	–4.75	–5.2	–5.5	–4 75	–5 2	–5.5	–4.75	–5 2	–5 5	–4.75	–5 2	–5 5	
	100EL	–4 20	–4.5	–5.5	–4.20	–4.5	–5 5	–4.20	–4.5	–5 5	–4.20	–4.5	–5 5	
I_{IH}	Input HIGH Current			150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{PLH} t_{PHL}	Propagation Delay to Output		260		185	260	335	190	265	340	215	290	365	ps
t_{SKEW}	Within-Device Skew[1] Duty Cycle Skew[2]		5 5			5 5	20 20		5 5	20 20		5 5	20 20	ps
V_{PP}	Minimum Input Swing[3]	150			150			150			150			mV
V_{CMR}	Common Mode Range[4]	–0.4		See[4]	–0.4		See[4]	–0.4		See[4]	–0.4		See[4]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

1 Within-device skew defined as identical transitions on similar paths through a device.

2 Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.

3 Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

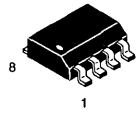
4 The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

Low Impedance Driver

MC10EL12
MC100EL12

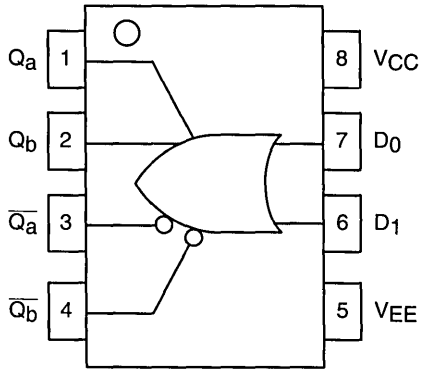
The MC10EL/100EL12 is a low impedance drive buffer. With two pairs of OR/NOR outputs the device is ideally suited for high drive applications such as memory addressing. The device is a function equivalent to the E112 device with higher performance capabilities. With propagation delays significantly faster than the E112 the EL12 is ideally suited for those applications which require the ultimate in AC performance.

- 290ps Propagation Delay
- Dual Outputs for 25Ω Drive Applications
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	Data Inputs
Qa, Qb	Data Outputs

3

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current 10EL		14		11	14	17	11	14	17	11	14	17	mA
	100EL		14		11	14	17	11	14	17	13	16	20	
V_{EE}	Power Supply Voltage 10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4 94	–5 2	–5.5	V
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current			150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output		280		170	280	450	180	290	450	210	320	480	ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		350		150	350	550	150	350	550	150	350	550	ps

Advance Information

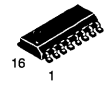
1:4 Clock Distribution Chip

MC10EL15
MC100EL15

The MC10EL/100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01μF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

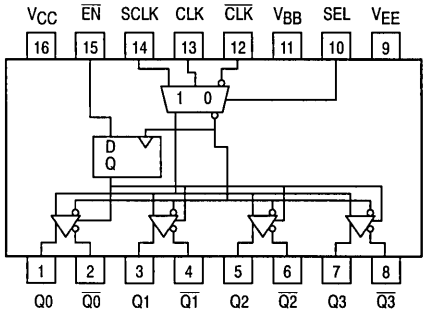
The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
SCLK	Scan Clock Input
$\overline{EN}$	Sync Enable
SEL	Clock Select Input
V_{BB}	Reference Output
Q_{0-3}	Diff Clock Outputs

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}	Operating Range[1,2]	–5.7 to –4.2	V

1 Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2 Parametric values specified at:
100EL Series:
–4 20V to –5.50V
10EL Series:
–4.94V to –5.50V

10EL SERIES
DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C		0°C		25°C		85°C		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltge	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

1 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

100EL SERIES
DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C			0°C to 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(max)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(min)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltge	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(max)

1 This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

AC/DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		25	35		25	35		25	35		25	35	mA
V_{BB}	Output Reference 10EL Voltage 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1 19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Propagation Delay CLK to Q t_{PLH} t_{PHL} SCLK to Q t_{PLH} t_{PHL}				420 500 350 400	520 600 500 550	620 700 650 700	440 520 350 400	540 620 500 550	640 720 650 700	480 560 410 460	580 660 560 610	680 760 710 760	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew[1]			200 50			200 50			200 50			200 50	ps
t_S	Setup Time $\overline{EN}$	100			100			100			100			ps
t_H	HoldTime $\overline{EN}$	500			500			500			500			ps
V_{PP}	Minimum Input Swing CLK	250			250			250			250			mV
V_{CMR}	Common Mode Range CLK	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	–2.0		–0 4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)				325		575	325		575	325		575	ps

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.

3

Differential Receiver

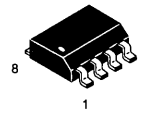
MC10EL16
MC100EL16

The MC10EL/100EL16 is a differential receiver. The device is functionally equivalent to the E116 device with higher performance capabilities. With output transition times significantly faster than the E116 the EL16 is ideally suited for interfacing with high frequency sources.

The EL16 provides a V_{BB} output for either single-ended use or as a DC bias for AC coupling to the device. The V_{BB} pin should be used only as a bias for the EL16 as its current sink/source capability is limited. Whenever used, the V_{BB} pin should be bypassed to ground via a 0.01µf capacitor.

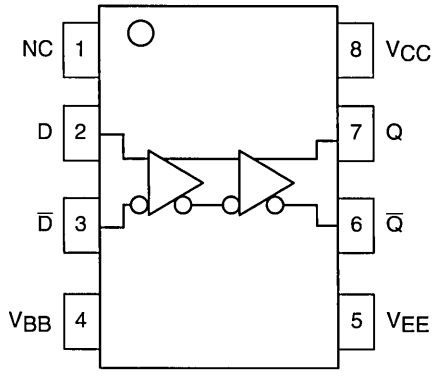
Under open input conditions (pulled to V_{EE}) internal input clamps will force the Q output LOW.

- 250ps Propagation Delay
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D	Data Inputs
Q	Data Outputs
V_{BB}	Ref. Voltage Output

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		−40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		18		14	18	22	14	18	22	14	18	22	mA
		100EL		18		14	18	22	14	18	22	16	21	26	
V_{BB}	Output Reference Voltage	10EL	−1.43		−1.30	−1.38		−1.27	−1.35		−1.25	−1.31		−1.19	V
		100EL	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	−1.38		−1 26	
V_{EE}	Power Supply Voltage	10EL	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	V
		100EL	−4.20	−4.5	−5.5	−4.20	−4.5	−5 5	−4.20	−4.5	−5 5	−4 20	−4.5	−5 5	
I_{IH}	Input HIGH Current				150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
t_{PLH} t_{PHL}	Propagation Delay to Output (Diff) (SE)		250 250		175 125	250 250	325 375	175 125	250 250	325 375	205 155	280 280	355 405	ps
t_{SKEW}	Duty Cycle Skew[1] (Diff)		5			5	20		5	20		5	20	ps
V_{PP}	Minimum Input Swing[2]	150			150			150			150			mV
V_{CMR}	Common Mode Range[3]	–0.4		See[3]	–0.4		See[3]	–0.4		See[3]	–0.4		See[3]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

1 Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.

2 Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

3 The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

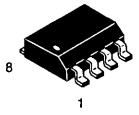
D Flip-Flop With Set and Reset

MC10EL31
MC100EL31

The MC10EL/100EL31 is a D flip-flop with set and reset. The device is functionally equivalent to the E131 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E131 the EL31 is ideally suited for those applications which require the ultimate in AC performance.

Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

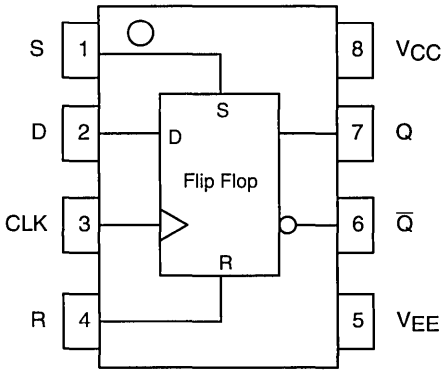
- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

D	S	R	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	H	X	Undef

Z = LOW to HIGH Transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		23		18	27	32	18	27	32	18	27	32	mA
		100EL		23		18	27	32	18	27	32	21	31	37	
V_{EE}	Power Supply Voltage	10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4 5	–5.5	–4.20	–4.5	–5 5	
I_{IH}	Input HIGH Current				150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		2.5		2.2	2.8		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R		 465 455		 365 345	 465 455	 580 580	 375 355	 475 465	 590 590	 430 400	 530 510	 645 645	ps
t_S t_H	Setup Time Hold Time		0 100		150 250	0 100		150 250	0 100		150 250	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			400			ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

3

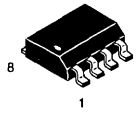
÷2 Divider

MC10EL32
MC100EL32

The MC10EL/100EL32 is an integrated ÷2 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01μF capacitor. Also note that the V_{BB} is designed to be used as an input bias on the EL32 only, the V_{BB} output has limited current sink and source capability.

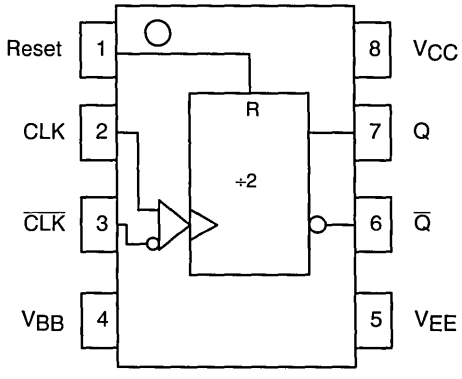
The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32's in a system.

- 510ps Propagation Delay
- 3.0GHz Toggle Frequency
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	Clock Inputs
Reset	Asynch Reset
V_{BB}	Ref Voltage Output
Q	Data Ouputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		25			25	30		25	30		25	30	mA
		100EL		25			25	30		25	30		29	35	
V_{EE}	Power Supply Voltage	10EL		–5 2		–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		100EL		–4.5		–4.20	–4.5	–5.5	–4.20	–4.5	–5 5	–4.20	–4 5	–5.5	
V_{BB}	Output Reference Voltage	10EL	–1 43		–1.30	–1.38		–1 27	–1.35		–1.25	–1.31		–1.19	V
		100EL	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	
I_{IH}	Input HIGH Current				150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		3.0		2.6	3.0		2.6	3.0		2.6	3 0		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q		 500 540		 410 440	 500 540	 590 640	 420 440	 510 540	 600 640	 450 450	 540 550	 630 650	 ps
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

1 Minimum input swing for which AC parameters are guaranteed

3

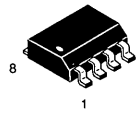
÷4 Divider

MC10EL33
MC100EL33

The MC10EL/100EL33 is an integrated ÷4 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01µF capacitor. Also note that the V_{BB} is designed to be used as an input bias on the EL33 only, the V_{BB} output has limited current sink and source capability.

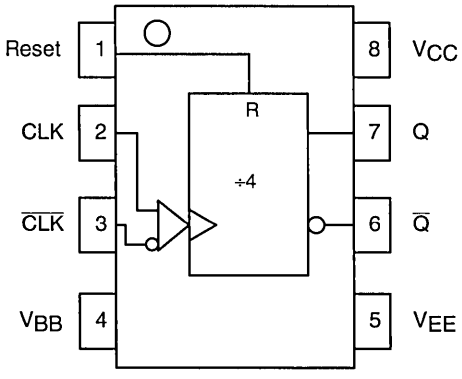
The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EL33's in a system.

- 650ps Propagation Delay
- 4.0GHz Toggle Frequency
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	Clock Inputs
Reset	Asynch Reset
V_{BB}	Ref Voltage Output
Q	Data Ouputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		27			27	33		27	33		27	33	mA
		100EL		27			27	33		27	33		31	37	
V_{EE}	Power Supply Voltage	10EL		–5 2		–4.75	–5 2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		100EL		–4.5		–4.20	–4.5	–5 5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
V_{BB}	Output Reference Voltage	10EL	–1.43		–1.30	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V
		100EL	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	
I_{IH}	Input HIGH Current				150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		4.2		3.8	4.2		3 8	4.2		3 8	4.2		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q		 630 460		 540 360	 630 460	 720 560	 550 360	 640 460	 730 560	 590 380	 670 480	 760 580	 ps
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

[1] Minimum input swing for which AC parameters are guaranteed.

3

MC10EL34
MC100EL34

Product Preview

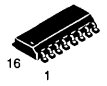
÷2, ÷4, ÷8 Clock Generation Chip

The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS™ Data Book DL140/D). If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL34 under single-ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

PIN DESCRIPTION

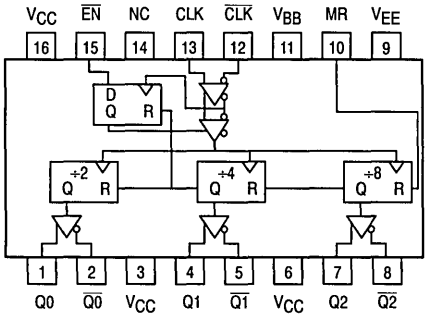
PIN	FUNCTION
CLK	Diff Clock Inputs
$\overline{EN}$	Sync Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0	Diff ÷2 Outputs
Q_1	Diff ÷4 Outputs
Q_2	Diff ÷8 Outputs

FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

Z = Low-to-High Transition
ZZ = High-to-Low Transition

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development Motorola reserves the right to change or discontinue this product without notice

AC/DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		65			65			65			65		mA
V_{BB}	Output Reference 10EL Voltage 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1 38		–1.19 –1.26	V
I_{IH}	Input High Current	150					150			150			150	µA
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR		1100 800			1100 800			1100 800			1100 800		ps
t_{SKEW}	Within-Device Skew		100			100			100			100		ps
t_S	Setup Time $\overline{EN}$		150			150			150			150		ps
t_H	Hold Time $\overline{EN}$		150			150			150			150		ps
V_{PP}	Minimum Input Swing CLK	250			250			250			250			mV
V_{CMR}	Common Mode Range CLK	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		400			400			400			400		ps

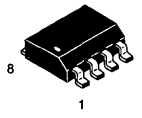
3

JK Flip-Flop

MC10EL35
MC100EL35

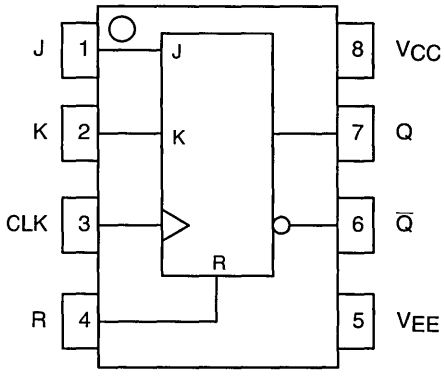
The MC10EL/100EL35 is a high speed JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

- 525ps Propagation Delay
- 2.2GHz Toggle Frequency
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

J	K	R	CLK	Qn+1
L	L	L	Z	Qn
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	$\overline{Qn}$
X	X	H	X	L

Z = LOW to HIGH Transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		27			27	32		27	32		27	32	mA
		100EL		27			27	32		27	32		32	37	
V_{EE}	Power Supply Voltage	10EL		–5.2		–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		100EL		–4.5		–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current				150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		2 0		1.8	2.2		1.8	2 2		1.8	2.2		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output MR		515 450		340 275	515 450	690 625	350 275	525 450	700 625	395 350	570 525	745 700	ps
t_S	Setup Time J, K		0		150	0		150	0		150	0		ps
t_H	Hold Time J, K		100		250	100		250	100		250	100		ps
t_{RR}	Reset Recovery	400	200		400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Reset	400			400			400			400			ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

3

Differential Clock D Flip-Flop

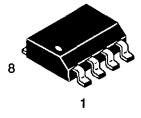
MC10EL51
MC100EL51

The MC10EL/100EL51 is a differential clock D flip-flop with reset. The device is functionally similar to the E151 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E151 the EL51 is ideally suited for those applications which require the ultimate in AC performance.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input (pulled down to V_{EE}) conditions.

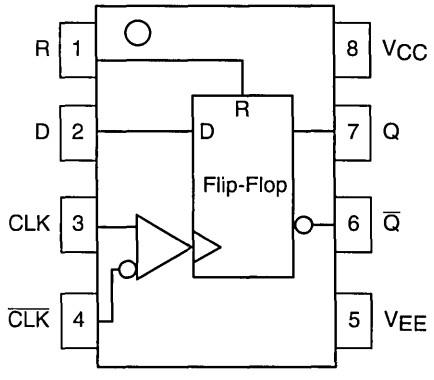
- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		−40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		24		19	24	29	19	24	29	19	24	29	mA
		100EL		24		19	24	29	19	24	29	24	30	36	
V_{EE}	Power Supply Voltage	10EL	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	−4.75	−5.2	−5.5	V
		100EL	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	
I_{IH}	Input HIGH Current				150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		2.8		2.2	2.8		2 2	2.8		2 2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R		465 455		375 355	465 455	555 555	385 355	475 465	565 565	440 410	530 510	620 620	ps
t_S	Setup Time		0		150	0		150	0		150	0		ps
t_H	Hold Time		100		250	100		250	100		250	100		ps
t_{RR}	Reset Recovery	400	200		400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Reset	400			400			400			400			ps
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
V_{CMR}	Common Mode Range[2]	–0 4		See[2]	–0.4		See[2]	–0.4		See[2]	–0.4		See[2]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

1 Minimum input swing for which AC parameters are guaranteed.

2 The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

3

Differential Data and Clock D Flip-Flop

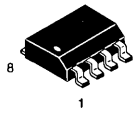
MC10EL52
MC100EL52

The MC10EL/100EL52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the E452 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452 the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL52 allow the device to also be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that under open input conditions (pulled down to V_{EE}) the outputs of the device will remain stable.

- 365ps Propagation Delay
- 2.0GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

PIN DESCRIPTION

PIN	FUNCTION
D	Data Input
CLK	Clock Input
Q	Data Output

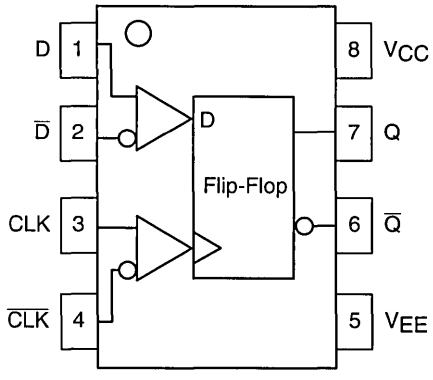
TRUTH TABLE

D	CLK	Q
L	Z	L
H	Z	H

Z = LOW to HIGH Transition

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	10EL		21		17	21	25	17	21	25	17	21	25	mA
		100EL		21		17	21	25	17	21	25	19	24	29	
V_{EE}	Power Supply Voltage	10EL	–4.94	–5.2	–5.5	–4.94	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current				150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		2 5		2 2	2.8		2 2	2.8		2 2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK		335		275	365	465	275	365	465	320	410	510	ps
t_S	Setup Time		0		125	0		125	0		125	0		ps
t_H	Hold Time		50		150	50		150	50		150	50		ps
t_{PW}	Minimum Pulse Width	400			400			400			400			ps
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
V_{CMR}	Common Mode Range[2]													V
	D (10EL)	–0.4		–1 6	–0.4		–1.6	–0.4		–1 6	–0.4		–1.6	
	D (100EL)	–0.4		–1.2	–0.4		–1.2	–0.4		–1.2	–0.4		–1.2	
	CLK (10EL)	–0.6		See[3]	–0.6		See[3]	–0 6		See[3]	–0 6		See[3]	
	CLK (100EL)	–0.8		See[3]	–0.8		See[3]	–0.8		See[3]	–0.8		See[3]	
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		225		100	225	350	100	225	350	100	225	350	ps

1 Minimum input swing for which AC parameters are guaranteed.

2 The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

3 The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

3

Advance Information

4:1 Differential Multiplexer

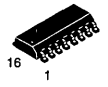
MC10EL57
MC100EL57

The MC10/100EL57 is a fully differential 4:1 multiplexer. By leaving the SEL1 line open (pulled LOW via the input pulldown resistors) the device can also be used as a differential 2:1 multiplexer with SEL0 input selecting between D0 and D1. The fully differential architecture of the EL57 makes it ideal for use in low skew applications such as clock distribution.

The SEL1 is the most significant select line. The binary number applied to the select inputs will select the same numbered data input (i.e., 00 selects D0).

Multiple V_{BB} outputs are provided for single-ended or AC coupled interfaces. In these scenarios, the V_{BB} output should be connected to the data bar inputs and bypassed via a 0.01µF capacitor to ground. Note that the V_{BB} output can source/sink up to 0.5mA of current without upsetting the voltage level.

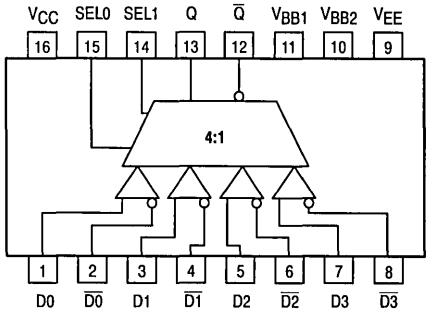
- Useful as Either 4:1 or 2:1 Multiplexer
- V_{BB} Output for Single-Ended Operation
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0–3	Diff Data Inputs
SEL0,1	Mux Select Inputs
V_{BB}	Reference Output
Q0	Data Outputs

FUNCTION TABLE

SEL1	SEL0	DATA OUT
L	L	D0
L	H	D1
H	L	D2
H	H	D3

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}	Operating Range[1,2]	–5.7 to –4.2	V

1 Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2 Parametric values specified at: 100EL Series: –4.20V to –5.50V 10EL Series: –4.94V to –5.50V

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

10EL SERIES
DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C		0°C		25°C		85°C		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltge	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0 5	—	0.5	—	0.3	—	µA

1 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

100EL SERIES
DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

		–40°C			0°C to 85°C				
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(max)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(min)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltge	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(max)

1 This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

AC/DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

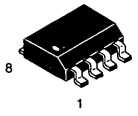
		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		15	20		15	20		15	20		15	20	mA
V_{BB}	Output Reference 10EL Voltage 100EL	–1.43 –1.38		–1 30 –1.26	–1.38 –1 38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1.19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Propagation Delay DATA to Q/$\overline{Q}$ t_{PLH} t_{PHL} SEL to Q/$\overline{Q}$ t_{PLH} t_{PHL}				400 340 400 450	500 440 525 575	600 540 650 700	400 340 400 450	500 440 525 575	600 540 650 700	440 370 450 480	540 470 575 605	640 570 700 730	ps
t_{SKEW}	Input Skew D_n, D_m to Q		TBD			TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing CLK	150			150			150			150			mV
V_{CMR}	Common Mode Range CLK	–2.0		–0 4	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	125		375	125		375	125		375	125		375	ps

2:1 Multiplexer

MC10EL58
MC100EL58

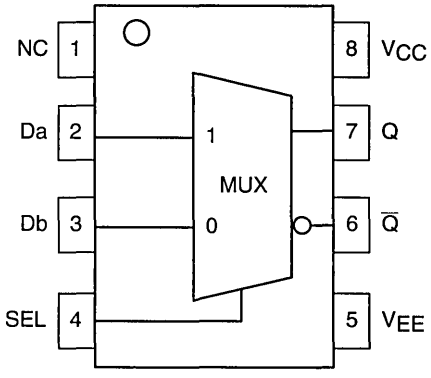
The MC10EL/100EL58 is a 2:1 multiplexer. The device is functionally equivalent to the E158 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E158 the EL58 is ideally suited for those applications which require the ultimate in AC performance.

- 230ps Propagation Delay
- High Bandwidth Output Transitions
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



FUNCTION TABLE

SEL	Data
H	a
L	b

PIN DESCRIPTION

PIN	FUNCTION
D0, D1	Data Inputs
Q	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current 10EL		14		11	14	17	11	14	17	11	14	17	mA
	100EL		14		11	14	17	11	14	17	13	16	19	
V_{EE}	Power Supply Voltage 10EL	−4.94	−5.2	−5.5	−4.94	−5.2	−5.5	−4.75	−5 2	−5.5	−4.75	−5.2	−5.5	V
	100EL	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	−4.20	−4.5	−5.5	
I_{IH}	Input HIGH Current			150			150			150			150	µA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

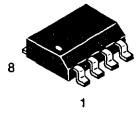
Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q		220		110	220	330	120	230	340	140	250	360	ps
	SEL to Q		250		140	250	360	150	260	370	170	280	390	
t_r t_f	Output Rise/Fall Times Q (20% − 80%)		225		100	225	350	100	225	350	100	225	350	ps

Coaxial Cable Driver

MC10EL89

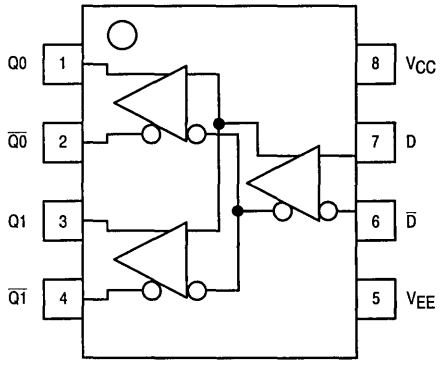
The MC10EL/100EL89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in Digital Video Broadcasting applications; for this application, since the system is polarity free, each output can be used as an idependent driver. The driver boasts a gain of approximately 40 and produces output swings twice as large as a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6V output swings allow for termination at both ends of the cable, while maintaining the required 800mV swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard –2.0V. All of the DC parameters are tested with a 50Ω to –3.0V load. The driver accepts a standard differential ECL input and can run off of the Digital Video Broadcast standard –5.0V supply.

- 375ps Propagation Delay
- 1.6V Output Swings
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D	Data Inputs
Q0, Q1	Data Outputs

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	18	23	28	18	23	28	18	23	28	18	23	28	mA
V_{OH}	Output HIGH Voltage[1]	–1.23	–1.10	–0.98	–1.17	–1.05	–0.93	–1.13	–1.02	–0 90	–1.06	–0.96	–0.81	V
V_{OL}	Output LOW Voltage[1]	–2.84	–2.72	–2.58	–2.84	–2.70	–2.56	–2.84	–2.70	–2.56	–2.84	–2 67	–2.51	V
V_{EE}	Power Supply Voltage	–4.75		–5.5	–4.75		–5.5	–4.75		–5.5	–4.75		–5.5	V
I_{IH}	Input HIGH Current			150			150			150			150	µA

[1] V_{OH} and V_{OL} specified for 50Ω to –3.0V load.

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay to Output		340		250	340	430	260	350	440	310	400	490	ps
t_{SKEW}	Within-Device Skew		5	20		5	20		5	20		5	20	
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
V_{CMR}	Common Mode Range[2]	–0.4		See[2]	–0.4		See[2]	–0.4		See[2]	–0.4		See[2]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		330		205	330	455	205	330	455	205	330	455	ps

1 Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

2 The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 3.0V.

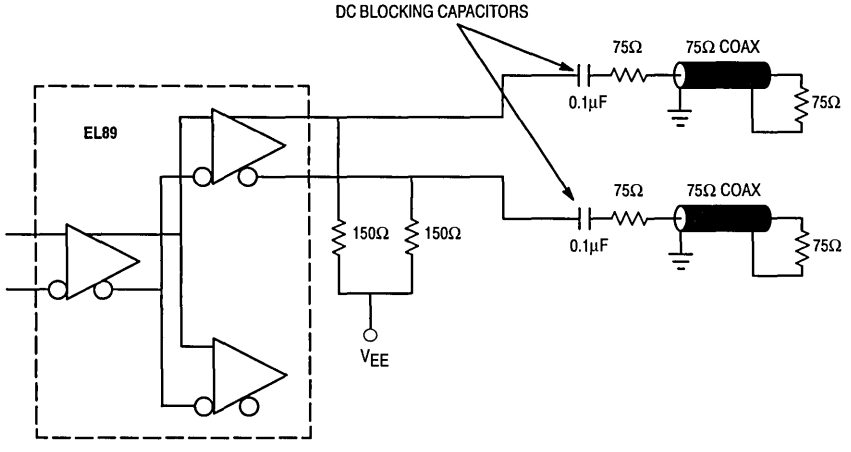


Figure 1. EL89 Termination Configuration

ECLinPS Lite Translators

Product Preview

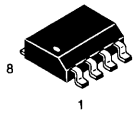
TTL to Differential PECL Translator

MC10ELT20
MC100ELT20

The MC10ELT/100ELT20 is a TTL to differential PECL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the single gate of the ELT20 makes it ideal for those applications where space, performance and low power are at a premium. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The ELT20 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

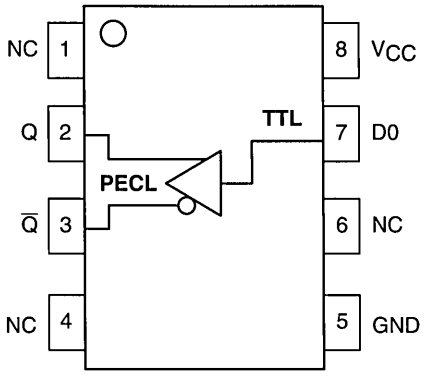
- 1.5ns Typical Propagation Delay
- Differential PECL Outputs
- Small Outline SOIC Package
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q	Diff PECL Outputs
D	TTL Input
V_{CC}	+5.0V Supply
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

Product Preview

Differential PECL to TTL Translator

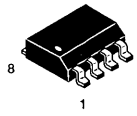
MC10ELT21
MC100ELT21

The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The V_{BB} output allows the ELT21 to also be used in a single-ended input mode. In this mode the V_{BB} output is tied to the $\overline{IN}$ input for a non-inverting buffer or the IN input for an inverting buffer. If used the V_{BB} pin should be bypassed to ground via a 0.01µF capacitor.

The ELT21 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

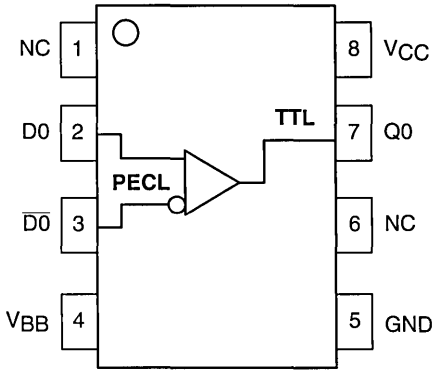
- 3.5ns Typical Propagation Delay
- Differential PECL Inputs
- Small Outline SOIC Package
- 24mA TTL Output
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q	TTL Output
D	Diff PECL Inputs
V_{CC}	+5.0V Supply
V_{BB}	Reference Output
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice

Product Preview

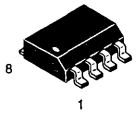
Dual TTL to Differential PECL Translator

MC10ELT22
MC100ELT22

The MC10ELT/100ELT22 is a dual TTL to differential PECL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT22 makes it ideal for applications which require the translation of a clock and a data signal. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The ELT22 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

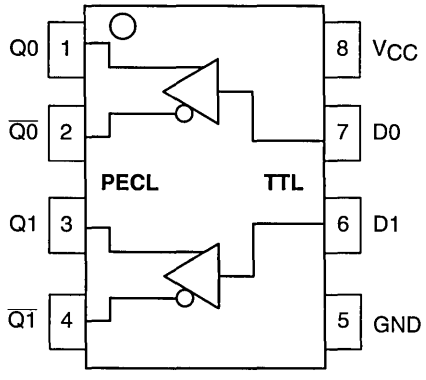
- 1.5ns Typical Propagation Delay
- <300ps Typical Output to Output Skew
- Differential PECL Outputs
- Small Outline SOIC Package
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	Diff PECL Outputs
Dn	TTL Inputs
V_{CC}	+5.0V Supply
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Product Preview

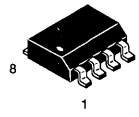
Dual Differential PECL to TTL Translator

MC100ELT23

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The ELT23 is available in only the ECL 100K standard. Since there are no PECL outputs or an external V_{BB} reference, the ELT23 does not require both ECL standard versions. The PECL inputs are differential; there is no specified difference between the 10H and 100K standards. Therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a V_{CC} of 5.0V.

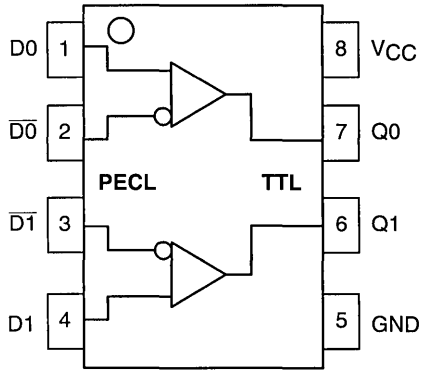
- 3.5ns Typical Propagation Delay
- <500ps Typical Output to Output Skew
- Differential PECL Inputs
- Small Outline SOIC Package
- 24mA TTL Outputs
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	TTL Outputs
Dn	Diff PECL Inputs
V_{CC}	+5.0V Supply
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Product Preview

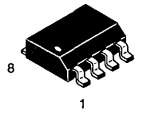
Dual TTL to Differential ECL Translator

MC10ELT24
MC100ELT24

The MC10ELT/100ELT24 is a TTL to differential ECL translator. Because ECL levels are used a +5V, -5.2V (or -4.5V) and ground are required. The small outline 8-lead SOIC package and the single gate of the ELT24 makes it ideal for those applications where space, performance and low power are at a premium. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The ELT24 is available in both ECL standards: the 10ELT is compatible with MECL 10H logic levels while the 100ELT is compatible with ECL 100K logic levels.

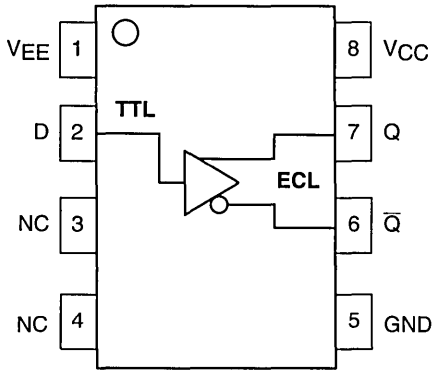
- 1.5ns Typical Propagation Delay
- Differential PECL Outputs
- Small Outline SOIC Package
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q	Diff ECL Outputs
D	TTL Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

Product Preview

Dual Differential ECL to TTL Translator

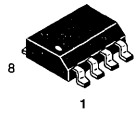
MC10ELT25
MC100ELT25

The MC10ELT/100ELT25 is a differential ECL to TTL translator. Because ECL levels are used a +5V, -5.2V (or -4.5V) and ground are required. The small outline 8-lead SOIC package and the single gate of the ELT25 makes it ideal for those applications where space, performance and low power are at a premium. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The V_{BB} output allows the ELT25 to also be used in a single-ended input mode. In this mode the V_{BB} output is tied to the $\overline{IN}$ input for a non-inverting buffer or the IN input for an inverting buffer. If used the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

The ELT25 is available in both ECL standards: the 10ELT is compatible with MECL 10H logic levels while the 100ELT is compatible with ECL 100K logic levels.

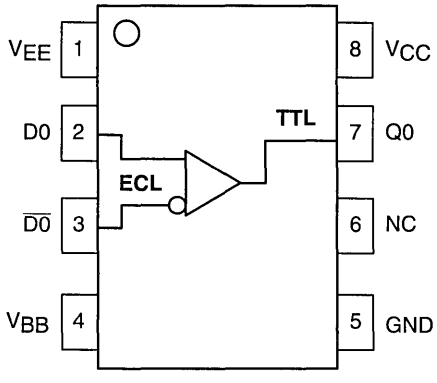
- 3.5ns Typical Propagation Delay
- Differential ECL Inputs
- Small Outline SOIC Package
- 24mA TTL Outputs
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q	Diff ECL Inputs
D	TTL Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
V_{BB}	Reference Output
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development Motorola reserves the right to change or discontinue this product without notice

Product Preview

1:2 Fanout Differential PECL to TTL Translator

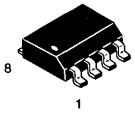
MC10ELT26
MC100ELT26

The MC10ELT/100ELT26 is a 1:2 fanout differential PECL to TTL translator. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the 1:2 fanout design of the ELT23 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The V_{BB} output allows the ELT26 to also be used in a single-ended input mode. In this mode the V_{BB} output is tied to the $\overline{IN}$ input for a non-inverting buffer or the IN input for an inverting buffer. If used the V_{BB} pin should be bypassed to ground via a 0.01µF capacitor.

The ELT26 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

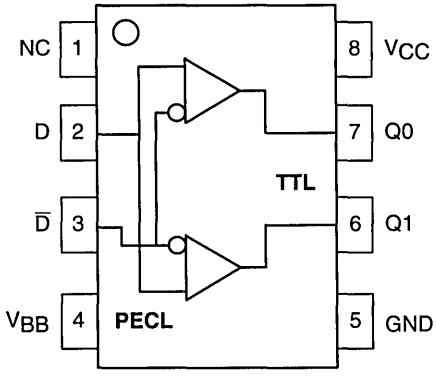
- 3.5ns Typical Propagation Delay
- <500ps Typical Output to Output Skew
- Differential PECL Inputs
- Small Outline SOIC Package
- 24mA TTL Outputs
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	TTL Outputs
D	Diff PECL Input
V_{CC}	+5.0V Supply
V_{BB}	Reference Output
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Product Preview

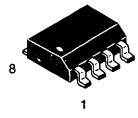
TTL to Differential PECL/ Differential PECL to TTL Translator

MC10ELT28
MC100ELT28

The MC10ELT/100ELT28 is a differential PECL to TTL translator and a TTL to differential PECL translator in a single package. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the dual translation design of the ELT28 makes it ideal for applications which are sending and receiving signals across a backplane. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The ELT28 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

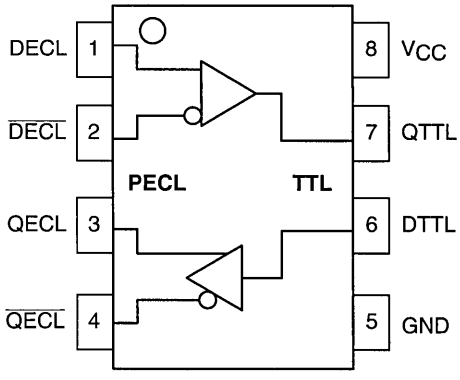
- 3.5ns Typical PECL to TTL Propagation Delay
- 1.5ns Typical TTL to PECL Propagation Delay
- Differential PECL Inputs/Ouputs
- Small Outline SOIC Package
- PNP TTL Inputs for Minimal Loading
- 24mA TTL Outputs
- Flow Through Pinouts



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04

3

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



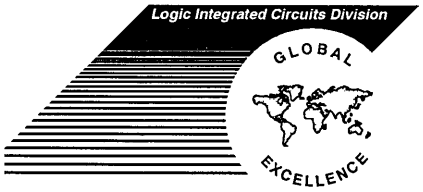
PIN DESCRIPTION

PIN	FUNCTION
QTTL	TTL Output
DTTL	TTL Inputs
QECL	Diff ECL Outputs
DECL	Diff ECL Inputs
V_{CC}	+5.0V Supply
GND	Ground

More information on this device *may* be available in the Motorola ECLinPS Lite Brochure — BR1330/D — available through Literature Distribution.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

igh Performance ECL Data
LinPS and ECLinPS Lite



This section contains a design guide written lusively with the ECLinPS product family in d. The design guide deals with system design ects of using the family. This section is not ant to be a replacement for the MECL System ign Handbook but rather a supplement to the rmation contained in it.

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Design Guide & Application Notes

4

SECTION 1
System Basics

Power Supply Considerations

The following text gives a brief description of the requirements and recommendations for treatment of power supplies in an ECLinPS system design. A more thorough narration on the general subject of power supplies can be found in the Motorola System Design Handbook.

V_{CC} Supply

As with all previous ECL families the ECLinPS logic family is designed to operate with negative power supplies; in other words with V_{CC} connected to ground. However, ECLinPS circuits will work fine with positive power supplies as long as special care has been taken to ensure a stable, quiet V_{CC} supply. For more detailed information about using positive supplies and ECL, designers are encouraged to refer to Application Note AN1406 on page 4-56. The output voltage levels for a positive supply system can be determined by simply subtracting the absolute value of the standard negative output levels from the desired V_{CC}.

To provide as small an AC impedance as possible, and minimize power bus IR drops, the V_{CC} supply should have a dedicated power plane. By providing a full ground plane in the system the designer ensures that the current return path for the signal traveling down a transmission line does not encounter any major obstructions. It is imperative that the noise and voltage drops be as small as possible on the V_{CC} plane as the internal switching references and output levels are all derived off of the V_{CC} power rail. Thus, any perturbations on this rail could adversely affect the noise margins of a system.

V_{EE} Supply

To take advantage of increased logic density and temperature compensated outputs, many designers are building array options with both, temperature compensated output levels and a -5.2V V_{EE} supply. To alleviate any problems with interfacing these arrays to ECLinPS 100E devices, Motorola has specified the operation of 100E devices to include the standard 10H V_{EE} voltage range. Moreover, because of the superior voltage compensation of the bias network, this guarantee comes without any changes in the DC or AC specification limits. With the availability of both 10H and 100K compatible devices in the ECLinPS family, there is generally no need to run 10E devices at 100K voltage levels. If, however, this is desired, the 10E devices will function at 100E V_{EE} levels with, at worst, a small degradation in AC performance for a few devices due to soft saturation of the current source device.

Although both the 10E and 100E devices can tolerate variations in the V_{EE} supply without any detrimental effects, it is recommended that the V_{EE} supply also have a dedicated powerplane. If this is not a feasible constraint, care should be taken so that the IR drops of the V_{EE} bus do not create a V_{EE} voltage outside of the specification range. To provide the switching currents resulting from stray capacitances and asymmetric loading, the V_{EE} power supply in an ECL system needs to be bypassed. It is recommended that the V_{EE} supply be bypassed at each device with an RF quality 0.01μF capacitor to ground. In addition, the supply should also be bypassed to ground with a 1.0μF – 10μF capacitor at the power inputs to a board. If a separate output termination plane is used the V_{EE} supply will be of a static nature as the output switching current will return to ground via the V_{TT} supply, thus, the bypassing of every device may be on the conservative side. If the design is going to include a liberal use of serial or Thevenin equivalent termination schemes, a properly bypassed V_{EE} plane is essential.

V_{TT} Supply

The output edge rates of the ECLinPS family necessitate an almost exclusive use of controlled impedance transmission lines for system interconnect (the details of this claim will be discussed in a latter section). Thus, unless Thevenin equivalent termination schemes are going to be used, a V_{TT} supply is a must in ECLinPS designs. The choice of using only Thevenin equivalent termination schemes to save a power supply should not be made lightly as the Thevenin scheme consumes up to ten times more power than the equivalent parallel termination to a -2.0V V_{TT} supply.

As was the case for the V_{EE} supply, a dedicated power plane, liberally bypassed as described above, should be used for the V_{TT} supply. In designs which rely heavily on parallel termination schemes the V_{TT} supply will be responsible for returning the switching current of the outputs to ground, therefore, a low AC impedance is a must. For bypassing, many SIP resistor packs have bypass capacitors integrated in their design to supply the necessary bypassing of the supply. The use of SIP resistors will be discussed more thoroughly in a later chapter.

Handling of Unused Inputs and Outputs

Unused Inputs

All ECLinPS devices have internal 50kΩ – 75kΩ pulldown resistors connected to V_{EE}. As a result, an input which is left open will be pulled to V_{EE} and, thus, set at a logic LOW. These internal pulldowns provide more than enough noise margin to keep the input from turning on if noise is coupled to the input, therefore, there is no need to tie the inputs to V_{EE} external to the package. In addition, by shorting the inputs to V_{EE} external to the package, one removes the current limiting effect of the pulldown resistor and, under extreme V_{EE} conditions, the input transistor could be permanently

damaged. If there are concerns about leaving sensitive inputs, such as clocks, open, they should be tied low via an unused output or a quiet connection to V_{TT}.

Unless otherwise noted on the data sheets, the outputs to differential input devices will go to a defined state when the inputs are left open. This is accomplished via an internal clamp. Note that this clamp will only take over if the voltage at the inputs fall below ≈ – 2.5V. Therefore, if equal voltages of greater than – 2.5V are placed on the inputs, the outputs will attain an undefined midswing state.

Unlike saturating logic families, the inputs to an ECLinPS, or any ECL device, cannot be tied directly to V_{CC} to implement a logic HIGH level. Tying inputs to V_{CC} will saturate the input transistor and the AC and DC performance will be seriously impaired. A logic HIGH on an ECLinPS input should be tied to a level no higher than 600mV below the V_{CC} rail and, more typically, no higher than the specified V_{IH}max limit. A resistor or diode tree can be used to generate a logic HIGH level or, more commonly, an output of an unused gate can be used.

Unused Outputs

The handling of unused outputs is guided by two criteria: power dissipation and noise generation. For single ended output devices it is highly recommended to leave unused outputs unterminated as there are no benefits in the alternative scheme. This not only saves the power associated with the output, but also reduces the noise on the V_{CC} line by reducing the current being switched through the inductance of the V_{CC} pins. For the counters and shift registers of the family, the count and shift frequencies will be maximized if the parallel outputs are left unterminated. Of course, for applications where these parallel outputs are needed this is not a viable alternative.

For the differential outputs, on the other hand, things are a little less cut and dry. If either of the outputs of a complimentary output pair is being used, both outputs of the pair should be terminated. This termination scheme minimizes the current being switched through the V_{CC} pin and, thus, minimizes the noise generated on V_{CC}. If, however, neither of the outputs of a complimentary pair are being used it makes most sense to leave these unterminated to save power. Note that the E111 device has special termination rules; these rules are outlined on the data sheet for the device.

Minimizing Simultaneous Switching Noise

A common occurrence among ECL families is the generation of crosstalk and other noise phenomena during simultaneous switching situations. Although the noise generated in ECL systems is minor compared to other technologies, there are methods to even further minimize the problem.

Figure 1.1 below illustrates the two output scenarios of an ECL device: differential outputs and single-ended outputs. During switching, the current in the output device will change by ≈17mA when loaded in the normal 50Ω to – 2.0V load. With differential outputs, as one output switches from a low to a high state the other switches from a high to a low state simultaneously, thus, the resultant current change through the V_{CCO} connection is zero. The current simply switches between the two outputs. However, for the single-ended output, the current change flows through the V_{CCO} connection of the output device. This current change through the V_{CCO} pin of the package causes a voltage spike due to the inductance of the pin.

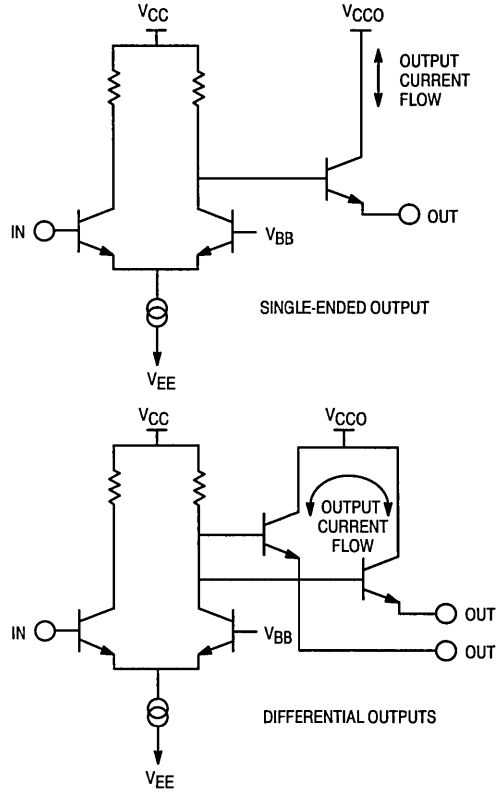


Figure 1.1. ECL Output Structures

Traditionally, manufacturers of ECL products have attempted to combat this problem by providing a separate V_{CC} pin for the output device (V_{CCO}, V_{CCA} etc.) and the internal circuitry. By doing this the noise generated on the V_{CCO} of the output devices would see a high impedance internal to the chip and not couple onto the the V_{CC} line which controls the output and internal bias levels. Unfortunately, in practice the noise generated on the V_{CCO} would couple into the chip V_{CC} through the collector base capacitance of the output device, thus, a large portion of the noise seen on the V_{CCO} line would also be seen on the V_{CC} line.

For the ECLinPS family and its associated edge speeds, it was decided that multiple V_{CCO} pins would be necessary to minimize the inductance and the associated noise generation. A design rule was established so that there would be no more than three single-ended outputs per V_{CCO} pin. Initially, the V_{CC} and V_{CCO} pins were kept isolated from one another. However, it was discovered that in certain

applications the parasitics of the package and the output device would combine to produce an instability which resulted in the outputs going into an oscillatory state. To alleviate this oscillation problem, it was necessary to make the V_{CC} and V_{CCO} metal common internal to the package. Subsequent evaluation showed that because of the liberal use of V_{CCO} pins, the noise generated is equal to or less than that of previous ECL families.

To further reduce the noise generated there are some things that can be done at the system level. As mentioned above, there should be adequate bypassing of the V_{CC} line and the guidelines for the handling of unused outputs should be followed. In addition, for wide single-ended output devices, an increase in the characteristic impedance of the transmission line interconnect will result in a smaller time rate of change of current; thus, reducing the voltage glitch caused by the inductance of the package. This noise improvement should, of course, be weighed against the potential slowing of the higher impedance trace to optimize the performance of the entire system. In addition, the connection between the device V_{CC} pins and the ground plane should be as small as possible to minimize the inductance of the V_{CC} line. Note that a device mounted in a socket will exhibit a larger amount of V_{CC} noise due to the added inductance of the socket pins.

Effects of Capacitive Loads

The issue of AC parametric shifts with load capacitance is a common concern especially with designers coming from the TTL and CMOS worlds. For ECLinPS type edge speeds, wire interconnect starts acting like transmission lines for lengths greater than 1/2". Therefore, for the majority of cases in ECLinPS designs, the load on an output is seen by the transmission line and not the output of the driving device. The effects of load capacitance on transmission lines will be discussed in detail in the next section.

If the load is close to the driving output (<1/2"), the resulting degradation will be 15–25ps/pF for both propagation delays and edge rates. In general, a capacitive load on an emitter follower has a greater impact on the falling edge than the rising edge. Therefore, the upper end of the range given above represents the effect on fall times and the associated propagation delays, while the lower end represents the effect on the rising output parameters.

For ECLinPS devices, the capacitive load produced by an input ranges from 1.2pF to 2.0pF. The majority (≈95%) of this capacitance is contributed by the package with very little added by the internal input circuitry. For this reason the range is generally a result of the difference between a corner and a center pin for the PLCC package. A good typical capacitance value for a center pin is 1.4pf and for a corner pin 1.7pf. The capacitances for the other pins can be deduced through a linear interpolation.

Wired-OR Connections

The use of wired-OR connections in ECL designs is a popular way to reduce total part count and optimize the speed performance of a system. The limitation of OR-tying ECL outputs has always been a combination of increased delay per OR-tie and the negative going disturbance seen at the output when one output switches from a high to a low while the rest of the outputs remain high. For high speed devices the latter problem is the primary limitation due to the increased sensitivity to this phenomena with decreasing output transition times. The following paragraph will attempt to describe the wire-OR glitch phenomena from a physical perspective.

Figure 1.2 illustrates a typical wire-OR situation. For simplicity, the discussion will deal with only two outputs; however, the argument could easily be expanded to include any number of outputs. If both the A and the B outputs start in the high state they will both supply equal amounts of current to the load. If the B output then transitions from a high to a low the line at the emitter of B will see a sudden decrease in the line voltage. This negative going transition on the line will continue downward at the natural fall time of the output until the A output responds to the voltage change and supplies the needed current to the load. This lag in the time it takes for A to correct the load current and return the line to a quiescent high level is comprised of three elements: the natural response time of the A output, the delay associated with the trace length between the two outputs and the time it takes for a signal to propagate through the package. The trace delay can be effectively forced to zero by OR-tying adjacent pins. The resulting situation can then be considered "best case". In this best case situation, if the delay through the package is not a significant portion of the transition time of the output, the resulting negative going glitch will be relatively small (≈100mV). A disturbance of this size will not propagate through a system. As the trace length between OR-tied outputs increases, the magnitude of the negative going disturbance will increase. Older ECL families specified the maximum delay allowed between OR-tied outputs to prevent the creation of a glitch which would propagate through a system.

As this glitch phenomena is a physical limitation, due to decreased edge rates, ECLinPS devices are susceptible to the problem to an even greater degree than previous slower ECL families. The package delay of even the 28-lead PLCC

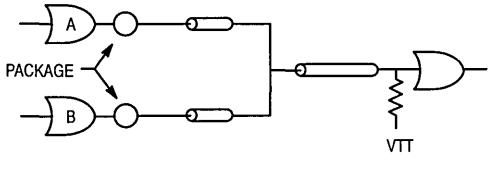


Figure 1.2. Typical Wire-OR Configuration

is a significant portion of the transition times for an ECLinPS device. Therefore, even in the best case situation described above, one can expect an ≈200mV glitch on the OR-tied line. A glitch of this magnitude will not propagate through the system but it is significantly worse than the best case situation of earlier ECL families. In fact, as long as the distance between OR-tied outputs is kept to less than 1/2" the resulting line disturbance will not be sufficient to propagate through most systems.

With this in mind, the following recommendations are offered for OR-tying in ECLinPS designs. First, OR-tying of clock lines should be avoided as even in the best case situation the disturbance on the line is significant and could cause false clocking in some situations. In addition, wire ORed outputs should be from the same package and preferably should be adjacent pins. Non-adjacent outputs should be within 1/2" of each other with the load resistor connection situated near the midpoint of the trace (Figure 1.2). By following these guidelines, the practice of wire-ORing ECL outputs can be expanded to the ECLinPS family without encountering problems in the system.

A detailed discussion of wire-OR connections in the ECLinPS world of performance is beyond the scope of this text. For this reason a separate application note has been written which deals with this situation in a much more thorough manner. Anyone planning to use wire-OR connections in their ECLinPS design is encouraged to contact a Motorola representative to obtain this application note.

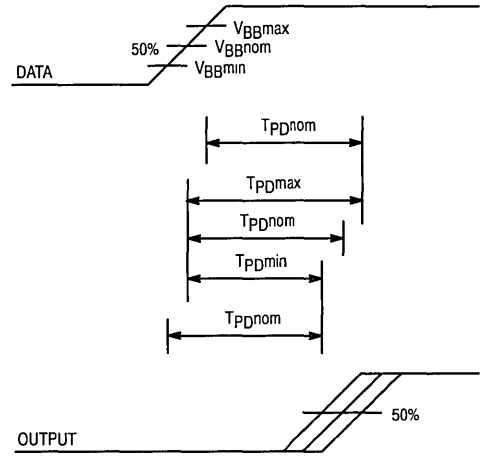


Figure 1.3. Delay vs Switching Reference Offset

Clock Distribution

Clock skew is a major contributor to the upper limit of operation of a high speed system; therefore, any reduction in this parameter will enhance the overall performance of a system. Through the ECLinPS family and new offerings in the 10H family, Motorola is providing devices uniquely designed to meet the demands of low skew clock distribution.

By far the largest contributor to system skew is the variation between different process lots of a given device. This variation is what defines the total delay window specified in the data sheets. This window can be minimized if the devices are fully differential due to the output level defined thresholds which ensure a "centered" input swing. The propagation delay windows of single-ended ECL and other logic technologies, are intimately tied to variations in the input thresholds. As illustrated in Figure 1.3 although the delays, when measured from the threshold of the input to the 50% point of the output, are equal; when measured from the specified 50% point of the input to the 50% point of the output, the delays will vary with any shift in the switching reference. Obviously, the magnitude of the delay difference is also proportional to the edge rate of the input. In addition to increasing the size of the delay windows, this reference shift will cause the duty cycle of the output of a device to be different than that of the input. Unfortunately, these thresholds are perhaps the most difficult aspects of a logic device to control. As a result, for the ultimate in low skew performance differential ECL devices are a must. A quick perusal of the ECLinPS databook will reveal a relatively large number of totally differential devices which will lend themselves nicely to very low skew applications such as clock distribution.

In addition to these generic differential devices there are several devices which were designed exclusively for clock distribution systems. With past ECL families designers were forced to build clock distribution trees with devices which were compromises at best. The ECLinPS family, however, was built around the E111 clock distribution chip; a fully differential 1:9 fanout device which boasts within part skews as well as part- to-part skews unequaled in today's market.

Additionally, to further deskew clock lines the E195 programmable delay chip is available. Although static delay lines can remove built-in path length difference skew, they cannot compensate for variations in the delays of the devices in the clock path. The E195 allows the user to delay, a signal over a 2ns range in ≈20ps steps. Through the use of this device, the designer can match skews between clocks to 20ps.

Although these two devices satisfy the needs for many ECL designers, they do overlook the needs of a special subset; the designer who mixes ECL and TTL technologies. When translating between ECL and TTL, much of the skew performance gained through the E111 is lost when passed through the translator and distributed in TTL. To solve this problem, a new set of translators has been introduced in the MECL 10H family. The H641 and H643 receive a differential ECL input and fan out nine TTL outputs with a guaranteed unparalleled skew between the TTL outputs. The H640 and H642 take differential ECL inputs and generate low skew TTL outputs which are ideal for driving clocks in 68030 and 68040 microprocessor systems. By using the ECL aspects of the E111 to distribute clock lines across the backplane to TTL cards and receiving and translating these signals with the H640, H641, H642 or H643, a TTL clock distribution tree can be designed with a performance level unheard of with past logic families.

Through the development of a library of differential devices, specialized low-skew distribution chips and high-resolution programmable delay chips, Motorola has serviced the need for low-skew clock distribution designs. These offerings open the door for even higher performance next generation machines. For more information on clock distribution, designers are encouraged to read Application Note AN1405 on page 4-49.

Metastability Behavior

The metastability behavior and measurement of a flip-flop is a complicated subject and necessitates much more time than is available in this forum for a thorough explanation. As a result, the following description is of an overview nature. Anyone interested in a more thorough narration on the subject is encouraged to read Application Note AN1504 on page 4-75, which contains a more detailed discussion on the subject.

In many designs, occasions arise where an asynchronous signal needs to be synchronized to the system clock. Generally, this task is accomplished with the use of a single or series of D flip-flops as pictured in Figure 1.4. Because the data signal and the clock signal are asynchronous, the system designer cannot guarantee that the setup and hold specifications for the device will be met. This in and of itself would not cause a problem if it was not for the metastable behavior of a D flip-flop. The metastable behavior of a flip-flop is described by the outputs of a device attaining a nondefined logic level or, perhaps, going into an oscillatory state when the data and the clock inputs to the flip-flop switch simultaneously. It has been shown that this metastable behavior occurs across technology boundaries as well as across performance levels within a technology.

For ECL the characteristic of a flip-flop in a metastable state is a device whose outputs are in a non-defined state near the midpoint of a normal output swing. The output will return randomly to one of the two defined states some time later (Figure 1.5). The two parameters of importance when discussing metastability are the metastablity window; the window in time for which a transition on both the data and the

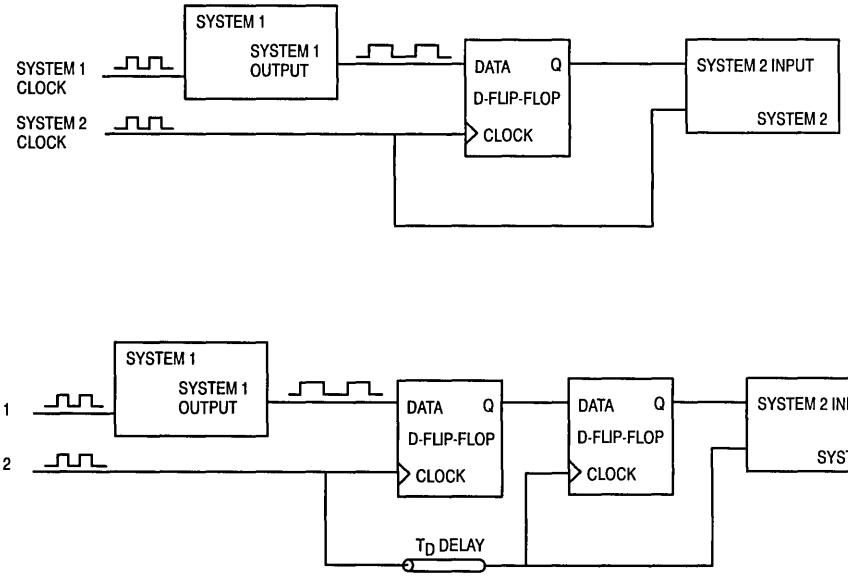


Figure 1.4. Clock Synchronization Schemes

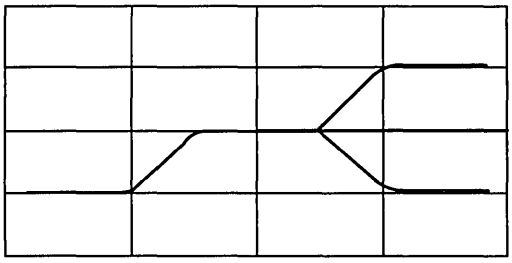


Figure 1.5. Metastable Behavior of an ECL Flip Flop

clock will cause a metastable output, and the settling time; the time it takes for a metastable output to return to a defined state. For the single flip-flop design of Figure 1.3, the data being fed into system 2 will be in an undefined state and, thus, unusable if the synchronizing flip-flop enters a metastable state. Because of this, a more popular design incorporates multiple flip-flop chains with cascading data inputs and clock inputs which are delayed with respect to each other. This redundancy of flip- flops helps to reduce the probability that the data entering system 2 will be at an undefined level which could wreak havoc on the logic of that system. This reduction in probability relies on the fact that even if the preceding flip-flop goes metastable, it will settle to a defined state prior to the clocking of the following flip-flop. Obviously, once the first flip-flop goes metastable there is an even chance that it will settle in the wrong state and, thus, information will be lost. However, there are error detection and correction methods to circumvent this problem. The larger the flip-flop chain the lower the probability of metastable data being fed into system 2.

Unfortunately for ECLinPS, levels of performance, both the window width and the settling time, are difficult or impossible to measure directly. The metastable window for an ECLinPS flip-flop is assuredly less than 5.0ps and most likely less than 1.0ps based on SPICE level simulation results. In either case, with today's measuring equipment, it would be impossible to measure this window width directly. Although it is feasible to measure the settling time for a given occurrence, this parameter is not fixed but, rather, is of a variable length which makes it impossible to provide an absolute guarantee.

The challenge then becomes, how to characterize metastability behavior given the above circumstances. The standard method in the industry is to use Stoll's[1] equation, combined with the standard MTBF equation, to develop the following relationship:

$$MTBF = 1 / (2 * f_C * f_D * T_P * 10^{-(t/\tau)})$$

where:

f_C:	Clock Frequency
f_D:	Data Frequency
T_p:	FF Propagation Delay
t:	Time Delay Between FF Clocks
τ:	FF Resolution Time Constant

Note that the clock frequency, data frequency and time delay between flip-flops are user-defined parameters, thus it is up to Motorola to provide only the propagation delays and the resolution time constants for the ECLinPS flip-flops.

The propagation delays are, obviously, already defined leaving only the resolution time constant yet to be determined. An evaluation fixture was fabricated and several ECLinPS flip-flops were evaluated for resolution time constants.The results of the evaluation showed that the time constant was somewhat dependent on the part type as all the flip-flops in the ECLinPS family do not use the same general design. The time constants range from 125–225 ps depending on the part type.

As an example, for a system with a 100MHz clock and 75MHz data rate, the required delay between clock edges of a cascaded flip-flop chain for the E151 register, assuming a τ of 200ps, would be:

$$MTBF = 1 / (2 * 100MHz * 75MHz * 800ps * 10^{-t/200ps})$$

solving for an MTBF of 10 years yields:

$t = 3.1ns$, therefore:

$$T_D = \Delta t + T_P = 3.9ns$$

So, for an MTBF of 10 years for the above situation the second flip-flop should be clocked 3.9ns after the first. Similar results can be found by applying the equation to different data and clock rates as well as different acceptable MTBF rates.

[1] Stoll, P. "How to Avoid Synchronization Problems," VLSI Design, November/December 1982. pp. 56–59.

SECTION 2
Transmission Line Theory

Introduction

The ECLinPS family has pushed the world of ECL into the realm of picoseconds. When output transitions move into this picosecond region it becomes necessary to analyze system interconnects to determine if transmission line phenomena will occur. A handy rule of thumb to determine if an interconnect trace should be considered a transmission line is if the interconnect delay is greater than 1/8th of the signal transition time, it should be considered a transmission line and afforded all of the attention required by a transmission line. If this rule is applied to the ECLinPS product line a typical PCB trace will attain transmission line behaviors for any length >1/4". Thus, a brief overview of transmission line theory is presented, including a discussion of distributed and lumped capacitance effects on transmission lines. For a more thorough discussion of transmission lines the reader is referred to Motorola's MECL Systems Design Handbook.

Background

Exact transmission line analysis can be both tedious and time consuming; therefore, assumptions for simplifying these types of calculations must be made. A reasonable assumption is that interconnect losses caused by factors such as bandwidth limitations, attenuation, and distortion are negligible for a typical PCB trace. The basis for this assumption is that losses due to the interconnect conductor are only a fraction of the total losses in the entire interface scheme. In addition, the conductivity of insulating material is very small; as a result, the dielectric losses are minimal. A second, and more fundamental, assumption is that transmission line behavior can be described by two parameters: line characteristic impedance (Z_O), and propagation delay (T_{PD})

Characteristic Impedance

An interconnect which consists of two conductors and a dielectric, characterized by distributed series resistances and inductances along with distributed parallel capacitances between them, is defined as a transmission line. These transmission lines exhibit a characteristic impedance over any length for which the distributed parameters are constant. Since the contribution of the distributed series resistance to the overall impedance is minimal, this term can be neglected when expressing the characteristic impedance of a line. The characteristic impedance is a dynamic quantity defined as the ratio of the transient voltage to the transient current passing through a point on the line. Thus, Z_O can be expressed in terms of the distributed inductance and capacitance of the line as shown by Equation 1.

$$Z_O = V/I = \sqrt{(L_O/C_O)} \qquad \text{(Equation 1)}$$

where:

L_O = Inductance per unit length (H)
C_O = Capacitance per unit length (F)

Propagation Delay

Propagation delay (T_{PD}) is also expressed as a function of both the inductance and capacitance per unit length of a transmission line. The propagation delay of the line is defined by the following equation:

$$T_{PD} = \sqrt{(L_O * C_O)} \qquad \text{(Equation 2)}$$

If L_O is expressed as microHenry's per unit length and capacitance as picoFarad's per unit length, the units for delay are nanoseconds per unit length. The propagation velocity is defined as the reciprocal of the propagation delay:

$$v = 1/T_{PD} = 1/\sqrt{(L_O * C_O)}$$

L_O and C_O can be determined using the easily measured parameters of line delay (T_D), line length (L), and the line characteristic impedance (Z_O) in conjunction with Equations 1 and 2. The propagation delay is defined as the ratio of line delay to line length:

$$T_{PD} = T_D/L$$

Combining equations 1 and 2 yields:

$$C_O = T_{PD}/Z_O \qquad \text{(Equation 3)}$$
$$L_O = T_{PD} * Z_O \qquad \text{(Equation 4)}$$

Termination and Reflection Theory

Figure 2.1 shows an ECLinPS gate driving a lossless transmission line of characteristic impedance Z_O, and terminated with resistance R_T. Modifying the circuit of Figure 2.1 such that the driving gate is represented by its equivalent circuit gives the configuration shown in Figure 2.2.

For a positive step function V_{IN}, a voltage step V_S, travels down the transmission line. The initial current in the transmission line is determined by the ratio V_S/Z_O. When the traveling wave arrives at the termination resistor R_T, Ohm's

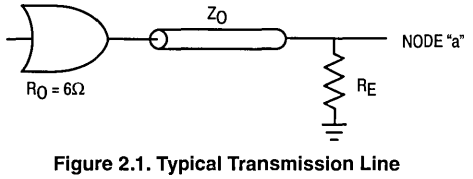


Figure 2.1. Typical Transmission Line Driving Scenario

Law must be maintained. If the line characteristic impedance and the termination resistance match (i.e. $Z_O=R_T$),the traveling wave does not encounter a discontinuity at the line-load interface; thus, the total voltage across the termination resistance is the incident voltage V_S. However, if mismatches between the line characteristic impedance and the termination resistance occur, a reflected wave must be set up to ensure Ohm's Law is obeyed at the line-load interface. In addition, the reflected wave may also encounter a discontinuity at the interface between the transmission line and the source resistance, thereby sending a re-reflected wave back towards the load. When neither the source nor the load impedance match the line characteristic impedance multiple reflections occur with the reflected signals being attenuated with each passage over the transmission line. The output response of this configuration appears as a damped oscillation, asymptotically approaching the steady state value, a phenomenon often referred to as ringing.

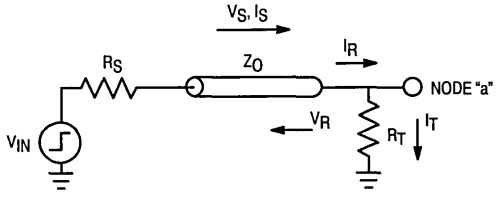


Figure 2.2. Thevenin Equivalent Circuit of Figure 2.1

In performing transmission line analysis, designers may encounter one of three impedance situations:

1. $R_S < Z_O$; $R_T \neq Z_O$
2. $R_S \leq Z_O$; $R_T = Z_O$
3. $R_S = Z_O$; $R_T \neq Z_O$

where:

R_S = Source Resistance

R_T = Termination Resistance

Case 1: $R_S < Z_O$; $R_T \neq Z_O$

The initial current in the transmission line is determined by the ratio V_S/Z_O. However, the final steady state current is determined by the ratio V_S/R_T, assuming ohmic losses in the transmission line are negligible. For case 1, an impedance discontinuity exists at the line-load interface which causes a reflected voltage and current to be generated at the instant the initial signal arrives at this interface. To determine the fraction of the traveling wave that will be reflected from the line-load interface, Kirchoff's current law is applied to node "a" in Figure 2.2. This results in the following:

$I_T = I_S + I_R$ where:

$I_T = V_T/R_T$

$I_S = V_S/Z_O$

$I_R = -V_R/Z_O$

Using substitution:

$$V_T/R_T = V_S/Z_O - V_R/Z_O \qquad \text{(Equation 5)}$$

Since only one voltage can exist at node "a" at any instant in time:

$$V_T = V_S + V_R \qquad \text{(Equation 6)}$$

Combining Equations 5 and 6, and solving for V_R yields:

$$(V_S + V_R)/R_T = V_S/Z_O - V_R/Z_O$$

$$V_R = ((R_T-Z_O)/(R_T+Z_O))*V_S$$

$$V_R/V_S = \rho_L = (R_T-Z_O)/(R_T+Z_O) \qquad \text{(Equation 7)}$$

Therefore:

$$V_R = \rho_L * V_S$$

The term ρ_L referred to as the load reflection coefficient, represents the fraction of the voltage wave arriving at the lineload interface that is reflected back toward the source.

Similarly, a source reflection coefficient can be derived as:

$$\rho_S = (R_S-Z_O)/(R_S+Z_O) \qquad \text{(Equation 8)}$$

From equations 7 and 8 it is apparent that multiple reflections will occur when neither the source nor the load impedances match the characteristic impedance of the line. A general equation for the total line voltage as a function of time and distance is expressed by Equation 9.

$$V(x,t) \quad V_A(t)*[U(t-T_{PD}*x) + \rho_L*U(t-T_{PD}(2L-x) + \rho_L*\rho_S*U(t-T_{PD}(2L+x)) + (\rho_L**2)*(\rho_S*U(t-T_{PD}(4L-x)) + (\rho_L**2)*\rho_S**2)*U(t-T_{PD}(4L+x)) + \ldots] + V_{DC} \qquad \text{(Equation 9)}$$

where:

V_A = Voltage Entering the Transmission Line
T_{PD} = Propagation Delay of the Line
L = Total Line Length
x = Distance to an Arbitrary Point on the Line
V_{DC} = Initial Quiescent Voltage of the Line

Finally, the output voltage, V_T can be derived from the reflection coefficient by combining Equations 6 and 7:

$$V_T=(1+(R_T-Z_O)/(R_T+Z_O))* V_S$$

$$V_T=(2*R_T/(R_T+Z_O))*V_S$$

The two possible configurations for the Case 1 conditions are $R_T > Z_O$ and $R_T < Z_O$. The following paragraphs will describe these two conditions in detail.

Configuration 1: $R_T > Z_O$

For the case in which $R_T > Z_O$, ρ_L is positive, and the initial current at node "a" is greater than the final quiescent current:

$$I_{INITIAL} > I_{FINAL}$$

Hence:

$$V_S/Z_O) > (V_S/R_T)$$

Thus, a reflected current, I_R, must flow toward the source in order to attain the final steady state current as shown in Figure 2.3.

An example of a line mismatched at both ends, with the termination resistance greater than the load resistance is shown

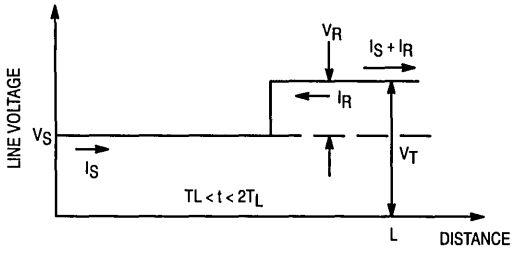


Figure 2.3. Reflected Voltage Wave for $R_T > Z_O$

in Figure 2.4. The initial steady state output voltage is given by:

$$V_{TI} = (65/71)^*(-1.75) = -1.60V$$

The final steady state output voltage is given by:

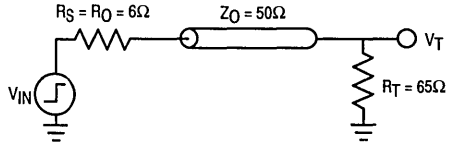


Figure 2.4. Transmission Line Model for $R_T > Z_O$

$$V_{TF} = (65/71)^*(-0.9) = -0.82V$$

The input voltage is a ramp from –1.75V to – 0.9V. The initial voltage traveling down the line is:

$$V_S = (50/56)^*0.85 = 0.76V$$

From Equations 7 and 8:

$$\rho_L = (R_T - Z_0)/(R_T+Z_0) = (65 - 50)/(65+50) = 0.13$$

$$\rho_S = (R_S - Z_0)/(R_S+Z_0) = (6 - 50)/(6+50) = -0.79$$

From Equation 9, the output voltage V_T after one line delay is:

$$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = -0.71V$$

Likewise, after a time equal to three times the line delay, the output voltage V_T is

$$V_T(L,3T_{PD}) = V_A(t)^*[\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = -0.83V$$

Additional iterations of Equation 9 can be performed to show that the ringing asymptotically approaches the final line voltage of – 0.82V. Ringing is a characteristic response for transmission lines mismatched at both ends with $R_T > R_O$. A SPICE representation of configuration 1 is illustrated in Figure 2.5.

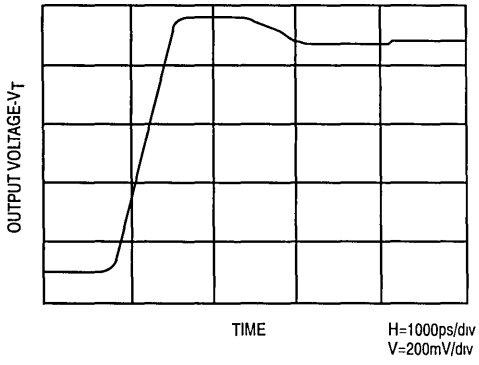


Figure 2.5. SPICE Results for Circuit of Figure 2.4

Configuration 2: $R_T < Z_O$

For the case in which $R_T < Z_O$, ρ_L is negative, and the initial current at node "a" is less than the final quiescent current.

$$I_{INITIAL} < I_{FINAL}$$

Hence:

$$(V_S/Z_O) < (V_S/R_T)$$

The reflected current, I_R, flows in the same direction as the initial source current in order to attain the final steady state current. The unique characteristic of configuration 2 is the negative reflection coefficient at both the source and load ends of the transmission line (Figure 2.6). Thus, signals approaching either end of the line are reflected with opposite polarity. In addition, the line voltage is a function of the pulse duration yielding steps of decreasing magnitude for input pulse durations greater than the line delay, and a series of attenuated pulses for input pulse durations less than the line delay.

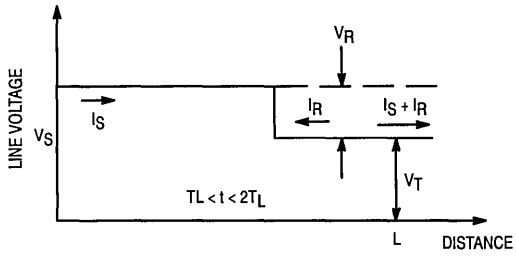


Figure 2.6. Reflected Voltage Wave for $R_T < Z_O$

An example of a line mismatched at both ends, with the termination resistance less than the line resistance, and the input pulse width greater than the line delay is shown in Figure 2.7.

The initial steady state output voltage is defined as:

$$V_{TI} = (35/41)^*(-1.75) = -1.49V$$

The final steady state output voltage is given by

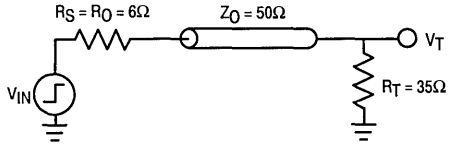


Figure 2.7. Transmission Line Model for $R_T < Z_O$

$$V_{TF} = (35/41)^*(-0.9) = -0.77V$$

For an input pulse from –1.75V to – 0.9V the initial voltage traveling down the line is:

$$V_S = (50/56)^*0.85 = 0.76V$$

From Equations 7 and 8,

$$\rho_L = (35 - 50)/(35+50) = -0.18$$

$$\rho_S = (6 - 50)/(6+50) = -0.79$$

From Equation 9, the output voltage V_T after one line delay is:

$$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = -0.87V$$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$$V_T(L,3T_{PD}) = V_A(t)^*[\rho_L{}^*\rho_L + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = -0.78V$$

Additional iterations of Equation 9 can be performed to show that the output response asymptotically approaches – 0.77 volts. Stair-steps are characteristic responses for transmission lines mismatched at both ends with $R_T < Z_O$, and a pulse width greater than the line delay. Figure 2.8 shows the results of a SPICE simulation for the case described by configuration 2.

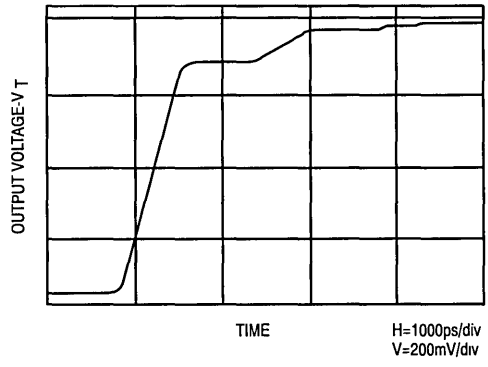


Figure 2.8. SPICE Results for Circuit of Figure 2.7 with Input Pulse Width > Line Delay

Figure 2.9 shows the line response for the same circuit as above, but for the case in which the input pulse width is less than the line delay. As in the previous example, the initial steady state voltage across the transmission line is –1.49 volts, and the reflection coefficients are – 0.18 and – 0.79 for the load and source respectively. However, the intermediate voltage across the transmission line is a series of positive-going pulses of decreasing amplitude for each round

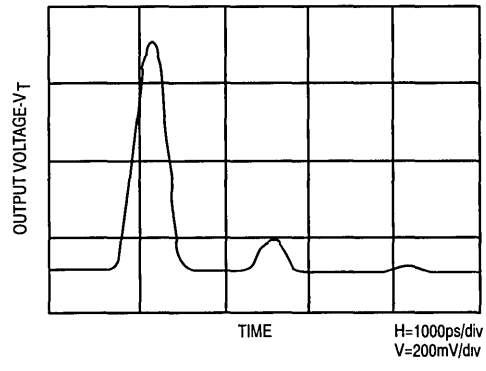


Figure 2.9. SPICE Results for Circuit of Figure 2.7 with Input Pulse < Line Delay

trip of the reflected voltage, until the final steady state voltage of 1.49 volts is reached.

Shorted Line

The shorted line is a special case of configuration 2 in which the load reflection coefficient is –1.0, and the reflections tend toward the steady state condition of zero line voltage and a current defined by the source voltage and the source resistance.

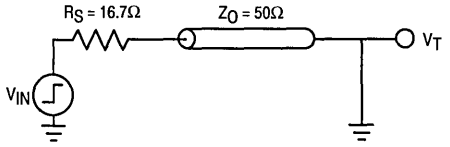


Figure 2.10. Transmission Line Model for Shorted Line

An example of a shorted line is shown in Figure 2.10. The transmission line response for the case in which the input pulse width is greater than the line delay is shown in Figure 2.11. The initial and final steady state voltages across the transmission line are zero. The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$$V_S = (50/66.7)^*0.85 = 0.64V$$

From Equations 7 and 8,
$\rho_L = (0-50)/(0+50) = -1$

$$\rho_S = (16.7-50)/(16.7+50) = -0.5$$

Upon reaching the shorted end of the line, the initial voltage waveform is inverted and reflected toward the source. At the source end, the voltage is partially reflected back toward the shorted end in accordance with the source reflection coefficient. Thus, the voltage at the shorted end of the transmission line is always zero while at the source end, the voltage is reduced for each round trip of the reflected voltage. The voltage at the source end tends toward the final steady state condition of zero volts across the transmission line. The values of the source and line characteristic impedances in this example are such that the amplitude decreases by 50% with each successive round trip across the transmission line.

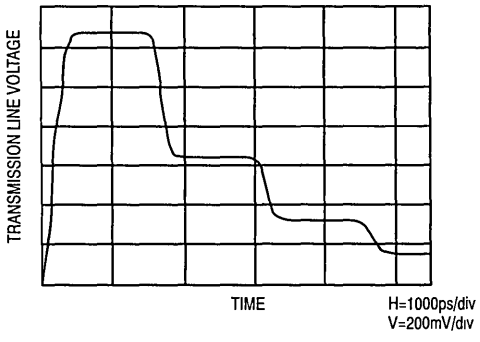


Figure 2.11. SPICE Results for Shorted Line with the Input Pulse Width > Line Delay

Figure 2.12 shows the line response for the same circuit as above, but for the case in which the input pulse width is less than the line delay. As in the previous example, the initial and final steady state voltages across the transmission line are zero, and the reflection coefficients are –1.0 and – 0.5 for the load and source respectively. However, the intermediate voltage across the transmission line is a series of negative pulses with the amplitude of each pulse decreasing for each round trip of the reflected voltage until the final steady state voltage of zero volts is attained. Again, for this example, the amplitude of the output response decreases by 50% for each successive reflection

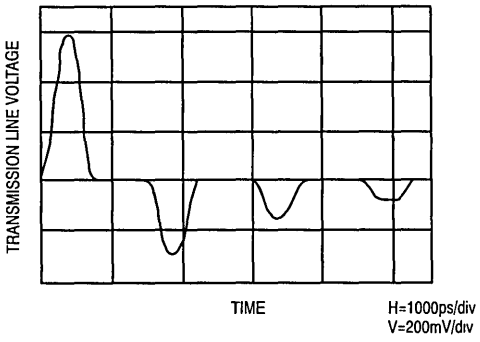


Figure 2.12. SPICE Results for Shorted Line with the Input Pulse Width < Line Delay

due to the choice of source and transmission line characteristic impedances.

Case 2: $R_S \leq Z_O$; $R_T = Z_O$

As in Case 1, the initial current in the transmission line is determined by the ratio of V_S/Z_O. Similarly, since $R_T = Z_O$ the final steady state current is also determined by the ratio V_S/Z_O. Because a discontinuity does not exist at the line-load interface, all the energy in the traveling step is absorbed by the termination resistance, in accordance with Ohm's Law. Therefore, no reflections occur and the output response is merely a delayed version of the input waveform.

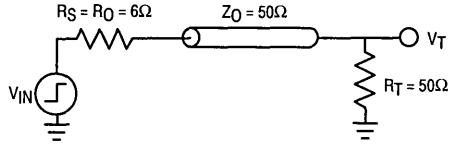


Figure 2.13. Transmission Line Model for Matched Termination

An example of a line mismatched at the source but matched at the load is shown in Figure 2.13. For an input pulse of –1.75V to – 0.9V is given by:

$$V_{TI} = (50/56)^*(-1.75) = -1.56V$$

The final steady state output voltage is given by

$$V_{TF} = (50/56)^*(-0.9) = -0.80V$$

The source is a step function with an 0.85 volt amplitude. The initial voltage traveling down the line is:

$$V_S = (50/56)^*0.85 = 0.76V$$

From Equations 7 and 8,

$\rho_L = (50-50)/(65+50) = 0$

$\rho_S = (6-50)/(6+50) = -0.79$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = -0.80V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)^*[\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = -0.80V$

Thus, the output response attains its final steady state value (Figure 2.14) after only one line delay when the termination

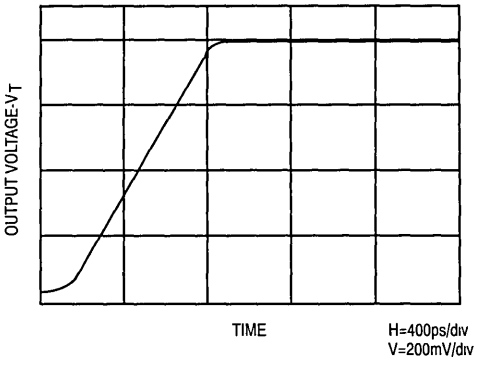


Figure 2.14. SPICE Results for Matched Termination

resistance matches the line characteristic impedance. Ringing or stair-step output responses do not occur since the load reflection coefficient is zero.

Case 3: $R_S = Z_O$; $R_T = Z_O$

When the termination resistance does not match the line characteristic impedance reflections arising from the load will occur. Fortunately, in case 3, the source resistance and the line characteristic impedance are equal, thus, the reflection coefficient is zero and the energy in these reflections is completely absorbed at the source; thus, no further reflections occur.

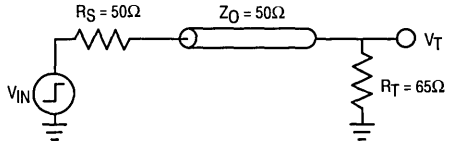


Figure 2.15. Transmission Line Model for $V_S = Z_O$

An example of a line mismatched at the load but matched at the source is shown in Figure 2.15. For an input pulse of −1.75V to − 0.9V the initial steady state output voltage is given by:

$V_{TI} = (65/115)^*(-1.75) = -0.99V$

The final steady state output voltage is given by

$V_{TF} = (65/115)^*(-0.9) = -0.51V$

The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$V_S = (50/100)^*0.85 = 0.43V$

From Equations 7 and 8,

$\rho_L = (65-50)/(65+50) = 0.13$

$\rho_S = (50-50)/(50+50) = 0$

From Equation 9, the output voltage V_T after one line delay is:

$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = -0.51V$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$V_T(L,3T_{PD}) = V_A(t)^*[\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = -0.51V$

Thus, the output response attains its final steady state value after one line delay when the source resistance matches the line characteristic impedance. Again, ringing or a stair-step output does not occur since the load reflection coefficient is zero (Figure 2.16).

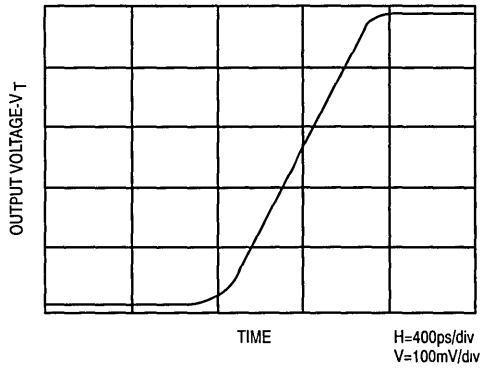


Figure 2.16. SPICE Results for Circuit of Figure 2.15

Series Termination

Series termination represents a special subcategory of Case 3 in which the load reflection coefficient is +1 and the source resistance is made equal to the line characteristic impedance by inserting a resistor, R_{ST}, between and in series with, the transmission line and the source resistance R_O. The reflections tend toward the steady state conditions of zero

current in the transmission line, and an output voltage equal to the input voltage. This type of termination is illustrated by the circuit configuration of Figure 2.17. The initial voltage down the line will be only half the amplitude of the input signal due to the voltage division of the equal source and line impedances.

$$V_S = (Z_O/(2^*Z_O))^*V_{IN} = V_{IN}/2 \qquad \text{(Equation 10)}$$

The load reflection coefficient tends to unity, thus, a voltage wave arriving at the load will double in amplitude, and a reflected wave with the same amplitude as the incident wave

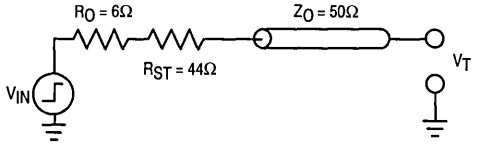


Figure 2.17. Series Terminated Transmission Line

will be reflected toward the source. Since the source resistance matches the line characteristic impedance all the energy in the reflected wave is absorbed, and no further reflections occur. This "source absorption" feature reduces the effects of ringing, making series terminations particularly useful for transmitting signals through a backplane or other interconnects where discontinuities exist.

As stated previously, the signal in the line is only at half amplitude and the reflection restores the signal to the full amplitude. It is important to ensure that all loads are located near the end of the transmission line so that a two step input signal is not seen by any of the loads.

4

For the series terminated circuit of Figure 2.17 with $R_O + R_{ST} = Z_O$ and an input pulse rising from –1.75V to – 0.9V, the initial line voltage, V_{TI} is –1.325V and the final line voltage, V_{TF}, is – 0.9V. The source is a step function with a 0.85 volt amplitude. The initial voltage traveling down the line is:

$$V_S = (50/100)^*0.85 = 0.43V$$

From Equations 7 and 8,

$$\rho_L = (\infty - 50)/(\infty+50) = 1$$

$$\rho_S = (50 - 50)/(50+50) = 0$$

From Equation 9, the output voltage V_T after one line delay is:

$$V_T(L,T_{PD}) = V_A(t)^*[1 + \rho_L] + V_{DC} = -0.9V$$

Likewise, after a time equal to three times the line delay, the output voltage V_T is:

$$V_T(L,3T_{PD}) = V_A(t)^*\rho_L{}^*\rho_S + \rho_L{}^{**}2^*\rho_S] + V_T(L,T_{PD}) = -0.9V$$

Since the load reflection coefficient is unity, the voltage at the output attains the full ECL swing, whereas the voltage at the beginning of the transmission line does not attain this level until the reflected voltage arrives back at the source termination (Figures 2.17 and 2.18). No other reflections occur because the source impedance and line characteristic impedance match.

Capacitive Effects on Propagation Delay

Lumped Capacitive Loads

The effect of load capacitance on propagation delay must

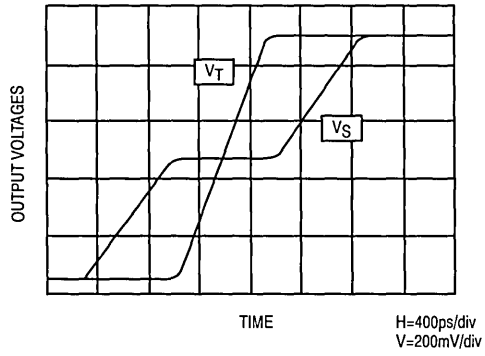


Figure 2.18. SPICE Results for Series Terminated Line

be considered when using high performance integrated circuits such as the ECLinPS family. Although capacitive loading affects both series and parallel termination schemes, it is more pronounced for the series terminated case. Figure 2.19a illustrates a series terminated line with a capacitive load C_L. Under the no load condition, C_L=0, the delay between the 50% point of the input waveform to the 50% point of the output waveform is defined as the line delay T_D. A capacitive load

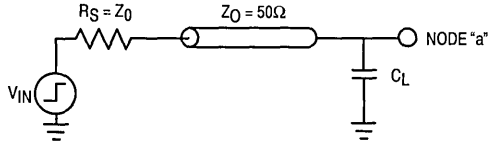


Figure 2.19a. Lumped Load Transmission Line Model

placed at the end of the line increases the rise time of the output signal, thereby increasing TD by an amount ΔT_D (Figure 2.19b). Figure 2.20 shows the increase in delay for load capacitances of 0, 1, 5, 10 and 20 picoFarads.

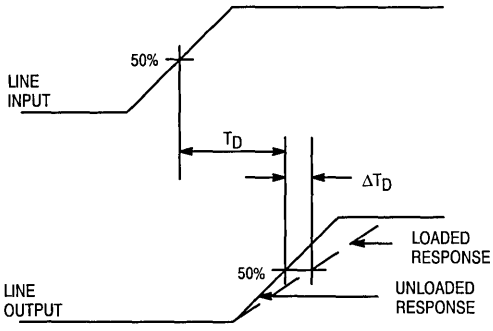


Figure 2.19b. ΔTD Introduced by Capacitive Load

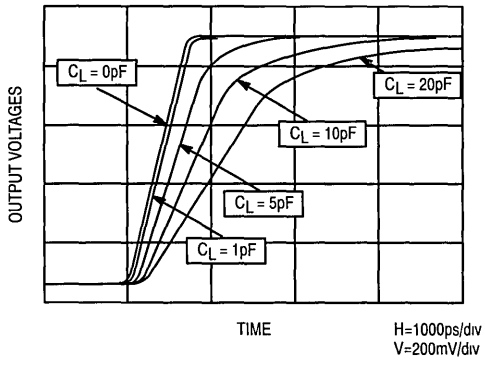
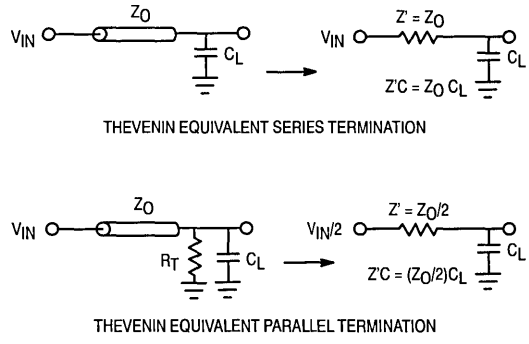


Figure 2.20. Line Delay vs Lumped Capacitive Load

The increase in propagation delay can be determined by using Thevenin's theorem to convert the transmission line into a single time constant network with a ramp input voltage. The analysis applies to both series and parallel terminations, since both configurations can be represented as a single time constant network with a time constant, τ, and a Thevenin impedance Z'.

Figure 2.21 shows the Thevenized versions for the series and parallel terminated configurations. The Thevenin impedance for the series configuration is approximately twice that for the parallel terminated case, thus the time constant will be two times greater for the series terminated configuration. Since τ is proportional to the risetime, the rise time will also be two times greater; thus the reason for the larger impact of capacitive loading on the series terminated configuration.



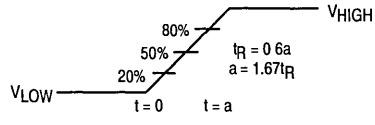


Figure 2.21. Thevenin Equivalent Lumped Capacitance Circuits

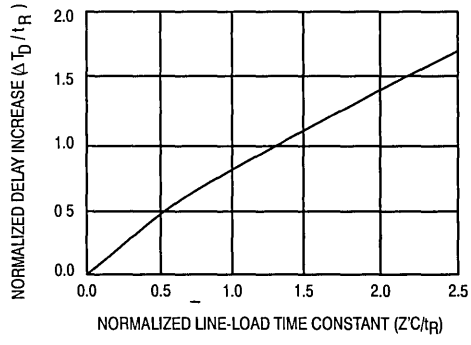


Figure 2.22. Normalized Delay Increase Due to Lumped Capacitive Load

The relationship between the change in delay and the line-load time constant is shown in Figure 2.22. Both the delay change (ΔT_D) and the line-load time constant (Z'C) are normalized to the 20–80% risetime of the input signal. This chart provides a convenient graphical approach for approximating delay increases due to capacitive loads as illustrated by the following example.

4

Given a 100Ω series terminated line with a 5pF load at the end of the line and a no load rise time of 400ps, the increase in delay, ΔT_D, can be determined using Figure 2.22. The normalized line-load time constant is:

$$Z'C/t_R = 100\Omega * 5pF/400ps = 1.25$$

Using this value and Figure 2.22:

$$\Delta T_D/t_R = 0.9$$

Therefore:

$$\Delta T_D = 0.9 * 400ps = 360ps$$

Thus, 360ps is added to the no load delay to arrive at the approximate delay for a 5pF load. For a 100Ω line employing a matched parallel termination scheme, Z' = 50Ω, the added delay is only 240ps. This added delay is significantly less than the one encountered for the series terminated case.

Thus, when critical delay paths are being designed it is incumbent on the designer to give special consideration to the termination scheme, lumped loading capacitance and line impedance to optimize the delay performance of the system.

Distributed Capacitive Loads

In addition to lumped loading, capacitive loads may be distributed along transmission lines. There are three consequences of distributed capacitive loading of transmission lines: reflections, lower line impedance, and increased propagation delay. A circuit configuration for observing distributed capacitive loading effects is shown in Figure 2.23.

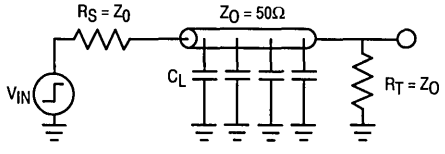


Figure 2.23. Transmission Line Model for Distributed Capacitive Load

Each capacitive load connected along a transmission line causes a reflection of opposite polarity to the incident wave. If the loads are spaced such that the risetime is greater than the time necessary for the incident wave to travel from one load to the next, the reflected waves from two adjacent loads will overlap. Figure 2.24 shows the output response for a transmission line with two distributed capacitive loads of 2.0pF separated by a line propagation time of 750ps. The upper trace, with a 20–80% input signal risetime of 400ps, shows two distinct reflections. The middle and lower traces with 20–80% risetimes of 750 ps and 950ps, respectively, show that overlap occurs as the risetime becomes longer than the line propagation delay.

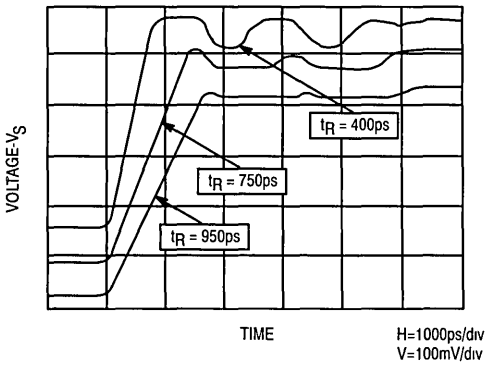


Figure 2.24. Reflections Due to Distributed Capacitance

Increasing the number of distributed capacitive loads effectively decreases the line characteristic impedance as demonstrated by Figure 2.25. The upper trace shows that reflections occur for approximately 3.5ns, during which time the characteristic impedance of the line appears lower(≈76Ω) than actual due to capacitive loading. After the reflections have ended, the transmission line appears as a short and the final steady state voltage is reached. The middle trace shows that decreasing the termination resistance to match the effective line characteristic impedance produces a response typical of a properly terminated line. Finally, the lower trace shows that the original steady state output can be attained by changing the source resistance to match the load resistance and the effective characteristic capacitance.

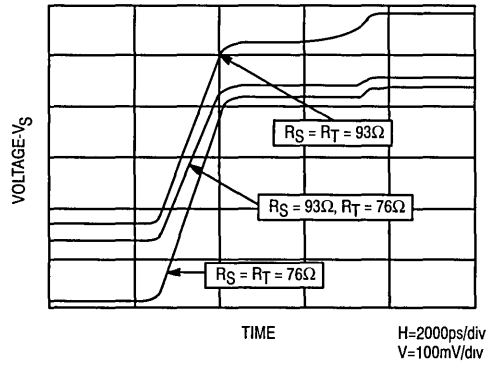


Figure 2.25. Characteristic Impedance Changes Due to Distributed Capacitive Loads

Reduced Line Characteristic Impedance

To a first order approximation the load capacitance (C_L) is represented as an increase in the intrinsic line capacitance along that portion of the transmission line for which the load capacitances are distributed. If the length over which the load capacitances are distributed is defined as "L" the distributed value of the load capacitance (C_D) is given by

$$C_D = C_L/L \qquad \text{(Equation 11)}$$

The reduced line impedance is obtained by adding C_D to C_O in Equation 1.

$$Z_O \sqrt{(L_O/C_O)}$$

$$Z_O' \sqrt{(L_O/(C_O + C_D))} = \sqrt{(L_O/(C_O{}^*(1+C_D/C_O)))}$$

$$Z_O' = Z_O/\sqrt{(1 + C_D/C_O)} \qquad \text{(Equation 12)}$$

For the circuit used to obtain the traces in Figure 2.25, the distributed load capacitance is 4pF. From Equation 3, C_O is calculated as

$$C_O = 750ps/93\Omega = 8pF$$

Hence:

$$Z_O' 93\Omega/\sqrt{(1 + 4pF/8pF)} = 76\Omega$$

Thus, the effective line impedance is 17Ω lower than the actual impedance while reflections are occurring on the line.

Line Delay Increase

The increase in line delay caused by distributed loading is calculated by adding the distributed capacitance (C_D) to the intrinsic line capacitance in Equation 2.

$$T_{PD} = \sqrt{(L_O{}^*C_O)}$$

$$T_{PD}' = \sqrt{(L_O{}^*(C_O+C_D))}$$

$$T_{PD}' = T_{PD}{}^*\sqrt{(1 + C_D/C_O)} \qquad \text{(Equation 1 3)}$$

Once again, for the circuit used to obtain the traces in Figure 2.25, the distributed load capacitance is 4pF. From the previous example, the intrinsic line capacitance is 8pF therefore,

$$T_{PD}' = 750ps\ {}^*\sqrt{(1 + 4pF/8pF)} = 919ps$$

Thus, the effect of distributed load capacitance on line delay is to increase the delay by 169ps. From Equation 13 it is obvious that the larger the C_O of the line the smaller will be the increase in delay due to a distributive capacitive load. Therefore, to obtain the minimum impedance change and lowest propagation delay as a function of gate loading, the lowest characteristic impedance line should be used as this results in a line with the largest intrinsic line capacitance.

SECTION 3
System Interconnect

Introduction

As mentioned earlier, edge rates of the ECLinPS family are such that most interconnects must be treated as transmission lines. Thus, a controlled impedance environment is necessary to produce predictable interconnect delays as well as limiting the reflection phenomena of undershoot and overshoot. The three most common techniques for circuit and/or system interconnect at high data rates are microstrip, stripline and coaxial cable; both microstrip and stripline are printed circuit board methods, whereas coaxial cable is most often used for interconnecting different parts of a system which are separated by relatively large distances. For slower speed applications (<300MHz), a twisted pair scheme also works well. The scope of this writing will not include the twisted pair technique; however, a detailed discussion of this topic can be found in the MECL System Design Handbook. Finally, wirewrap boards are not recommended for the ECLinPS family because the fast edge speeds exceed the capabilities of normal wirewrapped connections. Mismatches at the connections cause reflections which distort the fast signal, significantly reducing the noise immunity of the system and perhaps causing erroneous operation.

Printed Circuit Boards

Printed circuit boards (PCB's) provide a reliable and economical means of interconnecting electrical signals between system components. Printed circuit boards consist of a dielectric substrate over which the conducting printed circuit material is placed. Three major categories of printed circuit boards exist:

1. Single-sided boards
2. Double-sided boards
3. Multilayer boards

The most common printed circuit board material used for digital designs is a glass-epoxy laminate. These boards use a fiberglass dielectric with copper foils bonded to both sides of the dielectric material by an epoxy resin. Other substrate materials include a fiberglass dielectric with a polyimide resin and fiberglass dielectric with a teflon resin. For multilayer boards, the inner layers are separated by sheets of prepreg which acts as both a dielectric material and a bonding agent between layers.

The choice of substrate material depends on the function for which the board will be used, the environment in which the board is to operate, and costs. Table 3.1 lists several physical qualities which characterize several of the the available PCB types. Each available substrate material has its own properties which makes it ideally suited for particular applications.

Glass-Epoxy

Possesses good moisture absorption, chemical and heat resistance properties as well as mechanical strength over standard humidity and temperature ranges. The most widely used versions are G10 and FR4, the fire resistant version of G10.

Glass-Polyimide

Good for elevated temperature operation because of its tight tolerance of the coefficient of thermal expansion. Very hard material, so it may damage drilling equipment when being drilled.

Glass-Teflon

Good for use when a low dielectric material is required. Very soft material, so it may be difficult to build features requiring precise geometries. Relatively expensive material.

Material	Dielectric Constant	Dissipation Factor	Thermal Coefficient of Expansion	Tensile Modulus
Glass-Epoxy	4.8 (1.0MHz)	0.022 (1.0MHz)	13 – 16 (10^{-6}°C)	2 5
PTFE	2.1 (10GHz)	0.0004 (10GHz)	224 (10^{-6}°C)	0 05
Glass-Polyimide	4.5 (1.0MHz)	0.10 (1.0MHz)	12 – 14 (10^{-6}°C)	2.8

Table 3.1. Characteristics of Common PCB Materials

Microstrip

A microstrip line is the easiest printed circuit interconnect to fabricate because it consists simply of a ground plane and flat signal conductor separated by a dielectric (Figure 3.1).

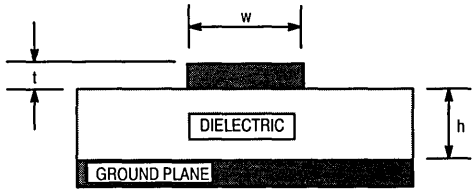


Figure 3.1. Microstrip Line

The characteristic impedance, Z_O, of a microstrip line is given by:

$$Z_O = \frac{87}{\sqrt{(\varepsilon_r + 1.41)}} \ln\left[\frac{(5.98 * h)}{(0.8w + t)}\right] \qquad \text{(Equation 1)}$$

where:

ε_r = Relative Dielectric Constant of the Substrate
w = Width of the Signal Trace
t = Thickness of Signal Trace
h = Thickness of the Dielectric

Equation 1 is accurate to within ±5% when:

$0.1 < w/h < 3.0$ and $1 < \varepsilon_r < 15$

To mitigate the effects of electric field fringing, an additional constraint is that the width of the ground plane be such that it extends past each edge of the signal line by at least the width of the signal line.

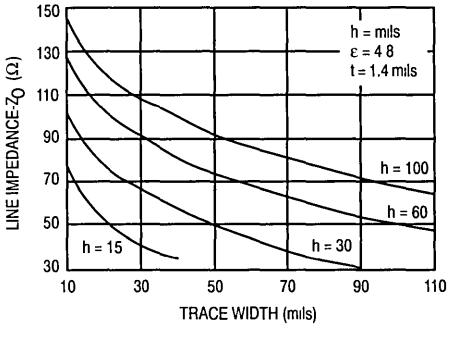
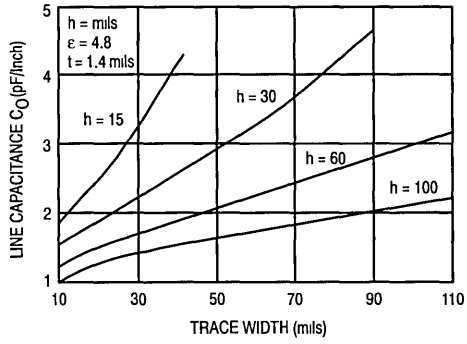


Figure 3.2. Microstrip Impedance vs Trace Width



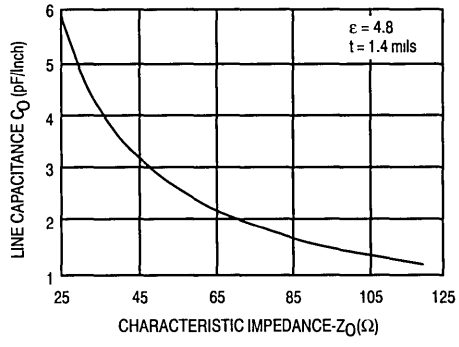


Figure 3.3. Line Capacitance vs Line Impedance and Trace Width

Figure 3.2 is a plot of characteristic impedance as a function of trace width and dielectric thickness for a dielectric constant of 4.8 and a trace thickness of 1.4mils (1 ounce copper). Using the equation for C_O, developed in the previous chapter, and Equation 1, above, the capacitance per unit length can be calculated for various trace widths. Figure 3.3 Plots C_O vs trace width for several different dielectric thicknesses. In addition, Figure 3.3 plots C_O vs the characteristic impedance for a microstrip line for the dielectric constant and trace thickness given above. The propagation delay for a signal on a microstrip line is described by the following equation:

$$T_{PD} = 1.016\sqrt{(0.475^{*}\varepsilon_r + 0.67)} \text{ ns/foot} \qquad \text{(eqt 2)}$$

where:

ε_r = Dielectric Constant of the Board Material

Note that the propagation delay is dependent only on the dielectric constant of the PCB substrate. Figure 3.4 plots the propagation delay of a microstrip line versus the dielectric constant of the PCB.

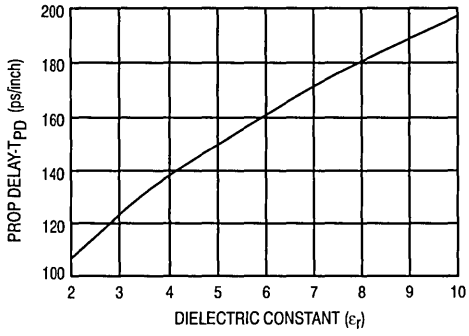


Figure 3.4. Propagation Delay vs Dielectric Constant

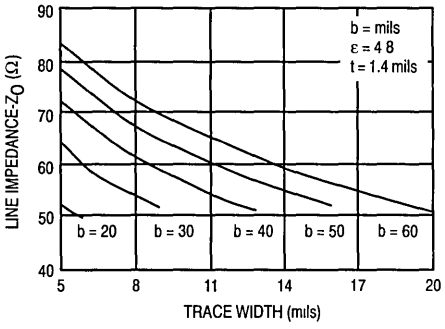


Figure 3.6. Stripline Impedance vs Trace Width

Stripline

Stripline is a printed circuit board interconnect in which a signal conductor is placed in a dielectric medium which is "sandwiched" between two conducting layers (Figure 3.5).

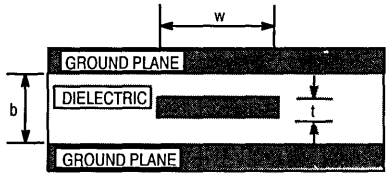
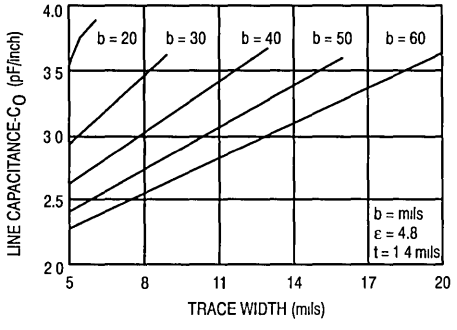


Figure 3.5. Stripline Structure



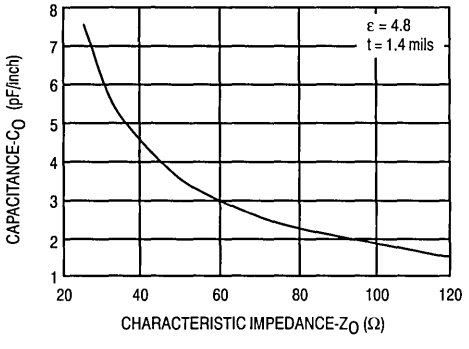


Figure 3.7. Stripline Capacitance vs Impedance and Trace Width

The characteristic impedance of the stripline is given by:

$$Z_O = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi(0.8w + t)}\right] \qquad \text{(Equation 3)}$$

where:

ε_r = Relative Dielectric Constant of the Substrate
w = Width of the Stripline
t = Thickness of the Stripline
b = Distance Between the Two Ground Planes

Equation 3 is accurate for the following dimension ratios:

$w/(b - t) < 0.35$ and $t/b < 0.25$

Once again, using a fairly typical ε_r of 4.8 and a copper trace thickness of 1.4 mils, the characteristic impedance of a stripline interconnect can be plotted for various trace widths and dielectric thicknesses (Figure 3.6).

As was the case with a microstrip line, the capacitance per unit length of a stripline trace can be calculated using the C_O equation from Chapter 2. The graphs of Figure 3.7 plot the capacitance of a stripline structure for a number of trace widths as well as the C_O versus the characteristic impedance of the line.

The propagation delay of a stripline trace is governed by the simple equation:

$$T_{PD} = 1.016\sqrt{\varepsilon_r} \text{ ns/ft} \qquad \text{(Equation 4)}$$

where:

ε_r = Dielectric Constant of the Board Material

Again, the propagation delay of the trace is dependent only on the relative dielectric constant of the PCB substrate. Using Equation 4 the delay of the line can be plotted vs dielectric constant (Figure 3.8).

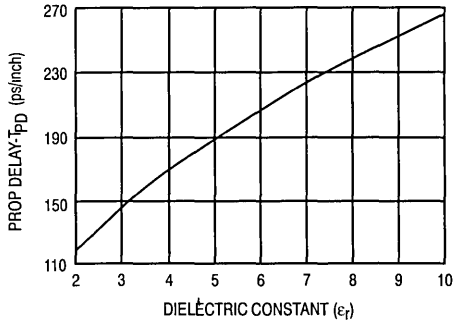


Figure 3.8. Stripline Propagation Delay vs Dielectric Constant

General Information

Since fiberglass-epoxy is by far the most widely used substrate in the industry, two important considerations should be mentioned:

1. The propagation delay for microstrip is ≈145ps per inch, whereas that for stripline is ≈185ps per inch. Since the propagation delay is governed by the dielectric of the substrate, a board material with a lower dielectric constant than glass-epoxy is required if a lower propagation delay is desired.

2. Cross coupled noise due to board geometries may require a substrate material with a lower dielectric constant. For example, the distance from the signal trace to the ground plane is a function of the substrate dielectric constant for a specified line characteristic impedance. Hence, the switching energy coupled into adjacent traces on the same signal plane is also a function of the dielectric constant. If the dielectric thickness and trace width must be maintained for a given line impedance, the spacing between traces must be increased to maintain the noise margin. Since the dielectric constant of glass-epoxy is relatively large, the increase in spacing between the traces may be unacceptable. So, a substrate material with a lower dielectric constant may be desirable. Generally, if the distance between traces is maintained at twice the distance to the ground plane, coupling between traces will be minimal.

Finally, printed circuit signal line shape variations play a significant role in modulating both the capacitance and inductance per unit length for a transmission line; in other words, shape variations cause reflections. Bends in printed circuit traces cause an increase in the capacitance per unit length and a decrease in the inductance per unit length with a pronounced effect for angles of 90° or more. Two techniques available to compensate for shape changes are:

1. Maintain a uniform trace width.

2. Cut the corners of the trace such that the length of the diagonal cut is in the range of 1.6 to 2.0 times the trace width.

Figure 3.9 illustrates these two techniques.

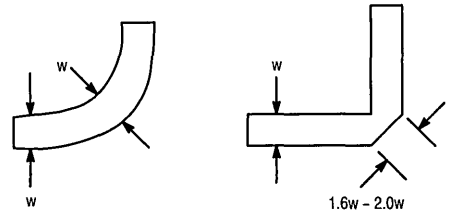


Figure 3.9. Compensation for Capacitive Effects of Trace Angles

Coaxial Cable

Coaxial cable is a two conductor transmission line consisting of a concentric inner conductor surrounded by a dielectric which in turn is surrounded by a tubular outer conductor (Figure 3.10). It is ideal for transmitting high frequency signals over long distances because of its well defined and uniform characteristic impedance. Moreover, crosstalk is minimized by the ground shield provided by the outer conductor.

The propagation delay is derived in the same way as a stripline interconnect and, thus, is described by Equation 4. Therefore, as with stripline structures, the delay is a function

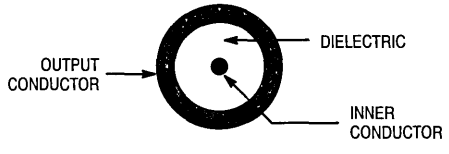


Figure 3.10. Cross Section of Coaxial Cable

of only the dielectric constant. The characteristic impedance and capacitance per unit length are parameters specified by the coaxial cable manufacturer; hence, the designer should look to the cable manufacturer for these parameters.

Coaxial Cable Lengths

The ECLinPS family operates with rise times as fast as several hundred picoseconds; thus, coaxial cable must be able to transmit these pulses without introducing a significant distortion. Viewing the ECLinPS output as a single time constant driver circuit terminated with a 50Ω load, the required line bandwidth(f_C) can be calculated as follows.

$$f_C = 0.35/t_R \qquad \text{(Equation 5)}$$

where:

t_R =10% to 90% Rise Time

Converting the typical 20% – 80% rise time value of 400ps to an equivalent 10% – 90% rise time value of 530ps, and using Equation 5 yields a bandwidth value of f_C = 660MHz

Below 1.0GHz the primary loss mechanism in transmission lines is skin effect, as dielectric losses for materials such as polyethylene and teflon are insignificant below this value. Since attenuation due to skin effect is proportional to the square root of frequency, a log-log plot of attenuation versus frequency produces a linear result. The maximum coaxial cable lengths for the ECLinPS family can be derived from the plot in Figure 3.11.

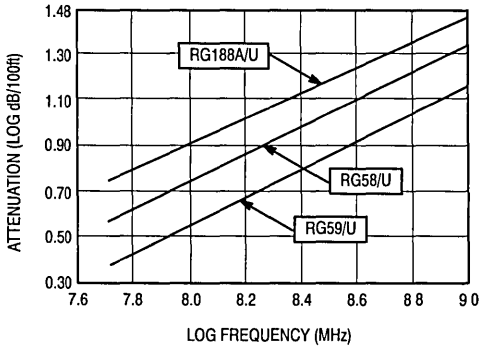


Figure 3.11. Coaxial Cable Attenuation vs Frequency

Typically for an ECL system, the minimum peak-to-peak signal swing is 600mV. The nominal peak-to-peak signal swing for the ECLinPS family is approximately 850mV. Thus, the maximum permissible attenuation is:

$$\text{Loss(dB)} = 20 * \log (V_{IN}/V_O)$$
$$= 20 * \log (0.85/0.6) = 3.0\text{dB}.$$

From Figure 3.11 the loss at 660MHz for RG58/U cable is 15 dB/100 feet. Therefore, the maximum length is

Max Length = 100 ft. * (3.0dB/15dB) = 20 ft.

Additional information concerning coaxial cable can be found in Motorola's MECL System Design Handbook.

Summary of Values

Table 3.2 is a compilation of propagation delays at nominal dielectric values for the three types of interconnects discussed.

Interconnect	T_{PD}	ε_r
Microstrip	145ps/in	4.8
Stripline	185ps/in	4.8
Coaxial Cable	123ps/in	2.1

Table 3.2 - Comparison of Interconnect Medium

Termination Techniques

From transmission line theory, a signal propagating down the line is partially reflected back to the source if the line is not terminated in its characteristic impedance. The magnitude of the reflected voltage signal is governed by the load reflection coefficient, ρ_L.

$$\rho_L = (R_T - Z_O) / (R_T + Z_O) \qquad \text{(Equation 6)}$$

where:

R_T = Load Impedance, and

Z_O = Characteristic Impedance of the Line

When the reflected signal arrives at the source it is re-reflected back toward the load with a magnitude dictated by the source reflection coefficient, ρ_S.

$$\rho_S = (R_S - Z_O) / (R_S + Z_O) \qquad \text{(Equation 7)}$$

where:

R_S = Source Impedance

Z_O = Characteristic Impedance of the Line

The reflected signal continues to be re-reflected by the source and load impedances and is attenuated with each passage over the transmission line. The output response appears as a damped oscillation asymptotically approaching the steady state value. This phenomena is often referred to as ringing.

The importance of minimizing the reflected signals lies in their adverse affect on noise margin and the potential for driving the input transistors of the succeeding stage into saturation. Both of these phenomena can lead to less than ideal system performance. To minimize the potential hazards associated with reflections on transmission lines three basic termination techniques are available:

1. Minimizing Unterminated line lengths
2. Parallel Termination
3. Series Termination

Unterminated Lines

Figure 3.12 illustrates an unterminated transmission line. This configuration is also referred to as a stub or an open line.

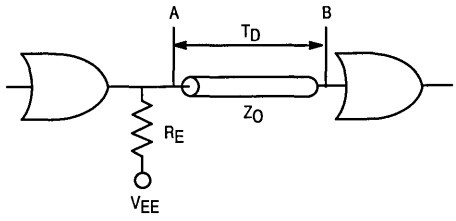


Figure 3.12. Unterminated Transmission Line

The function of R_E is to provide the drive current for a high to low transition at the driver output. Since the reflection coefficient at the load is of opposite polarity to that at the source, the signal will be reflected back and forth over the transmission with the polarity changing after each reflection from the source impedance. Thus, steps appear at the input to the receiving gate. When R_E is too large, steps appear in the trailing edge of the propagating signal that slows the edge speed of the input to the receiving gate, subsequently causing an increase in the net propagation delay. A reasonable negative-going signal swing at the input of the receiving gate results when the value of R_E is selected to produce an initial step of 600mV at the driving gate. Hence:

$$I^*Z_O > 0.6 \qquad \text{(Equation 8)}$$

$$(V_{OH} - V_{EE})/(R_E + Z_O)\ ^*\ Z_O \geq 0.6$$

$$6.2Z_O \geq R_E\ (10E),\ 4.9Z_O \geq R_E\ (100E) \qquad \text{(Equation 9)}$$

Load resistors of less than 180Ω should not be used because the heavy load may cause a reduction in noise immunity when the output is in the high state due to an increased output emitter-follower V_{BE} drop.

When the driver gate delivers a full ECL swing, the signal propagates from point A arriving at point B a time T_D later. At point B, the signal is reflected as a function of ρ_L. The input impedance of the receiving gate is large relative to the line characteristic impedance, therefore:

$$\rho_L = (R_T - Z_O) / (R_T + Z_O) \approx 1 \qquad \text{(Equation 10)}$$

A large positive reflection occurs resulting in overshoot. The reflected signal reaches point A at time $2T_D$, and a large negative reflection results because the output impedance of the driver gate is much less than the line characteristic impedance (i.e. $R_O << Z_O$). In this case, the reflection coefficient is negative.

$$\rho_S = (R_O - Z_O)/(R_O + Z_O) \qquad \text{(Equation 11)}$$

The signal is re-reflected back toward the load arriving at time $3T_D$ resulting in undershoot at point B. This re-reflection of signals continues between the source and load impedances causing ringing to appear on the output response.

The impetus in restricting interconnect lengths is to mitigate the effects of overshoot and undershoot. A handy rule of thumb is that the undershoot can be limited to less than 15% of the logic swing if the two way line delay is less than the rise time of the pulse With an undershoot of < 15%, the physics of the situation will result in an overshoot which will not cause saturation problems at the receiving input. Thus, the maximum line length can be determined using Equation 12.

$$L_{max} < t_R/2^*T_{PD}\ \text{(unit length)} \qquad \text{(Equation 12)}$$

where:

L = Line Length

t_R = Rise time

T_{PD} = Propagation Delay per unit Length

Further, the propagation delay increases with gate loading, thus, the actual delay per unit length (T_{PD}') is given as:

$$T_{PD}' = T_{PD}\ ^*\sqrt{(1 + C_D / (L^* C_O))}$$

Substitution of the modified delay per unit length into Equation 12 and rearranging yields Equation 13:

$$t_R \geq (2\ ^*\ L)\ ^*\ T_{PD}\ ^*\ \sqrt{(1 + C_D / (L\ ^*\ C_O))} \qquad \text{(Equation 13)}$$

Solving Equation 13 for the maximum line length produces:

$$L_{max} = 0.5\ ^*\ (\sqrt{(\ (C_D / C_O)\ ^{**}\ 2 + (t_R/T_{PD})\ ^{**}\ 2)} - C_D/C_O \qquad \text{(Equation 14)}$$

Assuming a worst case capacitance of 2pF and a rise time of 200 ps for the ECLinPS family gives a value of 0.3 inches for the maximum open line length.

Table 3.3 shows maximum open line lengths derived from SPICE simulations for single and double gate loads, a maximum overshoot of 40% and undershoot of 20% was assumed. The simulation results indicate that for a 50Ω line, a stub length of ≤ 0.3 inches will limit the overshoot to less than 40%, and the undershoot to within 20% of the logic swing. Signal traces will most assuredly be larger than 0.3″ for all but the simplest of interconnects, thus, for most practical applications, it will be necessary to use ECLinPS devices in a controlled impedance environment.

$Z_O(\Omega)$	Microstrip		Stripline	
	Fanout = 1	Fanout = 2	Fanout = 1	Fanout = 2
	L_{max} (in)	L_{max} (in)	$L_{(max)}$ (in)	$L_{(max)}$ (in)
50	0.3	0 2	0.3	0.15
68	0.3	0.15	0 25	0.1
75	0.3	0.15	0.25	0.1
82	0.3	0 1	0.25	0.1
90	100	0.1	0 25	0.1
100	0.25	0.1	0.25	0.1

Table 3.3. SPICE Derived Maximum Open Line Lengths for ECLinPS Designs

Parallel Termination

When the fastest circuit performance or the ability to drive distributed loads is desired, parallel termination is the method of choice. An important feature of the parallel termination scheme is the undistorted waveform along the full length of the line. A parallel terminated line is one in which the receiving end is terminated to a voltage (V_{TT}) through a resistor (R_T) with a value equal to the line characteristic impedance (Figure 3.13a). An advantage of this technique is that power consumption can be decreased by a judicious choice of V_{TT}. For 50Ω systems, the typical value of V_{TT} is negative two volts.

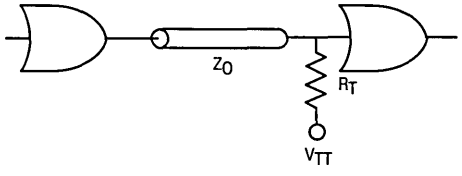


FIGURE 3.13A PARALLEL TERMINATION TO V_{TT}

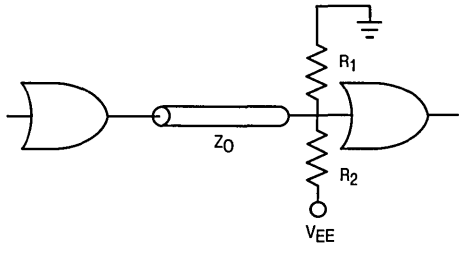


FIGURE 3.13B THEVENIN EQUIVALENT PARALLEL TERMINATION

Figure 3.13 Parallel Termination Schemes

Although the single resistor termination to V_{TT} conserves power, it offers the disadvantage of requiring an additional supply voltage. An alternate approach to using a single power supply is to use a resistor divider network as shown in Figure 3.13b. The Thevenin equivalent of the two resistors is a single resistor equal to the characteristic impedance of the line, and terminated to V_{TT}. The values for resistors R1 and R2 may be obtained from the following relationships:

$$R_2 = (V_{EE} / V_{TT}) * Z_O \quad \text{(Equation 15)}$$

$$R_1 = (R_2 * V_{TT})/(V_{EE} - V_{TT}) \quad \text{(Equation 16)}$$

For a nominal 10E supply voltage of – 5.2V and V_{TT} of – 2V:

$$R_2 = 2.6 * Z_O \quad \text{(Equation 17)}$$

$$R_1 = R_2 / 1.6 \quad \text{(Equation 18)}$$

For a nominal 100E supply voltage of – 4.5V and V_{TT} of – 2V

$$R_2 = 2.25 * Z_O \quad \text{(Equation 19)}$$

$$R1 = R2 / 1.25 \quad \text{(Equation 20)}$$

Table 3.4 provides a reference of values for the resistor divider network of Figure 3.13b.

ZO (Ω)	10E		100E	
	R_1 (Ω)	R_2 (Ω)	R_1 (Ω)	R_2 (Ω)
50	81	130	90	113
70	113	182	126	158
75	121	195	135	169
80	130	208	144	180
90	146	234	161	202
100	162	260	180	225
120	194	312	216	270
150	243	390	270	338

Table 3.4. Thevenin Termination Resistor Values

For both configurations, when the equivalent termination resistance matches the line impedance no reflection occurs because all the energy in the signal is absorbed by the termination. Hence, the primary tradeoff between the two types of termination schemes are power versus power supply requirements. As mentioned earlier, the V_{TT} scenario requires an extra power supply; however, the Theveninization technique will consume 10 fold more DC power. Fortunately, this extra power consumption will not be seen on the die, therefore, both techniques will result in the same die junction temperatures.

ECLinPS output drivers consists of emitter followers designed to drive a 50Ω load into a negative two volt supply (V_{TT}). Under these conditions, the nominal 10E output levels are –1.75 volts at 5mA for the low state and – 0.9 volts at 22mA for the high state. For the 100E devices, the nominal output levels are – 0.955 volts at 20.9mA for the high state and 1.705 volts at 5.9mA for the low state.

Figure 3.14 shows the nominal output characteristics for ECLinPS devices driving various load impedances returned to a negative two volt supply. This plot applies to both 10E and 100E versions of the ECLinPS family. The output resistances, R_H (high state output resistance) and R_L (low state output resistance), are obtained from the reciprocal of the slope at the desired operating point. Many applications require loads other than 50Ω, the resulting V_{OH} and V_{OL} levels can be estimated using the following technique.

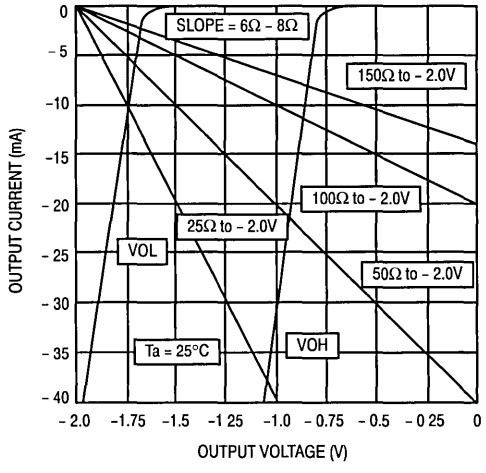


Figure 3.14. ECLINPS Output Characteristics

10E Devices

The equivalent output circuit is shown in Figure 3.15. The output levels are estimated from Figure 3.15 as follows:

$$V_{OH} = -770mV - 6^{*}I_{HOUT} \qquad \text{(Equation 21)}$$

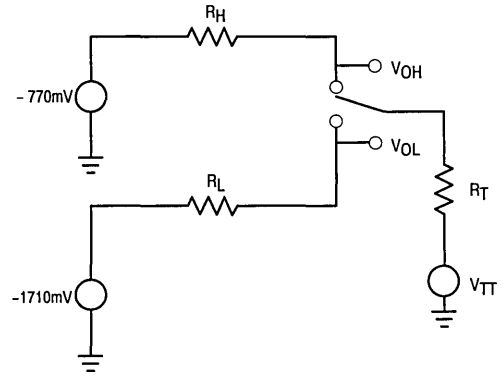


Figure 3.15. Equivalent Model for Calculating 10E Output Levels

where:

$$I_{HOUT} = (-770mV - V_{TT})/(6\Omega + R_T)$$

and

$$V_{OL} = -1710mV - 8^{*}I_{LOUT} \qquad \text{(Equation 22)}$$

where:

$$I_{LOUT} = (-1710mV - V_{TT}) / (8\Omega + R_T)$$

100E Devices

The equivalent output circuit is shown in Figure 3.16. The output levels are estimated from Figure 3.16 as follows:

$$V_{OH} = -830mV - 6^{*}I_{HOUT} \qquad \text{(Equation 23)}$$

where:

$$I_{HOUT} = (-830mV - V_{TT}) / (6\Omega + R_T)$$

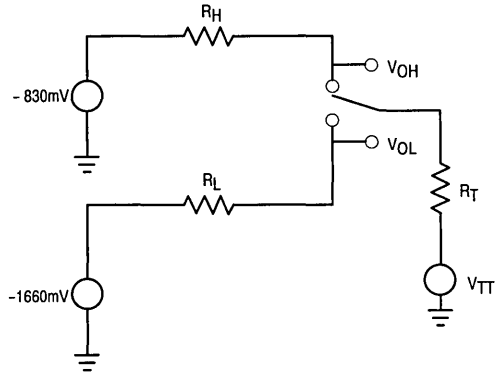


Figure 3.16. Equivalent Circuit for Calculating 100E Output Levels

and

$$V_{OL} = -1660mV - 8 * I_{LOUT} \quad \text{(Equation 24)}$$

where:

$$I_{LOUT} = (-1660mV - V_{TT})/(8\Omega + R_T)$$

SIP Resistors

The choice of resistor type for use as the termination resistor has several alternatives. Although the use of a discrete, preferably chip resistor, offers the best isolation and lowest parasitic additions, there are SIP resistor packs which will work fine for ECLinPS designs. SIP resistors offer a level of density which is impossible to obtain using their discrete counterparts. However, there are some guidelines which the user should follow when using SIP resistor packs. Always terminate complimentary outputs in the same pack to minimize inductance effects on the SIP power pin. Noise generated on this pin will couple directly into all of the resistors in the pack. In addition, the SIP package should incorporate bypass capacitors in the design (Figure 3.17). These capacitors are necessary to help maintain a solid V_{TT} level within the package, again mitigating any potential crosstalk or feed through effects. A 10 pin SIP like the DALE CSRC-10B21-500J/103M, is suitable for providing 50Ω terminations while maintaining a relatively noise free environment to non-switching inputs.

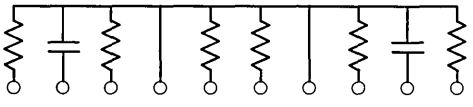


Figure 3.17. Standard ECL 10 pin SIP

Series Termination Technique

Series Damping is a technique in which a termination resistance is placed between the driver and the transmission line with no termination resistance placed at the receiving end of the line (Figure 3.18).

Series Termination is a special case of series damping in which the sum of the termination resistor (R_{ST}) and the output impedance of the driving gate (R_O) is equal to the line characteristic impedance.

$$R_{ST} + R_O = Z_O$$

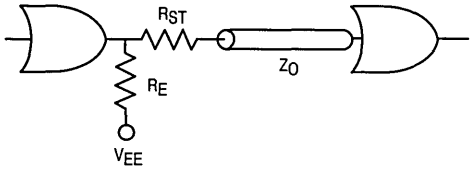


Figure 3.18. Series Termination

As mentioned in the Transmission line section, series termination techniques are useful when the interconnect lengths are long or impedance discontinuities exist on the line. Additionally, the signal travels down the line at half amplitude minimizing problems associated with crosstalk. Unfortunately, a drawback with this technique is the possibility of a two step signal appearing when the driven inputs are far from the end of the transmission line. To avoid this problem, the distance between the end of the transmission line and input gates should adhere to the guidelines specified in Table 3.3 from the section on unterminated lines.

Series Termination Theory

When the output of the series terminated driver gate switches, a change in voltage (ΔV_B) occurs at the input to the transmission line:

$$\Delta V_B = V_{IN} * (Z_O) / (R_{ST} + R_S + Z_O) \quad \text{(Equation 25)}$$

where:

V_{IN} = Internal Voltage Change
Z_O = Line Characteristic Impedance
R_S = Output Impedance of the Driver Gate
R_{ST} = Termination Resistance

Since $Z_O = R_{ST} + R_S$ substitution into Equation 25 yields:

$$\Delta V_B = V_{IN}/2 \quad \text{(Equation 26)}$$

From Equation 26 an incident wave of half amplitude propagates down the transmission line. Since the transmission line is unterminated at the receiving end, the reflection coefficient at the load is approximately unity; therefore, the reflection causes the voltage to double at the receiving end. When the reflected wave arrives at the source end, its energy is absorbed by the series resistance, producing no further reflections as the impedance is equal to the characteristic impedance of the line.

An extension of the series termination technique, using parallel fanout, eliminates the problem of lumped loading at the expense of extra transmission lines (Figure 3.19).

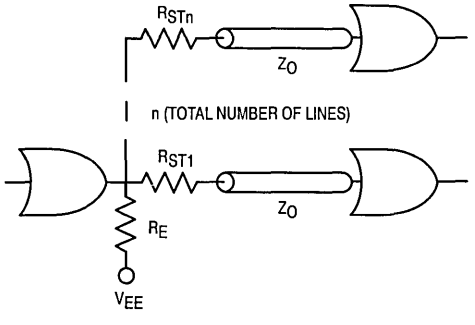


Figure 3.19. Parallel Fanout using Series Termination

Calculation of R_E

R_E functions to establish V_{OH} and V_{OL} levels and to provide the negative going drive into R_{ST} and Z_O when the driver output switches to the low state. The value of R_E must

be such that the required current is supplied to each transmission line while not allowing the output transistor to turn off when switching from a high to a low state. An appropriate model is to treat the output emitter follower as a simple switch (Figure 3.20).

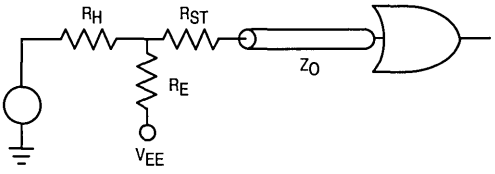


Figure 3.20. Equivalent Circuit for R_E Determination

The worst case scenario occurs when the driver output emitter follower is cutoff during a negative going transition. When this happens, the switch can be considered opened and, at the instant it opens, the line characteristic impedance behaves as a linear resistor returned to V_{OH}. The model becomes a simple series resistive network as shown in Figure 3.21.

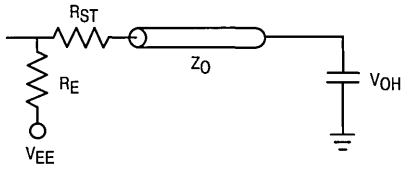


Figure 3.21. Equivalent Circuit with Output Cutoff

The maximum current occurs at the instant the switch opens and is given by Equation 27.

$$I_{MAX} = (V_{OH} - V_{EE}) / (R_E + R_{ST} = Z_O) \text{(Equation 27)}$$

The initial current must be sufficient to generate a transient voltage equal to half of the logic swing since the voltage at the receiving end of the line doubles for the series terminated case. To insure the pull down current is large enough to handle reflections caused by discontinuities and load capacitances, the transient voltage is increased by 25%. Therefore,

$$I_{INIT} = (1.25 * V_{SWING}/2) / Z_O \qquad \text{(Equation 28)}$$

To satisfy the initial constraints $I_{MAX} > I_{INT}$

$$(V_{OH} - V_{EE}) / (R_E + R_{ST} + Z_O) > (1.25 * V_{SWING}/2) / Z_O$$

For the 10E series

$$V_{OH} = -0.9V,\ V_{SWING} = 0.85V,\ V_{EE} = -5.2$$

$$[-0.9 - (-5.2)] / R_{ST} + R_E + Z_O) \geq 0.531 / Z_O$$

$$7.10 * Z_O - R_{ST} \geq R_E \qquad \text{(Equation 29)}$$

For the 100E series:

$$V_{OH} = -0.955V,\ V_{SWING} = 0.75,\ V_{EE} = -4.5V$$

$$6.56 * Z_O - R_{ST} > R_E \qquad \text{(Equation 30)}$$

Figure 3.19 showed a modification of the series termination scheme in which several series terminated lines are driven by a single ECL gate. The principle concern when applying this technique is to maintain the current in the output emitter follower below the maximum rated value. The value for R_E can be calculated by viewing the circuit in terms of conductances.

$$G_E > G_1 + G_2 + \ldots + G_n \qquad \text{(Equation 31)}$$

For the 10E series

$$1 / R_E \geq \quad 1 / (7.10 * Z_{O1} - R_{ST1}) + 1 / (7.10 * Z_{O2} - R_{ST2}) + 1 / (7.10 * Z_{O3} - R_{STn})$$

For the case where

$$Z_{O1}=Z_{O2}=\ldots Z_{On} \text{ and } R_{ST1}=R_{ST2}=R_{STn}$$

$$R_E \leq (7.10 * Z_O - R_{ST}) / n \qquad \text{(Equation 32)}$$

where n is the number of parallel circuits.

For the 100E series

$$1 / R_E \geq \quad 1 / (6.56 * Z_{O1} - R_{ST1}) + 1 / (6.56 * Z_{O2} - R_{ST2}) + 1 / (6.56 * Z_{O3} - R_{STn})$$

For the case where

$$Z_{O1}=Z_{O2}=\ldots Z_{On} \text{ and } R_{ST1}=R_{ST2}=R_{STn}$$

$$R_E \leq (6.56 * Z_O - R_{ST}) / n \qquad \text{(Equation 33)}$$

where n is the number of parallel circuits.

When a series terminated line is driving more than a single ECL load the issue of maximum number of loads must be addressed. The factor limiting the number of loads is the voltage drop across the termination resistor caused by the input currents to the ECL loads when the loads are in the quiescent high state. A good rule of thumb is to determine if the loss in high state noise margin is acceptable. The loss in noise margin is given by

$$NM_{LOSS} = I_T * (R_{ST} + R_O) \qquad \text{(Equation 34)}$$

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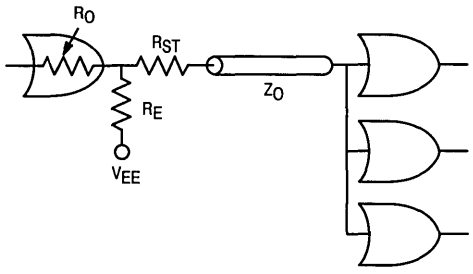


Figure 3.22. Noise Margin Loss Example

where:

I_T = Sum of I_{INH} Currents

For the majority of devices in the ECLinPS family the typical maximum value for quiescent high state input current is 150μA. Thus, for the circuit shown in Figure 3.22, in which three gate loads are present in a 50Ω environment, the loss in high state noise margin is calculated as:

$$NM_{LOSS} = 3 * 150\mu A * 50\Omega = 22.5mV$$

ECLinPS I/O SPICE Modeling Kit

Due to the heavier reliance on simulation tools for initial prototyping, Motorola has put together a SPICE modeling kit aimed at aiding the customer in modeling board interconnect behavior. The kit includes representative drivers and receivers as well as the necessary SPICE model parameters. In addition, tips are provided for simulating a wide range of output conditions. The kit, in conjunction with today's CAD tools, can greatly simplify the design and characterization of critical nets in a design. Anyone interested in using SPICE for this purpose, is encouraged to read Application Note AN1503 located on page 4-65.

SECTION 4
Interfacing With ECLinPS

Interfacing to Existing ECL Families

There currently exists two basic standards for high performance ECL logic devices: 10H and 100K. To maximize system flexibility each member of the ECLinPS family is available in both of the existing ECL standards: 10E series devices are compatible with the MECL 10H family; 100E series devices are compatible with ECL 100K.

The difference in the DC behavior of the outputs of the two different standards necessitates caution when mixing the two technologies into a single ended input design. As illustrated in Figure 4.1 and Table 4.1, there is no problem when a 10H device is used to drive a 100K device; however, problems arise when the scenario is reversed.

For the case of a 100K device driving a 10H device, the worst case noise margin is reduced to 35mV, a noise margin which is unacceptable for most designs. Since the problems of interfacing are an output tracking rate vs a V_{BB} tracking rate problem, if the system uses only differential interconnect between the two technologies there will be no loss of noise margin and the design will operate as desired.

Fortunately, the ECLinPS family, by offering devices in both standards, allows the user to integrate higher performance technology into his design without having to battle these interface problems.

Another area of concern when interfacing to older, slower logic families, is the behavior of ECLinPS devices with slower input edge rates. Typically, other than clock inputs, the ECLinPS family will function properly for edge speeds of up to 20ns. For edges significantly slower than 20ns, the Schmitt trigger circuit of Figure 4.2 can be used to sharpen the edge rates reliably.

Obviously, a very slow edge rate will amplify differences in delay paths due to any offset of the V_{BB} switching reference. This extra delay should be included in speed calculations of a design. For calculation purposes a worst case ± 200ps/ns

Drvr > Rcvr	NM – High	NM – Low
10H > 10H	150mV	150mV
10H > 100H	145mV	125mV
100H > 100H	130mV	135mV
100H > 10H	35mV	130mV

Table 4-1. Worst-Case Noise Margins of a Mixed 10H and 100K Design

gate-gain delay (delay vs input edge rate) can be assumed or a more typical value of ±75ps/ns can be used.

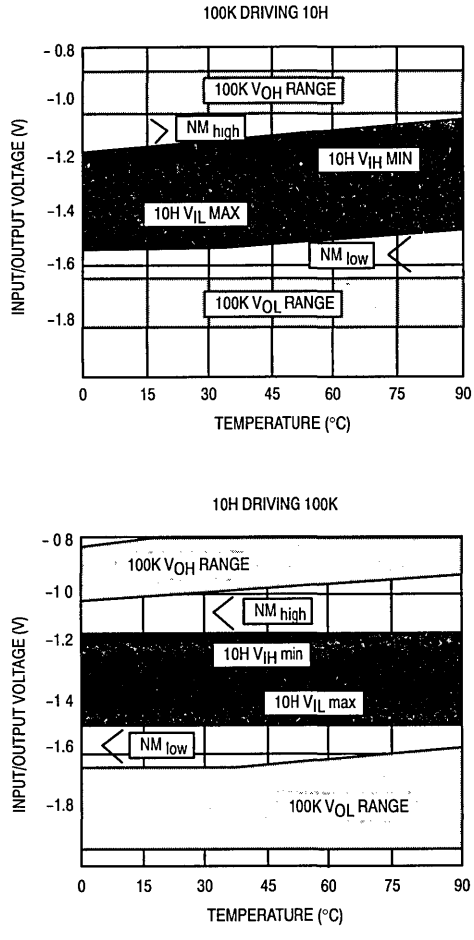


Figure 4.1. Interfacing 10H ECL and 100K ECL

Clock inputs on flip-flop devices in the ECLinPS family are especially sensitive to slow edge rates. Flip-flops have been successfully clocked in a noise free bench setup environment with edge rates of up to 20ns. However, in ATE systems where more noise is present, clocking problems arise with input edge rates of greater than 6.0 or 7.0ns. To ensure reliable operation in a system with input clock edges slower than 7.0ns, it is recommended that the signals be buffered

4

with an ECLinPS buffer circuit (E122, E116, E101, etc.) or, for extreme conditions, the Schmitt trigger of Figure 4.2 to provide the gain necessary to sharpen the edges on the clock pulse.

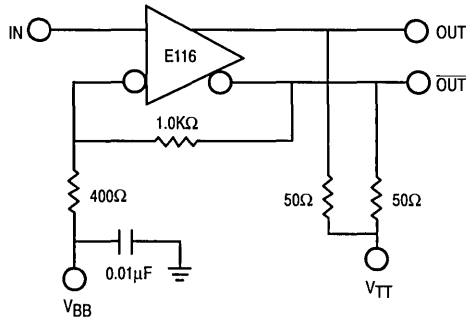


Figure 4.2. Schmitt Trigger w/100MV of Hysteresis

Interfacing to TTL/CMOS Logic

To interface ECLinPS devices to TTL or CMOS subsystems there exists several new product offerings, as well as several existing devices, in the MECL 10KH family which are ideally suited to the task. These translation devices are specially suited for clock distribution, DRAM driving as well as general purpose translation in both single supply and dual supply environments. In mixed technology environments, it is recommended that the noisy supplies of TTL and CMOS circuits be isolated from the ECL supplies. This can be done either through separate power planes in the board or a common plane with isolated ECL and TTL power sub-planes. The planes of common voltages (i.e. ECL V_{CC} and TTL ground for split supply systems or common V_{CC} and ground for a single supply system) should then be connected to a common system ground or power supply through an appropriate edge connector.

Interfacing to GaAs Logic

In general GaAs logic is designed to interface directly with ECL; however, in some instances, the worst case V_{OH} of a GaAs output can go as high as – 0.3V. An ECLinPS device, depending on the input structure, may become saturated when driven with a – 0.3V signal. Application Note AN1404, on page 4-41, deals exclusively with this phenomenon.

AC Coupling

In some cases, it may be necessary to interface an ECLinPS design with a signal which lacks any DC offset.The differential devices in the ECLinPS family are ideally suited for this application. As pictured in Figure 4.3, the signal can be AC coupled and biased around the V_{BB} switching reference of the device. Note that this scheme only works for a data stream with no DC bias, for data streams such as RZ or unencoded NRZ DC, restoration must be performed prior to AC coupling it to an ECLinPS device.

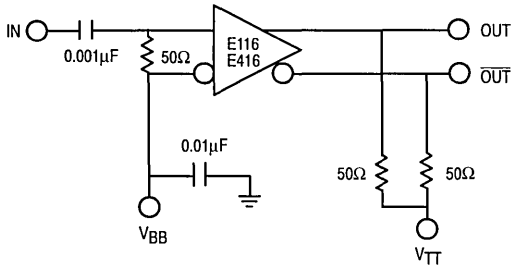


Figure 4.3. AC Couple Circuit

The 50Ω resistor of Figure 4.3 provides the termination impedance while the V_{BB} pin provides the DC offset. The capacitor used to couple the signal must have an impedance of << 50Ω for all frequency components of the input signal. Because large capacitors appear somewhat inductive at high frequencies, it may be necessary to use a small capacitor in parallel with a larger one to achieve satisfactory operation. In addition, it is important to bypass the V_{BB} line when used in this manner to minimize the noise coupled into the device.

Because the AC signal is biased around V_{BB}, the output of the ECLinPS device, when AC coupled, will have a duty cycle identical to the input. Thus, this type of application is ideal for transforming high frequency sinusoidal waveforms from an oscillator into a square wave with a 50% duty cycle. The E416 device is a specialized line receiver with a much higher bandwidth than alternative ECLinPS devices; therefore, for frequencies of > 500MHz, it is recommended that the designer use this device.

The above mentioned scenario will work fine as long as the input signal is present, however, if the the inputs to the AC coupled device are left open, problems may occur. With no input signal both inputs will go to V_{BB} and an undefined output, and perhaps, an oscillating output, will result. If a defined output is necessary for an open input scenario, the circuit of Figure 4.4 can be used. The resistor tree between V_{CC} and V_{BB} creates an offset between the two inputs so that if the driving signal is lost, a stable defined output will occur.

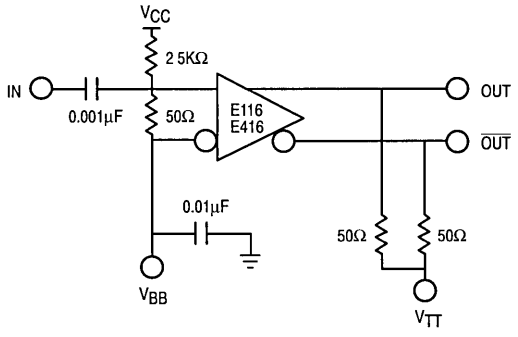


Figure 4.4. AC Couple Circuit with DC Offset

Unfortunately, this configuration will adversely affect the duty cycle of the output. Depending on the frequency of the output, the duty cycle will change due to the longer distance to threshold on a rising edge as opposed to a falling edge. With this in mind, it becomes obvious that the smallest feasible offset would be the best solution. For stability, a minimum of 25mV is recommended, however, this will not produce full ECL levels at the outputs of an E116 and, thus, another differential gate should be used to further amplify the signal. The gain of the E416, on the other hand, is sufficient to produce acceptable levels at the outputs for DC input voltage differences of 25mV. If a 150mV offset is used, full ECL levels will be seen at the outputs of the E116, however, the price in duty cycle skew will be high. Of course, if the signal is divided after it is received, the duty cycle will be restored.

When using the circuit of Figure 4.4 care should be taken to limit the current sunk by the V_{BB} pin to a maximum of 0.5mA. To achieve an offset of greater than 25mV for the circuit of Figure 4.4, the DC current will necessarily need to be greater than 0.5mA. To alleviate this dilemma, one of the gates of the E116 can be configured as pictured in Figure 4.5 to generate a V_{BB} reference with the necessary current sinking capability. A single gate configured in this way will source or sink up to 10mA without a significant shift in the generated V_{BB} level. If more current is needed, several gates can be connected in parallel to provide the extra drive capability.

Note that the circuit pictured in Figure 4.4 will result in the Q outputs going high when the inputs are left open. If the opposite is desired, the resistor to V_{CC} can be tied to the inverting input and V_{BB} to the non-inverting input.

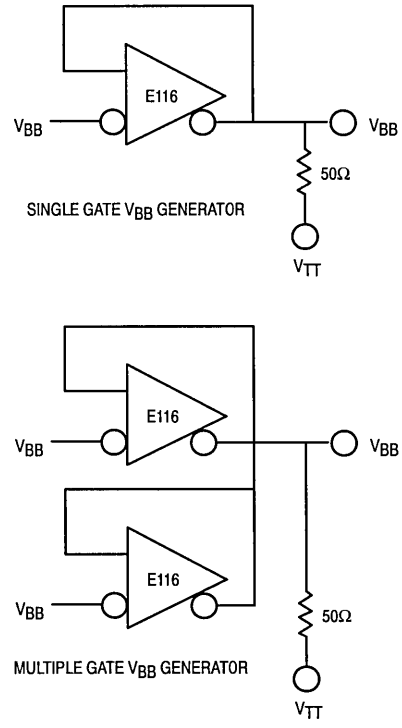


Figure 4.5. High Current V_{BB} Generator

SECTION 5
Package and Thermal Information

Package Choice

ECLinPS is offered in the 28-lead plastic leaded chip carrier (PLCC) package, a leaded surface mount IC package. The lead form is of the "J-lead" type. For detailed dimensions of the 28-lead PLCC refer to the package description drawings at the end of this section.

The PLCC was selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve these qualities still further, the cost of these is prohibitive for many applications.

The PLCC features considerably faster propagation delay and reduced parasitics compared to a DIP package of similar pin-count; two properties that make it eminently suitable for very high performance logic.

The 28-lead PLCC for the ECLinPS family is available in tape and reel form to further facilitate automatic pick and place. The characteristics of the 28-lead PLCC reel are described in Figure 5.1 below.

General Information

REEL SIZE: 13" (330mm)
TAPE WIDTH: 24mm
UNITS/REEL: 500

Mechanical Polarization

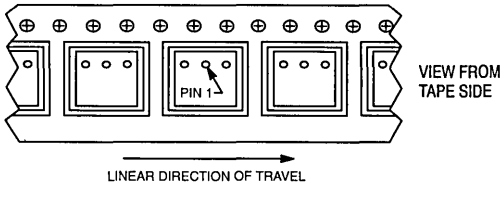


Figure 5.1. 28-Lead PLCC Tape & Reel Information

Orders must be full reels or multiples of full reels as no partial reels will be shipped. An R2 suffix has been established to add to the end of the part number to signify the desire for tape and reel product. Therefore, to order the MC10E111FN in tape and reel the part number would become MC10E111FNR2.

Reliability of Plastic Packages

Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. As the temperature of the silicon (junction temperature) increases, an intermetallic compound forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation, relating junction temperature to bond failure, was established. The application of this equation yields the table of Figure 5.2. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds)

ECLinPS devices are designed with chip power levels that permit acceptable reliability levels, in most systems, under the conventional 500 lfpm (2.5m/s) airflow.

Thermal Management

As in any system, proper thermal management is essential to establish the appropriate trade-off between performance, density, reliability and cost. In particular, the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of surface mount devices (SMD) is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that SMD packages generally require less board space than their through hole counterparts so that designs incorporating SMD technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

$$T = 6.376 \times 10^{-9} e \left[\frac{11554.267}{273.15 + T_J} \right]$$

Where:
T = Time to 0.1% bond failure

Junction Temp. (°C)	Time (Hrs.)	Time (yrs.)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20 4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Figure 5.2 Tj vs Time to 0.1% Bond Failure

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach, can positively impact the thermal resistance and, thus, the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however, PCB substrate material, layout density, size of the air-gap between the board and the package, amount of exposed copper interconnect, use of thermally-conductive epoxies and number of boards in a box, can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. The user should also account for the different power dissipations of the different devices in his system and space them on the PCB accordingly. In this way, the heat load is spread across a larger area and "hot spots" do not appear in the layout. Copper interconnect traces act as heat radiators, therefore, significant thermal dissipation can be achieved through the addition of interconnect traces on the top layer of the board. Finally, the use of thermally conductive epoxies can accelerate the transfer of heat from the device to the PCB where it can more easily be passed to the ambient.

The advent of SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

The following equation can be used to estimate the junction temperature of a device in a given environment:

$$T_J = T_A + P_D \Theta_{JA}$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
Θ_{JA} = Avg Pkg Thermal Resistance (Junction Ambient)

The power dissipation factor is made up of two elements: the internal gate power and the power associated with the output terminations. Essentially, the two contributors can be calculated separately, then added to give the total power dissipation for a device.

To calculate the power of the internal gates the user simply multiplies the I_{EE} of the device times V_{EE}. Since I_{EE} in ECL is a constant parameter, frequency need not be factored into the calculations. A worst case or typical number for chip power can be calculated by using either worst case or typical data book values for the I_{EE} and V_{EE} of a device.

Next, the power of the outputs needs to calculated so that the total power dissipation for a device can be determined. The output power is dependent on the termination resistance and the termination scheme used to pulldown the outputs. The most typical termination scheme for ECLinNPS designs is a parallel termination into – 2.0V. For this scheme, the following equation describes the power for a single output of the device:

$$P_{DOUT} = I_{OUT} * V_{OUT} = (V_{OUT} - (-2)) R_T * V_{OUT}$$

where:

V_{OUT} = V_{OH} or V_{OL}
R_T = Termination Resistance

The power dissipated in the output of a device is dependent on the duty cycle of that output. For an output terminated to V_{TT} the worst case situation would be if the output was in the high state all of the time, for an output terminated to V_{EE} the low state will represent worst case. For single ended output devices, typically the power is calculated with the outputs in the worst case and for a 50% duty cycle. For differential outputs, the power for a differential pair is constant since they are always in complimentary states, therefore, for a given output, the power will simply be the average of the high and low state output powers. Figure 5.3 shows the various output power levels for the different output types and conditions. In addition, the table includes power numbers for various other termination resistances and alternative termination schemes. These numbers can be derived by determining the I_{OUT} and V_{OUT} for the different alternatives and applying the equation above.

Termination Resistance	Output Power (mW)					
	Differential Output		Single-ended Output (50%) Duty Cycle)		Single-ended Output (Worst Case)	
	10E	100E	10E	100E	10E	100E
50 to – 2.0V	14.3	15.0	14.3	15.0	19.8	20 0
68 to – 2.0V	10.5	11.1	10.5	11.1	14.6	14.7
100 to – 2.0V	7.1	7.5	7.1	7.5	9 9	10 0
510 to – 5.2V	9.7	9.8	9.7	9.8	11.8	11.7
330 to – 5.2V	15.0	15.1	15.0	15.1	18 3	18 0
180 to – 5.2V	27.5	27.8	27.5	27.8	33.5	33.1
510 to – 4.5V	—	7.8	—	7.8	—	9.3
330 to – 4.5V	—	12.3	—	12 3	—	14.4
180 to – 4.5V	—	22.6	—	22.6	—	26 4

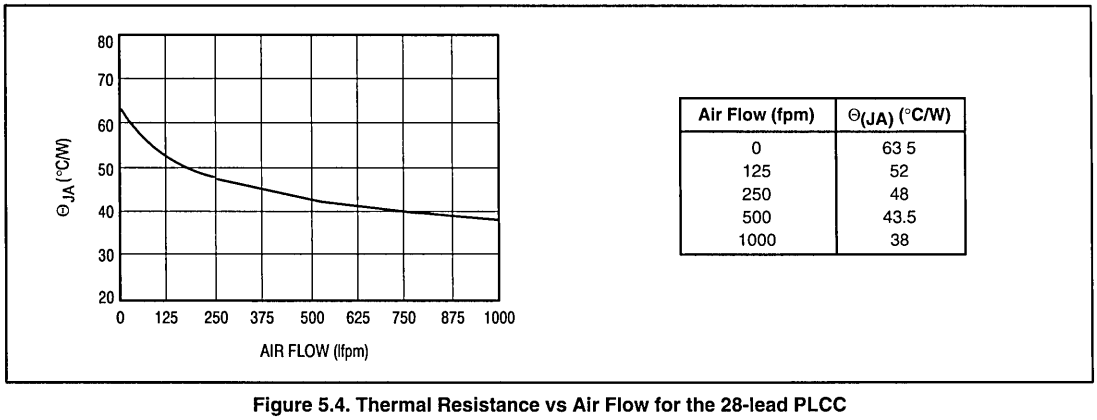
Figure 5.3 Output Power for Various Termination Schemes

Now that the power dissipation of a device can be calculated, one needs to determine which level of the parameter (i.e. typical, max, etc..) to use to estimate the long term reliability of the system. Since this number is statistical in nature, simply applying the worst case numbers will be overly pessimistic as these parameters vary statistically themselves. It is not very likely, for instance, that every device type will be operating at the maximum specified I_{EE} level. Assuming all worst case conditions can have a significant impact on the resulting junction, temperature estimates leading to erroneous conclusions about the reliability of the design.

Another important parameter for calculating the junction temperature of a device is the junction-ambient thermal resistance, Θ_{JA}, of the package. Θ_{JA} is expressed in °C per watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external package ambient temperature. Standard lab measurements of this parameter for the 28-lead PLCC yields the graph of Figure 5.4.

An alternative calculation scheme for T_J substitutes the case temperature (T_C) and the junction-to-case (Θ_{JC}) thermal resistance for their ambient counterparts in the T_J equation previously mentioned. The Θ_{JC} for the 28-lead PLCC is 32°C/W. This parameter is measured by submerging the device in a liquid bath and measuring the temperature of the bath, therefore, it represents an average case temperature.

4



Air Flow (fpm)	$\Theta_{(JA)}$ (°C/W)
0	63 5
125	52
250	48
500	43.5
1000	38

Figure 5.4. Thermal Resistance vs Air Flow for the 28-lead PLCC

The difficulty in using this method arises in the determination of the case temperature in an actual system. The case temperature is a function of the location at which the temperature is measured on the package. Therefore, to use the Θ_{JC} mentioned above, the case temperature would have to be measured at several different points and averaged to represent the T_C of the device. This, in practice, could prove difficult and relatively inaccurate.

Junction Temperature Calculation Example

As an example, the power dissipation for a 10E151, 6-bit register function, will be calculated for 500 lfpm airflow; both a worst case number and a typical number will be calculated. From the data sheet the typical and maximum I_{EE}'s for the device are 65mA and 85mA respectively. There are six differential output pairs.

Chip Power =

65mA * 5.2V=338mW typical

85mA * 5.46V = 464mW worst case

Output Power =

((–1.75 – (– 2))/50*1.75 + (– 0.9 (– 2))/50*0.9))/2 = 14.3mW

Total Power Pd =

338mW + 14.3*12 = 510mW typical

464mW + 14.3*12 = 635mW worst case

Junction Temperature =

T_A + 43.5°C/W* 0.510W = T_A + 22°C typical

T_A + 43.5°C/W* 0.635W = T_A + 28°C worst case

Note that in this case, the worst case junction temperatures are not significantly larger than the typical case This is due mainly to the fact that the device has differential outputs. A higher I_{EE}, single ended device would show a much larger discrepancy between the worst case and typical values.

Limitations to Calculation Technique

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the Θ_{JA} of the 28-lead PLCC package. Since this parameter is a function of not only the package, but also the test fixture, the results may not be applicable for every environmental condition. The 28-lead PLCC test fixture used was a 2.24″ × 2.24″ × 0.062″, FR4 type, glass epoxy board with 1 oz. copper used for interconnects. The copper represented about 50% coverage of the test fixture.

If the user's actual application does not come close to approximating this situation it may be necessary to use a different method for determining the junction temperature of a device. An empirical equation relating junction temperature to the actual case temperature and lead temperature of a device has been established. This equation has the advantage of being universal for all environmental conditions, however, the disadvantage of having to make actual thermocouple temperature measurements may limit its use.

The equation describing the junction temperature is as follows:

$$T_J = 24P_D + 0.313T_C + 0.687T_L \text{ °C/W } (\pm 2\text{°C/W})$$

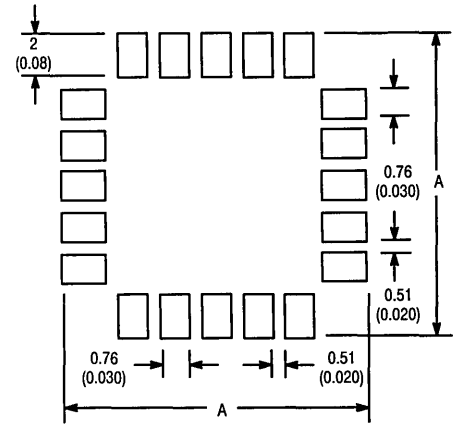
where:

P_D = Power Dissipation of the Device (W)
T_C = Case Temperature (°C)
T_L = Lead Temperature (°C)

T_C is measured at the top-center surface of the package, taking care that the thermocouple makes good contact with the case without transporting a significant amount of heat from the measurement point. The lead temperature is used to compensate for the differences in the ratio of heat transfer through the leads and the top surface of the package. This difference impacts the actual T_C of the package. As mentioned earlier, this method of determining the junction temperature is effective for almost all environmental conditions except those that incorporate an external heatsink. Of all the techniques mentioned in this document, the application of this equation will lead to the most accurate assessment of the junction temperature of a device.

Heatsinks

A plastic fin type heatsink recently developed by EG&G Engineering for a 40-lead PLCC was modified to fit the 28-lead



Unit: mm (inch)
Min. Value

Dimension A	Inches	mm
PLCC-20	0.430	10.9
PLCC-28	0.530	13.5
PLCC-44	0.630	16

Figure 5.5 - PLCC PCO Solder Pad Dimensions

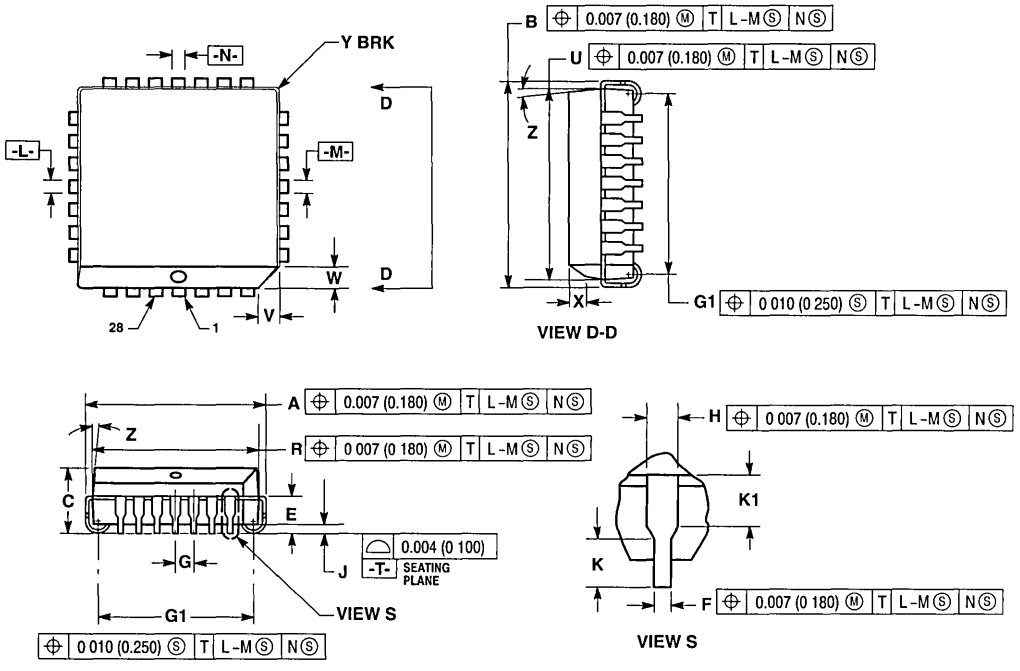
PLCC and evaluated. The addition of the heatsink showed a decrease of 20°C/W in the thermal resistance of the 28-lead PLCC in a natural convection air flow environment. The test device was suspended in air to simulate a dense board application where minimal heat will transfer from the device to the PCB substrate.

For more detailed information on availability and performance of heatsinks the user is encouraged to contact the numerous heatsink vendors.

Package Dimensions

Figure 5.5 on the previous page provides recommended printed circuit board solder pad dimensions for several PLCC packages. With this information and the 28-lead PLCC dimensions provided in Figure 5.6, the system designer should have all of the information necessary to successfully mount 28-lead PLCC packages on a surface mount PCB.

Package Outlines



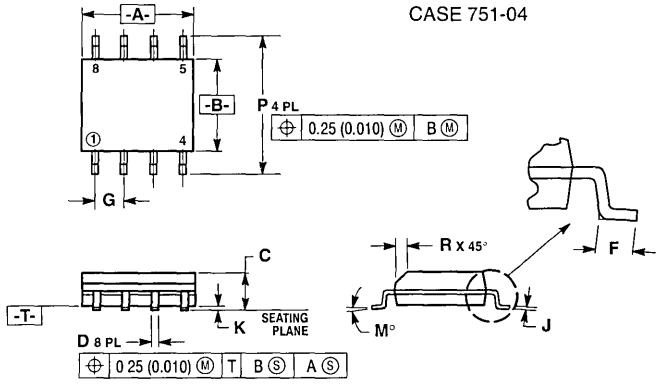
FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

NOTES
1 DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE
2 DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE
3 DIM R AND U DO NOT INCLUDE MOLD FLASH ALLOWABLE MOLD FLASH IS 0 010 (0 250) PER SIDE
4 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5 CONTROLLING DIMENSION INCH
6 THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0 012 (0 300) DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY
7 DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0 037 (0 940) THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0 025 (0 635)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0 485	0 495	12 32	12 57
B	0 485	0 495	12 32	12 57
C	0 165	0 180	4 20	4 57
E	0 090	0 110	2 29	2 79
F	0 013	0 019	0 33	0 48
G	0 050 BSC		1 27 BSC	
H	0 026	0 032	0 66	0 81
J	0 020	—	0 51	—
K	0 025	—	0 64	—
R	0 450	0 456	11 43	11 58
U	0 450	0 456	11 43	11 58
V	0 042	0 048	1 07	1 21
W	0 042	0 048	1 07	1 21
X	0 042	0 056	1 07	1 42
Y	—	0 020	—	0 50
Z	2°	10°	2°	10°
G1	0 410	0 430	10 42	10 92
K1	0 040	—	1 02	—

Figure 5.6. 28-Lead PLCC Dimensions

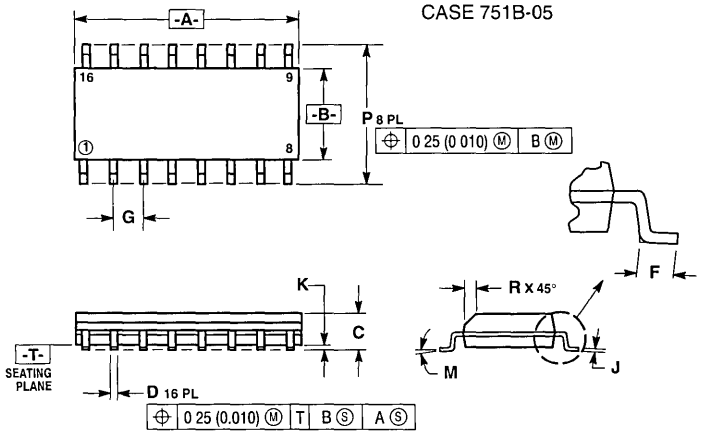
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-04



NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
2 CONTROLLING DIM MILLIMETER
3 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION
4 MAXIMUM MOLD PROTRUSION 0 15 (0 006) PER SIDE
5 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0 127 (0 005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4 80	5 00	0 189	0 196
B	3 80	4 00	0 150	0 157
C	1 35	1 75	0 054	0 068
D	0 35	0 49	0 014	0 019
F	0 40	1 25	0 016	0 049
G	1 27 BSC		0 050 BSC	
J	0 18	0 25	0 007	0 009
K	0 10	0 25	0 004	0 009
M	0°	7°	0°	7°
P	5 80	6 20	0 229	0 244
R	0 25	0 50	0 010	0 019

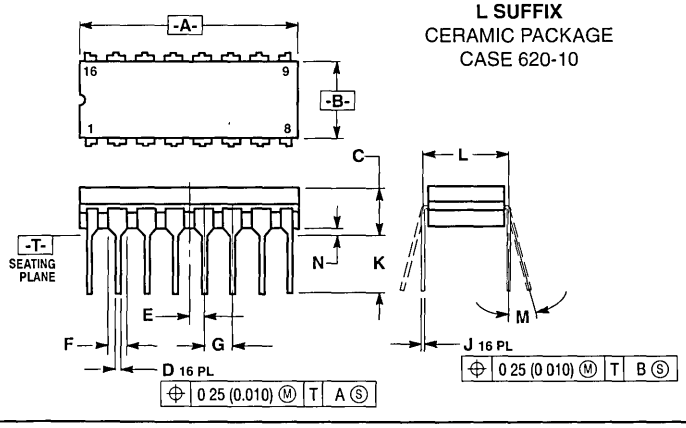
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05



NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
2 CONTROLLING DIMENSION MILLIMETER
3 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION
4 MAXIMUM MOLD PROTRUSION 0 15 (0 006) PER SIDE
5 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0 127 (0 005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9 80	10 00	0 386	0 393
B	3 80	4 00	0 150	0 157
C	1 35	1 75	0 054	0 068
D	0 35	0 49	0 014	0 019
F	0 40	1 25	0 016	0 049
G	1 27 BSC		0 050 BSC	
J	0 19	0 25	0 008	0 009
K	0 10	0 25	0 004	0 009
M	0°	7°	0°	7°
P	5 80	6 20	0 229	0 244
R	0 25	0 50	0 010	0 019

L SUFFIX
CERAMIC PACKAGE
CASE 620-10



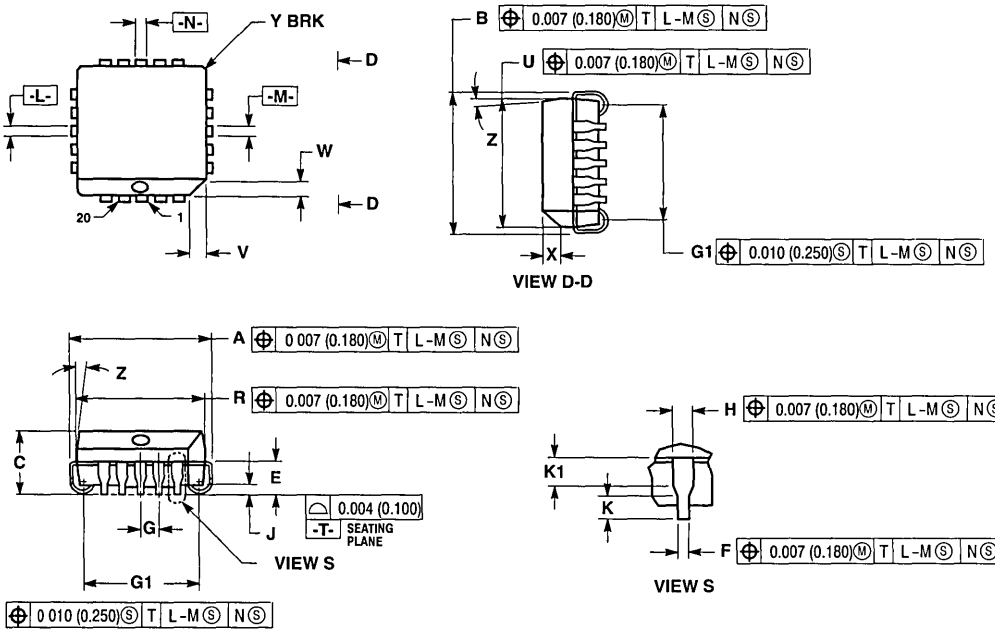
NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
2 CONTROLLING DIMENSION INCH
3 DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL
4 DIM F MAY NARROW TO 0 76 (0 030) WHERE THE LEAD ENTERS THE CERAMIC BODY

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0 750	0 785	19 05	19 93
B	0 240	0 295	6 10	7 49
C	—	0 200	—	5 08
D	0 015	0 020	0 39	0 50
E	0 050 BSC		1 27 BSC	
F	0 055	0 065	1 40	1 65
G	0 100 BSC		2 54 BSC	
J	0 008	0 015	0 21	0 38
K	0 125	0 170	3 18	4 31
L	0 300 BSC		7 62 BSC	
M	0°	15°	0°	15°
N	0 020	0 040	0 51	1 01

4

Package Outlines

FN SUFFIX
PLASTIC PACKAGE
CASE 775-02



NOTES
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE
3. DIM R AND U DO NOT INCLUDE MOLD FLASH ALLOWABLE MOLD FLASH IS 0 010 (0 250) PER SIDE
4. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
5. CONTROLLING DIMENSION INCH
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0 012 (0 300) DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0 037 (0 940) THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0 025 (0 635)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0 385	0 395	9 78	10 03
B	0 385	0 395	9 78	10 03
C	0 165	0 180	4 20	4 57
E	0 090	0 110	2 29	2 79
F	0 013	0 019	0 33	0 48
G	0 050 BSC		1 27 BSC	
H	0 026	0 032	0 66	0 81
J	0 020	—	0 51	—
K	0 025	—	0 64	—
R	0 350	0 356	8 89	9 04
U	0 350	0 356	8 89	9 04
V	0 042	0 048	1 07	1 21
W	0 042	0 048	1 07	1 21
X	0 042	0 056	1 07	1 42
Y	—	0 020	—	0 50
Z	2°	10°	2°	10°
G1	0 310	0 330	7 88	8 38
K1	0 040	—	1 02	—

SECTION 6
Quality & Reliability

Quality

The Motorola culture is a culture of quality. Throughout all phases of product development, from defining and designing to shipping the product, Motorola strives for total customer satisfaction through "Six Sigma" and "On Time Delivery" programs.

Defining Products

From the beginning, the goal of the ECLinPS family was to be "customer" defined. Extensive work was done up front to identify part types which were perfectly suited to the needs of our customers. This definition phase ensured a level of quality for the family in that the customer defines the product rather than the supplier dictating product types.

Designing Products

Superior quality products start with the design, and the design of a product starts with an IC process. Extensive work was done with the MOSAIC III process to ensure a solid platform for quality products. Process reliability studies were performed to uncover any weaknesses in the initial process so that enhancements could be made to strengthen it before it was released to production. In addition, comprehensive characterization and correlation work was completed on the process to ensure the utmost in modeling parameter accuracy.

The design of the products strictly adhered to the design rules set forth by the process designers. Conservative, manufacturable layout rules were followed to minimize the performance variability due to a marginally manufacturable product. In addition, the use of statistical modeling methods, such as factorial and response surface techniques, in the designing of the IC's leads to products with a reduced sensitivity to variations in the manufacturing process.

Manufacturing Process

Through SPC and continual engineering work, the manufacture of the MOSAIC III process is both monitored and enhanced on a continuous basis. Statistical data is gathered at both probe and final test through the device data collection to monitor the distribution of a parameter to its specification limits. In addition, final quality assurance gates are set up to guarantee the quality of outgoing product.

Product Characterization

Products are both DC and AC characterized for all data book environmental conditions prior to the release of the product to production. The distributions of the parameters are compared to their specification limits to ensure that Motorola "manufactures" quality products as opposed to "testing" quality products through distribution truncation. In addition, ongoing AC characterization is performed to enhance the distributions of the AC parameters of the device. In doing so, as the distributions warrant, further enhancements to the AC specifications can be achieved.

Reliability

To ensure the long term reliability of ECLinPS products, extensive accelerated life testing is performed prior to production release. This qualification work is performed by Logic Reliability Engineering, an organization specifically dedicated to monitoring and guaranteeing the quality and and reliability of logic products. The accelerated life test consists of the following:

Operating Life Test: 145°C Mil. Std. 883
Temperature Cycle: –65°C to 150°C Mil. Std. 883
Pressure, Temperature, Humidity (Hermeticity)

A minimum of two lots, 250 die per lot taken from three different waters in the lot constitute a qualification sample. Various intermediate readouts are taken to monitor the performance more closely. In addition, the devices are tested beyond the specification limits to determine where and how they will fail.

Another responsibility of the reliability group is that of failure analysis. This failure analysis service is supported for both internal purposes and for servicing the needs of our customers. Analysis entails everything from simple package examination to internal microprobing to SEM analysis of IC structures. The results of the analysis are returned to the customer and if the analysis suggests a potential problem with the device the information is also passed to the internal product groups.

RAP: Reliability Audit Program

The Reliability Audit Program (RAP) devised in March 1977 is the Motorola internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations and monthly reporting of results. These reports are available at all sales offices. Also available is the "Reliability and Quality Handbook" which contains data for all Motorola semiconductors (BR518/D).

Quality & Reliability

Rap is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in Figure 6.1. Frequency of testing is specified per internal document 12MRM15301A.

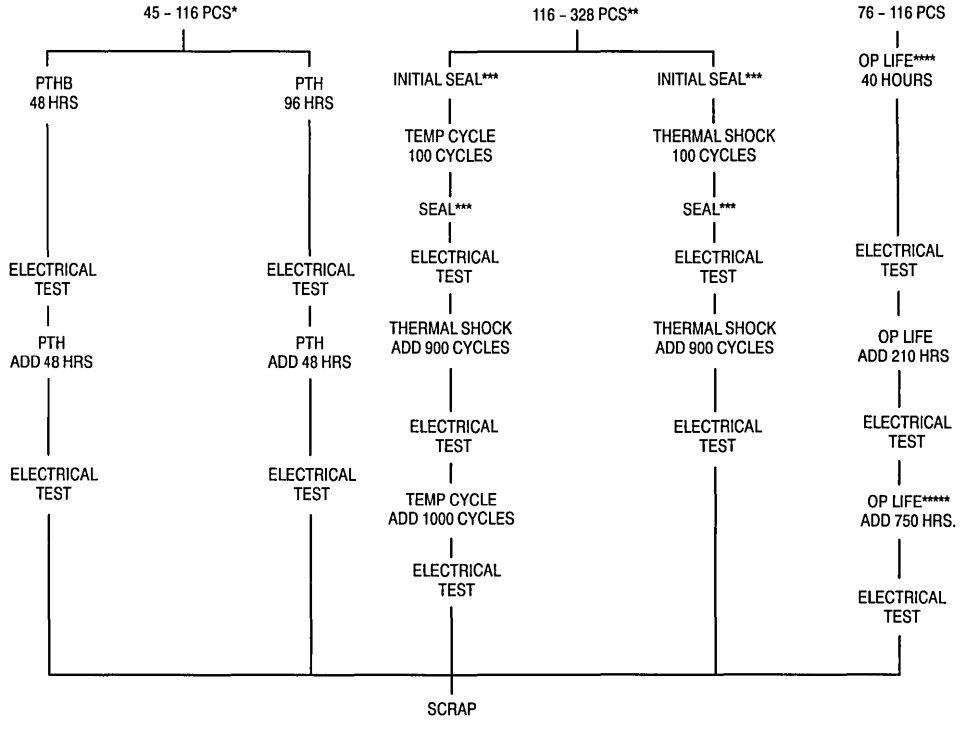


Figure 6.1. Reliability Audit Program Test Flow

* PTH will be run as a substitute if PTHB sockets are not available. Only required on plastics packages.

** Thermal Shock will be run if Temp Cycle is not available.

*** Seal (fine and gross) only required on hermetic packages.

**** All units for Op Life to be AC/DC tested before and after being stressed. All units failing AC after stress will be analyzed.

***** One sample per month

PTHB

15psig/121°C/100% RH at rated V_{CC} or V_{EE} – to be performed on plastic encapsulated devices only.

Temp Cycle

Mil. Std. 883, Method 1010, Condition C, – 65°C to 150°C

Op Life

Mil. Std. 883, Method 1005, Condition C (Power plus Reverse Bias), T_A = 145°C.

Notes:

1 All standard 25°C DC and functional parameters will be measured Go/NoGo at each readout

2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis

3 Sampling to include all package types routinely

4 Device types sampled will be by generic type within each digital IC product family (MECL, TTL, etc.) and will include all assembly locations (Korea, Phillipines, Malaysia, etc)

5. 16 hrs PTHB is equivalent to ≈ 800 hrs. of 85°C/85% RH THB for $V_{CC} \leq 15V$.

6 Only moisture related failures (like corrosion) are criteria for failure on PTHB test

7. Special device specifications (48A's) for digital products will reference 12MRM15301A as a source of generic data for any customer requiring monthly audit reports

AN1404
Application Note

ECLinPS™ Circuit Performance at Non-Standard VIH Levels

Prepared by
Todd Pearson
ECL Applications Engineering

This application note explains the consequences of driving an ECLinPS device with an input voltage HIGH level (V_{IH}) which does not meet the maximum voltage specified in the ECLinPS Databook.

4

AN1404

ECLinPS Circuit Performance at Non-Standard VIH Levels

Introduction

When interfacing ECLinPS devices to various other technologies times arise where the the input voltages do not meet the specification limits outlined in the ECLinPS data book. The purpose of this document is to explain the consequences of driving an ECLinPS device with an input voltage HIGH level (V_{IH}) which does not meet the maximum voltage specified in the ECLinPS Databook.

The results outlined in this document should not be viewed as guarantees by Motorola but rather as representative information from which the reader can base design decisions. It is up to the reader to assess the risks of implementing the non-standard interface and deciding if that level of risk is acceptable for the system design. Motorola's guarantee on V_{IH} will continue to be the specification standards established for the 10H™ and 100K ECL technologies.

Overview

The upper end of the V_{IH} spec of an ECLinPS, or any other ECL, input is limited by saturation affects of the input transistor. Figure 1 below illustrates a typical ECL input (excluding pulldown resistors and ESD structures); the structure is a basic differential amplifier configuration. With a logic HIGH level asserted at the input the collector of that transistor will be pulled down below the V_{CC} rail by the gate current passing through the collector load resistor. The voltage at the collector of the input transistor (V_C) will be dependent on the gate current and the size of the collector load resistor associated with the input gate.

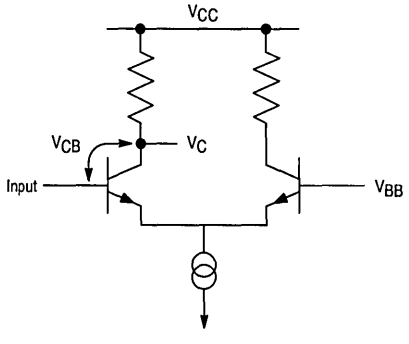


Figure 1. Typical ECLinPS Input Structure

As the input V_{IH} increases towards V_{CC} the collector base junction of the input transistor becomes forward biased; as this forward bias condition increases the transistor will move into the saturation region. The value of V_{CB} at which the transistor begins to saturate is process dependent and will vary from logic family to logic family. Fortunately the MOSAIC III process used to implement the ECLinPS family incorporates a deep n+ collector doping. This deep collector helps to mitigate the effects of saturation of transistors by requiring a larger collector-base forward bias to enter the saturation region.

V_{IH}max and the ECLinPS Family

As previously mentioned the MOSAIC III™ process allows for ECLinPS devices to operate at V_{IH}max levels somewhat higher than those specified in the databook, however the exact value of V_{IH} for which saturation problems will occur varies from device to device and even among different inputs for a given device. This variation is a result of the different input configurations used on the various inputs of ECLinPS devices.

The easiest way to define an acceptable V_{IH}max for each device in the family is to define at what point the input transistor will saturate and specify for each input what the worst case input transistor collector voltage will be. With this information designers will be able to determine on a part by part, input by input basis what input voltage levels will be acceptable for their application.

Simulation Results

The input saturation phenomenon was characterized through SPICE simulations and the results will be reported in the following text. For simplicity of simulation a buffer similar to the E122 was used. Since the outputs of this buffer drive off chip, the V_{IH}max performance of this structure will be worse than the typical input structure. Both a 100K and a 10H style buffer were analyzed to note any discrepancies between the two standards. As expected the simulation results showed no difference in the saturation susceptibility of a 100K versus a 10H style buffer. Therefore the simulation results of only the 100K style buffer will be presented to minimize redundancy of information.

The following text will refer to Figures 4–8 in the appendix of this document. Figures 4–8 are graphical plots of the input and output waveforms of an E122 style buffer (structure similar to that of Figure 1) for various V_{IH} levels. V(in) represents the input voltage while V(q) and V(qb) represent the output voltages. The V(vbb) line was included for measurement purposes only and will be ignored.

Figure 4 represents the "standard" operation of the device as a standard V_{IH} input was used. Note that in this condition the propagation delays measure in the 215–225ps range and the I_{INH} was 42.5µA. The I_{INH} of this device is simply a measure of the base current of the input transistor when that transistor is conducting current. We will be monitoring both of these conditions as well as any degradation in the output waveforms as a sign of the input transistor becoming saturated. As can be seen in Figures 5 and 6 none of the parameters change for V_{IH} levels of up to –0.4V. With a collector voltage, V_C, of –1.0V these V_{IH}'s correspond to a collector base forward bias of 600mV. As the V_{IH} of the input moves closer to V_{CC}, Figures 7 and 8, three phenomena start to occur: the I_{INH} increases, the delays increase and significant changes occur to the output low level of the QB pin.

In Figure 7 the I_{INH} of the input transistor has more than doubled from the "standard" level. This increase in base current leads to an increase in the V_{OL} level as the collector current must reduce to maintain the constant emitter current. As the collector current reduces, the IR drop across the collector load resistor reduces, thus raising the V_{OL} level on the QB output. Although the V_{OL} level has shifted the overall propagation delay has remained essentially unchanged.

Finally, when the input is switched all the way up to V_{CC} the V_{OL} level no longer remains in spec as the input base current has jumped to almost 1ma and there has been significant degradation in the high-low propagation delay. It is apparent that for this condition an E122 style buffer will not perform adequately for most systems.

From this information it can be concluded that for a collector-base forward bias of ≤600mV there will be no adverse conditions on the performance of the device. The performance starts to degrade with further forward bias until at a forward bias voltage of ≈1.0V the device will fail both its DC and AC specifications.

ECLinPS Input Structures

There are four basic input structures which will affect the V_{IH}max performance of ECLinPS devices. The four structures are as follows: an internal buffer, an external buffer, an emitter follower input buffer and a series gated emitter follower input.

The internal buffers are input structures whose outputs drive other gates internal to the device, the voltage swings of the input transistor collectors (V_C) on these devices will be ≈800mV. An external buffer is one in which the outputs are fed external to the chip. Because of the relatively large base drive of the output emitter follower for these structures the V_C voltage will typically be a couple hundred milivolts lower than for the internal buffer. Note that because of the larger output swings of a 10E device, a 10E style external buffer will require a V_{IH}max input level more near the specified value. Both of these structures are similar to that pictured in Figure 1.

The third and fourth structures are somewhat different in design than the first two. Figure 2 illustrates an emitter follower input structure. For the basic emitter follower input the input voltages are dropped by an additional V_{BE} (≈800mV) before they are fed into the differential amplifier input gate. The switching reference is also shifted down by one diode drop to remain centered in the input swing. Obviously this input structure will represent the "best case" in the area of extended V_{IH}max performance. In fact this type of input structure will allow for input voltages even several hundred millivolts above the V_{CC} rail. This characteristic makes these type devices ideal for interfacing with differential oscillators whose outputs lack any DC offset. In the emitter follower structure the limiting factor will be the saturation of the emitter follower device whose collector is at V_{CC}. From the previous simulation results this would suggest a maximum V_{IH} of +0.6V.

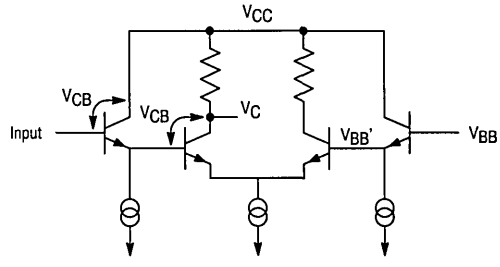


Figure 2. Emitter Follower Input Structure

The series gate emitter follower input will represent the absolute worst case situation for a 100E device. Figure 3 represents a series gate emitter follower input for a 10E and a 100E device. From this figure it is apparent that the lower switching level (B input level) is going to be much more susceptible to V_{IH}max for the 100E device than the 10E device. The two diode drops used for the 10E device is not possible for a 100E device due to the smaller V_{EE} voltage of a 100E device.

To summarize the external gate will represent the worst case V_{IH}max situation for a 10E device while the series gate emitter follower case will represent worst case for a 100E device. In either situation the standard emitter follower will allow the most leeway for non-standard V_{IH}max performance.

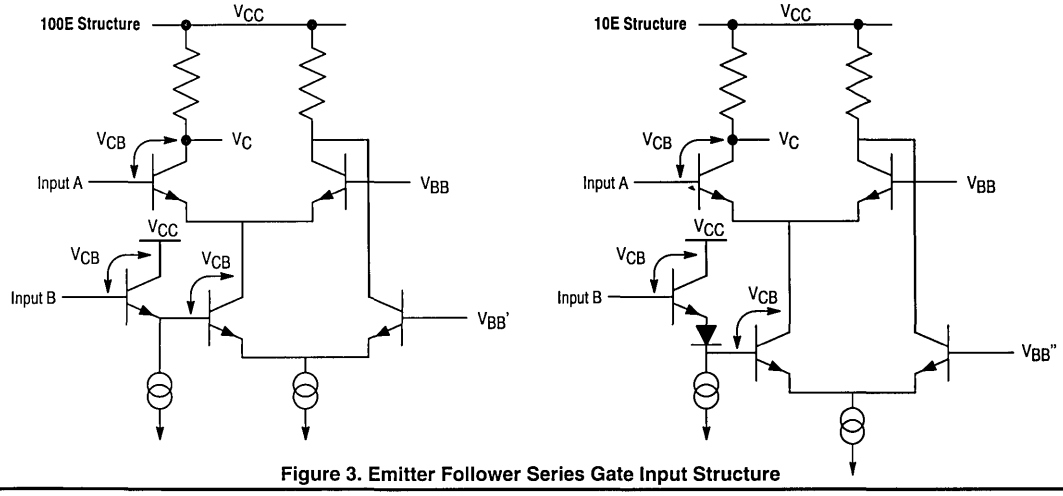


Figure 3. Emitter Follower Series Gate Input Structure

Other Considerations

When driving ECLinPS devices with other than standard input levels there is another phenomena that should be considered; namely effects of non-centered switching references on the AC performance of a device. For non-standard input voltages the midpoint of the voltage swing may not correspond to the internal V_{BB} switching reference. If this is the case the resulting AC variation should be included in the evaluation of a design.

An input voltage swing not centered about the switching reference will exhibit a delay skew between the two input edge transitions. The size of this skew will be dependent on both the voltage offset of the reference voltage and the midpoint of the input swing and the slew rate of the input as it passes through the threshold region. As an example for the case in which the V_{IH} = –0.5V and the V_{IL} remains at –1.7V the midpoint of the swing will be at –1.1V versus a –1.32V V_{BB} reference. With a typical slew rate of 1ps/mV for ECLinPS type edge rates the rising input edge delay will be 220ps longer than normal and the falling edge delay will be 220ps faster. This results in a 440ps skew between the two input transitions that would not be seen for an ideal switching reference.

The only means of correcting this skew is to lower the V_{IL} level to recenter the swing or provide a different switching reference for the device. The latter can be accomplished by buffering the signal with a differential input device with one input tied to an externally generated switching reference. Raising the V_{IL} level is not recommended due to the obvious loss of low end noise margin accompanied by any such shift.

Conclusions

Simulations show that forward bias levels of ≤600mV on the input transistor will keep the input transistor in the active region and the performance of the device will not be compromised. This forward bias voltage can be increased with varying degrees of performance degradation to levels somewhat higher than 600mV. Initial effects will be an increase in the I_{INH} current and a decrease in the output V_{OL} level on the QB output of the input gate. As the forward bias increases further the propagation delays through the device will be adversely affected.

The following example will outline the use of the table in the appendix to analyze the potential performance of a design using non-standard V_{IH} levels. If a design called for the 10E112 and the 10E416 to be driven by a –0.2V input signal a designer would want to know if these two devices would perform to specifications under these conditions. From the table the worst case collector voltage V_C would be –1.05V and 0.0V respectively. Subtracting these values from –0.2V yields forward bias voltages of 850mV and –200mV respectively. From this information the designer would conclude that the 10E416 will function with no problems however the 10E112 could suffer performance degradation under these same conditions.

The device information contained in the appendix of this document will provide designers with all of the information necessary to evaluate the input transistor forward bias conditions for all of the ECLinPS devices for different input voltages. With these numbers and the information provided in this document designers will be able to make informed decisions about their designs to meet the performance desired at an acceptable level of risk.

Appendix

Device	Input	Input Structure	V_C (10E Typical) (V)	V_C (10E Worst Case) (V)	V_C (100E Typical) (V)	V_C (100E Worst Case) (V)
E016	All	INT	–0.80	–0.90	–0 80	–0 90
E101	All	EF	–0 15	–0 25	–0.10	–0.20
E104/107	Dna	EXT	–0 95	–1.05	–0.90	–1.00
	Dnb	SG	–0.50	–0 60	–1.20	–1.30
E111	All	INT	–0 80	–0.90	–0 80	–0.90
E112	Dn	EXT	–0.95	–1.05	–0 90	–1.00
	EN/	INT	–0.80	–0 90	–0.80	–0.90
E116	All	EXT	–0.95	–1.05	–0.90	–1.00
E122	All	EXT	–0 95	–1.05	–0 90	–1.00
E131	D	INT	–0.90	–1 00	–0.90	–1 00
	Other	SG	–0.50	–0 60	–1.20	–1 30
E141	All	INT	–0.80	–0.90	–0.80	–0 90
E142	All	INT	–0.80	–0.90	–0.80	–0.90
E143	All	INT	–0 80	–0 90	–0.80	–0.90
E150	Dn	EXT	–0 95	–1.05	–0.90	–1.00
	Other	INT	–0 80	–0.90	–0.80	–0.90
E151	All	INT	–0.80	–0.90	–0.80	–0.90
E154	All	INT	–0.80	–0 90	–0 80	–0 90
E155	All	INT	–0.80	–0 90	–0.80	–0.90
E156	All	INT	–0 80	–0 90	–0.80	–0.90
E157	Dn	EXT	–0 95	–1.05	–0.90	–1.00
	SEL	INT	–0 80	–0 90	–0 80	–0.90
E158	Dn	EXT	–0.95	–1 05	–0.90	–1.00
	SEL	INT	–0 80	–0.90	–0 80	–0 90
E160	R, CLK	SG	–0.50	–0 60	–1.20	–1.30
	Other	INT	–0 80	–0.90	–0 80	–0.90
E163	All	INT	–0.80	–0 90	–0.80	–0.90
E164	All	INT	–0.80	–0 90	–0.80	–0.90
E166	All	INT	–0 80	–0.90	–0.80	–0.90
E167	All	INT	–0.80	–0.90	–0 80	–0.90
E171	All	INT	–0 80	–0.90	–0.80	–0.90
E175	All	INT	–0.80	–0.90	–0.80	–0.90
E195	All	INT	–0 80	–0.90	–0.80	–0.90
E196	All	INT	–0.80	–0.90	–0.80	–0.90
E212	All	INT	–0 80	–0.90	–0.80	–0 90
E241	All	INT	–0 80	–0.90	–0.80	–0.90
E256	All	INT	–0.80	–0.90	–0.80	–0.90
E336	All	INT	–0.80	–0 90	–0 80	–0 90
E337	All	INT	–0.80	–0.90	–0.80	–0.90
E404	All	EF	0 00	0.00	0 00	0.00
E416	All	EF	0 00	0.00	0.00	0.00
E431	All	INT	–0.80	–0.90	–0.80	–0.90
E451	All	INT	–0 80	–0.90	–0.80	–0 90
E452	All	INT	–0 80	–0.90	–0 80	–0.90
E457	Dn	EF	0 00	0.00	0.00	0 00
	SEL	INT	–0 80	–0.90	–0 80	–0.90

INT = Internal Gate, EXT = External Gate, EF = Emitter Follower Input; SG = Series Gated Input

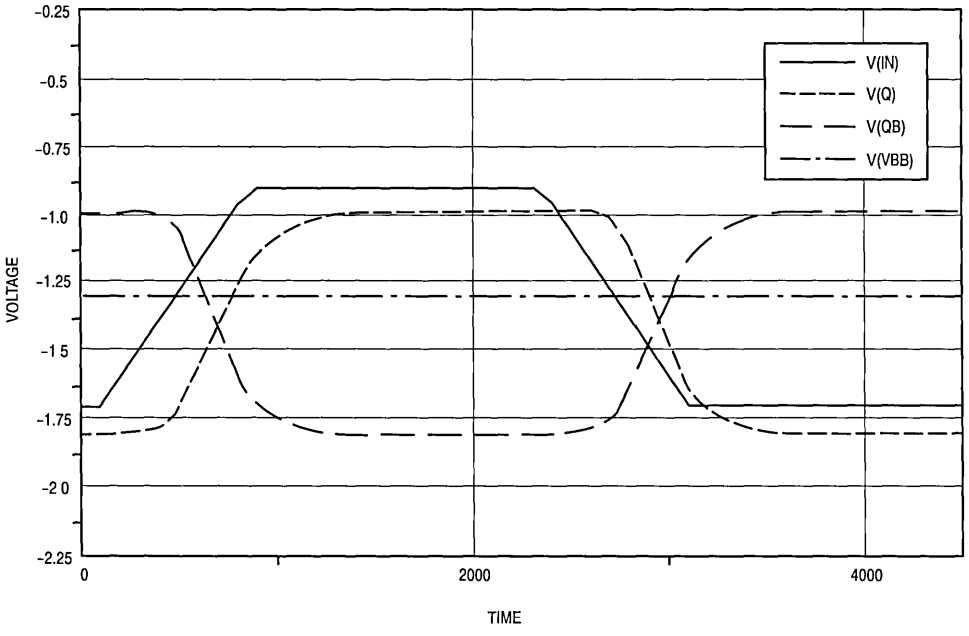


Figure 4. Input and Output Waveforms for V_{IH} = –0.9
(V_{OL} = –1.8; T_{PD}++ = 215ps; T_{PD}– – = 225ps; I_{INH} = 42.5µA)

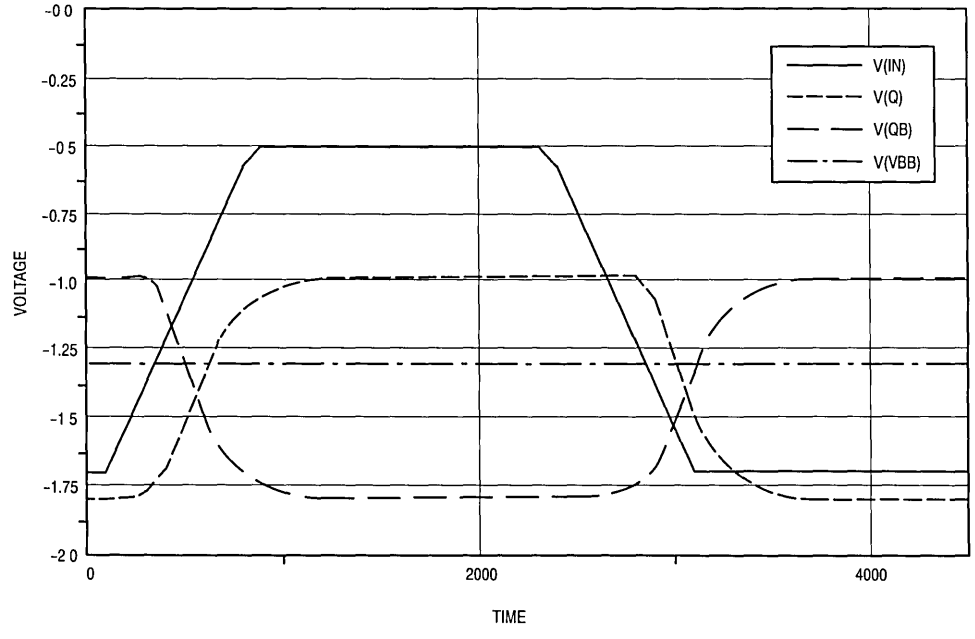


Figure 5. Input and Output Waveforms for V_{IH} = –0.5
(V_{OL} = –1.8; T_{PD}++ = 204ps; T_{PD}– – = 207ps; I_{INH} = 43.4µA)

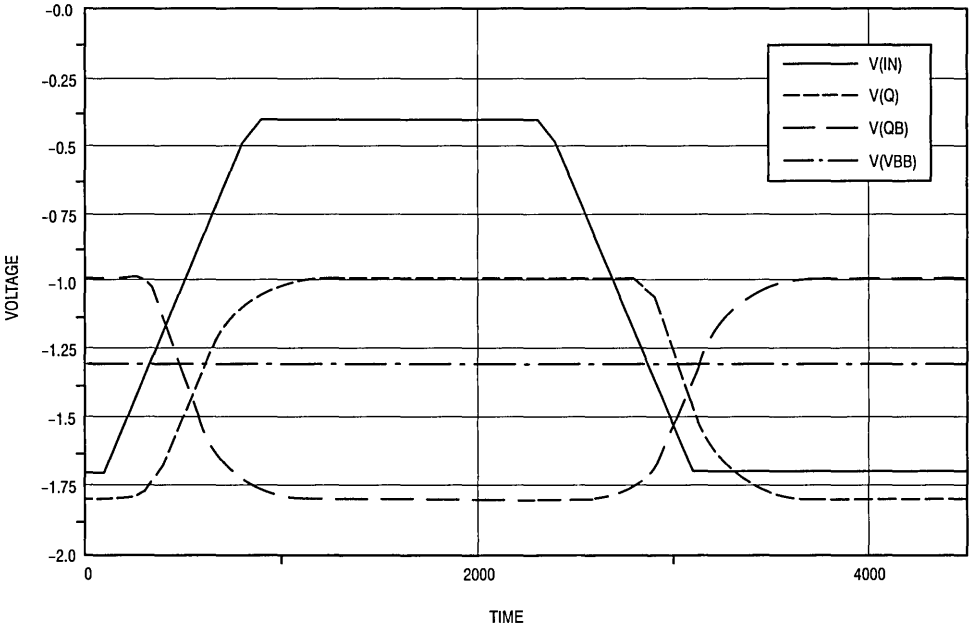


Figure 6. Input and Output Waveforms for V_{IH} = –0.4
(V_{OL} = –1.8; T_{PD}++ = 201ps; T_{PD}– – = 206ps; I_{INH} = 46.7µA)

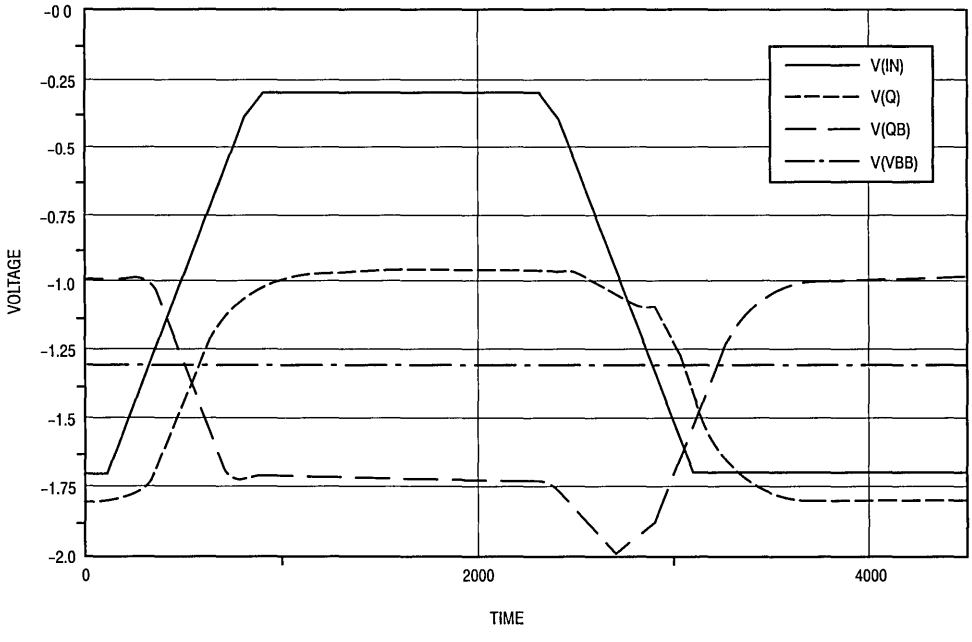


Figure 7. Input and Output Waveforms for V_{IH} = –0.3
(V_{OL} = –1.8; T_{PD}++ = 196ps; T_{PD}– – = 198ps; I_{INH} = 114.8µA)

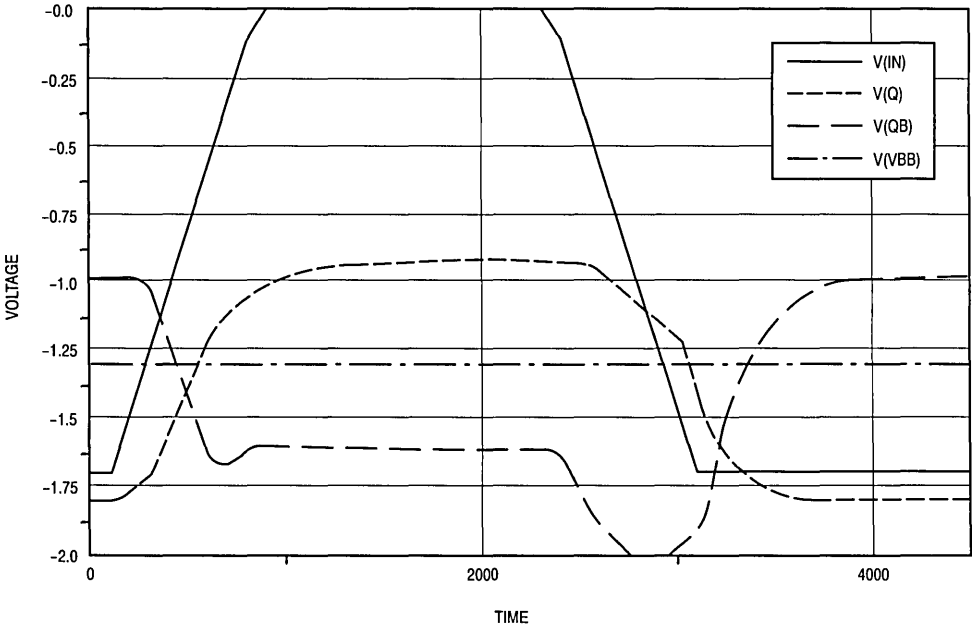


Figure 8. Input and Output Waveforms for V_{IH} = 0.0
(V_{OL} = –1.8; T_{PD}++ = 196ps; T_{PD}– – = 287ps; I_{INH} = 912µA)

AN1405
Application Note

ECL Clock Distribution Techniques

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This application note provides information on system design using ECL logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

4

ECL Clock Distribution Techniques

INTRODUCTION

The ever increasing performance requirements of today's systems has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions within a system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or more costly, faster logic. ECL logic technologies offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies.

SKEW DEFINITIONS

The skew introduced by logic devices can be divided into three parts: duty cycle skew, output-to-output skew and part-to-part skew. Depending on the specific application, each of the three components can be of equal or overriding importance.

Duty Cycle Skew

The duty cycle skew is a measure of the difference between the T_{PLH} and T_{PHL} propagation delays (Figure 1). Because differences in T_{PLH} and T_{PHL} will result in pulse width distortion the duty cycle skew is sometimes referred to as pulse skew. Duty cycle skew is important in applications where timing operations occur on both edges or when the duty cycle of the clock signal is critical. The later is a common requirement when driving the clock inputs of advanced microprocessors.

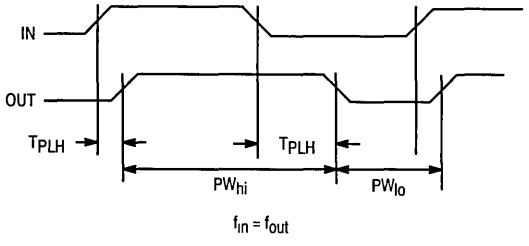

Figure 1. Duty Cycle Skew

Output-to-Output Skew

Output-to-output skew is defined as the difference between the propagation delays of all the outputs of a device. A key constraint on this measurement is the requirement that the output transitions are identical, therefore if the skew between all edges produced by a device is important the output-to-output skew would need to be added to the duty cycle skew to get the total system skew. Typically the output-to-output skew will be smaller than the duty cycle skew for TTL and CMOS devices. Because of the near zero duty cycle skew of a differential ECL device the output-to-output skew will generally be larger. The output-to-output skew is important in systems where either a single device can provide all of the necessary clocks or for the first level device of a nested clock distribution tree. In these two situations the only parameter of importance will be the relative position of each output with respect to the other outputs on that die. Since these outputs will all see the same environmental and process conditions the skew will be significantly less than the propagation delay windows specified in the standard device data sheet.

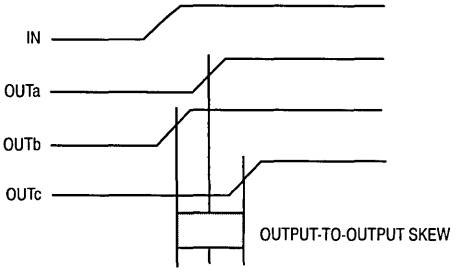

Figure 2. Output-to-Output Skew

Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize. Because the part-to-part skew is dependent on both process variations and variations in the environment the resultant specification is significantly larger than for the other two components of skew. Many times a vendor will provide subsets of part-to-part skew specifications based on non-varying environmental conditions. Care should be taken in reading data sheets to fully understand the conditions under which the specified limits are guaranteed. If the part-to-part skew is specified and is different than the specified propagation delay window for the device one can be assured there are constraints on the part-to-part skew specification.

Power supply and temperature variations are major contributors to variations in propagation delays of silicon devices. Constraints on these two parameters are commonly seen in part-to-part skew specifications. Although there are situations where the power supply variations could be ignored, it is difficult for this author to perceive of a realistic system whose devices are all under identical thermal conditions. Hot spots on boards or cabinets, interruption in air flow and variations in IC density of a board all lead to thermal gradients within a system. These thermal gradients will guarantee that devices in various parts of the system are under different junction temperature conditions. Although it is unlikely that a designer will need the entire commercial temperature range, a portion of this range will need to be considered. Therefore, a

part-to-part skew specified for a single temperature is of little use, especially if the temperature coefficient of the propagation delay is relatively large.

For designs whose clock distribution networks lie on a single board which utilizes power and ground planes an assumption of non-varying power supplies would be a valid assumption and a specification limit for a single power supply would be valuable. If, however, various pieces of the total distribution tree will be on different boards within a system there is a very real possibility that each device will see different power supply levels. In this case a specification limit for a fixed V_{CC} will be inadequate for the design of the system. Ideally the data sheets for clock distribution devices should include information which will allow designers to tailor the skew specifications of the device to their application environment.

SYSTEM ADVANTAGES OF ECL

Skew Reductions

ECL devices provide superior performance in all three areas of skew over their TTL or CMOS competitors. A skew reducing mechanism common to all skew parameters is the faster propagation delays of ECL devices. Since, to some extent, all skew represent a percentage of the typical delays faster delays will usually mean smaller skews. ECL devices, especially clock distribution devices, can be operated in either single-ended or differential modes. To minimize the skew of these devices the differential mode of operation should be used, however even in the single-ended mode the skew performance will be significantly better than for CMOS or TTL drivers.

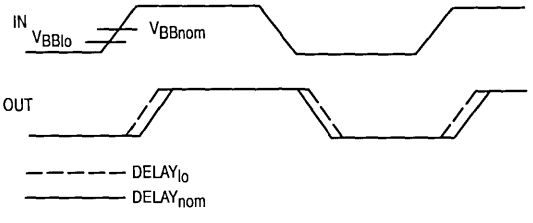

Figure 3. V_{BB} Induced Duty Cycle Skew

ECL output buffers inherently show very little difference between T_{PLH} and T_{PHL} delays. What differences one does see are due mainly to switching reference levels which are not ideally centered in the input swing (see Figure 3). For worst case switching reference levels the pulse skew of an ECL device will still be less than 300ps. If the ECL device is used differentially the variation in the switching reference will not impact the duty cycle skew as it is not used. In this case the pulse skew will be less than 50ps and can generally be ignored in all but the highest performance designs. The problem of generating clocks which are capable of meeting the duty cycle requirements of the most advanced microprocessors, would be a trivial task if differential ECL compatible clock inputs were used. TTL and CMOS clock drivers on the other hand have inherent differences between the T_{PLH} and T_{PHL} delays in addition to the problems with non-centered switching thresholds. In devices specifically designed to minimize this parameter it generally cannot be guaranteed to anything less than 1ns.

The major contributors to output-to-output skew is IC layout and package choice. Differences in internal paths and paths through the package generally can be minimized regardless of the silicon technology utilized at the die level, therefore ECL devices offer less of an advantage in this area than for other skew parameters. CMOS and TTL output performance is tied closely to the power supply levels and the stability of the power busses within the chip. Clock distribution trees by definition always switch simultaneously, thus creating significant disturbances on the internal power busses. To alleviate this problem multiple power and ground pins are utilized on TTL and CMOS clock distribution devices. However even with this strategy TTL and CMOS clock distribution devices are limited to 500ps – 700ps output-to-output skew guarantees. With differential ECL outputs very little if any noise is generated and coupled onto the internal power supplies. This coupled with the faster propagation delays of the output buffers produces output-to-output skews on ECL clock chips as low as 50ps.

Two aspects of ECL clock devices will lead to significantly smaller part-to-part skews than their CMOS and TTL competitors: faster propagation delays and delay insensitivity to environmental variations. Variations in propagation delays with process are typically going to be based on a percentage of the typical delay of the device. Assuming this percentage is going to be approximately equivalent between ECL, TTL and CMOS processes, the faster the device the smaller the delay variations. Because state-of-the-art ECL devices are at least 5 times faster than TTL and CMOS devices, the expected delay variation would be one fifth those of CMOS and TTL devices without even considering environmental dependencies.

The propagation delays of an ECL device are insensitive to variations in power supply while CMOS and TTL device propagation delays vary significantly with changes in this parameter. Across temperature the percentage variation for all technologies is comparable, however, again the faster propagation delays of ECL will reduce the magnitude of the variation. Figure 4 on the following page represents normalized propagation delay versus temperature and power supply for the three technologies.

Low Impedance Line Driving

The clock requirements of today's systems necessitate an almost exclusive use of controlled impedance interconnect. In the past this requirement was unique to the performance levels associated with ECL technologies, and in fact precluded its use in all but the highest performance systems. However the high performance CMOS and TTL clock distribution chips now require care in the design and layout of PC boards to optimize their performance, with this criteria established the migration from these technologies to ECL is simplified. In fact, the difficulties involved in designing with these "slower" technologies in a controlled impedance environment may even enhance the potential of using ECL devices as they are ideally suited to the task.

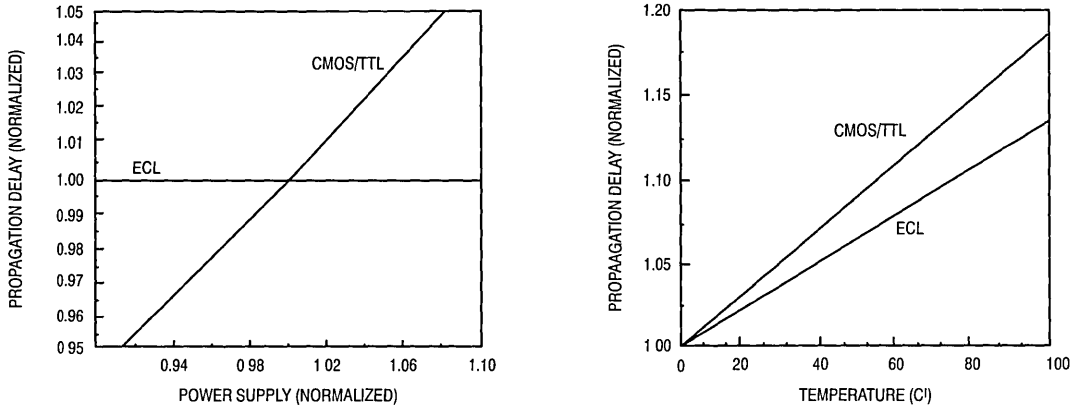

Figure 4. T_{PD} vs Environmental Condition Comparison

The low impedance outputs and high impedance inputs of an ECL device are ideal for driving 50Ω to 130Ω controlled impedance transmission lines. The specified driving impedance of ECL is 50Ω, however this value is used only for convenience sake due to the 50Ω impedance of most commonly used measurement equipment. Utilizing higher impedance lines will reduce the power dissipated by the termination resistors and thus should be considered in power sensitive designs. The major drawback of higher impedance lines (delays more dependent on capacitive loading) may not be an issue in the point to point interconnect scheme generally used in low skew clock distribution designs.

Differential Interconnect

The device skew minimization aspects of differential ECL have already been discussed however there are other system level advantages that should be mentioned. Whenever clock lines are distributed over long distances the losses in the line and the variations in power supply upset the ideal relationship between input voltages and switching thresholds. Because differential interconnect "carries" the switching threshold information from the source to the load the relationship between the two is less likely to be changed. In addition for long lines the smaller swings of an ECL device produce much lower levels of cross-talk between adjacent lines and minimizes EMI radiation from the PC board.

There is a cost associated with fully differential ECL, more pins for equivalent functions and more interconnect to be laid on a typically already crowded PC board. The first issue is really a non-issue for clock distribution devices. The output-to-output and duty cycle skew are very much dependent on quiet internal power supplies. Therefore the pins sacrificed for the complimentary outputs would otherwise have to be used as power supply pins, thus functionality is actually gained for an equivalent pin count as the inversion function is also available on a differential device. The presence of the inverted signal could be invaluable for a design which clocks both off the positive and negative edges. Figure 5 shows a method of obtaining very low skew (<50ps) 180° shifted two phase clocks.

It is true that differential interconnect requires more signals to be routed on the PC board. Fortunately with the wide data and address buses of today's designs the clock lines represent a small fraction of the total interconnect. The final choice as to whether or not to use differential interconnect lies in the level of skew performance necessary for the design. It should be noted that although single-ended ECL provides less attractive skew performance than differential ECL, it does provide significantly better performance than equivalent CMOS and TTL functions.

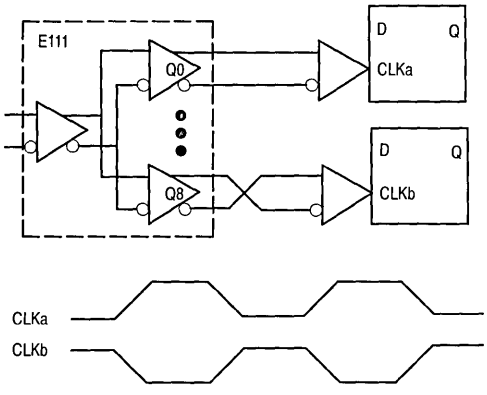

Figure 5. 180° Shifted Two Phase Clocks

USING ECL WITH POSITIVE SUPPLIES

It is hard to argue with the clock distribution advantages of ECL presented thus far, but it may be argued that except for all ECL designs it is too costly to include ECL devices in the distribution tree. This claim is based on the assumption that at least two extra power supplies are required; the negative V_{EE} supply and the negative V_{TT} termination voltage. Fortunately both these assumptions are false. PECL (Positive ECL) is an acronym which describes using ECL devices with a positive rather than negative power supply. It is important to understand that all ECL devices are also PECL devices By

using ECL devices as PECL devices on a +5 volt supply and incorporating termination techniques which do not require a separate termination voltage (series termination, thevenin equivalent) ECL can be incorporated in a CMOS or TTL design with no added cost.

The reason for the choice of negative power supplies as standard for ECL is due to the fact that all of the output levels and internal switching bias levels are referenced to the V_{CC} rail. It is generally easier to keep the grounds quieter and equal potential throughout a system than it is with a power supply. Because the DC parameters are referenced to the V_{CC} rail any disturbances or voltage drops seen on V_{CC} will translate 1:1 to the output and internal reference levels. For this reason when communicating with PECL between two boards it is recommended that only differential interconnect be used. By using differential interconnect V_{CC} variations within the specified range will not in any way affect the performance of the device.

Finally mentioning ECL to a CMOS designer invariably conjures up visions of space heaters as their perception of ECL is high power. Although it is true that the static power of ECL is higher than for CMOS the dynamic power differences between the technologies narrows as the frequency increases. As can be seen in Figure 6 at frequencies as low as 20MHz the per gate power of ECL is actually less than for CMOS. Since clock distribution devices are never static it does not make sense to compare the power dissipation of the two technologies in a static environment.

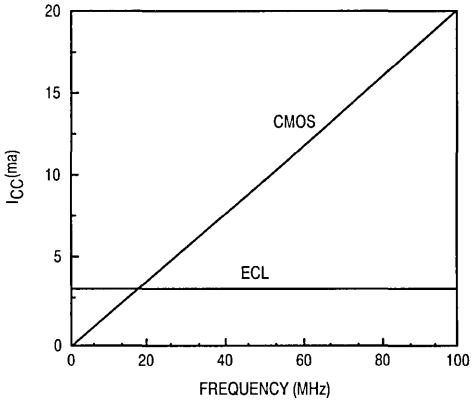

Figure 6. ICC/Gate vs Frequency Comparison

MIXED SIGNAL CLOCK DISTRIBUTION

ECL Clock Distribution Networks

Clock distribution in a ECL system is a relatively trivial matter. Figure 7 illustrates a two level clock distribution tree which produces nine differential ECL clocks on six different cards. The ECLinPS E211 device gives the flexibility of disabling each of the cards individually. In addition the synchronous registered enables will disable the device only when the clock is already in the LOW state, thus avoiding the problem of generating runt pulses when an asynchronous disable is used. The device also provides a muxed clock input for incorporating a high speed system clock and a lower speed test or scan clock within the same distribution tree. The ECLinPS E111 device is used to receive the signals from the backplane and distribute it on the card. The worst case skew between all 54 clocks in this situation would be 275ps assuming that all the loads and signal traces are equalized.

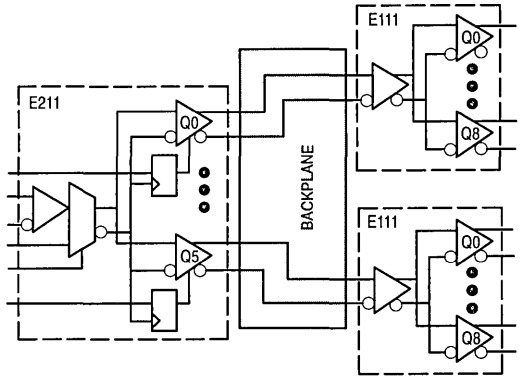

Figure 7. ECL Clock Distribution Tree

Mixed Technology Distribution Networks

Building clock networks in TTL and CMOS systems can be a little more complicated as there are more alternatives available. For simple one level distribution trees fanout devices like the MECL 10H645 1:9 TTL to TTL fanout tree can be used. However as the number of levels of fanout increases the addition of ECL devices in an other wise TTL or CMOS system becomes attractive. In Figure 8 on the next page an E111 device is combined with a MECL H641 device to produce 81 TTL level clocks. Analyzing the skew between the 81 clocks yields a worst case skew, allowing for the full temperature and V_{CC} range variation, of 1.25ns. Under ideal situations, no variation in temperature or V_{CC} supply, the skew would be only 750ps. When compared with distribution trees utilizing only TTL or CMOS technologies these numbers represent ≈50% improvement, more if the environmental conditions vary to any degree. For a 50MHz clock the total skew between the 81 TTL clocks is less than 6.5% of the clock period, thus providing the designer extra margin for layout induced skew to meet the overall skew budget of the design.

Many designers have already realized the benefits of ECL clock distribution trees and thus are implementing them in their designs. Furthermore where they have the capability, i.e. ASICs, they are building their VLSI circuits with ECL compatible clock inputs. Unfortunately other standard VLSI circuits such as microprocessors, microprocessor support chips and memory still cling to TTL or CMOS clock inputs. As a result many systems need both ECL and TTL clocks within the same system. Unlike the situation outlined in Figure 8 the ECL levels are not merely intermediate signals but rather are driving the clock inputs of the logic. As a result the ECL edges need to be matched with the TTL edges as pictured in Figure 9.

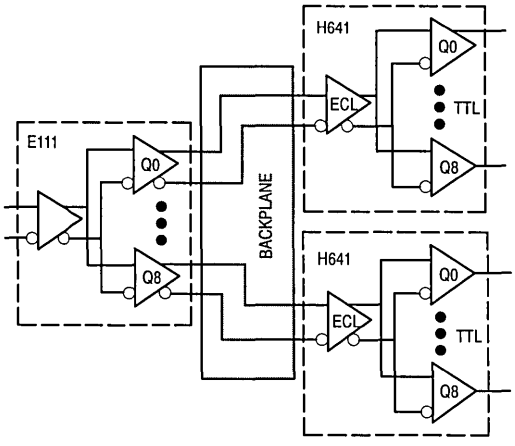

Figure 8. ECL to TTL Clock Distribution

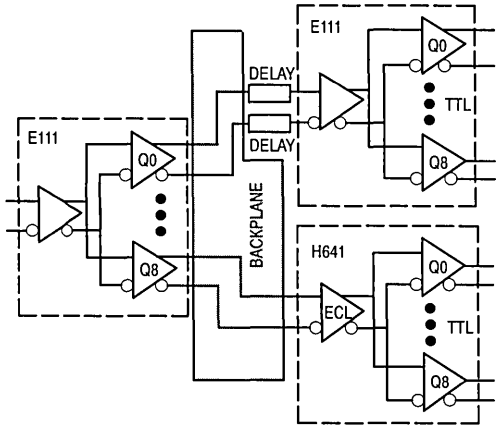

Figure 9. Mixed ECL and TTL Distribution

An ECL clock driver will be significantly faster than a TTL or CMOS equivalent function. Therefore to de-skew the ECL and TTL signals of Figure 9 a delay needs to be added to the input of the ECL device. Because a dynamic delay adjust would not lend itself to most production machines a static delay would be used. The value of the delay element would be a best guess estimate of the differences in the two propagation delays. It is highly unlikely that the temperature coefficients of the propagation delays of the ECL devices, TTL devices and delay devices would be equal. Although these problems will add skew to the system, the resultant total skew of the distribution network will be less than if no ECL chips were used.

PLL Based Clock Drivers

A potential solution for the problem outlined in Figure 9 is in the use of phase locked loop based clock distribution chips. Because these devices feedback an output and lock it to a reference clock input the delay differences between the various technology output buffers will be eliminated. One might believe that with all of the euphoria surrounding the performance of PLL based clock distribution devices that the need for any ECL in the distribution tree will be eliminated. However when analyzed further the opposite appears to be the case.

For a single board design with a one level distribution system there obviously is no need for ECL. When, however, a multiple board system is required where nested levels of devices are needed ECL once again becomes useful. One major aspect of part-to-part skew for PLL based clock chips often overlooked is the dependence on the skew of the various reference clocks being locked to. As can be seen in Figure 10 the specified part-to-part skew of the device would necessarily need to be added to the reference clock skew to get the overall skew of the clock tree. From the arguments presented earlier this skew will be minimized if the reference clock is distributed in ECL. It has not been shown as of yet where a PLL based ECL clock distribution chip can provide the skew performance of the simple fanout buffer. From a system standpoint the buffer type circuits are much easier to design with and thus given equivalent performance would represent the best alternative. The extra features provided by PLL based chips could all be realized if they were used in only the final stage of the distribution tree.

The MC88LV970 is a PLL based clock driver which features differential PECL reference clock inputs. When combined with the very low skew MC10E111 fanout buffer, very low skew clock trees can be realized for multiprocessor MPP designs. There will be a family of devices featuring various technology compatible inputs and outputs to allow for the building of precisely aligned clock trees based on either ECL, TTL, CMOS or differential GTL (or a mixture of all four) compatible levels.

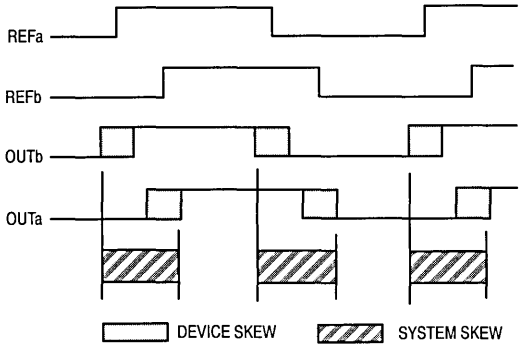

Figure 10. System Skew For PLL Clock Distribution

Conclusion

The best way to maximize the performance of any synchronous system is to spend the entire clock period performing value added operations. Obviously any portion of the clock period spent idle due to clock skew limits the potential performance of the system. Using ECL technology devices in clock distribution networks will minimize all aspects of skew and thus maximize the performance of a system. Unfortunately the VLSI world is not yet ECL clock based so that the benefits of a totally ECL based distribution tree cannot be realized for many systems. However there are methods of incorporating ECL into the intermediate levels of the tree to significantly reduce the overall skew. In addition the system designers can utilize their new found knowledge to incorporate ECL compatible clocks on those VLSI chips of which they have control while at the same time pressuring other VLSI vendors in doing the same so that future designs can enjoy fully the advantages of distributing clocks with ECL.

AN1406
Application Note

Designing With PECL (ECL at +5.0V)

Prepared by
Cleon Petty
Todd Pearson
ECL Applications Engineering

This application note provides detailed information on designing with Positive Emitter Coupled Logic (PECL) devices.

4

Designing With PECL (ECL at +5.0V)

The High Speed Solution for the CMOS/TTL Designer

Introduction

PECL, or Positive Emitter Coupled Logic, is nothing more than standard ECL devices run off of a positive power supply. Because ECL, and therefore PECL, has long been the "black magic" of the logic world many misconceptions and falsehoods have arisen concerning its use. However, many system problems which are difficult to address with TTL or CMOS technologies are ideally suited to the strengths of ECL. By breaking through the wall of misinformation concerning the use of ECL, the TTL and CMOS designers can arm themselves with a powerful weapon to attack the most difficult of high speed problems.

It has long been accepted that ECL devices provide the ultimate in logic speed; it is equally well known that the price for this speed is a greater need for attention to detail in the design and layout of the system PC boards. Because this requirement stems only from the speed performance aspect of ECL devices, as the speed performance of any logic technology increases these same requirements will hold. As can be seen in Table 1 the current state-of-the-art TTL and CMOS logic families have attained performance levels which require controlled impedance interconnect for even relatively short distances between source and load. As a result system designers who are using state-of-the-art TTL or CMOS logic are already forced to deal with the special requirements of high speed logic; thus it is a relatively small step to extend their thinking from a TTL and CMOS bias to include ECL devices where their special characteristics will simplify the design task.

Table 1. Relative Logic Speeds

Logic Family	Typical Output Rise/Fall	Maximum Open Line Length (L_{max})*
10KH	1.0ns	3"
ECLinPS	400ps	1"
FAST	2.0ns	6"
FACT	1.5ns	4"

* Approximate for stripline interconnect ($L_{max} = T_r/2T_{pd}$)

System Advantages of ECL

The most obvious area to incorporate ECL into an otherwise CMOS/TTL design would be for a subsystem which requires very fast data or signal processing. Although this is the most obvious it may also be the least common. Because of the need for translation between ECL and CMOS/TTL technologies the performance gain must be greater than the overhead required to translate back and forth between technologies. With typical delays of six to seven nanoseconds for translating between technologies, a significant portion of the logic would need to be realized using ECL for the overall system performance to improve. However, for very high speed subsystem requirements ECL may very well provide the best system solution.

Transmission Line Driving

Many of the inherent features of an ECL device make it ideal for driving long, controlled impedance lines. The low impedance of the open emitter outputs and high input impedance of any standard ECL device make it ideally suited for driving controlled impedance lines. Although designed to drive 50Ω lines an ECL device is equally adept at driving lines of impedances of up to 130Ω without significant changes in the AC characteristics of the device. Although some of the newer CMOS/TTL families have the ability to drive 50Ω lines many require special driver circuits to supply the necessary currents to drive low impedance transmission interconnect. In addition the large output swings and relatively fast output slew rates of today's high performance CMOS/TTL devices exacerbate the problems of crosstalk and EMI radiation. The problems of crosstalk and EMI radiation, along with common mode noise and signal amplitude losses, can be alleviated to a great degree with the use of differential interconnect. Because of their architectures, neither CMOS nor TTL devices are capable of differential communication. The differential amplifier input structure and complimentary outputs of ECL devices make them perfectly suited for differential applications. As a result, for systems requiring signal transmission between several boards, across relatively large distances, ECL devices provide the CMOS/TTL designer a means of ensuring reliable transmission while minimizing EMI radiation and crosstalk.

Figure 1 shows a typical application in which the long line driving, high bandwidth capabilities of ECL can be utilized. The majority of the data processing is done on wide bit width words with a clock cycle commensurate with the bandwidth capabilities of CMOS and TTL logic. The parallel data is then serialized into a high bandwidth data stream, a bandwidth which requires ECL technologies, for transmission across a long line to another box or machine. The signal is received differentially and converted back to relatively low speed parallel data where it can be processed further in CMOS/TTL logic. By taking advantage of the bandwidth and line driving capabilities of ECL the system minimizes the number of lines required for interconnecting the subsystems without sacrificing the overall performance. Furthermore by taking advantage of PECL this application can be realized with a single five volt power supply. The configuration of Figure 1 illustrates a situation where the mixing of logic technologies can produce a design which maximizes the overall performance while managing power dissipation and minimizing cost.

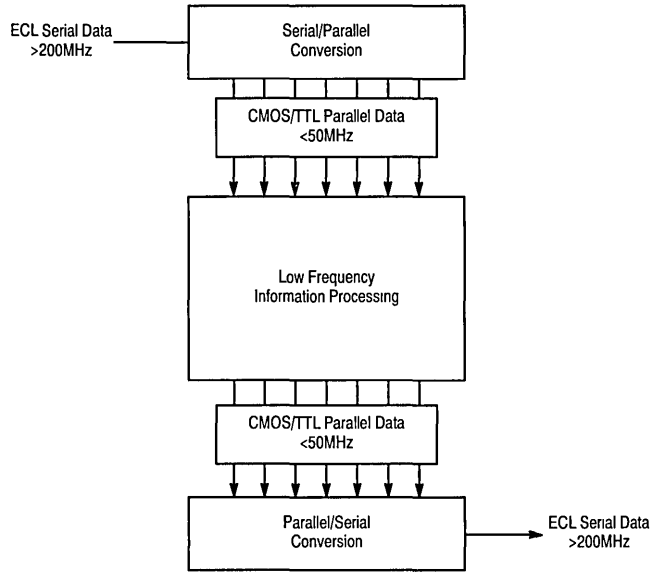

Figure 1. Typical Use of ECL's High Bandwidth, Line Driving Capabilities

Clock Distribution

Perhaps the most attractive area for ECL in CMOS/ TTL designs is in clock distribution. The ever increasing performance capabilities of today's designs has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions throughout an entire system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or costly, faster logic. ECL logic has the capability of significantly reducing the clock skew of a system over an equivalent design utilizing CMOS or TTL technologies.

The skew introduced by a logic device can be broken up into three areas; the part-to-part skew, the within-part skew and the rise-to-fall skew. The part-to-part skew is defined as the differences in propagation delays between any two devices while the within-device skew is the difference between the propagation delays of similar paths for a single device. The final portion of the device skew is the rise-to-fall skew or simply the differences in propagation delay between a rising input and a failing input on the same gate. The within-device skew and the rise-to-fall skew combine with delay variations due to environmental conditions and processing to comprise the part-to-part skew. The part-to-part skew is defined by the propagation delay window described in the device data sheets.

Careful attention to die layout and package choice will minimize within-device skew. Although this minimization is independent of technology, there are other characteristics of ECL which will further reduce the skew of a device. Unlike their CMOS/TTL counterparts, ECL devices are relatively insensitive to variations in supply voltage and temperature. Propagation delay variations with environmental conditions must be accounted for in the specification windows of a device. As a result because of ECLs AC stability the delay windows for a device will inherently be smaller than similar CMOS or TTL functions.

The virtues of differential interconnect in line driving have already been addressed, however the benefits of differential interconnect are even more pronounced in clock distribution. The propagation delay of a signal through a device is intimately tied to the switching threshold of that device. Any deviations of the threshold from the center of the input voltage swing will increase or decrease the delay of the signal through the device. This difference will manifest itself as rise-to-fall skew in the device. The threshold levels for both CMOS and TTL devices are a function of processing, layout, temperature and other factors which are beyond the control of the system level designer. Because of the variability of these switching references, specification limits must be relaxed to guarantee acceptable manufacturing yields. The level of relaxation of these specifications increases with increasing logic depth. As the depth of the logic within a device increases the input signal will switch against an increasing number of reference levels; each encounter will add skew when the reference level is not perfectly centered. These relaxed timing windows add directly to the overall system skew. Differential ECL, both internal and external to the die, alleviates this threshold sensitivity as a DC switching reference is no longer required. Without the need for a switching reference the delay windows, and thus system skew, can be significantly reduced while maintaining acceptable manufacturing yields.

What does this mean to the CMOS/TTL designer? It means that CMOS/TTL designers can build their clock generation card and backplane clock distribution using ECL. Designers will not only realize the benefits of driving long lines with ECL but will also be able to realize clock distribution networks with skew specs unheard of in the CMOS/TTL world. Many specialized functions for clock distribution are available from Motorola (MC10/100E111, MC10/100E211, MC10/100EL11).

Care must be taken that all of the skew gained using ECL for clock distribution is not lost in the process of translating into CMOS/TTL levels. To alleviate this problem the MC10/100H646 can be used to translate and fanout a differential ECL input signal into TTL levels. In this way all of the fanout on the backplane can be done in ECL while the fanout on each card can be done in the CMOS/TTL levels necessary to drive the logic.

Figure 2 illustrates the use of specialized fanout buffers to design a CMOS/TTL clock distribution network with minimal skew. With 50ps output-to-output skew of the MC10/100E111 and 1ns part-to-part skew available on the MC10/100H646 or MC10/100H641, a total of 72 or 81 TTL clocks, respectively, can be generated with a worst case skew between all outputs of only 1.05ns. A similar distribution tree using octal CMOS or TTL buffers would result in worst case skews of more than 6ns. This 5ns improvement in skew equates to about 50% of the up/down time of a 50MHz clock cycle. It is not difficult to imagine situations where an extra 50% of time to perform necessary operations would be either beneficial or even a life saver. For more information about using ECL for clock distribution, refer to application note AN1405/D – ECL Clock Distribution Techniques.

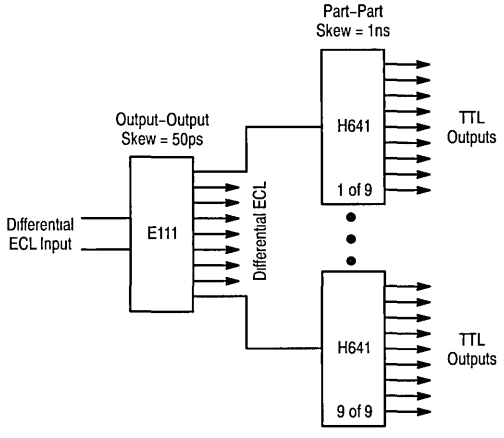

Figure 2. Low Skew Clock Fanout Tree

PECL versus ECL

Nobody will argue that the benefits presented thus far are not attractive, however the argument will be made that the benefits are not enough to justify the requirements of including ECL devices in a predominantly CMOS/TTL design. After all the inclusion of ECL requires two additional negative voltage supplies; V_{EE} and the terminating voltage V_{TT}. Fortunately this is where the advantages of PECL come into play. By using ECL devices on a positive five volt CMOS/TTL power supply and using specialized termination techniques ECL logic can be incorporated into CMOS/TTL designs without the need for additional power supplies. What about power dissipation you ask, although it is true that in a DC state ECL will typically dissipate more power than a CMOS/TTL counterpart, in applications which operate continually at frequency, i.e.. clock distribution, the disparity between ECL and CMOS/TTL power dissipation is reduced. The power dissipation of an ECL device remains constant with frequency while the power of a CMOS/TTL device will increase with frequency. As frequencies approach 50MHz the difference between the power dissipation of a CMOS or TTL gate and an ECL gate will be minimal. 50MHz clock speeds are becoming fairly common in CMOS/TTL based designs as today's high performance MPUs are fast approaching these speeds. In addition, because ECL output swings are significantly less than those of CMOS and TTL the power dissipated in the load will be significantly less under continuous AC conditions.

It is clear that PECL can be a powerful design tool for CMOS/TTL designers, but where can one get these PECL devices. Perhaps the most confusing aspect of PECL is the misconception that a PECL device is a special adaptation of an ECL device. In reality *every* ECL device is also a PECL device; there is nothing magical about the negative voltage supply used for ECL devices. The only real requirement of the power supplies is that the potential difference described in the device data sheets appears across the upper and lower power supply rails (V_{CC} and V_{EE} respectively). A potential stumbling block arises in the specified V_{EE} levels for the various ECL families. The 10H and 100K families specify parametric values for potential differences between V_{CC} and V_{EE} of 4.94V to 5.46V and 4.2V to 4.8V respectively; this poses a problem for the CMOS/TTL designer who works with a typical V_{CC} of 5.0V ±5%. However, because both of these ECL standards are voltage compensated both families will operate perfectly fine and meet all of the performance specifications when operated on standard CMOS/TTL power supplies. In fact, Motorola is extending the V_{EE} specification ranges of many of their ECL families to be compatible with standard CMOS/TTL power supplies. Unfortunately earlier ECL families such as MECL 10K™ are not voltage compensated and therefore any reduction in the potential difference between the two supplies will result in an increase in the V_{OL} level, and thus a decreased noise margin. For the typical CMOS/TTL power supplies a 10K device will experience an ≈50mV increase in the V_{OL} level. Designers should analyze whether this loss of noise margin could jeopardize their designs before implementing PECL formatted 10K using 5.0V ± 5% power supplies.

The traditional choice of a negative power supply for ECL is the result of the upper supply rail being used as the reference for the I/O and internal switching bias levels of the technology. Since these critical parameters are referenced to the upper rail any noise on this rail will couple 1:1 onto them; the result will be reduced noise margins in the design. Because, in general, it is a simpler task to keep a ground rail relatively noise free, it is beneficial to use the ground rail as this reference. However when careful attention is paid to the power supply design, PECL can be used to optimize system performance. Once again the use of differential PECL will simplify the designer's task as the noise margins of the system will be doubled and any noise riding on the upper V_{CC} rail will appear as common mode noise; common mode noise will be rejected by the differential receiver.

MECL to PECL DC Level Conversion

Although using ECL on positive power supplies is feasible, as with any high speed design there are areas in which special attention should be placed. When using ECL devices with positive supplies the input output voltage levels need to be translated. This translation is a relatively simple task. Since these levels are referenced off of the most positive rail, V_{CC}, the following equation can be used to calculate the various specified DC levels for a PECL device:

PECL Level = V_{CC}NEW – |Specification Level|

As an example, the V_{OHMAX} level for a 10H device operating with a V_{CC} of 5.0V at 25°C would be as follows:

PECL Level = 5.0V – |–0.81V|
PECL Level = (5.0 – 0.81)V = 4.19V

The same procedure can be followed to calculate all of the DC levels, including V_{BB} for any ECL device. Table 2 at the bottom of the page outlines the various PECL levels for a V_{CC} of 5.0V for both the 10H and 100K ECL standards. As mentioned earlier any changes in V_{CC} will show up 1:1 on the output DC levels. Therefore any tolerance values for V_{CC} can be transferred to the device I/O levels by simply adding or subtracting the V_{CC} tolerance values from those values provided in Table 2.

PECL Termination Schemes

PECL outputs can be terminated in all of the same ways standard ECL, this would be expected since an ECL and a PECL device are one in the same. Figure 3 illustrates the various output termination schemes utilized in typical ECL systems. For best performance the open line technique in Figure 3 would not be used except for very short interconnect between devices; the definition of short can be found in the various design guides for the different ECL families. In general for the fastest performance and the ability to drive distributive loads the parallel termination techniques are the best choice. However occasions may arise where a long uncontrolled or variable impedance line may need to be driven; in this case the series termination technique would be appropriate. For a more thorough discourse on when and where to use the various termination techniques the reader is referred to the MECL System Design Handbook (HB205/D) and the design guide in the ECLinPS Databook (DL140/D). The parallel termination scheme of Figure 3 requires an extra V_{TT} power supply for the impedance matching load resistor. In a system which is built mainly in CMOS/TTL this extra power supply requirement may prohibit the use of this technique. The other schemes of Figure 3 use only the existing positive supply and ground and thus may be more attractive for the CMOS/ TTL based machine.

Parallel Termination Schemes

Because the techniques using an extra V_{TT} power supply consume significantly less power, as the number of PECL devices incorporated in the design increases the more attractive the V_{TT} supply termination scheme becomes. Typically ECL is specified driving 50Ω into a –2.0V, therefore for PECL with a V_{CC} supply different than ground the V_{TT} terminating voltage will be V_{CC} – 2.0V. Ideally the V_{TT} supply would track 1:1 with V_{CC}, however in theory this scenario is highly unlikely. To ensure proper operation of a PECL device within the system the tolerances of the V_{TT} and the V_{CC} supplies should be considered. Assume for instance that the nominal case is for a 50Ω load (R_t) into a +3.0V supply; for a 10H compatible device with a V_{OHmax} of –0.81V and a realistic V_{OLmin} of –1 .85V the following can be derived:

$I_{OHmax} = (V_{OHmax} - V_{TT})/R_t$
$I_{OHmax} = (\{5.0 - 0.81\} - 3.0)/50 = 23.8mA$
$I_{OLmin} = (V_{OLmin} - V_{TT})/R_t$
$I_{OLmin} = (\{5.0 - 0.81\} - 3.0)/50 = 3.0mA$

If +5% supplies are assumed a V_{CC} of V_{CCnom} –5% and a V_{TT} of V_{TTnom} +5% will represent the worst case. Under these conditions, the following output currents will result:

$I_{OHmax} = (\{4.75 - 0.81\} - 3.15)/50 = 15.8mA$
$I_{OLmin} = (\{4.75 - 1.85\} - 3.15)/50 = 0mA$

Using the other extremes for the supply voltages yields:

$I_{OHmax} = 31.8mA$
$I_{OLmin} = 11mA$

Table 2. ECL/PECL DC Level Conversion for V_{CC} = 5.0V

	10E Characteristics						100E Characteristics		
	0°C		25°C		85°C		0 to 85°C		
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
V_{OH}	–1.02/3.98	–0.84/4.16	–0.98/4.02	–0.81/4 19	–0.92/4.08	–0.735/4.265	–1.025/3.975	–0.880/4.120	V
V_{OL}	–1.95/3 05	–1.63/3 37	–1.95/3.05	–1.63/3 37	–1.95/3.05	–1.600/3 400	–1.810/3.190	–1 620/3 380	V
V_{OHA}	—	—	—	—	—	—	—	–1.610/3 390	V
V_{OLA}	—	—	—	—	—	—	–1 035/3.965	—	V
V_{IH}	–1.17/3.83	–0 84/4.16	–1.13/3.87	–0 81/4.19	–1.07/3.93	–0 735/4.265	–1.165/3.835	–0 880/4.120	V
V_{IL}	–1.95/3.05	–1.48/3 52	–1.95/3 05	–1 48/3.52	–1.95/3.05	–1 450/3 550	–1.810/3.190	–1.475/3.525	V
V_{BB}	–1.38/3.62	–1.27/3.73	–1.35/3 65	–1.25/3.75	–1.31/3 69	–1.190/3.810	–1.380/3.620	–1.260/3.740	V

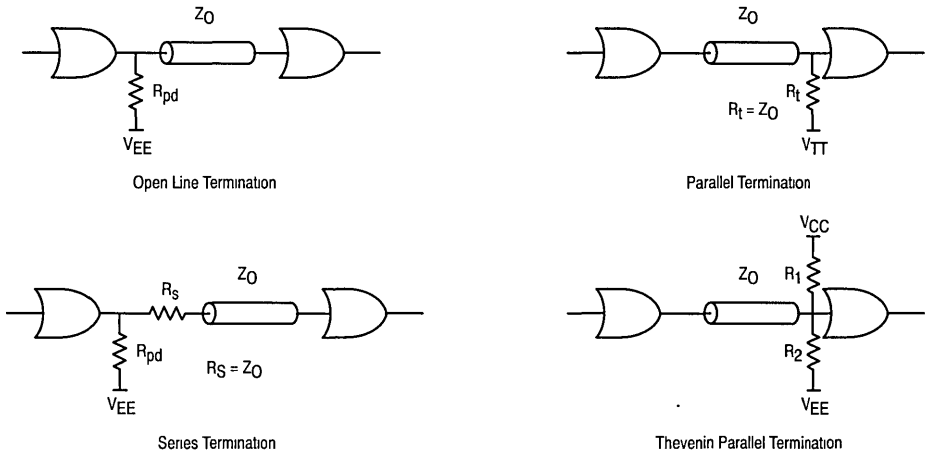

Figure 3. Termination Techniques for ECL/PECL Devices

The changes in the I_{OH} currents will affect the DC V_{OH} levels by ≈±40mV at the two extremes. However in the vast majority of cases the DC levels for ECL devices are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen. The I_{OL} situation on the other hand does pose a potential AC problem. In the worst case situation the output emitter follower could move into the cutoff state. The output emitter followers of ECL devices are designed to be in the conducting "on" state at all times. If cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again this situation will arise only under a number of simultaneous worst case situations and therefore is highly unlikely to occur, but because of the potential it should not be overlooked.

Thevenin Equivalent Termination Schemes

The Thevenin equivalent parallel termination technique of Figure 3 is likely the most attractive scheme for the CMOS/TTL designer who is using a small amount of ECL. As mentioned earlier this technique will consume more power, however the absence of an additional power supply will more than compensate for the extra power consumption. In addition, this extra power is consumed entirely in the external resistors and thus will not affect the reliability of the IC. As is the case with standard parallel termination, the tolerances of the V_{TT} and V_{CC} supplies should be addressed in the design phase. The following equations provide a means of determining the two resistor values and the resulting equivalent V_{TT} terminating voltage.

$$R1 = R2\ (\{V_{CC} - V_{TT}\}/\{V_{TT} - V_{EE}\})$$
$$R2 = Z_O\ (\{V_{CC} - V_{EE}\}/\{V_{CC} - V_{TT}\})$$
$$V_{TT} = V_{CC}\ (R2/\{R1 + R2\})$$

For the typical setup:

V_{CC} = 5.0V; V_{EE} = GND; V_{TT} = 3.0V; and Z_O = 50Ω

$$R2 = 50\ (\{5 - 0\}/\{5-3\}) = 125\Omega$$
$$R1 = 125\ (\{5-3\}/\{3-0\}) = 83.3\Omega$$

checking for V_{TT}

$$V_{TT} = 5\ (125/\{125 - 83.3\}) = 3.0V$$

Because of the resistor divider network used to generate V_{TT} the variation in V will be intimately tied to the variation in V_{CC}. Differentiating the equation for V_{TT} with respect to V_{CC} yields:

$$dV_{TT}/dV_{CC} = R2/(R1 + R2)\ dV_{CC}$$

Again for the nominal case this equation reduces to:

$$\Delta V_{TT} = 0.6\ \Delta V_{CC}$$

So that for ΔV_{CC} = ±5% = ±0.25V, ΔV_{TT} = ±0.15V.

As mentioned previously the real potential for problems will be if the V_{OL} level can potentially put the output emitter follower into cutoff. Because of the relationship between the V_{CC} and V_{TT} levels the only situation which could present a problem will be for the lowest value of V_{CC}. Applying the equation for I_{OLmin} under this condition yields:

$$I_{OLmin} = (\{V_{OLmin} - V_{TT}\}/R_t$$
$$I_{OLmin} = (\{4.75 - 1.85\} - 2.85)/50 = 1.0mA$$

From this analysis it appears that there is no potential for the output emitter follower to be cutoff. This would suggest that the Thevenin equivalent termination scheme is actually a better design to compensate for changes in V_{CC} due to the fact that these changes will affect V_{TT}, although not 1:1 as would be ideal, in the same way. To make the design even more immune to potential output emitter follower cutoff the designer can design for nominal operation for the worst case situation. Since the designer has the flexibility of choosing the V_{TT} level via the selection of the R1 and R2 resistors the following procedure can be followed.

Let V_{CC} = 4.75V and $V_{TT} = V_{CC} - 2.0V$ = 2.75V
Therefore:

R2 = 119Ω and R1 = 86Ω thus:
I_{OHmax} = 23mA and I_{OLmin} = 3.0mA

Plugging in these values for the equations at the other extreme for V_{CC} = 5.25V yields:

V_{TT} = 3.05V, I_{OHmax} = 28mA and I_{OLmin} = 5.2mA

Although the output currents are slightly higher than nominal, the potential for performance degradation is much less and the results of any degradation present will be significantly less dramatic than would be the case when the output emitter follower is cutoff. Again in most cases the component manufactures will provide devices with typical output levels; typical levels significantly reduces any chance of problems. However it is important that the system designer is aware of where any potential problems may come from so they can be dealt with during the initial design.

Differential ECL Termination

Differential ECL outputs can be terminated using two different strategies. The first strategy is to simply treat the complimentary outputs as independent lines and terminate them as previously discussed. For simple interconnect between devices on a single board or short distances across the backplane this is the most common method used. For interconnect across larger distances or where a controlled impedance backplane is not available the differential outputs can be distributed via twisted pair of ribbon cable (use of ribbon cable assumes every other wire is a ground so that a characteristics impedance will arise). Figure 4 illustrates common termination techniques for twisted pair/ribbon cable applications. Notice that Thevenin equivalent termination techniques can be extended to twisted pair and ribbon cable applications as pictured in Figure 4. However for twisted pair/ribbon cable applications the standard termination technique picture in Figure 4 is somewhat simpler and also does not require a separate termination voltage supply. If however the Thevenin techniques are necessary for a particular application the following equations can be used:

$$R1 + R2 = Z_O/2$$
$$R3 = R1\,(V_{TT} - V_{EE})/(V_{OH} + V_{OL} - 2V_{TT})$$
$$V_{TT} = (R3\{V_{OH} + V_{OL}\} + R1\{V_{EE}\})/(R1 + 2R3)$$

where V_{OH}, V_{OL}, V_{EE} and V_{TT} are PECL voltage levels.

Plugging in the various values for V_{CC} will show that the V_{TT} tracks with V_{CC} at a rate of approximately 0.7:1. Although this rate is approaching ideal it would still behoove the system designer to ensure there are no potential situations where the output emitter follower could become cutoff. The calculations are similar to those performed previously and will not be repeated.

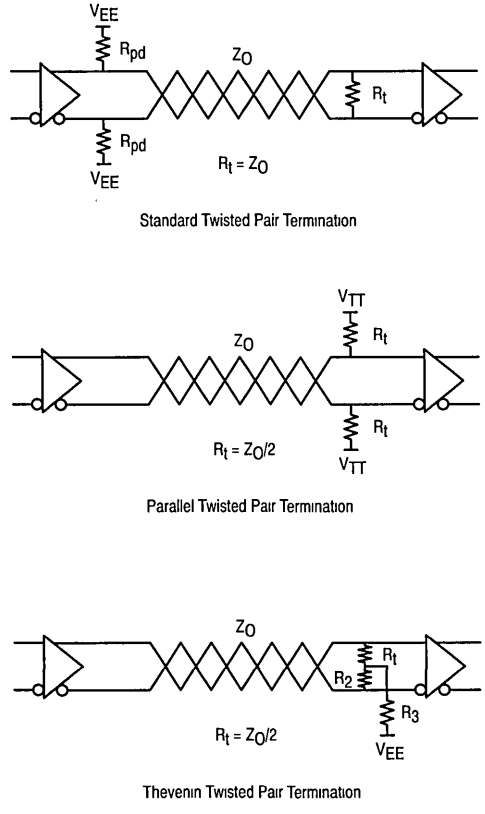

Figure 4. Twisted Pair Termination Techniques

Noise and Power Supply Distribution

Since ECL devices are top rail referenced it is imperative that the V_{CC} rail be kept as noise free and variation free as possible. To minimize the V_{CC} noise of a system liberal bypassing techniques should be employed. Placing a bypass capacitor of 0.01µF to 0.1µF on the V_{CC} pin of every device will help to ensure a noise free V_{CC} supply. In addition when using PECL in a system populated heavily with CMOS and TTL logic the two power supply planes should be isolated as much as possible. This technique will help to keep the large current spike noise typically seen in CMOS and TTL drivers from coupling into the ECL devices. The ideal situation would be multiple power planes; two dedicated to the PECL V_{CC} and ground and the other two to the CMOS/TTL V_{CC} and ground. However if these extra planes are not feasible due to board cost or board thickness constraints common planes with divided subplanes can be used (Figure 5). In either case the planes or sub planes should be connected to the system power via separate paths. Use of separate pins of the board connectors is one example of connecting to the system supplies.

For single supply translators or dual supply translators which share common power pins the package pins should be connected to the ECL V_{CC} and ground planes to ensure the noise introduced to the part through the power plane is minimal. For translating devices with separate TTL and ECL

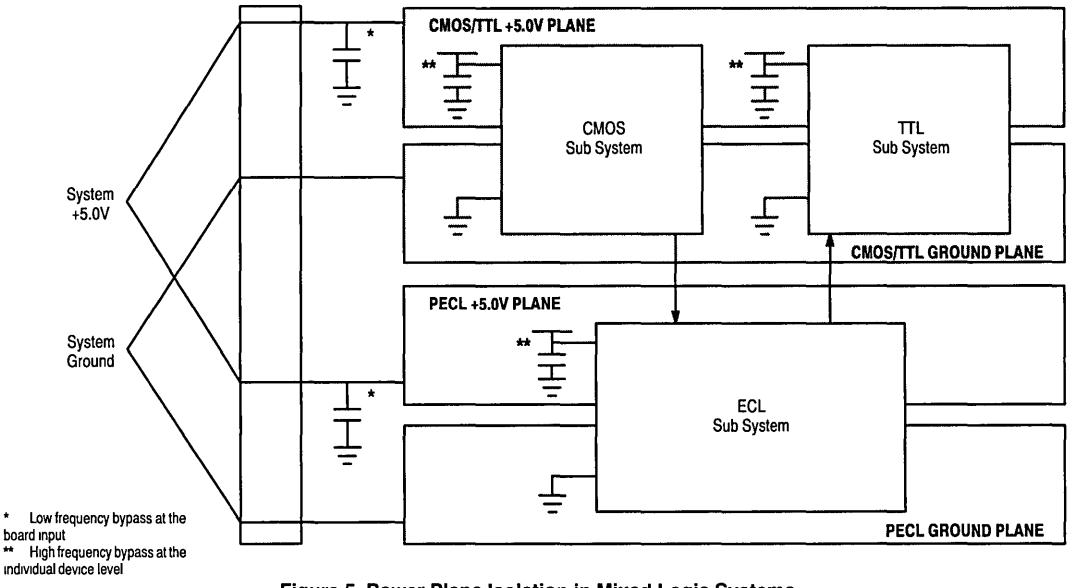

Figure 5. Power Plane Isolation in Mixed Logic Systems

power supply pins, the pins should be tied to the appropriate power planes.

Another concern is the interconnect between two cards with separate connections to the V_{CC} supply. If the two boards are at the opposite extremes of the V_{CC} tolerance, with the driver being at the higher limit and the receiver at the lower limit, there is potential for soft saturation of the receiver input. Soft saturation will manifest itself as degradation in AC performance. Although this scenario is unlikely, again the potential should be examined. For situations where this potential exists there are devices available which are less susceptible to the saturation problem. This variation in V_{CC} between boards will also lead to variations in the input switching references. This variation will lead to switching references which are not ideally centered in the input swing and cause rise/fall skew within the receiving device. Obviously the later skew problem can be eliminated by employing differential interconnect between boards.

When using PECL to drive signals across a backplane, situations may arise where the driver and the receiver are on different power supplies. A potential problem exists if the receiver is powered down independent of the driver. Figure 6 (on the following page) represents a generic driver/receiver pair. From Figure 6, one can see if the receiver is powered down and presents a path to ground through its V_{CC} pin while the driver is still powered at +5.0V the base/collector junction of the input transistor of the receiver will be forward biased and conduct current. Although the collector load resistor will limit the current in the situation of Figure 6, the current may still be enough to damage the junction or exceed the current handling capability of the base electrode metal stripe. Either of these situations could lead to degradation of the reliability of the devices. Because different devices have different ESD protection schemes, and input architectures, the extent of the potential problem will vary from device to device.

Another issue that arises in driving backplanes is situations where the input signals to the receiver are lost and present an open input condition. Many differential input devices will become unstable in this situation, however, most of the newer designs, and some of the older designs, incorporate internal clamp circuitry to guarantee stable outputs under open input conditions. All of the ECLinPS (except for the E111), ECLinPS Lite, and H600 devices, along with the MC10125, 10H125 and 10114 will maintain stable outputs under open input conditions.

Conclusion

The use of ECL logic has always been surrounded by clouds of misinformation; none of those clouds have been thicker than the one concerning PECL. By breaking through this cloud of misinformation the traditional CMOS/TTL designers can approach system problems armed with a complete set of tools. For areas within their designs which require very high speed, the driving of long, low impedance lines or the distribution of very low skew clocks, designers can take advantage of the built in features of ECL. By incorporating this ECL logic using PECL methodologies this inclusion need not require the addition of more power supplies to unnecessarily drive up the cost of their systems. By following the simple guidelines presented here CMOS/TTL designers can truly optimize their designs by utilizing ECL logic in areas in which they are ideally suited. Thus bringing to market products which offer the ultimate in performance at the lowest possible cost.

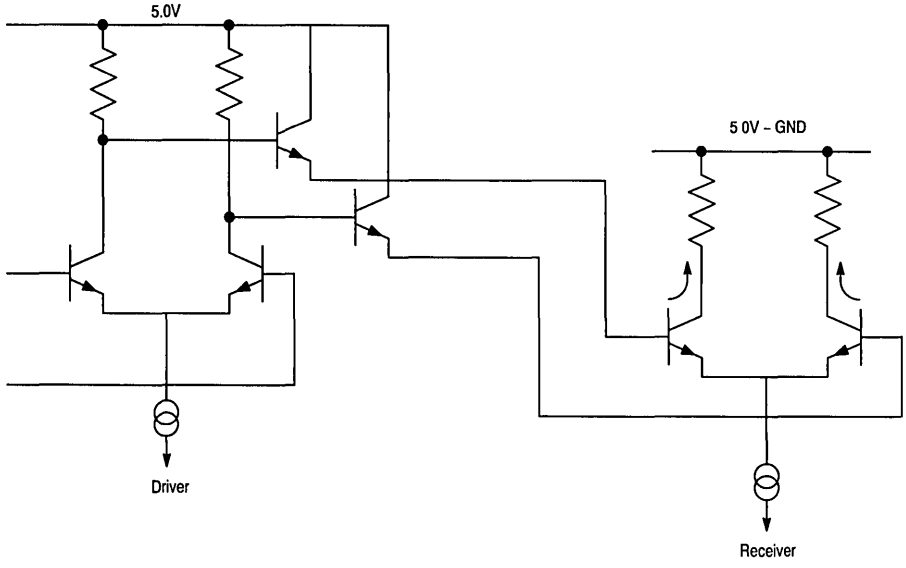

Figure 6. Generic Driver/Receiver Pair

AN1503
Application Note

ECLinPS™ I/O SPICE Modelling Kit

Prepared by
Todd Pearson
ECLinPS Applications Engineering

This application note provides the SPICE information necessary to accurately model system interconnect situations for high speed ECLinPS designs. The note includes information on both the standard ECLinPS family, as well as the ECLinPS Lite products.

4

ECLinPS I/O SPICE Modelling Kit

Objective

The objective of this kit is to provide customers with enough circuit schematic and SPICE parameter information to allow them to perform system level interconnect modelling for the Motorola ECLinPS and ECLinPS Lite logic families. The ECLinPS and ECLinPS Lite families are Motorola's highest performance ECL families. With packaged gate delays of 300ps and output edge rates as low as 175ps these two families define the state-of-the-art in ECL logic. This kit is not intended to provide the user with the information necessary to perform extensive device modelling for any particular ECLinPS or ECLinPS Lite device. If users wish to perform the latter type of SPICE modelling they are encouraged to contact an ECLinPS Applications Engineer to obtain more detailed schematics and SPICE parameter information.

Schematic Information

The kit contains representative schematics for the different I/O circuits used in the ECLinPS and ECLinPS Lite families. In addition a worst case package model schematic is included for more accurate system level modelling. The package model represents the parasitics as they are seen on a corner pin, a sizable distance from an AC ground. If more typical values are desired a 20% reduction in the capacitance and the inductance of the package model can be used. This package model should be placed on all external inputs to the input gates, all outputs of the output gates and on the V_{CC} line. If desired the model can also be placed on the V_{EE} line, however this is not necessary due to the static nature of V_{EE}.

4

There is only one schematic, Figure 1, to represent the input structures of the family. For interconnect purposes this one schematic will adequately represent all of the ECLinPS devices except the differential input devices and the simple gates. The schematic in Figure 1 can be modified to represent differential devices by simply adding the package model and the ESD structure to the "V_{BB}" input and using this as the inverted signal input. For the simple gates the input gate is actually the output gate represented by Figure 2. Therefore these devices should be modelled with the circuit of Figure 2 with the appropriate package model and ESD circuitry from Figure 1 added to the schematic. For the devices in the ECLinPS Lite family outlined in the appendix whose output and input buffers are one in the same the ESD circuitry and package models should be added to the appropriate output buffer. A list of devices which incorporate this structure is included in the appendix of this document.

There are five basic output structures needed to represent both families. The structure in Figure 2 mentioned above represents the structure used in the majority of the family, a simple 50Ω drive output cell. Figures 3 and 4 represent the special output functions used in the ECLinPS and ECLinPS Lite families. Figure 3 shows the circuit configuration for a multiple output device (ie E112). Notice the doubling of the gate current necessary to drive the multiple output emitter followers. Figure 4 is the typical bidirectional 25Ω output structure used for the two bus driving functions currently in the ECLinPS family. Notice the doubled output emitter follower (OEF). This is necessary to provide a small enough V_{BE} to produce an acceptable V_{OH} level while providing the current necessary for 25Ω drive. In addition the collector load resistors have been increased to provide a cutoff V_{OL}. Due to the larger collector load resistor the gate current is increased 3x to reduce the relative size of the collector load resistors so that the I_b of the OEF does not produce an I_R drop across the collector load resistor sufficient to create a marginal V_{OH}.

The schematics in Figures 5 and 6 represent the bandwidth enhanced ECLinPS and ECLinPS Lite devices. Because the bandwidth of standard ECLinPS devices are limited by their rise and fall times, the bandwidth can be enhanced by simply using higher current levels in the output buffers. This added current allows the parasitic capacitances of the gate to charge and discharge more quickly, thus enhancing the transition time performance of the device. Thus far two levels of gate current increase have been used to reach two different plateaus of performance. The majority of the enhanced bandwidth ECLinPS and ECLinPS Lite devices utilize the 2x current increase of Figure 4. A full outline of the devices which utilize these buffers can be found in the appendix.

The schematics of Figure 7 represent the temperature compensation networks present in the output structures for 100E devices. The output buffer schematics all reference one of the temperature compensation networks. The temperature compensation circuitry should be placed as pictured in the output buffer schematics with L and R representing left and right of the schematic. Obviously for 10E circuit outputs these networks can be ignored. Also included in the appendix is the package model of Figure 8 and the ESD circuitry of Figure 9. The ECLinPS ESD should be added to any input of an ECLinPS device being driven by a signal off chip. The ECLinPS Lite ESD should be added to both the inputs and outputs for any ECLinPS Lite device being modelled. Finally the appropriate package model (8–lead SOIC for ECLinPS Lite or 28–lead PLCC for ECLinPS) should be included on all input and output pins and at least the V_{CC} power supply.

Both the typical and multiple output circuits show differential inputs and outputs. If the user is simulating a single ended device the OEF and associated package model and load resistor of the unneeded output should be deleted from the schematic. If the user chooses to drive an output cell directly instead of using the input cell either of the following two driving approaches can be used:

	IN	V_{BB}	Rise/Fall
Diff	–1 2V > –1 6V	–1.6V > –1.2V	180ps (20% – 80%)
S.E.	–0.9V > –1.75V	–1.325V	180ps (20% – 80%)

SPICE Parameter Information

In addition to the schematics a listing of the SPICE parameters for the transistors referenced in the schematics is included. These parameters represent a typical device of the given transistor size. Varying these parameters will obviously affect the voltage levels, the propagation delays, and the transition times of a device. For the type of modelling for which this information is intended the actual propagation delay of a device will not be modelled, as a result variations in this parameter are meaningless. Furthermore the voltage levels and transition times can be more easily varied by other means. This will be addressed in the next section.

All of the resistors referenced in the schematics are polysilicon resistors and thus there is no need to provide parasitic capacitance models for these resistors in the netlist. The only devices needed in the SPICE netlist are illustrated in the schematics.

Modelling Information

The bias driver schematics are not included as they were deemed unnecessary for interconnect simulation, in addition their use also results in a relatively large increase in simulation time. Alternatively the internal reference voltages (V_{BB} and V_{CS}) should be driven with ideal constant voltage sources. The following table summarizes the voltage levels for these internal references as well typical input voltage parameters.

Parameter	Typical Level	Worst Case
V_{BB}	−1.325V	Data Book
V_{CS}	V_{EE} + 1.33V	±50mV
V_{IH}	−0.9V (10E); −0.95V (100E)	Data Book
V_{IL}	−1.75V (10E); −1.7V (100E)	Data Book
Rise/Fall	400ps (20% – 80%)	Data Book

The schematics and SPICE parameters provided will provide a somewhat typical output waveshape which may not represent the worst case system situation. Fortunately there are some simple adjustments that can be made to the schematics to provide output characteristics at or near the corners of the data book specification limits. First to adjust the V_{OH} level one simply needs to lower the V_{CC} value below ground by the amount one wishes to alter the V_{OH} level. This V_{CC} adjustment will obviously also result in a change in the V_{OL} level. To change the V_{OL} level independent of the V_{OH} level the collector load resistors can be increased or decreased depending on the change desired (Note: V_{OH} will change slightly due the the I_bR drop portion of the V_{OH} level). The V_{OL} can also be changed by increasing/decreasing the current in the gate via the current source resistor. In addition to changing the V_{OL} level, by increasing/decreasing the gate current the output rise and fall times will decrease/increase due to the additional current available to charge and discharge the stray capacitance on the collectors of the output differential pair. If the user would like to adjust the levels and transition times of an output gate to represent a corner of the guaranteed specification the following sequence should be followed:

1) Adjust the gate current to produce the desired output slew rate
2) Adjust the V_{CC} for the desired V_{OH}
3) Adjust the collector load resistor for the desired V_{OL}

Summary

The information included in this kit should provide the user with all of the information necessary to do SPICE level system interconnect modelling. The block diagram of Figure 10 illustrates the type of situation which can be effectively modelled using the ECLinPS I/O SPICE Modelling Kit. The schematic information provided in this document is available in netlist form through EMAIL or an IBM or Macintosh disk, although with today's advanced design tools it will probably be a simpler task to enter the schematics in a good schematic capture package than it would be to manipulate the generic netlist. If however the netlist are desired, clarification is needed or additional information is necessary the user is encourage to contact any ECLinPS Application Engineering personnel for assistance.

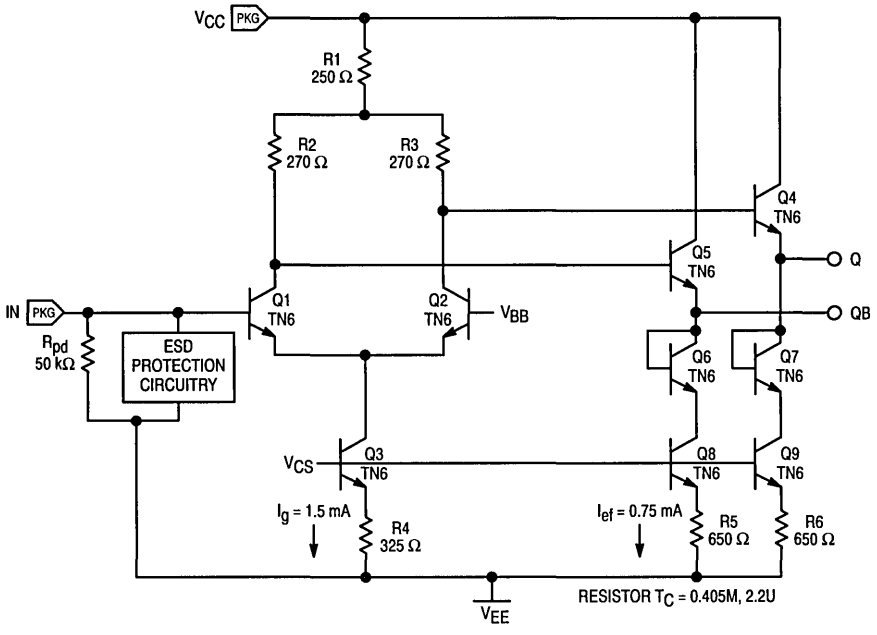

Figure 1. Typical Input Schematic

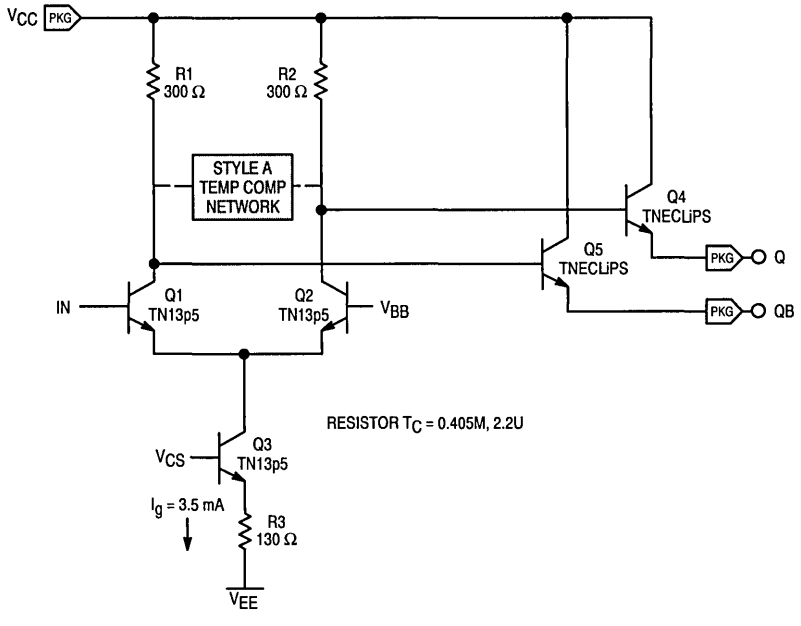

Figure 2. Typical Output Schematic

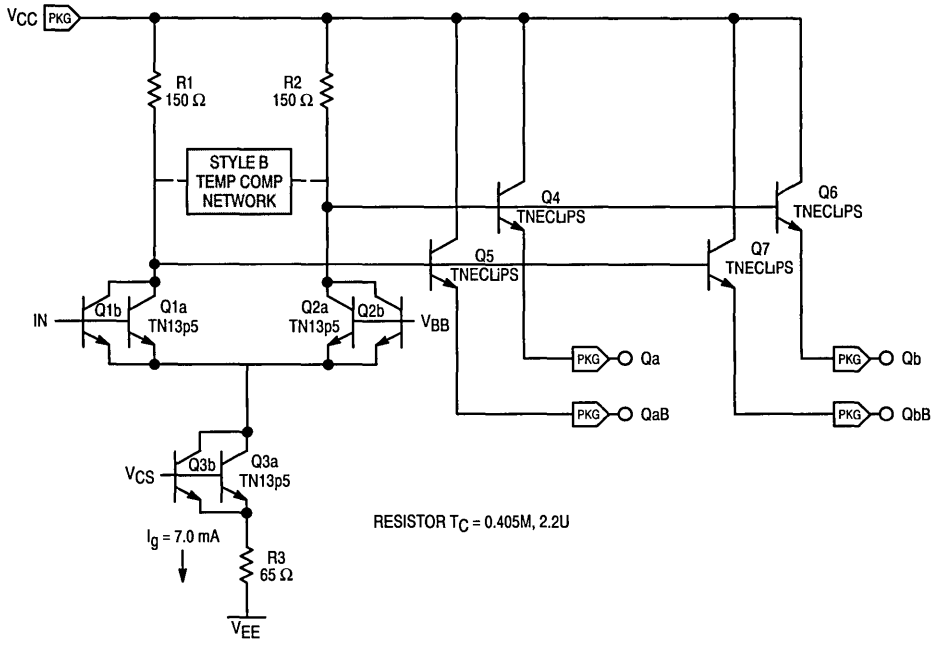

Figure 3. Multiple Output Schematic

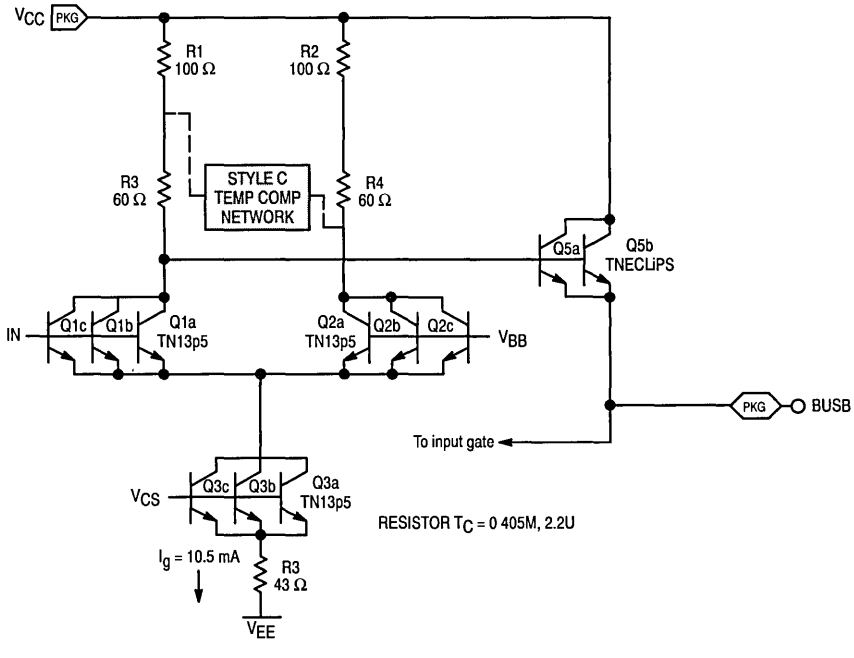

Figure 4. 25 Ω Bus Driver Output

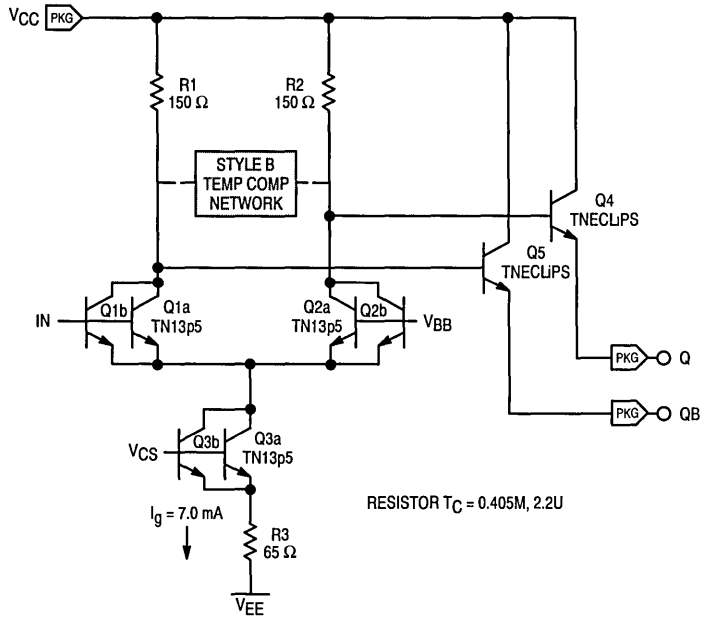

Figure 5. 2x Current Output Schematic

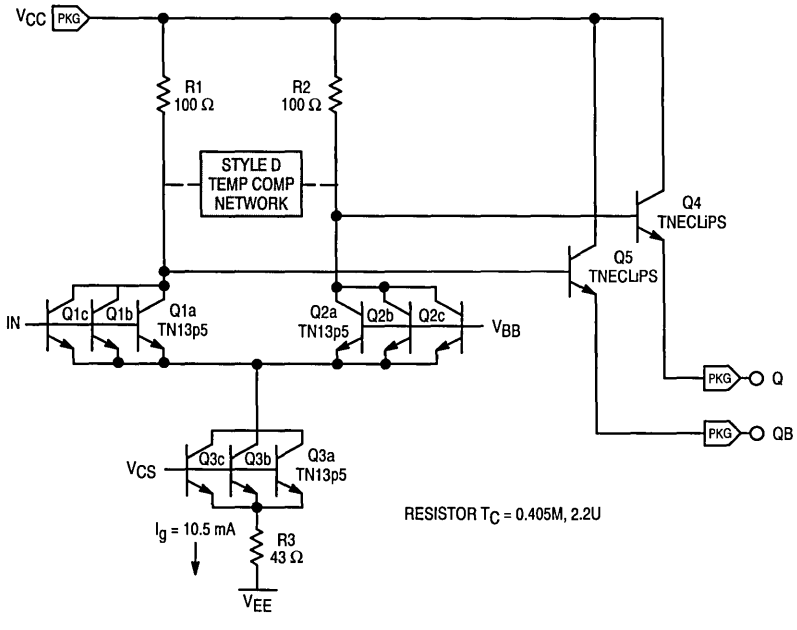

Figure 6. 3x Current Output Schematic

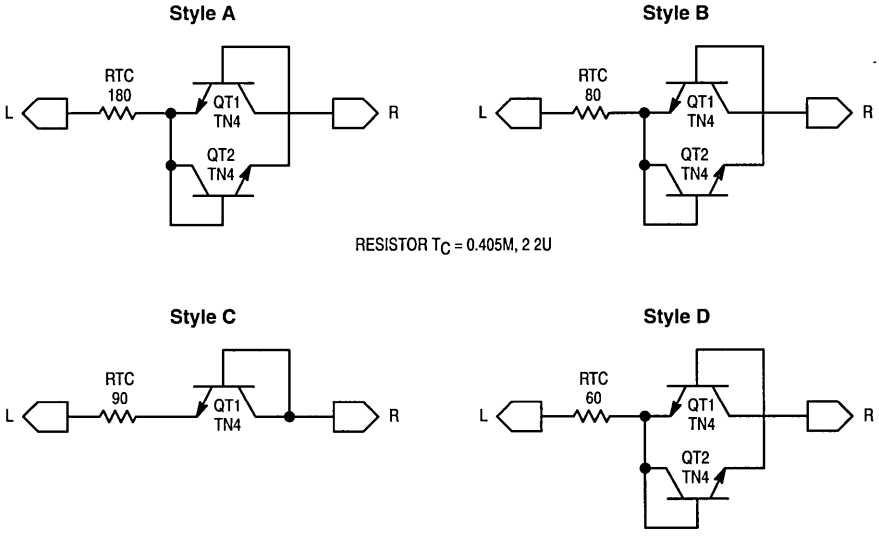

Figure 7. Temperature Compensation Networks

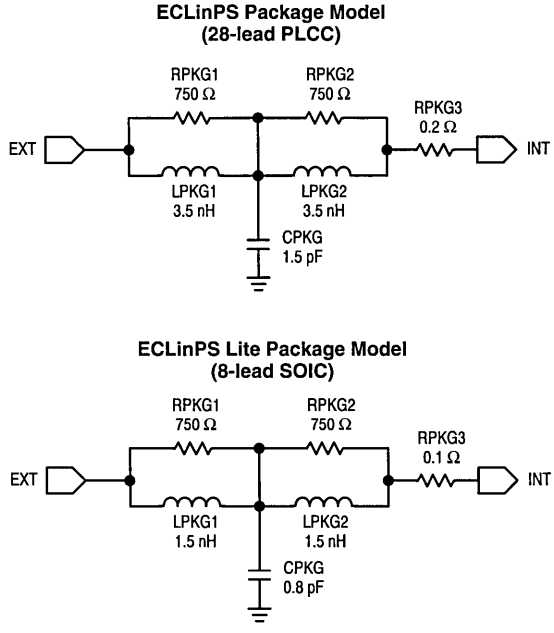

Figure 8. Package Model Schematics

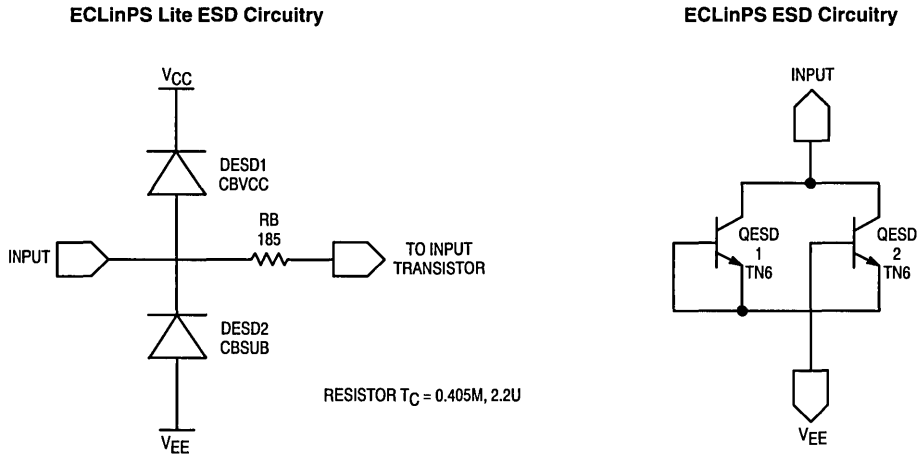

Figure 9. ESD Protection Circuitry

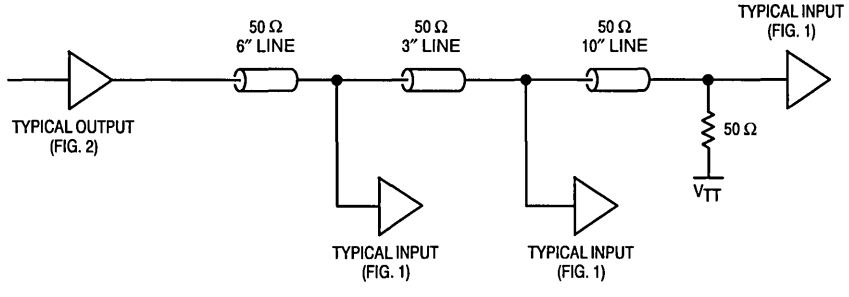

Figure 10. Typical Application for I/O SPICE Modeling Kit

APPENDIX

Schematic/ECLinPS Device Cross Reference

Typical Input	Differential Input	Combination I/O (Gates)
ECLinPS E016, E131, E141, E142, E101, E104, E107, E112, E143, E150 (LEN, MR), E116, E122, E150 (Data), E151, E154, E155, E156, E158 (Data), E158 (SEL), E160, E163, E166, E167, E171, E193, E241, E256, E336, E337	E111, E451, E195, E196, E404, E416, E431, E452, E457, E211	E101, E104, E107, E112, E116, E122, E150 (D), E158 (D), E157 (D)
ECLinPS Lite EL01, EL12, EL31, EL32 (R), EL33 (R), EL35, EL51 (D, R)	EL05, EL11, EL16, EL32 (CLK), EL33 (CLK), EL51 (CLK), EL52, EL89	

Multiple Output Cell	25Ω Bus Outputs	2x Current Output
ECLinPS E112, E212	E336, E337	E195, E196, E211, E404, E457
ECLinPS Lite EL12*		EL01, EL04*, EL05, EL07*, EL11, EL16, EL31, EL32, EL33, EL35, EL51, EL52, EL58*, EL89

3x Current Output	Standard Output
E416	All Others

* These ECLinPS Lite device's inputs feed directly into the output buffer.

SPICE Transistor Model Parameters

```
**** 1.75u x 4.0u emitter
.MODEL TN4          NPN
+ ( IS= 5.27E-18  BF=120  NF=1  VAF=30  IKF=6.48mA
+  ISE= 2.75E-16 BR=10   NE=2  VAR=5   IKR=567uA
+  IRB= 8.1uA    RB= 461.6 RBM= 142.5 RE= 21.6 RC= 83.1
+  CJE= 19.9fF   VJE= .9   MJE= .4          XTB= 0.73
+  CJC= 25.1fF   VJC= .67  MJC= .32         XCJC= .3
+  CJS= 49.6fF   VJS= .6   MJS= .4          FC= .9
+  TF= 8pS       TR= 1nS   XTF= 10   VTF= 1.4V  ITF= 17.0mA
+  ISC= 0  EG=1.11  XTI= 4.0  PTF=0  KF=0  AF=1  NR=1  NC=2)*
*

**** 1.75u x 4.75u emitter
.MODEL TN4P75       NPN
+ ( IS= 6.50E-18  BF=120  NF=1  VAF=30  IKF=8.0mA
+  ISE= 3.40E-16 BR=10   NE=2  VAR=5   IKR=700uA
+  IRB= 10uA     RB= 378.5 RBM= 120 RE= 17.5 RC= 74.0
+  CJE= 23.6fF   VJE= .9   MJE= .4          XTB= 0.73
+  CJC= 27.4fF   VJC= .67  MJC= .32         XCJC= .3
+  CJS= 53.8fF   VJS= .6   MJS= .4          FC= .9
+  TF= 8pS       TR= 1nS   XTF= 10   VTF= 1.4V  ITF= 21.0mA
+  ISC= 0  EG=1.11  XTI= 4.0  PTF=0  KF=0  AF=1  NR=1  NC=2)
*
```

SPICE Transistor Model Parameters (cont.)

```
**** 1.75u x 6.0u emitter
.MODEL TN6        NPN
+ ( IS= 8.56E-18  BF=120  NF=1  VAF=30  IKF=10.5mA
+  ISE= 4.48E-16 BR=10   NE=2  VAR=5   IKR=922uA
+  IRB= 13.2uA    RB= 291.4 RBM= 95.0 RE= 13.3 RC= 62.7
+  CJE= 29.9fF   VJE= .9   MJE= .4          XTB= 0.73
+  CJC= 31.2fF   VJC= .67  MJC= .32         XCJC= .3
+  CJS= 60.9fF   VJS= .6   MJS= .4          FC= .9
+  TF= 8pS       TR= 1nS   XTF= 10   VTF= 1.4V  ITF= 27.6mA
+  ISC= 0  EG=1.11  XTI= 4.0  PTF=0  KF=0  AF=1  NR=1  NC=2)
*

**** 1.75u x 13.5u emitter
.MODEL TN13P5        NPN
+ ( IS= 2.09E-17  BF=120  NF=1  VAF=30  IKF=25.7mA
+  ISE= 1.09E-15 BR=10   NE=2  VAR=5   IKR=2.25mA
+  IRB= 32.2uA    RB= 122.6 RBM= 42.2 RE= 5.44 RC= 32.8
+  CJE= 67.4fF   VJE= .9   MJE= .4          XTB= 0.73
+  CJC= 53.8fF   VJC= .67  MJC= .32         XCJC= .3
+  CJS= 103fF    VJS= .6   MJS= .4          FC= .9
+  TF= 8pS       TR= 1nS   XTF= 10   VTF= 1.4V  ITF= 67.5mA
+  ISC= 0  EG=1.11  XTI= 4.0  PTF=0  KF=0  AF=1  NR=1  NC=2)
*

****ECLinPS Lite ESD Diodes
.MODEL CBVCC D
+ (IS= 1.00E-15 CJO= 527fF Vj= 0.545 M= 0.32 BV= 14.5 IBV= 0.1E-6
+ XTI= 5 TT=1nS)

.MODEL CBSUB D
+ (IS= 1.00E-15 CJO= 453fF TT= 1nS)


**** Output Emitter Follower
.MODEL TNECLIPS        NPN
+ ( IS= 2.27E-16  BF=120  NF=1  VAF=30  IKF=279mA
+  ISE= 1.19E-14 BR=10   NE=2  VAR=5   IKR=24.4mA
+  IRB= 349uA     RB= 15.98 RBM= 4.17 RE= .501 RC= 11.1
+  CJE= 611fF    VJE= .9   MJE= .4          XTB= 0.73
+  CJC= 440fF    VJC= .67  MJC= .32         XCJC= .3
+  CJS= 668fF    VJS= .6   MJS= .4          FC= .9
+  TF= 8pS       TR= 1nS   XTF= 10   VTF= 1.4V  ITF= 733mA
+  ISC= 0  EG=1.11  XTI= 4.0  PTF=0  KF=0  AF=1  NR=1  NC=2)
```

AN1504
Application Note

Metastability and the ECLinPS™ Family

Prepared by
Rennie Wm. Dover
Todd Pearson
ECLinPS Applications Engineering

This application note examines the concept of metastability and provides a theoretical discussion of how it occurs, including examples of the metastable condition. An equation characterizing metastability and a test circuit derived from that equation are presented. Metastability results are then applied to the ECLinPS family.

4

Metastability and the ECLinPS Family

Introduction

Metastability is a central issue anytime a designer wishes to synchronize two or more asynchronous signals. A popular method for accomplishing this task is to employ a D flip-flop as the synchronizing element (Figure 1).

As shown in Figure 1, synchronization can be accomplished using a single D flip-flop; more typically, several D flip-flops are cascaded to provide synchronization while reducing the probability of a metastable or "anomalous" state occurring at the input of System 2. Unfortunately the information at the data and clock inputs of flip-flops used as synchronizing elements is asynchronous by nature, thus the manufacturer specifications for set-up and hold times may not be observed. A series of timing diagrams is shown in Figure 2 demonstrating three possible timing relationships between the data and clock signals; to the right of each data trace is the corresponding output waveform. In the first case the data adheres to the specified set-up and hold times, hence the output attains the proper state. In case 2 the set-up time is violated such that the output of the D flip-flop does not change state. Case 3 represents a violation of the set-up and hold times whereby the D flip-flop enters a metastable state. The resolving time for a flip-flop in this metastable state is indeterminate. Further, the final settling state of the flip-flop having been in this metastable condition cannot be guaranteed.

Metastability Theory

A bistable device such as a flip-flop has two stable output states: the "1" or high state and the "0" or low state. When the manufacturers specified set-up and hold times are observed the flip-flop will achieve the proper output state (Figure 3). However if the set-up and hold times are violated the device may enter a metastable state, thereby increasing the propagation delay, as indicated by the output response shown in Figure 4.

To better understand flip-flop metastability, the operation of a typical ECLinPS D flip-flop is reviewed. The schematic of a D flip-flop is shown in Figure 5.

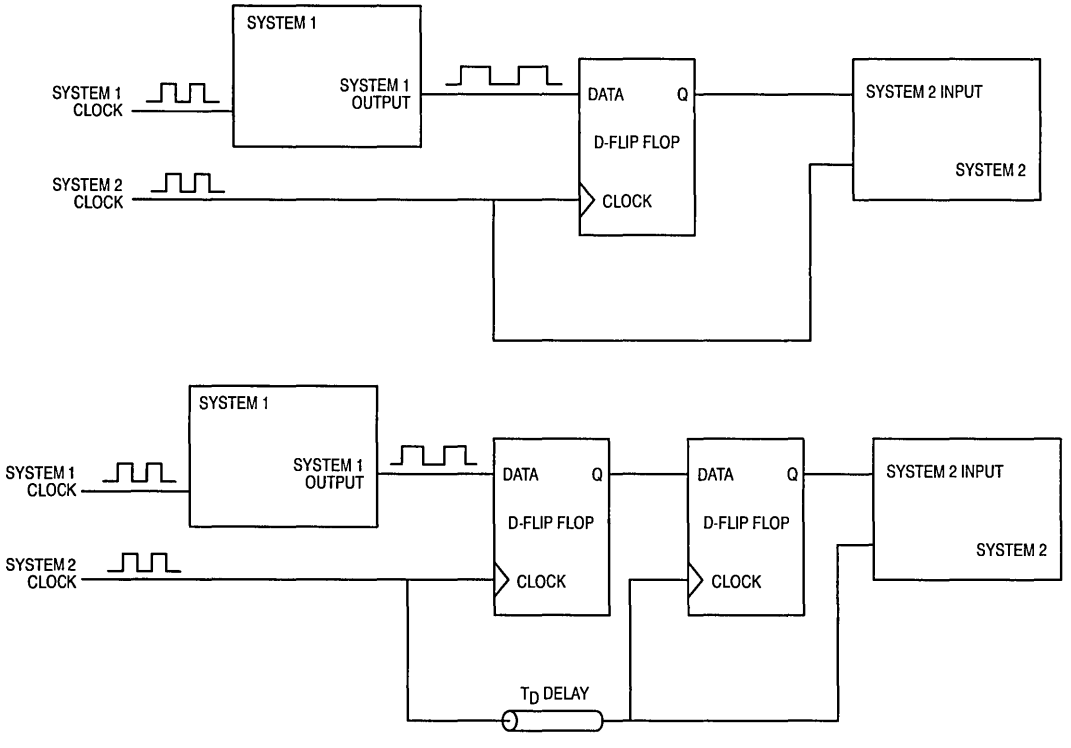

Figure 1. Clock Synchronization Schemes

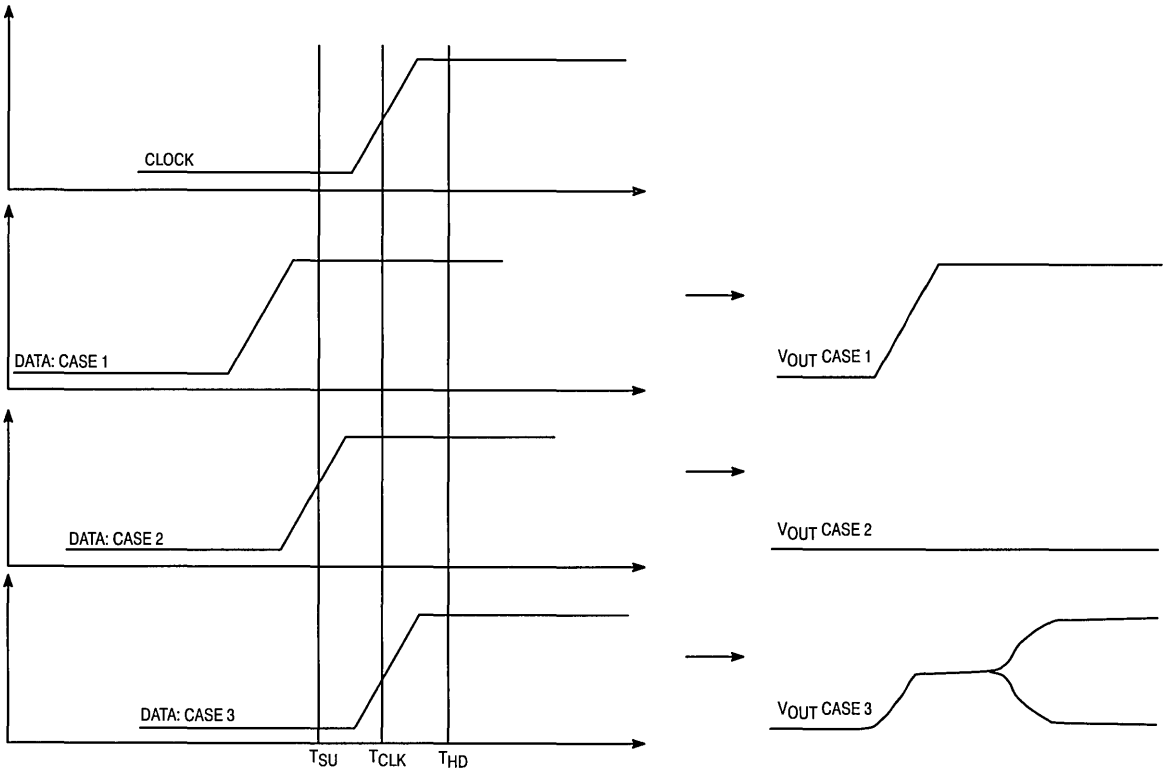

Figure 2. Timing Relationships Between Data and Clock Signals for a D Flip-Flop

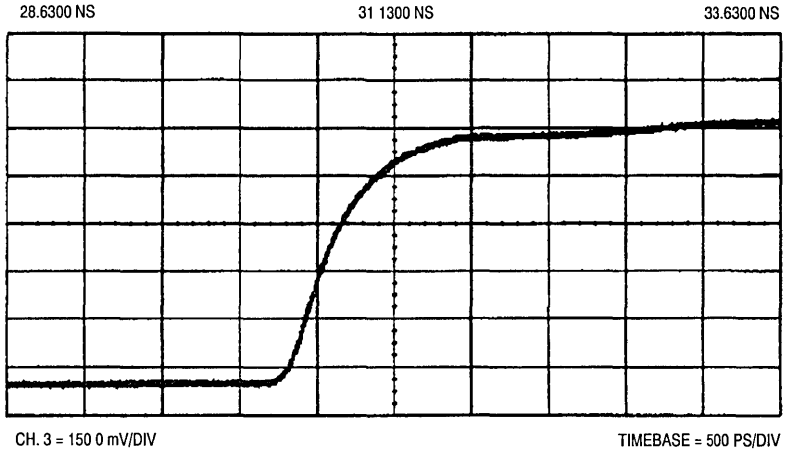

Figure 3. Typical Flip-Flop Output Response

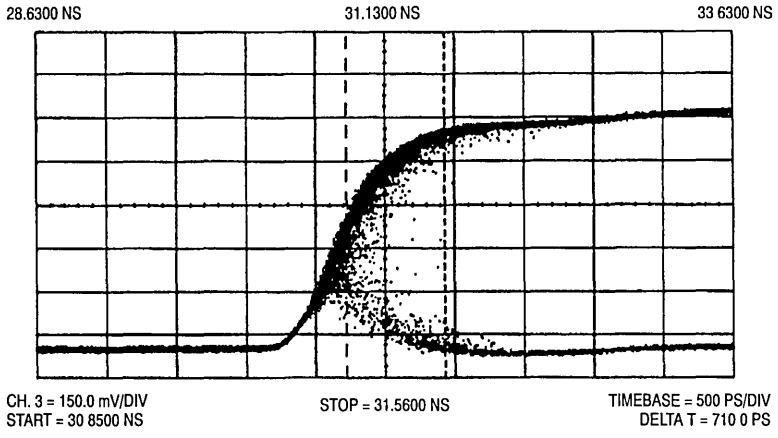

Figure 4. Metastable Flip-Flop Output Response

The flip-flop shown in Figure 5 can be divided into two functional blocks: Master latch and Slave latch. Under optimal operating conditions the clock is low when data arrives at the input to the master latch; after the specified set-up time the clock input is raised to a high level, and the data is latched. When the clock signal goes to the low state, the slave portion of the circuit becomes transparent and transfers the latched data to the output. Changes at the input will have no affect on the output when the "slave latch" is transparent.

The master and slave latches each consist of two subsections: Data and Regenerative (Figure 5). Since the master latch accepts signals from external sources it is the section most susceptible to metastability problems. When the clock signal goes to a high state the current in the master latch clock differential pair switches from the regenerative to the data side. If the set-up and hold times are observed the circuit will function properly. However, if the data and clock signals change such that the set-up and hold times are violated, the data differential pair, the regenerative differential pair and the clock differential pair for the master will share the same switch current. In addition there will not be enough current to charge and discharge the transistor parasitic capacitances, creating an RC feedback loop via the collector nodes of the data and regenerative differential pairs. Thus the master latch enters a metastable state which appears at the output since the slave latch is transparent under these conditions. Theoretically, there is no upper bound on the length of time this metastable state can last, although in practice circuits eventually do leave the metastable region.

4

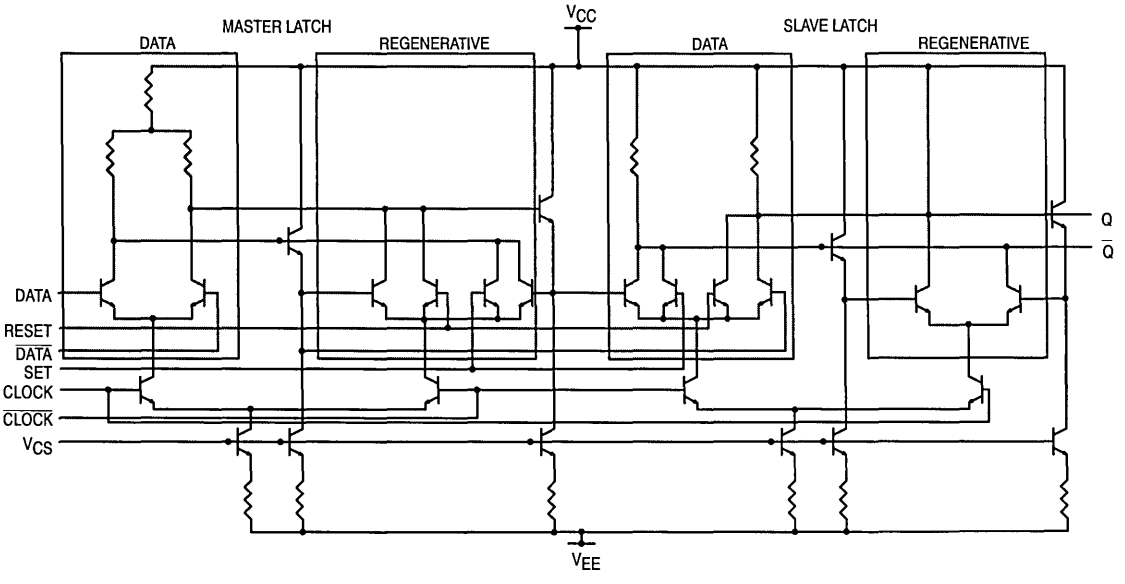

Figure 5. ECLinPS D Flip-Flop

Metastable Equations

Flip-flop propagation delay as a function of the input signal is represented in Figure 6.

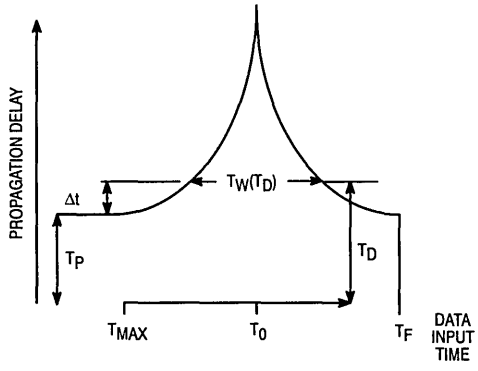

Figure 6. Flip-Flop Response Time Plot

The ordinate is the flip-flop propagation delay time, and the abscissa is the time that data arrives at the flip-flop input relative to reference time, T_0. For devices with positive set-up times T_0 represents the clock transition time with the difference between T_0 and T_{MAX} being the minimum allowable set-up time. Thus data arriving before time T_{MAX} will elicit a nominal propagation delay, T_P, when clocked. For data appearing between times T_{MAX} and T_F the propagation delay will be longer than T_P because the set-up and/or hold times have been violated; and the device enters the metastable state. Data occurring at the input after time T_F will have no affect on the output, hence the output does not change and the propagation delay is defined as zero.

For devices with zero or negative set-up times the same response plot applies, however the abscissa is shifted such that the value of T0 is no longer the clock transition time. The same concepts are valid for derivation of metastability equations for each case: positive, negative or zero set-up and hold times. To clarify the flip-flop response plot, Figure 7a illustrates a case in which the propagation delay is T_P. Data arrives at time T_A, allowing the proper set-up time prior to a clock transition and is maintained at this level for the specified hold time. Figure 7b is an example in which the propagation delay is longer than T_P since the data arrives at time T_A, violating the set-up time.

Using the response plot in Figure 6, Stoll[1] developed the concept of a failure window to facilitate the characterization of metastability. The value of $T_W(T_D)$ is the width of the window for which a propagation delay of time duration T_D occurs, and is the range of data input times relative to the clock input for which a failure will occur. The value of T_D is the maximum allowable propagation delay; delays longer than T_D constitute a failure. The failure window is described mathematically as:

$$T_W(T_D) = T_P * 10^{-(\Delta t)/\tau} \qquad \text{(eqt 1)}$$

Where:	$T_W(T_D)$	Failure Window Width
	T_P	Nominal Propagation Delay
	T_D	Delay After Clock That Constitutes a Failure
	τ	Flip-Flop Resolution Time Constant
	Δt	Excess Delay ($T_D - T_P$)

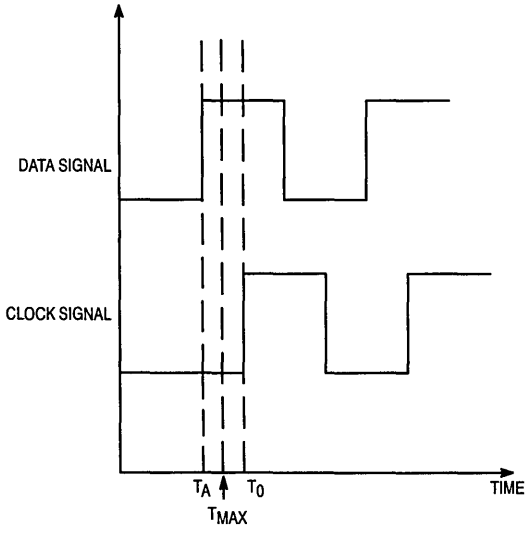

Figure 7a. Proper Set-Up and Hold Times

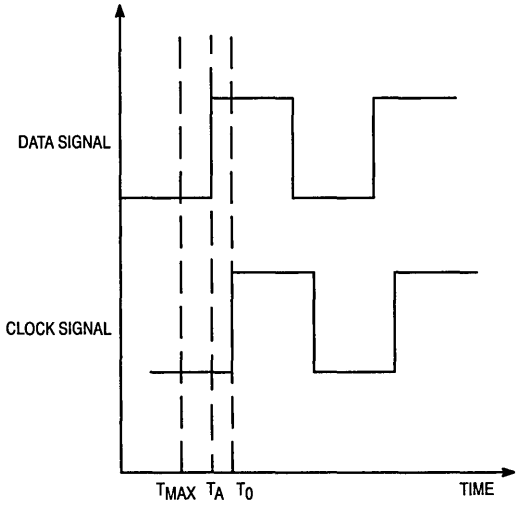

Figure 7b. Violation of Set-Up and Hold Times

This equation only applies for narrow window widths i.e. those times well up on the response plot of Figure 6.

To summarize, when the set-up and hold times are obeyed the flip-flop will have a nominal propagation delay, T_P. If the data and clock signals arrive such that the set-up and hold times are violated there will be an excess delay as indicated in the response plot of Figure 6. This excess delay is caused by the flip-flop entering the metastable region. For data signals arriving much later than the clock signal the flip-flop will not change state, thus the propagation delay is zero by definition. The window width is the range of input arrival times relative to the clock for which the output response does not attain a defined value within the time period T_D. Since T_D represents the maximum allowable delay, the window width represents the relative range of input times for which a failure will occur.

Equation 1 can be combined with the industry accepted definition for system level Mean Time Between Failures (eqt. 2)[2] to derive an equation yielding Mean Time Between Failures as a function of system design and semiconductor device parameters.

$$MTBF = 1/(2*f_C*f_D*T_W(T_D)) \qquad \text{(eqt 2)}$$

Where: f_C Clock Frequency
f_D Data Frequency

$$MTBF = 1/(2*f_C*f_D*T_P*10^{-(\Delta t)/\tau}) \qquad \text{(eqt 3)}$$

The system's designer can use Equation 3 to address the issue of metastability. τ and T_P are provided in the ECLinPS Data Book (DL140/D). MTBF, f_c and f_d are system design parameters. Thus the designer can use this equation to determine the value of T_D.

Test Circuitry For Metastable Evaluation

Equation 3 provides the impetus for the design of a metastability test circuit capable of providing a value of τ, the flip-flop resolution time constant. Transforming this equation into a "linear" form by taking the logarithm of both sides yields Equation 4:

$$\log MTBF = -\log (2*f_C*f_D*T_P) + \Delta t/\tau \qquad \text{(eqt 4)}$$

Plotting log MTBF versus Δt yields a line with slope $1/\tau$, and log MTBF intercept of $-\log(2*f_C*f_d*T_P)$. Thus, the test circuit must accept the clock and data input frequencies as a function of Δt and yield MTBF as an output. The circuit configuration shown in Figure 8 fulfills these criteria.

The test circuitry can be categorized into five functional blocks: DUT, adjustable delay portion, comparator section, counter–set circuitry, and the counter. Starting with the comparator portion of the circuit, the output of the DUT is fed into the comparator; if the DUT output falls in the range V_{BB} – 0.15 volts < V_{BB} < V_{BB} + 0.15 volts, the DUT is defined as being in a metastable condition(Fig. 9).

For DUT output states in the metastable region the comparator output attains a logic high level. When the DUT output does not fall within this range it is in a "defined high or low level," and the output of the comparator will be at a logic low level. If the comparator output is at a logic high level, indicating metastability, the counter–set section sends out a periodic waveform which increments the counter. If the DUT is not metastable the output of the "counter–set" circuitry is constant and the counter (HP–8335A) is not incremented. The total number of counts over a specified time period is a measure of MTBF.

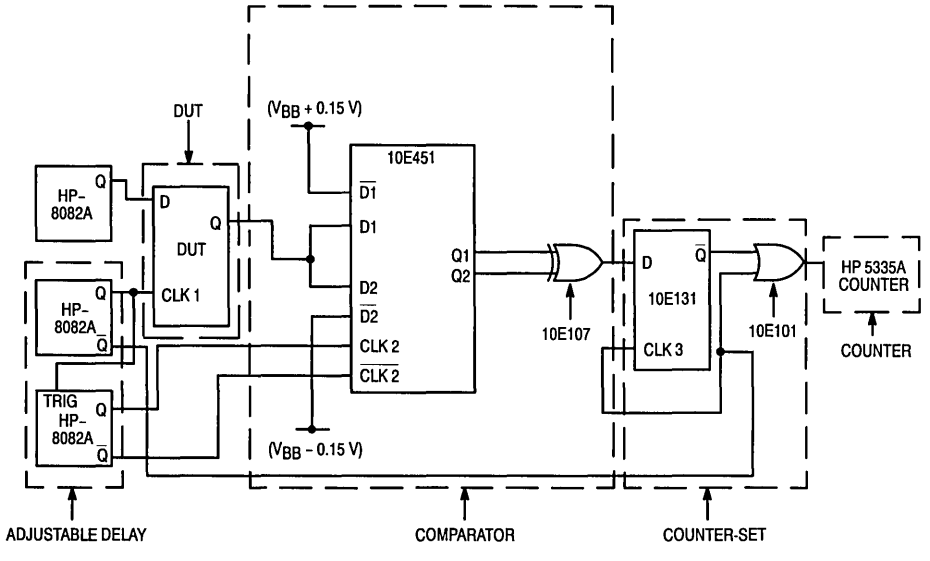

Figure 8. Metastability Test Circuit

Pulse generator #1 (PG 1) supplies the data signal to the DUT. To ensure asynchronous signals between the DUT data and clock signals, a separate pulse generator, PG2, provides the clock signal to the DUT. Generator PG2 also provides the clocking signal to the comparator circuitry via its inverting output terminal. Pulse generator PG3 supplies the clock signals to the E451 portion of the comparator section. To increase the probability of the DUT entering the metastable state the DUT data frequency is set at 1.33 times the DUT clock frequency. The value of Δt is the delay between the noninverting clock signals for the DUT and the E451. Finally, the inverting terminal of PG2 supplies the clock signal for the counter-set circuitry.

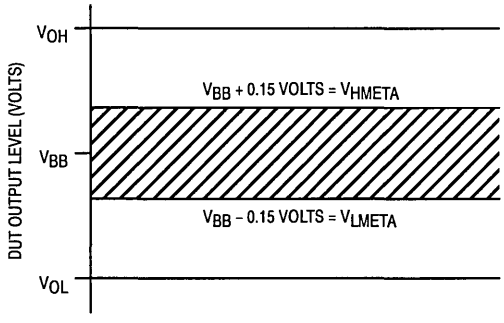

Figure 9. Output Response Defining the Metastable Region

To take advantage of the precision 50Ω input impedance of the test measurement equipment, the circuit power supplies are shifted by +2.0 volts. Thus all input signals, bias voltages, and comparator values have been shifted by +2.0 volts as shown in Table 1.

Table 1. ECL Levels After Translating by +2.0V

Parameter	Typical (V)		Shifted (V)	
	10E	100E	10E	100E
V_{IL}	–1.75	–1.70	+0.25	+0.30
V_{IH}	–0.90	–0.95	+1.10	+1.05
V_{BB}	–1.30	–1.30	+0.70	+0.70
V_{CC}	0.00	0.00	+2.00	+2.00
V_{EE}	–5.20	–4.50	–3.20	–2.50
V_{Hmeta}	–1.15	–1.15	+0.85	+0.85
V_{Lmeta}	–1.45	–1.45	+0.55	+0.85

Results

An example of using a log MTBF versus Δt plot to determine τ is shown in Figure 10.

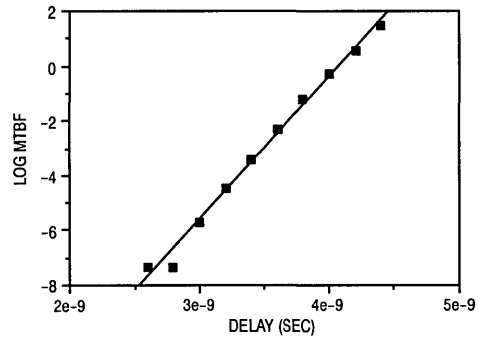

Figure 10. Plot of Log MTBF versus Delay

From Equation 4 the slope of the line is the reciprocal of τ. Measurements similar to these were performed to characterize the ECLinPS family as well as D flip-flops from various vendors. The results are shown in Table 2:

Table 1. τ Values for Several Flip-Flops

Device Type	τ
Motorola 10E431	125 psec
Motorola 10E151	185 psec
Motorola 10E131	200 psec
Motorola 10H131	718 psec
Signetics 100131	890 psec
Signetics 100151	1172 psec
National 100131	1594 psec

Having determined the value of τ, the system designer can use this information in conjunction with Equation 3 to aid in optimizing the system design.

Example

As an example, assume the system configuration shown in Figure 11, in which the output from System 1 is to be synchronized to System 2 using a 10E151 D flip-flop.

Further, the equivalent output signal for System 1 is 75 MHz whereas the clock frequency for System 2, as well as the synchronizing element, is 100 MHz. Under these conditions the data and clock inputs to the D flip-flop are asynchronous and the system designer must consider the possibility of the D flip-flop entering the metastable state. Therefore the system designer must determine how long the flip-flop will remain in the metastable region in order to decide when the data at the output of the flip-flop will attain a defined state and can be clocked into System 2.

The solution to this dilemma is found with Equation 3:

$$MTBF = 1/(2*f_C*f_D*T_P*10^{-(\Delta t)/\tau})$$

The values for fc and fd were specified as 100 MHz and 75 MHz, respectively. Assuming the D flip-flop is a Motorola 10E151, a worse case value of propagation delay (Tp) of 800 psec is obtained from the ECLinPS Device Data Book. The value of t is given in Table 2 as 185 psec. Substituting these values into Equation 3 yields:

$$MTBF = 1/(2*f_C*f_D*T_P*10^{-(\Delta t/185\ psec)})$$

At this point the system designer must specify an acceptable MTBF. For this example an MTBF of 5 years is assumed. Therefore the value of Δt is calculated to be

$$\Delta t = 2.83\ nsec$$

From the relationship

$$\Delta t = T_D - T_P$$

the value of T_D is calculated to be

$$T_D = 3.63\ nsec$$

Thus for an MTBF of 5 years the designer should delay the clocking of the data from the output of the flip-flop into System 2 by 3.63 nsec.

Conclusion

Metastability has become a critical issue with system designers. In order to better serve our customers, Motorola has characterized the ECLinPS family for metastability using the concept of a failure window. The nominal flip-flop resolution time constant for the ECLinPS family, excluding the E131 and E431 devices as these flip-flops use alternative architectures, has been determined to be 185 psec. The resolution time constant for the E131 and E431 devices is 200 psec and 125 psec, respectively. Thus the system designer can use the value of τ in conjunction with Equation 3 to determine the metastable induced excess delay for a specified MTBF. Although this application note does not present a method for avoiding metastability, it does provide a means for the designer to quantitatively incorporate metastability in their designs.

References

1 Stoll, P. "How to Avoid Synchronization Problems" VLSI Design, November/December 1982. pp. 56–59.

2 Nootbaar, K. "Design, Testing, and Application of a Metastable-Hardened flip-flop," Wescon/87, Section 16–2 pp. 1–9.

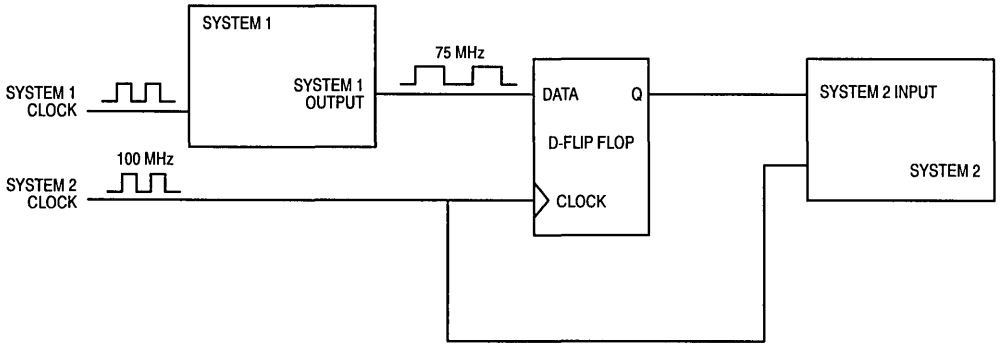

Figure 11. System Example

Logic Literature Listing

For additional information, refer to the following Motorola Logic Documents, available through the Literature Distribution Center.

LOGIC NEW PRODUCT CALENDAR

BR1332/D ..... Logic New Product Calendar

SELECTOR GUIDES

SG73/D ..... Motorola Semiconductor Master Selection Guide
SG127/D ..... Surface Mount Products Selector Guide
SG365/D ..... Timing Solutions Folder Selector Guide
SG366/D ..... TTL, ECL, CMOS and Special Logic Circuits Selector Guide

DATA BOOKS

BR1330/D ..... ECLinPS Lite™ (Single Gate ECL Devices and Translators)
BR1333/D ..... Timing Solutions
BR1334/D ..... High Performance Frequency Control Products
DL121/D ..... FAST and LS TTL Data
DL122/D ..... MECL Data
DL129/D ..... High-Speed CMOS Data
DL131/D ..... CMOS Logic Data
DL138/D ..... FACT Data

DESIGN HANDBOOKS

HB205/D ..... MECL Systems Design Handbook

APPLICATION NOTES

AN1091/D ..... Low Skew Clock Drivers and Their System Design Considerations
AN1092/D ..... Driving High Capacitance DRAMs in an ECL System
AN1400/D ..... H64x Clock Driver I/O SPICE Modelling Kit
AN1401/D ..... Using SPICE to Analyze the Effects of Board Layout on System Skew When Designing With the MC10/100640 Family of Clock Drivers
AN1402/D ..... MC10/100H600 Translator Family I/O SPICE Modelling Kit
AN1403/D ..... FACT™ I/O Model Kit
AN1404/D ..... ECLinPS™ Circuit Performance at Non-Standard VIH Levels
AN1405/D ..... ECL Clock Distribution Techniques
AN1406/D ..... Designing With PECL (ECL at +5.0V)
AN1407/D ..... Performance Testing With the ALExIS™ Mini-Evaluation Boards
AN1408/D ..... Power Dissipation for Active SCSI Terminators
AN1410/D ..... Configuring and Applying the MC54/74HC4046A Phase-Locked Loop
AN1503/D ..... ECLinPS™ I/O SPICE Modelling Kit
AN1504/D ..... Metastability and the ECLinPS™ Family

OTHER LITERATURE

BR1331/D ..... ALExIS - Advanced Low-Power Expandable Interface Solutions Folder
BR1409/D ..... Motorola ECL300™ LogicArray

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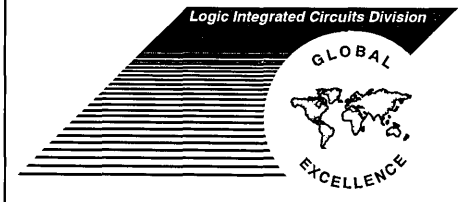

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