MOTOROLA

DL156/D
REV 3

Fast Static RAM

Component and Module Data

MOTOROLA FAST STATIC RAM DATA

Q3/95
DL156
REV 3

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MOTOROLA

Fast Static RAM
Component and Module Data

Motorola offers a broad range of fast SRAMs for virtually any digital data processing system application. This data book contains complete specifications for individual FSRAM circuits in data sheet form, as well as an explanation of Motorola's reliability and quality program and an applications section.

For information on Dynamic RAM devices, please refer to DL155/D.

New Motorola memories are being introduced continually. For the latest releases, additional technical information, and pricing, please contact your nearest authorized Motorola distributor or Motorola Sales Office. A complete listing of distributors and sales offices is included at the back of this book.

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Selector Guide and Cross Reference

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		25	—	Paradigm	PDM41096									
		25	—	Samsung	KM684002									
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		12	20	Motorola	MCM72BA32	136		DIMM				◊	◊	6–84
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		9	—	Paradigm	PDM44018									
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		7	12.5	**Motorola**	MCM67N618A	52		PLCC		◊		◊	◊	5–148
		8.5/10/12	12/15/16.6	**Motorola**	MCM69F618	100		TQFP		◊		◊		5–179
		5/6/7	10/12/13.3	**Motorola**	MCM69P618	100		TQFP		◊		◊		5–190
		5/6/7	—	**Motorola**	MCM69T618	119		PBGA		◊		◊		4–152
	128K x 8	15	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊		3–39
		15	—	Cypress	CY7C109A									
		15	—	Cypress	CY7C1009									
		15	—	IDT	IDT71024S									
		15	—	Micron	MT5C1008									
		15	—	NEC	µPD431008									
		15	—	Quality	QS812880									
		15	—	Samsung	KM681002									
		15	—	Sony	CXK581120J									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
1M (cont.)	128K x 8 (cont.)	20	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊		3–39
		20	—	Cypress	CY7C109A									
		20	—	Cypress	CY7C1009									
		20	—	Fujitsu	MB82008									
		20	—	IDT	IDT71024S									
		20	—	Micron	MT5C1008									
		20	—	NEC	µPD431008									
		20	—	Quality	QS812880									
		20	—	Samsung	KM681002									
		20	—	Samsung	KM681001									
		20	—	Sharp	LH521007AK									
		20	—	Sony	CXK581120									
		25	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊		3–39
		25	—	Cypress	CY7C109A									
		25	—	Cypress	CY7C1009									
		25	—	Fujitsu	MB82008									
		25	—	IDT	IDT71024S									
		25	—	Micron	MT5C1008									
		25	—	Samsung	KM681001									
		25	—	Sharp	LH521007AS									
		25	—	Quality	QS812880									
		35	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊		3–39
		35	—	Cypress	CY7C109A									
		35	—	Cypress	CY7C1009									
		35	—	Fujitsu	MB82008									
		35	—	IDT	IDT71024S									
		35	—	Micron	MT5C1008									
		35	—	Samsung	KM681001									
		35	—	Sharp	LH521007AS									
		35	—	Quality	QS812880									
		15	—	**Motorola**	MCM6226BA	32	300/400	SOJ				◊		3–45
		17	—	**Motorola**	MCM6226BA	32	300/400	SOJ				◊		3–45
		20	—	**Motorola**	MCM6226BA	32	300/400	SOJ				◊		3–45
		25	—	**Motorola**	MCM6226BA	32	300/400	SOJ				◊		3–45
		35	—	**Motorola**	MCM6226BA	32	300/400	SOJ				◊		3–45
		8	—	**Motorola**	MCM6726B	32	400	SOJ	◊			◊		2–88
		8	—	NEC	µPD461008									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
1M (cont.)	128K x 8 (cont.)	8	—	Samsung	KM68B1002									
		10	—	**Motorola**	MCM6726B	32	400	SOJ	◊			◊		2–88
		10	—	IDT	IDT71B124									
		10	—	Samsung	KM68B1002									
		12	—	**Motorola**	MCM6726B	32	400	SOJ	◊			◊		2–88
		12	—	IDT	IDT71B124									
		12	—	Micron	MT5C128K8A1									
		12	—	Paradigm	PDM41024									
		12	—	Samsung	KM68B1002									
		6	—	**Motorola**	MCM6726C	32	400	SOJ	◊			◊		2–94
		7	—	**Motorola**	MCM6726C	32	400	SOJ	◊			◊		2–94
		8	—	**Motorola**	MCM6926	32	400	SOJ	◊			◊		2–124
		10	—	**Motorola**	MCM6926	32	400	SOJ	◊			◊		2–124
		12	—	**Motorola**	MCM6926	32	400	SOJ	◊			◊		2–124
		15	—	**Motorola**	MCM6926	32	400	SOJ	◊			◊		2–124
	128K x 9	—	16	**Motorola**	MCM67D709	52		PLCC	◊	◊		◊		4–125
		—	20	**Motorola**	MCM67D709	52		PLCC	◊	◊		◊		4–125
		5	10	**Motorola**	MCM67Q709	86		PBGA	◊	◊		◊		4–135
		6	12	**Motorola**	MCM67Q709	86		PBGA	◊	◊		◊		4–135
	256K x 4	15	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊		3–70
		15	—	Cypress	CY7C106A									
		15	—	Fujitsu	MB82B005									
		15	—	IDT	IDT71028S									
		15	—	Micron	MT5C1005DJ									
		15	—	Mitsubishi	M5M51004P									
		17	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊		3–70
		20	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊		3–70
		20	—	Cypress	CY7C106A									
		20	—	Fujitsu	MB82B005									
		20	—	Hitachi	HM624256AJ									
		20	—	IDT	IDT7101285									
		20	—	Micron	MT5C1005DJ									
		20	—	Mitsubishi	M5M51004P									
		20	—	NEC	µPD431004									
		20	—	Samsung	KM641001									
		20	—	Sharp	LH521002AK									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
1M (cont.)	256K x 4 (cont.)	25	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊		3–70
		25	—	Cypress	CY7C106A									
		25	—	Fujitsu	MB82B005									
		25	—	Hitachi	HM624256AJ									
		25	—	IDT	IDT7101285									
		25	—	Micron	MT5C1005DJ									
		25	—	Mitsubishi	M5M51004P									
		25	—	NEC	µPD431004									
		25	—	Samsung	KM641001									
		25	—	Sharp	LH521002AK									
		35	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊		3–70
		35	—	Cypress	CY7C106A									
		35	—	Fujitsu	MB82B005									
		35	—	Hitachi	HM624256AJ									
		35	—	IDT	IDT7101285									
		35	—	Micron	MT5C1005DJ									
		35	—	Mitsubishi	M5M51004P									
		35	—	NEC	µPD431004									
		35	—	Samsung	KM641001									
		35	—	Sharp	LH521002AK									
		15	—	**Motorola**	MCM6229BA	28	300/400	SOJ				◊		3–76
		17	—	**Motorola**	MCM6229BA	28	300/400	SOJ				◊		3–76
		20	—	**Motorola**	MCM6229BA	28	300/400	SOJ				◊		3–76
		25	—	**Motorola**	MCM6229BA	28	300/400	SOJ				◊		3–76
		35	—	**Motorola**	MCM6229BA	28	300/400	SOJ				◊		3–76
		8	—	**Motorola**	MCM6729B	32	400	SOJ	◊			◊		2–112
		8	—	Samsung	KM64B1003									
		10	—	**Motorola**	MCM6729B	32	400	SOJ	◊			◊		2–112
		10	—	IDT	IDT71B128									
		10	—	Samsung	KM64B1003									
		12	—	**Motorola**	MCM6729B	32	400	SOJ	◊			◊		2–112
		12	—	IDT	IDT71B128									
		12	—	Micron	MT5C256KA1									
		12	—	Samsung	KM64B1003									
		12	—	Toshiba	TC55B4257P									
		6	—	**Motorola**	MCM6729C	32	400	SOJ	◊			◊		2–118
		7	—	**Motorola**	MCM6729C	32	400	SOJ	◊			◊		2–118

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
1M (cont.)	256K x 4 (cont.)	8	—	**Motorola**	MCM6929	32	400	SOJ	◊			◊		2–131
		10	—	**Motorola**	MCM6929	32	400	SOJ	◊			◊		2–131
		12	—	**Motorola**	MCM6929	32	400	SOJ	◊			◊		2–131
		15	—	**Motorola**	MCM6929	32	400	SOJ	◊			◊		2–131
		5	10	**Motorola**	MCM67Q804	36	400	SOJ	◊	◊		◊		4–145
		5	—	Samsung	KM741006									
		5	—	Sony	CXK77410									
		6	12	**Motorola**	MCM67Q804	36	400	SOJ	◊	◊		◊		4–145
		6	—	Samsung	KM741006									
		6	—	Sony	CXK77410									
	1M x 1	15	—	**Motorola**	MCM6227B	28	300/400	SOJ						3–58
		15	—	Cypress	CY7C107A									
		15	—	Cypress	CY7C1007									
		15	—	Micron	MT5C1001DJ									
		15	—	Sony	CXK81020SJ									
		17	—	**Motorola**	MCM6227B	28	300/400	SOJ						3–58
		20	—	**Motorola**	MCM6227B	28	300/400	SOJ						3–58
		20	—	Cypress	CY7C107A									
		20	—	Cypress	CY7C1007									
		20	—	Hitachi	HM621100A									
		20	—	Micron	MT5C1001DJ									
		20	—	NEC	µPD431001									
		25	—	**Motorola**	MCM6227B	28	300/400	SOJ						3–58
		25	—	Cypress	CY7C107A									
		25	—	Cypress	CY7C1007									
		25	—	Fujitsu	MB82B001									
		25	—	Hitachi	HM621100A									
		25	—	Micron	MT5C1001DJ									
		25	—	NEC	µPD431001									
		25	—	Samsung	KM611001									
		35	—	**Motorola**	MCM6227B	28	300/400	SOJ						3–58
		35	—	Cypress	CY7C107A									
		35	—	Fujitsu	MB82B001									
		35	—	Hitachi	HM621100A									
		35	—	Micron	MT5C1001DJ									
		35	—	NEC	µPD431001									
		35	—	Samsung	KM611001									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
512K	32K x 18	10	—	Motorola	MCM67A518	52		PLCC			◊	◊		4–92
		12	—	Motorola	MCM67A518	52		PLCC			◊	◊		4–92
		12	—	Paradigm	PDM41518									
		15	—	Motorola	MCM67A518	52		PLCC			◊	◊		4–92
		15	—	Paradigm	PDM41518									
		9	15	Motorola	MCM67B518	52		PLCC		◊		◊	◊	5–31
		9	—	IC Works	ICW73B586									
		9	—	Paradigm	PDM44518									
		9	—	Samsung	KM718B513									
		10	—	Motorola	MCM67B518	52		PLCC		◊		◊	◊	5–31
		12	20	Motorola	MCM67B518	52		PLCC		◊		◊	◊	5–31
		12	—	IC Works	ICW73B586									
		12	—	Paradigm	PDM44518									
		12	—	Samsung	KM718B513									
		6	10	Motorola	MCM67C518	52		PLCC		◊		◊	◊	5–40
		7	12.5	Motorola	MCM67C518	52		PLCC		◊		◊	◊	5–40
		9	15	Motorola	MCM67C518	52		PLCC		◊		◊	◊	5–40
		9	15	Motorola	MCM67H518	52		PLCC		◊		◊	◊	5–49
		9	—	IDT	IDT71420									
		9	—	Paradigm	PDM44528									
		9	—	Samsung	KM718B514									
		10	16.6	Motorola	MCM67H518	52		PLCC		◊		◊	◊	5–49
		10	—	Cypress	CY7C178									
		10	—	IDT	IDT71420									
		10	—	Paradigm	PDM44528									
		10	—	Samsung	KM718B514									
		12	20	Motorola	MCM67H518	52		PLCC		◊		◊	◊	5–49
		12	—	IDT	IDT71420									
		12	—	Samsung	KM718B514									
		6	10	Motorola	MCM67J518	52		PLCC		◊		◊	◊	5–58
		7	12.5	Motorola	MCM67J518	52		PLCC		◊		◊	◊	5–58
		9	15	Motorola	MCM67J518	52		PLCC		◊		◊	◊	5–58
		9	12.5	Motorola	MCM67M518	52		PLCC		◊		◊	◊	5–67
		9	12.5	Paradigm	PDM44538									
		11	15	Motorola	MCM67M518	52		PLCC		◊		◊	◊	5–67
		14	20	Motorola	MCM67M518	52		PLCC		◊		◊	◊	5–67

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K	**16K x 16**	12	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊	4–65
		12	—	Micron	MT58C1616EJ									
		15	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊	4–65
		15	—	Micron	MT58C1616EJ									
		20	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊	4–65
		20	—	Micron	MT58C1616EJ									
		25	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊	4–65
		25	—	Micron	MT58C1616EJ									
		12	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊	4–72
		12	—	Micron	MT5C2516EJ									
		15	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊	4–72
		15	—	Micron	MT5C2516EJ									
		20	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊	4–72
		20	—	Micron	MT5C2516EJ									
		25	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊	4–72
		25	—	Micron	MT5C2516EJ									
		12	—	**Motorola**	MCM62996	52		PLCC				◊		3–106
		15	—	**Motorola**	MCM62996	52		PLCC				◊		3–106
		20	—	**Motorola**	MCM62996	52		PLCC				◊		3–106
		25	—	**Motorola**	MCM62996	52		PLCC				◊		3–106
	32K x 8	12	—	**Motorola**	MCM6206BA	28	300	SOJ				◊		3–9
		15	—	**Motorola**	MCM6206BA	28	300	SOJ				◊		3–9
		20	—	**Motorola**	MCM6206BA	28	300	SOJ				◊		3–9
		25	—	**Motorola**	MCM6206BA	28	300	SOJ				◊		3–9
		12	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊		3–15
		12	—	Cypress	CY7B199									
		12	—	Cypress	CY7C199									
		12	—	Hitachi	HM62832									
		12	—	Micron	MT5C2568DJ									
		12	—	Mitsubishi	M5M52B78									
		12	—	Samsung	KM68B257									
		15	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊		3–15
		15	—	Cypress	CY7B199									
		15	—	Cypress	CY7C199									
		15	—	Hitachi	HM62832									
		15	—	IDT	IDT71256									
		15	—	IDT	IDT71256SA									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K (cont.)	32K x 8 (cont.)	15	—	Micron	MT5C2568									
		15	—	Mitsubishi	M5M5278									
		15	—	NEC	µPD43258A									
		15	—	Quality	QS83280									
		15	—	Samsung	KM68B257									
		15	—	Sony	CXK58258A									
		20	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊		3–15
		20	—	Cypress	CY7B199									
		20	—	Cypress	CY7C199									
		20	—	Hitachi	HM62832									
		20	—	IDT	IDT71256									
		20	—	IDT	IDT71256SA									
		20	—	Micron	MT5C2568									
		20	—	Mitsubishi	M5M5278									
		20	—	NEC	µPD43258A									
		20	—	Performance	P41256									
		20	—	Quality	QS83280									
		20	—	Samsung	KM68257									
		20	—	Sharp	LH52258A									
		20	—	Sony	CXK58258									
		20	—	Toshiba	TC55328									
		25	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊		3–15
		25	—	Cypress	CY7C199									
		25	—	Hitachi	HM62832									
		25	—	IDT	IDT71256									
		25	—	Micron	MT5C2568									
		25	—	Mitsubishi	M5M5278									
		25	—	NEC	µPD43258									
		25	—	Performance	P41256									
		25	—	Quality	QS83280									
		25	—	Samsung	KM68257									
		25	—	Sharp	LH52258A									
		25	—	Sony	CXK58258A									
		25	—	Toshiba	TC55328									
		15	—	**Motorola**	MCM6306D	28	300	SOJ				◊		3–112
		20	—	**Motorola**	MCM6306D	28	300	SOJ				◊		3–112
		25	—	**Motorola**	MCM6306D	28	300	SOJ				◊		3–112

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K (cont.)	**32K x 8 (cont.)**	8	—	**Motorola**	MCM6706B	28	300	SOJ				◊		2–21
		8	—	Samsung	KM68B261									
		10	—	**Motorola**	MCM6706B	28	300	SOJ				◊		2–21
		10	—	Cypress	CY7B199									
		10	—	Hitachi	HM67832									
		10	—	IDT	IDT71B256SA									
		10	—	Mitsubishi	M5M52B78									
		10	—	Paradigm	PDM41256									
		10	—	Samsung	KM68B257									
		10	—	Toshiba	TC55B328									
		12	—	**Motorola**	MCM6706B	28	300	SOJ				◊		2–21
		6	—	**Motorola**	MCM6706BR	32	300	SOJ	◊			◊		2–27
		6	—	Cypress	CY7B1099									
		6	—	NEC	µPD46258LA									
		7	—	**Motorola**	MCM6706BR	32	300	SOJ	◊			◊		2–27
		7	—	NEC	µPD46258LA									
		7	—	Samsung	KM68B261									
		8	—	**Motorola**	MCM6706BR	32	300	SOJ	◊			◊		2–27
		8	—	Cypress	CY7B1099									
		8	—	NEC	µPD46258LA									
		8	—	Samsung	KM68B261									
		5	—	**Motorola**	MCM6706CR	32	300	SOJ	◊			◊		2–33
		5.5	—	**Motorola**	MCM6706CR	32	300	SOJ	◊			◊		2–33
	32K x 9	15	—	**Motorola**	MCM6205D	32	300	SOJ				◊		3–3
		15	—	Cypress	CY7C188							◊		
		15	—	Mitsubishi	M5M5279									
		15	—	NEC	µPD43259									
		15	—	Sony	CXK59288									
		15	—	Toshiba	TC55329									
		20	—	**Motorola**	MCM6205D	32	300	SOJ				◊		3–3
		20	—	Cypress	CY7C188									
		20	—	Mitsubishi	M5M5279									
		20	—	NEC	µPD43259									
		20	—	Sony	CXK59288									
		20	—	Toshiba	TC55329									
		25	—	**Motorola**	MCM6205D	32	300	SOJ				◊		3–3
		25	—	Cypress	CY7C188									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K (cont.)	32K x 9 (cont.)	25	—	Fujitsu	MB8299									
		25	—	Mitsubishi	M5M5279									
		25	—	NEC	μPD43259									
		25	—	Sony	CXK59288									
		25	—	Toshiba	TC55329									
		10	—	**Motorola**	MCM6705A	32	300	SOJ						2–3
		10	—	IDT	IDT71B259									
		10	—	Mitsubishi	M5M52B79P									
		10	—	Toshiba	TC55B329P									
		12	—	**Motorola**	MCM6705A	32	300	SOJ						2–3
		12	—	Cypress	CY7C188									
		12	—	IDT	IDT71B259									
		12	—	Mitsubishi	M5M52B79P									
		12	—	Toshiba	TC55B329P									
		15	—	**Motorola**	MCM62110	52		PLCC		◊	◊	◊	◊	4–10
		17	—	**Motorola**	MCM62110	52		PLCC		◊	◊	◊	◊	4–10
		20	—	**Motorola**	MCM62110	52		PLCC		◊	◊	◊	◊	4–10
		11	15	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊	5–3
		11	15	IC Works	ICW79B586									
		11	15	Paradigm	PDM44259									
		11	15	Samsung	KM79C86									
		12	20	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊	5–3
		12	—	IC Works	ICW79B586									
		12	—	Samsung	KM79C86									
		14	20	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊	5–3
		14	—	Cypress	CY7B173–14C									
		14	—	Samsung	KM79C86									
		19	25	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊	5–3
		19	—	Cypress	CY7B173–18C									
		19	—	Samsung	KM79C86									
		19	—	SGS-Thomson	MK62486Q19									
		11	15	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊	5–12
		11	—	Paradigm	PDM44659									
		12	20	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊	5–12
		14	2	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊	5–12
		14	—	Cypress	CY7B174–14C									
		19	25	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊	5–12

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K (cont.)	32K x 9 (cont.)	19	—	Cypress	CY7B174–18C									
		19	—	SGS-Thomson	MK62940Q19									
	64K x 4	12	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ						3–21
		12	—	Cypress	CY7B194									
		12	—	Cypress	CY7C194									
		12	—	Micron	MT5C2564									
		15	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ						3–21
		15	—	Cypress	CY7B194									
		15	—	Cypress	CY7C194									
		15	—	Micron	MT5C2564									
		15	—	Mitsubishi	M5M5258									
		15	—	NEC	µPD43254B									
		15	—	Quality	QS86440									
		20	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ						3–21
		20	—	Cypress	CY7B194									
		20	—	Cypress	CY7C194									
		20	—	Micron	MT5C2564									
		20	—	Mitsubishi	M5M5258									
		20	—	NEC	µPD43254B									
		20	—	Performance	P4C1258									
		20	—	Quality	QS86440									
		20	—	Toshiba	TC55464									
		25	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ						3–21
		25	—	Cypress	CY7C194									
		25	—	Fujitsu	MB81C84A									
		25	—	Hitachi	HM6208									
		25	—	Micron	MT5C2564									
		25	—	Mitsubishi	M5M5258									
		25	—	NEC	µPD43254B									
		25	—	Performance	P41258									
		25	—	SGS-Thompson	IMS1820D3									
		25	—	Sharp	LH52252									
		25	—	Toshiba	TC55464									
		12	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊		3–27
		12	—	Cypress	CY7B195									
		12	—	Cypress	CY7B196									
		12	—	Cypress	CY7C194									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K (cont.)	64K x 4 (cont.)	12	—	Cypress	CY7C195									
		12	—	Cypress	CY7C196									
		12	—	Micron	MT5C2565									
		15	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊		3–27
		15	—	Cypress	CY7B195									
		15	—	Cypress	CY7B196									
		15	—	Cypress	CY7C194									
		15	—	Cypress	CY7C195									
		15	—	Cypress	CY7C196									
		15	—	IDT	IDT61298SA									
		15	—	Micron	MT5C2565									
		15	—	Mitsubishi	M5M5259									
		15	—	NEC	µPD43253B									
		15	—	Quality	QS86446									
		20	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊		3–27
		20	—	Cypress	CY7B195									
		20	—	Cypress	CY7B196									
		20	—	Cypress	CY7C194									
		20	—	Cypress	CY7C195									
		20	—	Cypress	CY7C196									
		20	—	IDT	IDT61298SA									
		20	—	Micron	MT5C2565									
		20	—	Mitsubishi	M5M5259									
		20	—	NEC	µPD43253B									
		20	—	Performance	P4C1298									
		20	—	Quality	QS86446									
		20	—	Samsung	KM64258B									
		20	—	Sharp	LH52253									
		20	—	Toshiba	TC55465									
		25	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊		3–27
		25	—	Cypress	CY7C195									
		25	—	Cypress	CY7C196									
		25	—	IDT	IDT61298SA									
		25	—	Micron	MT5C2565									
		25	—	Mitsubishi	M5M5259									
		25	—	NEC	µPD43253B									
		25	—	Performance	P4C1298									

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
256K (cont.)	64K x 4 (cont.)	25	—	Quality	QS86446									
		25	—	Samsung	KM64258B									
		25	—	Sharp	LH52253									
		25	—	Toshiba	TC55465									
		8	—	**Motorola**	MCM6709B	28	300	SOJ				◊		2–64
		8	—	Samsung	KM64B258A									
		10	—	**Motorola**	MCM6709B	28	300	SOJ				◊		2–64
		10	—	Hitachi	HM6709SH									
		10	—	IDT	IDT61B298SA									
		10	—	Micron	MT5C2565DJ									
		10	—	Paradigm	PDM41298									
		10	—	Paradigm	PDM41251									
		10	—	Samsung	KM64B258A									
		10	—	Toshiba	TC55B465									
		12	—	**Motorola**	MCM6709B	28	300	SOJ				◊		2–64
		12	—	Hitachi	HM6709SH									
		12	—	Samsung	KM64B258A									
		12	—	Toshiba	TC55B465									
		6	—	**Motorola**	MCM6709BR	28	300	SOJ	◊			◊		2–70
		6	—	Cypress	CY7C1094									
		6	—	Cypress	CY7C1095									
		6	—	Cypress	CY7C1096									
		6	—	Samsung	KM68257									
		7	—	**Motorola**	MCM6709BR	28	300	SOJ	◊			◊		2–70
		8	—	**Motorola**	MCM6709BR	28	300	SOJ	◊			◊		2–70
		8	—	Cypress	CY7C1094									
		8	—	Cypress	CY7C1095									
		8	—	Samsung	KM64B258A									
192K	8K x 24	20	—	**Motorola**	MCM56824A	52, 86		PLCC, PBGA				◊	◊	4–3
		25	—	**Motorola**	MCM56824A	52, 86		PLCC, PBGA				◊	◊	4–3
		35	—	**Motorola**	MCM56824A	52, 86		PLCC, PBGA				◊	◊	4–3
128K	8K x 16	10	—	**Motorola**	MCM67T316	44		PLCC		◊			◊	4–83
		12	20	**Motorola**	MCM67T316	44		PLCC		◊			◊	4–83
		8	—	Cypress	CY7C1096									
64K	8K x 8	15.5	—	**Motorola**	MCM62X308	28	300	SOJ		◊			◊	4–20
		17	—	**Motorola**	MCM62X308	28	300	SOJ		◊			◊	4–20
		17	—	**Motorola**	MCM62Y308	32	300	SOJ		◊			◊	4–39

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function	Page No.
48K	4K x 12	—	18	Motorola	MCM62973A	44		PLCC		◊			◊	4–60
		—	20	Motorola	MCM62973A	44		PLCC		◊		◊	◊	4–60
	4K x 10	—	30	Motorola	MCM62963A	44		PLCC		◊			◊	4–55

Asynchronous BiCMOS Fast SRAMs

2

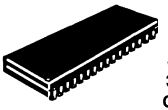
3.3 V Supply

5 V Supply and ECL

2

MCM6705A

32K x 9 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857–02

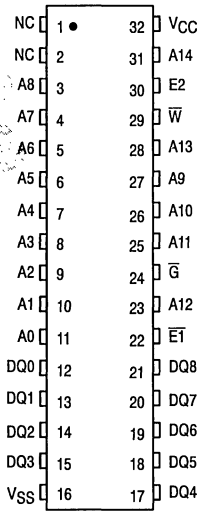
The MCM6705A is a 294,912 bit static random access memory organized as 32,768 words of 9 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

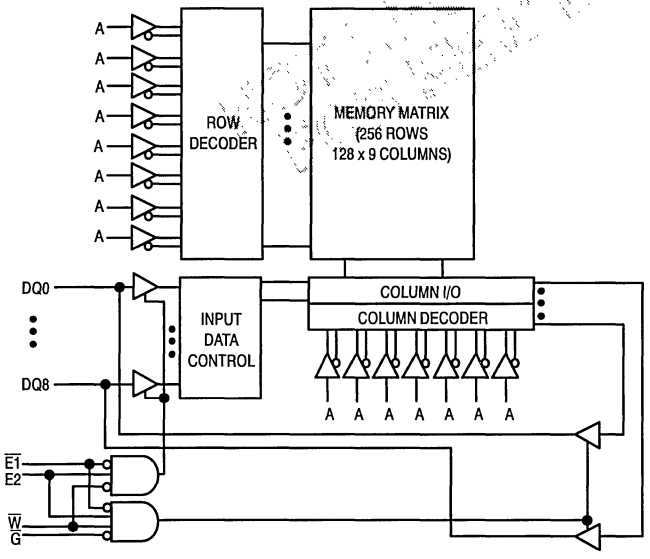
The MCM6705A is available in a 300 mil, 32 lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6705A–10 = 10 ns
  MCM6705A–12 = 12 ns

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

REV 4
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature – Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
**V_{IL} (min) = –0.5 V dc @ 30.0 mA; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6705A–10	MCM6705A–12	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = max, f = f_{max})	I_{SB1}	125	120	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E1}$ ≥ V_{CC} – 0.2 V, or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	55	55	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

2

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1, 2, and 3)

Parameter	Symbol	MCM6705A–10		MCM6705A–12		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	ns	4
Address Access Time	t_{AVQV}	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	ns	5, 6, 7
Chip Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).
9. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

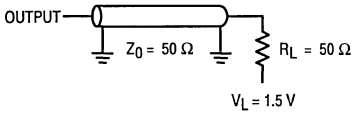


Figure 1A

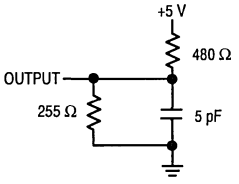
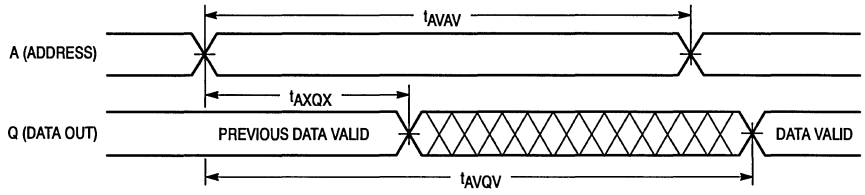


Figure 1B

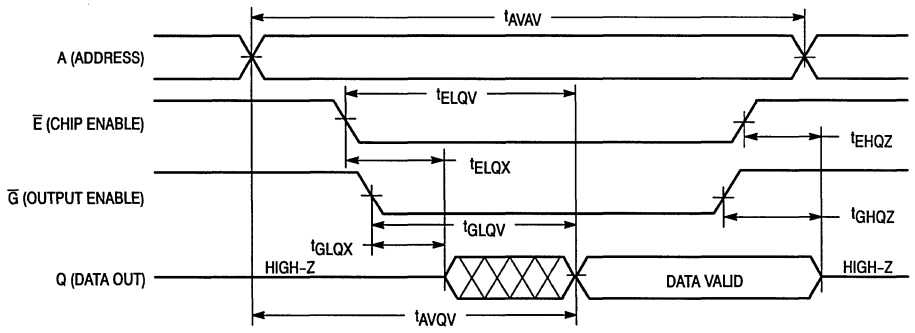
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 9)

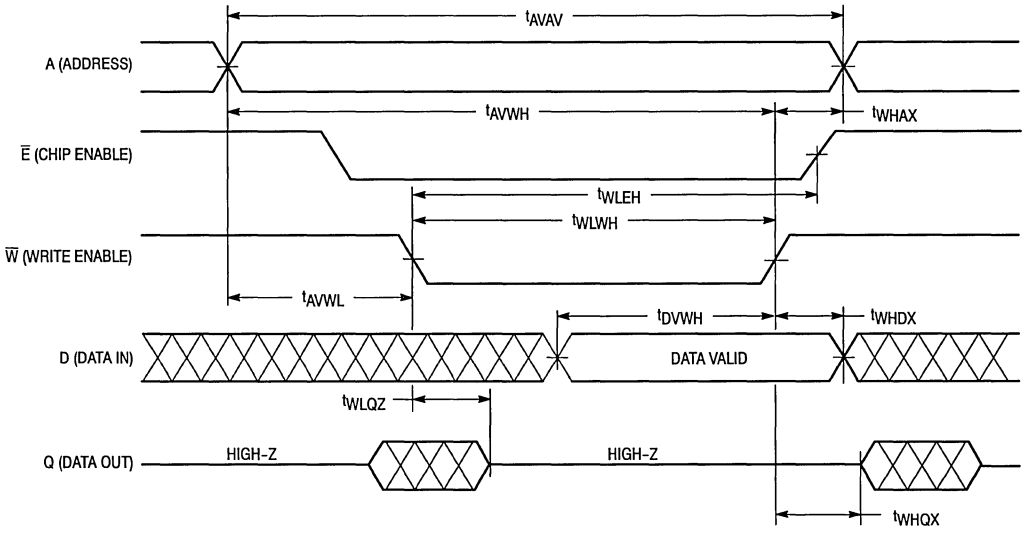


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6705A–10		MCM6705A–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. Parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

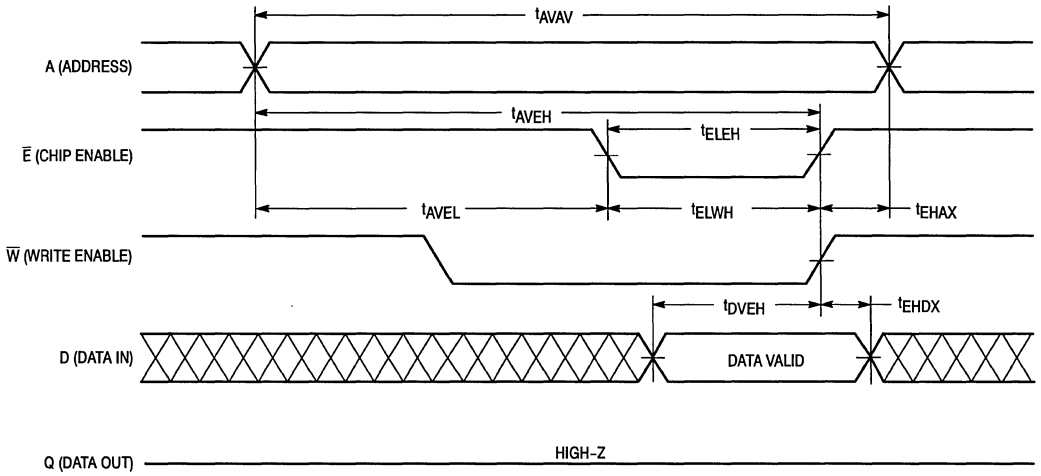


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

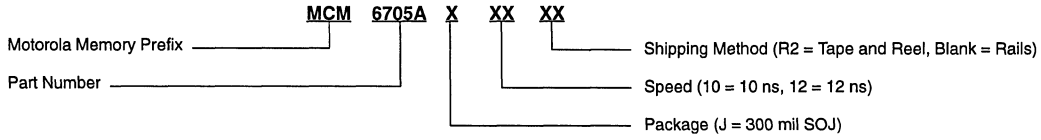
Parameter	Symbol	MCM6705A–10		MCM6705A–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	8	—	9	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6705AJ10 MCM6705AJ10R2
MCM6705AJ12 MCM6705AJ12R2

MCM6706A

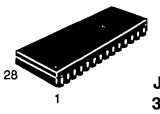
32K x 8 Bit Static Random Access Memory

The MCM6706A is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6706A is available in a 300 mil, 28–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706A–8 = 8 ns
  MCM6706A–10 = 10 ns
  MCM6706A–12 = 12 ns

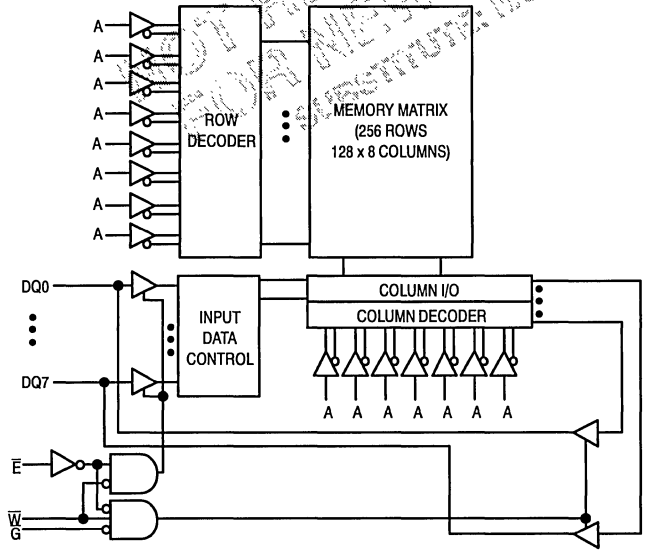


J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT

A14	1	28	V_{CC}
A12	2	27	$\overline{W}$
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{G}$
A2	8	21	A10
A1	9	20	$\overline{E}$
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
V_{SS}	14	15	DQ3

BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground

REV 6
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
**V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706A–8	6706A–10	6706A–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	175	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	130	120	115	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	50	50	50	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

2

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	MCM6706A–8		MCM6706A–10		MCM6706A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

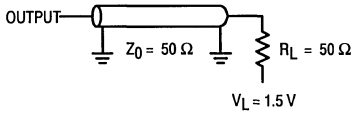


Figure 1A

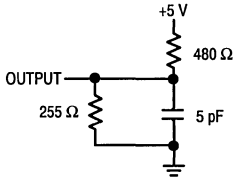
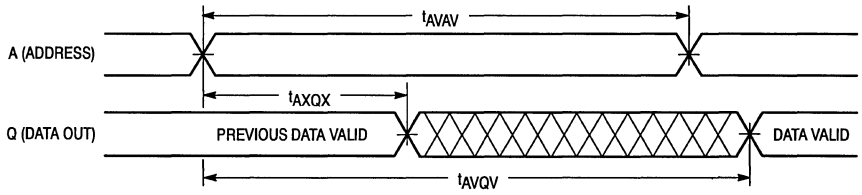


Figure 1B

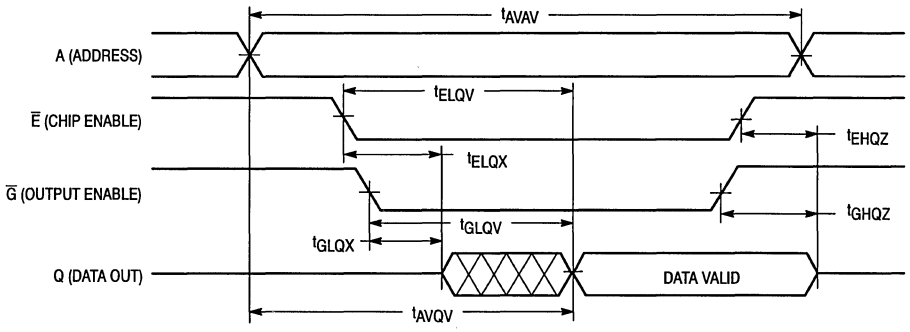
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

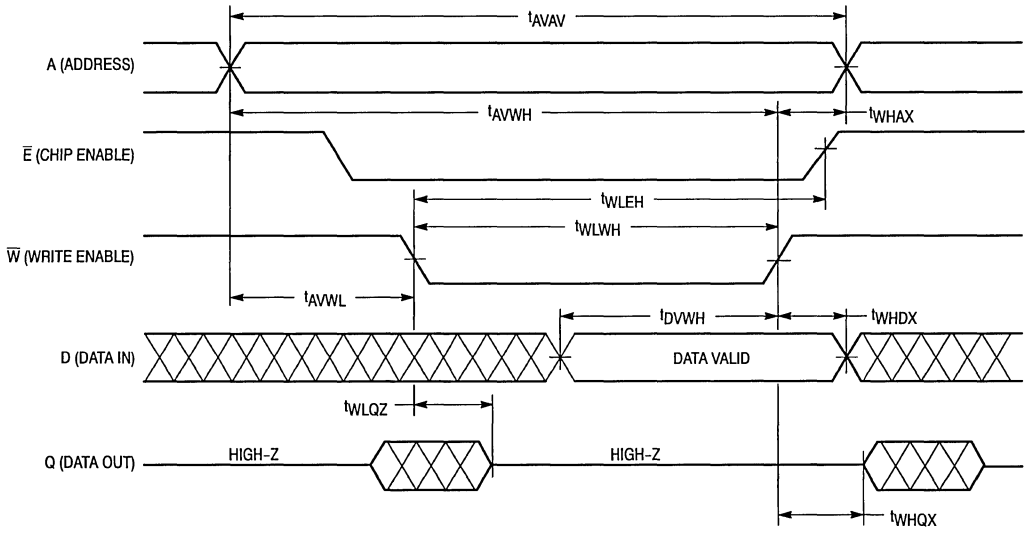


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706A–8		MCM6706A–10		MCM6706A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Wirte High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

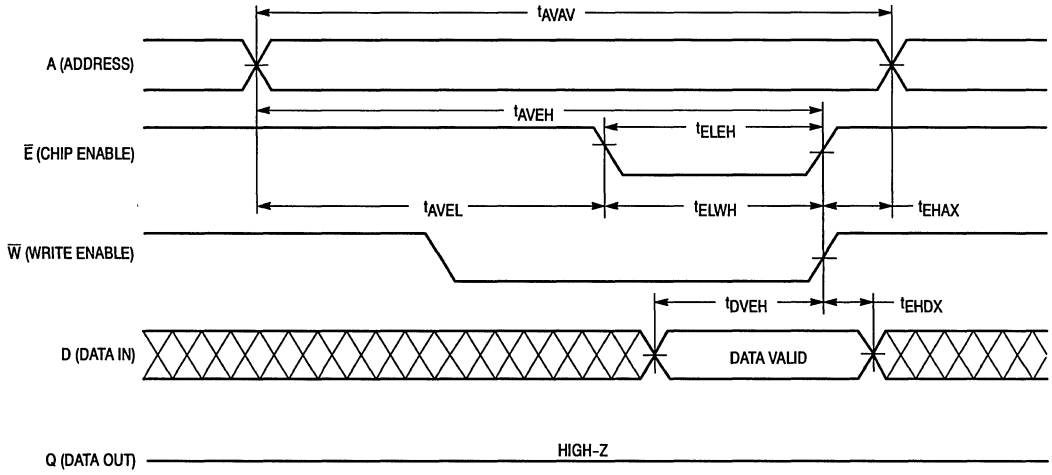


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706A–8		MCM6706A–10		MCM6706A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

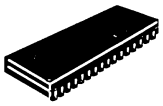
MCM 6706A X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706AJ8, MCM6706AJ10, MCM6706AJ12, MCM6706AJ8R2, MCM6706AJ10R2, MCM6706AJ12R2

MCM6706AR

32K x 8 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857–02

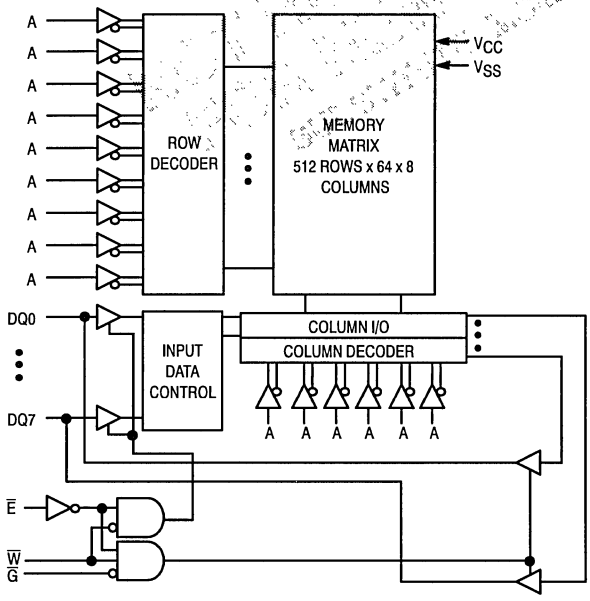
The MCM6706AR is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6706AR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 32–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706AR–6 = 6 ns
  MCM6706AR–7 = 7 ns
  MCM6706AR–8 = 8 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



PIN ASSIGNMENT

A0	1	32	NC
A1	2	31	A14
A2	3	30	A13
A3	4	29	A12
$\overline{E}$	5	28	$\overline{G}$
DQ0	6	27	DQ7
DQ1	7	26	DQ6
VCC	8	25	VSS
VSS	9	24	VCC
DQ2	10	23	DQ5
DQ3	11	22	DQ4
$\overline{W}$	12	21	A11
A4	13	20	A10
A5	14	19	A9
A6	15	18	A8
A7	16	17	NC

PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	–6	–7	–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	235	225	215	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	85	75	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

2

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	–6		–7		–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	2.5	—	2.5	—	2.5	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	0	3.5	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	0	3.5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

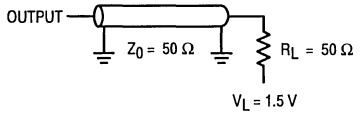


Figure 1A

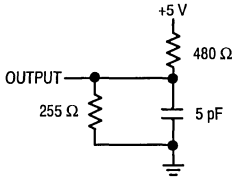
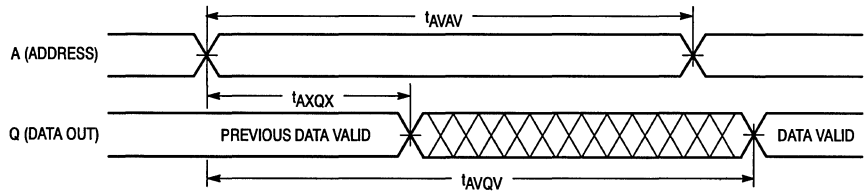


Figure 1B

TIMING LIMITS

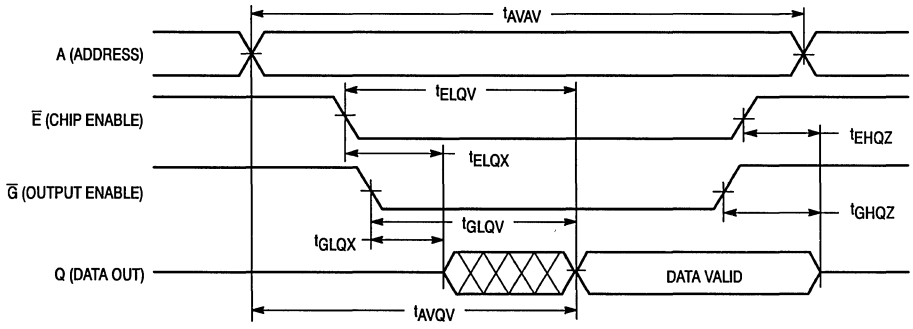
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



2

READ CYCLE 2 (See Note 8)

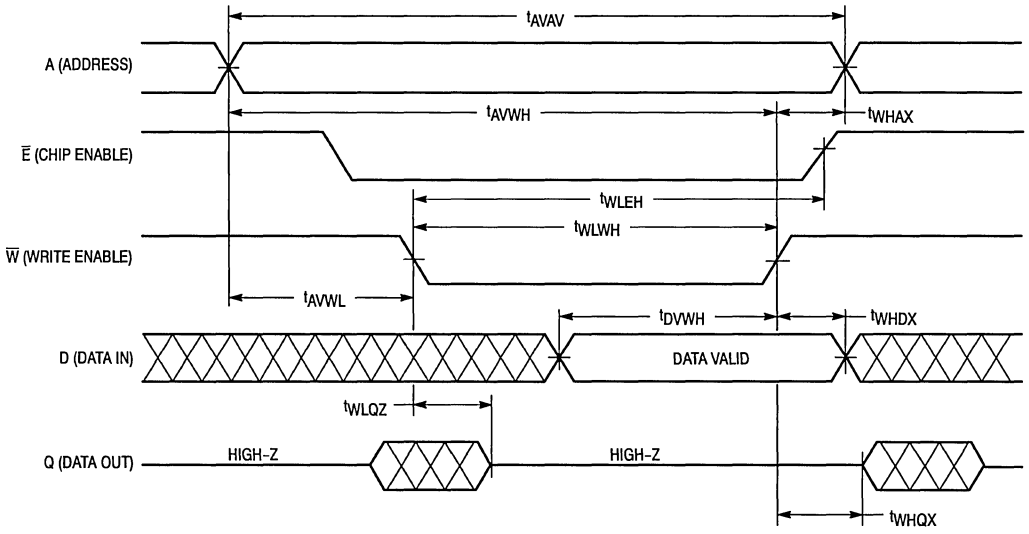


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706AR–6		MCM6706AR–7		MCM6706AR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	0	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

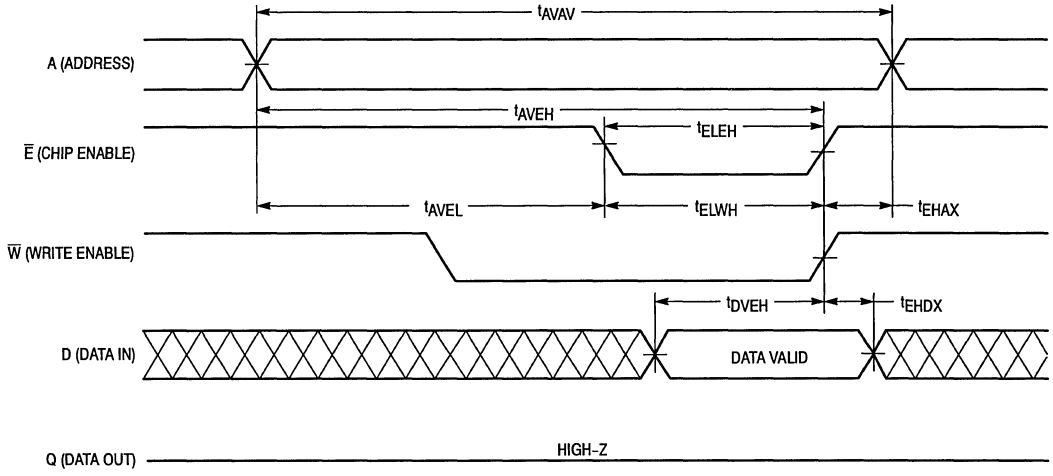


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706AR–6		MCM6706AR–7		MCM6706AR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	5	—	6	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706AR X X XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706ARJ6, MCM6706ARJ7, MCM6706ARJ8, MCM6706ARJ6R2, MCM6706ARJ7R2, MCM6706ARJ8R2

MCM6706B

Product Preview

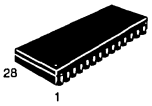
32K x 8 Bit Static Random Access Memory

The MCM6706B is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

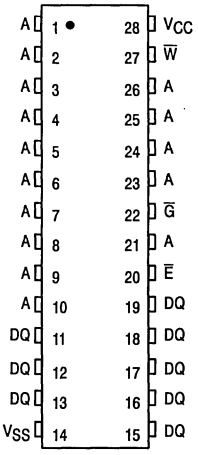
The MCM6706B is available in a 300 mil, 28–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706B–8 = 8 ns
  MCM6706B–10 = 10 ns
  MCM6706B–12 = 12 ns



J PACKAGE
300 MIL SOJ
CASE 810B–03

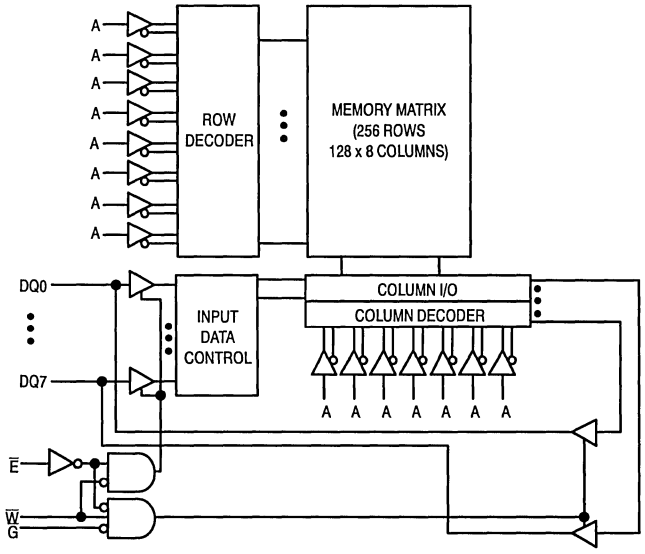
PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

4/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706B–8	6706B–10	6706B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	175	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	75	70	65	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	MCM6706B–8		MCM6706B–10		MCM6706B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

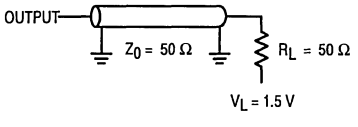


Figure 1A

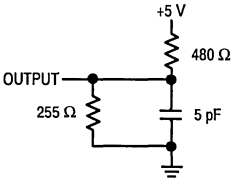
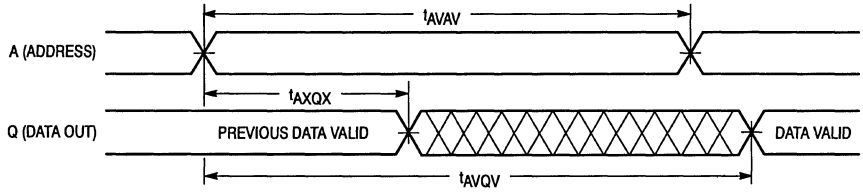


Figure 1B

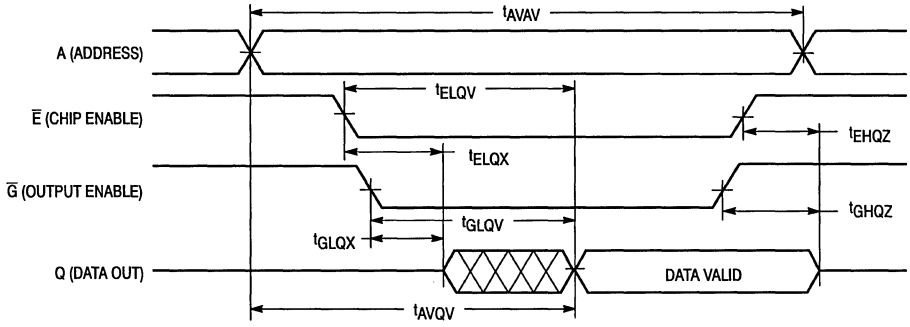
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

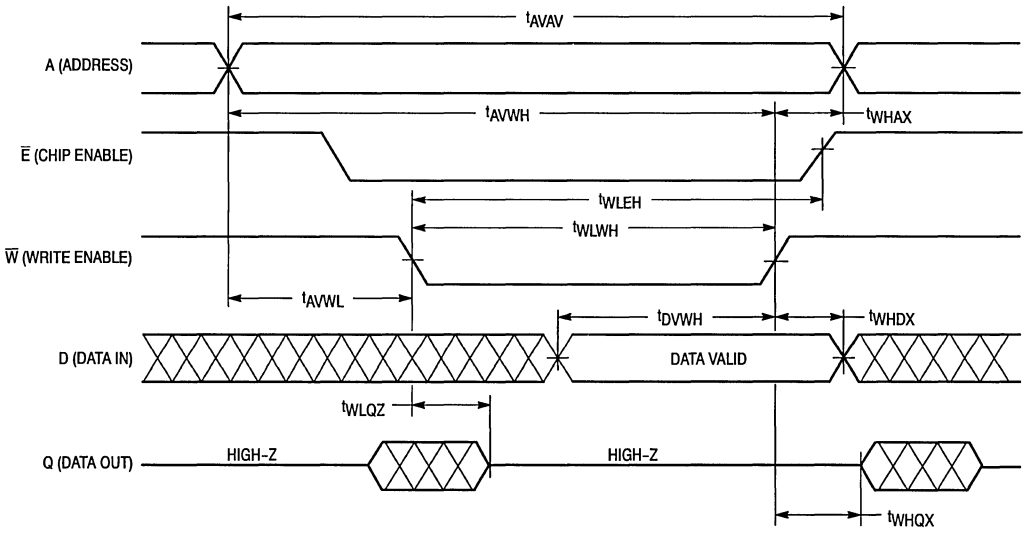


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706B–8		MCM6706B–10		MCM6706B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Wirte High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

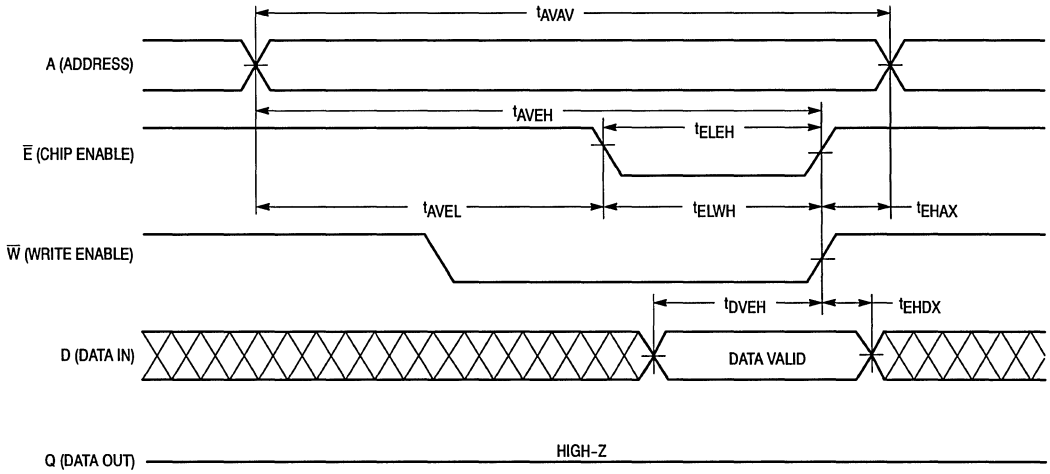


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

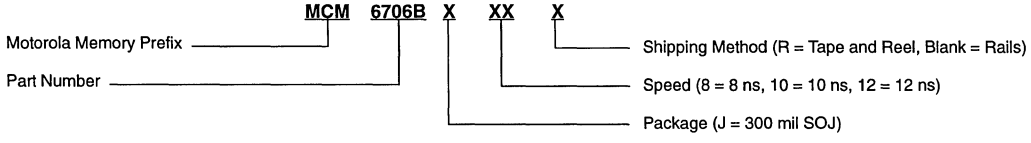
Parameter	Symbol	MCM6706B–8		MCM6706B–10		MCM6706B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

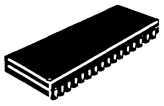


Full Part Numbers — MCM6706BJ8 MCM6706BJ8R
MCM6706BJ10 MCM6706BJ10R
MCM6706BJ12 MCM6706BJ12R

MCM6706BR

Product Preview

32K x 8 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857–02

2

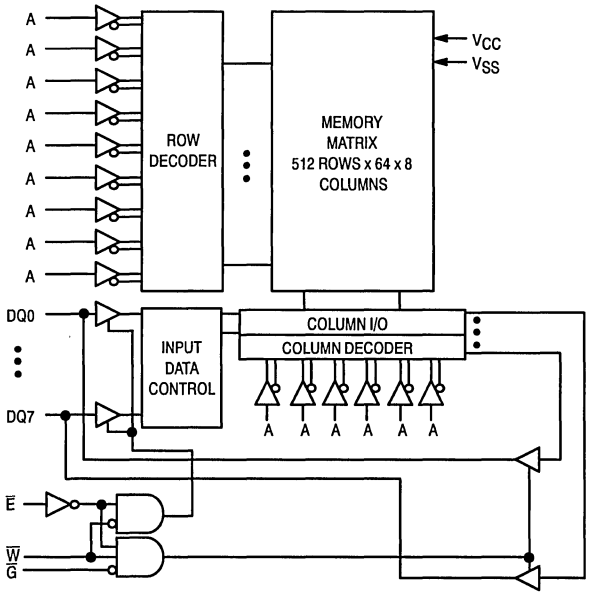
The MCM6706BR is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

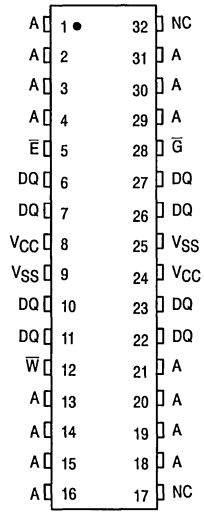
The MCM6706BR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 32–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706BR–6 = 6 ns
  MCM6706BR–7 = 7 ns
  MCM6706BR–8 = 8 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	–6	–7	–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	215	205	195	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	85	75	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	6706BR–6		6706BR–7		6706BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	0	3.5	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	0	3.5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

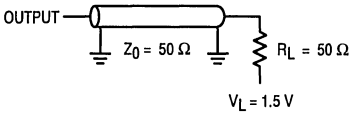


Figure 1A

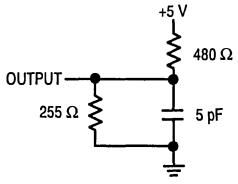
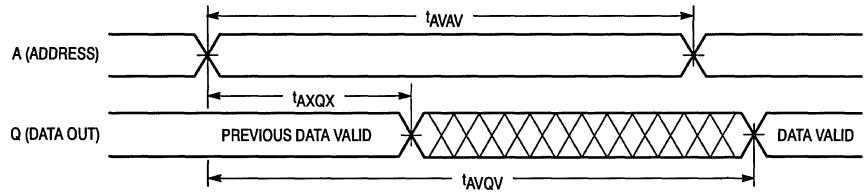


Figure 1B

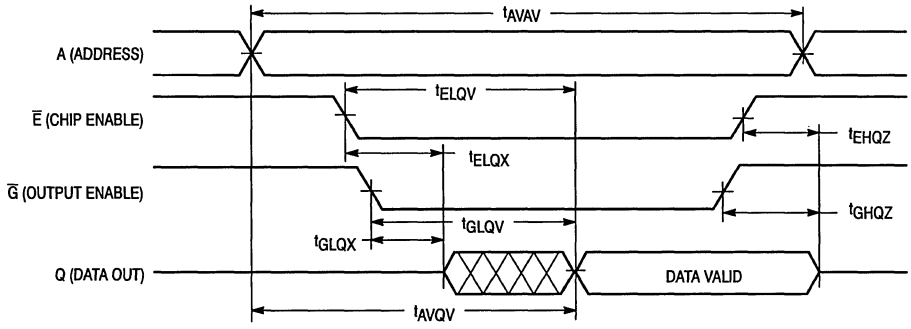
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

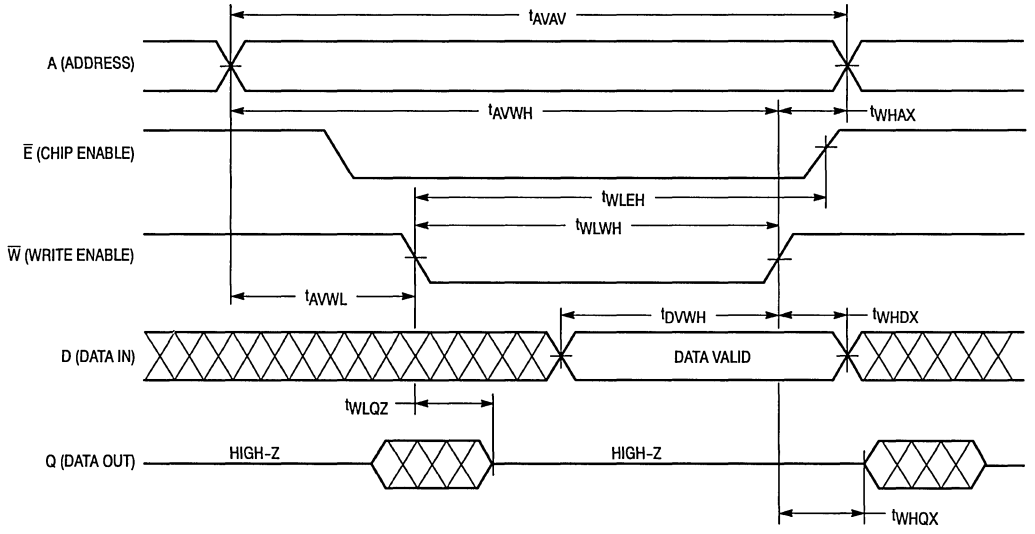


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6706BR–6		6706BR–7		6706BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	0	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

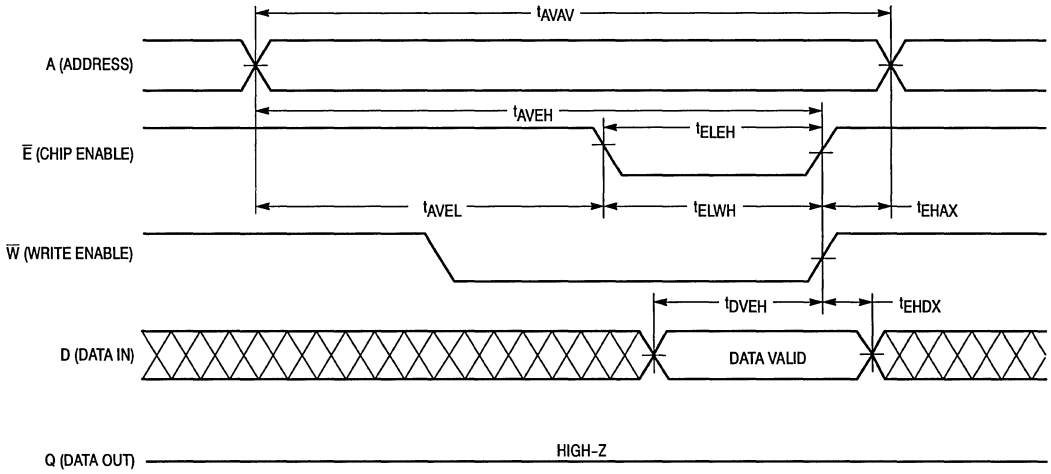


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6706BR–6		6706BR–7		6706BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	5	—	6	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706BR X X XX

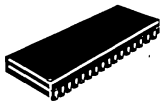
- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706BRJ6, MCM6706J7, MCM6706BRJ8, MCM6706BRJ6R, MCM6706BRJ7R, MCM6706BRJ8R

MCM6706CR

Product Preview

32K x 8 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857–02

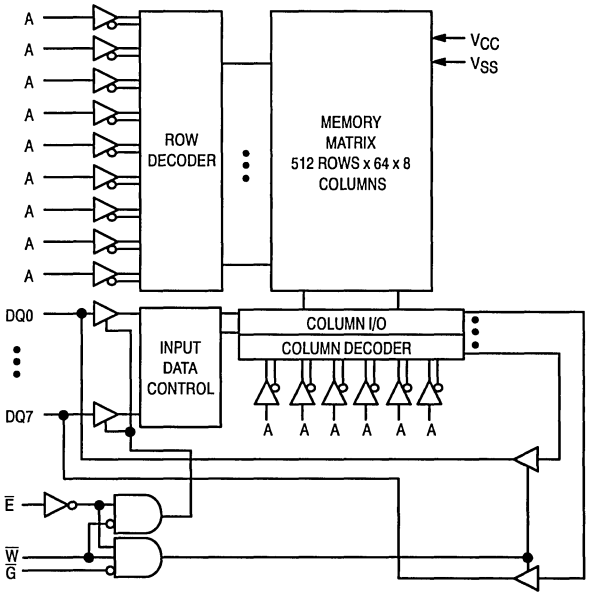
The MCM6706CR is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon–gate BiC-MOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6706CR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 32–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706CR–5 = 5 ns
  MCM6706CR–5.5 = 5.5 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



PIN ASSIGNMENT

A	1	32	NC
A	2	31	A
A	3	30	A
A	4	29	A
$\overline{E}$	5	28	$\overline{G}$
DQ	6	27	DQ
DQ	7	26	DQ
V_{CC}	8	25	V_{SS}
V_{SS}	9	24	V_{CC}
DQ	10	23	DQ
DQ	11	22	DQ
$\overline{W}$	12	21	A
A	13	20	A
A	14	19	A
A	15	18	A
A	16	17	NC

PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6706CR–5	MCM6706CR–5.5	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	240	235	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	120	115	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	30	30	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

2

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	MCM6706CR–5		MCM6706CR–5.5		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	5	—	5.5	—	ns	3
Address Access Time	t_{AVQV}	—	5	—	5.5	ns	
Chip Enable Access Time	t_{ELQV}	—	5	—	5.5	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	2.0	—	2.0	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

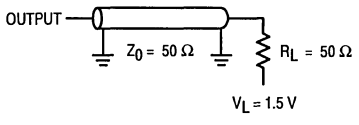


Figure 1A

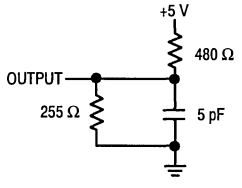
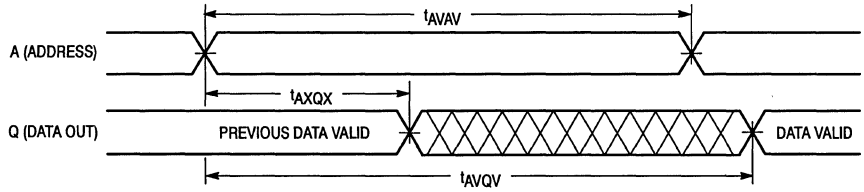


Figure 1B

TIMING LIMITS

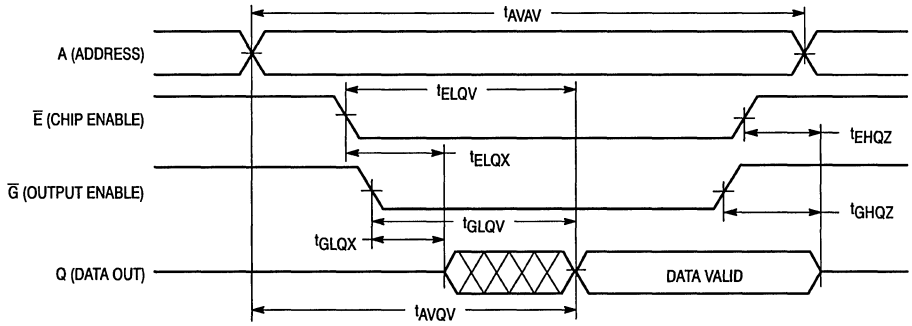
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



2

READ CYCLE 2 (See Note 8)

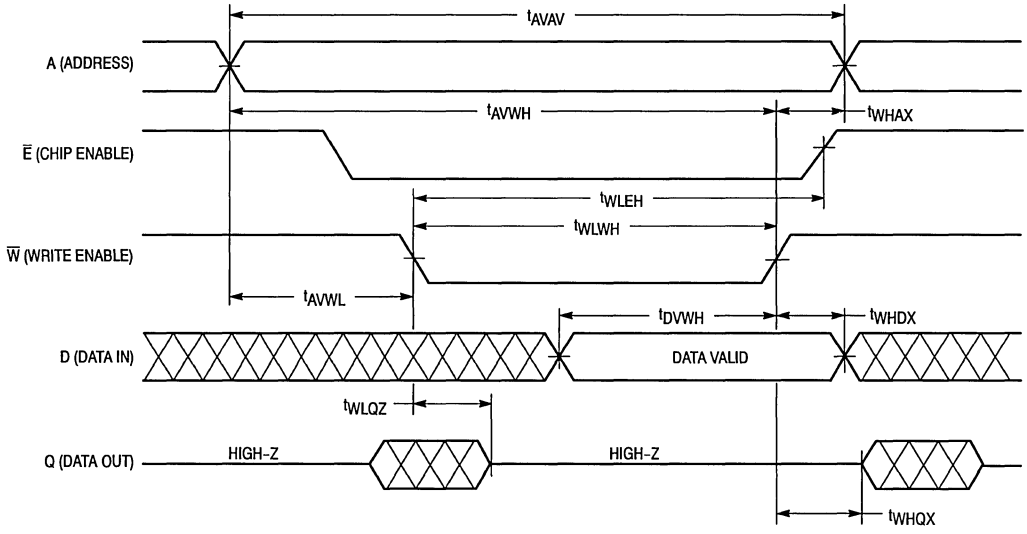


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706CR–5		MCM6706CR–5.5		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	5	—	5.5	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	6	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	6	—	6	—	ns	
Data Valid to End of Write	t_{DVWH}	3.5	—	3	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

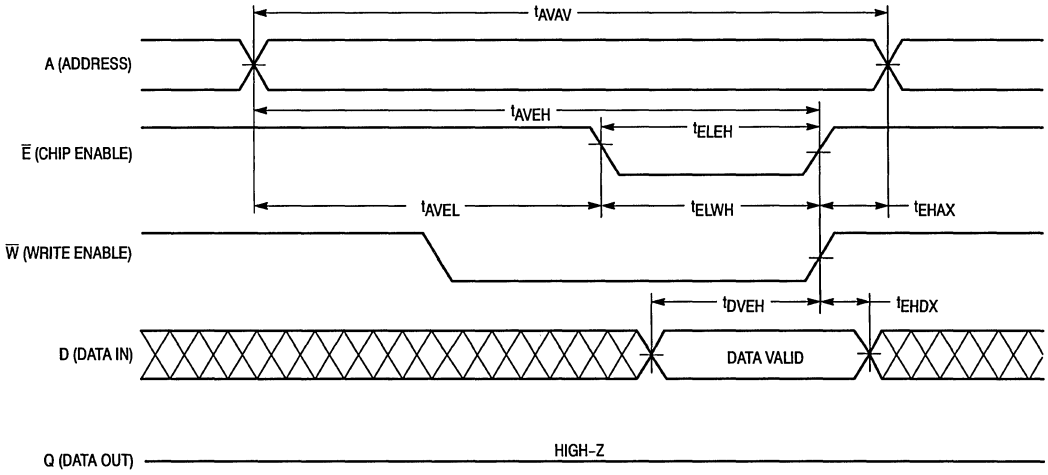


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706CR–5		MCM6706CR–5.5		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	5	—	5.5	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	5	—	5.5	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	5	—	5.5	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706CR X X X

- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (5 = 5 ns, 5.5 = 5.5 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706CRJ5, MCM6706CRJ5R, MCM6706CRJ5.5, MCM6706CRJ5.5R

MCM6706R

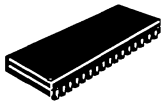
32K x 8 Bit Static Random Access Memory

The MCM6706R is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

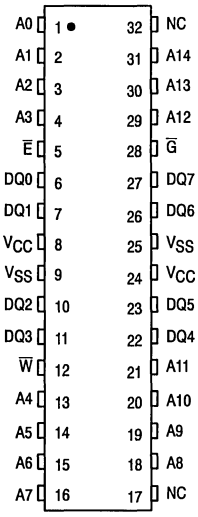
The MCM6706R meets JEDEC standards and is available in a revolutionary pinout 300 mil, 32–lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706R–6 = 6 ns
  MCM6706R–7 = 7 ns
  MCM6706R–8 = 8 ns
- Center Power and I/O Pins for Reduced Noise

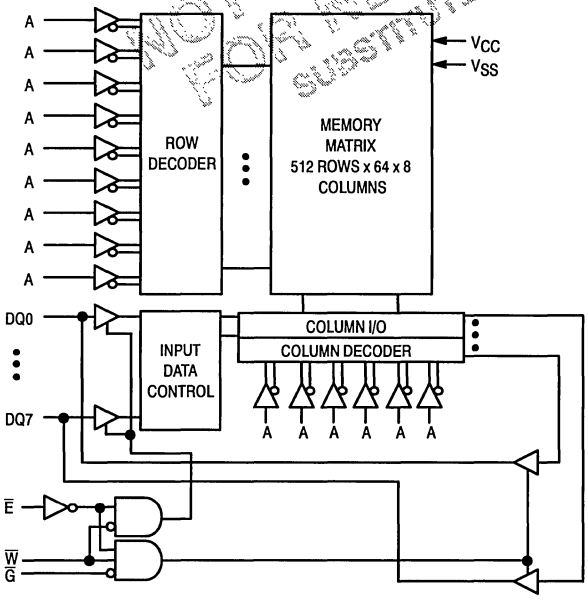


J PACKAGE
300 MIL SOJ
CASE 857–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706R–6	6706R–7	6706R–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	205	200	195	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	90	85	mA	1, 2. 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	MCM6706R–6		MCM6706R–7		MCM6706R–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4 ,5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	0	4	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	0	4	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

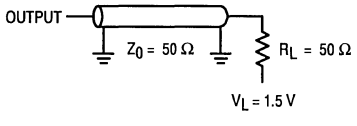


Figure 1A

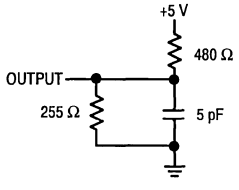
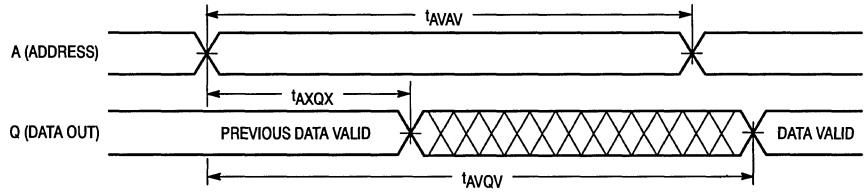


Figure 1B

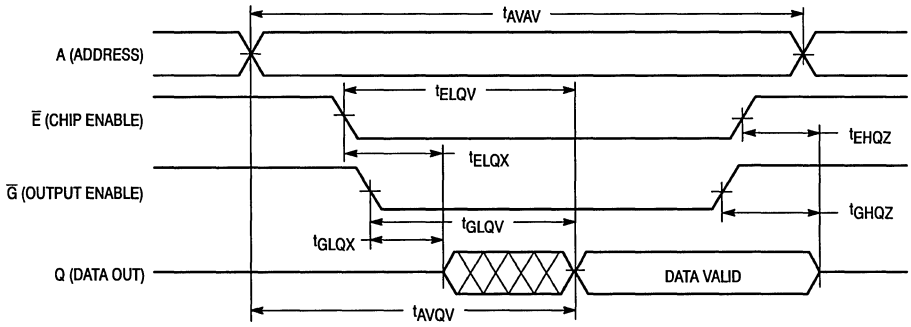
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

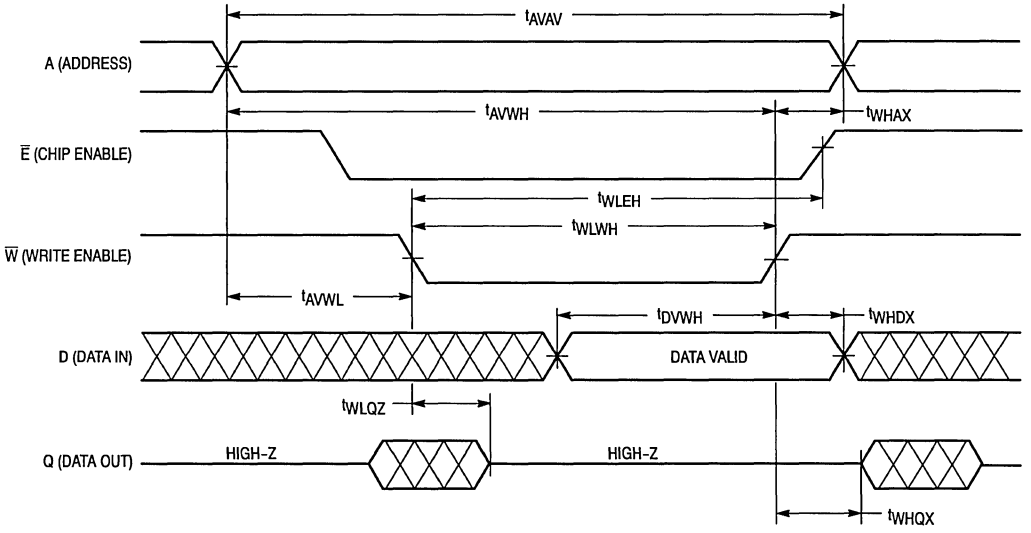


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706R–6		MCM6706R–7		MCM6706R–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	0	4	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

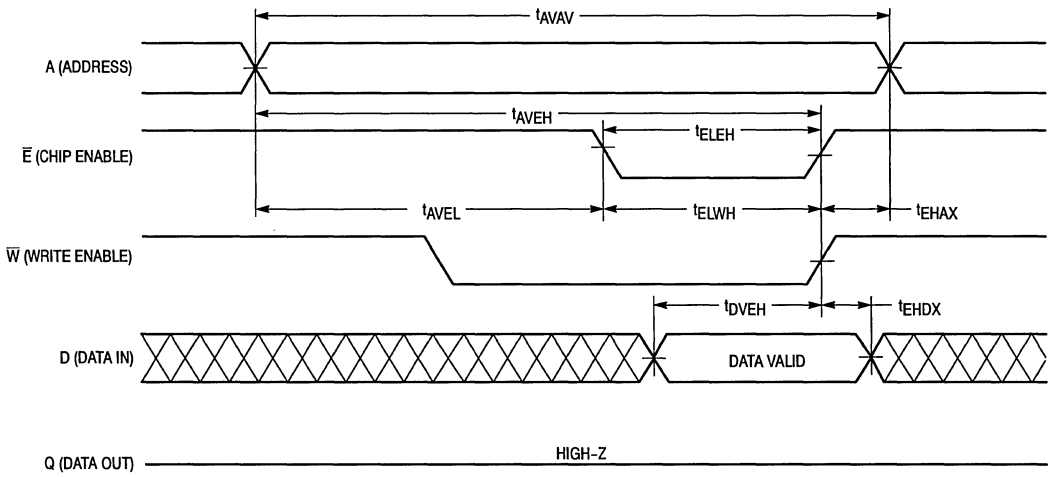


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6706R–6		MCM6706R–7		MCM6706R–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	5	—	6	—	7	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706R X XX XX

- MCM — Motorola Memory Prefix
- 6706R — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6706J6, MCM6706RJ7, MCM6706RJ8, MCM6706RJ6R2, MCM6706RJ7R2, MCM6706RJ8R2

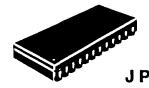
MCM6708A

64K x 4 Bit Static RAM

The MCM6708A is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

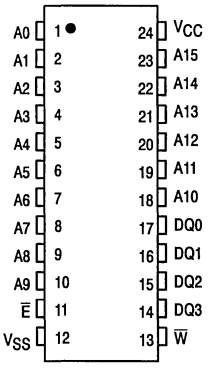
The MCM6708A is available in a 300 mil, 24 lead plastic surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times:
  MCM6708A–8 = 8 ns
  MCM6708A–10 = 10 ns
  MCM6708A–12 = 12 ns

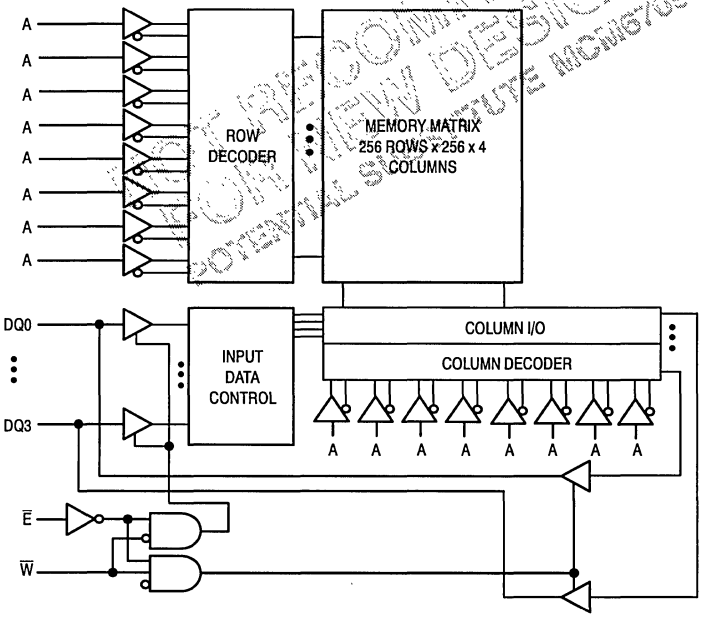


J PACKAGE
300 MIL SOJ
CASE 810A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
W	Write Enable
E	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6708A–8	MCM6708A–10	MCM6708A–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	185	175	165	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	120	110	105	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	50	50	50	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	5	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6708A–8		MCM6708A–10		MCM6708A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	4.5	0	5	0	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

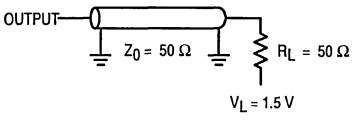


Figure 1A

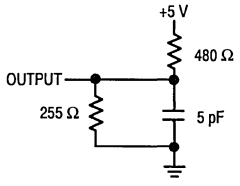
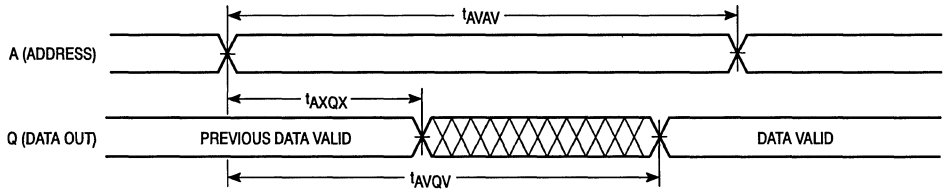


Figure 1B

TIMING LIMITS

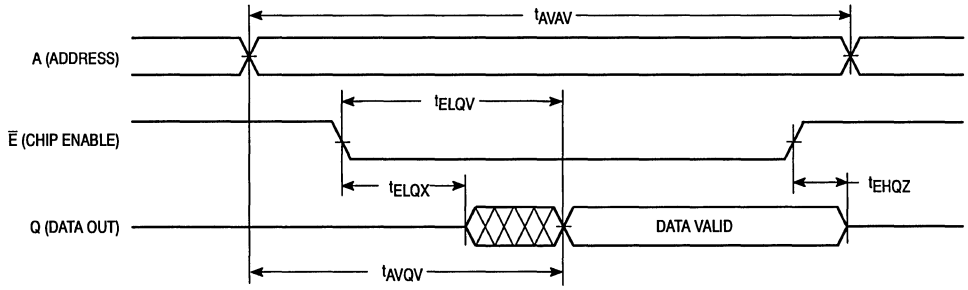
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

READ CYCLE 2 (See Note)



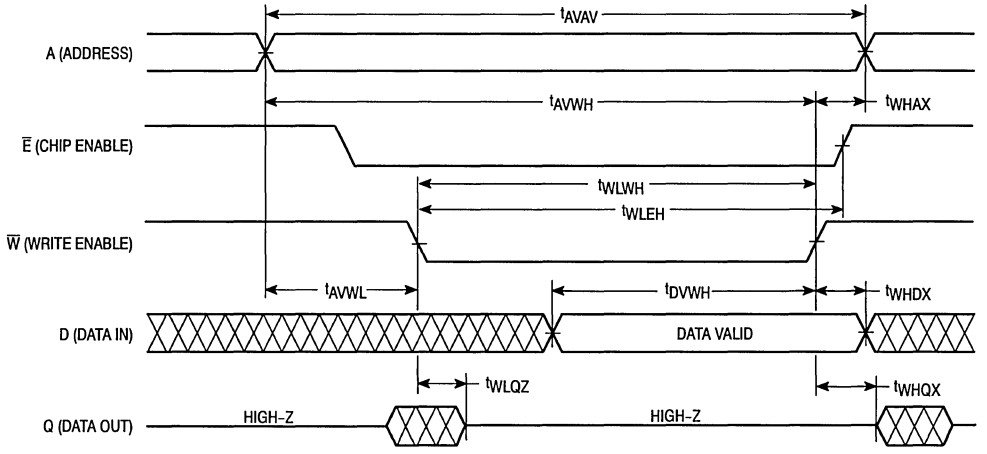
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6708A–8		MCM6708A–10		MCM6708A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

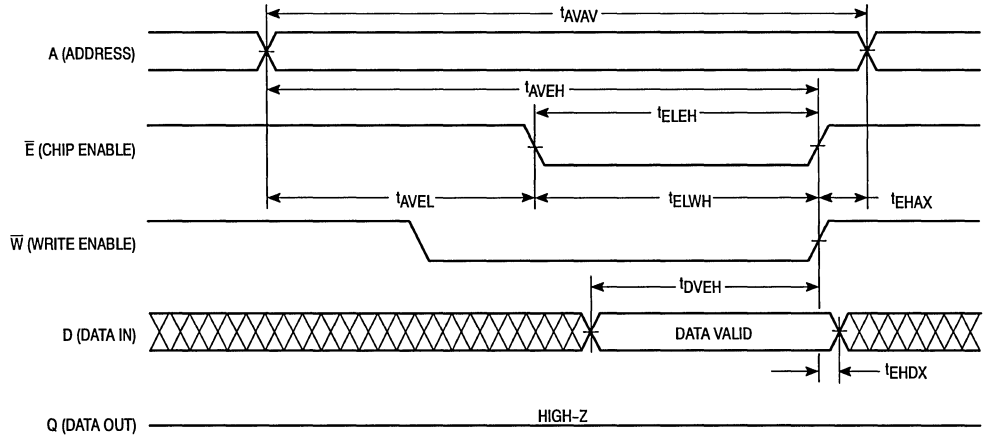


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

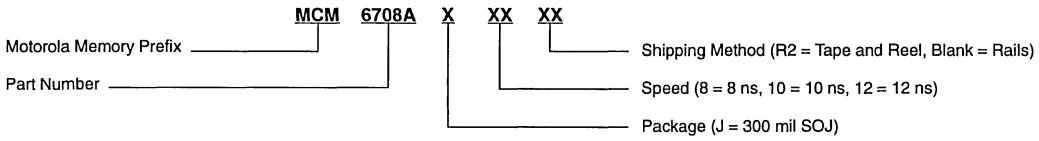
Parameter	Symbol	MCM6708A–8		MCM6708A–10		MCM6708A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6708AJ8 MCM6708AJ8R2
MCM6708AJ10 MCM6708AJ10R2
MCM6708AJ12 MCM6708AJ12R2

2

MCM6709A

64K x 4 Bit Static RAM

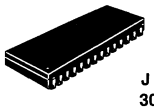
2

The MCM6709A is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) provides increased system flexibility and eliminates bus contention problems.

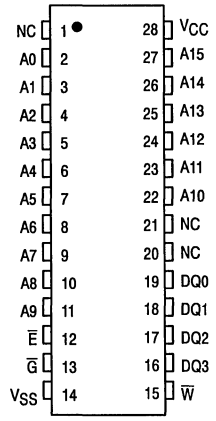
The MCM6709A is available in a 300 mil, 28 lead plastic surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times:
  MCM6709A–8 = 8 ns
  MCM6709A–10 = 10 ns
  MCM6709A–12 = 12 ns

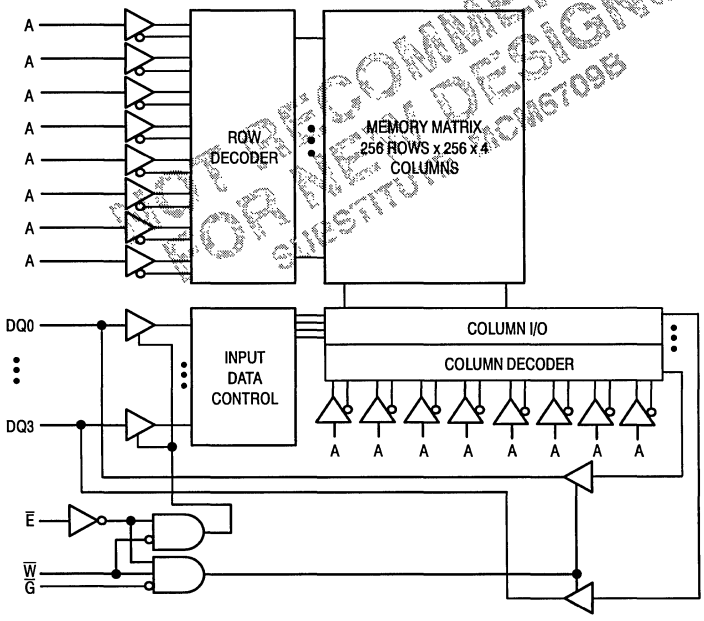


J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709A–8	MCM6709A–10	MCM6709A–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	185	175	165	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	120	110	105	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	50	50	50	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	5	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709A–8		MCM6709A–10		MCM6709A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

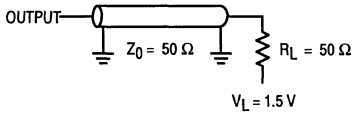


Figure 1A

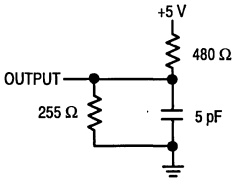
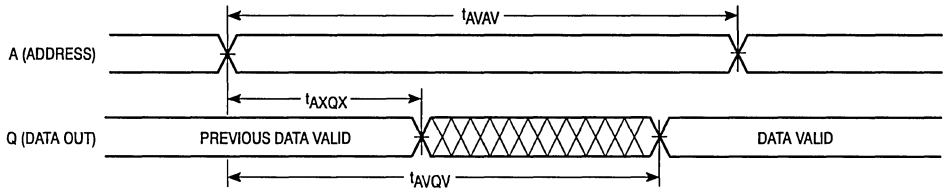


Figure 1B

TIMING LIMITS

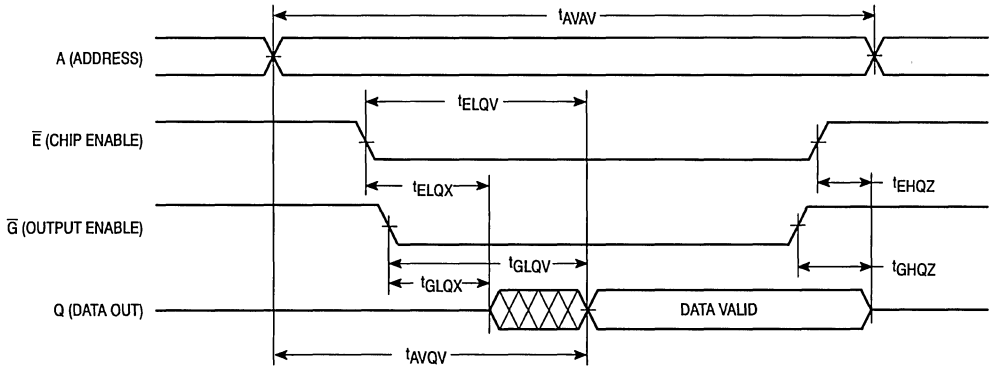
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



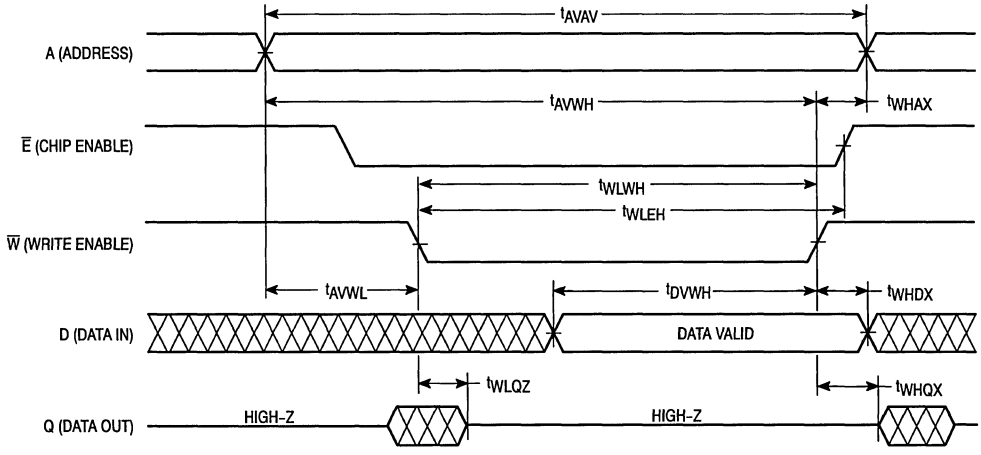
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709A–8		MCM6709A–10		MCM6709A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

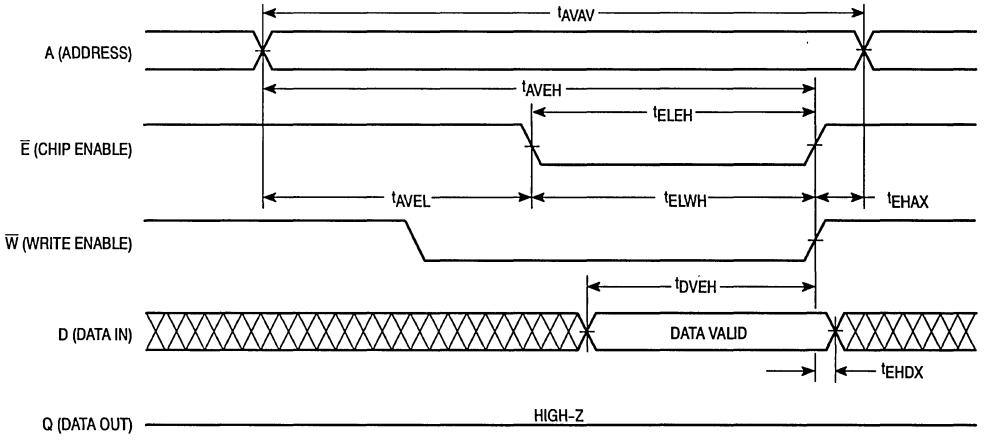


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709A–8		MCM6709A–10		MCM6709A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6709A X XX XX

- MCM — Motorola Memory Prefix
- 6709A — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6709AJ8, MCM6709AJ8R2, MCM6709AJ10, MCM6709AJ10R2, MCM6709AJ12, MCM6709AJ12R2

MCM6709AR

64K x 4 Bit Static RAM

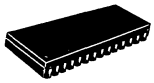
2

The MCM6709AR is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

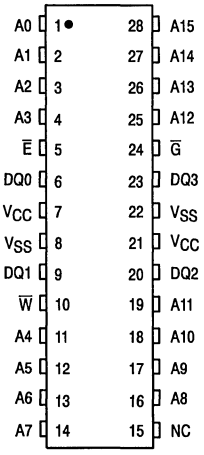
The MCM6709AR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 28 lead plastic surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Center Power and I/O Pins for Reduced Noise
- Three State Outputs
- Fast Access Times: MCM6709AR–6 = 6 ns
  MCM6709AR–7 = 7 ns

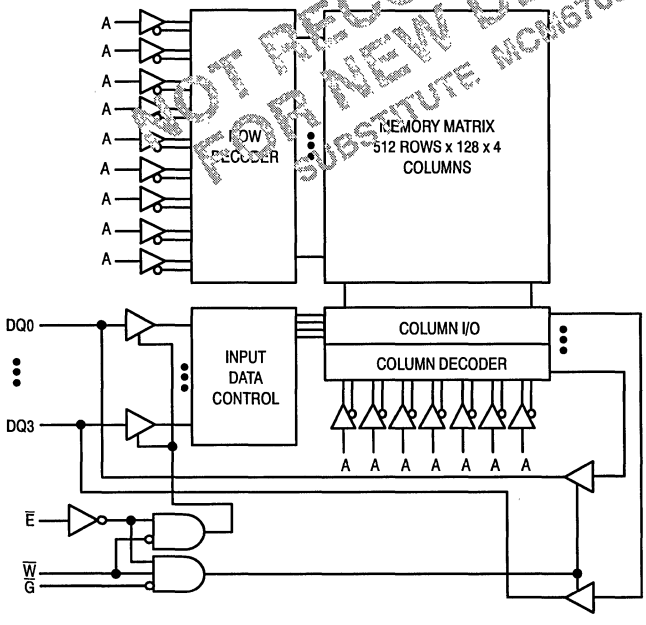


J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709AR–6	MCM6709AR–7	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	235	225	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	85	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709AR–6		MCM6709AR–7		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	2.5	—	2.5	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. .All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

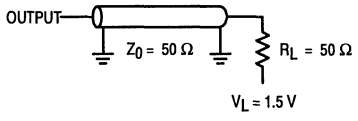


Figure 1A

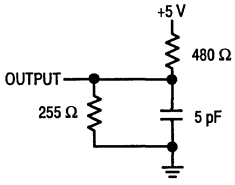
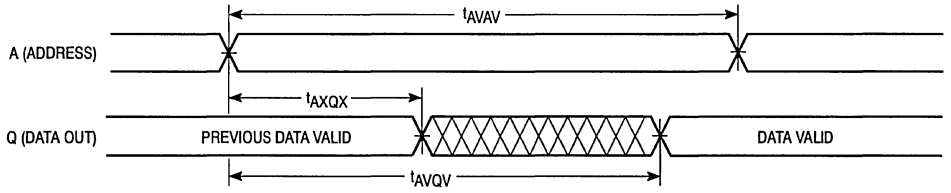


Figure 1B

TIMING LIMITS

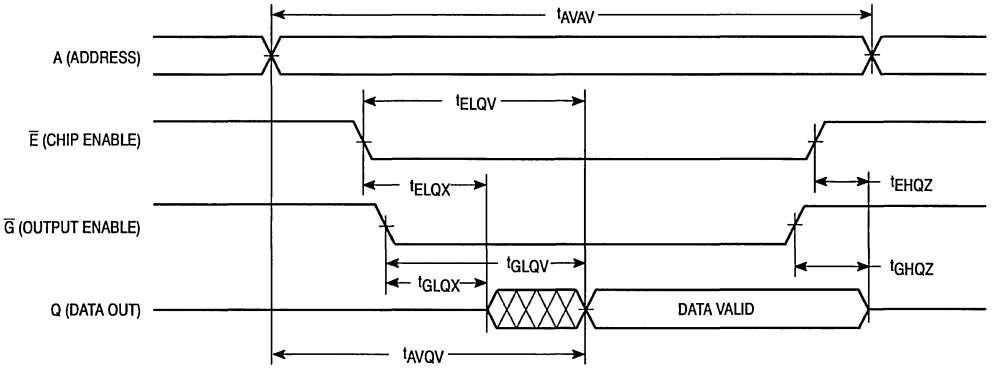
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



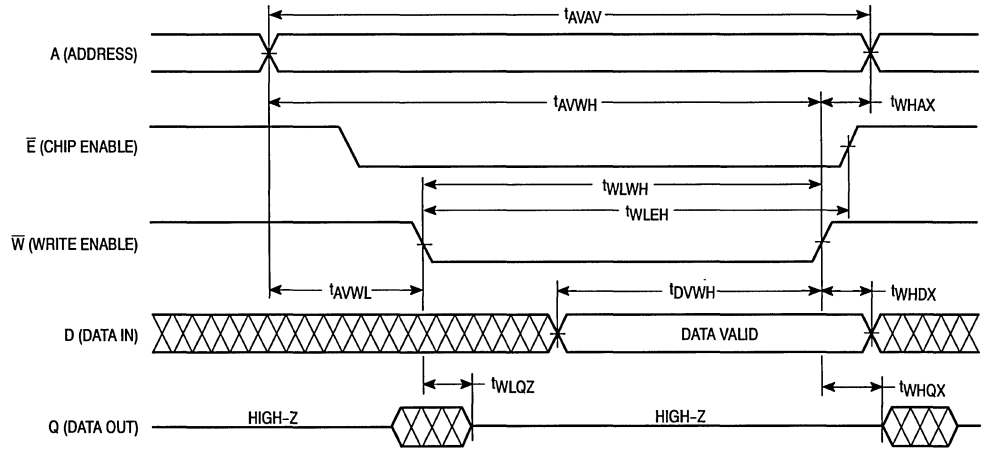
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709AR–6		MCM6709AR–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

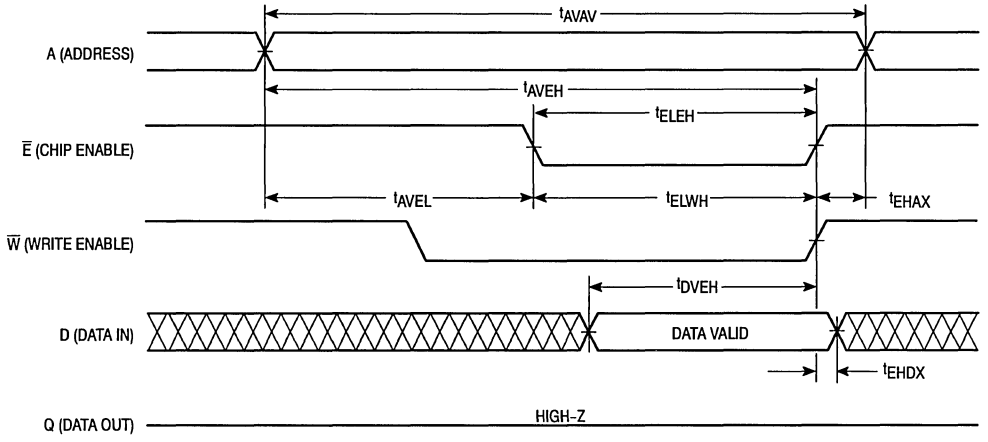


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

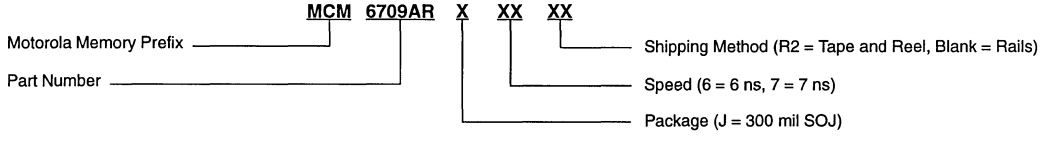
Parameter	Symbol	MCM6709AR–6		MCM6709AR–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	5	—	6	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6709ARJ6 MCM6709ARJ6R2
MCM6709ARJ7 MCM6709ARJ7R2

2

MCM6709B

Product Preview

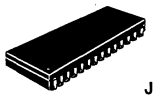
64K x 4 Bit Static RAM

The MCM6709B is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$), a special control feature of the MCM6709B, provides increased system flexibility and eliminates bus contention problems.

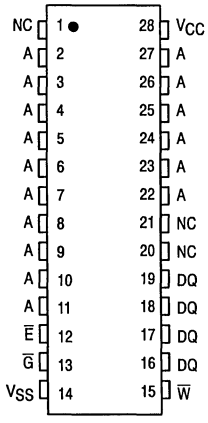
The MCM6709B is available in a 300 mil, 28 lead plastic surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6709B–8 = 8 ns
  MCM6709B–10 = 10 ns
  MCM6709B–12 = 12 ns

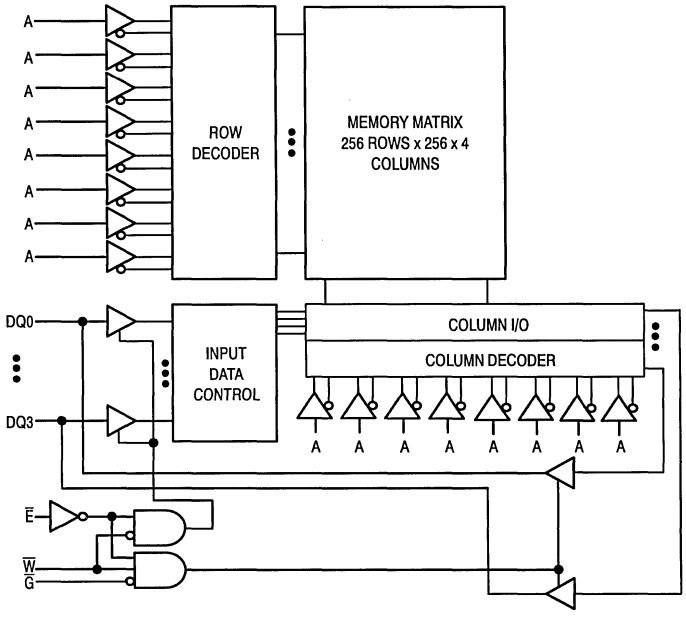


J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains informantion on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709B–8	MCM6709B–10	MCM6709B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	185	175	165	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	120	110	105	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	5	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709B–8		MCM6709B–10		MCM6709B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	1	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

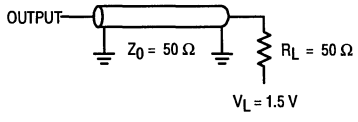


Figure 1A

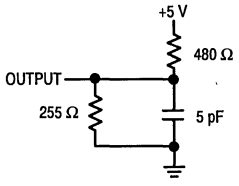
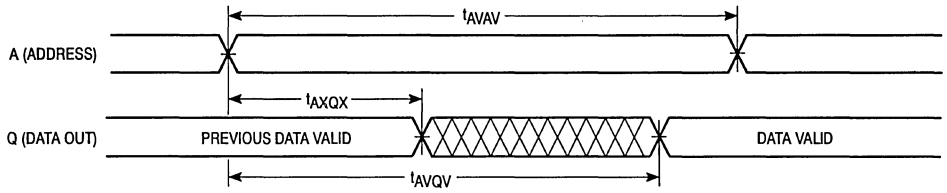


Figure 1B

TIMING LIMITS

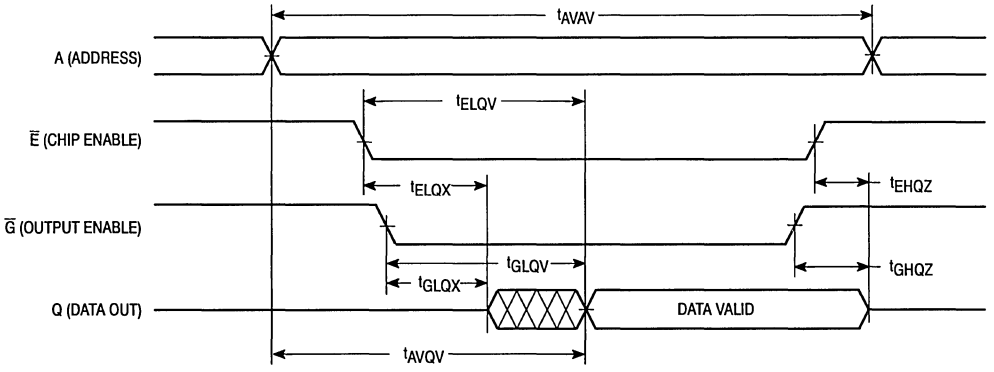
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



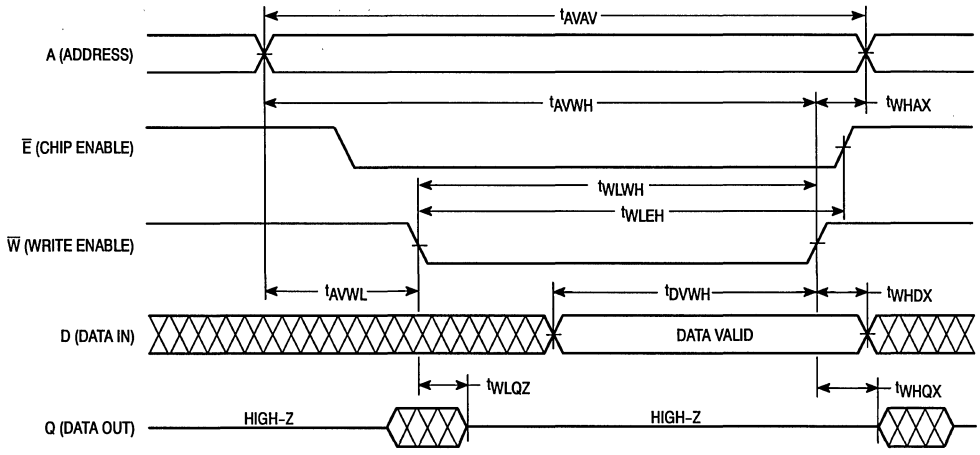
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709B–8		MCM6709B–10		MCM6709B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

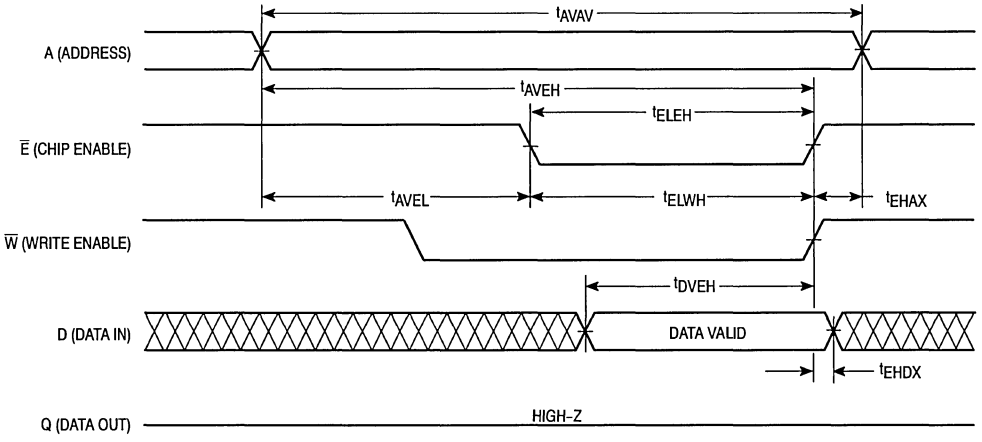


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709B–8		MCM6709B–10		MCM6709B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6709B X XX X

- MCM: Motorola Memory Prefix
- 6709B: Part Number
- X: Package (J = 300 mil SOJ)
- XX: Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X: Shipping Method (R = Tape and Reel, Blank = Rails)

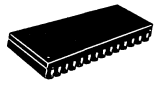
Full Part Numbers — MCM6709BJ8, MCM6709BJ8R, MCM6709BJ10, MCM6709BJ10R, MCM6709BJ12, MCM6709BJ12R

MCM6709BR

2

Product Preview

64K x 4 Bit Static RAM



J PACKAGE
300 MIL SOJ
CASE 810B–03

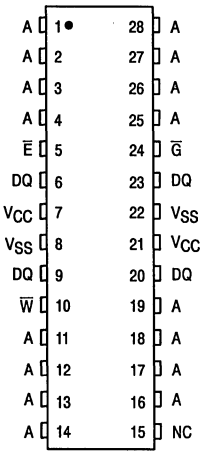
The MCM6709BR is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

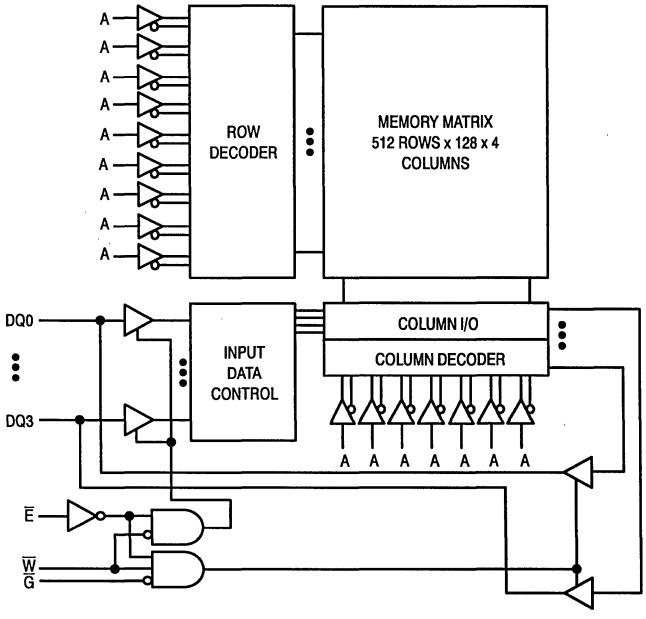
The MCM6709BR meets JEDEC standards and is available in a revolutionary pinout 300 mil, 28 lead plastic surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Center Power and I/O Pins for Reduced Noise
- Three State Outputs
- Fast Access Times:
  MCM6709BR–6 = 6 ns
  MCM6709BR–7 = 7 ns
  MCM6709BR–8 = 8 ns

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709BR–6	MCM6709BR–7	MCM6709BR–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	215	205	195	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	85	75	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709BR–6		MCM6709BR–7		MCM6709BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	—	3	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	0	3.5	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	0	3.5	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

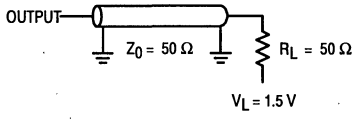


Figure 1A

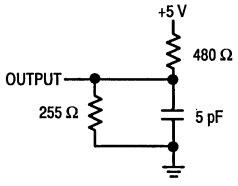
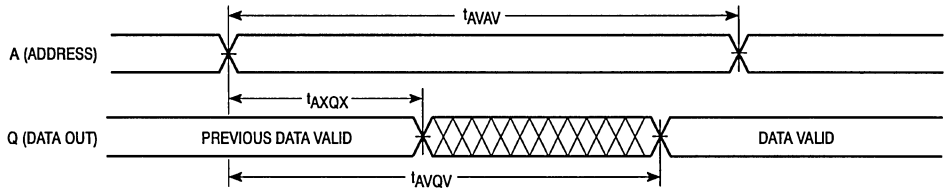


Figure 1B

TIMING LIMITS

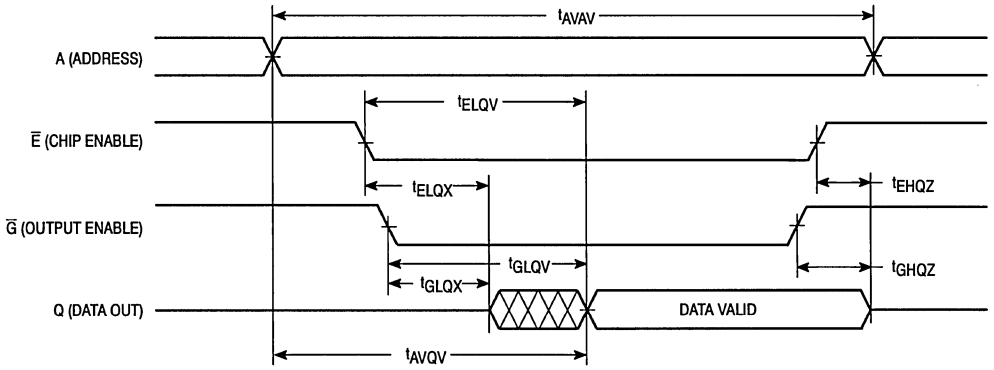
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



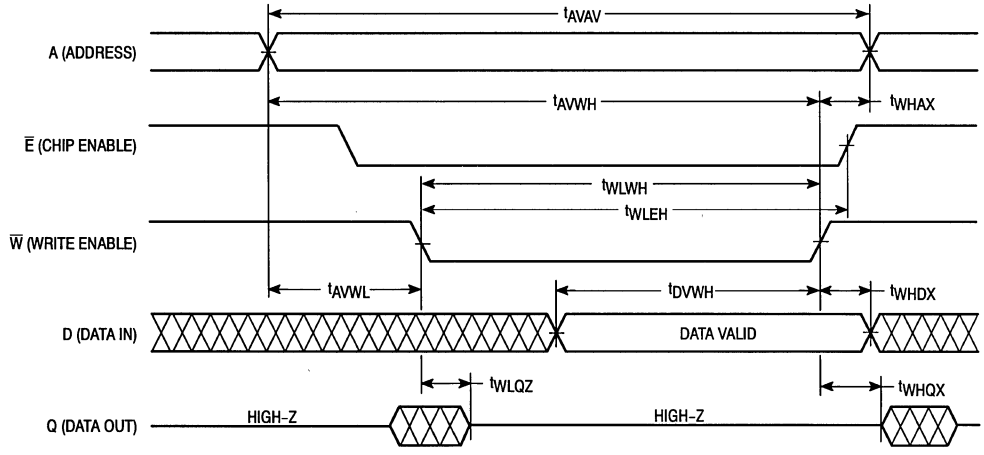
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709BR–6		MCM6709BR–7		MCM6709BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	0	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

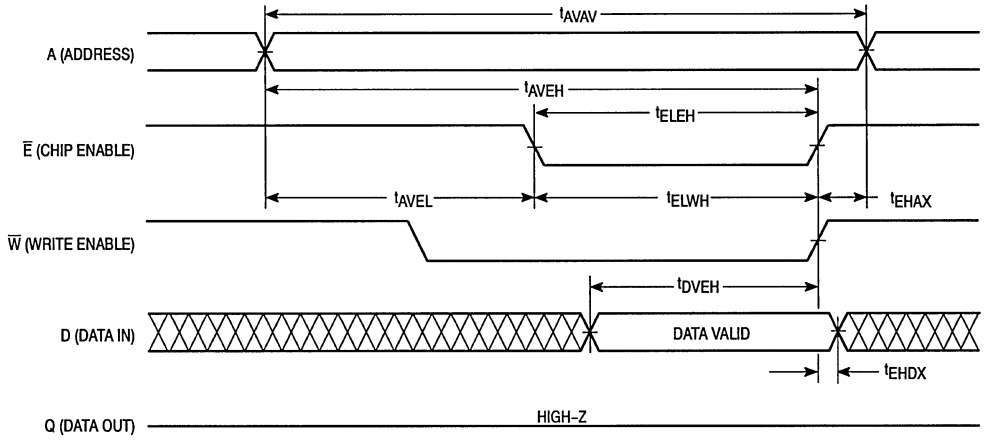


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709BR–6		MCM6709BR–7		MCM6709BR–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	5	—	6	—	7	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6709BR X X X

- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6709BRJ6, MCM6709BRJ6R, MCM6709BRJ7, MCM6709BRJ7R, MCM6709BRJ8, MCM6709BRJ8R

MCM6709R

64K x 4 Bit Static RAM

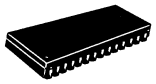
2

The MCM6709R is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

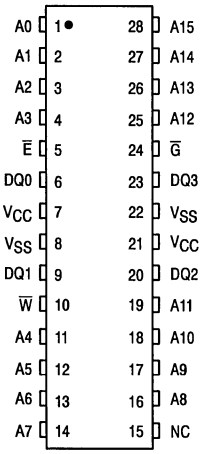
The MCM6709R meets JEDEC standards and is available in a revolutionary pinout 300 mil, 28 lead plastic surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Center Power and I/O Pins for Reduced Noise
- Three State Outputs
- Fast Access Times: MCM6709R–6 = 6 ns
  MCM6709R–7 = 7 ns
  MCM6709R–8 = 8 ns

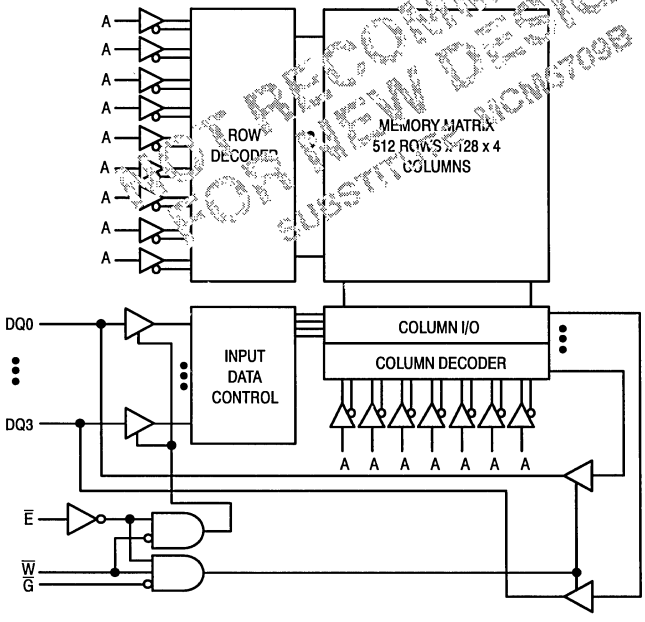


J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

REV 1
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High–Z	—
L	H	H	Read	High–Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
**V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709R–6	MCM6709R–7	MCM6709R–8	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	190	185	mA	1, 2, 3
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	85	80	75	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol	MCM6709R–6		MCM6709R–7		MCM6709R–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	0	4	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	0	4	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

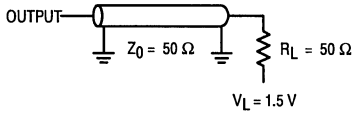


Figure 1A

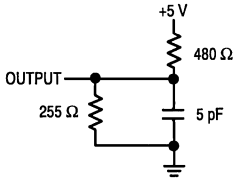
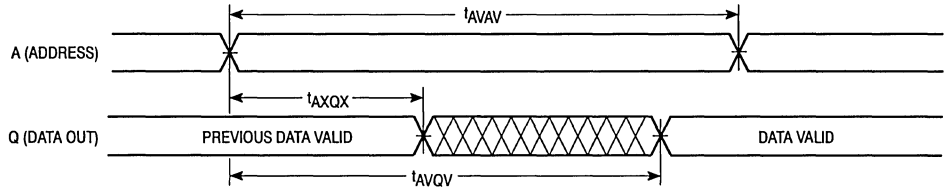


Figure 1B

TIMING LIMITS

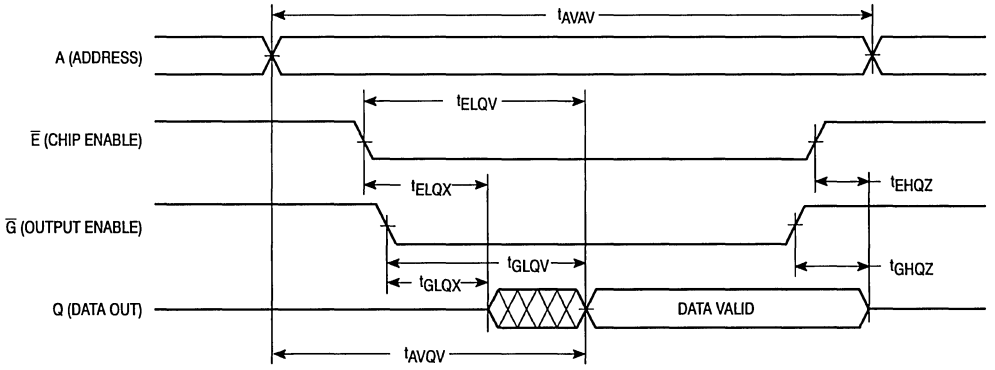
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



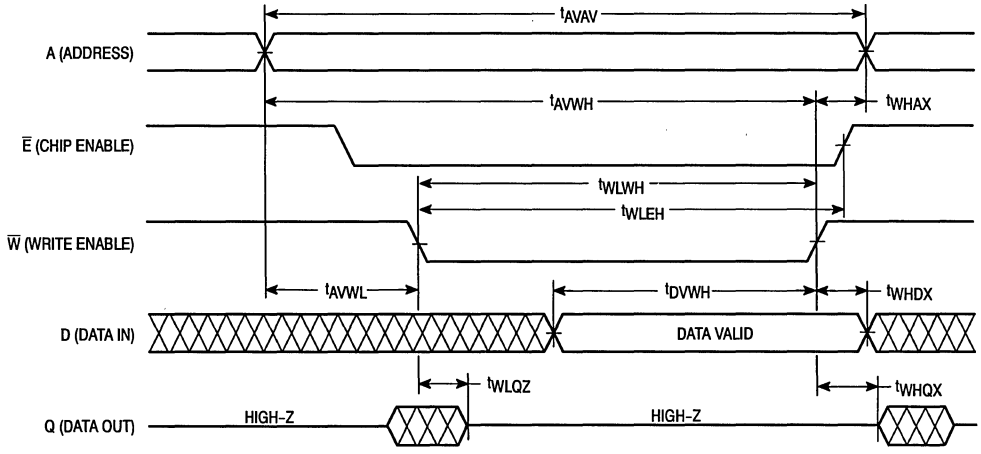
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709R–6		MCM6709R–7		MCM6709R–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	0	4	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

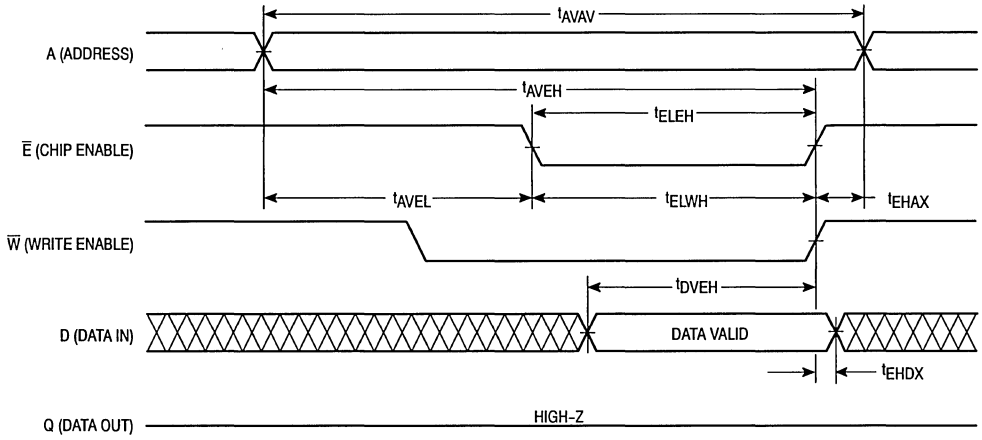


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709R–6		MCM6709R–7		MCM6709R–8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	5	—	6	—	7	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6709R X X X

- MCM: Motorola Memory Prefix
- 6709R: Part Number
- X: Package (J = 300 mil SOJ)
- X: Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- X: Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6709RJ6, MCM6709RJ7, MCM6709RJ8, MCM6709RJ6R2, MCM6709RJ7R2, MCM6709RJ8R2

MCM6726

2

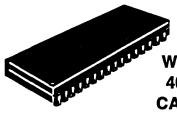
128K x 8 Bit Fast Static Random Access Memory

The MCM6726 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

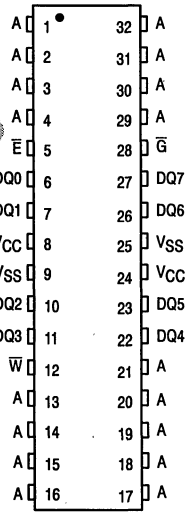
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

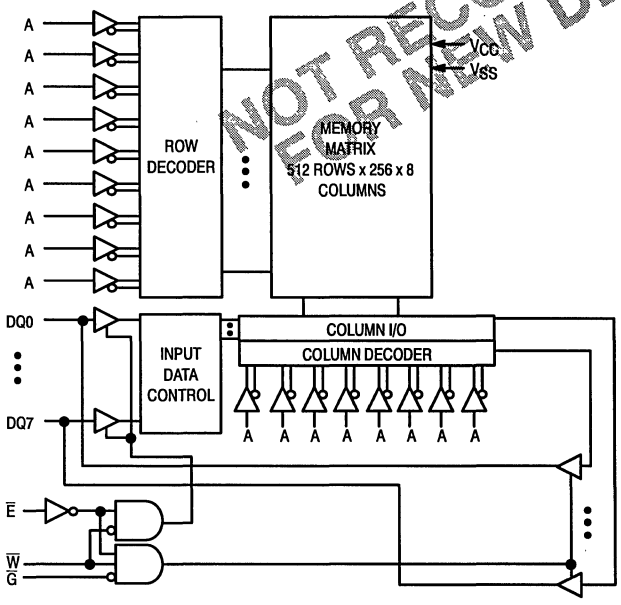


WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 5
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6726–10	MCM6726–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	175	165	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6726–10		MCM6726–12		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	5	0	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

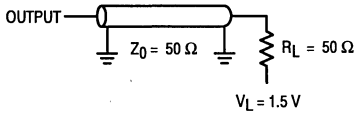


Figure 1A

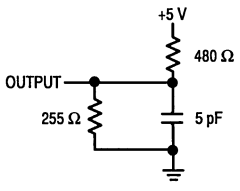
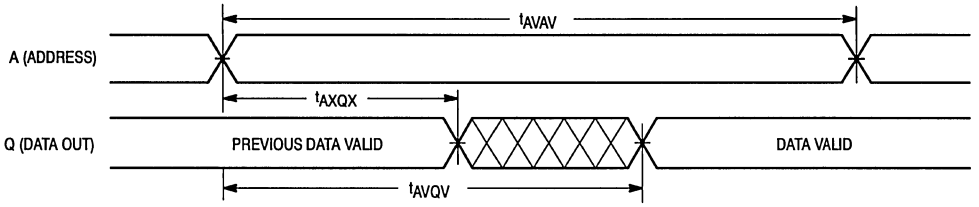


Figure 1B

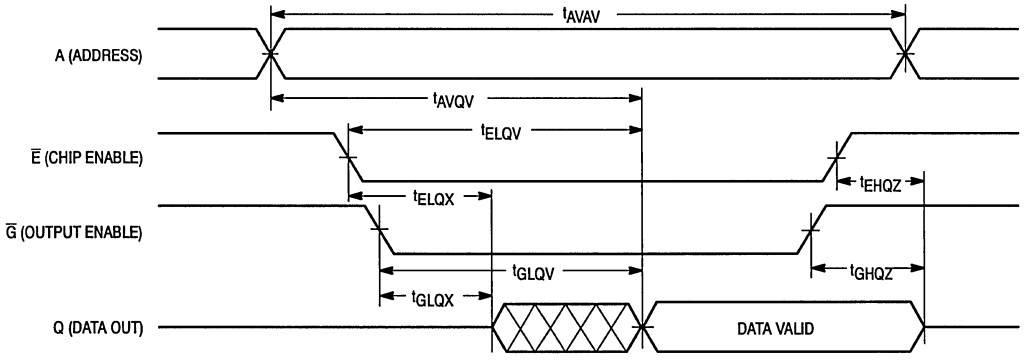
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

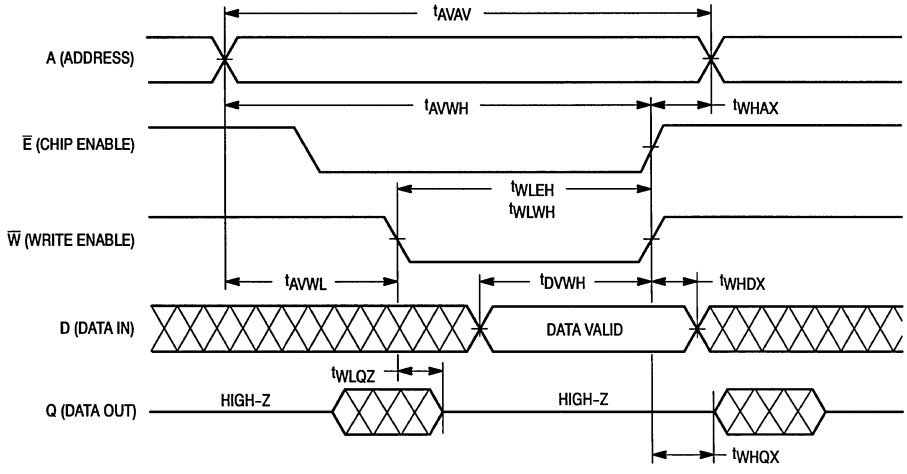


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6726–10		MCM6726–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

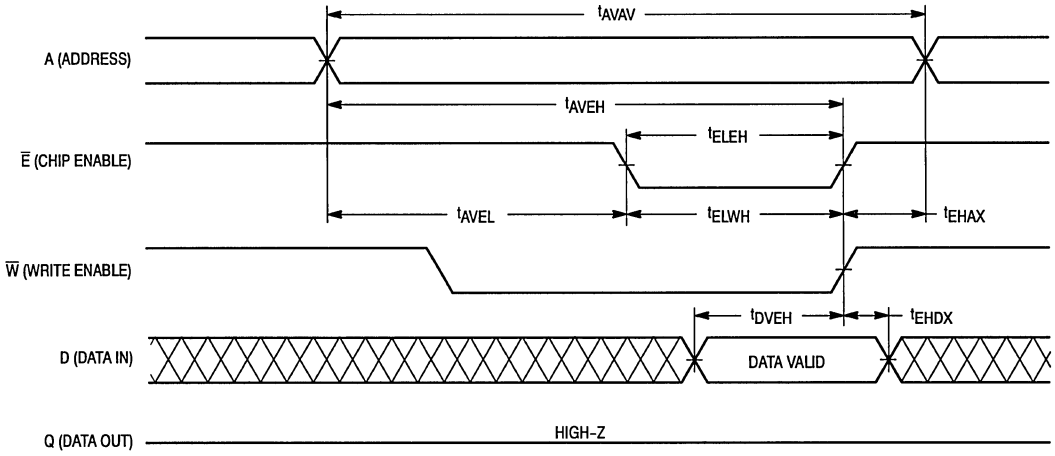


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6726–10		MCM6726–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6726 WJ XX XX

- MCM — Motorola Memory Prefix
- 6726 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (10 = 10 ns, 12 = 12 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6726WJ10 MCM6726WJ12
MCM6726WJ10R2 MCM6726WJ12R2

MCM6726B

128K x 8 Bit Fast Static Random Access Memory

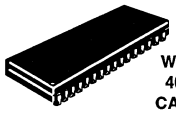
2

The MCM6726B is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

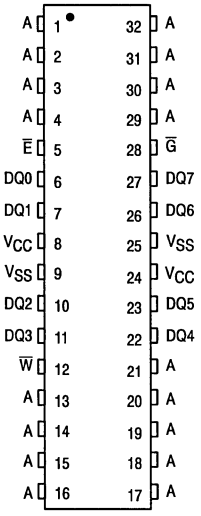
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

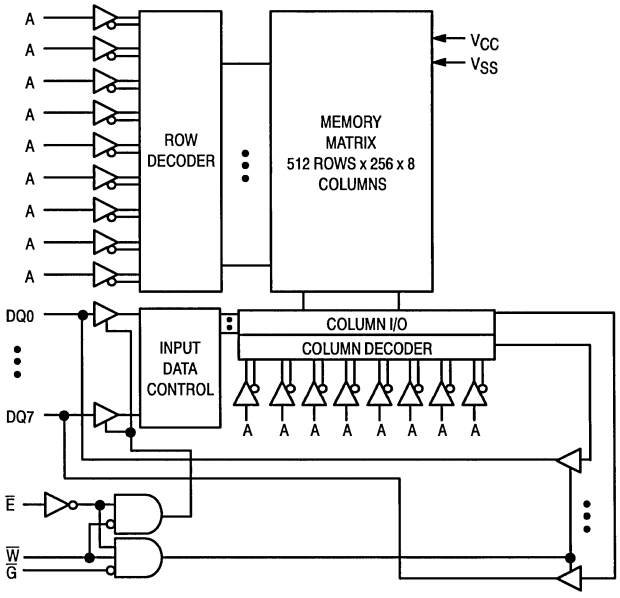


WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

REV 2
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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726B–8	6726B–10	6726B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	175	165	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6726B–8		6726B–10		6726B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	0	5	0	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	0	5	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

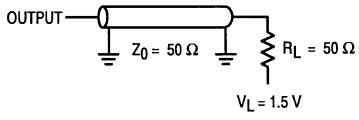


Figure 1A

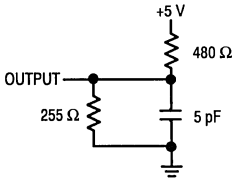
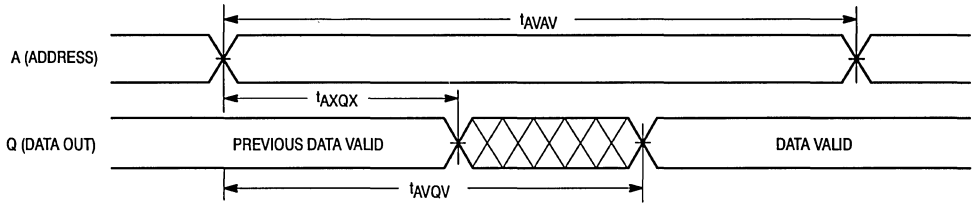


Figure 1B

TIMING LIMITS

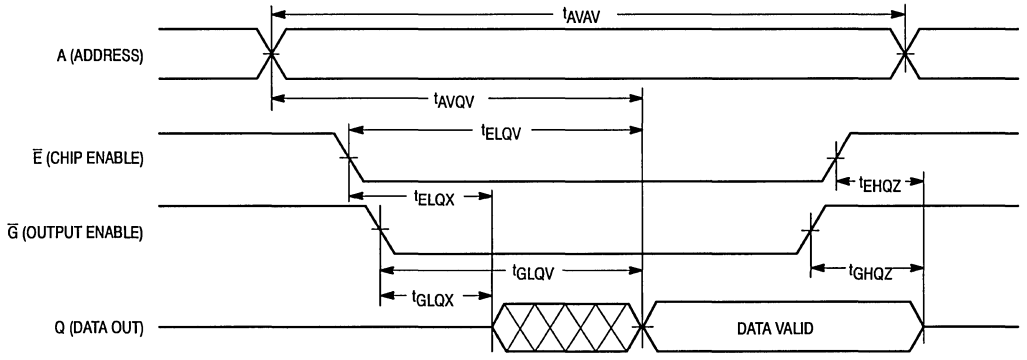
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



2

READ CYCLE 2 (See Note 8)

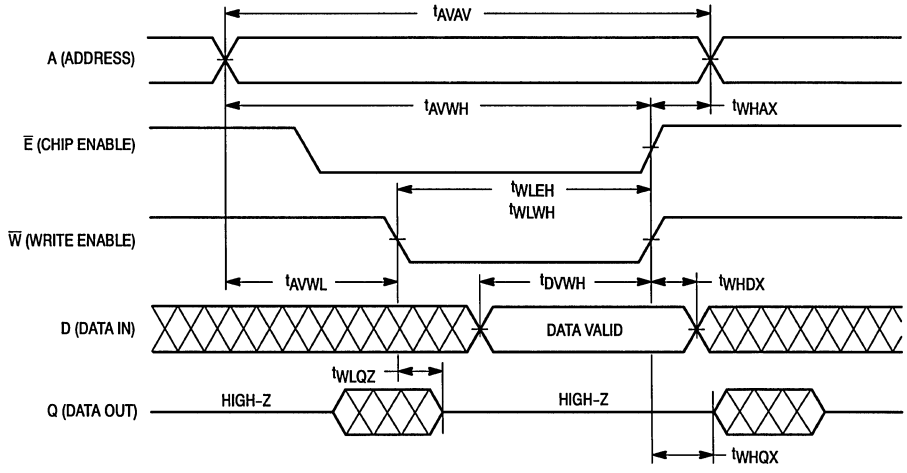


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726B–8		6726B–10		6726B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

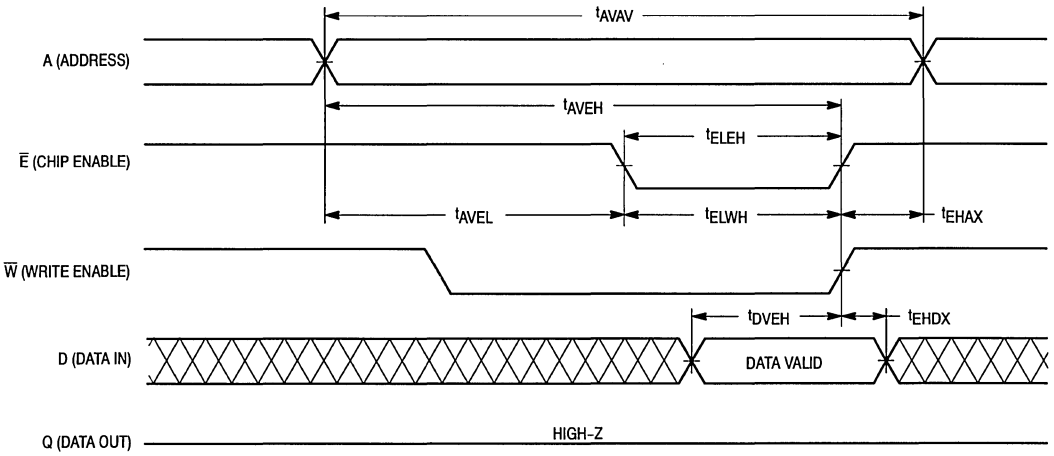


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726B–8		6726B–10		6726B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6726B WJ XX X

- MCM — Motorola Memory Prefix
- 6726B — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6726BWJ8, MCM6726BWJ8R, MCM6726BWJ10, MCM6726BWJ10R, MCM6726BWJ12, MCM6726BWJ12R

MCM6726C

128K x 8 Bit Fast Static Random Access Memory

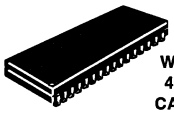
2

The MCM6726C is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

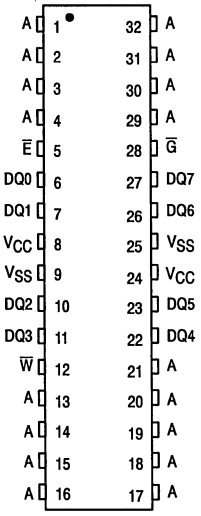
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 6, 7 ns
- Center Power and I/O Pins for Reduced Noise

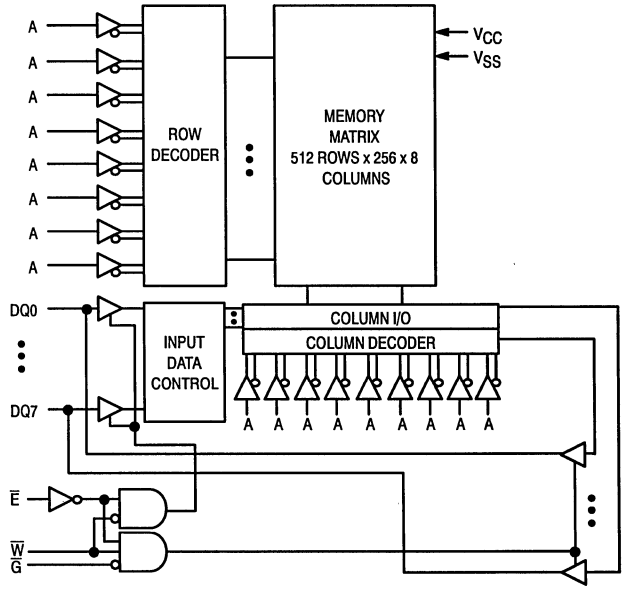


WJ PACKAGE
400 MIL SOJ
CASE 857A–01

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726C–6	6726C–7	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	250	220	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	100	100	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	60	60	mA	

NOTES:
1. Reference AC Operating Conditions and Characterisitics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data States are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6726C–6		6726C–7		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	ns	
Enable Access Time	t_{ELQV}	—	6	—	7	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	3	0	3.5	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	3	0	3.5	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

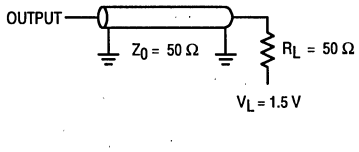


Figure 1A

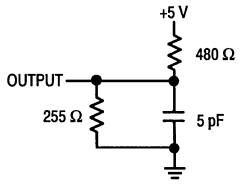
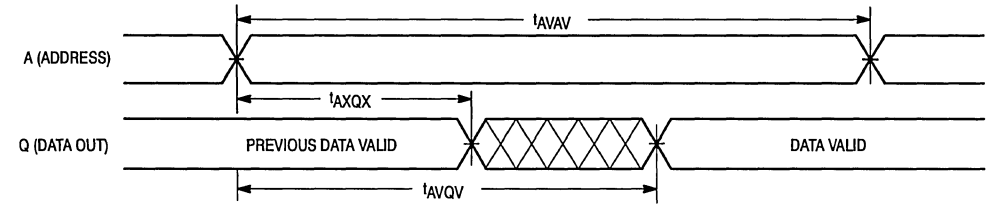


Figure 1B

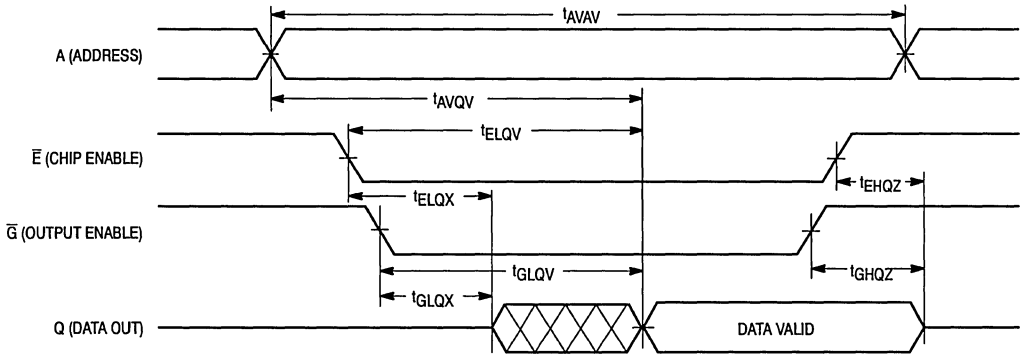
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

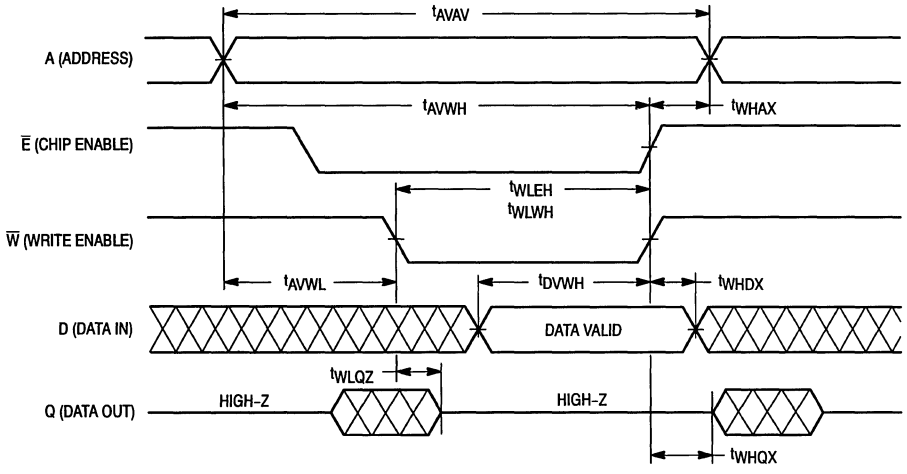


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726C–6		6726C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	6	—	7	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

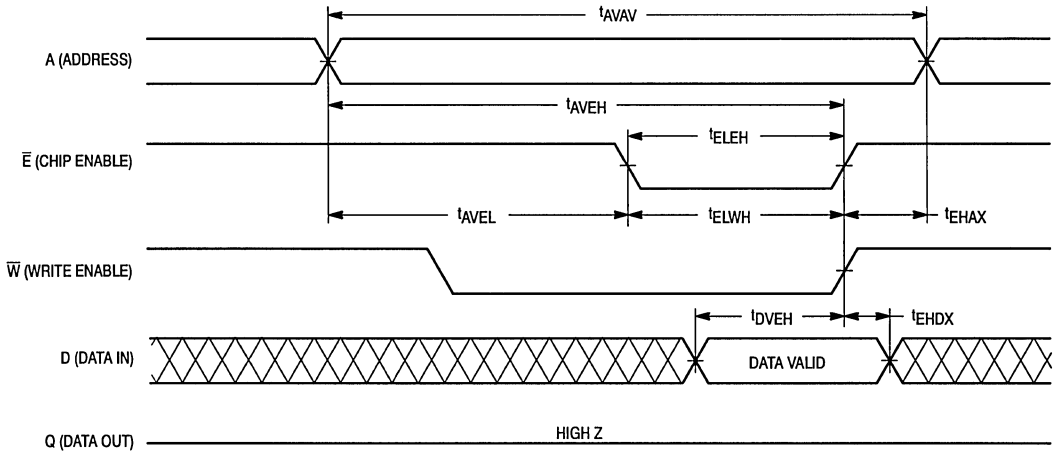


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6726C–6		6726C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	5	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6726C WJ X X

- MCM: Motorola Memory Prefix
- 6726C: Part Number
- WJ: Package (WJ = 400 mil SOJ)
- X: Speed (6 = 6 ns, 7 = 7 ns)
- X: Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6726CWJ6 MCM6726CWJ7
MCM6726CWJ6R MCM6726CWJ7R

MCM6728B

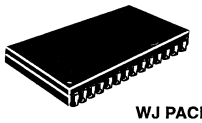
256K x 4 Bit Fast Static Random Access Memory

2

The MCM6728B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

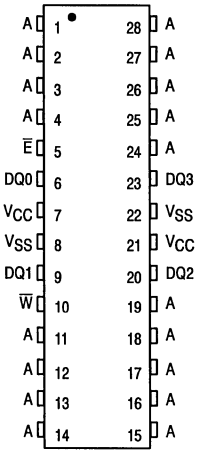
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

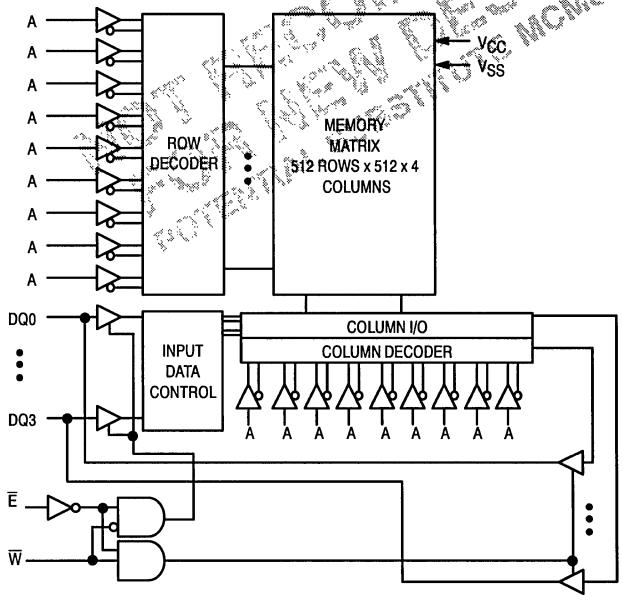


WJ PACKAGE
400 MIL SOJ
CASE 810–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

REV 2
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6728B–8	6728B–10	6728B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	165	155	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6728B–8		6728B–10		6728B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	4	0	5	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, for a given device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

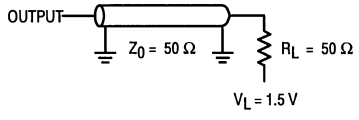


Figure 1A

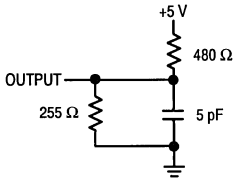
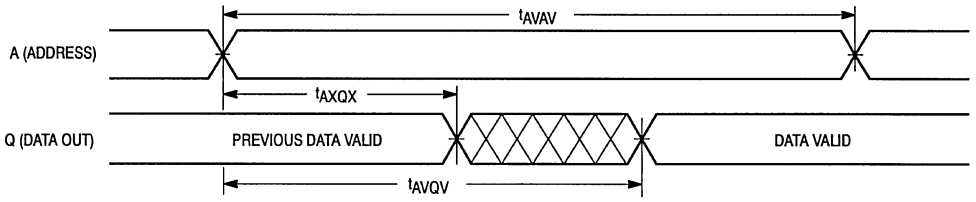


Figure 1B

TIMING LIMITS

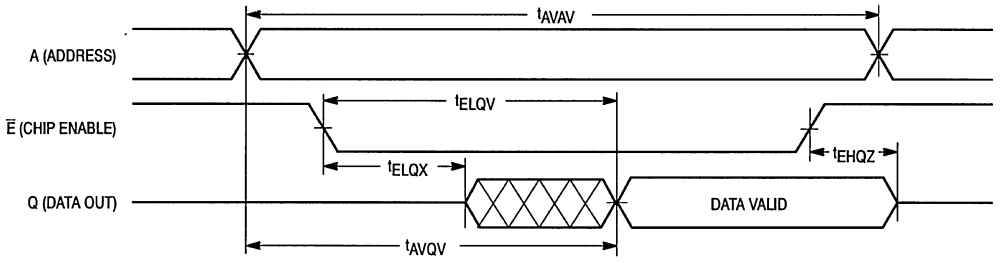
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



2

READ CYCLE 2 (See Note 8)

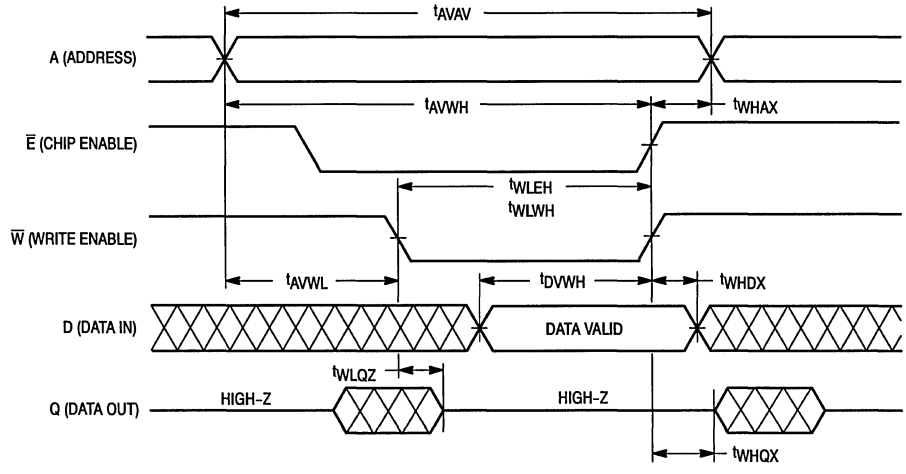


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6728B–8		6728B–10		6728B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

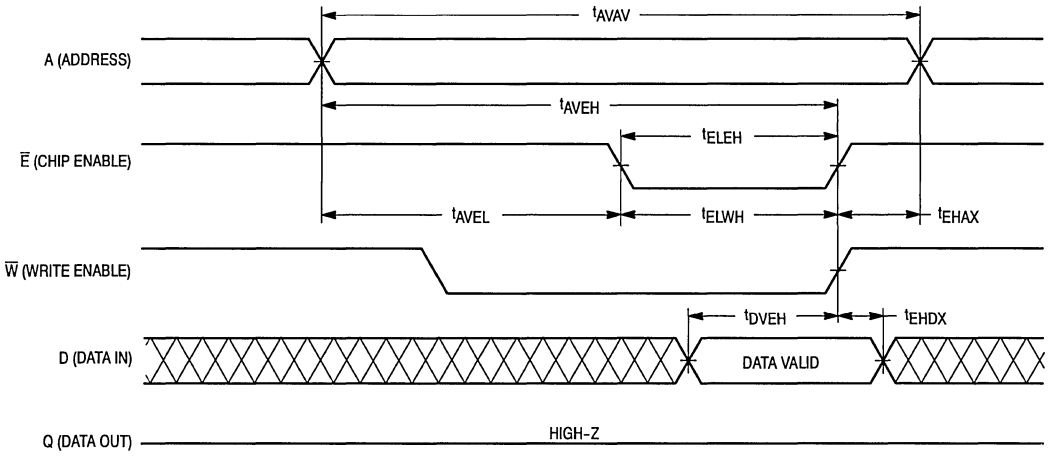


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6728B–8		6728B–10		6728B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6728B WJ XX X

- MCM: Motorola Memory Prefix
- 6728B: Part Number
- WJ: Package (WJ = 400 mil SOJ)
- XX: Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- X: Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6728BWJ8, MCM6728BWJ8R, MCM6728BWJ10, MCM6728BWJ10R, MCM6728BWJ12, MCM6728BWJ12R

MCM6729

256K x 4 Bit Fast Static Random Access Memory

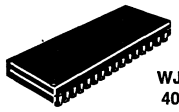
2

The MCM6729 is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

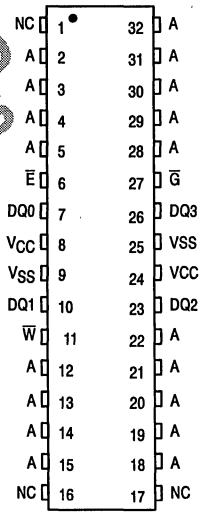
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

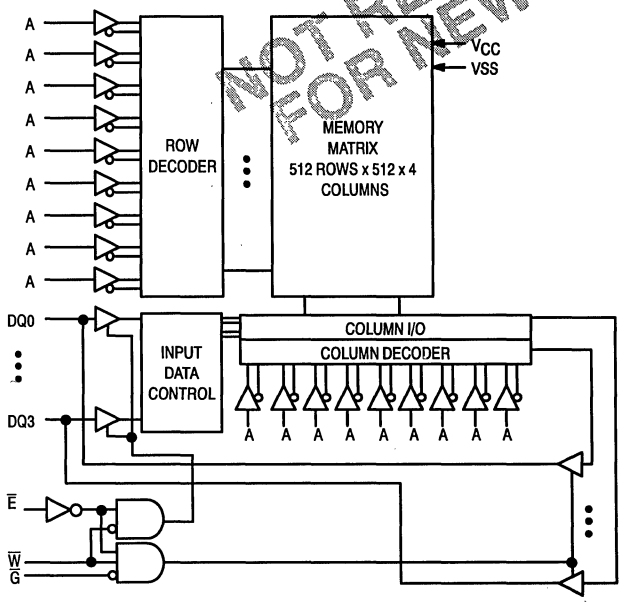


WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

REV 4
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6729–10	MCM6729–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	165	155	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM6729–10		MCM6729–12		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	5	0	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

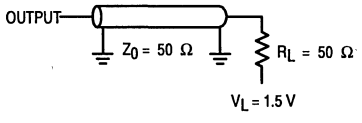


Figure 1A

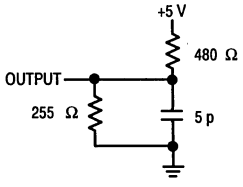
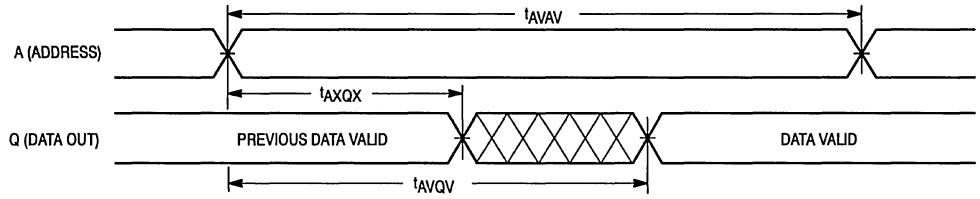


Figure 1B

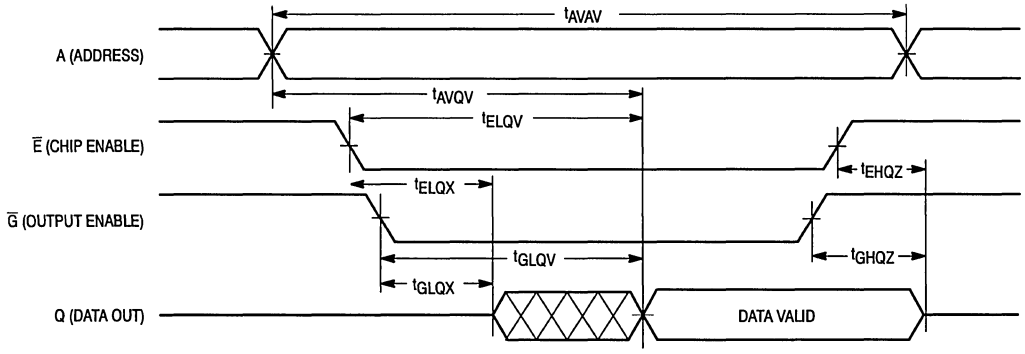
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

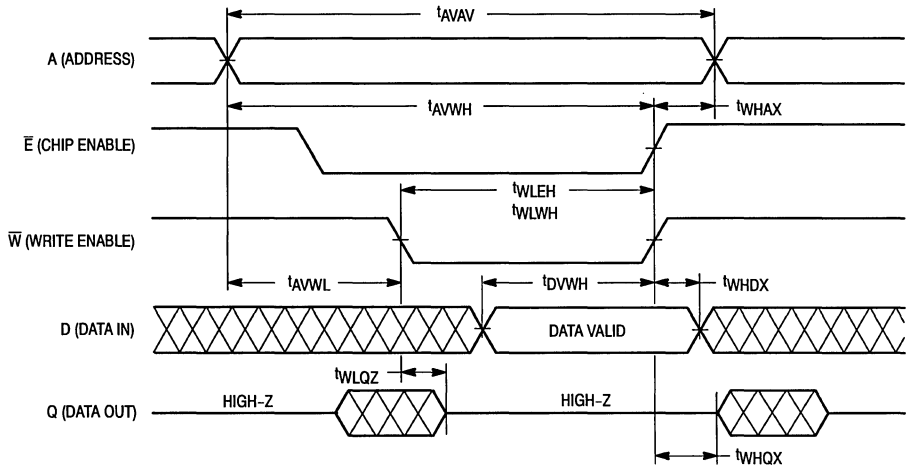


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6729–10		MCM6729–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

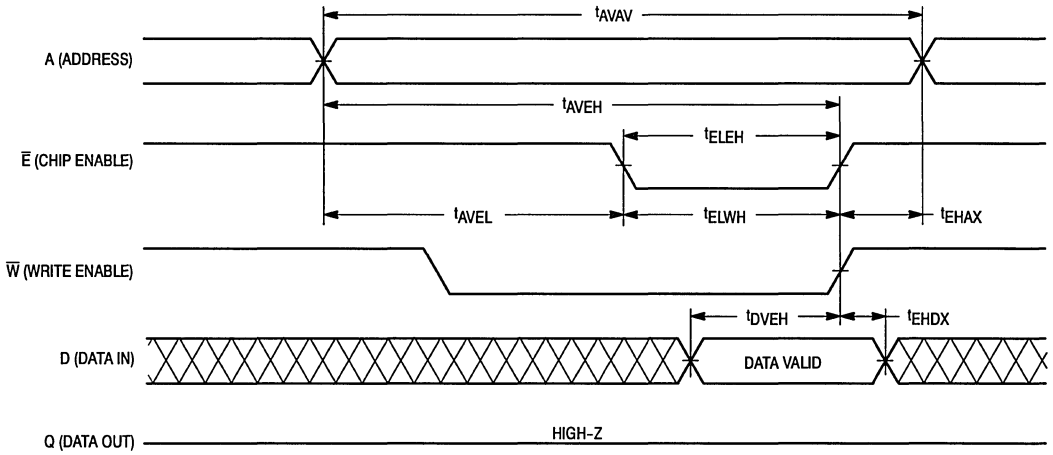


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6729–10		MCM6729–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729 WJ XX XX

- MCM — Motorola Memory Prefix
- 6729 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (10 = 10 ns, 12 = 12 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6729WJ10, MCM6729WJ10R2, MCM6729WJ12, MCM6729WJ12R2

MCM6729B

256K x 4 Bit Fast Static Random Access Memory

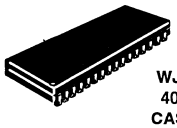
2

The MCM6729B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

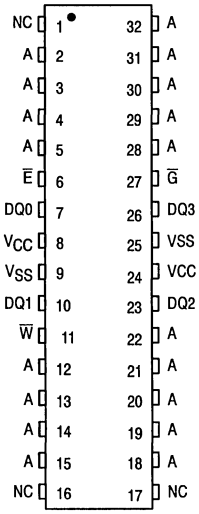
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12 ns
- Center Power and I/O Pins for Reduced Noise

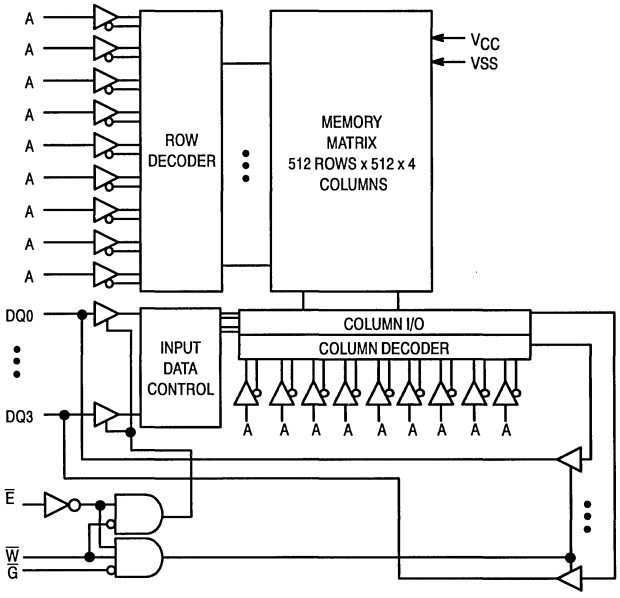


WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

REV 2
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6729B–8	6729B–10	6729B–12	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	195	165	155	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA	

NOTES:
1. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6729B–8		6729B–10		6729B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	4	0	5	0	6	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

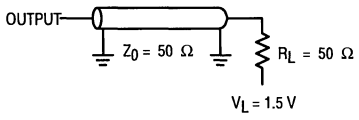


Figure 1A

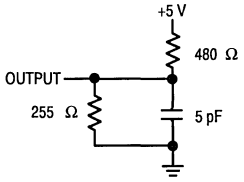
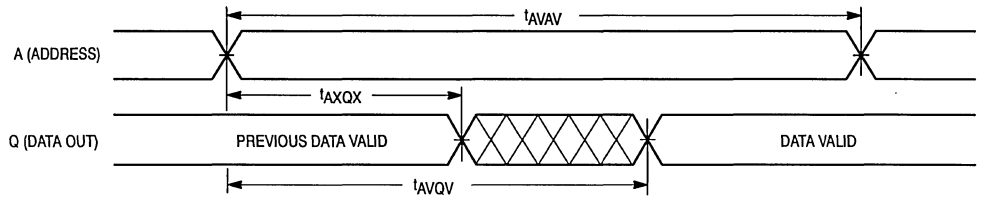


Figure 1B

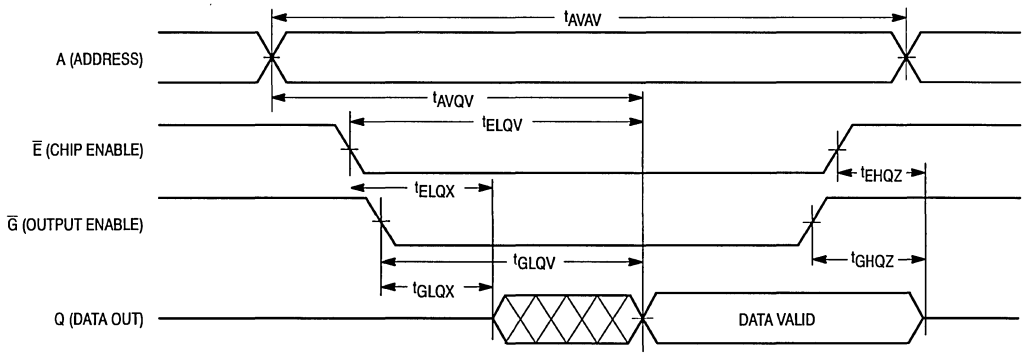
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

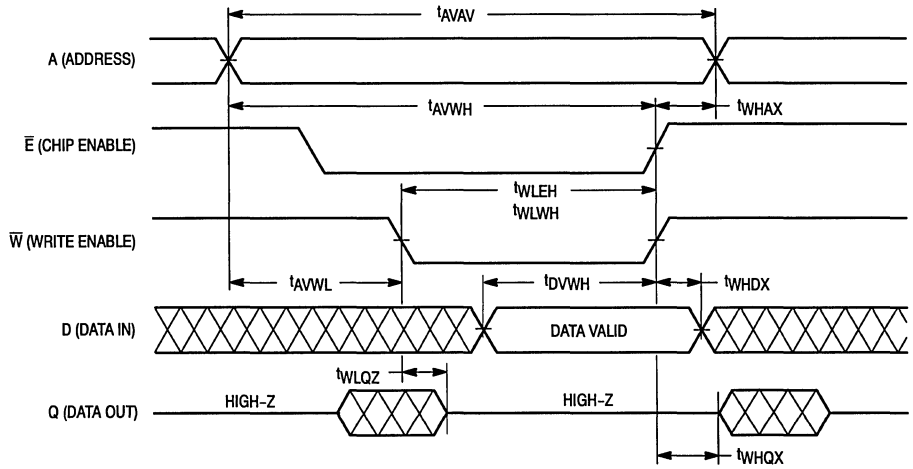


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729B–8		6729B–10		6729B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

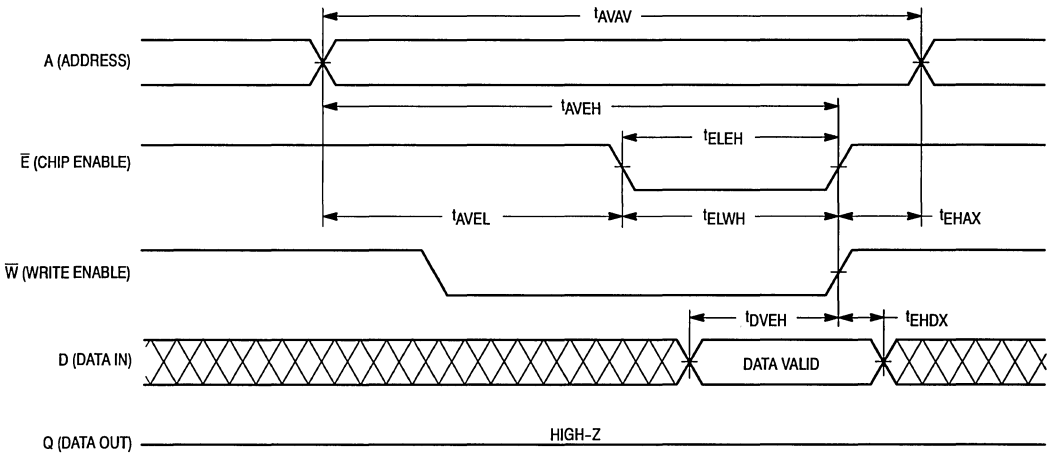


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729B–8		6729B–10		6729B–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729B WJ XX X

- Motorola Memory Prefix
- Part Number
- Shipping Method (R = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6729BWJ8 MCM6729BWJ10 MCM6729BWJ12
MCM6729BWJ8R MCM6729BWJ10R MCM6729BWJ12R

MCM6729C

256K x 4 Bit Fast Static Random Access Memory

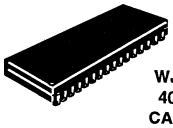
2

The MCM6729C is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

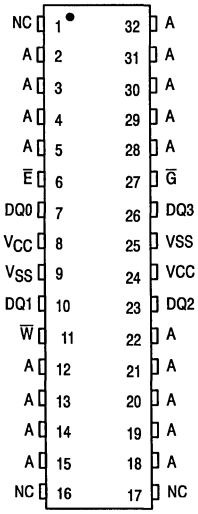
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 6, 7 ns
- Center Power and I/O Pins for Reduced Noise

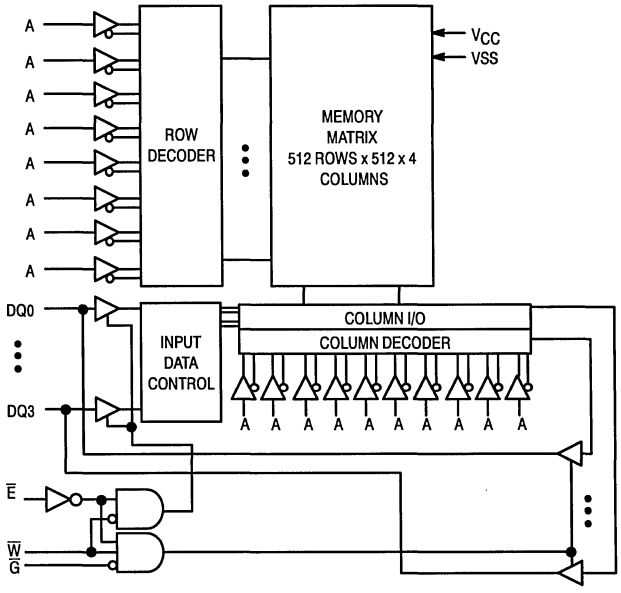


WJ PACKAGE
400 MIL SOJ
CASE 857A–01

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

REV 1
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6729C–6	6729C–7	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	250	220	mA	1, 2, 3
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	100	100	mA	1, 2, 3
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	60	60	mA	

NOTES:
1. Reference AC Operating Conditions and Characterisitics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3 V, V_{IH} = 3 V).
2. All addresses transition simultaneously low (LSB) and then high (MSB).
3. Data States are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6729C–6		6729C–7		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Access Time	t_{AVQV}	—	6	—	7	ns	
Enable Access Time	t_{ELQV}	—	6	—	7	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	3	0	3.5	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	3	0	3.5	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

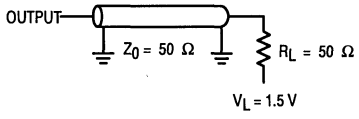


Figure 1A

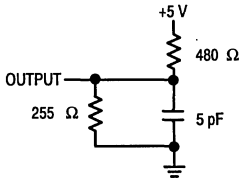
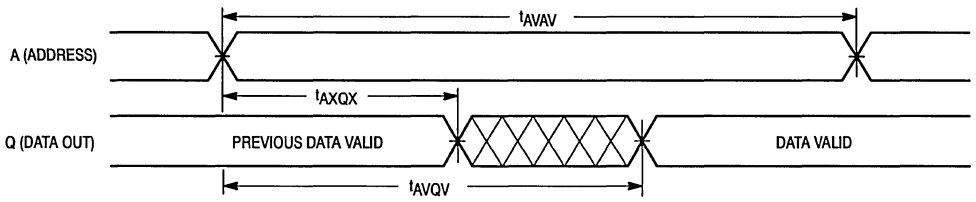


Figure 1B

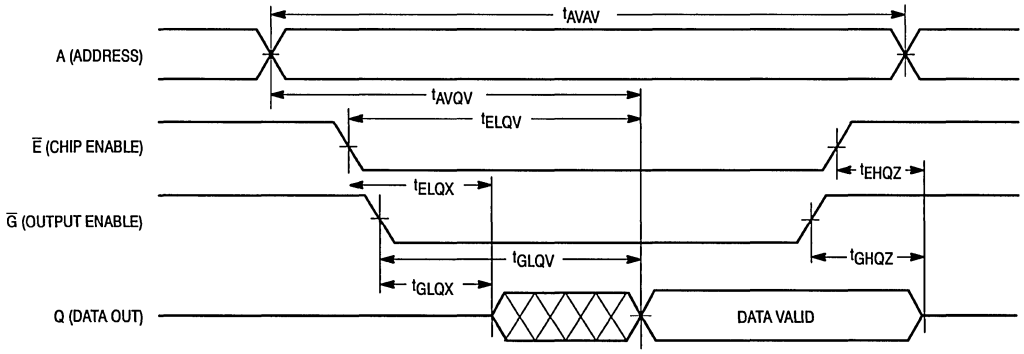
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

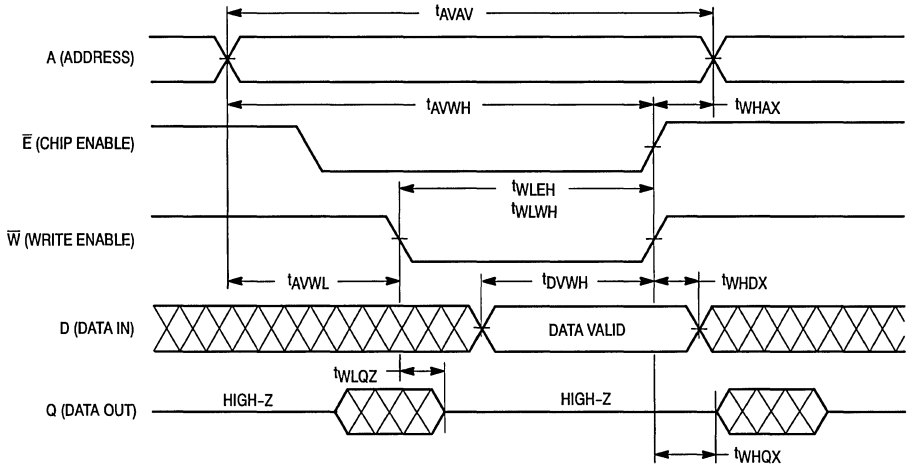


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729C–6		6729C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	6	—	7	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	6	—	7	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	3	—	3.5	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	3.5	0	3.5	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

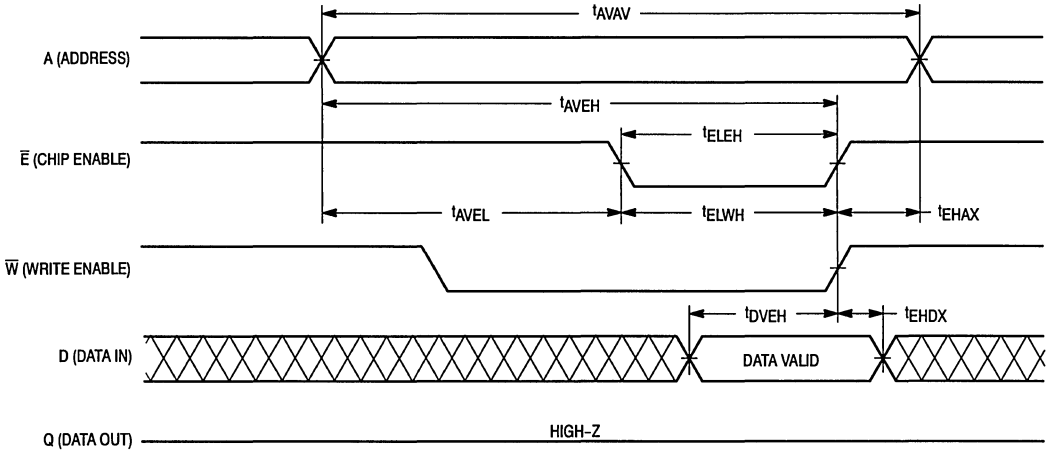


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6729C–6		6729C–7		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	6	—	7	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	6	—	7	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	5	—	6	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	3	—	3.5	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729C WJ X X

- MCM — Motorola Memory Prefix
- 6729C — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- X — Speed (6 = 6 ns, 7 = 7 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

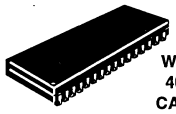
Full Part Numbers — MCM6729CWJ6 MCM6729CWJ7
MCM6729CWJ6R MCM6729CWJ7R

2

MCM6926

Product Preview

128K x 8 Bit Fast Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A–02

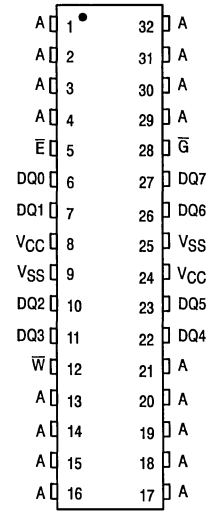
The MCM6926 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

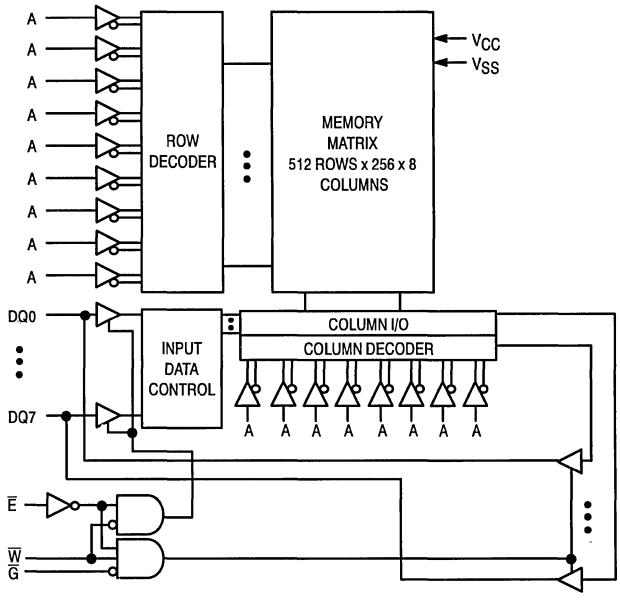
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+3.3 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

2/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{CC} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All address transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

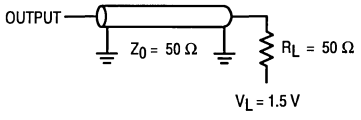


Figure 1A

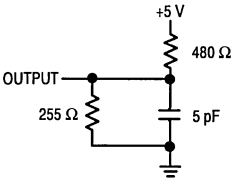
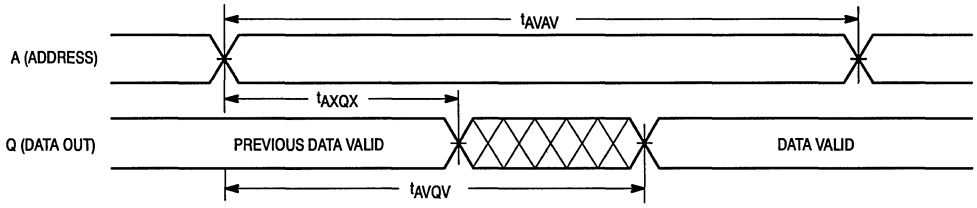


Figure 1B

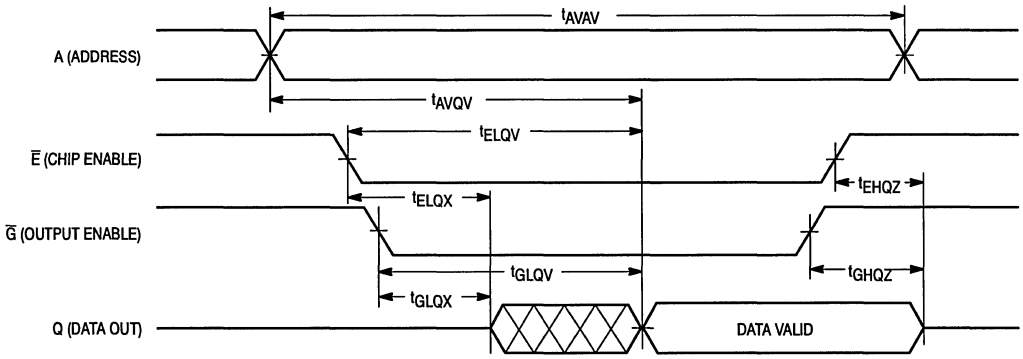
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

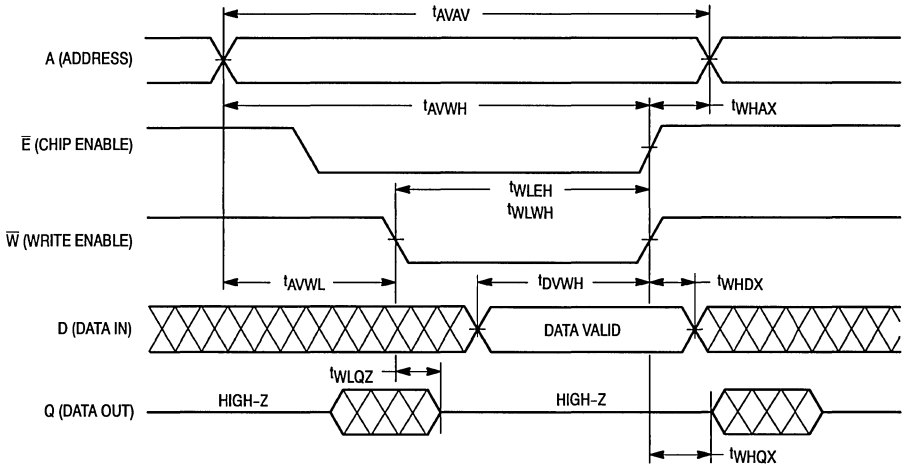


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

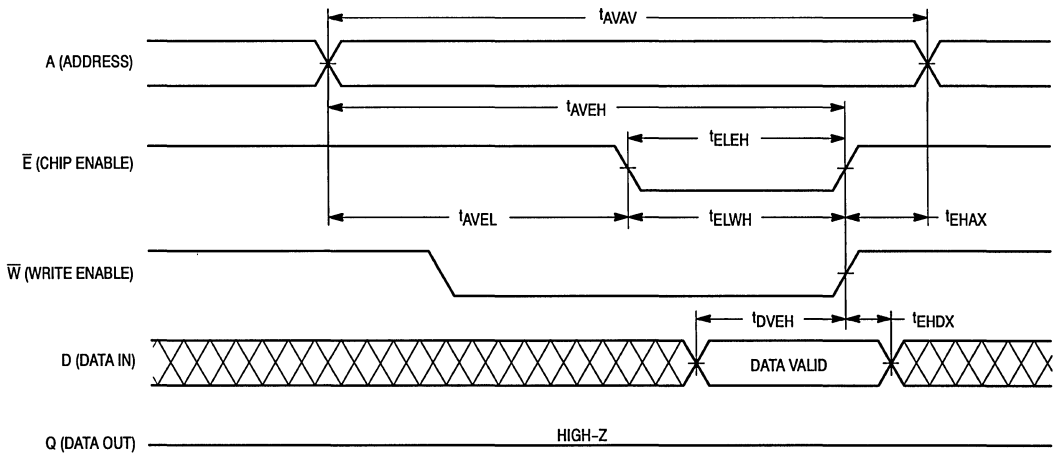


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6926–8		6926–10		6926–12		6926–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6926 WJ XX X

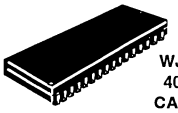
- MCM — Motorola Memory Prefix
- 6926 — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6926WJ8, MCM6926WJ8R, MCM6926WJ10, MCM6926WJ10R, MCM6926WJ12, MCM6926WJ12R, MCM6926WJ15, MCM6926WJ15R

MCM6929

Product Preview

256K x 4 Bit Fast Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A–02

2

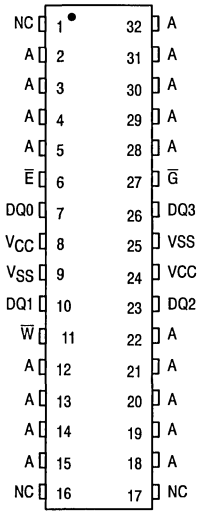
The MCM6929 is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

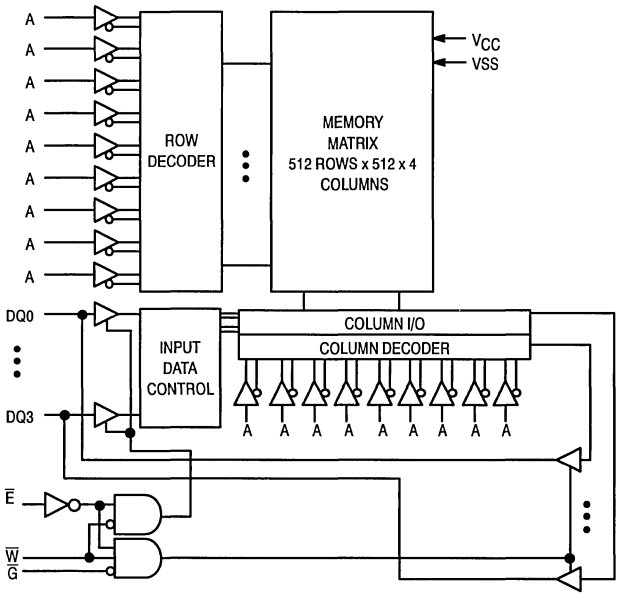
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small–outline J–leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

4/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	0.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	—	150	—	130	—	120	—	110	mA	2, 3, 4
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E} \geq V_{CC} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{CC} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V).
3. All addresses transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	—	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

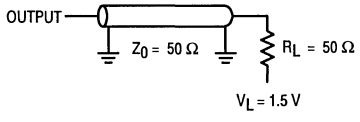


Figure 1A

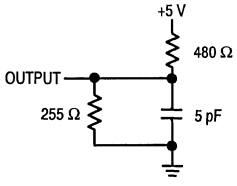
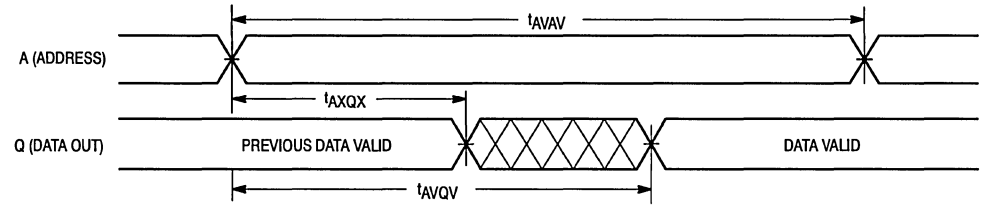


Figure 1B

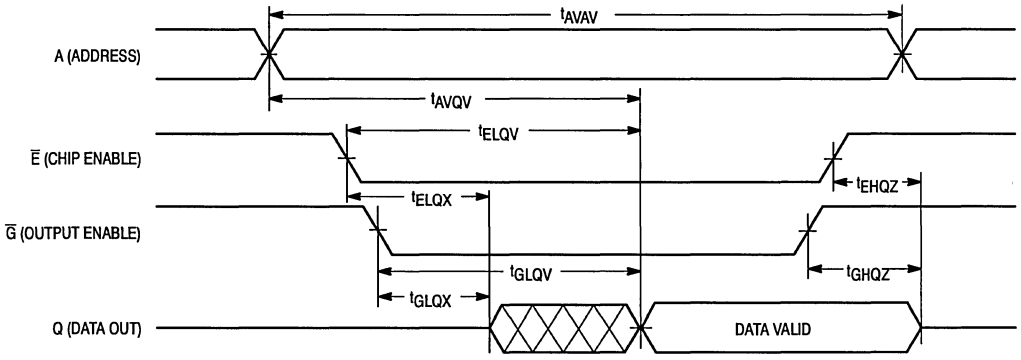
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

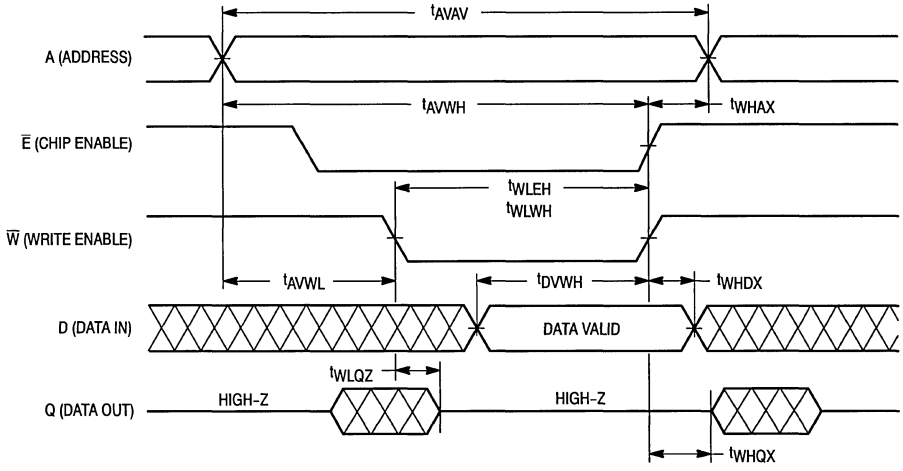


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

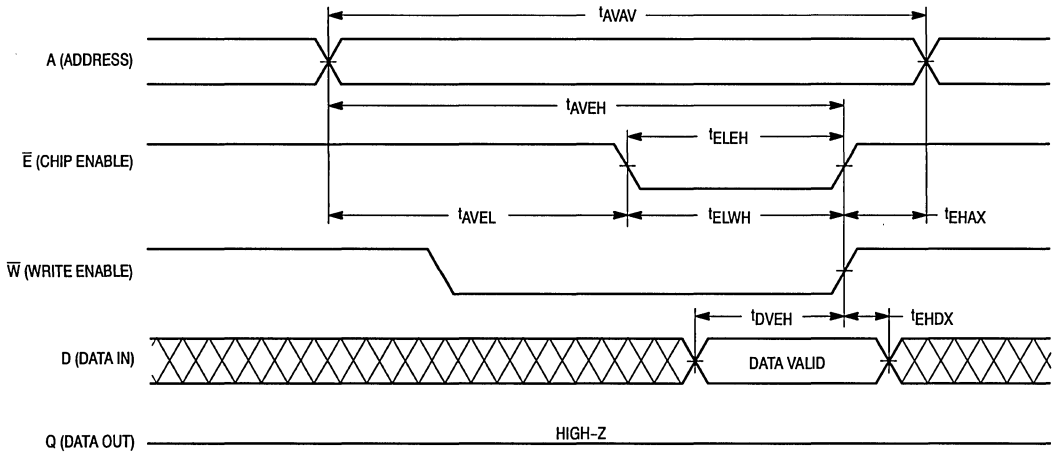


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6929–8		6929–10		6929–12		6929–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6929 WJ XX X

- MCM: Motorola Memory Prefix
- 6929: Part Number
- WJ: Package (WJ = 400 mil SOJ)
- XX: Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- X: Shipping Method (R = Tape and Reel, Blank = Rails)

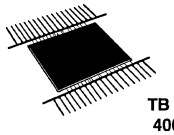
Full Part Numbers — MCM6929WJ8, MCM6929WJ8R, MCM6929WJ10, MCM6929WJ10R, MCM6929WJ12, MCM6929WJ12R, MCM6929WJ15, MCM6929WJ15R

MCM101524

2

Product Preview

1M x 4 Bit Fast Static Random Access Memory with ECL I/O



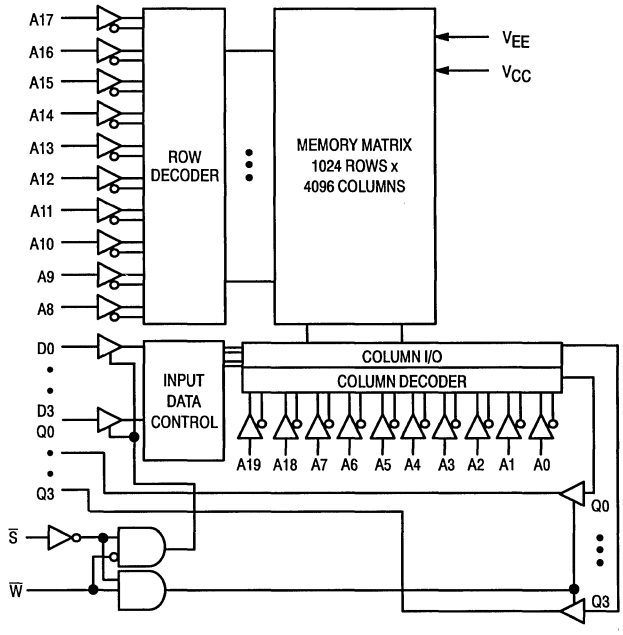
TB PACKAGE
400 MIL TAB
CASE 984A–01

The MCM101524 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits. This circuit is fabricated using high performance silicon–gate BiCMOS technology. Asynchronous design eliminates the need for external clocks or timing strobes.

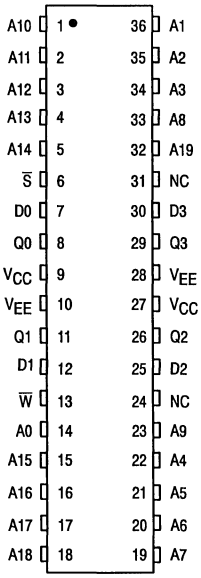
The MCM101524 is available in a 400 mil, 36 lead TAB.

- Fast Access Times: 12, 15 ns
- Equal Address and Chip Select Access Times
- Power Operation: – 195 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0 – A19 ..... Address Inputs	W ..... Write Enable
S ..... Chip Select	D0 – D3 ..... Data Input
Q0 – Q3 ..... Data Output	NC ..... No Connection
VEE ..... Power Supply	VCC ..... Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
9/94

TRUTH TABLE (X = Don't Care)

$\overline{S}$	$\overline{W}$	Operation	Data	Output	Current
H	X	Not Enabled	X	L	—
L	H	Read	X	Q	I_{EE}
L	L	Write	X	L	I_{EE}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential (to Ground)	V_{EE}	– 7.0 to + 0.5	V
Voltage Relative to V_{CC} for Any Pin Except V_{EE}	V_{in}, V_{out}	V_{EE} – 0.5 to + 0.5	V
Output Current (per I/O)	I_{out}	– 50	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 30 to + 85	°C
Operating Temperature	T_J	0 to + 60	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

2

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = – 5.2 V ± 5%, T_J = 0 to + 60°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{EE}	– 5.46	– 5.2	– 4.94	V
Input High Voltage	V_{IH}	– 1165	—	– 880	mV
Input Low Voltage	V_{IL}	– 1810	—	– 1475	mV
Output High Voltage	V_{OH}	– 1025	—	– 880	mV
Output Low Voltage	V_{OL}	– 1810	—	– 1620	mV
Input Low Current	I_{IL}	– 50	—	—	µA
Input High Current	I_{IH}	—	—	220	µA
Chip Select Input Low Current	$I_{IL(CS)}$	0.5	—	170	µA
Operating Power Supply Current: t_{AVAV} = 20 ns (All Outputs Open)*	I_{EE}	—	—	– 195	mA
Quiescent Power Supply Current: f_o = 0 MHz (Outputs Open)	I_{EEQ}	—	—	– 150	mA
Voltage Compensation (V_{OH})	$\Delta V_{OH}/\Delta V_{EE}$	± 35 mV/V @ – 4.94 to – 5.46 V			
Voltage Compensation (V_{OL})	$\Delta V_{OL}/\Delta V_{EE}$	± 60 mV/V @ – 4.94 to – 5.46 V			

* Address Increment

RISE/FALL TIME CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	20% to 80%	0.5	1.0	1.5	ns
Output Fall Time	t_f	20% to 80%	0.5	1.0	1.5	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address and Data	C_{in}	3.5	7	pF
	$\overline{S}$, $\overline{W}$	C_{ck}	4	7	
Output Capacitance	Q	C_{out}	4	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{EE} = – 5.2 V ± 5%, V_{CC} = 0 V, T_J = 0 to +60°C, Unless Otherwise Noted)

Input Pulse Levels ..... – 1.7 V to – 0.9 V (See Figure 1)
Input Rise/Fall Time ..... 1 ns
Input Timing Measurement Reference Level 50%
Output Timing Measurement Reference Level .. V_{OH} = – 1165 mV
V_{OL} = – 1475 mV
Output Load (AC Test Circuit) ..... See Figure 2

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM101524–12		MCM101524–15		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	ns	2, 3
Address Access Time	t_{AVQV}	—	12	—	15	ns	
Chip Select Access Time	t_{SLQV}	—	12	—	15	ns	6
Select High to Output Low	t_{SHQL}	0	8	0	9	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	ns	
Power Up Time	t_{SLIEEH}	0	—	0	—	ns	4
Power Down Time	t_{SHIEEL}	—	12	—	15	ns	4

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{S} \leq V_{IL}$).
6. Addresses valid prior to or coincident with $\overline{S}$ going low.

AC TEST CONDITIONS

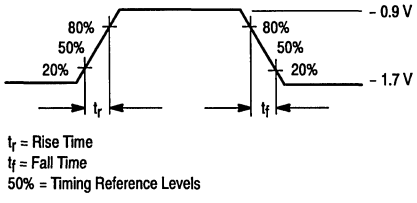


Figure 1. Input Levels

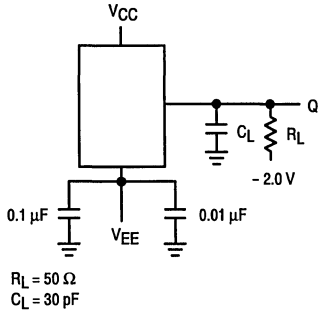
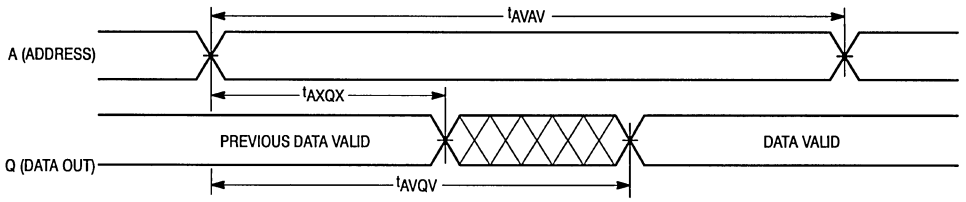
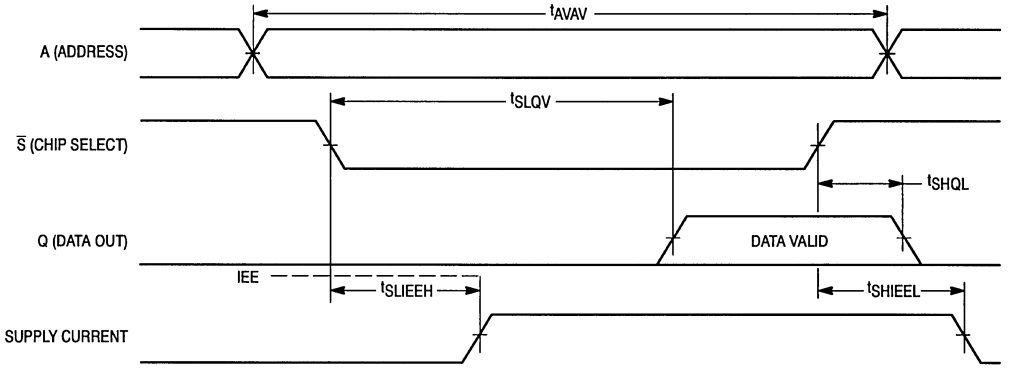


Figure 2. AC Test Circuit

READ CYCLE 1 (See Notes 1, 2, and 5)



READ CYCLE 2 (See Note 6)

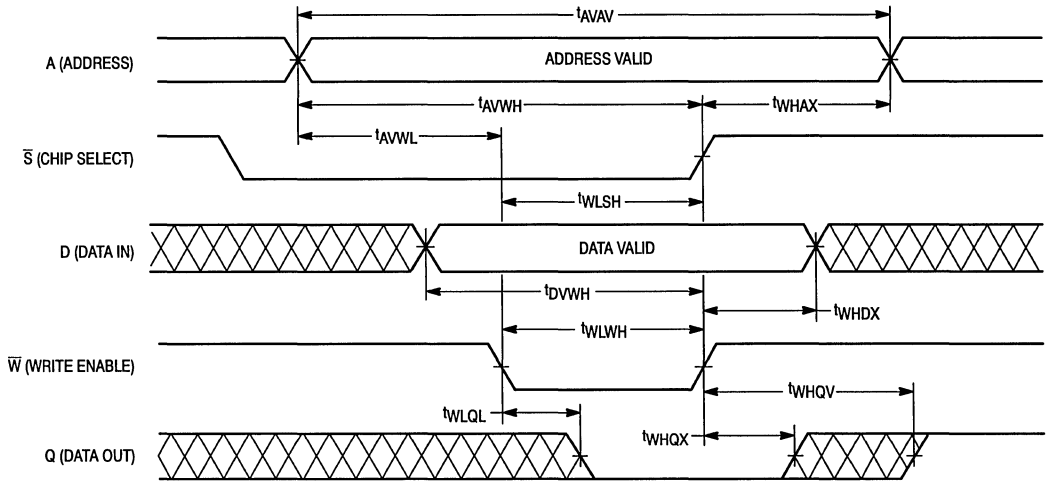


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM101524–12		MCM101524–15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	1	—	1	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLSH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	8	—	9	—	ns	
Data Hold Time	t_{WHDX}	1	—	1	—	ns	
Write High to Output Active	t_{WHQX}	4	—	4	—	ns	4
Write High to Output Valid	t_{WHQV}	—	13	—	16	ns	
Write Recovery Time	t_{WHAX}	1	—	1	—	ns	
Write Low to Output Low	t_{WLQL}	0	8	0	9	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

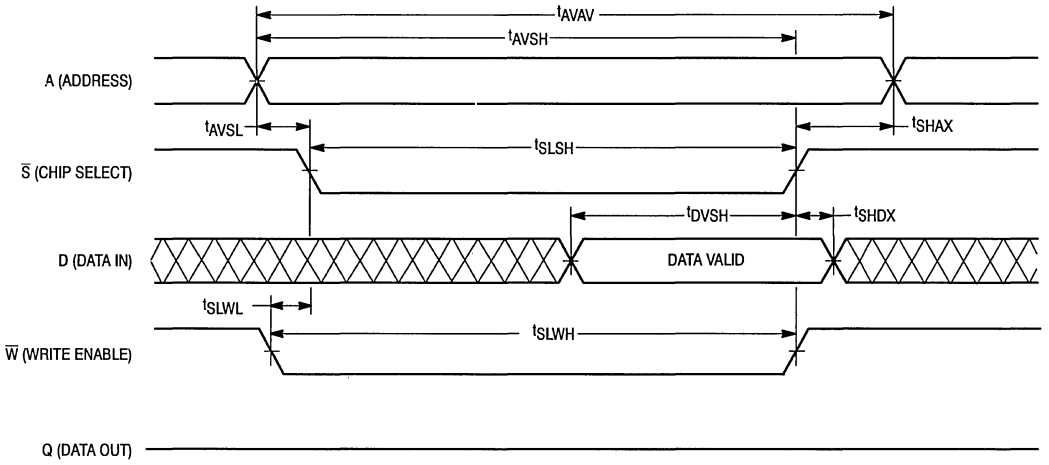


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

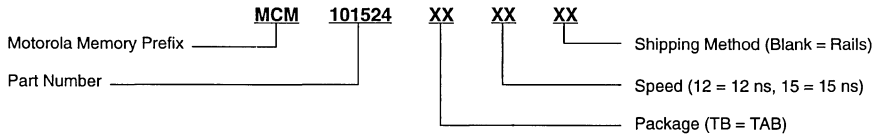
Parameter	Symbol	MCM101524–12		MCM101524–15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	1	—	1	—	ns	
Address Valid to End of Write	t_{AVSH}	9	—	10	—	ns	
Write Pulse Width ($\overline{S}$) / ($\overline{W}$)	t_{SLSH} / t_{SLWH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVSH}	8	—	9	—	ns	
Chip Select Set–Up Time	t_{SLWL}	0	—	0	—	ns	
Data Hold Time	t_{SHDX}	1	—	1	—	ns	
Write Recovery Time	t_{SHAX}	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)



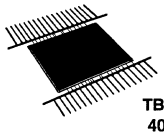
Full Part Numbers — MCM101524TB12
MCM101524TB15

MCM101525

2

Product Preview

2M x 2 Bit Fast Static Random Access Memory with ECL I/O



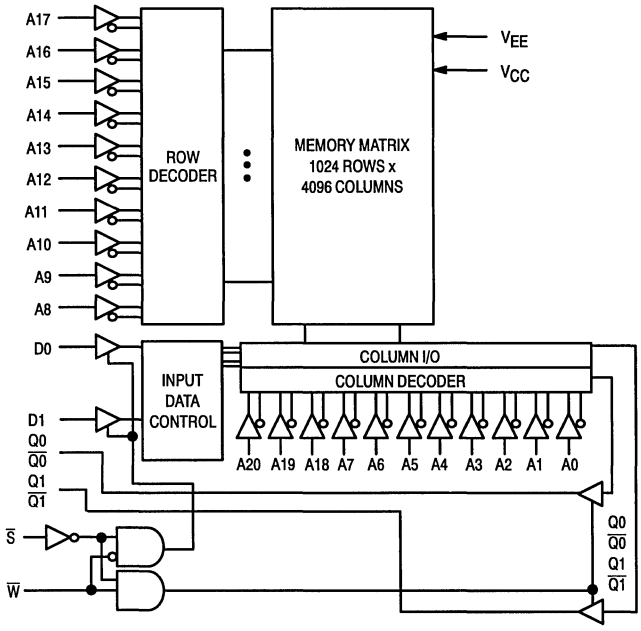
TB PACKAGE
400 MIL TAB
CASE 984A–01

The MCM101525 is a 4,194,304 bit static random access memory organized as 2,097,152 words of 2 bits. This device features complementary outputs. This circuit is fabricated using high performance silicon–gate BiCMOS technology. Asynchronous design eliminates the need for external clocks or timing strobes.

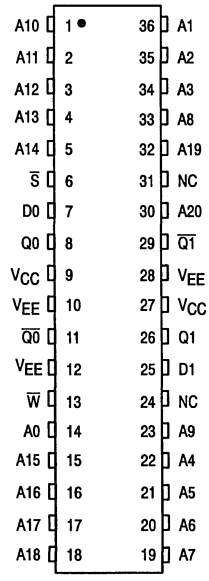
The MCM101525 is available in a 400 mil, 36 lead TAB.

- Fast Access Times: 12, 15 ns
- Equal Address and Chip Select Access Time
- Power Operation: – 195 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0 – A20 ..... Address Inputs	W ..... Write Enable
S ..... Chip Select	D0 – D1 ..... Data Input
Q0 – Q1 ..... Data Output	Q0 and Q1 .. Complementary Data Out
NC ..... No Connection	VEE ..... Power Supply
VCC ..... Ground	

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{S}$	$\overline{W}$	Operation	Data	Output	Current
H	X	Not Enabled	X	L	—
L	H	Read	X	Q/$\overline{Q}$	I_{EE}
L	L	Write	X	L	I_{EE}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential (to Ground)	V_{EE}	– 7.0 to + 0.5	V
Voltage Relative to V_{CC} for Any Pin Except V_{EE}	V_{in}, V_{out}	V_{EE} – 0.5 to + 0.5	V
Output Current (per I/O)	I_{out}	– 50	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 30 to + 85	°C
Operating Temperature	T_J	0 to + 60	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = – 5.2 V ± 5%, T_J = 0 to + 60°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{EE}	– 5.46	– 5.2	– 4.94	V
Input High Voltage	V_{IH}	– 1165	—	– 880	mV
Input Low Voltage	V_{IL}	– 1810	—	– 1475	mV
Output High Voltage	V_{OH}	– 1025	—	– 880	mV
Output Low Voltage	V_{OL}	– 1810	—	– 1620	mV
Input Low Current	I_{IL}	– 50	—	—	µA
Input High Current	I_{IH}	—	—	220	µA
Chip Select Input Low Current	$I_{IL(CS)}$	0.5	—	170	µA
Operating Power Supply Current: t_{AVAV} = 20 ns (All Outputs Open)*	I_{EE}	—	—	– 195	mA
Quiescent Power Supply Current: f_O = 0 MHz (Outputs Open)	I_{EEQ}	—	—	– 150	mA
Voltage Compensation (V_{OH})	$\Delta V_{OH}/\Delta V_{EE}$	± 35 mV/V @ – 4.94 to – 5.46 V			
Voltage Compensation (V_{OL})	$\Delta V_{OL}/\Delta V_{EE}$	± 60 mV/V @ – 4.94 to – 5.46 V			

* Address Increment

RISE/FALL TIME CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	20% to 80%	0.5	1.0	1.5	ns
Output Fall Time	t_f	20% to 80%	0.5	1.0	1.5	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address and Data	C_{in}	3.5	7	pF
	$\overline{S}$, $\overline{W}$	C_{ck}	4	7	
Output Capacitance	$\overline{Q}$, Q	C_{out}	4	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{EE} = – 5.2 V ± 5%, V_{CC} = 0 V, T_J = 0 to +60°C, Unless Otherwise Noted)

Input Pulse Levels ..... – 1.7 V to – 0.9 V (See Figure 1)
Input Rise/Fall Time ..... 1 ns
Input Timing Measurement Reference Level 50%
Output Timing Measurement Reference Level .. V_{OH} = – 1165 mV
V_{OL} = – 1475 mV
Output Load (AC Test Circuit) ..... See Figure 2

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM101525–12		MCM101525–15		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	ns	2, 3
Address Access Time	t_{AVQV}	—	12	—	15	ns	
Chip Select Access Time	t_{SLQV}	—	12	—	15	ns	6
Select High to Output Low	t_{SHQL}	0	8	0	9	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	ns	
Power Up Time	t_{SLIEEH}	0	—	0	—	ns	4
Power Down Time	t_{SHIEEL}	—	12	—	15	ns	4

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{S} \leq V_{IL}$).
6. Addresses valid prior to or coincident with $\overline{S}$ going low.

AC TEST CONDITIONS

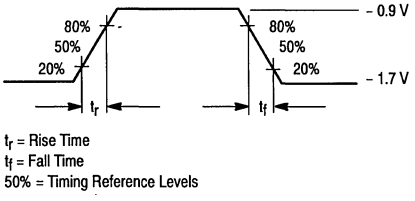


Figure 1. Input Levels

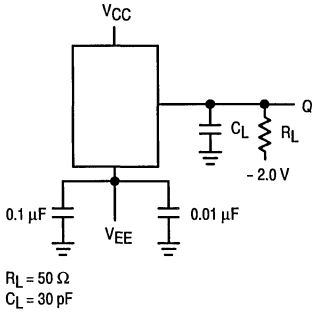
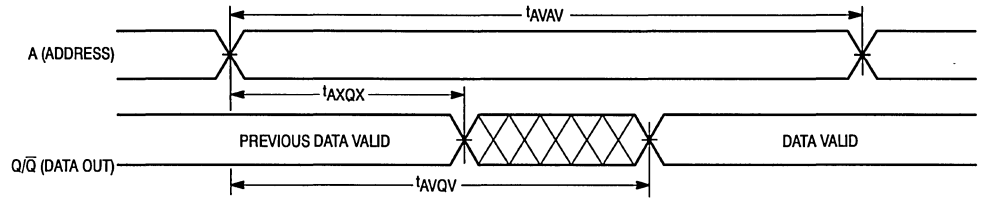
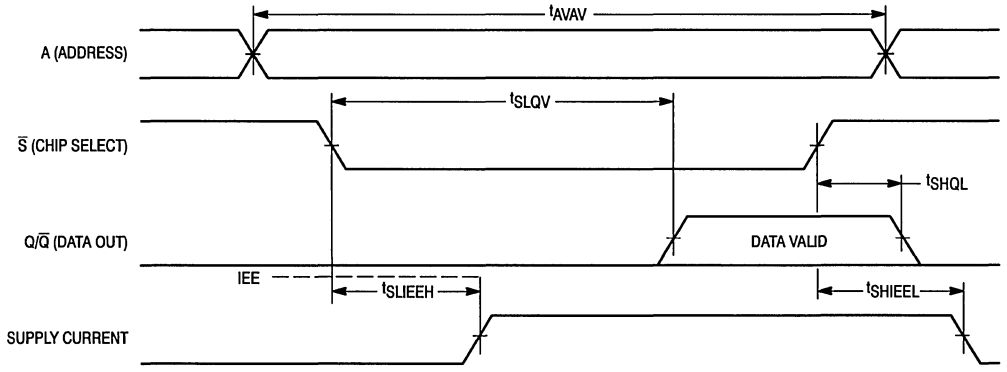


Figure 2. AC Test Circuit

READ CYCLE 1 (See Notes 1, 2, and 5)



READ CYCLE 2 (See Note 6)

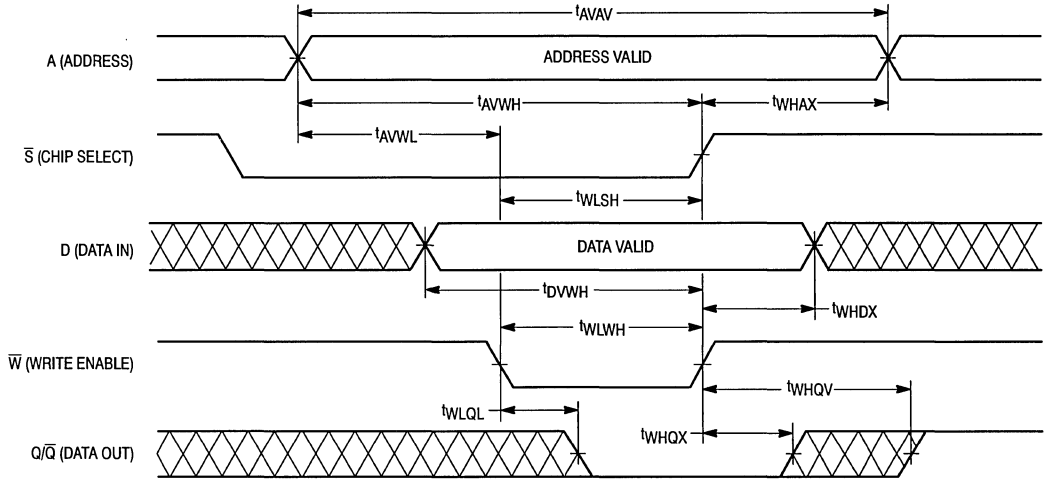


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM101525–12		MCM101525–15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	1	—	1	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLSH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	8	—	9	—	ns	
Data Hold Time	t_{WHDX}	1	—	1	—	ns	
Write High to Output Active	t_{WHQX}	4	—	4	—	ns	4
Write High to Output Valid	t_{WHQV}	—	13	—	16	ns	
Write Recovery Time	t_{WHAX}	1	—	1	—	ns	
Write Low to Output Low	t_{WLQL}	0	8	0	9	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

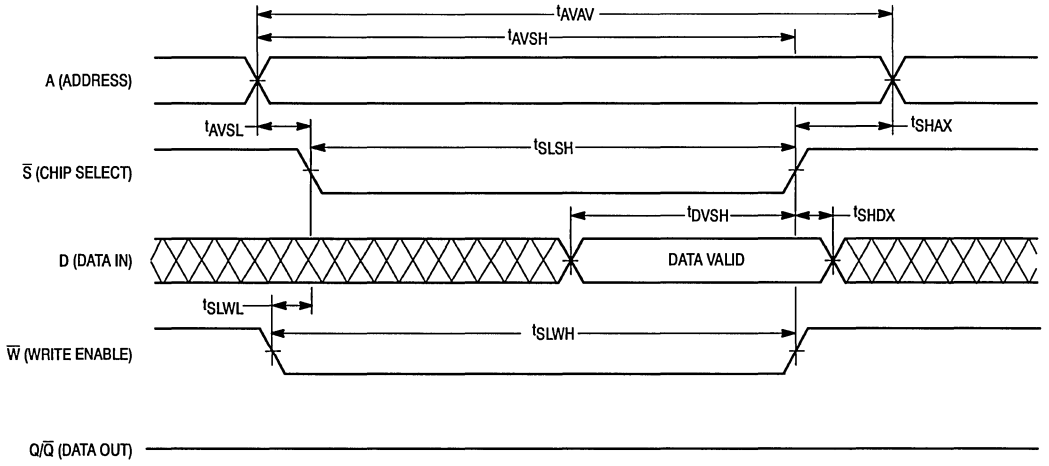


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

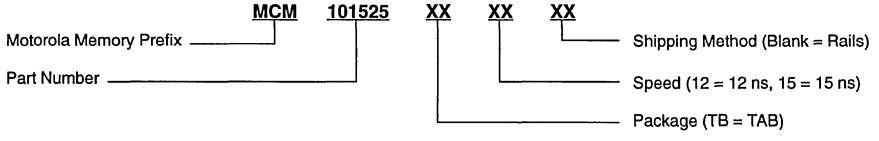
Parameter	Symbol	MCM101525–12		MCM101525–15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	1	—	1	—	ns	
Address Valid to End of Write	t_{AVSH}	9	—	10	—	ns	
Write Pulse Width ($\overline{S}$)	t_{SLSH}	8	—	9	—	ns	
Write Pulse Width ($\overline{W}$)	t_{SLWH}						
Data Valid to End of Write	t_{DVSH}	8	—	9	—	ns	
Chip Select Set–Up Time	t_{SLWL}	0	—	0	—	ns	
Data Hold Time	t_{SHDX}	1	—	1	—	ns	
Write Recovery Time	t_{SHAX}	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM101525TB12
MCM101525TB15

2

Asynchronous CMOS Fast SRAMs

3

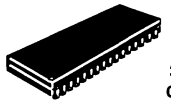
3.3 Volt Supply

5 Volt Supply

3

MCM6205D

32K x 9 Bit Fast Static RAM



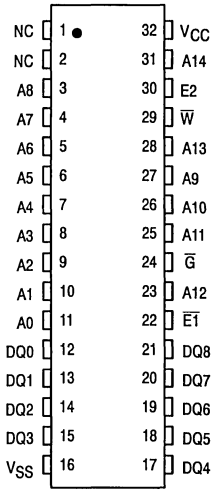
J PACKAGE
300 MIL SOJ
CASE 857–02

The MCM6205D is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

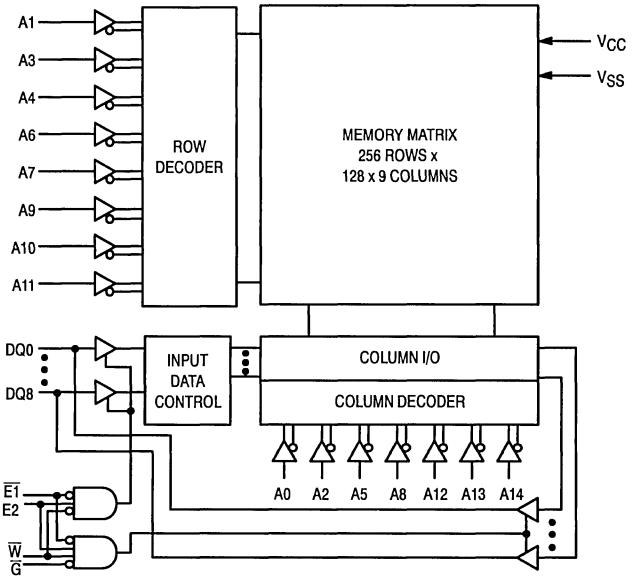
This device meets JEDEC standards for functionality and pinout, and is available in a plastic small–outline J–leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 15, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 130 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ8	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

3

REV 1
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or $\overline{G}$ = V_{IH} or E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 15	– 20	– 25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	140	135	130	mA
AC Standby Current ($\overline{E1}$ = V_{IH}, or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	40	40	35	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ ≥ V_{CC} – 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	MCM6205D–15		MCM6205D–20		MCM6205D–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	—	25	ns	4
Output Enable Access Time	t_{GLQV}	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	8	0	9	0	10	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	7	0	8	0	10	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

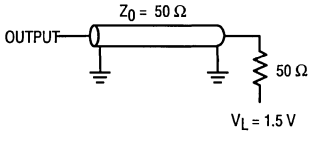


Figure 1A

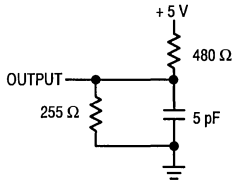
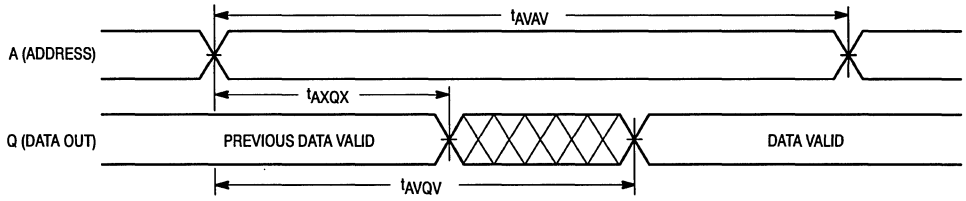


Figure 1B

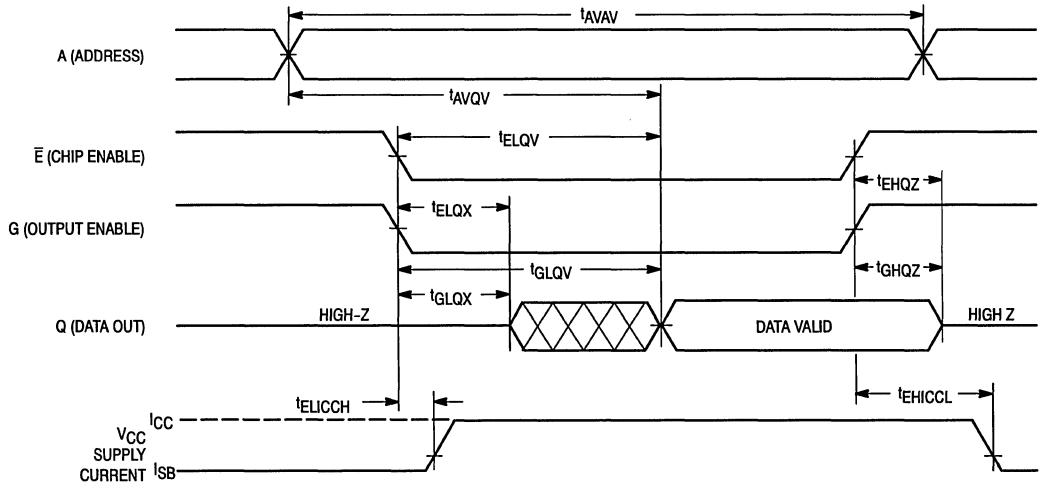
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

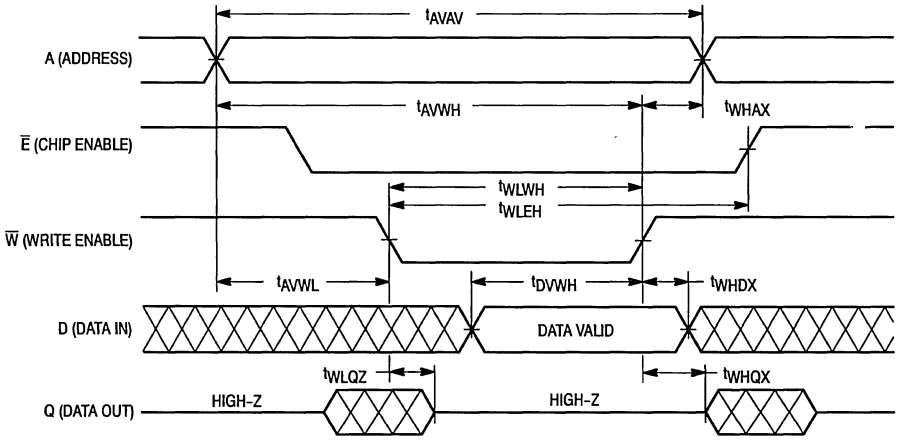


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6205D–15		MCM6205D–20		MCM6205D–25		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	0	8	0	10	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

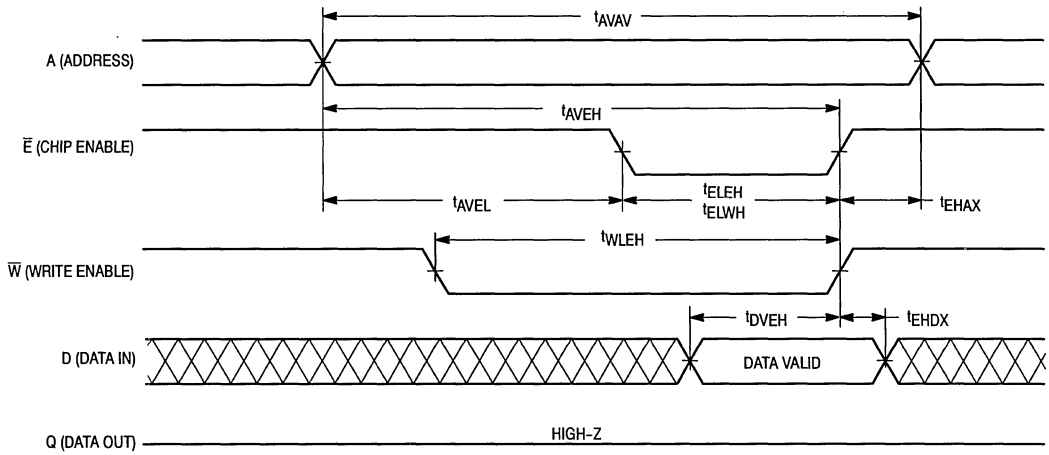


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6205D–15		MCM6205D–20		MCM6205D–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	12	—	15	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6205D X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6205DJ15, MCM6205DJ15R2, MCM6205DJ20, MCM6205DJ20R2, MCM6205DJ25, MCM6205DJ25R2

MCM6206BA

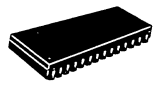
Product Preview

32K x 8 Bit Fast Static RAM

The MCM6206BA is fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

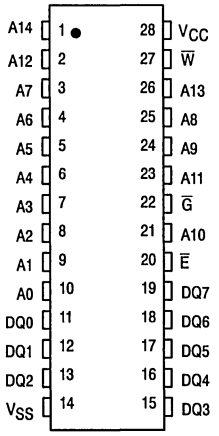
This device meets JEDEC standards for functionality and pinout, and is available in plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20 and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 125 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output



J PACKAGE
300 MIL SOJ
CASE
810B–03

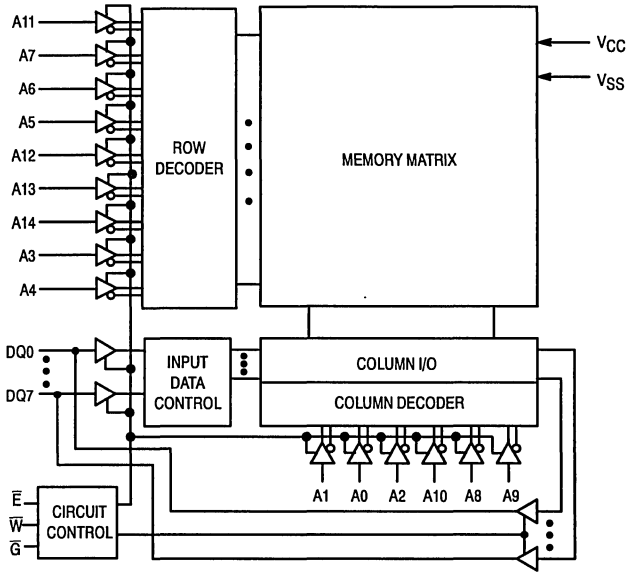
PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	H	Output Disabled	I_{CCA}	High–Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	140	135	130	125	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	40	35	35	30	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	10	10	10	10	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	ns	3
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	4,5,6
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	7	0	8	0	9	0	10	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

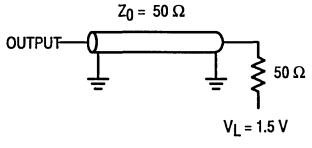


Figure 1A

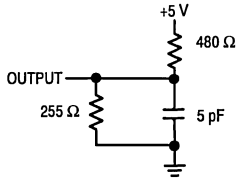


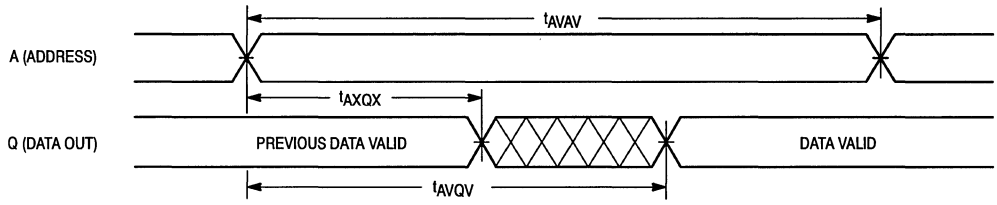
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

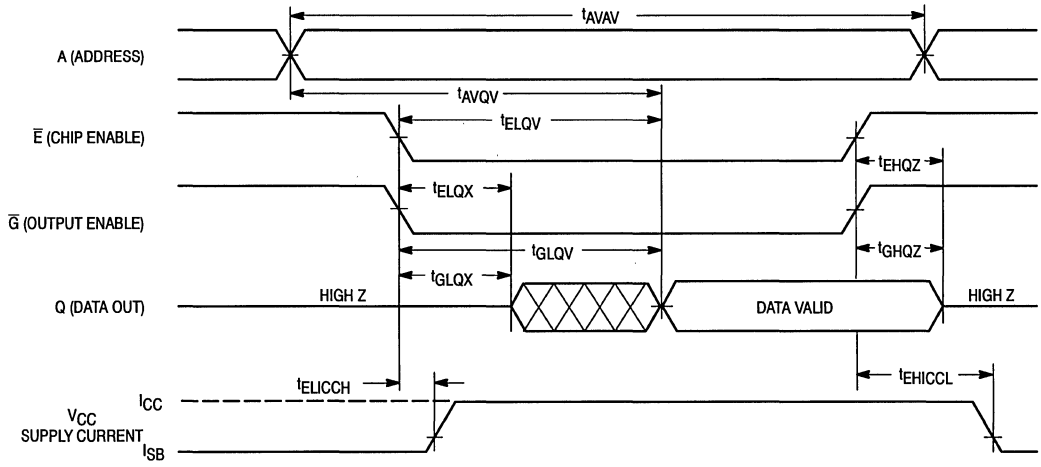
3

READ CYCLE 1 (See Note 7)



3

READ CYCLE 2 (See Note 3)

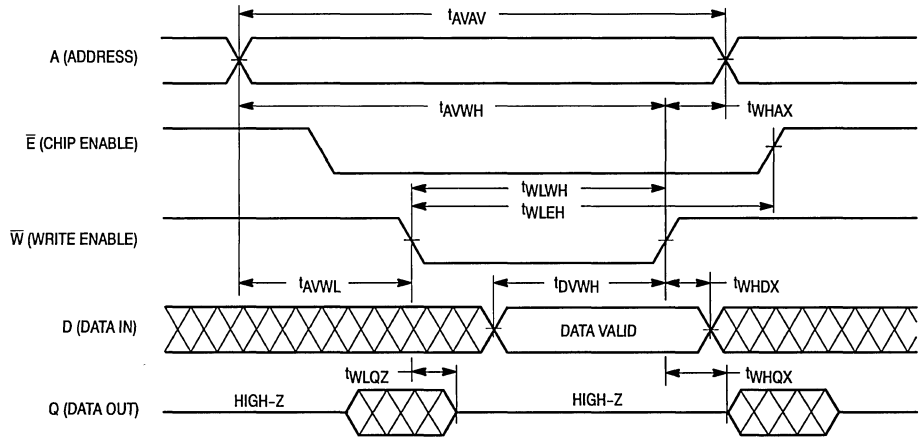


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	10	—	10	—	12	—	15	—	ns	4
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	6	0	7	0	8	0	10	ns	5,6,7
Write High to Output Active	t_{WHQX}	2	—	2	—	2	—	2	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

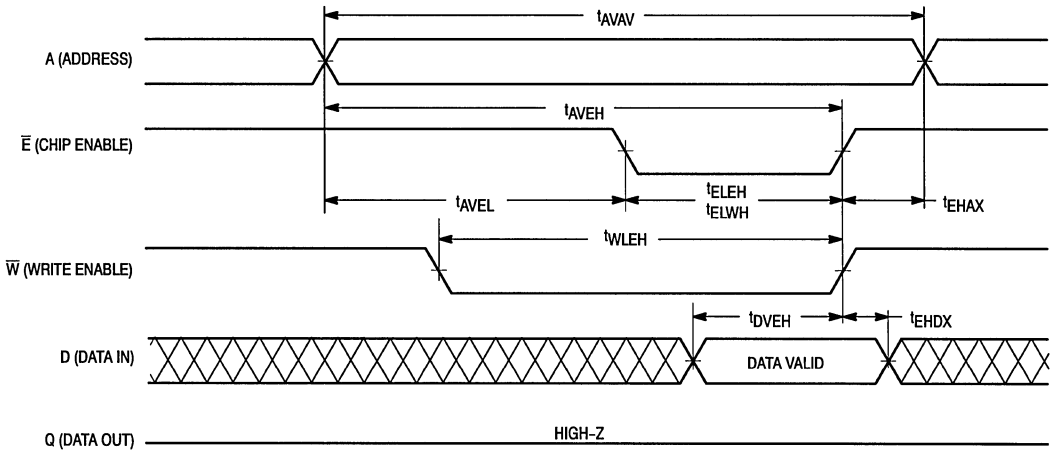


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol	-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	10	—	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	9	—	10	—	12	—	15	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206BA EJ XX X

- MCM — Motorola Memory Prefix
- 6206BA — Part Number
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)
- EJ — Package (J = 300 mil SOJ, E = Evolutionary Pinout)
- X — Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6206BAEJ12 MCM6206BAEJ12R
MCM6206BAEJ15 MCM6206BAEJ15R
MCM6206BAEJ20 MCM6206BAEJ20R
MCM6206BAEJ25 MCM6206BAEJ25R

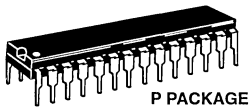
MCM6206D

32K x 8 Bit Fast Static RAM

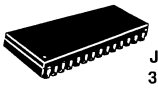
The MCM6206D is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual–in–line and plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 125 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output

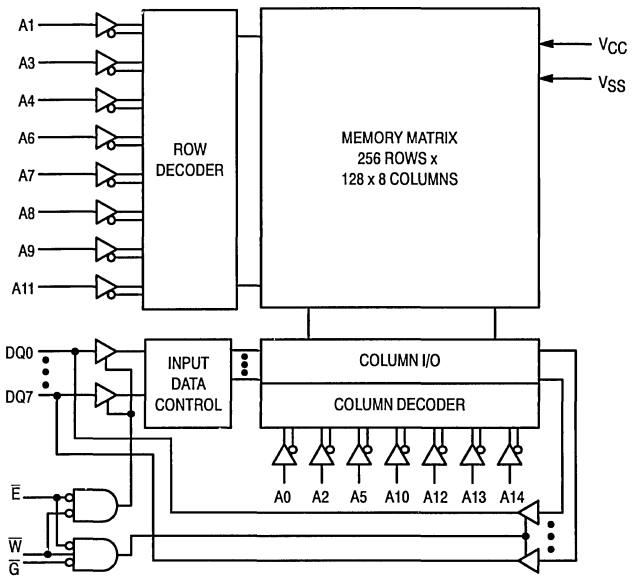


P PACKAGE
300 MIL PLASTIC
CASE 710B–01

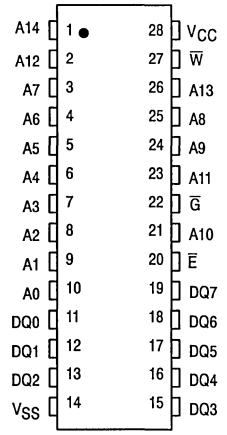


J PACKAGE
300 MIL SOJ
CASE 810B–03

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

3

REV 1
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	H	Output Disabled	I_{CCA}	High–Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	140	135	130	125	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	40	35	35	30	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	–12		–15		–20		–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	ns	3
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	4,5,6
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	7	0	8	0	9	0	10	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

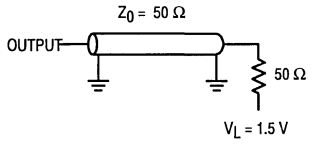


Figure 1A

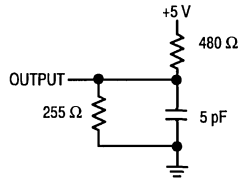
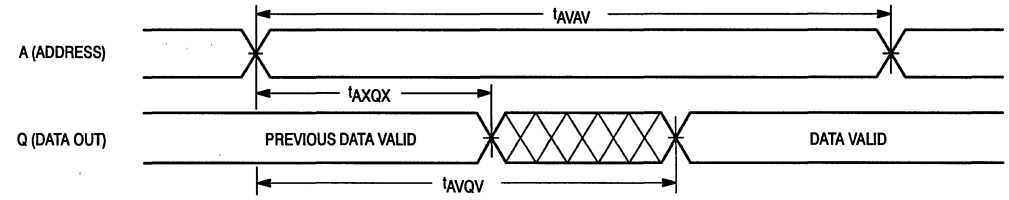


Figure 1B

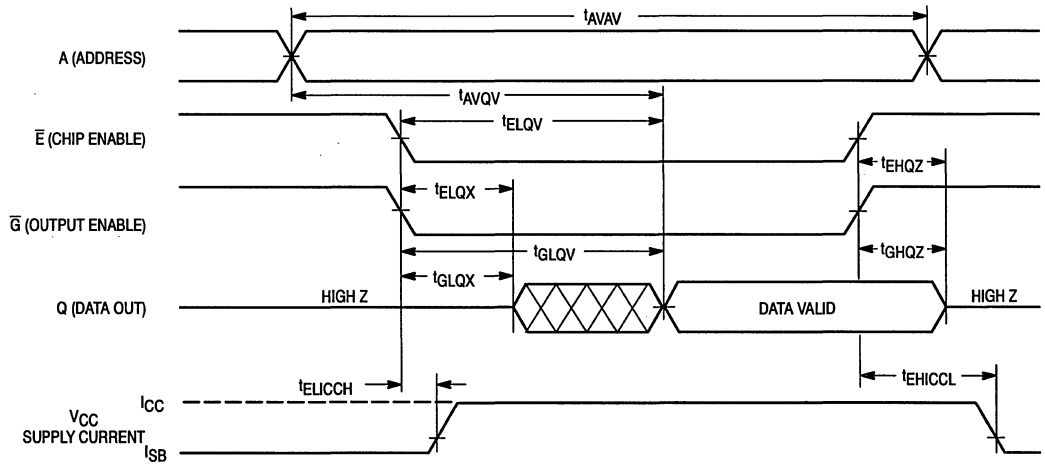
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)

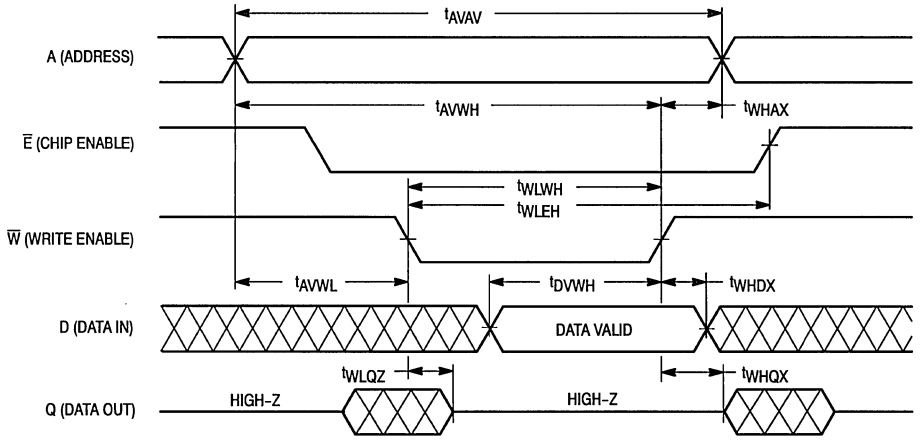


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–20		–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	10	—	10	—	12	—	15	—	ns	4
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	6	0	7	0	8	0	10	ns	5,6,7
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

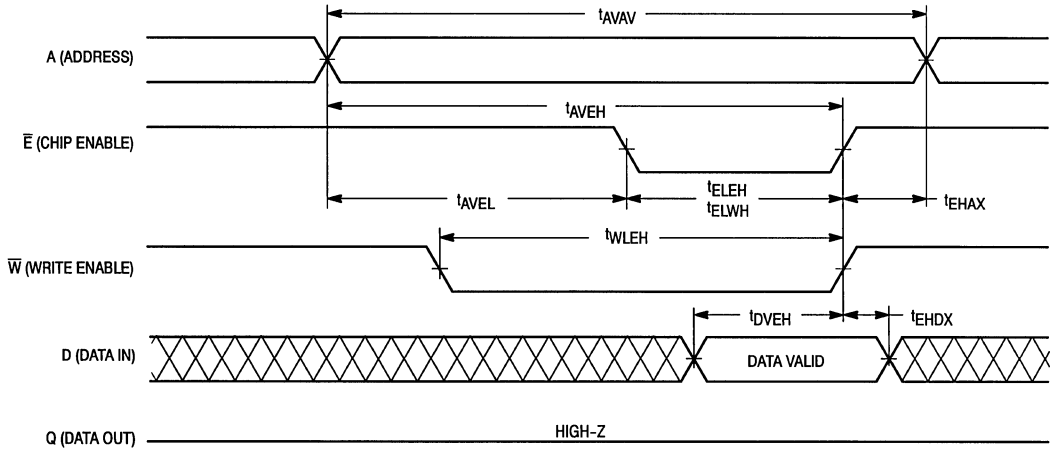


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol	-12		-15		-20		-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	ns	
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	10	—	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	9	—	10	—	12	—	15	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206D X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)
- Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)

Full Part Numbers —			
	MCM6206DP12	MCM6206DJ12	MCM6206DJ12R2
	MCM6206DP15	MCM6206DJ15	MCM6206DJ15R2
	MCM6206DP20	MCM6206DJ20	MCM6206DJ20R2
	MCM6206DP25	MCM6206DJ25	MCM6206DJ25R2

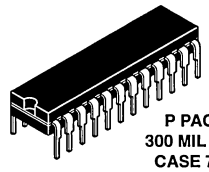
MCM6208C

64K x 4 Fast Static RAM

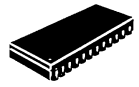
The MCM6208C is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual–in–line and plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Low Power Operation: 135 –165 mA Maximum AC
- Fully TTL Compatible — Three–State Output



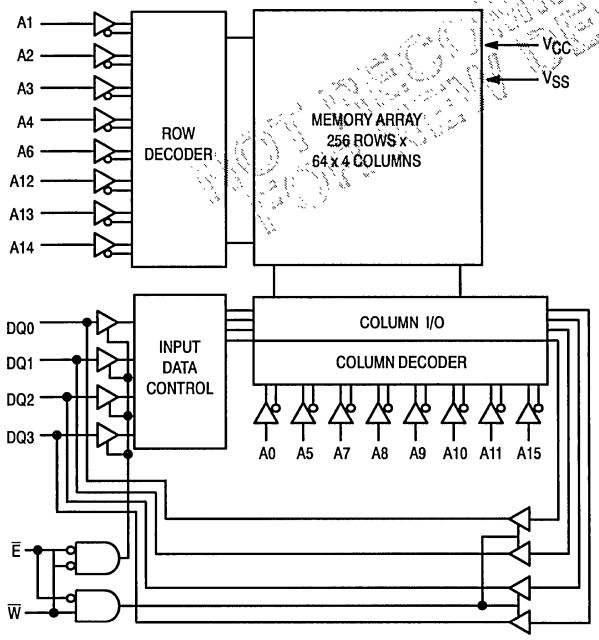
P PACKAGE
300 MIL PLASTIC
CASE 724A–01



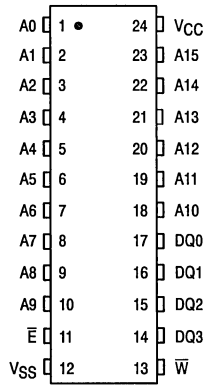
J PACKAGE
300 MIL SOJ
CASE 810A–02

3

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A15	Address Input
DQ0 – DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V*, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V, V_{CC} = Max, f = 0 MHz)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	– 35	Unit
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	165	155	145	135	135	mA
Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	55	50	45	40	40	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	–12		–15		–20		–25		–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	—	25	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	—	25	ns	3
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	12	—	—	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active1	t_{ELQX}	4	—	4	—	4	—	4	—	4	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	0	6	0	8	0	9	0	10	0	10	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	10	0	—	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E1} \le V_{IL}$).

AC TEST LOADS

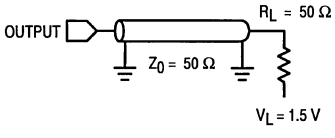


Figure 1A

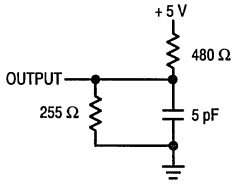
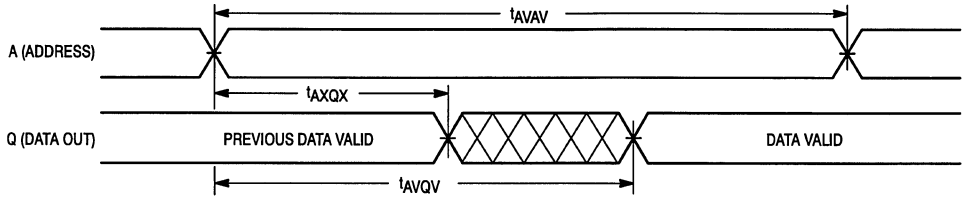


Figure 1B

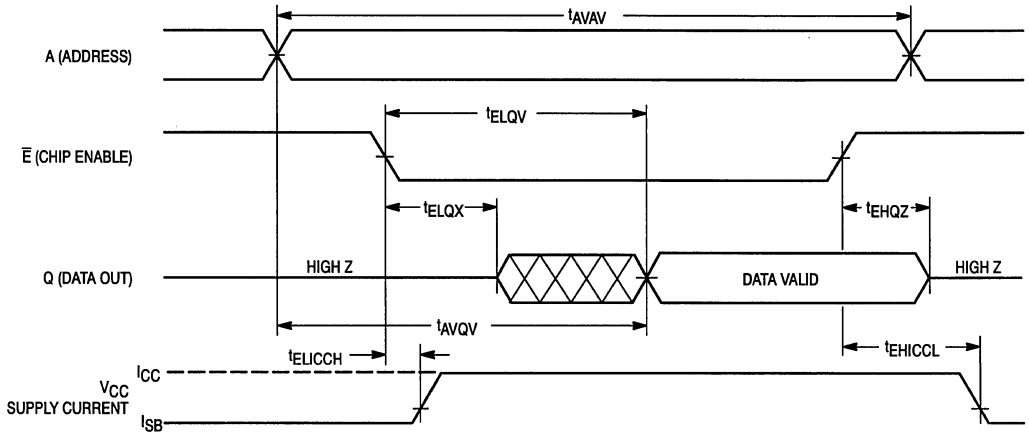
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)

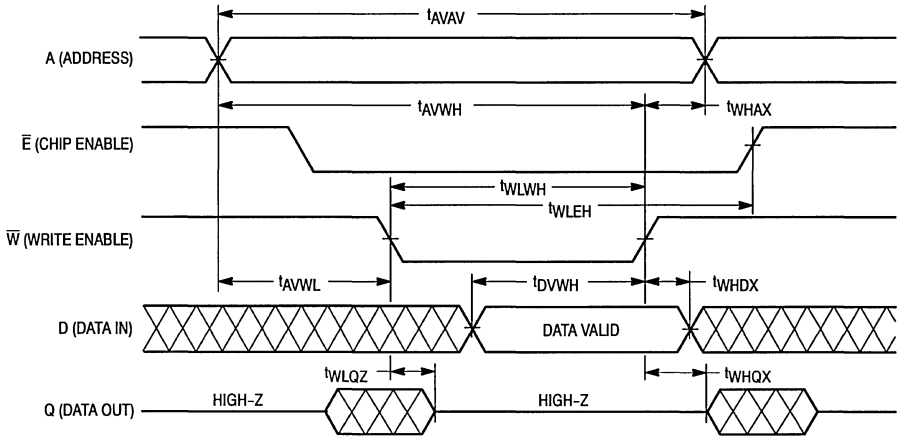


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width, $\overline{E}$ High	t_{WLWH}, t_{WLEH}	8	—	10	—	12	—	15	—	15	—	ns	
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	0	7	0	8	0	10	0	10	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	4	—	4	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

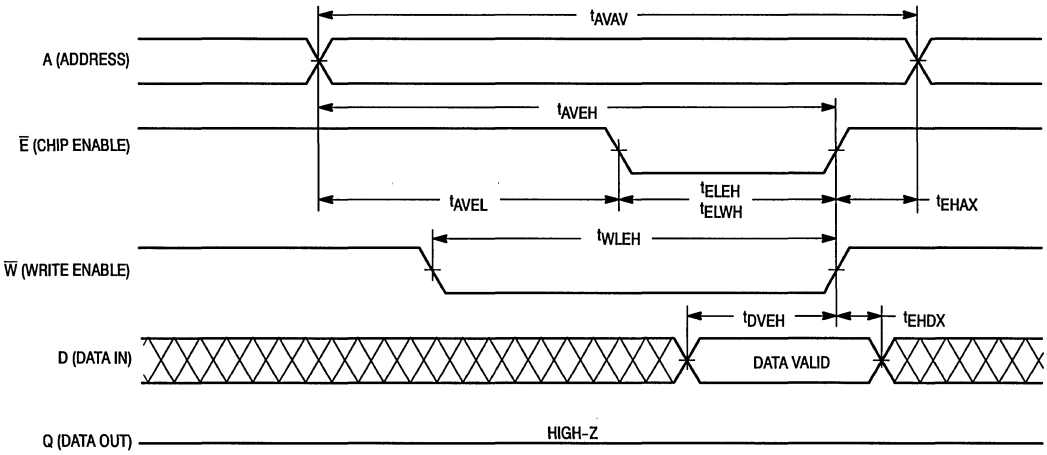


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	10	—	12	—	15	—	20	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	8	—	10	—	12	—	15	—	15	—	ns	3, 4
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6208C X XX XX

- MCM — Motorola Memory Prefix
- 6208C — Part Number
- X — Package (P = Plastic DIP, J = Plastic SOJ)
- XX — Speed (12 = 12ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —			
	MCM6208CP12	MCM6208CJ12	MCM6208CJ12R2
	MCM6208CP15	MCM6208CJ15	MCM6208CJ15R2
	MCM6208CP20	MCM6208CJ20	MCM6208CJ20R2
	MCM6208CP25	MCM6208CJ25	MCM6208CJ25R2
	MCM6208CP35	MCM6208CJ35	MCM6208CJ35R2

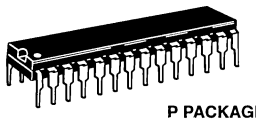
MCM6209C

64K x 4 Bit Fast Static RAM
With Output Enable

The MCM6209C is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual–in–line and plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 135 – 165 mA Maximum AC
- Fully TTL Compatible — Three–State Output

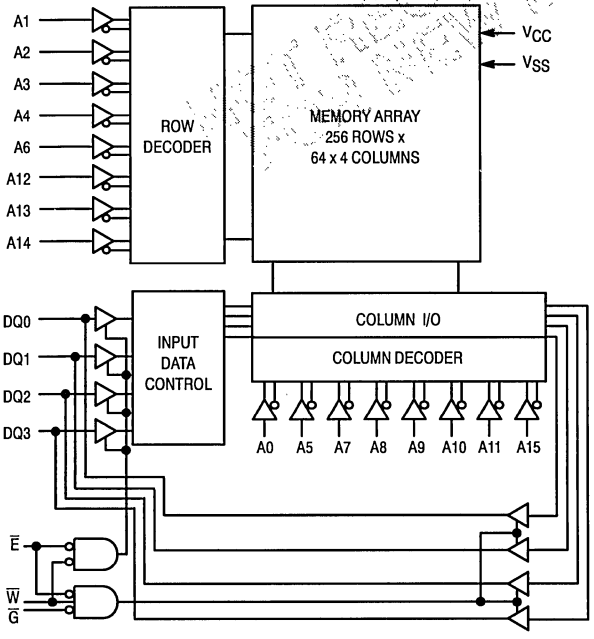


P PACKAGE
300 MIL PLASTIC
CASE 710B–01

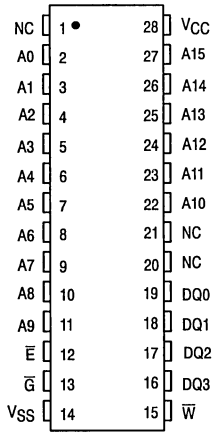
J PACKAGE
300 MIL SOJ
CASE 810B–03

3

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A15	Address Input
DQ0 – DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read
L	X	L	Write	I_{CCA}	High–Z	Write

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V*, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V, V_{CC} = Max, f = 0 MHz)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	– 35	Unit
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	165	155	145	135	130	mA
Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	55	50	45	40	35	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	–12		–15		–20		–25		–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	—	35	ns	3
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	4	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	0	6	0	8	0	9	0	10	0	10	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	10	0	—	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ ≤ V_{IL}).

AC TEST LOADS

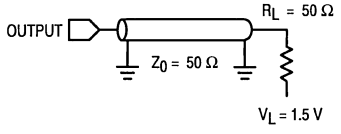


Figure 1A

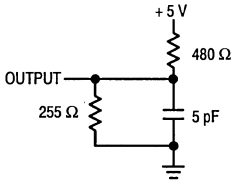
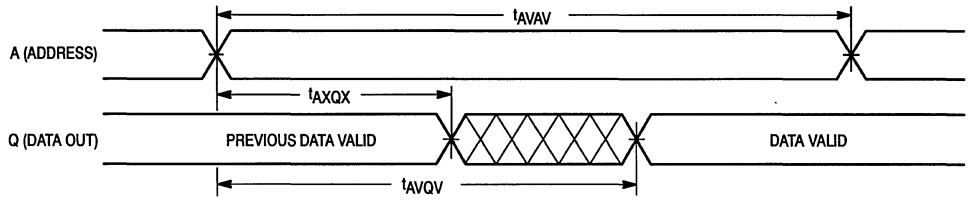


Figure 1B

TIMING LIMITS

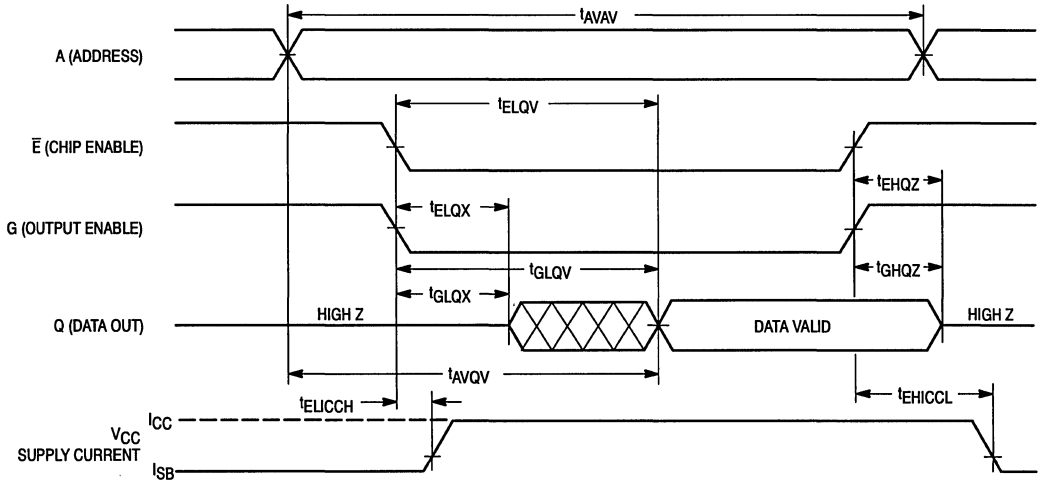
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



3

READ CYCLE 2 (See Notes 2 and 4)

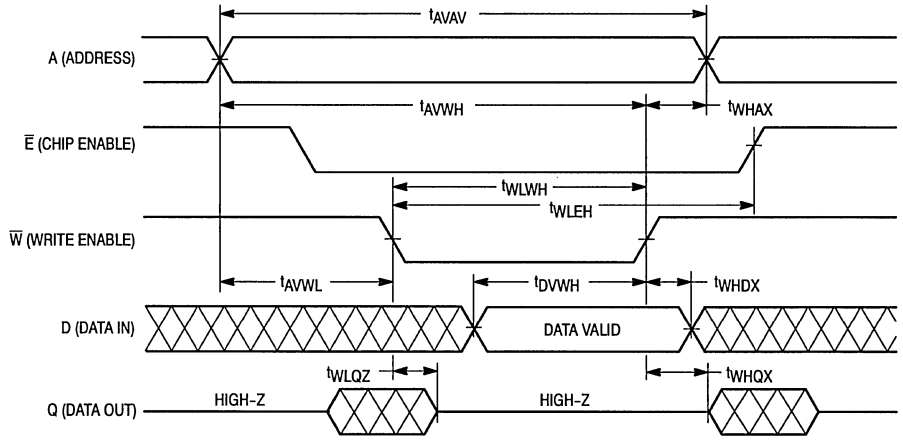


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	–12		–15		–20		–25		–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	8	—	10	—	12	—	15	—	15	—	ns	4
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	6	0	7	0	8	0	10	0	10	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	4	—	4	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 2)

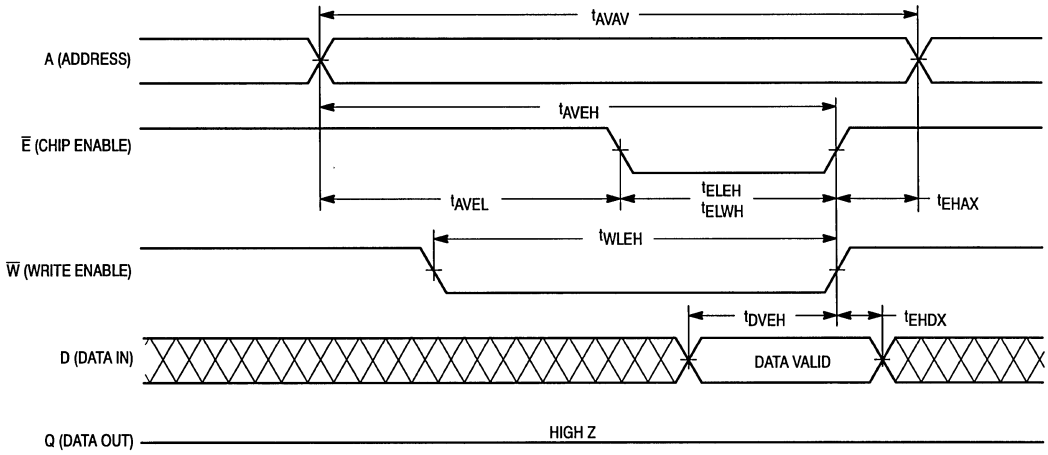


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	10	—	12	—	15	—	20	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	8	—	10	—	12	—	15	—	15	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6209C X XX XX

- MCM — Motorola Memory Prefix
- 6209C — Part Number
- XX — Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)
- X — Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers —

MCM6209CP15	MCM6209CJ15	MCM6209CJ15R2
MCM6209CP20	MCM6209CJ20	MCM6209CJ20R2
MCM6209CP25	MCM6209CJ25	MCM6209CJ25R2
MCM6209CP35	MCM6209CJ35	MCM6209CJ35R2

MCM6226A

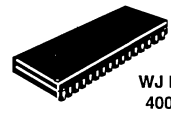
128K x 8 Bit Static Random Access Memory

The MCM6226A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226A is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6226A is available in 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 180/160/150/140 mA Maximum, Active AC

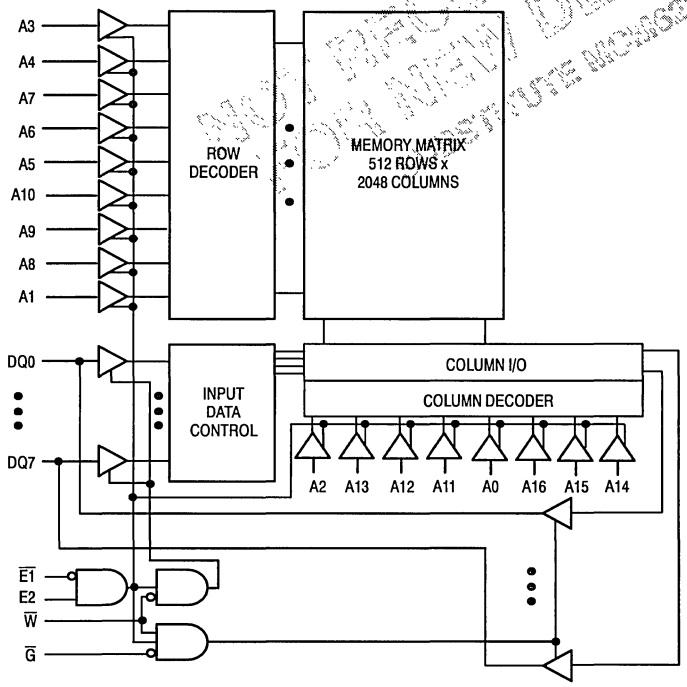


WJ PACKAGE
400 MIL SOJ
CASE 857A–02

PIN ASSIGNMENT

NC	1	32	V_{CC}
A0	2	31	A16
A1	3	30	E2
A2	4	29	$\overline{W}$
A3	5	28	A15
A4	6	27	A14
A5	7	26	A13
A6	8	25	A12
A7	9	24	$\overline{G}$
A8	10	23	A11
A9	11	22	$\overline{E1}$
A10	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
V_{SS}	16	17	DQ3

BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

REV 4
5/95

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High–Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} to 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ**	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6226A–20: t_{AVAV} = 20 ns		—	150	180	
MCM6226A–25: t_{AVAV} = 25 ns		—	135	160	
MCM6226A–35: t_{AVAV} = 35 ns		—	125	150	
MCM6226A–45: t_{AVAV} = 45 ns		—	120	140	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
**Typical values are measured at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQ	C_{in}	4	6	pF
	$\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{ck}	5	8	
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6226A–20		6226A–25		6226A–35		6226A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	4
Address Access Time	t_{AVQV}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	—	45	ns	5
Output Enable Access Time	t_{GLQV}	—	8	—	10	—	15	—	15	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	0	15	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	0	12	0	15	ns	6, 7, 8
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

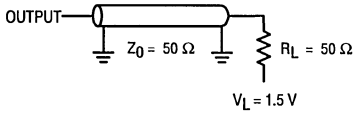


Figure 1A

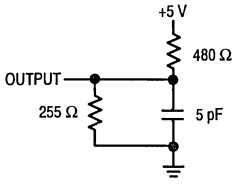
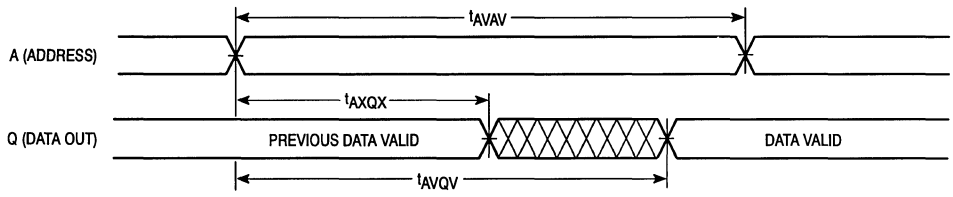


Figure 1B

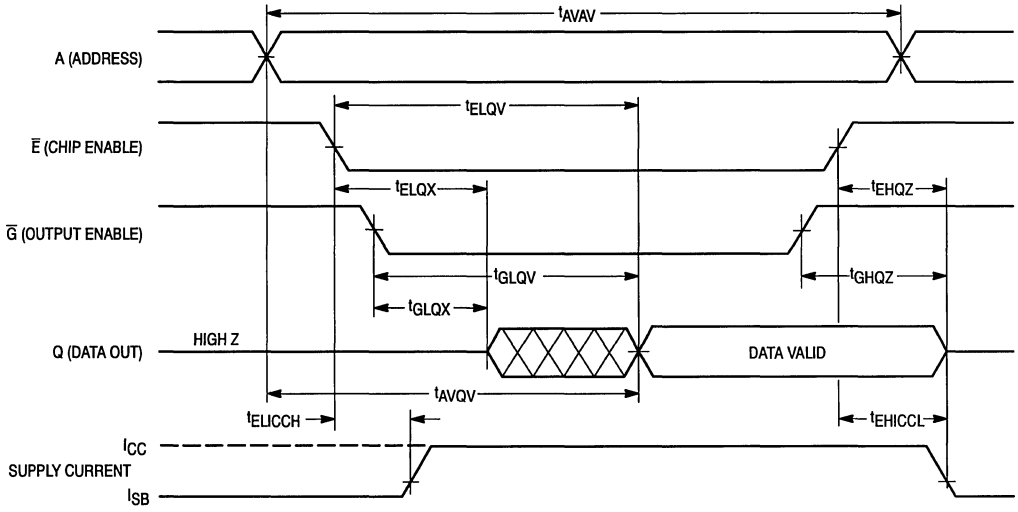
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

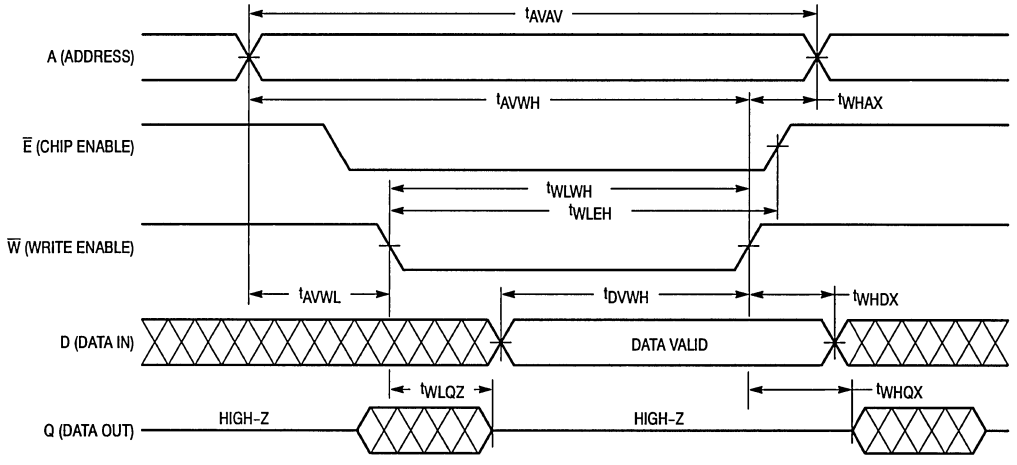


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226A–20		6226A–25		6226A–35		6226A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	0	20	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)



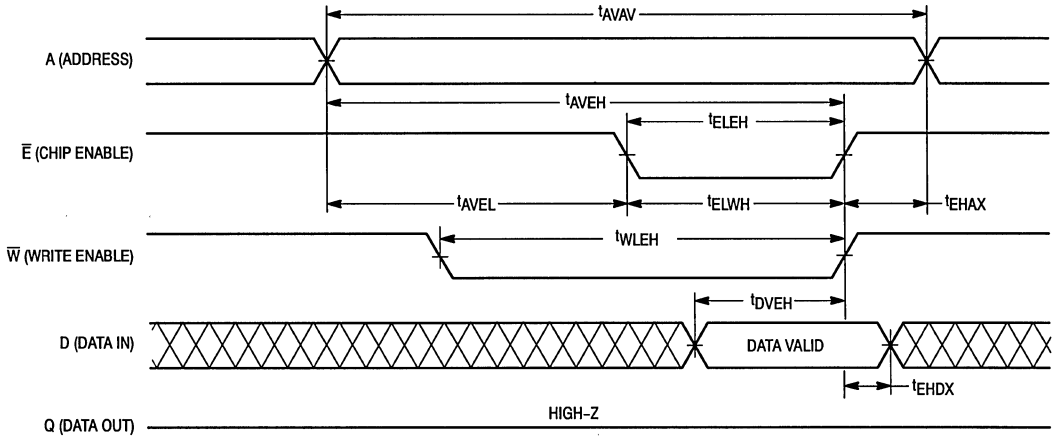
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226A–20		6226A–25		6226A–35		6226A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	25	—	ns	6, 7
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

3

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6226A WJ XX XX

- MCM — Motorola Memory Prefix
- 6226A — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6226AWJ20, MCM6226AWJ20R2, MCM6226AWJ25, MCM6226AWJ25R2, MCM6226AWJ35, MCM6226AWJ35R2, MCM6226AWJ45, MCM6226AWJ45R2

MCM6226B

128K x 8 Bit Static Random Access Memory

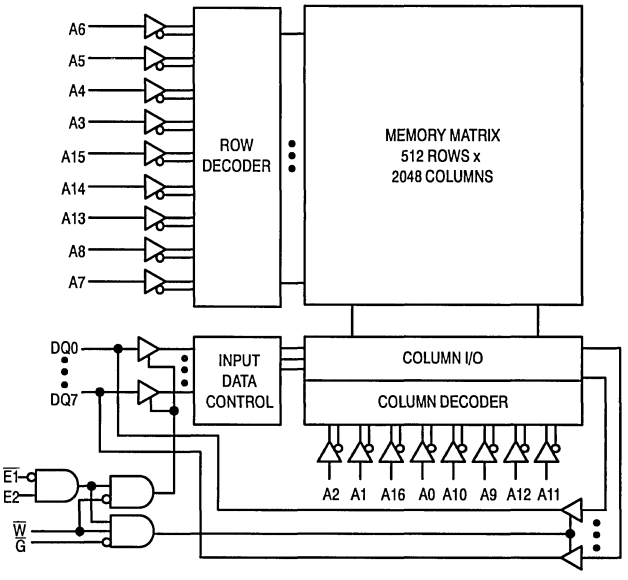
The MCM6226B is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226B is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

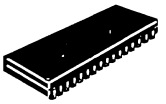
The MCM6226B is available in 300 mil and 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 130/125/120/115/110 mA Maximum, Active AC

BLOCK DIAGRAM

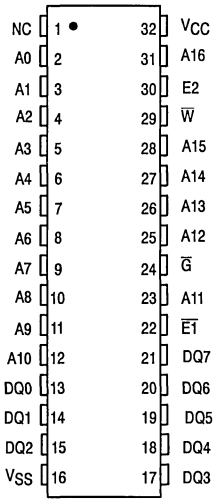


WJ PACKAGE
400 MIL SOJ
CASE 857A–02



J PACKAGE
300 MIL SOJ
CASE 857–02

PIN ASSIGNMENT



PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

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TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High–Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6226B–15: t_{AVAV} = 15 ns	I_{CCA}	—	130	mA
	MCM6226B–17: t_{AVAV} = 17 ns		—	125	
	MCM6226B–20: t_{AVAV} = 20 ns		—	120	
	MCM6226B–25: t_{AVAV} = 25 ns		—	115	
	MCM6226B–35: t_{AVAV} = 35 ns		—	110	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f ≤ f_{max})	MCM6226B–15: t_{AVAV} = 15 ns	I_{SB1}	—	40	mA
	MCM6226B–17: t_{AVAV} = 17 ns		—	35	
	MCM6226B–20: t_{AVAV} = 20 ns		—	30	
	MCM6226B–25: t_{AVAV} = 25 ns		—	25	
	MCM6226B–35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6226B–15		6226B–17		6226B–20		6226B–25		6226B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	5
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

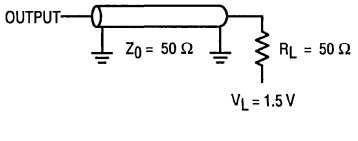


Figure 1A

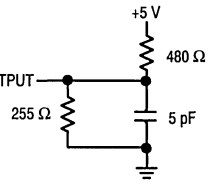
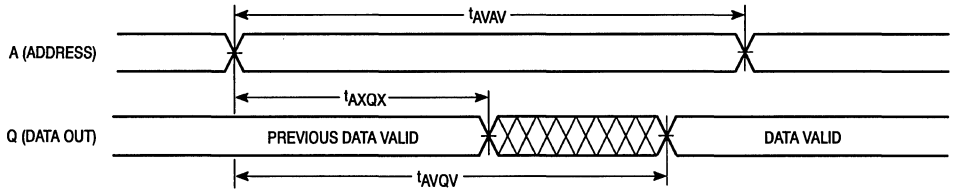


Figure 1B

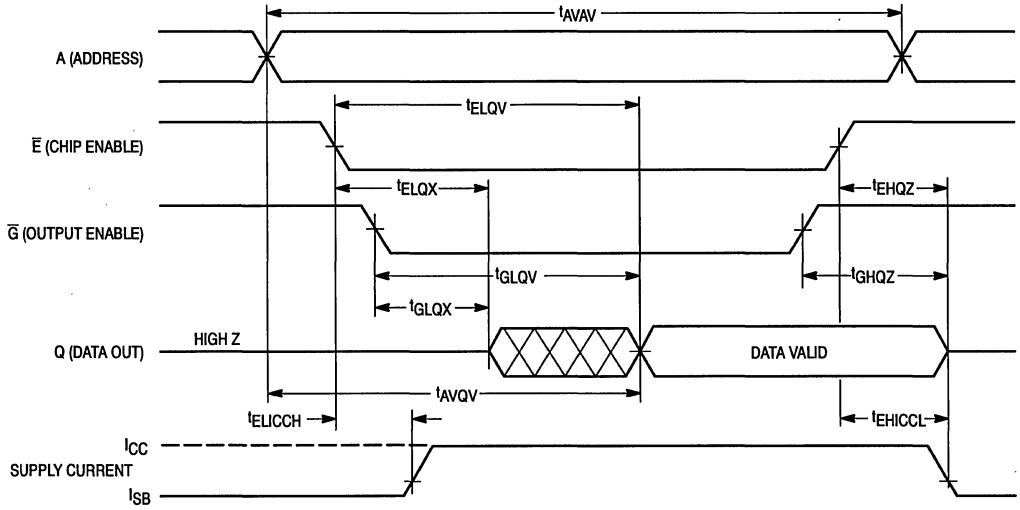
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

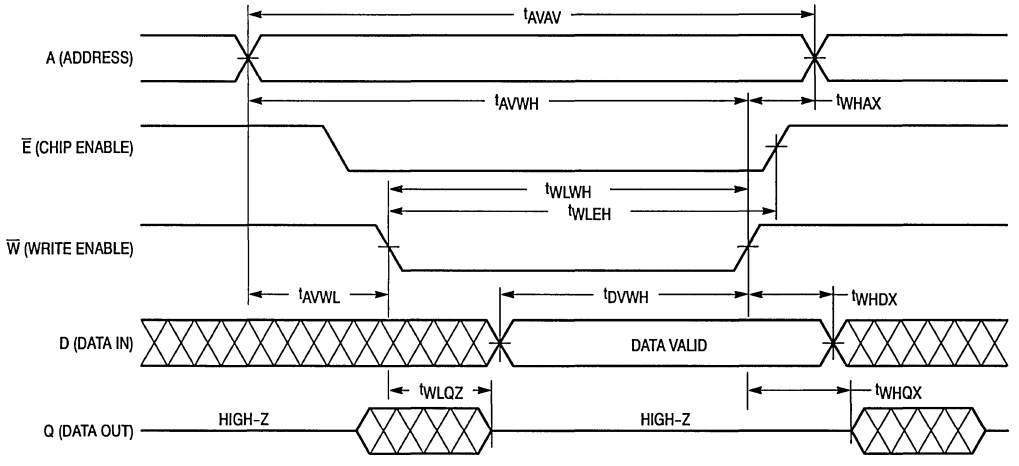


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226B–15		6226B–17		6226B–20		6226B–25		6226B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

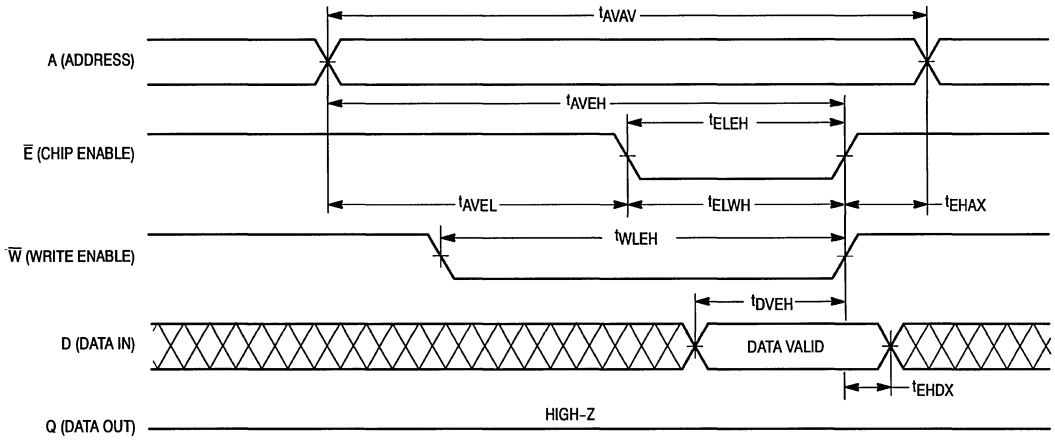


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226B–15		6226B–17		6226B–20		6226B–25		6226B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	6, 7
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6226B X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (WJ = 400 mil SOJ, J = 300 mil SOJ)

Full Part Numbers —				
	MCM6226BJ15	MCM6226BJ15R2	MCM6226BWJ15	MCM6226BWJ15R2
	MCM6226BJ17	MCM6226BJ17R2	MCM6226BWJ17	MCM6226BWJ17R2
	MCM6226BJ20	MCM6226BJ20R2	MCM6226BWJ20	MCM6226BWJ20R2
	MCM6226BJ25	MCM6226BJ25R2	MCM6226BWJ25	MCM6226BWJ25R2
	MCM6226BJ35	MCM6226BJ35R2	MCM6226BWJ35	MCM6226BWJ35R2

MCM6226BA

Product Preview

128K x 8 Bit Static Random Access Memory

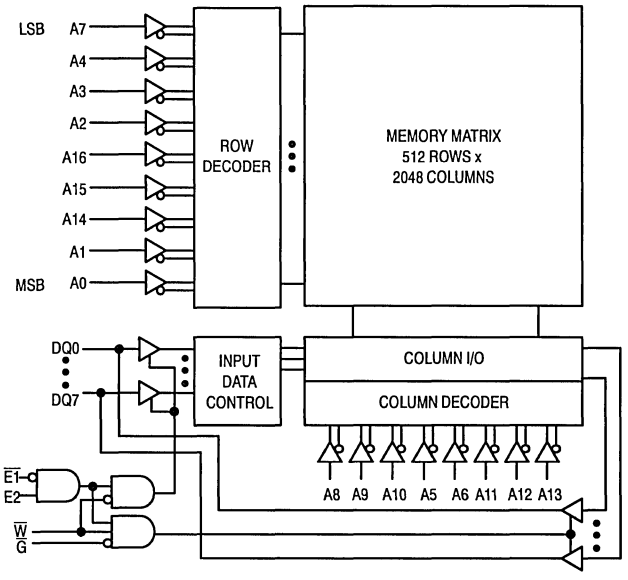
The MCM6226BA is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226BA is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

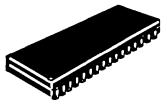
The MCM6226BA is available in 300 mil and 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 180/170/160/140/115 mA Maximum, Active AC

BLOCK DIAGRAM

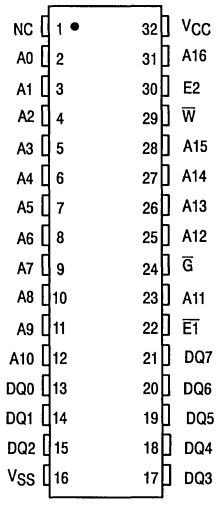


WJ PACKAGE
400 MIL SOJ
CASE 857A–02



J PACKAGE
300 MIL SOJ
CASE 857–02

PIN ASSIGNMENT



PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High–Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, all inputs = V_{IL} or V_{IH}, V_{IL} = 0, V_{IH} ≥ 3 V, cycle time ≥ t_{AVAV} min, V_{CC} = max)	MCM6226BA–15: t_{AVAV} = 15 ns	I_{CCA}	—	180	mA
	MCM6226BA–17: t_{AVAV} = 17 ns		—	170	
	MCM6226BA–20: t_{AVAV} = 20 ns		—	150	
	MCM6226BA–25: t_{AVAV} = 25 ns		—	130	
	MCM6226BA–35: t_{AVAV} = 35 ns		—	120	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f = f_{max})	MCM6226BA–15: t_{AVAV} = 15 ns	I_{SB1}	—	45	mA
	MCM6226BA–17: t_{AVAV} = 17 ns		—	40	
	MCM6226BA–20: t_{AVAV} = 20 ns		—	35	
	MCM6226BA–25: t_{AVAV} = 25 ns		—	30	
	MCM6226BA–35: t_{AVAV} = 35 ns		—	25	
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	6226BA–15		6226BA–17		6226BA–20		6226BA–25		6226BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	5
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

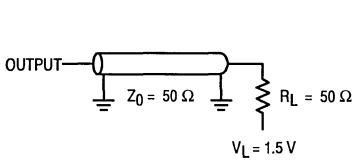


Figure 1A

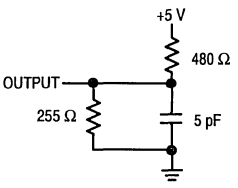
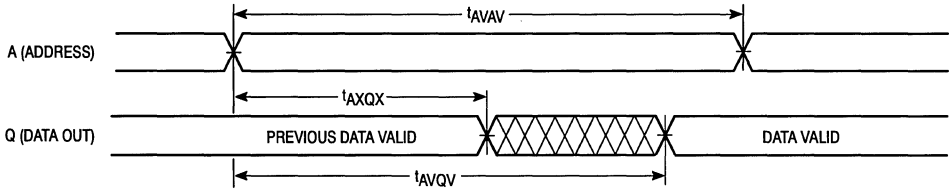


Figure 1B

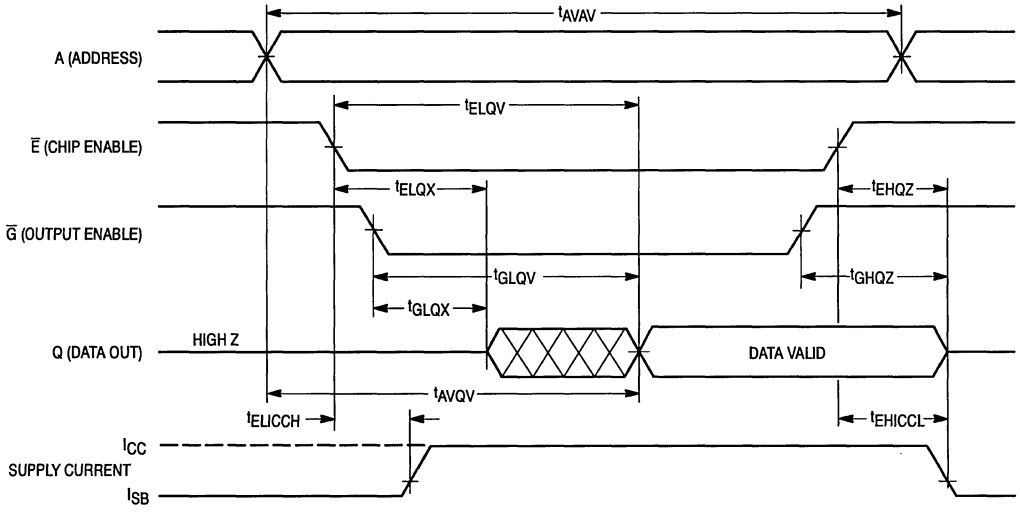
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

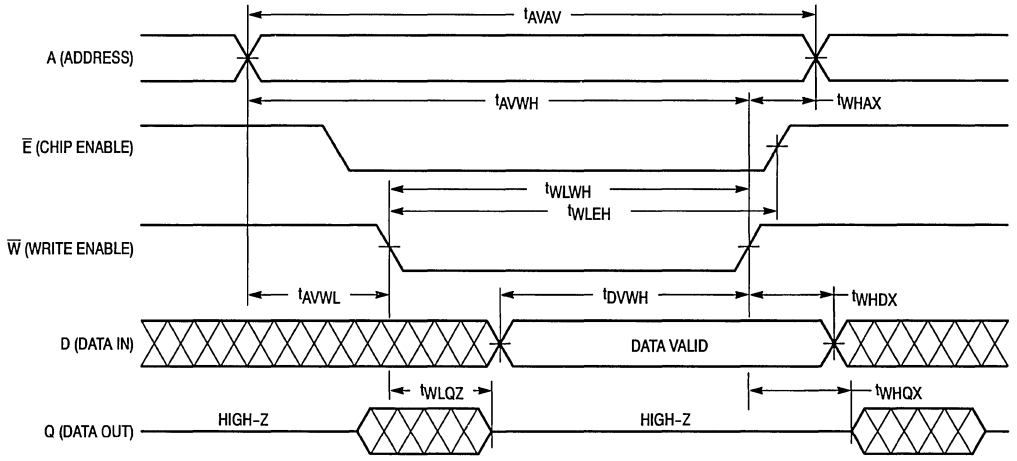


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226BA–15		6226BA–17		6226BA–20		6226BA–25		6226BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

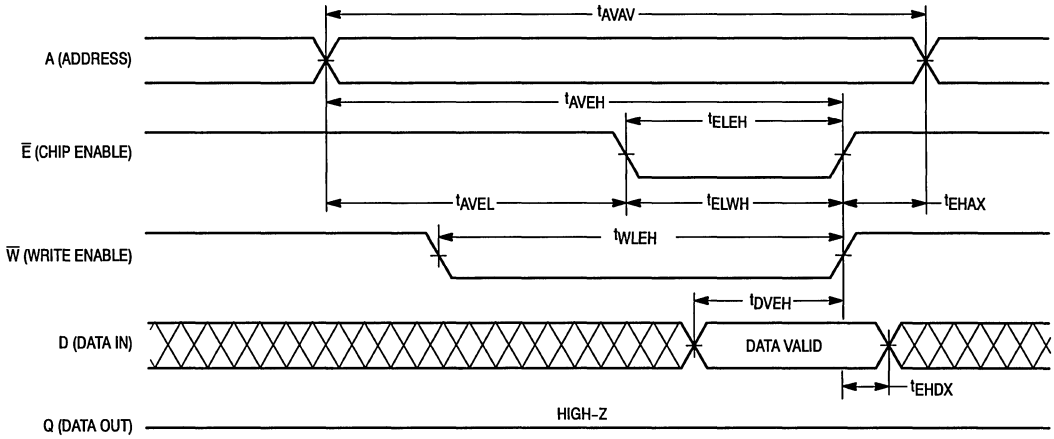


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol	6226BA–15		6226BA–17		6226BA–20		6226BA–25		6226BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	14	—	15	—	17	—	20	—	ns	6, 7
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	8	—	9	—	9	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6226BA X XX XX

- MCM: Motorola Memory Prefix
- 6226BA: Part Number
- X: Package (WJ = 400 mil SOJ, J = 300 mil SOJ)
- XX: Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX: Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM6226BAJ15	MCM6226BAJ15R2	MCM6226BAWJ15	MCM6226BAWJ15R2
MCM6226BAJ17	MCM6226BAJ17R2	MCM6226BAWJ17	MCM6226BAWJ17R2
MCM6226BAJ20	MCM6226BAJ20R2	MCM6226BAWJ20	MCM6226BAWJ20R2
MCM6226BAJ25	MCM6226BAJ25R2	MCM6226BAWJ25	MCM6226BAWJ25R2
MCM6226BAJ35	MCM6226BAJ35R2	MCM6226BAWJ35	MCM6226BAWJ35R2

MCM6226BB

Product Preview

128K x 8 Bit Static Random Access Memory

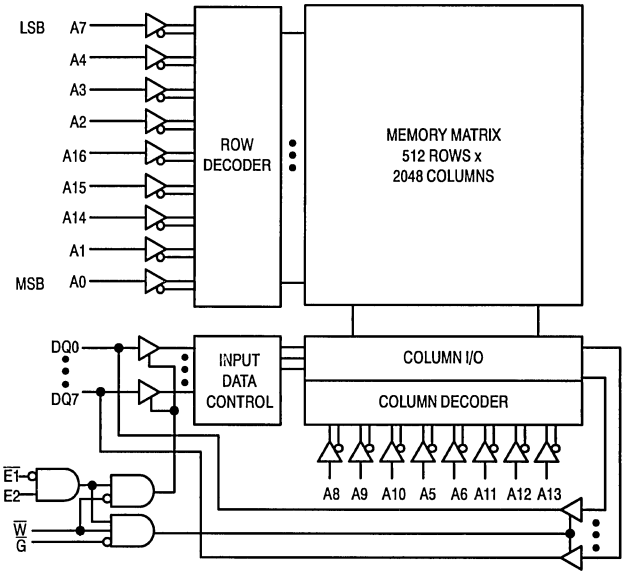
The MCM6226BB is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226BB is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

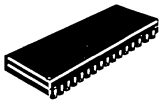
The MCM6226BB is available in 300 mil and 400 mil, 32 lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 180/170/160/140/115 mA Maximum, Active AC

BLOCK DIAGRAM

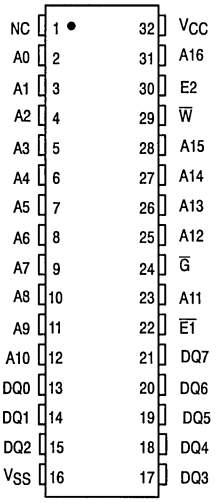


WJ PACKAGE
400 MIL SOJ
CASE 857A–02



J PACKAGE
300 MIL SOJ
CASE 857–02

PIN ASSIGNMENT



PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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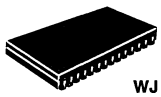
MCM6227A

1M x 1 Bit Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 810–03

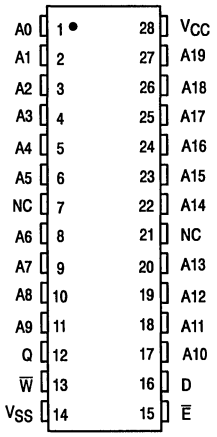
The MCM6227A is a 1,048,576 bit static random–access memory organized as 1,048,576 words of 1 bit, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6227A is equipped with a chip enable ($\overline{E}$) pin. In less than a cycle time after $\overline{E}$ goes high, the part enters a low–power standby mode, remaining in that state until $\overline{E}$ goes low again.

The MCM6227A is available in 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three–State Output
- Low Power Operation: 160/140/130/120 mA Maximum, Active AC

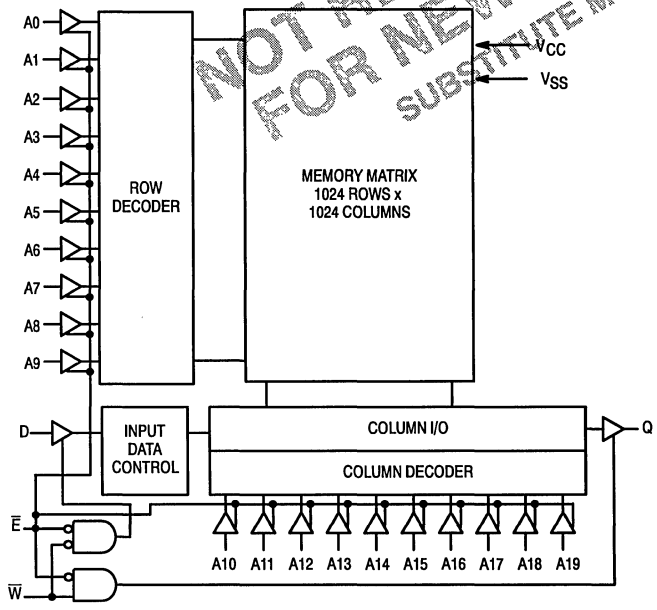
PIN ASSIGNMENT



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



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MCM6227A TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{out}	Read	I_{CCA}
L	L	Write	High–Z	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ*	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6227A–20: t_{AVAV} = 20 ns		—	120	160	
MCM6227A–25: t_{AVAV} = 25 ns		—	110	140	
MCM6227A–35: t_{AVAV} = 35 ns		—	100	130	
MCM6227A–45: t_{AVAV} = 45 ns		—	90	120	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*Typical values are measured at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and D, Q $\overline{E}$ and $\overline{W}$	C_{in}	4 5	6 8	pF
Input and Output Capacitance	D, Q	C_{in}, C_{out}	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6227A–20		6227A–25		6227A–35		6227A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	2,3
Address Access Time	t_{AVQV}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	—	45	ns	4
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	—	18	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \leq V_{IL}$).

AC TEST LOADS

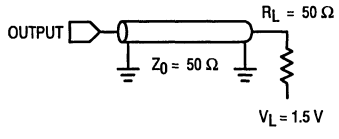


Figure 1A

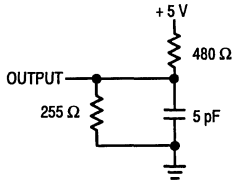
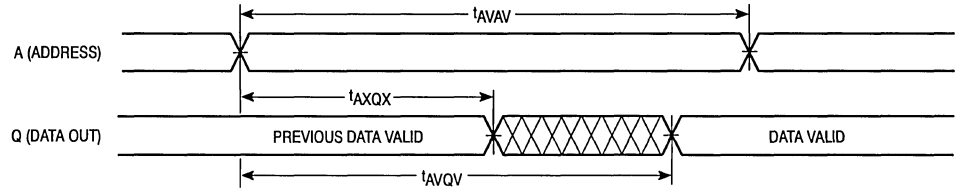


Figure 1B

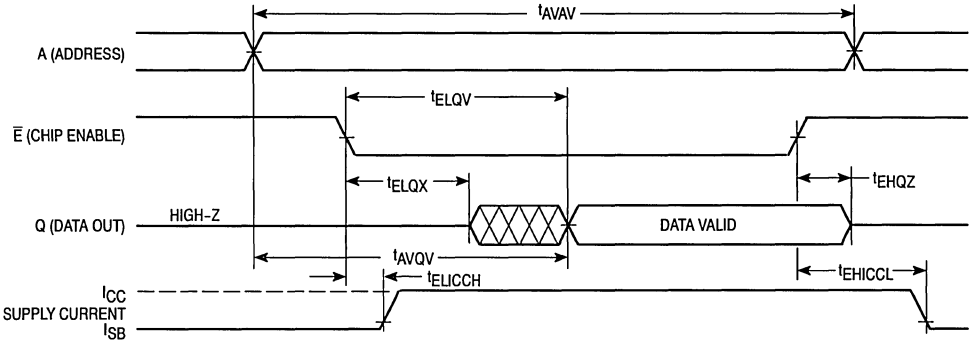
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)

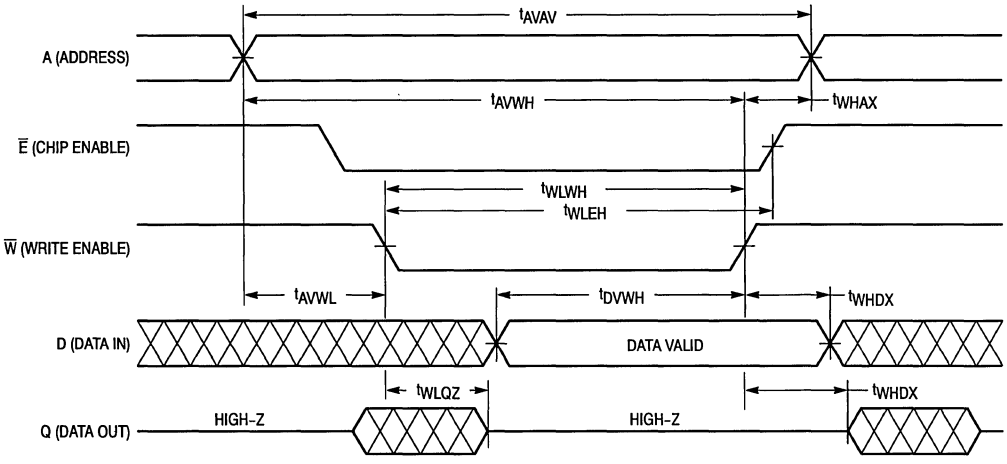


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6227A–20		6227A–25		6227A–35		6227A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	0	20	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1 and 2)

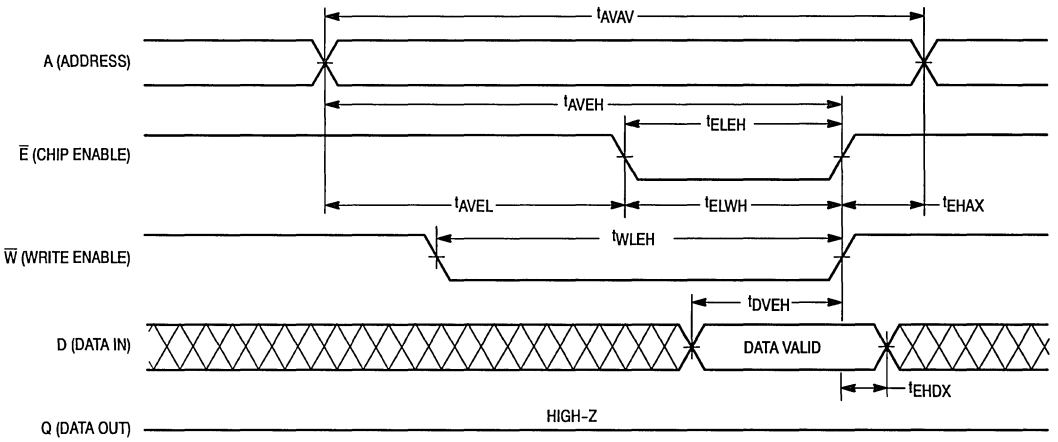


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6227A–20		6227A–25		6227A–35		6227A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	25	—	ns	4, 5
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6227A WJ XX XX

- MCM — Motorola Memory Prefix
- 6227A — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6227AWJ20, MCM6227AWJ20R2, MCM6227AWJ25, MCM6227AWJ25R2, MCM6227AWJ35, MCM6227AWJ35R2, MCM6227AWJ45, MCM6227AWJ45R2

MCM6227B

1M x 1 Bit Static Random Access Memory

The MCM6227B is a 1,048,576 bit static random–access memory organized as 1,048,576 words of 1 bit, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6227B is each equipped with a chip enable ($\overline{E}$) pin. This feature provides reduced system power requirements without degrading access time performance.

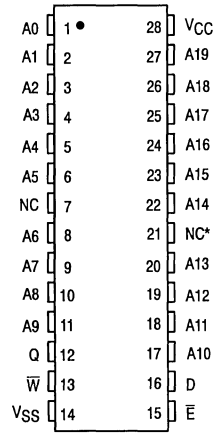
The MCM6227B is available in 300 mil and 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three–State Output
- Low Power Operation: 115/110/105/100/95 mA Maximum, Active AC

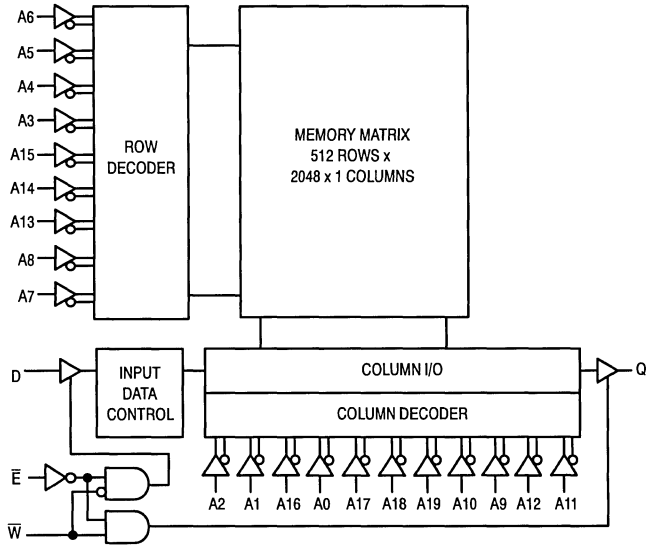
J PACKAGE
300 MIL SOJ
CASE 810B–03

WJ PACKAGE
400 MIL SOJ
CASE 810–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

REV 2
5/95

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{out}	Read	I_{CCA}
L	L	Write	High–Z	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} +0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}			mA
MCM6227B–15: t_{AVAV} = 15 ns		—	115	
MCM6227B–17: t_{AVAV} = 17 ns		—	110	
MCM6227B–20: t_{AVAV} = 20 ns		—	105	
MCM6227B–25: t_{AVAV} = 25 ns		—	100	
MCM6227B–35: t_{AVAV} = 35 ns		—	95	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f ≤ f_{max})	I_{SB1}			mA
MCM6227B–15: t_{AVAV} = 15 ns		—	40	
MCM6227B–17: t_{AVAV} = 17 ns		—	35	
MCM6227B–20: t_{AVAV} = 20 ns		—	30	
MCM6227B–25: t_{AVAV} = 25 ns		—	25	
MCM6227B–35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and D, Q $\overline{E}$ and $\overline{W}$	C_{in}	4 5	6 8	pF
Input and Output Capacitance	D, Q	C_{in}, C_{out}	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6227B–15		6227B–17		6227B–20		6227B–25		6227B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$).

AC TEST LOADS

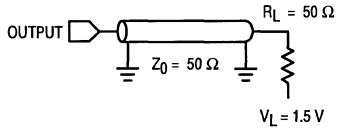


Figure 1A

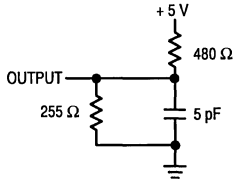
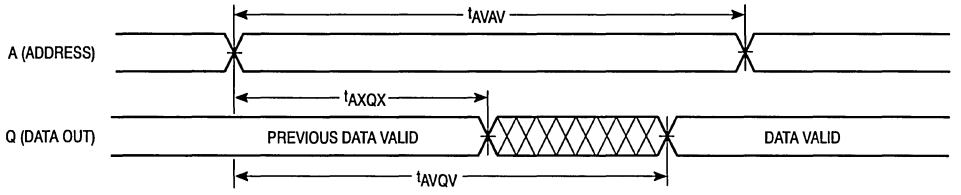


Figure 1B

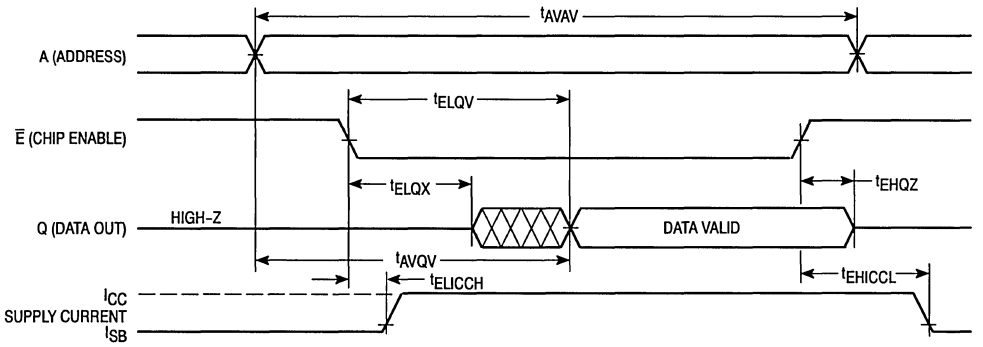
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)



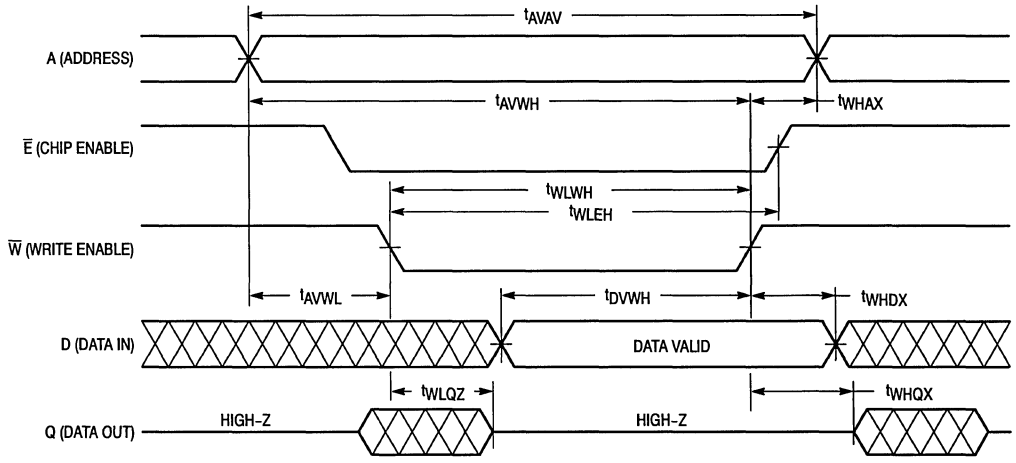
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6227B–15		6227B–17		6227B–20		6227B–25		6227B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	7	0	8	0	8	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1 and 2)

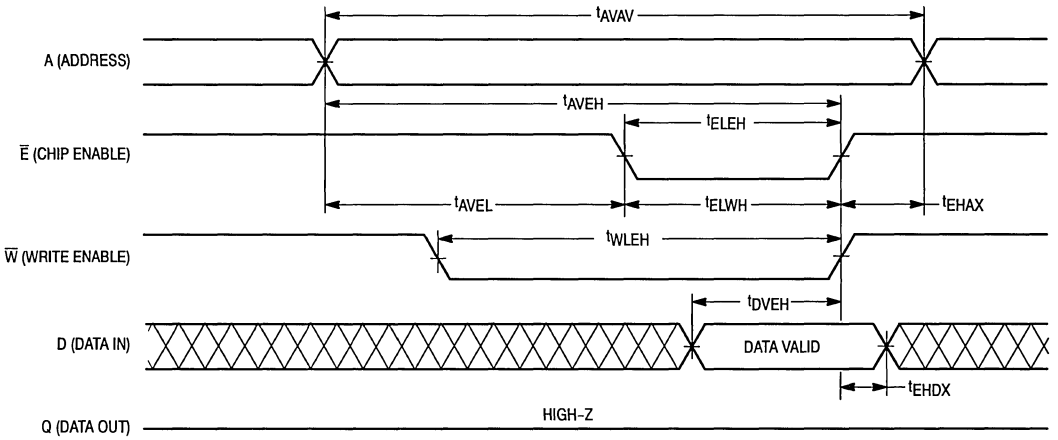


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	6227B–15		6227B–17		6227B–20		6227B–25		6227B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	4, 5
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6227B XX XX XX

- MCM — Motorola Memory Prefix
- 6227B — Part Number
- XX — Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Package (J = 300 mil SOJ, WJ = 400 mil SOJ)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —				
	MCM6227BJ15	MCM6227BJ15R2	MCM6227BWJ15	MCM6227BWJ15R2
	MCM6227BJ17	MCM6227BJ17R2	MCM6227BWJ17	MCM6227BWJ17R2
	MCM6227BJ20	MCM6227BJ20R2	MCM6227BWJ20	MCM6227BWJ20R2
	MCM6227BJ25	MCM6227BJ25R2	MCM6227BWJ25	MCM6227BWJ25R2
	MCM6227BJ35	MCM6227BJ35R2	MCM6227BWJ35	MCM6227BWJ35R2

MCM6229A

256K x 4 Bit Static Random Access Memory

The MCM6229A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

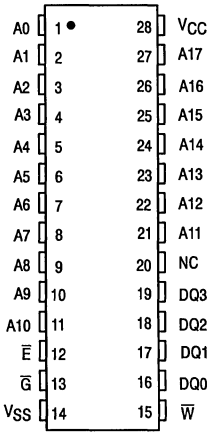
The MCM6229A is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6229A is available in 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Low Power Operation: 170/150/140/130 mA Maximum, Active AC

WJ PACKAGE
400 MIL SOJ
CASE 810–03

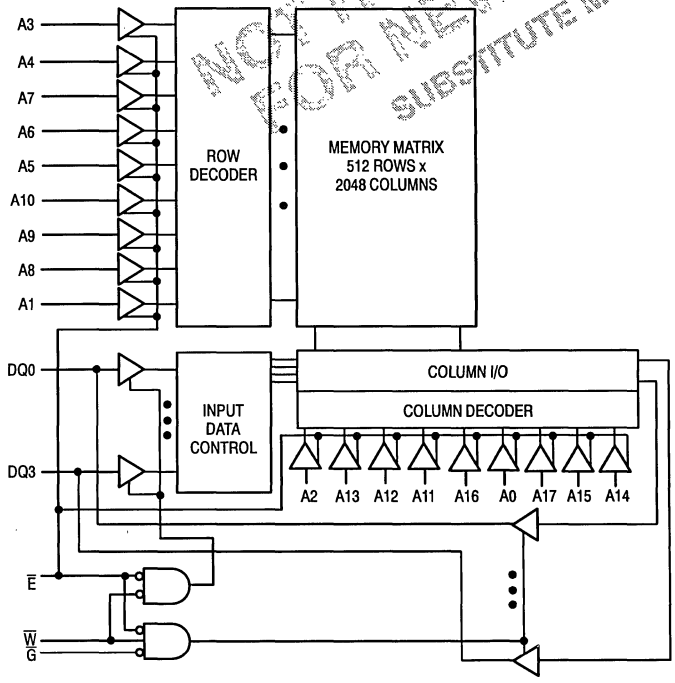
PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ*	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6229A–20: t_{AVAV} = 20 ns		—	140	170	
MCM6229A–25: t_{AVAV} = 25 ns		—	120	150	
MCM6229A–35: t_{AVAV} = 35 ns		—	110	140	
MCM6229A–45: t_{AVAV} = 45 ns		—	100	130	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*Typical measurements are taken at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQ	C_{in}	4	6	pF
	$\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{ck}	5	8	
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6229A–20		6229A–25		6229A–35		6229A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	2,3
Address Access Time	t_{AVQV}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	—	45	ns	4
Output Enable Access Time	t_{GLQV}	—	8	—	10	—	15	—	15	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	5,6,7
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	0	15	ns	5,6,7
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	0	12	0	15	ns	5,6,7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

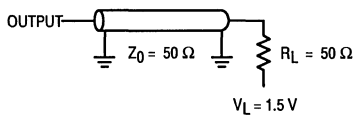


Figure 1A

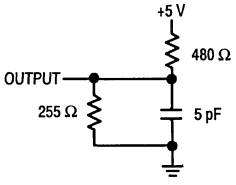
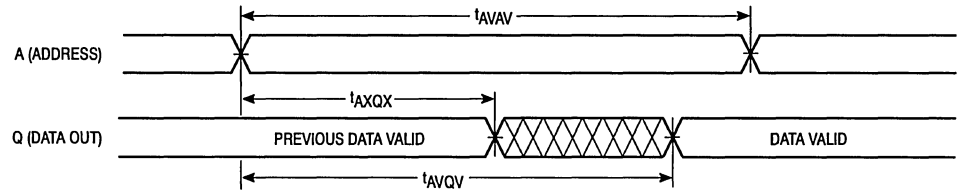


Figure 1B

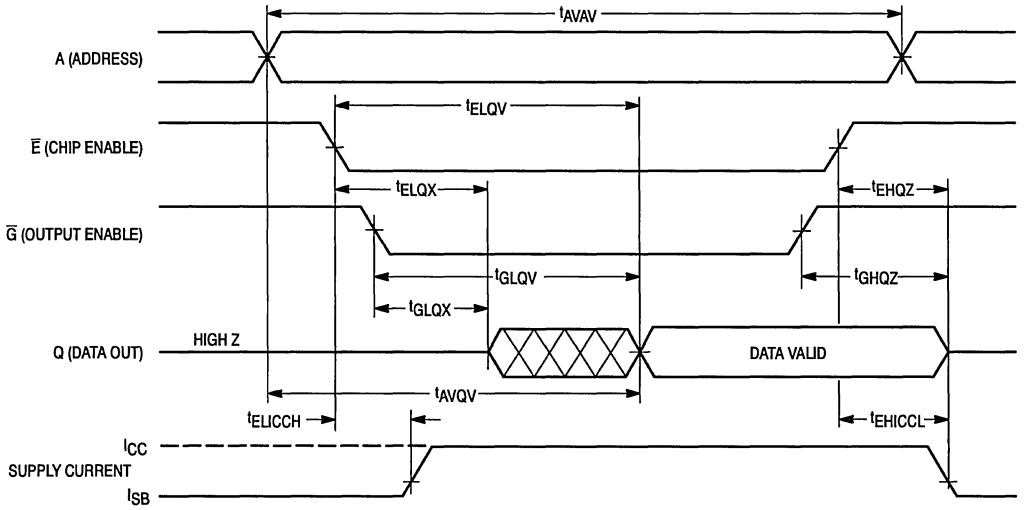
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)

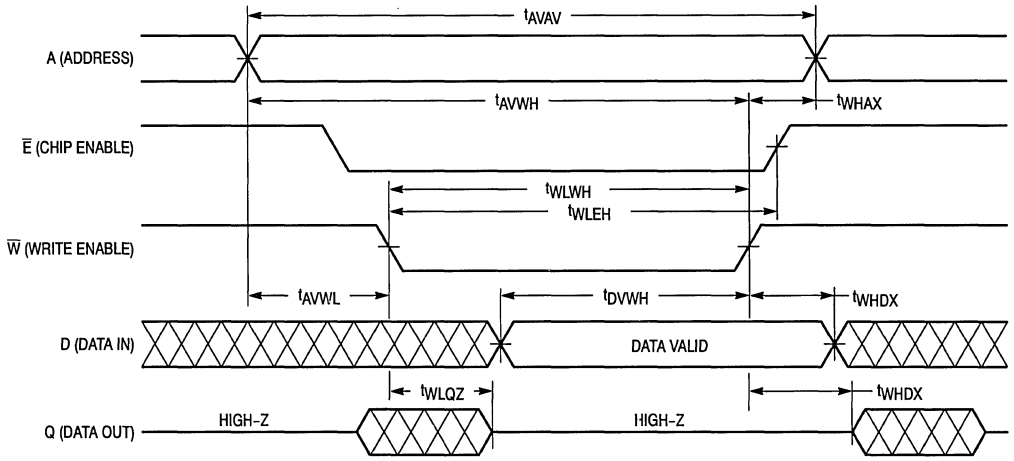


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229A–20		6229A–25		6229A–35		6229A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	0	20	ns	5,6,7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

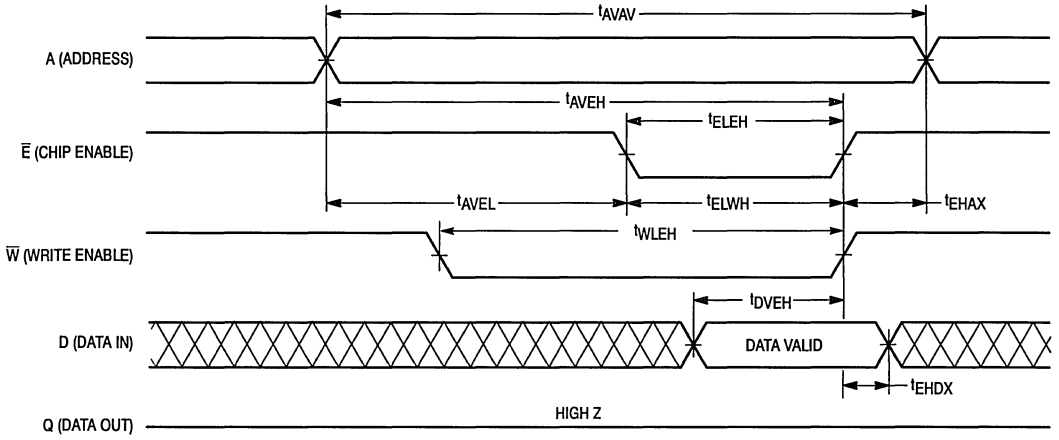


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

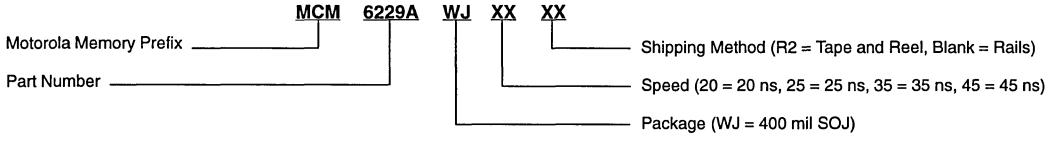
Parameter	Symbol	6229A–20		6229A–25		6229A–35		6229A–45		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	45	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	25	—	ns	5, 6
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6229AWJ20 MCM6229AWJ20R2
MCM6229AWJ25 MCM6229AWJ25R2
MCM6229AWJ35 MCM6229AWJ35R2
MCM6229AWJ45 MCM6229AWJ45R2

MCM6229B

256K x 4 Bit Static Random Access Memory

The MCM6229B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6229B is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

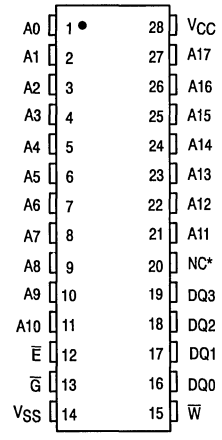
The MCM6229B is available in 300 mil and 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

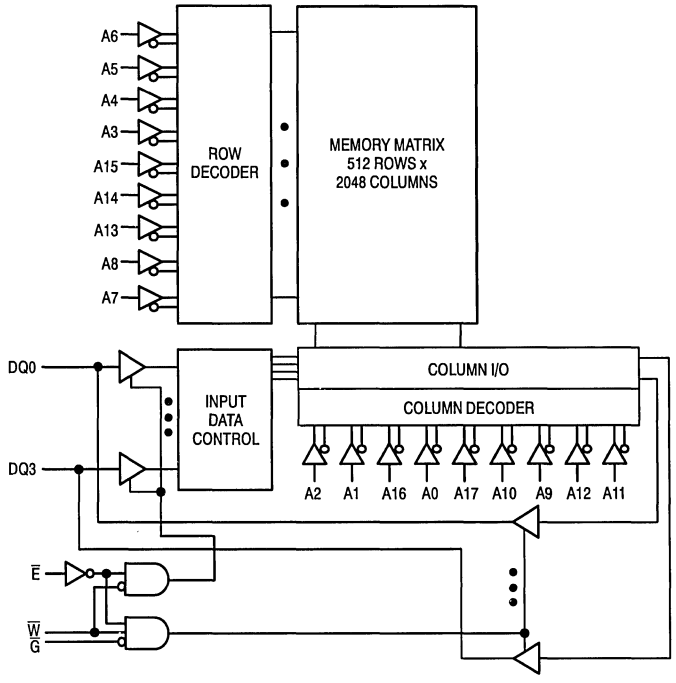
J PACKAGE
300 MIL SOJ
CASE 810B–03

WJ PACKAGE
400 MIL SOJ
CASE 810–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC*	No Connection

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}			mA
MCM6229B–15: t_{AVAV} = 15 ns		—	120	
MCM6229B–17: t_{AVAV} = 17 ns		—	115	
MCM6229B–20: t_{AVAV} = 20 ns		—	110	
MCM6229B–25: t_{AVAV} = 25 ns		—	105	
MCM6229B–35: t_{AVAV} = 35 ns		—	100	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f ≤ f_{max})	I_{SB1}			mA
MCM6229B–15: t_{AVAV} = 15 ns		—	40	
MCM6229B–17: t_{AVAV} = 17 ns		—	35	
MCM6229B–20: t_{AVAV} = 20 ns		—	30	
MCM6229B–25: t_{AVAV} = 25 ns		—	25	
MCM6229B–35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs except Clocks & DQs $\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6229B–15		6229B–17		6229B–20		6229B–25		6229B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6 ,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

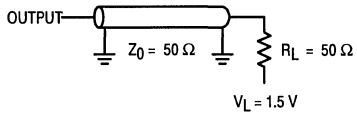


Figure 1A

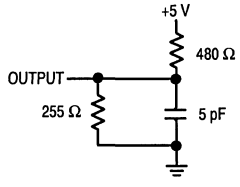
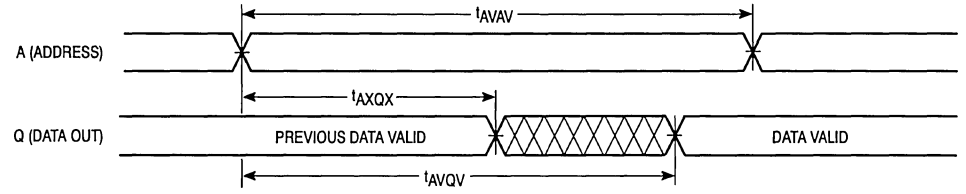


Figure 1B

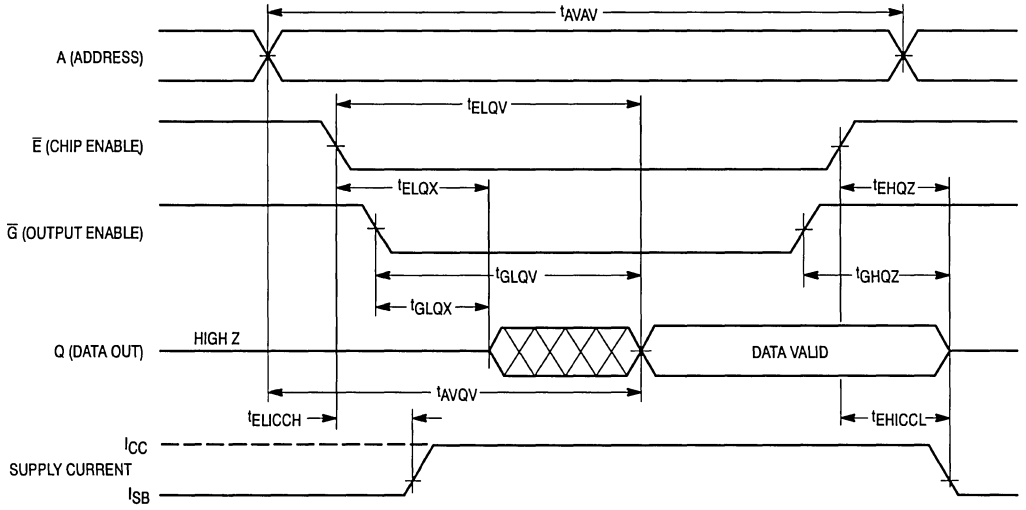
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)

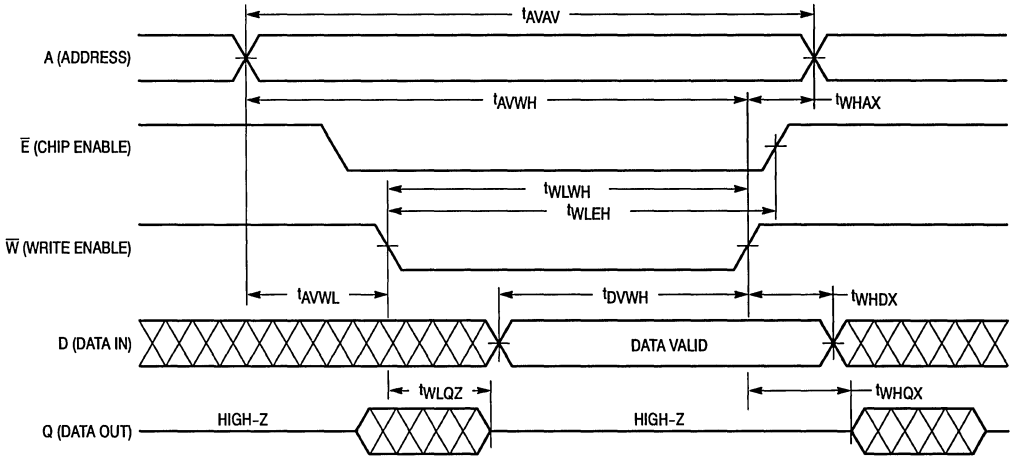


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229B–15		6229B–17		6229B–20		6229B–25		6229B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

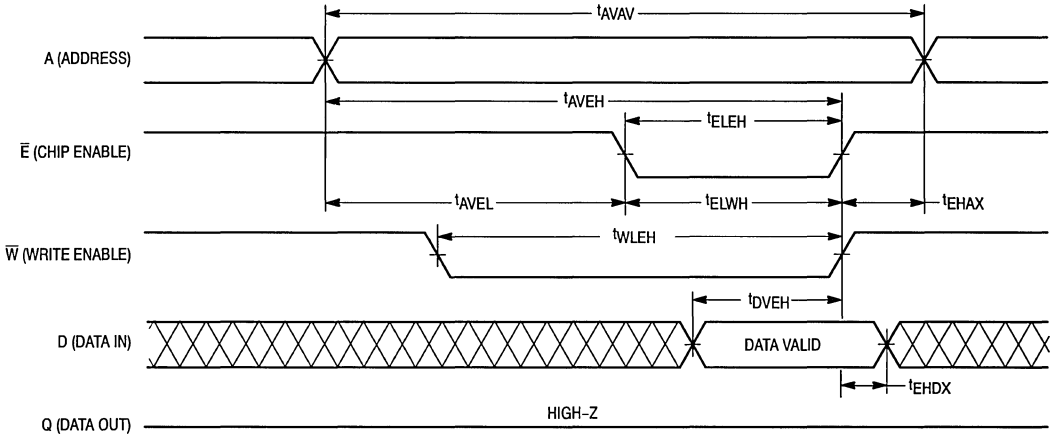


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229B–15		6229B–17		6229B–20		6229B–25		6229B–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	11	—	12	—	15	—	20	—	ns	5, 6
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6229B XX XX XX

Motorola Memory Prefix

Part Number

Shipping Method (R2 = Tape and Reel, Blank = Rails)

Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)

Package (J = 300 mil SOJ, WJ = 400 mil SOJ)

Full Part Numbers —				
	MCM6229BJ15	MCM6229BJ15R2	MCM6229BWJ15	MCM6229BWJ15R2
	MCM6229BJ17	MCM6229BJ17R2	MCM6229BWJ17	MCM6229BWJ17R2
	MCM6229BJ20	MCM6229BJ20R2	MCM6229BWJ20	MCM6229BWJ20R2
	MCM6229BJ25	MCM6229BJ25R2	MCM6229BWJ25	MCM6229BWJ25R2
	MCM6229BJ35	MCM6229BJ35R2	MCM6229BWJ35	MCM6229BWJ35R2

MCM6229BA

Product Preview

256K x 4 Bit Static Random Access Memory

J PACKAGE
300 MIL SOJ
CASE 810B–03

WJ PACKAGE
400 MIL SOJ
CASE 810–03

3

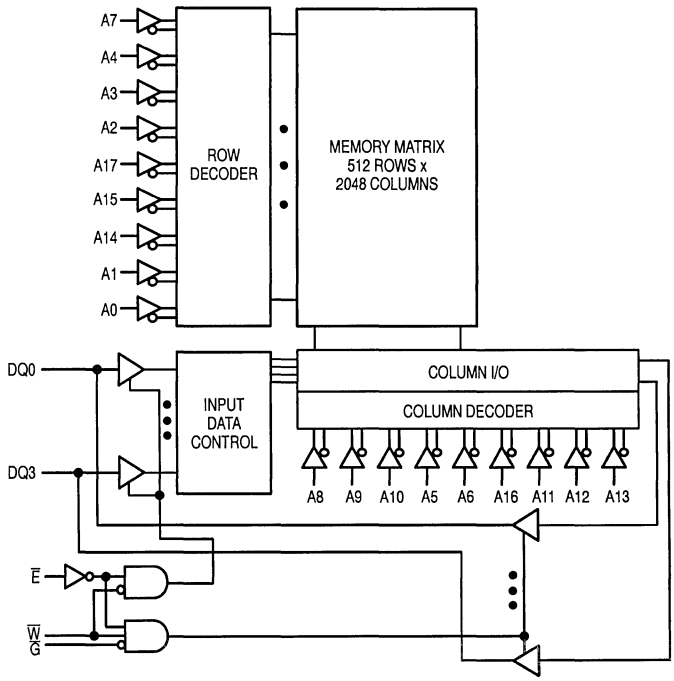
The MCM6229BA is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6229BA is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

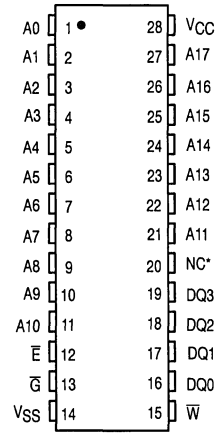
The MCM6229BA is available in 300 mil and 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC*	No Connection

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

5/95

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, all inputs = V_{IL} or V_{IH}, V_{IL} = 0, V_{IH} ≥ 3 V, cycle time ≥ t_{AVAV} min, V_{CC} = max)	MCM6229BA–15: t_{AVAV} = 15 ns MCM6229BA–17: t_{AVAV} = 17 ns MCM6229BA–20: t_{AVAV} = 20 ns MCM6229BA–25: t_{AVAV} = 25 ns MCM6229BA–35: t_{AVAV} = 35 ns	I_{CCA}	— — — — —	135 120 115 110 100	mA
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	MCM6229BA–15: t_{AVAV} = 15 ns MCM6229BA–17: t_{AVAV} = 17 ns MCM6229BA–20: t_{AVAV} = 20 ns MCM6229BA–25: t_{AVAV} = 25 ns MCM6229BA–35: t_{AVAV} = 35 ns	I_{SB1}	— — — — —	45 40 35 30 25	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs except Clocks & DQs $\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6229BA–15		6229BA–17		6229BA–20		6229BA–25		6229BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6 ,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

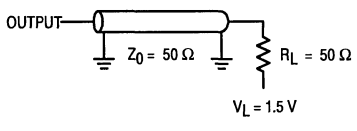


Figure 1A

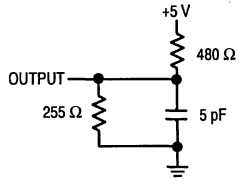
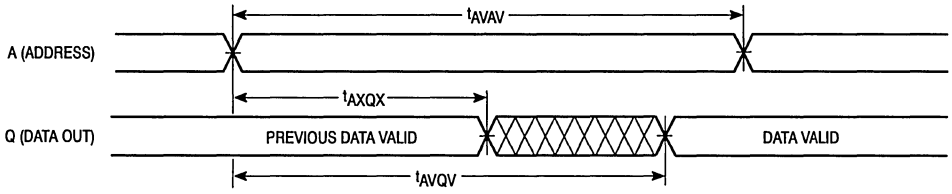


Figure 1B

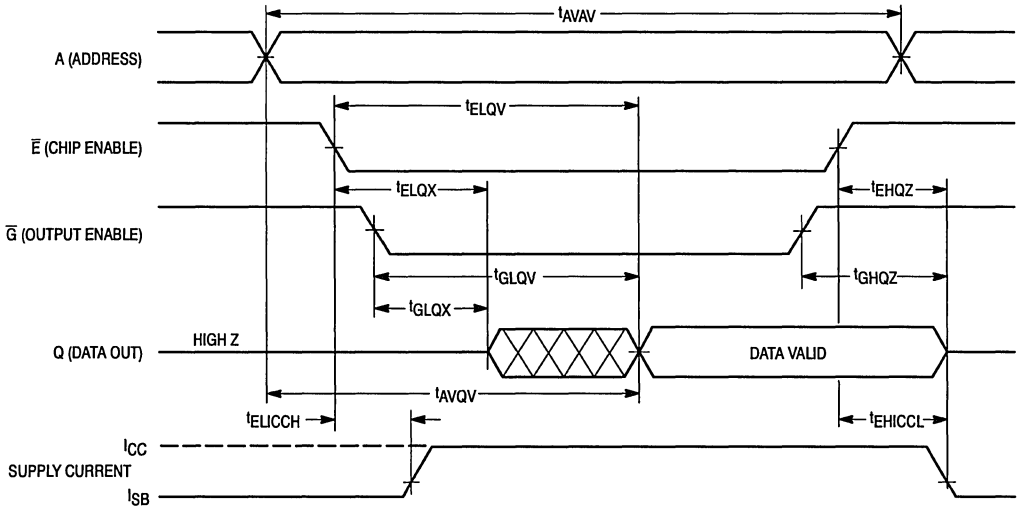
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)



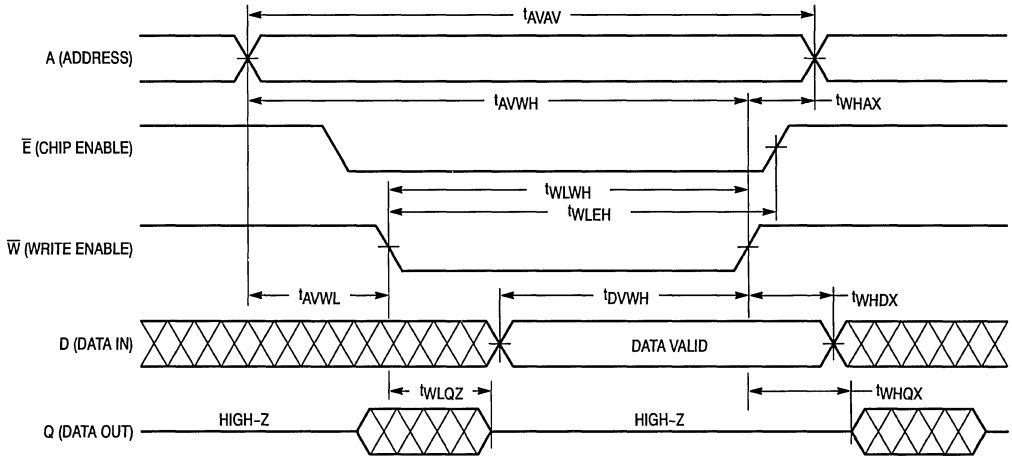
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BA–15		6229BA–17		6229BA–20		6229BA–25		6229BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

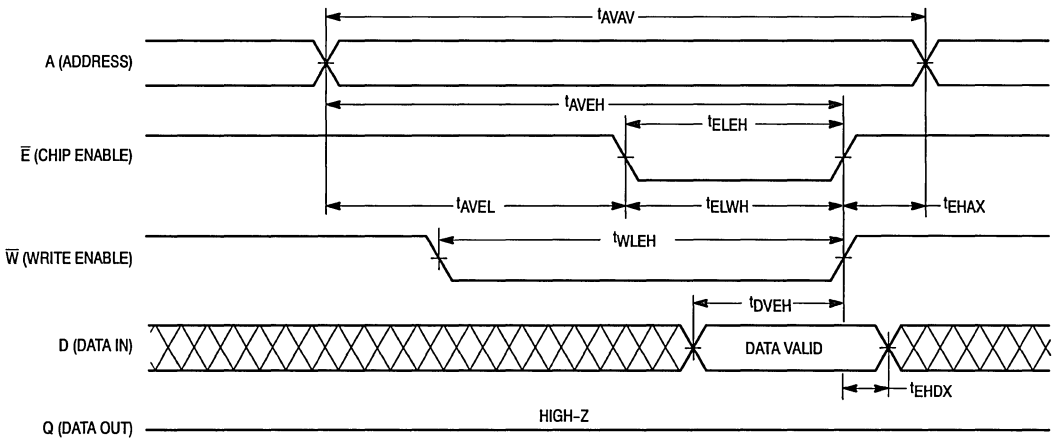


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BA–15		6229BA–17		6229BA–20		6229BA–25		6229BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	14	—	15	—	17	—	20	—	ns	5, 6
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	8	—	9	—	9	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6229BA XX XX X

Motorola Memory Prefix

Part Number

Shipping Method (R = Tape and Reel, Blank = Rails)

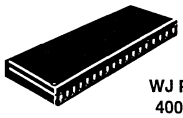
Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)

Package (J = 300 mil SOJ, WJ = 400 mil SOJ)

Full Part Numbers —				
	MCM6229BAJ15	MCM6229BAJ15R	MCM6229BAWJ15	MCM6229BAWJ15R
	MCM6229BAJ17	MCM6229BAJ17R	MCM6229BAWJ17	MCM6229BAWJ17R
	MCM6229BAJ20	MCM6229BAJ20R	MCM6229BAWJ20	MCM6229BAWJ20R
	MCM6229BAJ25	MCM6229BAJ25R	MCM6229BAWJ25	MCM6229BAWJ25R
	MCM6229BAJ35	MCM6229BAJ35R	MCM6229BAWJ35	MCM6229BAWJ35R

MCM6246

512K x 8 Bit Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 893–01

The MCM6246 is a 4,194,304 bit static random access memory organized as 524,288 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6246 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

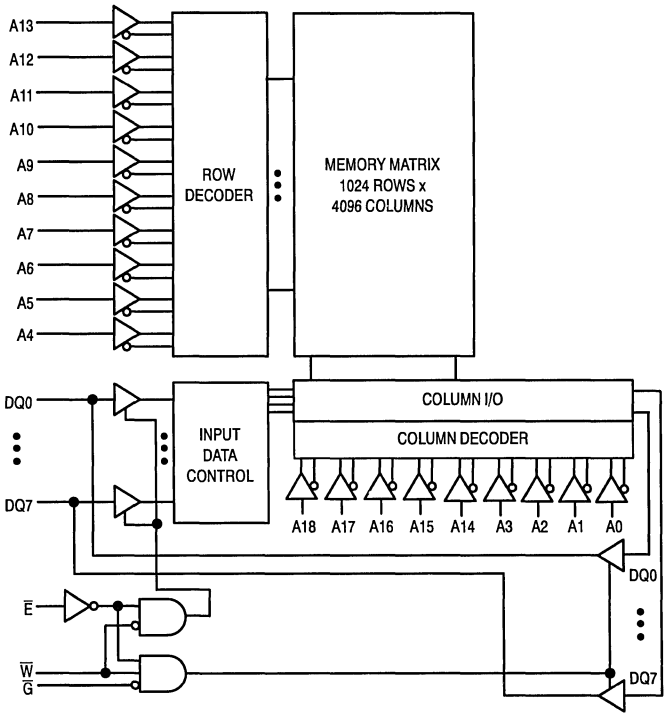
The MCM6246 is available in a 400 mil, 36–lead surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 200/185/170 mA Maximum, Active AC

PIN ASSIGNMENT

A6	1	36	NC
A7	2	35	A1
A8	3	34	A0
A9	4	33	A5
A17	5	32	A4
$\overline{E}$	6	31	$\overline{G}$
DQ0	7	30	DQ7
DQ1	8	29	DQ6
V_{CC}	9	28	V_{SS}
V_{SS}	10	27	V_{CC}
DQ2	11	26	DQ5
DQ3	12	25	DQ4
$\overline{W}$	13	24	A16
A18	14	23	A15
A10	15	22	A14
A11	16	21	A3
A12	17	20	A2
A13	18	19	NC

BLOCK DIAGRAM



PIN NAMES

A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ7	Data Input/Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High–Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6246–20: t_{AVAV} = 20 ns	I_{CC}	—	185	200	mA
	MCM6246–25: t_{AVAV} = 25 ns		—	170	185	
	MCM6246–35: t_{AVAV} = 35 ns		—	155	170	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6246–20: t_{AVAV} = 20 ns	I_{SB1}	—	55	60	mA
	MCM6246–25: t_{AVAV} = 25 ns		—	45	50	
	MCM6246–35: t_{AVAV} = 35 ns		—	35	40	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

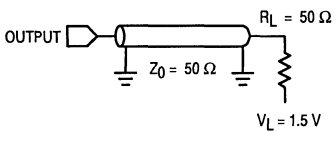


Figure 1A

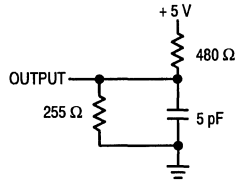
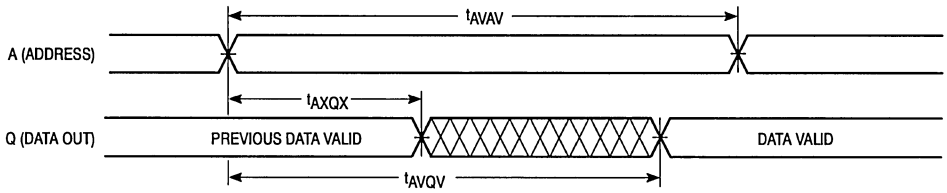


Figure 1B

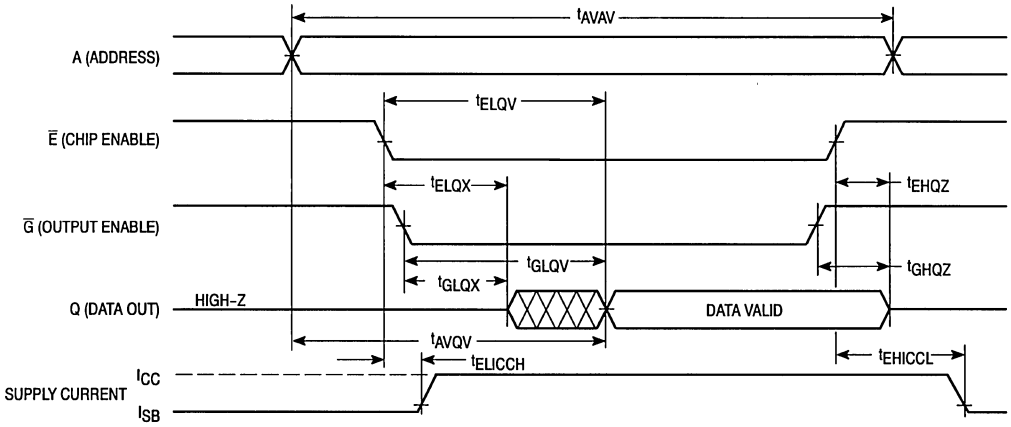
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note)



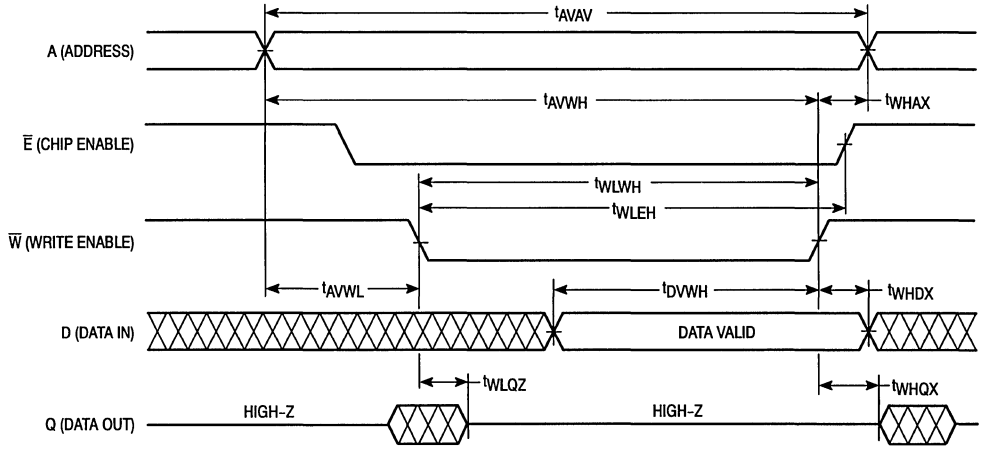
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low/ $\overline{E}$ going high.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

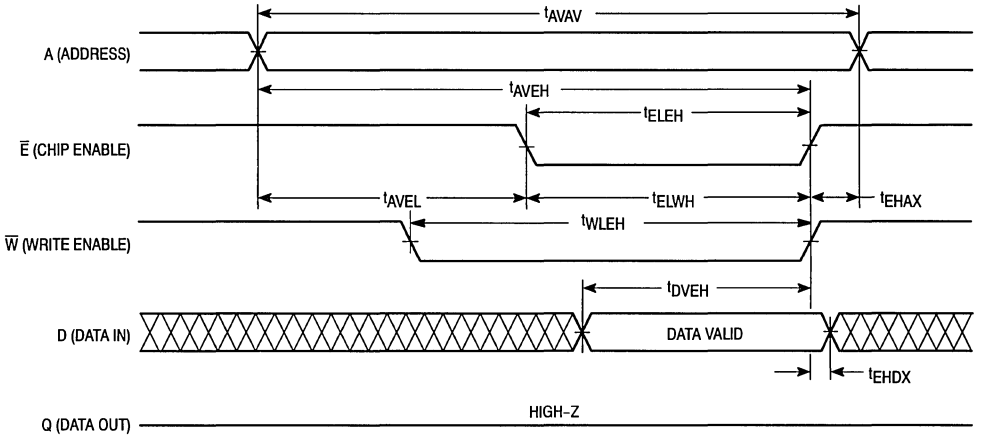


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6246–20		MCM6246–25		MCM6246–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	ns	5,6
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

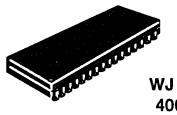
MCM 6246 XX XX XX

- MCM: Motorola Memory Prefix
- 6246: Part Number
- XX: Package (WJ = 400 mil SOJ)
- XX: Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX: Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6246WJ20 MCM6246WJ20R2
MCM6246WJ25 MCM6246WJ25R2
MCM6246WJ35 MCM6246WJ35R2

MCM6249

1M x 4 Bit Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A–02

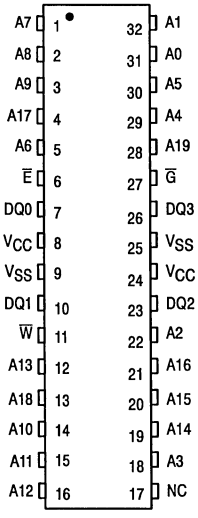
The MCM6249 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6249 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

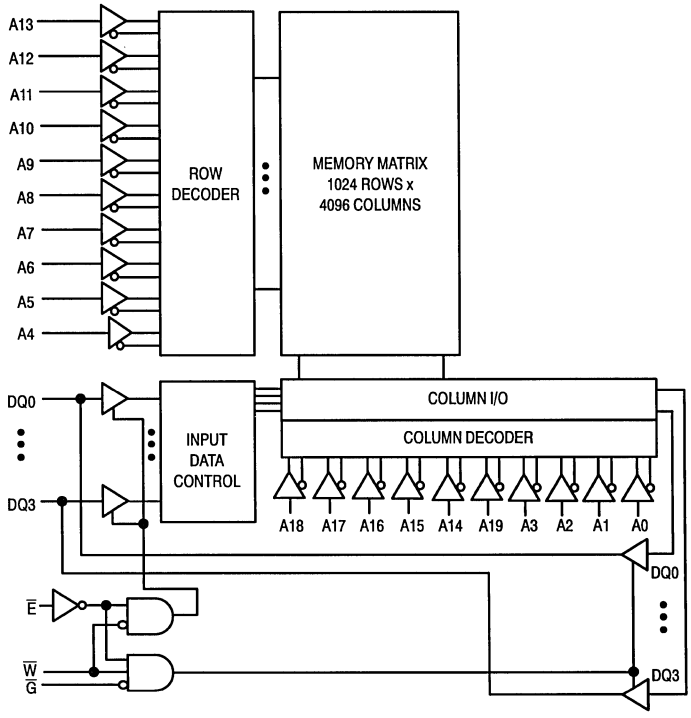
The MCM6249 is available in a 400 mil, 32–lead surface–mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 190/175/160 mA Maximum, Active AC

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

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TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High–Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6249–20: t_{AVAV} = 20 ns	I_{CC}	—	175	190	mA
	MCM6249–25: t_{AVAV} = 25 ns		—	160	175	
	MCM6249–35: t_{AVAV} = 35 ns		—	145	160	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6249–20: t_{AVAV} = 20 ns	I_{SB1}	—	50	60	mA
	MCM6249–25: t_{AVAV} = 25 ns		—	40	50	
	MCM6249–35: t_{AVAV} = 35 ns		—	35	40	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

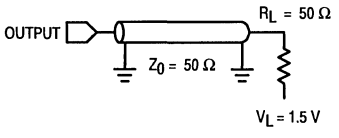


Figure 1A

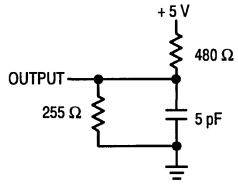
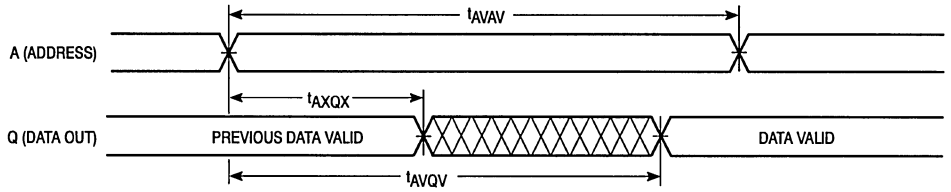


Figure 1B

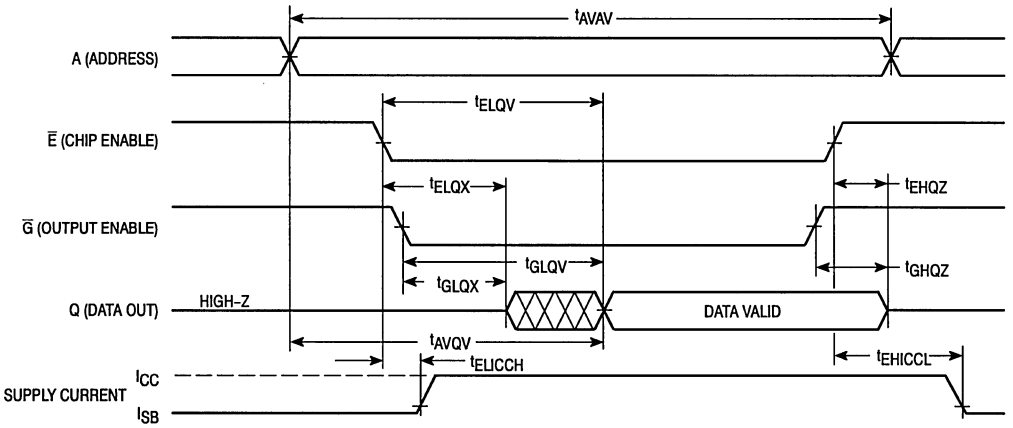
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note)



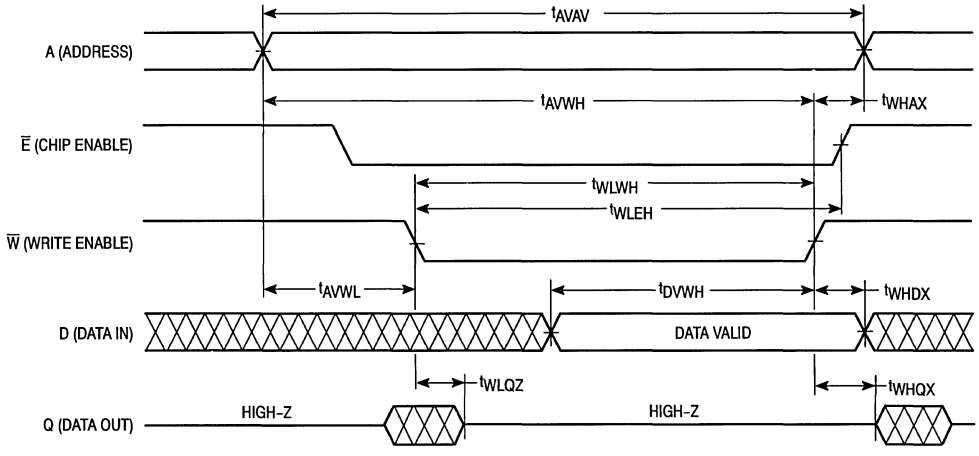
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

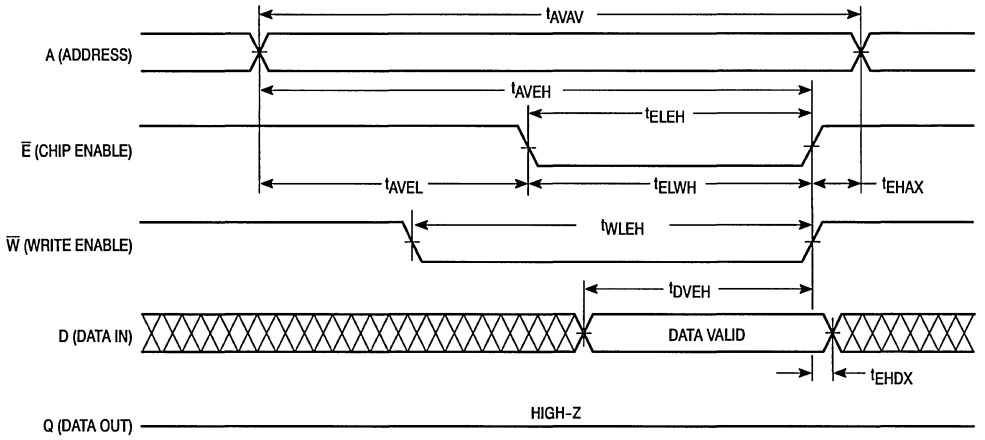


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6249–20		MCM6249–25		MCM6249–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	15	—	17	—	20	—	ns	5,6
Write Pulse Width	t_{WLEH}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6249 XX XX XX

- MCM — Motorola Memory Prefix
- 6249 — Part Number
- XX — Package (WJ = 400 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6249WJ20 MCM6249WJ20R2
MCM6249WJ25 MCM6249WJ25R2
MCM6249WJ35 MCM6249WJ35R2

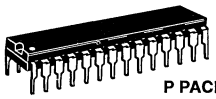
MCM6264C

8K x 8 Bit Fast Static RAM

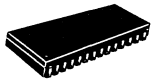
The MCM6264C is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual–in–line and plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 110 – 150 mA Maximum AC
- Fully TTL Compatible — Three State Output

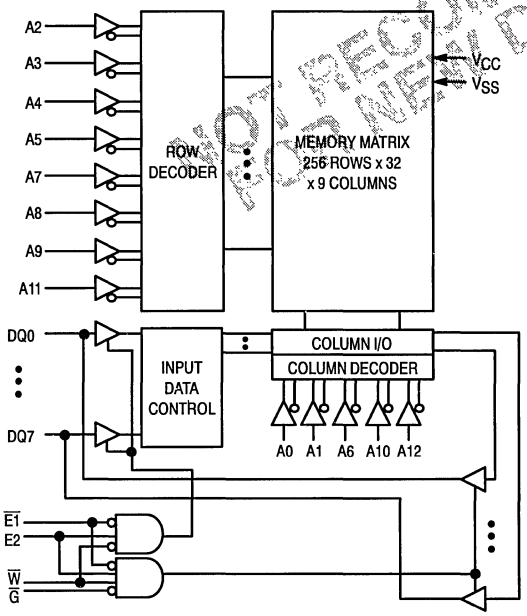


P PACKAGE
300 MIL PLASTIC
CASE 710B–01

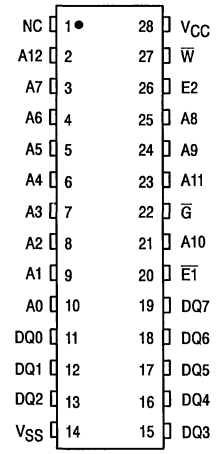


J PACKAGE
300 MIL SOJ
CASE 810B–03

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A12	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

REV 2
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	– 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	120	110	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	35	30	30	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	11	—	12	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	4	—	ns	5, 6 ,7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	8	0	9	0	10	0	11	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	9	0	10	ns	5, 6, 7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

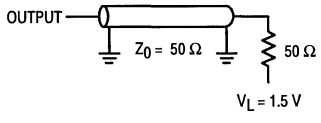


Figure 1A

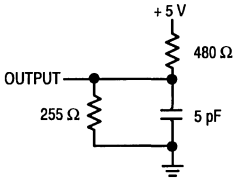
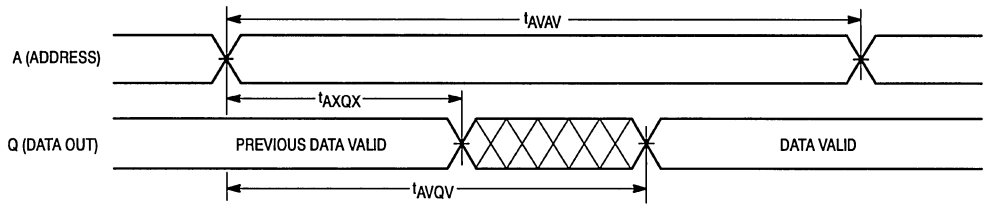


Figure 1B

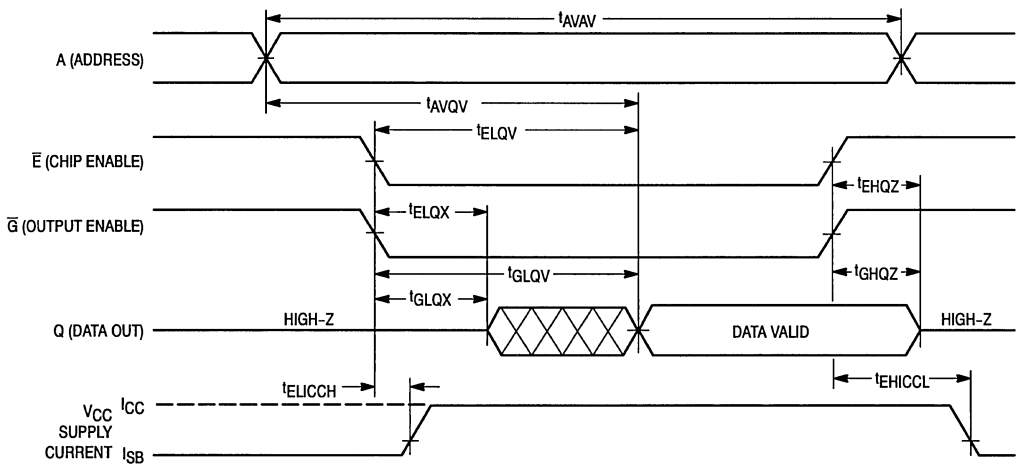
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)



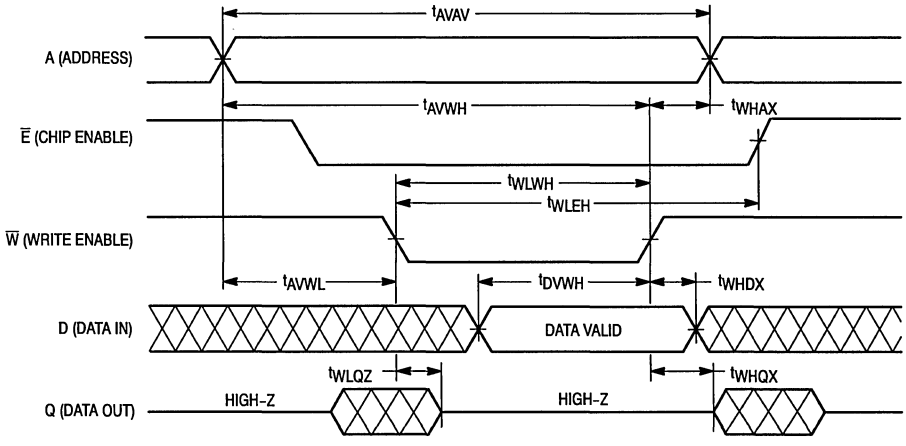
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	8	—	10	—	12	—	15	—	17	—	ns	5
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	6	0	7	0	8	0	10	0	12	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

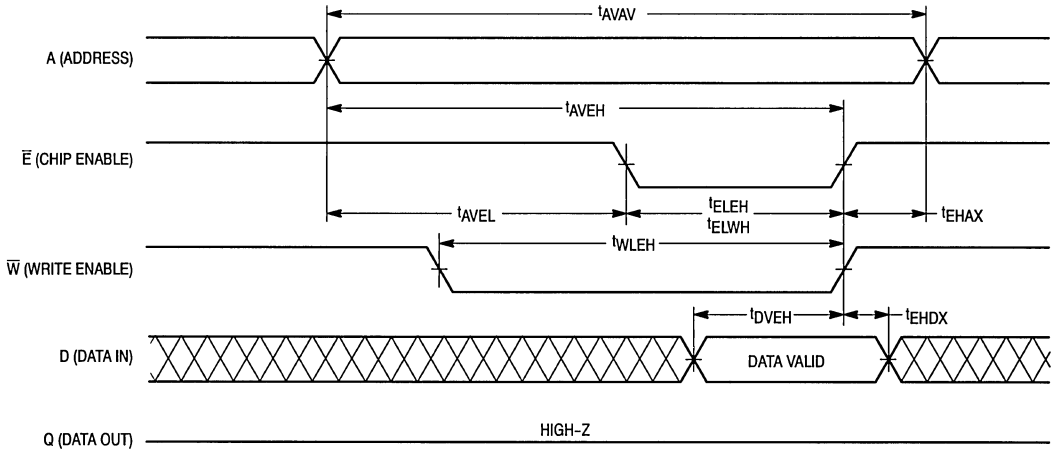


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–20		–25		–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	10	—	12	—	15	—	25	—	ns	4, 5
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6264C X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (P = 300 mil Plastic, J = 300 mil SOJ)

Full Part Numbers —			
	MCM6264CP12	MCM6264CJ12	MCM6264CJ12R2
	MCM6264CP15	MCM6264CJ15	MCM6264CJ15R2
	MCM6264CP20	MCM6264CJ20	MCM6264CJ20R2
	MCM6264CP25	MCM6264CJ25	MCM6264CJ25R2
	MCM6264CP35	MCM6264CJ35	MCM6264CJ35R2

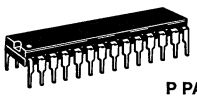
MCM6265C

8K x 9 Bit Fast Static RAM

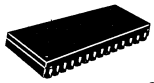
The MCM6265C is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual–in–line and plastic small–outline J–leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 110 – 150 mA Maximum AC
- Fully TTL Compatible — Three State Output

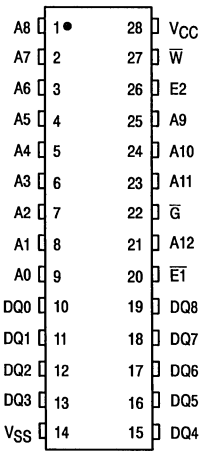


P PACKAGE
300 MIL PLASTIC
CASE 710B–01

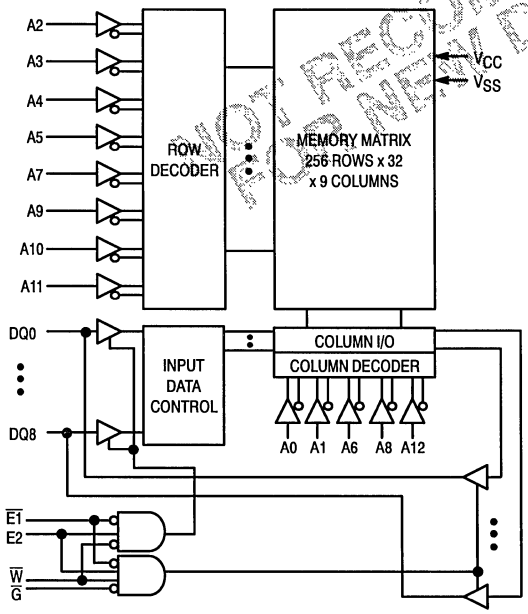


J PACKAGE
300 MIL SOJ
CASE 810B–03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A12	Address Input
DQ0 – DQ8	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

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TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	– 12	– 15	– 20	– 25	– 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	120	110	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	35	30	30	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	8	—	10	—	11	—	12	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	8	0	9	0	10	0	11	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	0	9	0	10	ns	5,6,7
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

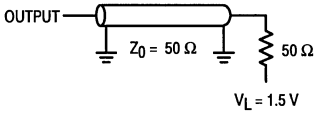


Figure 1A

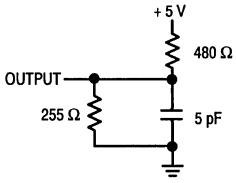
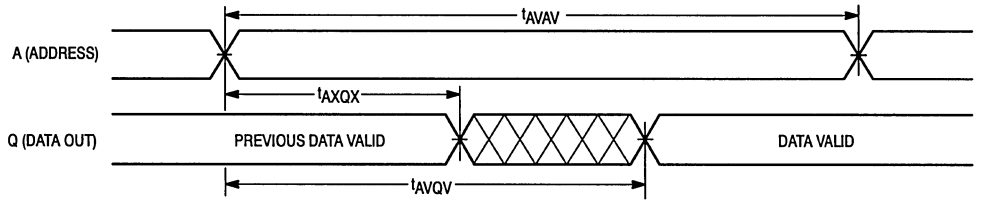


Figure 1B

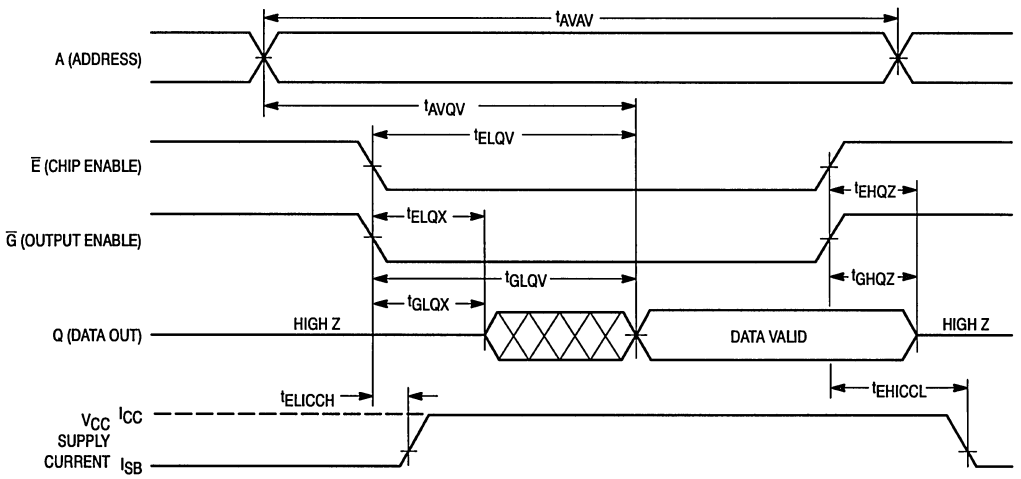
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)



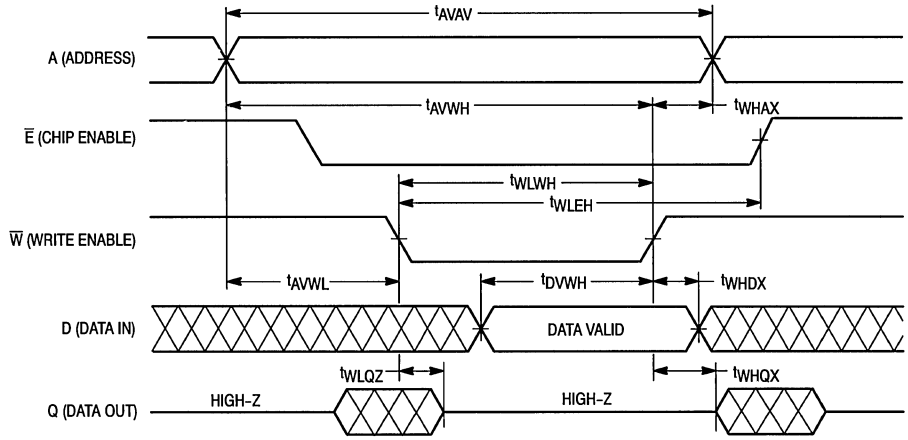
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	–12		–15		–20		–25		–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	8	—	10	—	12	—	15	—	17	—	ns	5
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	6	0	7	0	8	0	10	0	12	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

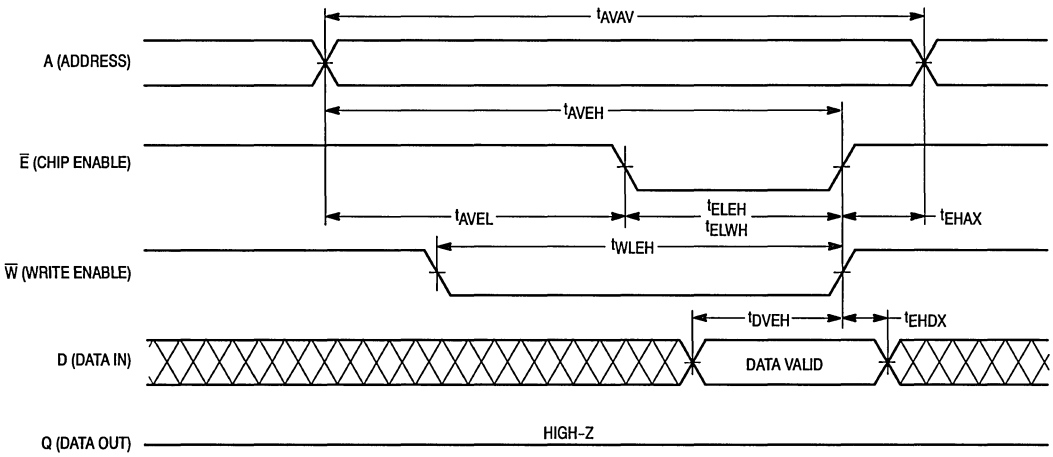


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	-12		-15		-20		-25		-35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	10	—	12	—	15	—	25	—	ns	4, 5
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6265C X XX XX

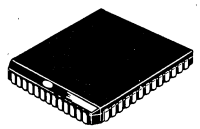
- MCM — Motorola Memory Prefix
- 6265C — Part Number
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM6265CP12	MCM6265CJ12	MCM6265CJ12R2
MCM6265CP15	MCM6265CJ15	MCM6265CJ15R2
MCM6265CP20	MCM6265CJ20	MCM6265CJ20R2
MCM6265CP25	MCM6265CJ25	MCM6265CJ25R2
MCM6265CP35	MCM6265CJ35	MCM6265CJ35R2

MCM62996

16K x 16 Bit Asynchronous Fast Static RAM



FN PACKAGE
52–LEAD PLCC
CASE 778–02

The MCM62996 is a 262,144 bit static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 16K x 16 SRAM core with active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

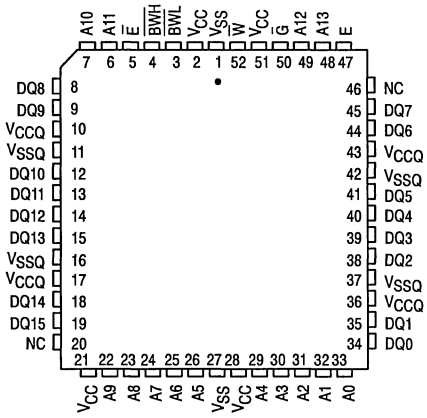
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62996 will be available in a 52–pin plastic leaded chip carrier PLCC.

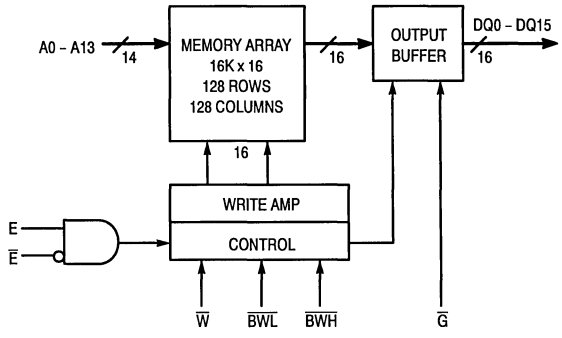
This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0 – A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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TRUTH TABLE (See Notes)

$\overline{E}$	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	X	Write Cycle All Bits	I_{CC}	High–Z
T	L	H	H	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	X	Write Cycle Lower 8 Bits	I_{CC}	High–Z
T	L	H	L	X	Write Cycle Upper 8 Bits	I_{CC}	High–Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and addresses satisfy the specified setup and hold times for the falling edge of LE. Data–in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = V_{SSQ} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}*	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL}(min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

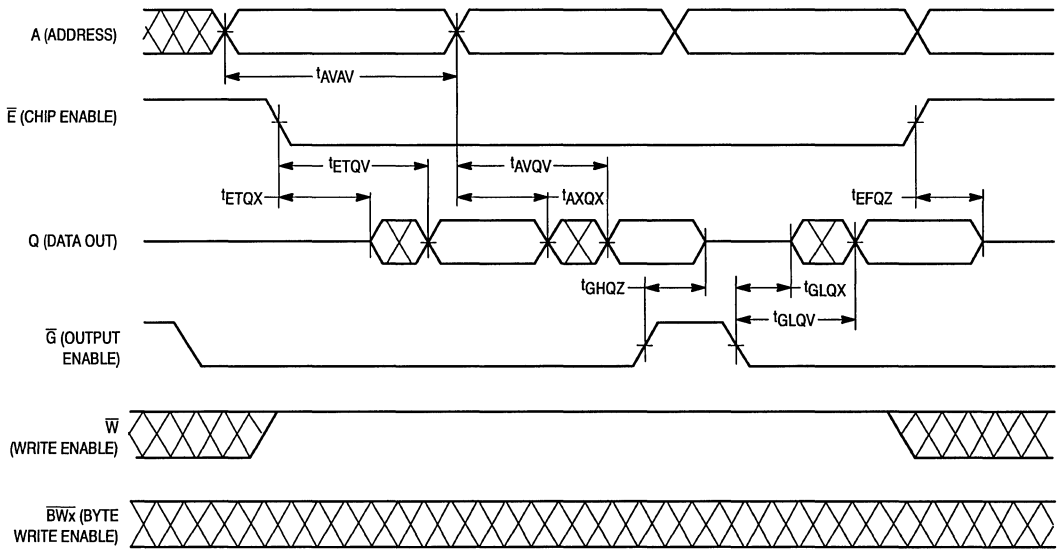
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62996–12		MCM62996–15		MCM62996–20		MCM62996–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	4
Access Times:										ns	5
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	6
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	0	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	0	9	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	0	8	2	10		
Power Up Time	t_{ETICCH}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
3. EF is defined by $\overline{E}$ going high or E going low.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

READ CYCLE



WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62996–12		MCM62996–15		MCM62996–20		MCM62996–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10		13		15		20			
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	6	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	6	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	6	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		6
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		7
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		6, 7
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		8, 9

NOTES:
1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high–impedance state.
7. If E and $\overline{E}$ go true coincident with or after $\overline{W}$ goes low the output will remain in a high–impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.

AC TEST LOADS

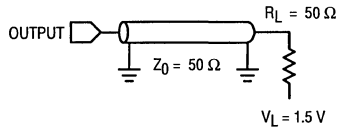


Figure 1A

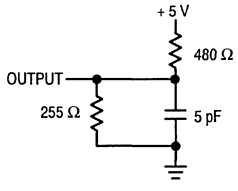
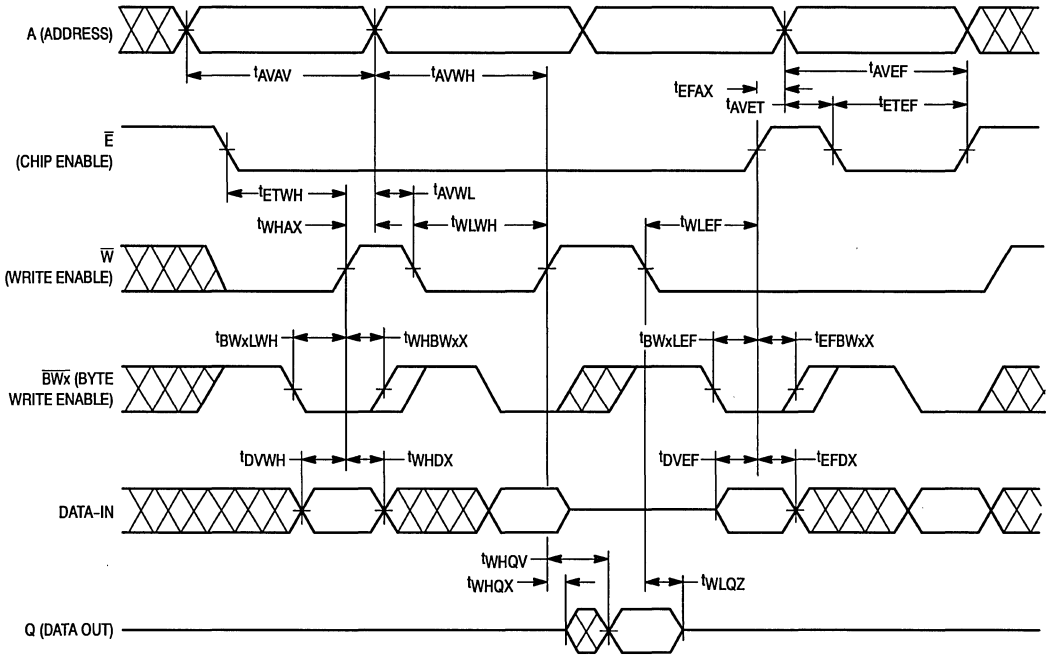


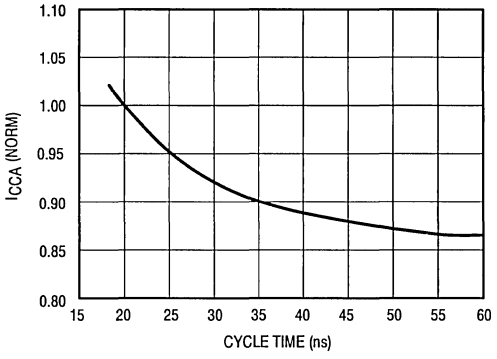
Figure 1B

WRITE CYCLE

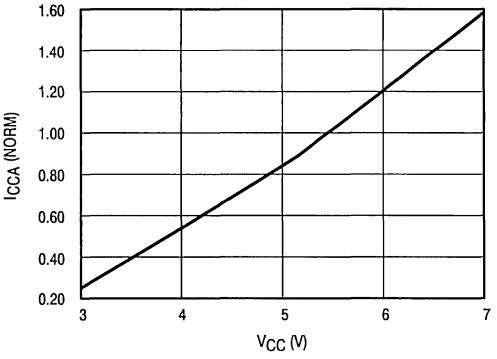

A (ADDRESS)
tAVAV
tAVWH
tAVEF
tEFAX
tAVET
tETEF
E
(CHIP ENABLE)
tETWH
tAVWL
tWHAX
tWLWH
tWLEF
W
(WRITE ENABLE)
tBWxLWH
tWHBWxX
tBWxLEF
tEFBWxX
BWx (BYTE
WRITE ENABLE)
tDVWH
tWHDX
tDVEF
tEFDX
DATA-IN
tWHQV
tWHQX
tWLQZ
Q (DATA OUT)

DERATING CURVES

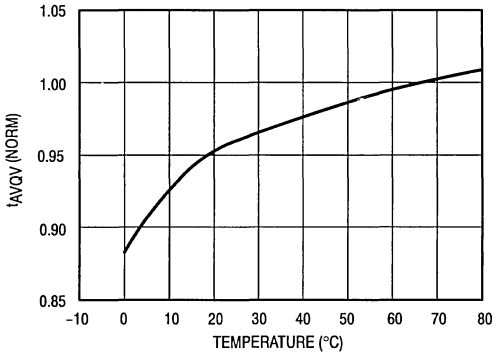
(Derating Curves Are Based On Component Typical Values)



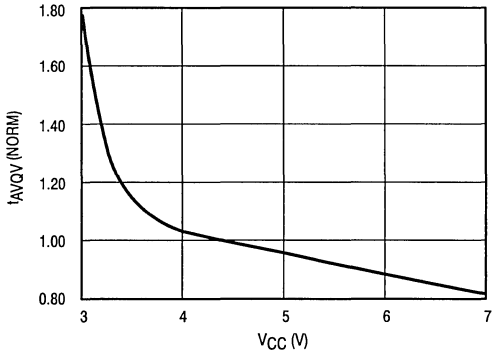
I_{CCA} vs Cycle Time



I_{CCA} vs V_{CC}



AVQV vs Temperature



AVQV vs V_{CC}

ORDERING INFORMATION

(Order by Full Part Number)

MCM	62996	FN	XX
Motorola Memory Prefix	Part Number	Package (FN = PLCC)	Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Full Part Numbers — MCM62996FN12 MCM62996FN15 MCM62996FN20 MCM62996FN25

MCM6306D

32K x 8 Bit 3.3 Volt Fast Static RAM

The MCM6306D is fabricated using Motorola's high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

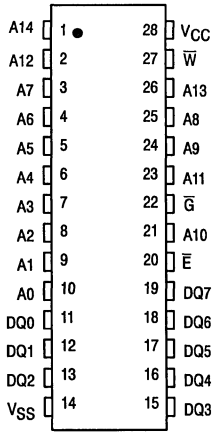
This device meets JEDEC standards for functionality and pinout, and is available in plastic small–outline J–leaded package.

J PACKAGE
300 MIL SOJ
CASE
810B–03

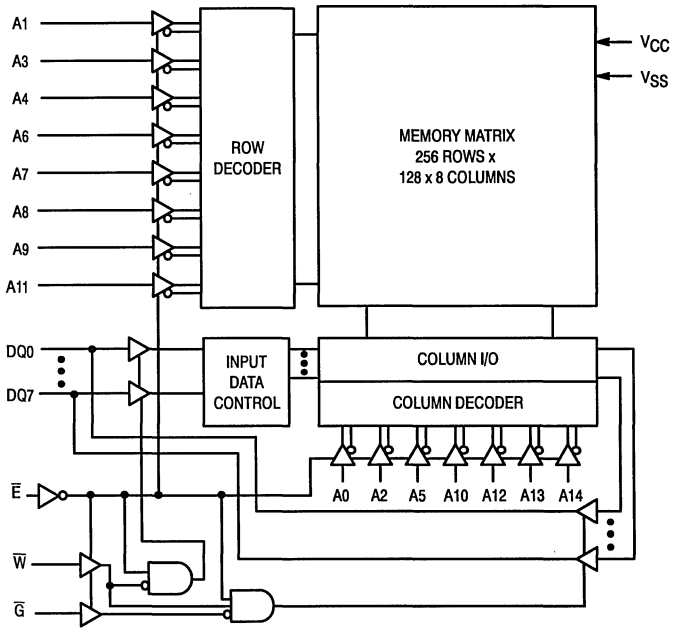
3

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 15, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 85 mA Maximum AC
- Fully 3.3 V CMOS — Three State Output
- 1 mA Standby Mode

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground

REV 1
5/95

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 5.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5*	V
Input or Output Current	I_{in}, I_{out}	± 20	mA
Power Dissipation	P_D	0.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

*V_{CC} + 2.0 V ac to V_{SS} – 2.0 V ac (Pulse width ≤ 20 ns).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board in still air.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)‡	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min))

**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min))

‡ For MCM6306DJ15B, 3.135 V ≤ V_{CC} ≤ 3.60 V

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
TTL Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
CMOS Output High Voltage (I_{OH} = – 100 µA)	V_{OH2}	V_{CC} – 0.1	—	V
CMOS Output Low Voltage (I_{OL} = 100 µA)	V_{OL2}	—	0.1	V

POWER SUPPLY CURRENTS

Parameter	Symbol	–15	–20	–25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	85	80	75	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	20	18	16	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V)	I_{SB2}	1	1	1	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

3

READ CYCLE (See Note 1)

Parameter	Symbol	–15		–20		–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	—	25	ns	3
Output Enable Access Time	t_{GLQV}	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	6
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	0	8	0	9	0	10	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	7	0	8	0	10	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

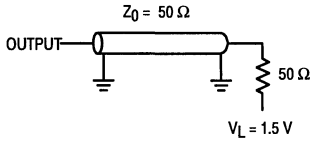


Figure 1A

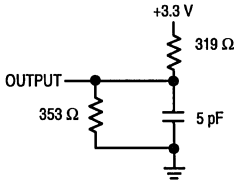
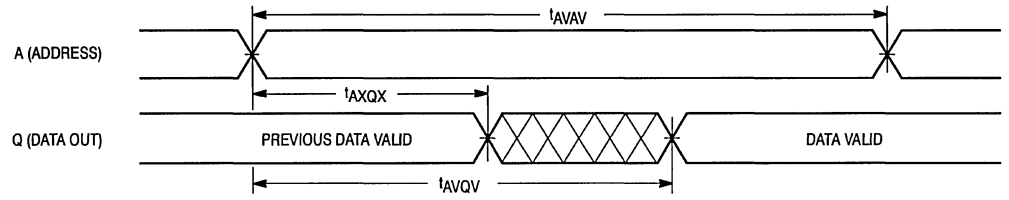


Figure 1B

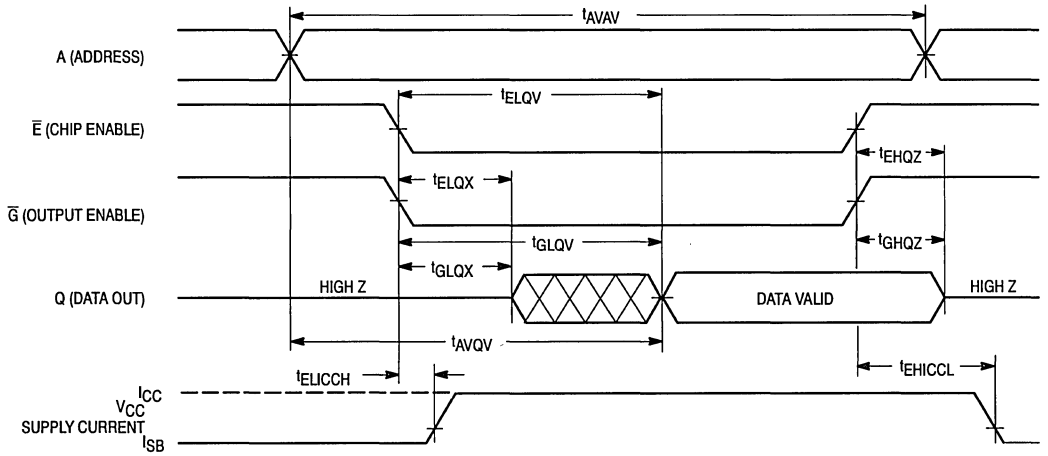
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)



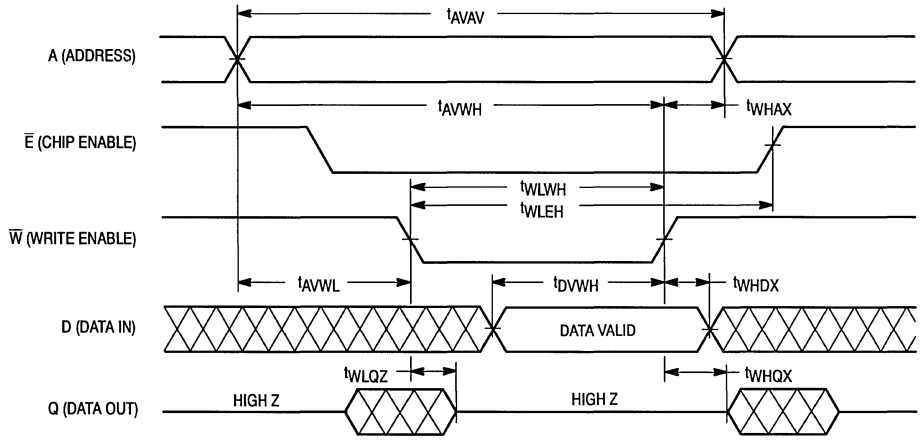
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–15		–20		–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	10	—	12	—	15	—	ns	4
Data Valid to End of Write	t_{DVWH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	0	8	0	10	ns	5,6,7
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)



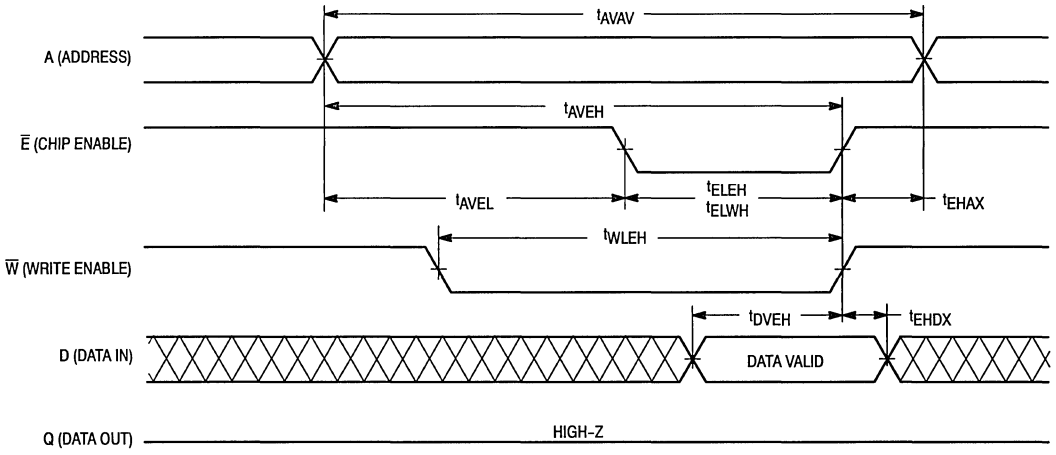
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol	–15		–20		–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	2
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	12	—	15	—	ns	3,4
Write Pulse Width	t_{WLEH}	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

3

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6306D X XX X XX

- MCM: Motorola Memory Prefix
- 6306D: Part Number
- X: Package (J = 300 mil SOJ)
- XX: Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns)
- X: V_{CC} Variance (Blank = ± 0.3 V, B = + 0.3 V, –5%)
- XX: Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6306DJ15, MCM6306DJ15R2, MCM6306DJ15BR2, MCM6306DJ20, MCM6306DJ20R2, MCM6306DJ25, MCM6306DJ25R2

3

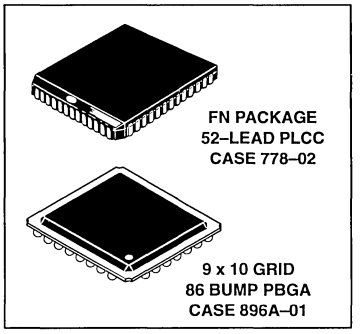
Application Specific Fast Static RAMs

4

4

MCM56824A

DSPRAM™
8K x 24 Bit Fast Static RAM



The MCM56824A is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic.

The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, useful in low–power applications. A single on–chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically re–partitioning the RAM array. Typical applications will logically map vector operands into upper memory with scalar operands being stored in lower memory. By connecting DSP56001 address A15 to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource irrespective of operand type. See application diagrams at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

The MCM56824A is available in a 52 pin plastic leaded chip–carrier (PLCC) and a 9 x 10 grid, 86 bump surface mount PBGA.

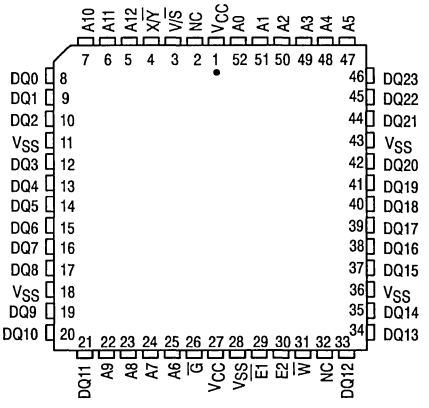
- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 20/25/35 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- Single Bit On–Chip Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three State Outputs
- High Board Density PLCC Package
- Low Power Standby Mode
- Fully TTL Compatible

PIN NAMES	
A0 – A11	Address Inputs
A12, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ23	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

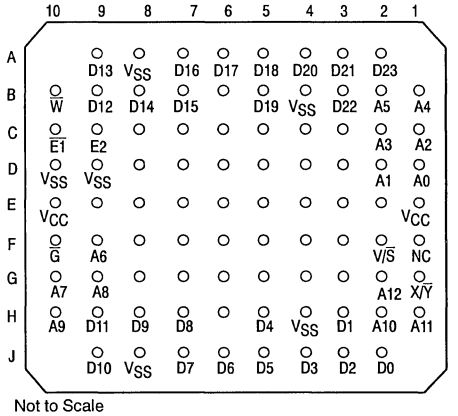
For proper operation of the device, all V_{SS} pins must be connected to ground.

PIN ASSIGNMENTS

PLCC



VIEW OF PBGA PACKAGE BOTTOM

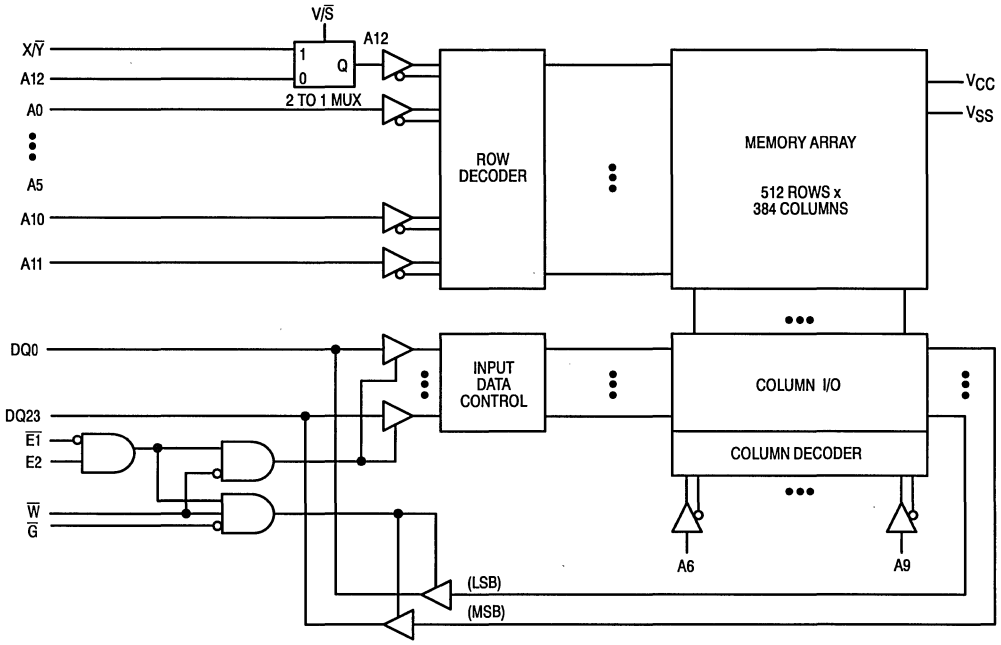


Not to Scale

DSPRAM is a trademark of Motorola, Inc.

REV 2
4/95

BLOCK DIAGRAM



4

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High–Z
X	L	X	X	X	Not Selected	I_{SB}	High–Z
L	H	H	H	X	Output Disable	I_{CC}	High–Z
L	H	L	H	H	Read Using X/$\overline{Y}$	I_{CC}	Data Out
L	H	L	H	L	Read Using A12	I_{CC}	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	I_{CC}	Data In
L	H	X	L	L	Write Using A12	I_{CC}	Data In

NOTE: X=don't care.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.75	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(i)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0 mA, All Other Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V) MCM56824A–20 Cycle Time: ≥ 20 ns MCM56824A–25 Cycle Time: ≥ 25 ns MCM56824A–35 Cycle Time: ≥ 35 ns	I_{CCA}	— — —	260 220 180	mA
Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, All Inputs = V_{IL} or V_{IH})	I_{SB1}	—	15	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0 – DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0 – DQ23	C_{out}	6	8	pF

AC TEST LOADS

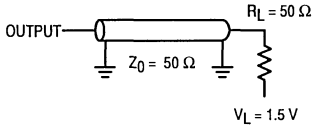


Figure 1A

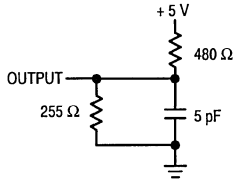


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

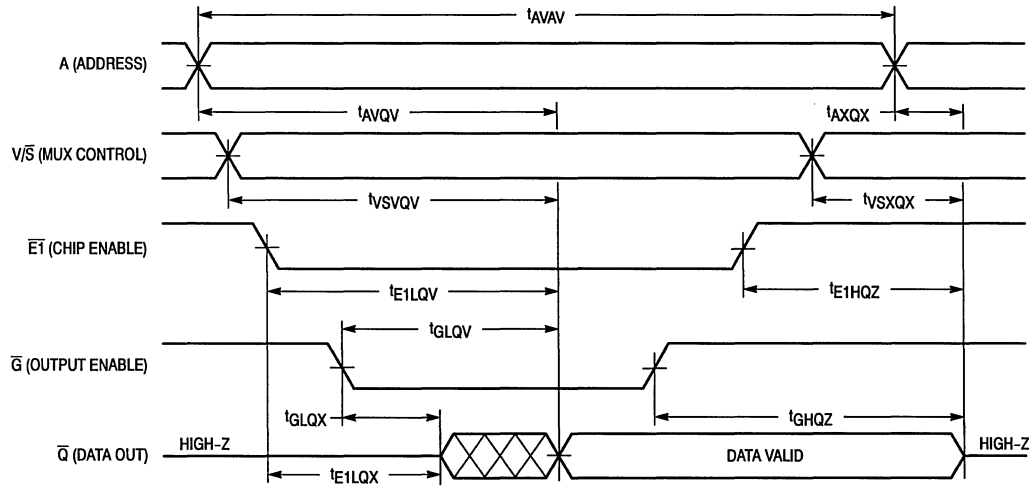
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Access Time	t_{AVQV}	—	20	—	25	—	35	ns	
MUX Control Valid to Output Valid	t_{VSVQV}	—	20	—	25	—	35	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	—	20	—	25	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	—	8	—	10	—	15	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	2	—	2	—	0	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	0	—	0	—	0	—	ns	5
Output Hold from Address Change	t_{AXQX}	4	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	4	—	5	—	5	—	ns	
Chip Enable to Output High–Z	t_{E1HQZ} t_{E2LQZ}	0	10	0	15	0	15	ns	4, 5
Output Enable High to Output High–Z	t_{GHQZ}	0	8	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or vector/scalar transition to the first address or vector/scalar transition.
3. Addresses valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

READ CYCLE

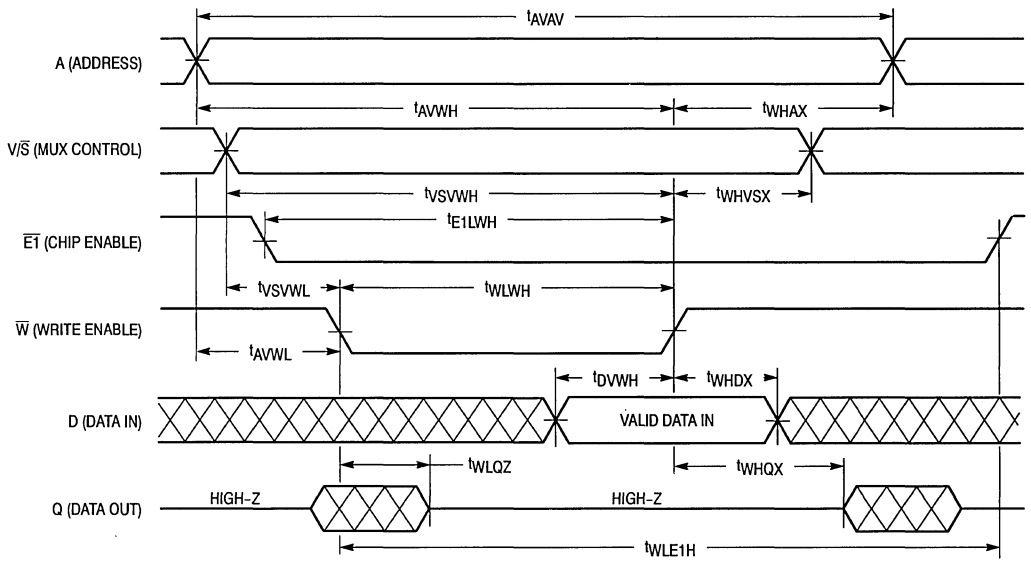


WRITE CYCLE TIMING (Write Enable Initiated, See Note 1)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	20	—	30	—	ns	
MUX Control Valid to End of Write	t_{VSVWH}	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	15	—	15	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	15	—	15	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	15	—	15	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	0	—	0	—	0	—	ns	
Write High to Output Low–Z	t_{WHQX}	4	—	5	—	5	—	ns	6
Write Low to Output High–Z	t_{WLQZ}	0	15	0	15	0	15	ns	6

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. Write must be high for all address transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high–impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

$\overline{WE}$ INITATED WRITE CYCLE



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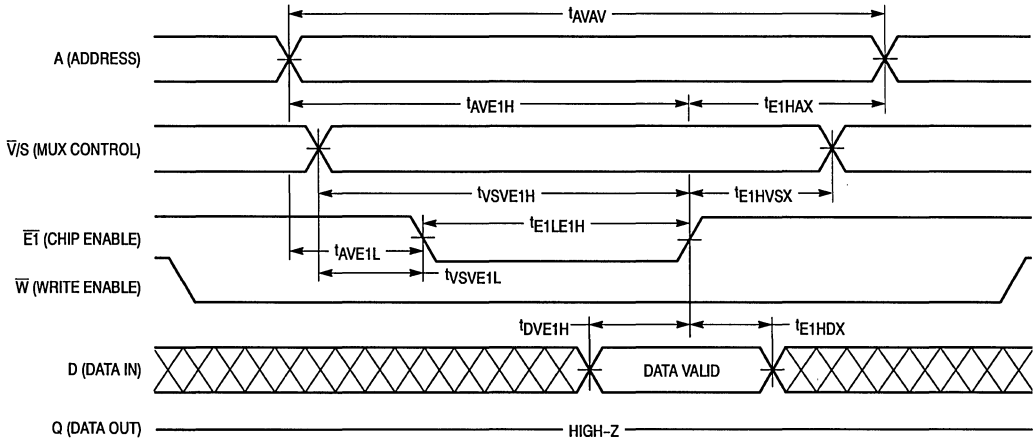
WRITE CYCLE TIMING (Chip Enable Initiated, See Note 1)

Parameter	Symbol	MCM56824A–20		MCM56824A–25		MCM56824A–35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVE1L} t_{AVE2H}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVE1L} t_{VSVE2H}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	15	—	20	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSVE1H} t_{VSVE2L}	15	—	20	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	12	—	15	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	8	—	10	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	0	—	0	—	0	—	ns	2

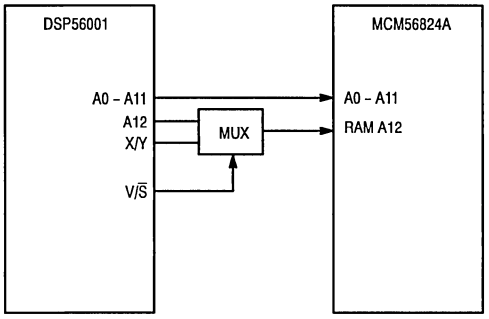
4

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high–impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.

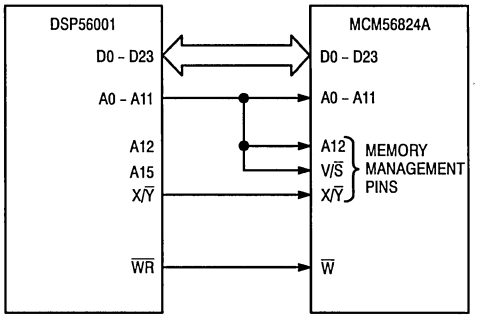
$\overline{E1}$ OR E2 INITIATED WRITE CYCLE

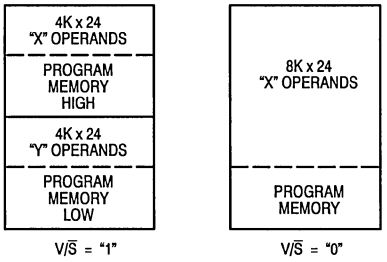


DSPRAM Multiplexed Vector/Scalar Address Maps



8K x 24 DSPRAM Used in Typical Application





4

ORDERING INFORMATION
(Order by Full Part Number)

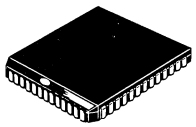
MCM 56824A XX XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = rails)
- Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (FN = PLCC, ZP = PBGA)

Full Part Numbers —	MCM56824AFN20	MCM56824AFN25	MCM56824AFN35
	MCM56824AZP20	MCM56824AZP25	MCM56824AZP35
	MCM56824AZP20R2	MCM56824AZP25R2	MCM56824AZP35R2

32K x 9 Bit Synchronous Dual I/O or Separate I/O Fast Static RAM with Parity Checker

MCM62110



FN PACKAGE
PLASTIC
CASE 778–02

The MCM62110 is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 32K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers, two sets of output latches, active high and active low chip enables, and a parity checker. The RAM checks odd parity during RAM read cycles. The data parity error ($\overline{DPE}$) output is an open drain type output which indicates the result of this check. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

The device has both asynchronous and synchronous inputs. Asynchronous inputs include the processor output enable ($\overline{POE}$), system output enable ($\overline{SOE}$), and the clock (K).

The address (A0 – A14) and chip enable ($\overline{E1}$ and E2) inputs are synchronous and are registered on the falling edge of K. Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of K. Writes to the RAM are self–timed.

All data inputs/outputs, PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three–state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

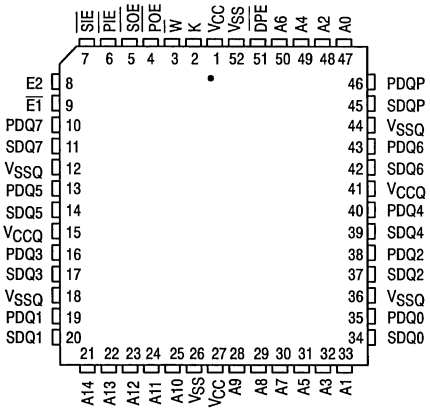
Additional power supply pins have been utilized for maximum performance. The output buffer power (V_{CCQ}) and ground pins (V_{SSQ}) are electrically isolated from V_{SS} and V_{CC}, and supply power and ground only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62110 is available in a 52–pin plastic leaded chip carrier (PLCC).

This device is ideally suited for pipelined systems and systems with multiple data buses and multiprocessing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access and Cycle Times: 15/17/20 ns Max
- Self–Timed Write Cycles
- Clock Controlled Output Latches
- Address, Chip Enable, and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three–State Outputs
- Odd Parity Checker During Reads
- Open Drain Output on Data Parity Error ($\overline{DPE}$) Allowing Wire–ORing of Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package
- Active High and Low Chip Enables for Easy Memory Depth Expansion
- Can be used as Separate I/O x9

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{E1}$	Active Low Chip Enable
E2	Active High Chip Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
$\overline{DPE}$	Data Parity Error
PDQ0 – PDQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0 – SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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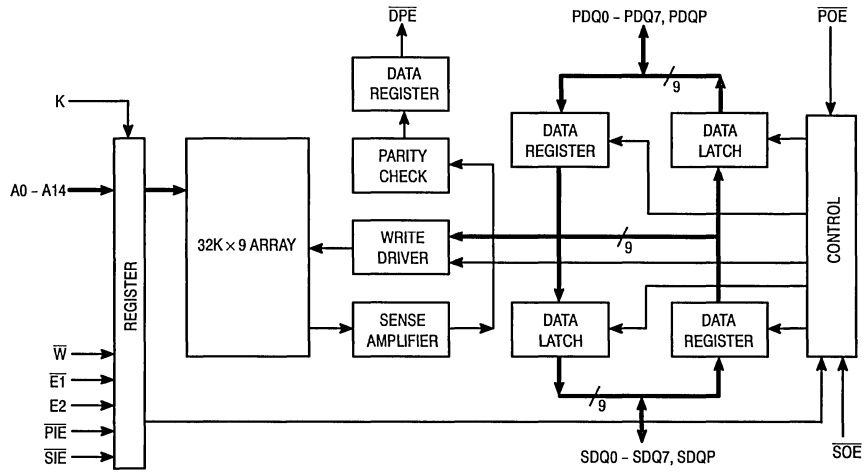
BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE (See Notes 1 and 2)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ0 – PDQ7, PDQP Output	SDQ0 – SDQ7, SDQP Output	$\overline{DPE}$	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High–Z	Parity Out	3, 4
1	1	1	1	0	Read	Copy Back	High–Z	Data Out	Parity Out	3, 4
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	Parity Out	3, 4
1	X	X	1	1	Read	NOP	High–Z	High–Z	1	
X	0	0	X	X	N/A	NOP	High–Z	High–Z	1	2, 5
0	0	1	1	1	Write	Processor Write Hit	Data In	High–Z	1	2, 6
0	1	0	1	1	Write	Allocate	High–Z	Data In	1	2
0	0	1	1	0	Write	Write Through	Data In	Stream Data	1	2, 7
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	1	2, 7
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	1	2, 7
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	1	2, 7
0	1	1	X	X	N/A	NOP	High–Z	High–Z	1	5
X	0	1	0	0	N/A	Invalid	Data In	Stream	1	2, 8
X	0	1	0	1	N/A	Invalid	Data In	High–Z	1	2, 8
X	1	0	0	0	N/A	Invalid	Stream	Data In	1	2, 8
X	1	0	1	0	N/A	Invalid	High–Z	Data In	1	2, 8

NOTES:

1. A '0' represents an input voltage ≤ V_{IL} and a '1' represents an input voltage ≥ V_{IH}. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. This table assumes that the chip is selected (i.e., $\overline{E1}$ = 0 and E2 = 1) and V_{CC} current is equal to I_{CCA}. If this is not true, the chip will be in standby mode, the V_{CC} current will equal I_{SB1} or I_{SB2} $\overline{DPE}$ will default to 1 and all RAM outputs will be in High–Z. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAM's behavior is not specified.
2. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don't care, and the corresponding outputs are High–Z.
3. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
4. $\overline{DPE}$ is registered on the rising edge of K at the beginning of the following clock cycle
5. No RAM cycle is performed.
6. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0 – PDQ7 and PDQP or SDQ0 – SDQ7 and SPDQ), and written into the RAM.
7. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
8. Data contention will occur.

PARITY CHECKER

Parity Scheme	$\overline{DPE}$
$\overline{E1} = V_{IH}$ and/or $E2 = V_{IL}$	1
$RAMP = \overline{RAM0} \oplus \overline{RAM1} \oplus \ldots \oplus \overline{RAM7}$	1
$RAMP \neq \overline{RAM0} \oplus \overline{RAM1} \oplus \ldots \oplus \overline{RAM7}$	0

NOTE: RAMP, $\overline{RAM0}$, $\overline{RAM1}$ . . . , refer to the data that is present on the RAMs internal bus, not necessarily data that resides in the RAM array. $\overline{DPE}$ is always delayed one clock, and is registered on the rising edge of K at the beginning of the following clock cycle (see AC CHARACTERISTICS).

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62110–15: t_{KHKH} = 15 ns MCM62110–17: t_{KHKH} = 17 ns MCM62110–20: t_{KHKH} = 20 ns	I_{CCA}	 — — —	 190 190 190	mA
TTL Standby Current (V_{CC} = Max, $\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	40	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA, $\overline{DPE}$: I_{OL} = + 23.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except I/Os)	C_{in}	2	3	pF
Input/Output Capacitance (PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, SDQP)	C_{out}	6	7	pF
Data Parity Error Output Capacitance ($\overline{DPE}$)	$C_{out(DPE)}$	6	7	pF

AC SPEC LOADS

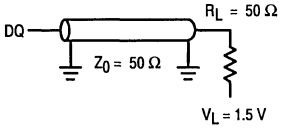


Figure 1A

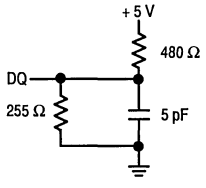


Figure 1B

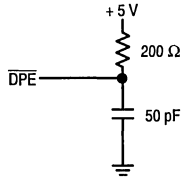


Figure 1C

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

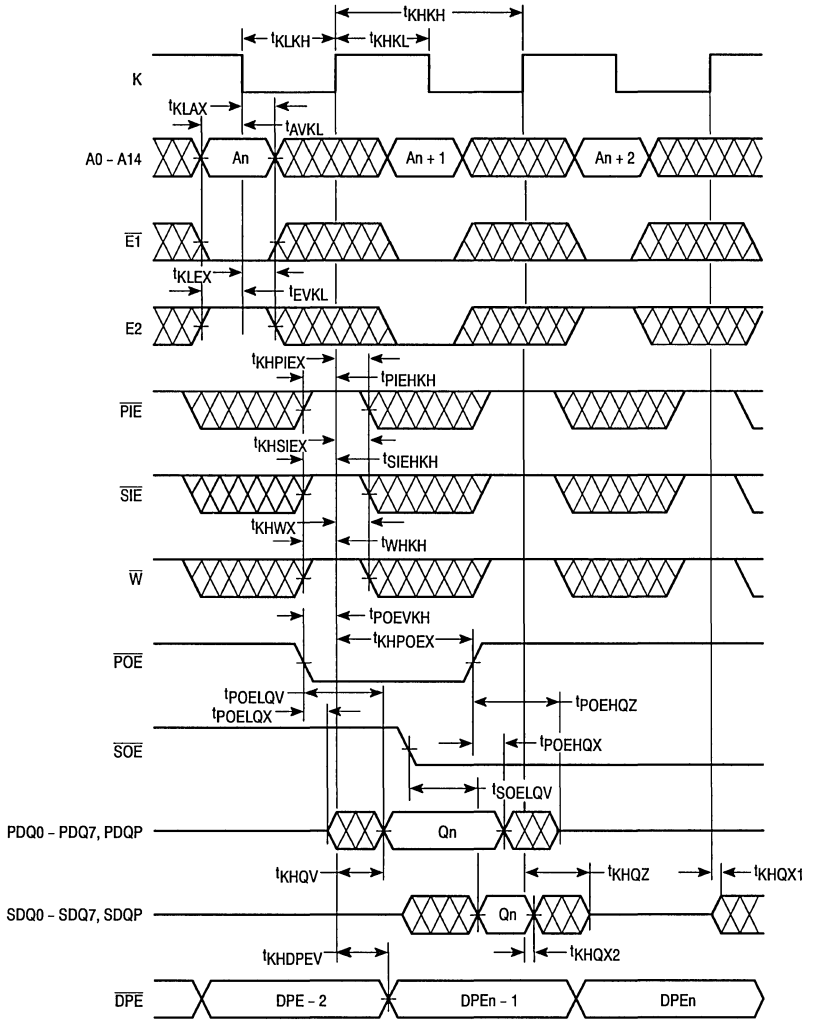
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Measurement Timing Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62110–15		MCM62110–17		MCM62110–20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time Clock High to Clock High	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Clock High to $\overline{DPE}$ Valid	t_{KHDPEV}	—	7	—	8	—	10	ns	5
Clock High to Output Valid	t_{KHQV}	—	7	—	7.5	—	10	ns	4, 3
Clock (K) High to Output Low Z After Write	t_{KHQX1}	8	—	8	—	8	—	ns	
Output Hold from Clock High	t_{KHQX2}	5	—	5	—	5	—	ns	4, 6
Clock High to Q High–Z ($\overline{E1}$ or E2 = False)	t_{KHQZ}	—	8	—	9	—	10	ns	6
Setup TImes: A	t_{AVKL}	2.5	—	2.5	—	2.5	—	ns	
$\overline{W}$	t_{WHKH}								
$\overline{E1}$, E2	t_{EVKL}								
$\overline{PIE}$	t_{PIEHKH}								
$\overline{SIE}$	t_{SIEHKH}								
$\overline{POE}$	t_{POEVKH}								7
$\overline{SOE}$	t_{SOEVKH}								7
Hold Times: A	t_{KLAX}	2	—	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}								
$\overline{E1}$, E2	t_{KLEX}								
$\overline{PIE}$	t_{KHPIEX}								
$\overline{SIE}$	t_{KHSIEX}								
$\overline{POE}$	t_{KHPOEX}								7
$\overline{SOE}$	t_{KHSOEX}								7
Output Enable High to Q High–Z	t_{POEHQZ} / t_{SOEHQZ}	0	8	0	9	0	9	ns	6
Output Hold from Output Enable High	t_{POEHQX} / t_{SOEHQX}	5	—	5	—	5	—	ns	6
Output Enable Low to Q Active	t_{POELQX} / t_{SOELQX}	0	—	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} / t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. Access time is controlled by t_{KLQV} if the clock low pulse width is less than (t_{KLQV}–t_{KHQV}); otherwise it is controlled by KHQV.
4. K must be at a high level for outputs to transition.
5. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.
7. These read cycle timings are used to guarantee proper parity operation only.

READ CYCLE (See Notes)



NOTES:
1. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

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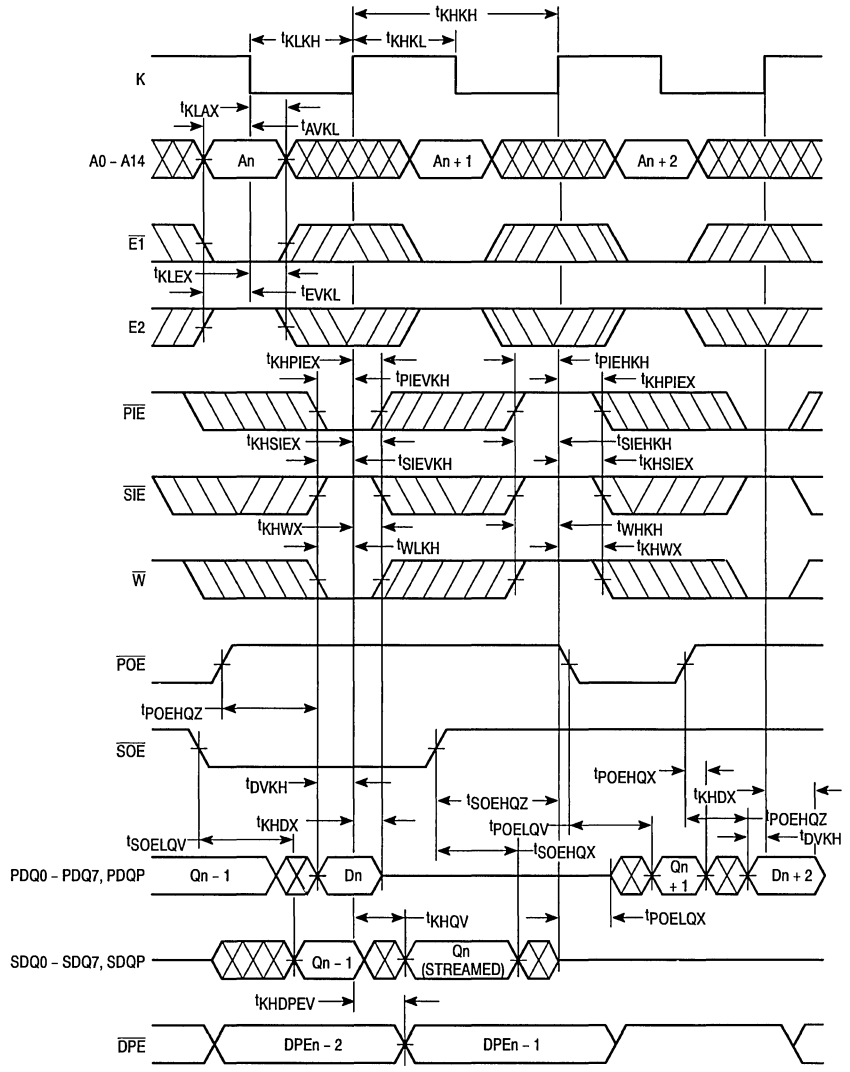
WRITE CYCLE (See Note 1)

Parameter	Symbol	MCM62110–15		MCM62110–17		MCM62110–20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Clock High to Output High–Z ($\overline{W} = V_{IL}$ and $\overline{SIE} = \overline{PIE} = V_{IH}$)	t_{KHQZ}	—	8	—	9	—	10	ns	3, 4
Setup Times: A $\overline{W}$ $\overline{E1}$, E2 $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{AVKL} t_{WLKH} t_{EVKL} t_{PIEVKH} t_{SIEVKH} t_{DVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: A $\overline{W}$ $\overline{E1}$, E2 $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KLAX} t_{KHWX} t_{KLEX} t_{KHPIEX} t_{KHSIEX} t_{KHDX}	2	—	2	—	2	—	ns	
Write with Streaming ($\overline{PIE} = \overline{SOE} = V_{IL}$ or $\overline{SIE} = \overline{POE} = V_{IL}$) Clock High to Output Valid	t_{KHQV}	—	7	—	7.5	—	8	ns	5
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	5	—	5	—	5	—	ns	
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A write is performed with $\overline{W} = V_{IL}$, $\overline{E1} = V_{IL}$, E2 = V_{IH} for the specified setup and hold times and either $\overline{PIE} = V_{IL}$ or $\overline{SIE} = V_{IL}$. If both $\overline{PIE} = V_{IL}$ and $\overline{SIE} = V_{IL}$ or $\overline{PIE} = V_{IH}$ and $\overline{SIE} = V_{IH}$, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. K must be at a high level for the outputs to transition.
4. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} for a given device.
5. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

WRITE THROUGH — READ — WRITE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is written.

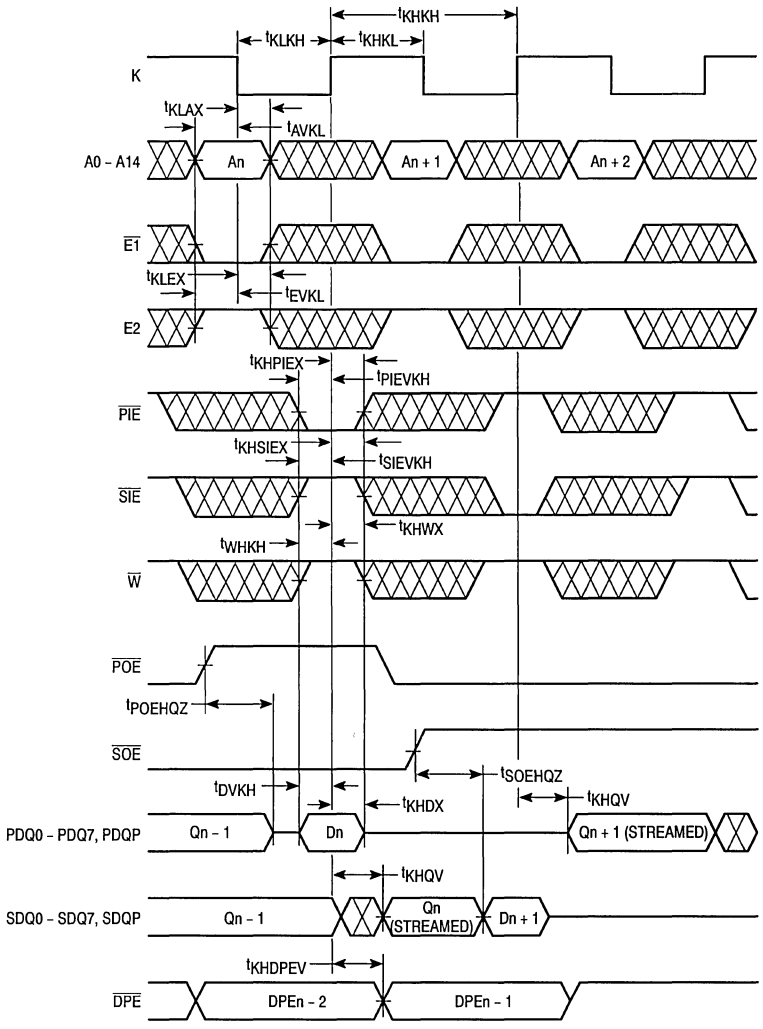
4

STREAM CYCLE (See Note 1)

Parameter	Symbol	MCM62110–15		MCM62110–17		MCM62110–20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Stream Cycle Time	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Stream Access Time	t_{KHQV}	—	7	—	7.5	—	8	ns	
Setup Times: A	t_{AVKL}	2.5	—	2.5	—	2.5	—	ns	
$\overline{W}$	t_{WHKH}								
$\overline{E1}$, E2	t_{EVKL}								
$\overline{PIE}$	t_{PIEVKH}								
$\overline{SIE}$	t_{SIEVKH}								
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}								
Hold Times: A	t_{KLAX}	2	—	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}								
$\overline{E1}$, E2	t_{KLEX}								
$\overline{PIE}$	t_{KHPIEX}								
$\overline{SIE}$	t_{KHSIEX}								
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}								
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	3
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	3
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, and t_{KHQZ} is less than t_{KHQX} for a given device.

STREAM CYCLE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

ORDERING INFORMATION
(Order by Full Part Number)

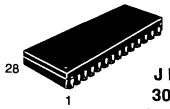
MCM	62110	FN	XX
Motorola Memory Prefix			Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns)
Part Number			Package (FN = PLCC)

Full Part Numbers — MCM62110FN15 MCM62110FN17 MCM62110FN20

Synchronous Line Buffer: 8K x 8 Bit Fast Static Dual Ported Memory

With IEEE Standard 1149.1 Test Access Port and Boundary–Scan (JTAG)

MCM62X308



J PACKAGE
300 MIL SOJ
CASE 810B–03

The MCM62X308 is a synchronous, dual ported memory organized as 8,192 words of 8 bits each, fabricated using Motorola's double–metal, double–poly, 0.65 μm CMOS process. It is intended for high speed video or other applications which process data on a line–by–line basis. Through the use of a single clock and port control inputs, separate read and write data ports provide simultaneous access to a common memory array. Simultaneous read/write access to the same address location is also allowed, with old data being read followed by a write of the new data. This allows multiple devices to be cascaded with the output of one directly driving the input of another. In this configuration the data stream can be tapped at strategic interconnect points to perform various digital filtering functions.

Since there are no external address inputs, separate internal read and write address counters are provided as a means of indexing the memory array. These counters are preloaded and then selectively incremented or decremented by asserting read enable (RE) and write enable (WE) inputs, allowing cycle to cycle control. The address counters can be reloaded back to their initial values through the use of the read reload ($\overline{RR}$) and write reload ($\overline{WR}$) control inputs. These inputs initiate the transfer of address reload register values into the address counters which index the memory array. When an address counter reaches 0000 (on down count) or FFFF (on up count), it will roll over on the next count. The TDI input is used to write the reload registers using special test access port instructions.

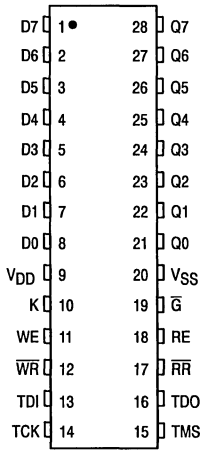
The read and write address counters are 16 bits long, and only 13 of the 16 bits are required to index the 8K deep memory array. The remaining three bits are used for depth expansion. These three bits are compared to the lower three bits in the control register, and as long as they are equal that port (i.e., read or write) will remain active. If the bits do not compare, the port will become inactive (i.e., for read outputs, high–z; for write inputs, disabled) however, the counter will continue to count on the rising edge of K as long as the port enable signal (RE or WE) is asserted. The TDI input is used to write the control register using special test access port instructions.

The output enable Input can be programmed to be either synchronous or asynchronous through the control register.

The MCM62X308 is available in a 28 pin SOJ package.

- 8K x 8 Fast Access Static Memory Array
- Single 5 V Power Supply — MCM62X308–15–5: ± 5%
  MCM62X308–17: ± 10%
- Synchronous, Simultaneous Read/Write Memory Access
- 50 MHz Maximum Clock Cycle Time, < 15 ns Read Access
- Single Clock Operation
- Separate Read/Write Address Counters with Reload Control
- Separate Up/Down Counter Control for Both Read and Write
- Programmable Output Enable Control (Synchronous or Asynchronous)
- Cascadable I/O Interface
- IEEE Standard 1149.1 Test Port (JTAG)
- Expand ID Register for Depth Expansion
- High Board Density SOJ Package
- Fully TTL Compatible

PIN ASSIGNMENT



PIN NAMES

K	Clock Input
WE	Write Enable Input
$\overline{WR}$	Write Address Reload Input
RE	.Read Enable Input
$\overline{RR}$	Read Address Reload Input
$\overline{G}$	Output Enable Input
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{DD}	+ 5 V Power Supply
V_{SS}	Ground

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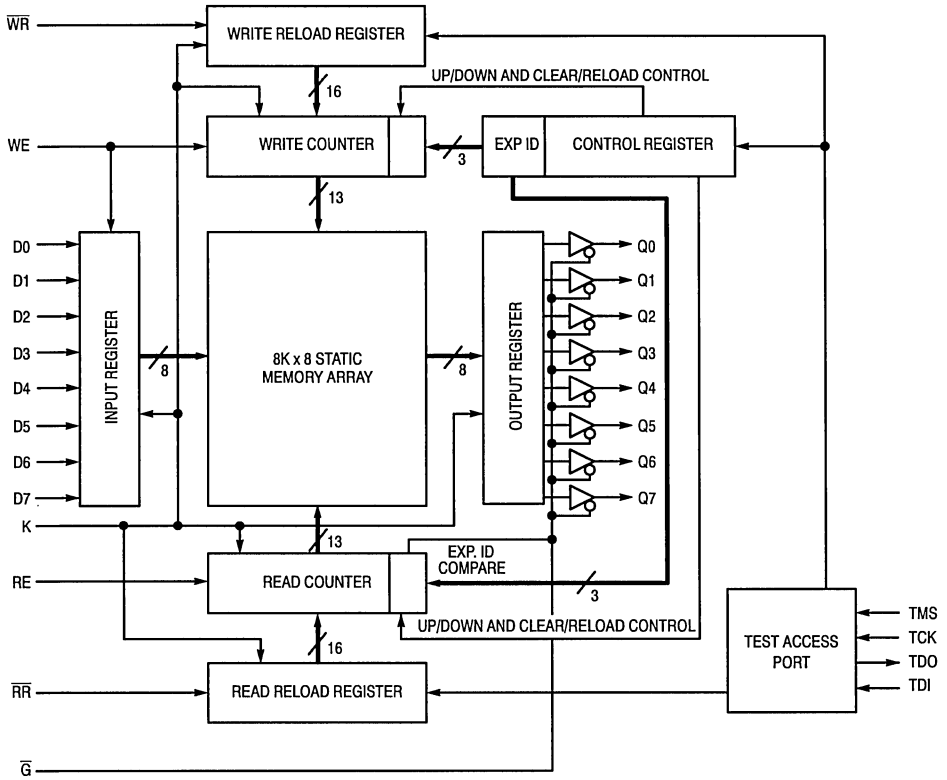
BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

WE	$\overline{WR}$	RE	$\overline{RR}$	$\overline{G}$	Match EXP ID (Read/Write)	Mode (Read/Write)	Supply Current	Q0 – 7 Status
X	L	X	L	L	Match Read/Match Write	Reload, Read/Reload, Write Disable	I_{CC}	Data Out
H	H	H	H	L	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	Data Out
L	H	L	H	L	Match Read/Match Write	Read Count Disable/Write Disable	I_{CC}	Data Out
H	H	H	H	H	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	High–Z
H	H	H	H	X	No Match Read/No Match Write	Count, No Read/No Write, Count	I_{SB}	High–Z
H	H	H	H	X	No Match Read/Match Write	Count, No Read/Write, Count	I_{SB}	High–Z
H	H	H	H	L	Match Read/No Match Write	Count, Read/No Write, Count	I_{CC}	Data Out

PIN DESCRIPTIONS

SOJ Pin Locations	Symbol	Type	Description
10	K	Input	**CLOCK** – System clock input pin accepting a minimum 8 ns clock high or clock low pulse at a minimum 20 ns clock cycle. All other synchronous inputs excluding the test access port are captured on the rising edge of this signal.
11	WE	Input	**WRITE ENABLE** – Write enable is captured on K leading edge. When asserted this causes the input data D0 – D7 to be written into the RAM address controlled by the write address counter and increments the counter for the next write.
18	RE	Input	**READ ENABLE** – Read enable is captured on K leading edge. When asserted increments the counter for the next read operation. This causes a read access from the RAM address controlled by the read address counter to be inserted in the output register Q0 – Q7.
12	$\overline{WR}$	Input	**WRITE RELOAD** – Write reload is captured on K leading edge. When asserted this causes the write address counter to be initialized to the contents of the write reload register or "cleared" as specified by control register bit 3. See control register bit 3 for "cleared" description.
17	$\overline{RR}$	Input	**READ RELOAD** – Read reload is captured on K leading edge. When asserted this causes the read address counter to be initialized to the contents of the read reload register or "cleared" as specified by control register bit 5. See control register bit 5 for "cleared" description.
19	$\overline{G}$	Input	**OUTPUT ENABLE** – When asserted low causes the outputs Q0 – Q7 to become active and when deasserted high causes them to High–Z. This pin can be either synchronous with K leading edge or asynchronous as specified by control register bit 7.
8, 7, 6, 5, 4, 3, 2, 1	D0 – D7	Input	**DATA INPUT**– The levels on these pins are captured on the K leading edge. The value captured will be written into the RAM if WE is also asserted and the expand ID bits match the upper three bits of the write address counter.
21, 22, 23, 24, 25, 26, 27, 28	Q0 – Q7	Output	**DATA OUTPUT** – Data outputs are available from the read output register < 15 ns from the rising edge of K when RE or $\overline{RR}$ is asserted. outputs are disabled when the upper three bits of the read address counter do not match the three expand ID bits of the control register. $\overline{G}$ will also control the disabling of the outputs either synchronously or asynchronously. See $\overline{G}$ description.

TEST ACCESS PORT PIN DESCRIPTIONS (The Test Access Port Conforms with the IEEE Standard 1149.1. It is also Used to Load Device Specific Registers Used to Configure the MCM62X308.)

SOJ Pin Locations	Symbol	Type	Description
14	TCK	Input	**TEST CLOCK** – Samples and clocks all TAP events. All inputs are captured on TCK rising edge and all outputs propagate from TCK falling edge. It also can take the place of K in device operation in certain test conditions.
15	TMS	Input	**TEST MODE SELECT** – Sampled on the rising edge of TCK. Determines the movement through the TAP state machine (Figure 2). This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
13	TDI	Input	**TEST DATA IN** – Sampled on the rising edge of TCK. This is the input side of the serial register placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP state machine and what instruction is active in the TAP instruction register. This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
16	TDO	Output	**TEST DATA OUT** – Output that is active depending on the state of the TAP state machine. Output changes off the trailing edge of TCK. This is the output side of the serial register placed between TDI and TDO.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITICS

(T_A = 0 to 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	MCM62X308–15–5	V_{DD}	4.75	5.0	5.25	V
	MCM62X308–17		4.50	5.0	5.50	
Input High Voltage		V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time = 20 ns)	I_{CCA}	—	150	mA
AC Standby Current (When Expand ID Bits Do Not Match the Read Address Counter, Cycle Time = 20 ns)	I_{SB}	—	100	mA
Output Low Voltage (I_{OL} = + 4.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance (Q0 – Q7, TDO)	C_{out}	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... Terminated 50 Ohm Transmission Line

READ/WRITE CYCLE TIMING

Parameter		Symbol	MCM62X308–15–5 Min	MCM62X308–15–5 Max	MCM62X308–17 Min	MCM62X308–17 Max	Unit	Notes
Cycle Time		t_{KHKH}	20	—	22	—	ns	
Clock High Time		t_{KHKL}	8	—	9	—	ns	
Clock Low Time		t_{KLKH}	8	—	9	—	ns	
Clock High to Output Valid		t_{KHQV}	5	15	5	17	ns	
Clock High to Output High–Z		t_{KHQZ}	5	15	5	15	ns	1
Output Enable Low to Output Valid		t_{GLQV}	3	10	3	10	ns	2, 4
Output Enable High to Output High–Z		t_{GHQZ}	0	5	0	5	ns	2, 3, 4
Setup Times:	RE	t_{REVKH}	2	—	2	—	ns	5
	WE	t_{WEVKH}						
	$\overline{WR}$	t_{WRVKH}						
	$\overline{G}$	t_{GVKH}						6
	$\overline{RR}$	t_{RRVKH}	3	—	3	—		5
	Data In	t_{DVKH}	1	—	1	—		5
Hold Times:	RE	t_{KHREX}	2	—	2	—	ns	5
	WE	t_{KHWEX}						
	$\overline{RR}$	t_{KHRRX}						
	$\overline{WR}$	t_{KHWRX}						
	$\overline{G}$	t_{KHGX}						6
	Data In	t_{KHDX}						

NOTES:
1. The outputs High–Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
2. $\overline{G}$ is a don't care when the three ID expansion bits do not match the upper three bits of the Read Address Counter.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction).
4. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQV} min for a given device and from device to device.
5. This is a synchronous device. All inputs must meet the specified setup and hold times for ***ALL*** rising edges of Clock except for $\overline{G}$ when it is programmed to be asynchronous.
6. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.

AC TEST LOADS

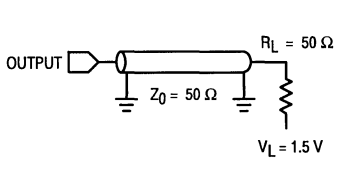


Figure 1A

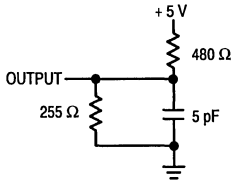
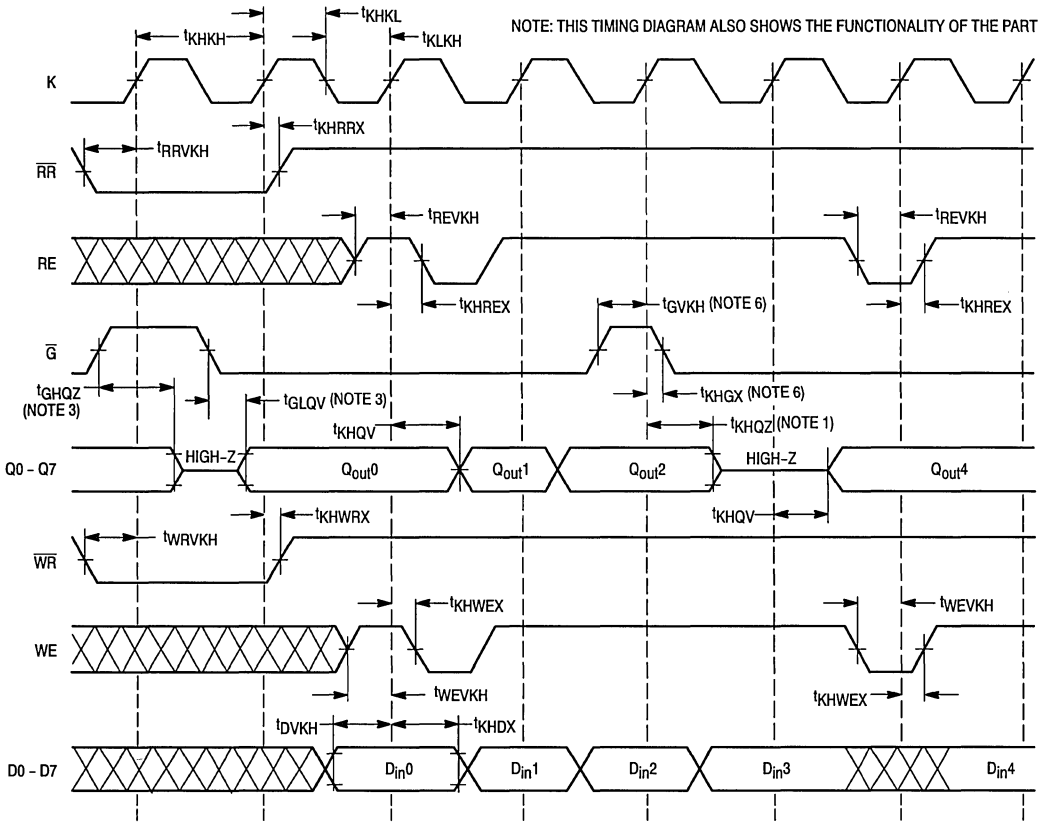


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ/WRITE CYCLE TIMING DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... 50 Ohm Transmission Line

TAP CONTROLLER TIMING

Parameter	Symbol	MCM62X308–15–5		MCM62X308–17		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CYC}	30	—	30	—	ns	
Clock High Time	t_{CKH}	12	—	12	—	ns	
Clock Low Time	t_{CKL}	12	—	12	—	ns	
Clock Low to Output Valid	t_A	5	9	5	9	ns	
Clock Low to Output High–Z	t_{CKZ}	0	9	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	0	9	ns	2, 3
Setup Time, Test Mode Select	t_S	2	—	2	—	ns	
Setup Time, Test Data In	t_{SD}	2	—	2	—	ns	
Hold Time, Test Mode Select	t_H	2	—	2	—	ns	
Hold Time, Test Data In	t_{HD}	2	—	2	—	ns	

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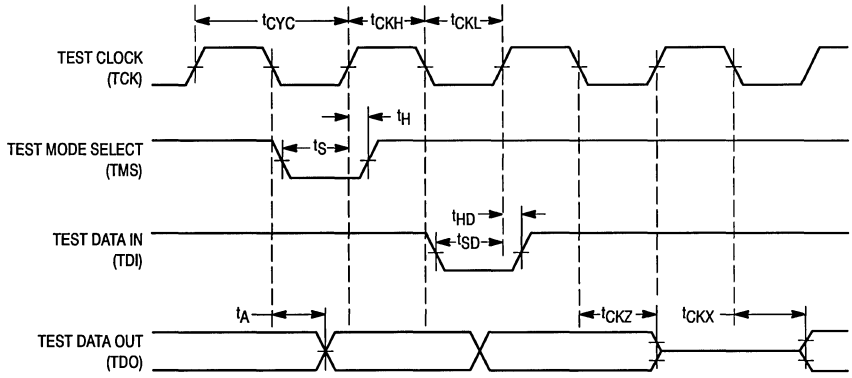
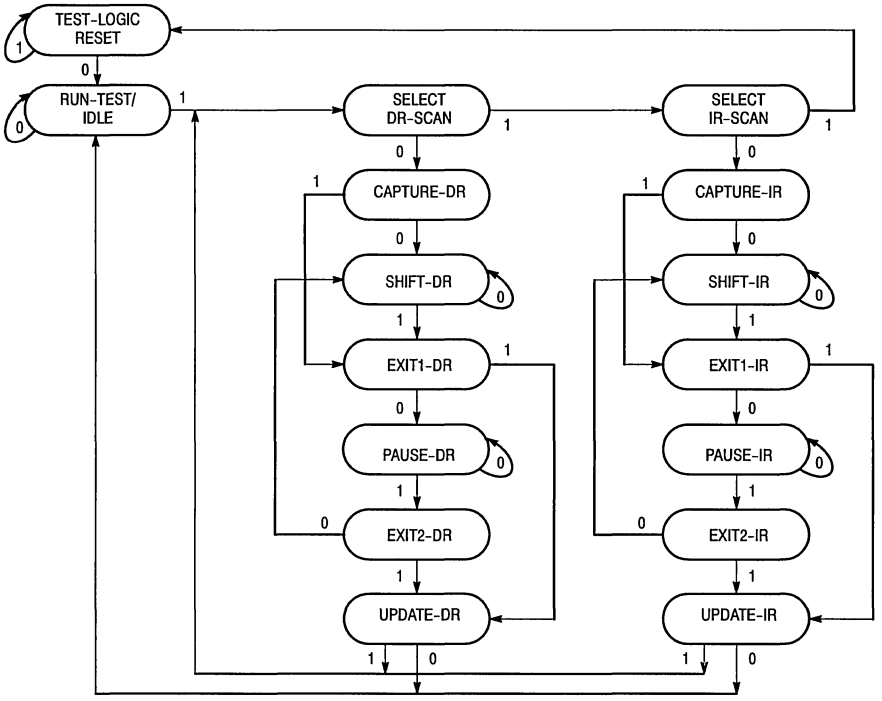
NOTES:
1. Test Data Out will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. Test Data Out is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

TAP CONTROLLER TIMING DIAGRAM





NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 2. TAP Controller State Diagram

TEST ACCESS PORT DESCRIPTIONS

INSTRUCTION SET

A four pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. There are two classes of instructions; standard instructions as defined in the IEEE 1149.1 standard and device specific, or public, instructions that are used to control the functionality of the device. When the TAP (Test Access Port) controller is in the Shift–IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction would be serially loaded through the TDI input (while 0101 will be shifted out of TDO). The TAP instruction set for this device is listed in Table 1.

TAP STANDARD INSTRUCTION SET

NOTE: The descriptions in this section are not intended to be used without the supporting IEEE 1149.1–1993 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instuction is used to allow scanning of the boudary–scan register without causing interference to the normal operation of the chip logic. The 22 bit boundary scan register contains bits for all device signal and clock pins and associated control signals (Table 2). This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. See the EXTEST instruction explanation below. It could also be used prior to the INTEST instruction to preload values into the input pins. As data is written into TDI, data also streams out of TDO which can be used to pre–sample the inputs and outputs. SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

Table 2 shows the boundary–scan bit definitions. The first column defines the bit's ordinal position in the boundary–scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted is 21. The second column is the pin name and the third column is the pin type.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins (i.e., Q0 – Q7). The EXTEST instruction would

then be loaded. During EXTEST the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run–Test/Idle state. In this state one cycle of TCK would cause the preloaded data on the ouput pins to be driven while the values on the input pins would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero). Note that TCK, not the Clock pin, K, is used as the clock input while K is only sampled during EXTEST. The input pins are sampled in the Captor–DR state. After one clock cycle of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). While in the Shift–DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run–Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary–scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will be sampled regardless of $\overline{G}$). Only one action will be performed in the Run–Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

Since device functionality can only be verified through sampling the outputs of the device, the most likely use of INTEST would be to first load up the boundary–scan register for a Write Reload and execute the reload in the Run–Test/Idle state. Then a write of the first address would be performed again using the boundary scan register to load up the input registers and executing the write in the Run–Test/Idle state. Lastly, a Read Reload would be executed in the same manner so that the data that had just been written in the first address would be read from the memory array and written into the output registers which would then be shifted out of TDO in the Shift–DR state.

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Table 1. TAP Instruction Set

Instruction	Code (Binary)	Description
Standard Instructions:		
BYPASS	1111*	Bypass Instruction
INTEST	0111	Intest Instruction
SAMPLE/PRELOAD	1100	Sample and/or Preload Instruction
EXTEST	0000	Extest Instruction
HIGHZ	1010	High–Z all Output pins while bypass reg. is between TDI and TDO
CLAMP	1001	Clamp Output pins while bypass reg. is between TDI and TDO
Device Specific (Public) Instructions:		
LDRREG	0001	Load Read Address Reload Register
LDWREG	0100	Load Write Address Reload Register
LDBREG	0101	Load both Address Reload Registers (Write then Read)
LDCONT	0010	Load Control Register
RDCOUNT	1000	Read the values of the Read and Write Address Counters
EZWRITE	0011	Serial Write (using Write Address Counter)
EZREAD	0110	Serial Read (using Read Address Counter)
EZREADZ	1110	Serial Read, outputs High–Z

*Default state at power–up.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values to be driven on the output pins when the CLAMP instruction is active. Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero.

HIGH–Z TAP INSTRUCTION

The High–Z instruction is provided to allow all the outputs to be placed in an inactive drive state (High–Z). During the High–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The Bypass instruction is the default instruction loaded in at power up. This instruction will place a single shift register between TDI and TDO during the Shift–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit Number	Pin Name	Pin Type
0	$\overline{RR}$	Input
1	RE	Input
2	$\overline{G}$	Input
3	Q0	Output
4	Q1	Output
5	Q2	Output
6	Q3	Output
7	Q4	Output
8	Q5	Output
9	Q6	Output
10	Q7	Output
11	D7	Input
12	D6	Input
13	D5	Input
14	D4	Input
15	D3	Input
16	D2	Input
17	D1	Input
18	D0	Input
19	K	Input
20	WE	Input
21	$\overline{WR}$	Input

NOTE: K is a sample–only scan bit. It cannot be pre–loaded for control purposes.

DEVICE SPECIFIC (PUBLIC) INSTRUCTIONS

LDCONT INSTRUCTION

The Control Register is an eight bit register that contains the control bits for the Address Registers and Counters and the Output Enable pin. When the LDCONT TAP instruction is loaded into the Instruction Register, the Control Register is placed between TDI and TDO when the TAP controller is in the Shift–DR state (Table 10). The power–up/preload state and function of the Control bits are found in Table 3.

The Expand ID bits provide system depth expansion. These three bits are compared to the upper three bits in the address counters. As long as the three Expand–ID bits match the three upper bits in the address counters the port will stay active. If they do not match, the port will deactivate (i.e., outputs will High–Z or write will be disabled); however, the counters will continue counting as long as RE and WE remain asserted (i.e., high) at the rising edge of Clock.

The Reload Control bits (3 and 5) are used to control either reloading the Read and Write Address Counters from the Reload Registers or clearing the counter when $\overline{RR}$ or $\overline{WR}$ is asserted. If these bits are set low the counters they control will be cleared to all zeroes if the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted and any value in the Reload Register is ignored. This means that if the initial address value desired is address 0000 (or FFFF when counting down) then there is no need to load the Address Reload Registers using the LDRREG, LDWREG, or the LDBREG instructions in the following description. If these bits are set high the counters are loaded up with the values in the Reload Registers when the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted.

The Up/Down count bits (4 and 6) determine the direction in which the respective Address Counter will count; if the bit is set low the counter will count up and if set high the counter will count down. If the counters are set to count down and the Reload control is set to the clear counter mode, then the initial value in the counters will be FFFF. To ensure that the counter will function properly, a reload (using $\overline{RR}$ or $\overline{WR}$) is required after the count direction is switched.

The Output Enable control bit (7) determines the functionality of the Output Enable pin, $\overline{G}$. When the bit is low, $\overline{G}$ functions asynchronously. When set high, $\overline{G}$ functions synchronously and must meet the specified setup and hold times to the Clock K.

The Control Register will also be preloaded. When the instruction 0010 (LDCONT) is in the Instruction Register and the controller is in the Capture–DR state the above preload values (all zeroes) will be loaded into the Control Register. All zeroes will also be loaded in the Control Register at power–up.

While new values are shifted in from TDI in the Shift–DR state, all zeroes will be output on TDO for the first eight bits.

LDRREG, LDWREG, AND LDBREG TAP INSTRUCTIONS

There are three instructions that may be used to load the 16 bit address reload registers: LDRREG (Load Read Address Reload Register), LDWREG (Load Write Address Reload Register), and LDBREG (Load both Address Reload Registers, Write followed by Read). Figure 3 illustrates how the Reload registers are placed between TDI and TDO. Tables 7, 8, and 9 describe each register. These instructions would be used only if the user needed to load the Reload Registers with a non–zero value. If the Address Counters are to always be reset to zeroes (or all 1s if counting down) then only the Control Register need be loaded to affect a reset of the counters.

The TAP controller has been set up to make it easier for the user to serially load the Reload Registers. When the TAP controller is clocked into the Capture–IR state (see state diagram) the instruction for loading both registers (0101) will be preloaded into the shift register. This allows the user to go directly to the Update–IR state instead of having to serially shift this instruction in through the TDI port. Once the load instruction has been entered the user can then clock over to the Capture–DR state where the value for the reload register(s) is serially loaded (see Figure 3).

RDCOUNT TAP INSTRUCTION

The RDCOUNT scan register is accessible after the RDCOUNT instruction is loaded into the TAP instruction register in the Shift–IR state and the TAP controller is then moved to the Shift–DR state. This scan register can then be used to shift out the values of the Read and Write Address Counters The RDCOUNT scan–register is a sample only register and can not be used to load values into the counters. See Table 4.

EZWRITE TAP INSTRUCTION AND SCAN PATH

The EZWRITE TAP instruction is provided to allow the user to more easily and quickly write a large number of bytes to the

device serially through the TDI port. EZWRITE shortens the scan path for a serial write to just the 8 bit Data in register (see Table 5).

The most likely use of this instruction is as follows: the user would first load the Control Register using the LDCONT instruction. This would initialize the Expand ID bits and the Write Counter. The Write Reload Register will need to be loaded using the LDWREG instruction if a non–zero starting address is desired. If 0000 was the first desired count, setting up the Control Register to "clear" the Write counter is all that is required (Bit 3 set to zero). A reload cycle using SAMPLE/PRELOAD ($\overline{WR}$ preloaded low) and INTEST would also have to be run in order to initialize the counter. While still in the INTEST instruction at the Shift–DR state, the proper values of WE and $\overline{WR}$ would then need to be preloaded for proper operation of EZWRITE (WE high and $\overline{WR}$ high). After all this initializing is done, the EZWRITE instruction would be loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state the EZWRITE scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data In register (see Table 5). The 8 bits to be written into the first address would be scanned in (sampled values from the Data In pins would be streaming out of TDO at the same time), then the TAP controller would be moved to the Run–Test/Idle state where one cycle of TCK would write the 8 bits into the address and increment the counter. The TAP controller would then move back to the Shift–DR state so that the next byte to be written can be serially loaded and the process would be repeated until all desired bytes were written. During EZWRITE the Q0 – Q7 pins will be in a High–Z state.

Table 3. Control Register Bit Description

Bit No.	Power Up and Preload State	Function
0 – 2	000	Expand ID bits for comparison with the upper 3 bits of the Read and Write Address counters
3	0	Reload Control of Write Address Counter (0 = clear counter, 1 = reload)
4	0	Up/Down count bit for Write Address Counter (0 = count up, 1 = count down)
5	0	Reload Control of Read Address Counter (0 = clear counter, 1 = reload)
6	0	Up/Down count bit for Read Address Counter (0 = count up, 1 = count down)
7	0	$\overline{G}$ Control (0 = asynchronous, 1 = synchronous)

4

EZREAD TAP INSTRUCTION AND SCAN PATH

The EZREAD TAP instruction is provided to allow the user to more easily and quickly read a large number of bytes from the device serially through the TDO port. EZREAD shortens the scan path for a serial read to just the 8 bit Data Out register (see Table 6).

To serially read the device the following would occur: initialization would be much like EZWRITE except that the Read Address Counter should be reladed with the count BEFORE the first one desired. So, if the first read needed to be address 0000 (and the counter is counting up), the Read Reload Register would have to be preloaded with FFFF using the LDRREG instruction. Again, SAMPLE/PRELOAD and INTEST instructions would need to be run to perform a reload cycle followed by another Boundary–scan that set RE and $\overline{RR}$ high in anticipation of the EZREAD instruction. Also, WE should be set low to prevent any unintended writes while reading. After this initializing, the EZREAD instruction would be loaded into the TAP instruction register in the Shift–IR state. The TAP controller would move to the Run–Test/Idle state where one cycle of TCK would increment the counter, read the 8 bits from that address, and load them into the Data Output register. The TAP controller would then move to the Shift–DR state and the EZREAD scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data Out register (see Table 6). In the Shift–DR state the Data Out register would be serially scanned out of the TDO port. This sequence through the TAP state machine would then be repeated until all desired bytes were read. EZREAD keeps the Q0 – Q7 pins active (if $\overline{G}$ is preloaded low) to allow parallel reading of the data out if desired.

EZREADZ TAP INSTRUCTION AND SCAN PATH

The EZREADZ TAP instruction behaves exactly like the EZREAD instruction except that the all outputs are held in a High–Z mode once the instruction is loaded.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the IEEE 1149.1 Test Access Port. To circuit disable the TAP controller without interfering with normal operation of the device TCK must be tied to V_{SS} to preclude midlevel inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response identical to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1 k resistor. TDO should remain unconnected.

With the four Test Access Port pins disabled, the device can only be used in its default power–up state. At power up, the device is configured to count up starting at address 0, the reload pins ($\overline{RR}$ and $\overline{WR}$) will clear the counters, the Expand ID bits are set to 000, and the Output Enable pin ($\overline{G}$) is configured as an asynchronous input.

Table 4. RDCOUNT Scan Register Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RAC0	Input
1	RAC1	Input
2	RAC2	Input
3	RAC3	Input
4	RAC4	Input
5	RAC5	Input
6	RAC6	Input
7	RAC7	Input
8	RAC8	Input
9	RAC9	Input
10	RAC10	Input
11	RAC11	Input
12	RAC12	Input
13	RAC13#	Input
14	RAC14#	Input
15	RAC15#	Input
16	WAC0	Input
17	WAC1	Input
18	WAC2	Input
19	WAC3	Input
20	WAC4	Input
21	WAC5	Input
22	WAC6	Input
23	WAC7	Input
24	WAC8	Input
25	WAC9	Input
26	WAC10	Input
27	WAC11	Input
28	WAC12	Input
29	WAC13#	Input
30	WAC14#	Input
31	WAC15#	Input

* RAC = Read Address Counter
WAC = Write Address Counter

\# These register bits are compared to the three Expand ID bits in the Control Register. (EX0 – 2). Only when there is a match is the read or write allowed to occur.

NOTE: Bit 0 closest to TDO.

Table 5. EZWRITE Scan Path Bit Definitions

Bit Number	Pin Name	Pin Type
0	D7	Input
1	D6	Input
2	D5	Input
3	D4	Input
4	D3	Input
5	D2	Input
6	D1	Input
7	D0	Input

Table 6. EZREAD and EZREADZ Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	Q0	Output
1	Q1	Output
2	Q2	Output
3	Q3	Output
4	Q4	Output
5	Q5	Output
6	Q6	Output
7	Q7	Output

Table 7. LDRREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit

* RRR = Read Reload Register

Table 8. LDBREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit
16	WRR0	Register bit
17	WRR1	Register bit
18	WRR2	Register bit
19	WRR3	Register bit
20	WRR4	Register bit
21	WRR5	Register bit
22	WRR6	Register bit
23	WRR7	Register bit
24	WRR8	Register bit
25	WRR9	Register bit
26	WRR10	Register bit
27	WRR11	Register bit
28	WRR12	Register bit
29	WRR13	Register bit
30	WRR14	Register bit
31	WRR15	Register bit

* RRR = Read Reload Register
WRR = Write Reload Register
NOTE: Bit 0 closest to TDO.

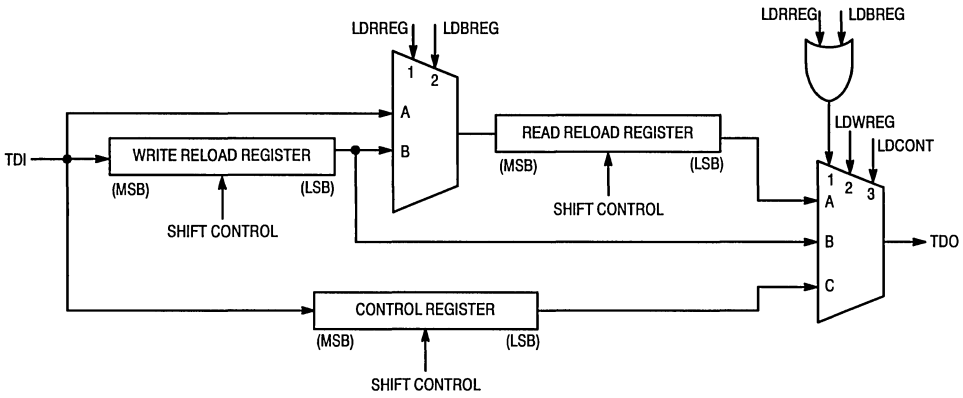
Table 9. LDWREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	WRR0	Register bit
1	WRR1	Register bit
2	WRR2	Register bit
3	WRR3	Register bit
4	WRR4	Register bit
5	WRR5	Register bit
6	WRR6	Register bit
7	WRR7	Register bit
8	WRR8	Register bit
9	WRR9	Register bit
10	WRR10	Register bit
11	WRR11	Register bit
12	WRR12	Register bit
13	WRR13	Register bit
14	WRR14	Register bit
15	WRR15	Register bit

* WRR = Write Reload Register

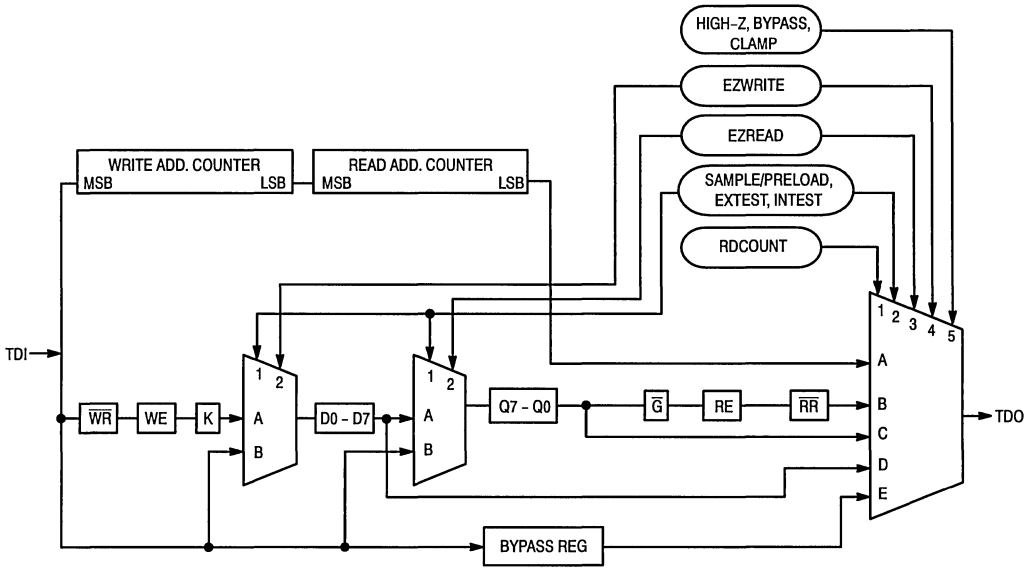
Table 10. LDCONT Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	EX0	Register bit
1	EX1	Register bit
2	EX2	Register bit
3	WCC	Register bit
4	UDW	Register bit
5	RCC	Register bit
6	UDR	Register bit
7	G CONT	Register bit



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 3. Register Load Paths



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFTSIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 4. Boundary Scan Paths

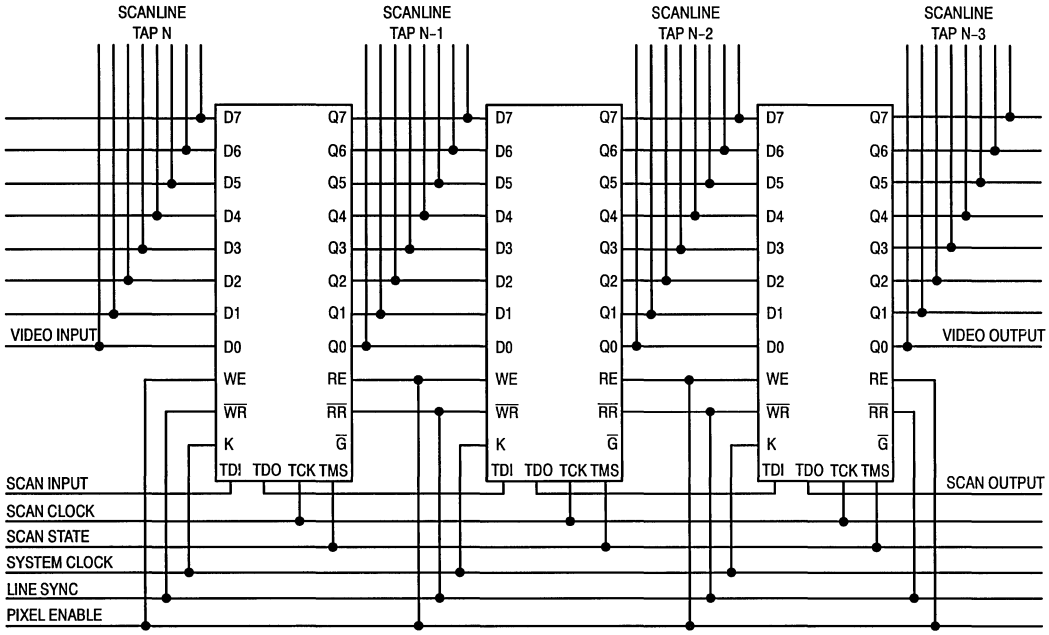


Figure 5. Multi–Stage 8–Bit Video Scanline Delay (8192 Pixels Maximum)

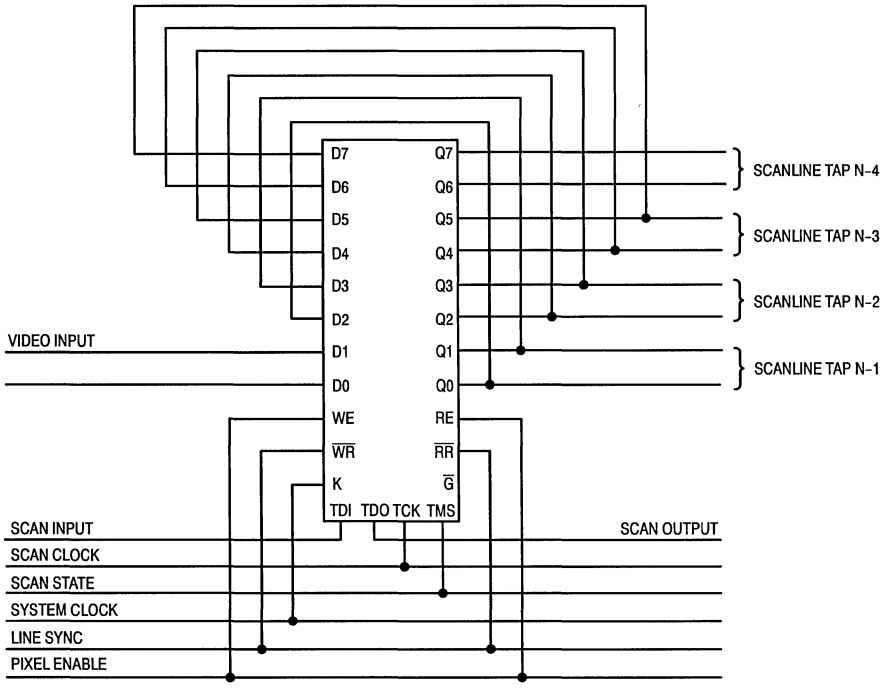


Figure 6. Multi–Stage 2–Bit Video Scanline Delay (8192 Pixels Maximum)

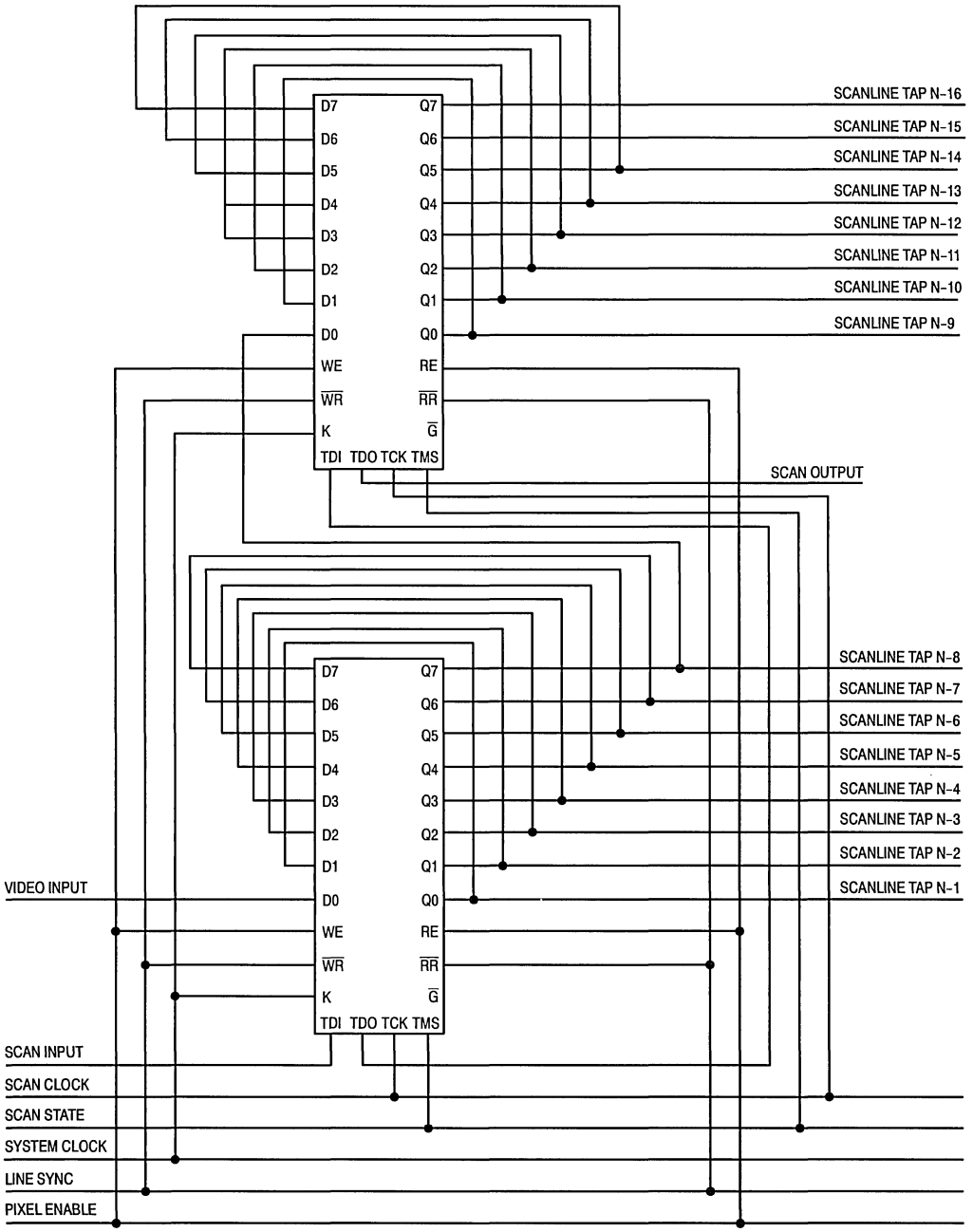


Figure 7. Multi–Stage 1–Bit Video Scanline Delay (8192 Pixels Maximum)

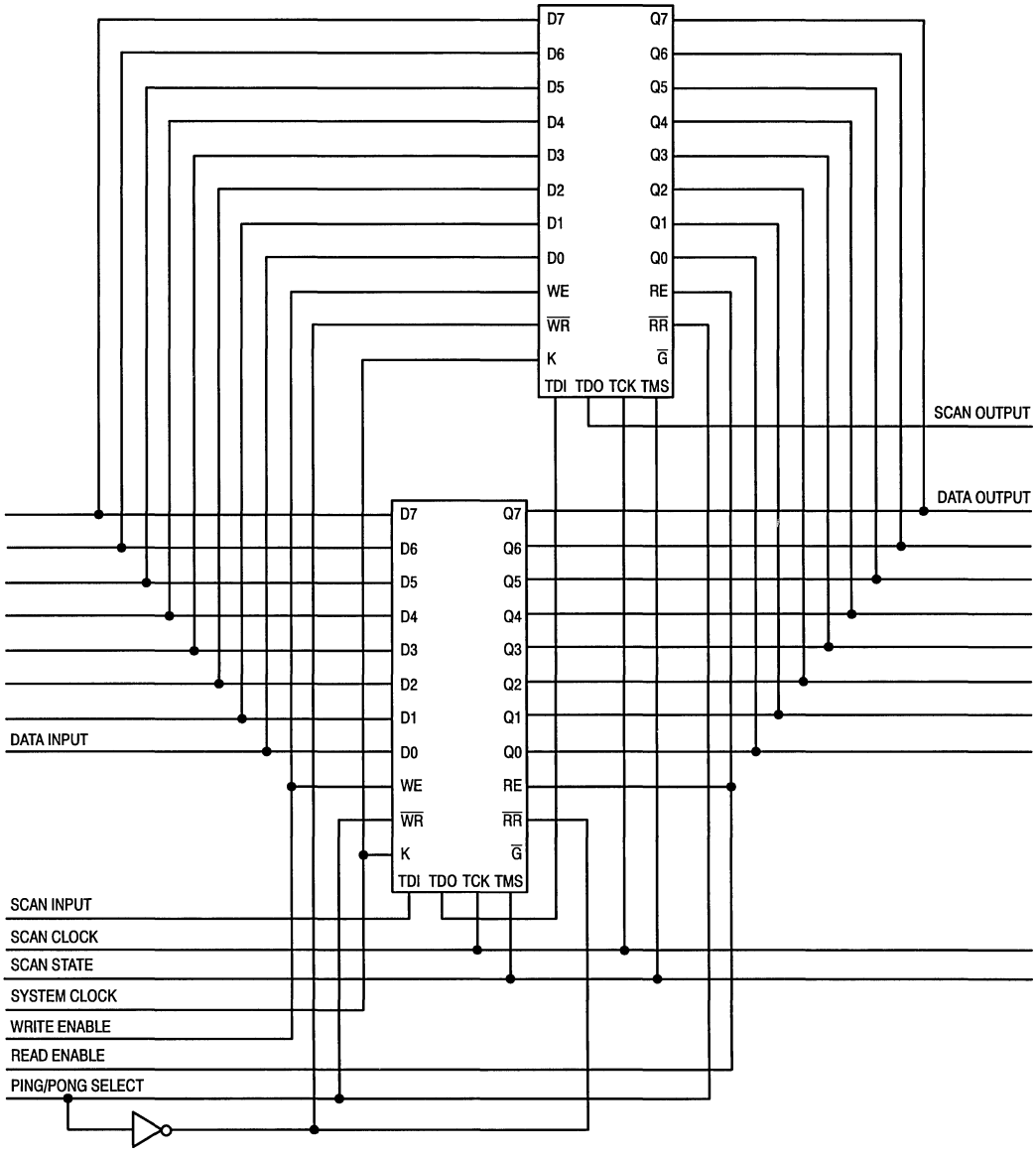


Figure 8. "Ping–Pong" Synchronizing Buffer (8192 Pixels Maximum)

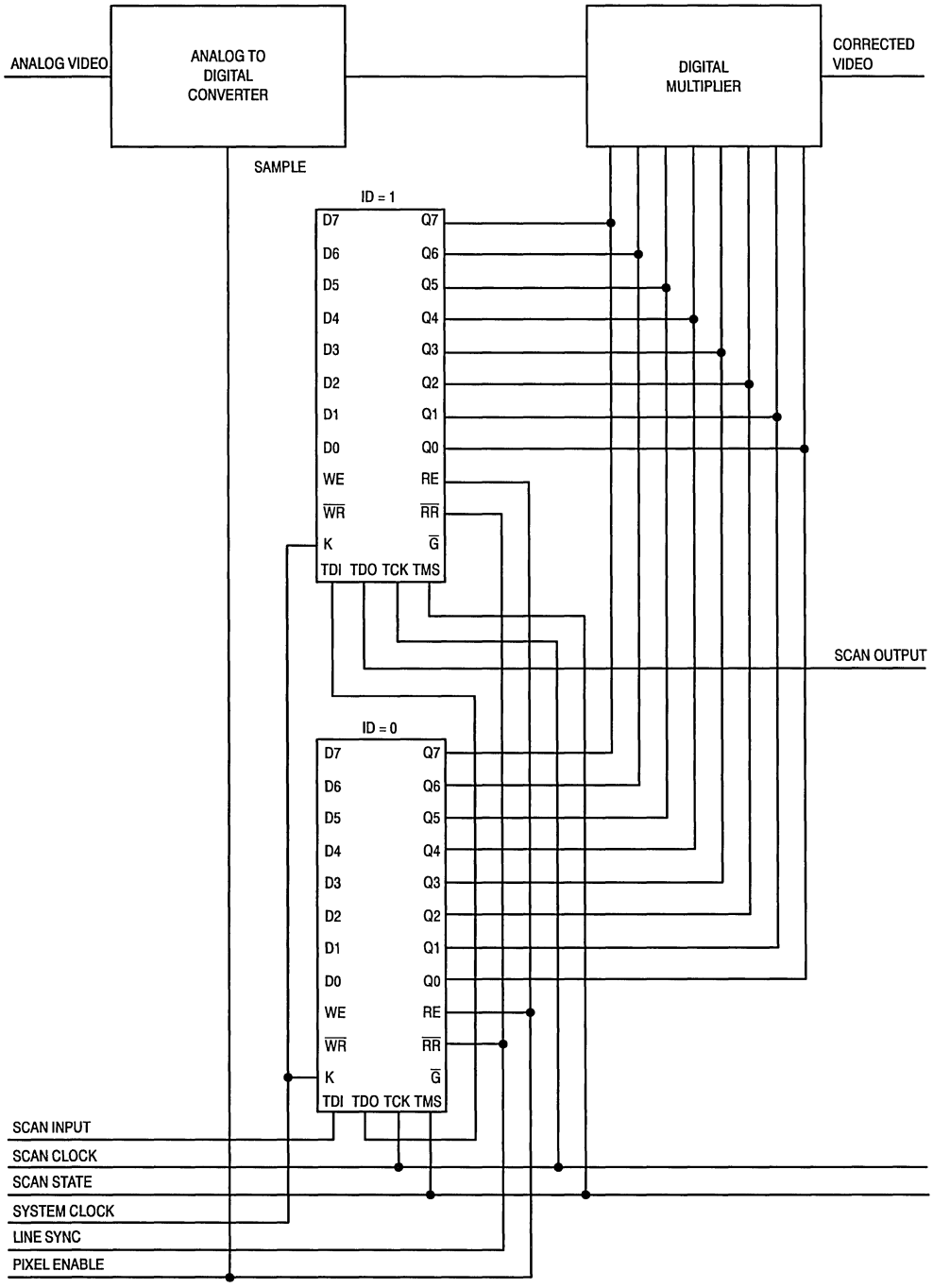


Figure 9. CCD Gain Correction, Buffer Written From Scan Input (16384 Pixels Maximum)

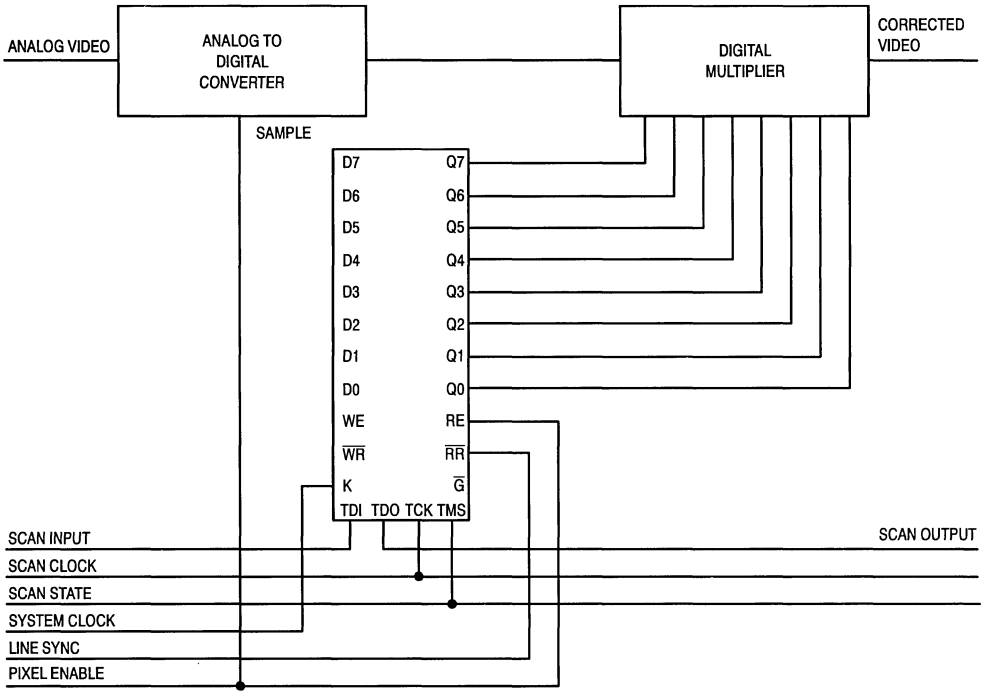


Figure 10. CCD Gain Correction, Buffer Written From Scan Input (8192 Pixels Maximum)

ORDERING INFORMATION

(Order by Full Part Number)

MCM 62X308 J XX

Motorola Memory Prefix — MCM

Part Number — 62X308

Package (J = SOJ) — J

Speed (15–5 = 15 ns, 17 = 17 ns) — XX

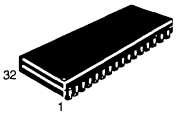
Full Part Numbers — MCM62X308J15–5 MCM62X308J17

Advance Information

MCM62Y308

Synchronous Line Buffer: 8K x 8 Bit Fast Static Dual Ported Memory

With IEEE Standard 1149.1 Test Access Port and Boundary–Scan (JTAG)



J PACKAGE
300 MIL SOJ
CASE 857–02

The MCM62Y308 is a synchronous, dual ported memory organized as 8,192 words of 8 bits each, fabricated using Motorola's double–metal, double–poly, 0.65 μm CMOS process. It is intended for high speed video or other applications which process data on a line–by–line basis. Through the use of a single clock and port control inputs, separate read and write data ports provide simultaneous access to a common memory array. Simultaneous read/write access to the same address location is also allowed, with old data being read followed by a write of the new data. This allows multiple devices to be cascaded with the output of one directly driving the input of another. In this configuration the data stream can be tapped at strategic interconnect points to perform various digital filtering functions.

Since there are no external address inputs, separate internal read and write address counters are provided as a means of indexing the memory array. These counters are preloaded and then selectively incremented or decremented by asserting read enable (RE) and write enable (WE) inputs, allowing cycle to cycle control. The address counters can be reloaded back to their initial values through the use of the read reload ($\overline{RR}$) and write reload ($\overline{WR}$) control inputs. These inputs initiate the transfer of address reload register values into the address counters which index the memory array. When an address counter reaches 0000 it will roll over on the next count. On the down count the roll over condition will cause the roll–over flag (WRF or RRF) to assert high. On the up count these flags must be treated as don't cares. The roll–over flag outputs are cleared when their associated roll–over reset pin is asserted low. The TDI input is used to write the reload registers using special test access port instructions.

The read and write address counters are 16 bits long, and only 13 of the 16 bits are required to index the 8K deep memory array. The remaining three bits are used for depth expansion. These three bits are compared to the lower three bits in the control register, and as long as they are equal that port (i.e., read or write) will remain active. If the bits do not compare, the port will become inactive (i.e., for read outputs, high–z; for write inputs, disabled) however, the counter will continue to count on the rising edge of K as long as the port enable signal (RE or WE) is asserted. The TDI input is used to write the control register using special test access port instructions.

The output enable Input can be programmed to be either synchronous or asynchronous through the control register.

The MCM62Y308 is available in a 32 pin SOJ package.

- 8K x 8 Fast Access Static Memory Array
- Single 5 V Power Supply — MCM62Y308–17: ± 5%
- Synchronous, Simultaneous Read/Write Memory Access
- 50 MHz Maximum Clock Cycle Time, < 15 ns Read Access
- Single Clock Operation
- Separate Read/Write Address Counters with Reload Control
- Separate Up/Down Counter Control for Both Read and Write
- Separate Roll–Over Flag Outputs for Read and Write
- Programmable Output Enable Control (Synchronous or Asynchronous)
- Cascadable I/O Interface
- IEEE Standard 1149.1 Test Port (JTAG)
- Expand ID Register for Depth Expansion
- High Board Density SOJ Package

PIN ASSIGNMENT

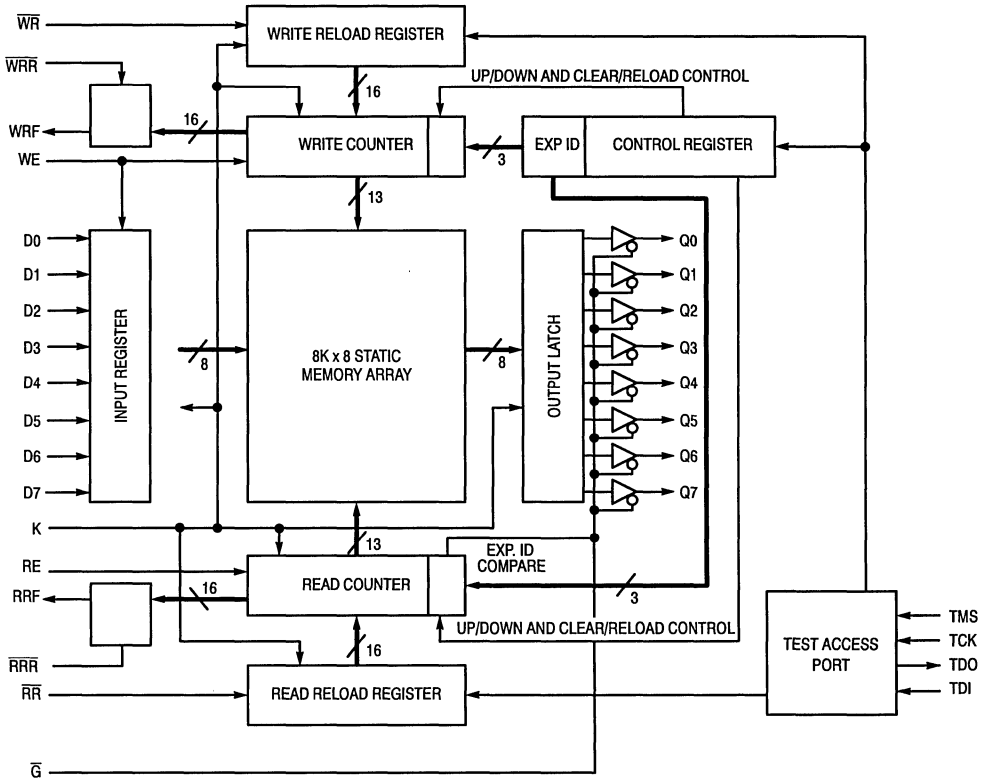
$\overline{WRR}$	1	32	WRF
D7	2	31	Q7
D6	3	30	Q6
D5	4	29	Q5
D4	5	28	Q4
D3	6	27	Q3
D2	7	26	Q2
D1	8	25	Q1
D0	9	24	Q0
V_{DD}	10	23	V_{SS}
K	11	22	$\overline{G}$
WE	12	21	RE
$\overline{WR}$	13	20	$\overline{RR}$
TDI	14	19	TDO
TCK	15	18	TMS
$\overline{RRR}$	16	17	RRF

PIN NAMES

K	Clock Input
WE	Write Enable Input
$\overline{WR}$	Write Address Reload Input
RE	Read Enable Input
$\overline{RR}$	Read Address Reload Input
RRF	Read Roll–Over Flag Output
WRF	Write Roll–Over Flag Output
$\overline{RRR}$	Read Roll–Over Reset Input
$\overline{WRR}$	Write Roll–Over Reset Input
$\overline{G}$	Output Enable Input
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{DD}	+ 5 V Power Supply
V_{SS}	Ground

REV 2
5/95

BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

WE	$\overline{WR}$	RE	$\overline{RR}$	$\overline{G}$	Match EXP ID (Read/Write)	Mode (Read/Write)	Supply Current	Q0 – 7 Status
X	L	X	L	L	Match Read/Match Write	Reload, Read/Reload, Write Disable	I_{CC}	Data Out
H	H	H	H	L	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	Data Out
L	H	L	H	L	Match Read/Match Write	Read Count Disable/Write Disable	I_{CC}	Data Out
H	H	H	H	H	Match Read/Match Write	Count, Read/Write, Count	I_{CC}	High–Z
H	H	H	H	X	No Match Read/No Match Write	Count, No Read/No Write, Count	I_{SB}	High–Z
H	H	H	H	X	No Match Read/Match Write	Count, No Read/Write, Count	I_{SB}	High–Z
H	H	H	H	L	Match Read/No Match Write	Count, Read/No Write, Count	I_{CC}	Data Out

PIN DESCRIPTIONS

SOJ Pin Locations	Symbol	Type	Description
11	K	Input	**CLOCK** – System clock input pin accepting a minimum 8 ns clock high or clock low pulse at a minimum 20 ns clock cycle. All other synchronous inputs excluding the test access port are captured on the rising edge of this signal.
12	WE	Input	**WRITE ENABLE** – Write enable is captured on K leading edge. When asserted this causes the input data D0 – D7 to be written into the RAM address controlled by the write address counter and increments the counter for the next write.
21	RE	Input	**READ ENABLE** – Read enable is captured on K leading edge. When asserted increments the counter for the next read operation. This causes a RAM read access from address controlled by the read address counter to be inserted in the output register Q0 – Q7.
13	$\overline{WR}$	Input	**WRITE RELOAD** – Write reload is captured on K leading edge. When asserted this causes the write address counter to be initialized to the contents of the write reload register or "cleared" as specified by control register bit 3. See control register bit 3 for "cleared" description.
20	$\overline{RR}$	Input	**READ RELOAD** – Read reload is captured on K leading edge. When asserted this causes the read address counter to be initialized to the contents of the read reload register or "cleared" as specified by control register bit 5. See control register bit 5 for "cleared" description.
22	G	Input	**OUTPUT ENABLE** – When asserted low causes the outputs Q0 – Q7 to become active and when deasserted high causes them to High–Z. This pin can be either synchronous with K leading edge or asynchronous as specified by control register bit 7.
9, 8, 7, 6, 5, 4, 3, 2	D0 – D7	Input	**DATA INPUT** – The levels on these pins are captured on the K leading edge. The value captured will be written into the RAM if WE is also asserted and the expand ID bits match the upper three bits of the write address counter.
24, 25, 26, 27, 28, 29, 30, 31	Q0 – Q7	Output	**DATA OUTPUT** – Data outputs are available from the read output register < 15 ns from the rising edge of K when RE or $\overline{RR}$ is asserted. outputs are disabled when the upper three bits of the read address counter do not match the three expand ID bits of the control register. $\overline{G}$ will also control the disabling of the outputs either synchronously or asynchronously. See $\overline{G}$ description.
17, 32	RRF, WRF	Output	**ROLL–OVER FLAG** – These signals are asserted high on the clock cycle where the address counters (write address counter for WRF and read address counter for RRF) roll–over to 0000 during count down. During count up these pins must be treated as don't cares.
16, 1	$\overline{RRR}$, $\overline{WRR}$	Input	**ROLL–OVER RESET** – The level on these pins is captured on the K leading edge. When asserted low, each will reset their associated roll–over flag output.

TEST ACCESS PORT PIN DESCRIPTIONS (The Test Access Port Conforms with the IEEE Standard 1149.1. It is also Used to Load Device Specific Registers Used to Configure the MCM62Y308.)

SOJ Pin Locations	Symbol	Type	Description
15	TCK	Input	**TEST CLOCK** – Samples and clocks all TAP events. All inputs are captured on TCK rising edge and all outputs propagate from TCK falling edge. It also can take the place of K in device operation in certain test conditions.
18	TMS	Input	**TEST MODE SELECT** – Sampled on the rising edge of TCK. Determines the movement through the TAP state machine (Figure 2). This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
14	TDI	Input	**TEST DATA IN** – Sampled on the rising edge of TCK. This is the input side of the serial register placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP state machine and what instruction is active in the TAP instruction register. This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.
19	TDO	Output	**TEST DATA OUT** – Output that is active depending on the state of the TAP state machine. Output changes off the trailing edge of TCK. This is the output side of the serial register placed between TDI and TDO.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITICS

(T_A = 0 to 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	MCM62Y308–17	V_{DD}	4.75	5.0	5.25	V
Input High Voltage		V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time = 20 ns)	I_{CCA}	—	150	mA
AC Standby Current (When Expand ID Bits Do Not Match the Read Address Counter, Cycle Time = 20 ns)	I_{SB}	—	100	mA
Output Low Voltage (I_{OL} = + 4.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance (Q0 – Q7, TDO, WRF, RRF)	C_{out}	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... Terminated 50 Ohm Transmission Line

READ/WRITE CYCLE TIMING

Parameter		Symbol	MCM62Y308–17 Min	MCM62Y308–17 Max	Unit	Notes
Cycle Time		t_{KHKH}	22	—	ns	
Clock High Time		t_{KHKL}	9	—	ns	
Clock Low Time		t_{KLKH}	9	—	ns	
Clock High to Output Valid		t_{KHQV}	5	17	ns	
Clock High to Roll–Over Flag Valid		t_{KHRFV}	5	11	ns	
Clock High to Output High–Z		t_{KHQZ}	5	15	ns	1
Output Enable Low to Output Valid		t_{GLQV}	3	10	ns	2, 4
Output Enable High to Output High–Z		t_{GHQZ}	0	5	ns	2, 3, 4
Setup Times:	RE	t_{REVKH}	2	—	ns	5
	WE	t_{WEVKH}				
	$\overline{WR}$	t_{WRVKH}				
	$\overline{RRR}$	t_{RRRVKH}				
	$\overline{WRR}$	t_{WRRVKH}				
	$\overline{G}$	t_{GVKH}				6
	$\overline{RR}$	t_{RRVKH}	3	—		5
	Data In	t_{DVKH}	1	—		
Hold Times:	RE	t_{KHREX}	2	—	ns	5
	WE	t_{KHWEX}				
	$\overline{RR}$	t_{KHRRX}				
	$\overline{WR}$	t_{KHWRX}				
	$\overline{RRR}$	t_{KHRRRX}				
	$\overline{WRR}$	t_{KHWRRX}				
	$\overline{G}$	t_{KHGX}				6
	Data In	t_{KHDX}				

NOTES:
1. The outputs High–Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
2. $\overline{G}$ is a don't care when the three ID expansion bits do not match the upper three bits of the Read Address Counter.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction.)
4. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQV} min for a given device and from device to device.
5. This is a synchronous device. All inputs must meet the specified setup and hold times for ***ALL*** rising edges of Clock except for $\overline{G}$ when it is programmed to be asynchronous.
6. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.

AC TEST LOADS

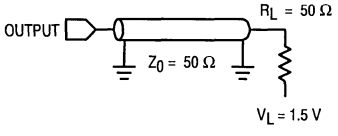


Figure 1A

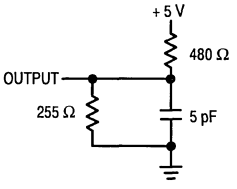
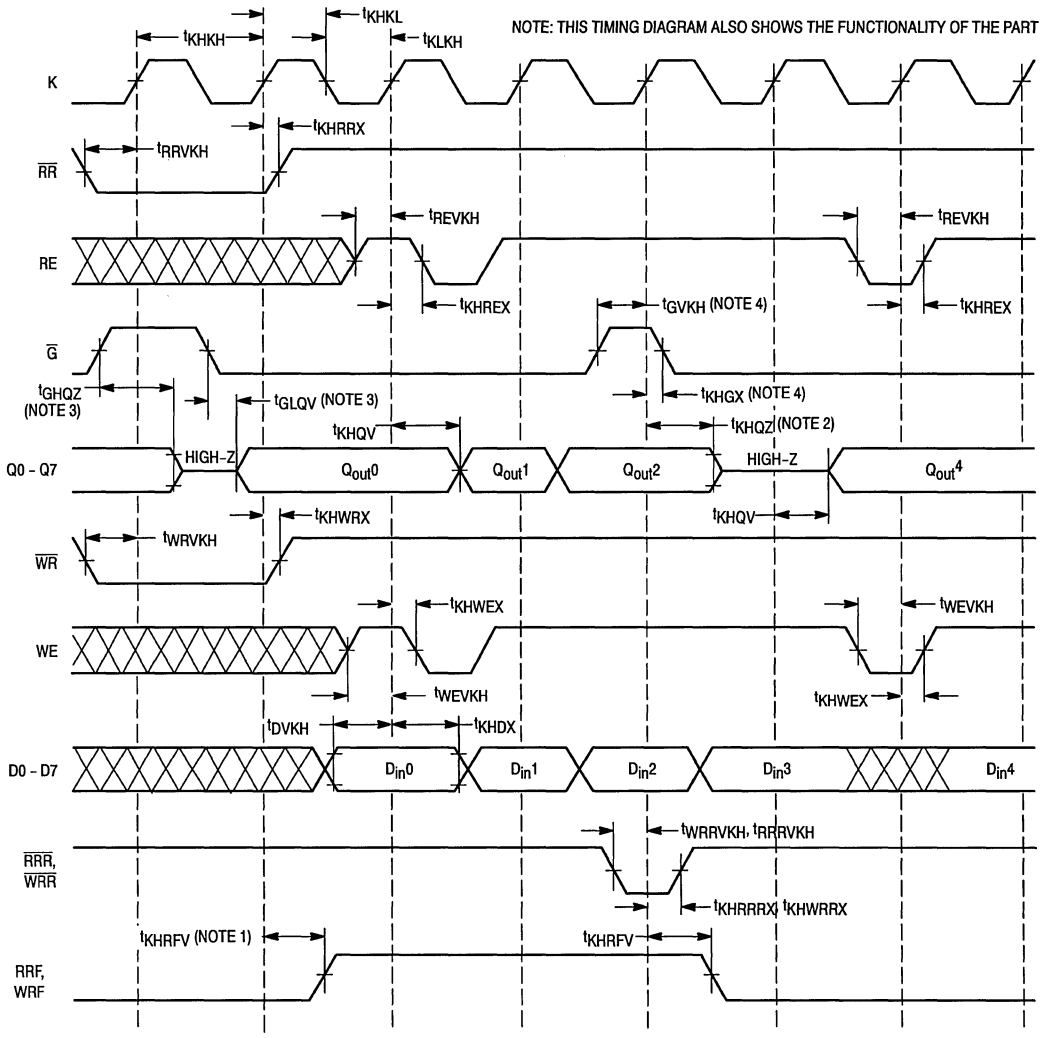


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ/WRITE CYCLE TIMING DIAGRAM



1. Roll–Over Outputs assert high when counters reach their initial value. This timing diagram shows the relationship between the roll–over output and reset pin only.
2. The outputs High–Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction.)
4. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.

AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

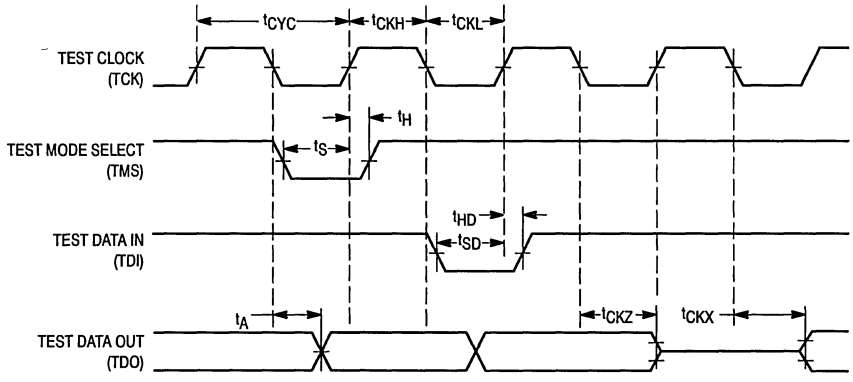
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... 50 Ohm Transmission Line

TAP CONTROLLER TIMING

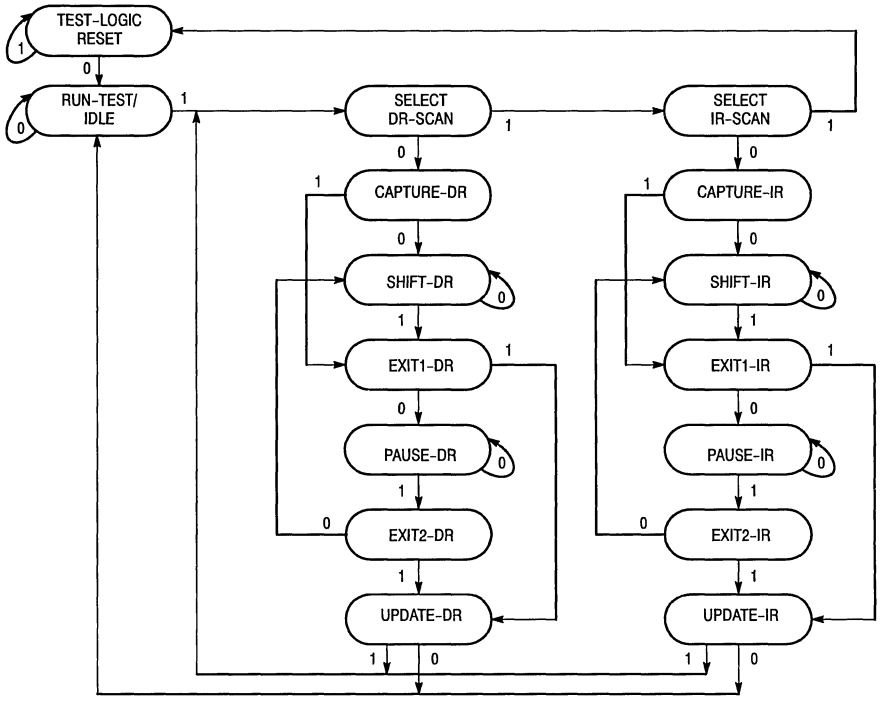
Parameter	Symbol	MCM62Y308–17		Unit	Notes
		Min	Max		
Cycle Time	t_{CYC}	30	—	ns	
Clock High Time	t_{CKH}	12	—	ns	
Clock Low Time	t_{CKL}	12	—	ns	
Clock Low to Output Valid	t_A	5	9	ns	
Clock Low to Output High–Z	t_{CKZ}	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	ns	2, 3
Setup Time, Test Mode Select	t_S	2	—	ns	
Setup Time, Test Data In	t_{SD}	2	—	ns	
Hold Time, Test Mode Select	t_H	2	—	ns	
Hold Time, Test Data In	t_{HD}	2	—	ns	

NOTES:
1. Test Data Out will High–Z from a clock low edge depending on the current state of the TAP state machine.
2. Test Data Out is active only in the SHIFT–IR and SHIFT–DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady–state voltage. This parameter is sampled and not 100% tested.

TAP CONTROLLER TIMING DIAGRAM



4



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 2. TAP Controller State Diagram

TEST ACCESS PORT DESCRIPTIONS

INSTRUCTION SET

A four pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. There are two classes of instructions; standard instructions as defined in the IEEE 1149.1 standard and device specific, or public, instructions that are used to control the functionality of the device. When the TAP (Test Access Port) controller is in the Shift–IR state the Instruction Register is placed between TDI and TDO, least significant bit closest to TDO. In this state the desired instruction would be serially loaded through the TDI input (while the previous instruction would be shifted out of TDO). The TAP instruction set for this device is listed in Table 1.

TAP STANDARD INSTRUCTION SET

NOTE: The descriptions in this section are not intended to be used without the supporting IEEE 1149.1–1993 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instuction is used to allow scanning of the boudary–scan register without causing interference to the normal operation of the chip logic. The 26 bit boundary scan register contains bits for all device signal and clock pins and associated control signals (Table 2). This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register. When the TAP controller is then moved to the Shift–DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. It would be used prior to the INTEST instruction to preload values into the input pins. As data is written into TDI, data also streams out of TDO which can be used to pre–sample the inputs and outputs. SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

Table 2 shows the boundary–scan bit definitions. The first column defines the bit's ordinal position in the boundary–scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted is 25. The second column is the pin name and the third column is the pin type.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins (i.e., Q0 – Q7, RRF, and WRF). The EXTEST instruction would then be loaded. During EXTEST the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run–Test/Idle state. In this state one cycle of TCK would cause the preloaded data on the ouput pins to be driven while the values on the input pins would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero; the value of the expand ID bits is ignored). Note that TCK, not the Clock pin, K, is used as the clock input while K is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). While in the Shift–DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run–Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary–scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will

Table 1. TAP Instruction Set

Instruction	Code (Binary)	Description
Standard Instructions:		
BYPASS	1111*	Bypass Instruction
INTEST	0111	Intest Instruction
SAMPLE/PRELOAD	1100	Sample and/or Preload Instruction
EXTEST	0000	Extest Instruction
HIGHZ	1010	High–Z all Output pins while bypass reg. is between TDI and TDO
CLAMP	1001	Clamp Output pins while bypass reg. is between TDI and TDO
Device Specific (Public) Instructions:		
LDRREG	0001	Load Read Address Reload Register
LDWREG	0100	Load Write Address Reload Register
LDBREG	0101	Load both Address Reload Registers (Write then Read)
LDCONT	0010	Load Control Register
RDCOUNT	1000	Read the values of the Read and Write Address Counters
EZWRITE	0011	Serial Write (using Write Address Counter)
EZREAD	0110	Serial Read (using Read Address Counter)
EZREADZ	1110	Serial Read, outputs High–Z

*Default state at power–up.

be sampled regardless of $\overline{G}$). Only one action will be performed in the Run–Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary–scan register is placed between TDI and TDO in the Shift–DR state of the TAP controller (Table 2). While in the Shift–DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run–Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary–scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will be sampled regardless of $\overline{G}$). Only one action will be performed in the Run–Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift–DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

Since device functionality can only be verified through sampling the outputs of the device, the most likely use of INTEST would be to first load up the boundary–scan register for a Write Reload and execute the reload in the Run–Test/Idle state. Then a write of the first address would be performed again using the boundary scan register to load up the input registers and executing the write in the Run–Test/Idle state. Lastly, a Read Reload would be executed in the same manner so that the data that had just been written in the first address would be read from the memory array and written into the output registers which would then be shifted out of TDO in the Shift–DR state. The values of the roll–over flags (RRF and WRF) would also be sampled and shifted out at the same time for comparison to expected values.

There are easier ways to serially read and write the memory array. See the EZREAD and EZWRITE TAP instruction explanation.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary–scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values to be driven on the output pins when the CLAMP instruction is active. Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero.

HIGH–Z TAP INSTRUCTION

The High–Z instruction is provided to allow all the outputs (except TDO) to be placed in an inactive drive state (High–Z), including the Read Roll–Over Flag and the Write Roll–Over Flag outputs. During the High–Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The Bypass instruction is the default instruction loaded in at power up. This instruction will place a single shift register between TDI and TDO during the Shift–DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Table 2. Boundary Scan Register Bit Definitions

Bit Number	Pin Name	Pin Type
0	RRF	Output
1	$\overline{RR}$	Input
2	RE	Input
3	$\overline{G}$	Input
4	Q0	Output
5	Q1	Output
6	Q2	Output
7	Q3	Output
8	Q4	Output
9	Q5	Output
10	Q6	Output
11	Q7	Output
12	WRF	Output
13	$\overline{WRR}$	Input
14	D7	Input
15	D6	Input
16	D5	Input
17	D4	Input
18	D3	Input
19	D2	Input
20	D1	Input
21	D0	Input
22	K	Input
23	WE	Input
24	$\overline{WR}$	Input
25	$\overline{RRR}$	Input

NOTE: K is a sample–only scan bit. It cannot be pre–loaded for control purposes.

DEVICE SPECIFIC (PUBLIC) INSTRUCTIONS

LDCONT TAP INSTRUCTION

The Control Register is an eight bit register that contains the control bits for the Address Registers and Counters and the Output Enable pin. When the LDCONT TAP instruction is loaded into the Instruction Register, the Control Register is placed between TDI and TDO when the TAP controller is in the Shift–DR state (see Figure 2 and Table 10). The power–up/preload state and function of the Control bits are found in Table 3.

The Expand ID bits provide system depth expansion. These three bits are compared to the upper three bits in the address counters. As long as the three Expand–ID bits match the three upper bits in the address counters the port will stay active. If they do not match, the port will deactivate (i.e., outputs will High–Z or write will be disabled); however, the counters will continue counting as long as RE and WE remain asserted (i.e., high) at the rising edge of Clock.

The Reload Control bits (3 and 5) are used to control either reloading the Read and Write Address Counters from the Reload Registers or clearing the counter when $\overline{RR}$ or $\overline{WR}$ is asserted. If these bits are set low the counters they control will be cleared to all zeroes if the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted and any value in the Reload Register is ignored. This means that if the initial address value desired is address 0000 (or FFFF when counting down) then there is no need to load the Address Reload Registers using the LDRREG, LDWREG, or the LDBREG instructions in the following description. If these bits are set high the counters are loaded up with the values in the Reload Registers when the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted.

The Up/Down count bits (4 and 6) determine the direction in which the respective Address Counter will count; if the bit is set low the counter will count up and if set high the counter will count down. If the counters are set to count down and the Reload control is set to the clear counter mode, then the initial value in the counters will be FFFF. To ensure that the counter will function properly, a reload (using $\overline{RR}$ or $\overline{WR}$) is required after the count direction is switched.

The Output Enable control bit (7) determines the functionality of the Output Enable pin, $\overline{G}$. When the bit is low, $\overline{G}$ functions asynchronously. When set high, $\overline{G}$ functions synchronously and must meet the specified setup and hold times to the Clock K.

The Control Register will also be preloaded. When the instruction 0010 (LDCONT) is in the Instruction Register and the controller is in the Capture–DR state the above preload values (all zeroes) will be loaded into the Control Register. All zeroes will also be loaded in the Control Register at power–up.

While new values are shifted in from TDI in the Shift–DR state, all zeroes will be output on TDO for the first eight bits.

LDRREG, LDWREG, AND LDBREG TAP INSTRUCTIONS

There are three instructions that may be used to load the 16 bit address reload registers: LDRREG (Load Read Address Reload Register), LDWREG (Load Write Address Reload Register), and LDBREG (Load both Address Reload Registers, Write followed by Read). Figure 2 illustrates how the Reload registers are placed between TDI and TDO. Tables 7, 8, and 9 describe each register. These instructions would be used only if the user needed to load the Reload Registers with a non–zero value. If the Address Counters are to always be reset to zeroes (or all 1s if counting down) then only the Control Register need be loaded to affect a reset of the counters.

The TAP controller has been set up to make it easier for the user to serially load the Reload Registers. When the TAP controller is clocked into the Capture–IR state (see state diagram) the instruction for loading both registers (0101) will be preloaded into the shift register. This allows the user to go directly to the Update–IR instead of having to serially shift this instruction in through the TDI port. Once the load instruction has been entered the user can then clock over to the Capture–DR state where the value for the reload register(s) is serially loaded (see Figure 2).

RDCOUNT TAP INSTRUCTION

The RDCOUNT scan register is accessible after the RDCOUNT instruction is loaded into the TAP instruction register in the Shift–IR state and the TAP controller is then moved to the Shift–DR state. This scan register can then be used to shift out the values of the Read and Write Address Counters The RDCOUNT scan–register is a sample only register and can not be used to load values into the counters. See Table 4.

EZWRITE TAP INSTRUCTION AND SCAN PATH

The EZWRITE TAP instruction is provided to allow the user to more easily and quickly write a large number of bytes to the device serially through the TDI port. EZWRITE shortens the scan path for a serial write to just the 8 bit Data in register (see Table 5).

The most likely use of this instruction is as follows: the user would first load the Control Register using the LDCONT instruction. This would initialize the Expand ID bits and the Write Counter. The Write Reload Register will need to be

Table 3. Control Register Bit Description

Bit No.	Power Up and Preload State	Function
0 – 2	000	Expand ID bits for comparison with the upper 3 bits of the Read and Write Address counters
3	0	Reload Control of Write Address Counter (0 = clear counter, 1 = reload)
4	0	Up/Down count bit for Write Address Counter (0 = count up, 1 = count down)
5	0	Reload Control of Read Address Counter (0 = clear counter, 1 = reload)
6	0	Up/Down count bit for Read Address Counter (0 = count up, 1 = count down)
7	0	$\overline{G}$ Control (0 = asynchronous, 1 = synchronous)

loaded using the LDWREG instruction if a non–zero starting address is desired. If 0000 was the first desired count, setting up the Control Register to "clear" the Write counter is all that is required (Bit 3 set to zero). A reload cycle using SAMPLE/PRELOAD ($\overline{WR}$ preloaded low) and INTEST would also have to be run in order to initialize the counter. While still in the INTEST instruction at the Shift–DR state, the proper values of WE and $\overline{WR}$ would then need to be preloaded for proper operation of EZWRITE (WE high and $\overline{WR}$ high). After all this initializing is done, the EZWRITE instruction would be loaded into the TAP instruction register in the Shift–IR state. When the TAP controller is then moved to the Shift–DR state the EZWRITE scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data In register (see Table 5). The 8 bits to be written into the first address would be scanned in (sampled values from the Data In pins would be streaming out of TDO at the same time), then the TAP controller would be moved to the Run–Test/Idle state where one cycle of TCK would write the 8 bits into the address and increment the counter. The TAP controller would then move back to the Shift–DR state so that the next byte to be written can be serially loaded and the process would be repeated until all desired bytes were written. During EZWRITE the Q0 – Q7 pins will be in a High–Z state.

4

EZREAD TAP INSTRUCTION AND SCAN PATH

The EZREAD TAP instruction is provided to allow the user to more easily and quickly read a large number of bytes from the device serially through the TDO port. EZREAD shortens the scan path for a serial read to just the 8 bit Data Out register (see Table 6).

To serially read the device the following would occur: initialization would be much like EZWRITE except that the Read Address Counter should be reladed with the count BEFORE the first one desired. So, if the first read needed to be address 0000 (and the counter is counting up), the Read Reload Register would have to be preloaded with FFFF using the LDRREG instruction. Again, SAMPLE/PRELOAD and INTEST instructions would need to be run to perform a reload cycle followed by another Boundary–scan that set RE and $\overline{RR}$ high in anticipation of the EZREAD instruction. Also, WE should be set low to prevent any unintended writes while reading. After this initializing, the EZREAD instruction would be loaded into the TAP instruction register in the Shift–IR state. The TAP controller would move to the Run–Test/Idle state where one cycle of TCK would increment the counter, read the 8 bits from that address, and load them into the Data Output register. The TAP controller would then move to the Shift–DR state and the EZREAD scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data Out register (see Table 6). In the Shift–DR state the Data Out register would be serially scanned out of the TDO port. This sequence through the TAP state machine would then be repeated until all desired bytes were read. EZREAD keeps the Q0 – Q7 pins active (if $\overline{G}$ is preloaded low) to allow parallel reading of the data out if desired.

EZREADZ TAP INSTRUCTION AND SCAN PATH

The EZREADZ TAP instruction behaves exactly like the EZREAD instruction except that the all outputs are held in a High–Z mode once the instruction is loaded.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the IEEE 1149.1 Test Access Port. To circuit disable the TAP controller without interfering with normal operation of the device TCK must be tied to V_{SS} to preclude midlevel inputs. Although TDI and TMS are designed in such a way that an undriven input will produce a response identical to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1 k resistor. TDO should remain unconnected.

With the four Test Access Port pins disabled, the device can only be used in its default power–up state. At power up, the device is configured to count up starting at address 0, the reload pins ($\overline{RR}$ and $\overline{WR}$) will clear the counters, the Expand ID bits are set to 000, and the Output Enable pin ($\overline{G}$) is configured as an asynchronous input.

Table 4. RDCOUNT Scan Register Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RAC0	Input
1	RAC1	Input
2	RAC2	Input
3	RAC3	Input
4	RAC4	Input
5	RAC5	Input
6	RAC6	Input
7	RAC7	Input
8	RAC8	Input
9	RAC9	Input
10	RAC10	Input
11	RAC11	Input
12	RAC12	Input
13	RAC13#	Input
14	RAC14#	Input
15	RAC15#	Input
16	WAC0	Input
17	WAC1	Input
18	WAC2	Input
19	WAC3	Input
20	WAC4	Input
21	WAC5	Input
22	WAC6	Input
23	WAC7	Input
24	WAC8	Input
25	WAC9	Input
26	WAC10	Input
27	WAC11	Input
28	WAC12	Input
29	WAC13#	Input
30	WAC14#	Input
31	WAC15#	Input

* RAC = Read Address Counter
WAC = Write Address Counter
\# These register bits are compared to the three Expand ID bits in the Control Register. (EX0 – 2). Only when there is a match is the read or write allowed to occur.
NOTE: Bit 0 closest to TDO.

Table 5. EZWRITE Scan Path Bit Definitions

Bit Number	Pin Name	Pin Type
0	D7	Input
1	D6	Input
2	D5	Input
3	D4	Input
4	D3	Input
5	D2	Input
6	D1	Input
7	D0	Input

Table 6. EZREAD and EZREADZ Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	Q0	Output
1	Q1	Output
2	Q2	Output
3	Q3	Output
4	Q4	Output
5	Q5	Output
6	Q6	Output
7	Q7	Output

Table 7. LDRREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit

* RRR = Read Reload Register

Table 8. LDBREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit
16	WRR0	Register bit
17	WRR1	Register bit
18	WRR2	Register bit
19	WRR3	Register bit
20	WRR4	Register bit
21	WRR5	Register bit
22	WRR6	Register bit
23	WRR7	Register bit
24	WRR8	Register bit
25	WRR9	Register bit
26	WRR10	Register bit
27	WRR11	Register bit
28	WRR12	Register bit
29	WRR13	Register bit
30	WRR14	Register bit
31	WRR15	Register bit

* RRR = Read Reload Register
WRR = Write Reload Register
NOTE: Bit number zero is closest to TDO.

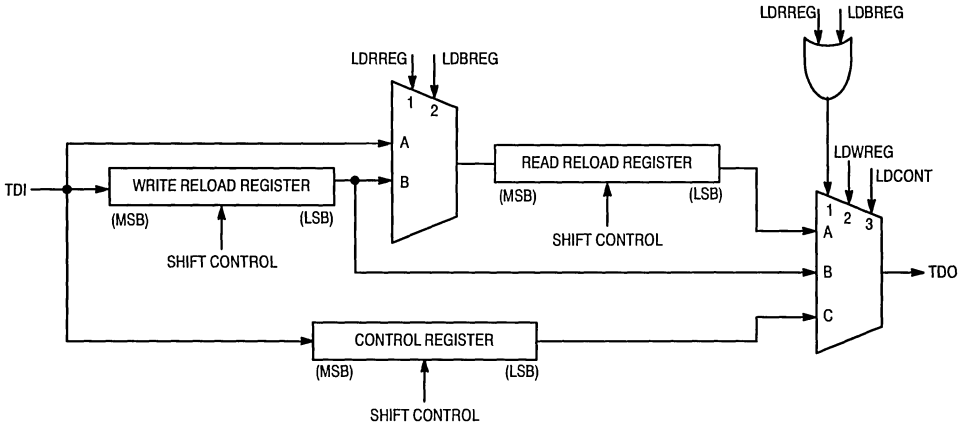
Table 9. LDWREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	WRR0	Register bit
1	WRR1	Register bit
2	WRR2	Register bit
3	WRR3	Register bit
4	WRR4	Register bit
5	WRR5	Register bit
6	WRR6	Register bit
7	WRR7	Register bit
8	WRR8	Register bit
9	WRR9	Register bit
10	WRR10	Register bit
11	WRR11	Register bit
12	WRR12	Register bit
13	WRR13	Register bit
14	WRR14	Register bit
15	WRR15	Register bit

* WRR = Write Reload Register

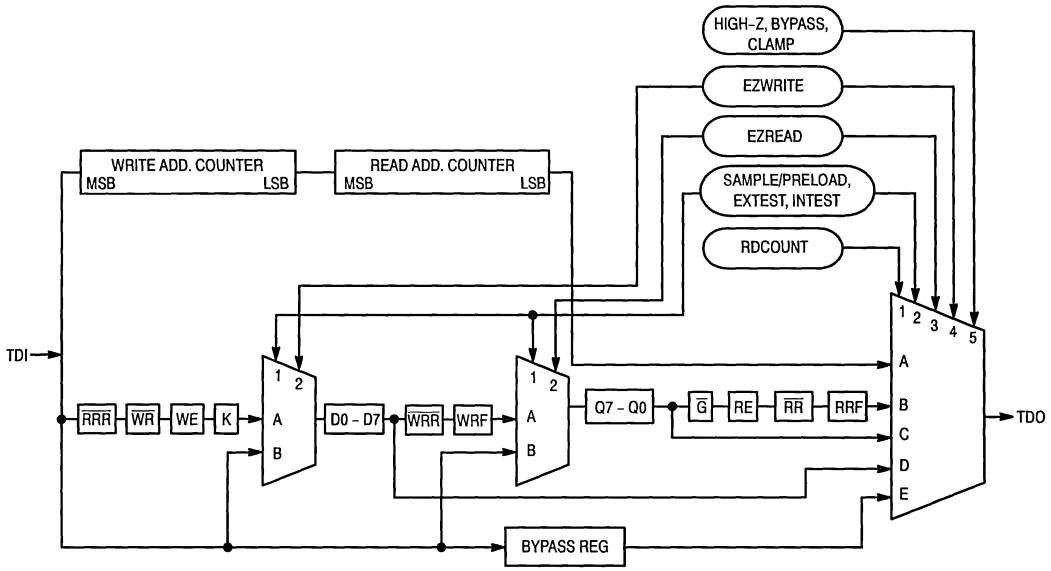
Table 10. LDCONT Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	EX0	Register bit
1	EX1	Register bit
2	EX2	Register bit
3	WCC	Register bit
4	UDW	Register bit
5	RCC	Register bit
6	UDR	Register bit
7	G CONT	Register bit



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

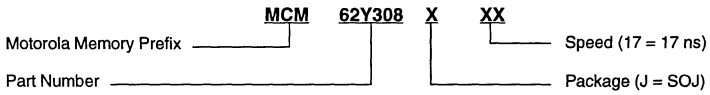
Figure 3. Register Load Paths



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 4. Boundary Scan Paths

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM62Y308J17

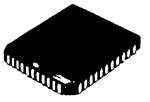
4

MCM62963A

Product Preview

4K x 10 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62963A is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit. This allows reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D9), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

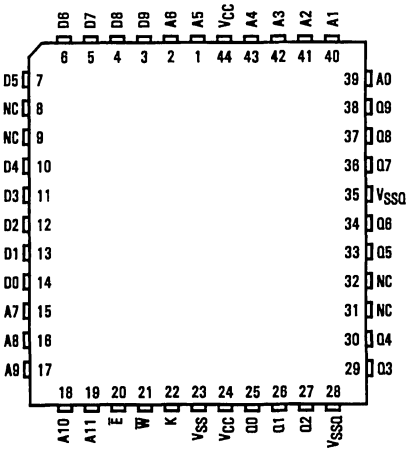
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62963A provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

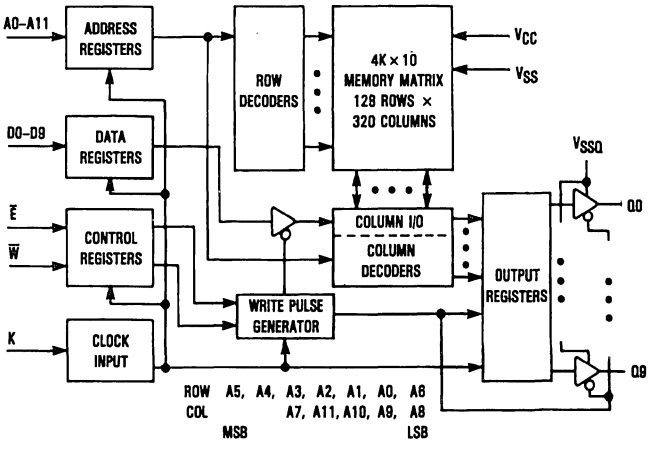
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 30 ns Max
- Fast Clock (K) Access Times: 13 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0–Q9	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, V_{out}=0 to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs=V_{IL} or V_{IH}, I_{out}=0 mA, Cycle Time≥t_{KHKH} min) t_{KHKH}=30 ns	I_{CCA}	—	140	mA
Standby Current ($\overline{E}=V_{IH}$, V_{IH}≥3.0 V, V_{IL}≤0.4 V, I_{out}=0 mA, Cycle Time≥ =t_{KHKH} min)	I_{SB}	—	30	mA
Output Low Voltage (I_{OL}=12.7 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−1.8 mA)	V_{OH}	2.8	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	3	4	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter		Symbol	MCM62963A-30		Unit	Notes
			Min	Max		
Read Cycle Time		t_{KHKH}	30	–	ns	2
Clock Access Time		t_{KHQV}	–	13	ns	3
Output Active from Clock High		t_{KHQX}	3	–	ns	4
Clock High to Q High Z ($\overline{E}=V_{IH}$)		t_{KHQZ}	–	13	ns	4
Clock Low Pulse Width		t_{KLKH}	5	–	ns	
Clock High Pulse Width		t_{KHKL}	5	--	ns	
Setup Times for:	$\overline{E}$	t_{EVKH}	5	–	ns	5
	A	t_{AVKH}				
	$\overline{W}$	t_{WHKH}				
Hold Times for:	$\overline{E}$	t_{KHEX}	3	–	ns	5
	A	t_{KHAX}				
	$\overline{W}$	t_{KHWX}				

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

4

AC TEST LOADS

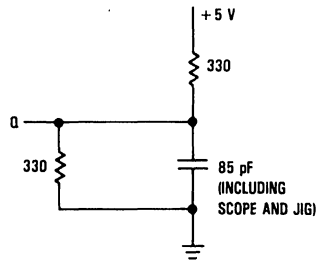


Figure 1A

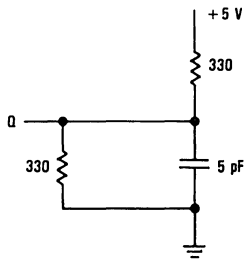
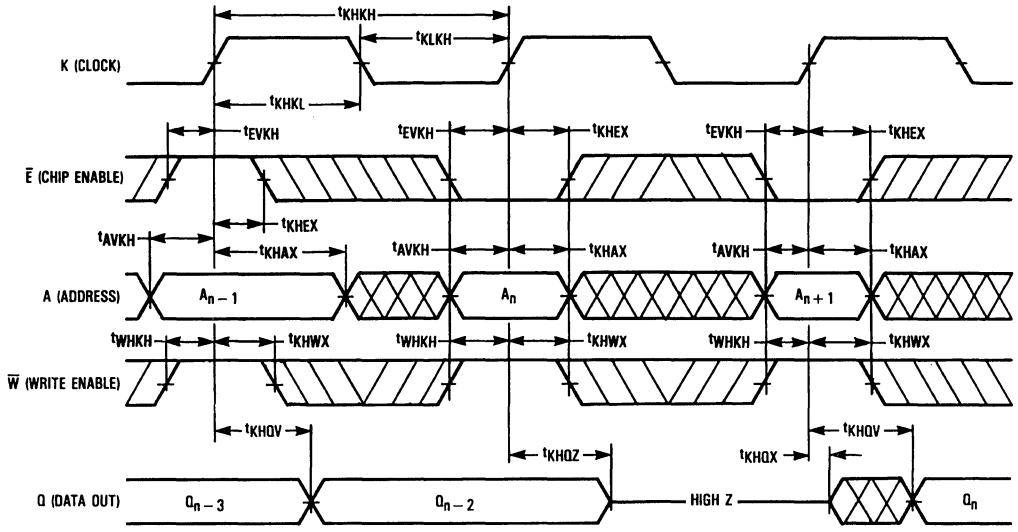
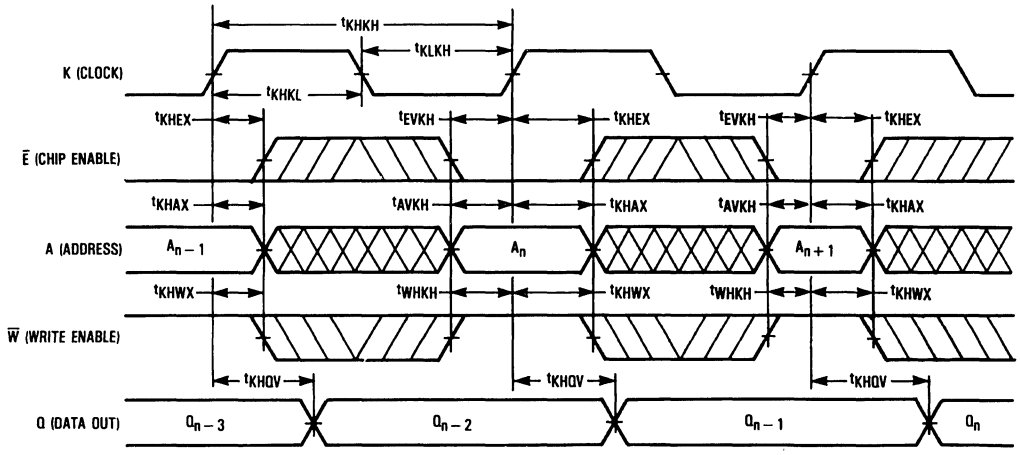


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



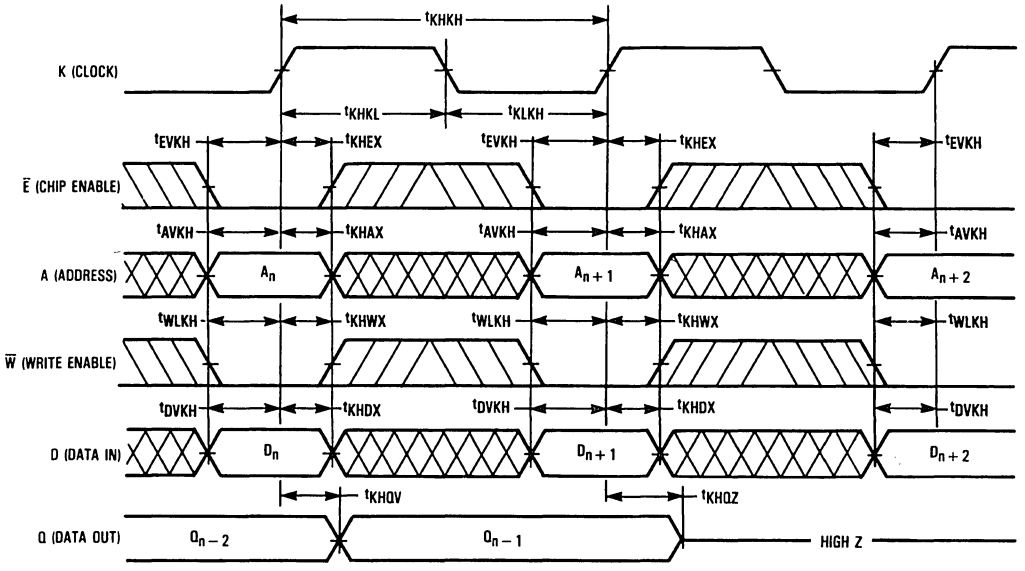
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

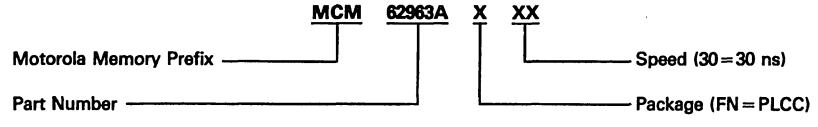
Parameter		Symbol	MCM62963A-30		Unit	Notes
			Min	Max		
Write Cycle Time		t_{KHKH}	30	—	ns	2
Clock High to Q High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	—	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	ns	4
	A	t_{AVKH}				
	$\overline{W}$	t_{WLKH}				
	D	t_{DVKH}				
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	ns	4
	A	t_{KHAX}				
	$\overline{W}$	t_{KHWX}				
	D	t_{KHDX}				

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



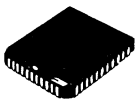
Full Part Number—MCM62963AFN30

MCM62973A

Product Preview

4K x 12 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62973A is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D11), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

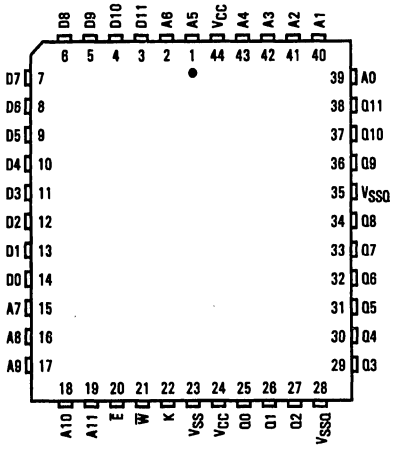
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62973A provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

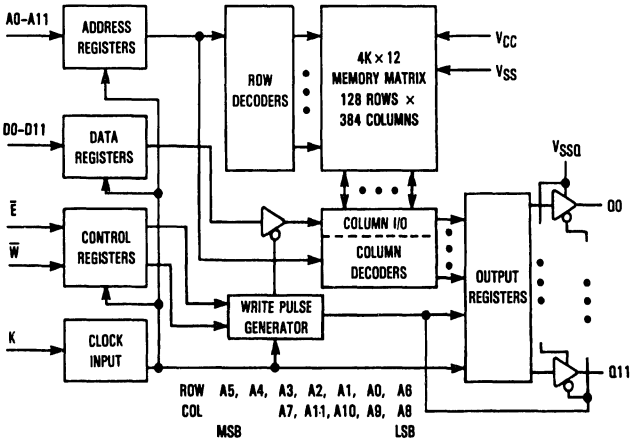
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 18/20 ns Max
- Fast Clock (K) Access Times: 10/10 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0–Q11	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of the clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, V_{out}=0 to V_{CC}, Outputs must be in High Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs=V_{IL} or V_{IH}, I_{out}=0 mA, Cycle Time≥t_{KHKH} min) MCM62973A-18: t_{KHKH}=18 ns MCM62973A-20: t_{KHKH}=20 ns	I_{CCA}	– –	170 160	mA
Standby Current ($\overline{E}=V_{IH}$, V_{IH}≥3.0 V, V_{IL}≤0.4 V, I_{out}=0 mA, Cycle Time≥ =t_{KHKH} min)	I_{SB}	–	30	mA
Output Low Voltage (I_{OL}=12.7 mA)	V_{OL}	–	0.4	V
Output High Voltage (I_{OH}=−1.8 mA)	V_{OH}	2.8	–	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	3	4	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62973A–18		MCM62973A–20		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	18	–	20	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	10	ns	3
Output Active from Clock High	t_{KHQX}	3	–	3	–	ns	4
Clock High to Q High Z ($\overline{E}$=V_{IH})	t_{KHQZ}	–	10	–	10	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	4	–	4	–	ns	5
A	t_{AVKH}						
$\overline{W}$	t_{WHKH}						
Hold Times for: $\overline{E}$	t_{KHEX}	2	–	2	–	ns	5
A	t_{KHAX}						
$\overline{W}$	t_{KHWX}						

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

AC TEST LOADS

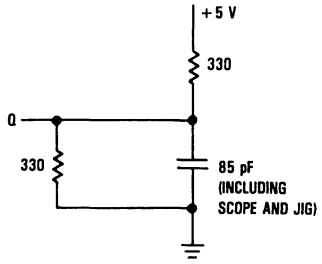


Figure 1A

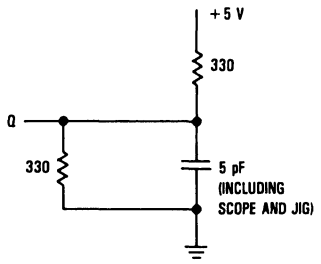
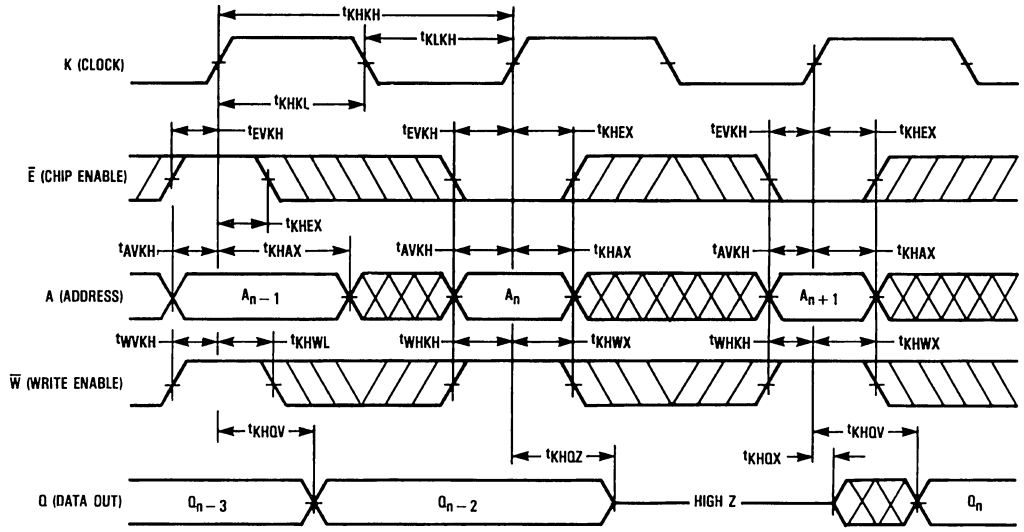
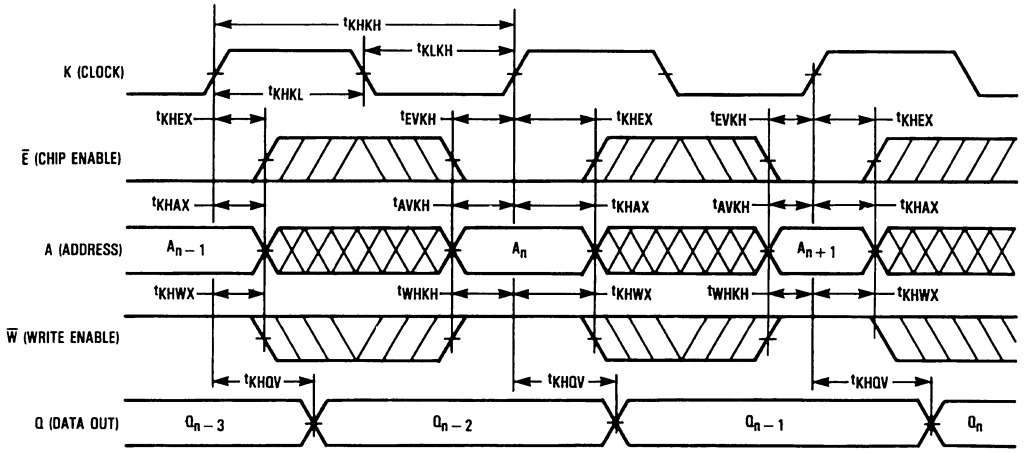


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

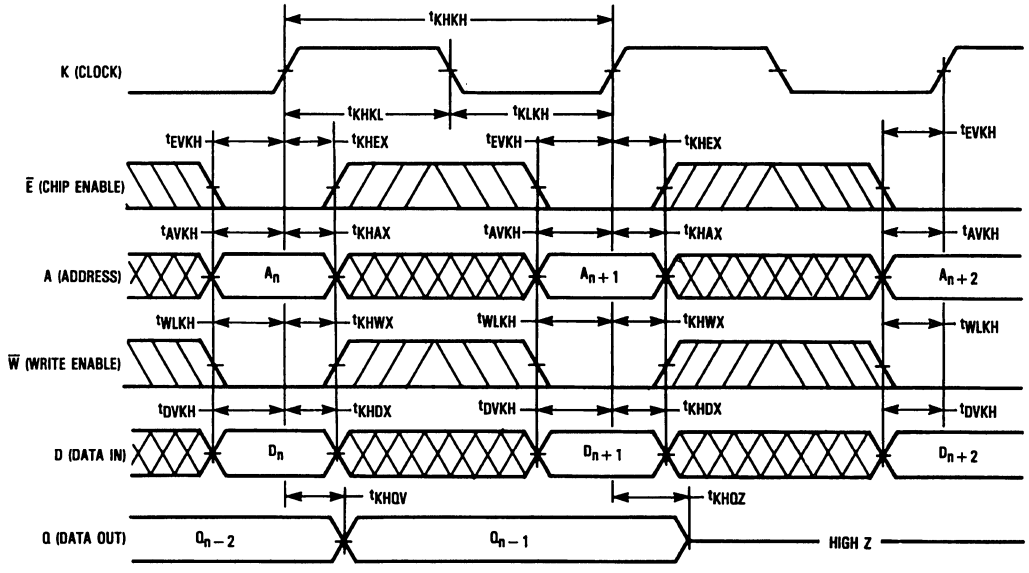
WRITE CYCLE (W Controlled, See Note 1)

Parameter		Symbol	MCM62973A-18		MCM62973A-20		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	18	–	20	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	4	–	4	–	ns	4
	A	t_{AVKH}						
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	$\overline{E}$	t_{KHEX}	2	–	2	–	ns	4
	A	t_{KHAX}						
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

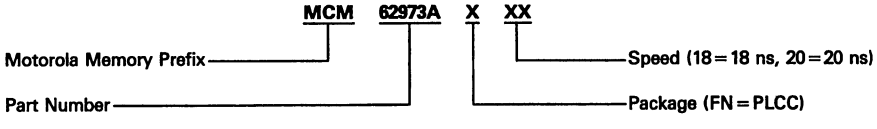
NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

4

WRITE CYCLE



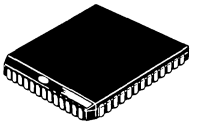
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM62973AFN18 MCM62973AFN20

MCM62990A

16K x 16 Bit Synchronous Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM62990A is a 262,144 bit synchronous static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry. Inputs to the device fall into two categories: synchronous and asynchronous. All synchronous inputs pass through positive–edge–triggered registers controlled by a single clock input (K). The synchronous inputs include all addresses, the two chip enables (SE and $\overline{SE}$), and the synchronous write enable ($\overline{SW}$).

Asynchronous inputs include the asynchronous byte write strobes ($\overline{AWL}$ and $\overline{AWH}$), output enable ($\overline{G}$), data input (DQ0 – DQ15), and the data latch enable (DL). Input data can be asynchronously latched by DL to provide simplified data–in timings during write cycles.

Address and write control are registered on–chip which greatly simplifies write cycles. Dual write strobes ($\overline{AWL}$ and $\overline{AWH}$) are provided to allow individually writeable bytes. $\overline{AWL}$ controls DQ0 – DQ7, the lower bits while $\overline{AWH}$ controls DQ8 – DQ15, the upper bits. In addition, the AWs allow late write cycles to be aborted if they are "false" during the low period of the clock. Dual chip enables (SE and $\overline{SE}$) are provided, allowing address decoding to be accomplished on–chip when the device is used in a dual bank mode.

An input data latch is provided. When data latch enable (DL) is high, the data latch is in the transparent state. When DL is low, the data latch is in the latched state. This data input latch simplifies write cycles by guaranteeing data hold time in a simple fashion.

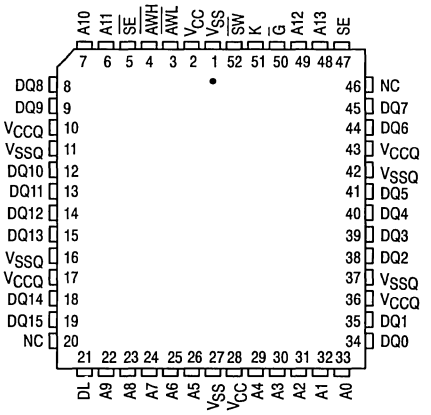
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, one set of power pins is electrically isolated from the other two and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62990A will be available in a 52 pin plastic leaded chip carrier (PLCC).

Typical applications for this device are cache memory and tag RAMs, memory in systems which are pipelined and systems which require wide data bus widths and reduced parts count.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Clock Controlled Registered Address, Write Control, and Dual Chip Enables
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

PIN ASSIGNMENT



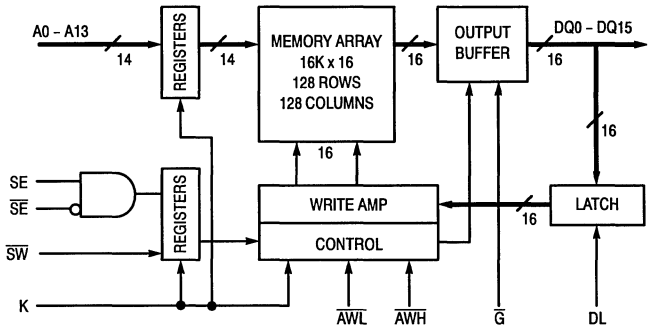
PIN NAMES	
A0 – A13	Address Inputs
K	Clock Input
DL	Data Latch Enable
$\overline{SW}$	Synchronous Write Enable
$\overline{AWL}$	Lower Byte Async Write Strobe
$\overline{AWH}$	Upper Byte Async Write Strobe
SE	Synchronous Chip Enable
$\overline{SE}$	Synchronous Chip Enable
$\overline{G}$	Asynchronous Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

4

REV 1
5/95

BLOCK DIAGRAM



TRUTH TABLE (See Notes)

SEs	$\overline{SW}$	$\overline{AWL}$	$\overline{AWH}$	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	H	X	Write Cycle All Bits Transparent Data In	I_{CC}	High–Z
T	L	H	H	X	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	H	X	Write Cycle Lower 8 Bits Transparent Data In	I_{CC}	High–Z
T	L	H	L	L	X	Write Cycle Upper 8 Bits Latched Data In	I_{CC}	High–Z

NOTES:
1. True (T) is SE = 1 and $\overline{SE}$ = 0.
2. Registered inputs (Addresses, $\overline{SW}$, SE, and $\overline{SE}$) satisfy the specified setup and hold times about the rising edge of clock (K). Data–in satisfies the specified setup and hold times for DL.
3. A transparent write cycle is defined by DL high during the write cycle.
4. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified setup and hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}**	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible) (V_{CCQ} must be ≤ V_{CC} at all times, including power up.)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)
** V_{CC} must be ≥ V_{CCQ} at all times, including power up.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G} = V_{IH}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current ($\overline{E} = V_{IH}$, $E = V_{IL}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	40	50	mA
Output Low Voltage ($I_{OL} = + 8.0$ mA)	V_{OL}	—	—	0.4	V
Output High Voltage ($I_{OH} = – 4.0$ mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25$°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	62990A–12		62990A–15		62990A–20		62990A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Times											
Clock High to Clock High	t_{KHKH}	15	—	15	—	20	—	25	—	ns	
Access Times										ns	4
Clock High to Output Valid	t_{KHQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Aborted Write Cycles										ns	
Clock Low to Asynchronous Write Strobes ($\overline{AWL}$, $\overline{AWH}$) High	t_{KLAWxH}	—	0	—	0	—	0	—	0		
Clock High to $\overline{AWx}$ Invalid	t_{KHAWxL}	2	—	2	—	2	—	2	—		
Output Buffer Control										ns	
Asynchronous Output Enable ($\overline{G}$) High to Output High Z	t_{GHQZ}	2	5	2	5	2	5	2	5		1
$\overline{G}$ Low to Output Low Z	t_{GLQX}	2	—	2	—	2	—	2	—		1
Reads:											
Clock (K) High to Output Low Z After Deselect or Write	t_{KHQX1}	8	—	8	—	8	—	8	—		1
Data Out Hold After Clock High	t_{KHQX2}	5	—	5	—	5	—	5	—		5
Writes:											
K High to Output High Z After Read	t_{KHQZ}	3	10	3	10	3	10	3	10		1
Clock										ns	
Clock High Time	t_{KHKL}	4	—	4	—	4	—	4	—		
Clock Low Time	t_{KLKH}	7	—	8	—	10	—	10	—		
Setup Times										ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—	3	—	3	—		5
Synchronous Write ($\overline{SW}$) Valid to Clock High	t_{SWVKH}	3	—	3	—	3	—	3	—		5
Synchronous Enables (SE, $\overline{SE}$) Valid to Clock High	t_{SEVKH}	3	—	3	—	3	—	3	—		5
Writes:											
Data–In Valid to Clock High	t_{DVKH}	5	—	6	—	6	—	7	—		2, 5
$\overline{AWL}$, $\overline{AWH}$ Low to Clock High	t_{AWxLKH}	6	—	6	—	6	—	7	—		5
Data Latch:											
Data–In Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		3, 5
Hold Times										ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—	2	—	2	—		5
Clock High to $\overline{SW}$ Invalid	t_{KHSWX}	3	—	3	—	3	—	3	—		5
Clock High to SE, $\overline{SE}$ Invalid	t_{KHSEX}	3	—	3	—	3	—	3	—		5
Writes:											
Clock High to Data–In Invalid	t_{KHDX}	2	—	2	—	2	—	2	—		2, 5
Clock High to $\overline{AWL}$, $\overline{AWH}$ High	t_{KHAWxH}	2	—	2	—	2	—	2	—		5
Clock High to DL High	t_{KHDLH}	2	—	2	—	2	—	2	—		3, 5
Data Latch:											
DL Low to Data–In Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		3, 5
DL High to Clock High	t_{DLHKH}	5	—	6	—	6	—	7	—		3, 5

NOTES:
1. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} and t_{GHQZ} is less than t_{GLQX} for a given device.
2. A transparent write cycle is defined by DL high during the write cycle.
3. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified hold time for the rising edge of clock (K).
4. Into rated load of 85 pF equivalent resistive load (see Figure 1A).
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for all rising edges of clock (K) or falling edges of data latch enable (DL).

AC TEST LOADS

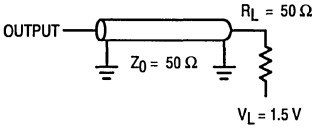


Figure 1A

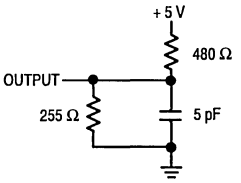
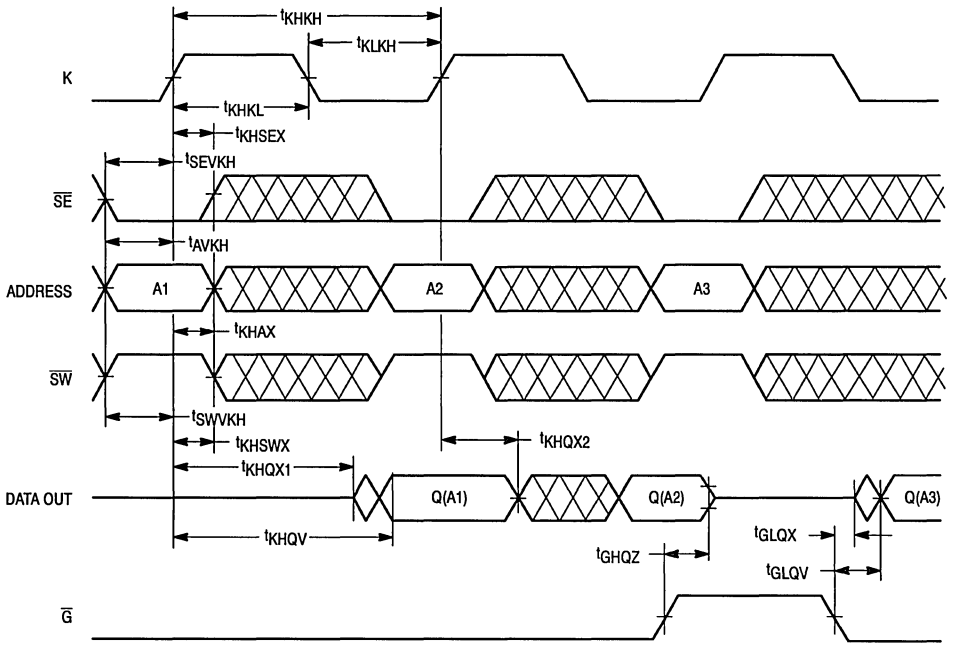


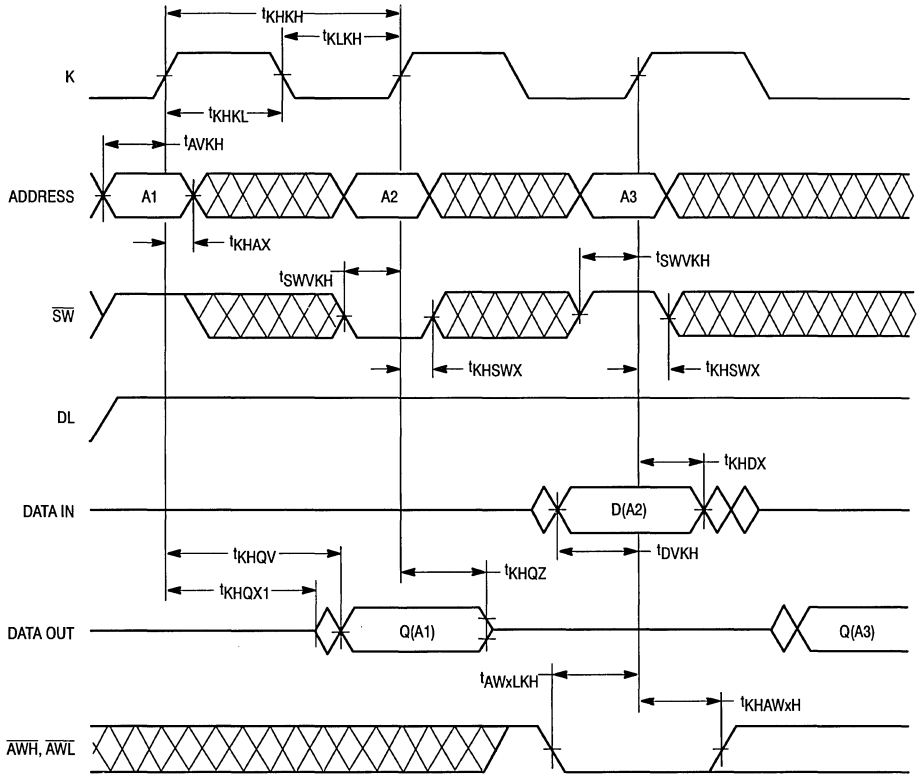
Figure 1B

READ CYCLES

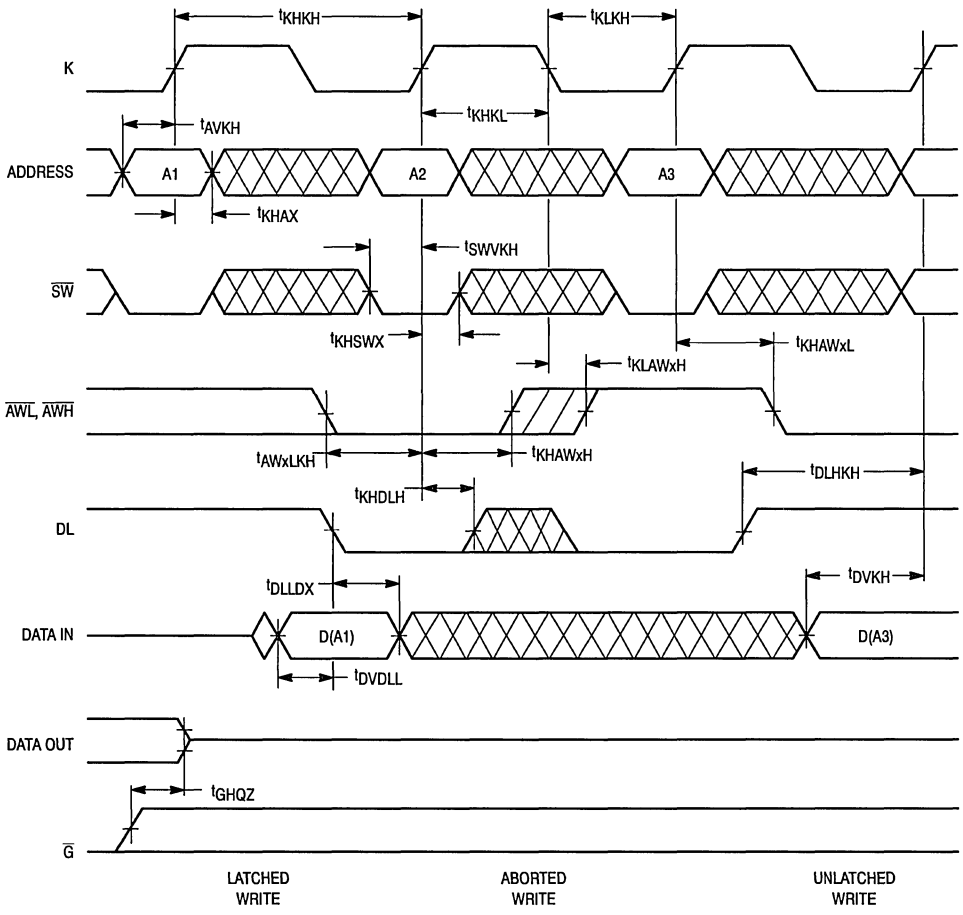


4

READ–UNLATCHED WRITE–READ CYCLES

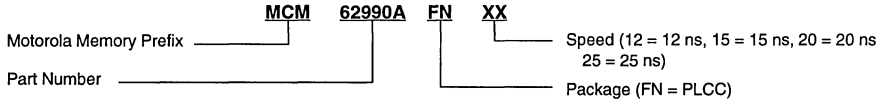


WRITE CYCLES



4

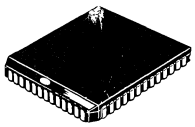
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM62990AFN12 MCM62990AFN15 MCM62990AFN20 MCM62990AFN25

MCM62995A

16K x 16 Bit Asynchronous/ Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM62995A is a 262,144 bit latched address static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Address, data in, and chip enable latches are provided. When latch enable (LE for address and chip enables and DL for data in) is high, the address, data in, and chip enable latches are in the transparent state. If latch enable (LE, DL) is tied high, the device can be used as an asynchronous SRAM. When latch enable (LE, DL) is low, the address, data in and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

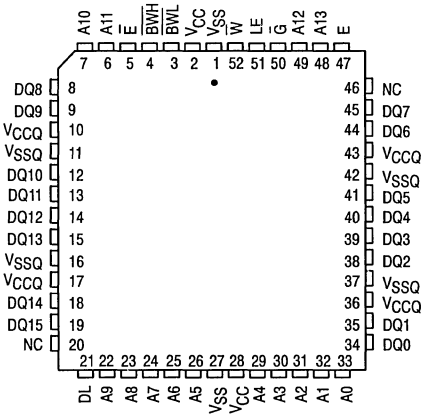
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62995A is available in a 52 pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

PIN ASSIGNMENT

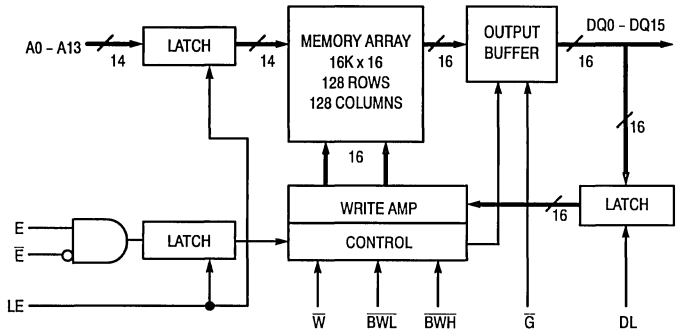


PIN NAMES	
A0 – A13	Address Inputs
LE	Latch Enable
DL	Data Latch Enable
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

REV 2
5/95

BLOCK DIAGRAM



TRUTH TABLE

Es	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	LE	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
T	H	X	X	H	X	H	Read Cycle	I_{CC}	High–Z
T	H	X	X	H	X	L	Read Cycle	I_{CC}	Data Out
T	H	X	X	L	X	L	Latched Read Cycle	I_{CC}	Data Out
T	L	L	L	H	H	X	Write Cycle All Bits	I_{CC}	High–Z
T	L	H	H	X	X	X	Aborted Write Cycle	I_{CC}	High–Z
T	L	L	H	H	H	X	Write Cycle Lower 8 Bits	I_{CC}	High–Z
T	L	H	L	H	L	X	Write Cycle Upper 8 Bits Latched Data–In	I_{CC}	High–Z
T	L	L	L	L	L	X	Latched Write Cycle Latched Data–In	I_{CC}	High–Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and Addresses satisfy the specified setup and hold times for the falling edge of LE. Data–in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC TEST LOADS

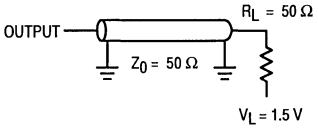


Figure 1A

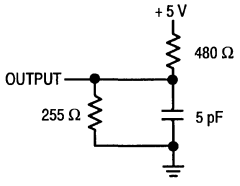


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, V_{CCQ} = 3.3 V or 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

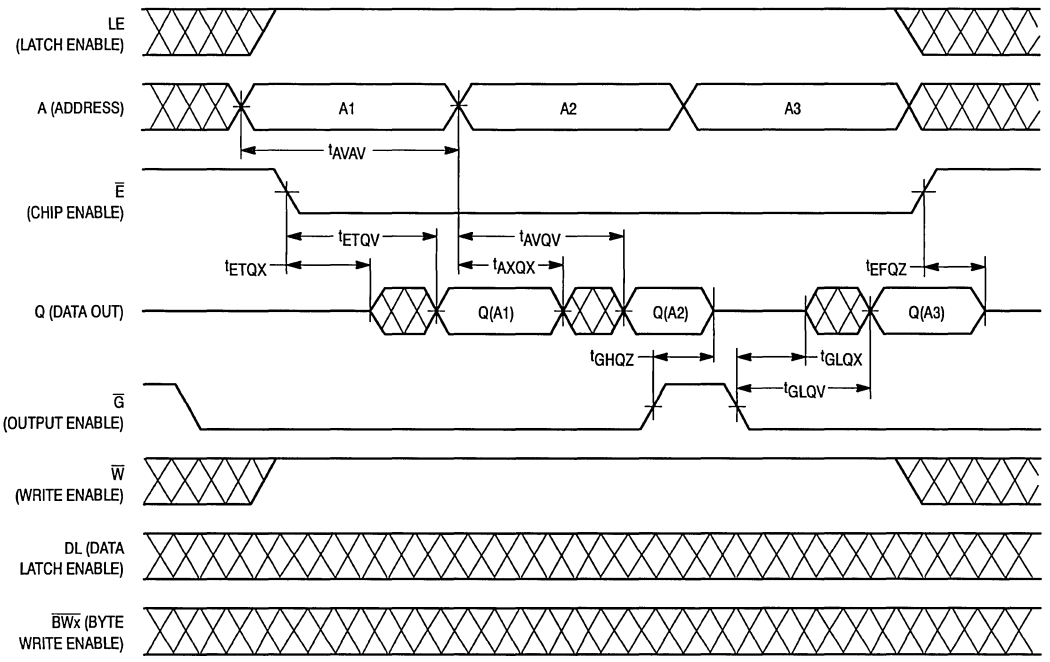
Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	6
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	2	9	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	8	2	10		
Power Up Time	t_{ETICCA}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. Write Enable is equal to V_{IH} for all read cycles.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All read cycle timing is referenced from the last valid address to the first transitioning address.
6. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

ASYNCHRONOUS READ CYCLES

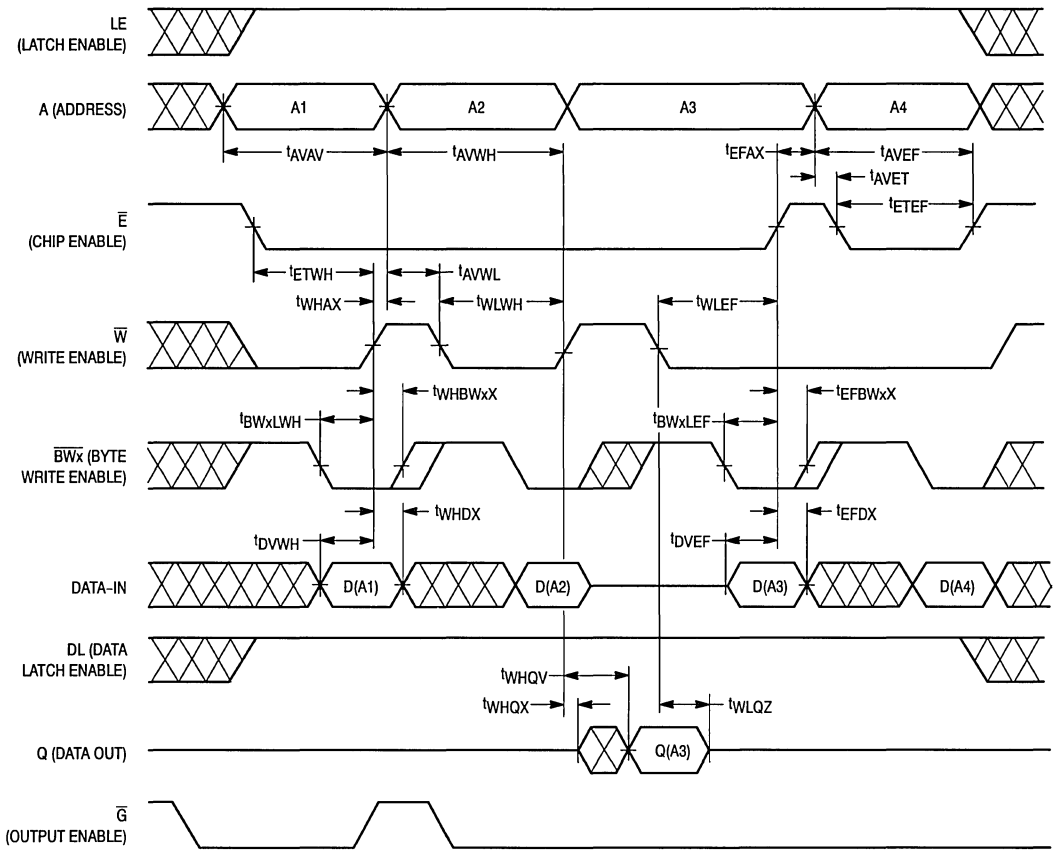


ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	6
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to E, $\overline{E}$ "False"	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		2
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ High to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:
1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
3. Write must be equal to V_{IH} for all address transitions.
4. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
5. EF is defined by $\overline{E}$ going high or E going low.
6. All write cycle timing is referenced from the last valid address to the first transitioning address.
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

ASYCHRONOUS WRITE CYCLE



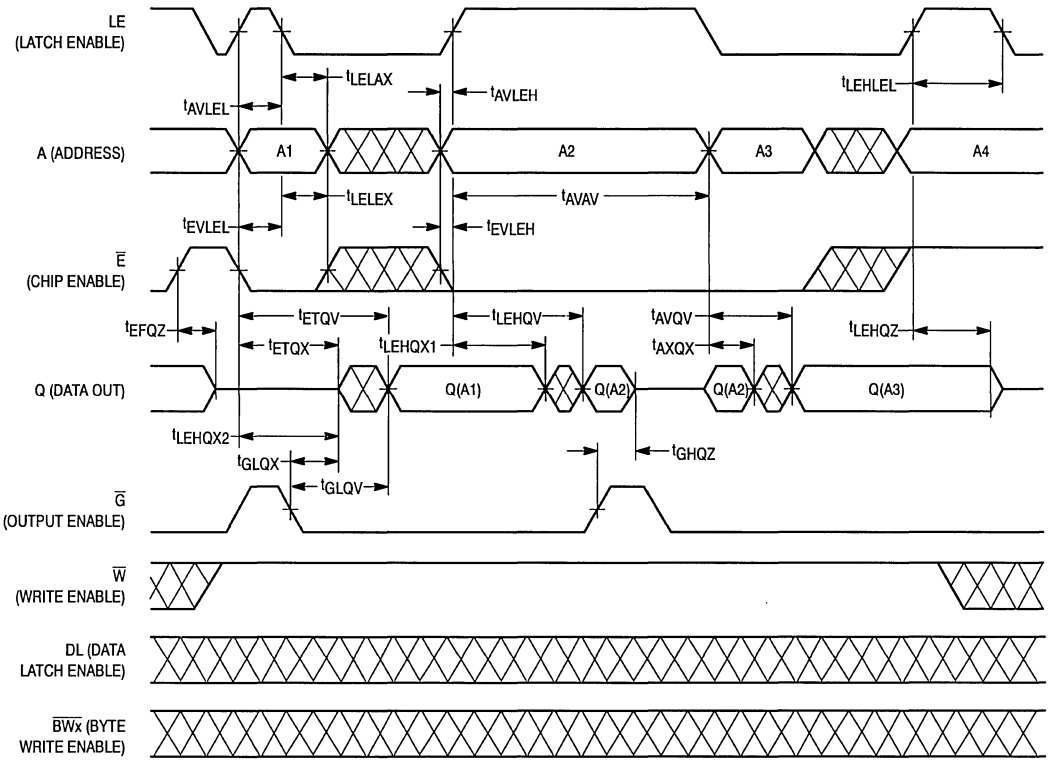
4

LATCHED READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		5
LE High to Output Valid	t_{LEHQV}	—	12	—	15	—	20	—	25		6
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Setup Times:										ns	
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		6
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		6
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Hold Times:										ns	6
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		
Output Hold:										ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—	4	—		
LE High to Output Invalid	t_{LEHQX1}	4	—	4	—	4	—	4	—		
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
LE High to Output Active	t_{LEHQX2}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High–Z	t_{EFQZ}	2	9	2	9	2	10	2	10		
LE High to Output High–Z	t_{LEHQZ}	2	9	2	9	2	10	2	10		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	8	2	10		

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. Addresses valid prior to or coincident with $\overline{E}$ going low and E going high
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



4

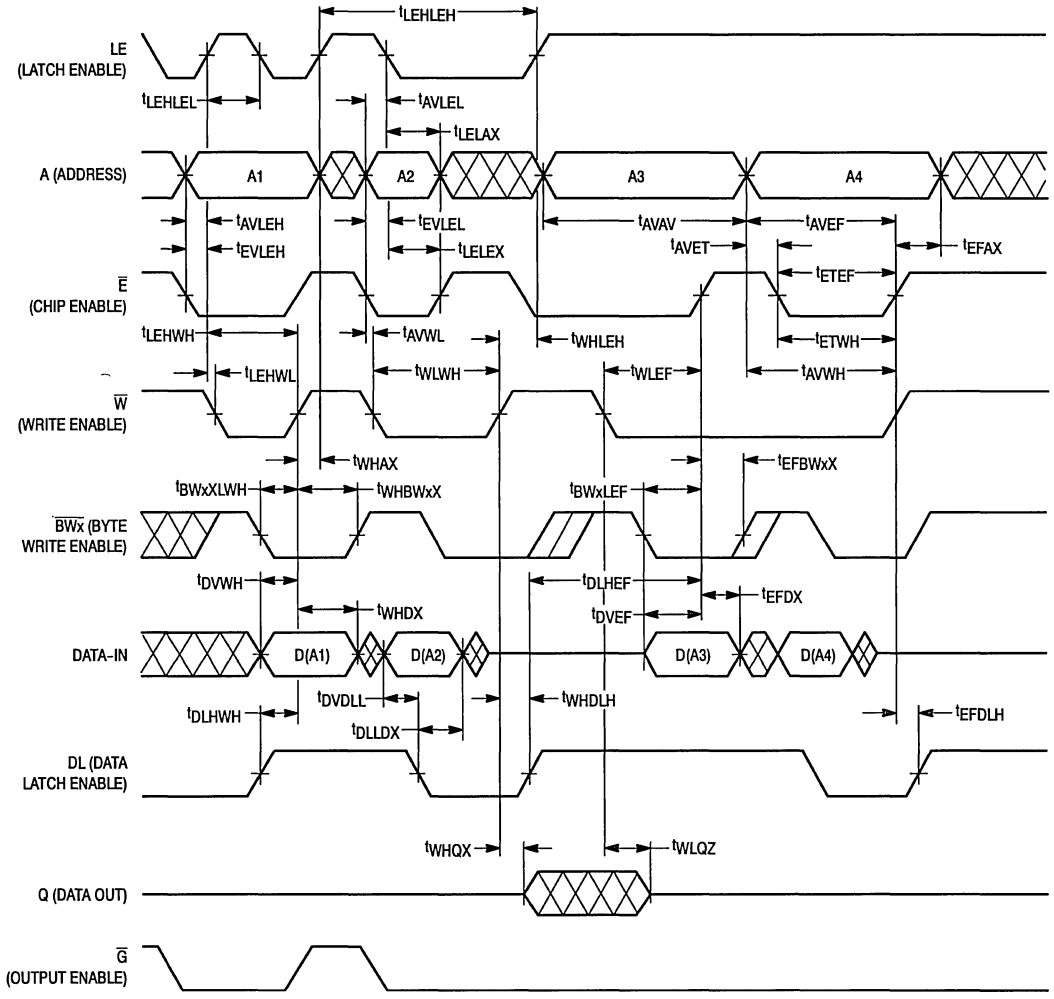
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A–12		62995A–15		62995A–20		62995A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times:										ns	5
Address Valid to Address Valid	t_{AVAV}	15	—	15	—	20	—	25	—		
LE High to LE High	t_{LEHLEH}	15	—	15	—	20	—	25	—		
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
LE High to $\overline{W}$ Low	t_{LEHWL}	0	—	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	5	—	6	—	8	—	10	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	8	—	10	—		
DL High to E, $\overline{E}$ "False"	t_{DLHEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Hold Times:										ns	
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		5
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		5
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to DL High	t_{EFDLH}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to LE High	t_{WHLEH}	0	—	0	—	0	—	0	—		
Write Pulse Width:										ns	
LE High to $\overline{W}$ High	t_{LEHWH}	12	—	13	—	15	—	20	—		6
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remians at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

LATCHED WRITE CYCLES



4

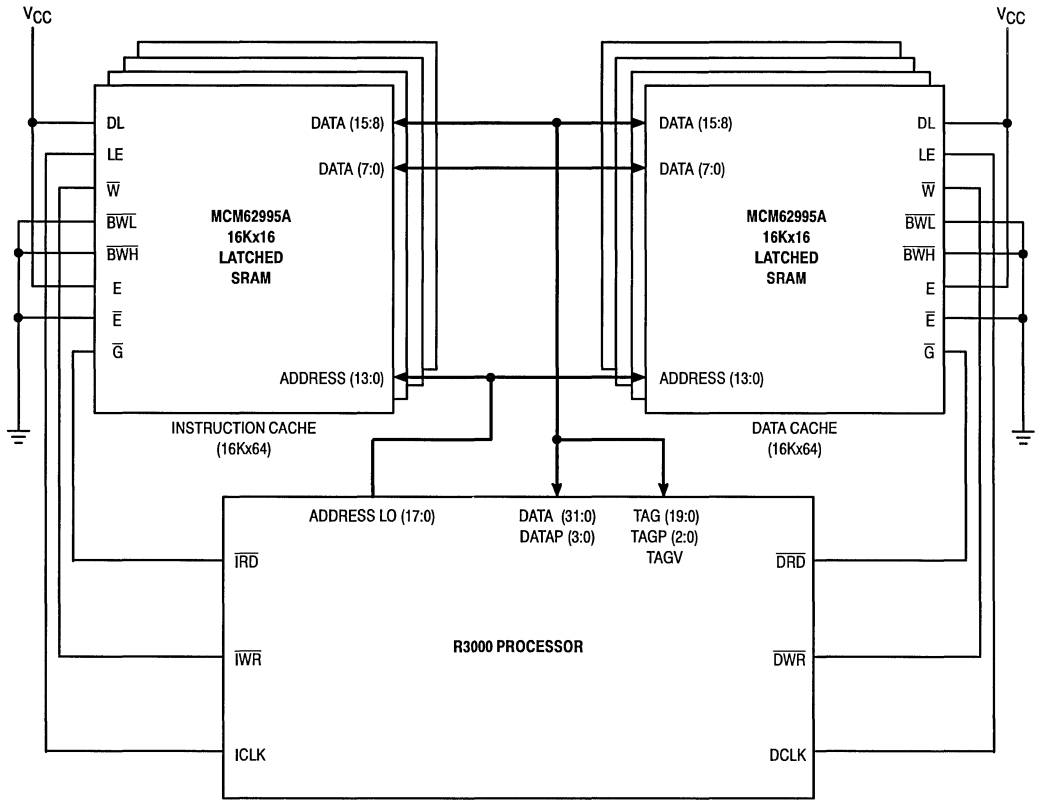


Figure 2. R3000 Application Example with 128K Byte Segregated Instruction/Data Cache Using Eight Motorola MCM62995A Latched SRAMs

ORDERING INFORMATION
(Order by Full Part Number)

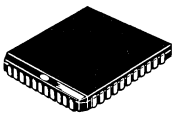
MCM 62995A FN XX

- MCM — Motorola Memory Prefix
- 62995A — Part Number
- FN — Package (FN = PLCC)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns 25 = 25 ns)

Full Part Numbers — MCM62995AFN12 MCM62995AFN15 MCM62995AFN20 MCM62995AFN25

MCM67T316

8K x 16 Bit Synchronous Cache Tag RAM



FN PACKAGE
44–LEAD PLCC
CASE 777–02

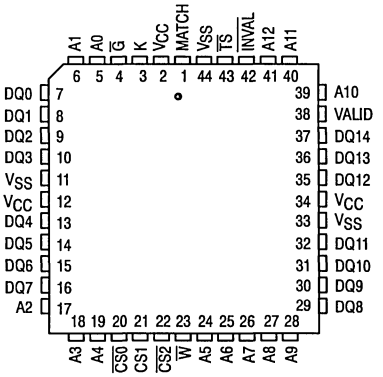
The MCM67T316 is a 131,072 bit synchronous static random access memory organized as 8,192 words of 16 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. Each word contains a 15–bit address tag and a valid bit.

The MCM67T316 compares the address tag stored in the RAM with the current input data. The result is either an active high MATCH level for a cache hit, or a low level for a cache miss. The valid bit is used to qualify a cache hit or miss. The entire tag memory can be invalidated by resetting all the valid bits. This is accomplished by holding the $\overline{\text{INVAL}}$ pin low for four consecutive cycles.

The MCM67T316 is available in a 44 pin PLCC package.

- 8K x 16 Fast Access Static Memory Array
- Single 5 V ± 10% Power Supply
- Fast Match Time: 10/12 ns Max
- Fast Clock Cycle Time: 15/25 ns Min
- Registered Address, Data, and Control Inputs
- Valid Bit on Each Word to Qualify a Cache Hit/Miss
- Four Cycles to Invalidate the Entire Tag Memory
- Cascadable to Two Cache Tags with No External Logic

PIN ASSIGNMENTS



PIN NAMES	
A0 – A12	Tag Address Inputs
K	Clock Input
$\overline{\text{TS}}$	Tag Select Input
$\overline{\text{W}}$	Tag Write Enable Input
VALID	Valid Bit Input/Output
$\overline{\text{INVAL}}$	Tag Invalidate Input
MATCH	Cache Match Output
$\overline{\text{G}}$	Output Enable Input
$\overline{\text{CS0}}$, CS1, $\overline{\text{CS2}}$	Chip Select Input
DQ0 – DQ14	Data Input/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

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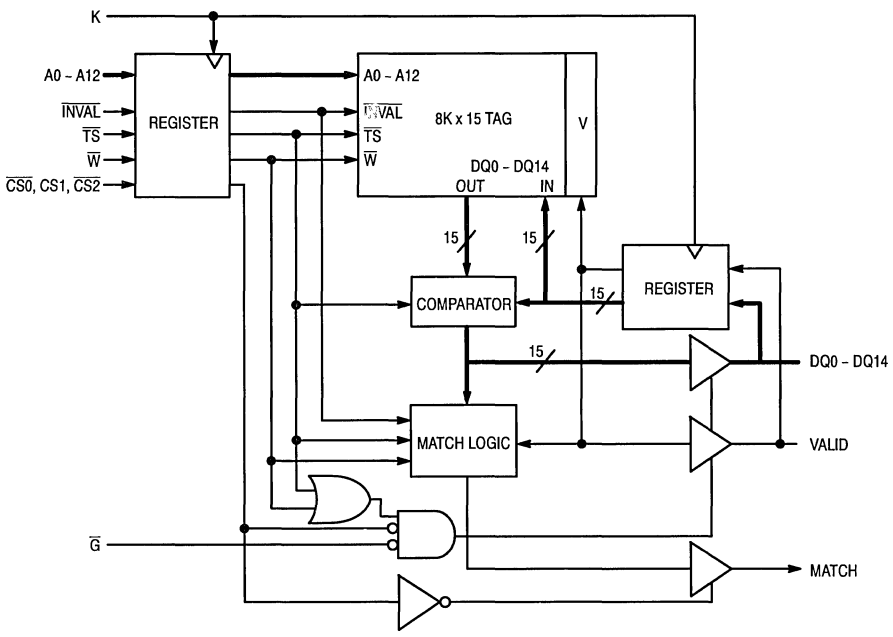
BLOCK DIAGRAM



TRUTH TABLE (See Notes)

W	TS	G	CS	INVAL	K	Mode	Supply Current	DQ0 – DQ14 Status	VALID Status	MATCH Status
X	H	L	T	H	L–H	Not Allowed	I_{CC}	Compare Out	Data Out	Data Out
X	H	H	T	H	L–H	Tag Compare	I_{CC}	Data In	High–Z	Data Out
H	L	L	T	H	L–H	Tag Read	I_{CC}	Data Out	Data Out	H
H	L	H	T	H	L–H	Tag Read	I_{CC}	High–Z	High–Z	H
L	L	L	T	H	L–H	Not Allowed	I_{CC}	High–Z	High–Z	H
L	L	H	T	H	L–H	Tag Write	I_{CC}	Data In	Data In	H
X	X	X	F	H	L–H	Chip Deselected	I_{SB}	High–Z	High–Z	High–Z
X	X	X	X	L	4 cycle	Invalidate Memory	I_{INV}	—	L	L

NOTES:
1. X means don't care, T means selected, F means deselected, and L–H means low to high transition.
2. All inputs except G must meet setup and hold times for low–to–high transition of clock (K).

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
5, 6, 17, 18, 19, 24, 25, 26, 27, 28, 39, 40, 41	A0 – A12	Input	ADDRESS – Registered on the rising clock edge. The 13 address input pins are used to select one of the 8,192 tag entries.
3	K	Input	CLOCK – The clock input pin accepts a minimum 5 ns clock high or clock low pulse at a minimum 15 ns clock cycle. All inputs except Output Enable are synchronous and controlled by the clock.
43	$\overline{TS}$	Input	TAG SELECT – Registered on rising clock edge, $\overline{TS}$ is active low. When this pin is asserted, the device is in tag access mode, where the memory can be modified. When this pin is high, the device is in tag compare mode. In this mode, the tag memory is used for address comparison only and cannot be modified.
23	$\overline{W}$	Input	TAG WRITE ENABLE – Registered on the rising clock edge, $\overline{W}$ is active low. When this pin is asserted in tag access mode ($\overline{TS}$ = 0), the device will write the data on DQ0 – DQ14 to memory. Set $\overline{W}$ high in the tag access mode to read the contents of the memory. This input is ignored in tag compare mode ($\overline{TS}$ = 1).
38	VALID	I/O	VALID BIT – Registered on the rising clock edge. This pin reflects the valid bit in tag compare mode and tag read mode. In tag access write mode, data on this pin is stored in the valid bit. If $\overline{INVAL}$ is asserted, VALID will be forced low. This pin will be three–stated if either the output is disabled ($\overline{G}$ = 1) or the device is deselected.
42	$\overline{INVAL}$	Input	TAG INVALIDATE – Registered on the rising clock edge, $\overline{INVAL}$ is active low. Assert this pin to set all valid bits low, which invalidates the entire tag memory. The tag memory can be invalidated even when deselected. For invalidation to complete, the $\overline{INVAL}$ pin must be asserted for four rising clock edges. The $\overline{INVAL}$ pin must be asserted at power–up to ensure that the valid bits for all address tags are set low.
1	MATCH	Output	TAG MATCH – In the tag compare mode ($\overline{TS}$ = 1), a high at this output indicates a cache hit, and a low indicates a cache miss. In the tag access mode ($\overline{TS}$ = 0), this output remains high, except when $\overline{INVAL}$ is asserted, which drives the MATCH output low. MATCH can be three–stated by deselecting the part, but $\overline{G}$ has no effect on the MATCH output.
4	$\overline{G}$	Input	OUTPUT ENABLE – Asynchronous pin, active low. When this pin is set high, the data pin (DQ0 – DQ14) and the VALID pin will be three–stated. The $\overline{G}$ input must be asserted to use VALID pin and data pins (DQ0 – DQ14) as outputs.
20, 22	$\overline{CS0}$, $\overline{CS2}$	Input	CHIP SELECT – Registered on the rising clock edge, $\overline{CS0}$ and $\overline{CS2}$ are active low. To enable this device, $\overline{CS0}$, $\overline{CS2}$ must be set low and CS1 set high. Otherwise, the device will be disabled, and all outputs will be three–stated.
21	CS1	Input	CHIP SELECT – Registered on the rising clock edge, CS1 is active high. To enable this device, $\overline{CS0}$, $\overline{CS2}$ must be set low and CS1 set high. Otherwise, the device will be disabled, and all outputs will be three–stated.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37	DQ0 – DQ14	I/O	DQ pins are registered on the rising clock edge. In tag access mode ($\overline{TS}$ = 0), data in the tag memory can be modified using these pins. In tag compare mode ($\overline{TS}$ = 1), the data is compared to the tag word specified by the address. If $\overline{INVAL}$ is asserted these pins go into an unknown state. These pins will be three–stated if either the outputs are disabled ($\overline{G}$ = 1) or the device is deselected.

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ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL}(min) = – 3.0 V ac (pulse width ≤ 10 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current (CS = Selected, $\overline{G}$ = V_{IH}, I_{out} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V, and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min) MCM67T316–10 MCM67T316–12	I_{CCA}	 — —	 — —	 275 250	mA
AC Supply Current ($\overline{INVAL}$ = V_{IL} for four cycles, I_{out} = 0 mA, All inputs = V_{IL} or V_{IH},V_{IL} = 0 V, and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min) MCM67T316–10 MCM67T316–12	I_{INV}	 — —	 — —	 305 280	mA
AC Standby Current (CS = Deselected, All inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	—	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... 50 Ohm Transmission Line

TAG COMPARE, READ, AND WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67T316–10		MCM67T316–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	25	—	ns	
Clock High Time	t_{KHKL}	5	—	8	—	ns	
Clock Low Time	t_{KLKH}	5	—	8	—	ns	
Clock High to MATCH Valid	t_{KHMV}	—	10	—	12	ns	
Clock High to Output Valid	t_{KHQV}	—	10	—	12	ns	
Output High to Output High–Z Due to $\overline{W}$	t_{KHWQZ}	—	8	—	8	ns	
Output High to Output High–Z	t_{KHQZ}	—	8	—	8	ns	
Output High to Output Change	t_{KHQX}	3	—	3	—	ns	
Output Enable Low to Output Valid	t_{GLQV}	—	8	—	8	ns	
Output Enable Low to Output Active	t_{GLQX}	3	—	3	—	ns	
Output Enable High to Output High–Z	t_{GHQZ}	—	8	—	8	ns	
Setup Times: Address Write Tag Select Invalid Chip Select Data In	t_{AVKH} t_{WVKH} t_{TSVKH} t_{IVVKH} t_{CSVKH} t_{DVKH}	3	—	3	—	ns	3
Hold Times: Address Write Tag Select Invalid Chip Select Data In	t_{KHAX} t_{KHWX} t_{KHTSX} t_{KHIVX} t_{KHCSX} t_{KHDX}	1	—	3	—	ns	3
Clock High to MATCH Active	t_{KHMX}	3	—	3	—	ns	
Clock High to MATCH Low After $\overline{INVAL}$ Low	t_{KHML}	—	8	—	8	ns	
Clock High to VALID Low After $\overline{INVAL}$ Low	t_{KHVL}	—	8	—	8	ns	

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of clock when the chip is selected. Chip enable must be valid at each rising edge of clock for the device to remain enabled.

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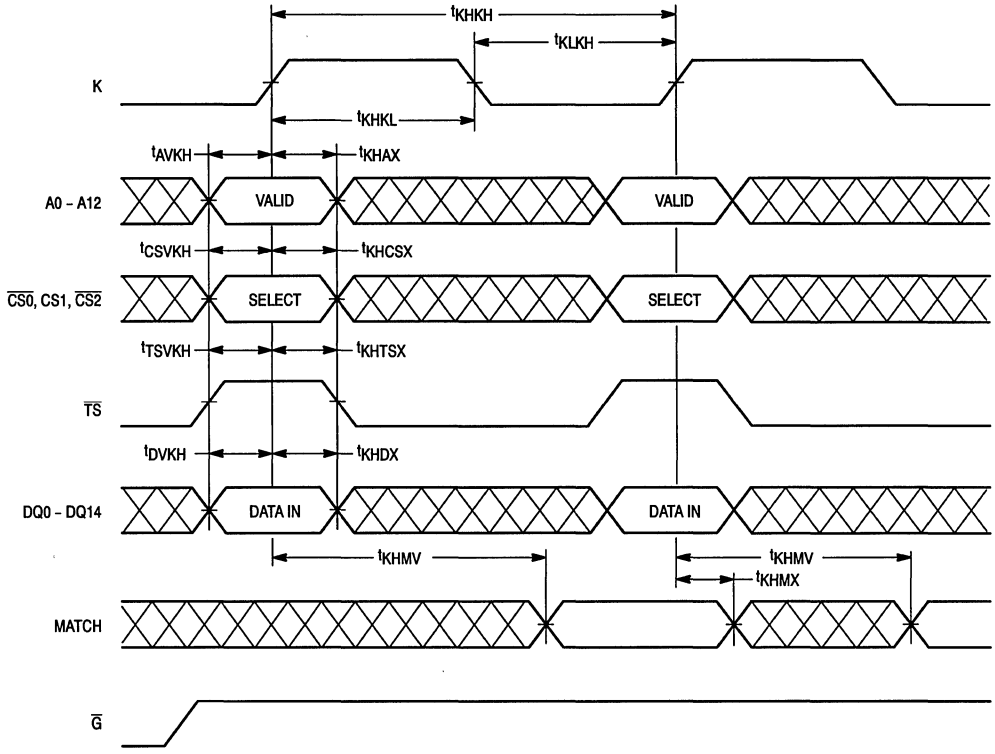
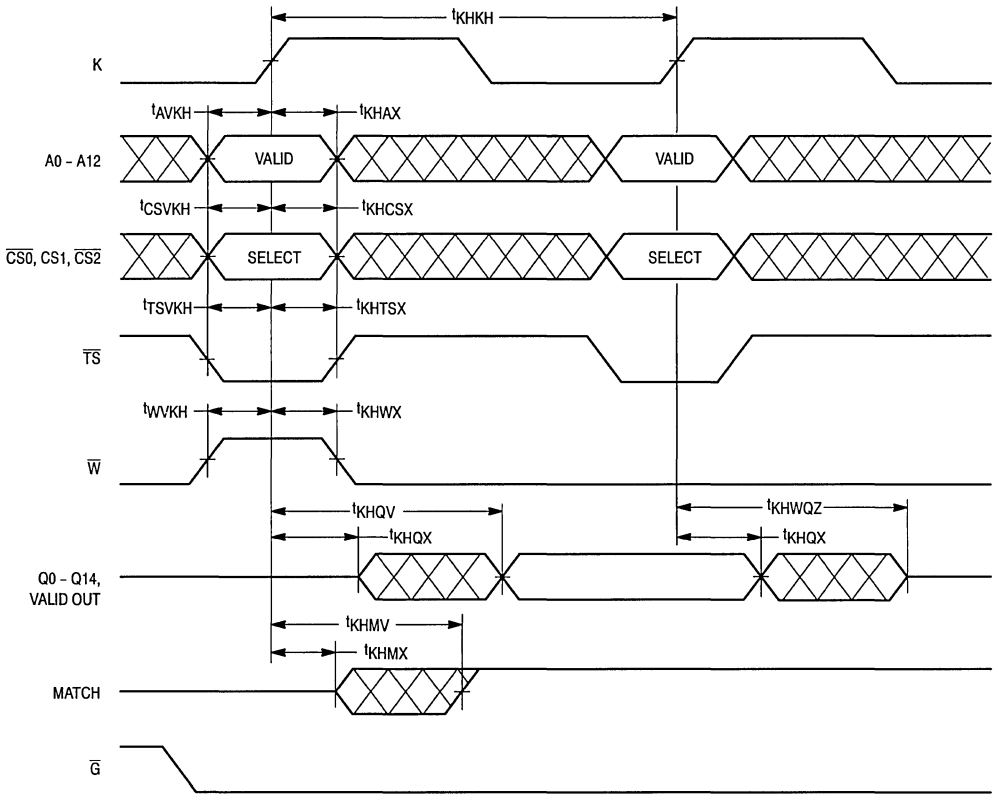
TAG COMPARE CYCLE



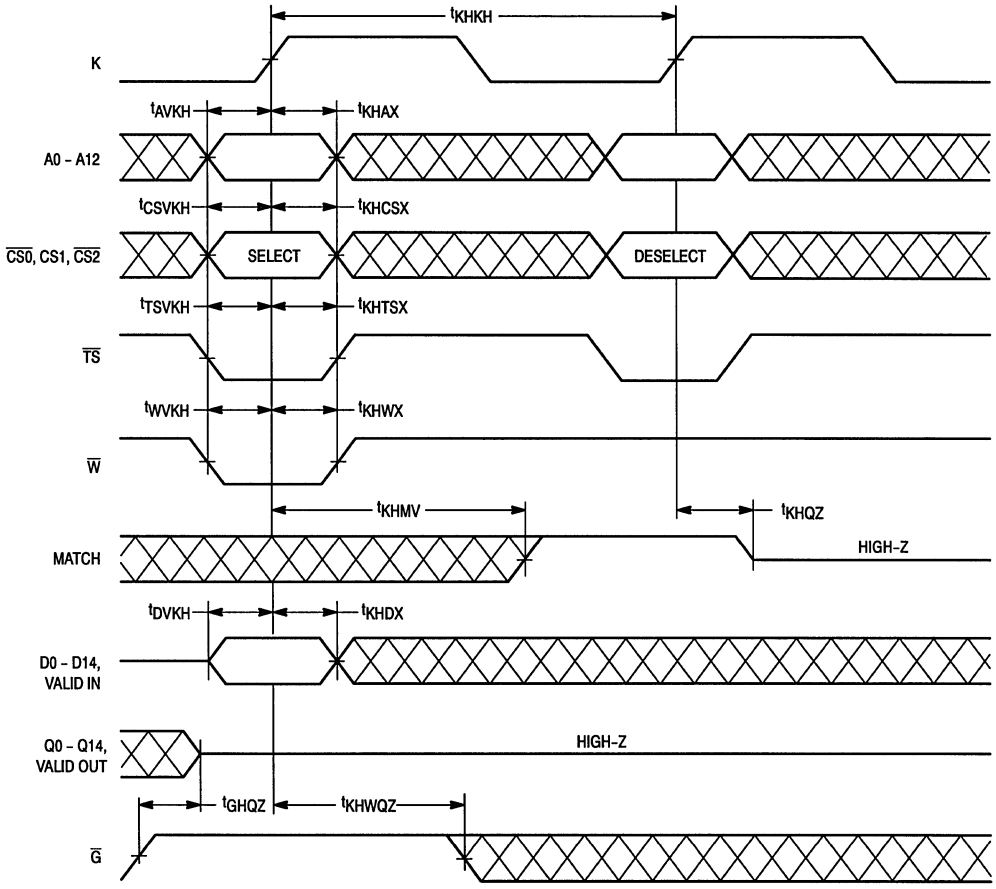
4

READ CYCLE

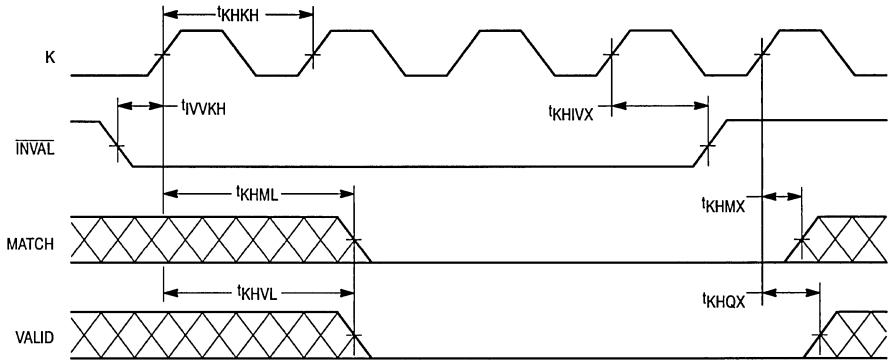

tKHKH
K
tAVKH
tKHAX
A0 - A12
VALID
VALID
tCSVKH
tKHCSX
CS0, CS1, CS2
SELECT
SELECT
tTSVKH
tKHTSX
TS
tWVKH
tKHWX
W
tKHQV
tKHQX
tKHWQZ
tKHQX
Q0 - Q14,
VALID OUT
tKHMV
tKHMX
MATCH
G

4

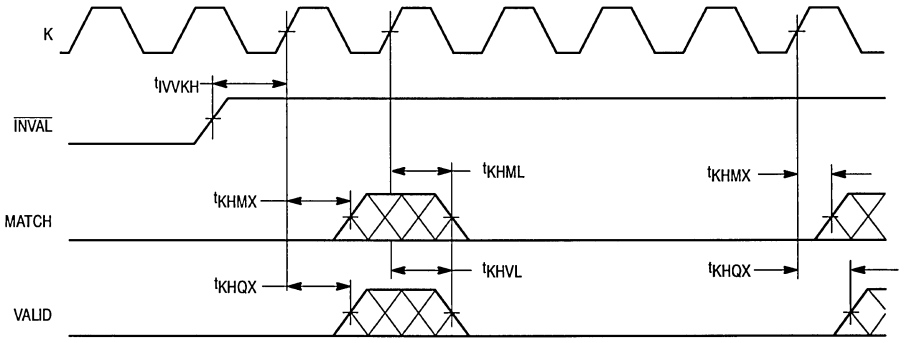
WRITE CYCLES



MEMORY INVALIDATION CYCLE



AT POWER–UP



NOTE: The first low to high transition of $\overline{\text{INVAL}}$ after power–up will initiate an invalidation cycle. All subsequent low to high transition will end invalidation cycles.

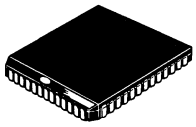
ORDERING INFORMATION
(Order by Full Part Number)

MCM	67T316	FN	XX
Motorola Memory Prefix			
Part Number			
			Speed (10 = 10 ns,12 = 12 ns)
		Package (FN = PLCC)	

Full Part Number — MCM67T316FN10
MCM67T316FN12

MCM67A518

32K x 18 Bit Asynchronous/ Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67A518 is a 589,824 bit latched address static random access memory organized as 32,768 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 32K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high, the device can be used as an asynchronous SRAM. When latch enables are low, the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

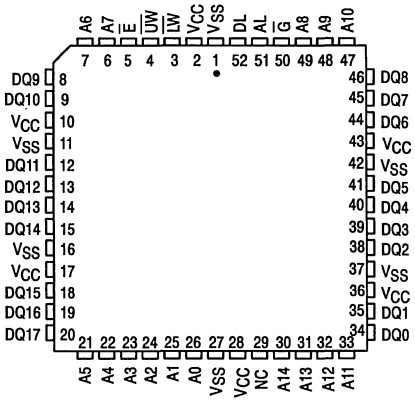
Additional power supply pins have been utilized and placed on the package for maximum performance.

The MCM67A518 will be available in a 52–pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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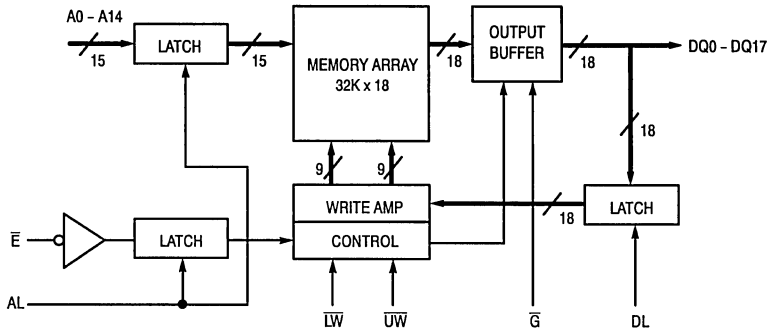
BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High–Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High–Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High–Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data–in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time ≥ t_{AVAV} min)	I_{CCA10} I_{CCA12} I_{CCA15}	—	290 275 260	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, f = f_{max})	I_{SB1}	—	75	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A518–10		MCM67A518–12		MCM67A518–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	9		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

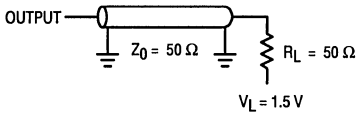


Figure 1A

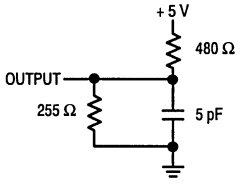
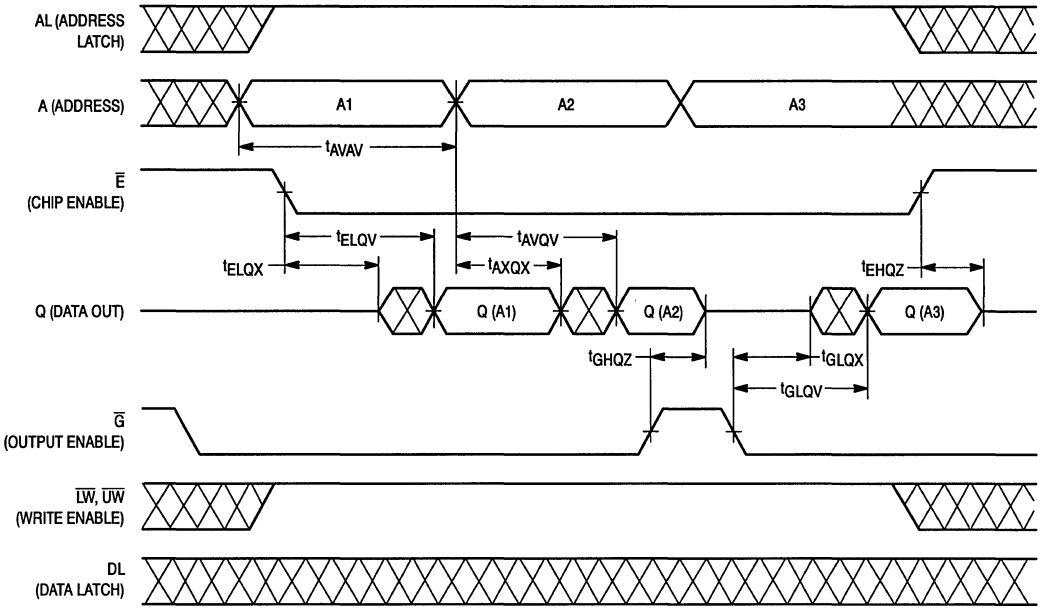


Figure 1B

ASYNCHRONOUS READ CYCLES



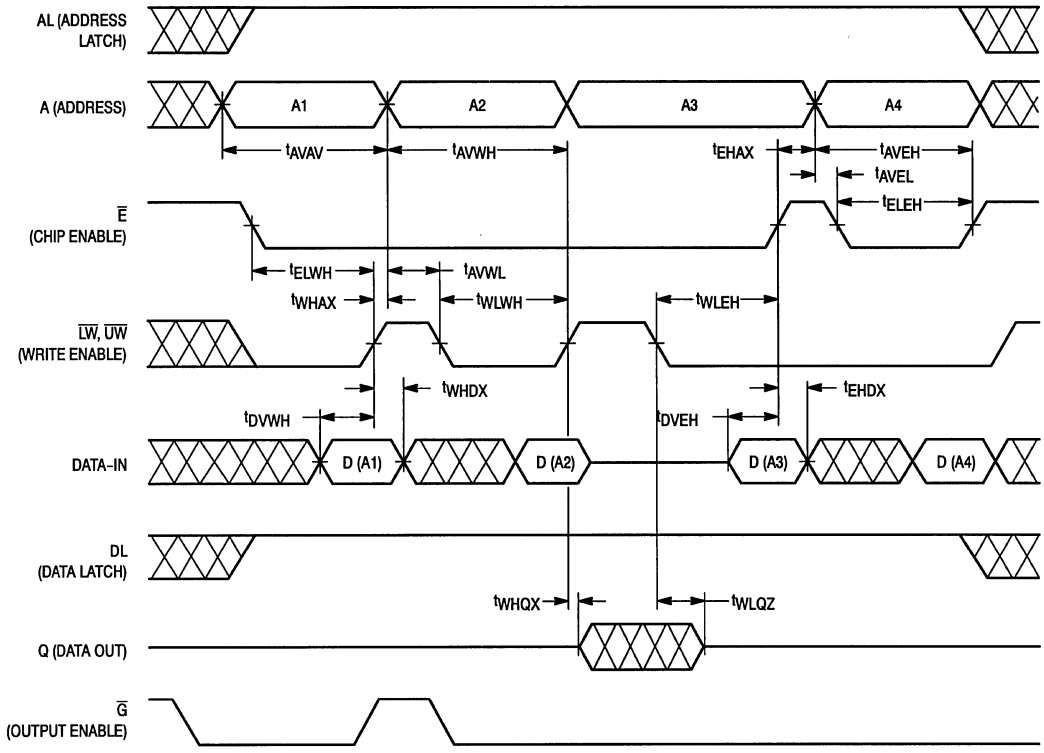
4

ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A518–10		MCM67A518–12		MCM67A518–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to $\overline{E}$ High	t_{AVEH}	9	—	10	—	13	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
Hold Times:								ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width:								ns	
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEF}	9	—	10	—	13	—		5
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		5, 6
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	10	—	12	—	15	—		
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	5	—		7
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		7, 8

NOTES:
1. W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE



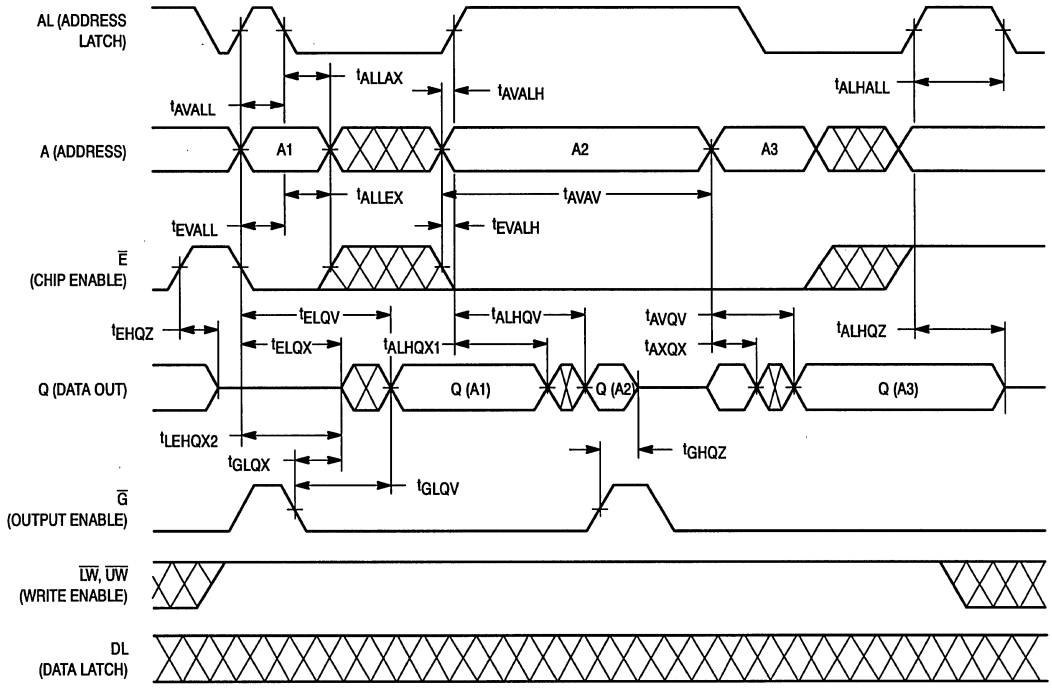
4

LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A518–10		MCM67A518–12		MCM67A518–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		3
AL High to Output Valid	t_{ALHQV}	—	10	—	12	—	15		4
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	2	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQZ}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	3	—	2	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	9		
AL High to Output High–Z	t_{ALHQZ}	2	5	2	6	2	9		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		

NOTES:
1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



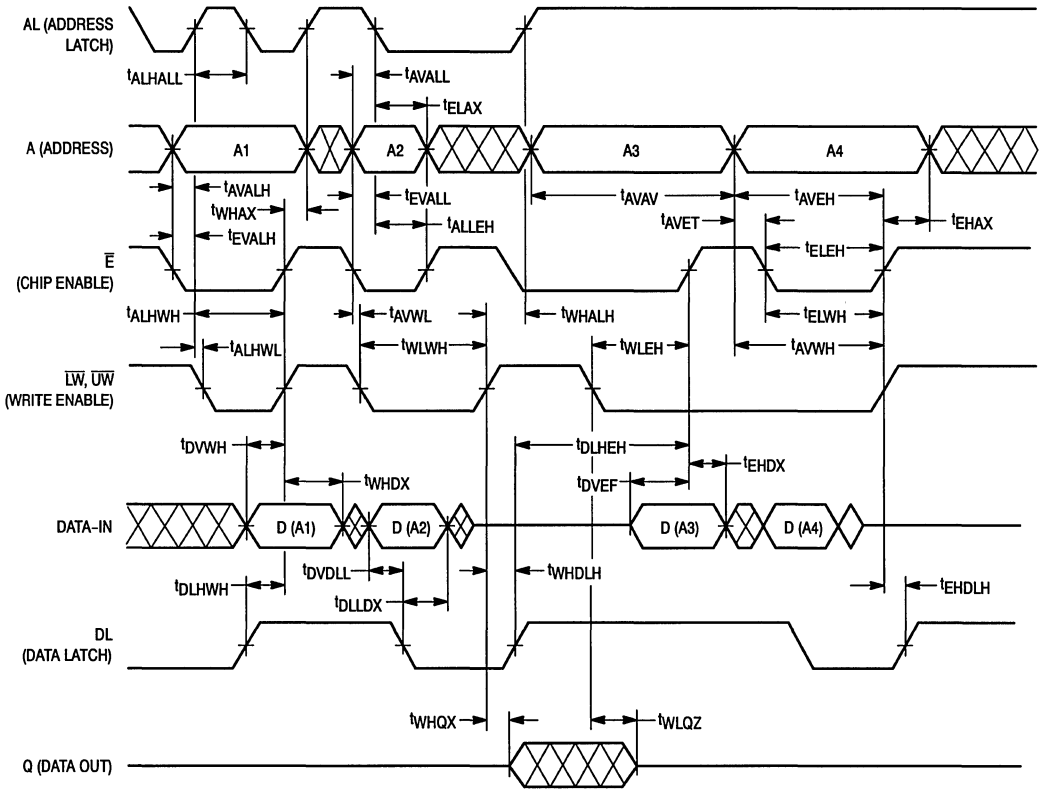
4

LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A518–10		MCM67A518–12		MCM67A518–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to End of Write	t_{AVEH}	9	—	10	—	13	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	7	—		
DL High to $\overline{E}$ High	t_{DLHEH}	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\overline{E}$ High	t_{ALLEH}	2	—	2	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EFDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	9	—	10	—	13	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		7
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	5	—	12	—	15	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	10	—	12	—	15	—		
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	5	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		8, 9

NOTES:
1. W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

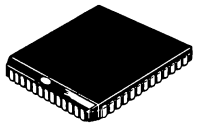
MCM 67A518 X XX

- MCM: Motorola Memory Prefix
- 67A518: Part Number
- X: Package (FN = PLCC)
- XX: Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)

Full Part Numbers — MCM67A518FN10 MCM67A518FN12 MCM67A518FN15

MCM67A618

64K x 18 Bit Asynchronous/ Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67A618 is a 1,179,648 bit latched address static random access memory organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 64K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high the device can be used as an asynchronous SRAM. When latch enables are low the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

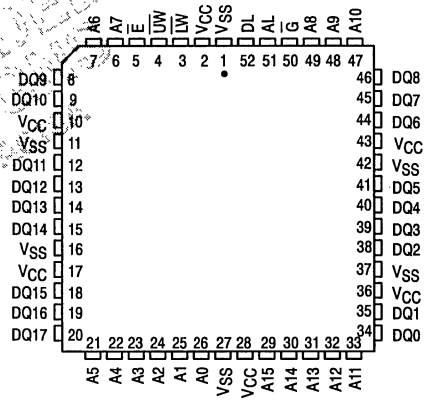
Six pair of power and ground pins have been utilized and placed on the package for maximum performance.

The MCM67A618 will be available in a 52–pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT



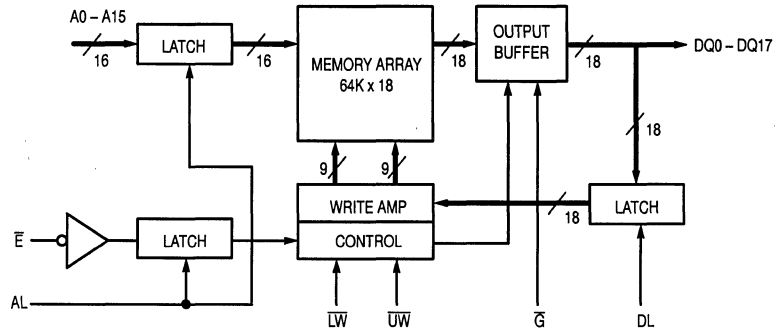
PIN NAMES	
A0 – A15	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

4

REV 4
5/95

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High–Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High–Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High–Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data–in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Standby Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA10} I_{CCA12} I_{CCA15}	—	290 280 265	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB1}	—	95	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	7		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

4

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

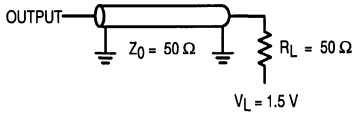


Figure 1A

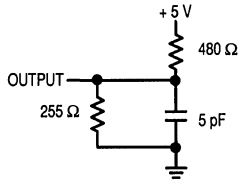
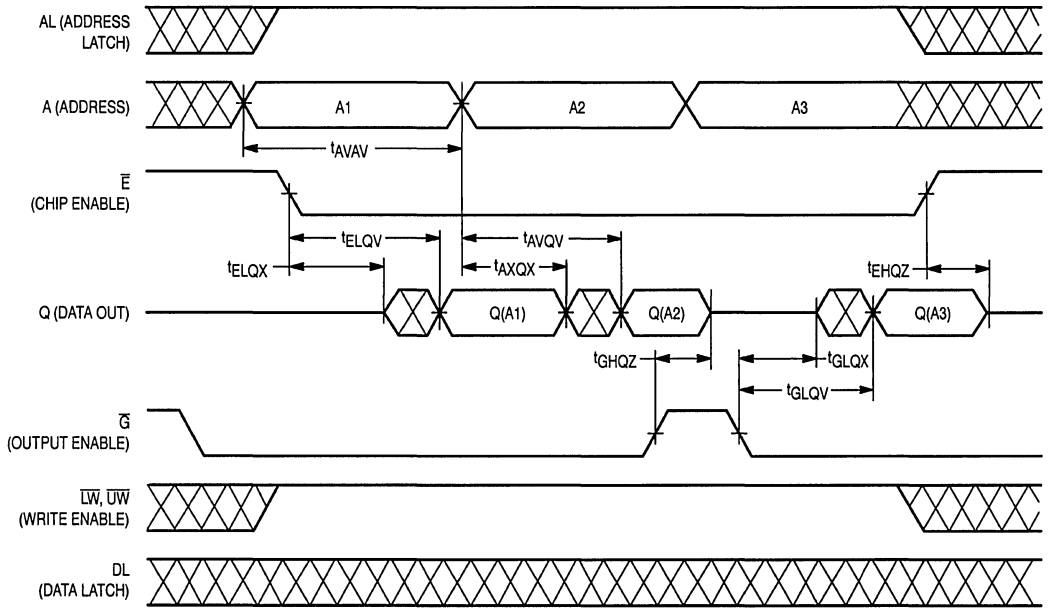


Figure 1B

ASYNCHRONOUS READ CYCLES



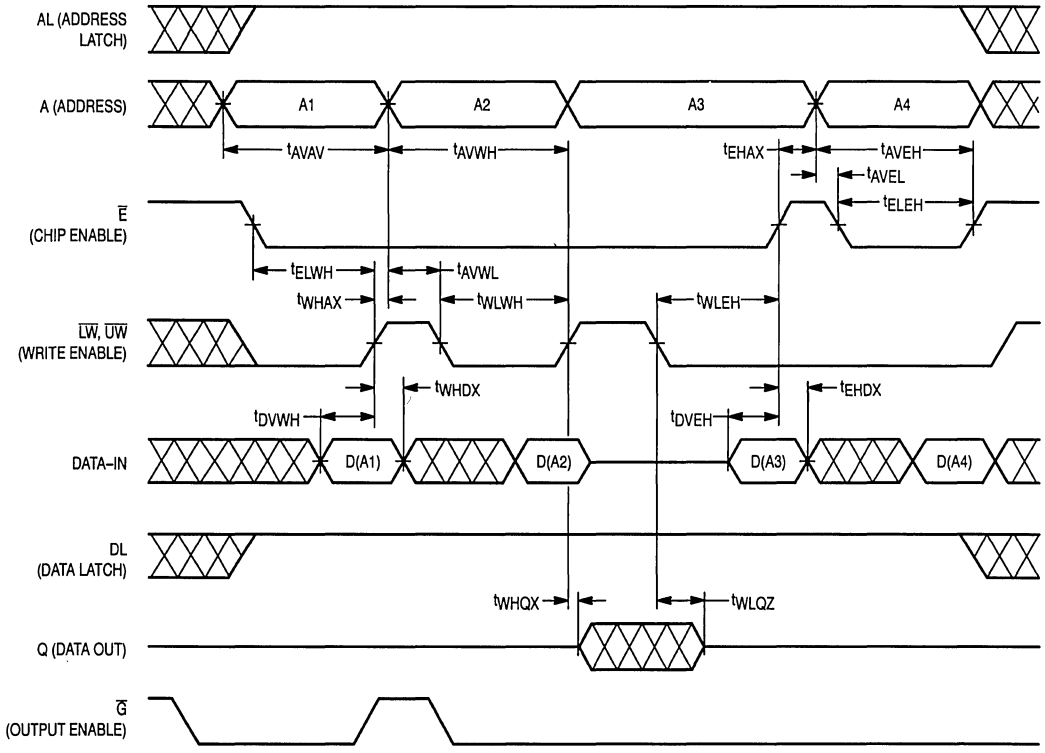
4

ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times: Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—	ns	
Address Valid to $\overline{E}$ High	t_{AVEH}	9	—	10	—	13	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
DataValid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
Hold Times: $\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	ns	
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width: Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		5
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		5, 6
Output Buffer Control: $\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	7
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		7, 8

NOTES:
1. W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE



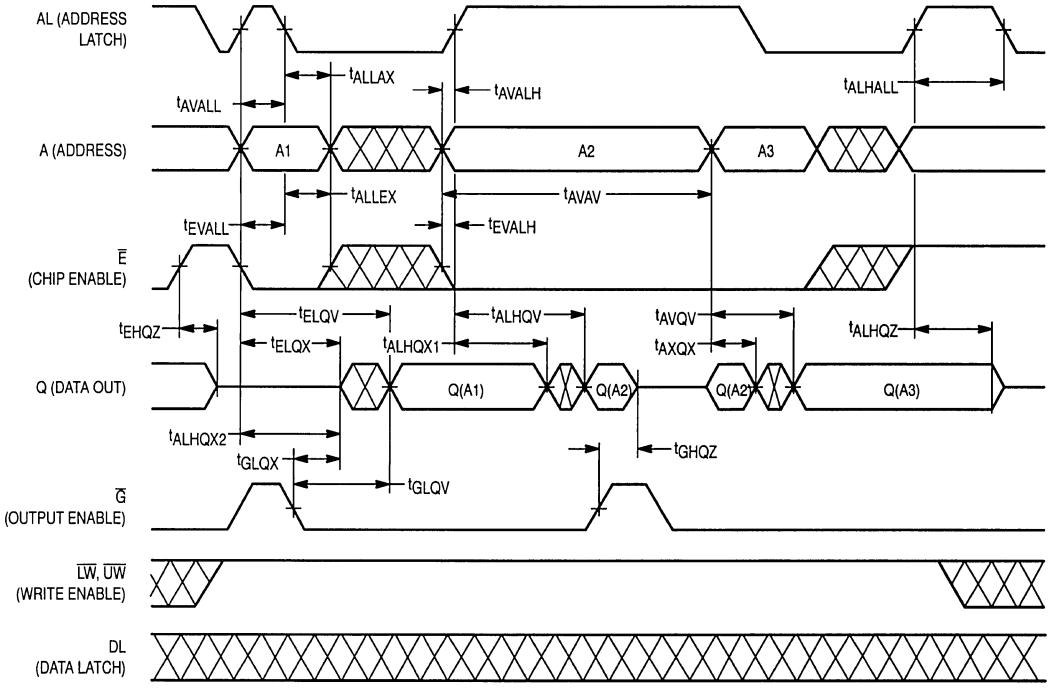
4

LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		3
AL High to Output Valid	t_{ALHQV}	—	10	—	12	—	15		4
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	2	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	3	—	3	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	9		
AL High to Output High–Z	t_{ALHQZ}	2	5	2	6	2	9		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		

NOTES:
1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{ALHQZ} is less than t_{ALHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



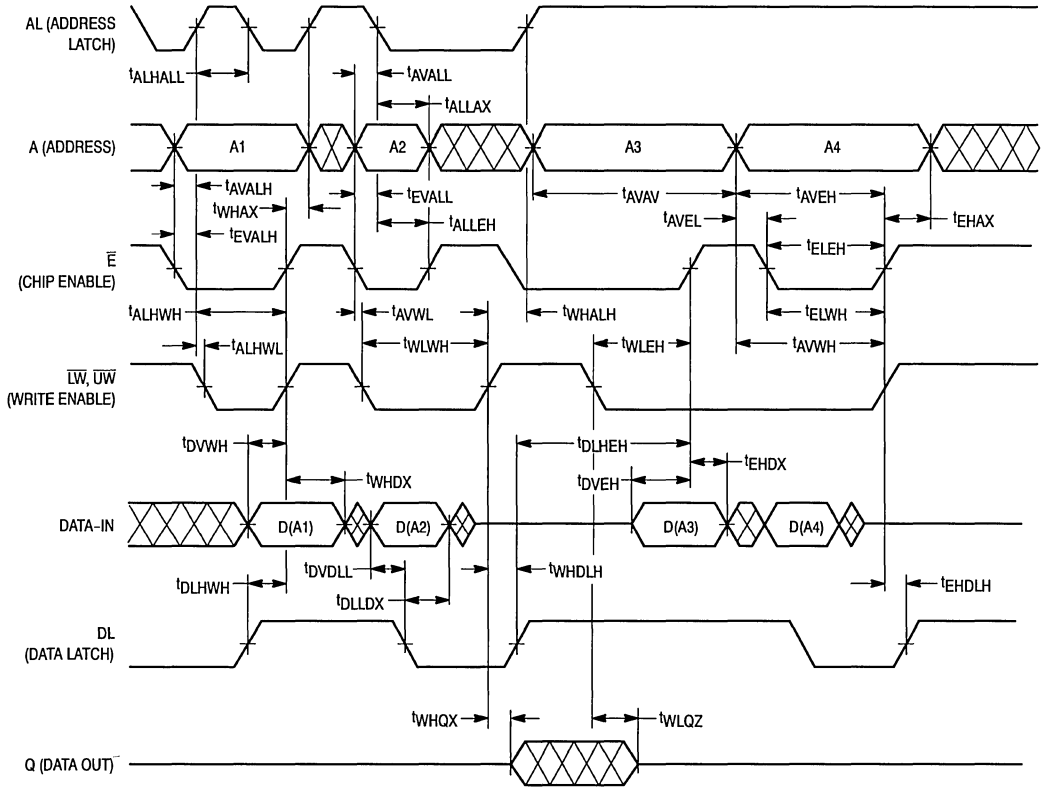
4

LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618–10		MCM67A618–12		MCM67A618–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to End of Write	t_{AVEH}	9	—	10	—	13	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	7	—		
DL High to $\overline{E}$ High	t_{DLHEH}	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\overline{E}$ High	t_{ALLEH}	2	—	2	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EHDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	9	—	10	—	13	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		7
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		8, 9

NOTES:
1. $\overline{W}$ refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION

(Order by Full Part Number)

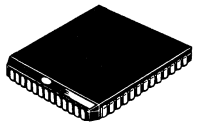
MCM	67A618	XX	XX
Motorola Memory Prefix	Part Number	Package (FN = PLCC)	Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)

Full Part Numbers — MCM67A618FN10 MCM67A618FN12 MCM67A618FN15

MCM67A618A

Product Preview

64K x 18 Bit Asynchronous/ Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67A618A is a 1,179,648 bit latched address static random access memory organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 64K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high the device can be used as an asynchronous SRAM. When latch enables are low the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data–in hold time in a simple fashion.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

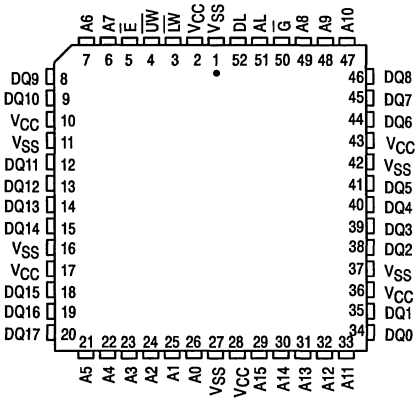
Six pair of power and ground pins have been utilized and placed on the package for maximum performance.

The MCM67A618A will be available in a 52–pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 10/12/15 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENT

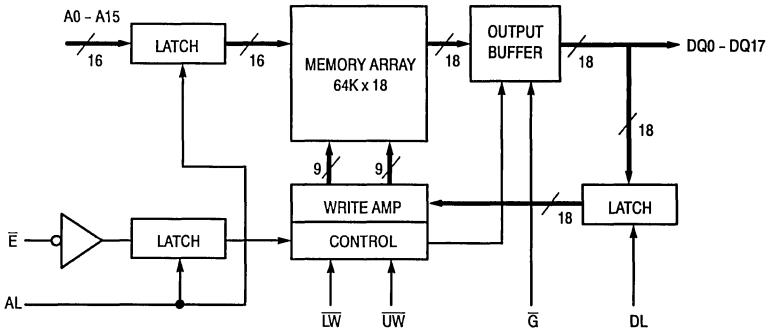


PIN NAMES	
A0 – A15	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High–Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High–Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High–Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High–Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High–Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data–in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Standby Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA10} I_{CCA12} I_{CCA15}	—	290 280 265	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{SB1}	—	95	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	7		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

4

AC TEST LOADS

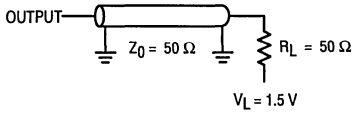


Figure 1A

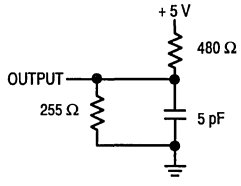
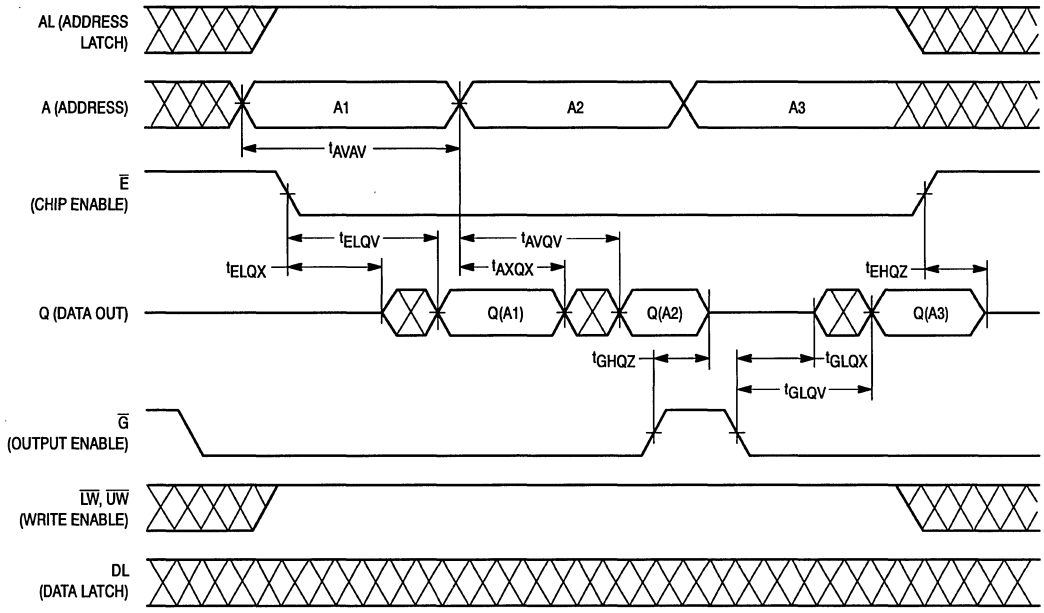


Figure 1B

ASYNCHRONOUS READ CYCLES

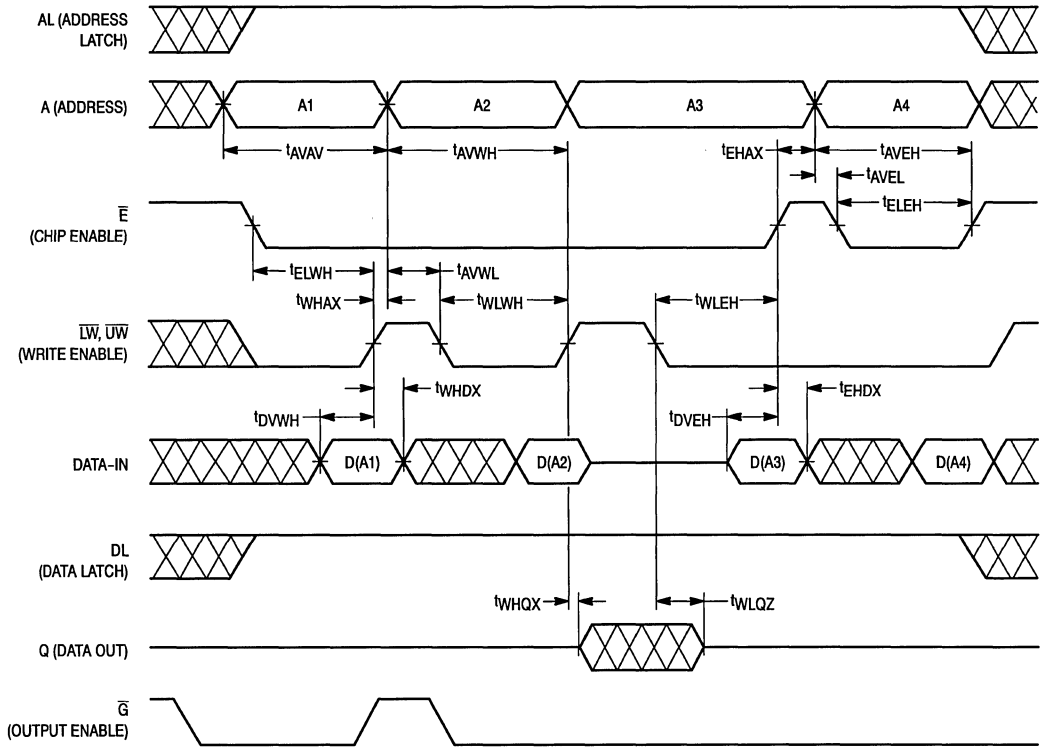


ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter		Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Times		t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:	Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—	ns	
	Address Valid to $\overline{E}$ High	t_{AVEH}	9	—	10	—	13	—		
	Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
	Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
	DataValid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
	Data Valid $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
Hold Times:	$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	ns	
	$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
	$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
	$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width:	Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—	ns	
	Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
	Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		5
	Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		6
	Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		5, 6
Output Buffer Control:	$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	7
	$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		7, 8

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE



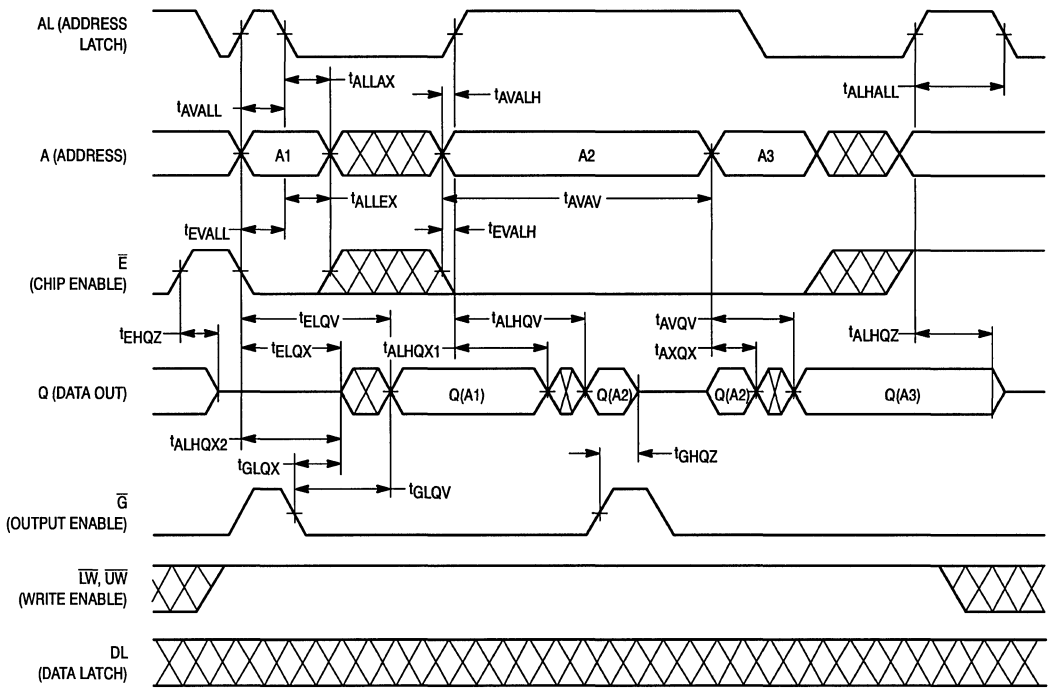
4

LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	10	—	12	—	15	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	10	—	12	—	15		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	10	—	12	—	15		3
AL High to Output Valid	t_{ALHQV}	—	10	—	12	—	15		4
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	7		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	2	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	3	—	3	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	3	—	3	—		
$\overline{E}$ High to Output High–Z	t_{EHQZ}	2	5	2	6	2	9		
AL High to Output High–Z	t_{ALHQZ}	2	5	2	6	2	9		
$\overline{G}$ High to Output High–Z	t_{GHQZ}	2	5	2	6	2	7		

NOTES:
1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{ALHQZ} is less than t_{ALHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



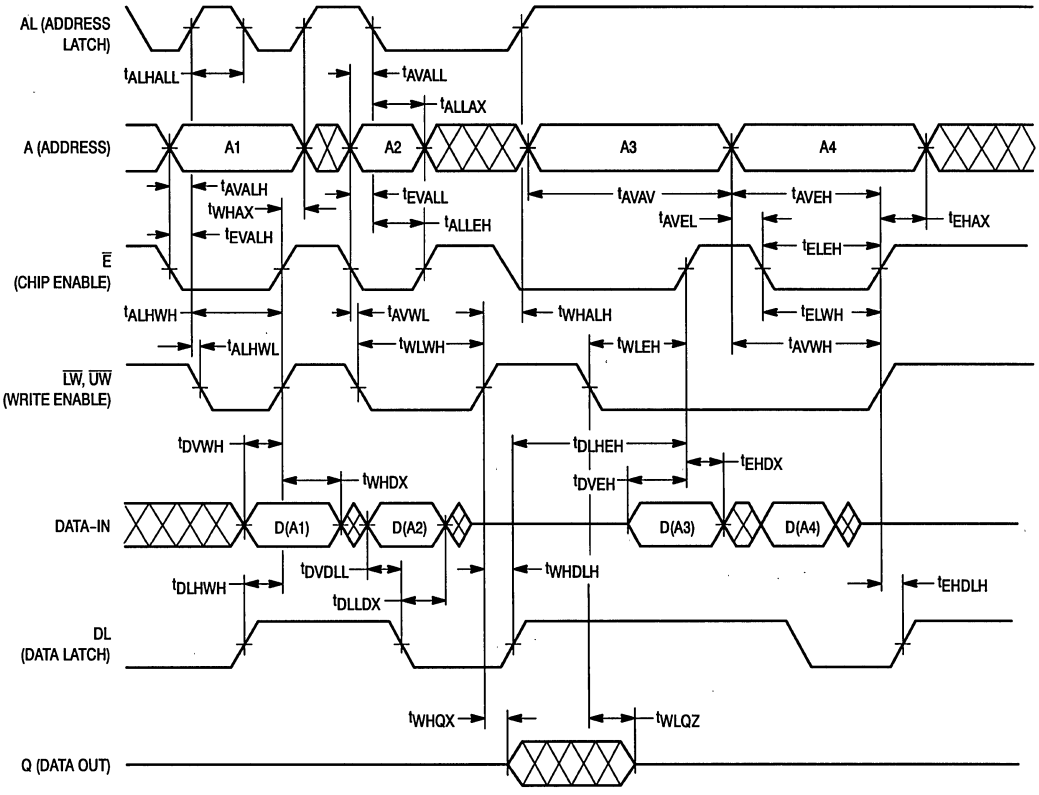
4

LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618A–10		MCM67A618A–12		MCM67A618A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	10	—	12	—	15	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	13	—		
Address Valid to End of Write	t_{AVEH}	9	—	10	—	13	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	7	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	5	—	6	—	7	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	7	—		
DL High to $\overline{E}$ High	t_{DLHEH}	5	—	6	—	7	—		
Hold Times:								ns	
AL Low to $\overline{E}$ High	t_{ALLEH}	2	—	2	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	2	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EHDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	9	—	10	—	13	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	9	—	10	—	13	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	8	—	9	—	12	—		
Write Pulse Width	t_{WLEH}	9	—	10	—	13	—		6
Enable to End of Write	t_{ELWH}	9	—	10	—	13	—		7
Enable to End of Write	t_{ELEH}	9	—	10	—	13	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	3	—	3	—		8
$\overline{W}$ Low to Output High–Z	t_{WLQZ}	0	5	0	6	0	9		8, 9

NOTES:
1. W (write) refers to either one or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

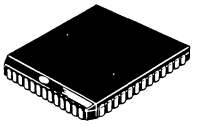
MCM 67A618A XX XX

- MCM — Motorola Memory Prefix
- 67A618A — Part Number
- XX — Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- XX — Package (FN = PLCC)

Full Part Numbers — MCM67A618AFN10 MCM67A618AFN12 MCM67A618AFN15

MCM67D709

128K x 9 Bit Synchronous Dual I/O Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67D709 is a 1,179,648 bit synchronous static random access memory organized as 131,072 words of 9 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. The device integrates a 128K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers and two sets of output latches. This device has increased output drive capability supported by multiple power pins.

Asynchronous inputs include the processor output enable ($\overline{POE}$) and the system output enable ($\overline{SOE}$).

The address inputs (A0 – A16) are synchronous and are registered on the falling edge of clock (K). Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of clock (K). Writes to the RAM are self–timed.

All data inputs/outputs, PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three–state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

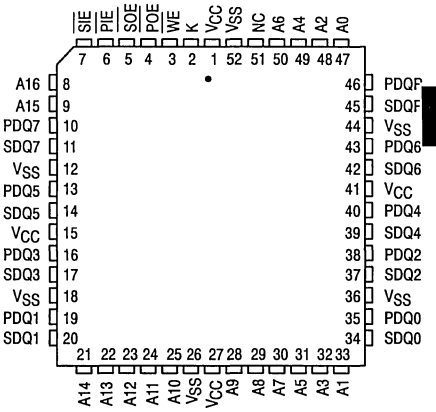
This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

The MCM67D709's dual I/Os can be used in x9 separate I/O applications. Common I/Os PDQ0 – 7, PDQP and SDQ0 – 7, SDQP can be treated as either inputs (D) or outputs (Q) depending on the state of the control pins. In order to dedicate PDQ0 – 7, PDQP as data (D) inputs and SDQ0 – 7, SDQP as outputs (Q), tie $\overline{SIE}$ and $\overline{POE}$ high. $\overline{SOE}$ becomes the asynchronous $\overline{G}$ for the outputs. $\overline{PIE}$ will need to track $\overline{W}$ for proper write/read operations.

This device is ideally suited for pipelined systems and systems with multiple data buses and multi–processing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 5% Power Supply
- 88110/88410 Compatibility: –16/60 MHz, –20/50 MHz
- Self–Timed Write Cycles
- Clock Controlled Output Latches
- Address and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three–State Outputs
- 3.3 V I/O Compatible
- High Board Density 52 Lead PLCC Package
- Can be used as Separate I/O x9 SRAM

PIN ASSIGNMENTS



PIN NAMES

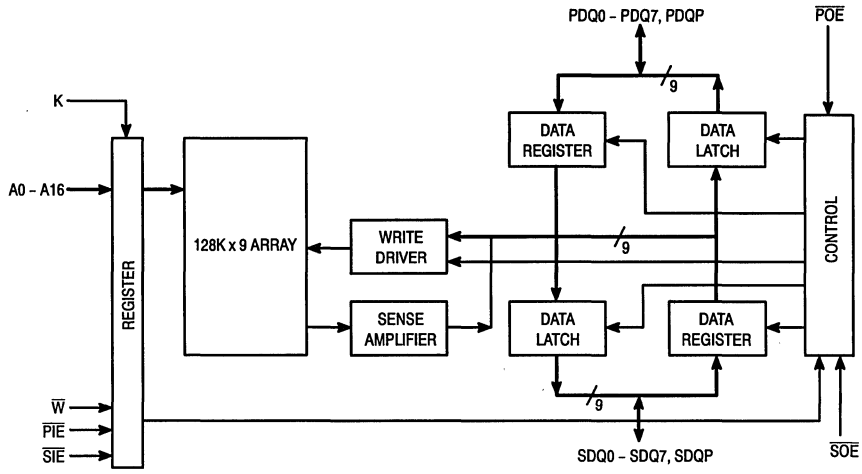
A0 – A16	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
PDQ0 – PDQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0 – SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

4

REV2
5/95

BLOCK DIAGRAM



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FUNCTIONAL TRUTH TABLE (See Notes 1 and 2)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ0 – PDQ7, PDQP Output	SDQ0 – SDQ7, SDQP Output	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High–Z	3
1	1	1	1	0	Read	Copy Back	High–Z	Data Out	3
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	3
1	X	X	1	1	Read	NOP	High–Z	High–Z	
X	0	0	X	X	N/A	NOP	High–Z	High–Z	2, 4
0	0	1	1	1	Write	Processor Write Hit	Data In	High–Z	2, 5
0	1	0	1	1	Write	Allocate	High–Z	Data In	2, 5
0	0	1	1	0	Write	Write Through	Data In	Stream Data	2, 6
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	2, 6
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	2, 6
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	2, 6
0	1	1	X	X	N/A	NOP	High–Z	High–Z	4
X	0	1	0	0	N/A	Invalid	Data In	Stream	2, 7
X	0	1	0	1	N/A	Invalid	Data In	High–Z	2, 7
X	1	0	0	0	N/A	Invalid	Stream	Data In	2, 7
X	1	0	1	0	N/A	Invalid	High–Z	Data In	2, 7

NOTES:

1. A '0' represents an input voltage ≤ V_{IL} and a '1' represents an input voltage ≥ V_{IH}. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAMs behavior is not specified.
2. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don't care, and the corresponding outputs are High–Z.
3. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
4. No RAM cycle is performed.
5. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0 – PDQ7 and PDQP or SDQ0 – SDQ7 and SPDQ), and written into the RAM.
6. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
7. Data contention will occur.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM67D709–16: t_{KHKH} = 16 ns MCM67D709–20: t_{KHKH} = 20 ns	I_{CCA}	— —	280 260	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except I/Os)	C_{in}	5	6	pF
Input/Output Capacitance (PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, SDQP)	C_{out}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Measurement Timing Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	Processor Frequency: 60 MHz MCM67D709–16 Min	60 MHz MCM67D709–16 Max	50 MHz MCM67D709–20 Min	50 MHz MCM67D709–20 Max	Unit	Notes
Read Cycle Time Clock High to Clock High	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Clock High to Output Valid	t_{KHQV}	—	6	—	7.5	ns	3
Clock (K) High to Output Low Z After Write	t_{KHQX1}	0	—	0	—	ns	
Output Hold from Clock High	t_{KHQX2}	2	—	3	—	ns	3, 4
Setup Times: A	t_{AVKL}	2	—	2	—	ns	
$\overline{W}$	t_{WHKH}	2		2			
$\overline{PIE}$	t_{PIEHKH}	2		2			
$\overline{SIE}$	t_{SIEHKH}	2		2			
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}	2		2			
$\overline{PIE}$	t_{KHPIEX}	2		2			
$\overline{SIE}$	t_{KHSIEX}	2		2			
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}	0	6	0	8	ns	4
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	2	—	5	—	ns	4
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	4
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. K must be at a high level for outputs to transition.
4. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

AC SPEC LOADS

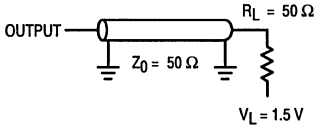


Figure 1A

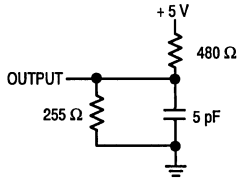
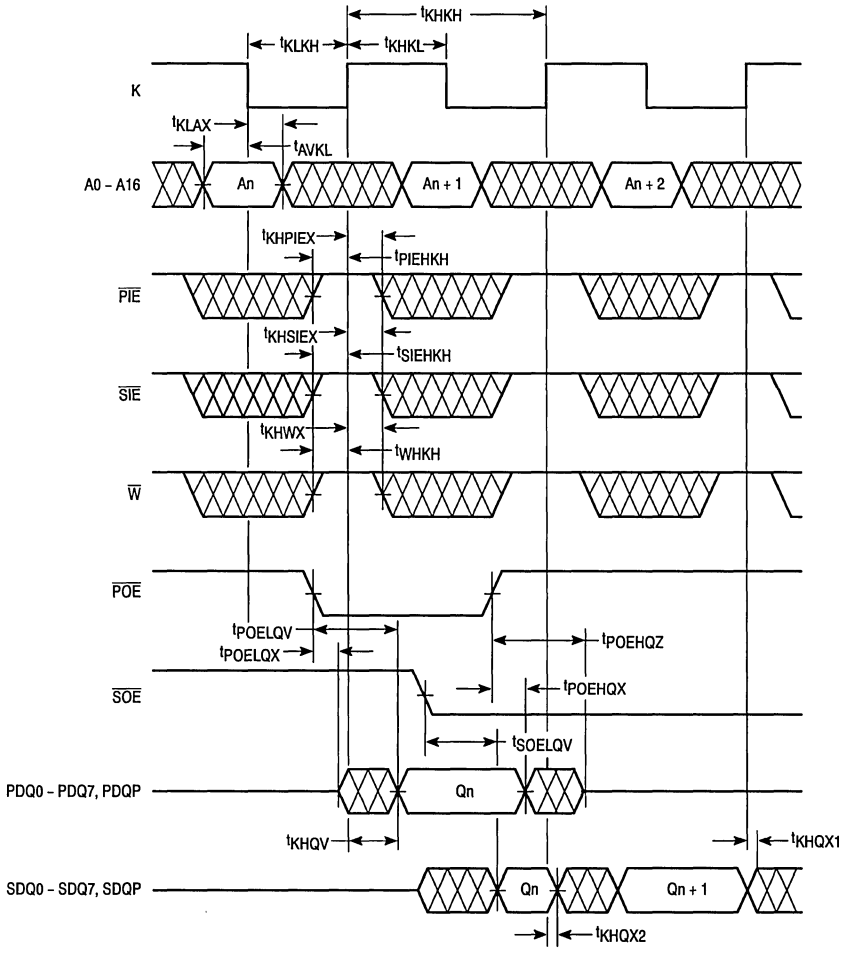


Figure 1B

READ CYCLE (See Note)



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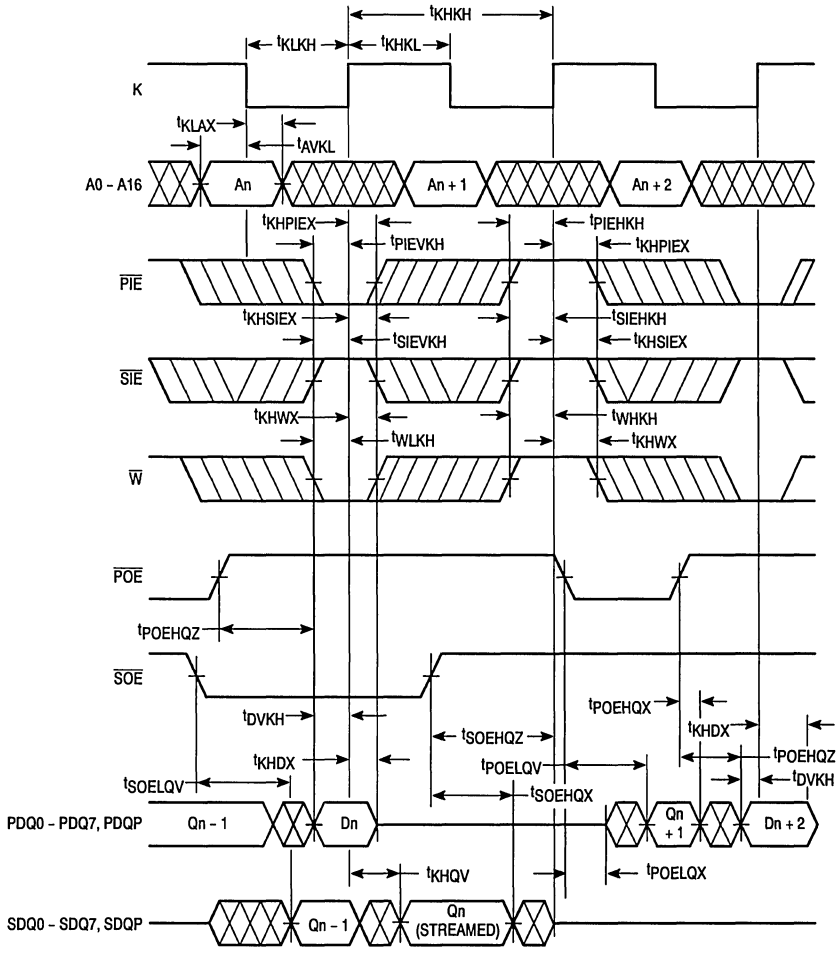
WRITE THROUGH – READ – WRITE (See Note 1)

Parameter	Symbol	Processor Frequency	60 MHz MCM67D709–16 Min	60 MHz MCM67D709–16 Max	50 MHz MCM67D709–20 Min	50 MHz MCM67D709–20 Max	Unit	Notes
Write Cycle Times	t_{KHKH}		16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}		5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}		7	—	7	—	ns	
Clock High to Output High–Z ($\overline{W}$ = V_{IL} and $\overline{SIE}$ = $\overline{PIE}$ = V_{IH})	t_{KHQZ}		—	8	—	8	ns	3, 4
Setup Times: A	t_{AVKL}		2	—	2	—	ns	
$\overline{W}$	t_{WLKH}		2		2			
$\overline{PIE}$	t_{PIEVKH}		2		2			
$\overline{SIE}$	t_{SIEVKH}		2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}		2		2			
Hold Times: A	t_{KLAX}		2	—	2	—	ns	
$\overline{W}$	t_{KHWX}		2		2			
$\overline{PIE}$	t_{KHPIEX}		2		2			
$\overline{SIE}$	t_{KHSIEX}		2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}		2		2			
Write with Streaming ($\overline{PIE}$ = $\overline{SOE}$ = V_{IL} or $\overline{SIE}$ = $\overline{POE}$ = V_{IL}) Clock High to Output Valid	t_{KHQV}		—	5	—	7	ns	5
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}		0	6	0	8	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}		2	—	5	—	ns	6
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}		0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}		—	5	—	6	ns	

NOTES:
1. A write is performed with $\overline{W}$ = V_{IL} for the specified setup and hold times and either $\overline{PIE}$ = V_{IL} or $\overline{SIE}$ = V_{IL}. If both $\overline{PIE}$ = V_{IL} and $\overline{SIE}$ = V_{IL} or $\overline{PIE}$ = V_{IH} and $\overline{SIE}$ = V_{IH}, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. K must be at a high level for the outputs to transition.
4. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested.
5. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.
6. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

WRITE THROUGH — READ — WRITE



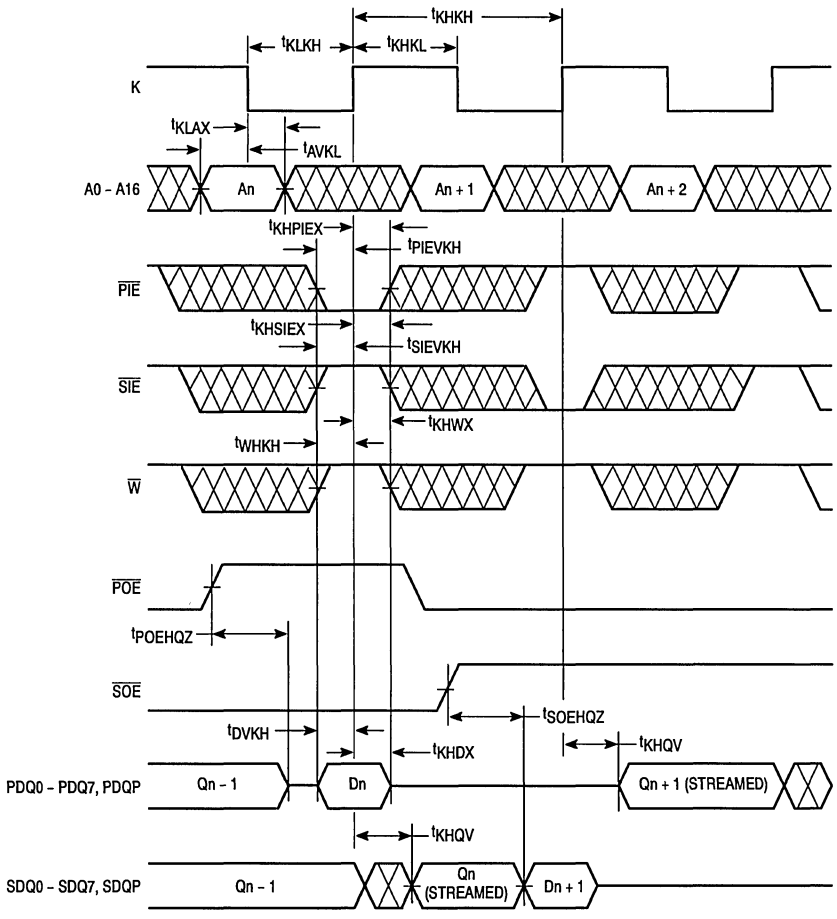
4

STREAM CYCLE (See Note 1)

Parameter	Symbol	Processor Frequency	60 MHz MCM67D709–16		50 MHz MCM67D709–20		Unit	Notes
			Min	Max	Min	Max		
Stream Cycle Time	t_{KHKH}		16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}		5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}		7	—	7	—	ns	
Stream Access Time	t_{KHQV}		—	6	—	7	ns	
Setup Times: A	t_{AVKL}		2	—	2	—	ns	
$\overline{W}$	t_{WHKH}		2		2			
$\overline{PIE}$	t_{PIEVKH}		2		2			
$\overline{SIE}$	t_{SIEVKH}		2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}		2		2			
Hold Times: A	t_{KLAX}		2	—	2	—	ns	
$\overline{W}$	t_{KHWX}		2		2			
$\overline{PIE}$	t_{KHPIEX}		2		2			
$\overline{SIE}$	t_{KHSIEX}		2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}		2		2			
Output Enable High to Q High–Z	t_{POEHQZ} t_{SOEHQZ}		0	6	0	8	ns	3
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}		0	—	0	—	ns	3
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}		—	5	—	6	ns	

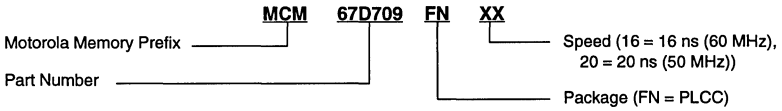
NOTES:
1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. Transition is measured ± 500 mV from steady–state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, for a given device.

STREAM CYCLE



4

ORDERING INFORMATION
(Order by Full Part Number)

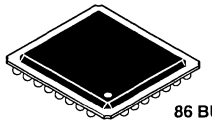


Full Part Numbers — MCM67D709FN16 MCM67D709FN20

4

MCM67Q709

128K x 9 Bit Separate I/O Synchronous Fast Static RAM



86 BUMP PBGA
CASE 896A–02

The Motorola MCM67Q709 is a 1,179,648 bit static random access memory, organized as 131,072 words of 9 bits. This device is fabricated using Motorola's high–performance silicon–gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A16), Data Input (D0 – D8), Data Output (Q0 – Q8), Write–Enable ($\overline{W}$), Chip–Enable ($\overline{E}$), and Output–Enable ($\overline{G}$), are registered in on the rising edge of Clock (K).

The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0–Q8) will be driven if $\overline{G}$ is registered low. The Transparent–Write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a Transparent Write (Write and Pass–Through). The input data is available at the ouputs on the next rising edge of clock (K).

The Pass–Through function is always enabled. $\overline{E}$ high disables the write to the array while allowing a pass through cycle to occur on the next rising edge of clock (K). Only a registered $\overline{G}$ high will three–state the outputs.

The MCM67Q709 is available in 86 bump surface mount PBGA (Plastic Ball Grid Array) package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time
- Boundary Scan Implementation
- PBGA package for high speed operation

PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D8	Data Inputs
Q0 – Q8	Data Outputs
K	Clock Input
SCK	Scan Clock Input
SE	Scan Enable
SDI	Scan Data Input
SDO	Scan Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENTS

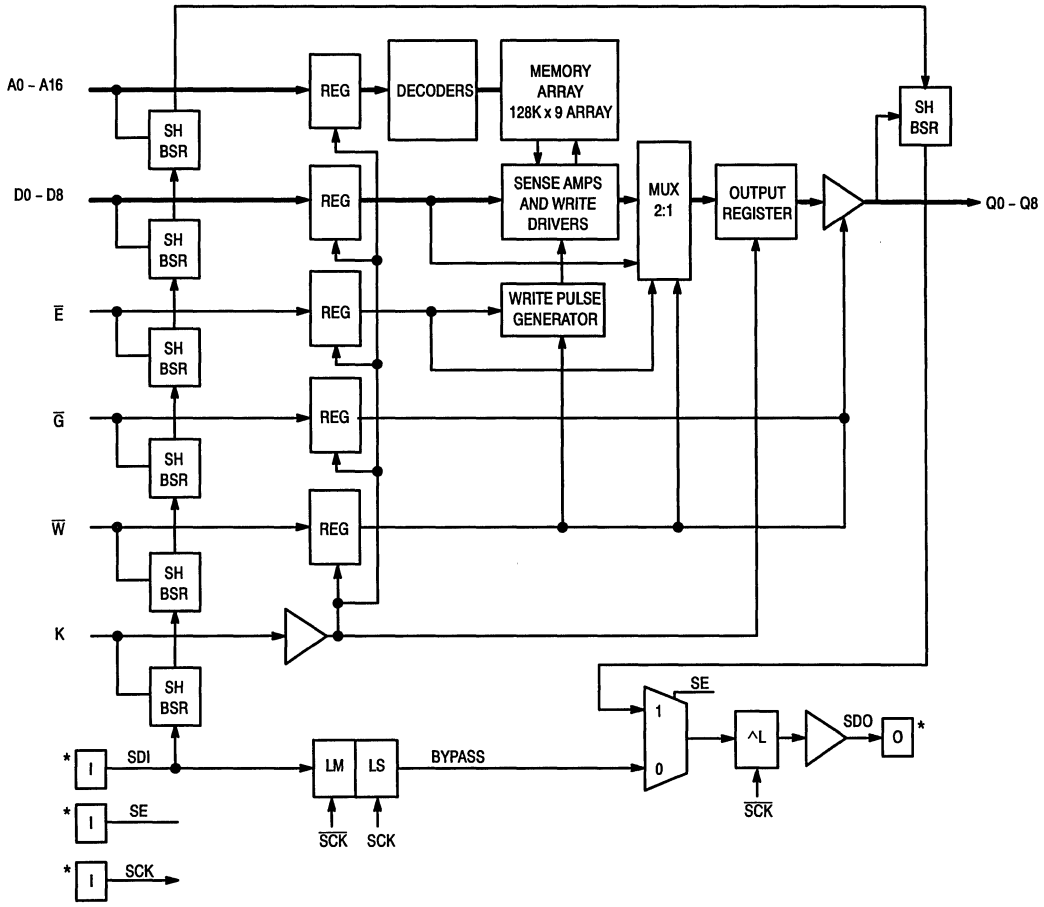
	1	2	3	4	5	6	7	8	9
A		$\overline{E}$	$\overline{W}$	V_{CC}	SDI	SDO	A4	A0	
B	A16	A14	$\overline{G}$	K	V_{SS}	A6	A2	V_{SS}	D8
C	D7	A15	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q8	V_{SS}
D	V_{SS}	Q7	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q6	D6
E	D5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}
F	V_{CC}	Q5	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D4	Q4
G	D3	Q3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D2	Q2
H	V_{SS}	D1	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D0	V_{SS}
J	Q1	A12	A10	V_{SS}	A9	A8	A5	A1	Q0
K		A13	A11	SCK	V_{CC}	SE	A7	A3	

TOP VIEW 86 BUMP Not to Scale

4

REV 2
4/95

BLOCK DIAGRAM



NOTES:

1. Bypass mode is entered with SE low and SCK cycled.
2. SH BSR = Shadow Bypass Scan Register.
3. 39 bumps used in Boundary Scan. V_{SS}, V_{CC}, NC, SDI, SDO, SE, and SCK not used in Scan Path.
4. SDO Output Sequence A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, K.

*Four added test pins.

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ ($t_n + 1$)	Mode	D0 – D8 (t_n)	Q0 – Q8 ($t_n + 1$)	V_{CC} Current
L	L	L	Write and Pass Thru	Valid	D0 – D8 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass Thru	Valid	D0 – D8 (t_n)	I_{CC}
		H	NOP	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	MCM67Q709–10 ns MCM67Q709–12 ns	I_{CCA}	— —	230 220	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67Q709–10		MCM67Q709–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	
Setup Times: A	t_{AVKH}	2	—	2	—	ns	3
$\overline{W}$	t_{WVKH}						
$\overline{E}$	t_{EVKH}						
$\overline{G}$	t_{GVKH}						
D0 – D8	t_{DVKH}						
Hold Times: A	t_{KHAX}	1	—	1	—	ns	3
$\overline{W}$	t_{KHWX}						
$\overline{E}$	t_{KHEX}						
$\overline{G}$	t_{KHGX}						
D0 – D8	t_{KHDX}						

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

AC SPEC LOADS

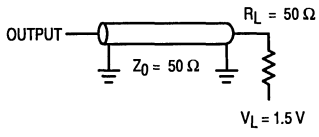


Figure 1A

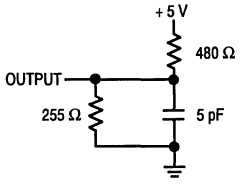
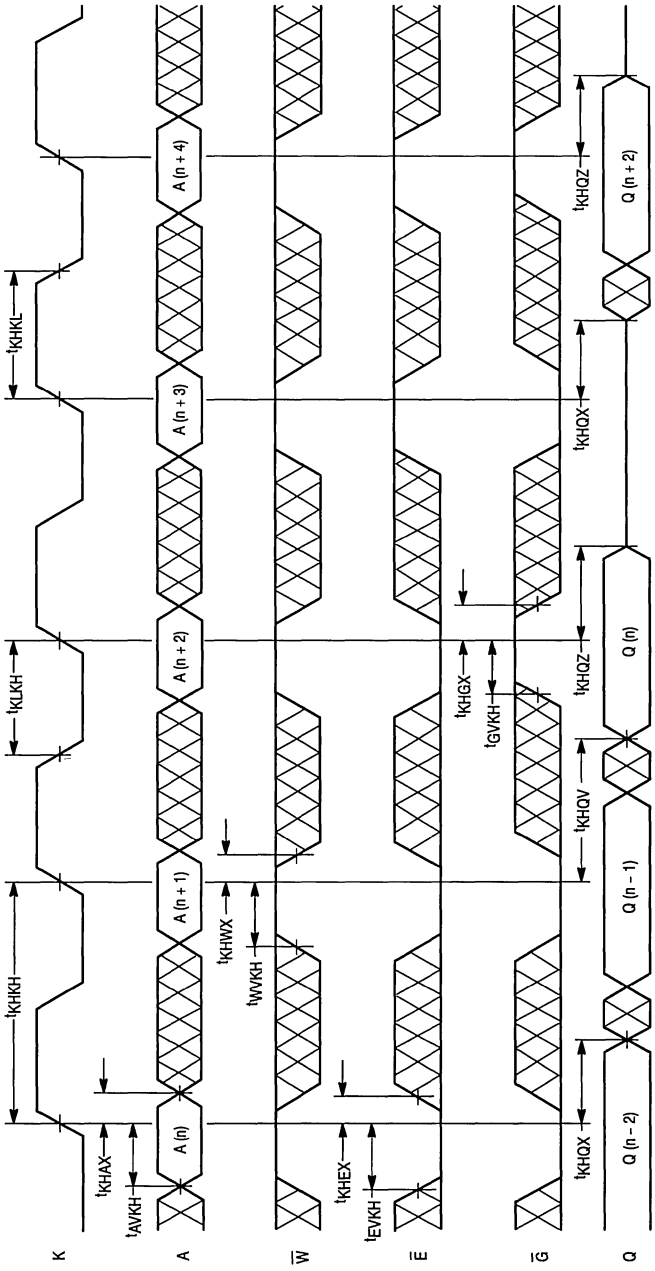


Figure 1B

READ CYCLE TIMING



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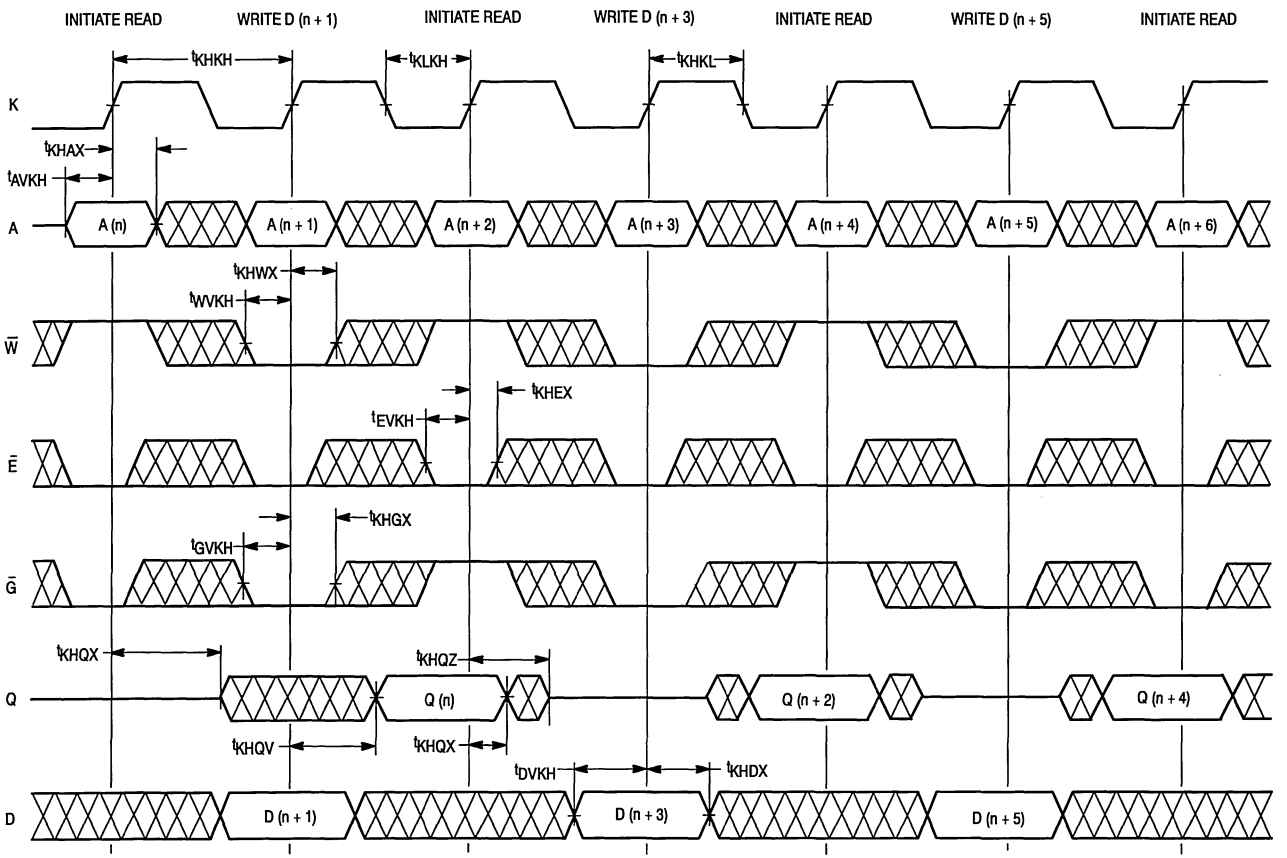
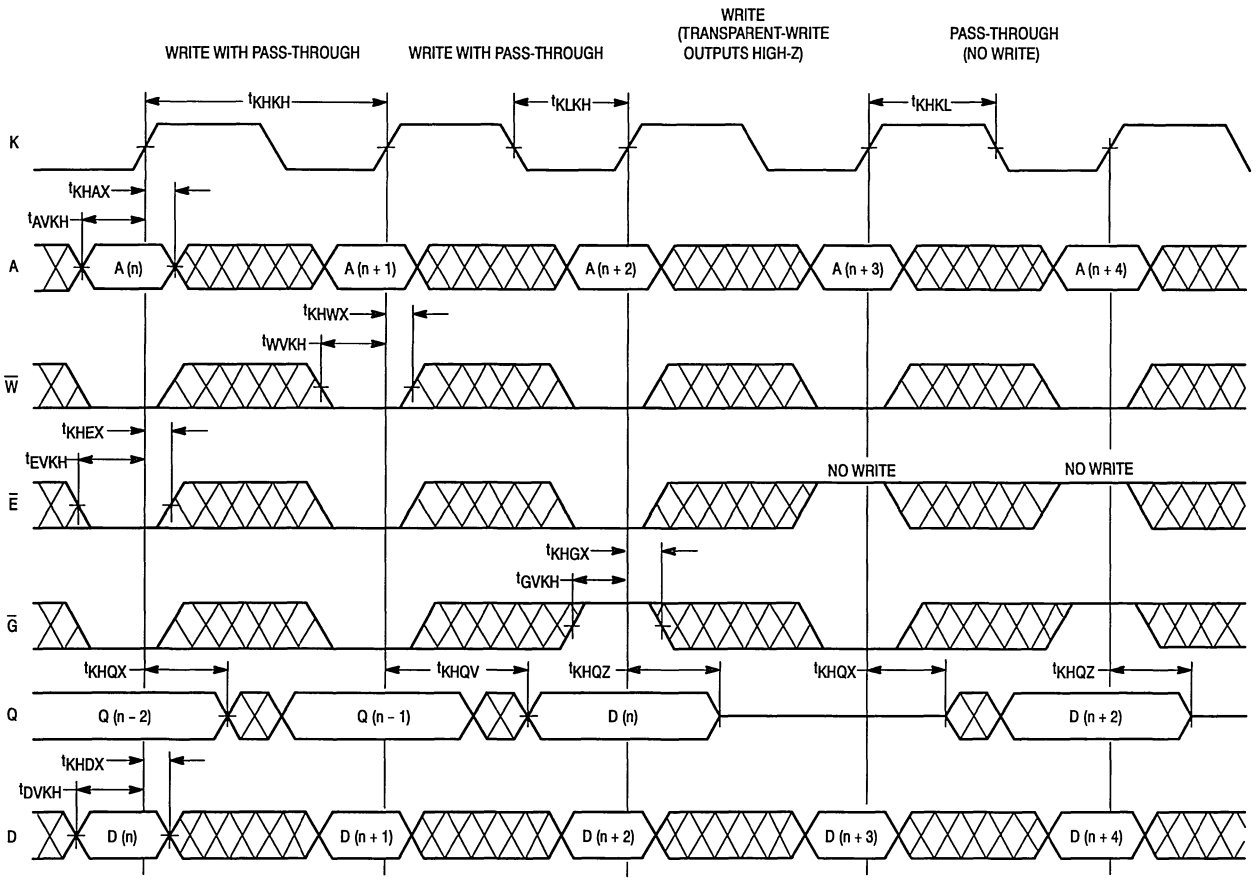
COMBINATION READ/WRITE CYCLE TIMING



TRANSPARENT-WRITE AND PASS-THROUGH CYCLE TIMING



BOUNDARY SCAN CYCLE TIMING

Parameter	Symbol	MCM67Q709–10		MCM67Q709–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CHCH2}	100	—	100	—	ns	
Clock High Pulse Width	t_{CHCL2}	40	—	40	—	ns	
Clock Low Pulse Width	t_{CLCH2}	40	—	40	—	ns	
Scan Mode Setup Time	t_{SS}	10	—	10	—	ns	1
Bypass Mode Setup Time	t_{BS}	10	—	10	—	ns	2
Scan Mode Recovery Time	t_{SR}	100	—	100	—	ns	3
SCK Low to SE Hold High	t_{CLMH}	10	—	10	—	ns	4
SE High to SCK High Setup	t_{MHCH}	10	—	10	—	ns	5
SCK High to SE Low Hold Time	t_{CHML}	10	—	10	—	ns	6
SDI Valid to SCK High Setup	t_{IVCH}	10	—	10	—	ns	
SCK High to SDI Don't Care	t_{CHIX}	10	—	10	—	ns	
SCK Low to SDO Valid	t_{CLOV}	—	20	—	20	ns	

NOTES:
1. The minimum delay required between ending normal operation and beginning scan operations.
2. The minimum delay required between ending Shift Mode and beginning Bypass Mode.
3. The minimum delay required before restarting normal RAM operation.
4. The minimum delay required before executing a Parallel Load operation.
5. The minimum delay required between a Parallel Load operation and a Shift.
6. Minimum Shift command hold time.

4

BOUNDARY SCAN

OVERVIEW

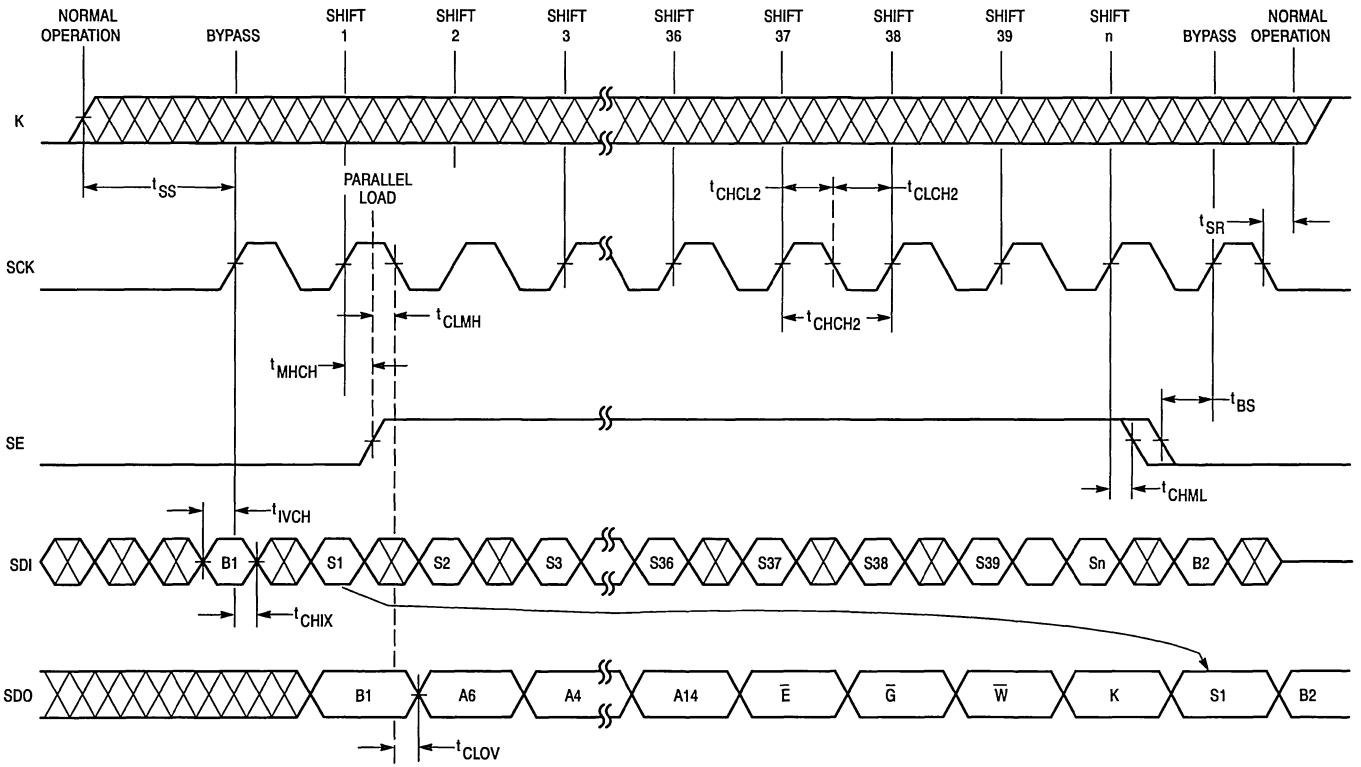
Boundary scan is a simple, non–intrusive scheme that allows verification of electrical continuity for each of a clocked RAM's logically active inputs and I/Os without adversely affecting RAM performance. Boundary scan allows the user to monitor the logic levels applied to each signal I/O on the RAM, and to shift them out in a serial bit stream.

OPERATION

Boundary scan requires four signal pins for implementation: Scan Data In (SDI), Scan Data Out (SDO), Scan Clock (SCK, active high), and Scan Enable (SE, active high).

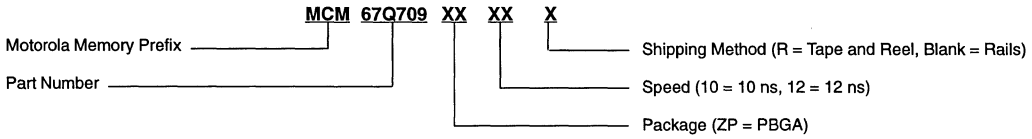
Boundary scan provides three modes of operation: (1) normal RAM operation, (2) scan, and (3) bypass. For normal RAM operation SCK and SE must be held low. The RAM will always return to normal operation immediately after the RAM receives a rising edge of the RAM input clock (K) with SCK and SE held low. To enter scan mode, SCK is activated. The first rising edge of SCK is used to latch in the data on the scan registers. SE is then driven high to disable additional input data from entering the scan registers. Every falling edge of SCK serially shifts data through the scan registers and onto the SDO pin. To enter bypass mode simply exercise SCK with SE held low. In this mode SDI is sampled on the rising edge of SCK. The level found on SDI is then driven out on SDO on the next falling edge of SCK.

BOUNDARY SCAN TIMING DIAGRAM



B1 and B2 = Bypass Serial Data from outside source
S1 – Sn + 1 = Serial Scan Data from outside source
S1 – Sn = RAMs Input Register contents
Scan Order is "A6, A4, A2, A0, D8, Q8, D6, Q6, D4, Q4, D2, Q2, D0, Q0, A1, A3, A5, A7, A8, A9, A10, A11, A12, A13, Q1, D1, Q3, D3, Q5, D5, Q7, D7, A15, A16, A14, $\overline{E}$, $\overline{G}$, $\overline{W}$, K"

ORDERING INFORMATION
(Order by Full Part Number)

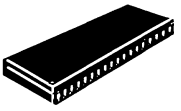


Full Part Numbers — MCM67Q709ZP10 MCM67Q709ZP12
MCM67Q709ZP10R MCM67Q709ZP12R

4

256K x 4 Bit Separate I/O Synchronous Fast Static RAM

MCM67Q804



WJ PACKAGE
400 MIL SOJ
CASE 893–01

The MCM67Q804 is a 1,048,576 bit static random access memory, organized as 262,144 x 4 bits. This device is fabricated using Motorola's high–performance silicon–gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM. It also features transparent–write and data pass–through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A17), Data Input (D0 – D3), Data Output (Q0 – Q3), Write–Enable ($\overline{W}$), Chip–Enable ($\overline{E}$), and Output–Enable ($\overline{G}$), are registered in on the rising edge of Clock (K).

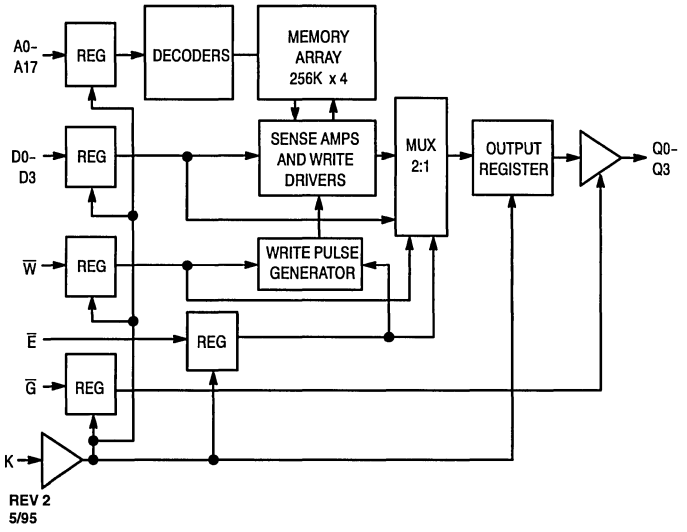
The control pins ($\overline{E}$, $\overline{W}$, $\overline{G}$) function differently in comparison to most synchronous SRAMs. This device will not deselect with $\overline{E}$ high. The RAM remains active at all times. If $\overline{E}$ is registered high, the output pins (Q0–Q8) will be driven if $\overline{G}$ is registered low. The Transparent–Write feature allows the output data to track the input data. $\overline{E}$, $\overline{G}$, and $\overline{W}$ must be asserted to perform a Transparent Write (Write and Pass–Through). The input data is available at the ouputs on the next rising edge of clock (K).

The pass–through function is always enabled. $\overline{E}$ high disables the write to the clock (K). only a clocked $\overline{G}$ high will three–state the outputs.

This device is available in a 400 mil, 36–lead surface–mount SOJ package.

- Single 5 V ± 5% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent–Write and Pass–Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time

BLOCK DIAGRAM



REV 2
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PIN ASSIGNMENT

NC	1	36	A17
A0	2	35	A16
A1	3	34	A15
A2	4	33	A14
A3	5	32	A13
$\overline{E}$	6	31	$\overline{G}$
D0	7	30	D3
Q0	8	29	Q3
V_{CC}	9	28	V_{SS}
V_{SS}	10	27	V_{CC}
Q1	11	26	Q2
D1	12	25	D2
$\overline{W}$	13	24	K
A4	14	23	A12
A5	15	22	A11
A6	16	21	A10
A7	17	20	A9
NC	18	19	A8

PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D3	Data Inputs
Q0 – Q3	Data Outputs
K	Clock Input
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

4

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ (t_{n+1})	Mode	D0 – D3	Q0 – Q3 (t_{n+1})	V_{CC} Current
L	L	L	Write and Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	Write	Valid	High–Z	I_{CC}
H	L	L	Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	NOP	Don't Care	High–Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High–Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)		V_{CC}	4.75	5.25	V
Input High Voltage		V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage		V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	MCM67Q804–10 ns MCM67Q804–12 ns	I_{CCA}	— —	180 170	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	3.3	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67Q804–10		MCM67Q804–12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	2	—	2	—	ns	
Clock High to Data Output High–Z	t_{KHQZ}	—	5	—	6	ns	
Setup Times: A $\overline{W}$ $\overline{E}$ $\overline{G}$ D0 – D3	t_{AVKH} t_{WVKH} t_{EVKH} t_{GVKH} t_{DVKH}	2	—	2	—	ns	3
Hold Times: A $\overline{W}$ $\overline{E}$ $\overline{G}$ D0 – D3	t_{KHAX} t_{KHWX} t_{KHEX} t_{KHGX} t_{KHDX}	1	—	1	—	ns	3

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

AC SPEC LOADS

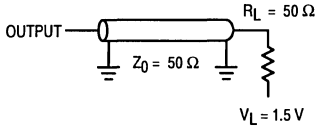

Figure 1A

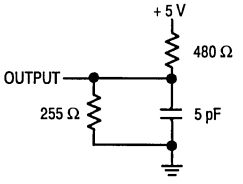

Figure 1B

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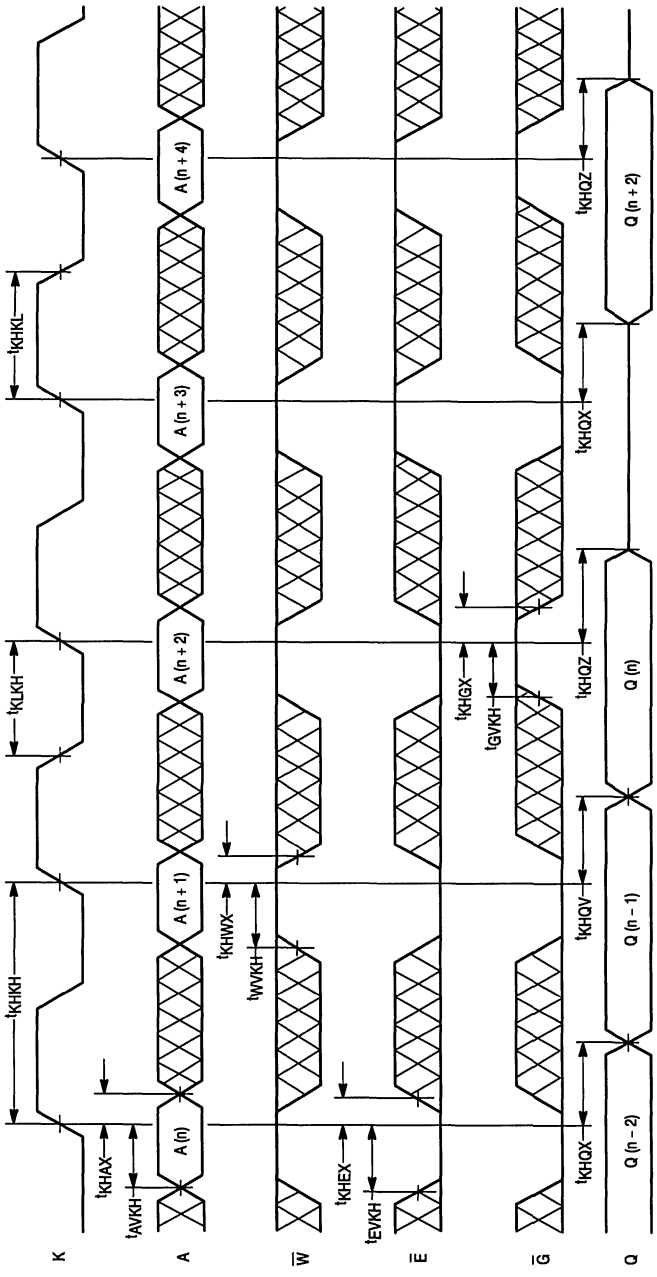
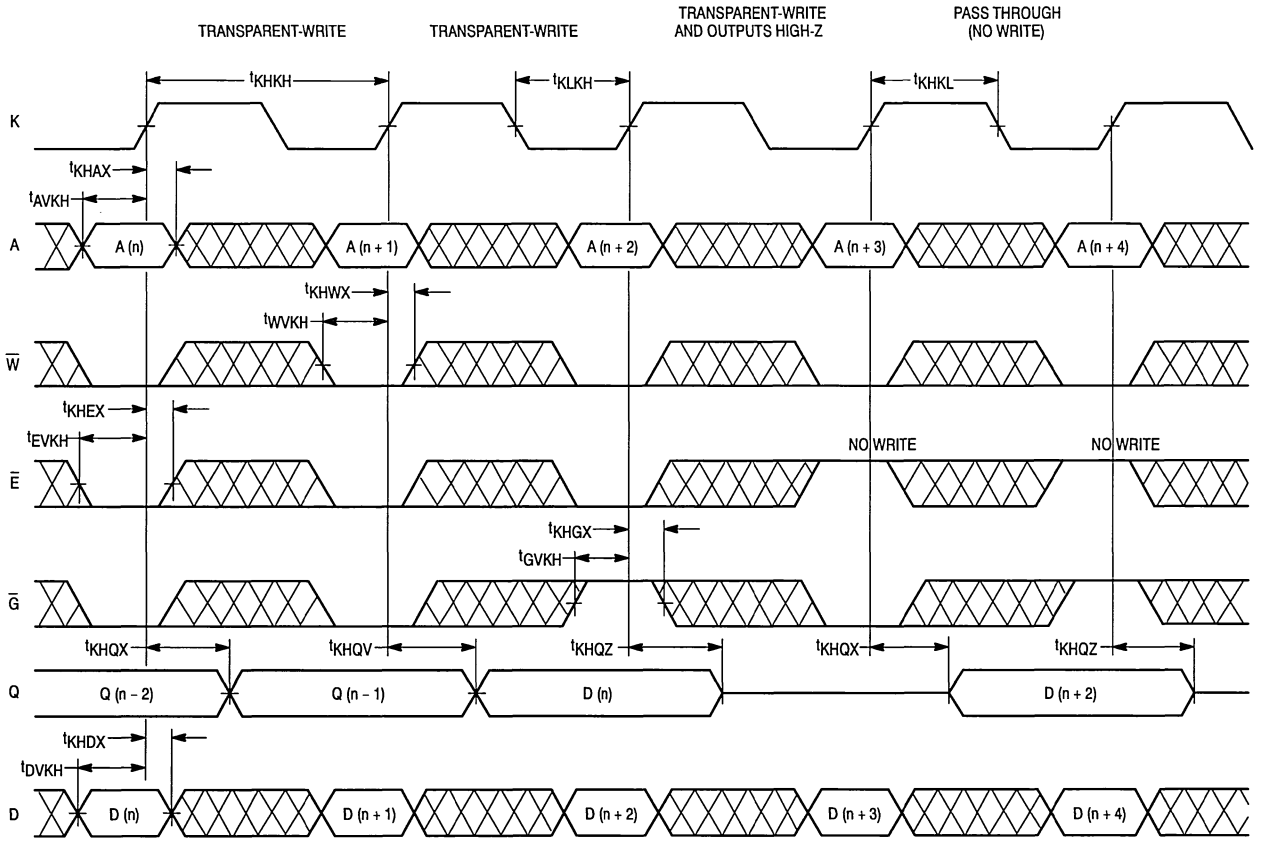
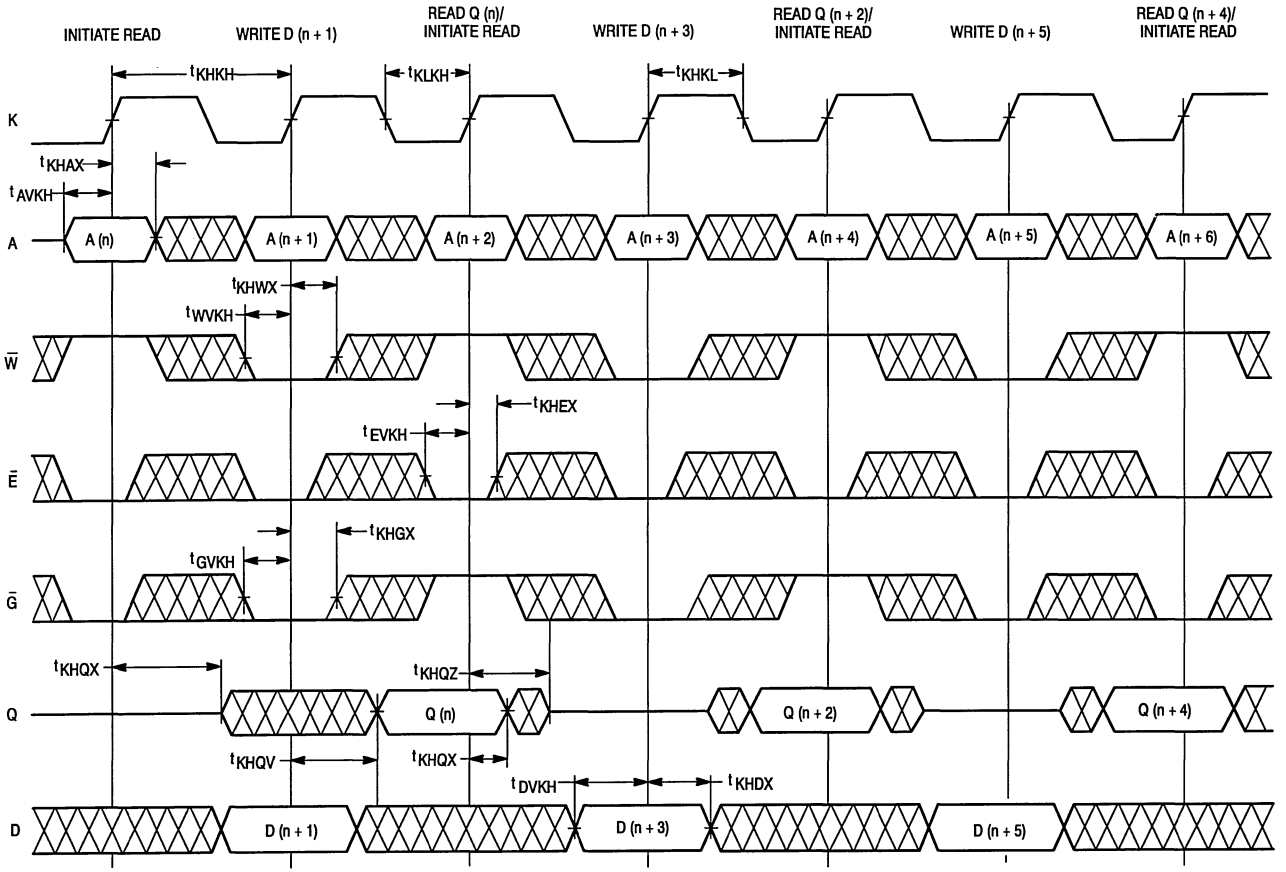
READ CYCLE TIMING



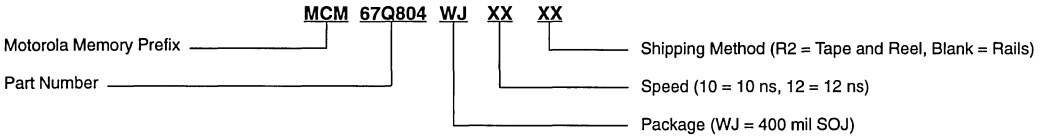
TRANSPARENT WRITE AND PASS–THROUGH CYCLE TIMING



COMBINATION READ/WRITE CYCLE TIMING



ORDERING INFORMATION
(Order by Full Part Number)



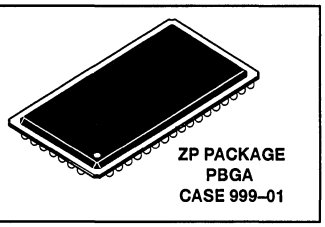
Full Part Numbers — MCM67Q804WJ10 MCM67Q804WJ12
MCM67Q804WJ10R2 MCM67Q804WJ12R2

4

MCM69T618

Product Preview

64K x 18 Bit Synchronous Pipelined Cache Tag RAM



ZP PACKAGE
PBGA
CASE 999–01

The MCM69T618 is a 1M bit synchronous fast static RAM with integrated tag compare function. It is designed to address tag RAM for 512KB, 1MB, or 2MB secondary cache as well as to be used as a data RAM for 512KB caches. This device is organized as 64K words of 18 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. It integrates input registers, output registers, tag comparators, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache tag RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), write enable ($\overline{SW}$) and chip enable ($\overline{SE}$) are all controlled through positive–edge–triggered noninverting registers. Data enable ($\overline{DE}$) is sampled on the rising clock edge while output enable ($\overline{G}$) and match output enable ($\overline{MG}$) are asynchronous.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, pipelined SRAM output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

Compare cycles begin as read cycles with output disabled so compare data can be loaded into the input register. The comparator compares the read data with the registered input data, and a match signal is generated. The match output is also stored by an output register and released to the match output buffer at the next rising edge of clock (K).

The MCM69T618 operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible.

- MCM69T618–5 = 5 ns Clock–to–Match / 10 ns cycle
  MCM69T618–6 = 6 ns Clock–to–Match / 12 ns cycle
  MCM69T618–7 = 7 ns Clock–to–Match / 13.3 ns cycle
- Single 3.3 V +10%, –5% Power Supply
- Pipelined Data Comparator
- Pipelined Chip Enable and Write Enable Control Signals
- 64K x 18 Organization Supports Up to 2MB Secondary Cache
- Synchronous Data Input Register Load Enable ($\overline{DE}$)
- Internally Self–Timed Write Cycle
- 119 Bump, 50 mil (1.27 mm) Pitch, 7 x 17 Plastic Ball Grid Array (PBGA)

PIN ASSIGNMENTS

	1	2	3	4	5	6	7
A	V_{CC}	SA	SA	NC	SA	SA	V_{CC}
B	NC	SE0	NC	NC	NC	$\overline{SE1}$	NC
C	NC	SA	SA	V_{CC}	SA	SA	NC
D	DQ9	NC	V_{SS}	NC	V_{SS}	DQ8	NC
E	NC	DQ10	V_{SS}	NC	V_{SS}	NC	DQ7
F	V_{CC}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ6	V_{CC}
G	NC	DQ11	NC	NC	V_{SS}	NC	DQ5
H	DQ12	NC	V_{SS}	$\overline{SW}$	V_{SS}	DQ4	NC
J	V_{CC}	V_{CC}	NC	V_{CC}	NC	V_{CC}	V_{CC}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ3
L	DQ14	NC	V_{SS}	$\overline{DE}$	NC	DQ2	NC
M	V_{CC}	DQ15	V_{SS}	NC	V_{SS}	NC	V_{CC}
N	DQ16	NC	V_{SS}	SA	V_{SS}	DQ1	NC
P	NC	DQ17	V_{SS}	SA	V_{SS}	NC	DQ0
R	$\overline{MG}$	SA	NC	V_{CC}	NC	SA	NC
T	NC	SA	SA	MATCH	SA	SA	NC
U	V_{CC}	NC	NC	NC	NC	NC	V_{CC}

TOP VIEW 119 BUMP PBGA Not to Scale

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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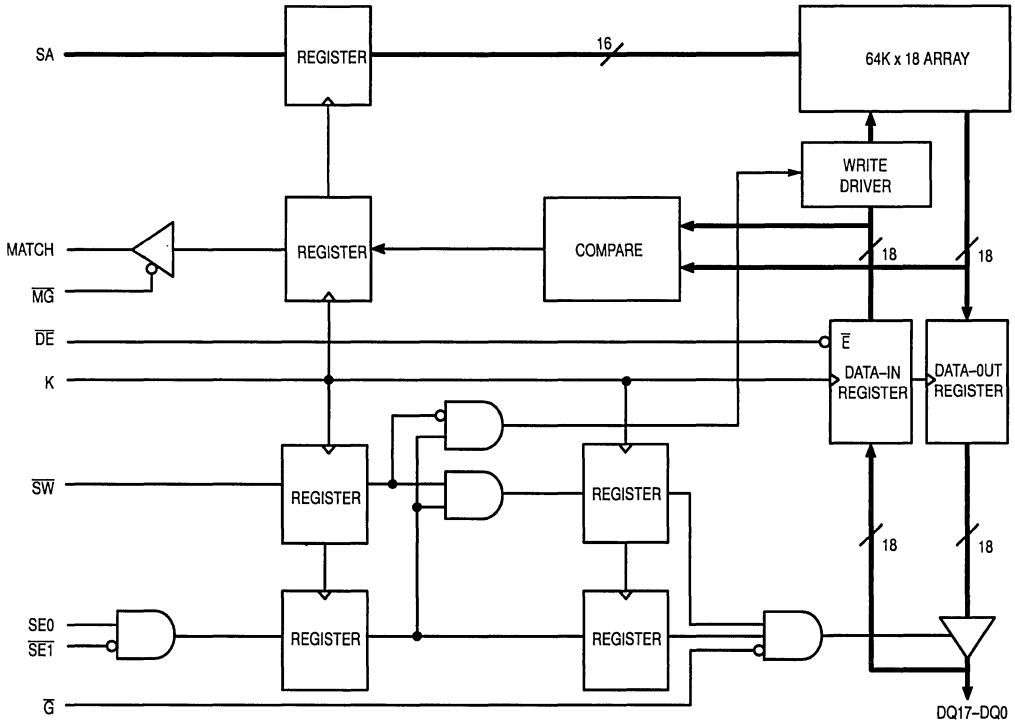
FUNCTIONAL BLOCK DIAGRAM



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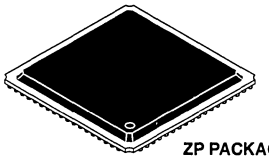
PIN DESCRIPTIONS

PBGA Pin Locations	Symbol	Type	Description
2A, 3A, 5A, 6A, 2C, 3C, 5C, 6C, 4N, 4P, 2R, 6R, 2T, 3T, 5T, 6T	SA	Input	Synchronous Address Inputs: Registered on the rising clock edge. The address pins select one of the 64K tag entries.
4K	K	Input	Clock: All the signals except $\overline{G}$ and $\overline{MG}$ are controlled by the clock.
4H	$\overline{SW}$	Input	Synchronous Write: Registered on the rising clock edge, active low. The $\overline{SW}$ input specifies whether a read or write cycle is to occur when the chip is enabled. A write command should not be issued within three cycles of a read command unless $\overline{G}$ is high or output drive contention may occur.
2B	SE0	Input	Synchronous Chip Enable: Registered on the rising clock edge, active high.
6B	$\overline{SE1}$	Input	Synchronous Chip Enable: Registered on the rising clock edge, active low.
4F	$\overline{G}$	Input	Output Enable: Asynchronous pin, active low. $\overline{G}$ must be low for read data to be output two cycles after a read command. If $\overline{G}$ is high, the data output will remain in high impedance even if a read command occurs internally.
6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 7P 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	DQx	I/O	Synchronous Data I/O: For write cycles, registered on the rising clock edge. Two cycles after a read command, the read data is output on the DQx pins provided that $\overline{G}$ is low. On the same cycle of a write command, the write data is input on the DQ signals.
4L	$\overline{DE}$	Input	Data Enable Input: Sampled on the rising clock edge, active low. The data input register is only updated when $\overline{DE}$ is low.
1R	$\overline{MG}$	Input	Match Output Enable: Asynchronous pin, active low. When $\overline{MG}$ is low, the MATCH output driver is on, otherwise the MATCH output driver is in high impedance.
4T	MATCH	Output	Two cycles after a compare cycle and if $\overline{MG}$ is low, MATCH will be high if the data presented to the DQ inputs matches the data stored in the RAM. MATCH will be low if the data does not match.
1A, 7A, 4C, 1F, 7F, 1J, 2J, 4J, 6J, 7J, 1M, 7M, 4R, 1U, 7U	V_{CC}	Supply	Power Supply: 3.3 V +10%, –5%. These pins act as thermal vias to pcb power plane.
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	V_{SS}	Supply	Ground: These pins act as thermal vias to pcb ground plane.
4A, 1B, 3B, 4B, 5B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 4E, 6E, 2F, 1G, 3G, 4G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 5L, 7L, 4M, 6M, 2N, 7N, 1P, 6P, 3R, 5R, 7R, 1T, 7T, 2U, 3U, 4U, 5U, 6U	NC	—	No Connection: There is no connection to the chip.

MPC2604GA

Product Preview

Integrated Secondary Cache for PowerPC™ Microprocessors



ZP PACKAGE
PBGA
CASE 1103–01

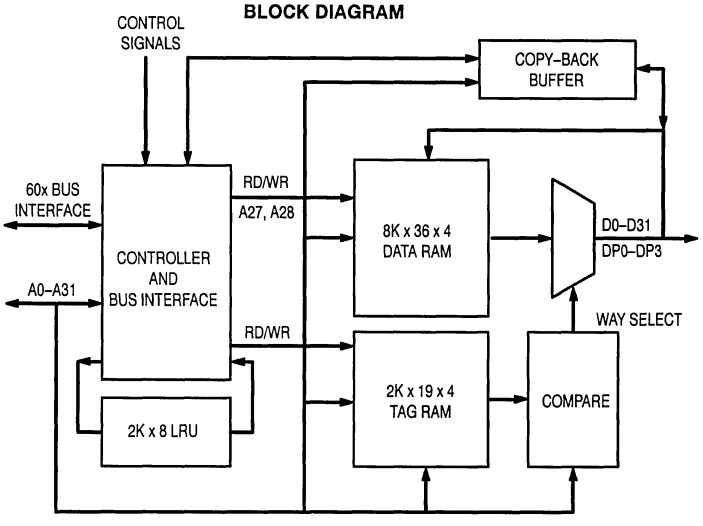
The MPC2604GA is an integrated look–aside cache with copy–back or optional write–through capability designed for PowerPC applications (MPC601, MPC603, and MPC604). Using 0.5 µm BiCMOS memory technology along with standard cell logic technology, the MPC2604GA integrates data, tag, host interface, and LRU memory with a cache controller to provide a two or four chip Level 2 cache solution for the 64 bit PowerPC bus.

- 4–Way Set Associative Cache Design
- 32K x 36 Data Memory Array
- 8K x 19 Tag Array
- Least Recently Used Cache Control Logic
- Copy–Back or Write–Through Modes of Operation
- Copy–Back Buffer for Improved Performance
- Single 5 V Power Supply with 3.3 V Compatible I/O
- 66 MHz Zero Wait State Performance (2–1–1–1 Burst)
- Two or Four Chip Cache Solution (256K or 512K Bytes)
- Single Clock Operation
- Compliant with Proposed IEEE Standard 1149.2 Test Access Port (JTAG)
- High Board Density 25mm PBGA Package

For further information on this product, please order document MPC2604GA/D.

4

BLOCK DIAGRAM



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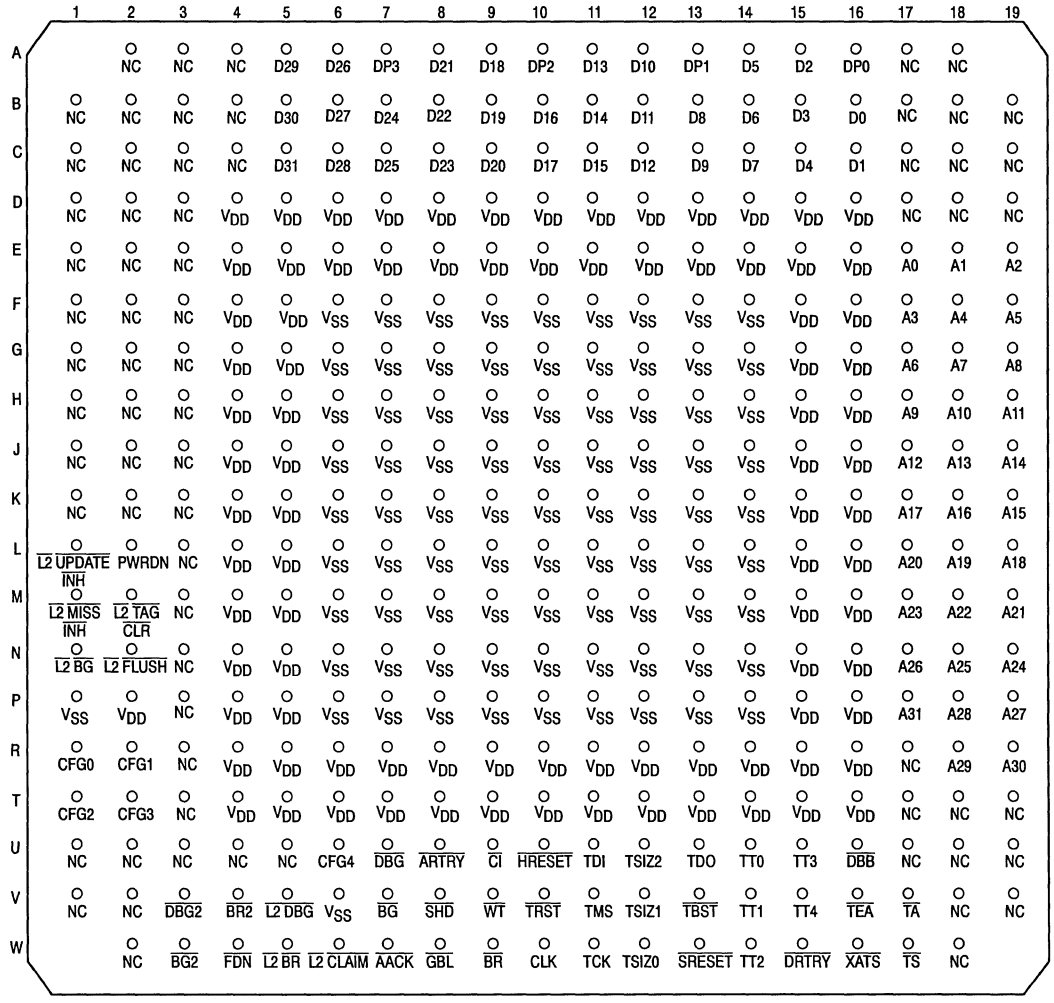
PIN ASSIGNMENTS



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A		NC	NC	NC	D29	D26	DP3	D21	D18	DP2	D13	D10	DP1	D5	D2	DP0	NC	NC	
B	NC	NC	NC	NC	D30	D27	D24	D22	D19	D16	D14	D11	D8	D6	D3	D0	NC	NC	NC
C	NC	NC	NC	NC	D31	D28	D25	D23	D20	D17	D15	D12	D9	D7	D4	D1	NC	NC	NC
D	NC	NC	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	NC	NC	NC
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	A0	A1	A2
F	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A3	A4	A5
G	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A6	A7	A8
H	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A9	A10	A11
J	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A12	A13	A14
K	NC	NC	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A17	A16	A15
L	$\overline{\text{L2 UPDATE INH}}$	PWRDN	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A20	A19	A18
M	$\overline{\text{L2 MISS INH}}$	$\overline{\text{L2 TAG CLR}}$	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A23	A22	A21
N	$\overline{\text{L2 BG}}$	$\overline{\text{L2 FLUSH}}$	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A26	A25	A24
P	V_{SS}	V_{DD}	NC	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	A31	A28	A27
R	CFG0	CFG1	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	NC	A29	A30
T	CFG2	CFG3	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	NC	NC	NC
U	NC	NC	NC	NC	NC	CFG4	$\overline{\text{DBG}}$	$\overline{\text{ARTRY}}$	$\overline{\text{CI}}$	$\overline{\text{HRESET}}$	TDI	TSIZ2	TDO	TT0	TT3	$\overline{\text{DBB}}$	NC	NC	NC
V	NC	NC	$\overline{\text{DBG2}}$	$\overline{\text{BR2}}$	$\overline{\text{L2 DBG}}$	V_{SS}	$\overline{\text{BG}}$	$\overline{\text{SHD}}$	$\overline{\text{WT}}$	$\overline{\text{TRST}}$	TMS	TSIZ1	$\overline{\text{TBST}}$	TT1	TT4	$\overline{\text{TEA}}$	$\overline{\text{TA}}$	NC	NC
W		NC	$\overline{\text{BG2}}$	$\overline{\text{FDN}}$	$\overline{\text{L2 BR}}$	$\overline{\text{L2 CLAIM}}$	$\overline{\text{AACK}}$	$\overline{\text{GBL}}$	$\overline{\text{BR}}$	CLK	TCK	TSIZ0	$\overline{\text{SRESET}}$	TT2	$\overline{\text{DRTRY}}$	$\overline{\text{XATS}}$	$\overline{\text{TS}}$	NC	

TOP VIEW (XRAY VIEW)

PIN DESCRIPTIONS

Pin Locations	Pin Name	Type	Description
17E–17P, 18E–18R, 19E–19R	A0 – A31	I/O	Address inputs from processor. Can also be outputs for processor snoop addresses A(0) = 0 indicates that a transfer is cacheable. A(0) = 1 indicates non–cacheable memory space. A(0) is MSB. A(31) is LSB.
7W	$\overline{AACK}$	I/O	Address acknowledge input/output.
8U	$\overline{ARTRY}$	I/O	Address retry status I/O. Generated when a read or write snoop to a dirty processor cache line has occurred.
7V	$\overline{BG}$	I	CPU bus grant input.
3W	$\overline{BG2}$	I	MPC2604GA logically ORs this signal with $\overline{BG}$. Used in multiprocessor write–through configuration.
9W	$\overline{BR}$	I	CPU bus request input.
4V	$\overline{BR2}$	I	MPC2604GA logically ORs this signal with $\overline{BR}$. Used in multiprocessor write–through configuration.
1R, 2R, 1T, 2T, 6U	CFG0–4	I	Configuration inputs. These must be tied to either V_{DD} or V_{SS}. CFG0 Defines Data Bus Side 0 Data Bus Low 1 Data Bus High CFG1 Defines Cache Size 0 256K 1 512K CFG2 Cache Line Selector For 512k Cache Size 0 Even Cache Lines 1 Odd Cache Lines CFG3 Initial Tag Lookup Extension 0 Enable 2–1–1–1 burst cycle, 2 clock non–burst operations 1 Enable 3–1–1–1 burst cycle, 3 clock non–burst operations CFG4 $\overline{AACK}$ Driver Enable 0 Disable $\overline{AACK}$ Driver 1 Enable $\overline{AACK}$ Driver
9U	$\overline{CI}$	I/O	Cache inhibit I/O.
10W	CLK	I	Clock input. This must be the same as the processor clock input.
16U	$\overline{DBB}$	I/O	Data bus busy. Used as input when processor is master, driven as an output after a qualified $\overline{L2\ DBG}$ when MPC2604GA is the bus master.
7U	$\overline{DBG}$	I	Data bus grant input from arbiter.
3V	$\overline{DBG2}$	I	MPC2604GA logically ORs this signal with $\overline{DBG}$. Used in multiprocessor write–through configuration.
5A, 6A, 8A, 9A, 11A, 12A, 14A, 15A, 5B–16B, 5C–16C	D0–D31	I/O	Data bus input and output.
16A, 13A, 10A, 7A	DP0–DP3	I/O	Data bus parity input and output.
15W	$\overline{DRTRY}$	I	Data retry input from system.
4W	$\overline{FDN}$	I/O	Flush done I/O used for communication between other MPC2604GA devices. Used as an input only during L2 flush operations on MPC2604GA parts where both CFG1 and CFG2 are wired high (that is, on the odd cache line pair of a 512K byte MPC2604GA cache configuration). In this case, the even cache line pair performs their flush first, and drives $\overline{L2\ BR}$ low until they are finished with their flush, then $\overline{L2\ BR}$ is driven high and put into high–Z mode.
8W	$\overline{GBL}$	I/O	Global status I/O from processor bus.
10U	$\overline{HRESET}$	I	Hard reset input from processor bus. This is a synchronous input that must be low for at least 10 clock cycles to ensure the MPC2604GA is properly reset.
1N	$\overline{L2\ BG}$	I	Bus grant input from arbiter.
5W	$\overline{L2\ BR}$	I/O	Bus request I/O. Normally used as an output.

6W	L2 CLAIM	O	L2 Memory Claim output. Used to claim the bus for processor initiated memory operations that hit the L2 cache. If CFG3 is low, L2 CLAIM goes true (low) before the rising edge of CLK following TS true. If CFG3 is high, L2 CLAIM goes true (low) before the second rising edge of CLK following TS true. L2 CLAIM then stays true until after the rising edge of CLK that follows AACK driven true.
5V	L2 DBG	I	Data bus grant input. Comes from system arbiter, used to start data tenure for bus operations where MPC2604GA is the bus master.
2N	L2 FLUSH	I	Causes cache to write back dirty lines and clears all tag valid bits.
1M	L2 MISS INH	I	Prevents line fills on misses when asserted.
1L	L2 UPDATE INH	I	Cache disable. When asserted, the MPC2604GA will not respond to signals on the local bus and internal states do not change.
2M	L2 TAG CLR	I	Invalidates all tags and holds cache in a reset condition.
2L	PWRDN	I	Provides low power mode. Disables internal clock tree and prevents address and data transitions into the RAM array.
8V	SHD	I/O	Indicates when a cache line is shared in a multiprocessor situation.
13W	SRESET	I	Soft reset input from processor bus.
17V	TA	I/O	Transfer acknowledge status I/O from processor bus.
13V	TBST	I/O	Transfer burst status I/O from processor bus. Used to distinguish between burstable and non–burstable memory operations.
11W	TCK	I	Test clock input for IEEE 1149.2 boundary scan (JTAG).
11U	TDI	I	Test data input for IEEE 1149.2 boundary scan (JTAG).
13U	TDO	O	Test data output for IEEE 1149.2 boundary scan (JTAG).
16V	TEA	I	Transfer error acknowledge status input from processor bus.
11V	TMS	I	Test mode select for IEEE 1149.2 boundary scan (JTAG).
10V	TRST	I	Test reset input for IEEE 1149.2 boundary scan (JTAG).
17W	TS	I/O	Transfer start I/O from processor bus (can also come from any bus master on the processor bus). Signals the start of either a processor or bus master cycle.
12U, 12V, 12W	TSIZ2–0	I/O	Transfer size I/O from processor bus.
15V, 15U, 14W, 14V, 14U	TT4–0	I/O	Transfer type I/O from processor bus.
9V	WT	I/O	Write through status input from processor bus. When tied to ground, the MPC2604GA will operate in write–through mode only (no copy–back).
16W	XATS	I	Extended address transfer start input. Used for tracking address/data tenures.
2A–4A, 17A, 18A, 1B–4B, 17B–19B, 1C–4C, 17C–19C, 1D–3D, 17D–19D, 1E–3E, 1F–3F, 1G–3G, 1H–3H, 1J–3J, 1K–3K, 3L, 3M, 3N, 3P, 3R, 17R, 3T, 17T–19T, 1U–5U, 17U–19U, 1V–2V, 18V–19V, 2W, 18W	NC	—	No connection: There is no connection to the chip.
4D–16D, 4E–16E, 4F, 5F, 15F, 16F, 4G, 5G, 15G, 16G, 4H, 5H, 15H, 16H, 4J, 5J, 15J, 16J, 4K, 5K, 15K 16K, 4L, 5L, 15L, 16L, 4M, 5M, 15M, 16M, 4N, 5N, 15N, 16N, 2P, 4P, 5P, 15P, 16P, 4R–16R, 4T–16T	V_{DD}	Supply	Power supply: 5.0 V ± 10%
6F–14F, 6G–14G, 6H–14H, 6J–14J, 6K–14K, 6L–14L, 6M–14M, 6N–14N, 1P, 6P–14P, 6R–14R, 6V	V_{SS}	Supply	Ground.

BurstRAMs

5

Processor Specific

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MCM62486B

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self–Timed Write

The MCM62486B is a 294,912 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated with Motorola's high–performance silicon–gate CMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

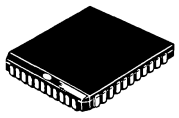
Addresses (A0 – A14), data inputs (D0 – D8), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM62486B (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

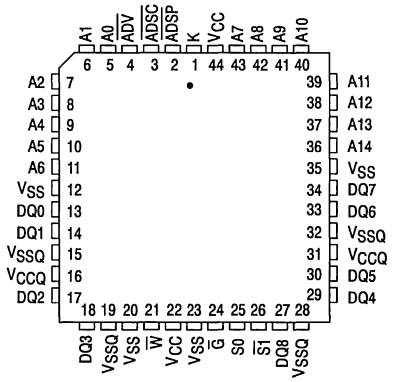
The MCM62486B will be available in a 44–pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user–controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply (± 5% for MCM62486BFN11)
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times:11/12/14/19 ns Max and Cycle Times:15/20/25 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL–Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion



FN PACKAGE
44–LEAD PLCC
CASE 777–01

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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i486 and Pentium are trademarks of Intel Corp.

REV 2
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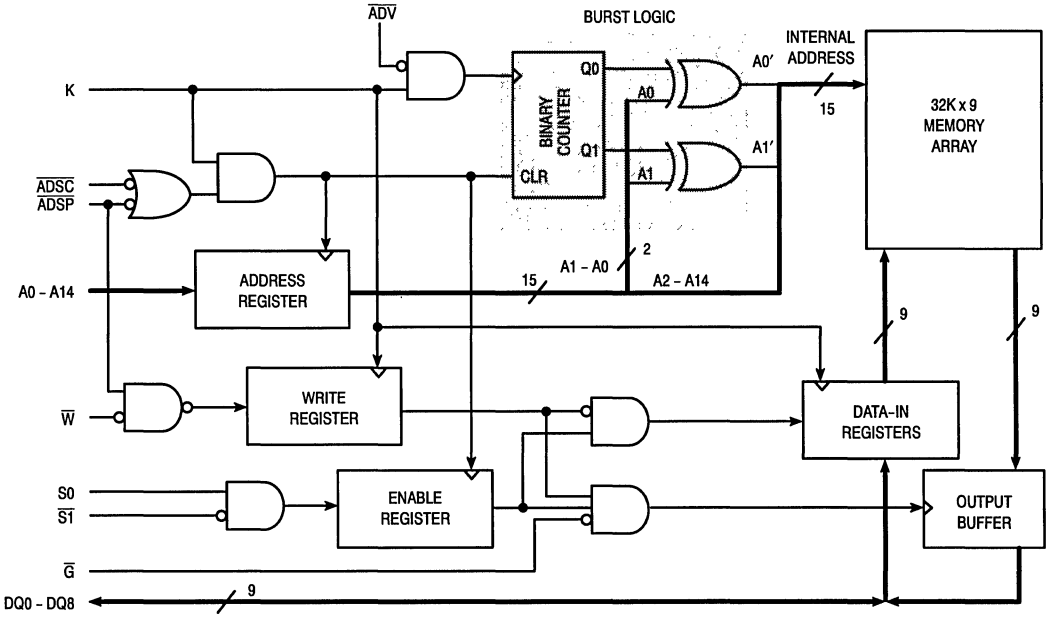
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address Used	Operation
F	L	X	X	X	L–H	N/A	Deselected
F	X	L	X	X	L–H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High–Z
Write	X	High–Z — Data In (DQ0 – DQ8)
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62486B–11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	160	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

5

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62486B–11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	62486B–11		62486B–12		62486B–14		62486B–19		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	20	—	20	—	25	—	ns	
Clock Access Time	t_{KHQV}	—	11	—	12	—	14	—	19	ns	
Output Enable Access	t_{GLQV}	—	5	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	6	—	ns	
Clock High to Q Change	t_{KHQX2}	3	—	3	—	4	—	4	—	ns	
Output Enable to Q Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	—	6	—	7	ns	4
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5.5	—	7	—	8	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5.5	—	7	—	8	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{S0VKH} t_{S1VKH}	2	—	2	—	3	—	3	—	ns	5
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHS0X} t_{KHS1X}	2	—	2	—	2	—	2	—	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
5. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{ADSP}$ and $\overline{ADSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

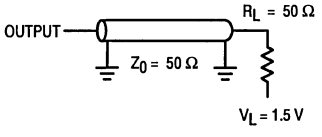


Figure 1A

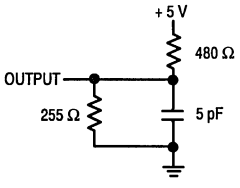
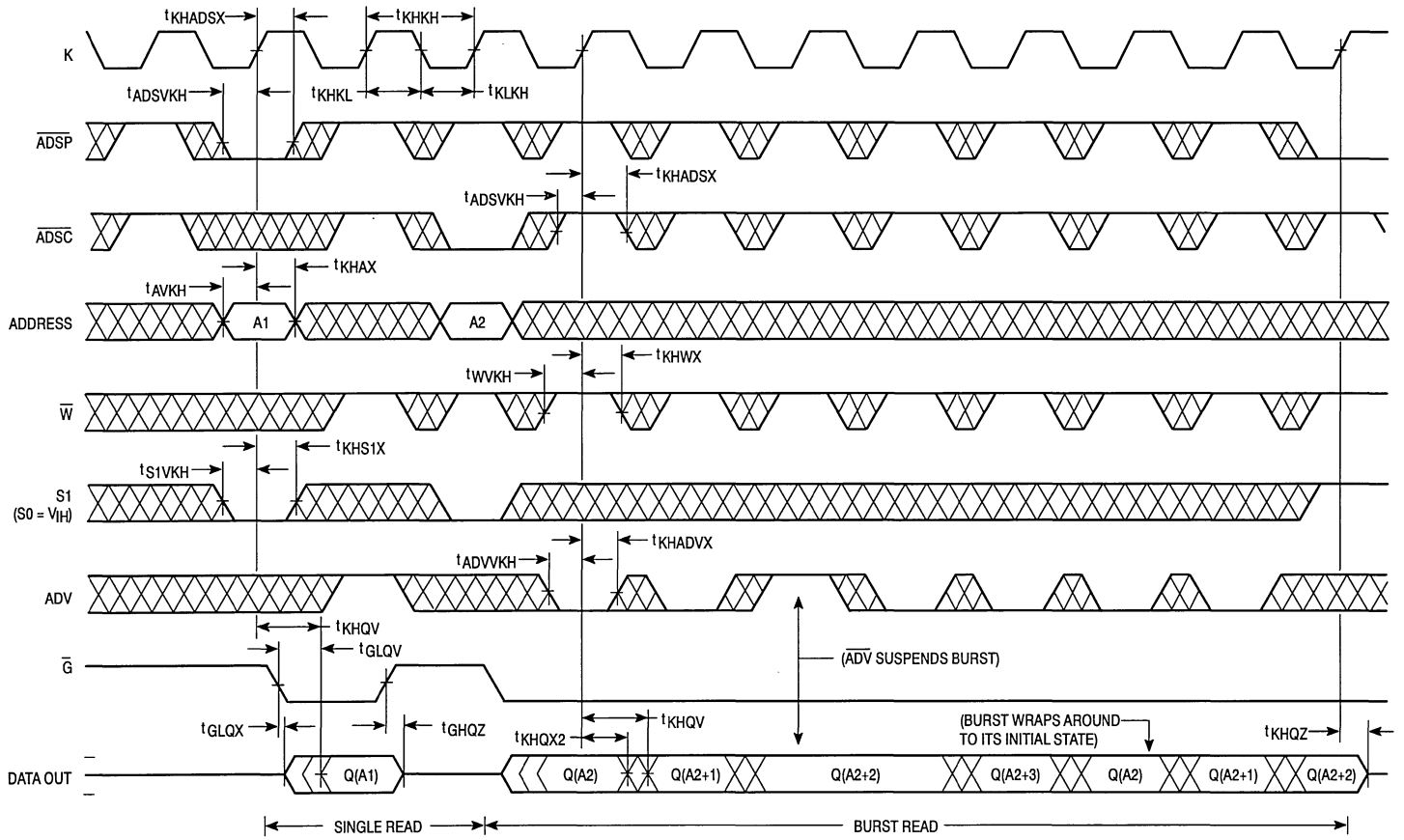


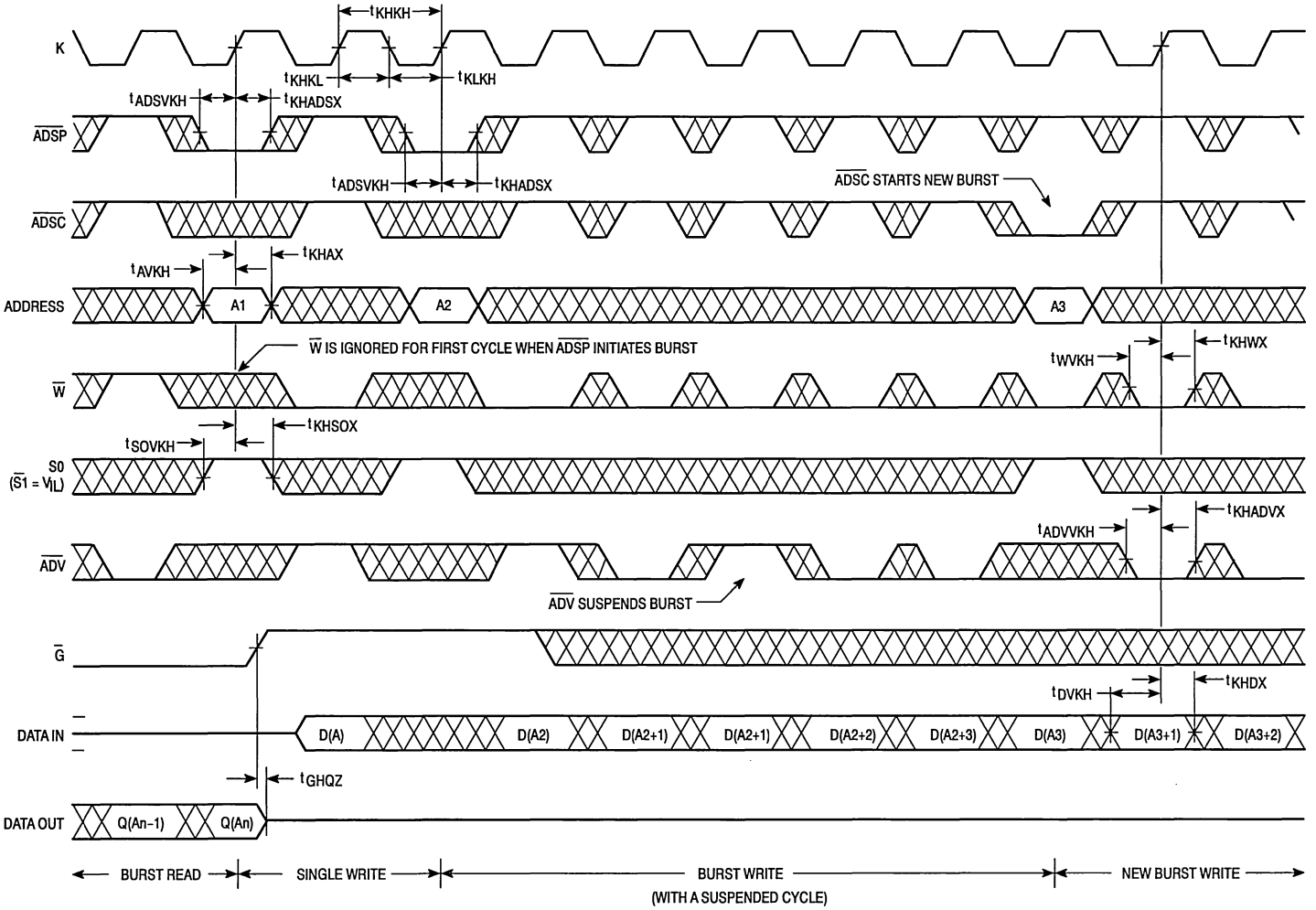
Figure 1B

READ CYCLES



NOTE: Q(A2) represents the first output data from the base address A2; Q(A2+1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



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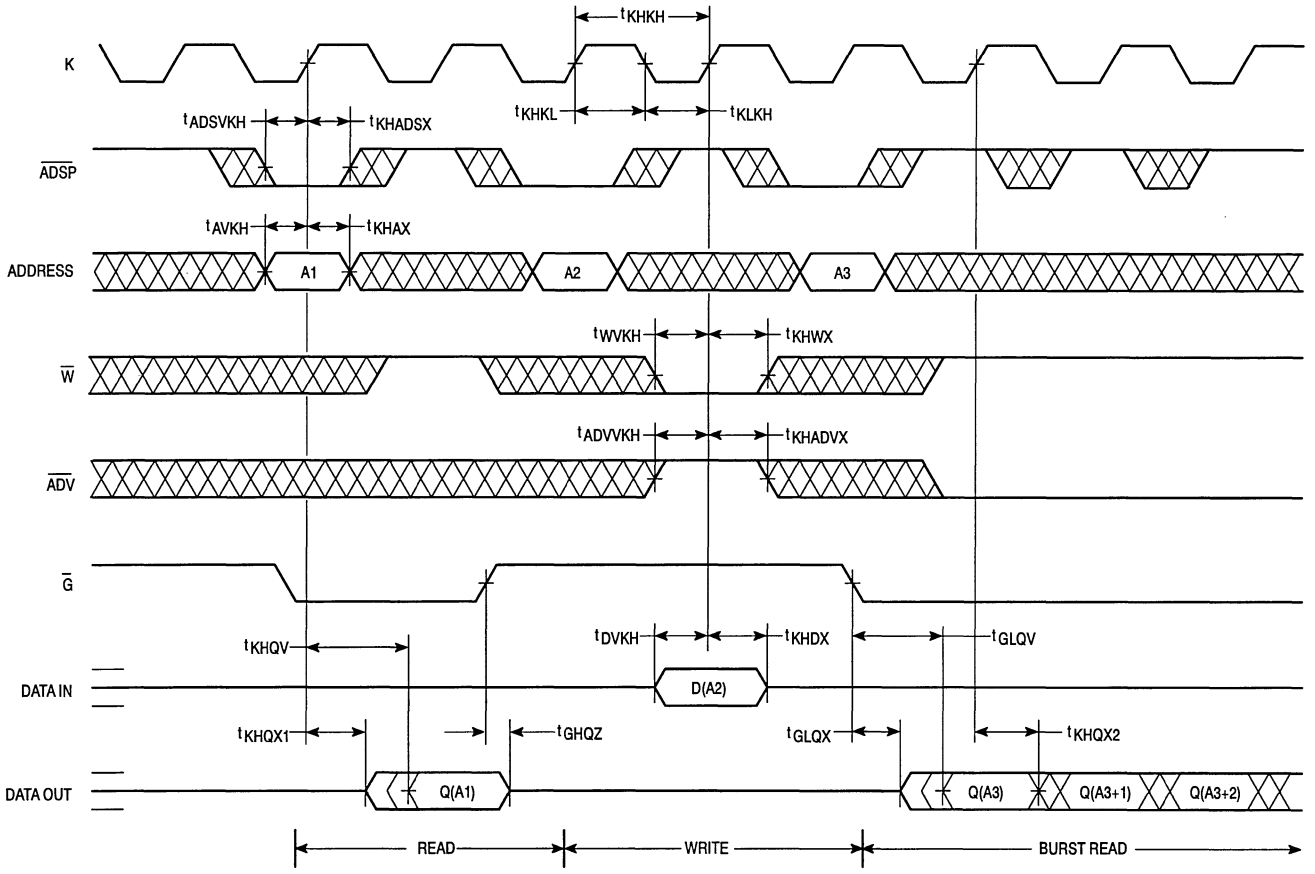
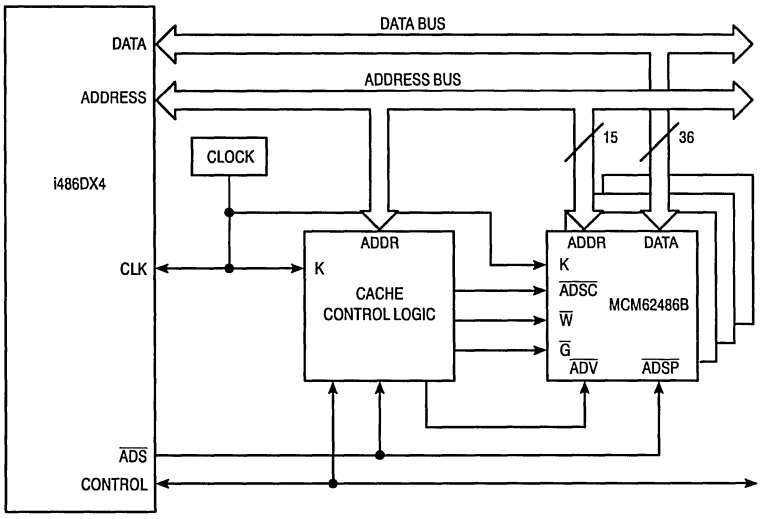
COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



128K Byte Burstable, Secondary Cache Using
4 MCM62486BFN19s With a 100 MHz i486DX4

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62486B XX XX

Motorola Memory Prefix

Part Number

Speed (11 = 11 ns, 12 = 12 ns, 14 = 14 ns, 19 = 19 ns)

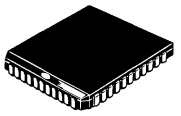
Package (FN = PLCC)

Full Part Numbers — MCM62486BFN11 MCM62486BFN12 MCM62486BFN14 MCM62486BFN19

MCM62940B

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
44–LEAD PLCC
CASE 777–02

The MCM62940B is a 294,912 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high–performance silicon–gate CMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ8), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive–edge–triggered noninverting registers.

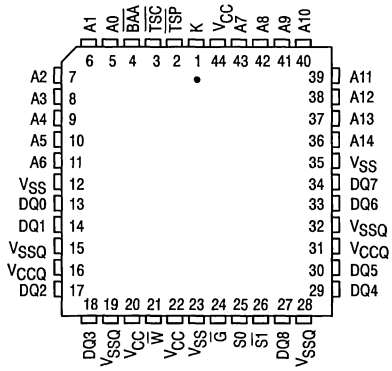
Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM62940B (burst sequence imitates that of the MC68040 and PowerPC) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62940B is packaged in a 44–pin plastic–leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user–controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply (± 5% for MCM62940BFN11)
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 11/12/14/19 ns Max, Cycle Times: 15/20/20/25 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL–Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Synchronous Write
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{BAA}$	Burst Address Advance
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

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PowerPC is a trademark of IBM Corp.

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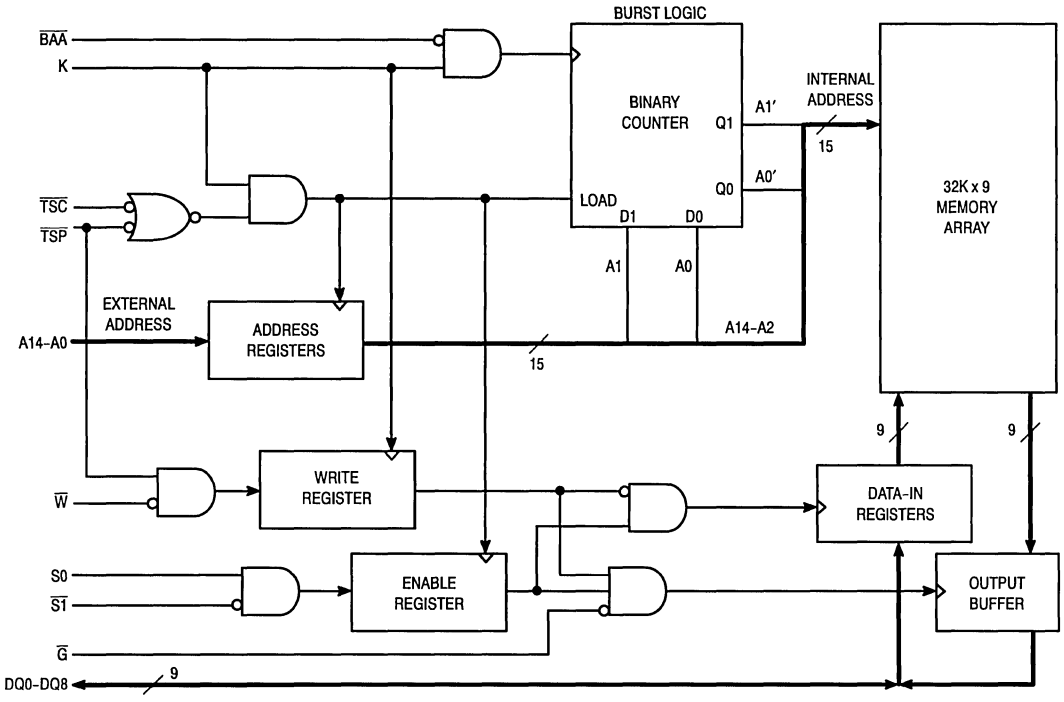
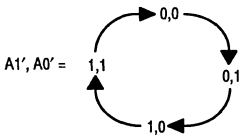
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the next external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**.

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

5

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
F	L	X	X	X	L–H	N/A	Deselected
F	X	L	X	X	L–H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies S0 = H and $\overline{S1}$ = L; F implies S0 = L or $\overline{S1}$ = H.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0–DQ8)
Read	H	High–Z
Write	X	High–Z — Data In (DQ0–DQ8)
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data requird setup time and held high throughout the input data hold time.

5

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62940B–11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	160	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible MC68040 and PowerPC bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62940B–11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	62940B–11		62940B–12		62940B–14		62940B–19		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	20	—	20	—	25	—	ns	
Clock Access Time	t_{KHQV}	—	11	—	12	—	14	—	19	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	5	—	5	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	—	6	—	7	ns	5
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t_{KHKL}	5.5	—	7	—	8	—	9	—	ns	
Clock Low Pulse Width	t_{KLKH}	5.5	—	7	—	8	—	9	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{TSVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{S0VKH} t_{S1VKH}	2	—	2	—	3	—	3	—	ns	6
Hold **Symbol**Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHS0X} t_{KHS1X}	2	—	2	—	2	—	2	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

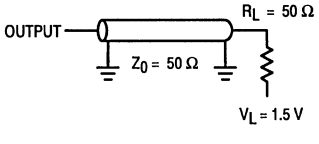


Figure 1A

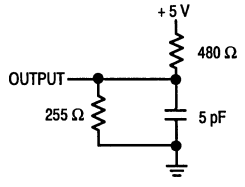
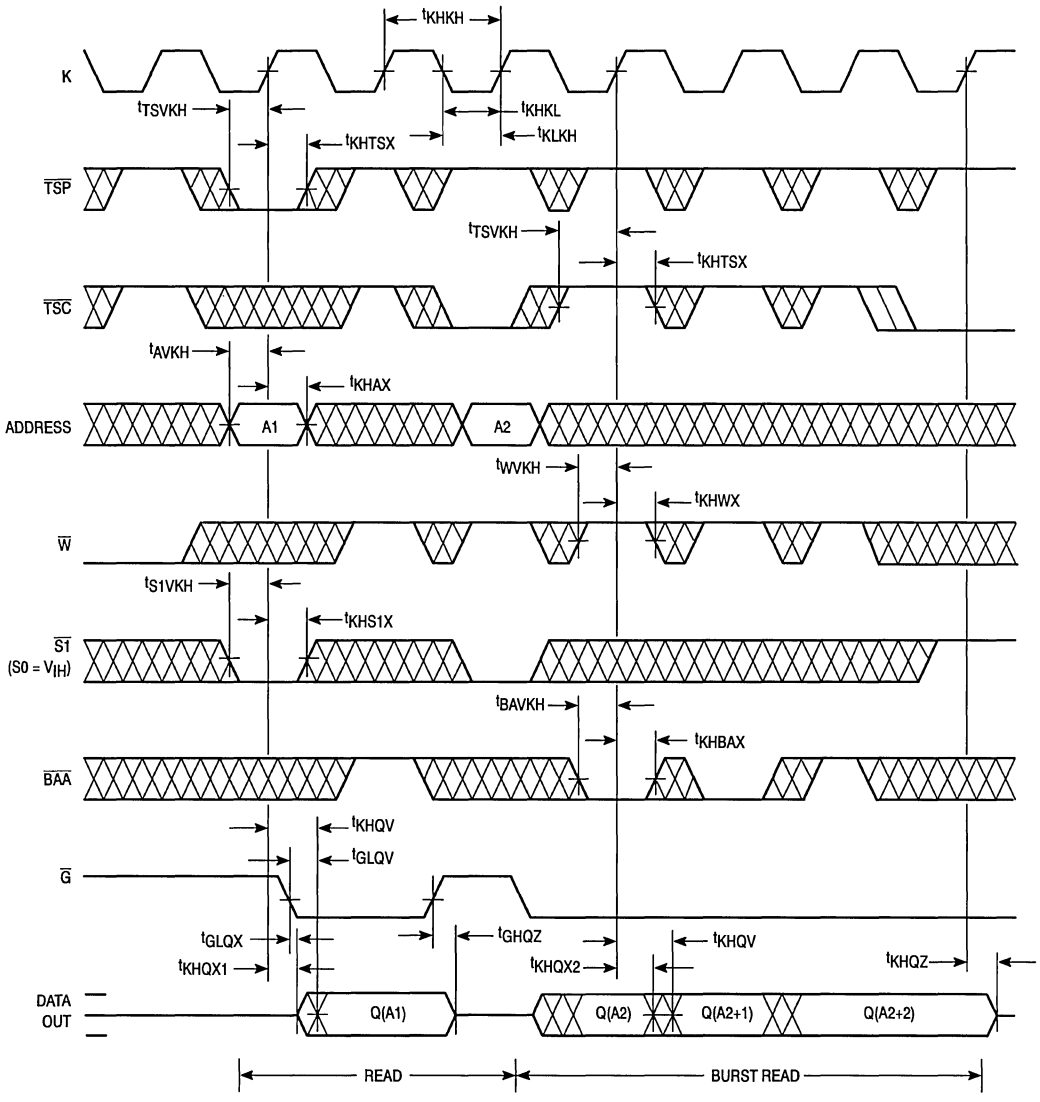


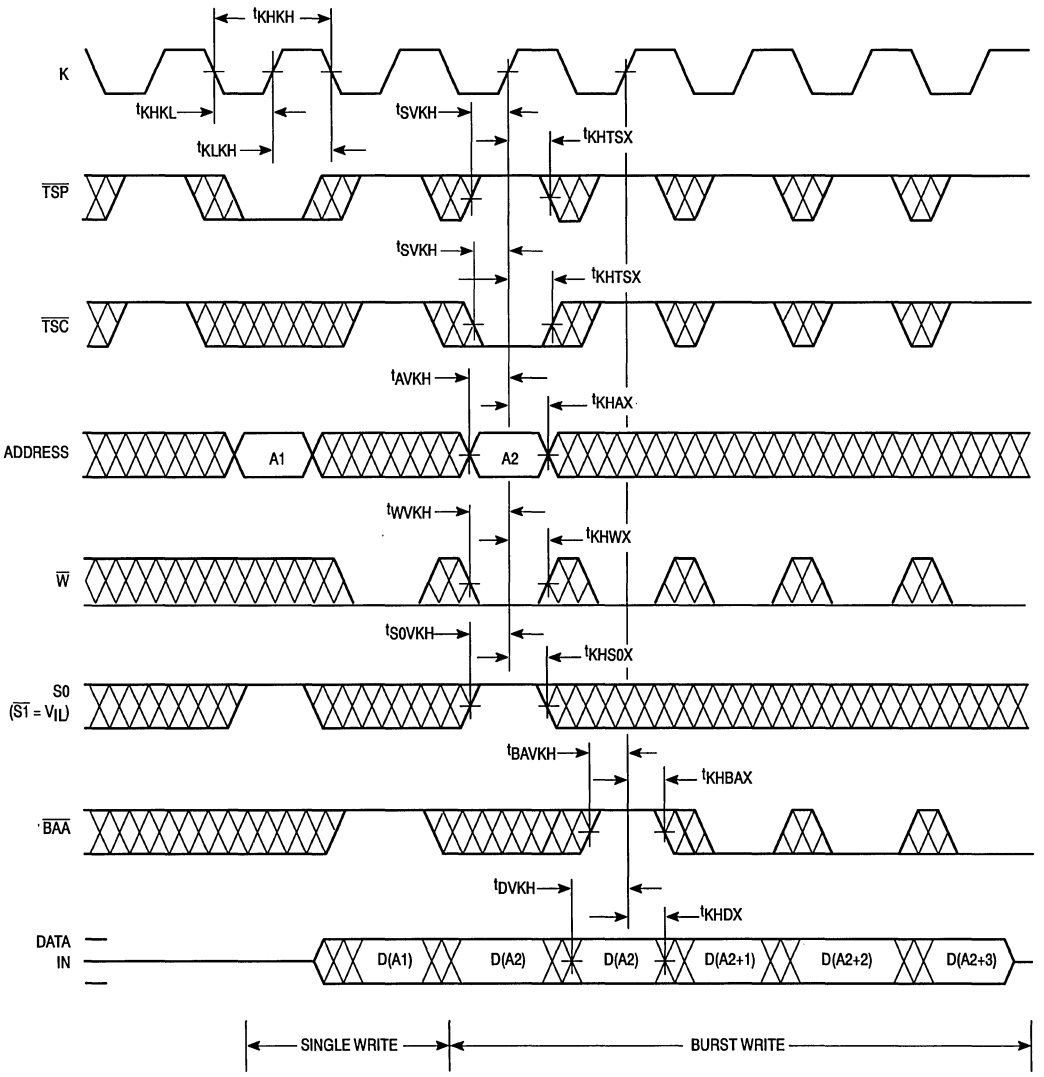
Figure 1B

READ CYCLES



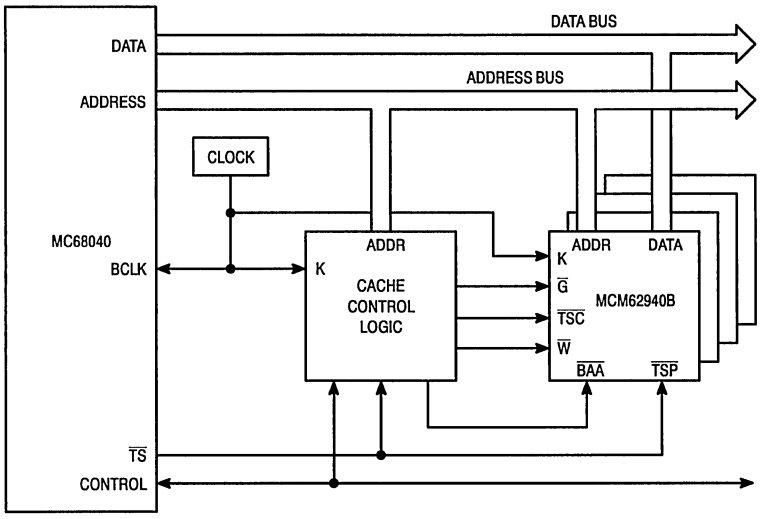
NOTE: Q(A2) represents the first output from the external address A2; Q(A2+1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLE



NOTE: $\overline{G} = V_{IH}$.

APPLICATION EXAMPLE



128K Byte Burstable, Secondary Cache
Using Four MCM62940BFN19s with a 33 MHz MC68040

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62940B XX XX

Motorola Memory Prefix

Part Number

Speed (11 = 11 ns, 12 = 12 ns, 14 = 14 ns, 19 = 19 ns)

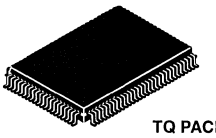
Package (FN = PLCC)

Full Part Numbers — MCM62940BFN11 MCM62940BFN12 MCM62940BFN14 MCM62940BFN19

MCM63P532

Product Preview

32K x 32 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM63P532 is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 32 bits each, fabricated with Motorola's high performance silicon gate CMOS technology. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM63P532 (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM63P532 operates from a 3.3 V power supply, all inputs and outputs are LVTTL compatible. All address and control inputs are 5 V tolerant.

- MCM63P532–7 = 7 ns access / 13.3 ns cycle
  MCM63P532–8 = 8 ns access / 15 ns cycle
  MCM63P532–9 = 9 ns access / 16.6 ns cycle
- Single 3.3 V + 10%, – 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- Sleep Mode (ZZ)
- 5 V Tolerant Address and Control Inputs
- 100 Pin TQFP Package

5

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PowerPC is a trademark of IBM Corp.
i960 and Pentium are trademarks of Intel Corp.

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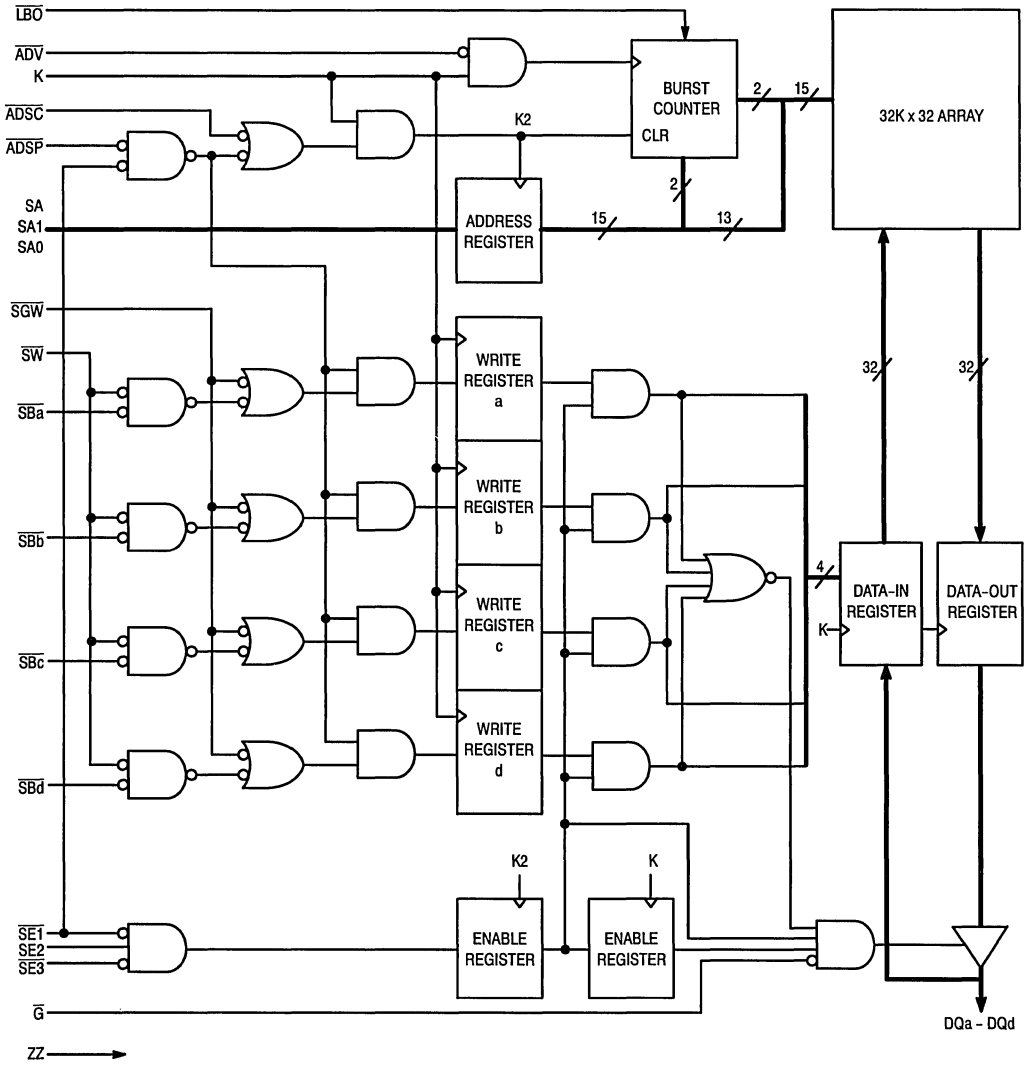
FUNCTIONAL BLOCK DIAGRAM



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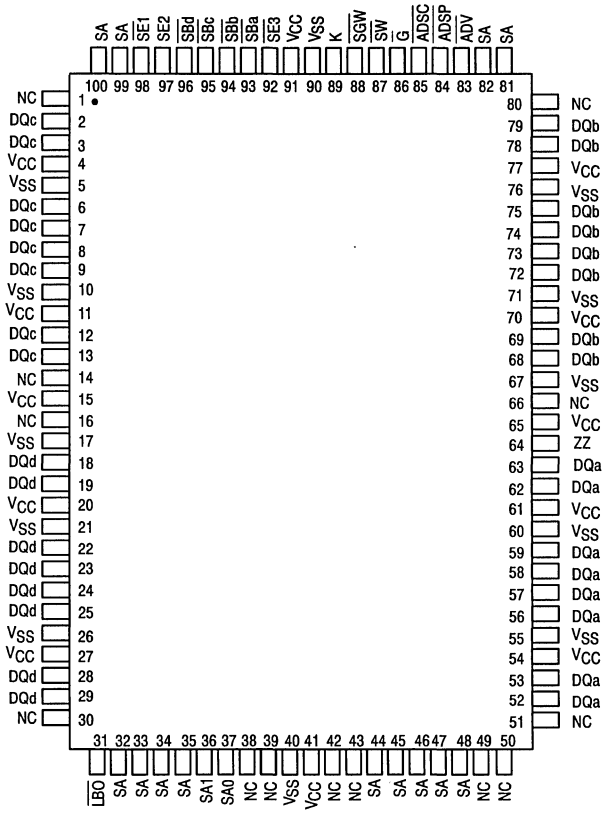
PIN ASSIGNMENTS



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: These pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$, $\overline{LBO}$, and ZZ.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst counter (68K/PowerPC) High–interleaved burst counter (486/i960/Pentium)
64	ZZ	Input	Sleep Mode: This active high asynchronous signal places the RAM into the lowest power mode. The ZZ pin disables the RAMs internal clock when placed in this mode. When ZZ is negated, the RAM remains in low power mode until it is commanded to READ or WRITE. Data integrity is maintained upon returning to normal operation.
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
(a) 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79 (c) 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V + 10%, – 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
1, 14, 16, 30, 38, 39, 42, 43, 49, 50, 51, 66, 80	NC	—	No Connection: There is no connection to the chip.

5

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ[5]
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ[5]
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.
5. This READ assumes the RAM was previously deselected.

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{G}$	I/O Status
Read	L	L	Data Out (DQx)
Read	L	H	High–Z
Write	L	X	High–Z
Deselected	L	X	High–Z
Sleep	H	X	High–Z

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{CC})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

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PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance		—	—	—	1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V +10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	3.135	3.3	3.6	V
Operating Temperature		T_J	20	—	110	°C
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	Address and Control Inputs‡	V_{IH}	2.0	—	5.5	V
	DQx				V_{CC}+0.5**	

* $V_{IL} \geq -1$ V for $t \leq t_{KHKH}/2$.

** $V_{IH} \leq V_{CC} + 1$ V for $t \leq t_{KHKH}/2$.

‡ Control includes K, SA $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{SE1}$, SE2, $\overline{SE3}$, $\overline{SW}$, $\overline{SGW}$, $\overline{SBx}$, $\overline{G}$, ZZ.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time $\geq t_{KHKH}$ min)	MCM63P532–7 MCM63P532–8 MCM63P532–9	I_{CCA}	—	—	TBD	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time $\geq t_{KHKH}$, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{CC}$ – 0.2 V)	MCM63P532–7 MCM63P532–8 MCM63P532–9	I_{SB1}	—	—	TBD	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{CC}$ – 0.2 V)	MCM63P532–7 MCM63P532–8 MCM63P532–9	I_{SB2}	—	—	TBD	mA
Sleep Mode Supply Current (Sleep Mode[2], Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or $\geq V_{CC}$ – 0.2 V)		I_{ZZ}	—	—	TBD	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4 mA)		V_{OH}	2.4	—	—	V

NOTE:

1. Device in Deselected mode as defined by the Truth Table.
2. Device in Sleep Mode as defined by the Asynchronous Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	3	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V + 10%, – 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM63P532–7		MCM63P532–8		MCM63P532–9		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	13.3	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4.5	—	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4.5	—	5	—	5	—	ns	
Clock Access Time	t_{KHQV}	—	7	—	8	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	6	—	6	—	7	ns	5
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	5
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	5
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5
Output Disable to Q High–Z	t_{GHQZ}	—	7	—	8	—	9	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	7	2	8	2	9	ns	6
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	 4
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	 4

NOTES:
1. Write applies to all $\overline{SBx}$, $\overline{SW}$, and $\overline{SGW}$ signals when the chip is selected and $\overline{ADSP}$ high.
2. Chip Enable applies to all $\overline{SE1}$, SE2 and $\overline{SE3}$ signals whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
5. Tested per AC Test Load.
6. Measured at ± 200 mV from steady state. Tested per High–Z Test Load.

AC TEST LOADS

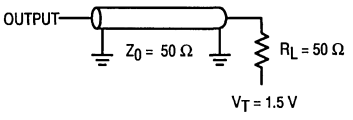


Figure 1A. AC Test Load

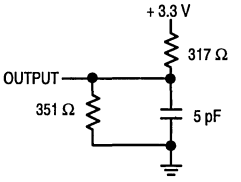
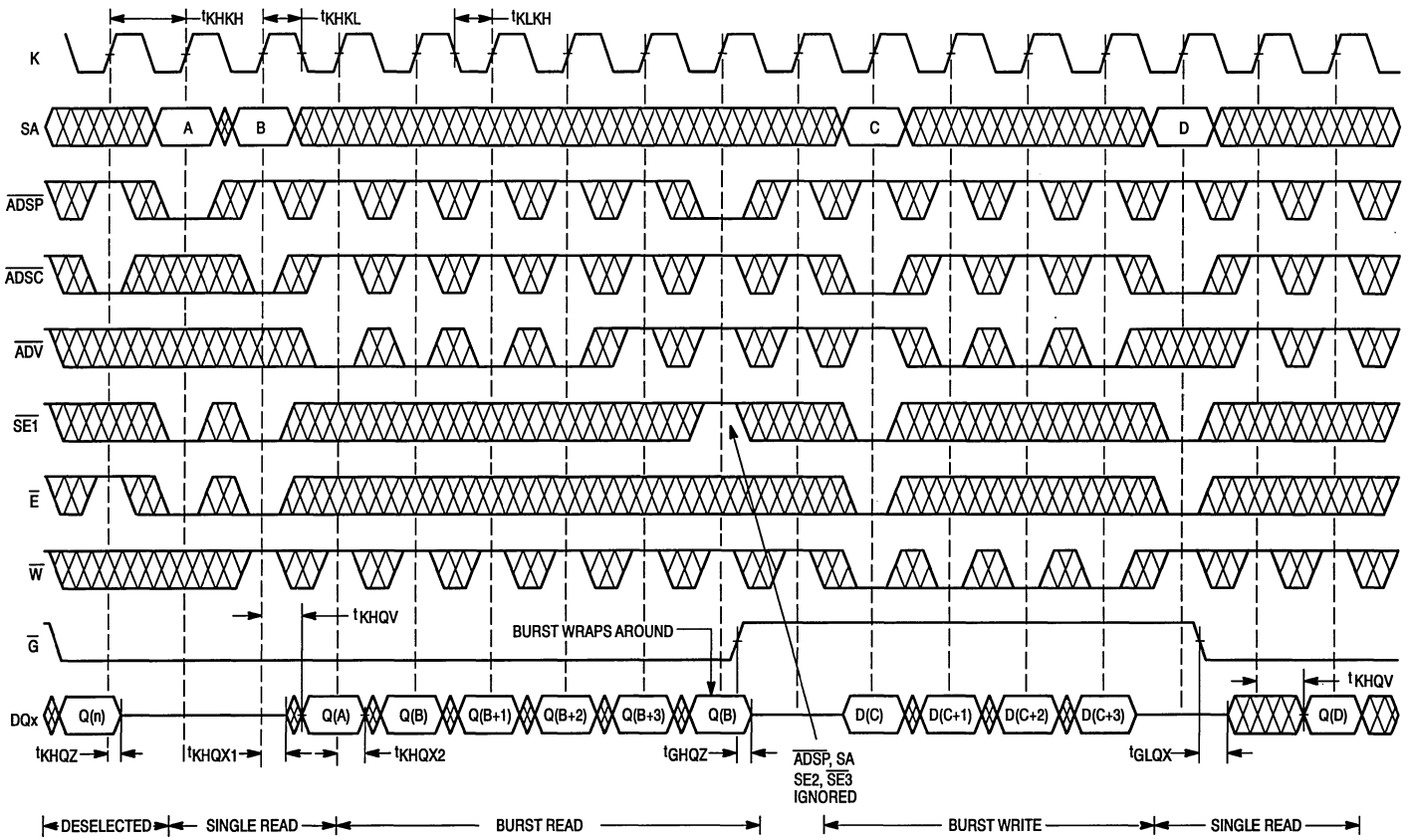


Figure 1B. High–Z Test Load

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM63P532 BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx32 BurstRAM (MCM63P532) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM63P532 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM63P532) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM63P532 device can replace two of the 5 V 32Kx18 devices assuming parity bits are not required. The MCM63P532 can be configured to function as if it were one of the 5 V BurstRAMs. Below is a table that lists control pins on the MCM63P532 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM63P532. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

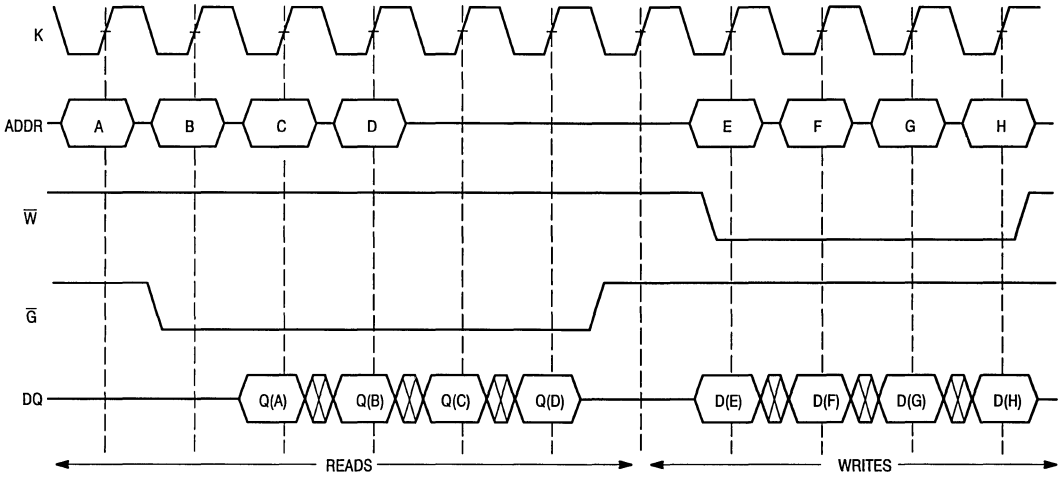
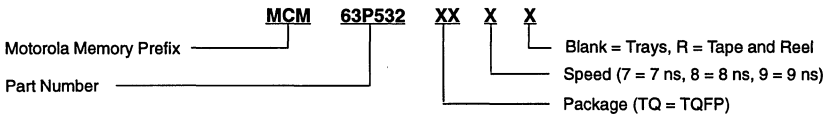


Figure 2. Configured as Non–Burst Pipelined Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)



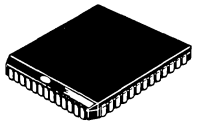
Full Part Numbers — MCM63P532TQ7 MCM63P532TQ8 MCM63P532TQ9
MCM63P532TQ7R MCM63P532TQ8R MCM63P532TQ9R

5

MCM67B518

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67B518 is a 589,824 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67B518 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

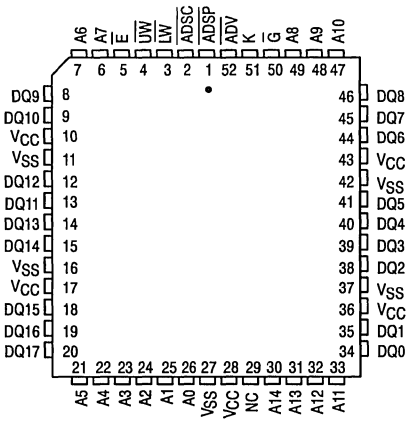
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENTS



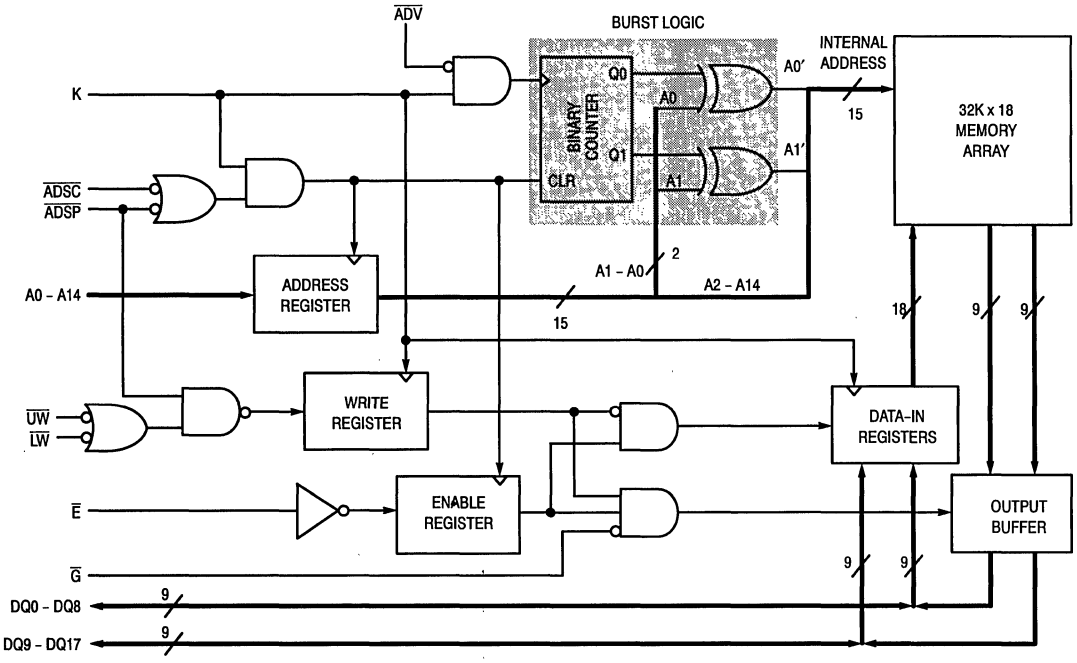
PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

REV 2
5/95

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	—	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67B518–9		MCM67B518–10		MCM67B518–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

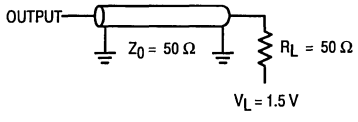


Figure 1A

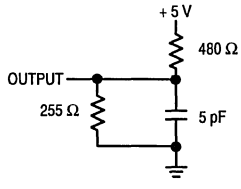
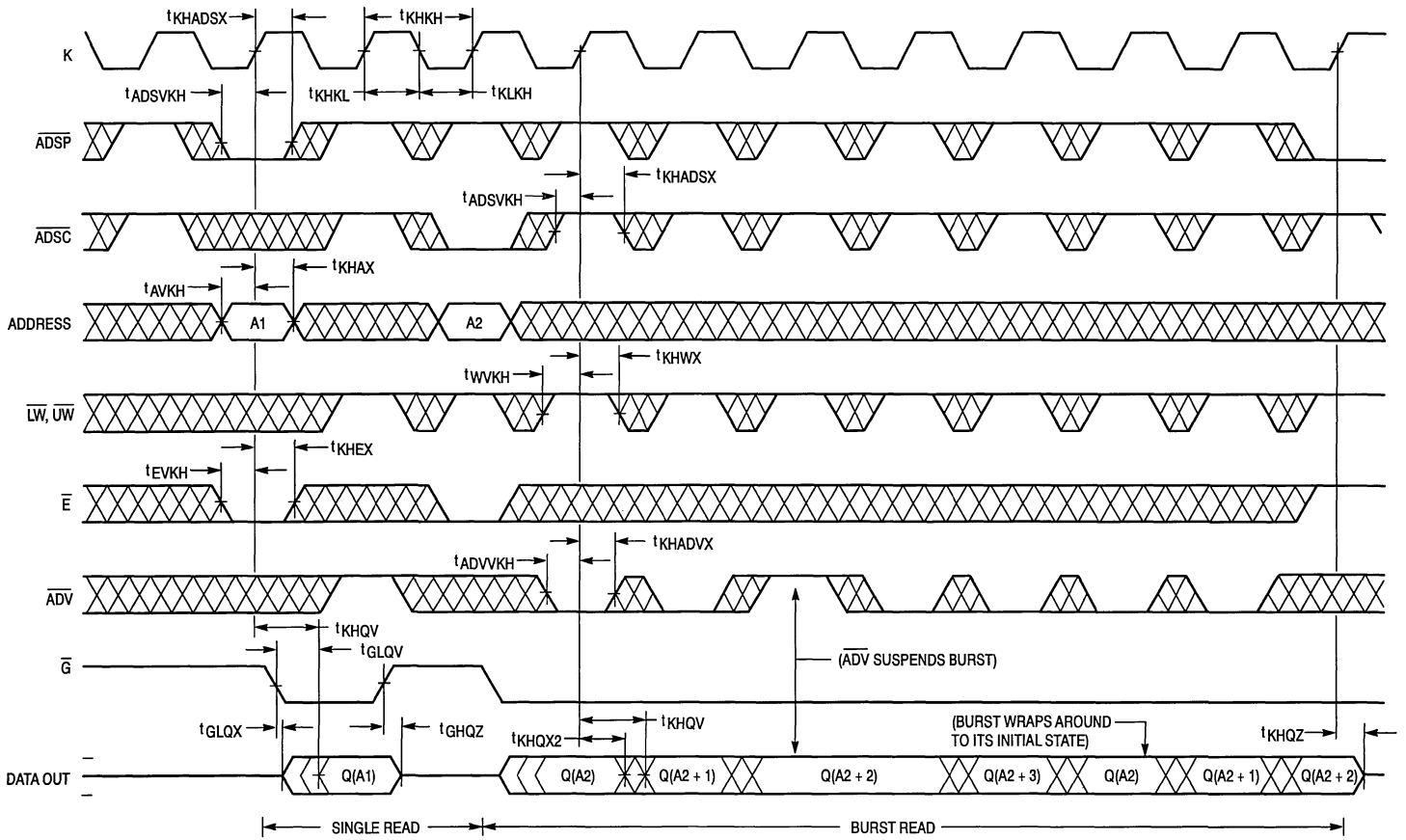


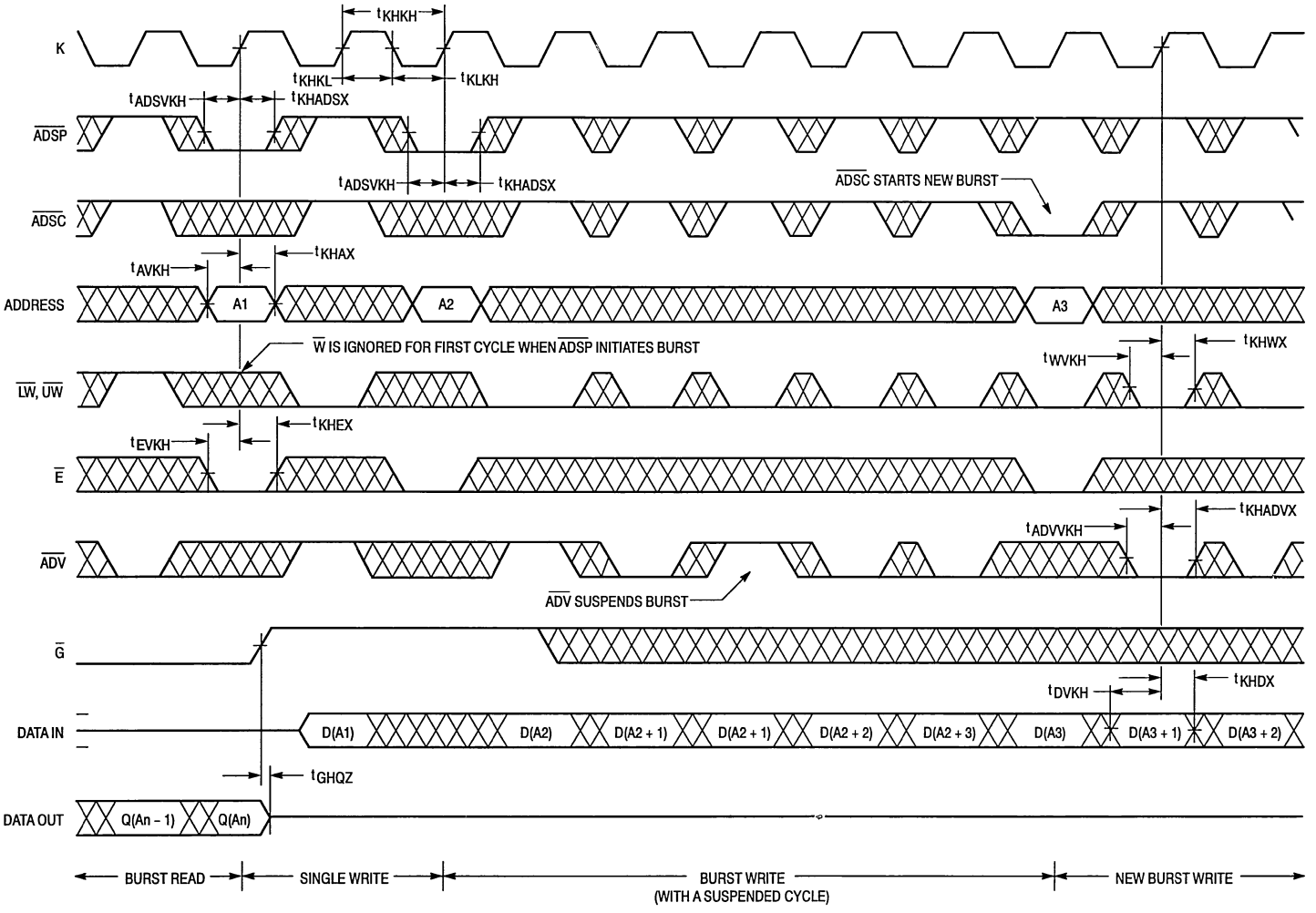
Figure 1B

READ CYCLES

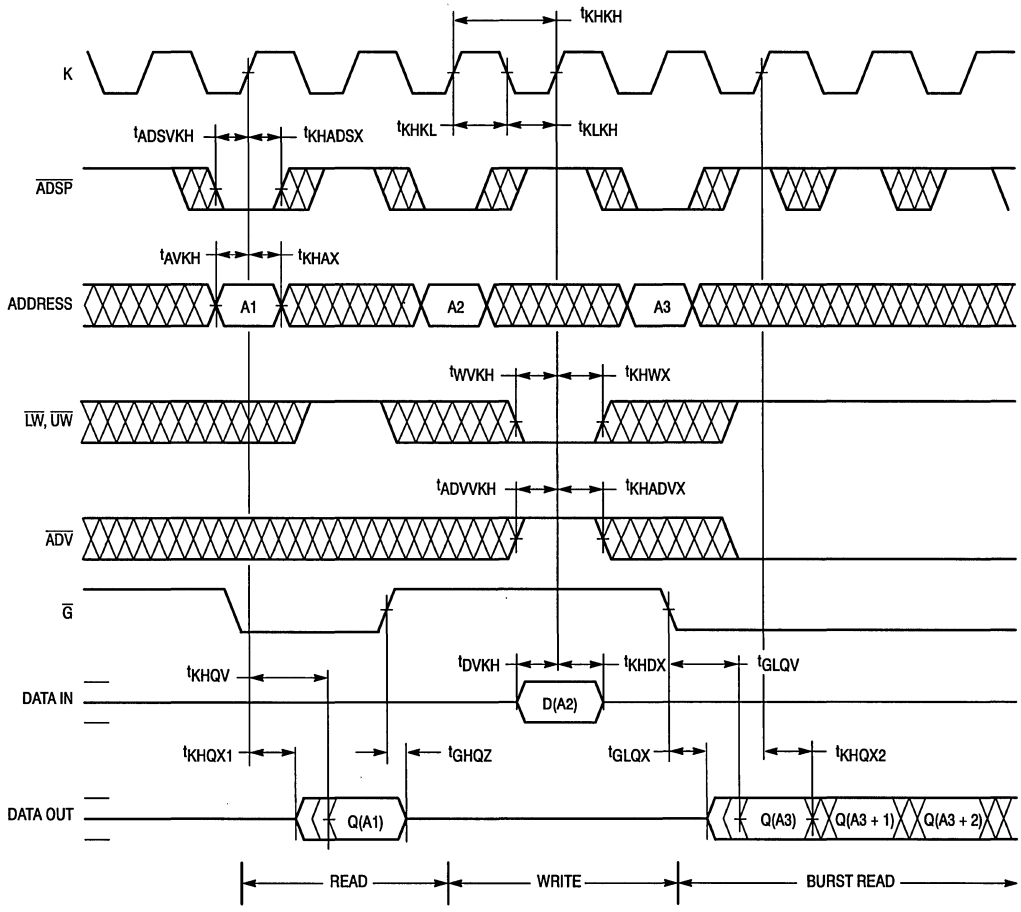


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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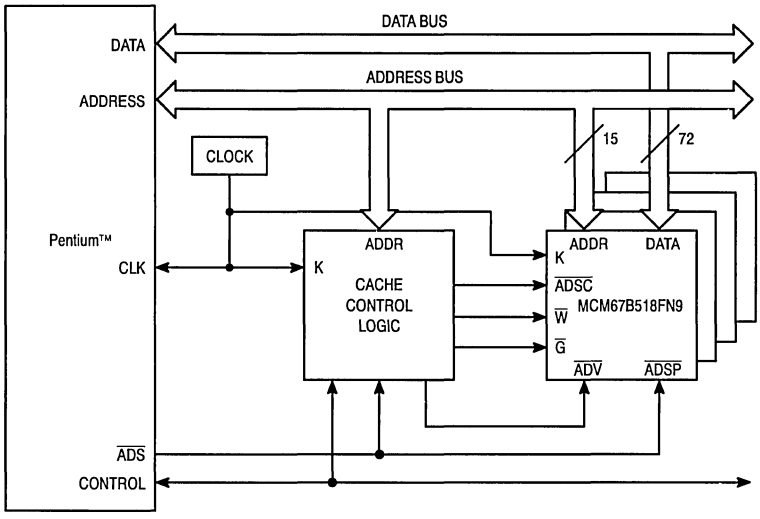
APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67B518FN9s with a 66 MHz (bus speed) Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

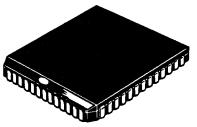
MCM	67B518	XX	XX
Motorola Memory Prefix			Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Part Number			Package (FN = PLCC)

Full Part Numbers — MCM67B518FN9 MCM67B518FN10 MCM67B518FN12

MCM67C518

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67C518 is a 589,824 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered non-inverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67C518 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

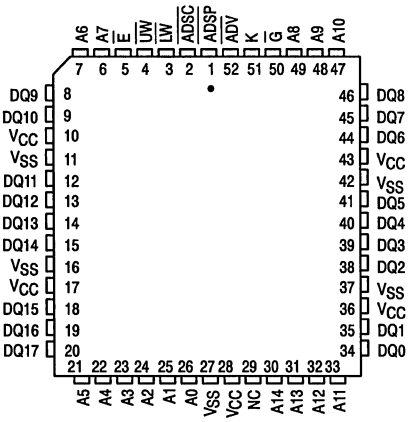
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 6 ns/100 MHz, 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENTS



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

REV 3
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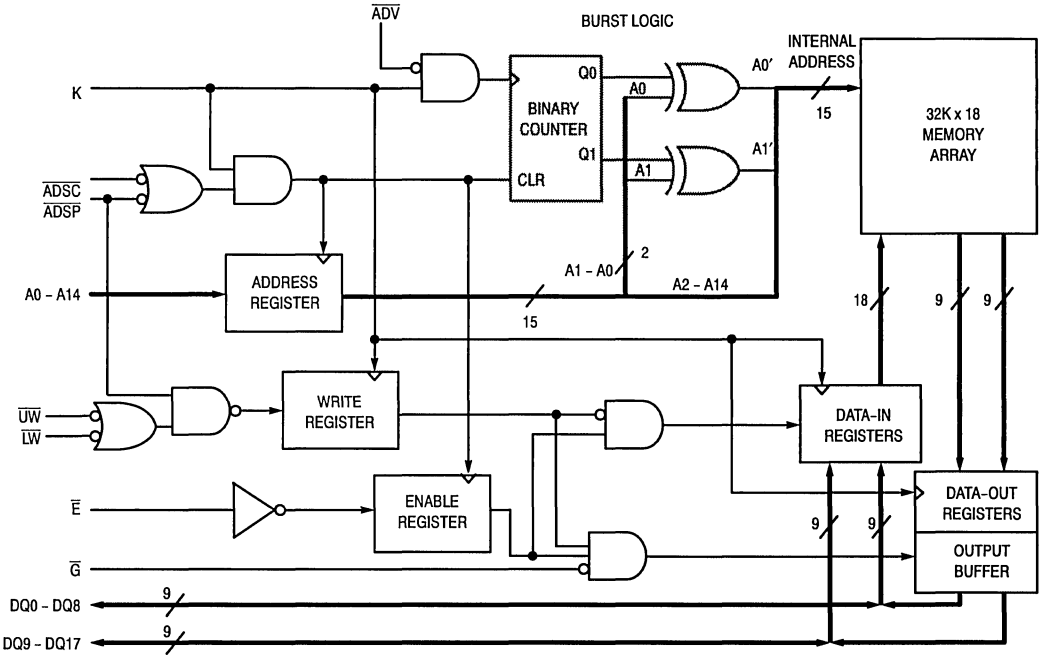
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

5

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA6} I_{CCA7} I_{CCA9}	—	310 290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67C518–6		MCM67C518–7		MCM67C518–9		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	—	6	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	2	—	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4	—	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

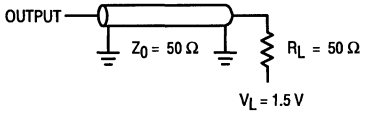


Figure 1A

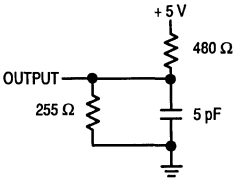
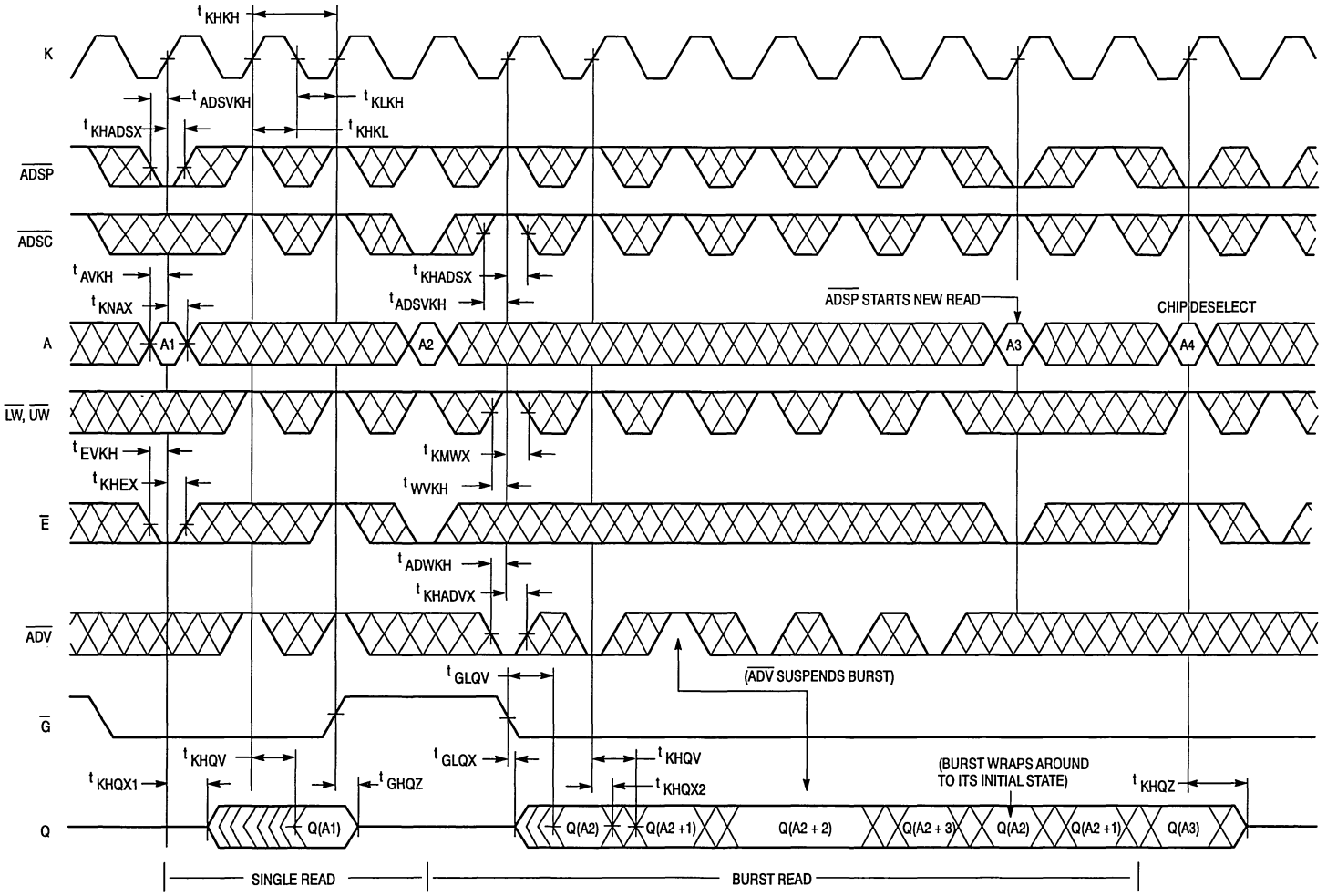


Figure 1B

READ CYCLES



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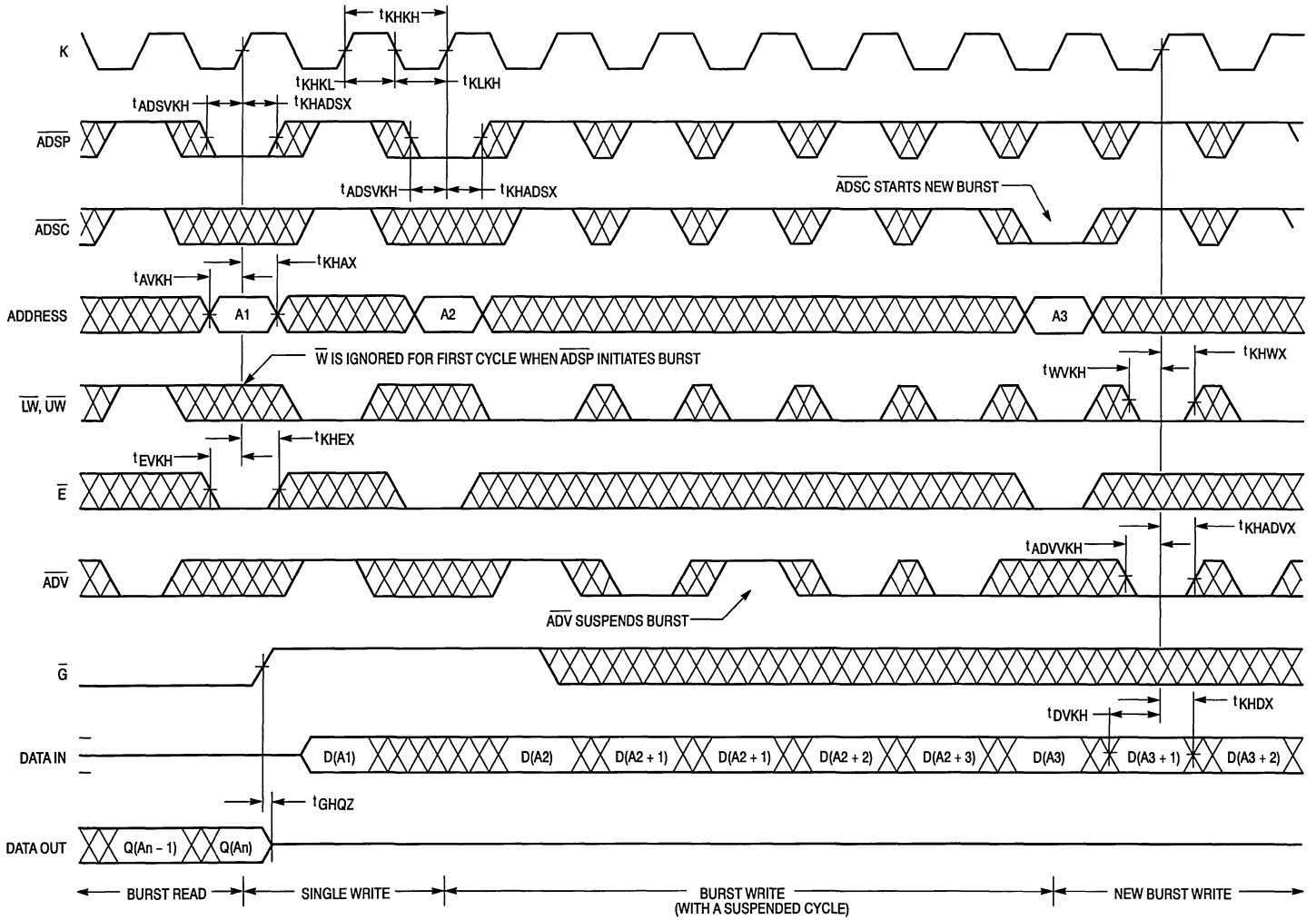
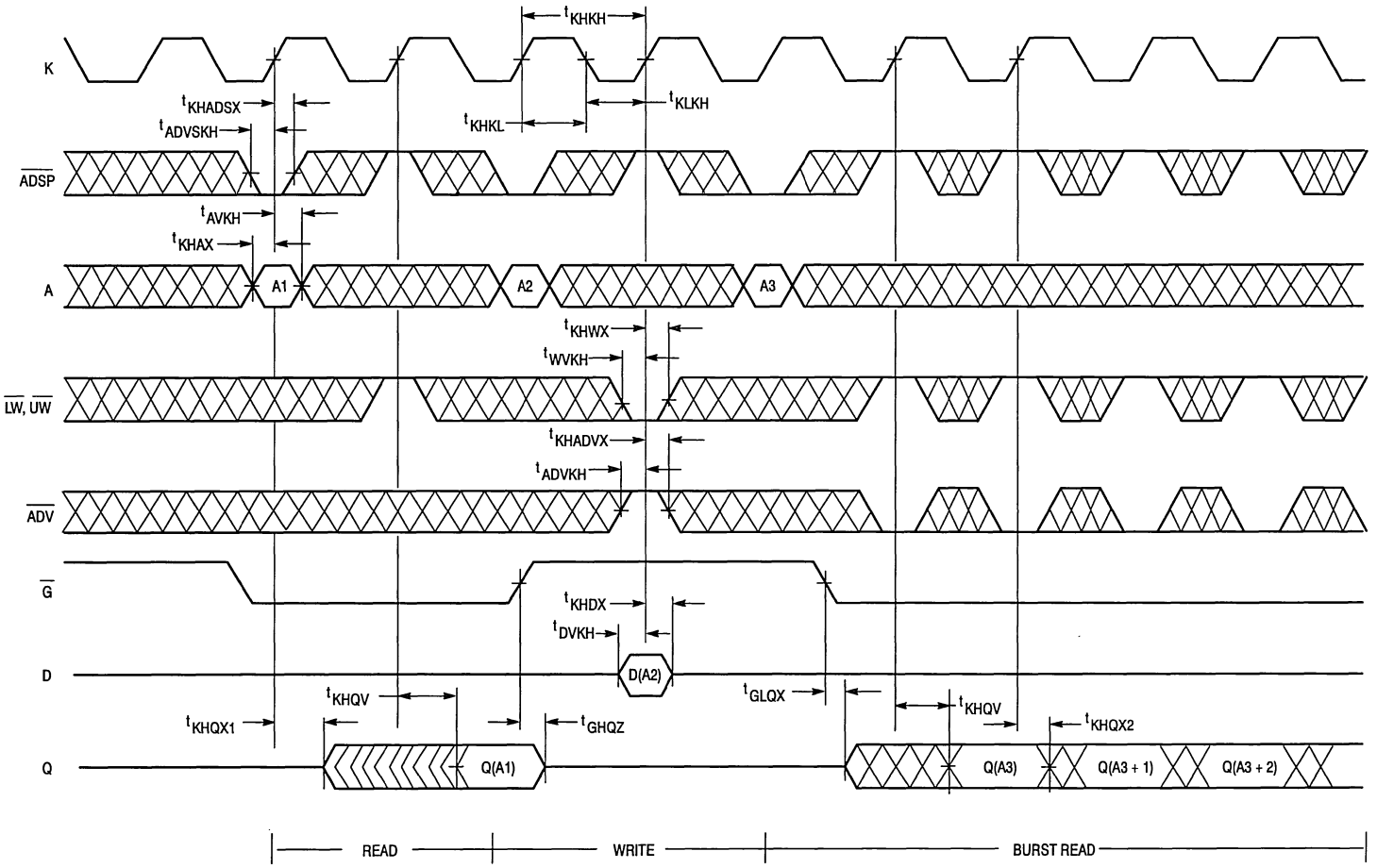
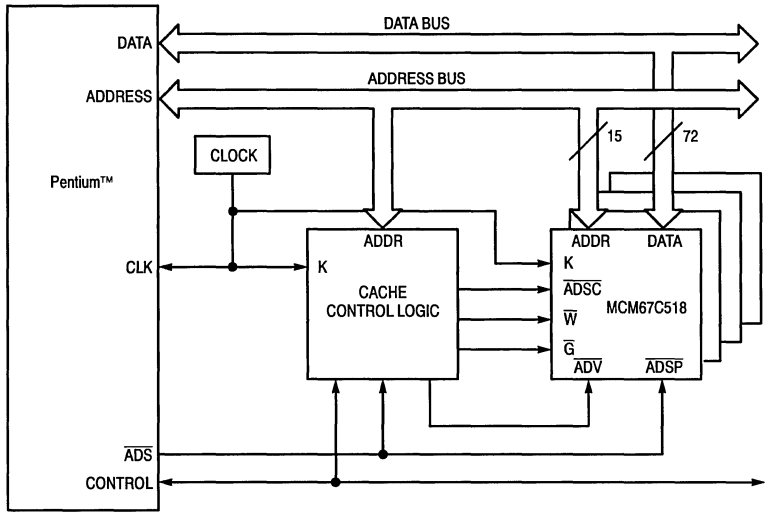
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67C518FN7s With a 75 MHz (bus speed) Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM	67C518	XX	X
Motorola Memory Prefix			Speed (6 = 6 ns, 7 = 7 ns, 9 = 9 ns)
Part Number			
		Package (FN = PLCC)	

Full Part Numbers — MCM67C518FN6 MCM67C518FN7 MCM67C518FN9

MCM67H518

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write

The MCM67H518 is a 589,824 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

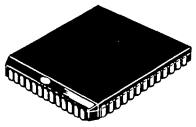
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67H518 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

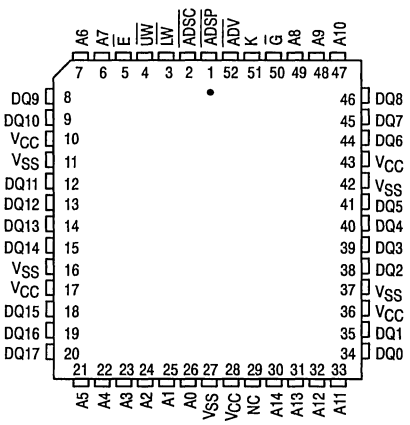
This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

5

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i486 and Pentium are trademarks of Intel Corp.

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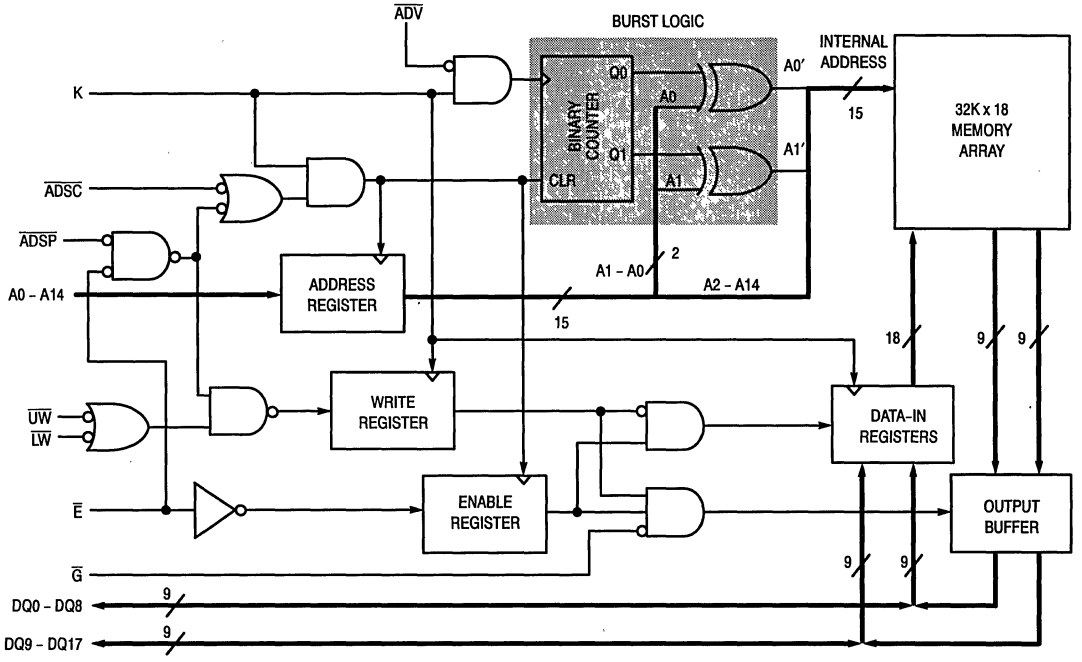
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ and $\overline{E}$ are sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$, $\overline{E}$, and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram). Note that when $\overline{E}$ and $\overline{ADSC}$ are high, $\overline{ADSP}$ is ignored – the external address is not registered in this case.
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	— — —	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67H518–9		MCM67H518–10		MCM67H518–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	6	3	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be asserted at each rising edge of clock for the device (when $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

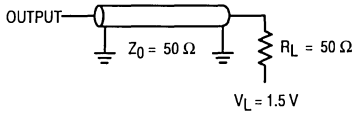


Figure 1A

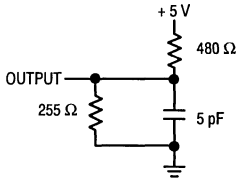
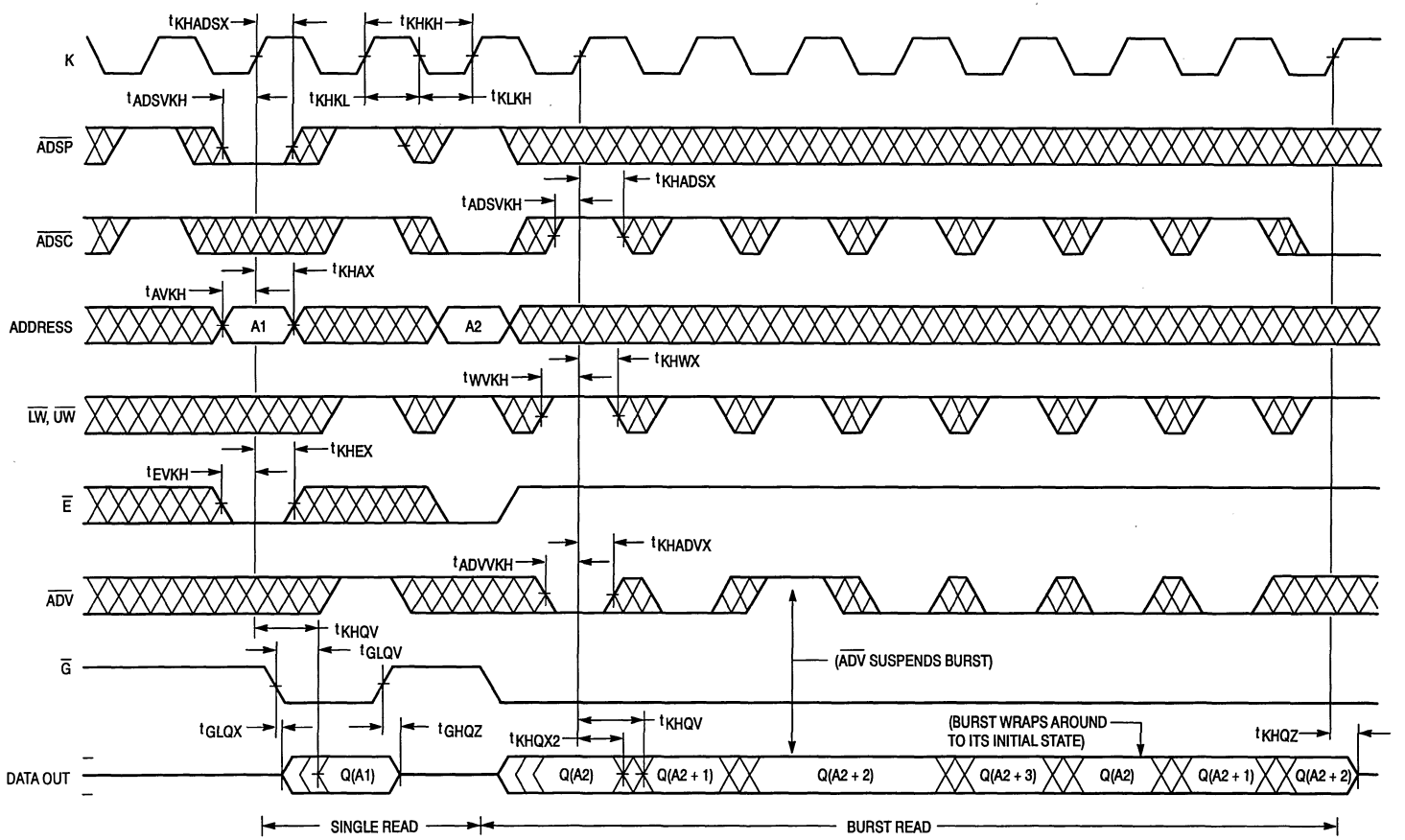


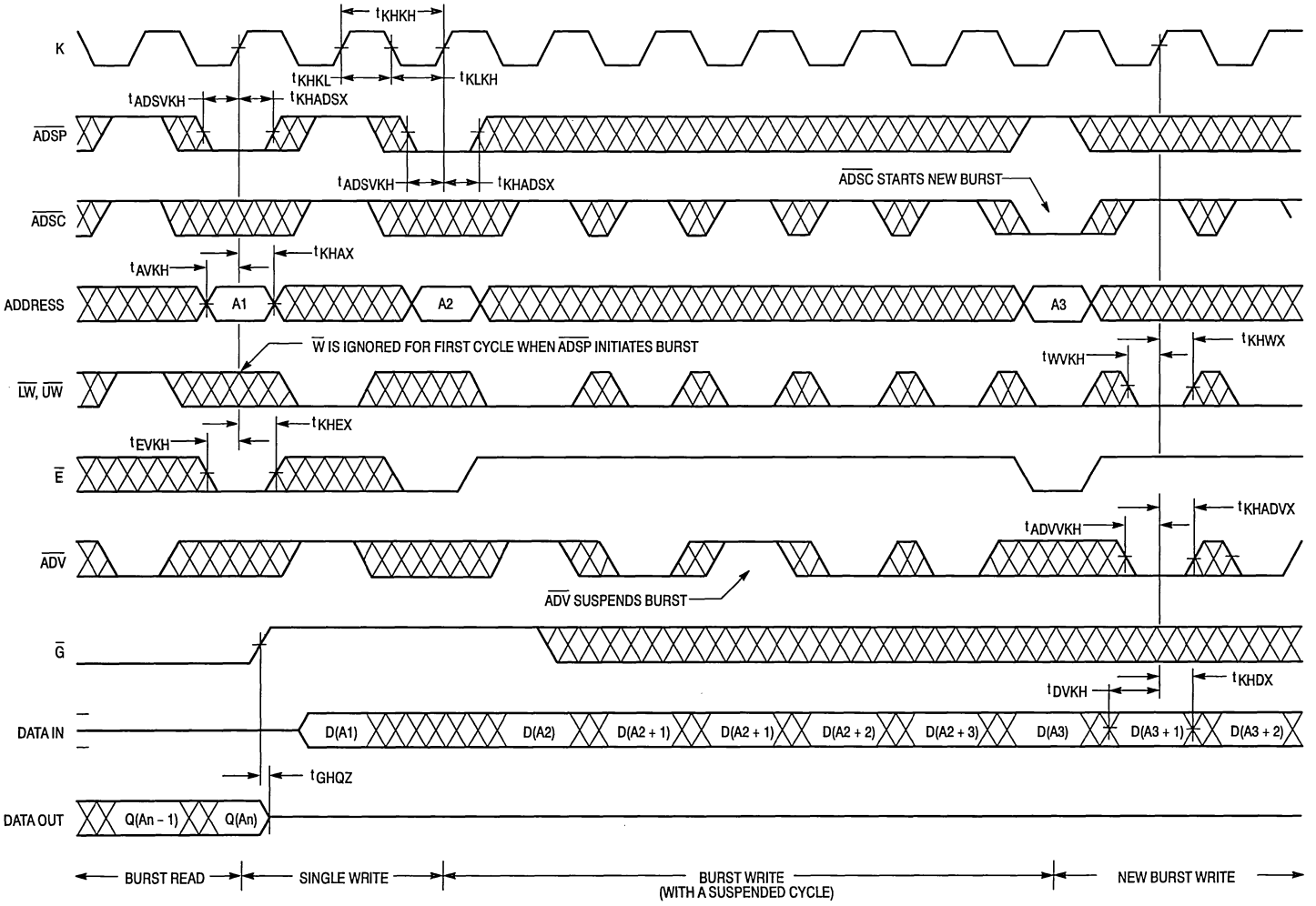
Figure 1B

READ CYCLES

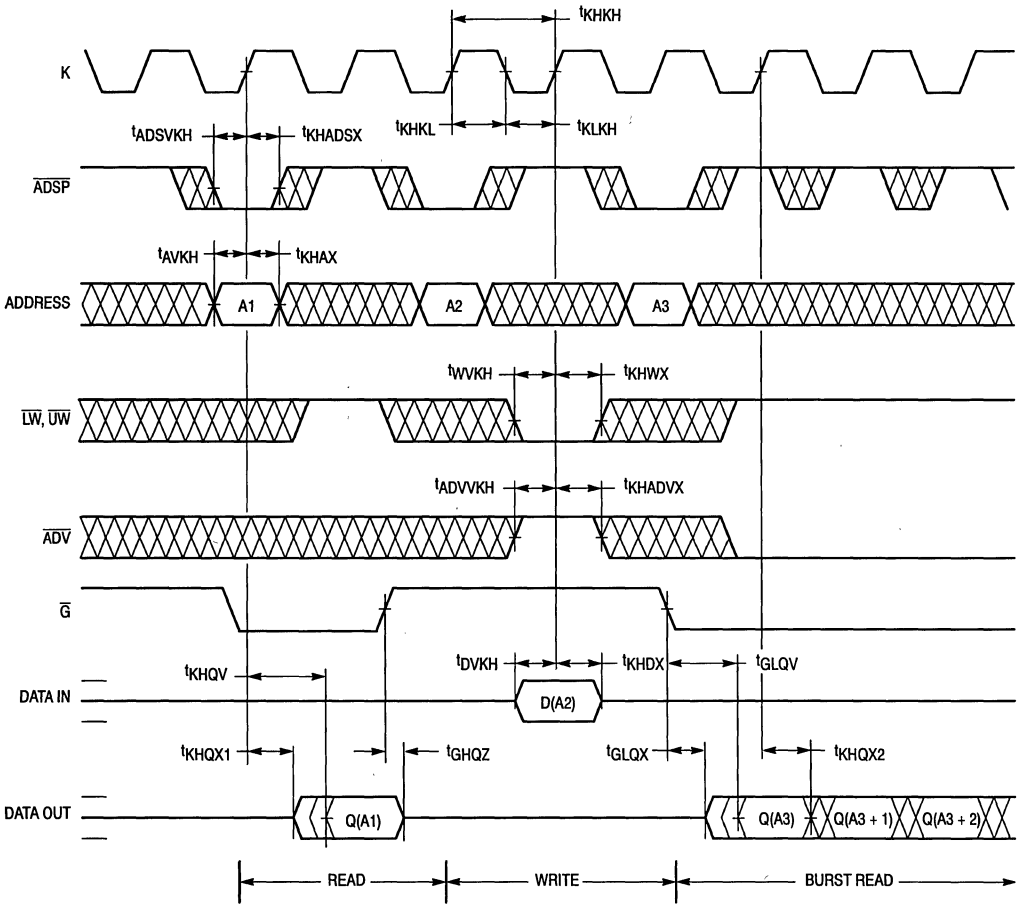


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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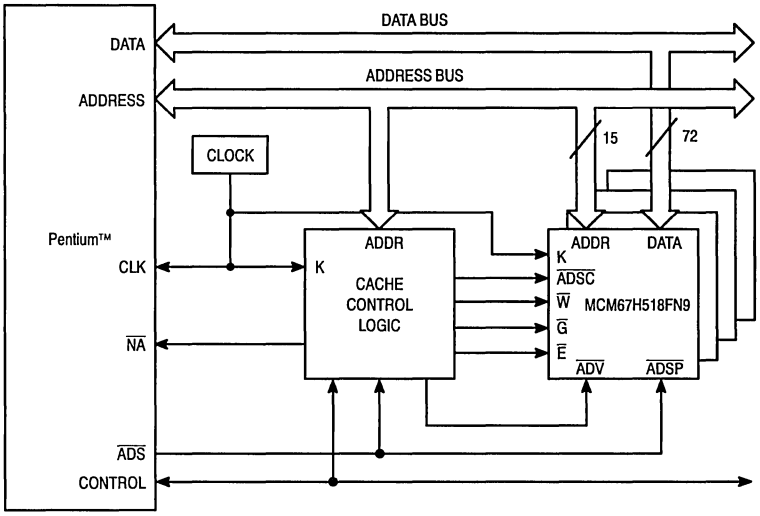
APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67H518FN9s with a 66 MHz Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

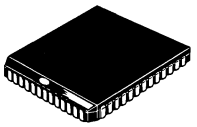
MCM	67H518	XX	XX
Motorola Memory Prefix			Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)
Part Number			Package (FN = PLCC)

Full Part Numbers — MCM67H518FN9 MCM67H518FN10 MCM67H518FN12

MCM67J518

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67J518 is a 589,824 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67J518 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

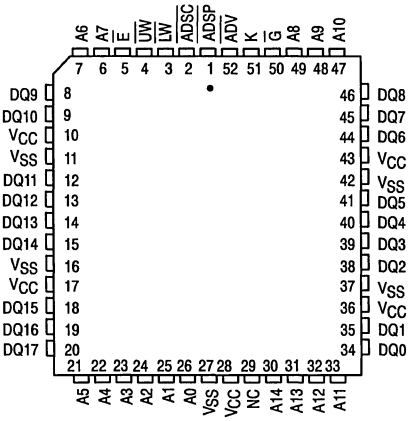
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 6 ns/100 MHz, 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

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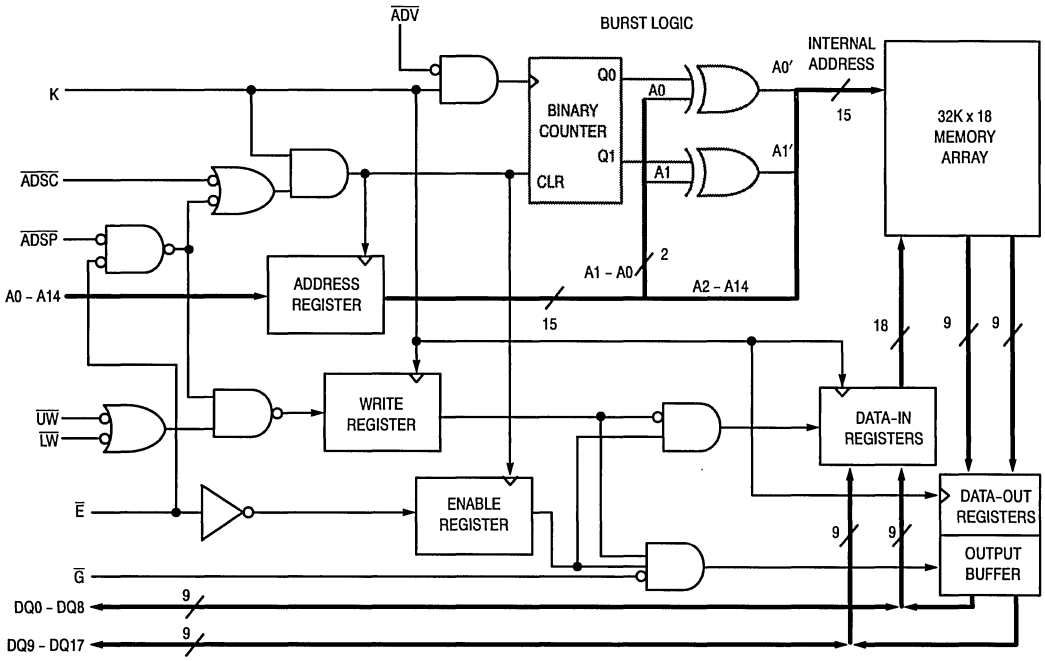
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram). When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA6} I_{CCA7} I_{CCA9}	—	310 290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486, Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67J518–6		MCM67J518–7		MCM67J518–9		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	—	6	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	2	—	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4	—	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 amd Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

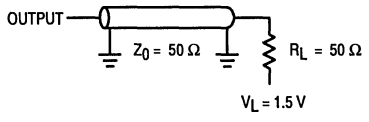


Figure 1A

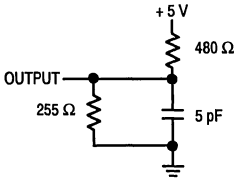
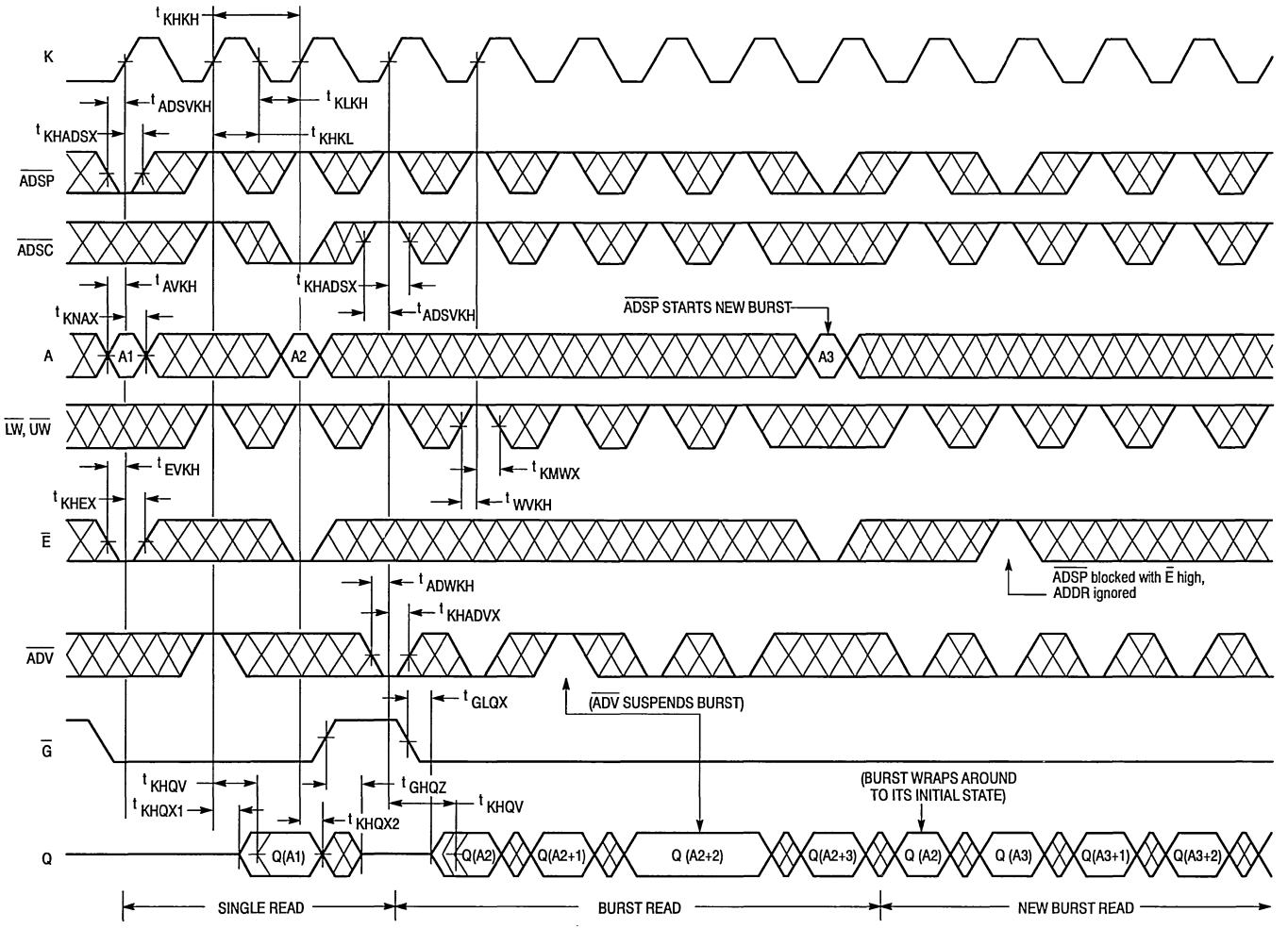
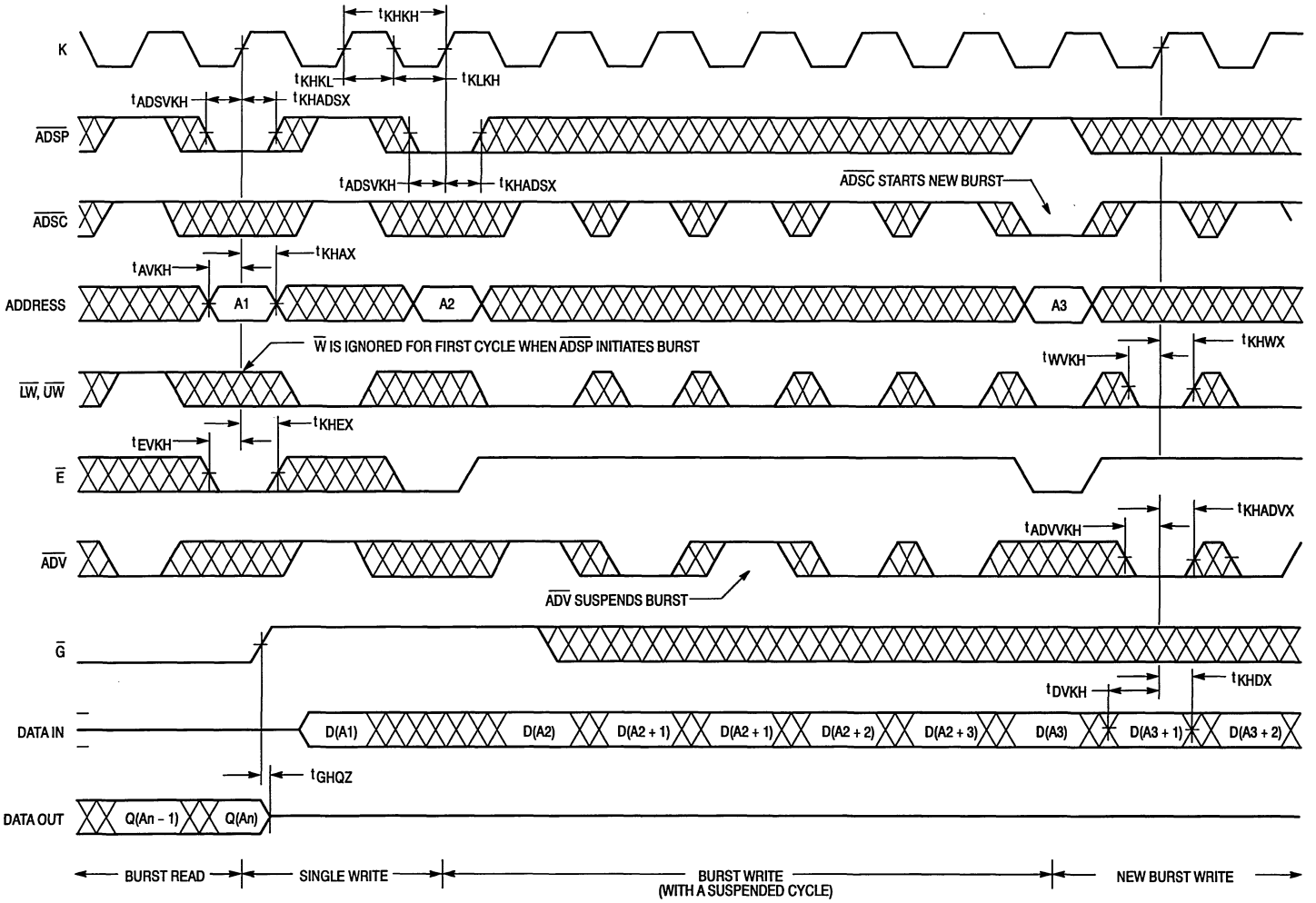


Figure 1B

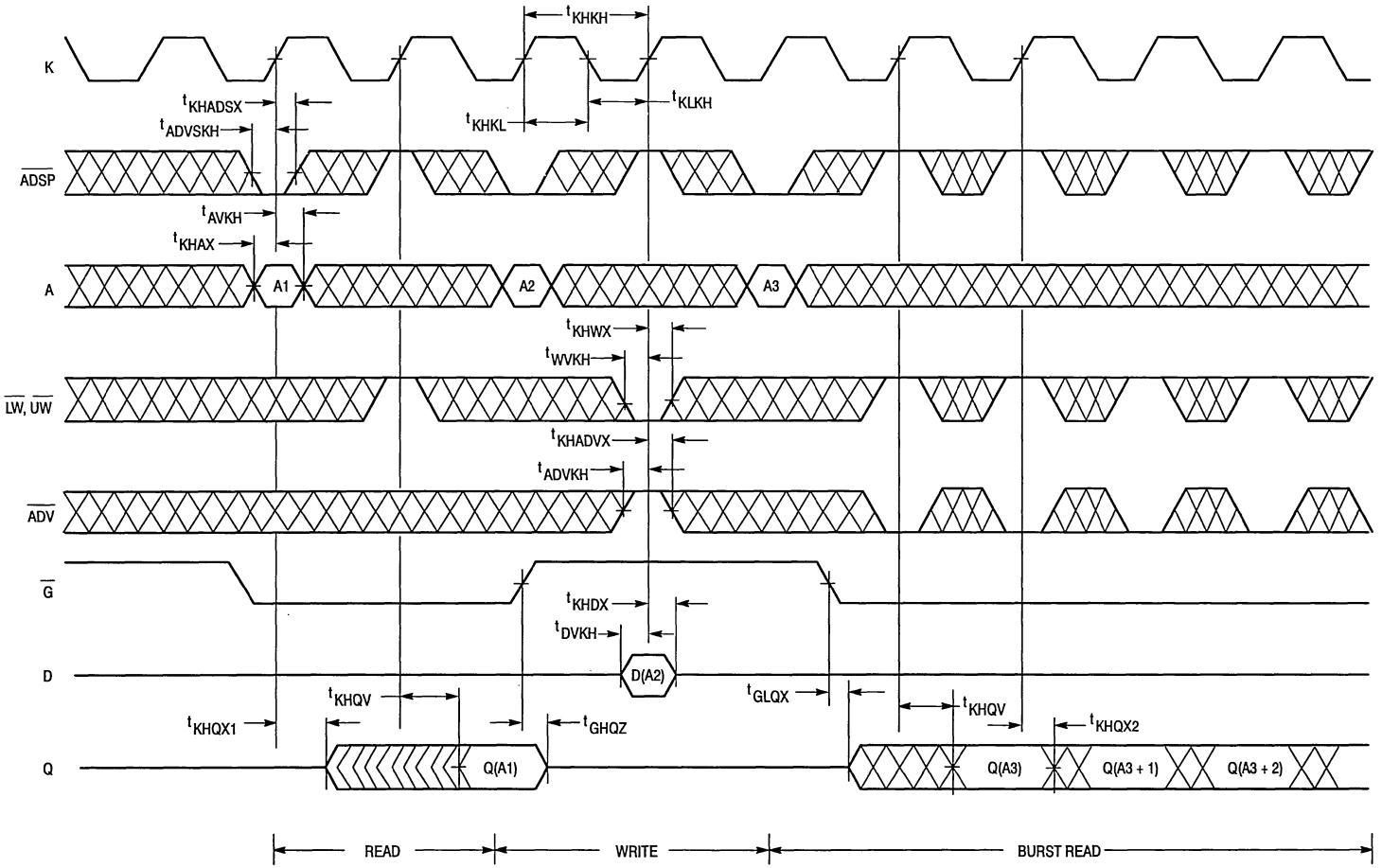
READ CYCLES


tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKHADSX
tKNAX
tADSVKH
ADSP STARTS NEW BURST
A
A1
A2
A3
LW, UW
tEVKH
tKMWX
tKHEX
tWVKH
E
tADWKH
tKHADVX
ADSP blocked with E high, ADDR ignored
ADV
tGLQX
(ADV SUSPENDS BURST)
G
tKHQV
tGHQZ
tKHQV
tKHQX1
tKHQX2
(BURST WRAPS AROUND TO ITS INITIAL STATE)
Q
Q(A1)
Q(A2)
Q(A2+1)
Q (A2+2)
Q(A2+3)
Q (A2)
Q (A3)
Q(A3+1)
Q(A3+2)
SINGLE READ
BURST READ
NEW BURST READ

WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



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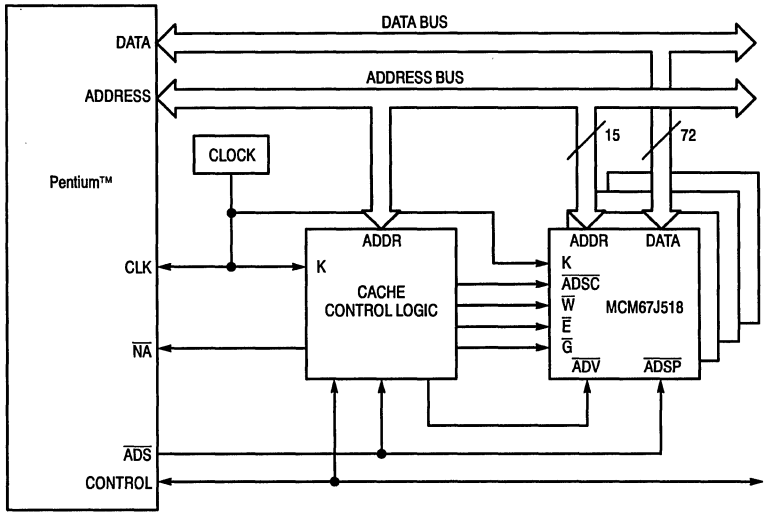
APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache Using
Four MCM67J518FN7s with a 75 MHz (Bus Speed) Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM	67J518	XX	X
Motorola Memory Prefix			Speed (6 = 6 ns, 7 = 7 ns, 9 = 9 ns)
Part Number			Package (FN = PLCC)

Full Part Numbers — MCM67J518FN6 MCM67J518FN7 MCM67J518FN9

MCM67M518

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write

The MCM67M518 is a 589,824 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ17), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive–edge–triggered noninverting registers.

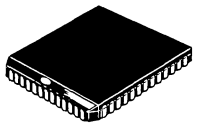
Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM67M518 (burst sequence imitates that of the MC68040 and PowerPC) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

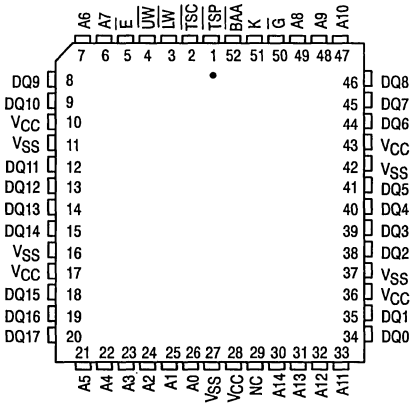
This device is ideally suited for systems that require wide data bus widths and cache memory.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/11/14 ns Max and Cycle Times: 12.5/15/20 ns Min
- Byte Writeable via Dual Write Strobes
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Board Density 52–PLCC Package
- 3.3 V I/O Compatible



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENT



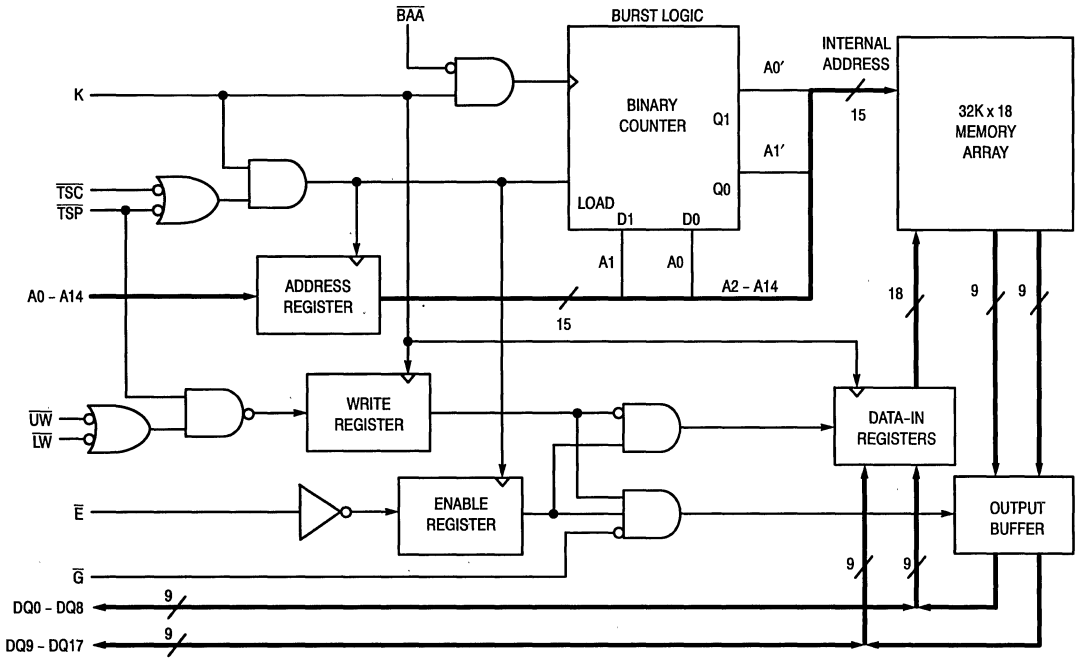
PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{BAA}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

REV 3
5/95

BLOCK DIAGRAM (See Note)



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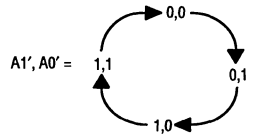
NOTE: All registers are positive–edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. Alternatively, a $\overline{TSP}$–initiated two cycle WRITE can be performed by asserting $\overline{TSP}$ and a valid address on the first cycle, then negating both $\overline{TSP}$ and $\overline{TSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA11} I_{CCA14}	—	290 275 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible MC68040 and PowerPC bus cycles.

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CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67M518–9		MCM67M518–11		MCM67M518–14		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12.5	—	15	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	11	—	14	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	6
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{TSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{BAVKH}								
Chip Select	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHTSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHBAX}								
Chip Select	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected. Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

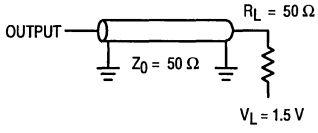


Figure 1A

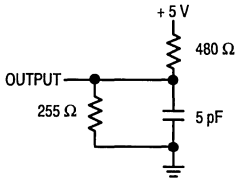
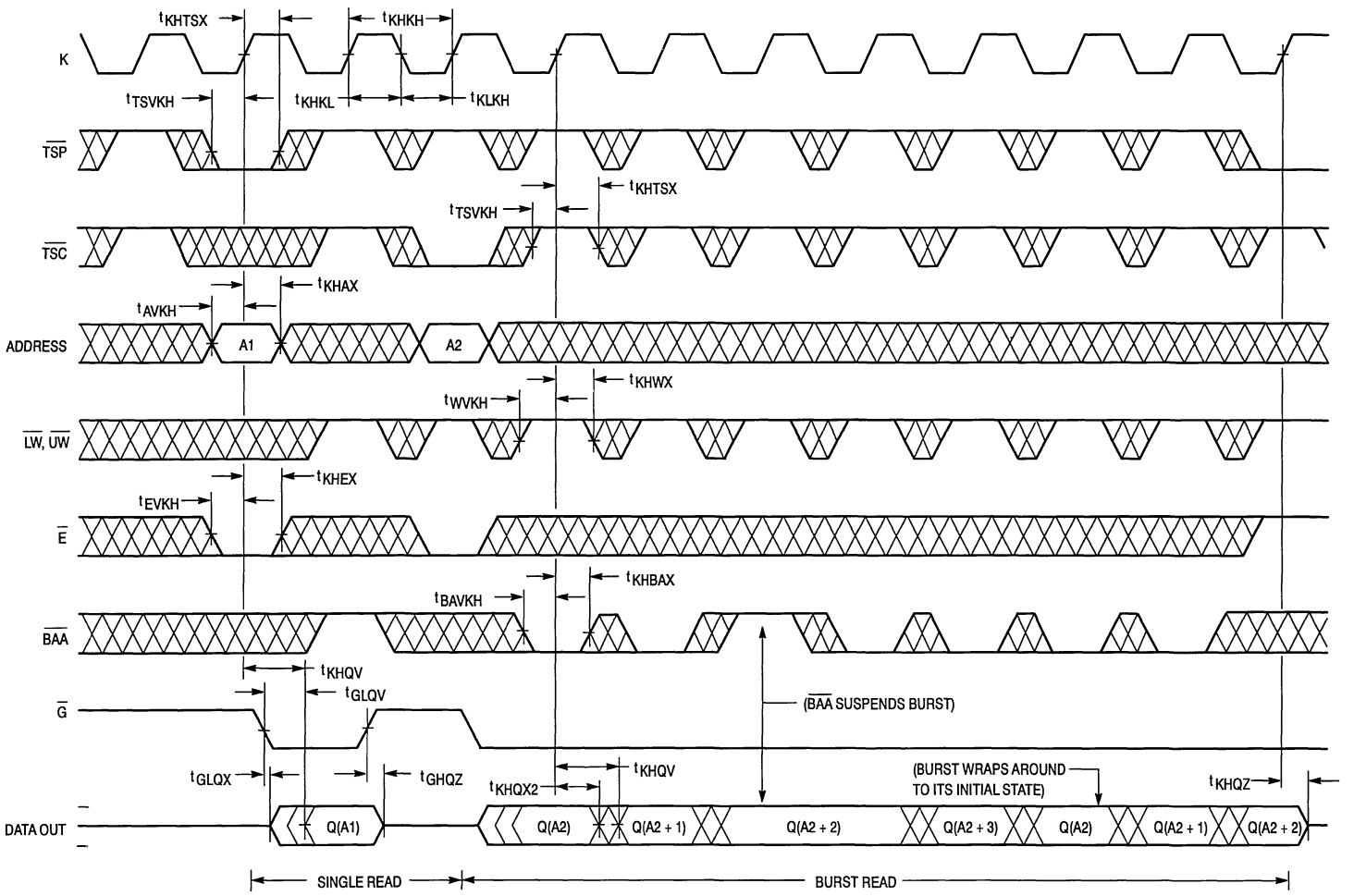


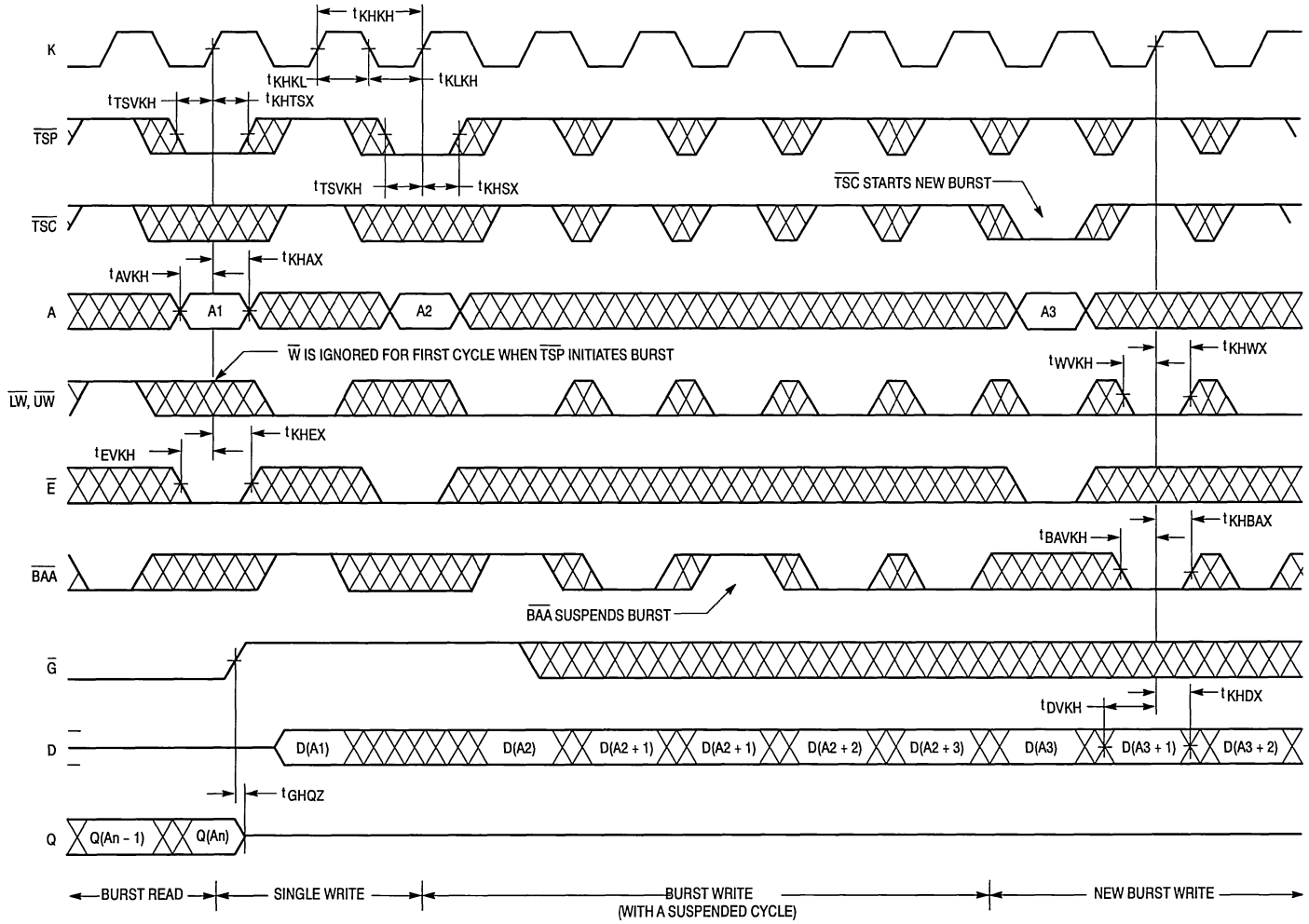
Figure 1B

READ CYCLES

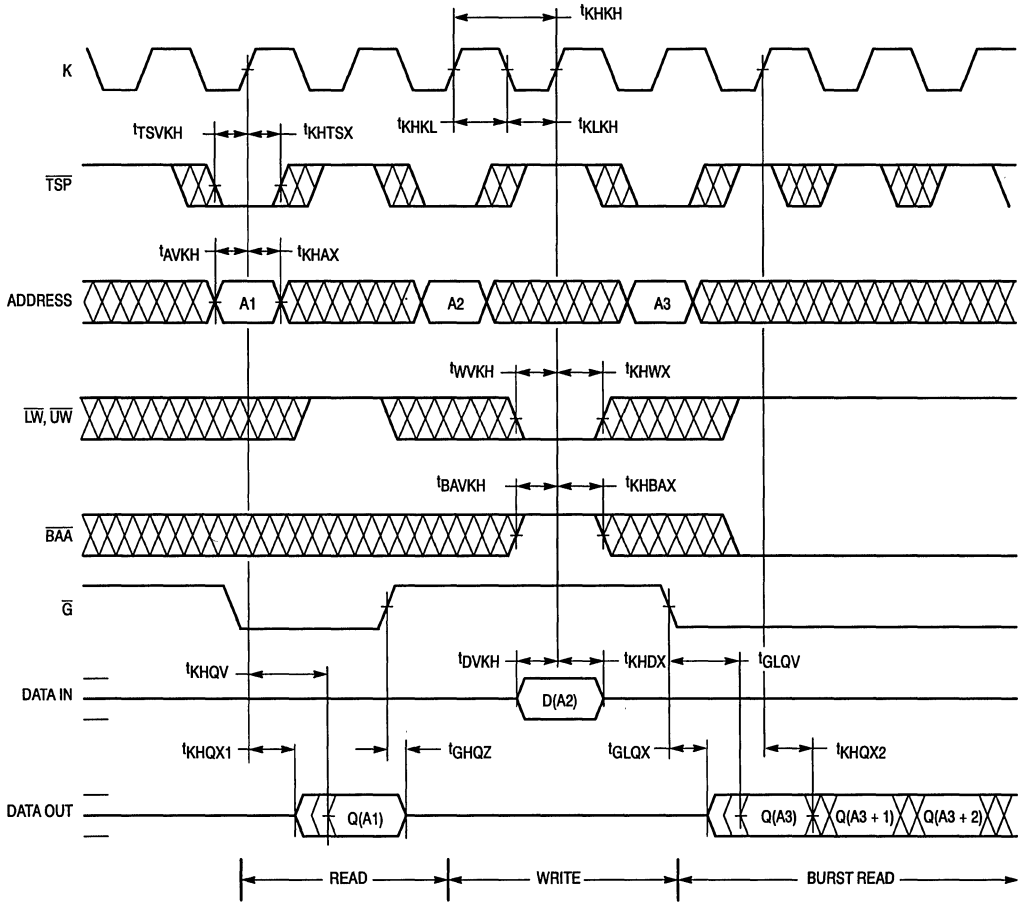


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{TSC}$ high)



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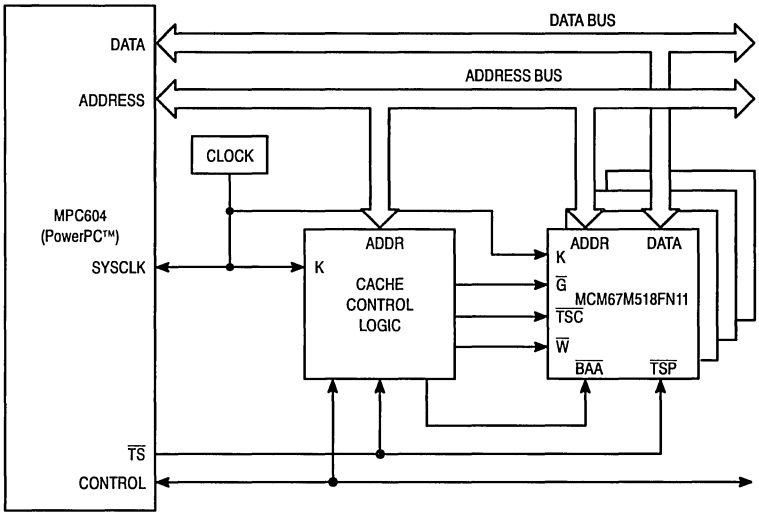
APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67M518FN11s with a 66 MHz (bus speed) MPC604 PowerPC™

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67M518 XX XX

Motorola Memory Prefix

Part Number

Speed (9 = 9 ns, 11 = 11 ns, 14 = 14 ns)

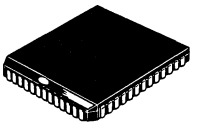
Package (FN = PLCC)

Full Part Numbers — MCM67M518FN9 MCM67M518FN11 MCM67M518FN14

MCM67B618

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67B618 is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67B618 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

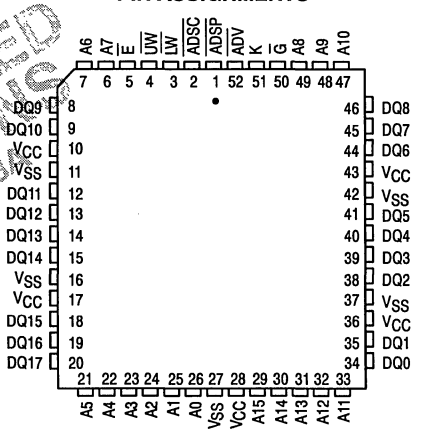
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENTS



PIN NAMES

A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

REV 7
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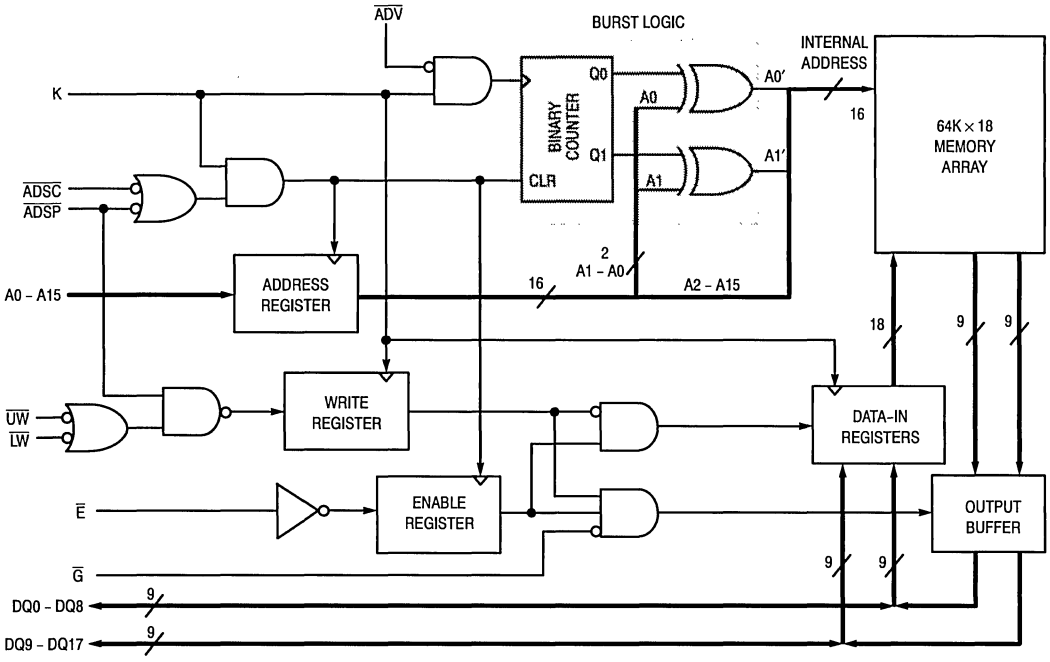
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

5

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	—	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67B618–9		MCM67B618–10		MCM67B618–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

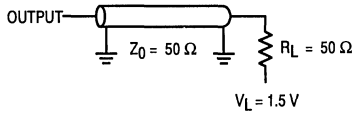


Figure 1A

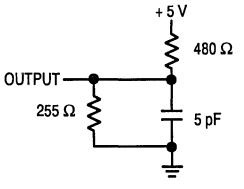
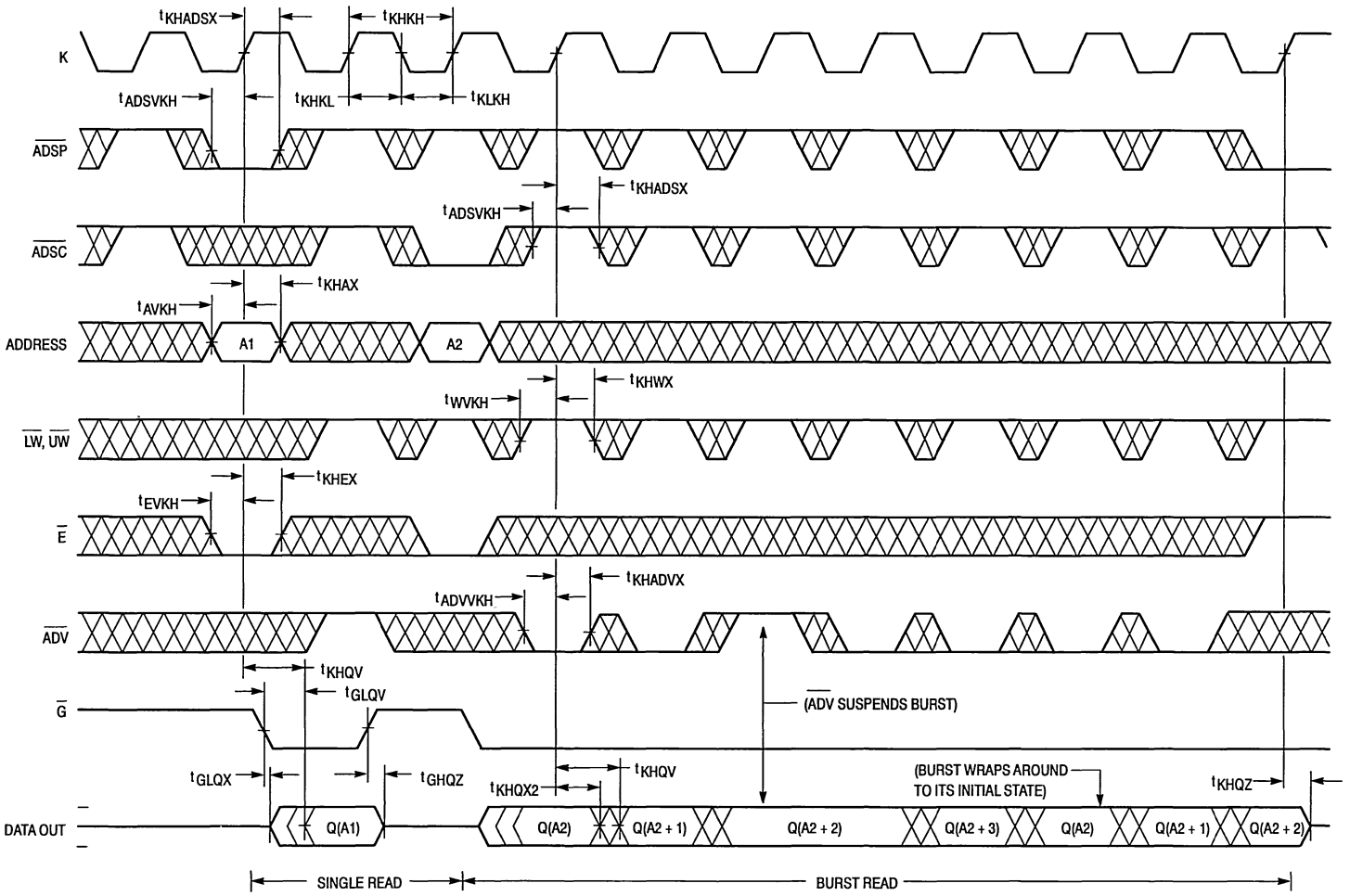


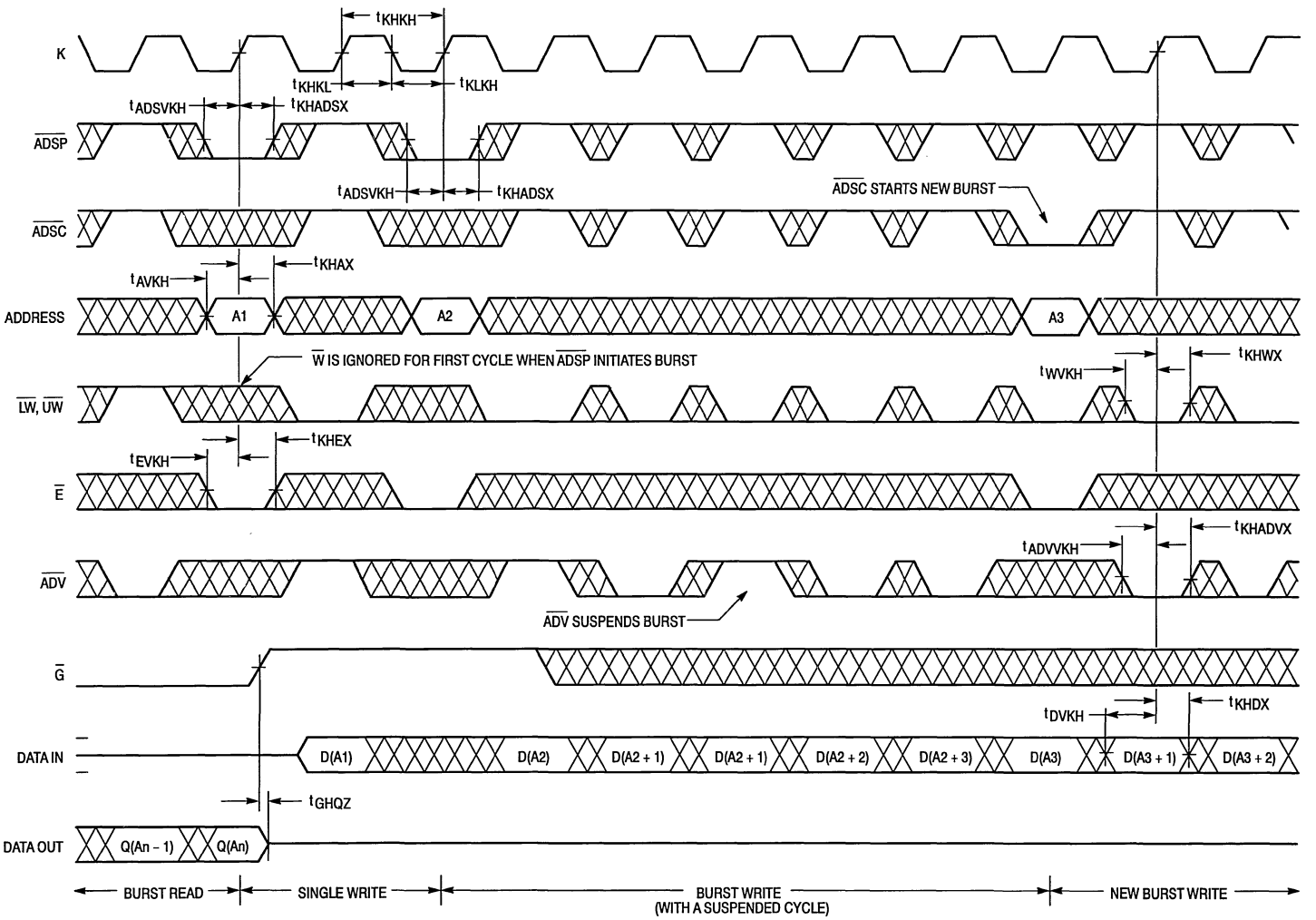
Figure 1B

READ CYCLES

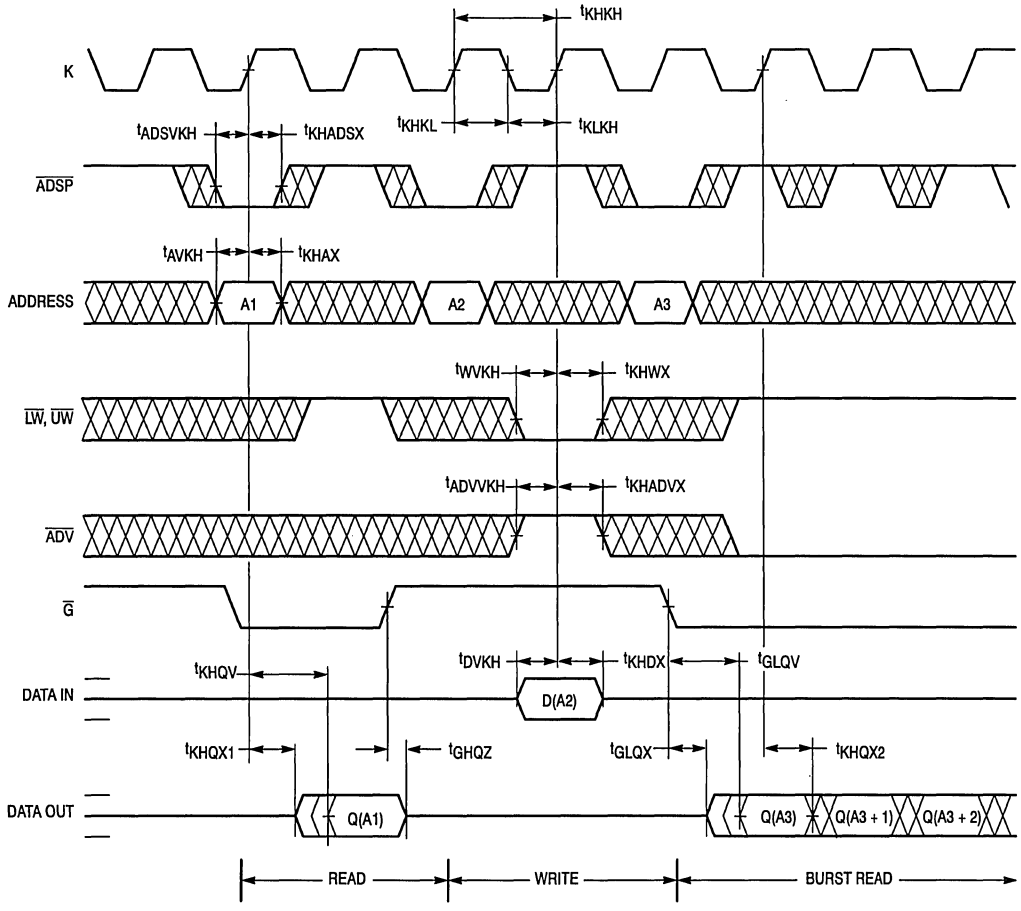


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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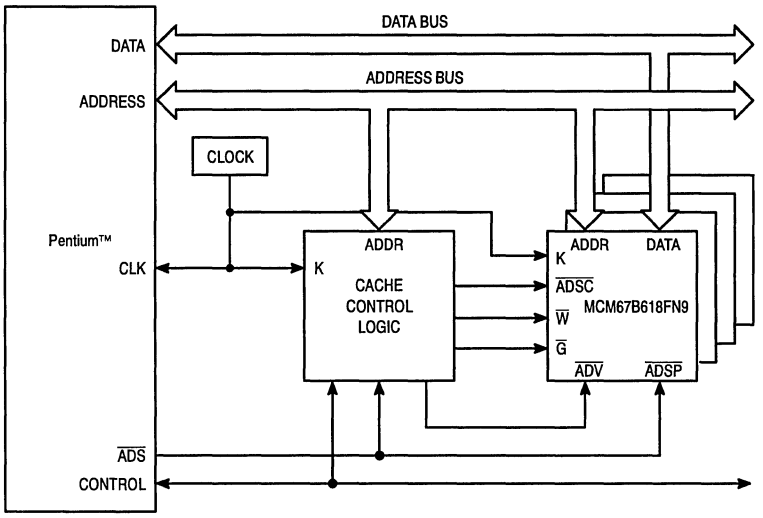
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67B618FN9s with a 66 MHz (bus speed) Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67B618 XX XX

Motorola Memory Prefix — MCM
Part Number — 67B618
Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns) — XX
Package (FN = PLCC) — XX

Full Part Numbers — MCM67B618FN9 MCM67B618FN10 MCM67B618FN12

MCM67B618A

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write

The MCM67B618A is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

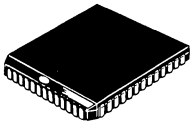
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67B618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

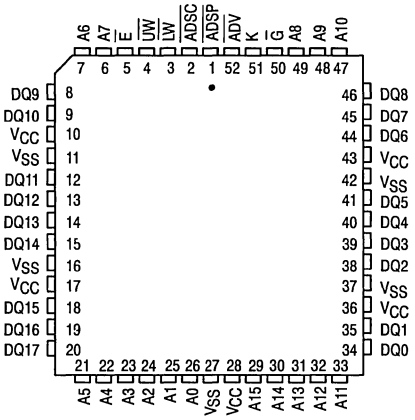
This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package



FN PACKAGE
PLASTIC
CASE 778–02

PIN ASSIGNMENTS



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

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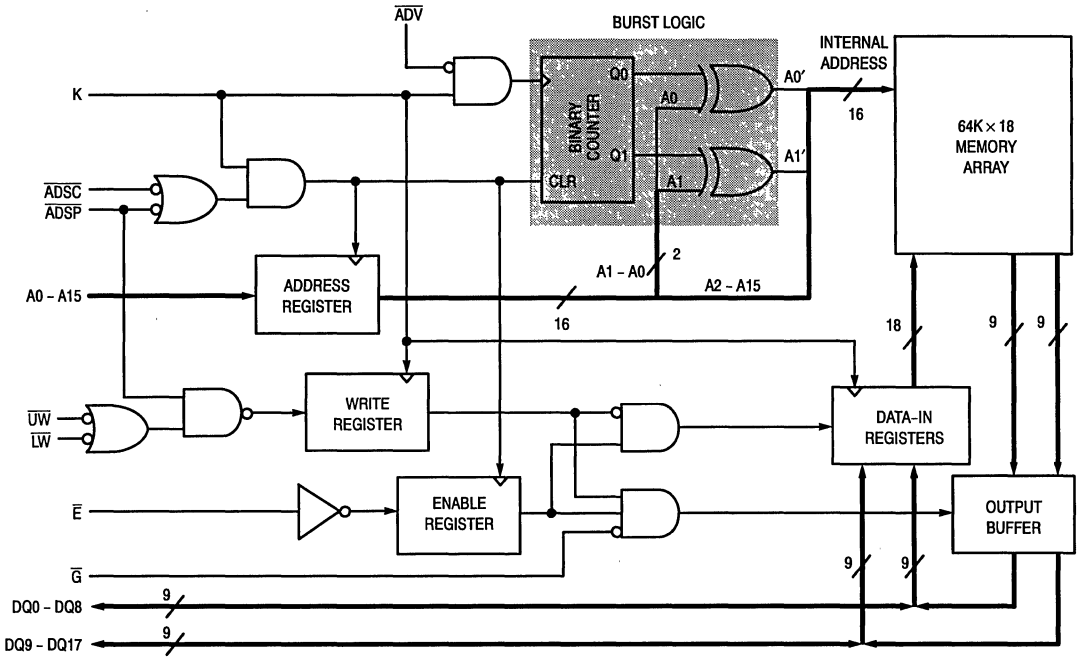
BLOCK DIAGRAM (See Note)



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NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	—	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67B618A–9		MCM67B618A–10		MCM67B618A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	—	7	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

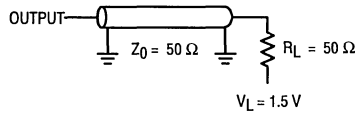

Figure 1A

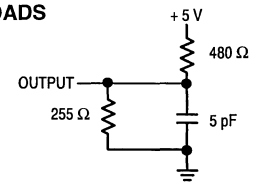

Figure 1B

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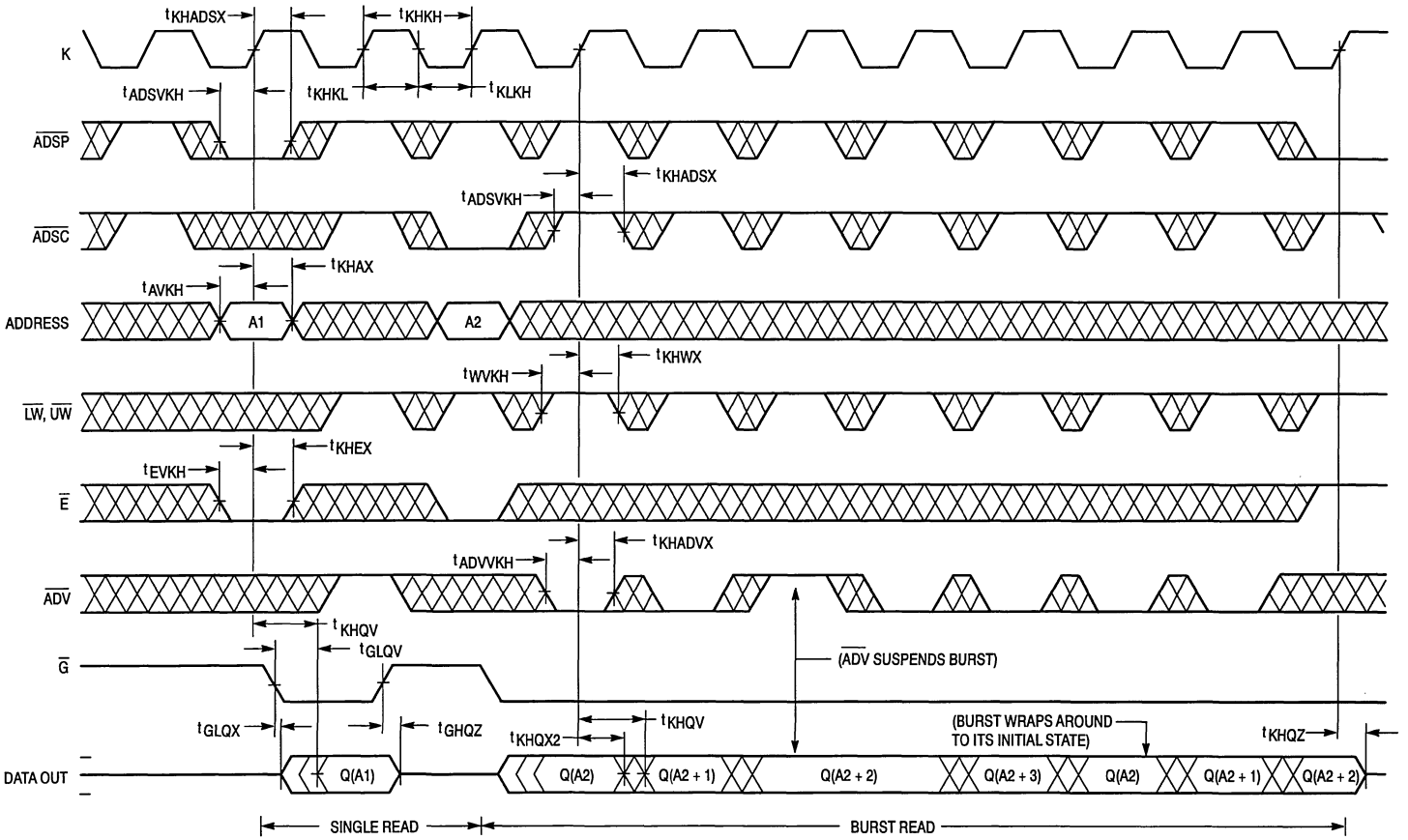
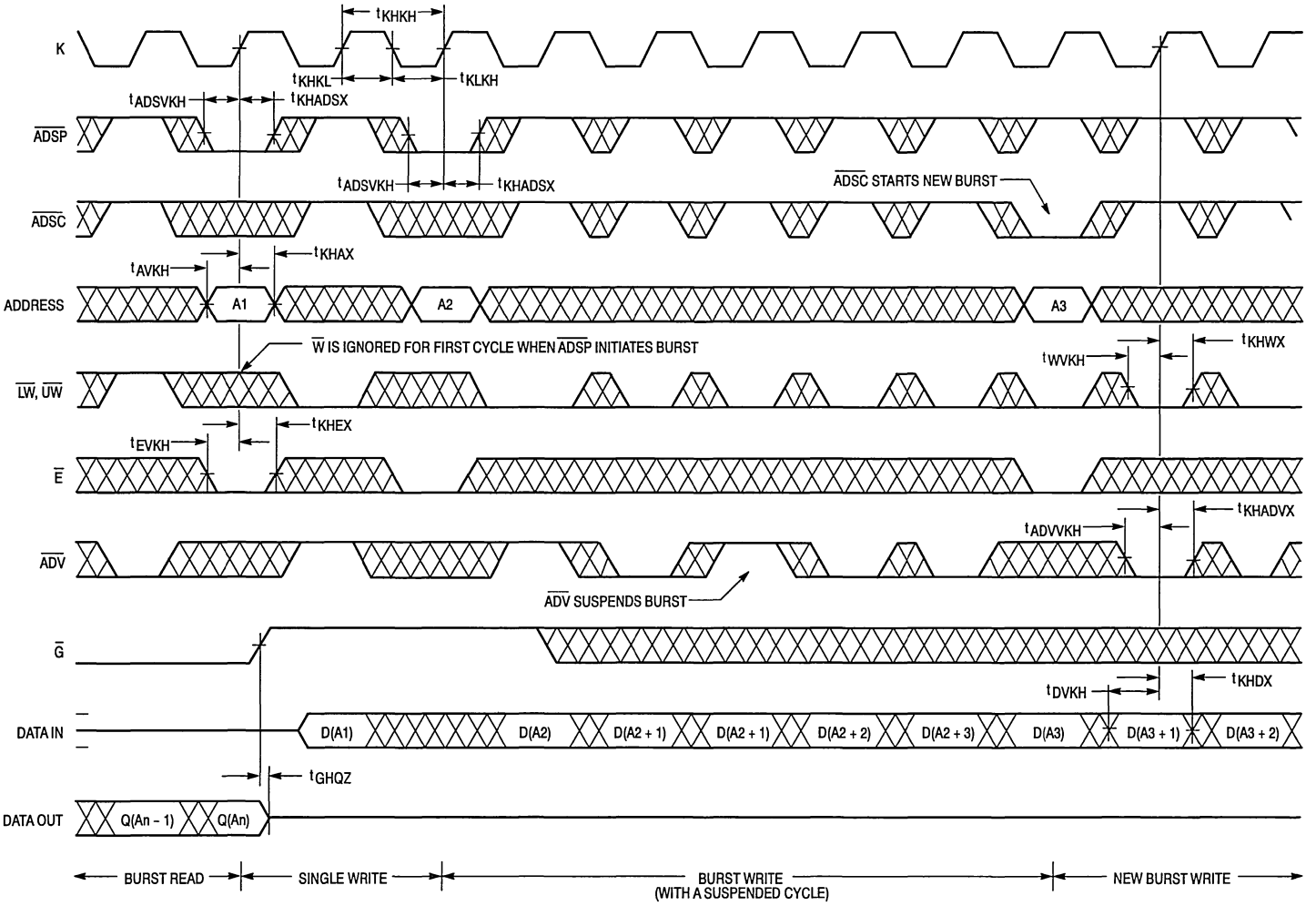
READ CYCLES

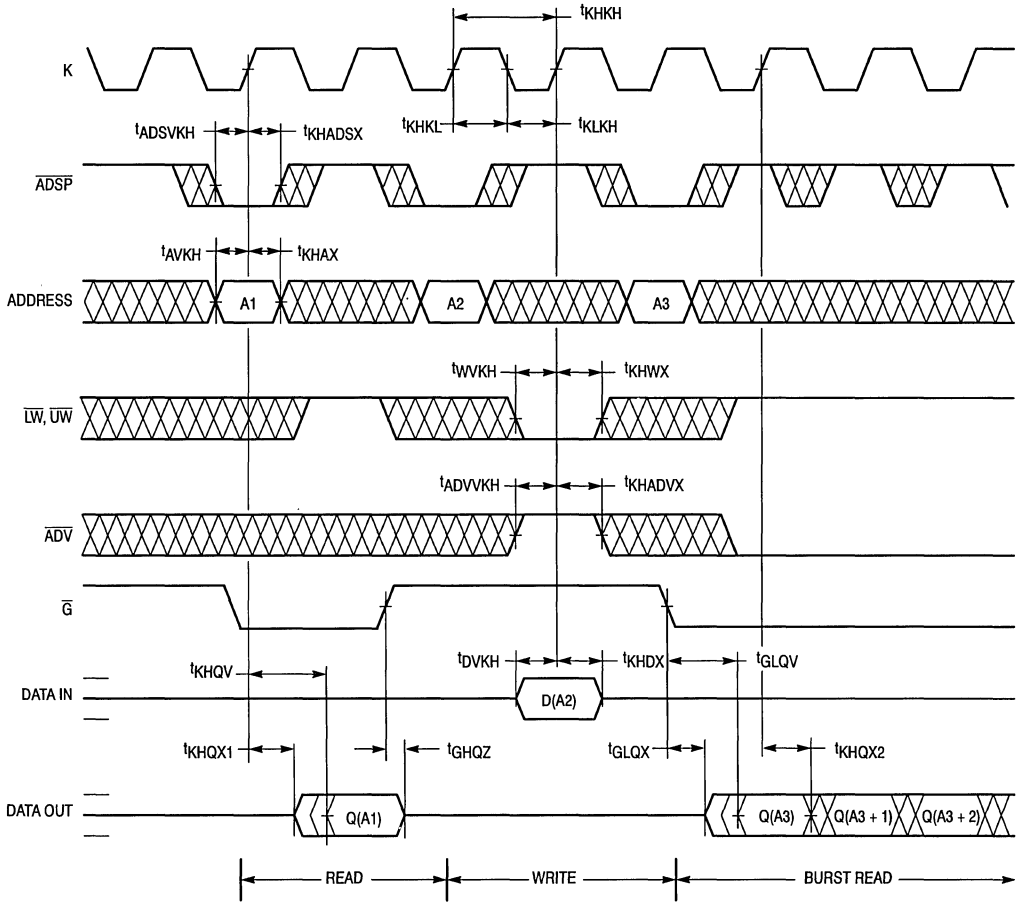


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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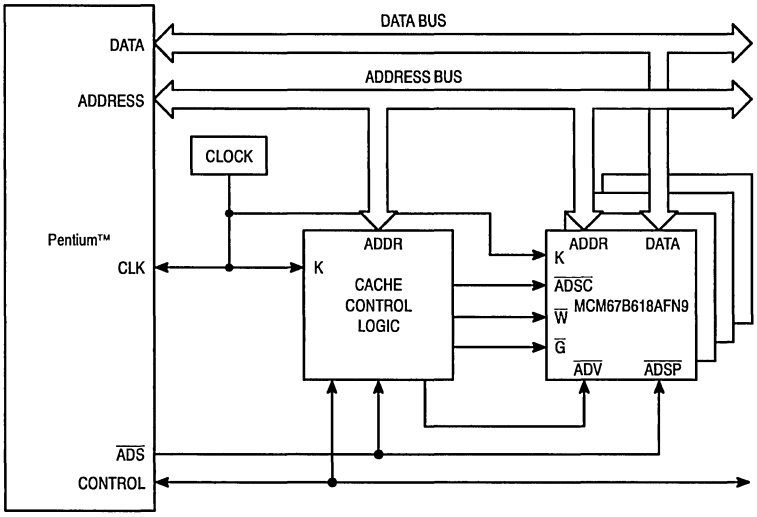
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67B618AFN9s with a 66 MHz Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67B618A XX XX

Motorola Memory Prefix

Part Number

Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns)

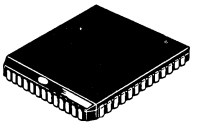
Package (FN = PLCC)

Full Part Numbers — MCM67B618AFN9 MCM67B618AFN10 MCM67B618AFN12

MCM67C618

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67C618 is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered non-inverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67C618 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

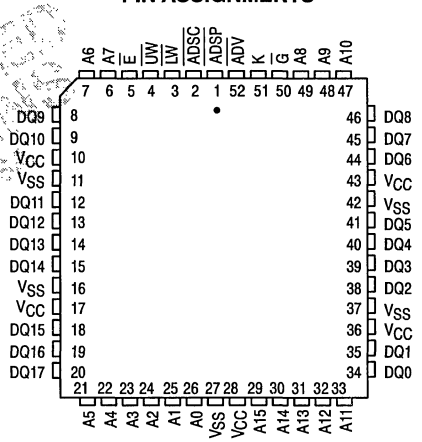
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 6 ns/100 MHz, 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENTS



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

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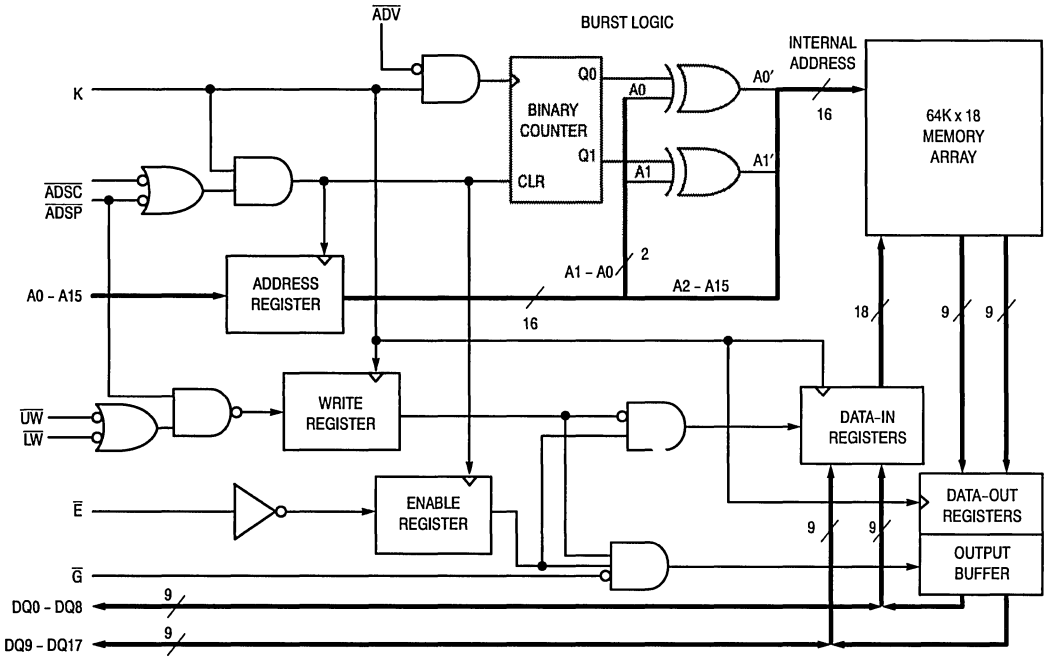
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

5

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA6} I_{CCA7} I_{CCA9}	—	310 290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67C618–6		MCM67C618–7		MCM67C618–9		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	—	6	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	2	—	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4.5	—	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4.5	—	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

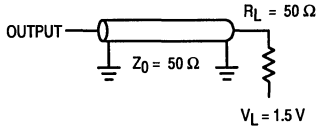


Figure 1A

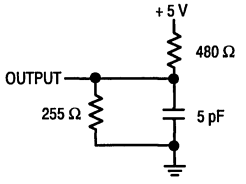
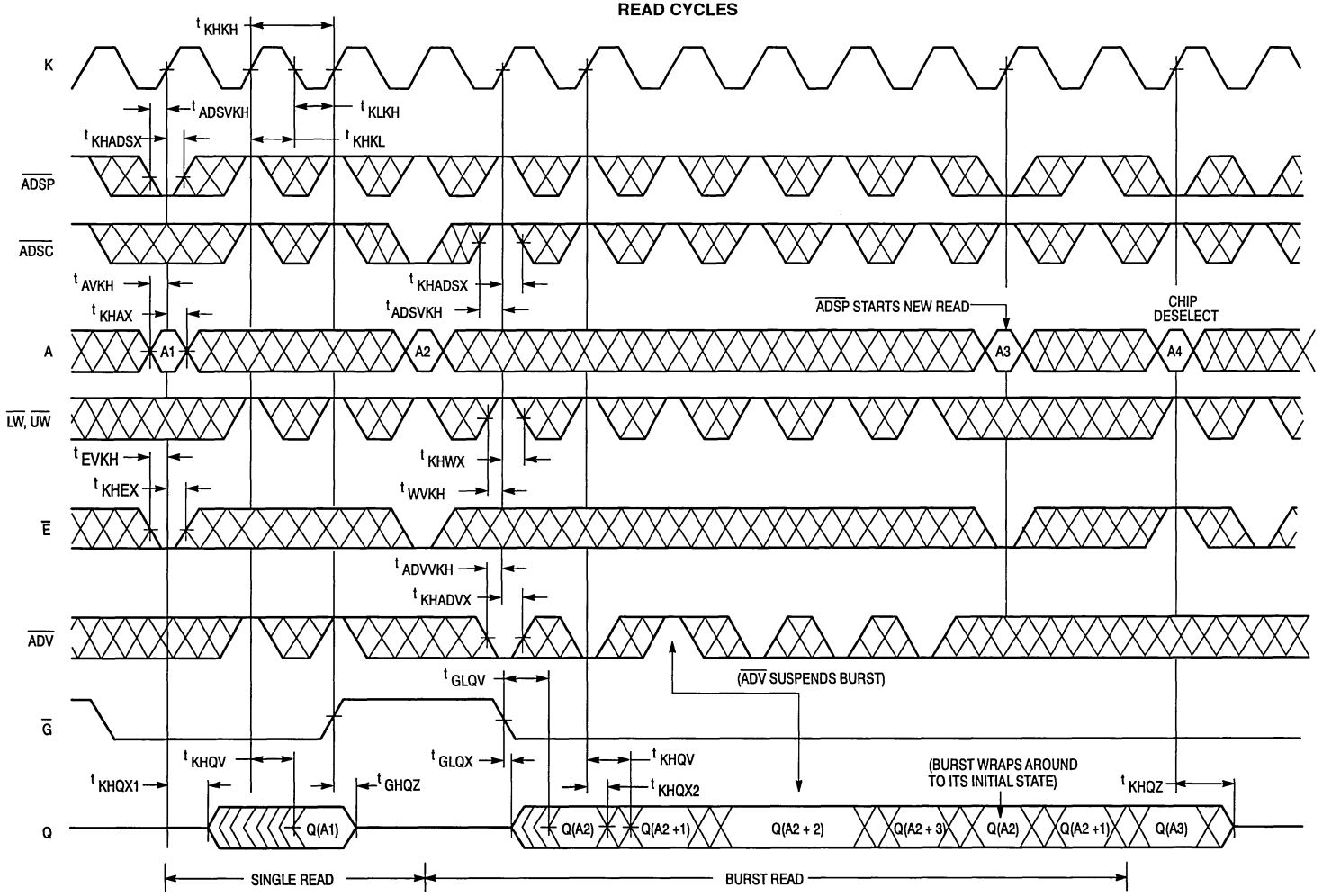
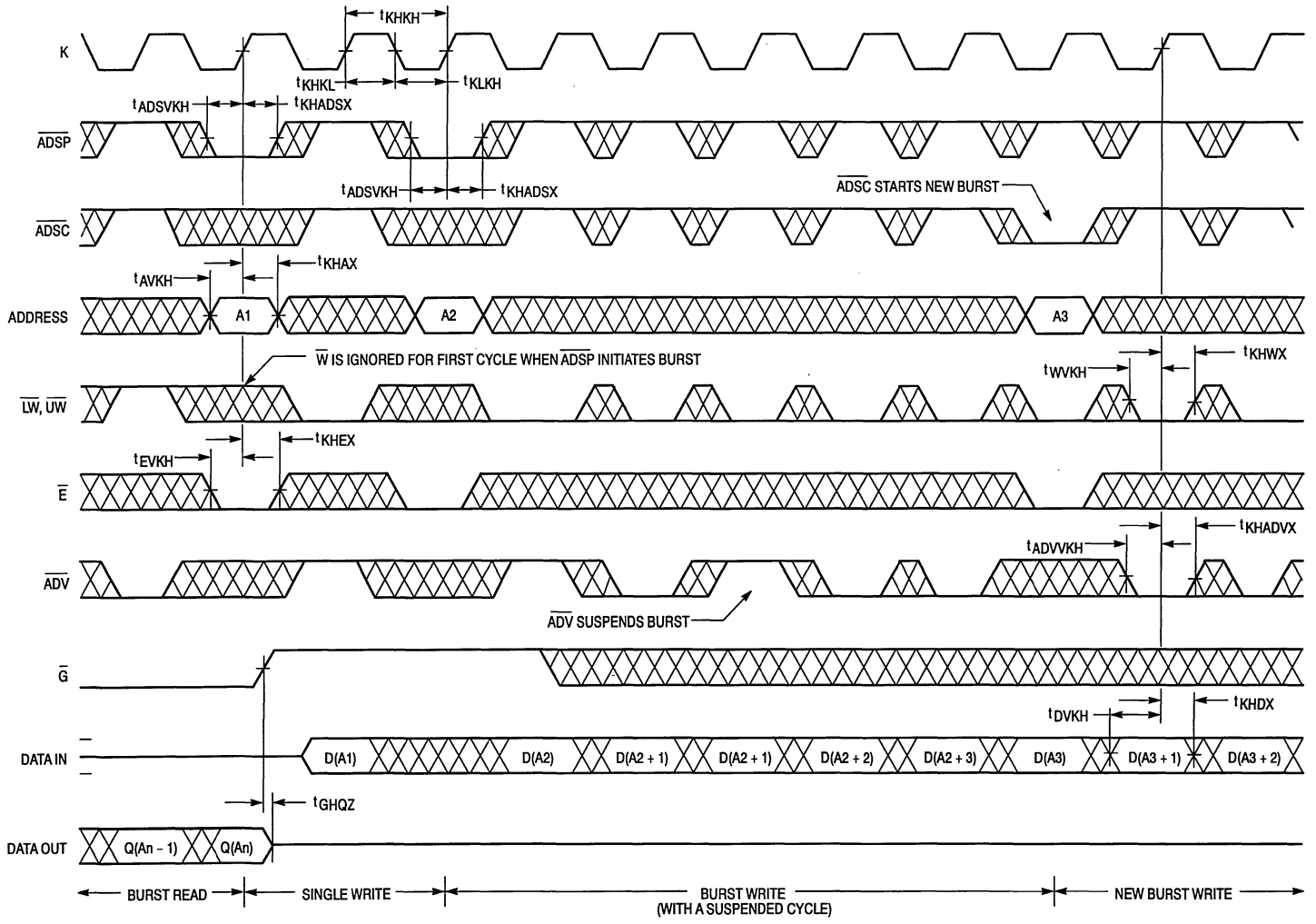


Figure 1B

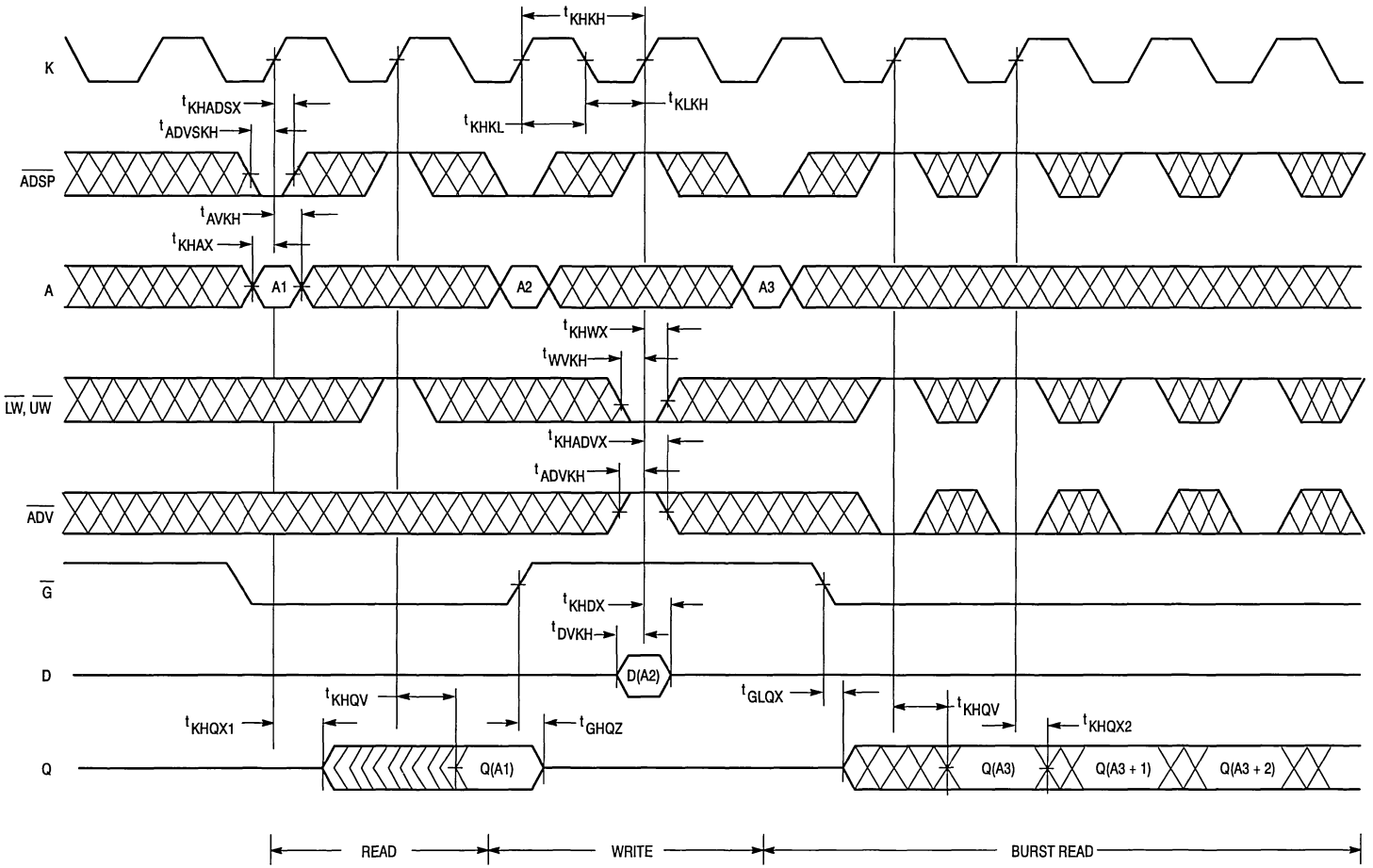
READ CYCLES


tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKHAX
tKHADSX
tADSVKH
ADSP STARTS NEW READ
CHIP DESELECT
A
A1
A2
A3
A4
LW, UW
tEVKH
tKHEX
tKHWX
tWVKH
E
tADVVKH
tKHADVX
ADV
(ADV SUSPENDS BURST)
tGLQV
G
tKHQV
tGLQX
tKHQV
tKHQX1
tGHQZ
tKHQX2
(BURST WRAPS AROUND TO ITS INITIAL STATE)
tKHQZ
Q
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
SINGLE READ
BURST READ

WRITE CYCLES

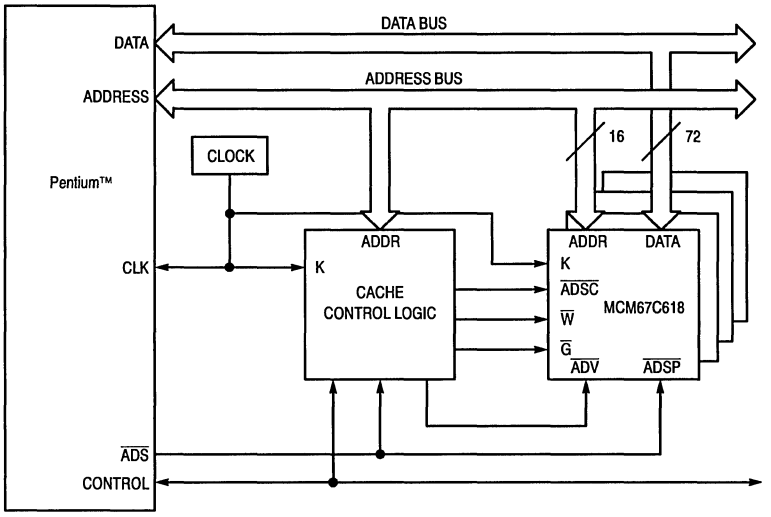


COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



5

APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache Using
Four MCM67C618FN7s With a 75 MHz (bus speed) Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM	67C618	XX	X
Motorola Memory Prefix	Part Number	Package (FN = PLCC)	Speed (6 = 6 ns, 7 = 7 ns, 9 = 9 ns)

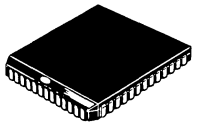
Full Part Number — MCM67C618FN6 MCM67C618FN7 MCM67C618FN9

MCM67C618A

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67C618A is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered non-inverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67C618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

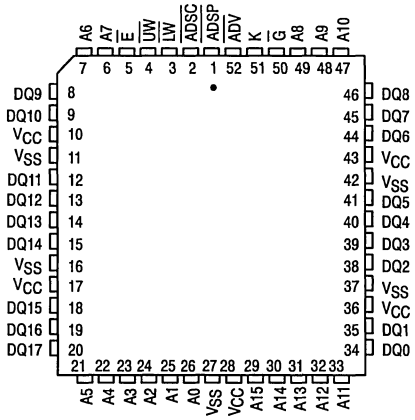
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 5 ns/100 MHz, 7 ns/80 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package

PIN ASSIGNMENTS



PIN NAMES

A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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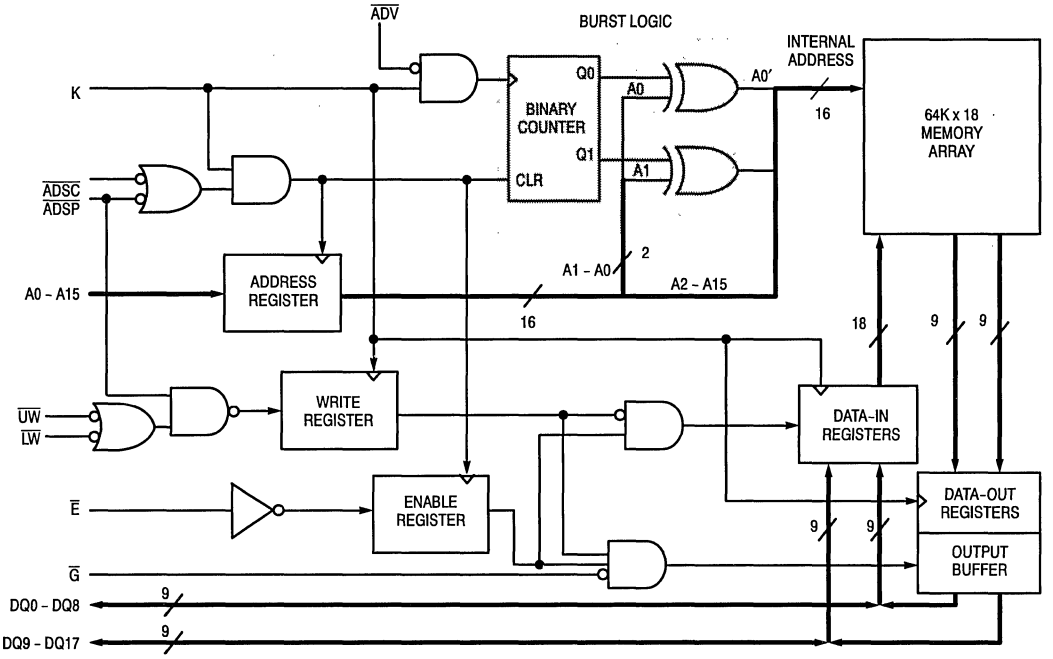
i486 and Pentium are trademarks of Intel Corp.

REV 1
5/95

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA5} I_{CCA7}	—	310 290	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67C618A–5		MCM67C618A–7		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	7	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4.5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}						
Data In	t_{DVKH}						
Write	t_{WVKH}						
Address Advance	t_{ADVVKH}						
Chip Enable	t_{EVKH}						
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}						
Data In	t_{KHDX}						
Write	t_{KHWX}						
Address Advance	t_{KHADVX}						
Chip Enable	t_{KHEX}						

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

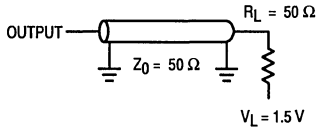


Figure 1A

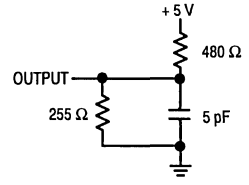
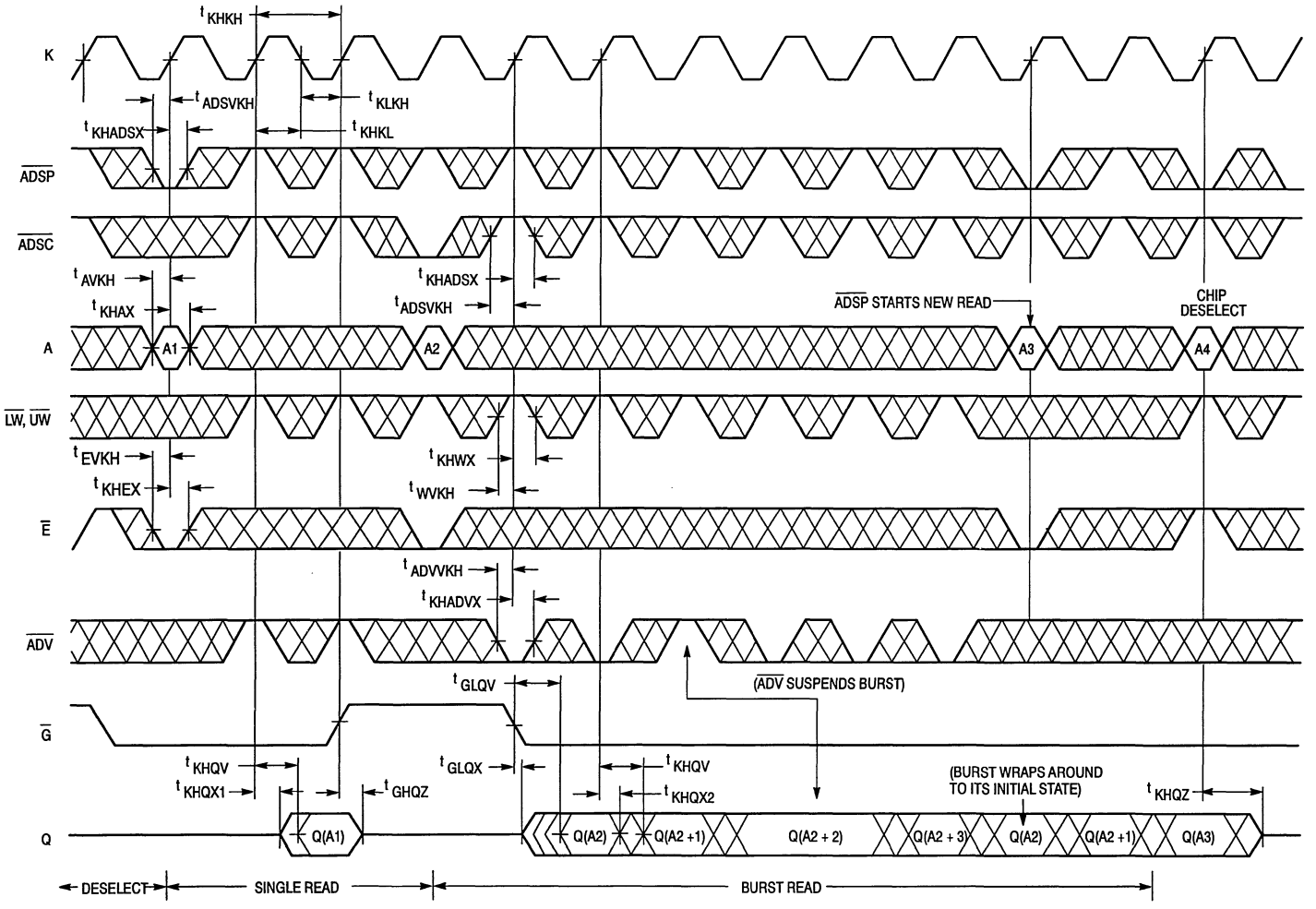
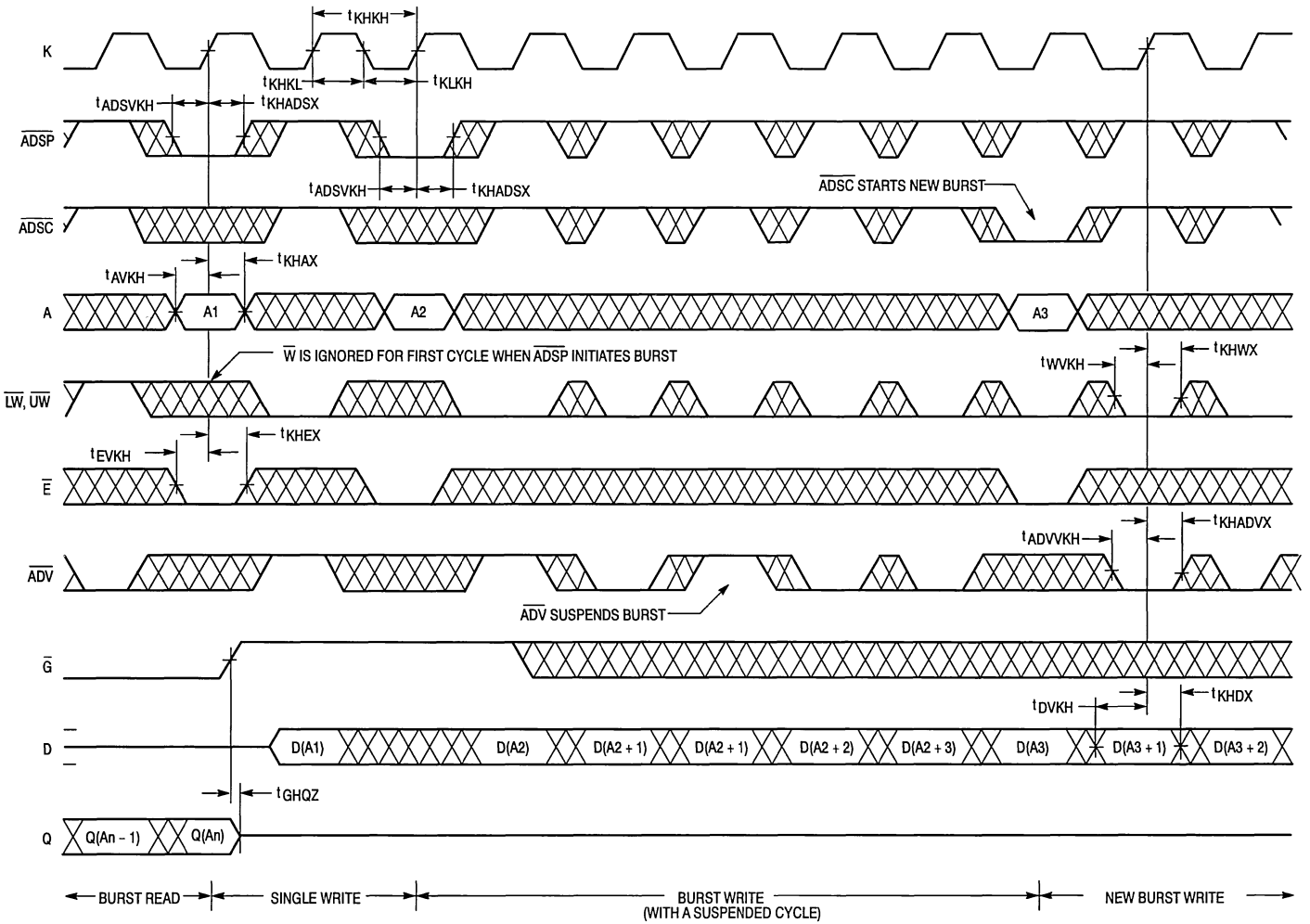


Figure 1B

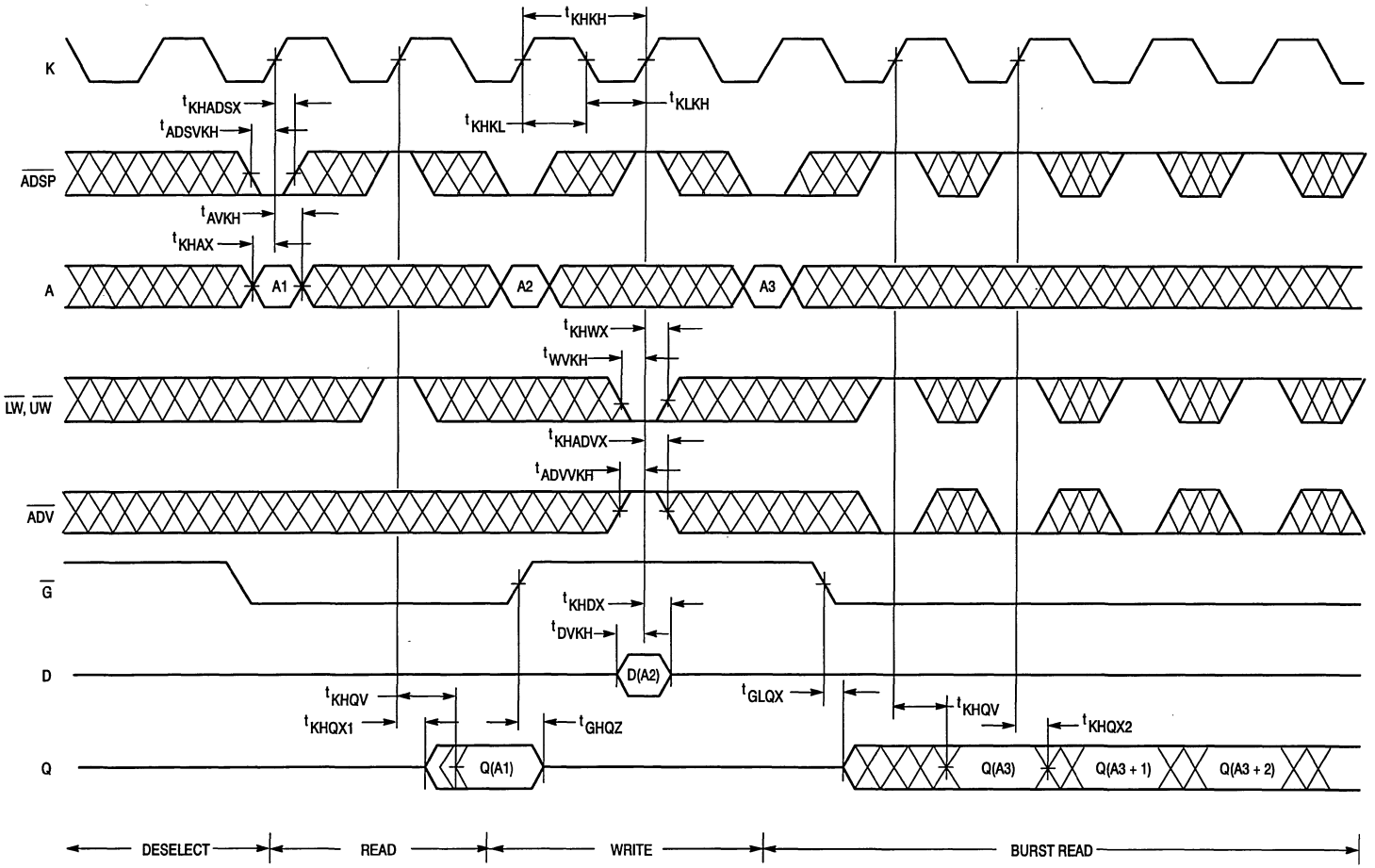
READ CYCLES


tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKHAX
tKHADSX
tADSVKH
ADSP STARTS NEW READ
CHIP DESELECT
A
A1
A2
A3
A4
LW, UW
tEVKH
tKHEX
tKHWX
tWVKH
E
tADVVKH
tKHADVX
ADV
tGLQV
(ADV SUSPENDS BURST)
G
tKHQV
tKHQX1
tGHQZ
tGLQX
tKHQV
tKHQX2
(BURST WRAPS AROUND TO ITS INITIAL STATE)
tKHQZ
Q
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
DESELECT
SINGLE READ
BURST READ

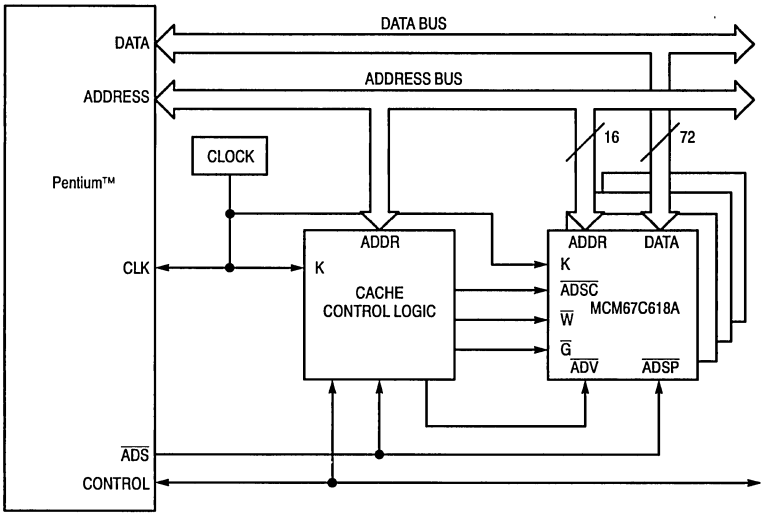
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache Using
Four MCM67C618AFN7s With a 75 MHz (bus speed) Pentium

Figure 2

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67C618A XX X

Motorola Memory Prefix — MCM

Part Number — 67C618A

Speed (5 = 5 ns, 7 = 7 ns) — X

Package (FN = PLCC) — XX

Full Part Numbers — MCM67C618AFN5 MCM67C618AFN7

MCM67H618A

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write

The MCM67H618A is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

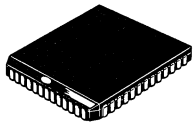
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67H618A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining



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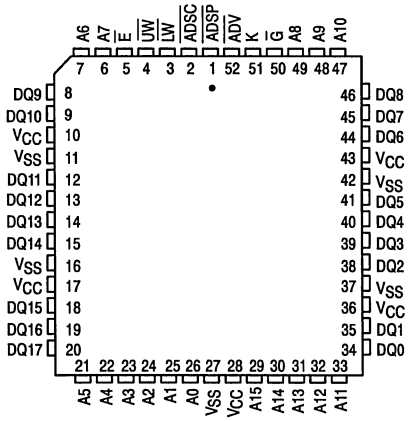
PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

All power supply and ground pins must be connected for proper operation of the device.

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i486 and Pentium are trademarks of Intel Corp.

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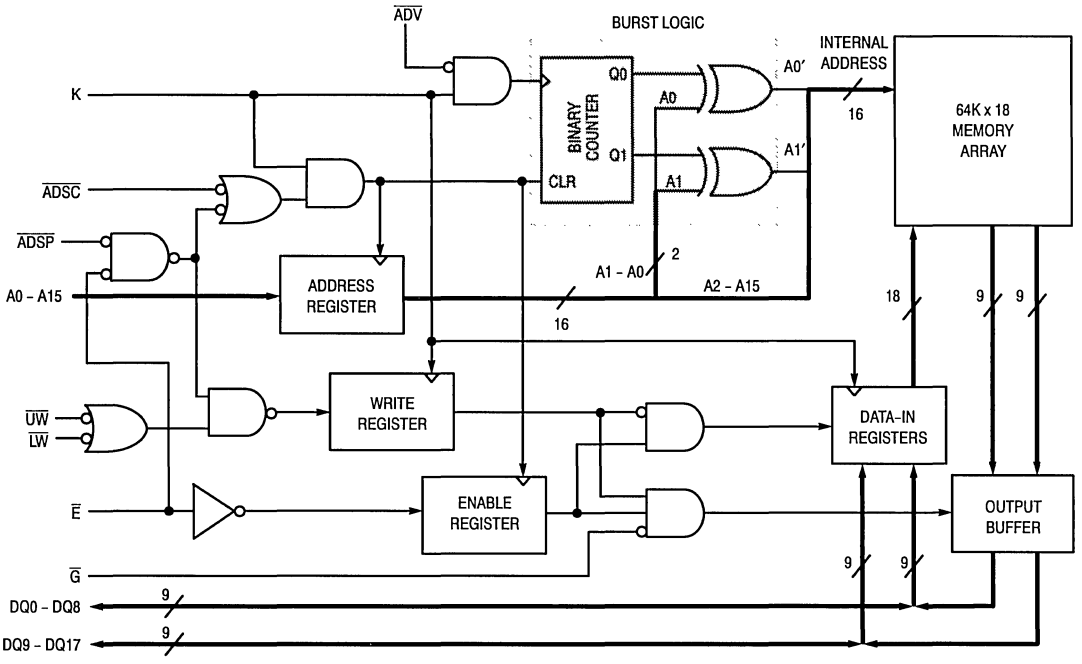
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ and $\overline{E}$ are sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$, $\overline{E}$, and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram). Note that when $\overline{E}$ and $\overline{ADSC}$ are high, $\overline{ADSP}$ is ignored – the external address is not registered in this case.
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE.** Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	— — —	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67H618A–9		MCM67H618A–10		MCM67H618A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	7
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	7

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be asserted at each rising edge of clock for the device (when $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

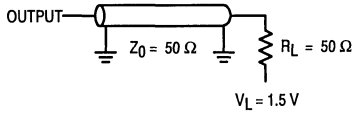


Figure 1A

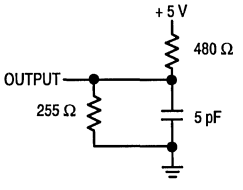
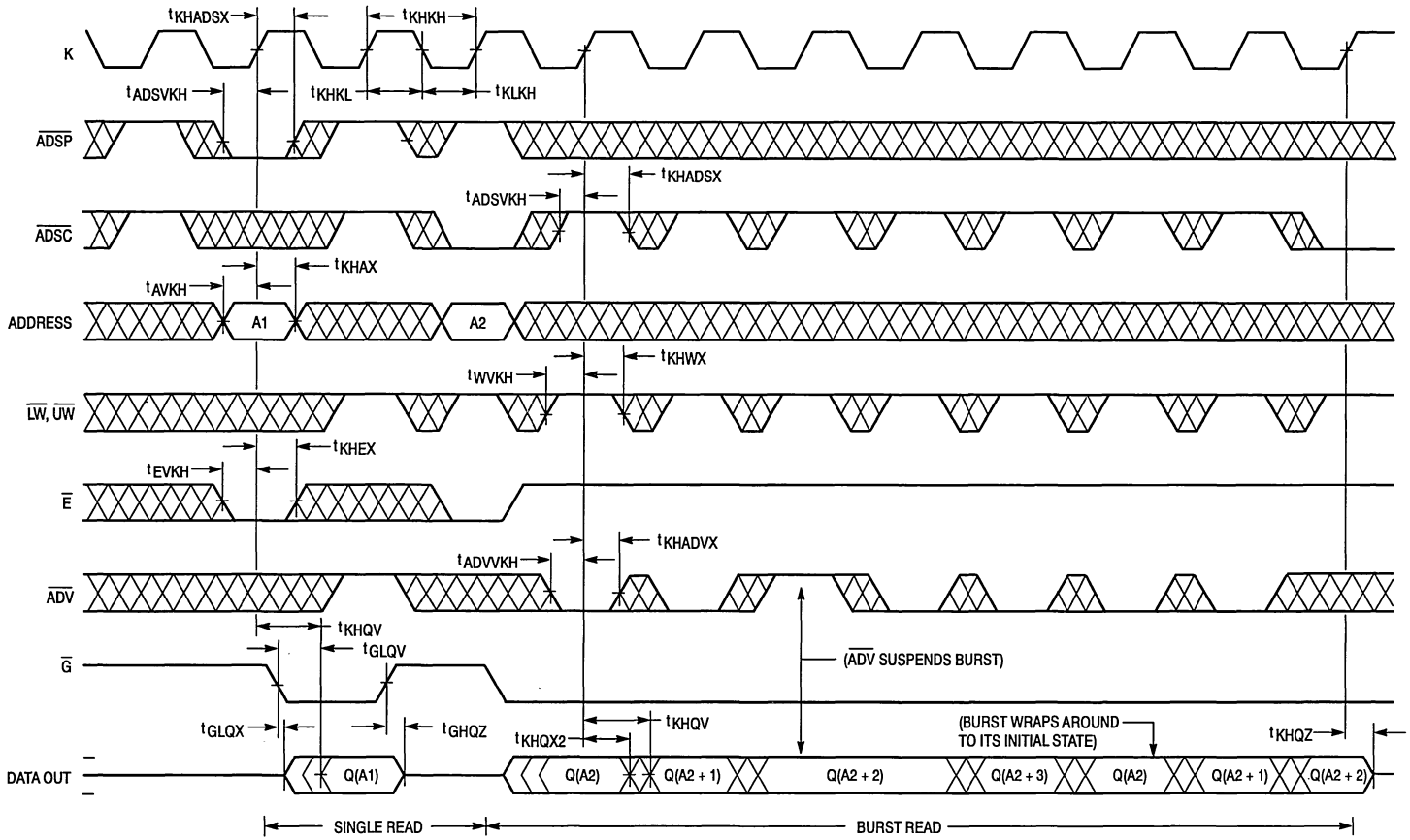


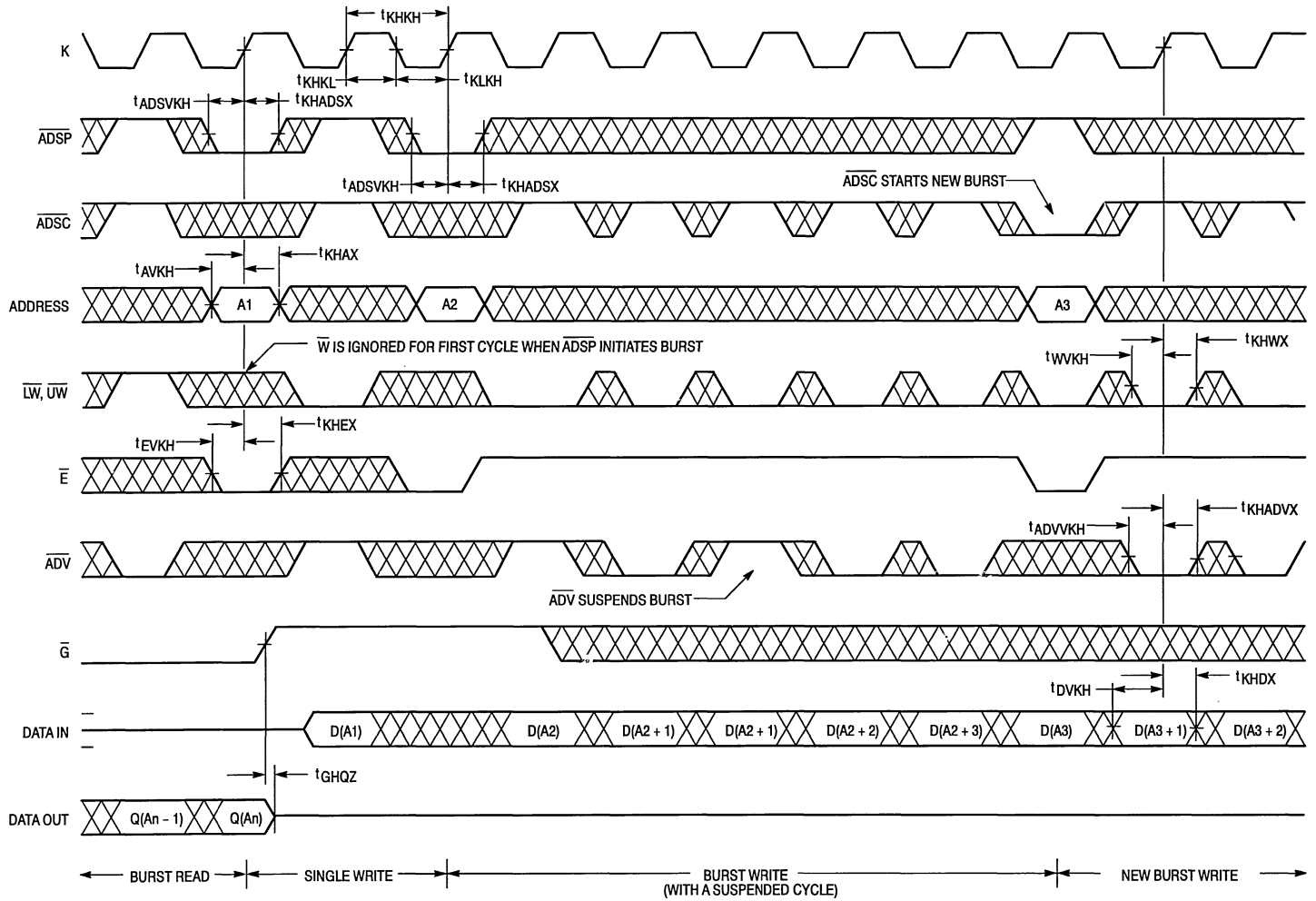
Figure 1B

READ CYCLES

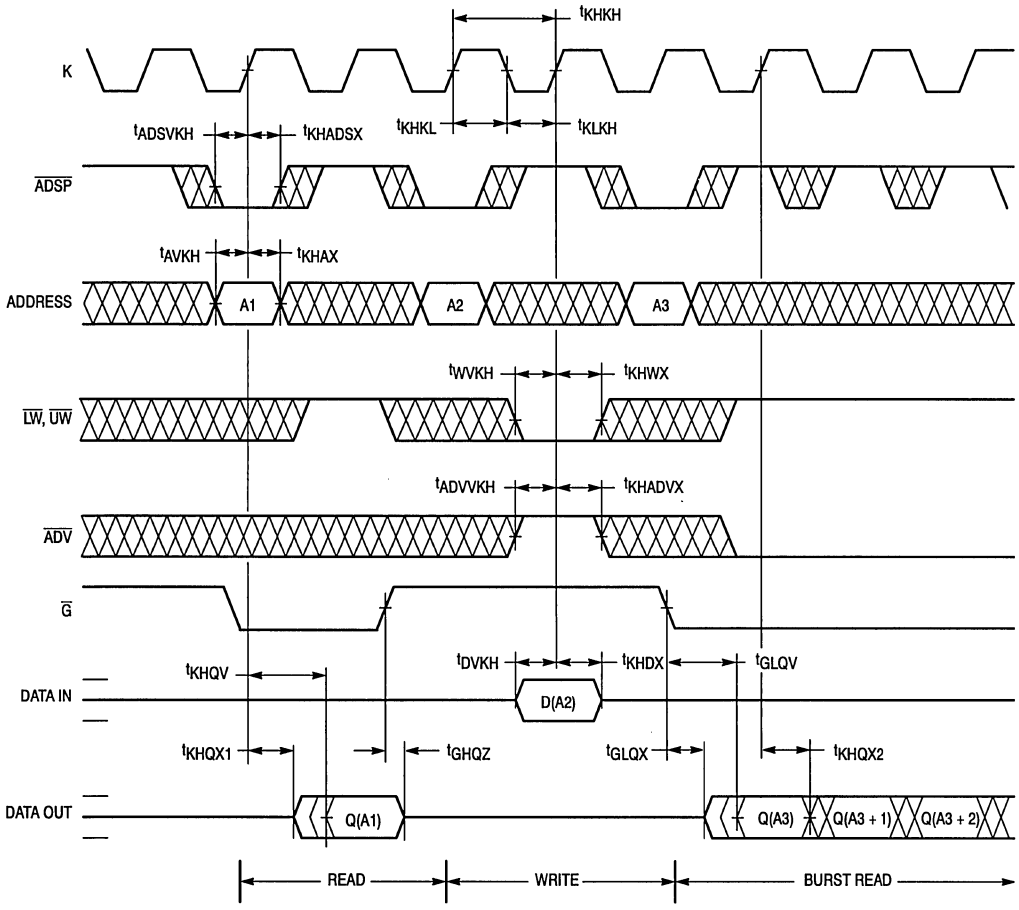


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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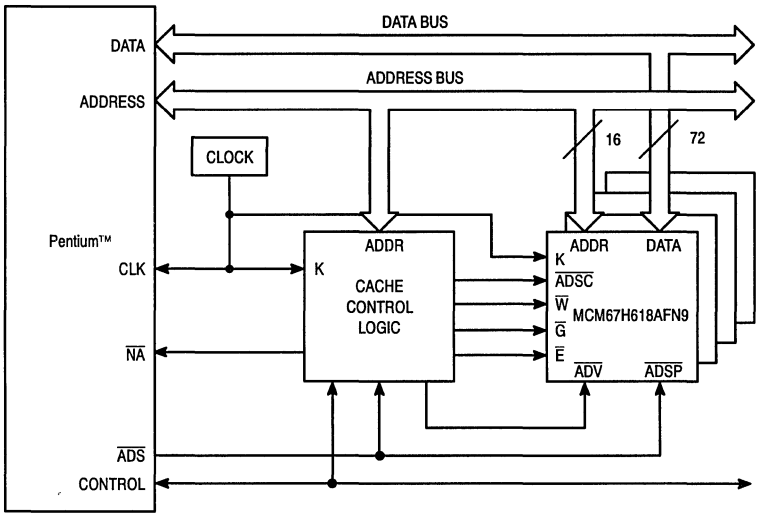
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67H618AFN9s with a 66 MHz Pentium

Figure 2

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ORDERING INFORMATION
(Order by Full Part Number)

MCM 67H618A XX XX

Motorola Memory Prefix — MCM

Part Number — 67H618A

Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns) — XX

Package (FN = PLCC) — XX

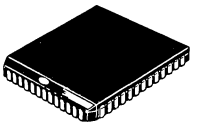
Full Part Numbers — MCM67H618AFN9 MCM67H618AFN10 MCM67H618AFN12

MCM67J618A

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67J618A is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive–edge–triggered non-inverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67J618A (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

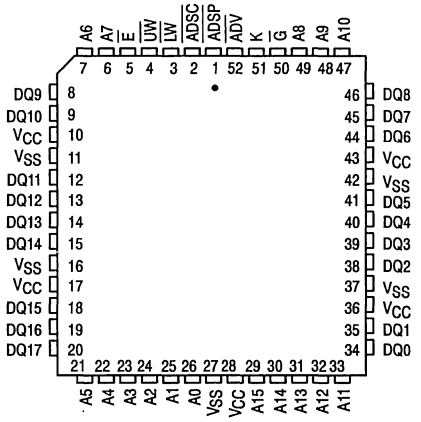
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 5 ns/100 MHz, 7 ns/80 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52–Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

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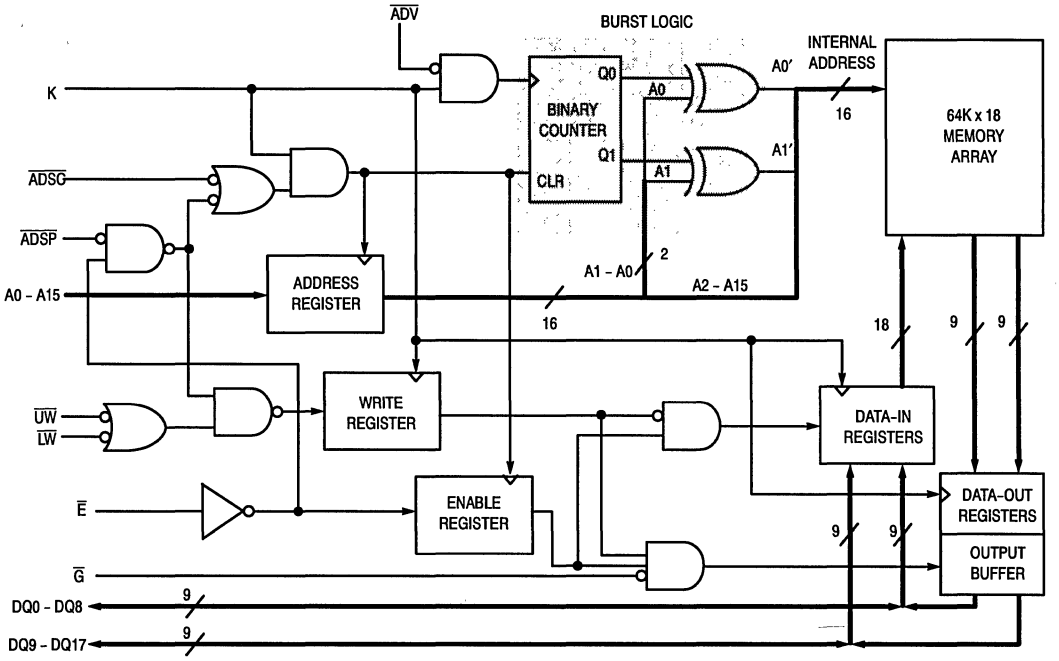
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram). When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	+ 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA5} I_{CCA7}	—	310 290	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486, Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67J618A–5		MCM67J618A–7		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	7	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{EVKH}	2.5	—	2.5	—	ns	7
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHEX}	0.5	—	0.5	—	ns	7

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 and Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

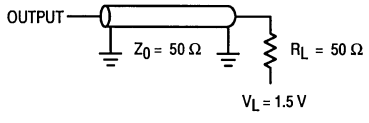


Figure 1A

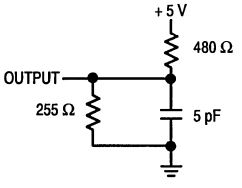
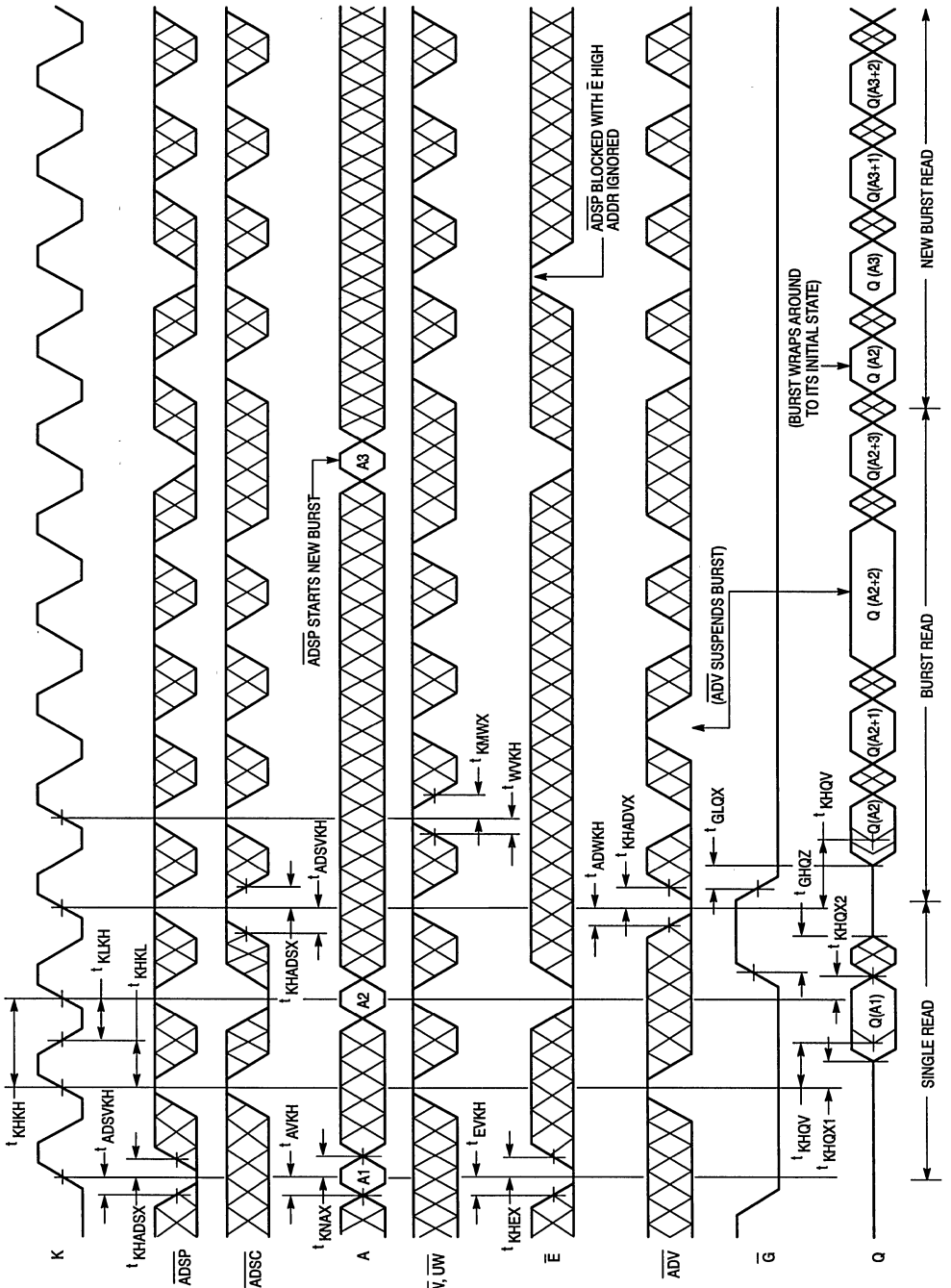
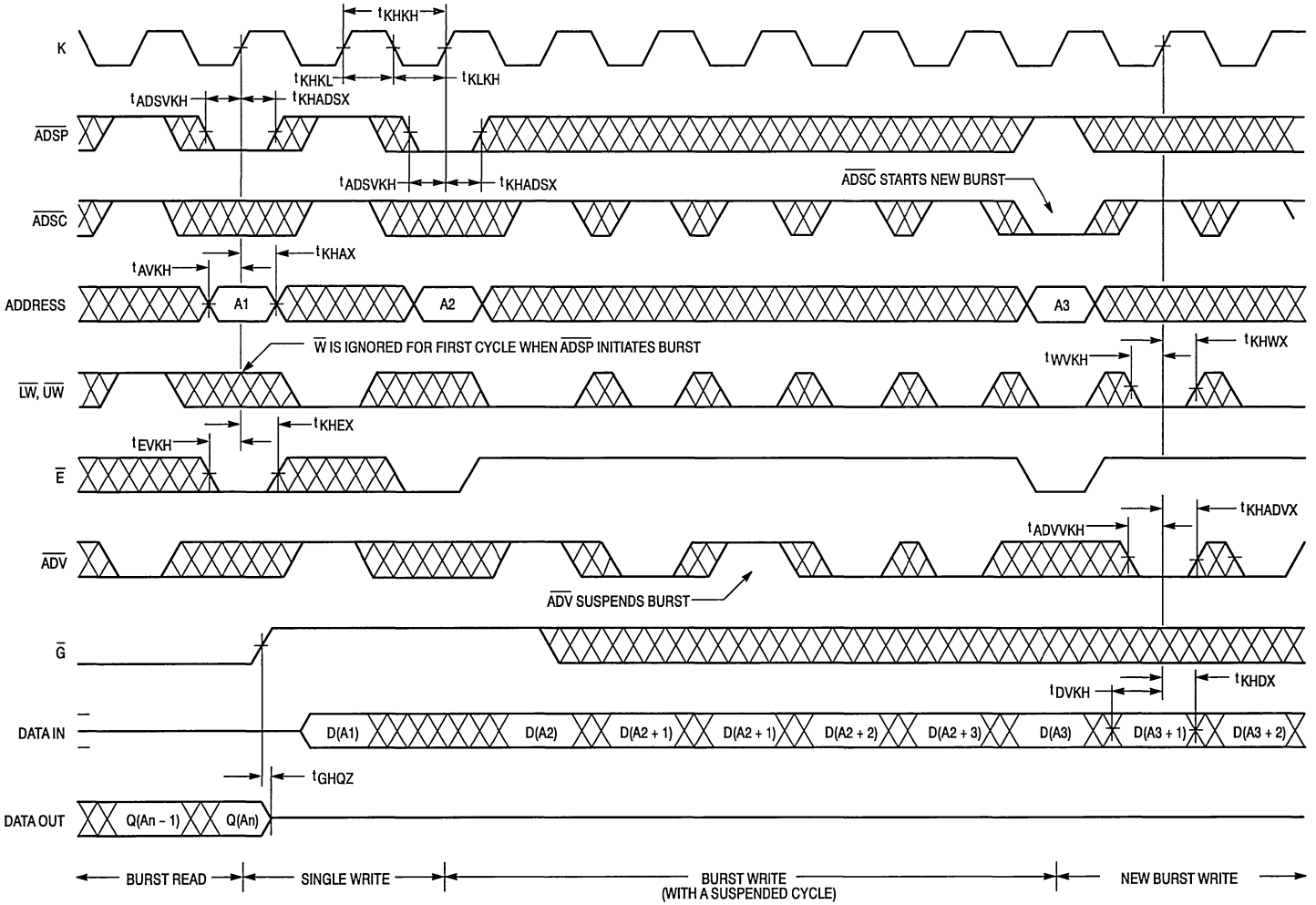


Figure 1B

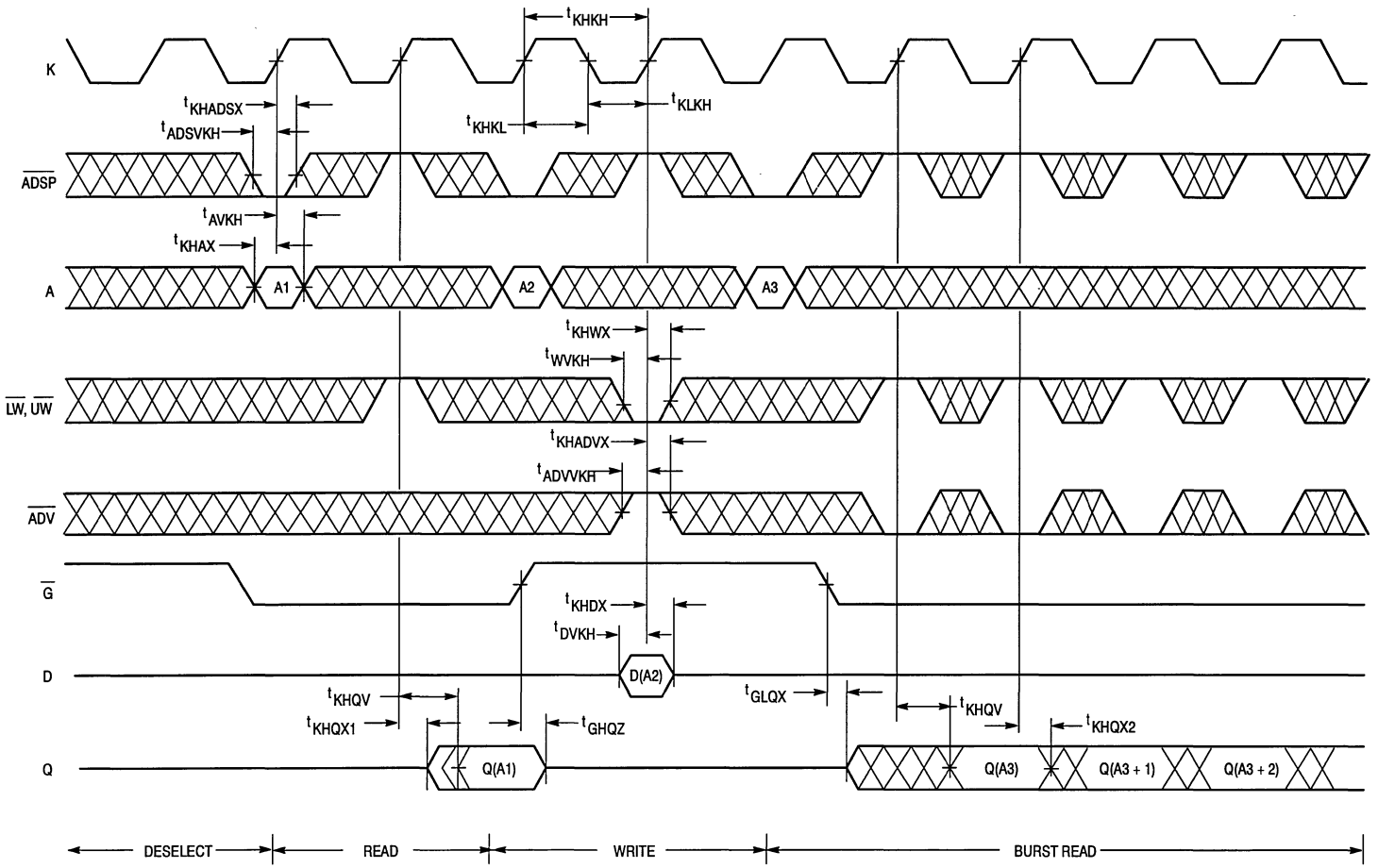
READ CYCLES


K
ADSP
ADSC
A
LW, UW
E
ADV
G
Q
tKHKH
tKLKH
tKHKL
tADSVKH
tKHADSX
tAVKH
tKNAX
tADSVKH
tKHADSX
tEVKH
tKHEX
tADWKH
tKHADVX
tKMWX
tWVKH
tGLQX
tGHQZ
tKHQV
tKHQX2
tKHQV
tKHQX1
A1
A2
A3
ADSP STARTS NEW BURST
(ADV SUSPENDS BURST)
ADSP BLOCKED WITH E HIGH
ADDR IGNORED
(BURST WRAPS AROUND
TO ITS INITIAL STATE)
Q(A1)
Q(A2)
Q(A2+1)
Q (A2+2)
Q(A2+3)
Q (A2)
Q (A3)
Q(A3+1)
Q(A3+2)
SINGLE READ
BURST READ
NEW BURST READ

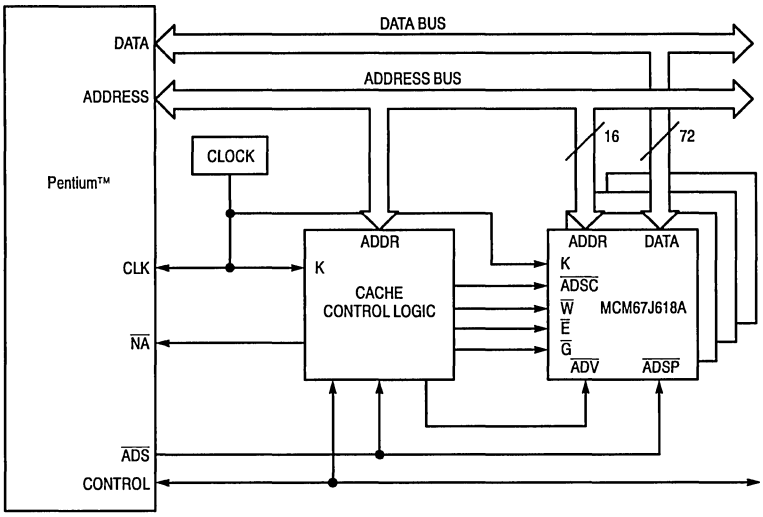
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache Using
Four MCM67J618AFN7s with a 75 MHz (Bus Speed) Pentium

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67J618A XX X

Motorola Memory Prefix — MCM

Part Number — 67J618A

Speed (5 = 5 ns, 7 = 7 ns) — X

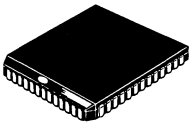
Package (FN = PLCC) — XX

Full Part Numbers — MCM67J618AFN5 MCM67J618AFN7

MCM67M618

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67M618 is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (DQ0 – DQ17), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM67M618 (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

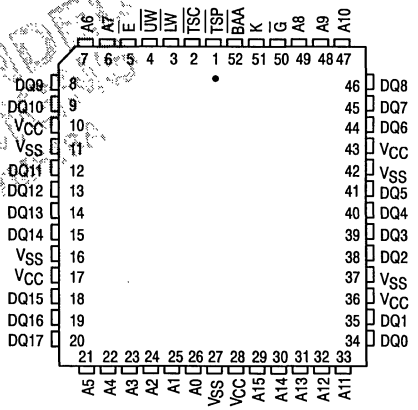
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/11/14 ns Max and Cycle Times: 12.5/15/20 ns Min
- Byte Writeable via Dual Write Strobes
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Board Density 52–PLCC Package
- 3.3 V I/O Compatible

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{BAA}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

5

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PowerPC is a trademark of IBM Corp.

REV 6
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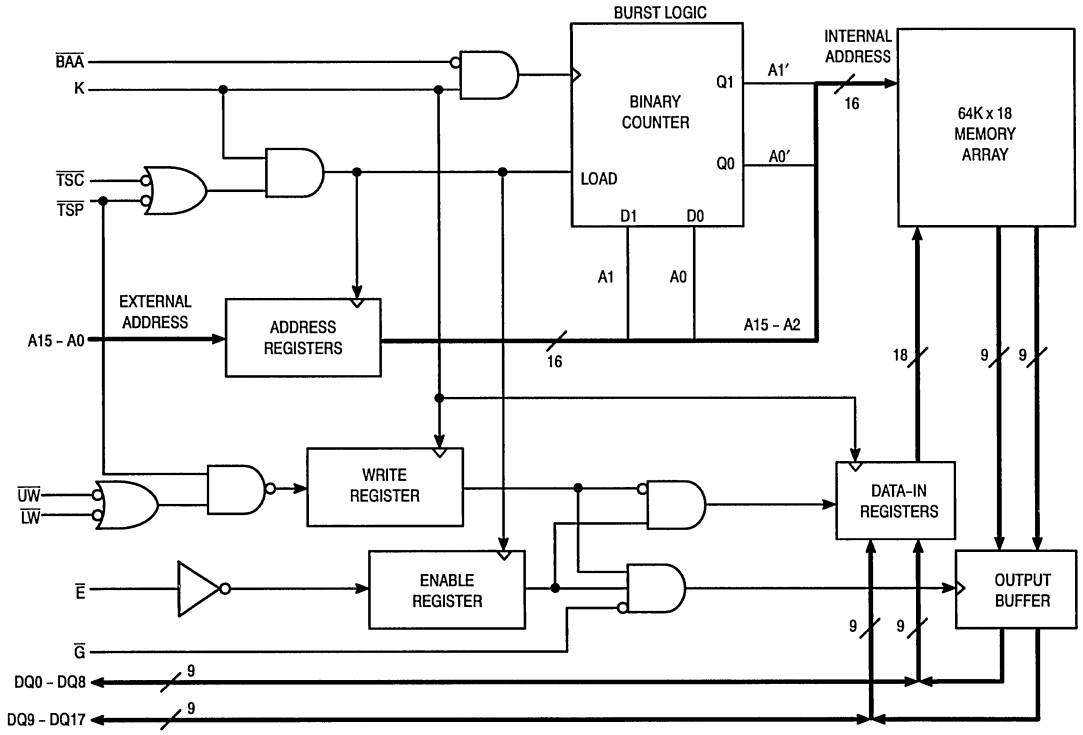
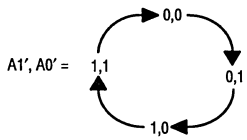
BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. Alternatively, a $\overline{TSP}$–initiated two cycle WRITE can be performed by asserting $\overline{TSP}$ and a valid address on the first cycle, then negating both $\overline{TSP}$ and $\overline{TSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

5

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

5

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA11} I_{CCA14}	—	290 275 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible 68040 and PowerPC bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	—	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	—	6	8	pF

5

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67M618–9		MCM67M618–11		MCM67M618–14		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12.5	—	15	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	11	—	14	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	6
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{TSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{BAVKH}								
Chip Select	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHTSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHBAX}								
Chip Select	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected. Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

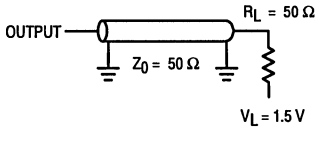


Figure 1A

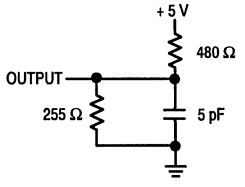
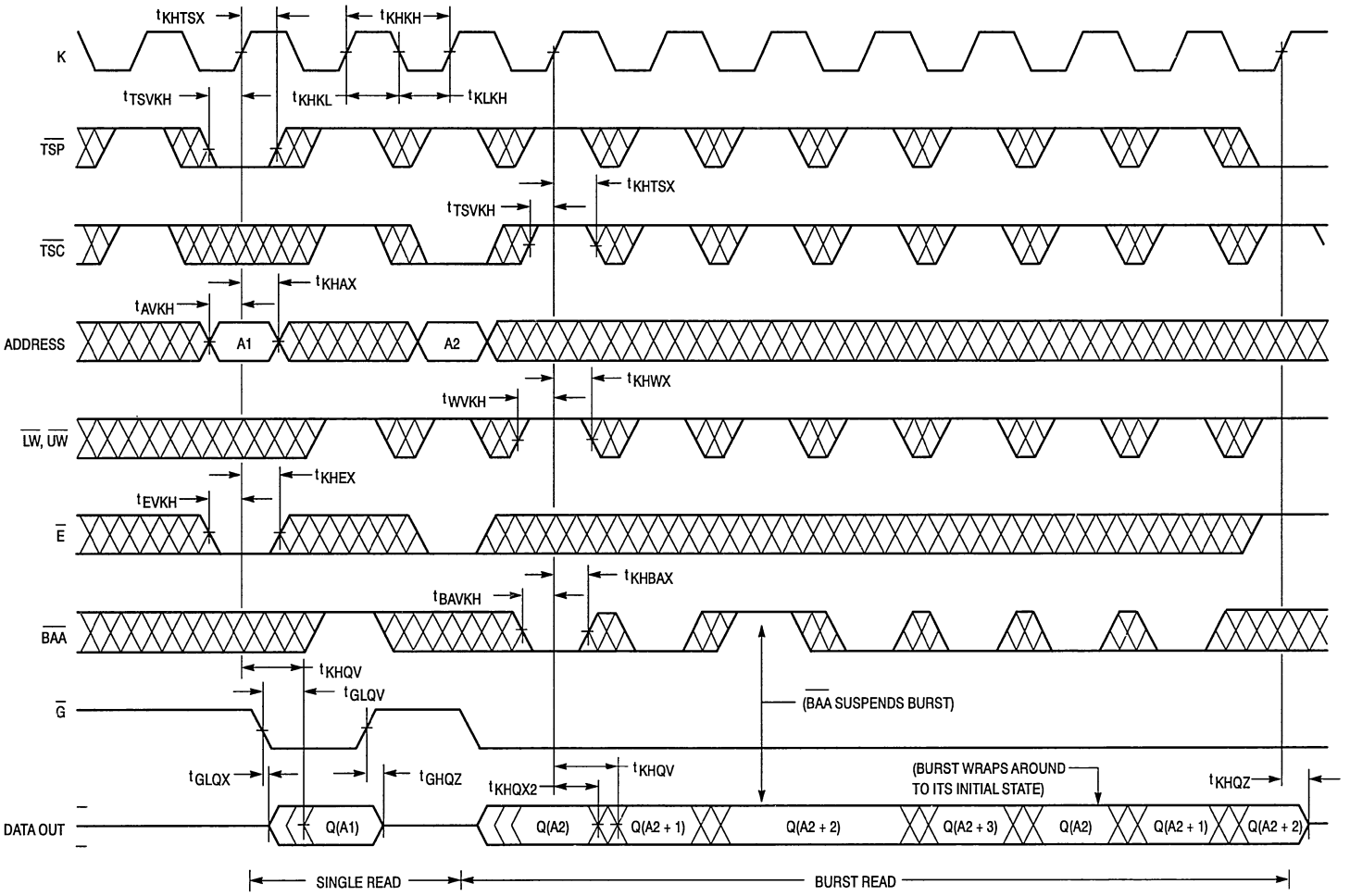


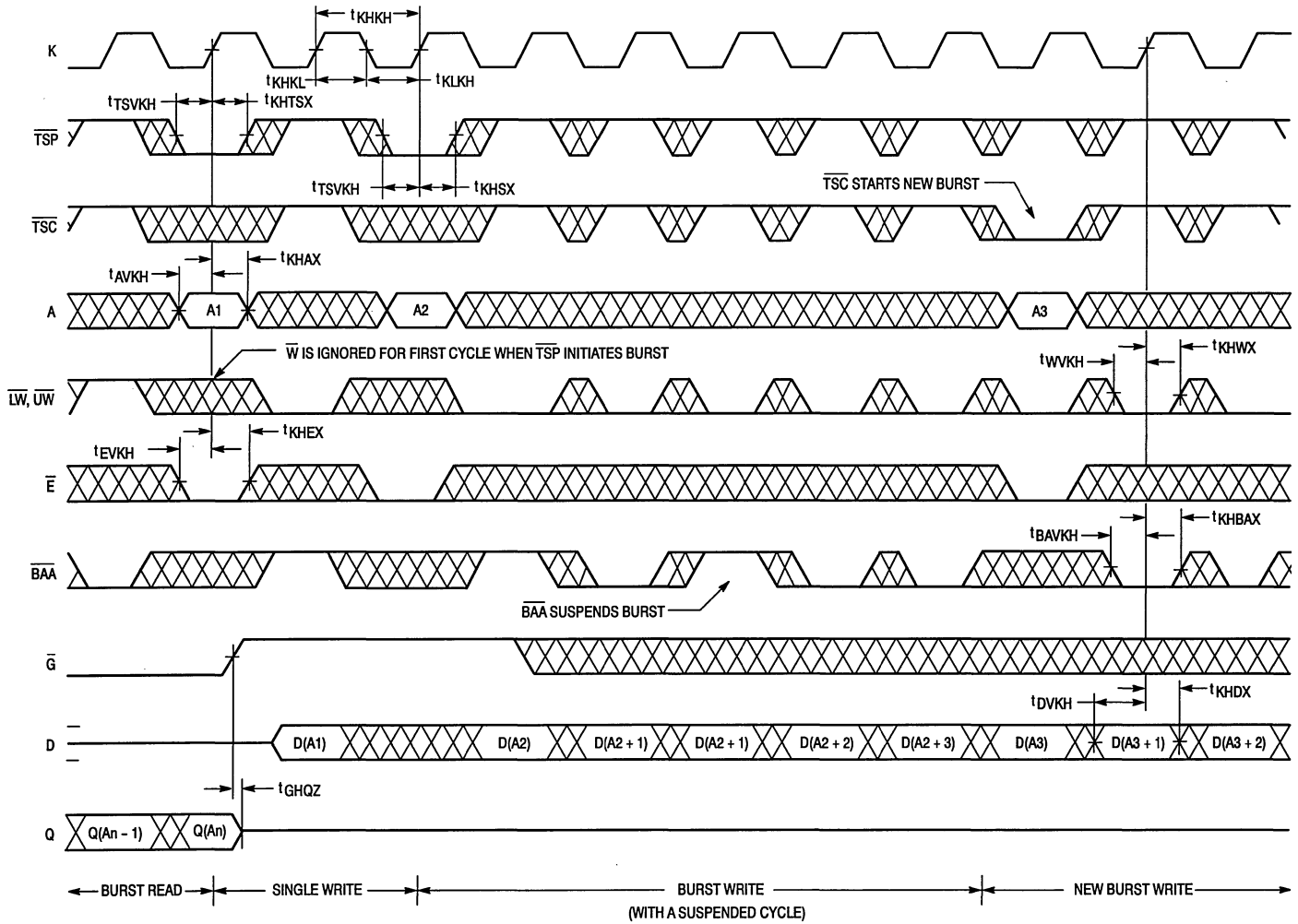
Figure 1B

READ CYCLES

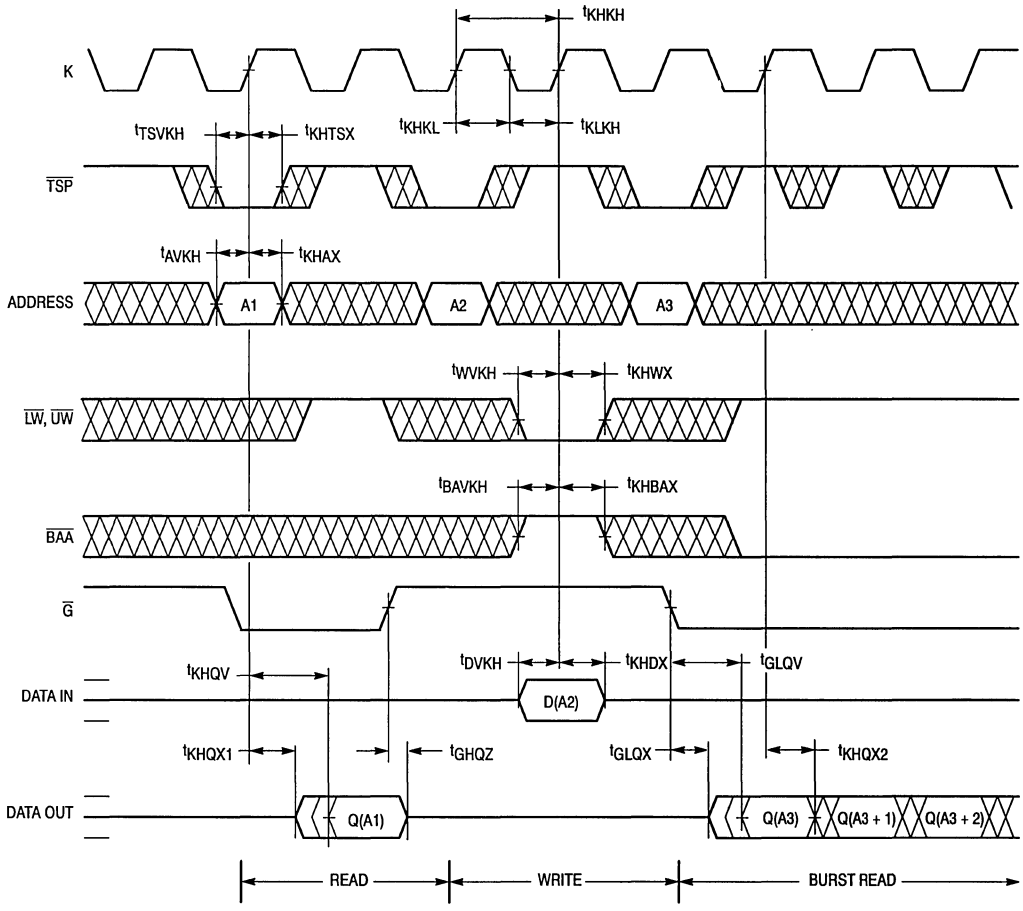


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{TSC}$ high)



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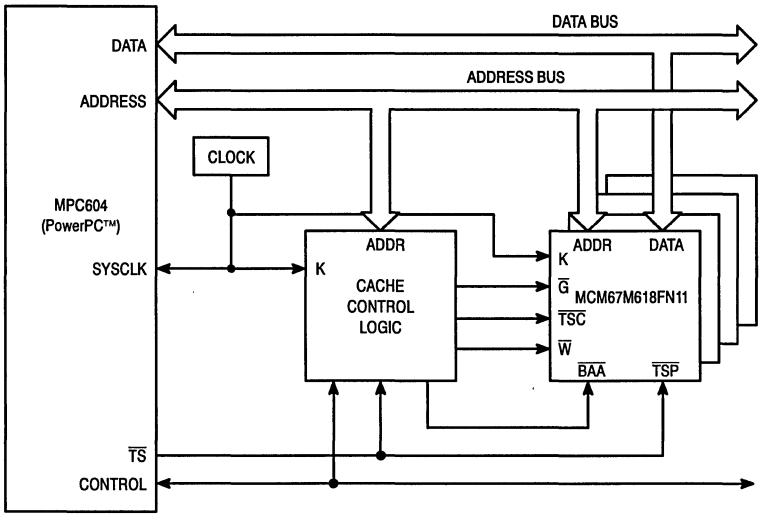
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67M618FN11s with a 66 MHz MPC604 PowerPC™

5

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67M618 XX XX

Motorola Memory Prefix — MCM
Part Number — 67M618
Speed (9 = 9 ns, 11 = 11 ns, 14 = 14 ns) — XX
Package (FN = PLCC) — XX

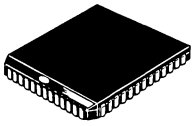
Full Part Numbers — MCM67M618FN9 MCM67M618FN11 MCM67M618FN14

MCM67M618A

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self–Timed Write



FN PACKAGE
PLASTIC
CASE 778–02

The MCM67M618A is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high–performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated using Motorola's high–performance silicon–gate BiCMOS technology. The device integrates input registers, a 2–bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (DQ0 – DQ17), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM67M618A (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

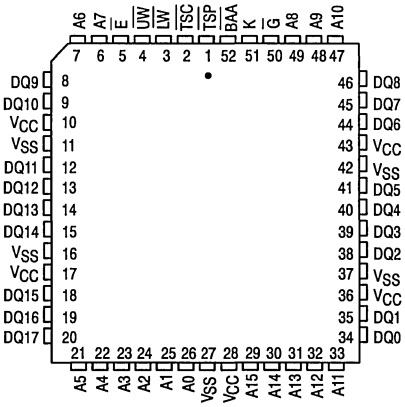
Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/10/12 ns Max
- Byte Writeable via Dual Write Strobes
- Internal Input Registers (Address, Data, Control)
- Internally Self–Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Board Density 52–PLCC Package
- 3.3 V I/O Compatible

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{BAA}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

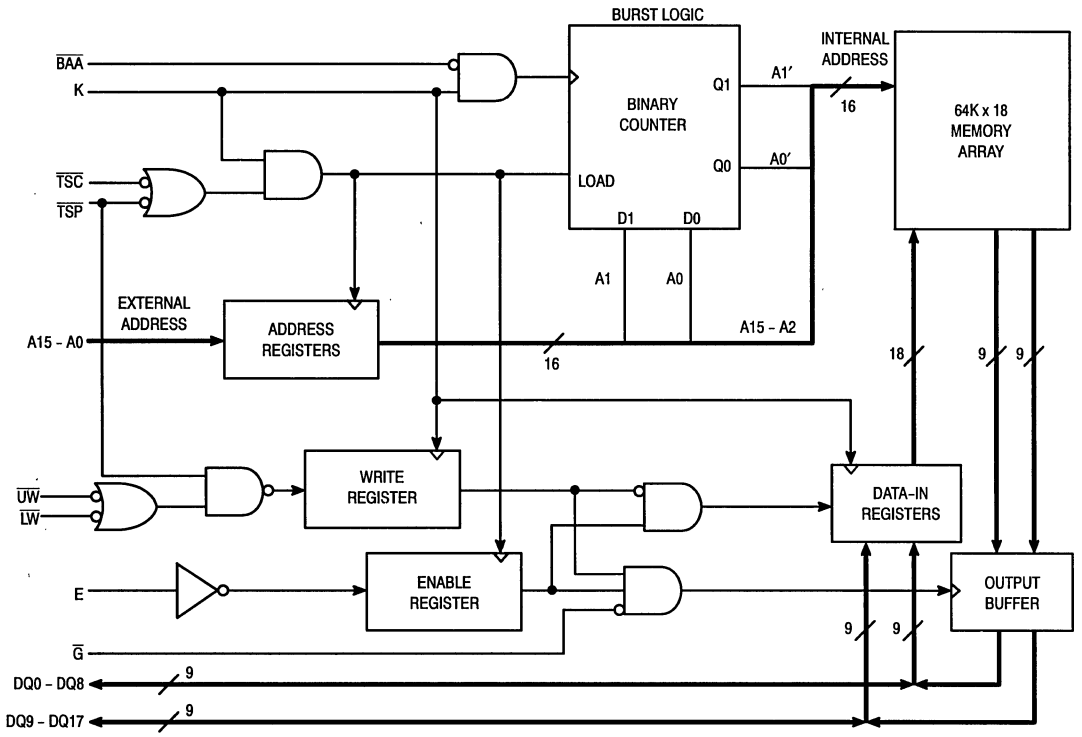
5

BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

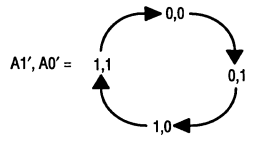
REV 1
5/95

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. Alternatively, a $\overline{TSP}$–initiated two cycle WRITE can be performed by asserting $\overline{TSP}$ and a valid address on the first cycle, then negating both $\overline{TSP}$ and $\overline{TSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA10} I_{CCA12}	—	275 265 250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	95	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible 68040 and PowerPC bus cycles.

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CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	—	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 3, and 4)

Parameter	Symbol	MCM67M618A–9		MCM67M618A–10		MCM67M618A–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High–Z	t_{KHQZ}	3	6	3	7	3	7	ns	6
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{TSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{BAVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHTSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHBAX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{TSP}$ or $\overline{TSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

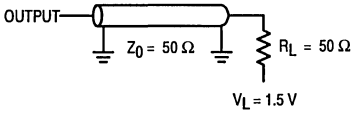


Figure 1A

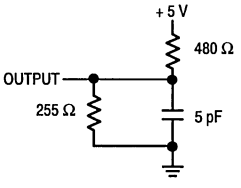
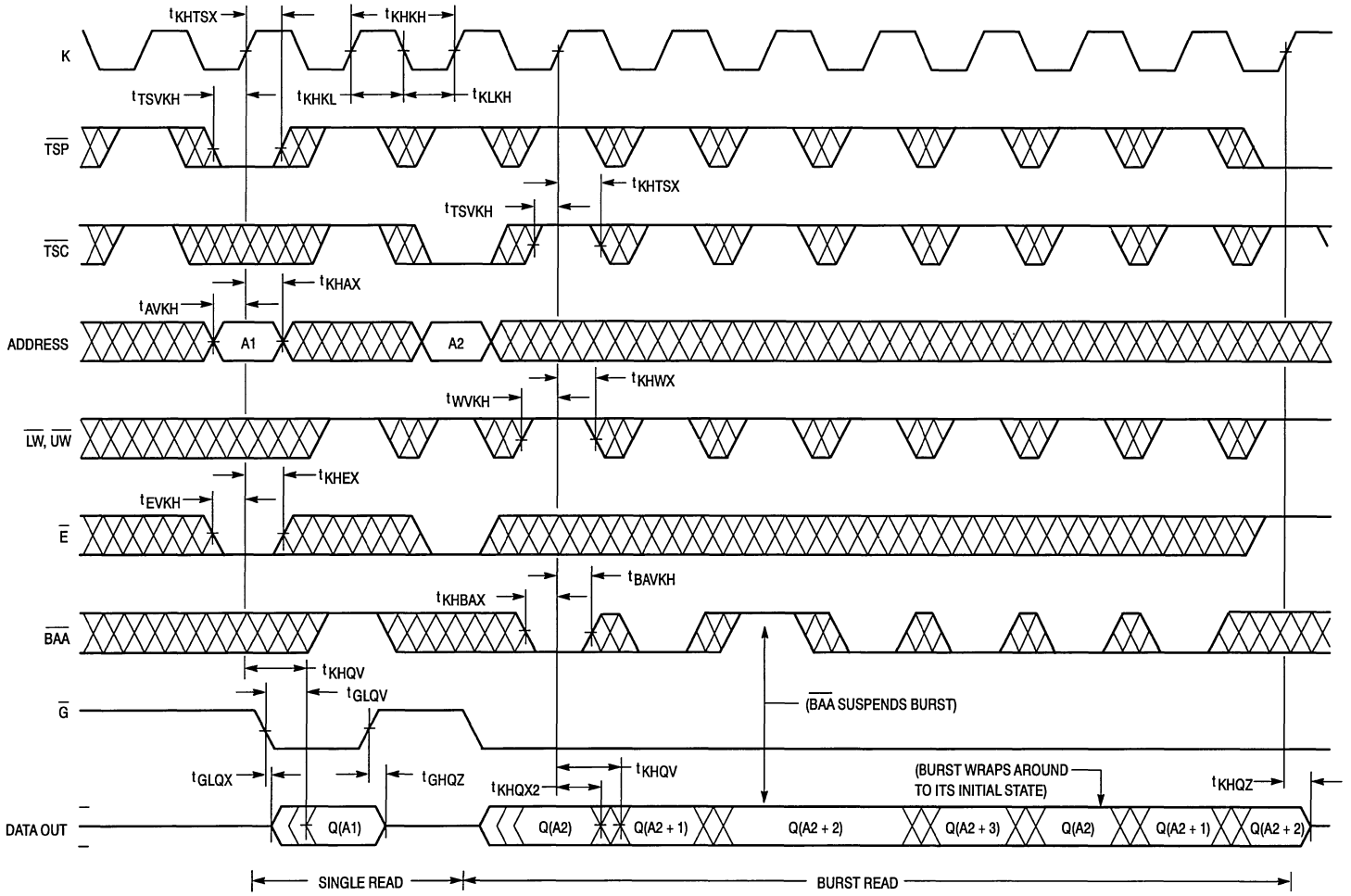


Figure 1B

READ CYCLES



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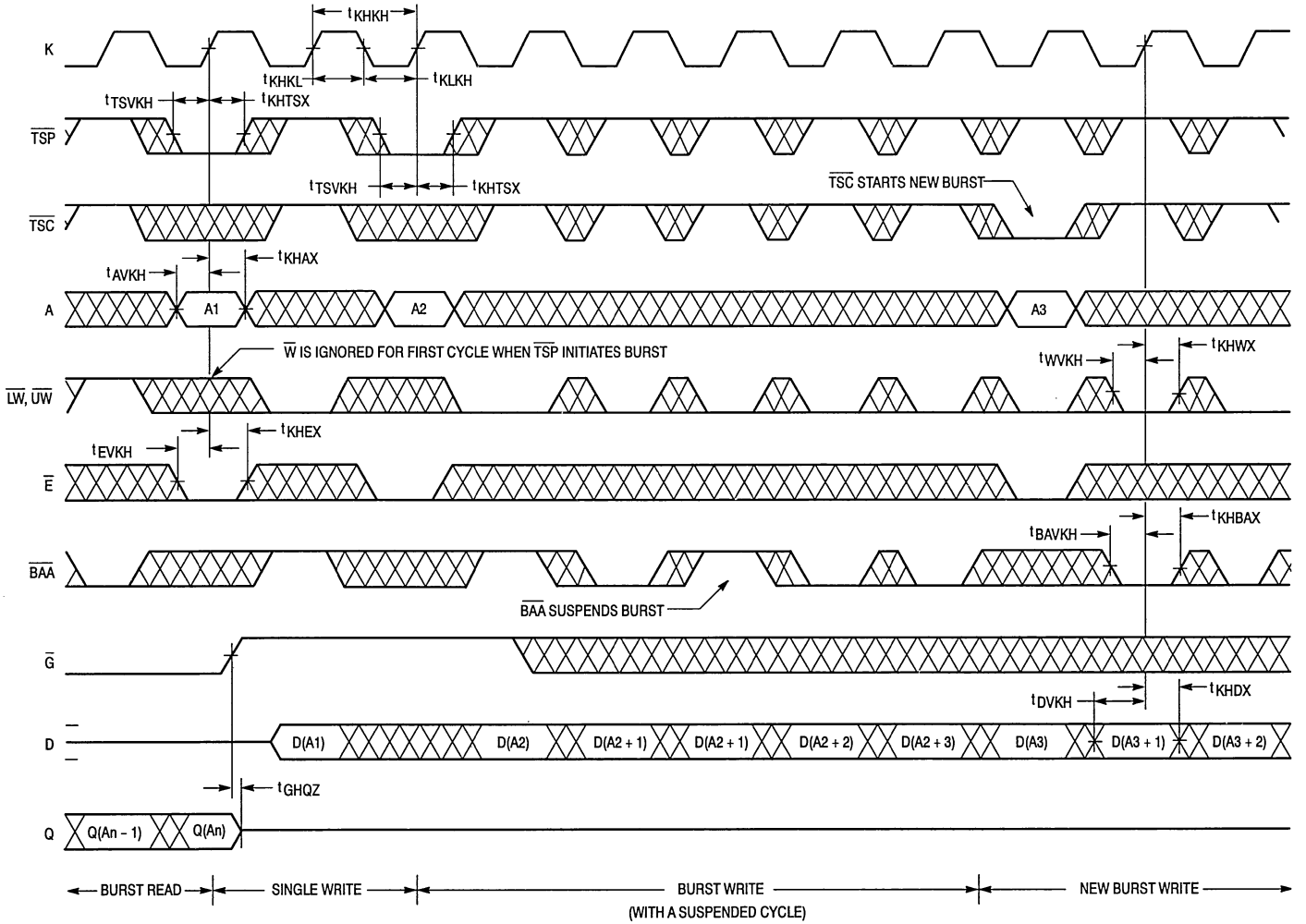
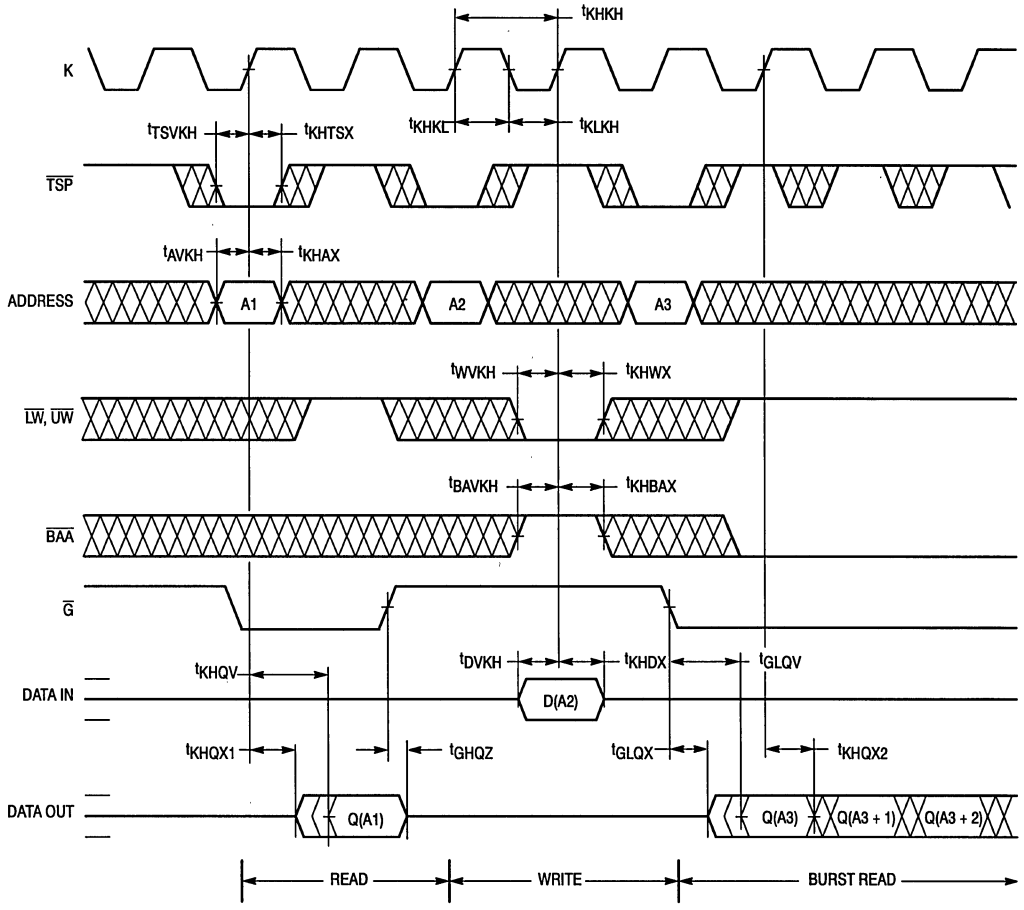
WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{TSC}$ high)



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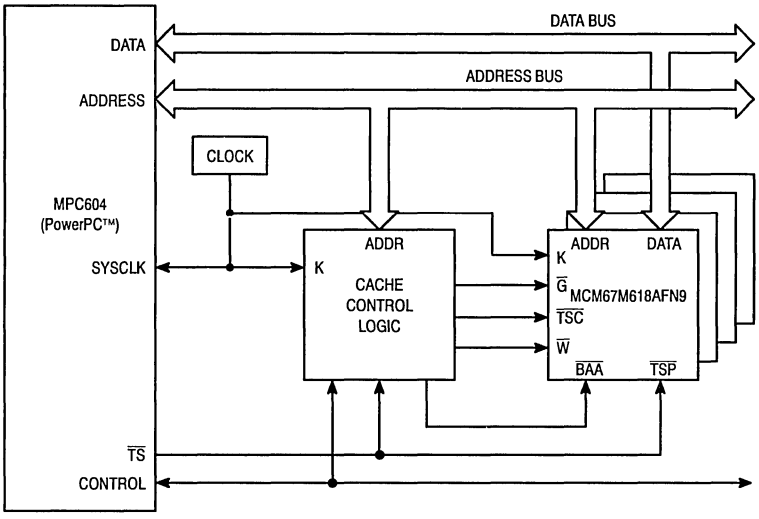
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
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5

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MCM 67M618A XX XX

Motorola Memory Prefix — MCM

Part Number — 67M618A

Speed (9 = 9 ns, 10 = 10 ns, 12 = 12 ns) — XX

Package (FN = PLCC) — XX

Full Part Numbers — MCM67M618AFN9 MCM67M618AFN10 MCM67M618AFN12

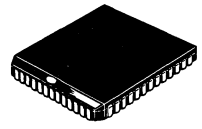
Full Part Numbers — MCM67M618AFN9 MCM67M618AFN10 MCM67M618AFN12

MCM67N618A

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778–02

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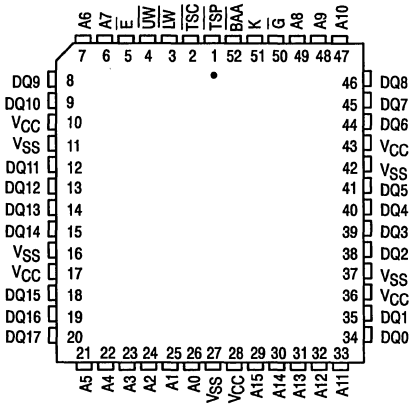
Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time: 5 ns/100 MHz, 7 ns/80 MHz
- Byte Writeable via Dual Write Strobes
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self–Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three–State Outputs
- Common Data Inputs and Data Outputs
- High Board Density 52–PLCC Package
- 3.3 V I/O Compatible

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{BAA}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

All power supply and ground pins must be connected for proper operation of the device.

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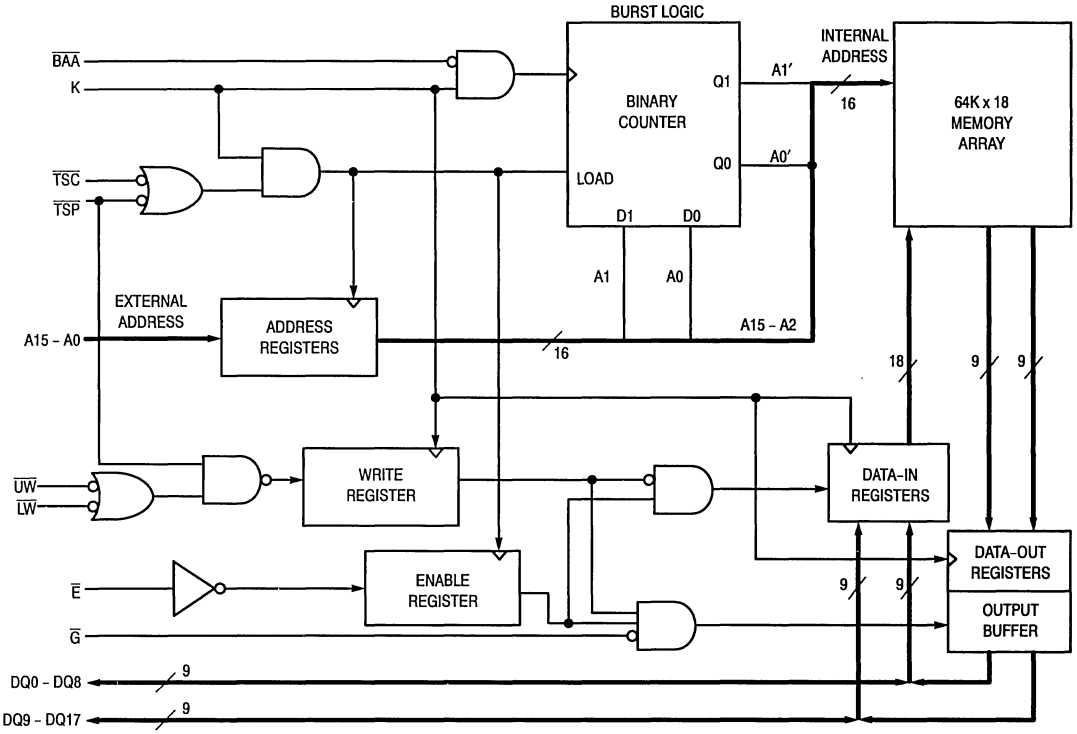
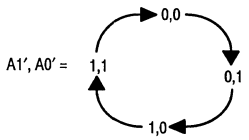
REV 1
5/95

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. Alternatively, a $\overline{TSP}$–initiated two cycle WRITE can be performed by asserting $\overline{TSP}$ and a valid address on the first cycle, then negating both $\overline{TSP}$ and $\overline{TSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

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SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

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ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA5} I_{CCA7}	—	310 290	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible 68040 and PowerPC bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	—	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67N618A–5		MCM67N618A–7		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	7	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	0	—	0	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	—	6	—	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	2	6	2	6	ns	
Clock High Pulse Width	t_{KHKL}	4.5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	4.5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	ns	7
Address Status	t_{TSVKH}						
Data In	t_{DVKH}						
Write	t_{WVKH}						
Address Advance	t_{BAVKH}						
Chip Select	t_{EVKH}						
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	ns	7
Address Status	t_{KHTSX}						
Data In	t_{KHDX}						
Write	t_{KHWX}						
Address Advance	t_{KHBAX}						
Chip Select	t_{KHEX}						

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected. Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

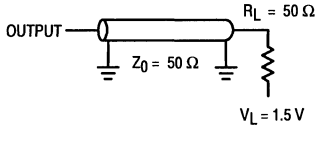


Figure 1A

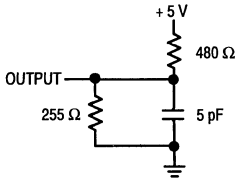
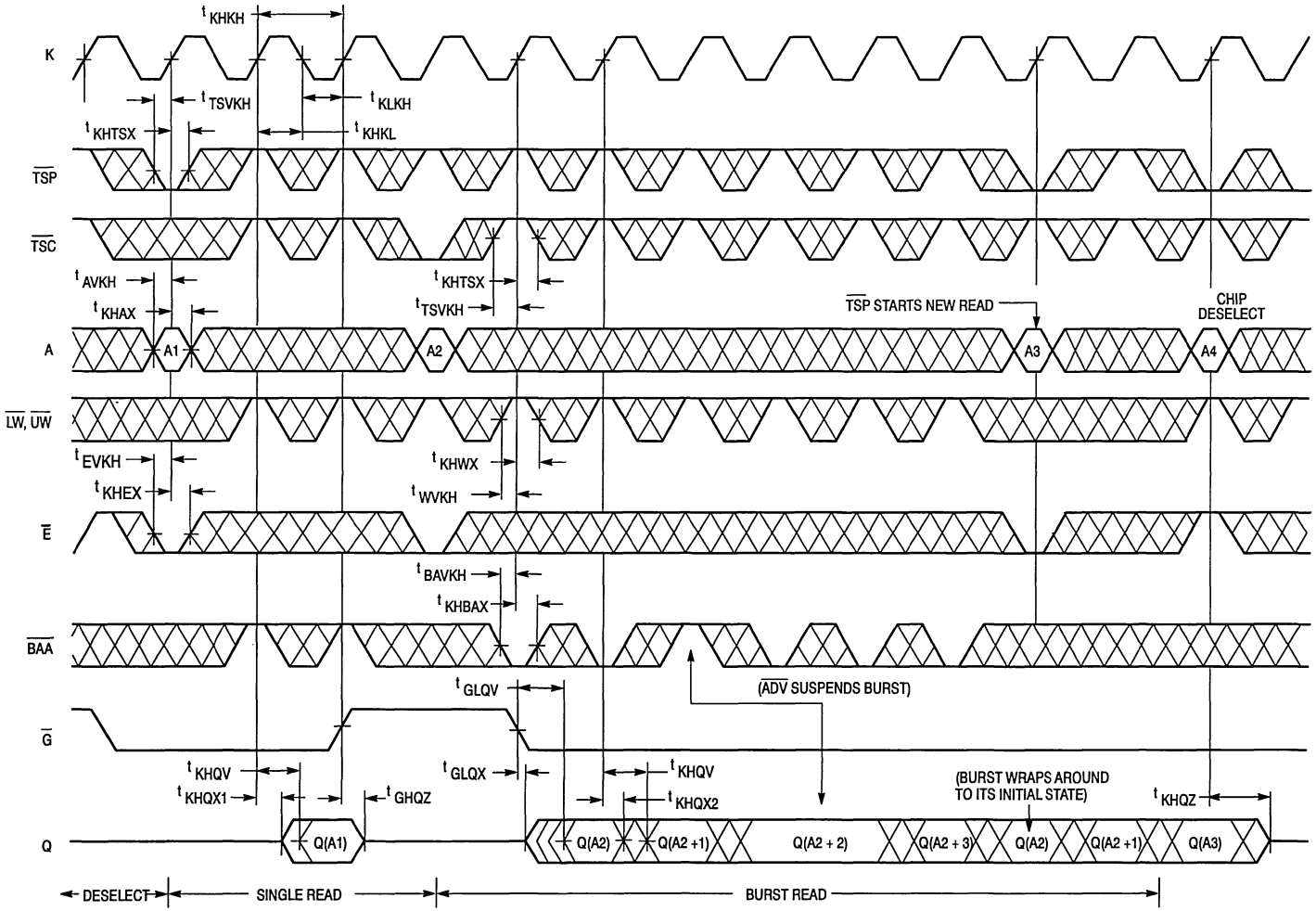


Figure 1B

READ CYCLES



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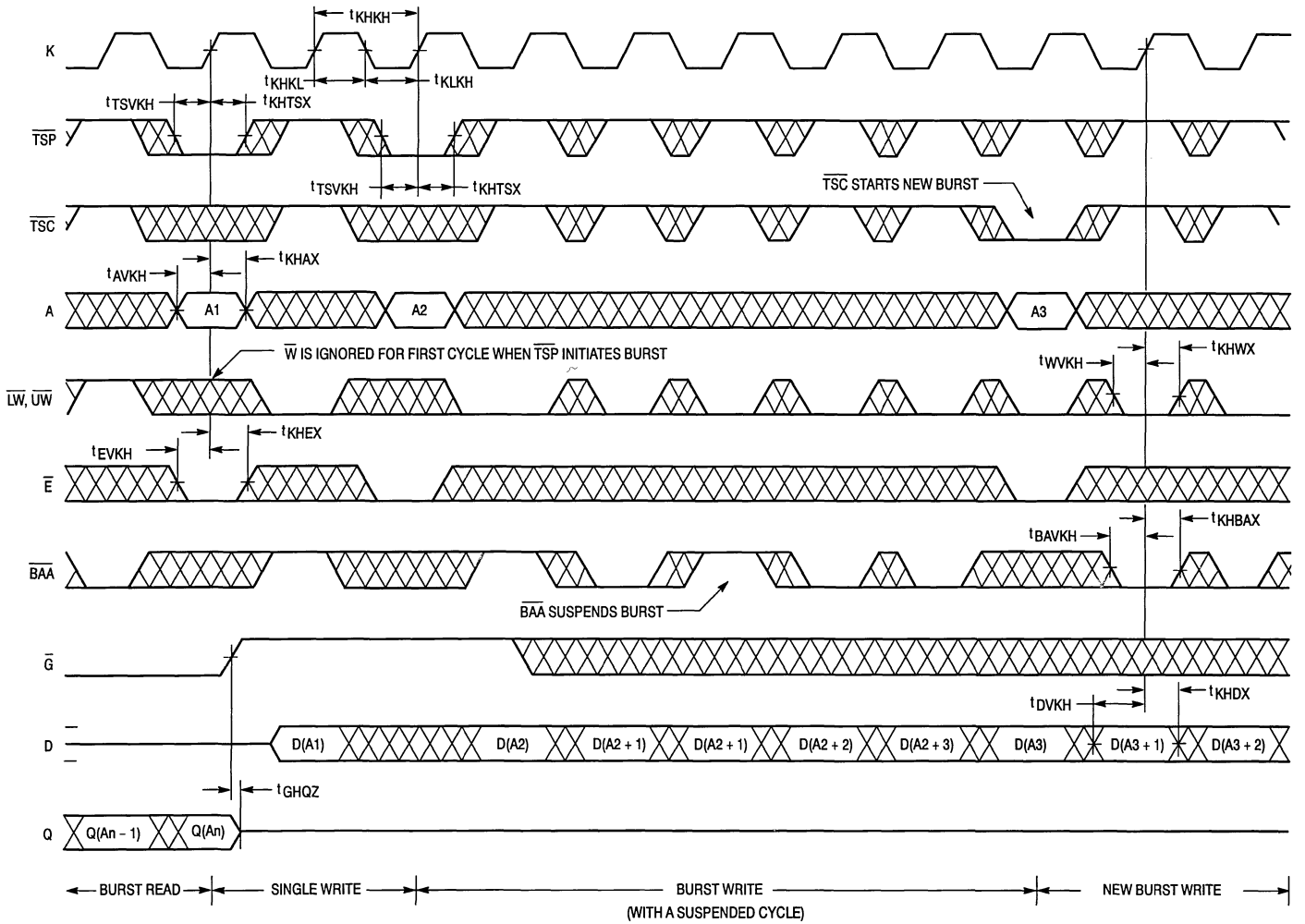
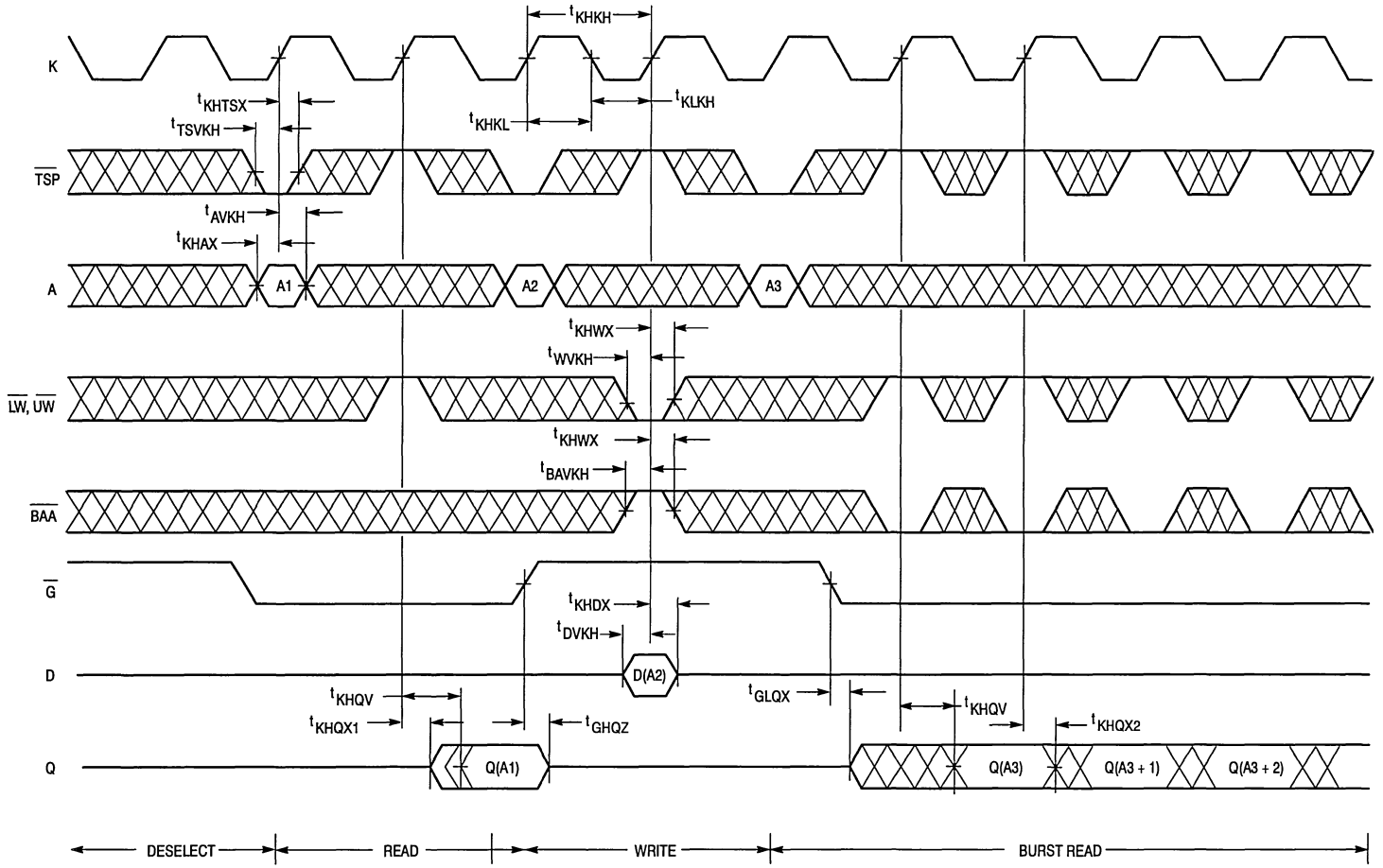
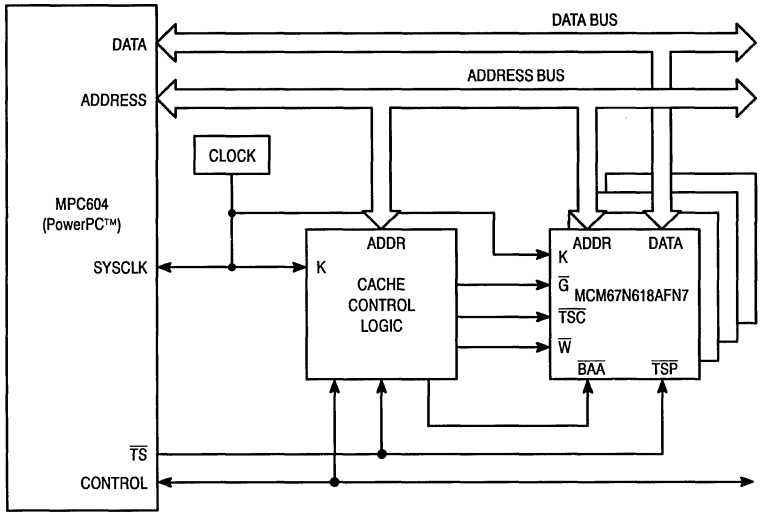
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{TSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67N618AFN7s with a 66 MHz (bus speed) MPC604 PowerPC

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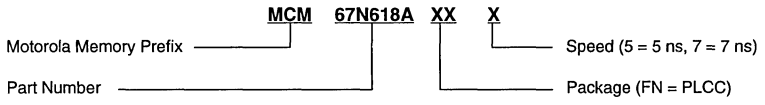
ORDERING INFORMATION
(Order by Full Part Number)

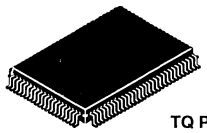


Full Part Numbers — MCM67N618AFN5 MCM67N618AFN7

MCM69F536

Product Preview

32K x 36 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F536 is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 36 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. This device integrates input registers, a 2 bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F536 (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$) and synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, and so on. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F536 operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible and 5 V tolerant.

- MCM69F536–8.5 = 8.5 ns access / 12 ns cycle
  MCM69F536–10 = 10 ns access / 15 ns cycle
  MCM69F536–12 = 12 ns access / 16.6 ns cycle
- Single 3.3 V ± 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant I/O
- 100 Pin TQFP Package

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BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.
i960 and Pentium are trademarks of Intel Corp.

REV 2
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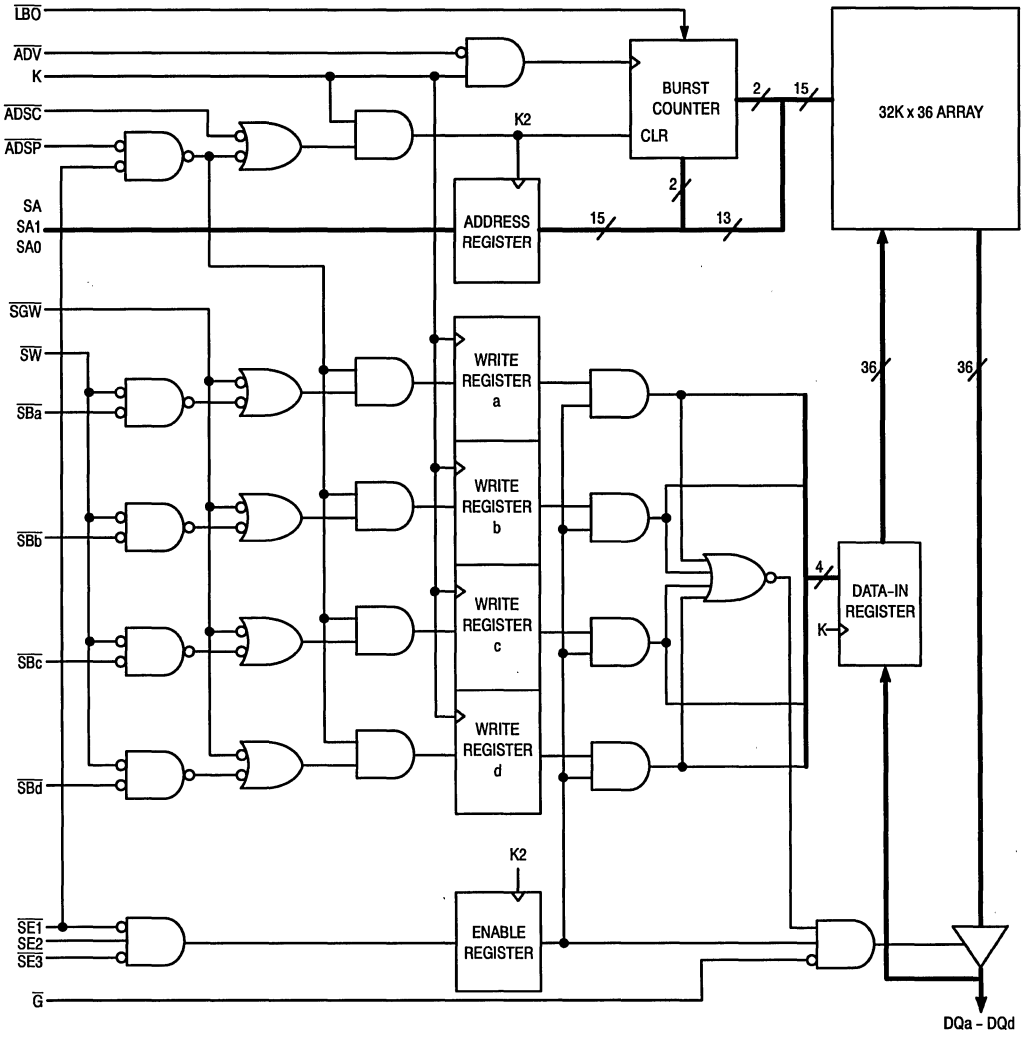
FUNCTIONAL BLOCK DIAGRAM



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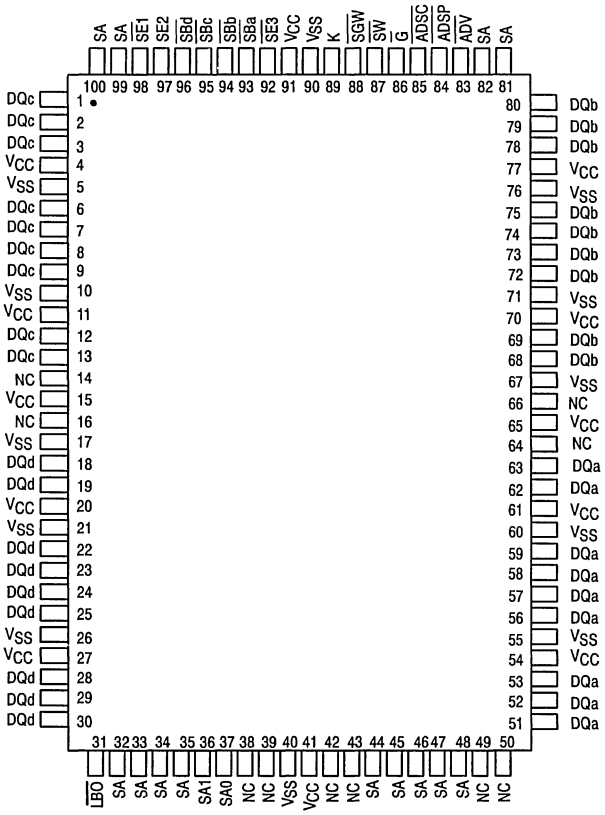
PIN ASSIGNMENTS



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst count (68K/PowerPC) High–interleaved burst count (486/i960/Pentium)
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V ± 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{CC}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

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ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance (Still Air)		—	—	—	1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	—	—	±1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	—	±1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F536–8.5 MCM69F536–10 MCM69F536–12	I_{CCA}	—	—	TBD	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} − 0.2 V)	MCM69F536–8.5 MCM69F536–10 MCM69F536–12	I_{SB1}	—	—	TBD	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} − 0.2 V)	MCM69F536–8.5 MCM69F536–10 MCM69F536–12	I_{SB2}	—	—	TBD	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)		V_{OH}	2.4	—	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69F536–8.5		MCM69F536–10		MCM69F536–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	6	ns	5
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	6	ns	5
Setup Times: Address	t_{ADKH}	2.5	—	2.5	—	2.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADSKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load.
5. Measured at ± 200 mV from steady state. Tested per High–Z Test Load.

AC TEST LOADS

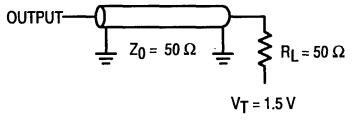


Figure 1A. AC Test Load

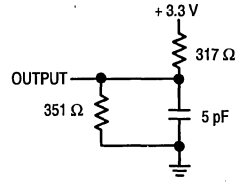
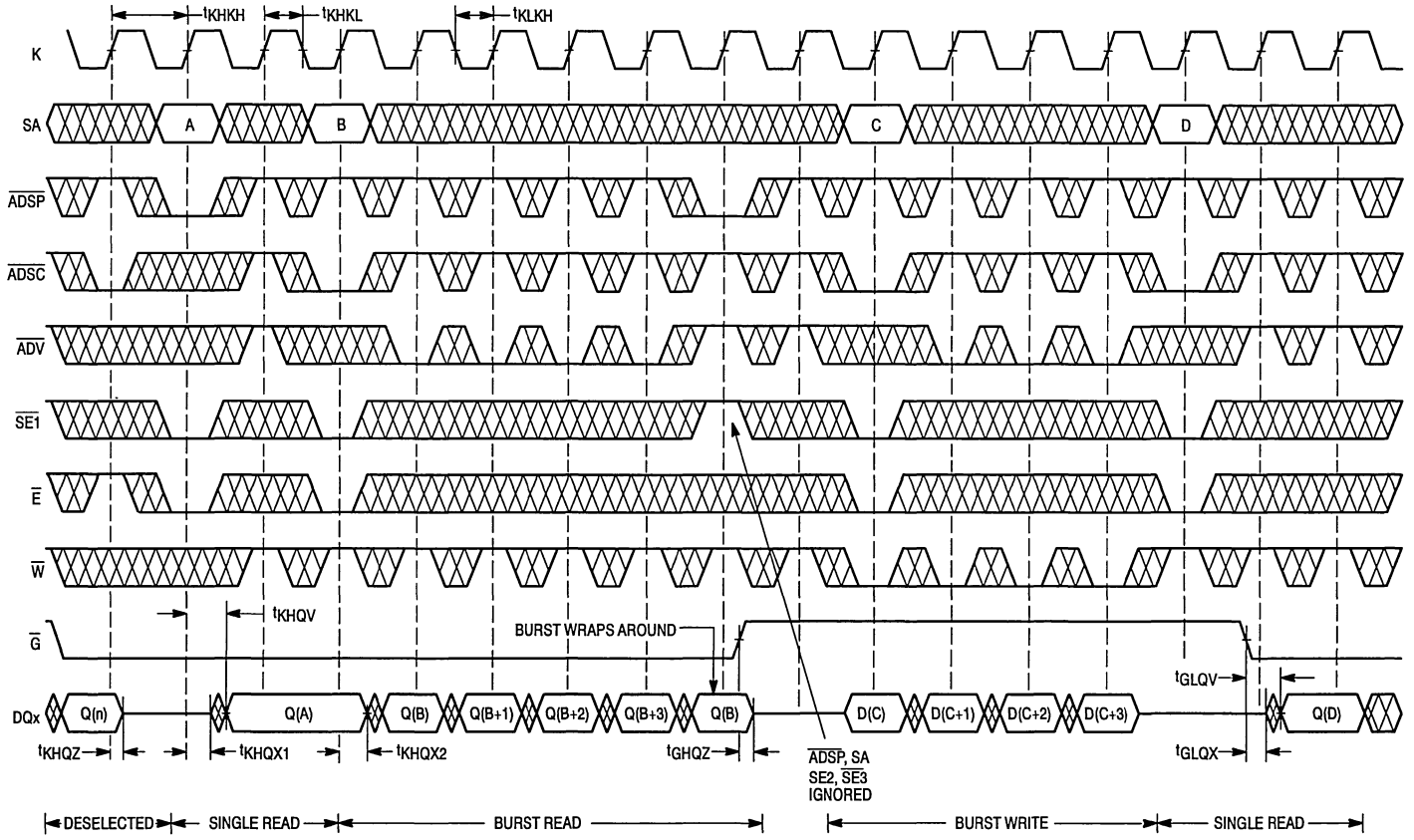


Figure 1B. High–Z Test Load

READ/WRITE CYCLES



NOTE: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and/or $\overline{SW}$ and $\overline{SBx}$ low.

The MCM69F536 BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, flow–through (non–pipelined) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F536 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69F536) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69F536 device can replace two of the 5 V 32Kx18 devices or replace four of the 5 V 32Kx9 devices. Below is a table that lists control pins on the MCM69F536 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM62486B	—	—	—	L	H
MCM62940B	—	—	—	L	L
MCM67B518	—	—	—	L	H
MCM67H518	—	—	—	—	H
MCM67M518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as it was intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F536. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Desired Operation	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

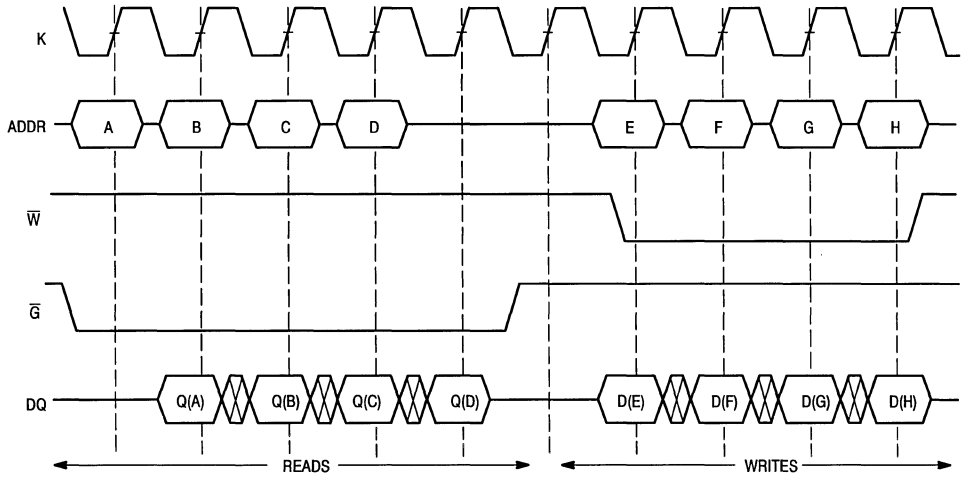
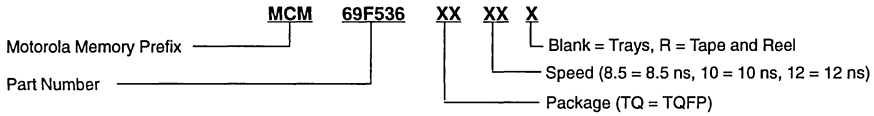


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)



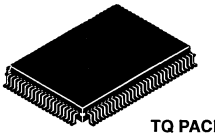
Full Part Numbers — MCM69F536TQ8.5 MCM69F536TQ10 MCM69F536TQ12
MCM69F536TQ8.5R MCM69F536TQ10R MCM69F536TQ12R

5

MCM69P536

Product Preview

32K x 36 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P536 is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 32K words of 36 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P536 (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to all bytes. The four bytes are designated as "a", "b", "c", and "d". $\overline{SBa}$ controls DQa, $\overline{SBb}$ controls DQb, etc. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. All bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P536 operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible and 5 V tolerant.

- MCM69P536–5 = 5 ns access / 10 ns cycle
  MCM69P536–6 = 6 ns access / 12 ns cycle
  MCM69P536–7 = 7 ns access / 13.3 ns cycle
- Single 3.3 V ± 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant I/O
- 100 Pin TQFP Package

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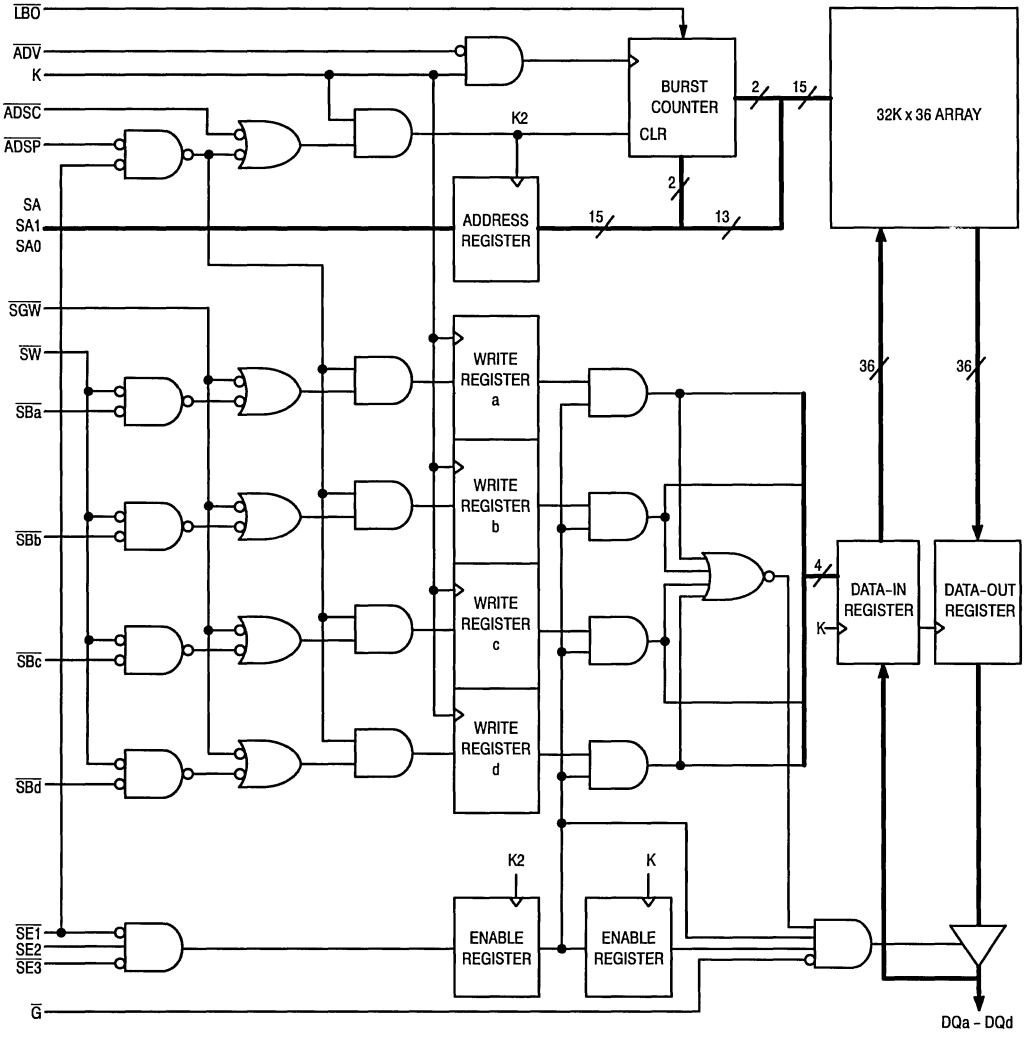
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.
i960 and Pentium are trademarks of Intel Corp.

REV2
5/95

FUNCTIONAL BLOCK DIAGRAM



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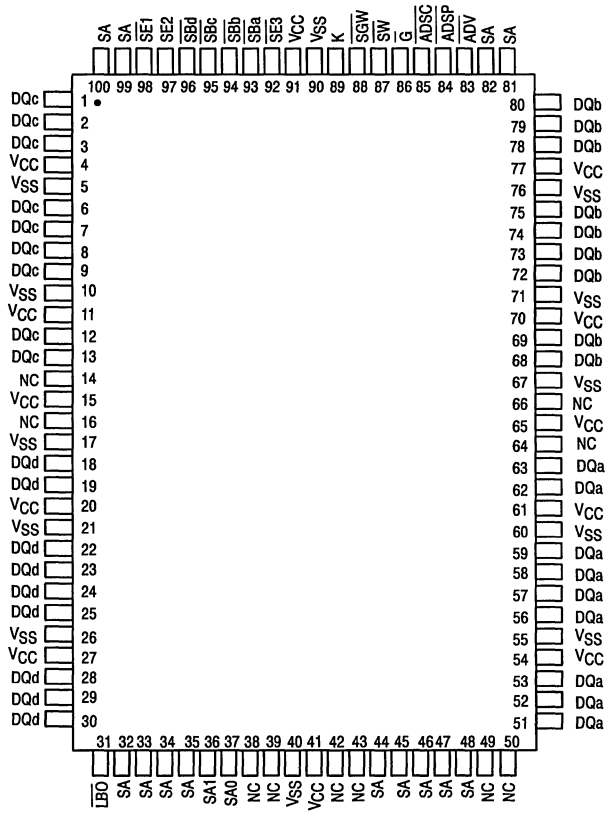
PIN ASSIGNMENTS



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
32, 33, 34, 35, 44, 45, 46, 47, 48, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
93, 94, 95, 96 (a) (b) (c) (d)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b, c, d). $\overline{SGW}$ overrides $\overline{SBx}$.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst counter (68K/PowerPC) High–interleaved burst counter (486/i960/Pentium)
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V ± 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
14, 16, 38, 39, 42, 43, 49, 50, 66	NC	—	No Connection: There is no connection to the chip.

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TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{CC}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$	$\overline{SBc}$	$\overline{SBd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte a	H	L	L	H	H	H
Write Byte b	H	L	H	L	H	H
Write Byte c	H	L	H	H	L	H
Write Byte d	H	L	H	H	H	L
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance (Still Air)		—	—	—	1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69P536–5 MCM69P536–6 MCM69P536–7	I_{CCA}	—	—	TBD	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69P536–5 MCM69P536–6 MCM69P536–7	I_{SB1}	—	—	TBD	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69P536–5 MCM69P536–6 MCM69P536–7	I_{SB2}	—	—	TBD	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4 mA)		V_{OH}	2.4	—	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69P536–5		MCM69P536–6		MCM69P536–7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	13.3	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	ns	5
Clock High to Q High–Z	t_{KHQZ}	2	5	2	5	2	5	ns	5
Setup Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{ADKH} t_{ADSKH} t_{DVKH} t_{WVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: Address $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ Data In Write Chip Enable	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load.
5. Measured at ± 200 mV from steady state. Tested per High–Z Test Load.

AC TEST LOADS

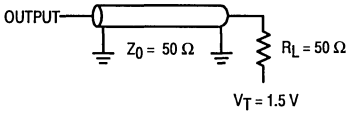

Figure 1A. AC Test Load

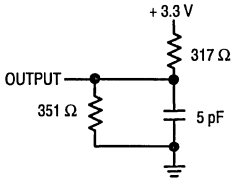

Figure 1B. High–Z Test Load

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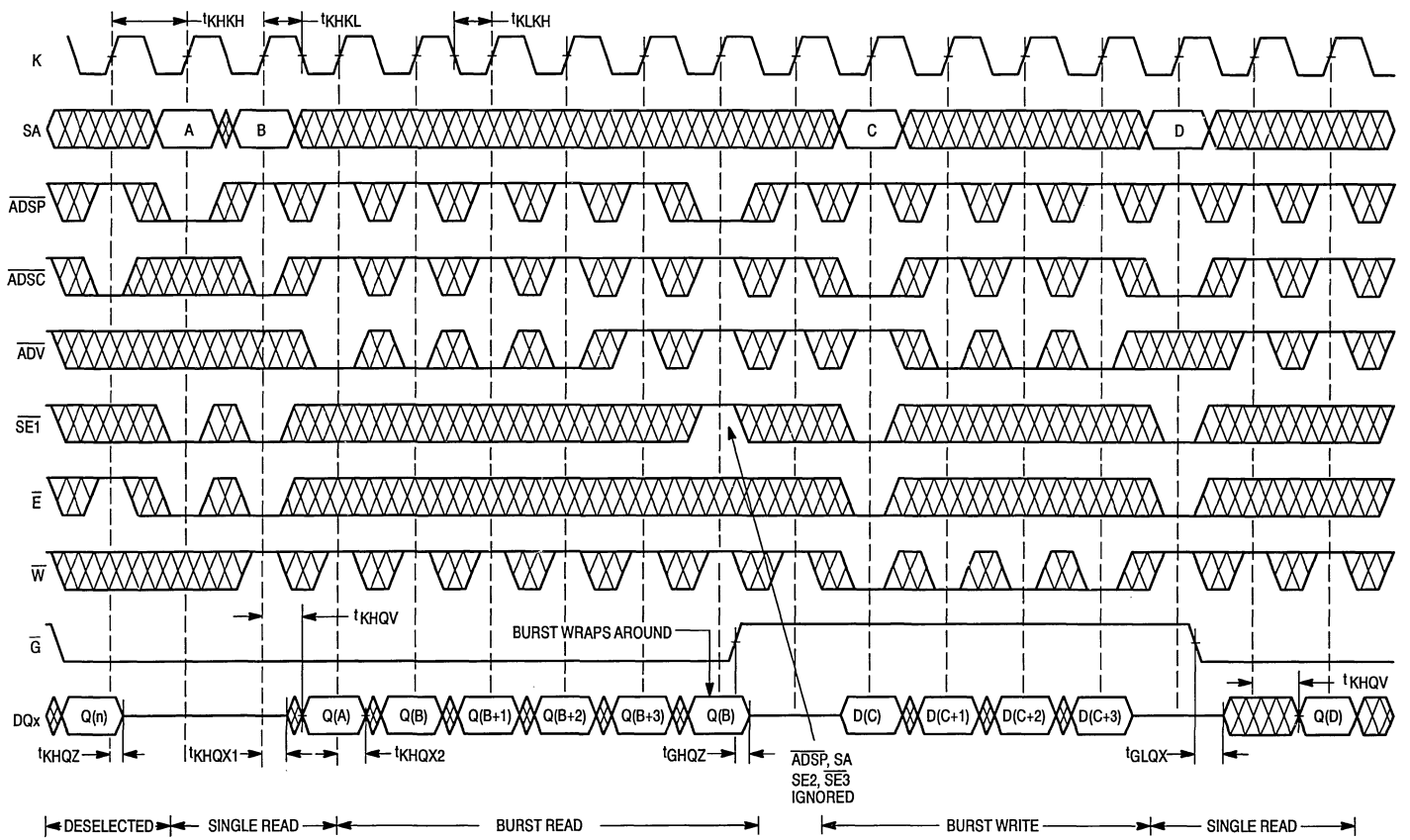
READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69P536 BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 32Kx36 BurstRAM (MCM69P536) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P536 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69P536) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V PLCC devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc. options. A single MCM69P536 device can replace two of the 5 V 32Kx18 devices. The MCM69P536 can be configured to function as if it were one of the 5 V BurstRAMs. Below is a table that lists control pins on the MCM69P536 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C518	—	—	—	L	H
MCM67J518	—	—	—	—	H
MCM67N518	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P536. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

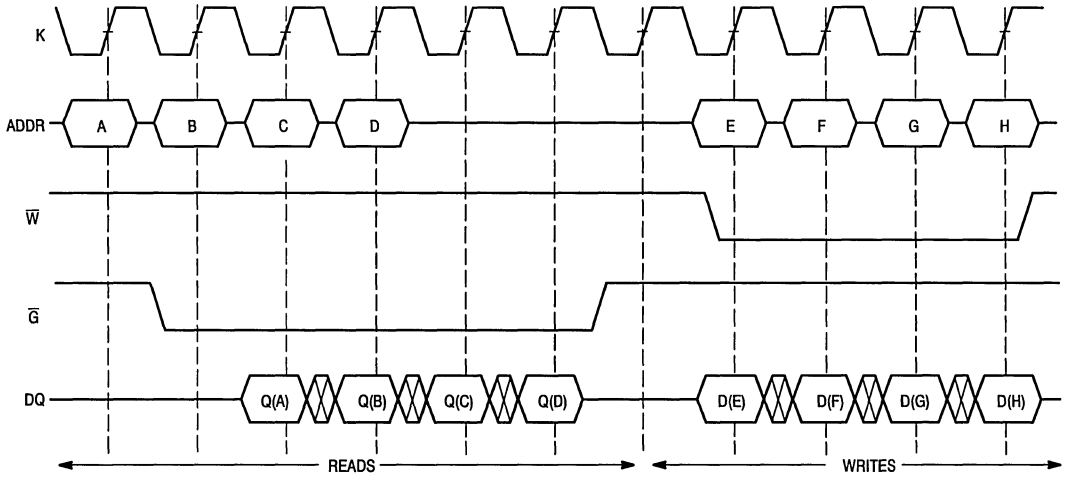
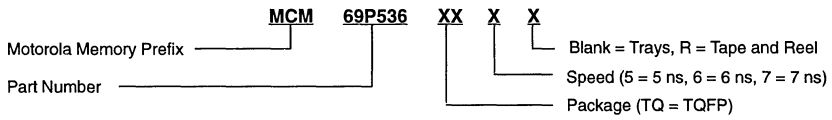


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)



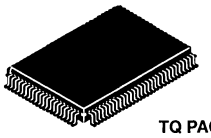
Full Part Numbers — MCM69P536TQ5 MCM69P536TQ6 MCM69P536TQ7
MCM69P536TQ5R MCM69P536TQ6R MCM69P536TQ7R

5

MCM69F618

Product Preview

64K x 18 Bit Flow–Through BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69F618 is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 64K words of 18 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. This device integrates input registers, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69F618 (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to both bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. Both bytes are written if either $\overline{SGW}$ is asserted or if all $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, a flow–through SRAM allows output data to simply flow freely from the memory array.

The MCM69F618 operates from a 3.3 V power supply and all inputs and outputs are LVTTL compatible and 5 V tolerant.

- MCM69F618–8.5 = 8.5 ns access / 12 ns cycle
  MCM69F618–10 = 10 ns access / 15 ns cycle
  MCM69F618–12= 12 ns access / 16.6 ns cycle
- Single 3.3 V ± 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant I/O
- 100 Pin TQFP Package

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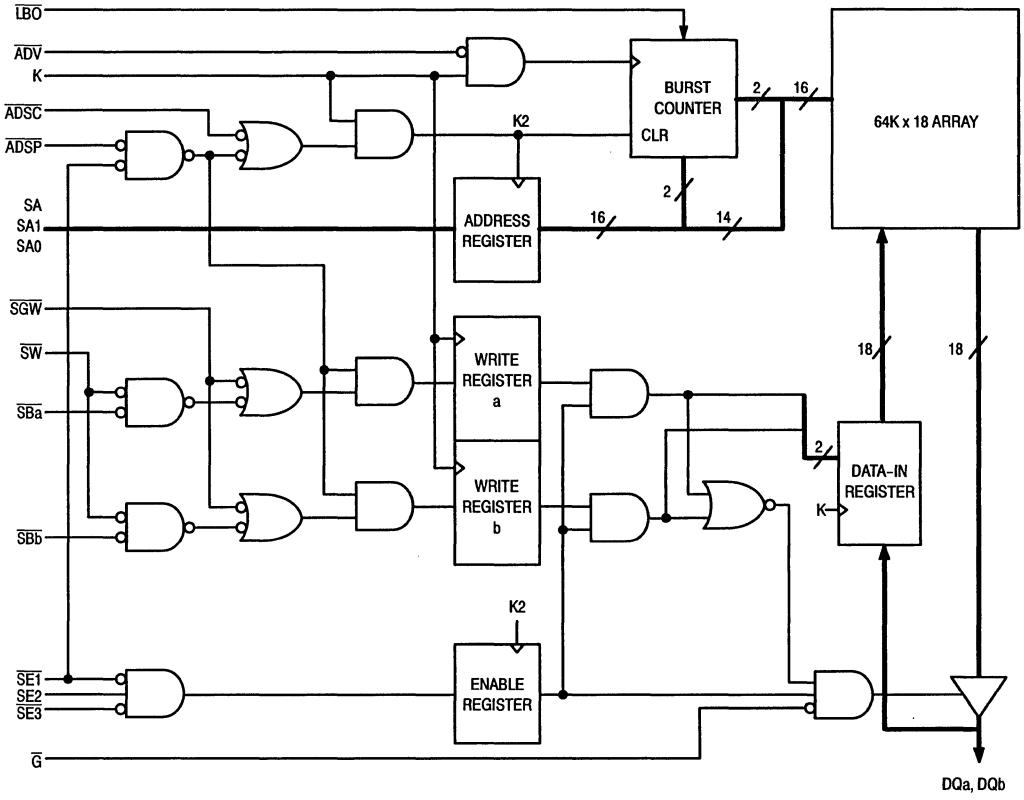
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.
i960 and Pentium are trademarks of Intel Corp.

REV2
5/95

FUNCTIONAL BLOCK DIAGRAM



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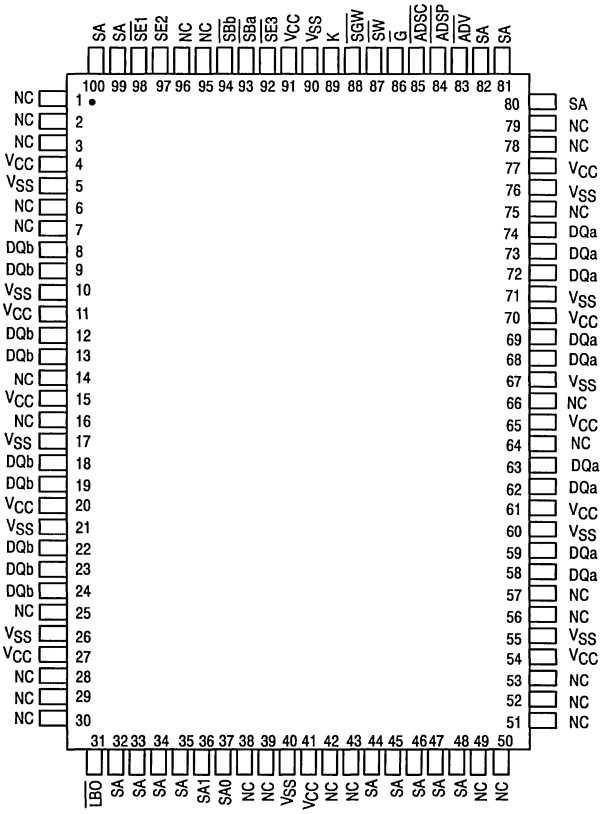
PIN ASSIGNMENTS



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
32, 33, 34, 35, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst counter (68K/PowerPC) High–interleaved burst counter (486/i960/Pentium)
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented this Sleep Mode (ZZ) feature.
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V ± 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	0	DQ	READ
Begin Read	External	0	1	0	1	0	X	0	DQ	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO}$ = V_{SS})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X00	X . . . X01	X . . . X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO}$ = V_{CC})

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X00	X . . . X11	X . . . X10
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . . X10	X . . . X01	X . . . X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

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ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance (Still Air)		—	—	—	1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC})		$I_{lkg(O)}$	—	—	± 1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time ≥ t_{KHKH} min)	MCM69F618–8.5 MCM69F618–10 MCM69F618–12	I_{CCA}	—	—	TBD	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69F618–8.5 MCM69F618–10 MCM69F618–12	I_{SB1}	—	—	TBD	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time ≥ t_{KHKH}, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS}$ + 0.2 V or ≥ V_{CC} – 0.2 V)	MCM69F618–8.5 MCM69F618–10 MCM69F618–12	I_{SB2}	—	—	TBD	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4 mA)		V_{OH}	2.4	—	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69F618–8.5		MCM69F618–10		MCM69F618–12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	12	—	15	—	16.6	—	ns	
Clock High Pulse Width	t_{KHKL}	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	6	—	ns	
Clock Access Time	t_{KHQV}	—	8.5	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	6	ns	5
Clock High to Q High–Z	t_{KHQZ}	3	5	3	5	3	6	ns	5
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load.
5. Measured at ± 200 mV from steady state. Tested per High–Z test load.

AC TEST LOADS

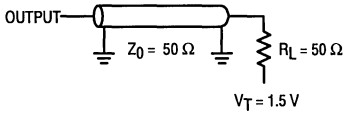


Figure 1A. AC Test Load

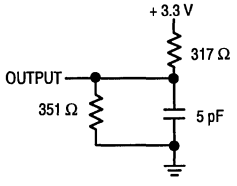
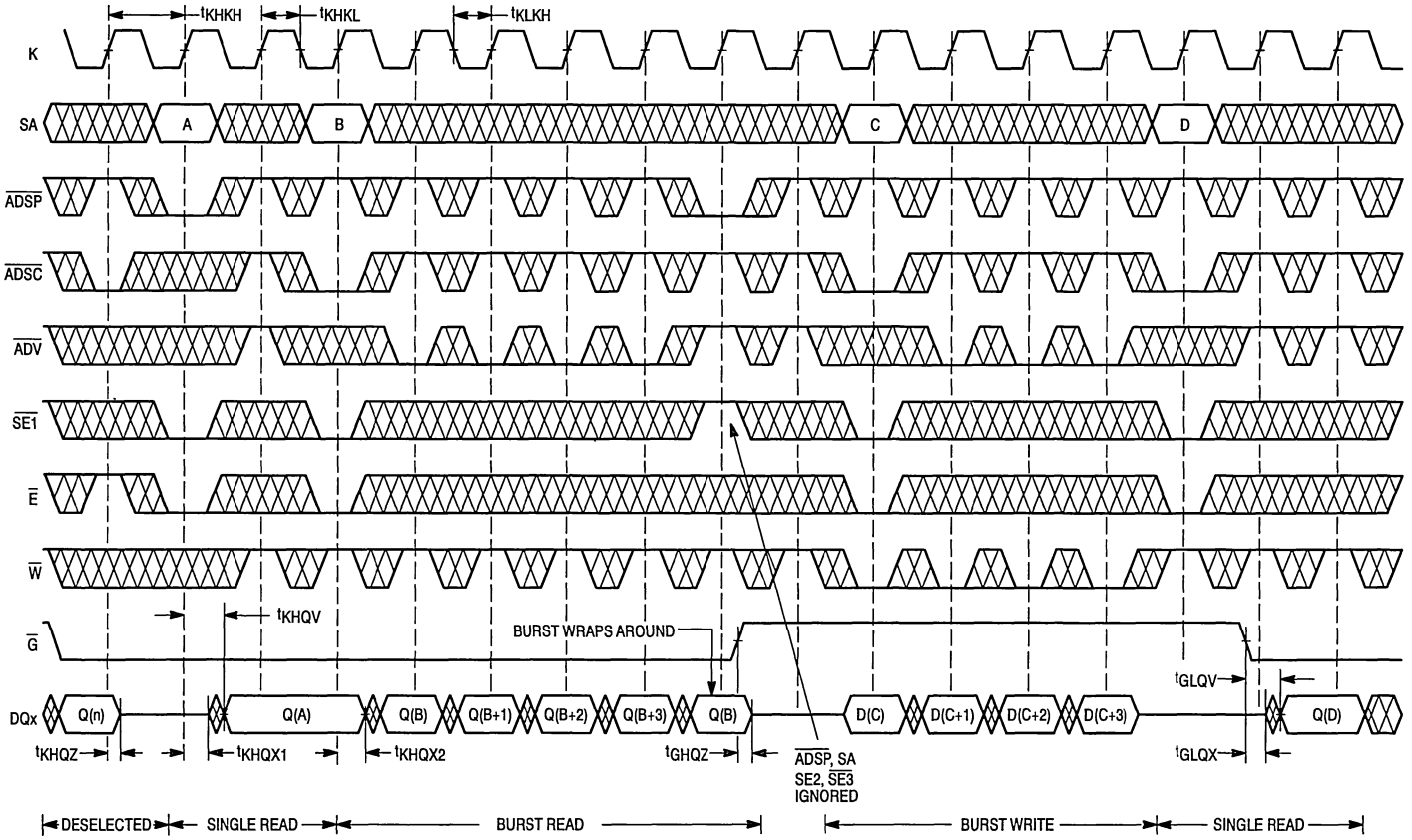


Figure 1B. High–Z Test Load

READ/WRITE CYCLES



Note: E low = SE2 high and SE3 low.
W low = SGW low and/or SW and SBx low.

APPLICATION INFORMATION

The MCM69F618 BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, flow–through (non–pipelined) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 18 BurstRAM (MCM69P618) allows the designer to maintain zero–wait state operation. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

For L2 cache designs that must minimize both latency and wait states, flow–through BurstRAMs are the best choice in achieving the highest performance in L2 cache design.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69F618 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69F618) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipeline support ("H" part), etc., options. The MCM69F618 can be configured to function as if it were one of the 5 V BurstRAMs. The following table lists control pins on the MCM69F618 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67B618	—	—	—	L	H
MCM67H618	—	—	—	—	H
MCM67M618	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69F618. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst Flow–Through SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

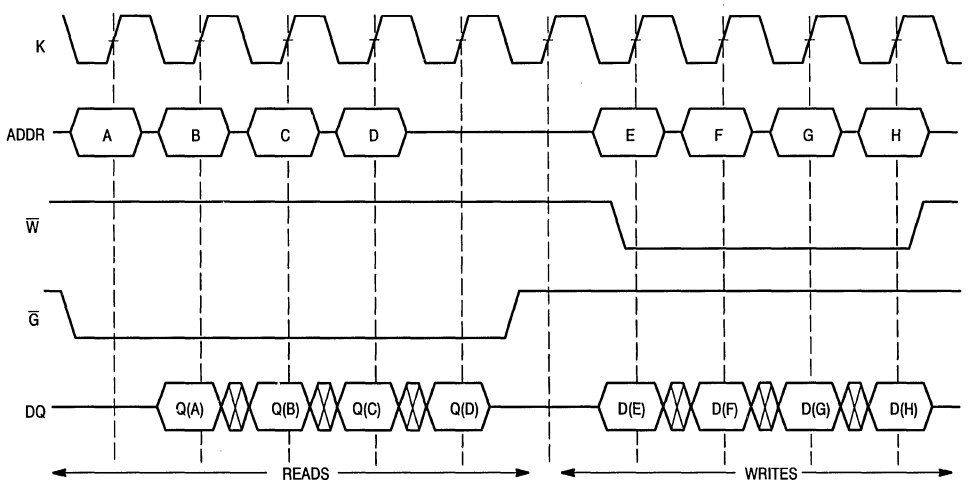
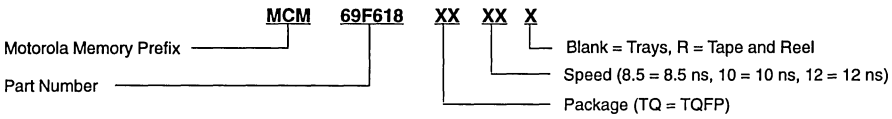


Figure 2. Configured as Non–Burst Synchronous SRAM

ORDERING INFORMATION
(Order by Full Part Number)



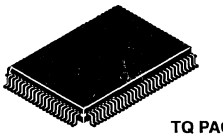
Full Part Numbers — MCM69F618TQ8.5 MCM69F618TQ10 MCM69F618TQ12
MCM69F618TQ8.5R MCM69F618TQ10R MCM69F618TQ12R

5

MCM69P618

Product Preview

64K x 18 Bit Pipelined BurstRAM™ Synchronous Fast Static RAM



TQ PACKAGE
TQFP
CASE 983A–01

The MCM69P618 is a 1M bit synchronous fast static RAM designed to provide a burstable, high performance, secondary cache for the 68K Family, PowerPC™, 486, i960™ and Pentium™ microprocessors. It is organized as 64K words of 18 bits each, fabricated with Motorola's high performance silicon gate BiCMOS technology. This device integrates input registers, an output register, a 2–bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (SA), data inputs (DQx), and all control signals except output enable ($\overline{G}$) and Linear Burst Order ($\overline{LBO}$) are clock (K) controlled through positive–edge–triggered noninverting registers.

Bursts can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ input pins. Subsequent burst addresses can be generated internally by the MCM69P618 (burst sequence operates in linear or interleaved mode dependent upon state of $\overline{LBO}$) and controlled by the burst address advance ($\overline{ADV}$) input pin.

Write cycles are internally self–timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off–chip write pulse generation and provides increased timing flexibility for incoming signals.

Synchronous byte write ($\overline{SBx}$), synchronous global write ($\overline{SGW}$), and synchronous write enable $\overline{SW}$ are provided to allow writes to either individual bytes or to both bytes. The two bytes are designated as "a" and "b". $\overline{SBa}$ controls DQa and $\overline{SBb}$ controls DQb. Individual bytes are written if the selected byte writes $\overline{SBx}$ are asserted with $\overline{SW}$. Both bytes are written if either $\overline{SGW}$ is asserted or if both $\overline{SBx}$ and $\overline{SW}$ are asserted.

For read cycles, pipelined SRAMs output data is temporarily stored by an edge–triggered output register and then released to the output buffers at the next rising edge of clock (K).

The MCM69P618 operates from a single 3.3 V power supply and all inputs and outputs are LVTTL compatible and 5 V tolerant.

- MCM69P618–5 = 5 ns access / 10 ns cycle
  MCM69P618–6 = 6 ns access / 12 ns cycle
  MCM69P618–7 = 7 ns access / 13.3 ns cycle
- Single 3.3 V ± 5% Power Supply
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self–Timed Write Cycle
- Byte Write and Global Write Control
- 5 V Tolerant I/O
- 100 Pin TQFP Package

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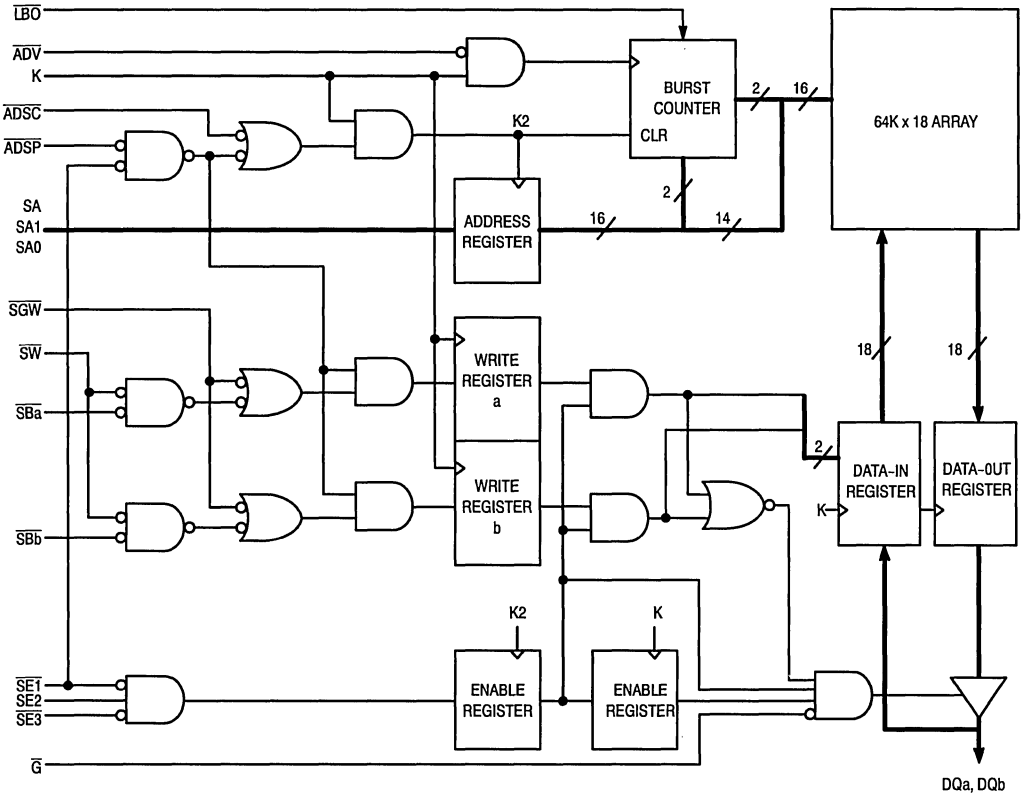
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.
i960 and Pentium are trademarks of Intel Corp.

REV2
5/95

FUNCTIONAL BLOCK DIAGRAM



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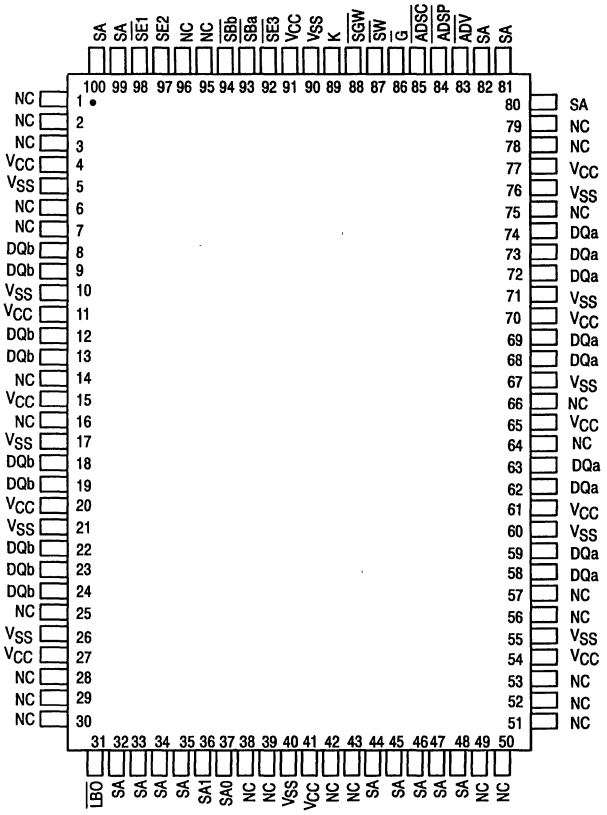
PIN ASSIGNMENTS



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
32, 33, 34, 35, 44, 45, 46, 47, 48, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA1,SA0	Input	Synchronous Address Inputs: these pins must be wired to the two LSBs of the address bus for proper burst operation. These inputs are registered and must meet setup and hold times.
89	K	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{G}$ and $\overline{LBO}$.
93, 94 (a) (b)	$\overline{SBx}$	Input	Synchronous Byte Write Inputs: "x" refers to the byte being written (byte a, b). $\overline{SGW}$ overrides $\overline{SBx}$.
87	$\overline{SW}$	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write $\overline{SBx}$ pins. If only byte write signals $\overline{SBx}$ are being used, tie this pin low.
88	$\overline{SGW}$	Input	Synchronous Global Write: This signal writes all bytes regardless of the status of the $\overline{SBx}$ and $\overline{SW}$ signals. If only byte write signals $\overline{SBx}$ are being used, tie this pin high.
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: Initiates READ, WRITE or chip deselect cycle (exception – chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{SE1}$ is high).
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: Initiates READ, WRITE or chip deselect cycle.
83	$\overline{ADV}$	Input	Synchronous Address Advance: Increments address count in accordance with counter type selected (linear/interleaved).
98	$\overline{SE1}$	Input	Synchronous Chip Enable: Active low to enable chip. Negated high–blocks $\overline{ADSP}$ or deselects chip when $\overline{ADSC}$ is asserted.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	$\overline{SE3}$	Input	Synchronous Chip Enable: Active low for depth expansion.
31	$\overline{LBO}$	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low–linear burst counter (68K/PowerPC) High–interleaved burst counter (486/i960/Pentium)
64	NC	Input	No Connection: There is no connection to the chip. For compatibility reasons, it is recommended that this pin be tied low for system designs that do not have a sleep mode associated with the cache/memory controller. Other vendors' RAMs may have implemented the Sleep Mode (ZZ) feature.
86	$\overline{G}$	Input	Asynchronous Output Enable Input: Low–enables output buffers (DQx pins). High – DQx pins are high impedance.
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	V_{CC}	Supply	Power Supply: 3.3 V ± 5%
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Supply	Ground
1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE (See Notes 1 through 4)

Next Cycle	Address Used	$\overline{SE1}$	SE2	$\overline{SE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{G}$ [3]	DQx	Write [2, 4]
Deselect	None	1	X	X	X	0	X	X	High–Z	X
Deselect	None	0	X	1	0	X	X	X	High–Z	X
Deselect	None	0	0	X	0	X	X	X	High–Z	X
Deselect	None	X	X	1	1	0	X	X	High–Z	X
Deselect	None	X	0	X	1	0	X	X	High–Z	X
Begin Read	External	0	1	0	0	X	X	X	High–Z	READ
Begin Read	External	0	1	0	1	0	X	X	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	1	High–Z	READ
Continue Read	Next	X	X	X	1	1	0	0	DQ	READ
Continue Read	Next	1	X	X	X	1	0	1	High–Z	READ
Continue Read	Next	1	X	X	X	1	0	0	DQ	READ
Suspend Read	Current	X	X	X	1	1	1	1	High–Z	READ
Suspend Read	Current	X	X	X	1	1	1	0	DQ	READ
Suspend Read	Current	1	X	X	X	1	1	1	High–Z	READ
Suspend Read	Current	1	X	X	X	1	1	0	DQ	READ
Begin Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Begin Write	Current	1	X	X	X	1	1	X	High–Z	WRITE
Begin Write	External	0	1	0	1	0	X	X	High–Z	WRITE
Continue Write	Next	X	X	X	1	1	0	X	High–Z	WRITE
Continue Write	Next	1	X	X	X	1	0	X	High–Z	WRITE
Suspend Write	Current	X	X	X	1	1	1	X	High–Z	WRITE
Suspend Write	Current	1	X	X	X	1	1	X	High–Z	WRITE

NOTES: 1. X = Don't Care. 1 = logic high. 0 = logic low.
2. Write is defined as either 1) any $\overline{SBx}$ and $\overline{SW}$ low or 2) $\overline{SGW}$ is low.
3. $\overline{G}$ is an asynchronous signal and is not sampled by the clock K. $\overline{G}$ drives the bus immediately (t_{GLQX}) following $\overline{G}$ going low.
4. On write cycles that follow read cycles, $\overline{G}$ must be negated prior to the start of the write cycle to ensure proper write data setup times. $\overline{G}$ must also remain negated at the completion of the write cycle to ensure proper write data hold times.

LINEAR BURST ADDRESS TABLE ($\overline{LBO} = V_{SS}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{LBO} = V_{CC}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

WRITE TRUTH TABLE

Cycle Type	$\overline{SGW}$	$\overline{SW}$	$\overline{SBa}$	$\overline{SBb}$
Read	H	H	X	X
Read	H	L	H	H
Write Byte a	H	L	L	H
Write Byte b	H	L	H	L
Write All Bytes	H	L	L	L
Write All Bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Package Power Dissipation (See Note 2)	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Storage Temperature	T_{stg}	– 55 to 125	°C

NOTES: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

2. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

PACKAGE THERMAL CHARACTERISTICS

Rating		Symbol	Max	Unit	Notes
Thermal Resistance (Still Air)		—	—	—	1
Junction to Ambient (@ 200 lfm)	Single Layer Board Four Layer Board	$R_{\theta JA}$	40 25	°C/W	2
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:
1. Junction temperature is a function of on–chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38–87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC–883 Method 1012.1).

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Operating Temperature	T_J	20	—	110	°C
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5**	V

* $V_{IL} \geq -2$ V for $t \leq t_{KHKH}/2$.
** $V_{IH} \leq 6$ V for $t \leq t_{KHKH}/2$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current ($0 \text{ V} \leq V_{in} \leq V_{CC}$)		$I_{lkg(I)}$	—	—	±1	µA
Output Leakage Current ($0 \text{ V} \leq V_{in} \leq V_{CC}$)		$I_{lkg(O)}$	—	—	±1	µA
AC Supply Current (Device Selected, All Outputs Open, All Inputs Toggling at $V_{in} \leq V_{IL}$ or $\geq V_{IH}$, Cycle Time $\geq t_{KHKH}$ min)	MCM69P618–5 MCM69P618–6 MCM69P618–7	I_{CCA}	—	—	TBD	mA
CMOS Standby Supply Current (Deselected[1], Clock (K) Cycle Time $\geq t_{KHKH}$, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS} + 0.2$ V or $\geq V_{CC} - 0.2$ V)	MCM69P618–5 MCM69P618–6 MCM69P618–7	I_{SB1}	—	—	TBD	mA
Clock Running Supply Current (Deselected[1], Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS} + 0.2$ V or $\geq V_{CC} - 0.2$ V)	MCM69P618–5 MCM69P618–6 MCM69P618–7	I_{SB2}	—	—	TBD	mA
Output Low Voltage (I_{OL} = 8 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = –4 mA)		V_{OH}	2.4	—	—	V

NOTE: 1. Device in Deselected mode as defined by the Truth Table.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	6	pF
Input/Output Capacitance	$C_{I/O}$	—	7	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_J = 20 to 110°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM69P618–5		MCM69P618–6		MCM69P618–7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12	—	13.3	—	ns	
Clock High Pulse Width	t_{KHKL}	3	—	4	—	4.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	3	—	4	—	4.5	—	ns	
Clock Access Time	t_{KHQV}	—	5	—	6	—	7	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	0	—	0	—	0	—	ns	4
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4
Output Disable to Q High–Z	t_{GHQZ}	—	5	—	5	—	5	ns	5
Clock High to Q High–Z	t_{KHQZ}	2	5	2	5	2	5	ns	5
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{ADKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	
$\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	t_{KHADX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Chip Enable	t_{KHEX}								

NOTES:
1. Write is defined as either any $\overline{SBx}$ and $\overline{SW}$ low or $\overline{SGW}$ is low. Chip Enable is defined as $\overline{SE1}$ low, SE2 high and $\overline{SE3}$ low whenever $\overline{ADSP}$ or $\overline{ADSC}$ is asserted.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care after write cycle begins. To prevent bus contention, $\overline{G}$ should be negated prior to start of write cycle.
4. Tested per AC Test Load.
5. Measured at ± 200 mV from steady state. Tested per High–Z test load.

AC TEST LOADS

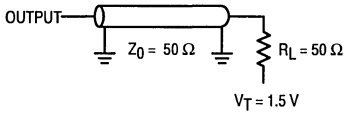


Figure 1A. AC Test Load

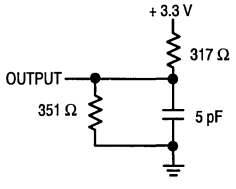
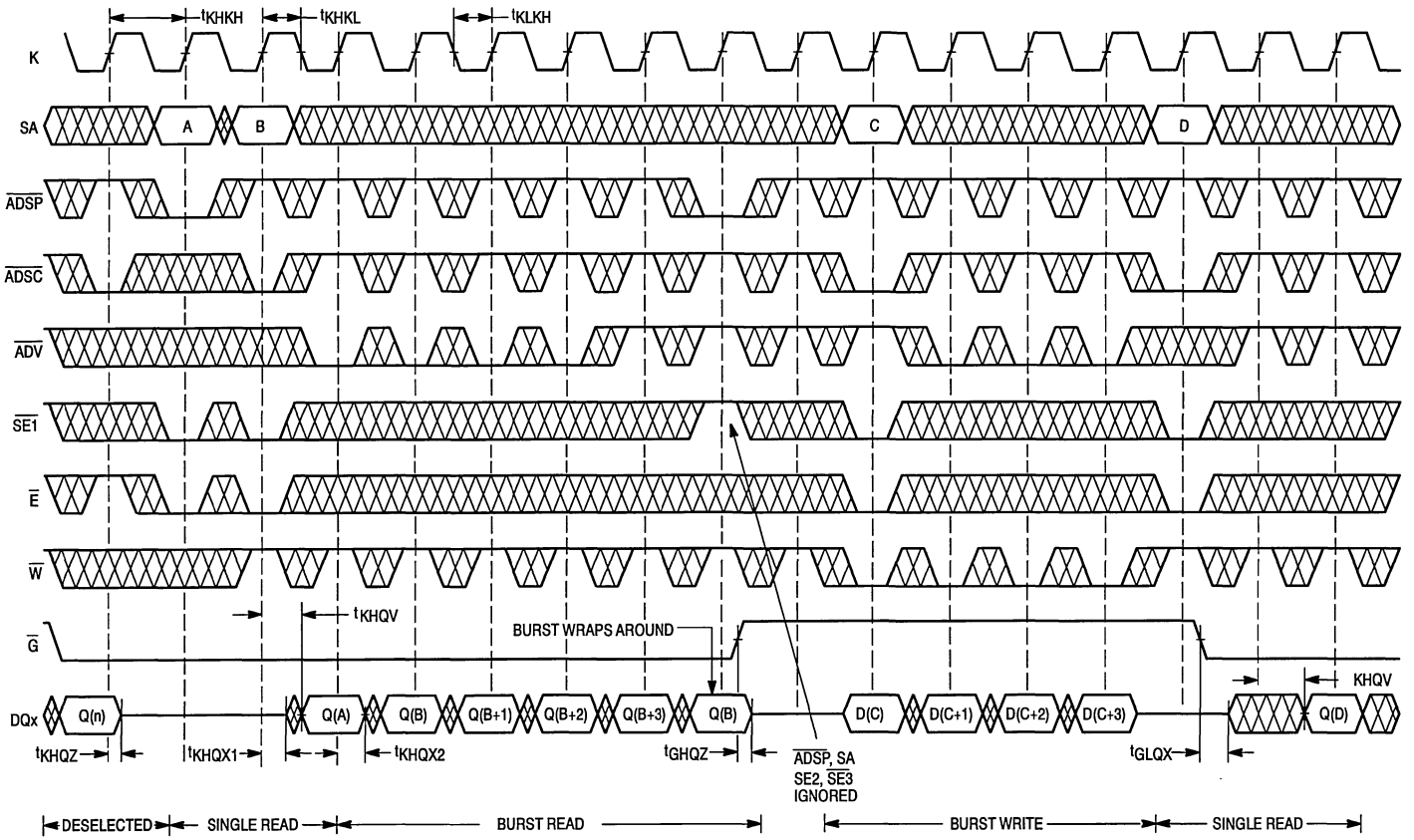


Figure 1B. High–Z Test Load

5

READ/WRITE CYCLES



Note: $\overline{E}$ low = SE2 high and $\overline{SE3}$ low.
$\overline{W}$ low = $\overline{SGW}$ low and / or $\overline{SW}$ and $\overline{SBx}$ low.

APPLICATION INFORMATION

The MCM69P618 BurstRAM is a high speed synchronous SRAM that is intended for use primarily in secondary or level two (L2) cache memory applications. L2 caches are found in a variety of classes of computers – from the desktop personal computer to the high–end servers and transaction processing machines. For simplicity, the majority of L2 caches today are direct mapped and are single bank implementations. These caches tend to be designed for bus speeds in the range of 33 to 66 MHz. At these bus rates, non–pipelined (flow–through) BurstRAMs can be used since their access times meet the speed requirements for a minimum–latency, zero–wait state L2 cache interface. Latency is a measure (time) of "dead" time the memory system exhibits as a result of a memory request.

For those applications that demand bus operation at greater than 66 MHz or multi–bank L2 caches at 66 MHz, the pipelined (register/register) version of the 64K x 18 BurstRAM (MCM69P618) allows the user to configure the RAM to support such designs. Multiple banks of BurstRAMs create additional bus loading and can cause the system to otherwise miss its timing requirements. The access time (clock–to–valid–data) of a pipelined BurstRAM is inherently faster than a non–pipelined device by a few nanoseconds. This does not come without cost. The cost is latency – "dead" time.

Since most L2 caches are tied to the processor bus and bus speeds continue to increase over time, pipelined (R/R) BurstRAMs are the best choice in achieving zero–wait state L2 cache performance. At bus speeds ranging from 66 MHz to 100 MHz, pipelined BurstRAMs are able to provide fast clock to valid data times required of these high speed buses.

FUNCTIONAL EQUIVALENT

The following describes the configuration of the MCM69P618 as a functional equivalent to a 5 V BurstRAM. A migration from 5 V BurstRAMs to 3.3 V BurstRAMs (e.g. MCM69P618) can be somewhat confusing due to functional and pinout differences. Because the 3.3 V devices offer more pins than the 5 V devices, it is no longer necessary to supply multiple part numbers for the different burst, address pipelined, etc., options. The MCM69P618 can be configured to function as if it were one of the 5 V BurstRAMs. The following table lists control pins on the MCM69P618 that can be tied off to either 3.3 V or ground in order to satisfy the migration to this 3.3 V RAM.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

5 V Device Numbers	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
MCM67C618	—	—	—	L	H
MCM67J618	—	—	—	—	H
MCM67N618	—	—	—	L	L

NOTE: If no tie value is given, then the pin should be used as intended on the 5 V device.

NON–BURST SYNCHRONOUS OPERATION

Although this BurstRAM has been designed for 68K–, PowerPC–, 486–, i960, and Pentium – based systems, these SRAMs can be used in other high speed L2 cache or memory applications that do not require the burst address feature. Most L2 caches designed with a synchronous interface can make use of the MCM69P618. The burst counter feature of the BurstRAM can be disabled, and the SRAM can be configured to act upon a continuous stream of addresses. See Figure 2.

CONTROL PIN TIE VALUES ($H \geq V_{IH}$, $L \leq V_{IL}$)

Non–Burst	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{SE1}$	$\overline{LBO}$
Sync Non–Burst, Pipelined SRAM	H	L	H	L	X

NOTE: Although X is specified in the table as a don't care, the pin must be tied either high or low.

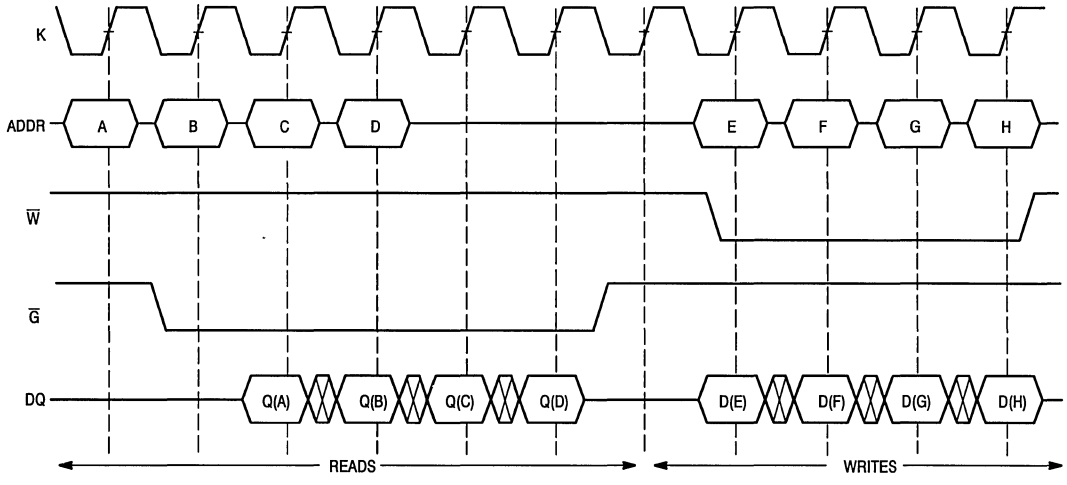
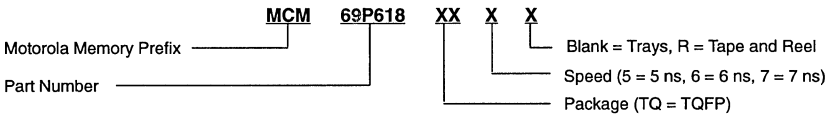


Figure 2. Configured as Non–Burst Synchronous SRAM (Register/Register Mode)

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM69P618TQ5 MCM69P618TQ6 MCM69P618TQ7
MCM69P618TQ5R MCM69P618TQ6R MCM69P618TQ7R

5

PowerPC Processor Applications

Pentium Applications

486 Processor Applications

R4000 Family

Networking and Buffer Applications

Fast SRAM Modules

6

6

MCM32A32
MCM32A64

128KB and 256KB Secondary Cache Fast Static RAM Modules

With Tag for 486 Processor Based Systems

The MCM32A32 and MCM32A64 are two products in Motorola's asynchronous secondary cache module family for the 486 processor. The modules are configured with 32–bit data, 8–bit tag, and an altered bit for writeback caches. The family supports all cache sizes of the 486 processor. They are offered in 33 and 50 MHz versions.

The 32A32 is a 128KB single bank cache of 32K x 32. The tag is 8K x 8, and the altered bit is 8K x 1.

The 32A64 is a 256KB double bank cache of 64K x 32. The tag is 16K x 8 and the altered bit is 16K x 1. The cache family is designed to interface with popular 486 chipsets with on–board cache controllers.

Cache upgrades are seamless, eliminating the need for motherboard jumpers.

PD0, 1, 2 are reserved for density identification:

MCM32A32: PD0 = gnd, PD1 = gnd, PD2 = open
MCM32A64: PD0 = open, PD1 = open, PD2 = gnd

- 64 Position Dual Readout SIMM for Circuit Density
- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times/Cycle Times: 15 ns/50 MHz, 20 ns/33 MHz
- Cache Byte Write, Byte Chip Enable, Bank Output Enable
- Tag Write Enable, Altered Write Enable, Tag/Altered Chip Enable
- Decoupling Capacitors Are Used For Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes

REV 1
5/95

PIN ASSIGNMENT
64 POSITION DUAL READOUT
128 PIN SIMM
TOP VIEW

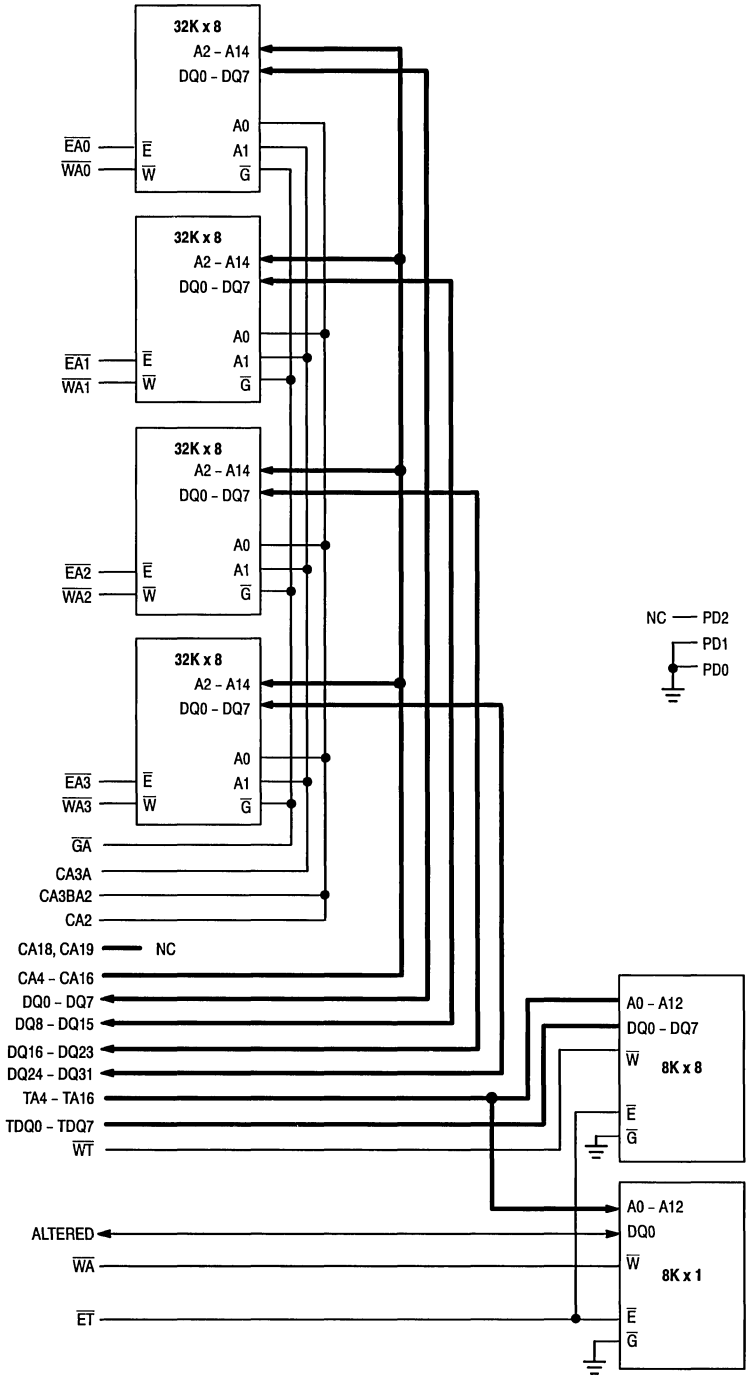
PD0	1	65	PD1
PD2	2	66	V_{SS}
DQ0	3	67	DQ1
DQ2	4	68	DQ3
DQ4	5	69	V_{CC}
DQ6	6	70	DQ5
DQ8	7	71	DQ7
V_{SS}	8	72	DQ9
DQ10	9	73	DQ11
DQ12	10	74	DQ13
DQ14	11	75	DQ15
DQ16	12	76	DQ17
DQ18	13	77	DQ19
DQ20	14	78	DQ21
V_{SS}	15	79	V_{SS}
DQ22	16	80	DQ23
DQ24	17	81	DQ25
V_{CC}	18	82	V_{CC}
DQ26	19	83	DQ27
DQ28	20	84	DQ29
DQ30	21	85	DQ31
NC	22	86	NC
NC	23	87	NC
V_{SS}	24	88	V_{SS}
$\overline{EA0}$	25	89	$\overline{EB0}$
$\overline{EA1}$	26	90	$\overline{EB1}$
$\overline{EA2}$	27	91	V_{CC}
$\overline{EA3}$	28	92	$\overline{EB2}$
V_{SS}	29	93	$\overline{EB3}$
$\overline{GA}$	30	94	$\overline{GB}$
$\overline{WA0}$	31	95	$\overline{WB0}$
$\overline{WA1}$	32	96	$\overline{WB1}$
$\overline{WA2}$	33	97	$\overline{WB2}$
$\overline{WA3}$	34	98	$\overline{WB3}$
$\overline{WT}$	35	99	$\overline{WA}$
$\overline{ET}$	36	100	V_{CC}
NC	37	101	NC
NC	38	102	NC
CA3A	39	103	CA3BA2
CA2	40	104	CA3B
V_{SS}	41	105	V_{SS}
CA4	42	106	CA5
CA6	43	107	CA7
CA8	44	108	CA9
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	CA17
CA18	49	113	CA19
V_{SS}	50	114	V_{SS}
TA4	51	115	TA5
TA6	52	116	TA7
TA8	53	117	TA9
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	TA17
TA18	58	122	TA19
V_{SS}	59	123	V_{SS}
TDQ0	60	124	TDQ1
TDQ2	61	125	TDQ3
TDQ4	62	126	TDQ5
TDQ6	63	127	TDQ7
ALT	64	128	V_{CC}

PIN NAMES

CA2 – CA19	Cache Address Inputs
$\overline{WA0}$ – $\overline{WA3}$; $\overline{WB0}$ – $\overline{WB3}$	Byte Write Enable
$\overline{EA0}$ – $\overline{EA3}$; $\overline{EB0}$ – $\overline{EB3}$	Cache Chip Enable
$\overline{GA}$, $\overline{GB}$	Bank Output Enable
DQ0 – DQ31	Cache Data Input/Output
TA4 – TA19	Tag Address Inputs
$\overline{WT}$	Tag Write Enable
$\overline{WA}$	Altered Write Enable
$\overline{ET}$	Tag/Altered Chip Enable
TDQ0 – TDQ7	Tag Data Input/Output
ALT	Altered Input/Output
PD0 – PD2	Presence Detect
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

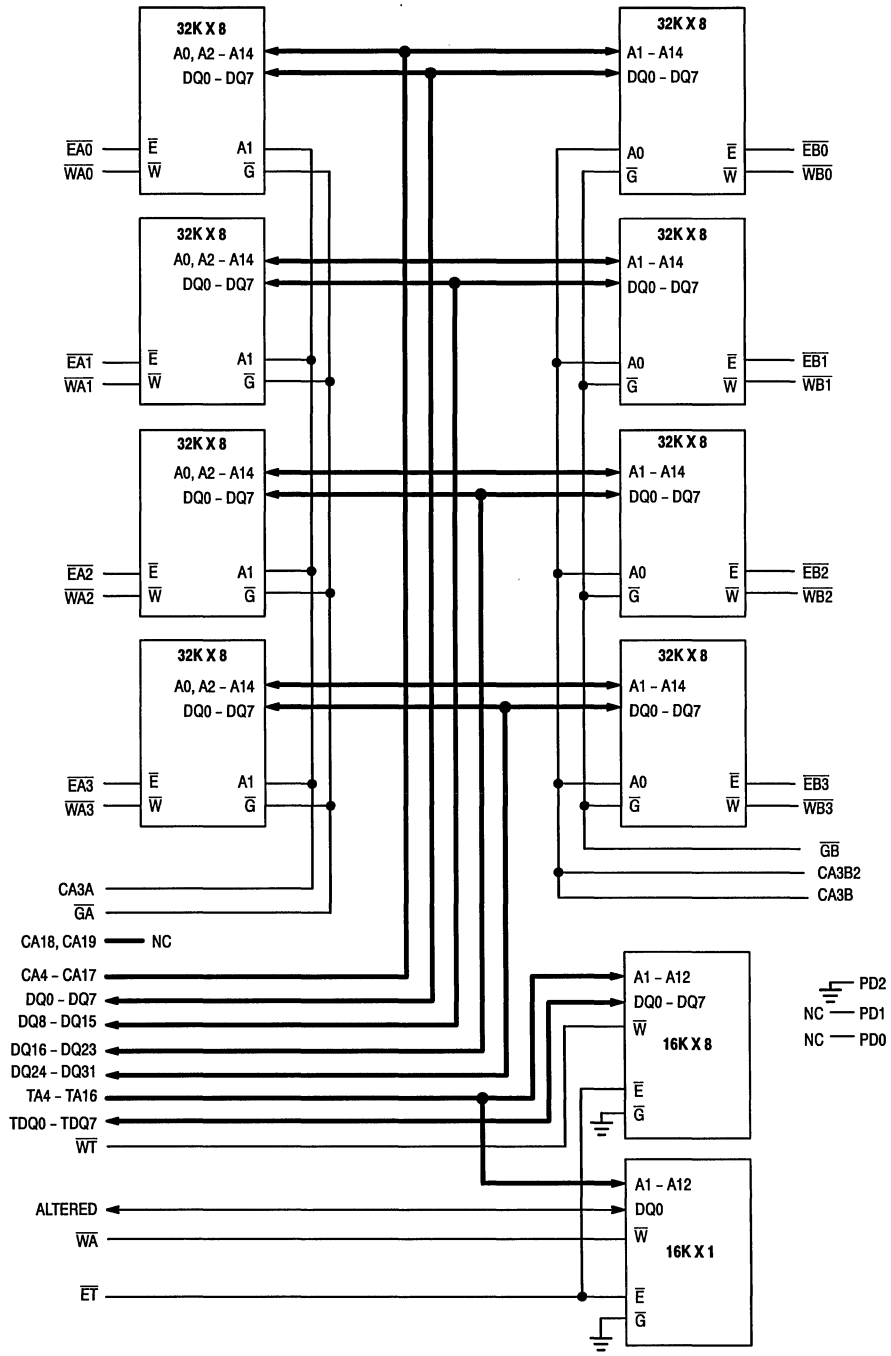
6

128KB BLOCK DIAGRAM



6

256KB BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

NOTE: $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	11.0	W
Ternperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 10	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 10	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	32A32 33 MHz	32A32 50 MHz	32A64 33 MHz	32A64 50 MHz	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	840	920	1530	1680	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	250	280	465	520	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	110	110	190	190	mA

6

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Cache Address Input Capacitance	C_{in}	48	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF
Tag Address Input Capacitance	C_{in}	18	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	33 MHz		50 MHz		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	ns	
Tag Access Time	t_{AVTV}	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	ns	4
Output Enable Access Time	t_{GLQV}	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	ns	5,6,7
Enable Low to Output Active	t_{ELQX}	4	—	4	—	ns	5,6,7
Enable High to Output High–Z	t_{EHQZ}	0	8	0	9	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	5,6,7
Output Enable High to Output High–Z	t_{GHQZ}	0	7	0	8	ns	5,6,7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E}$ = $\overline{E}$xx, $\overline{ET}$; $\overline{W}$ = $\overline{W}$xx, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

6

AC TEST LOADS

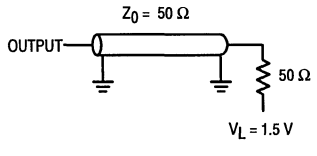


Figure 1A

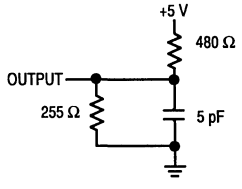
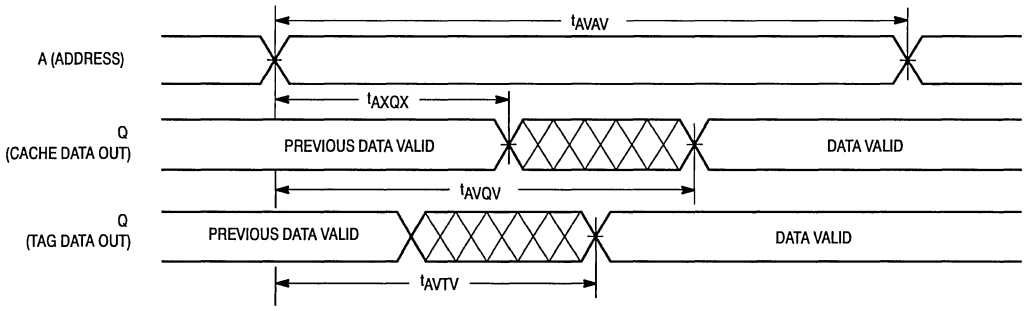


Figure 1B

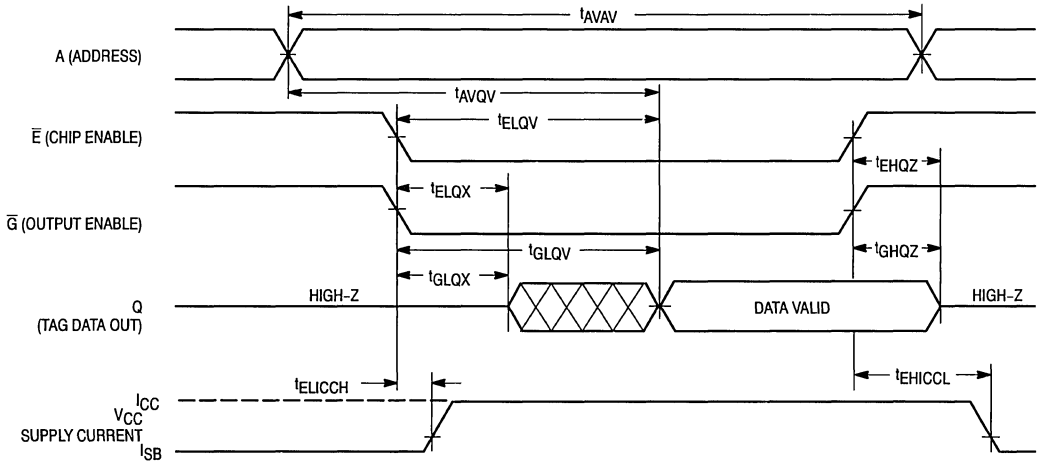
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)



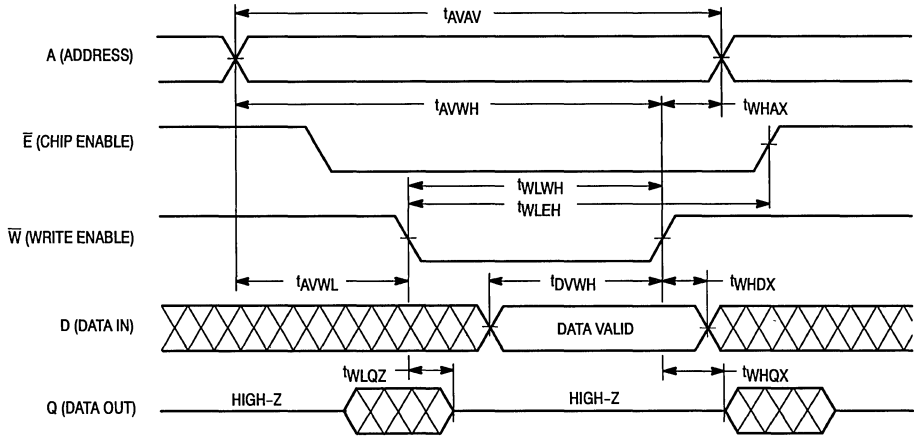
6

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	50 MHz		33 MHz		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	10	—	15	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	0	8	ns	6,7,8
Write High to Output Active	t_{WHQX}	0	—	0	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

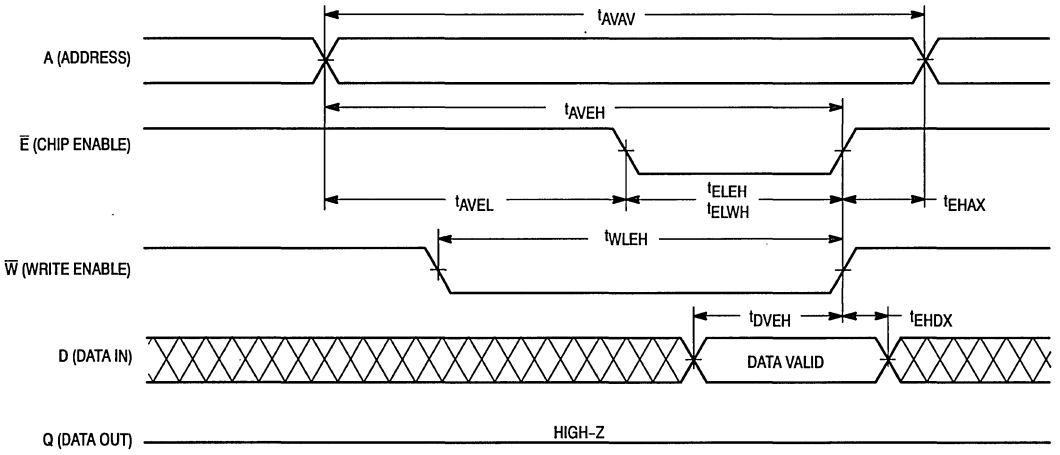


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

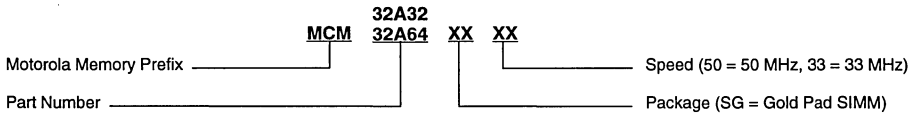
Parameter	Symbol	50 MHz		33 MHz		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	ns	
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	10	—	12	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32A32SG50 MCM32A32SG33
MCM32A64SG50 MCM32A64SG33

MCM321024

Advance Information

1M x 32 Bit Fast Static RAM Module

The MCM321024 is an 32M bit static random access memory module organized as 1,048,576 words of 32 bits. The module is a 72–lead single in–line memory module (SIMM) consisting of eight MCM6249 fast static RAMs packaged in 32–lead SOJ packages and mounted on a printed circuit board along with sixteen decoupling capacitors.

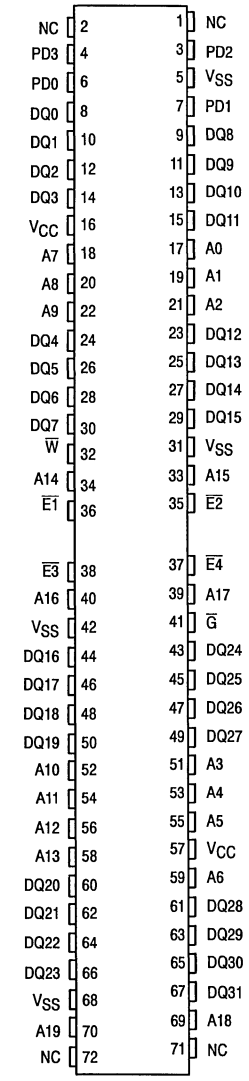
The MCM6249 is a high–performance CMOS fast static RAM organized as 1,048,576 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM321024 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

PD0 – PD3 are reserved for density identification. PD0 and PD2 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 1520/1400 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Six–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

PIN ASSIGNMENT
TOP VIEW
72 LEAD SIMM — CASE TBD



PIN NAMES	
A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, V_{SS} must be connected to ground.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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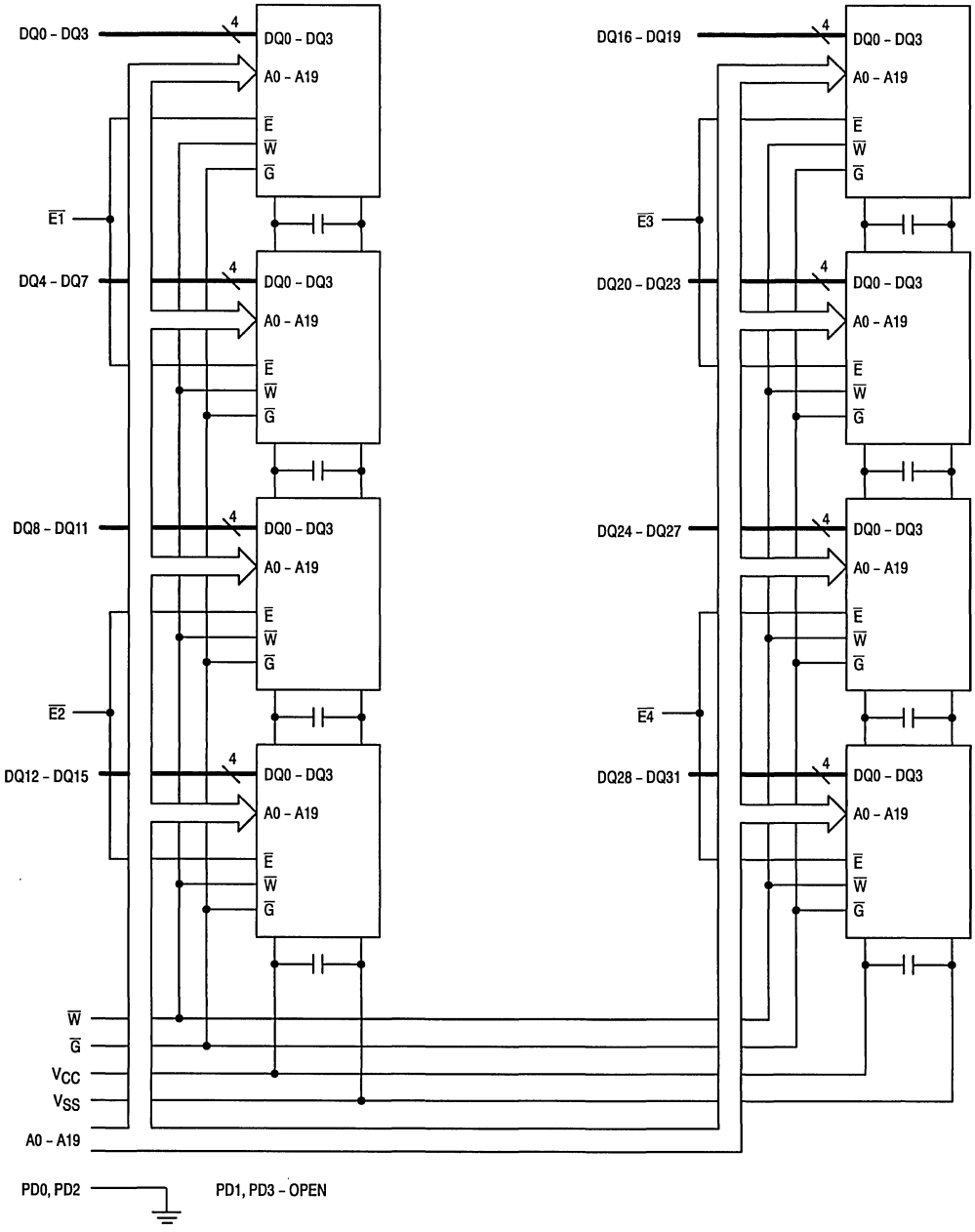
FUNCTIONAL BLOCK DIAGRAM
1M x 32 MEMORY MODULE



6

TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	8.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

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DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 8	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min) MCM321024–20: t_{AVAV} = 20 ns MCM321024–25: t_{AVAV} = 25 ns	I_{CCA}	— —	1440 1320	1520 1400	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)	I_{SB1}	—	400	480	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	80	120	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31, $\overline{W}$, $\overline{G}$, and $\overline{E1}$ – $\overline{E4}$) $\overline{E1}$ – $\overline{E4}$ $\overline{W}$, $\overline{G}$	C_{in}	32 10 40	48 14 64	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	7	—	9	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}). See Read Cycle 1.

AC TEST LOADS

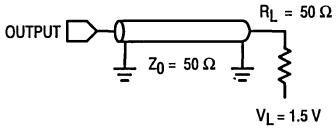

Figure 1A

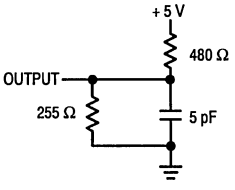

Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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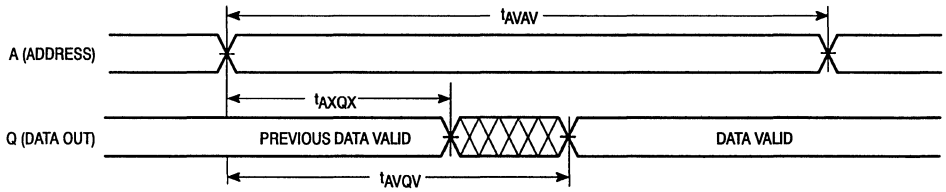
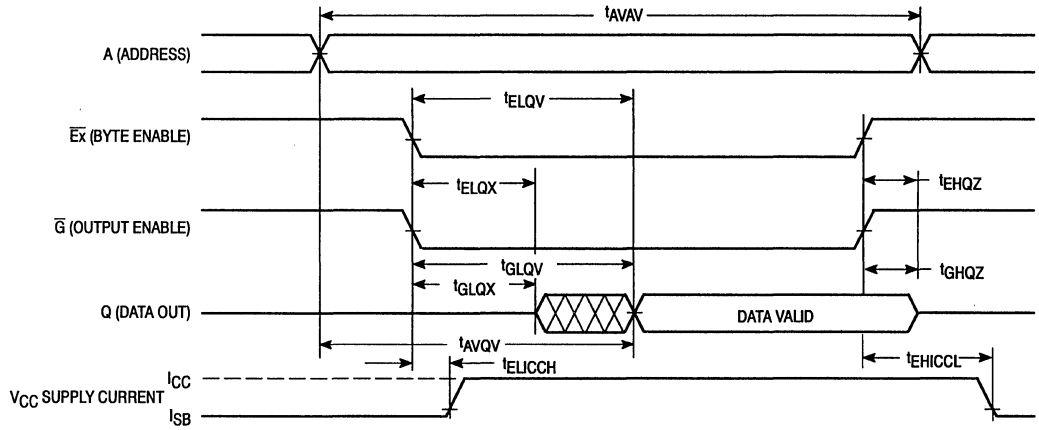
READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

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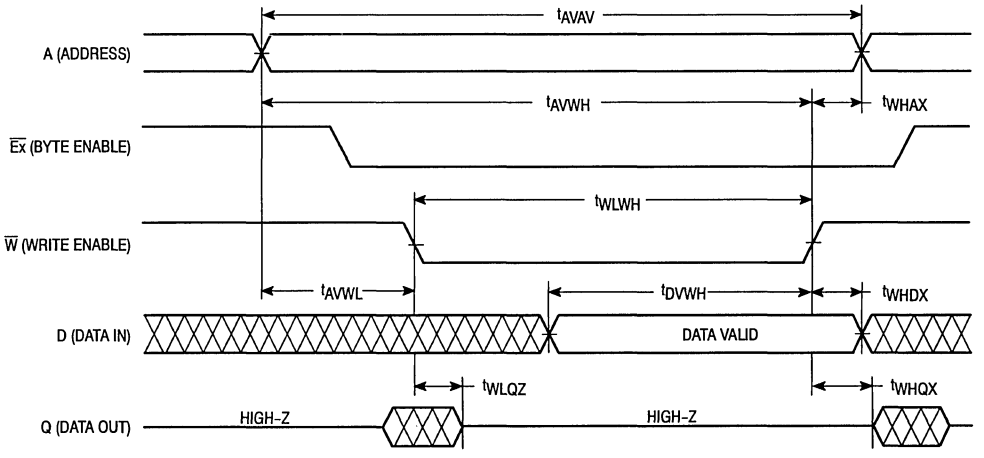
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

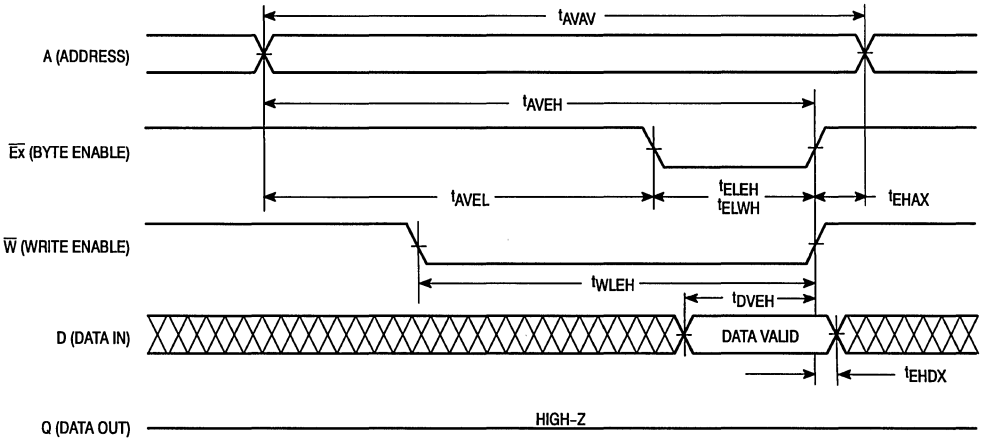


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM321024–20		MCM321024–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	15	—	17	—	ns	4,5
Enable to End of Write	t_{ELWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



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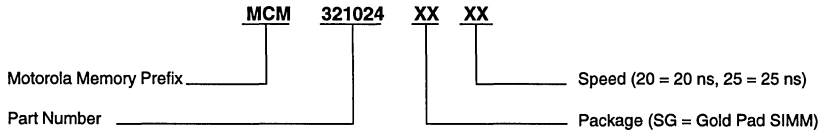
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM321024SG20 MCM321024SG25

MCM32128A

128K x 32 Bit Fast Static RAM Module

The MCM32128A is a 4M bit static random access memory module organized as 131,072 words of 32 bits. The module is offered in a 64–lead single in–line memory module (SIMM). Four MCM6226 fast static RAMs, packaged in 32–lead SOJ packages are mounted on a printed circuit board along with four decoupling capacitors.

The MCM6226 is a high–performance CMOS fast static RAM organized as 131,072 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

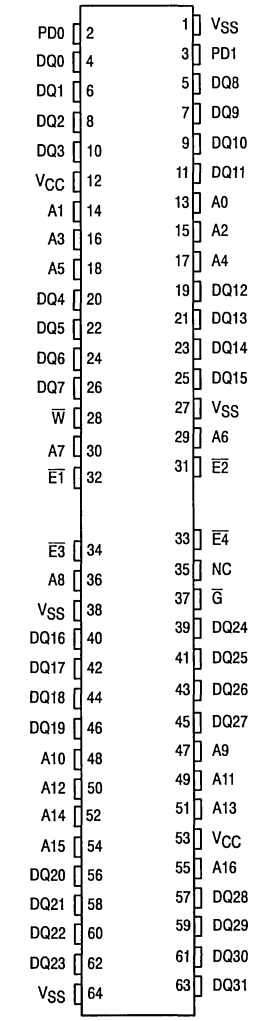
The MCM32128A is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 520/480/460 mA Maximum, Active AC
- High Board Density ZIP or SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte
- High Quality Four–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

PIN NAMES	
A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
TOP VIEW
64-LEAD SIMM – CASE TBD



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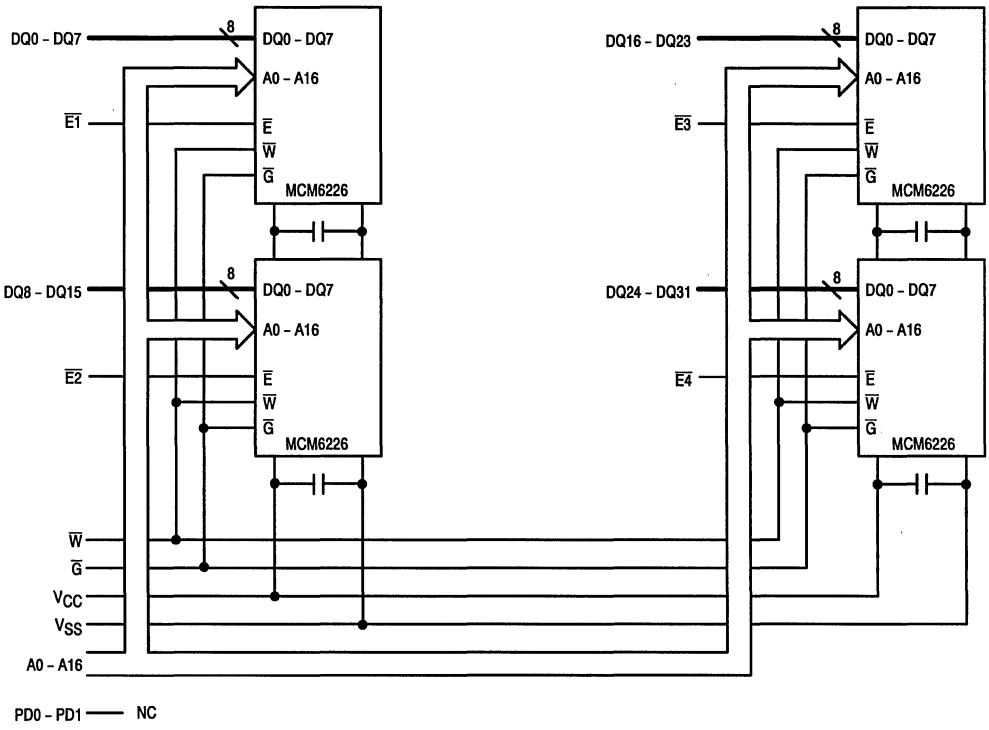
FUNCTIONAL BLOCK DIAGRAM

128K x 32 MEMORY MODULE



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TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	4.4	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 4	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 4	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min)	MCM32128A–15: t_{AVAV} = 15 ns MCM32128A–20: t_{AVAV} = 20 ns MCM32128A–25: t_{AVAV} = 25 ns	I_{CCA}	— — —	520 480 460	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)		I_{SB1}	—	160	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)		I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$) ($\overline{E1}$ – $\overline{E4}$)	C_{in} C_{in}	24 14	pF pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	9	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32128A–15		MCM32128A–20		MCM32128A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	8	—	9	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	8	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

6

AC TEST LOADS

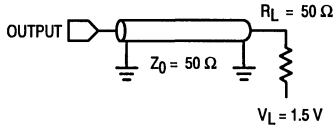


Figure 1A

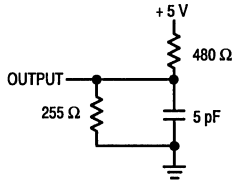
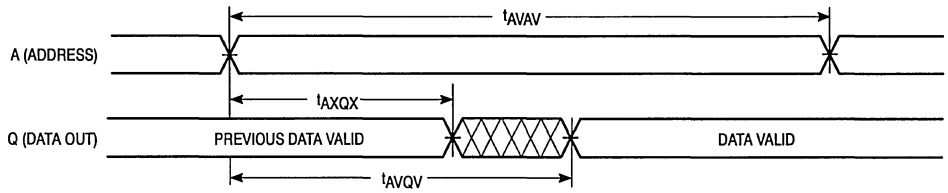


Figure 1B

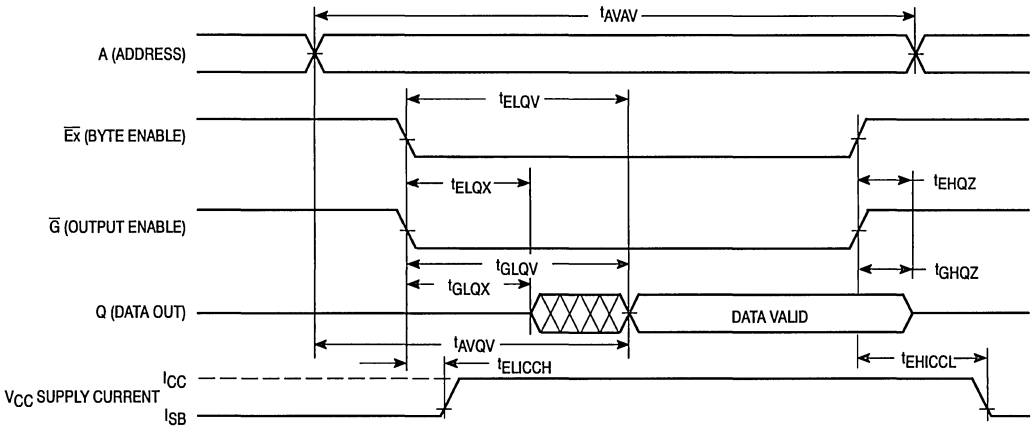
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

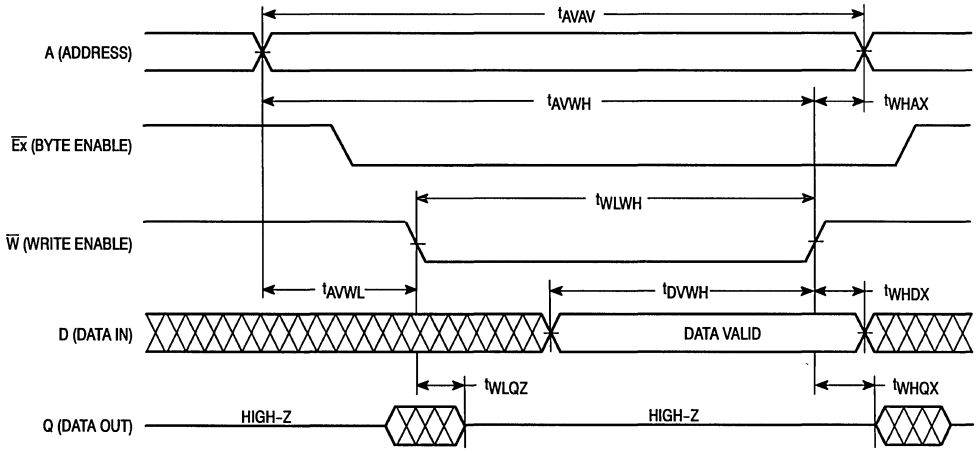
6

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32128A–15		MCM32128A–20		MCM32128A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	8	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

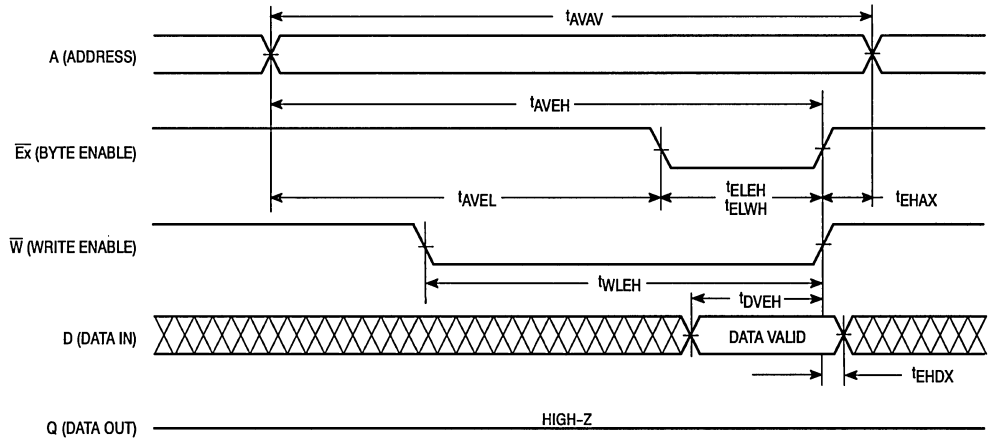


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

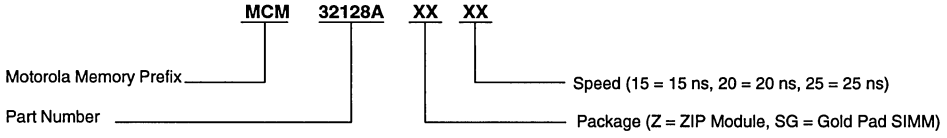
Parameter	Symbol	MCM32128A–15		MCM32128A–20		MCM32128A–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	10	—	12	—	15	—	ns	4,5
Enable to End of Write	t_{ELWH}	10	—	12	—	15	—	ns	
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32128AZ15 MCM32128AZ20 MCM32128AZ25
MCM32128ASG15 MCM32128ASG20 MCM32128ASG25

MCM32257B

256K x 32 Bit Fast Static RAM Module

The MCM32257B is an 8M bit static random access memory module organized as 262,144 words of 32 bits. The module is a 64–lead zig–zag in–line package (ZIP) of eight MCM6229 fast static RAMs packaged in 28–lead SOJ packages and mounted on a printed circuit board along with eight decoupling capacitors.

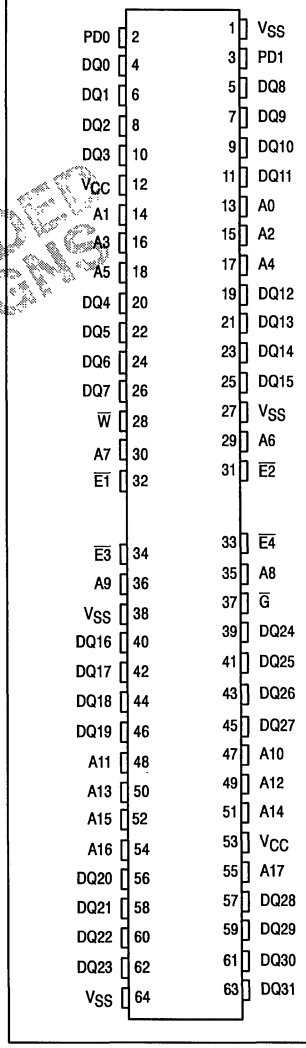
The MCM6229 is a high–performance CMOS fast static RAM organized as 262,144 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32257B is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1} - \overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

PD0 and PD1 are reserved for density identification. PD0 and PD1 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 15/20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 960/880/840 mA Maximum, Active AC
- High Board Density ZIP Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Four–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

PIN ASSIGNMENT
TOP VIEW
64 LEAD ZIP — CASE 871–01



PIN NAMES	
A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1} - \overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density

For proper operation of the device, V_{SS} must be connected to ground.

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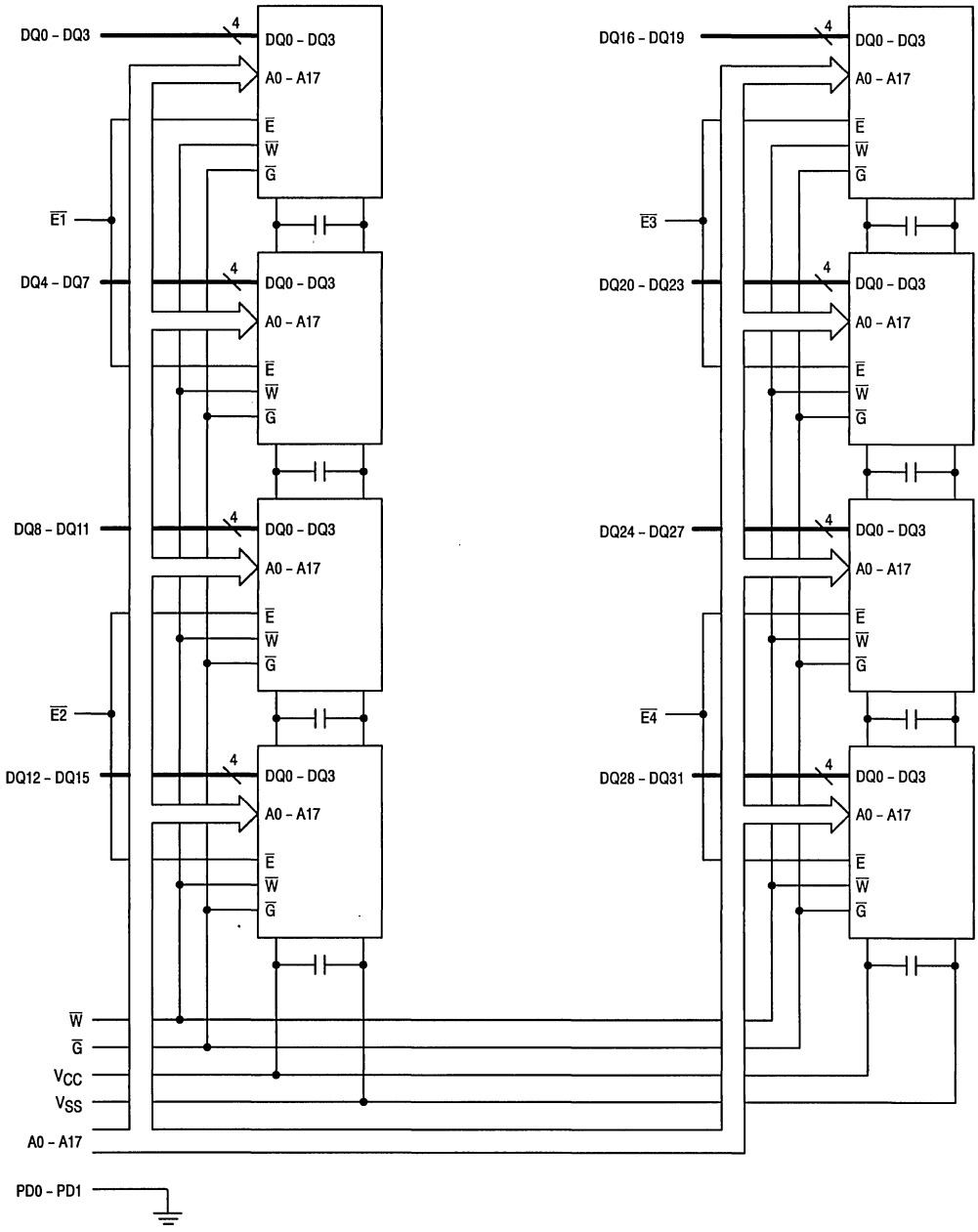
5/95

FUNCTIONAL BLOCK DIAGRAM
256K x 32 MEMORY MODULE



6

TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	8.8	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

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DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 8	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min)	MCM32257B–15: t_{AVAV} = 15 ns MCM32257B–20: t_{AVAV} = 20 ns MCM32257B–25: t_{AVAV} = 25 ns	I_{CCA}	— — —	960 880 840	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)		I_{SB1}	—	320	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)		I_{SB2}	—	40	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$) ($\overline{E1}$ – $\overline{E4}$)	C_{in}	48 14	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32257B–15		MCM32257B–20		MCM32257B–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	15	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	8	—	9	—	10	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	8	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	8	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}). See Read Cycle 1.

AC TEST LOADS

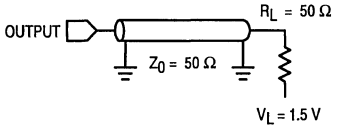


Figure 1A

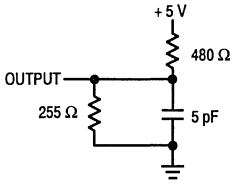


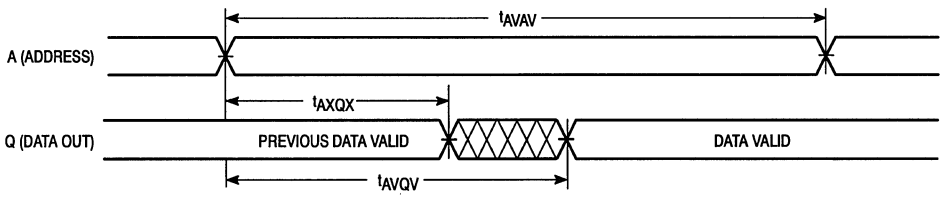
Figure 1B

TIMING LIMITS

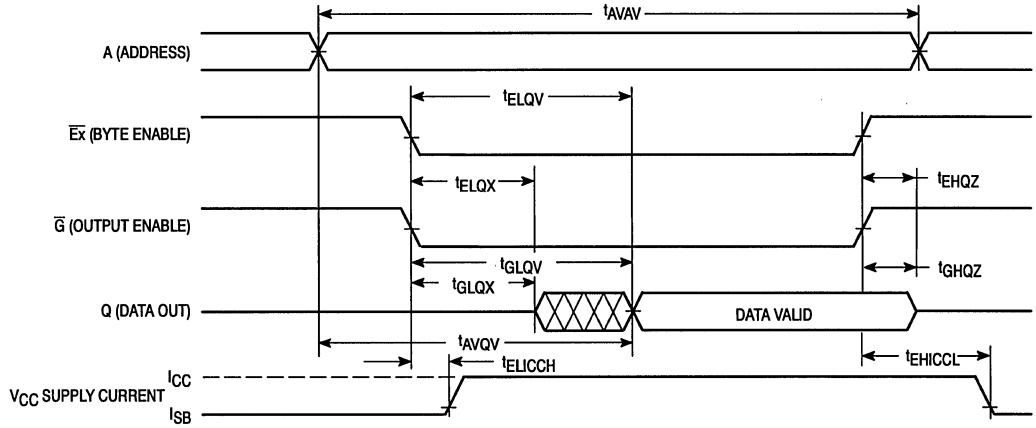
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

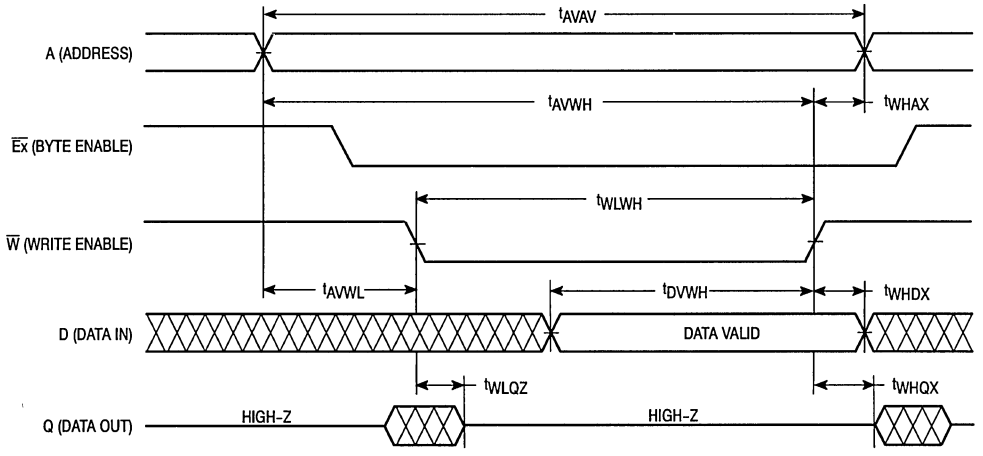
6

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32257B–15		MCM32257B–20		MCM32257B–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	8	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

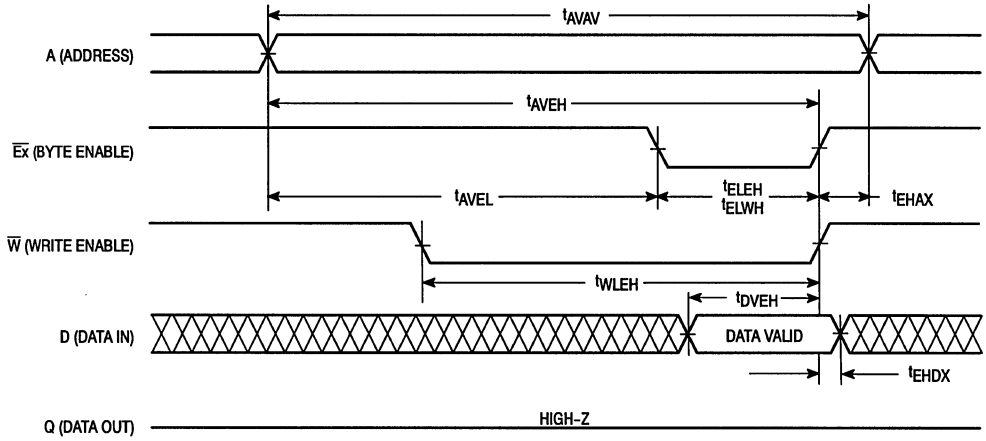


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32257B–15		MCM32257B–20		MCM32257B–25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	10	—	12	—	15	—	ns	4,5
Enable to End of Write	t_{ELWH}	10	—	12	—	15	—	ns	
Write Pulse Width	t_{WLEH}	10	—	12	—	15	—	ns	
Data Valid to End of Write	t_{DVEH}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



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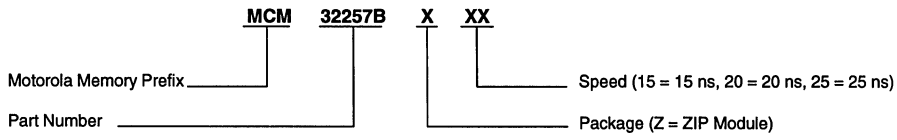
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32257BZ15 MCM32257BZ20 MCM32257BZ25

MCM32515

Advance Information

512K x 32 Bit Fast Static RAM Module

The MCM32515 is a 16M bit static random access memory module organized as 524,288 words of 32 bits. The module is offered in a 72–lead single in–line memory module (SIMM). Four MCM6246 fast static RAMs, packaged in 36–lead SOJ packages are mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6246 is a high–performance CMOS fast static RAM organized as 524,288 words of 8 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32515 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20/25 ns
- Three–State Outputs
- Fully TTL Compatible
- JEDEC Standard Pinout
- Power Requirement: 800/740 mA Maximum, Active AC
- High Board Density SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte
- High Quality Six–Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State–of–the–Art Fast Static RAMs

PIN NAMES	
A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD3	Package Density
NC	No Connect

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
TOP VIEW
72-LEAD SIMM – CASE TBD

NC	2	1	NC
PD3	4	3	PD2
PD0	6	5	V_{SS}
DQ0	8	7	PD1
DQ1	10	9	DQ8
DQ2	12	11	DQ9
DQ3	14	13	DQ10
V_{CC}	16	15	DQ11
A7	18	17	A0
A8	20	19	A1
A9	22	21	A2
DQ4	24	23	DQ12
DQ5	26	25	DQ13
DQ6	28	27	DQ14
DQ7	30	29	DQ15
$\overline{W}$	32	31	V_{SS}
A14	34	33	A15
$\overline{E1}$	36	35	$\overline{E2}$
$\overline{E3}$	38	37	$\overline{E4}$
A16	40	39	A17
V_{SS}	42	41	$\overline{G}$
DQ16	44	43	DQ24
DQ17	46	45	DQ25
DQ18	48	47	DQ26
DQ19	50	49	DQ27
A10	52	51	A3
A11	54	53	A4
A12	56	55	A5
A13	58	57	V_{CC}
DQ20	60	59	A6
DQ21	62	61	DQ28
DQ22	64	63	DQ29
DQ23	66	65	DQ30
V_{SS}	68	67	DQ31
NC	70	69	A18
NC	72	71	NC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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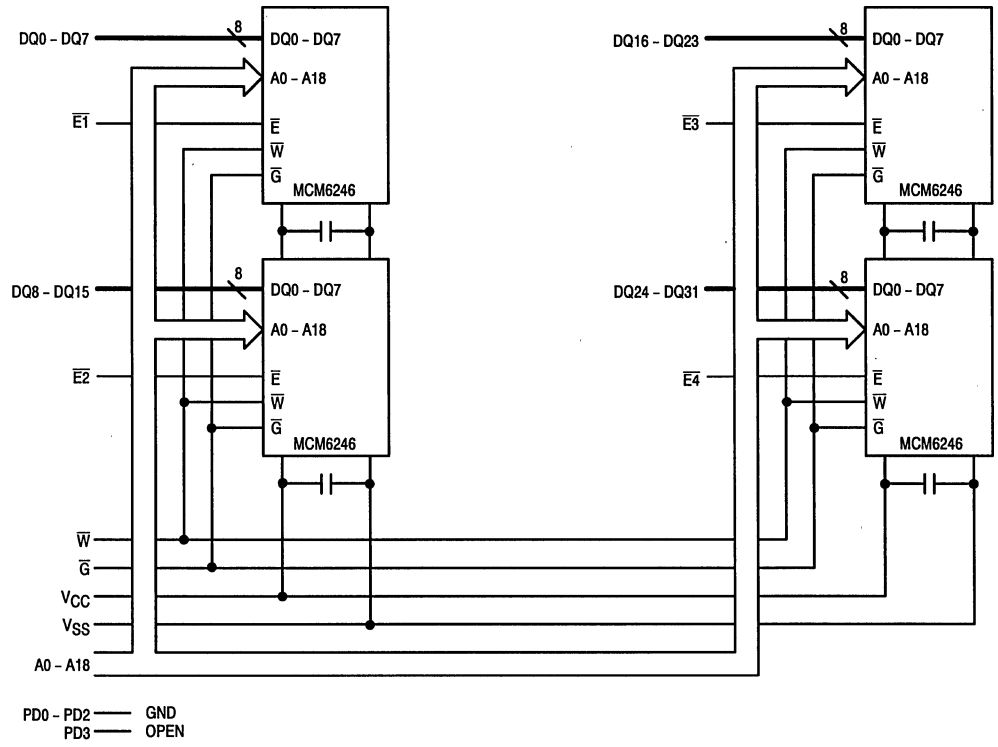
FUNCTIONAL BLOCK DIAGRAM

512K x 32 MEMORY MODULE



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TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High–Z	—
L	H	H	Read	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	4.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 4	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 4	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min) MCM32515–20: t_{AVAV} = 20 ns MCM32515–25: t_{AVAV} = 25 ns	I_{CCA}	— —	760 700	800 740	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)	I_{SB1}	—	220	240	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	40	60	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31, $\overline{W}$, $\overline{G}$, and $\overline{E1}$ – $\overline{E4}$) ($\overline{E1}$ – $\overline{E4}$) ($\overline{W}$, $\overline{G}$)	C_{in}	16 10 20	24 14 32	pF
Input/Output Capacitance	(DQ0 – DQ31)	C_{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM32515–20		MCM32515–25		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	—	20	—	25	ns	
Output Enable Access Time	t_{GLQV}	—	7	—	9	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4,5,6
Enable High to Output High–Z	t_{EHQZ}	0	9	0	10	ns	4,5,6
Output Enable High to Output High–Z	t_{GHQZ}	0	9	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{E}$xs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

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AC TEST LOADS

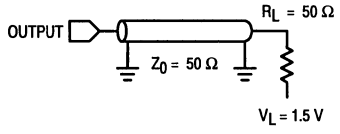


Figure 1A

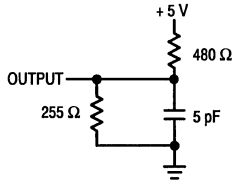
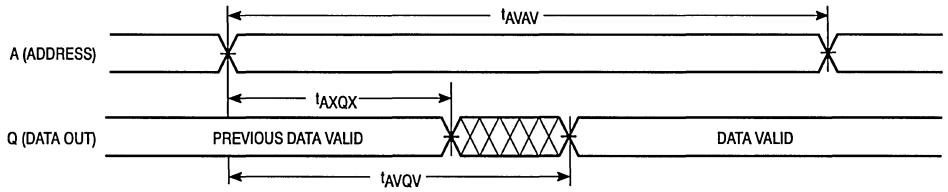


Figure 1B

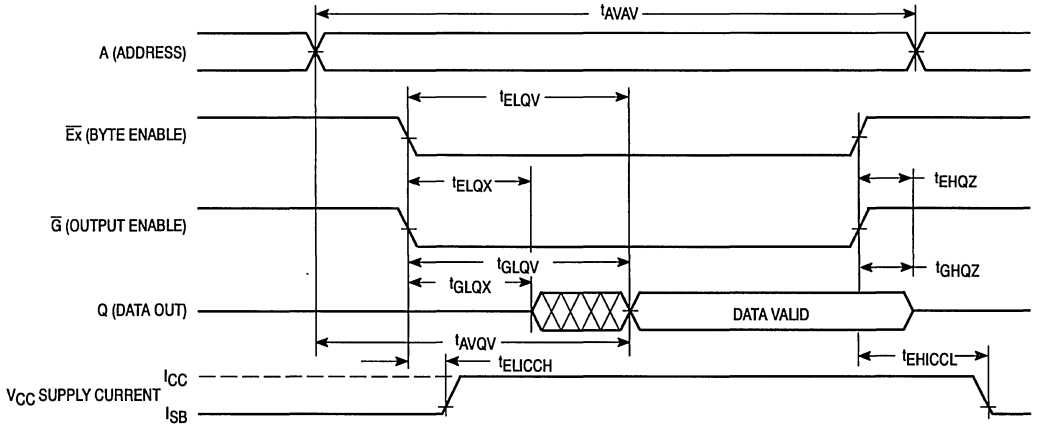
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

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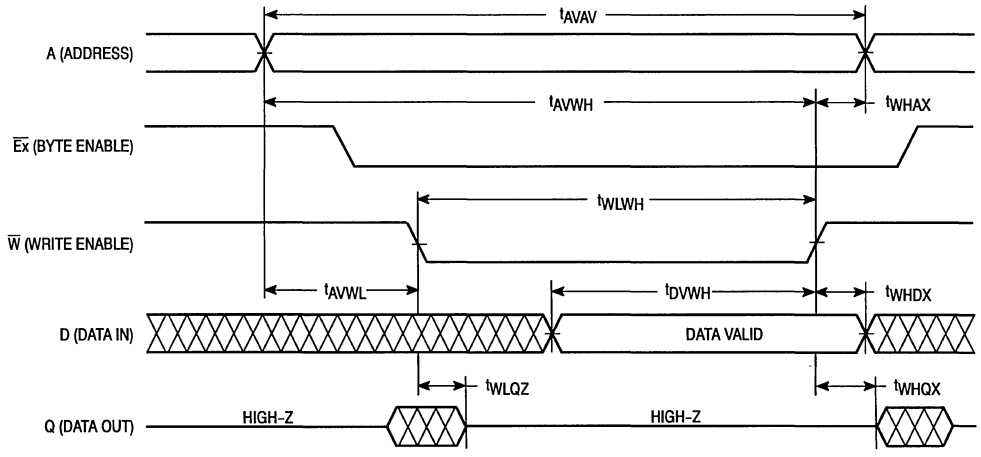
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32515–20		MCM32515–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVWH}	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	9	0	10	ns	4,5,6
Write High to Output Active	t_{WHQX}	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

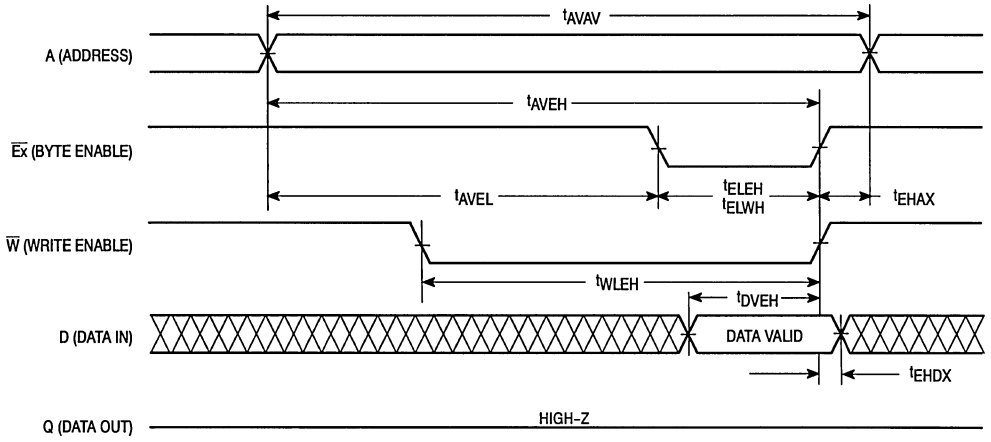


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM32515–20		MCM32515–25		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	15	—	17	—	ns	
Enable to End of Write	t_{ELEH}	15	—	17	—	ns	4,5
Enable to End of Write	t_{ELWH}	15	—	17	—	ns	
Write Pulse Width	t_{WLEH}	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



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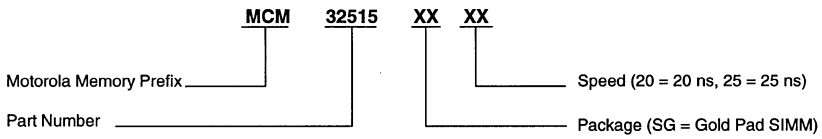
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32515SG20 MCM32515SG25

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MCM4464 Series

1MB R4000 Secondary Cache Fast Static RAM Module Set

Four MCM4464 modules comprise a full 1 MB of secondary cache for the R4000 processor. Each module contains nine MCM6709J fast static RAMs for a cache data size of 64K x 36. The tag portion, dependent on word line size, contains either two MCM6709J or one MCM6706J fast static RAMs. All input signals, except A0 and $\overline{WE}$ are buffered using 74FBT2827 drivers with series 25 Ω resistors.

The MCM6709J and MCM6706J are fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for internal clocks or timing strobes.

All 1MB R4000 supported secondary cache options are available.

- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Access Time: 12/15/17 ns
- Zero Wait–State Operation
- Unified or Split Seconday Cache Modules are Available (See Ordering Information for Details)
- Word Line Sizes of 4, 8, 16, and 32 are Available (See Ordering Information for Details)
- The Pin Compatible MCM44256 Series is also Available to Support a Full 4MB R4000 Secondary Cache.
- Decoupling Capacitors are Used for Each Fast Static RAM and Buffer, Along with Bulk Capacitance for Maximum Noise Immunity
- High Quality Multi–Layer FR4 PWB with Separate Power and Ground Planes

PIN NAMES	
A0 – A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{DCS}$	Data Enable
$\overline{TCS}$	Tag Enable
$\overline{OE}$	Output Enable
DQ0 – DQ35	Data Input / Output
TDQ0 – TDQ7	TAG Data Input / Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
80 LEAD SIMM — TOP VIEW

V_{CC}	2	1	V_{SS}
DQ1	4	3	DQ0
DQ3	6	5	DQ2
DQ5	8	7	DQ4
V_{SS}	10	9	DQ6
DQ8	12	11	DQ7
DQ10	14	13	DQ9
DQ12	16	15	DQ11
DQ14	18	17	DQ13
DQ15	20	19	V_{SS}
DQ17	22	21	DQ16
DQ19	24	23	DQ18
DQ21	26	25	DQ20
V_{SS}	28	27	DQ22
DQ23	30	29	V_{CC}
DQ25	32	31	DQ24
DQ27	34	33	DQ26
DQ29	36	35	DQ28
DQ30	38	37	V_{SS}
DQ32	40	39	DQ31
DQ34	42	41	DQ33
V_{SS}	44	43	DQ35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
V_{CC}	54	53	V_{SS}
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
V_{SS}	62	61	A11
A13	64	63	A12
A15	66*	65	A14
NC	68*	67	NC
TDQ0	70	69	$\overline{TCS}$
TDQ1	72	71	V_{SS}
TDQ3	74	73	TDQ2
TDQ5	76	75	TDQ4
TDQ7	78	77	TDQ6
V_{SS}	80	79	V_{CC}

NOTE: Pin assignment is for unified cache. For split cache option, Pin 68 becomes Address MSB (A15) and Pin 66 is NC.

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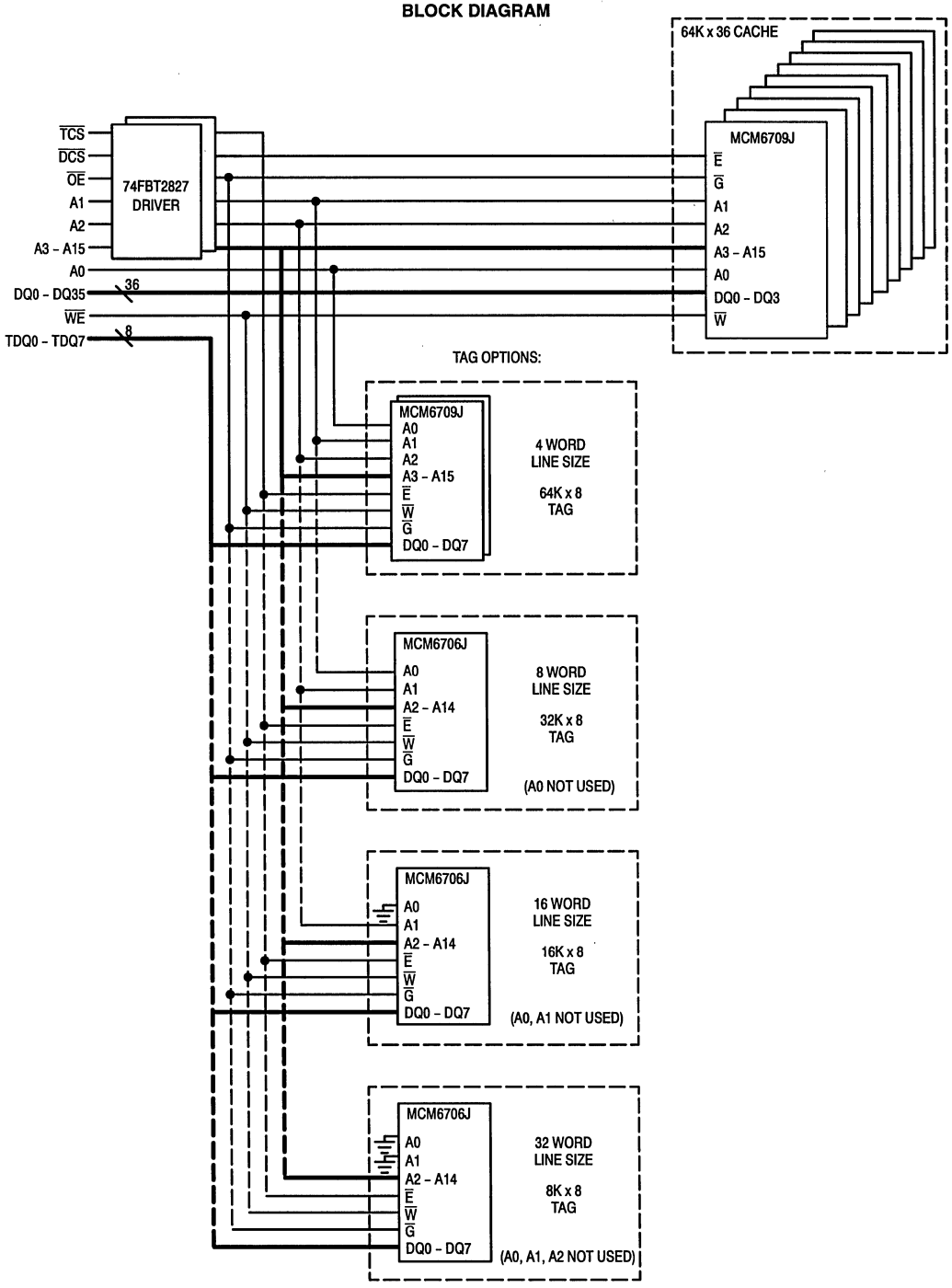
REV 1
8/94

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	10	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 25 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

These BiCMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at leat 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}				V
(DQ0 – 35, TDQ0 – 7, $\overline{WE}$, A0)		2.2	—	V_{CC} + 0.3 V*	
(A1 – A15, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)		2.0	—	V_{CC} + 0.3 V*	
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 10	µA
Output Leakage Current ($\overline{G}$, $\overline{xCS}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 10	µA
AC Supply Current ($\overline{G}$, $\overline{xCS}$ = V_{IL}, I_{out} = 0 mA)	I_{CCA}	—	—	1850	mA
Output Low Voltage (I_{OL} = + 8 mA)	V_{OL}	—	—	0.4	V
OUtput High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

Note: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (A0, $\overline{WE}$)	C_{in}	—	110	pF
Input Capacitance (A1 – A15, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)	C_{in}	—	10	pF
Input/Output Capacitance	C_{out}	—	10	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Access Time	t_{AVQV}	—	12	—	15	—	17	ns	
A0 Access Time	t_{A0QV}	—	10	—	12	—	14	ns	
Data/Tag Enable Access Time	t_{ELQV}	—	12	—	15	—	17	ns	
Output Enable Access Time	t_{GLQV}	—	9	—	10	—	11	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Hold from A0 Change	t_{A0XQX}	4	—	4	—	4	—	ns	
Data/Tag Enable Low to Output Active	t_{ELQX}	2	—	2	—	2	—	ns	3, 4
Data/Tag Enable High to Output High–Z	t_{EHQZ}	1	9	1	10	1	11	ns	3, 4
Output Enable Low to Output Active	t_{GLQX}	1	—	1	—	1	—	ns	3, 4
Output Enable High to Output High–Z	t_{GHQZ}	1	9	1	10	1	11	ns	3, 4

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

AC TEST LOADS

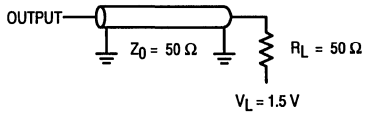


Figure 1A

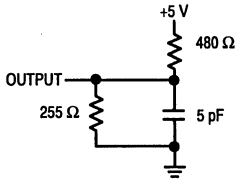
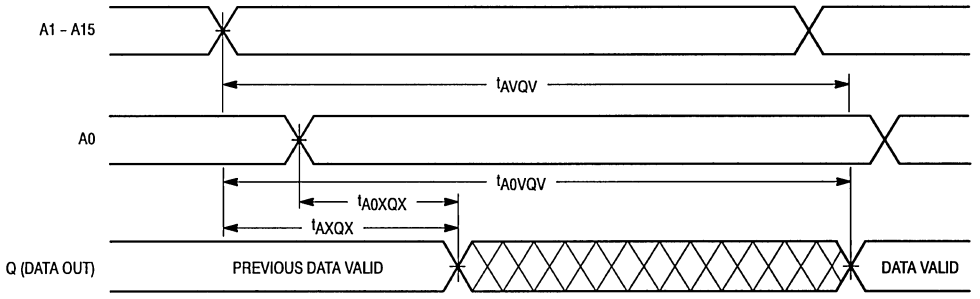


Figure 1B

TIMING LIMITS

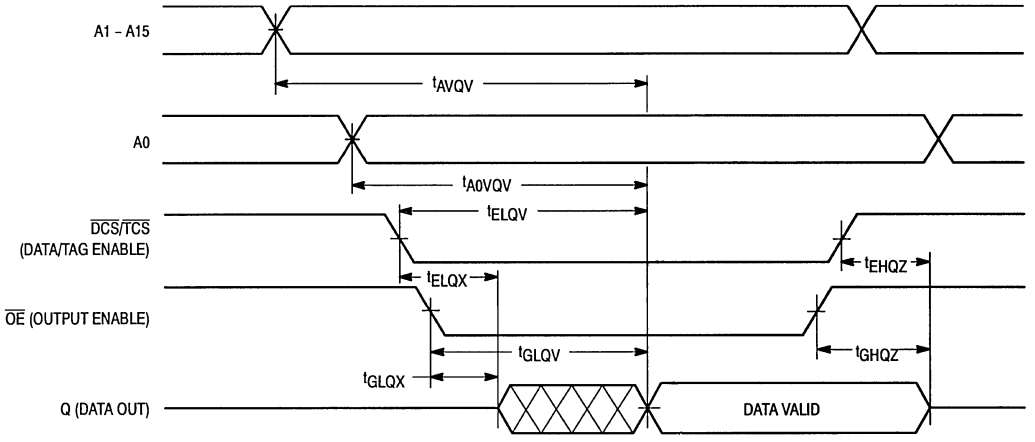
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Module is continuously selected ($\overline{DCS}$ or $\overline{TCS}$ = V_{IL}, $\overline{OE}$ = V_{IL}).

READ CYCLE 2 (See Note)



NOTE: Address valid prior to or coincident with $\overline{DCS}$ or $\overline{TCS}$ going low.

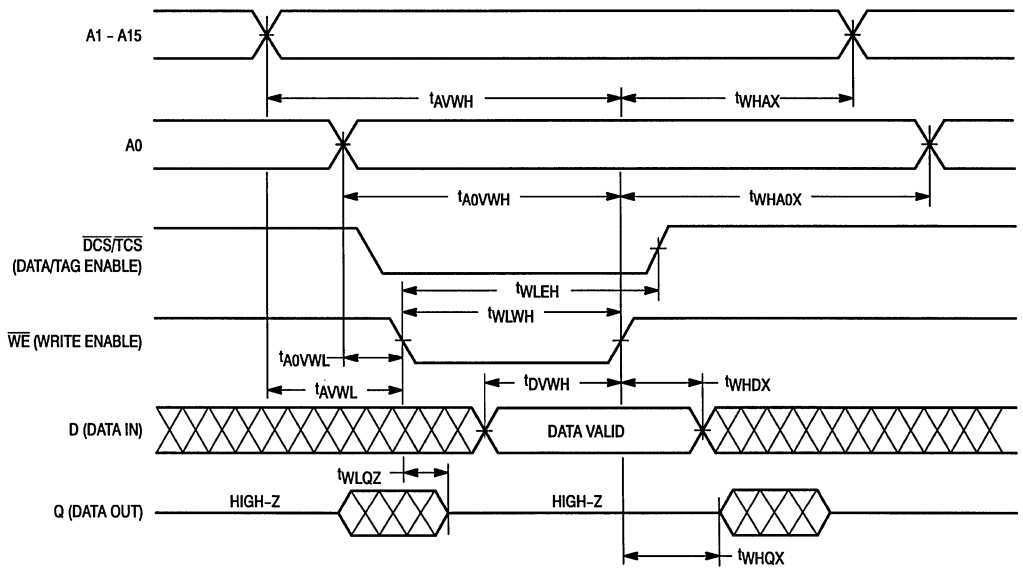
6

WRITE CYCLE 1 ($\overline{WE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVWL}	5	—	5	—	5	—	ns	
A0 Setup Time	t_{A0VWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VWH}	10	—	12	—	14	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	7	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	3, 4
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	3, 4
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	
Write Recovery Time – A0	t_{WHA0X}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1

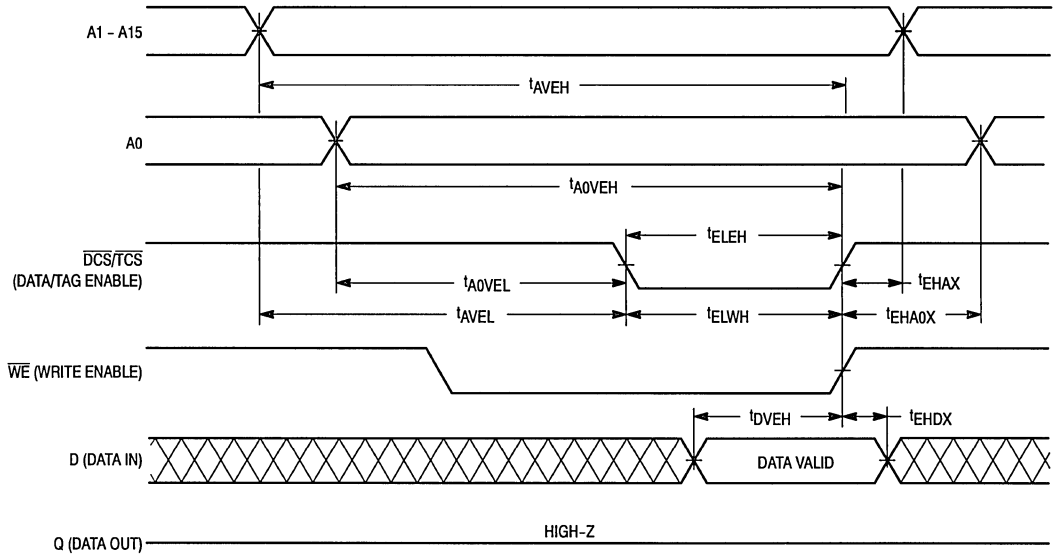


WRITE CYCLE 2 ($\overline{DCS}$ or $\overline{TCS}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VEH}	10	—	12	—	14	—	ns	
Data/Tag Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	5	—	5	—	5	—	ns	
Write Recovery Time	t_{EHAX}	5	—	5	—	5	—	ns	
Write Recovery Time – A0	t_{EHA0X}	5	—	5	—	5	—	ns	

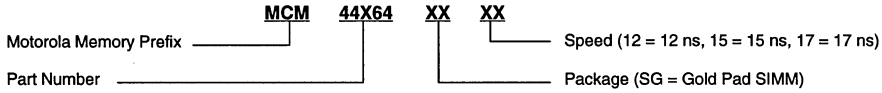
NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.

WRITE CYCLE 2



6

ORDERING INFORMATION
(Order by Full Part Number)



Part Number	Unified/Split	Word Line Size	TAG Depth
MCM44A64	Unified	4	64K
MCM44B64	Unified	8	32K
MCM44C64	Unified	16	16K
MCM44D64	Unified	32	8K
MCM44E64	Split	4	64K
MCM44F64	Split	8	32K
MCM44G64	Spllit	16	16K
MCM44H64	Split	32	8K

MCM44256 Series

4MB R4000 Secondary Cache Fast Static RAM Module Set

Four MCM44256 modules comprise a full 4 MB of secondary cache for the R4000 processor. Each module contains nine MCM6729WJ fast static RAMs for a cache data size of 256K x 36. The tag portion, dependent on word line size, contains either two MCM6729WJ or one MCM6726WJ fast static RAMs. All input signals, except A0 and $\overline{WE}$ are buffered using 74FBT2827 drivers with series 25 Ω resistors.

The MCM6729WJ and MCM6726WJ are fabricated using high–performance silicon–gate BiCMOS technology. Static design eliminates the need for internal clocks or timing strobes.

All 4MB R4000 supported secondary cache options are available.

- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Access Time: 12/15/17 ns
- Zero Wait–State Operation
- Unified or Split Seconday Cache is Supported
- Word Line Sizes of 4, 8, 16, and 32 are Available (See Ordering Information for Details)
- Decoupling Capacitors are Used for Each Fast Static RAM and Buffer, Along with Bulk Capacitance for Maximum Noise Immunity
- High Quality Multi–Layer FR4 PWB with Separate Power and Ground Planes

PIN ASSIGNMENT
80 LEAD SIMM — TOP VIEW

V_{CC}	2	1	V_{SS}
DQ1	4	3	DQ0
DQ3	6	5	DQ2
DQ5	8	7	DQ4
V_{SS}	10	9	DQ6
DQ8	12	11	DQ7
DQ10	14	13	DQ9
DQ12	16	15	DQ11
DQ14	18	17	DQ13
DQ15	20	19	V_{SS}
DQ17	22	21	DQ16
DQ19	24	23	DQ18
DQ21	26	25	DQ20
V_{SS}	28	27	DQ22
DQ23	30	29	V_{CC}
DQ25	32	31	DQ24
DQ27	34	33	DQ26
DQ29	36	35	DQ28
DQ30	38	37	V_{SS}
DQ32	40	39	DQ31
DQ34	42	41	DQ33
V_{SS}	44	43	DQ35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
V_{CC}	54	53	V_{SS}
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
V_{SS}	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
TDQ0	70	69	$\overline{TCS}$
TDQ1	72	71	V_{SS}
TDQ3	74	73	TDQ2
TDQ5	76	75	TDQ4
TDQ7	78	77	TDQ6
V_{SS}	80	79	V_{CC}

PIN NAMES

A0 – A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{DCS}$	Data Enable
$\overline{TCS}$	Tag Enable
$\overline{OE}$	Output Enable
DQ0 – DQ35	Data Input / Output
TDQ0 – TDQ7	TAG Data Input / Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

For proper operation of the device, V_{SS} must be connected to ground.

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REV 1
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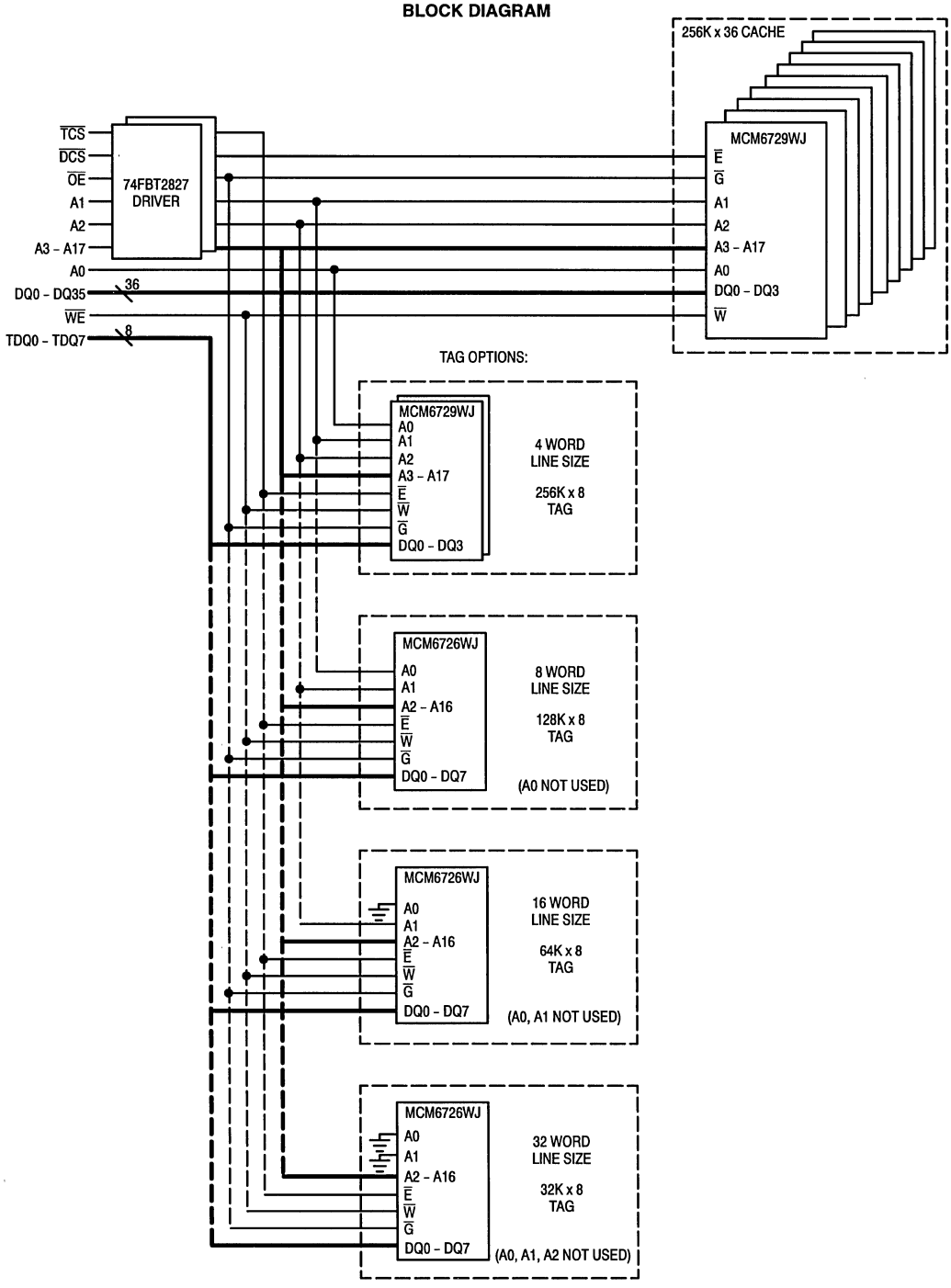
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	10	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 25 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

These BiCMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at leat 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}				V
(DQ0 – 35, TDQ0 – 7, $\overline{WE}$, A0)		2.2	—	V_{CC} + 0.3 V*	
(A1 – A17, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)		2.0	—	V_{CC} + 0.3 V*	
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
** V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 10	µA
Output Leakage Current ($\overline{G}$, $\overline{xCS}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 10	µA
AC Supply Current ($\overline{G}$, $\overline{xCS}$ = V_{IL}, I_{out} = 0 mA)	I_{CCA}	—	—	1750	mA
Output Low Voltage (I_{OL} = + 8 mA)	V_{OL}	—	—	0.4	V
OUtput High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (A0, $\overline{WE}$)	C_{in}	—	110	pF
Input Capacitance (A1 – A17, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)	C_{in}	—	10	pF
Input/Output Capacitance	C_{out}	—	10	pF

6

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Access Time	t_{AVQV}	—	12	—	15	—	17	ns	
A0 Access Time	t_{A0AQV}	—	10	—	12	—	14	ns	
Data/Tag Enable Access Time	t_{ELQV}	—	12	—	15	—	17	ns	
Output Enable Access Time	t_{GLQV}	—	9	—	10	—	11	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Hold from A0 Change	t_{A0XQX}	4	—	4	—	4	—	ns	
Data/Tag Enable Low to Output Active	t_{ELQX}	2	—	2	—	2	—	ns	3, 4
Data/Tag Enable High to Output High–Z	t_{EHQZ}	1	9	1	10	1	11	ns	3, 4
Output Enable Low to Output Active	t_{GLQX}	1	—	1	—	1	—	ns	3,4
Output Enable High to Output High–Z	t_{GHQZ}	1	9	1	10	1	11	ns	3, 4

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

AC TEST LOADS

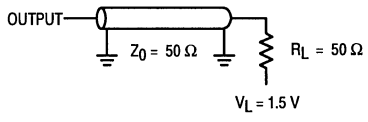


Figure 1A

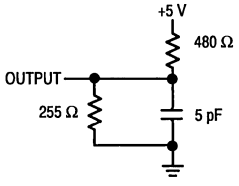


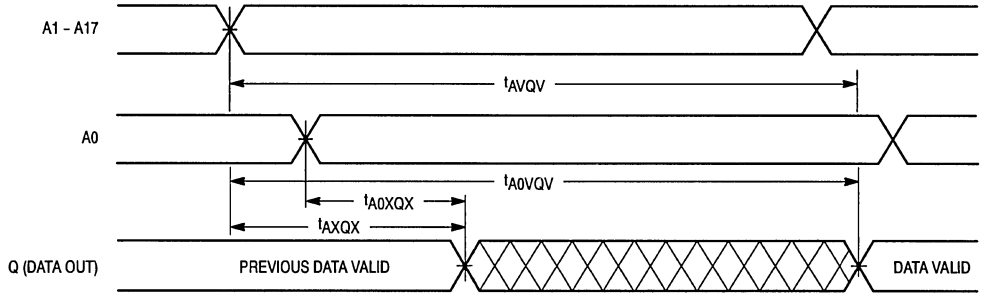
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

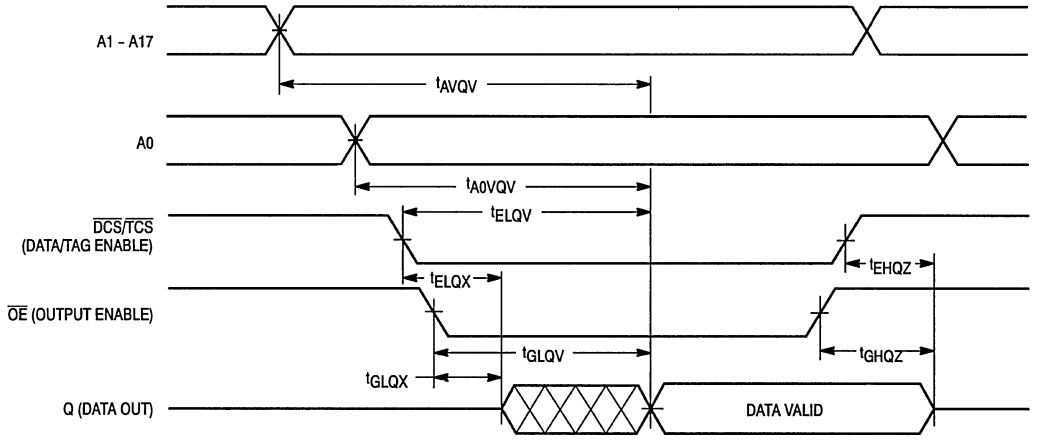
6

READ CYCLE 1 (See Note)



NOTE: Module is continuously selected ($\overline{DCS}$ or $\overline{TCS}$ = V_{IL}, $\overline{OE}$ = V_{IL})

READ CYCLE 2 (See Note)



NOTE: Address valid prior to or coincident with $\overline{DCS}$ or $\overline{TCS}$ going low.

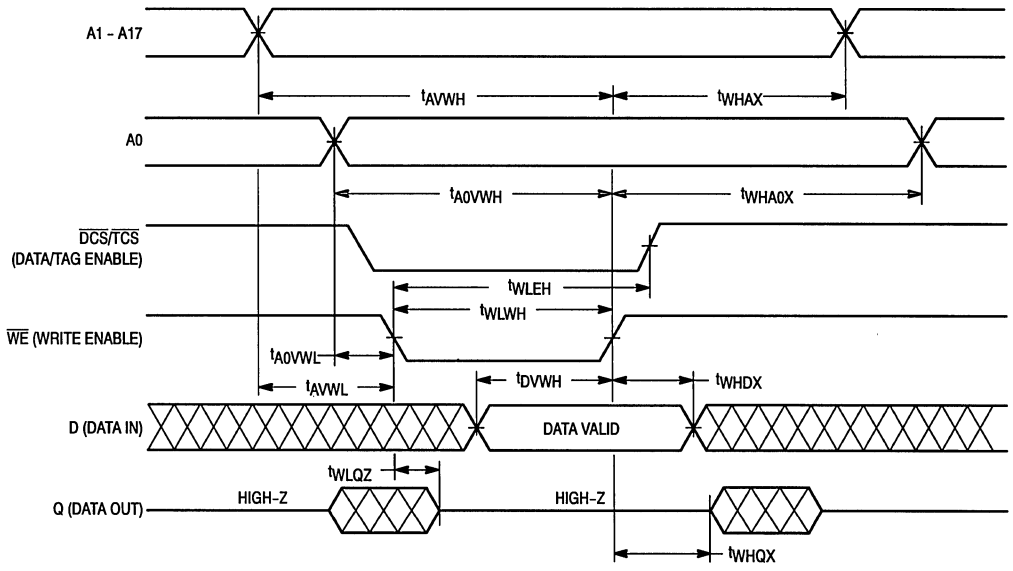
6

WRITE CYCLE 1 ($\overline{WE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVWL}	5	—	5	—	5	—	ns	
A0 Setup Time	t_{A0VWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VWH}	10	—	12	—	14	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	7	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	6	—	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	3, 4
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	3, 4
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	
Write Recovery Time – A0	t_{WHA0X}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1

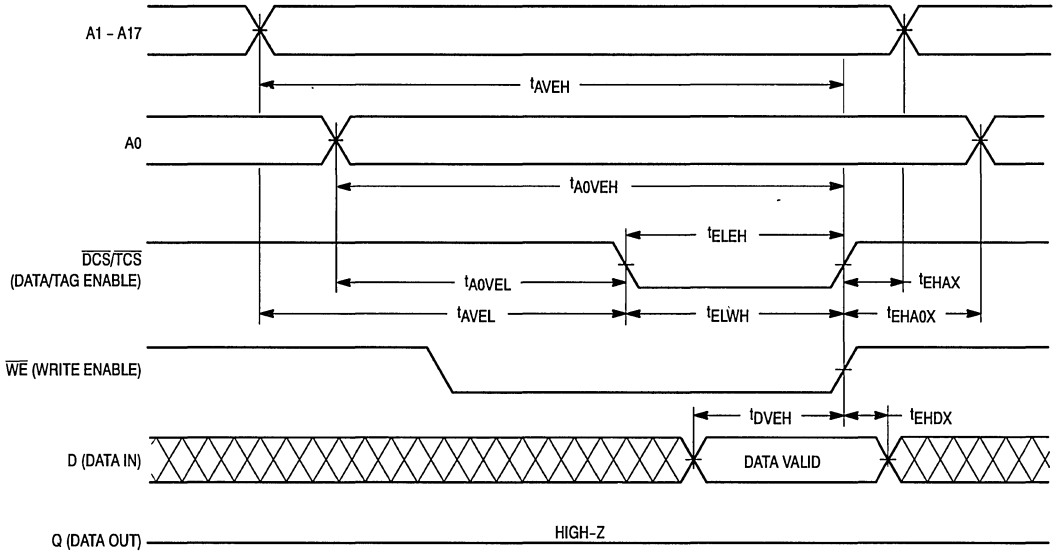


WRITE CYCLE 2 ($\overline{DCS}$ or $\overline{TCS}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–12		–15		–17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VEH}	10	—	12	—	14	—	ns	
Data/Tag Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	6	—	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	5	—	5	—	5	—	ns	
Write Recovery Time	t_{EHAX}	5	—	5	—	5	—	ns	
Write Recovery Time – A0	t_{EHA0X}	5	—	5	—	5	—	ns	

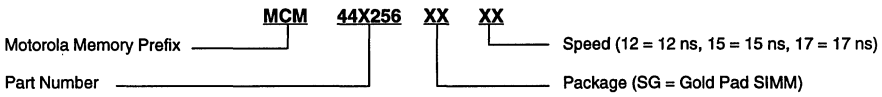
NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.

WRITE CYCLE 2



6

ORDERING INFORMATION
(Order by Full Part Number)



Part Number	Unified/Split	Word Line Size	TAG Depth
MCM44A256	Unified/Split	4	256K
MCM44B256	Unified/Split	8	128K
MCM44C256	Unified/Split	16	64K
MCM44D256	Unified/Split	32	32K

6

MCM32A732
MCM32A832
MCM32A932
MCM32A764
MCM32A864
MCM32A964

Advance Information

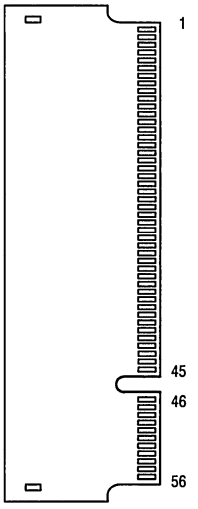
128KB/256KB Secondary Cache Module

With Tag, Valid, and Dirty for i486 Processor Systems

This family of cache modules is well suited to provide the secondary cache for the Intel 82420 PCI chipset. This family provides the 128K Byte and 256K Byte cache sizes with valid, dirty and a choice of 7, 8, or 9 tag bits. The tag/valid bits have 12 ns access times for zero wait states at 33 MHz clock speeds. The PD pins map into the configuration register of the 82420 for auto–configuration of the cache controller during system startup.

- Low Profile Edge Connector: Burndy Part Number: CELP2X56SC3Z48
- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Cycle Time: Up to External Processor Bus Speed of 33 MHz
- Cache Byte Write, Bank Chip Enable, Bank Output Enable
- Decoupling Capacitors are Used for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes

112–LEAD
CARD EDGE
CASE 1112–01
TOP VIEW



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BurstRAM is a registered trademark of Motorola.
I486 is a registered trademark Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
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PIN ASSIGNMENT
CACHE MODULE
112–LEAD CARDEDGE
TOP VIEW

PD4	PD3	PD2	PD1	PD0	Cache Size	Main Memory Max	Module
NC	NC	NC	NC	NC	—	—	No Module
V_{CC}	V_{CC}	NC	NC	V_{CC}	128KB	16MB	32A732
V_{CC}	NC	NC	NC	V_{CC}	128KB	32MB	32A832
V_{CC}	NC	V_{CC}	NC	V_{CC}	128KB	64MB	32A932
V_{CC}	V_{CC}	NC	V_{CC}	NC	256KB	32MB	32A764
V_{CC}	NC	NC	V_{CC}	NC	256KB	64MB	32A864
V_{CC}	NC	V_{CC}	V_{CC}	NC	256KB	128MB	32A964

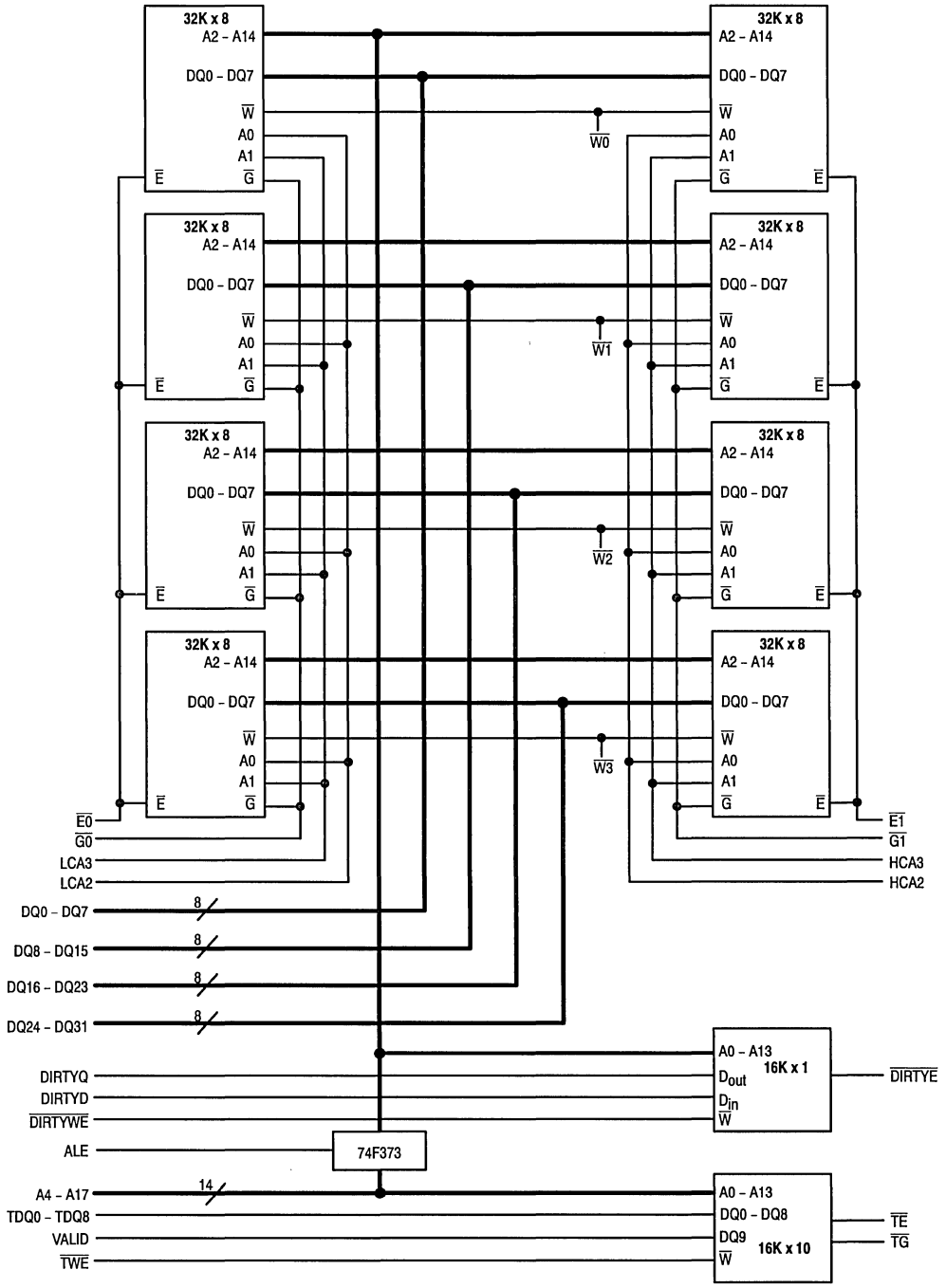
PIN NAMES	
A4 – A19	Address Inputs
HCA2, HCA3	Upper Bank Address Inputs
LCA2, LCA3	Lower Bank Address Inputs
ALE	Address Latch Enable
$\overline{Wx}$	Byte Write Enable
$\overline{E0}$, $\overline{E1}$	Bank Chip Enable
$\overline{G0}$, $\overline{G1}$	Bank Output Enable
DQ0 – DQ31	Cache Data Input/Output
TDQ0 – TDQ8	Tag Data Input/Output
$\overline{TWE}$	Tag Write Enable
$\overline{TG}$	Tag Output Enable
$\overline{TE}$	Tag Chip Enable
VALID	Valid Bit
$\overline{DIRTYWE}$	Dirty Write Enable
$\overline{DIRTYE}$	Dirty Chip Enable
DIRTYD	Dirty Data Input
DIRTYQ	Dirty Data Output
PD0 – PD4	Presence Detect
NC	No Connect
V_{CC}	+5 V Power Supply
V_{SS}	Ground

V_{SS}	57	1	V_{SS}
DQ0	58	2	DQ1
DQ2	59	3	DQ3
DQ4	60	4	DQ5
DQ6	61	5	DQ7
V_{CC}	62	6	V_{CC}
NC	63	7	NC
DQ8	64	8	DQ9
DQ10	65	9	DQ11
DQ12	66	10	DQ13
V_{SS}	67	11	V_{SS}
DQ14	68	12	DQ15
DQ16	69	13	DQ17
DQ18	70	14	DQ19
DQ20	71	15	DQ21
V_{CC}	72	16	V_{CC}
DQ22	73	17	DQ23
NC	74	18	NC
DQ24	75	19	DQ25
DQ26	76	20	DQ27
V_{SS}	77	21	V_{SS}
DQ28	78	22	DQ29
DQ30	79	23	DQ31
LA2	80	24	HA2
LA3	81	25	HA3
V_{CC}	82	26	V_{CC}
A4	83	27	A5
A6	84	28	A7
A8	85	29	A9
A10	86	30	A11
A12	87	31	A13
A14	88	32	A15
A16	89	33	NC
NC	90	34	NC
V_{SS}	91	35	V_{SS}
DIRTYD	92	36	DIRTYQ
TDQ0	93	37	TDQ1
TDQ2	94	38	TDQ3
TDQ4	95	39	TDQ5
V_{SS}	96	40	V_{SS}
TDQ6	97	41	TDQ7*
VALID	98	42	TDQ8**
$\overline{TE}$	99	43	ALE
$\overline{TWE}$	100	44	$\overline{WE0}$
V_{CC}	101	45	V_{CC}
V_{SS}	102	46	V_{SS}
$\overline{TG}$	103	47	$\overline{WE1}$
$\overline{DIRTYWE}$	104	48	$\overline{WE2}$
$\overline{DIRTYE}$	105	49	$\overline{WE3}$
V_{CC}	106	50	V_{CC}
$\overline{G0}$	107	51	$\overline{G1}$
$\overline{E0}$	108	52	$\overline{E1}$
PD0	109	53	PD1
PD2	110	54	PD3
PD4	111	55	NC
V_{SS}	112	56	V_{SS}

* No Connect for 32A864, 32A832

** No Connect for 32A764, 32A864, 32A732, 32A832

486 256KB CACHE MODULE BLOCK DIAGRAM WITH 9 TAG BITS



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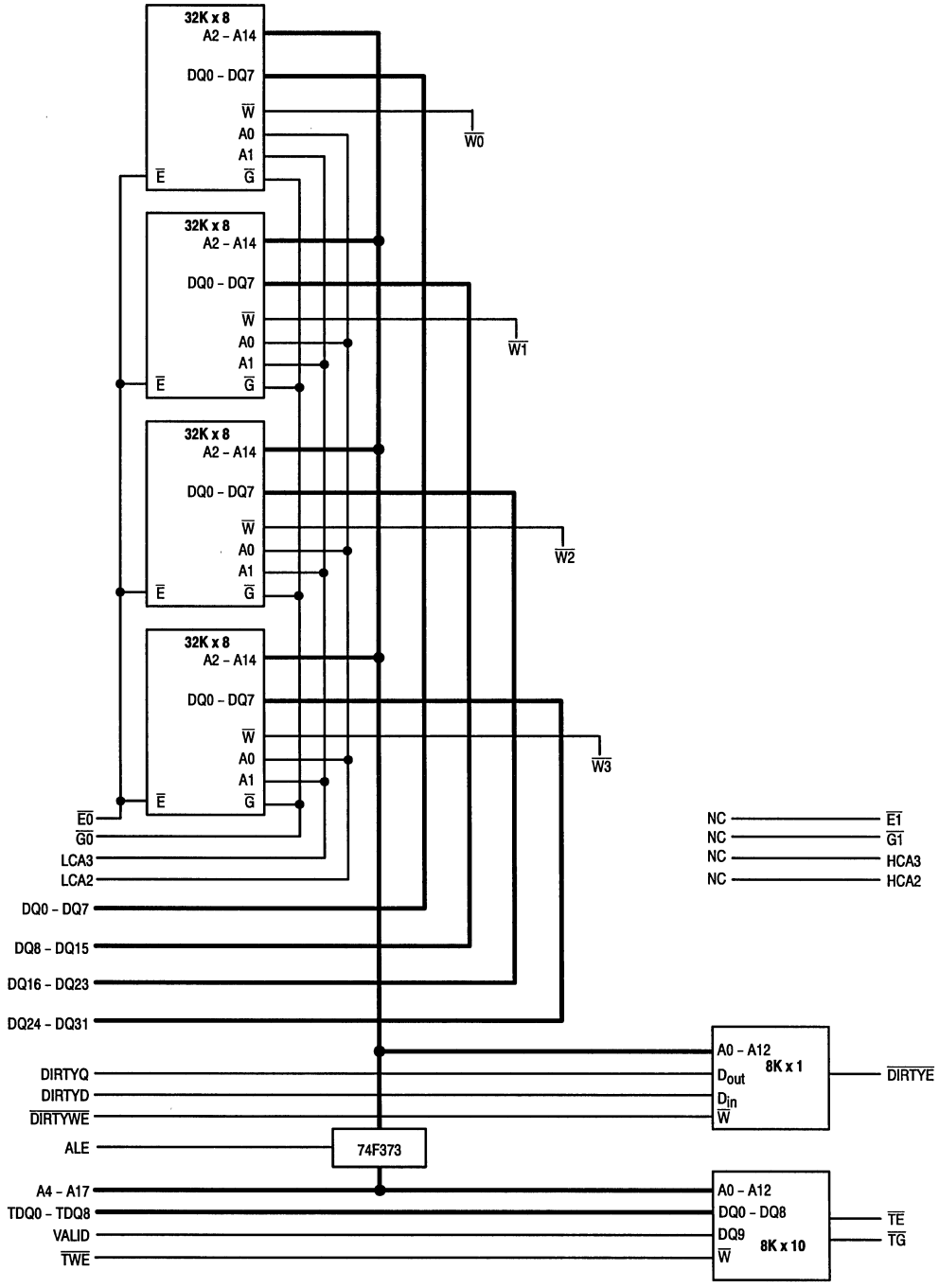
486 128KB CACHE MODULE BLOCK DIAGRAM WITH 9 TAG BITS



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	H	Output Disabled	I_{CCA}	High–Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

NOTE: $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	11.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 10	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 10	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	32Ax32 33 MHz	32Ax64 33 MHz	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	750	1250	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	180	300	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	120	200	mA

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CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Cache Address Input Capacitance	C_{in}	48	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF
Tag Address Input Capacitance	C_{in}	18	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol	Data		Tag/Valid		Dirty		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	30	—	30	—	30	—	ns	3
Address Access Time xCA2–3	t_{AVQV}	—	20	—	12	—	—	ns	9
(Transparent Mode) A4 – A19	t_{AVQV}	—	25	—	12	—	25		
Chip Select Access Time	t_{ELQV}	—	20	—	12	—	20	ns	4
Output Enable to Output Valid	t_{GLQV}	—	10	—	6	—	—	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	5,6,7
Enable Low to Output Active	t_{ELQX}	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High–Z	t_{EHQZ}	—	9	—	7	—	9	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High–Z	t_{GHQZ}	—	8	—	6	—	—	ns	5,6,7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
9. TAG Address Access Time t_{AVTV}.

6

AC TEST LOADS

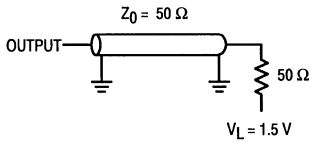


Figure 1A

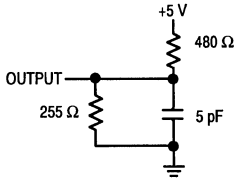
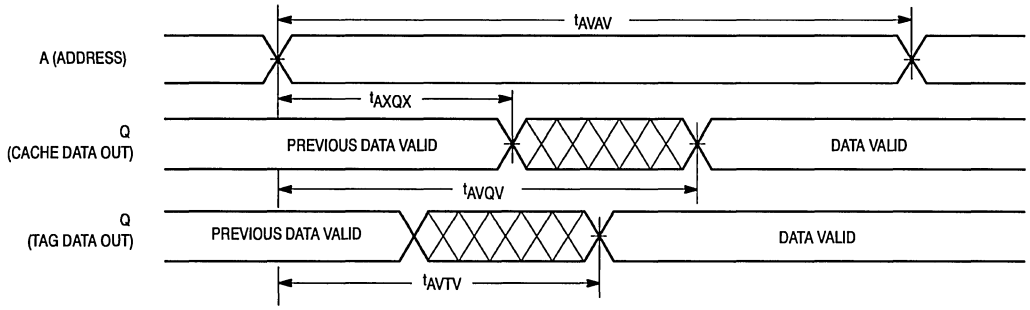


Figure 1B

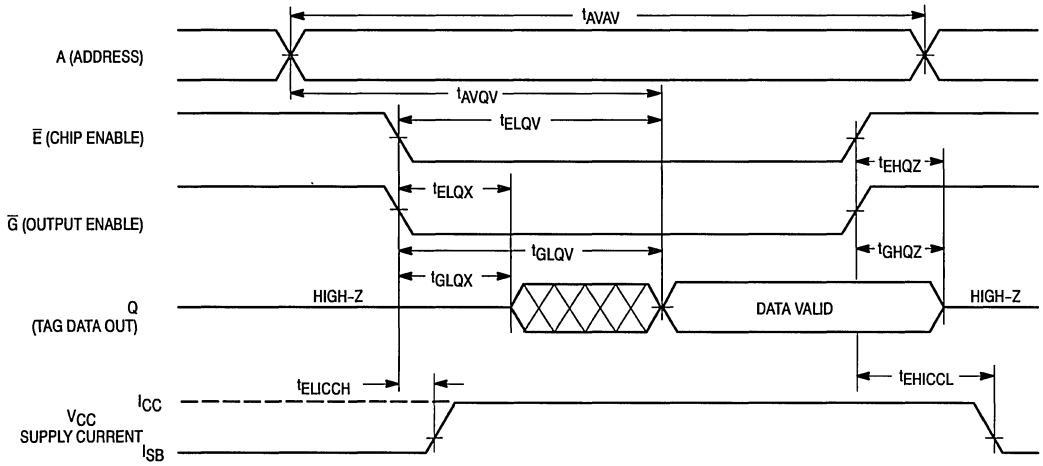
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)



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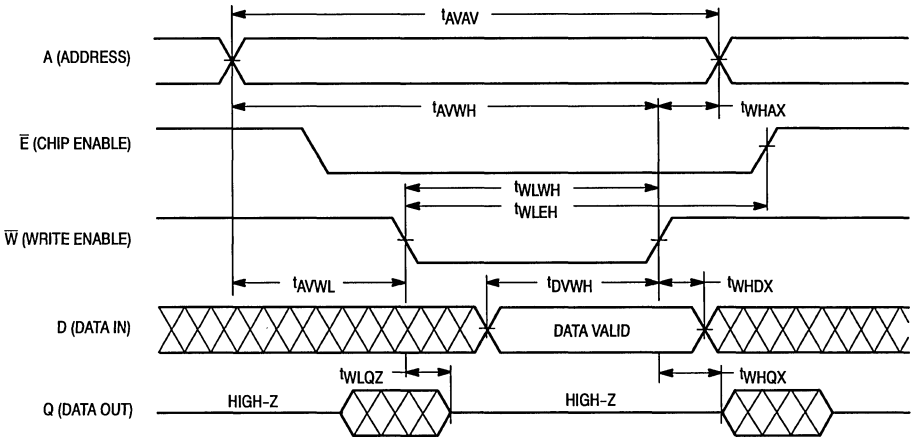
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	Data		Tag/Valid		Dirty		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	30	—	30	—	30	—	ns	4
Address Setup Time (A4 – A5)	t_{AVWL}	2	—	—	—	—	—	ns	
Address Setup Time (A6 – A19)		10	—	2	—	10	—		
Address Valid to End of Write	t_{AVWH}	20	—	10	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	12	—	12	—	ns	
Data Setup to Write Time	t_{DVWH}	8	—	6	—	8	—	ns	
Data Hold from Write Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	8	0	6	0	8	ns	6,7,8
Write High to Output Active	t_{WHQX}	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

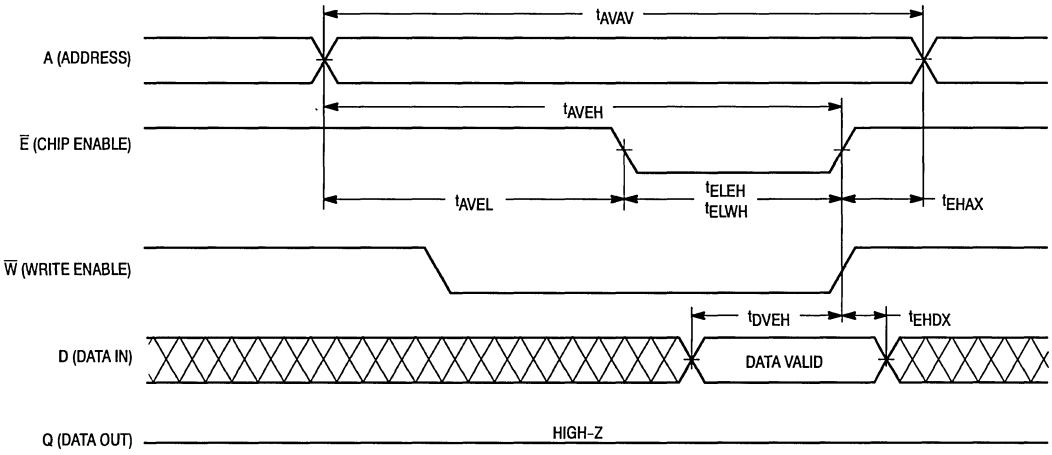


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	Data		Tag/Valid		Dirty		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	30	—	30	—	30	—	ns	4
Address Setup Time (A4 – A5) (A6 – A19)	t_{AVEL}	2 10	— —	— 2	— —	— 10	— —	ns	
Address Valid to End of Write	t_{AVEH}	20	—	10	—	20	—	ns	
Write Pulse Width	t_{ELEH}, t_{ELWH}	15	—	10	—	15	—	ns	
Data Setup to Write Time	t_{DVEH}	8	—	6	—	8	—	ns	
Data Hold from Write Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



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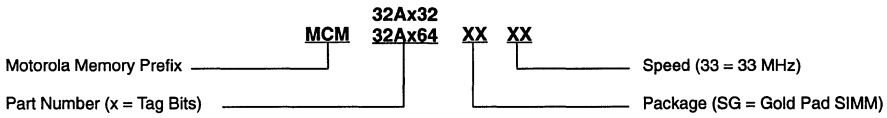
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32A732SG33 MCM32A764SG33
MCM32A832SG33 MCM32A864SG33
MCM32A932SG33 MCM32A964SG33

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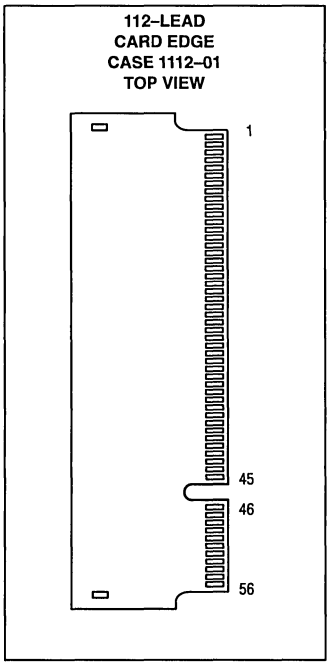
MCM32N864
MCM32N865
MCM32P864
MCM32P865

Advance Information

256KB Secondary Cache Module

With Tag and Optional Dirty for 486 Processor Systems



These 256K Byte cache modules offer dual asynchronous 32K x 32 banks of memory. There is a 16K x 8 tag memory for main memory cacheability up to 64 Megabytes. The MCM32N865 and MCM32P865 include a 16K x 1 common I/O dirty bit for writeback cache capability. The modules are designed to support common 486 chipsets which utilize chip enable ($\overline{CEx}$) byte control and bank write enable ($\overline{CWEx}$). The MCM32N864 and MCM32N865 operate at 5 V while the MCM32P864 and MCM32P865 operate at 3.3 V power. PD pins are provided for cache size identification at system startup

- 64MB of Cacheable Memory
- Low Profile Edge Connector: Burndy Part Number: CELP2X56SC3Z48
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Cycle Time: Up to External Processor Bus Speed of 33 MHz
- Cache Bank Write, Byte Chip Enable, Bank Output Enable
- Decoupling Capacitors are Used for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 5 V and 3.3 V Power Supplies are Supported

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1
6/95

PIN ASSIGNMENT
CACHE MODULE
112 PIN CARDEDGE
TOP VIEW

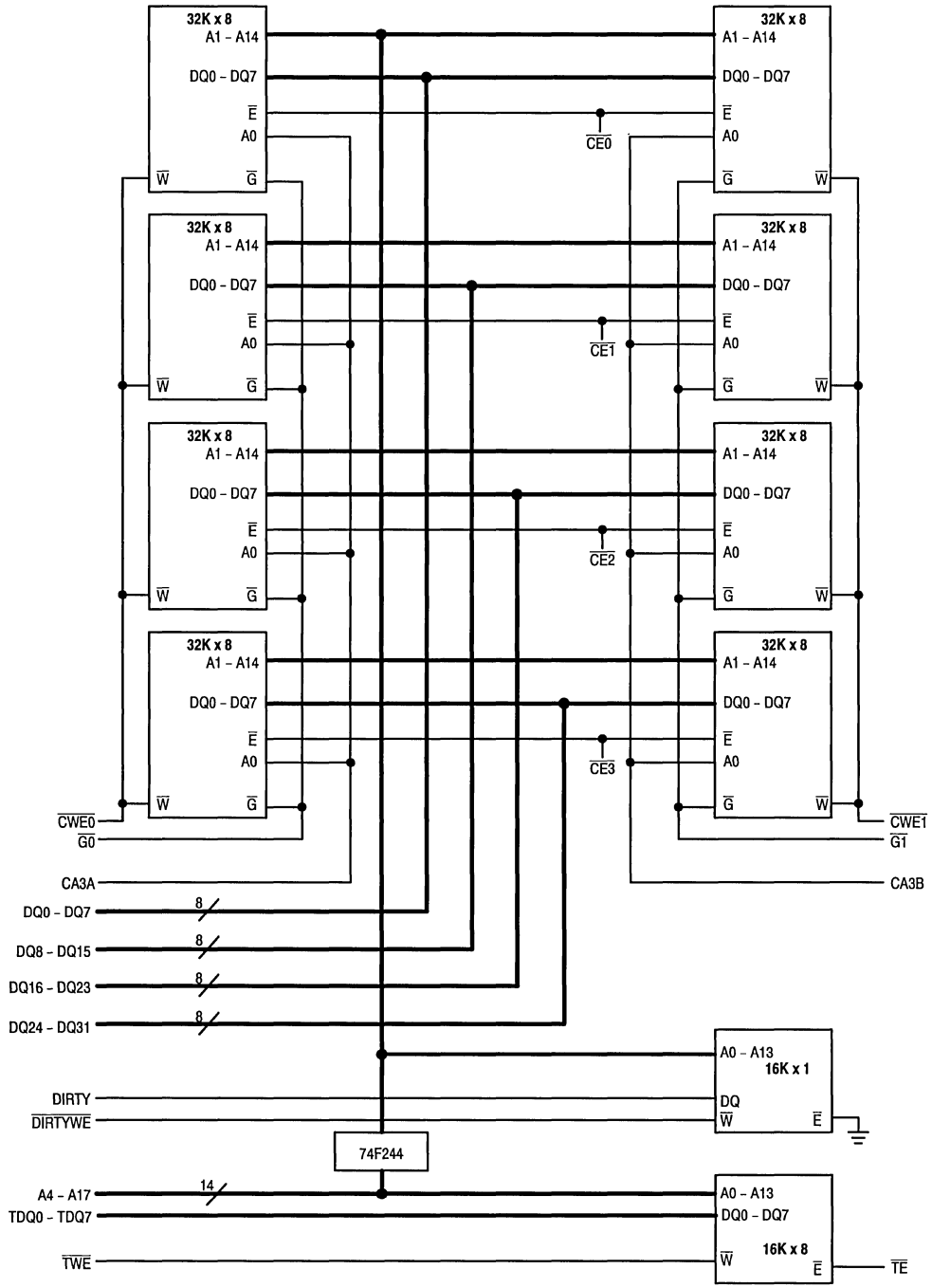
V_{SS}	57	1	V_{SS}
DQ0	58	2	DQ1
DQ2	59	3	DQ3
DQ4	60	4	DQ5
DQ6	61	5	DQ7
$V_{CC}5$	62	6	$V_{CC}3$
NC	63	7	NC
DQ8	64	8	DQ9
DQ10	65	9	DQ11
DQ12	66	10	DQ13
V_{SS}	67	11	V_{SS}
DQ14	68	12	DQ15
DQ16	69	13	DQ17
DQ18	70	14	DQ19
DQ20	71	15	DQ21
$V_{CC}5$	72	16	$V_{CC}3$
DQ22	73	17	DQ23
NC	74	18	NC
DQ24	75	19	DQ25
DQ26	76	20	DQ27
V_{SS}	77	21	V_{SS}
DQ28	78	22	DQ29
DQ30	79	23	DQ31
CA3B	80	24	NC
CA3A	81	25	NC
$V_{CC}5$	82	26	$V_{CC}3$
A4	83	27	A5
A6	84	28	A7
A8	85	29	A9
A10	86	30	A11
A12	87	31	A13
A14	88	32	A15
A16	89	33	A17
NC	90	34	NC
V_{SS}	91	35	V_{SS}
NC	92	36	NC
TDQ0	93	37	TDQ1
TDQ2	94	38	TDQ3
TDQ4	95	39	TDQ5
V_{SS}	96	40	V_{SS}
TDQ6	97	41	TDQ7
NC	98	42	DIRTY*
$\overline{TE}$	99	43	NC
$\overline{TWE}$	100	44	$\overline{CE0}$
$V_{CC}5$	101	45	$V_{CC}3$
V_{SS}	102	46	V_{SS}
NC	103	47	$\overline{CE1}$
*$\overline{DIRTYWE}$	104	48	$\overline{CE2}$
NC	105	49	$\overline{CE3}$
$V_{CC}5$	106	50	$V_{CC}3$
$\overline{G0}$	107	51	$\overline{G1}$
$\overline{CWE0}$	108	52	$\overline{CWE1}$
PD0	109	53	PD1
PD2	110	54	PD3
NC	111	55	NC
V_{SS}	112	56	V_{SS}

PD3	PD2	PD1	PD0	Cache Size	Dirty	Module
NC	NC	NC	NC	—	—	No Module
NC	GND	NC	NC	256KB	No	32N864 32P864
GND	GND	NC	NC	256KB	Yes	32N865 32P865

PIN NAMES	
A4 – A17	Address Inputs
CA3A, CA3B	Bank Address Inputs
$\overline{CWEx}$	Bank Write Enable
$\overline{CEx}$	Byte Chip Enable
$\overline{G0}$, $\overline{G1}$	Bank Output Enable
DQ0 – DQ31	Cache Data Input/Output
TDQ0 – TDQ8	Tag Data Input/Output
$\overline{TWE}$	Tag Write Enable
$\overline{TE}$	Tag Chip Enable
$\overline{DIRTYWE}$	Dirty Write Enable
DIRTY	Dirty Input/Output
PD0 – PD3	Presence Detect
NC	No Connect
$V_{CC}5$	+5 V Power Supply
$V_{CC}3$	+3.3 V Power Supply
V_{SS}	Ground

* No Connect for MCM32N864 and MCM32P864

MCM32N865
486 256KB CACHE MODULE BLOCK DIAGRAM
WITH 8 TAG BITS AND DIRTY



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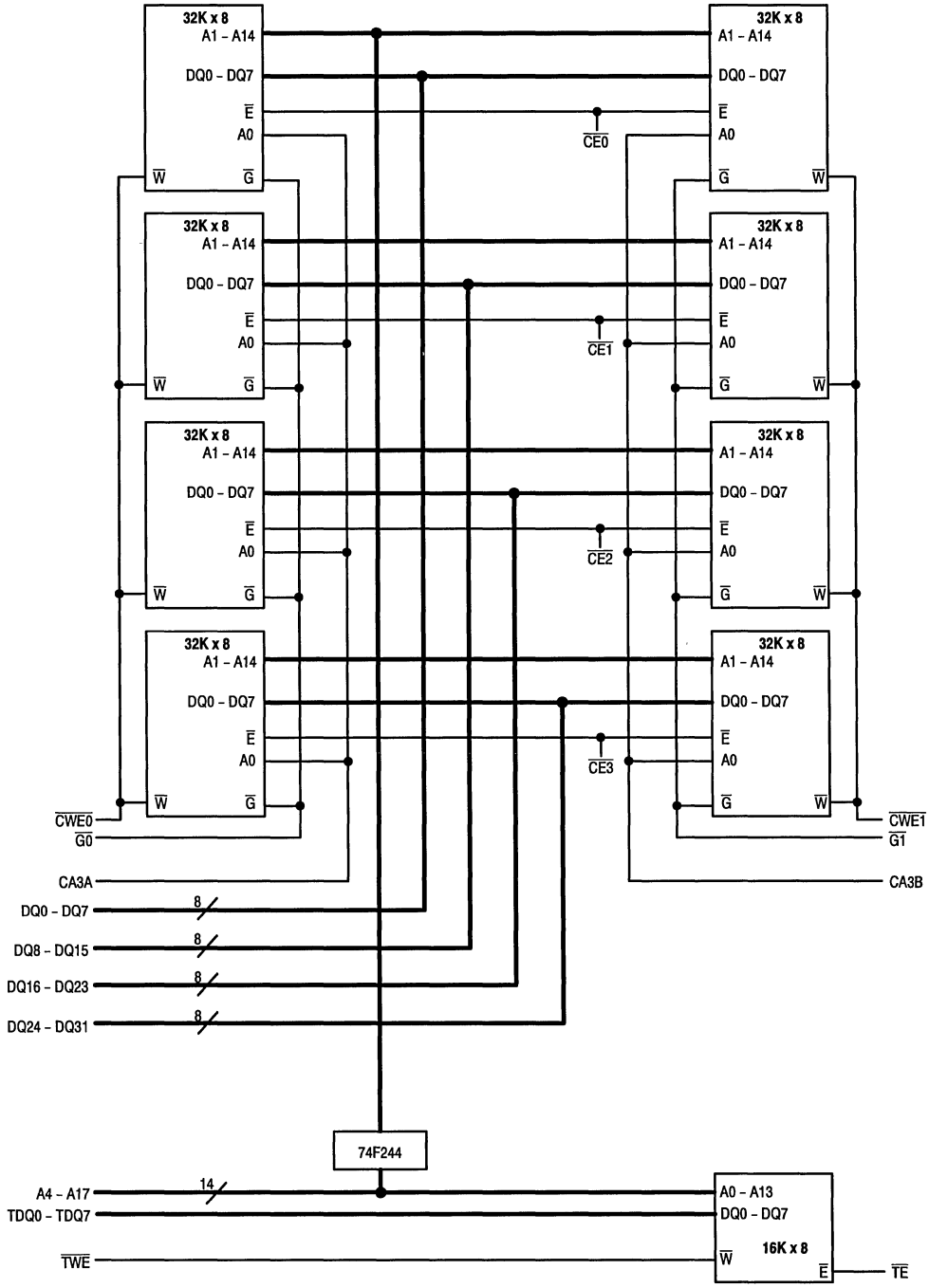
MCM32N864
486 128KB CACHE MODULE BLOCK DIAGRAM
WITH 8 TAG BITS



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MCM64AF32

Product Preview

256K Asynchronous Secondary Cache Module for Pentium™

The MCM64AF32 is designed to provide 256K of asynchronous L2 cache for the Pentium microprocessor in conjunction with Intel's Triton chip set. The module is configured as 32K x 64 bits in a 160 pin card edge connector. The module uses eight Motorola 3.3 V 32K x 8 FSRAMs for the cache memory, one Motorola 5 V 32K x 8 FSRAM for the tag RAM, and an upper order address latch.

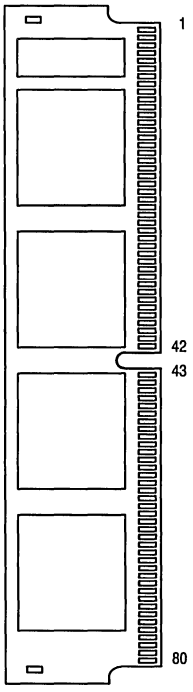
Eight write enables are provided for byte write control.

PD0–PD4 identify density and functionality.

This cache module is plug and pin compatible with the other members of Motorola's Triton chip set module family, the MCM72JG32SG66 (a 256K byte pipelined BurstRAM module) and the MCM72JG64SG66 (a 512K byte pipelined BurstRAM module).

- Low–Cost Asynchronous Solution for Triton Chip Set
- All Cache Data Inputs and Outputs are LVTTL (3.3 V I/O) Compatible
- All Tag I/Os are TTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 15 ns for Data RAMs and Tag RAM
- Decoupling Capacitors for each Fast Static RAM and Logic Device
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 160 Pin Card Edge Module
- Burndy Connector, Part Number: CELP2X80SC3Z48

160–LEAD
CARD EDGE
CASE TBD*
TOP VIEW



* SEE CHAPTER 9 FOR PRELIMINARY CASE OUTLINE.

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Pentium is a trademark of Intel Corp.

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PIN ASSIGNMENT
160–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
(RSVD) NC	86	6	NC (RSVD)
$V_{CC}5$	87	7	$V_{CC}3$
(RSVD) NC	88	8	$\overline{TWE}$
($\overline{CADV}$) CAA4	89	9	CAA3 ($\overline{CADS}$)
V_{SS}	90	10	V_{SS}
$\overline{COE}$	91	11	$\overline{CWE4}$
$\overline{CWE5}$	92	12	$\overline{CWE6}$
$\overline{CWE7}$	93	13	$\overline{CWE0}$
$\overline{CWE1}$	94	14	$\overline{CWE2}$
$V_{CC}5$	95	15	$V_{CC}3$
$\overline{CWE3}$	96	16	CAB4 ($\overline{CCS}$)
CAB3	97	17	NC ($\overline{GWE}$)
CALE	98	18	NC ($\overline{BWE}$)
V_{SS}	99	19	V_{SS}
(RSVD) NC	100	20	NC (A3)
(A4) NC	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
$V_{CC}5$	105	25	$V_{CC}3$
A17	106	26	NC (A18)
V_{SS}	107	27	V_{SS}
A9	108	28	A12
A14	109	29	A13
A15	110	30	NC ($\overline{ADSP}$)
(RSVD) NC	111	31	NC ($\overline{CS}$/$\overline{ECS1}$)
PD0	112	32	NC ($\overline{ECS2}$)
PD2	113	33	PD1
PD4	114	34	PD3
V_{SS}	115	35	V_{SS}
(CLK0) NC	116	36	NC (CLK1)
V_{SS}	117	37	V_{SS}
DQ63	118	38	DQ62
$V_{CC}5$	119	39	$V_{CC}3$
DQ61	120	40	DQ60
DQ59	121	41	DQ58
DQ57	122	42	DQ56
V_{SS}	123	43	V_{SS}
DQ55	124	44	DQ54
DQ53	125	45	DQ52
DQ51	126	46	DQ50
DQ49	127	47	DQ48
V_{SS}	128	48	V_{SS}
DQ47	129	49	DQ46
DQ45	130	50	DQ44
DQ43	131	51	DQ42
$V_{CC}5$	132	52	$V_{CC}3$
DQ41	133	53	DQ40
DQ39	134	54	DQ38
DQ37	135	55	DQ36
V_{SS}	136	56	V_{SS}
DQ35	137	57	DQ34
DQ33	138	58	DQ32
DQ31	139	59	DQ30
$V_{CC}5$	140	60	$V_{CC}3$
DQ29	141	61	DQ28
DQ27	142	62	DQ26
DQ25	143	63	DQ24
V_{SS}	144	64	V_{SS}
DQ23	145	65	DQ22
DQ21	146	66	DQ20
DQ19	147	67	DQ18
$V_{CC}5$	148	68	$V_{CC}3$
DQ17	149	69	DQ16
DQ15	150	70	DQ14
DQ13	151	71	DQ12
V_{SS}	152	72	V_{SS}
DQ11	153	73	DQ10
DQ9	154	74	DQ8
DQ7	155	75	DQ6
$V_{CC}5$	156	76	$V_{CC}3$
DQ5	157	77	DQ4
DQ3	158	78	DQ2
DQ1	159	79	DQ0
V_{SS}	160	80	V_{SS}

PRESENCE DETECT TABLE

Cache Size and Functionality	Module	PD4	PD3	PD2	PD1	PD0
256KB Async	MCM64AF32	V_{SS}	NC	V_{SS}	V_{SS}	NC
512KB Async	—	V_{SS}	V_{SS}	NC	V_{SS}	NC
256K Burst	—	V_{SS}	NC	V_{SS}	NC	V_{SS}
256K Pipe Burst	MCM72JG32	V_{SS}	NC	V_{SS}	NC	NC
512K Burst	—	V_{SS}	V_{SS}	NC	NC	V_{SS}
512K Pipe Burst	MCM72JG64	V_{SS}	V_{SS}	NC	NC	NC
512K 2–Bank Burst	—	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}

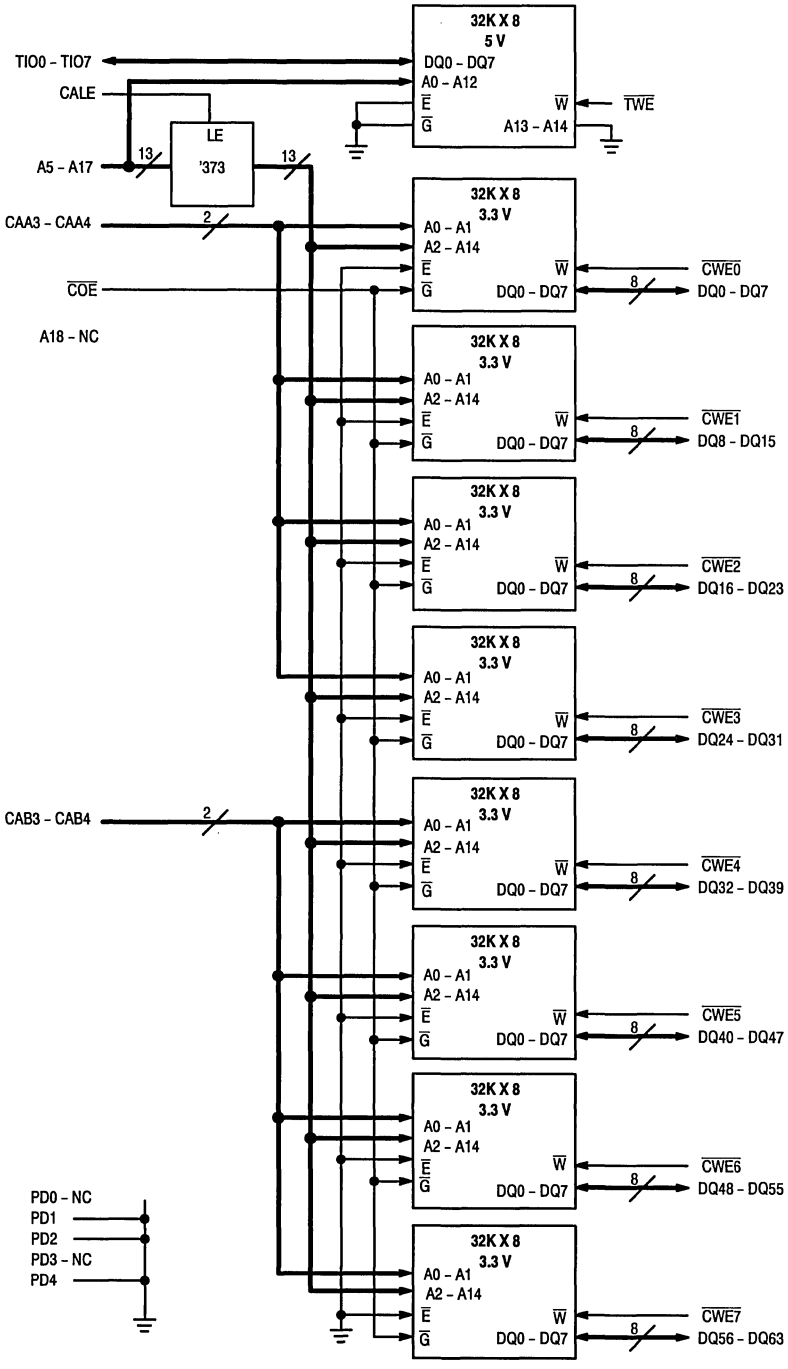
PIN NAMES

$\overline{TIO0}$ – TIO7	Tag RAM I/O
$\overline{TWE}$	Tag Write Enable
CALE	Address Latch Enable
A5 – A17	Address Inputs
$\overline{CWE0}$ – $\overline{CWE7}$	Cache Write Enable
CAA3 –CAA4	Cache Address A
$\overline{CAB3}$ – CAB4	Cache Address B
$\overline{COE}$	Cache Output Enable
DQ0 – DQ63	Data Input/Output
PD0 – PD4	Presence Detect
$V_{CC}3$	+ 3.3 V Power Supply
$V_{CC}5$	+ 5.0 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, V_{SS} must be connected to ground.

NOTE: Signals in parentheses indicate pin designations for burstable members of the Triton chip set module family.

MCM64AF32 MODULE BLOCK DIAGRAM



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PIN DESCRIPTIONS

160–Lead Card Edge Pin Locations	Symbol	Type	Description
21, 22, 23, 24, 28, 29, 102, 103, 104, 106, 108, 109, 110	A5 – A17	Input	Address Inputs: These inputs are latched into data RAMs and must meet setup and hold times. The tag RAM addresses are not latched. (See Block Diagram).
9, 89	CAA3, CAA4	Input	Cache Address A: Low order address inputs for bursting. Not latched.
16, 97	CAB3, CAB4	Input	Cache Address B: Low order address inputs for bursting. Not latched.
98	CALE	Input	Address Latch Enable: Active low signal latches A5 – A17.
11, 12, 13, 14, 92, 93, 94, 96	$\overline{\text{CWE0}}$ – $\overline{\text{CWE7}}$	Input	Cache Data Write Enable: Active low write signal for data RAMs.
8	$\overline{\text{TWE}}$	Input	Tag Write Enable: Active low write signal for tag RAMs.
—	$\overline{\text{CS}}$	Input	Chip Select: Active low chip enable for tag and data RAMs. Not used.
91	$\overline{\text{COE}}$	Input	Cache Output Enable: Asynchronous active low output enable for data RAMs.
38, 40, 41, 42, 44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 61, 62, 63, 65, 66, 67, 69, 70, 71, 73, 74, 75, 77, 78, 79, 118, 120, 121, 122, 124, 125, 126, 127, 129, 130, 131, 133, 134, 135, 137, 138, 139, 141, 142, 143, 145, 146, 147, 149, 150, 151, 153, 154, 155, 157, 158, 159	DQ0 – DQ63	I/O	Data I/O
2, 3, 4, 5, 82, 83, 84, 85	TIO0 – TIO7	I/O	Tag RAM I/O: Drives data out during tag compare cycles. Stores data to tag RAM during tag WRITE cycles.
33, 34, 112, 113, 114	PD0 – PD4		Presence Detect: See Presence Detect Table.
7, 15, 25, 39, 52, 60, 68, 76	$V_{CC}3$	Supply	Power Supply: 3.3 V ± 5%.
87, 95, 105, 119, 132, 140, 148, 156	$V_{CC}5$	Supply	Power Supply: 5.0 V ± 5%.
1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160	V_{SS}	Supply	Ground
6, 17, 18, 20, 26, 30, 31, 32, 36, 86, 88, 100, 101, 111, 116	NC	—	No Connection: There is no connection to the module.

TRUTH TABLE FOR TAG AND DATA RAMs (X = Don't Care)

$\overline{COE}$	$\overline{CWE}$	Mode	V_{CC} Current	Output	Cycle
H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Power Supply Voltage	for Tag for Data	V_{CC5} V_{CC3}	– 0.5 to + 7.0 – 0.5 to + 5.0	V
Voltage Relative to V_{SS}		V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5*	V
Output Current (per I/O)		I_{out}	± 20	mA
Temperature Under Bias		T_{bias}	– 10 to + 85	°C
Operating Temperature		T_A	0 to + 70	°C
Storage Temperature – Plastic		T_{stg}	– 55 to + 125	°C

* For data RAMs, V_{CC} + 2.0 V ac to V_{SS} – 2.0 V ac (pulse width ≤ 20 ns).

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}3$ = 3.3 V ± 5%, V_{CC5} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	Tag RAM Data RAM and Latch	V_{CC}	4.75 3.135	5.0 3.3	5.25 3.465	V
Input High Voltage		V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage		V_{IL}	– 0.5**	0.0	0.8	V

* For Tag, V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns).
For Data, V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min)).
** For Tag, V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
For Data, V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min)).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 2	µA
Output Leakage Current ($\overline{COE}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 2	µA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
CMOS Output Low Voltage (I_{OL} = 100 µA)	V_{OL2}	—	0.1	V
CMOS Output High Voltage (I_{OH} = – 100 µA)	V_{OH2}	V_{CC} – 0.1	—	V

NOTE: NOTE: Good decoupling of the local power supply should always be used.

POWER SUPPLY CURRENTS

Parameter	Symbol	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	780	mA

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CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	($\overline{TWE}$, CALE, $\overline{CWE0}$ – $\overline{CWE7}$)	C_{in}	8	pF
	(A5 – A17)		14	
	(CAA3, CAA4, CAB3, CAB4)		26	
	($\overline{COE}$)		50	
Input/Output Capacitance	(DQ0 – DQ63)	$C_{I/O}$	8	pF
	(TIO0 – TIO7)		10	

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

DATA RAMs READ CYCLE (See Note 1)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time (CAAx, CABx)	t_{AVQV}	—	15	ns	
Latched Address Access Time (A5 – A17)	t_{LAVQV}	—	22	ns	
Latched Address to CALE Low Setup Time	t_{AVCALL}	4	—	ns	
Latched Address to CALE Low Hold Time	t_{CALAX}	3	—	ns	
Enable Access Time	t_{ELQV}	—	15	ns	3
Output Enable Access Time	t_{GLQV}	—	8	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	6
Enable Low to Output Active	t_{ELQX}	4	—	ns	4, 5, 6
Enable High to Output High–Z	t_{EHQZ}	0	8	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	ns	4, 5, 6
Output Enable High to Output High–Z	t_{GHQZ}	0	7	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0	—	ns	
Power Down Time	t_{EHICCL}	—	15	ns	

NOTES:
1. $\overline{CWE}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Addresses valid prior to or coincident with $\overline{CS}$ going low.
4. At any given voltage and temperature, t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{COE}$ = V_{IL}).

AC TEST LOADS

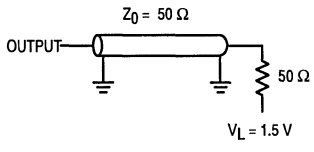


Figure 1A

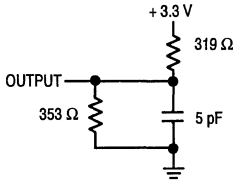
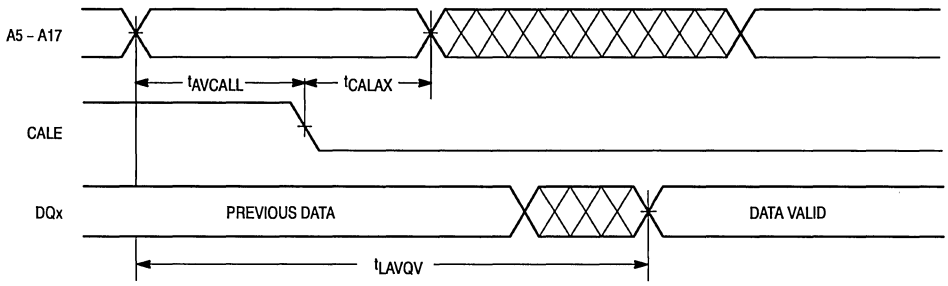


Figure 1B

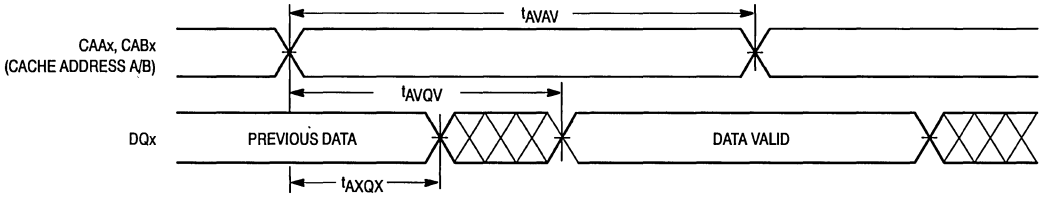
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

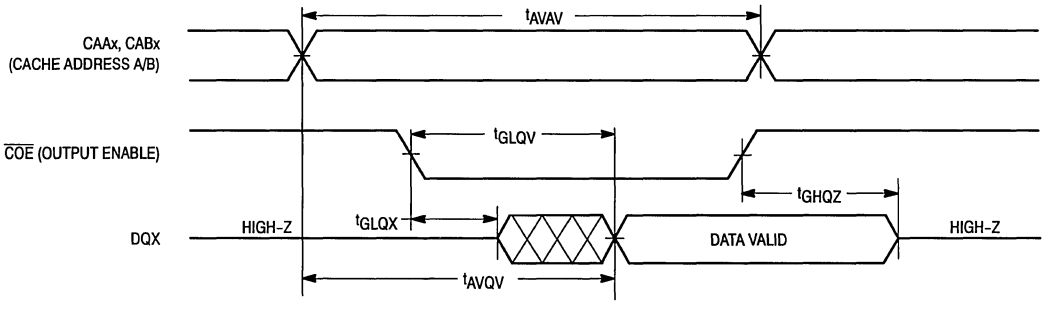
DATA RAMs FIRST ACCESS READ CYCLE (See Note 7)



DATA RAMs BURST ACCESS READ CYCLE (CALE ≤ V_{IL}) (See Note 7)



DATA RAMs READ CYCLE 3 (CALE ≤ V_{IL}) (See Note 3)



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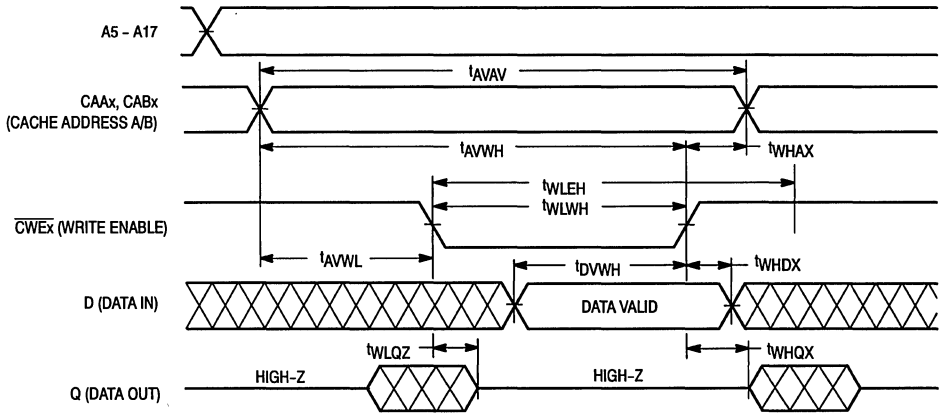
DATA RAMs WRITE CYCLE ($\overline{CWE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	ns	
Write Pulse Width, $\overline{COE}$ High	t_{WLWH}, t_{WLEH}	10	—	ns	4
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	4	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ low.
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $\overline{COE} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

DATA RAMs WRITE CYCLE (CALE ≥ V_{IH}) ($\overline{CWE}$ Controlled, See Notes 1 and 2)



TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

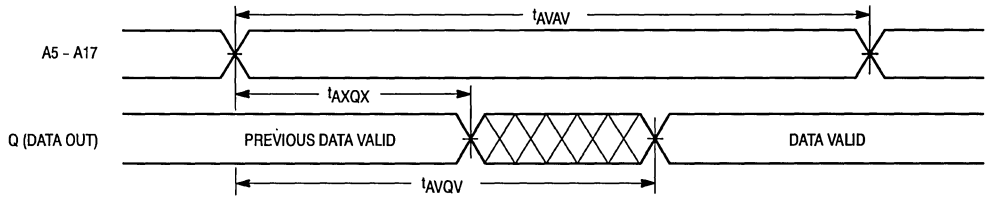
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

TAG RAM READ CYCLE (See Notes 1 and 5)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time	t_{AVQV}	—	15	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	3, 4

NOTES:
1. $\overline{CWE}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{COE}$ = V_{IL}).

TAG RAM READ CYCLE (See Note 5)



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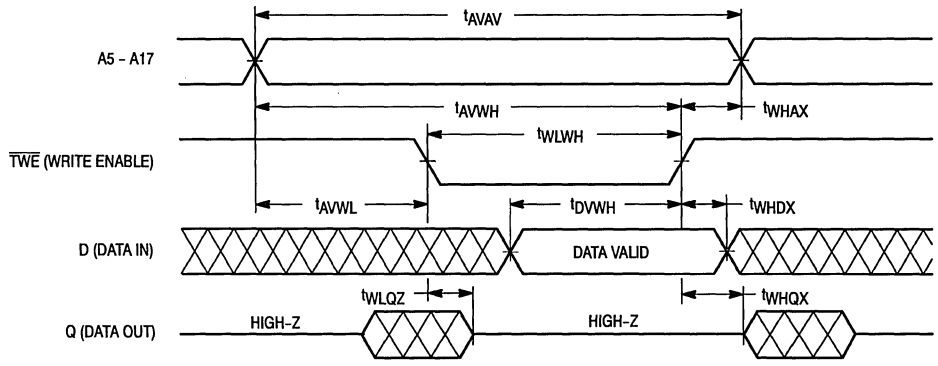
TAG RAM WRITE CYCLE (See Notes 1 and 2)

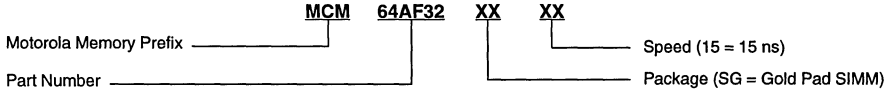
Parameter	Symbol	-15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	4	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ is low.
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $\overline{COE} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

TAG RAM WRITE CYCLE (See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number — MCM64AF32SG15

MCM64AG32

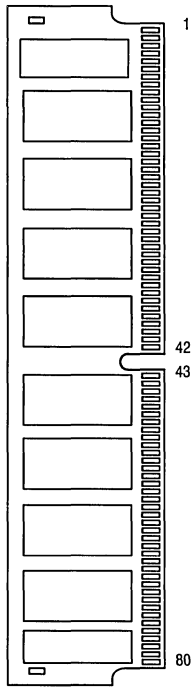
Product Preview

256KB Secondary Cache Module for Pentium™

The MCM64AG32 is designed to provide asynchronous 256KB secondary cache for the Pentium microprocessor using VLSI 82C590 chip set. The modules are configured as 32K x 64 bits in a 160 pin card edge memory module. Each module uses eight of Motorola's MCM6306 3.3 V power supply SRAM components.

- All Inputs and Outputs are LVTTL Compatible
- Multiple V_{SS} Pins and Decoupling Capacitors for Maximum Noise Immunity
- Three State Outputs
- Byte Write Enable
- Fast SRAM Access Times: 15 ns
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible
- Low Cost Solution for use with VLSI 82C590
- Presence Detect Pins Enable Active Probing by the System to Determine Cache Size and Type thus Supporting Multiple Cache Options Without Jumpers
- 160 Pin Card Edge Module
- Burndy Connector, Part Number: CELP2X80SC3Z48

160–LEAD
CARD EDGE
CASE TBD*
TOP VIEW



* SEE CHAPTER 9 FOR PRELIMINARY CASE OUTLINE.

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PIN ASSIGNMENT
160–LEAD CARD EDGE MODULE
TOP VIEW

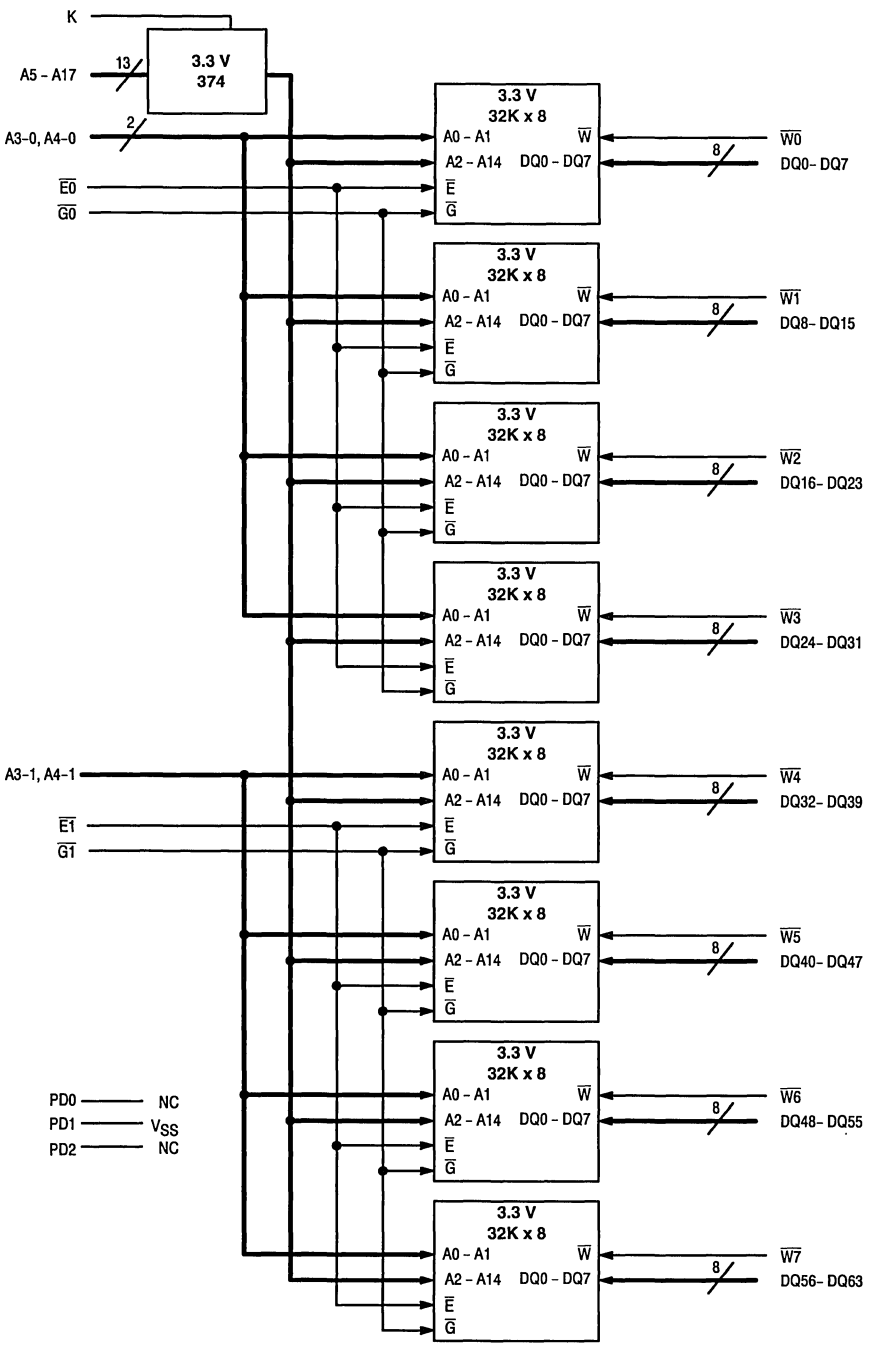
V_{SS}	81	1	V_{SS}
DQ63	82	2	DQ62
$V_{CC}5$	83	3	$V_{CC}3$
DQ61	84	4	DQ60
$V_{CC}5$	85	5	$V_{CC}3$
DQ59	86	6	DQ58
DQ57	87	7	DQ56
V_{SS}	88	8	V_{SS}
NC	89	9	NC
DQ55	90	10	DQ54
DQ53	91	11	DQ52
DQ51	92	12	DQ50
V_{SS}	93	13	V_{SS}
DQ49	94	14	DQ48
DQ47	95	15	DQ46
DQ45	96	16	DQ44
DQ43	97	17	DQ42
V_{SS}	98	18	V_{SS}
DQ41	99	19	DQ40
NC	100	20	NC
DQ39	101	21	DQ38
DQ37	102	22	DQ36
DQ35	103	23	DQ34
V_{SS}	104	24	V_{SS}
DQ33	105	25	DQ32
DQ31	106	26	DQ30
DQ29	107	27	DQ28
DQ27	108	28	DQ26
DQ25	109	29	DQ24
V_{SS}	110	30	V_{SS}
NC	111	31	NC
DQ23	112	32	DQ22
DQ21	113	33	DQ20
$V_{CC}5$	114	34	$V_{CC}3$
DQ19	115	35	DQ18
V_{SS}	116	36	V_{SS}
DQ17	117	37	DQ16
$V_{CC}5$	118	38	$V_{CC}3$
DQ15	119	39	DQ14
DQ13	120	40	DQ12
V_{SS}	121	41	V_{SS}
DQ11	122	42	DQ10
$V_{CC}5$	123	43	$V_{CC}3$
DQ9	124	44	DQ8
NC	125	45	NC
$V_{CC}5$	126	46	$V_{CC}3$
DQ7	127	47	DQ6
DQ5	128	48	DQ4
DQ3	129	49	DQ2
DQ1	130	50	DQ0
V_{SS}	131	51	V_{SS}
NC	132	52	NC
NC	133	53	NC
NC	134	54	A5
NC	135	55	A6
A7	136	56	A8
V_{SS}	137	57	V_{SS}
A9	138	58	A10
A11	139	59	A12
A13	140	60	A14
A15	141	61	A16
A17	142	62	NC
V_{SS}	143	63	V_{SS}
NC	144	64	PD0
PD1	145	65	PD2
K	146	66	NC
NC	147	67	NC
V_{SS}	148	68	V_{SS}
$\overline{W7}$	149	69	$\overline{W6}$
$\overline{W5}$	150	70	$\overline{W4}$
$\overline{W3}$	151	71	$\overline{W2}$
$\overline{W1}$	152	72	$\overline{W0}$
V_{SS}	153	73	V_{SS}
A3 – 1	154	74	A3 – 0
$\overline{E1}$	155	75	$\overline{E0}$
A4 – 1	156	76	A4 – 0
$\overline{G1}$	157	77	$\overline{G0}$
$V_{CC}5$	158	78	$V_{CC}3$
NC	159	79	NC
V_{SS}	160	80	V_{SS}

Cache Size and Functionality	Module	PD2	PD1	PD0
256KAsync	MCM64AG32	NC	V_{SS}	NC
256K Burst	—	V_{SS}	V_{SS}	NC
512K Burst	—	V_{SS}	V_{SS}	V_{SS}

PIN NAMES	
A3–0 – A4–0	Address Inputs
A3–1 – A4–1	Address Inputs
A5 – A19	Address Inputs
K	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write Enable
$\overline{E0}$ – $\overline{E1}$	Module Enable
$\overline{G0}$ – $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
PD0 – PD2	Presence Detect
$V_{CC}3$	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connect

For proper operation of the device, V_{SS} must be connected to the ground.
$V_{CC}5$ does not need to be wired to module.

MCM64AG32 BLOCK DIAGRAM

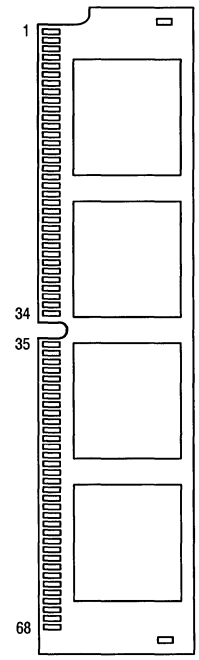


6

256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™

MCM72BA32
MCM72BA64

136–LEAD DIMM
CASE 1104–01
TOP VIEW



The MCM72BA32SG and MCM72BA64SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 136 pin dual readout single inline memory module (DIMM). The module uses four of Motorola's MCM67B518 or MCM67B618 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board TAG.

PD0 – PD2 are reserved for density and speed identification.

- Pentium–style Burst Counter on Board
- Dual Readout SIMM for Circuit Density
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz, 60 MHz, 50MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible

6

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

REV 2
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PIN ASSIGNMENT
136–LEAD DIMM
TOP VIEW

PD0	1	69	V_{SS}
PD1	2	70	PD2
DQ0	3	71	V_{CC}
DQ1	4	72	DQ2
V_{CC}	5	73	DQ3
DQ4	6	74	DQ5
DQ6	7	75	DQ7
DQP0	8	76	V_{SS}
DQ8	9	77	DQ9
DQ10	10	78	DQ11
V_{SS}	11	79	DQ12
K0	12	80	V_{SS}
V_{SS}	13	81	DQ13
DQ14	14	82	DQ15
V_{CC}	15	83	DQP1
DQ16	16	84	V_{SS}
DQ17	17	85	DQ18
DQ19	18	86	DQ20
DQ21	19	87	DQ22
V_{CC}	20	88	DQ23
DQP2	21	89	V_{SS}
DQ24	22	90	DQ25
DQ26	23	91	DQ27
DQ28	24	92	DQ29
V_{SS}	25	93	DQ30
DQ31	26	94	V_{SS}
DQP3	27	95	$\overline{E0}$
V_{SS}	28	96	$\overline{W1}$
$\overline{W0}$	29	97	$\overline{W3}$
$\overline{W2}$	30	98	$\overline{G0}$
$\overline{ADSP}$	31	99	$\overline{ADSC}$
$\overline{ADV}$	32	100	V_{SS}
V_{CC}	33	101	$\overline{G1}$
$\overline{W4}$	34	102	$\overline{W5}$
$\overline{W6}$	35	103	$\overline{W7}$
DQ32	36	104	$\overline{E1}$
DQ33	37	105	DQ34
V_{SS}	38	106	DQ35
DQ36	39	107	DQ37
DQ38	40	108	V_{CC}
DQ39	41	109	DQP4
DQ40	42	110	DQ41
V_{CC}	43	111	DQ42
DQ43	44	112	DQ44
DQ45	45	113	V_{SS}
DQ46	46	114	DQ47
DQP5	47	115	DQ48
V_{SS}	48	116	DQ49
K1	49	117	V_{SS}
V_{SS}	50	118	DQ50
DQ52	51	119	DQ51
DQ53	52	120	DQ54
DQ55	53	121	DQ56
DQP6	54	122	V_{SS}
V_{CC}	55	123	DQ57
DQ58	56	124	DQ59
DQ60	57	125	DQ61
DQ62	58	126	DQ63
DQP7	59	127	V_{CC}
A0	60	128	A1
A2	61	129	A3
A4	62	130	A5
A6	63	131	A7
A8	64	132	NC
A10	65	133	A9
A12	66	134	A11
A14	67	135	A13
V_{SS}	68	136	A15*

PD2	PD1	PD0	Cache Size	Module
V_{SS}	NC	NC	512KB	72BA64SG66/60
V_{SS}	NC	V_{SS}	512KB	72BA64SG50
V_{SS}	V_{SS}	NC	256KB	72BA32SG66/60
V_{SS}	V_{SS}	V_{SS}	256KB	72BA32SG50

PIN NAMES

A0 – A15	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{ADV}$	Burst Advance
PD0 – PD2	Presence Detect
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

* This pin on the MCM72BA32 is a No Connect (NC)

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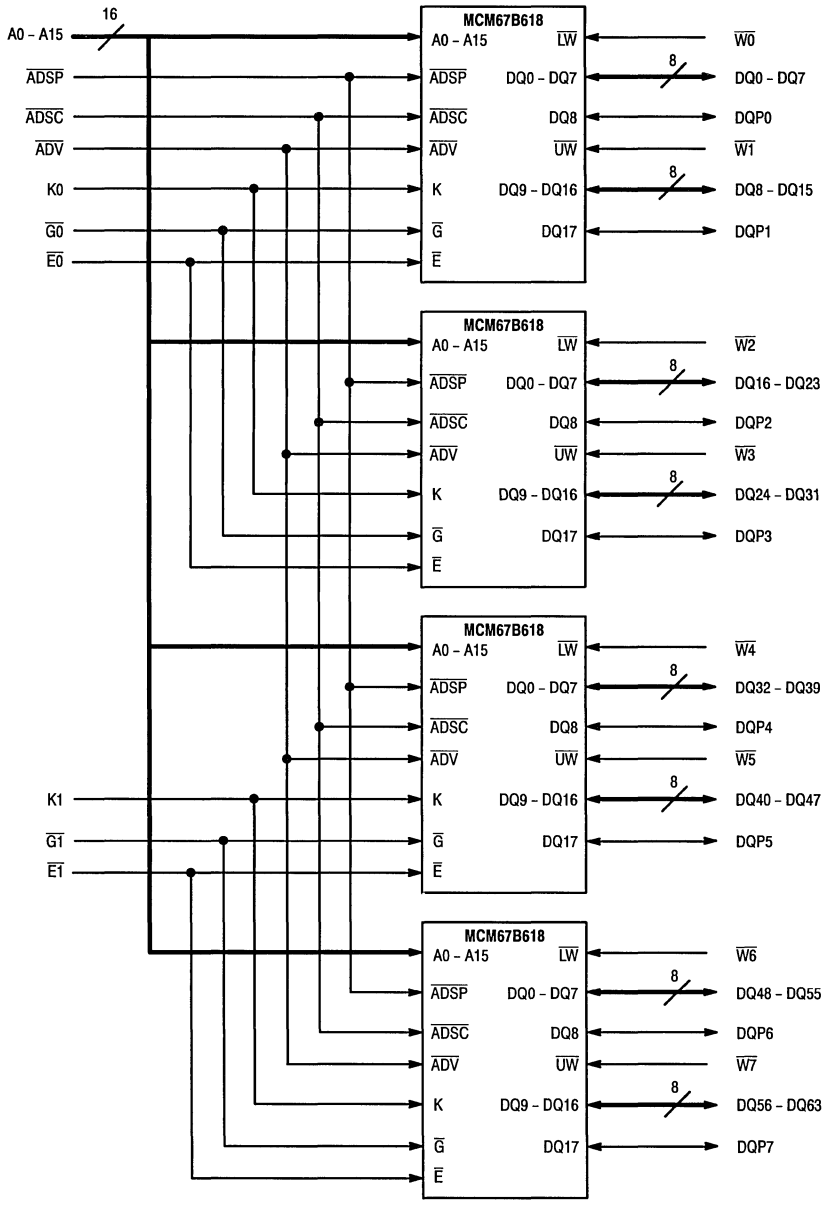
64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



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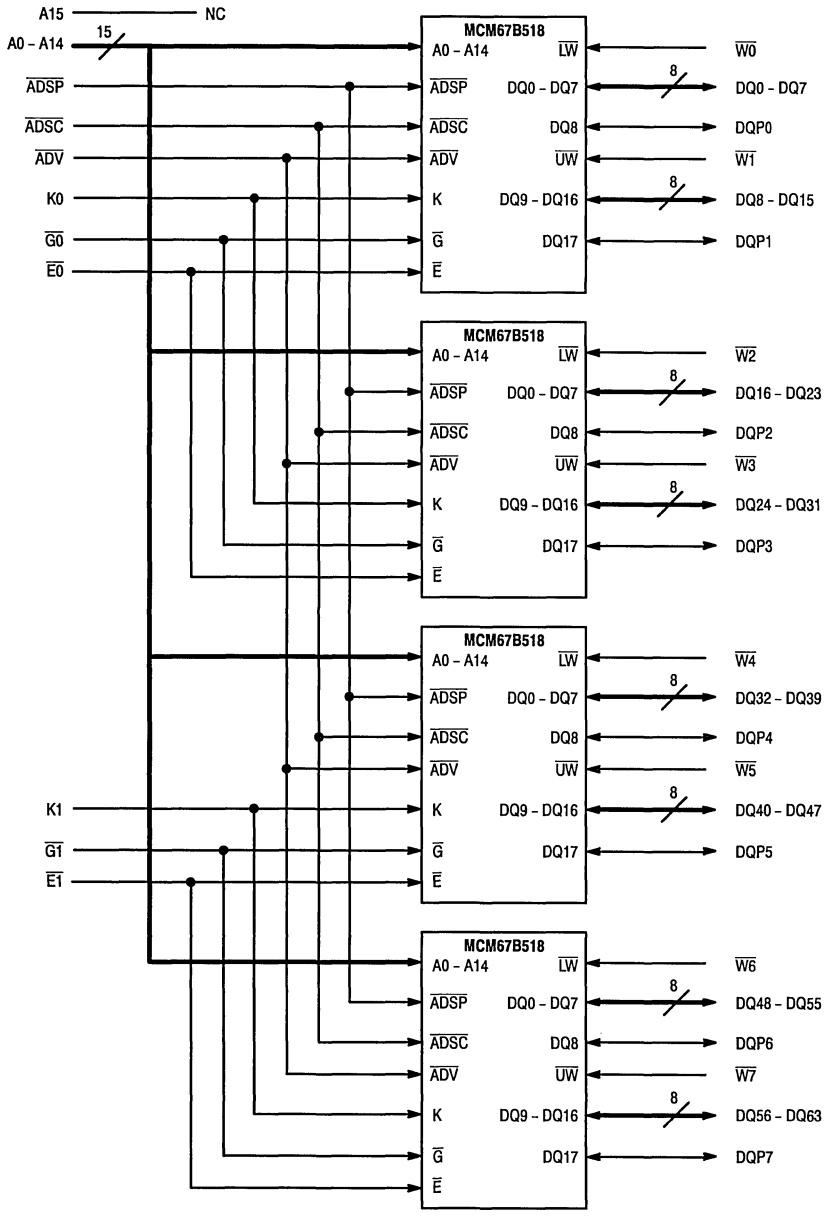
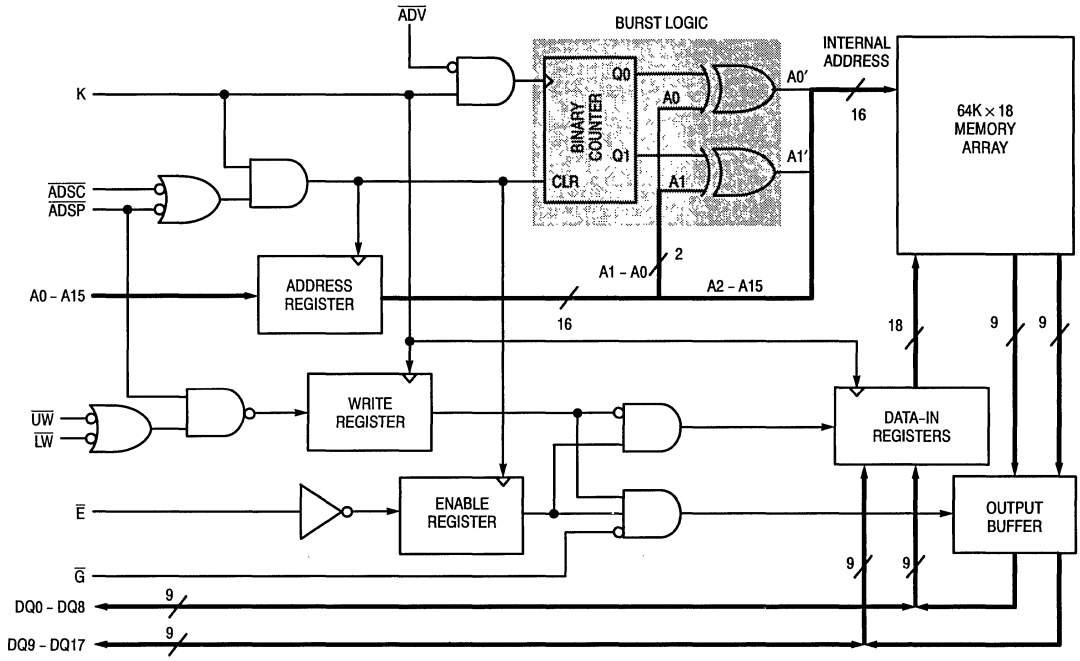
32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



6

MCM67B618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66} I_{CCA60} I_{CCA50}	—	1100 1100 1000	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	300	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	(A0 – A15, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$)	C_{in}	25	32	pF
Input/Output Capacitance	(DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	10	pF
Input Capacitance	(Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	12	15	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{Wx}$ refers to any or all byte write enables)

Parameter	Symbol	MCM72BA64SG66		MCM72BA64SG60		MCM72BA64SG50		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.7	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	2	6	2	7	ns	5
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	6
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible Pentium external bus cycles.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

6

AC TEST LOADS

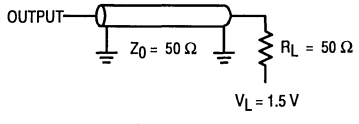


Figure 1A

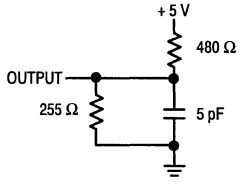
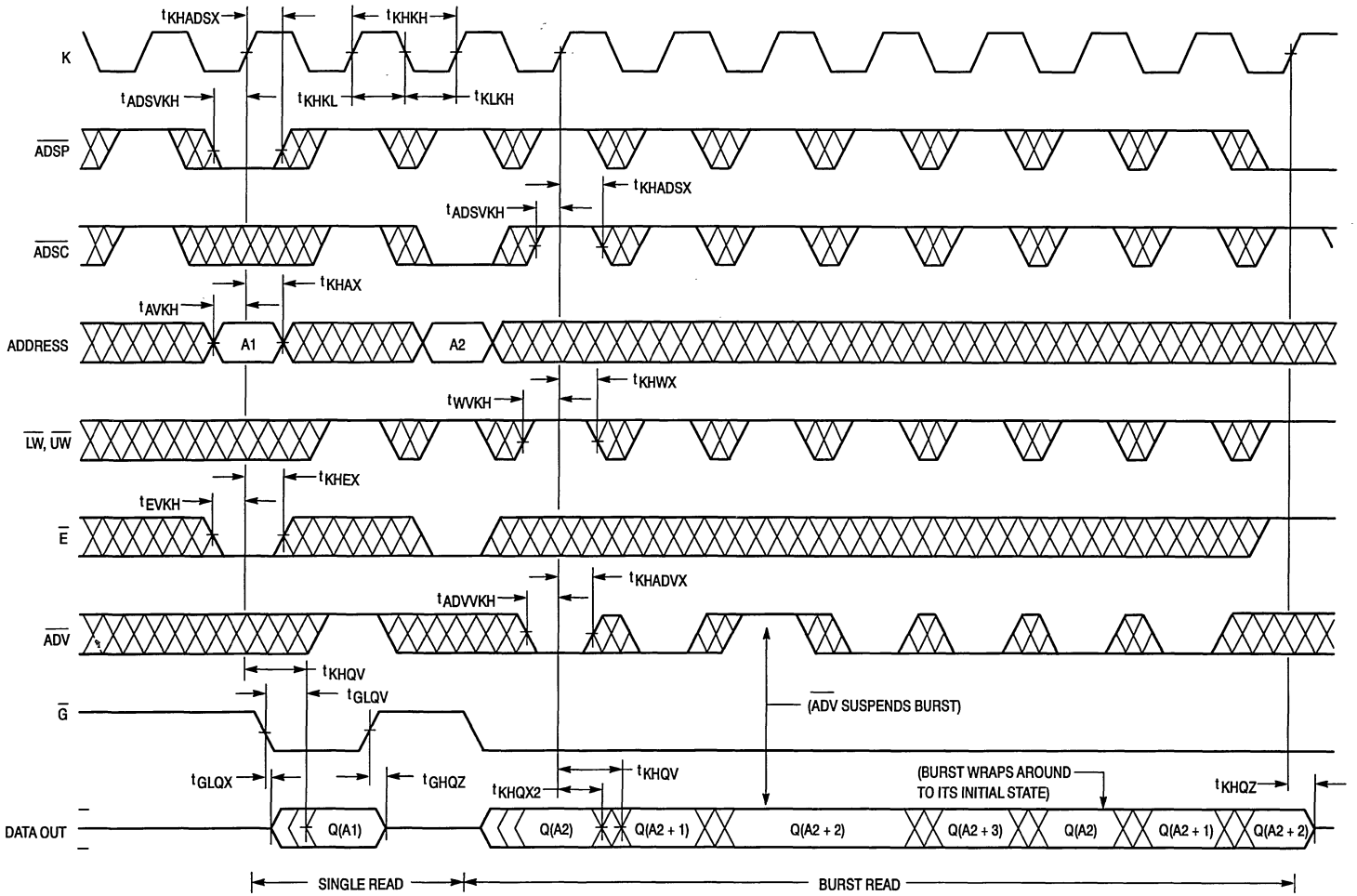


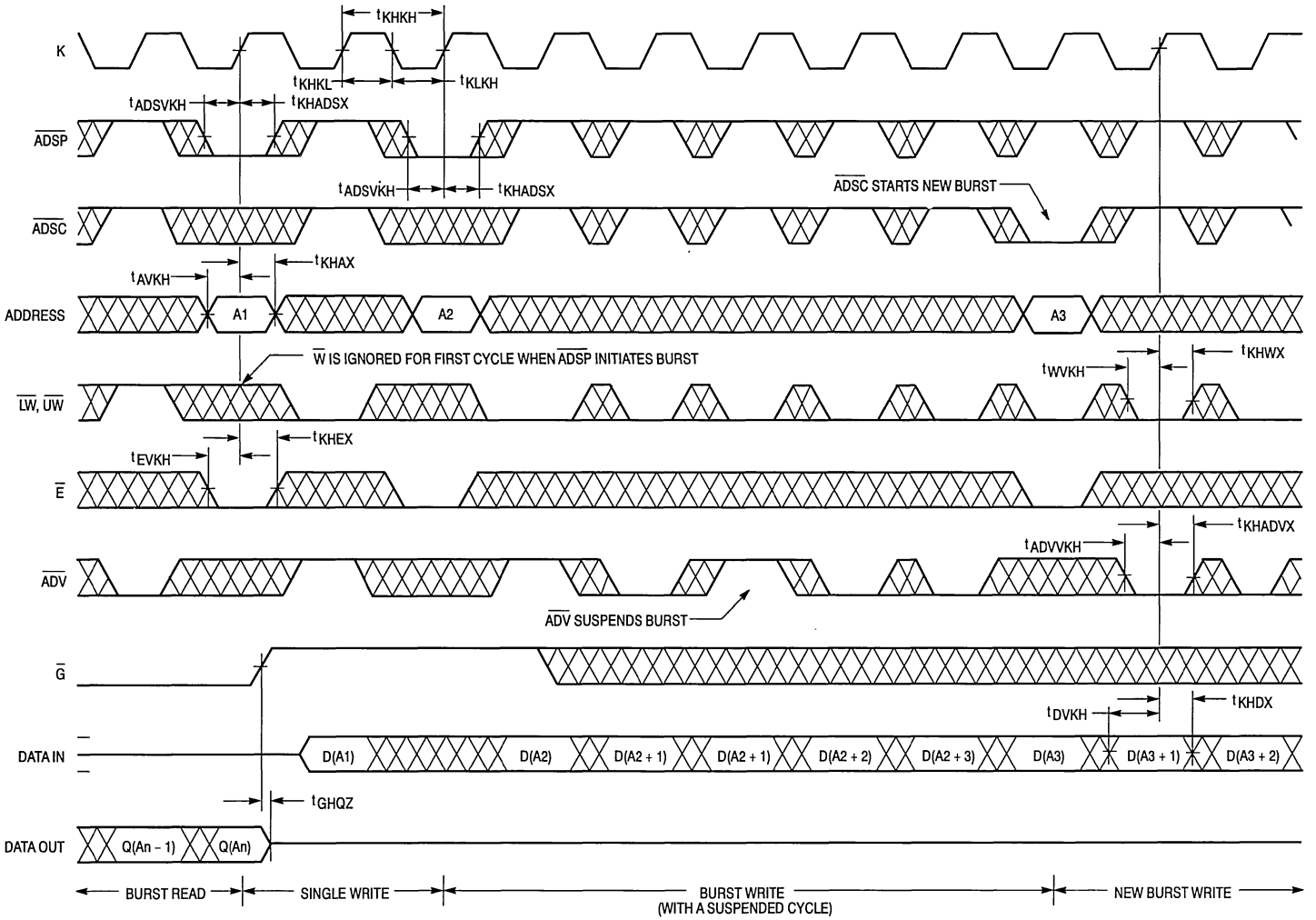
Figure 1B

READ CYCLES

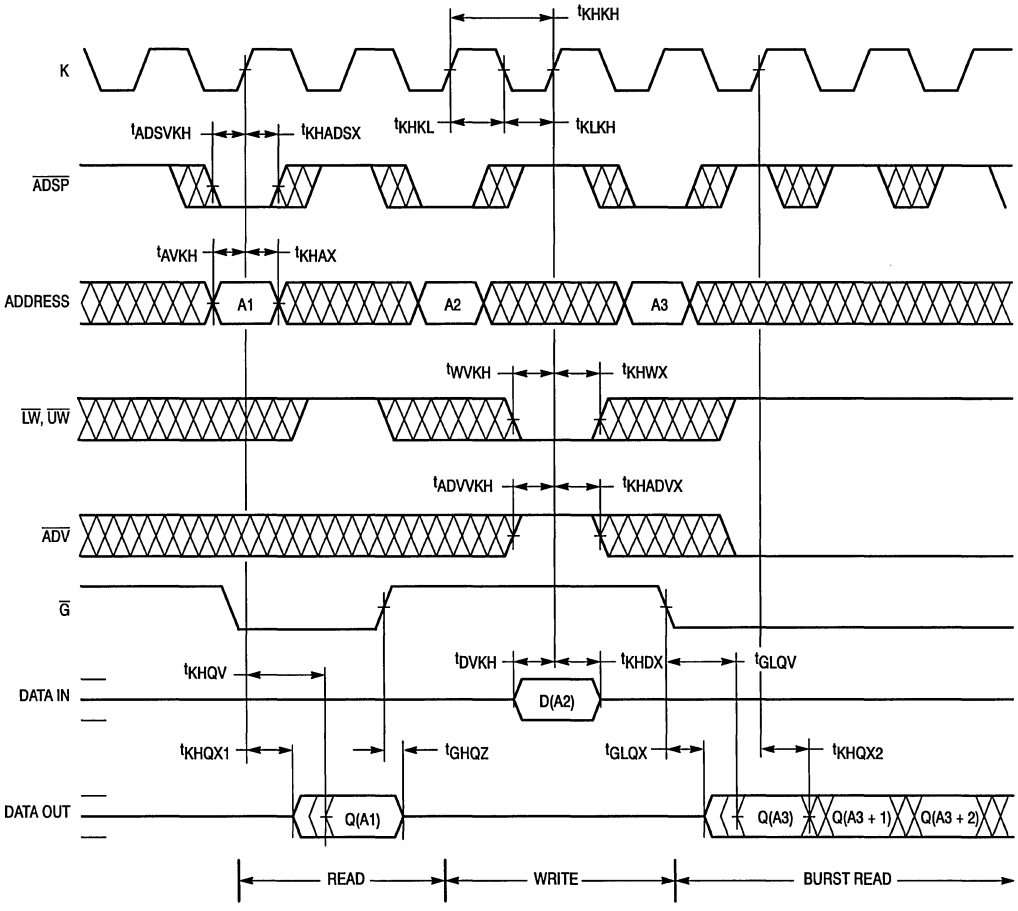


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE



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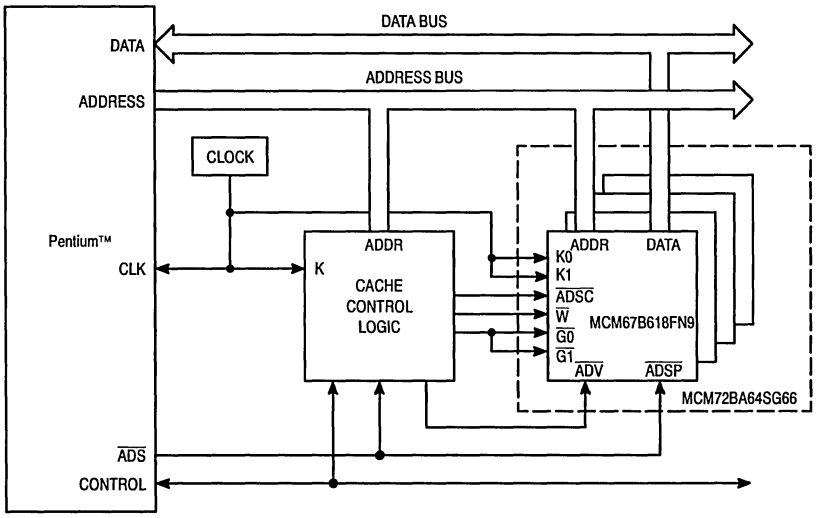
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72BA64SG66 with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72BA32 72BA64	XX	XX
Motorola Memory Prefix				
Part Number				
Speed (66 = 66 MHz, 60 = 60 MHz, 50 = 50 MHz)				
Package (SG = Gold Pad SIMM)				

Full Part Numbers —			
	MCM72BA32SG66	MCM72BA32SG60	MCM72BA32SG50
	MCM72BA64SG66	MCM72BA64SG60	MCM72BA64SG50

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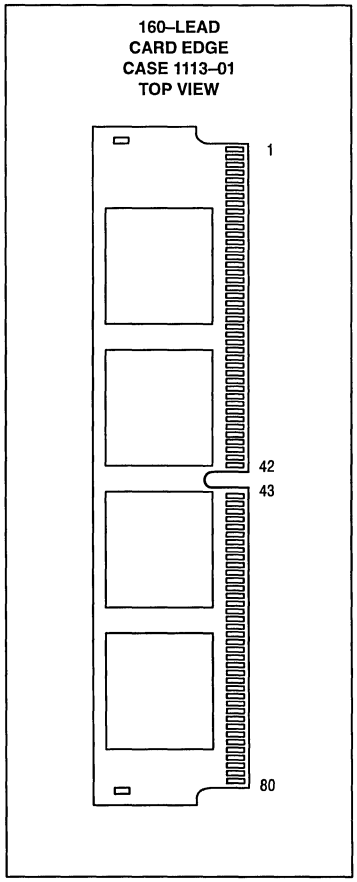
256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™

MCM72BB32
MCM72BB64



The MCM72BB32SG and MCM72BB64SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 160 pin card edge memory module. Each module uses four of Motorola's MCM67B518 or MCM67B618 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board tag.

PD0 – PD2 are reserved for density identification.

- Pentium–style Burst Counter on Board
- 160 Pin Card Edge Module
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz, 60 MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible
- Burndy Connector, Part Number: CELP2X80SC3Z48

6

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

REV 1
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PIN ASSIGNMENT
160–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
DQ63	82	2	DQ62
$V_{CC}5$	83	3	$V_{CC}3$*
DQ61	84	4	DQ60
$V_{CC}5$	85	5	$V_{CC}3$*
DQ59	86	6	DQ58
DQ57	87	7	DQ56
V_{SS}	88	8	V_{SS}
DQP7	89	9	DQP6
DQ55	90	10	DQ54
DQ53	91	11	DQ52
DQ51	92	12	DQ50
V_{SS}	93	13	V_{SS}
DQ49	94	14	DQ48
DQ47	95	15	DQ46
DQ45	96	16	DQ44
DQ43	97	17	DQ42
V_{SS}	98	18	V_{SS}
DQ41	99	19	DQ40
DQP5	100	20	DQP4
DQ39	101	21	DQ38
DQ37	102	22	DQ36
DQ35	103	23	DQ34
V_{SS}	104	24	V_{SS}
DQ33	105	25	DQ32
DQ31	106	26	DQ30
DQ29	107	27	DQ28
DQ27	108	28	DQ26
DQ25	109	29	DQ24
V_{SS}	110	30	V_{SS}
DQP3	111	31	DQP2
DQ23	112	32	DQ22
DQ21	113	33	DQ20
$V_{CC}5$	114	34	$V_{CC}3$*
DQ19	115	35	DQ18
V_{SS}	116	36	V_{SS}
DQ17	117	37	DQ16
$V_{CC}5$	118	38	$V_{CC}3$*
DQ15	119	39	DQ14
DQ13	120	40	DQ12
V_{SS}	121	41	V_{SS}
DQ11	122	42	DQ10
$V_{CC}5$	123	43	$V_{CC}3$*
DQ9	124	44	DQ8
DQP1	125	45	DQP0
$V_{CC}5$	126	46	$V_{CC}3$*
DQ7	127	47	DQ6
DQ5	128	48	DQ4
DQ3	129	49	DQ2
DQ1	130	50	DQ0
V_{SS}	131	51	V_{SS}
A3B	132	52	A3A
A4B	133	53	A4A
A5B	134	54	A5A
A6B	135	55	A6A
A7	136	56	A8
V_{SS}	137	57	V_{SS}
A9	138	58	A10
A11	139	59	A12
A13	140	60	A14
A15	141	61	A16
A17	142	62	A18**
V_{SS}	143	63	V_{SS}
*A19	144	64	PD0
PD1	145	65	PD2
K0	146	66	K1
*K2	147	67	K3*
V_{SS}	148	68	V_{SS}
$\overline{W7}$	149	69	$\overline{W6}$
$\overline{W5}$	150	70	$\overline{W4}$
$\overline{W3}$	151	71	$\overline{W2}$
$\overline{W1}$	152	72	$\overline{W0}$
V_{SS}	153	73	V_{SS}
$\overline{ADSC1}$	154	74	$\overline{ADSC0}$
$\overline{E1}$	155	75	$\overline{E0}$
$\overline{ADV1}$	156	76	$\overline{ADV0}$
$\overline{G1}$	157	77	$\overline{G0}$
$V_{CC}5$	158	78	$V_{CC}3$*
$\overline{ADSP1}$	159	79	$\overline{ADSP0}$
V_{SS}	160	80	V_{SS}

PD2	PD1	PD0	Cache Size	Module
V_{SS}	V_{SS}	NC	256KB	72BB32SG
V_{SS}	V_{SS}	V_{SS}	512KB	72BB64SG

PIN NAMES

A3 – A18	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{ADSC0}$, $\overline{ADSC1}$	Controller Address Status
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Status
$\overline{ADV0}$, $\overline{ADV1}$	Burst Advance
PD0 – PD2	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
V_{SS}	Ground

* No Connect for MCM72BB32/MCM72BB64
** No Connect for MCM72BB32

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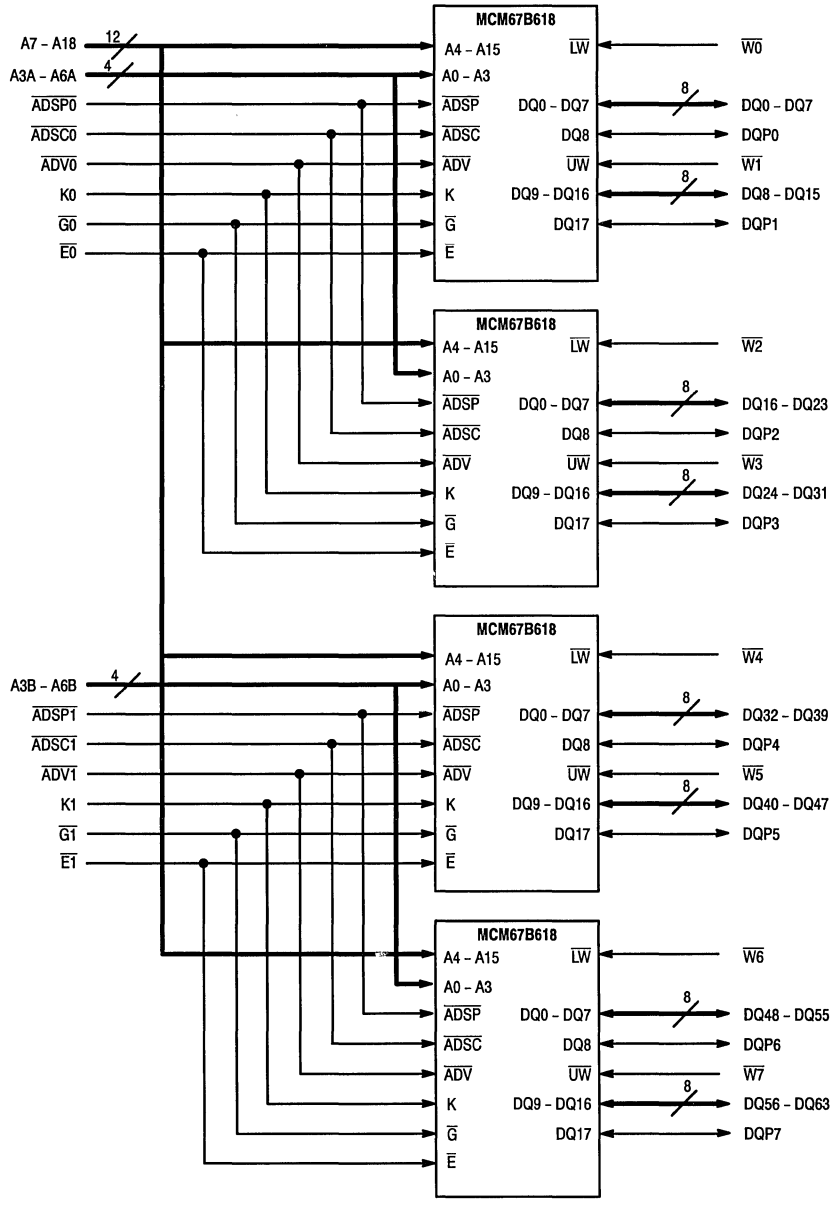
64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



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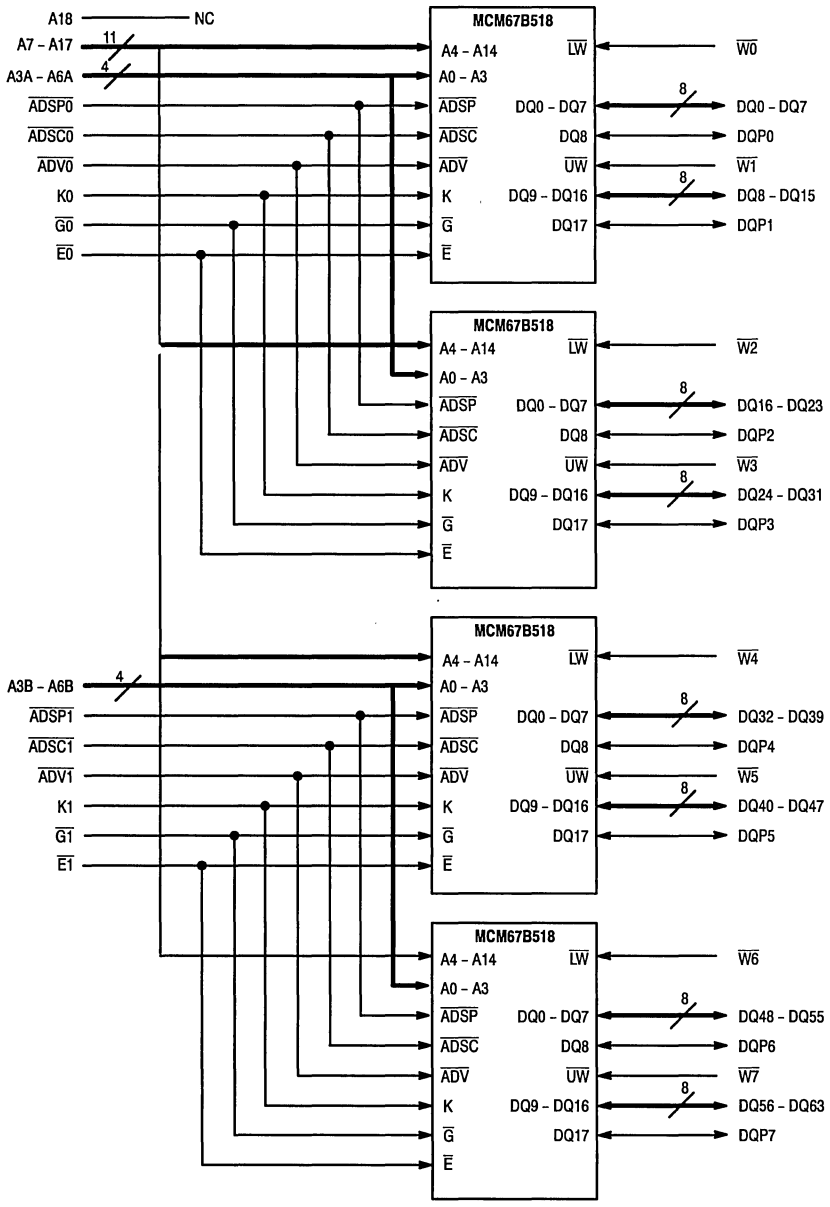
32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



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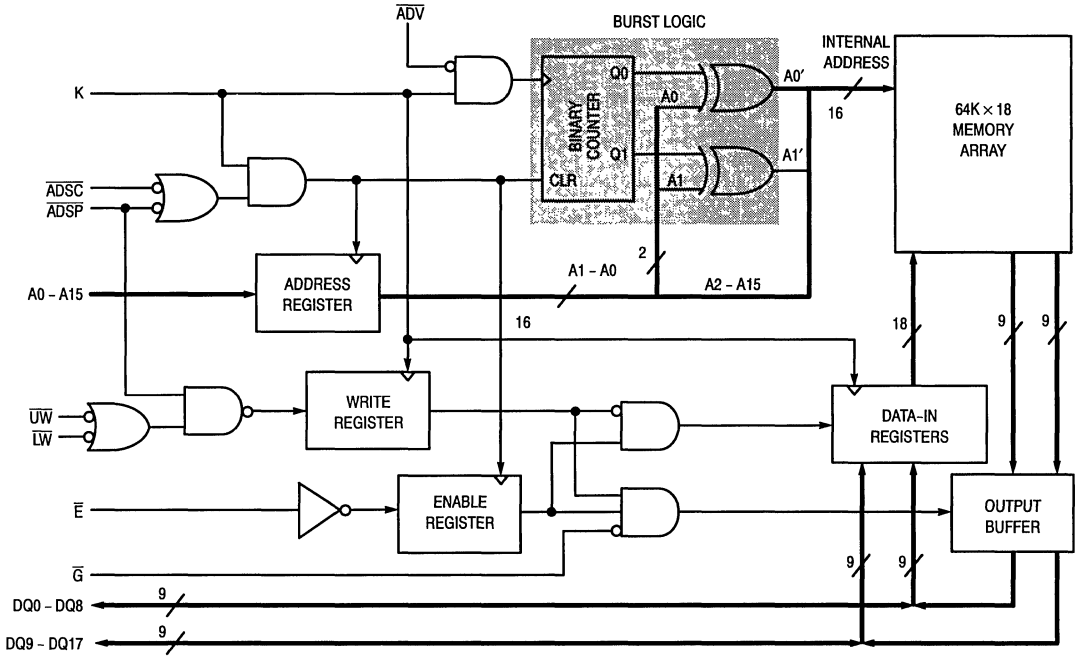
MCM67B618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66} I_{CCA60}	—	1100 1060	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	380	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(A7 – A18)	C_{in}	20	pF
Input Capacitance	(A3x – A6x, $\overline{ADSPx}$, $\overline{ADSCx}$, $\overline{ADVx}$, Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	10	pF
Input/Output Capacitance	(DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{Wx}$ refers to any or all byte write enables)

Parameter	Symbol	MCM72BB64SG66		MCM72BB64SG60		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.7	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	2	6	ns	5
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	ns	6
Address Status	t_{ADSVKH}						
Data In	t_{DVKH}						
Write	t_{WVKH}						
Address Advance	t_{ADVVKH}						
Chip Enable	t_{EVKH}						
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}						
Data In	t_{KHDX}						
Write	t_{KHWX}						
Address Advance	t_{KHADVX}						
Chip Enable	t_{KHEX}						

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible Pentium external bus cycles.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

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AC TEST LOADS

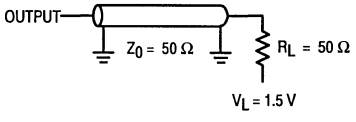


Figure 1A

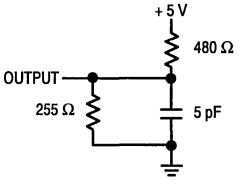
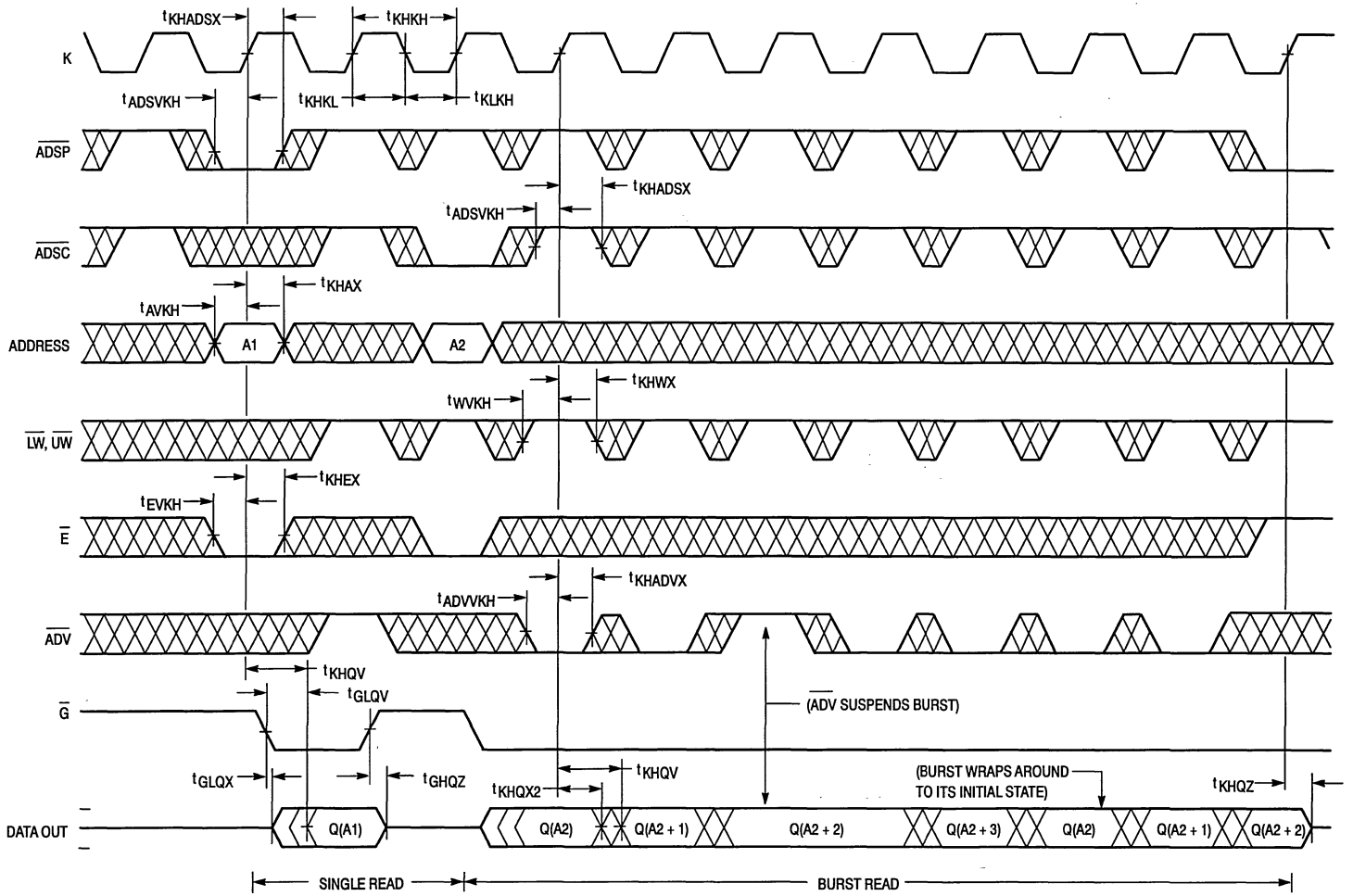


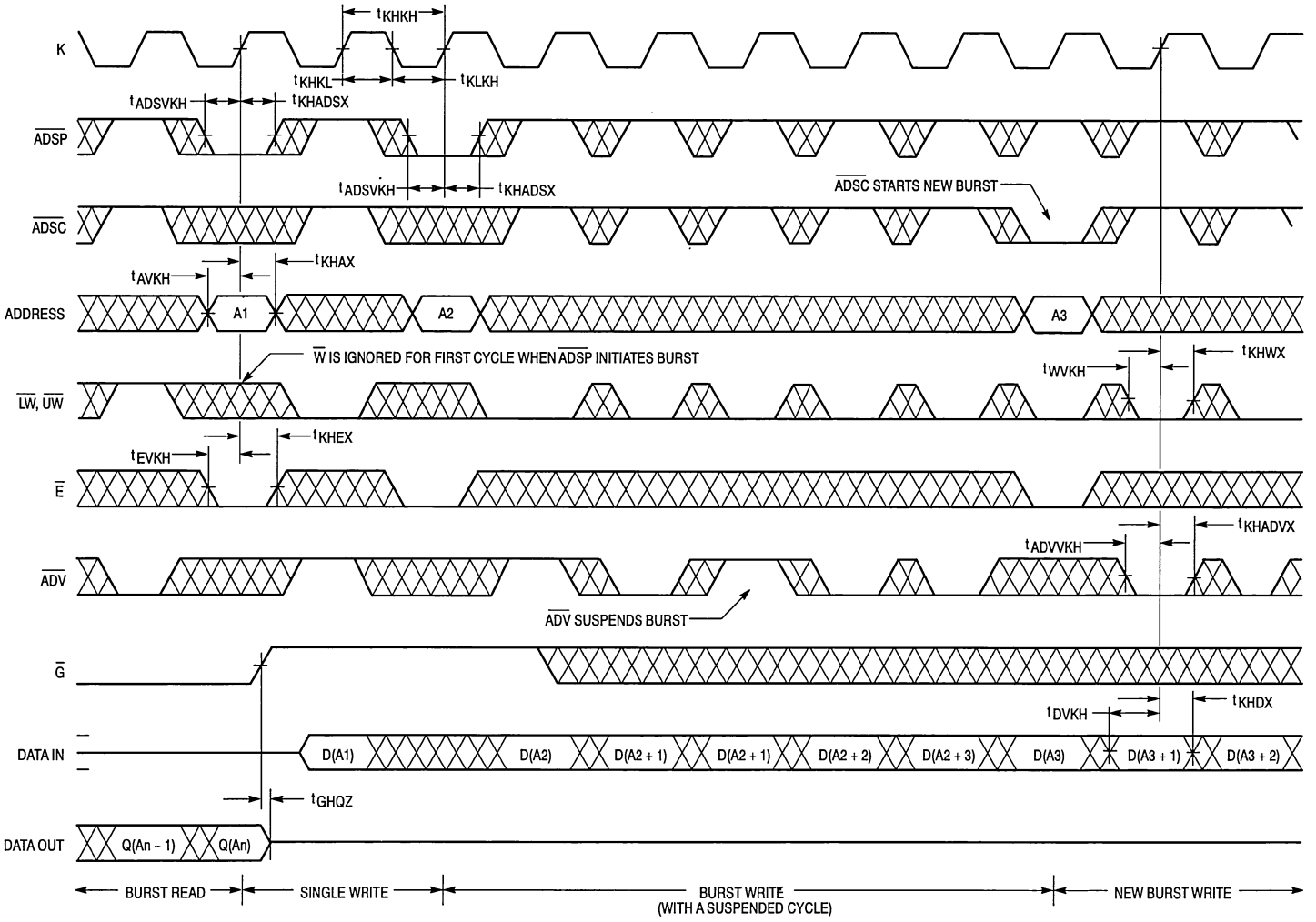
Figure 1B

READ CYCLES



NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



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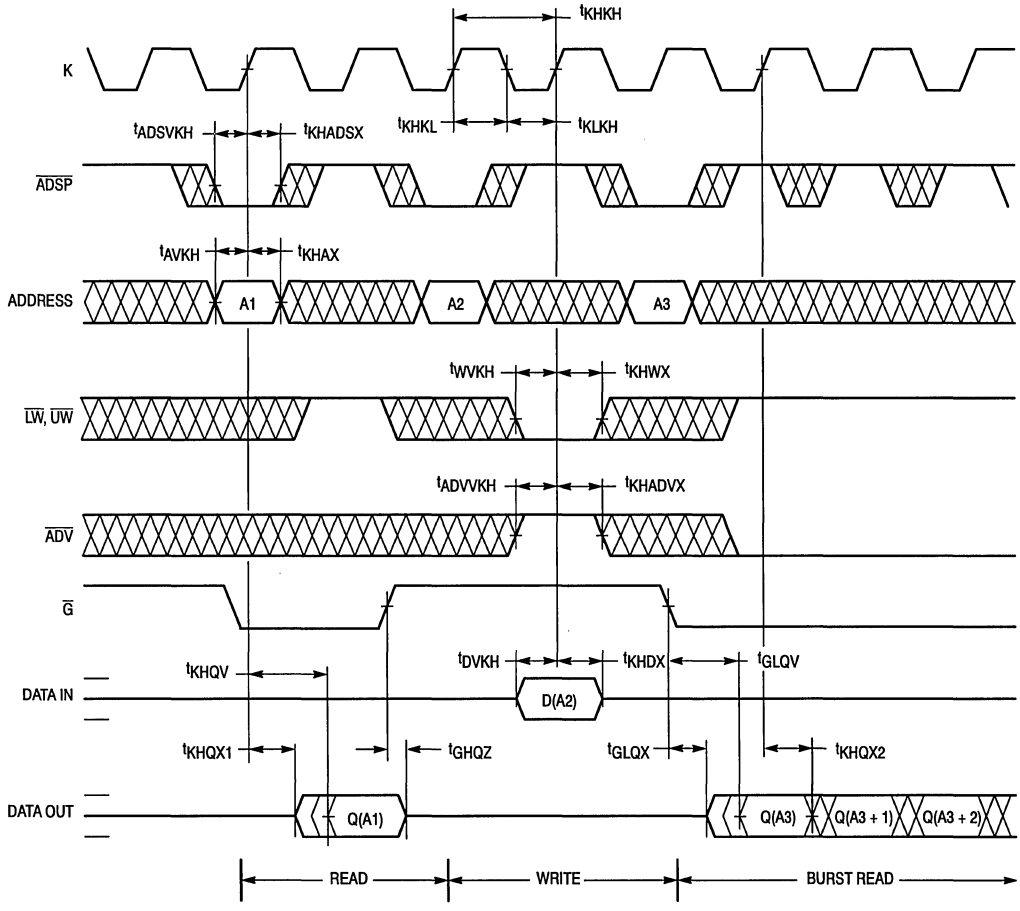
COMBINATION READ/WRITE CYCLE



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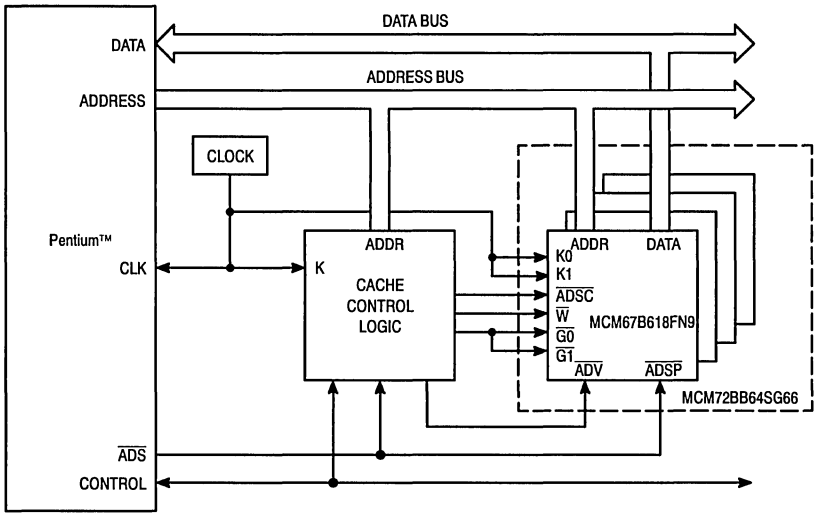
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72BB64SG66 with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72BB32 72BB64	XX	XX
	Motorola Memory Prefix			Speed (66 = 66 MHz, 60 = 60 MHz)
	Part Number			Package (SG = Gold Pad SIMM)

Full Part Numbers — MCM72BB32SG66 MCM72BB32SG60
MCM72BB64SG66 MCM72BB64SG60

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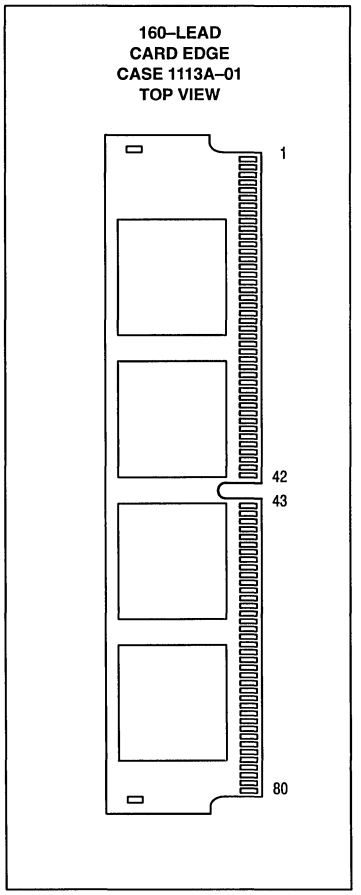
256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™

MCM72BF32
MCM72BF64



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Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

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- Three State Outputs
- Byte Parity, Byte Write Enables
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- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Series 20 Ω Resistors for Noise Immunity

6

BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

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PIN ASSIGNMENT
160–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
DQ63	82	2	DQ62
$V_{CC}5$	83	3	$V_{CC}3$*
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$V_{CC}5$	85	5	$V_{CC}3$*
DQ59	86	6	DQ58
DQ57	87	7	DQ56
V_{SS}	88	8	V_{SS}
DQP7	89	9	DQP6
DQ55	90	10	DQ54
DQ53	91	11	DQ52
DQ51	92	12	DQ50
V_{SS}	93	13	V_{SS}
DQ49	94	14	DQ48
DQ47	95	15	DQ46
DQ45	96	16	DQ44
DQ43	97	17	DQ42
V_{SS}	98	18	V_{SS}
DQ41	99	19	DQ40
DQP5	100	20	DQP4
DQ39	101	21	DQ38
DQ37	102	22	DQ36
DQ35	103	23	DQ34
V_{SS}	104	24	V_{SS}
DQ33	105	25	DQ32
DQ31	106	26	DQ30
DQ29	107	27	DQ28
DQ27	108	28	DQ26
DQ25	109	29	DQ24
V_{SS}	110	30	V_{SS}
DQP3	111	31	DQP2
DQ23	112	32	DQ22
DQ21	113	33	DQ20
$V_{CC}5$	114	34	$V_{CC}3$*
DQ19	115	35	DQ18
V_{SS}	116	36	V_{SS}
DQ17	117	37	DQ16
$V_{CC}5$	118	38	$V_{CC}3$*
DQ15	119	39	DQ14
DQ13	120	40	DQ12
V_{SS}	121	41	V_{SS}
DQ11	122	42	DQ10
$V_{CC}5$	123	43	$V_{CC}3$*
DQ9	124	44	DQ8
DQP1	125	45	DQP0
$V_{CC}5$	126	46	$V_{CC}3$*
DQ7	127	47	DQ6
DQ5	128	48	DQ4
DQ3	129	49	DQ2
DQ1	130	50	DQ0
V_{SS}	131	51	V_{SS}
A3B	132	52	A3A
A4B	133	53	A4A
A5B	134	54	A5A
A6B	135	55	A6A
A7	136	56	A8
V_{SS}	137	57	V_{SS}
A9	138	58	A10
A11	139	59	A12
A13	140	60	A14
A15	141	61	A16
A17	142	62	A18**
V_{SS}	143	63	V_{SS}
*A19	144	64	PD0
PD1	145	65	PD2
K0	146	66	K1
*K2	147	67	K3*
V_{SS}	148	68	V_{SS}
$\overline{W7}$	149	69	$\overline{W6}$
$\overline{W5}$	150	70	$\overline{W4}$
$\overline{W3}$	151	71	$\overline{W2}$
$\overline{W1}$	152	72	$\overline{W0}$
V_{SS}	153	73	V_{SS}
$\overline{ADSC1}$	154	74	$\overline{ADSC0}$
$\overline{E1}$	155	75	$\overline{E0}$
$\overline{ADV1}$	156	76	$\overline{ADV0}$
$\overline{G1}$	157	77	$\overline{G0}$
$V_{CC}5$	158	78	$V_{CC}3$*
$\overline{ADSP1}$	159	79	$\overline{ADSP0}$
V_{SS}	160	80	V_{SS}

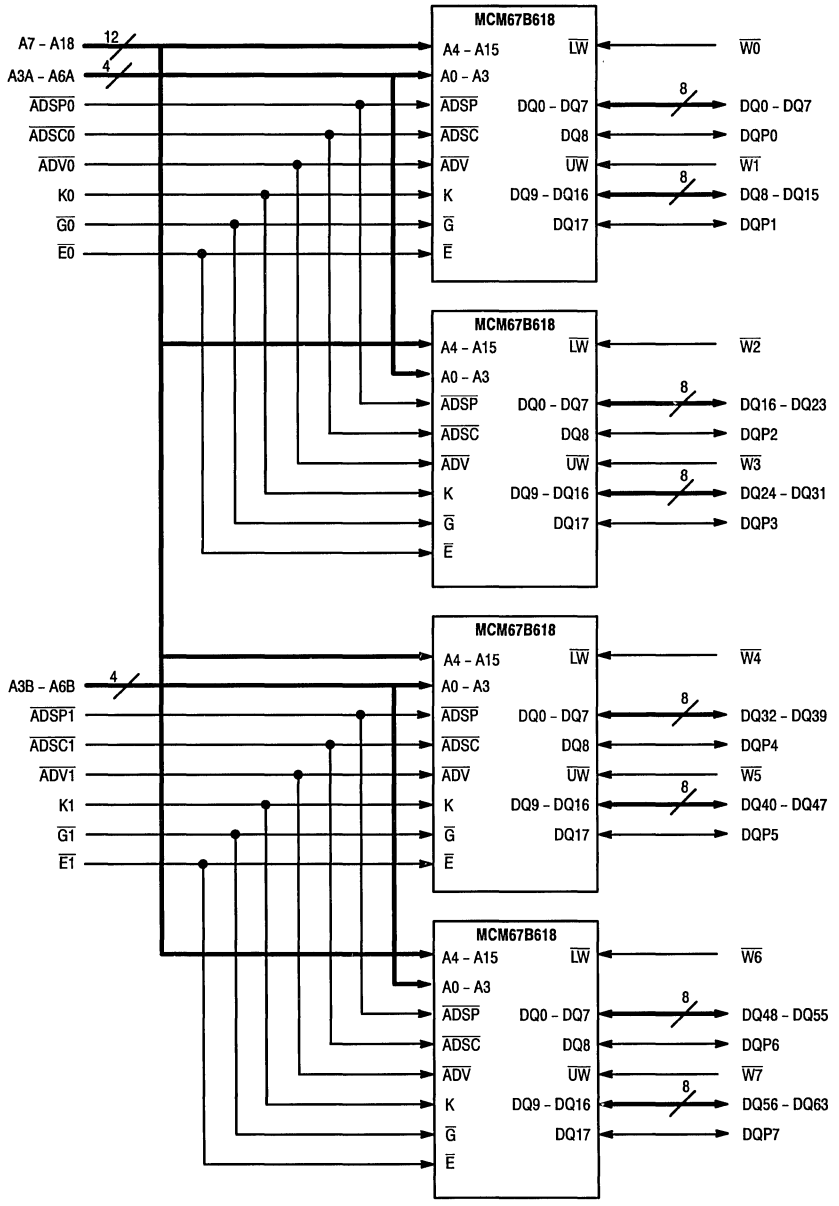
PD2	PD1	PD0	Cache Size	Module
V_{SS}	V_{SS}	NC	256KB	72BF32SG
V_{SS}	V_{SS}	V_{SS}	512KB	72BF64SG

PIN NAMES	
A3 – A18	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
$\overline{DQP0}$ – $\overline{DQP7}$	Data Parity Input/Output
$\overline{ADSC0}$, $\overline{ADSC1}$	Controller Address Status
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Status
$\overline{ADV0}$, $\overline{ADV1}$	Burst Advance
PD0 – PD2	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
$V_{CC}3$	+ 3.3 V Power Supply
V_{SS}	Ground

* No Connect for MCM72BF32/MCM72BF64
** No Connect for MCM72BF32

6

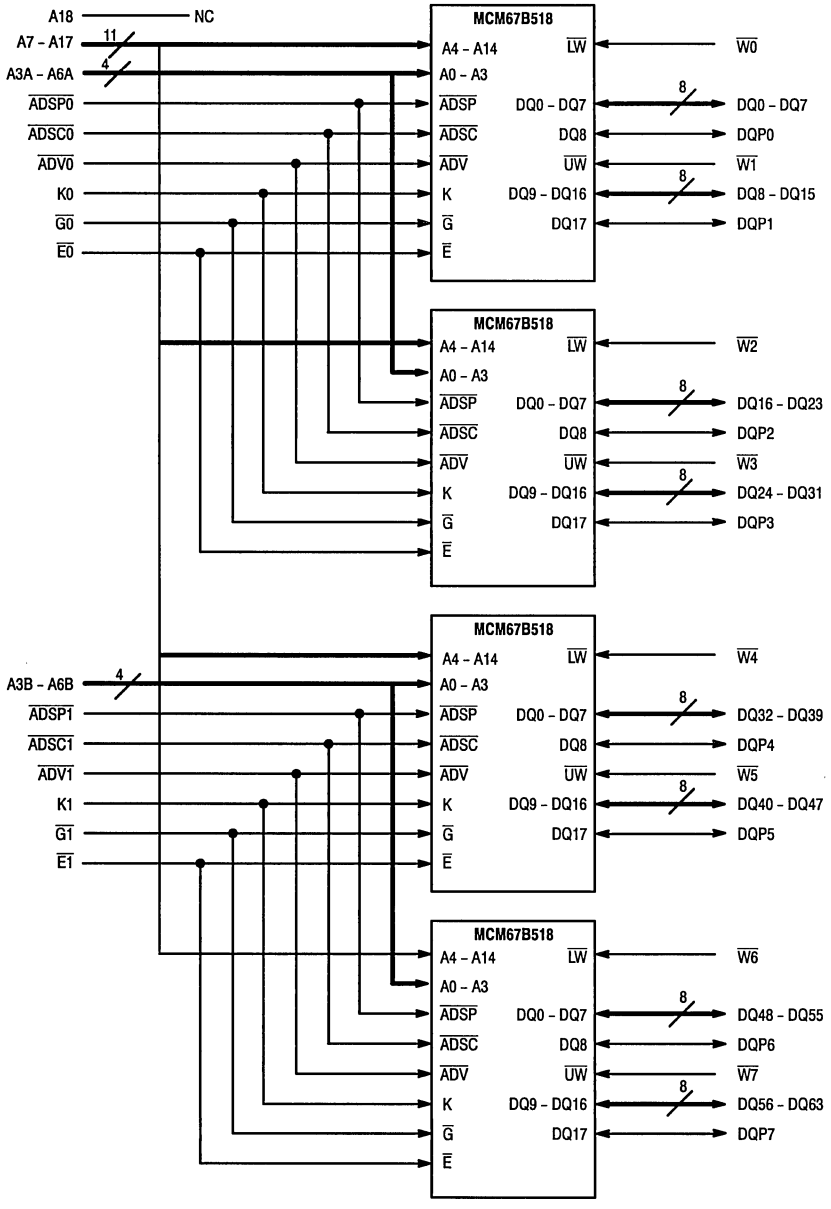
64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



DQ0 – DQ63 and DQP0 – DQP7 have 20 Ω series termination resistors.

6

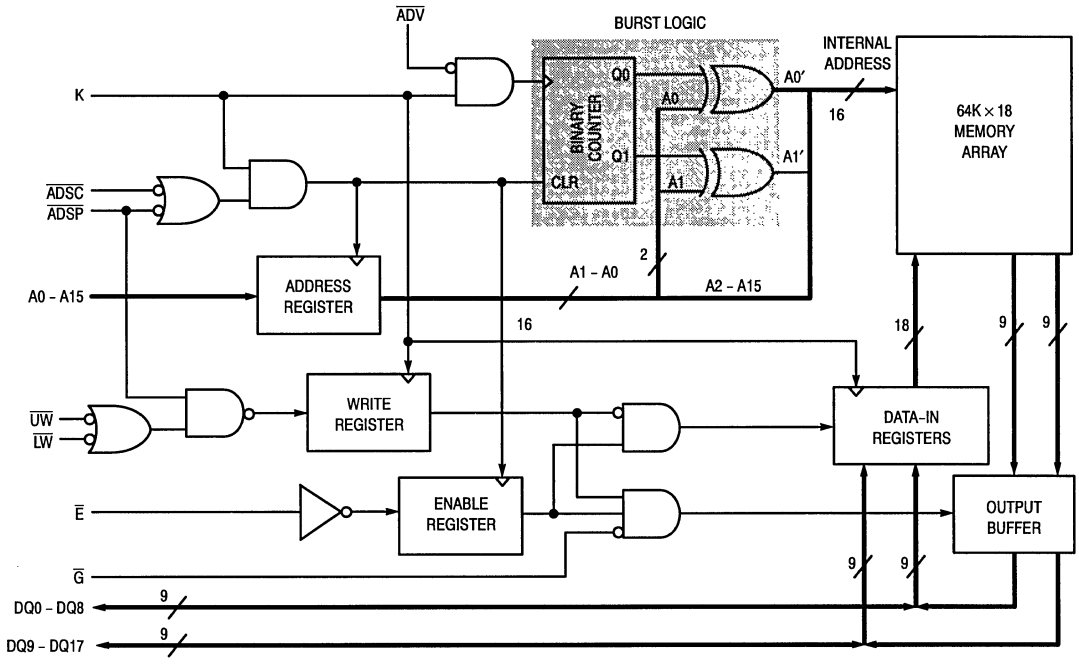
32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



DQ0 - DQ63 and DQP0 - DQP7 have 20 Ω series termination resistors.

6

MCM67B618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66} I_{CCA60}	—	1100 1060	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	380	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(A7 – A18)	C_{in}	20	pF
Input Capacitance	(A3x – A6x, $\overline{ADSPx}$, $\overline{ADSCx}$, $\overline{ADVx}$, Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	10	pF
Input/Output Capacitance	(DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{Wx}$ refers to any or all byte write enables)

Parameter	Symbol	MCM72BF64SG66		MCM72BF64SG60		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.7	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	2	6	ns	5
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	ns	6
Address Status	t_{ADSVKH}						
Data In	t_{DVKH}						
Write	t_{WVKH}						
Address Advance	t_{ADVVKH}						
Chip Enable	t_{EVKH}						
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}						
Data In	t_{KHDX}						
Write	t_{KHWX}						
Address Advance	t_{KHADVX}						
Chip Enable	t_{KHEX}						

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible Pentium external bus cycles.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

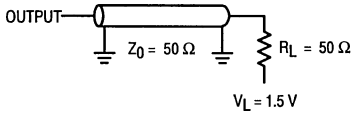


Figure 1A

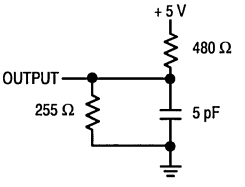
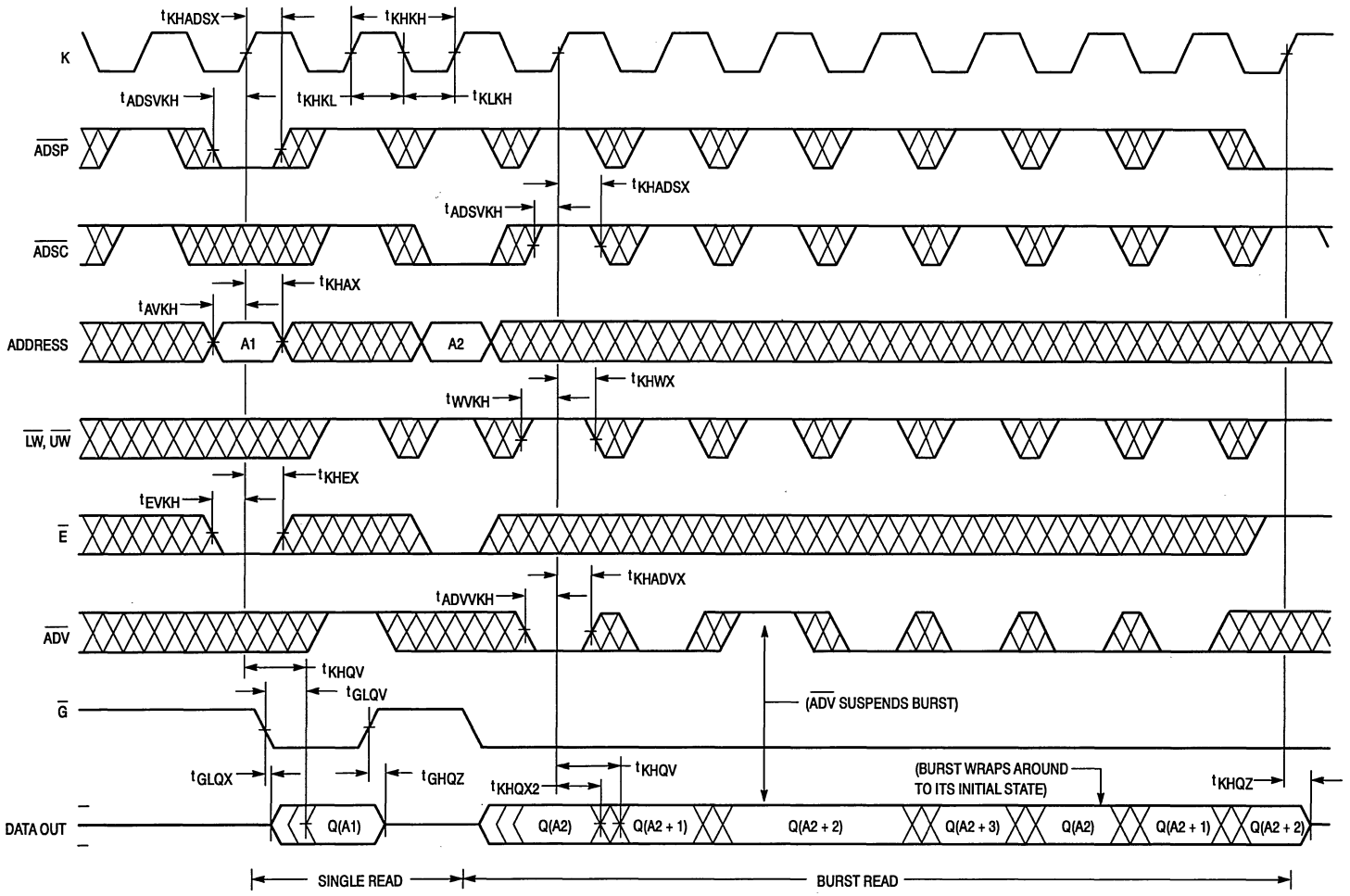


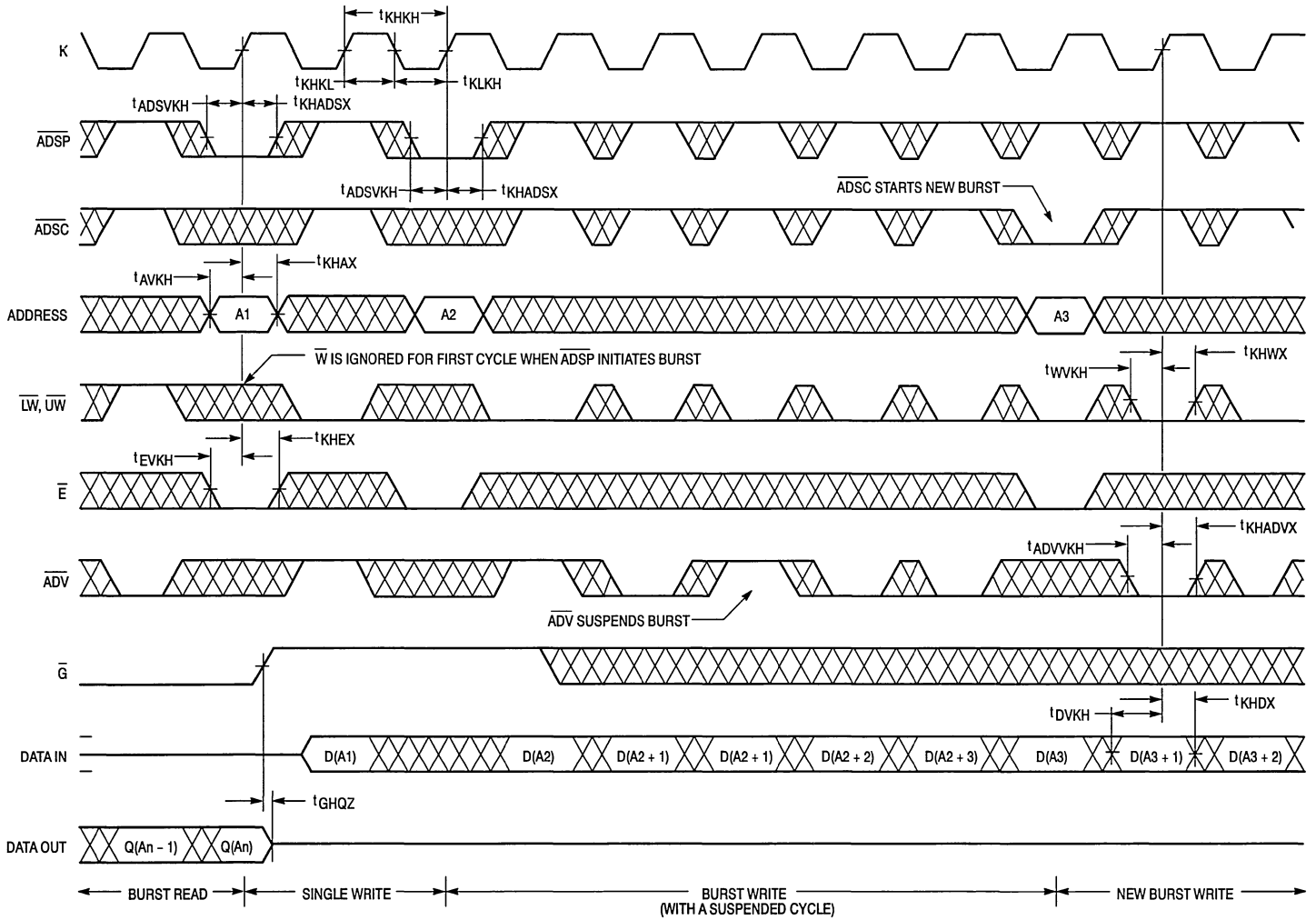
Figure 1B

READ CYCLES



NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



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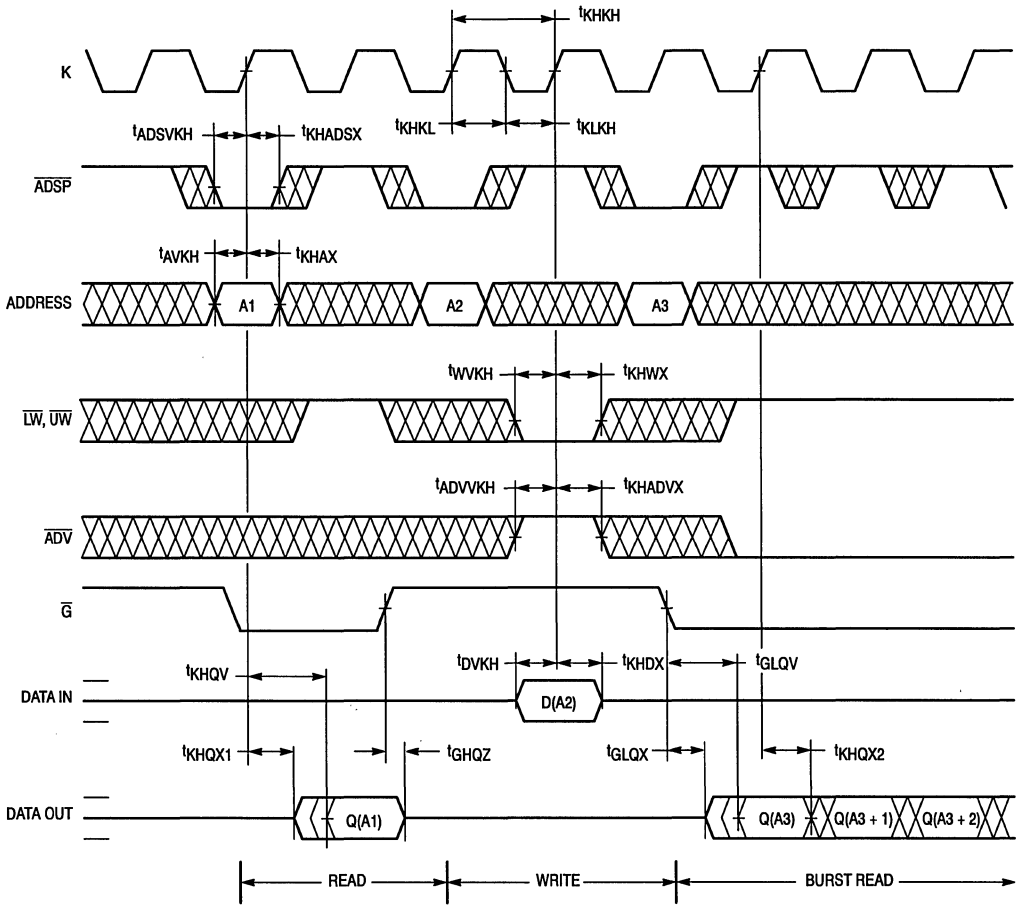
COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{ADSC}$ high)



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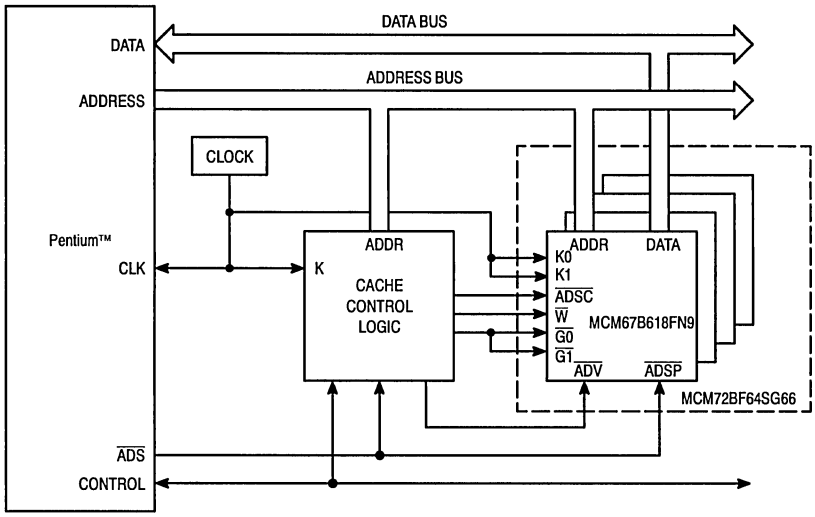
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72BF64SG66 with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72BF32 72BF64	XX	XX	
Motorola Memory Prefix					Speed (66 = 66 MHz, 60 = 60 MHz)
Part Number					Package (SG = Gold Pad SIMM)

Full Part Numbers — MCM72BF32SG66, MCM72BF32SG60
MCM72BF64SG66, MCM72BF64SG60

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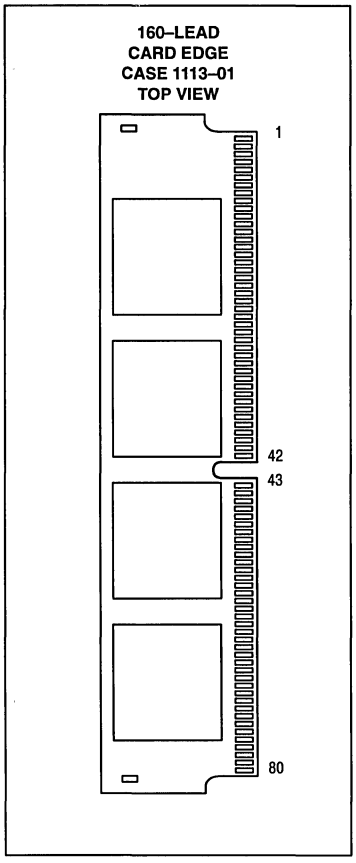
256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™

MCM72CB32
MCM72CB64



The MCM72CB32SG and MCM72CB64SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 160 pin card edge memory module. The module uses four of Motorola's MCM67C518 or MCM67C618 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board tag.

PD0 – PD2 are reserved for density and speed identification.

- Pentium–style Burst Counter on Board
- 160 Pin Card Edge Module
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz, 80 MHz, 100 MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible
- Burndy Connector, Part Number: CELP2X80SC3Z48

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BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

REV 1
5/95

PIN ASSIGNMENT
160–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}	V_{SS}	121	41	V_{SS}
DQ63	82	2	DQ62	DQ9	124	44	DQ8
$V_{CC}5$	83	3	$V_{CC}3$*	DQP1	125	45	DQP0
DQ61	84	4	DQ60	$V_{CC}5$	126	46	$V_{CC}3$*
$V_{CC}5$	85	5	$V_{CC}3$*	DQ7	127	47	DQ6
DQ59	86	6	DQ58	DQ5	128	48	DQ4
DQ57	87	7	DQ56	DQ3	129	49	DQ2
V_{SS}	88	8	V_{SS}	DQ1	130	50	DQ0
DQP7	89	9	DQP6	V_{SS}	131	51	V_{SS}
DQ55	90	10	DQ54	A3B	132	52	A3A
DQ53	91	11	DQ52	A4B	133	53	A4A
DQ51	92	12	DQ50	A5B	134	54	A5A
V_{SS}	93	13	V_{SS}	A6B	135	55	A6A
DQ49	94	14	DQ48	A7	136	56	A8
DQ47	95	15	DQ46	V_{SS}	137	57	V_{SS}
DQ45	96	16	DQ44	A9	138	58	A10
DQ43	97	17	DQ42	A11	139	59	A12
V_{SS}	98	18	V_{SS}	A13	140	60	A14
DQ41	99	19	DQ40	A15	141	61	A16
DQP5	100	20	DQP4	A17	142	62	A18**
DQ39	101	21	DQ38	V_{SS}	143	63	V_{SS}
DQ37	102	22	DQ36	*A19	144	64	PD0
DQ35	103	23	DQ34	PD1	145	65	PD2
V_{SS}	104	24	V_{SS}	K0	146	66	K1
DQ33	105	25	DQ32	*K2	147	67	K3*
DQ31	106	26	DQ30	V_{SS}	148	68	V_{SS}
DQ29	107	27	DQ28	$\overline{WE7}$	149	69	$\overline{WE6}$
DQ27	108	28	DQ26	$\overline{WE5}$	150	70	$\overline{WE4}$
DQ25	109	29	DQ24	$\overline{WE3}$	151	71	$\overline{WE2}$
V_{SS}	110	30	V_{SS}	$\overline{WE1}$	152	72	$\overline{WE0}$
DQP3	111	31	DQP2	V_{SS}	153	73	V_{SS}
DQ23	112	32	DQ22	$\overline{ADSC1}$	154	74	$\overline{ADSC0}$
DQ21	113	33	DQ20	$\overline{E1}$	155	75	$\overline{E0}$
$V_{CC}5$	114	34	$V_{CC}3$*	$\overline{ADV1}$	156	76	$\overline{ADV0}$
DQ19	115	35	DQ18	$\overline{G1}$	157	77	$\overline{G0}$
V_{SS}	116	36	V_{SS}	$V_{CC}5$	158	78	$V_{CC}3$*
DQ17	117	37	DQ16	$\overline{ADSP1}$	159	79	$\overline{ADSP0}$
$V_{CC}5$	118	38	$V_{CC}3$*	V_{SS}	160	80	V_{SS}
DQ15	119	39	DQ14				
DQ13	120	40	DQ12				

PD2	PD1	PD0	Cache Size	Module
V_{SS}	V_{SS}	NC	256KB	72CB32SG
V_{SS}	V_{SS}	V_{SS}	512KB	72CB64SG

PIN NAMES

A3 – A18	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{ADSC0}$, $\overline{ADSC1}$	Controller Address Status
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Status
$\overline{ADV0}$, $\overline{ADV1}$	Burst Advance
PD0 – PD2	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
V_{SS}	Ground

* No Connect for MCM72CB32/MCM72CB64
** No Connect for MCM72CB32

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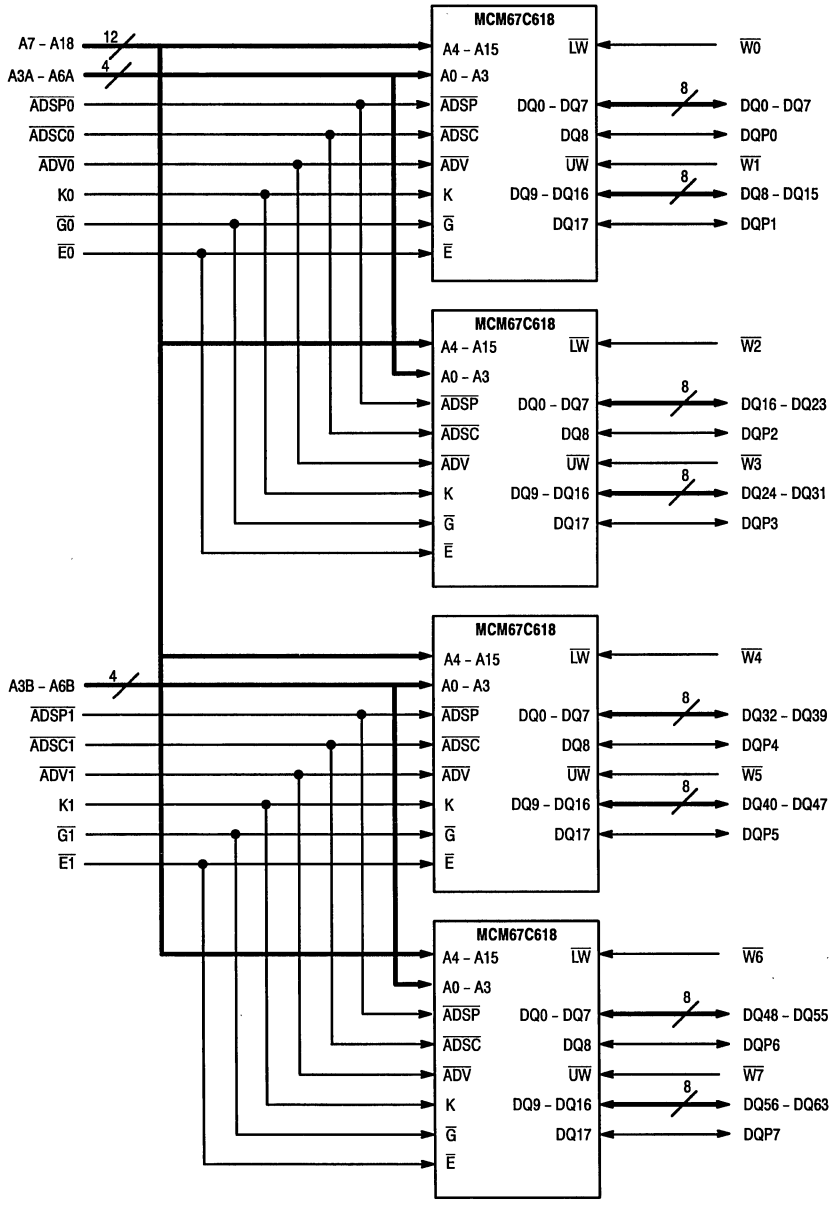
64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



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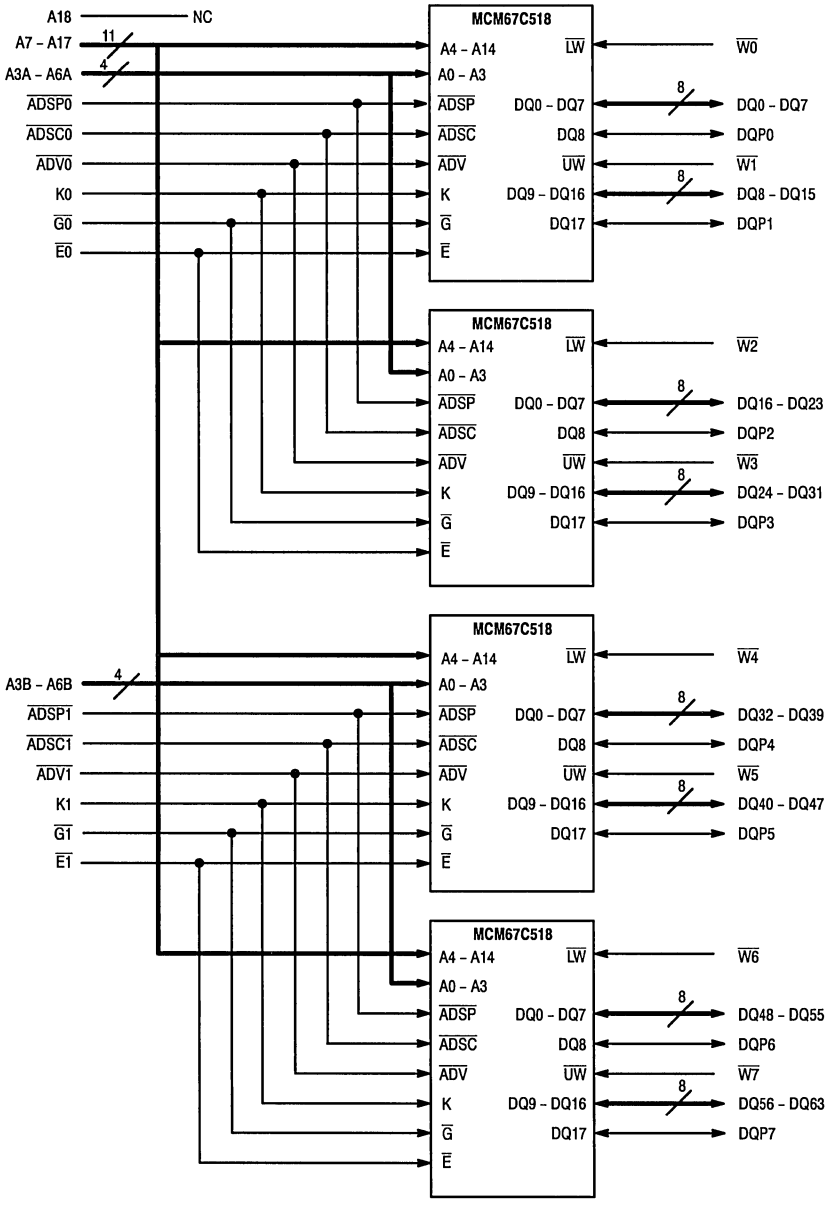
32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



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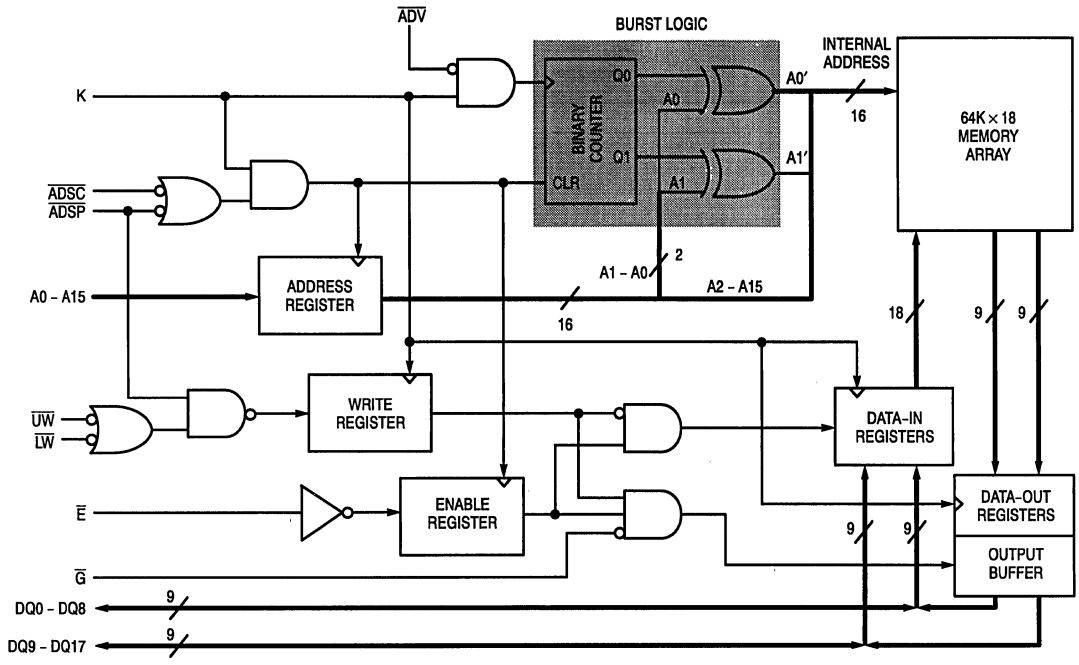
MCM67C618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.4	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66} I_{CCA80} I_{CCA100}	—	1100 1160 1240	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	300	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(A7 – A18)	C_{in}	20	pF
Input Capacitance	(A3 – A6, $\overline{ADSPx}$, $\overline{ADSCx}$, $\overline{ADVx}$, Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	10	pF
Input/Output Capacitance	(DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM72CB64SG100		MCM72CB64SG80		MCM72CB64SG66		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	10	—	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	—	6	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	2	—	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	1	—	1	—	1	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	2	6	2	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	4	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	4	—	5	—	6	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}								
Data In	t_{DVKH}								
Write	t_{WVKH}								
Address Advance	t_{ADVVKH}								
Chip Enable	t_{EVKH}								
Hold Times: Address	t_{KHAX}	0.5	—	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}								
Data In	t_{KHDX}								
Write	t_{KHWX}								
Address Advance	t_{KHADVX}								
Chip Enable	t_{KHEX}								

NOTES:
1. In setup and hold time W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

6

AC TEST LOADS

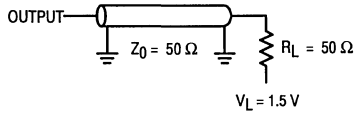


Figure 1A

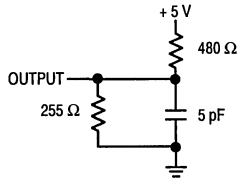
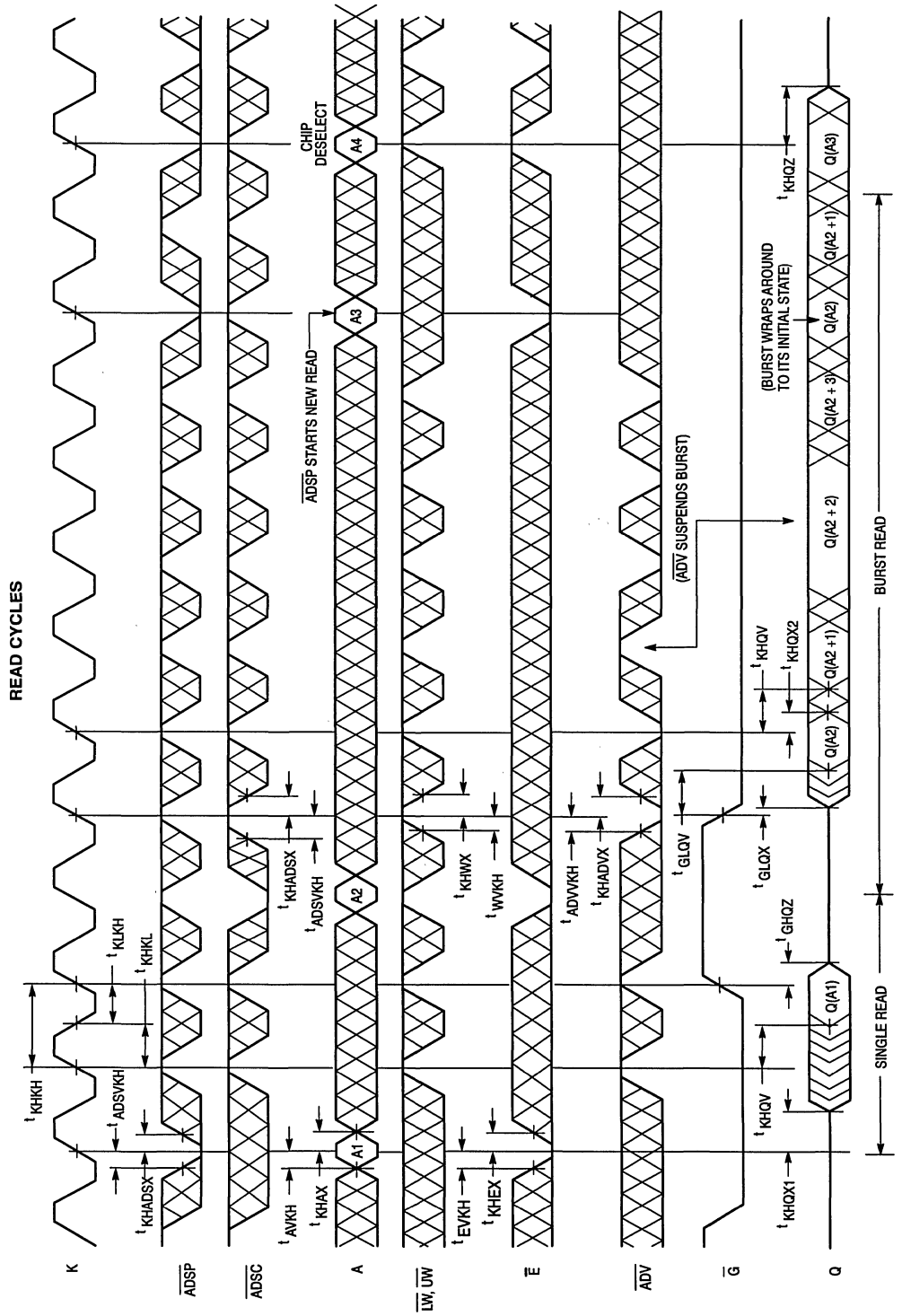
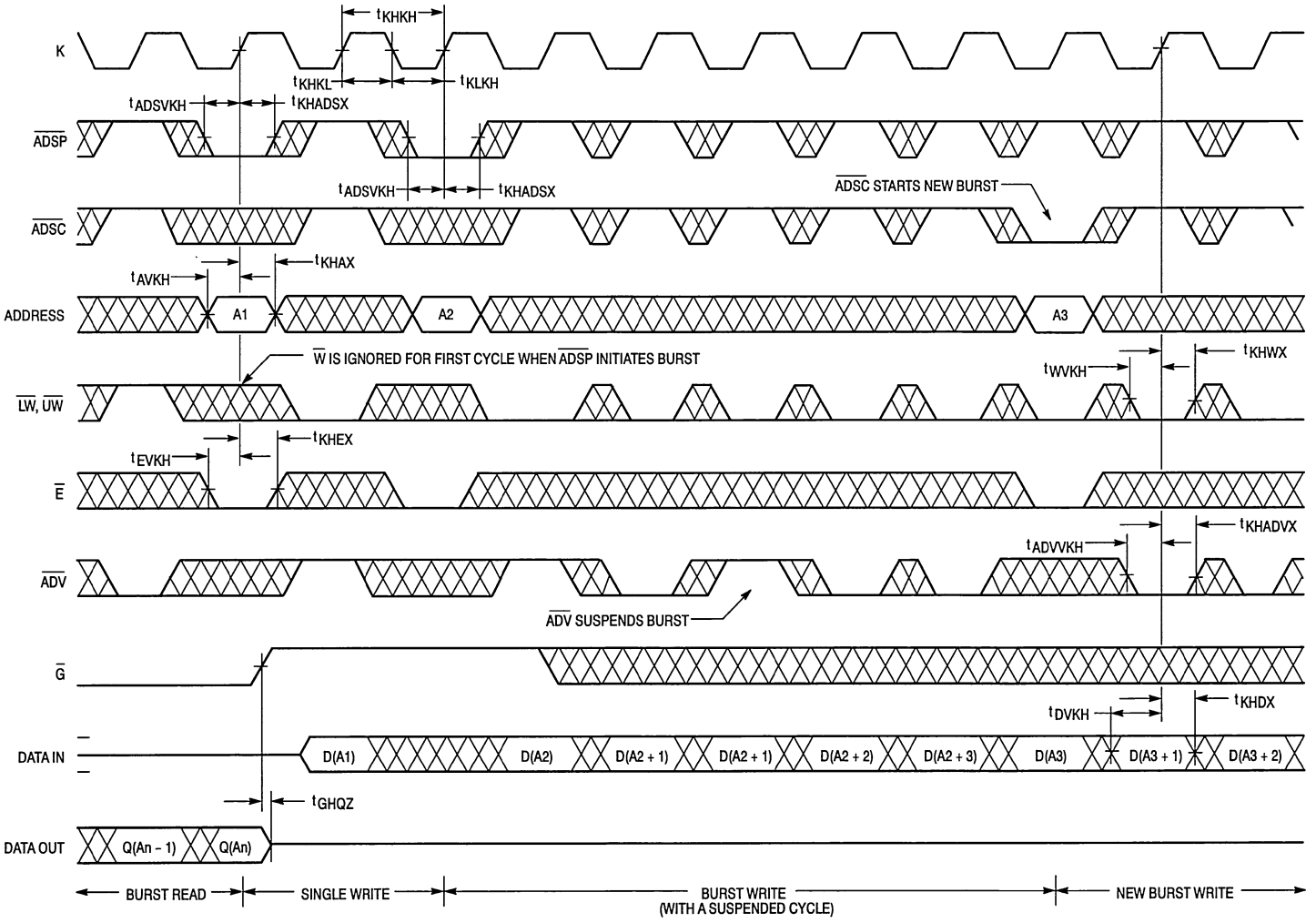


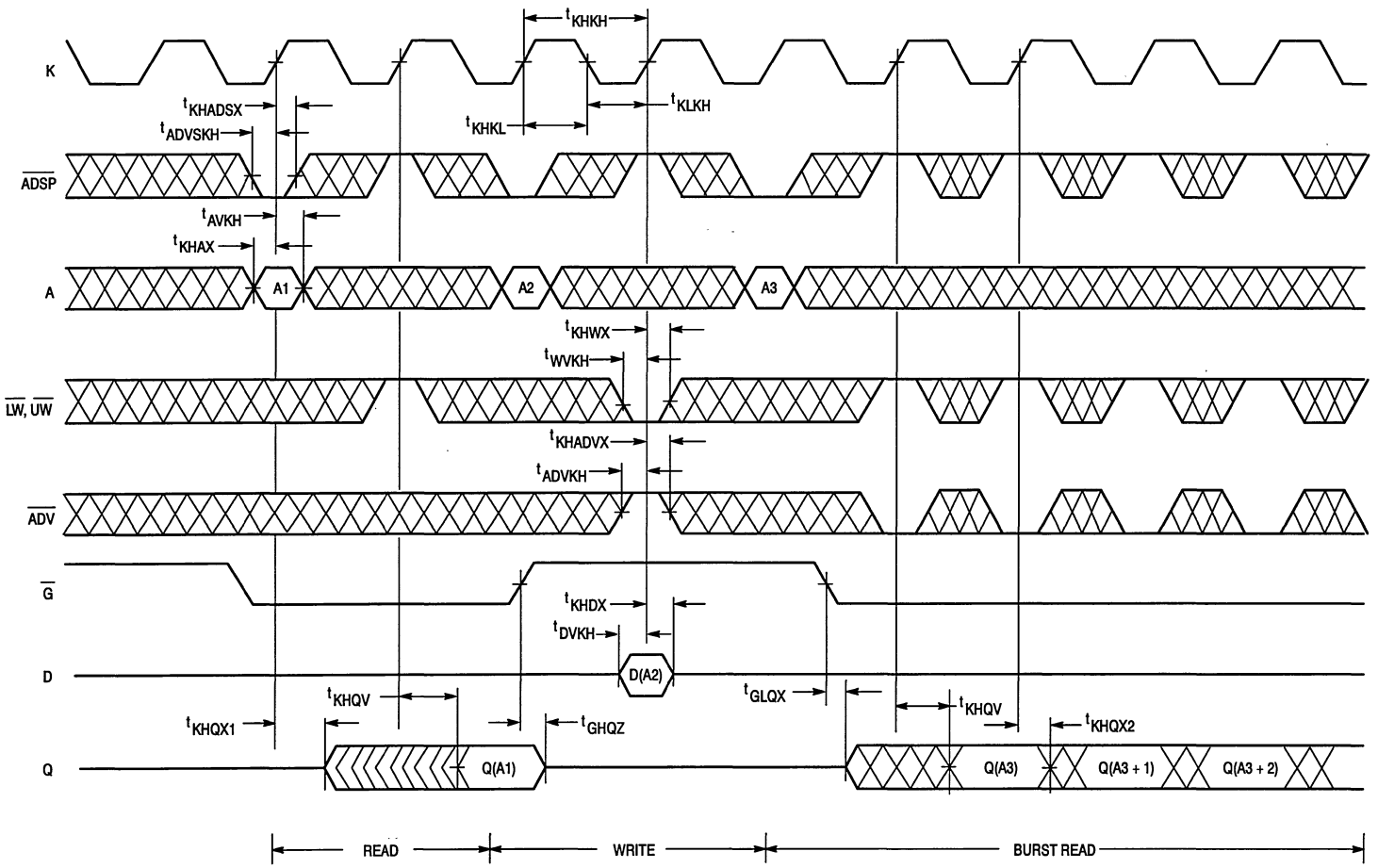
Figure 1B


READ CYCLES
K
ADSP
ADSC
A
LW, UW
E
ADV
G
Q
tKHKH
tKLKH
tKHKL
tADSVKH
tKHADSX
tAVKH
tKHAX
tKHADSX
tADSVKH
tKHWX
tWVKH
tEVKH
tKHEX
tADVVKH
tKHADVX
tGLQV
tGLQX
tGHQZ
tKHQV
tKHQX1
tKHQV
tKHQX2
tKHQZ
A1
A2
A3
A4
CHIP DESELECT
ADSP STARTS NEW READ
(ADV SUSPENDS BURST)
(BURST WRAPS AROUND TO ITS INITIAL STATE)
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
SINGLE READ
BURST READ

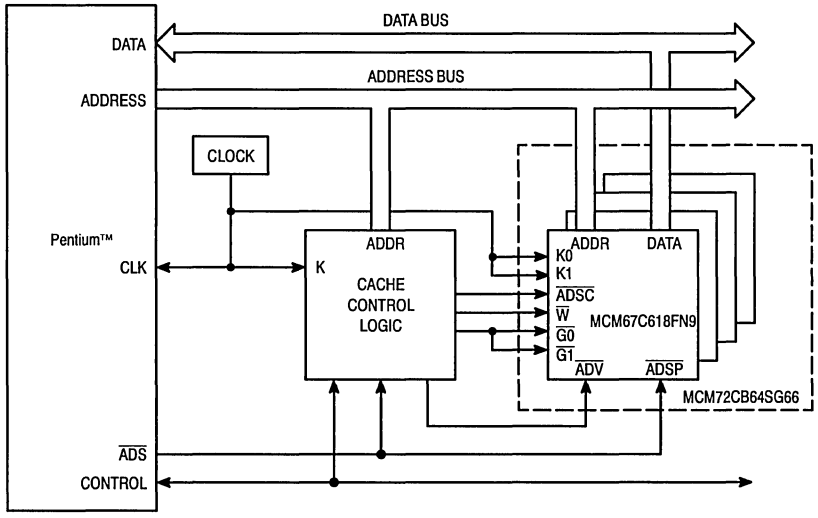
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72CB64SG66 with a 75 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

72CB32
MCM 72CB64 XX XX

Motorola Memory Prefix
Part Number
Speed (66 = 66 MHz, 80 = 80 MHz, 100 = 100 MHz)
Package (SG = Gold Pad SIMM)

Full Part Numbers —	MCM72CB32SG66	MCM72CB32SG80	MCM72CB32SG100
	MCM72CB64SG66	MCM72CB64SG80	MCM72CB64SG100

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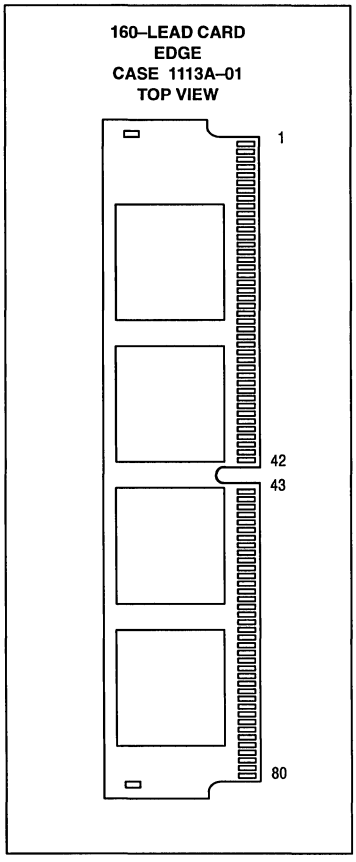
MCM72CF32
MCM72CF64

Advance Information

256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™



The MCM72CF32SG and MCM72CF64SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 160 pin card edge memory module. The module uses four of Motorola's MCM67C518 or MCM67C618 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board tag.

PD0 – PD2 are reserved for density identification.

- Pentium–style Burst Counter on Board
- Pipelined Data Out
- 160 Pin Card Edge Module
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Series 20Ω Resistors for Noise Immunity

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BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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PIN ASSIGNMENT
68–LEAD CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
DQ63	82	2	DQ62
$V_{CC}5$	83	3	$V_{CC}3$*
DQ61	84	4	DQ60
$V_{CC}5$	85	5	$V_{CC}3$*
DQ59	86	6	DQ58
DQ57	87	7	DQ56
V_{SS}	88	8	V_{SS}
DQP7	89	9	DQP6
DQ55	90	10	DQ54
DQ53	91	11	DQ52
DQ51	92	12	DQ50
V_{SS}	93	13	V_{SS}
DQ49	94	14	DQ48
DQ47	95	15	DQ46
DQ45	96	16	DQ44
DQ43	97	17	DQ42
V_{SS}	98	18	V_{SS}
DQ41	99	19	DQ40
DQP5	100	20	DQP4
DQ39	101	21	DQ38
DQ37	102	22	DQ36
DQ35	103	23	DQ34
V_{SS}	104	24	V_{SS}
DQ33	105	25	DQ32
DQ31	106	26	DQ30
DQ29	107	27	DQ28
DQ27	108	28	DQ26
DQ25	109	29	DQ24
V_{SS}	110	30	V_{SS}
DQP3	111	31	DQP2
DQ23	112	32	DQ22
DQ21	113	33	DQ20
$V_{CC}5$	114	34	$V_{CC}3$*
DQ19	115	35	DQ18
V_{SS}	116	36	V_{SS}
DQ17	117	37	DQ16
$V_{CC}5$	118	38	$V_{CC}3$*
DQ15	119	39	DQ14
DQ13	120	40	DQ12
V_{SS}	121	41	V_{SS}
DQ11	122	42	DQ10
$V_{CC}5$	123	43	$V_{CC}3$*
DQ9	124	44	DQ8
DQP1	125	45	DQP0
$V_{CC}5$	126	46	$V_{CC}3$*
DQ7	127	47	DQ6
DQ5	128	48	DQ4
DQ3	129	49	DQ2
DQ1	130	50	DQ0
V_{SS}	131	51	V_{SS}
A3B	132	52	A3A
A4B	133	53	A4A
A5B	134	54	A5A
A6B	135	55	A6A
A7	136	56	A8
V_{SS}	137	57	V_{SS}
A9	138	58	A10
A11	139	59	A12
A13	140	60	A14
A15	141	61	A16
A17	142	62	A18**
V_{SS}	143	63	V_{SS}
*A19	144	64	PD0
PD1	145	65	PD2
K0	146	66	K1
*K2	147	67	K3*
V_{SS}	148	68	V_{SS}
$\overline{WE7}$	149	69	$\overline{WE6}$
$\overline{WE5}$	150	70	$\overline{WE4}$
$\overline{WE3}$	151	71	$\overline{WE2}$
$\overline{WE1}$	152	72	$\overline{WE0}$
V_{SS}	153	73	V_{SS}
$\overline{ADSC1}$	154	74	$\overline{ADSC0}$
$\overline{E1}$	155	75	$\overline{E0}$
$\overline{ADV1}$	156	76	$\overline{ADV0}$
$\overline{G1}$	157	77	$\overline{G0}$
$V_{CC}5$	158	78	$V_{CC}3$*
$\overline{ADSP1}$	159	79	$\overline{ADSP0}$
V_{SS}	160	80	V_{SS}

PD2	PD1	PD0	Cache Size	Module
V_{SS}	V_{SS}	NC	256KB	72CF32SG
V_{SS}	V_{SS}	V_{SS}	512KB	72CF64SG

PIN NAMES	
A3 – A18	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{ADSC0}$, $\overline{ADSC1}$	Controller Address Status
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Status
$\overline{ADV0}$, $\overline{ADV1}$	Burst Advance
PD0 – PD2	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
V_{SS}	Ground

* No Connect for MCM72CF32/MCM72CF64
** No Connect for MCM72CF32

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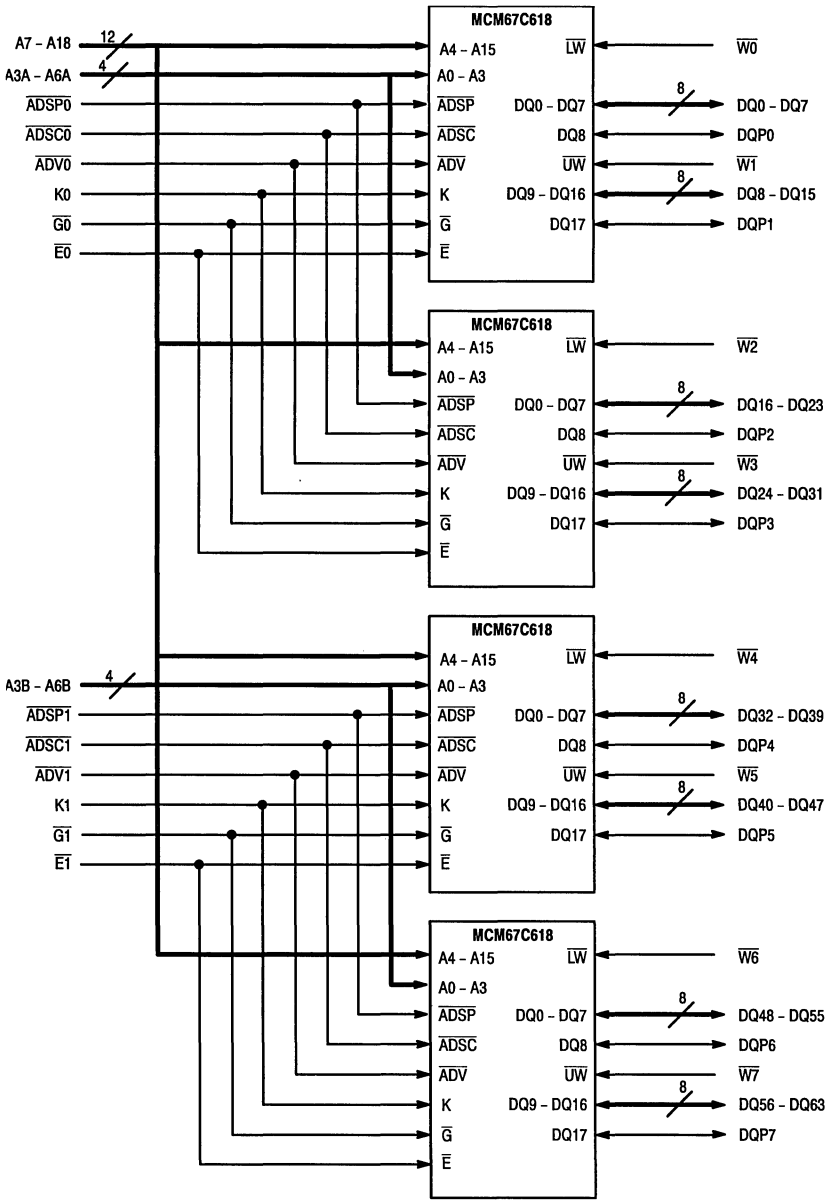
64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



DQ 0–63 and DQP 0–7 are series terminated with 20Ω resistors.

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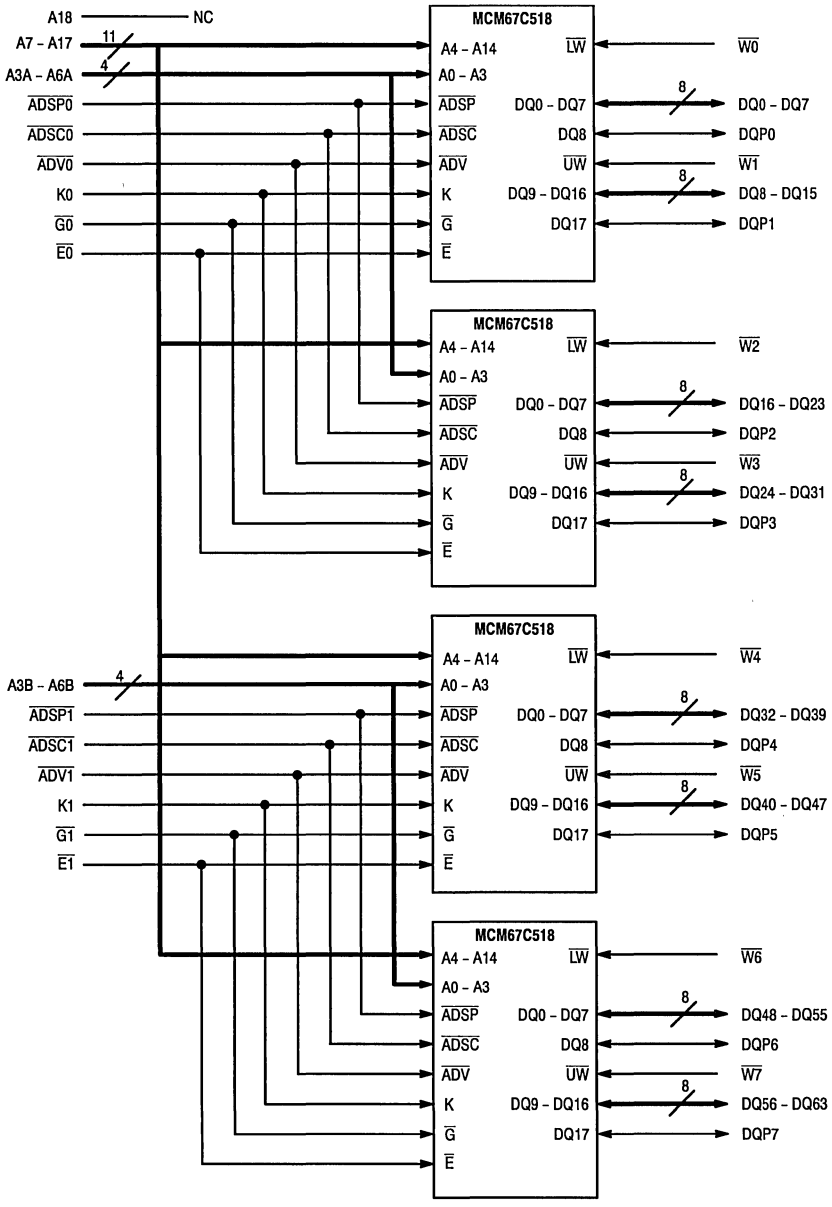
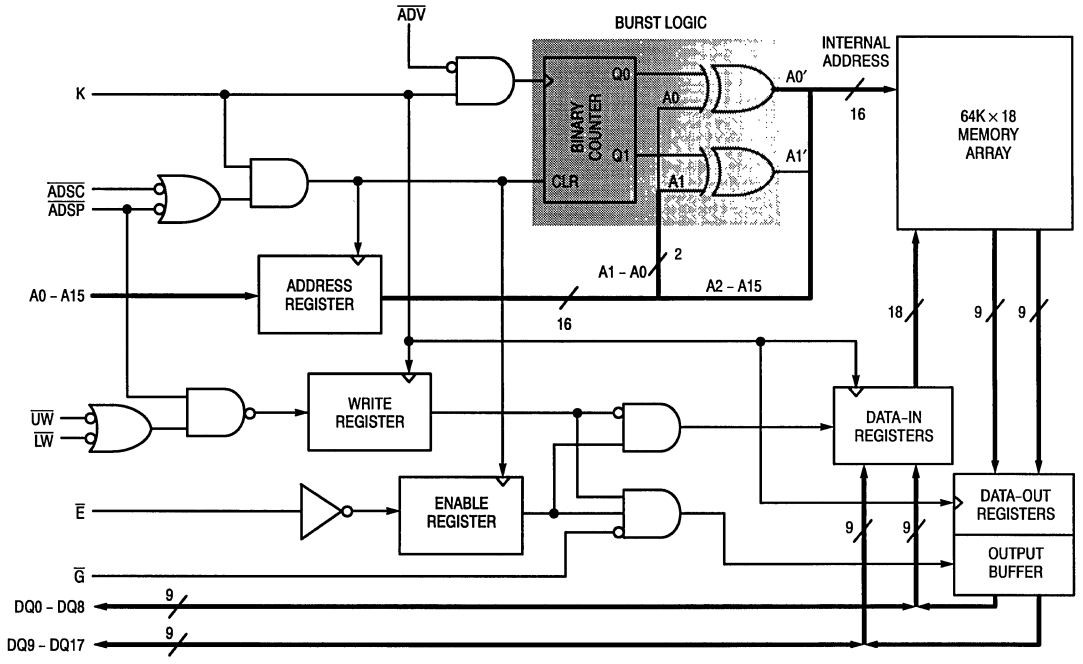
32K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



DQ0–63 and DQP0–7 are series terminated with 20Ω resistors.

MCM67C618 BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by asserting $\overline{ADSP}$ and a valid address on the first cycle, then negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.4	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66}	—	1100	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	300	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Input Capacitance (A7 – A18)	C_{in}	20	pF
Input Capacitance (A3 – A6, $\overline{ADSPx}$, $\overline{ADSCx}$, $\overline{ADVx}$, Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	10	pF
Input/Output Capacitance (DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM72CF64SG66 Min	MCM72CF64SG66 Max	Unit	Notes
Cycle Time	t_{KHKH}	15	—	ns	
Clock Access Time	t_{KHQV}	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	—	6	ns	
Clock High to Output Active	t_{KHQX1}	2	—	ns	
Clock High to Output Change	t_{KHQX2}	2	—	ns	
Output Enable to Output Active	t_{GLQX}	1	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	ns	6
Clock High to Q High–Z	t_{KHQZ}	—	6	ns	
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Setup Times: Address	t_{AVKH}	2.5	—	ns	7
Address Status	t_{ADSVKH}				
Data In	t_{DVKH}				
Write	t_{WVKH}				
Address Advance	t_{ADVVKH}				
Chip Enable	t_{EVKH}				
Hold Times: Address	t_{KHAX}	0.5	—	ns	7
Address Status	t_{KHADSX}				
Data In	t_{KHDX}				
Write	t_{KHWX}				
Address Advance	t_{KHADVX}				
Chip Enable	t_{KHEX}				

NOTES:
1. In setup and hold time W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

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AC TEST LOADS

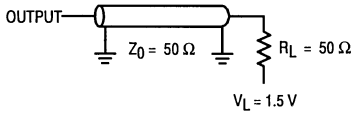


Figure 1A

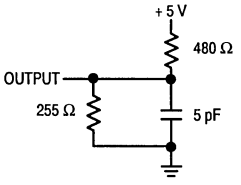
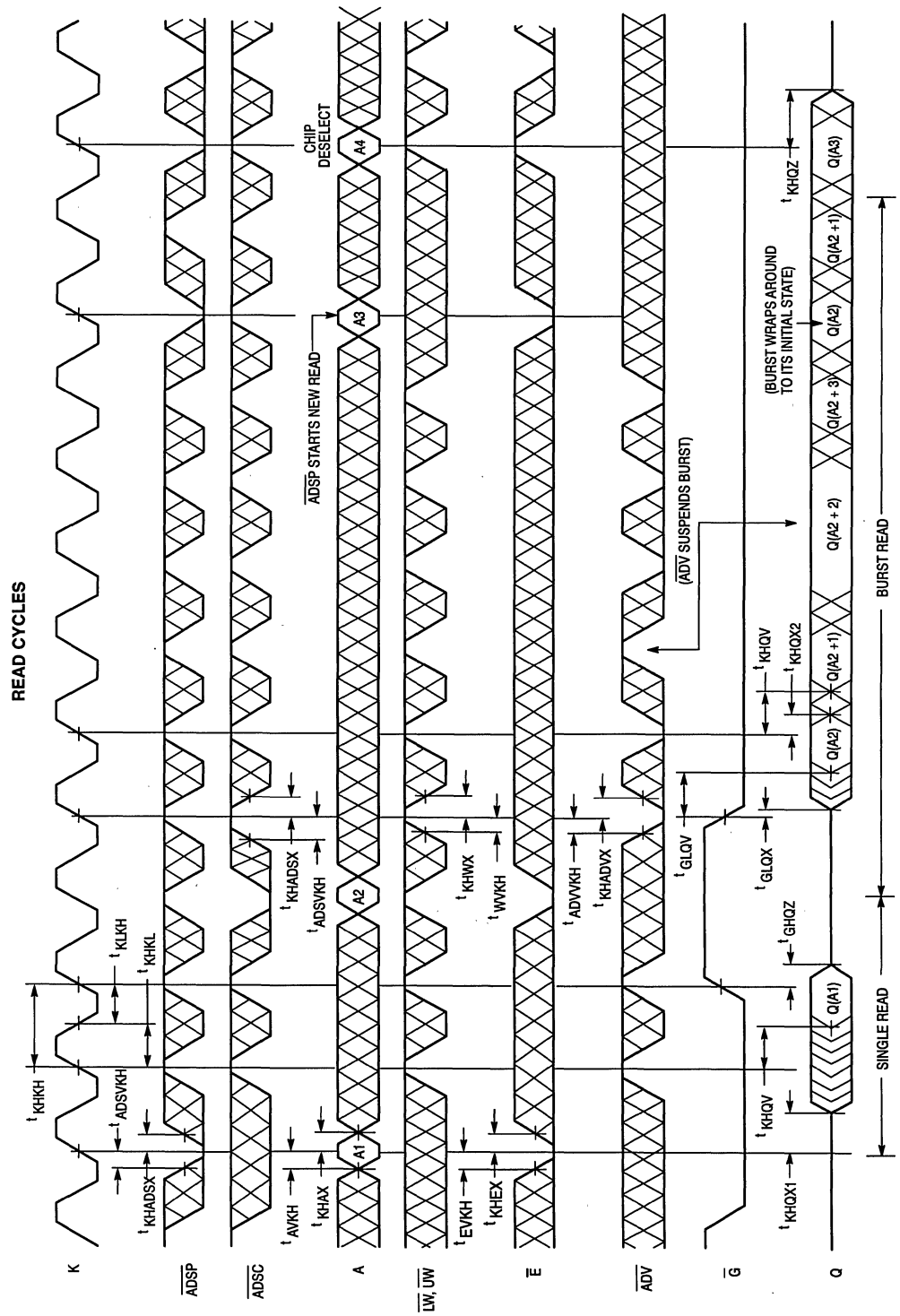
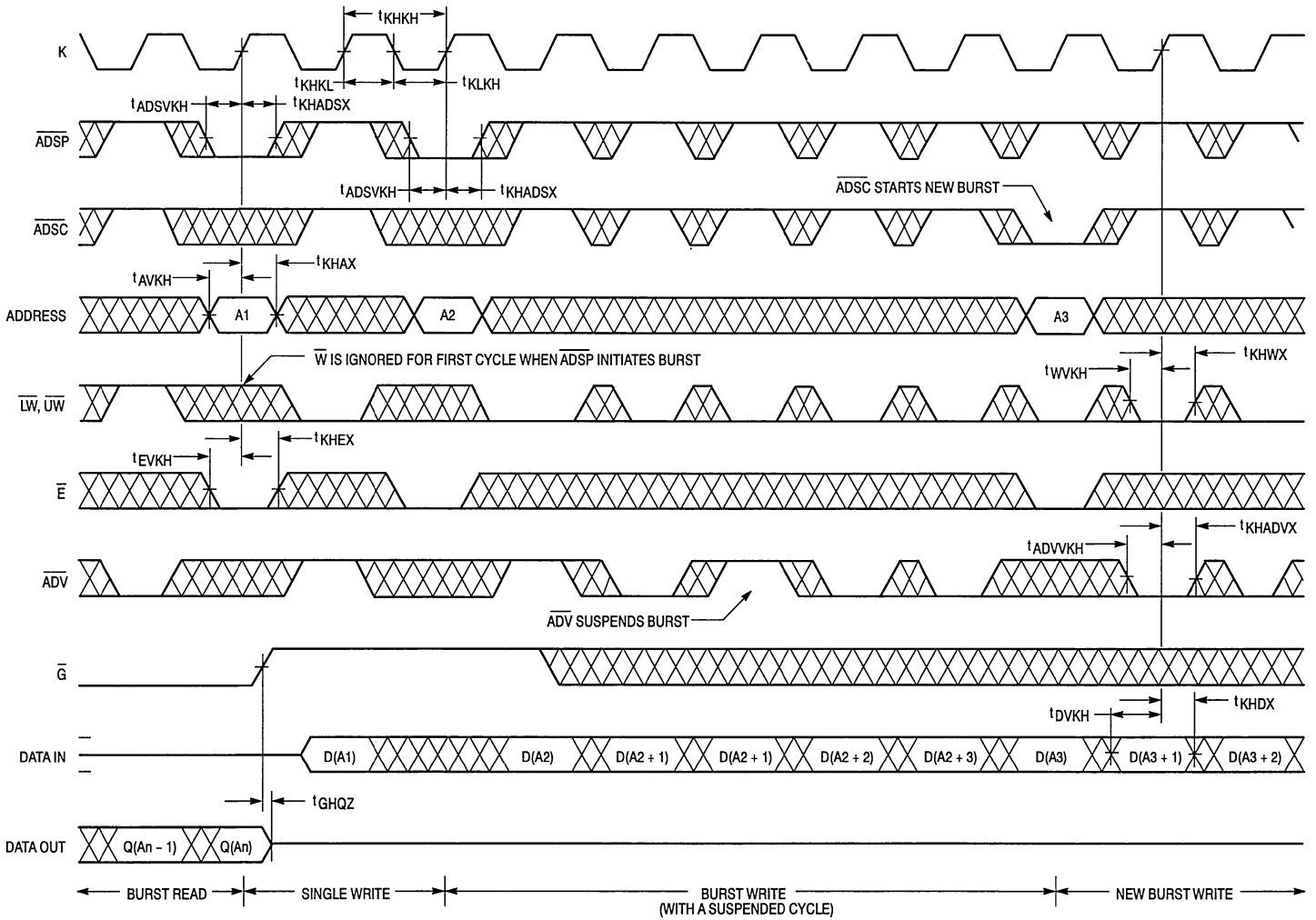


Figure 1B

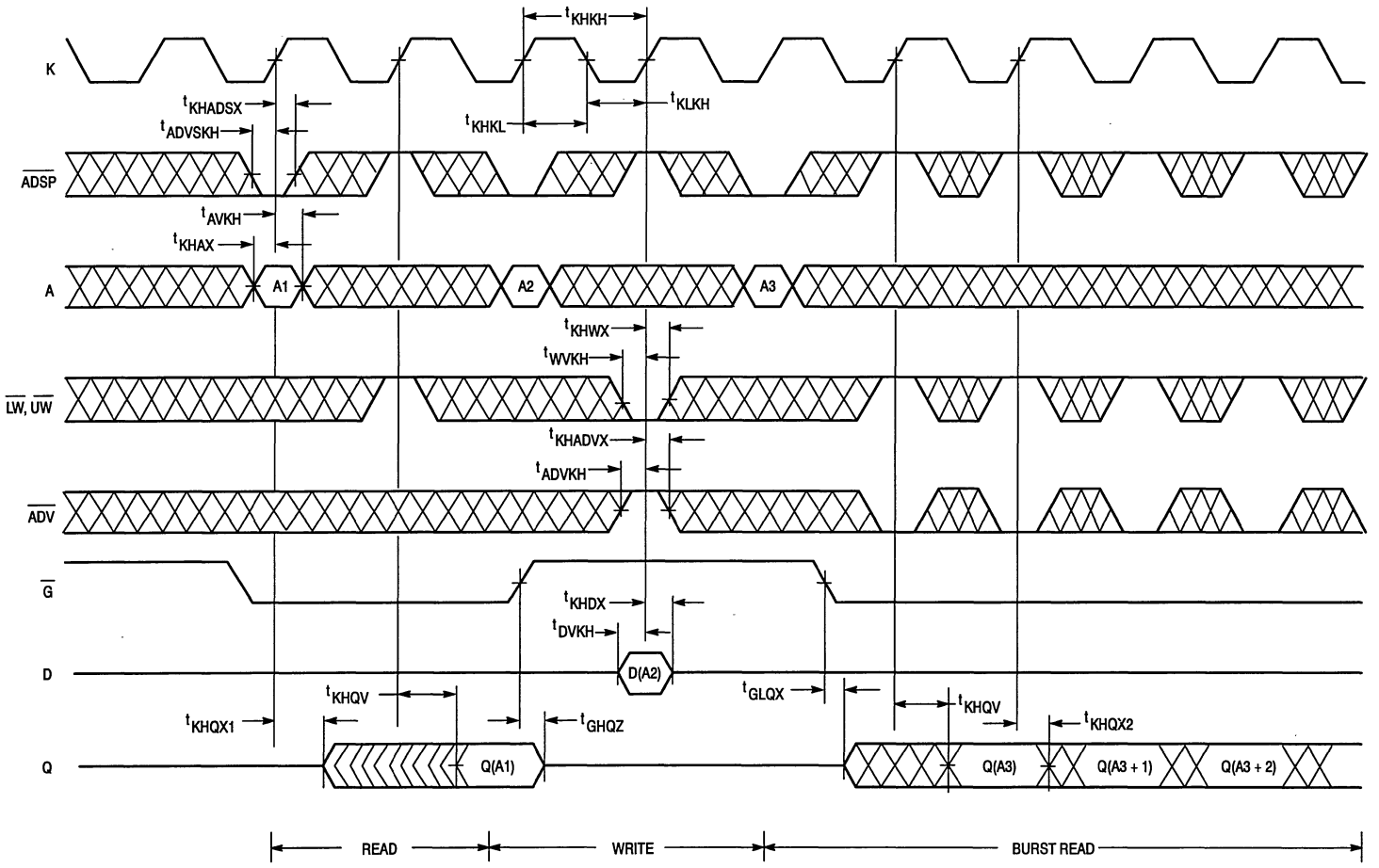
READ CYCLES


K
ADSP
ADSC
A
LW, UW
E
ADV
G
Q
tKHKH
tKLKH
tKHKL
tADSVKH
tKHADSX
tAVKH
tKHAX
tKHADSX
tADSVKH
tKHWX
tWVKH
tADVVKH
tKHADVX
tGLQV
tGLQX
tGHQZ
tKHQV
tKHQX2
tKHQX1
tKHQZ
A1
A2
A3
A4
CHIP DESELECT
ADSP STARTS NEW READ
(ADV SUSPENDS BURST)
(BURST WRAPS AROUND TO ITS INITIAL STATE)
Q(A1)
Q(A2)
Q(A2 +1)
Q(A2 + 2)
Q(A2 + 3)
Q(A2)
Q(A2 +1)
Q(A3)
SINGLE READ
BURST READ

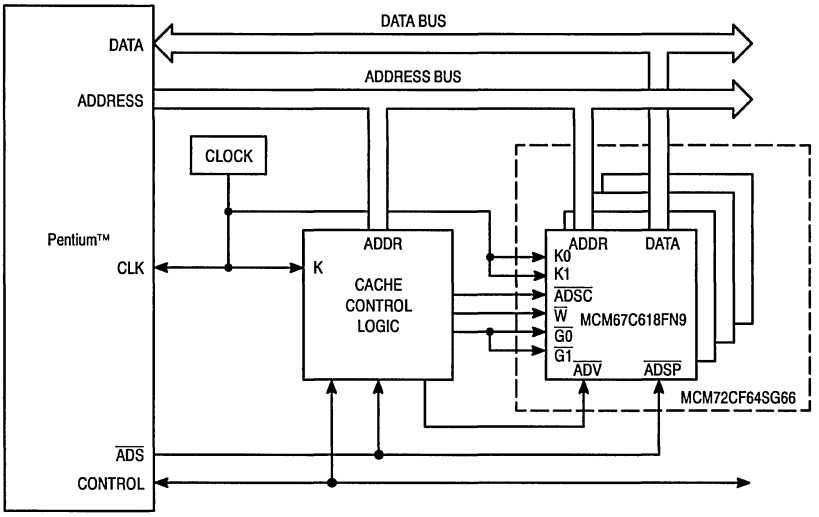
WRITE CYCLES



COMBINATION READ/WRITE CYCLES ($\overline{E}$ low, $\overline{ADSC}$ high)



APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MCM72CF64SG66 with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

	MCM	72CF32 72CF64	XX	XX	
Motorola Memory Prefix					Speed (66 = 66 MHz)
Part Number					Package (SG = Gold Pad SIMM)

Full Part Numbers — MCM72CF32SG66
MCM72CF64SG66

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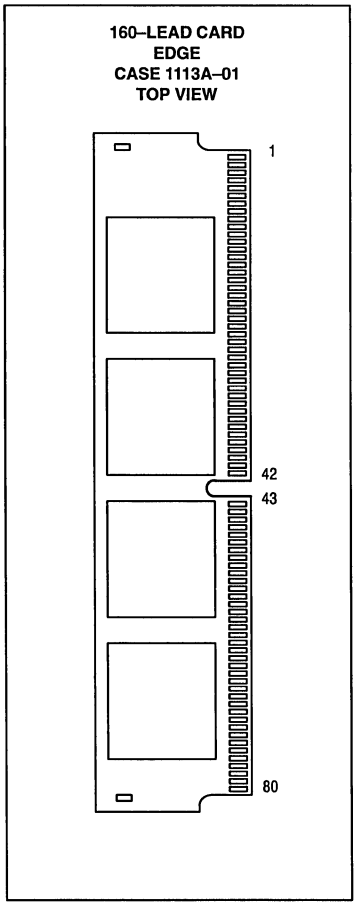
MCM72JG32
MCM72JG64

Advance Information

256K and 512K Pipelined BurstRAM™ Sedcondary Cache Module for Pentium™



The MCM72JG32 and MCM72JG64 are designed to provide a burstable, high performance, 256K/512K L2 cache for the Pentium microprocessor in conjunction with Intel's Triton chip set. The modules are configured as 32K x 64 and 64K x 64 bits in a 160 pin card edge memory module. Each module uses four of Motorola's 5 V 32K x 18 or 64K x 18 BurstRAMs and one Motorola 5 V 32K x 8 FSRAM for the tag RAM.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or cache address status ($\overline{CADS}$). Subsequent burst addresses are generated internal to the BurstRAM by the cache burst advance ($\overline{CADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLK0, CLK1) input. Eight write enables are provided for byte write control.

PD0 – PD4 map into the Triton chip set for auto–configuration of the cache control.

Module family pinout supports 5 V and 3.3 V components. It is recommended that all power supplies be connected.

These cache modules are plug and pin compatible with the MCM64AF32SG15, a 256K byte asynchronous module also designed for the Pentium microprocessor in conjunction with Intel's Triton chip set.

- Pentium–Style Burst Counter on Chip
- Pipelined Data Out
- 160 Pin Card Edge Module
- Address Pipeline Supported by $\overline{ADSP}$ Disabled with $\overline{Ex}$
- All Cache Data and Tag I/Os are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz
- Fast SRAM Access Times: 15 ns for Tag RAM
  9 ns for Data RAMs
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB with Separate Power and Ground Planes
- I/Os are 3.3 V Compatible on Data RAMs
- Burndy Connector, Part Number: CELP2X80SC3Z48
- Series 20 Ω Resistors for Noise Immunity

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BurstRAM is a trademark of Motorola.
Pentium is a trademark of Intel Corp.

REV 1
4/95

PIN ASSIGNMENT
160–PIN CARD EDGE MODULE
TOP VIEW

V_{SS}	81	1	V_{SS}
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
(RSVD) NC	86	6	NC (RSVD)
$V_{CC}5$	87	7	$V_{CC}3$
(RSVD) NC	88	8	$\overline{TWE}$
*(CAA4) $\overline{CADV}$	89	9	$\overline{CADS}$ (CAA3)*
V_{SS}	90	10	V_{SS}
$\overline{COE}$	91	11	$\overline{CWE4}$
$\overline{CWE5}$	92	12	$\overline{CWE6}$
$\overline{CWE7}$	93	13	$\overline{CWE0}$
$\overline{CWE1}$	94	14	$\overline{CWE2}$
$V_{CC}5$	95	15	$V_{CC}3$
$\overline{CWE3}$	96	16	$\overline{CCS}$ (CAB4)*
*(CAB3) NC	97	17	NC ($\overline{GWE}$)**
*(CALE) NC	98	18	NC ($\overline{BWE}$)**
V_{SS}	99	19	V_{SS}
(RSVD) NC	100	20	A3
A4	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
$V_{CC}5$	105	25	$V_{CC}3$
A17	106	26	NC (A18)†
V_{SS}	107	27	V_{SS}
A9	108	28	A12
A14	109	29	A13
A15	110	30	$\overline{ADSP}$
(RSVD) NC	111	31	NC ($\overline{ECS1}$, $\overline{CS}$)
PD0	112	32	NC ($\overline{ECS2}$)
PD2	113	33	PD1
PD4	114	34	PD3
V_{SS}	115	35	V_{SS}
CLK0	116	36	CLK1
V_{SS}	117	37	V_{SS}
DQ63	118	38	DQ62
$V_{CC}5$	119	39	$V_{CC}3$
DQ61	120	40	DQ60
DQ59	121	41	DQ58
DQ57	122	42	DQ56
V_{SS}	123	43	V_{SS}
DQ55	124	44	DQ54
DQ53	125	45	DQ52
DQ51	126	46	DQ50
DQ49	127	47	DQ48
V_{SS}	128	48	V_{SS}
DQ47	129	49	DQ46
DQ45	130	50	DQ44
DQ43	131	51	DQ42
$V_{CC}5$	132	52	$V_{CC}3$
DQ41	133	53	DQ40
DQ39	134	54	DQ38
DQ37	135	55	DQ36
V_{SS}	136	56	V_{SS}
DQ35	137	57	DQ34
DQ33	138	58	DQ32
DQ31	139	59	DQ30
$V_{CC}5$	140	60	$V_{CC}3$
DQ29	141	61	DQ28
DQ27	142	62	DQ26
DQ25	143	63	DQ24
V_{SS}	144	64	V_{SS}
DQ23	145	65	DQ22
DQ21	146	66	DQ20
DQ19	147	67	DQ18
$V_{CC}5$	148	68	$V_{CC}3$
DQ17	149	69	DQ16
DQ15	150	70	DQ14
DQ13	151	71	DQ12
V_{SS}	152	72	V_{SS}
DQ11	153	73	DQ10
DQ9	154	74	DQ8
DQ7	155	75	DQ6
$V_{CC}5$	156	76	$V_{CC}3$
DQ5	157	77	DQ4
DQ3	158	78	DQ2
DQ1	159	79	DQ0
V_{SS}	160	80	V_{SS}

PRESENCE DETECT TABLE

Cache Size and Functionality	Module	PD4	PD3	PD2	PD1	PD0
256K Async	MCM64AF32	V_{SS}	NC	V_{SS}	V_{SS}	NC
512K Async	—	V_{SS}	V_{SS}	NC	V_{SS}	NC
256K Burst	—	V_{SS}	NC	V_{SS}	NC	V_{SS}
256K Pipe Burst	MCM72JG32	V_{SS}	NC	V_{SS}	NC	NC
512K Burst	—	V_{SS}	V_{SS}	NC	NC	V_{SS}
512K Pipe Burst	MCM72JG64	V_{SS}	V_{SS}	NC	NC	NC
512K 2–Bank Burst	—	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}

PIN NAMES

A3 – A18	Cache Address
DQ0 – DQ63	Data Input/Output
CLK0, CLK1	Clock
$\overline{CWE0}$ – $\overline{CWE7}$	Cache Write Enable
$\overline{BWE}$**	Byte Write Enable
$\overline{GWE}$**	Global Write Enable
TIO0 – TIO7	Tag Input/Output
$\overline{TWE}$	Tag Write Enable
$\overline{CADS}$	Cache Address Status
$\overline{ADSP}$	Address Status Processor
$\overline{CADV}$	Cache Burst Advance
$\overline{COE}$	Cache Output Enable
$\overline{CCS}$	Cache Chip Select
RSVD	Reserved for Future Use
PD0 – PD4	Presence Detect
$V_{CC}5$	+ 5 V Power Supply
$V_{CC}3$	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connect

NOTES:
- * Signals in parentheses indicate pin descriptions for asynchronous Triton chip set module.
- ** Signals in parentheses will be implemented in future burstable Triton modules.
- † NC for MCM72JG32, A18 for MCM72JG64.

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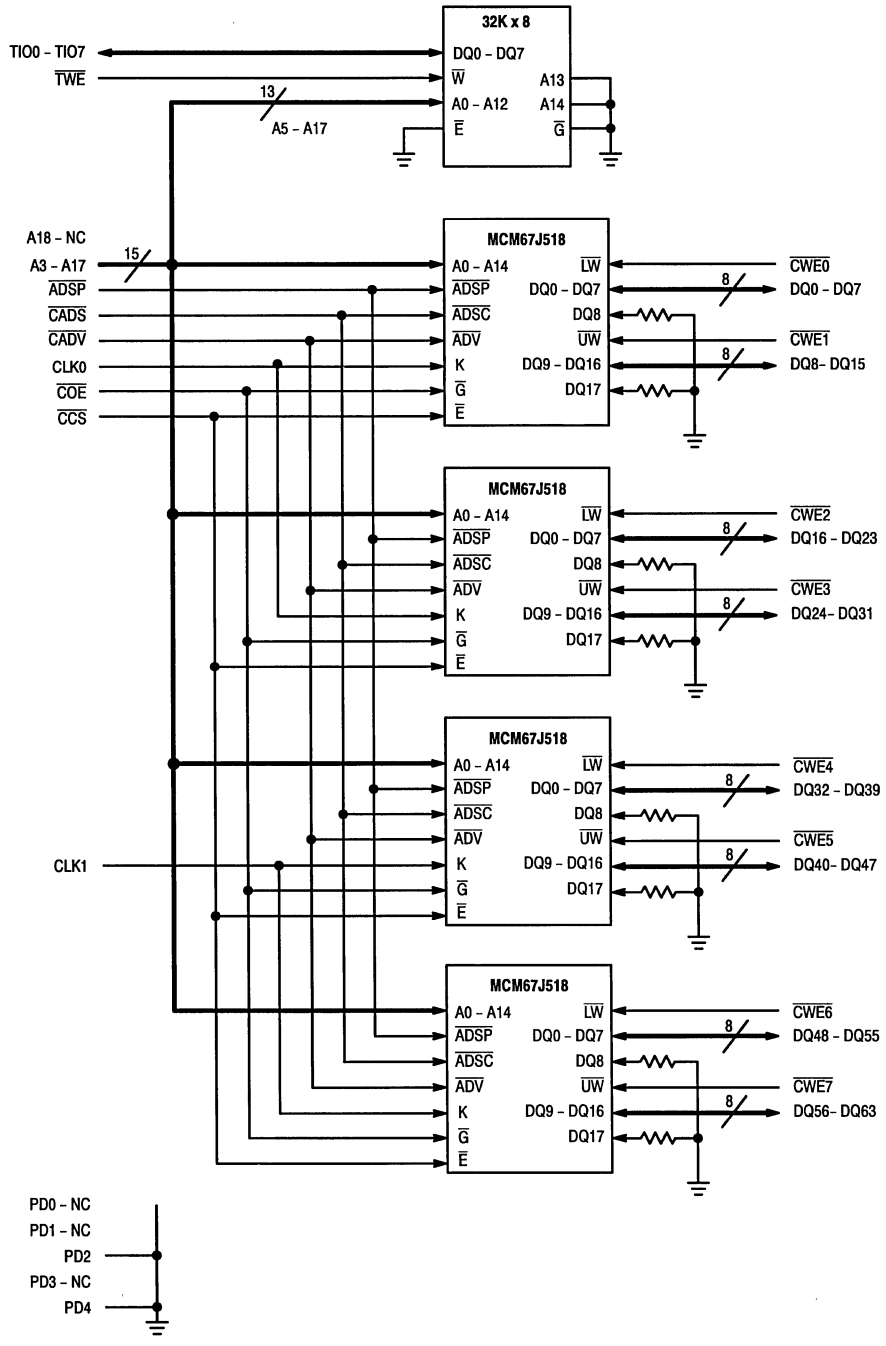
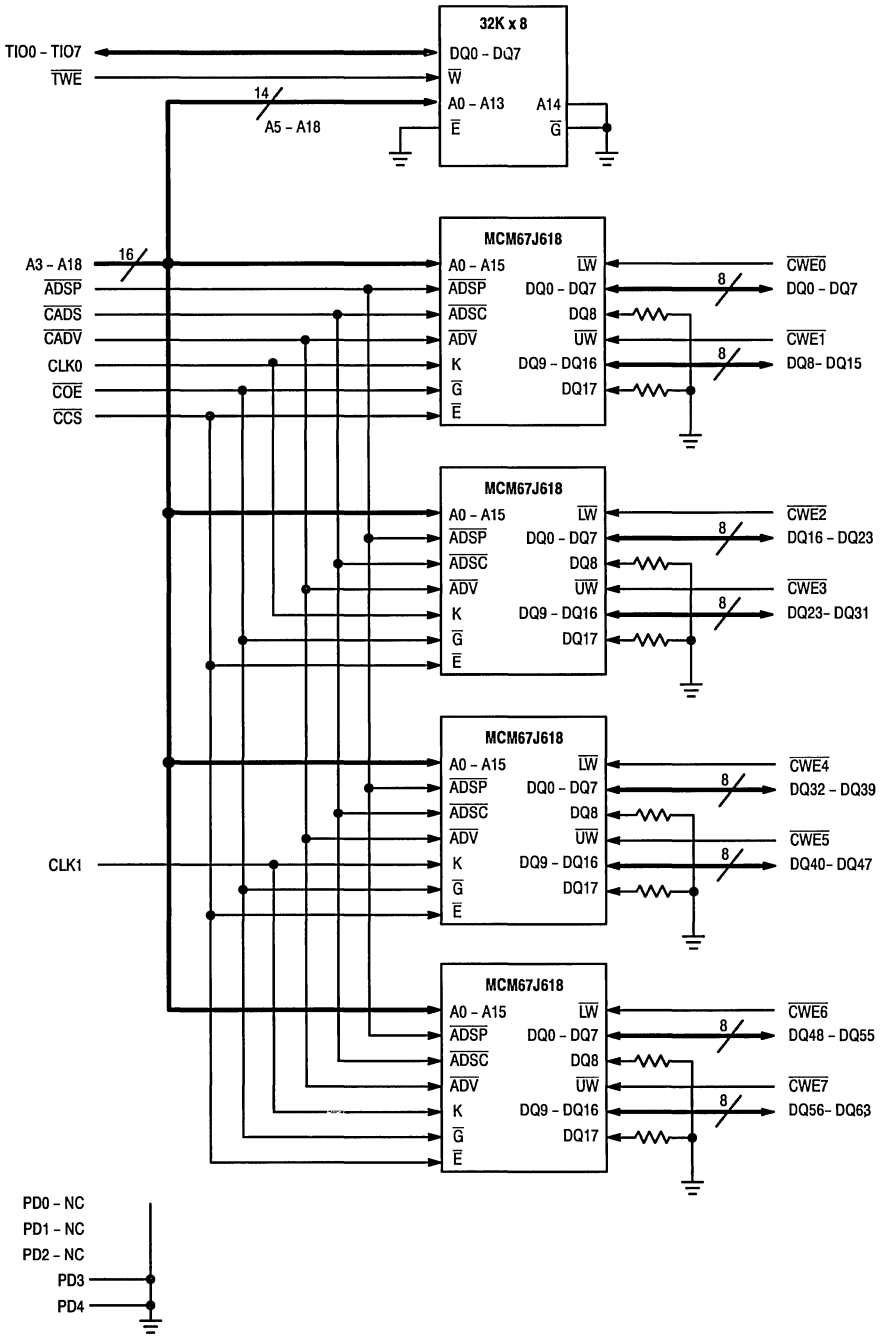
MCM72JG32 MODULE BLOCK DIAGRAM



MCM72JG64 MODULE BLOCK DIAGRAM



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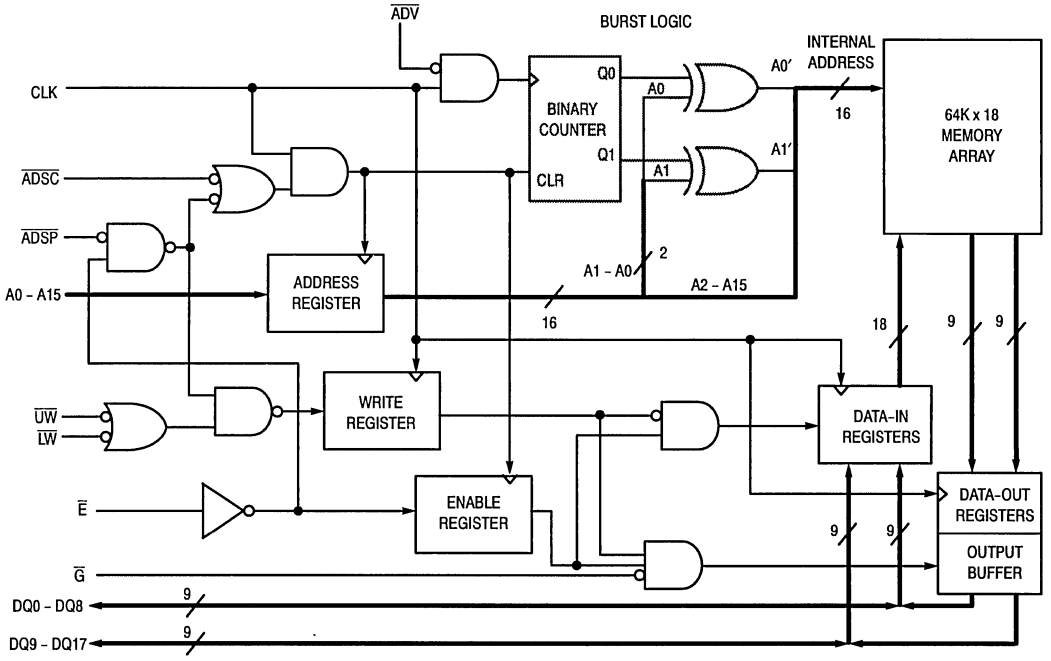
PIN DESCRIPTIONS

160–Lead Card Edge Pin Locations	Symbol	Type	Description
20, 21, 22, 23, 24, 28, 29, 101, 102, 103, 104, 106, 108, 109, 110	A3 – A18	Input	Address Inputs: These inputs are registered into data RAMs and must meet setup and hold times. The tag RAM addresses are not registered.
36, 116	CLK0, CLK1	Input	Clock: This signal registers the address, data in, and all control signals except $\overline{COE}$.
11, 12, 13, 14, 92, 93, 94, 96	$\overline{CWE0}$ – $\overline{CWE7}$	Input	Cache Data Byte Write Enable: Active low write signal for data RAMs.
8	$\overline{TWE}$	Input	Tag Write Enable: Active low write signal for tag RAMs.
—	$\overline{BWE}$	Input	Byte Write Enable: To be used in future modules.
—	$\overline{GWE}$	Input	Global Write Enable: To be used in future modules.
16	$\overline{CCS}$	Input	Chip Select: Active low chip enable for data RAMs.
30	$\overline{ADSP}$	Input	Address Status Processor: Initiates READ, WRITE, or chip deselect cycle (Exception–chip deselect does not occur when $\overline{ADSP}$ is asserted and $\overline{CCS}$ is high.
9	$\overline{CADS}$	Input	Cache Address Status: Initiates READ, WRITE, or chip deselect cycle.
89	$\overline{CADV}$	Input	Cache Burst Advance: Increments address count in accordance with interleaved count style.
91	$\overline{COE}$	Input	Cache Output Enable: Active low asynchronous input. Low–enables output buffers (DQ pins) High–DQx pins are high impedance.
38, 40, 41, 42, 44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 61, 62, 63, 65, 66, 67, 69, 70, 71, 73, 74, 75, 77, 78, 79, 118, 120, 121, 122, 124, 125, 126, 127, 129, 130, 131, 133, 134, 135, 137, 138, 139, 141, 142, 143, 145, 146, 147, 149, 150, 151, 153, 154, 155, 157, 158, 159	DQ0 – DQ63	I/O	Synchronous Data I/O: Drives data out of data RAMs during READ cycles. Stores data to data RAMs during WRITE cycles.
2, 3, 4, 5, 82, 83, 84, 85	TIO0 – TIO7	I/O	Tag RAM I/O: Drives data out during tag compare cycles. Stores data to tag RAM during tag WRITE cycles.
33, 34, 112, 113, 114	PD0 – PD4	—	Presence Detect: See Presence Detect Table
7, 15, 25, 39, 52, 60, 68, 76	$V_{CC}3$	Supply	Power Supply: 3.3 V ± 5%.
87, 95, 105, 119, 132, 140, 148, 156	$V_{CC}5$	Supply	Power Supply: 5.0 V ± 5%.
1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160	V_{SS}	Supply	Ground
6, 17, 18, 26, 31, 32, 86, 88, 97, 98, 100, 111	NC	—	No Connection: There is no connection to the module.

64K x 18 BurstRAM BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{CWE}$ and $\overline{ADSC}$) is performed using the new external address. Alternatively, an $\overline{ADSP}$–initiated two cycle WRITE can be performed by negating both $\overline{ADSP}$ and $\overline{ADSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write cycle in WRITE CYCLES timing diagram). When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{CWE}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

64K x 18 BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

NOTE: The above BurstRAM Block Diagram and Burst Sequence Table apply specifically tothe 64K x 18 chip. The 32K x 18 chip is functionally identical but has no A15.

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SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{CWEx}$	CLK0/1	Address Used	Operation
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{COE}$ must meet setup and hold times for the low–to–high transition of clock (CLK0/1).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{COE}$	I/O Status
Read	L	Data Out
Read	H	High–Z
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

6

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}5$	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{COE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
TTL Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

POWER SUPPLY CURRENTS

Parameter	Symbol	Max	Unit
AC Supply Current ($\overline{COE}$ = V_{IH}, $\overline{CCS}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	1300	mA
AC Standby Current ($\overline{COE}$ = V_{IH}, $\overline{CCS}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	340	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	(Address and Control)	C_{in}	28	pF
Input Capacitance	(CLK0, CLK1)	C_{in}	12	pF
Input/Output Capacitance	(DQ0 – DQ63)	$C_{I/O}$	10	pF

6

DATA RAMs AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

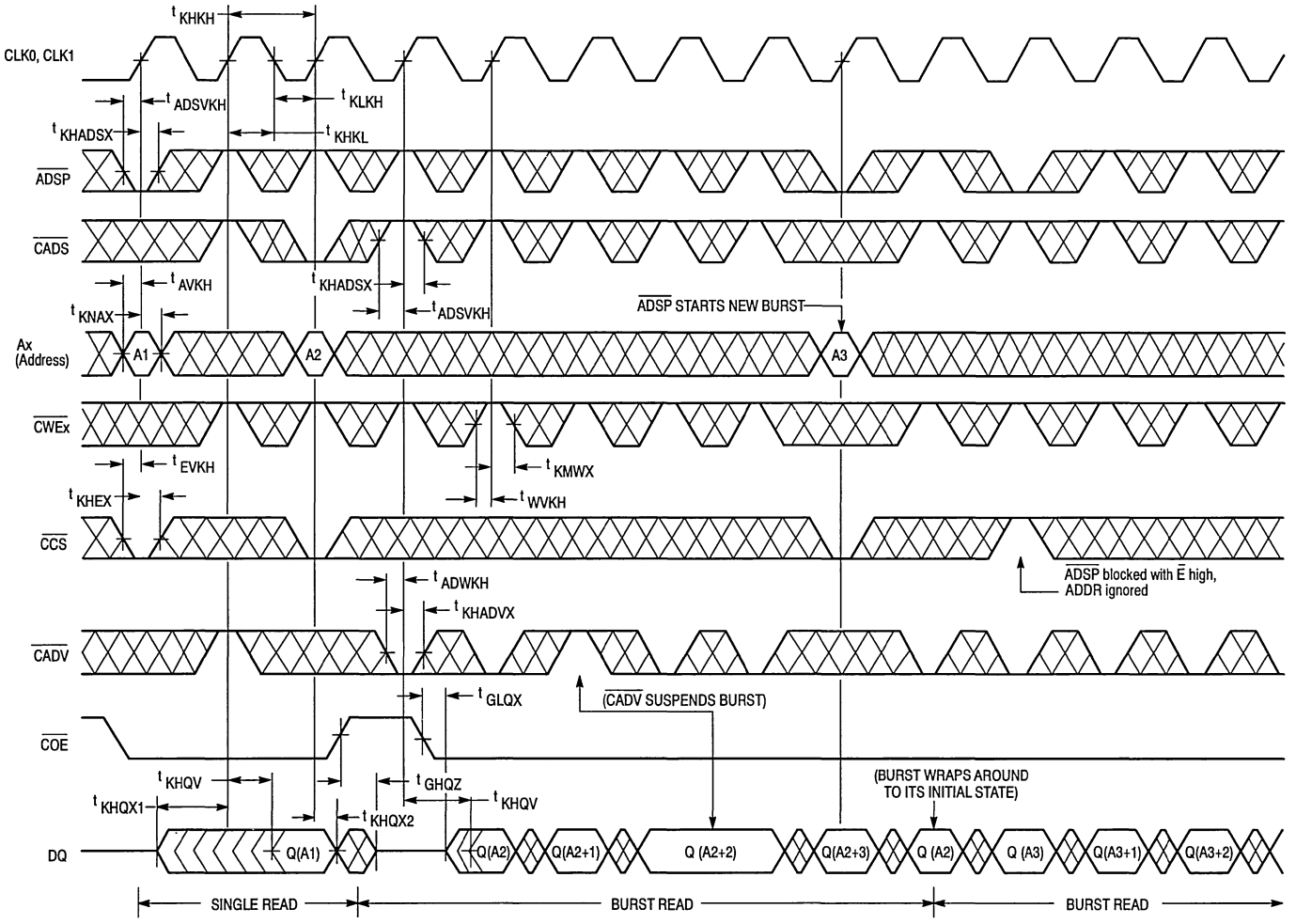
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter		Symbol	MCM72JG32–66 MCM72JG64–66 Min	Max	Unit	Notes
Cycle Time		t_{KHKH}	15	—	ns	
Clock Access Time		t_{KHQV}	—	7	ns	5
Output Enable to Output Valid		t_{GLQV}	—	5	ns	
Clock High to Output Active		t_{KHQX1}	2	—	ns	
Clock High to Output Change		t_{KHQX2}	2	—	ns	
Output Enable to Output Active		t_{GLQX}	1	—	ns	
Output Disable to Q High–Z		t_{GHQZ}	—	6	ns	6
Clock High to Q High–Z		t_{KHQZ}	2	6	ns	
Clock High Pulse Width		t_{KHKL}	5	—	ns	
Clock Low Pulse Width		t_{KLKH}	5	—	ns	
Setup Times:	Address	t_{AVKH}	2.5	—	ns	7
	Address Status	t_{ADSVKH}				
	Data In	t_{DVKH}				
	Write	t_{WVKH}				
	Address Advance	t_{ADVVKH}				
	Chip Enable	t_{EVKH}				
Hold Times:	Address	t_{KHAX}	0.5	—	ns	7
	Address Status	t_{KHADSX}				
	Data In	t_{KHDX}				
	Write	t_{KHWX}				
	Address Advance	t_{KHADVX}				
	Chip Enable	t_{KHEX}				

NOTES:
1. In setup and hold times, W (write) refers to either one or both byte write enables $\overline{LW}$ and $\overline{UW}$.
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from CLK or $\overline{COE}$.
4. $\overline{COE}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 amd Pentium external bus cycles.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of CLK whenever $\overline{ADSP}$ or $\overline{CADS}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of CLK when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{CADS}$ is low) to remain enabled.

DATA RAMs READ CYCLES



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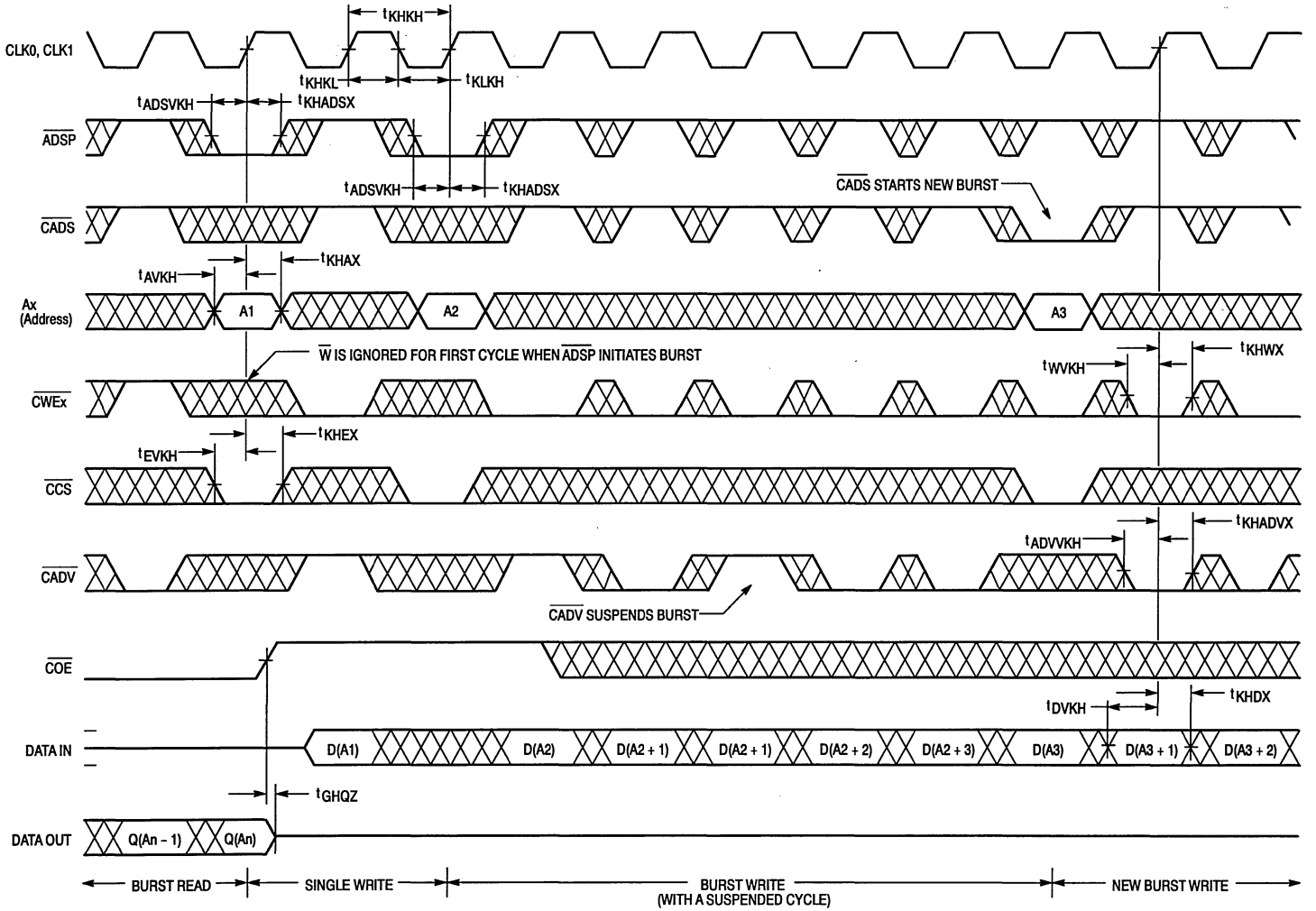
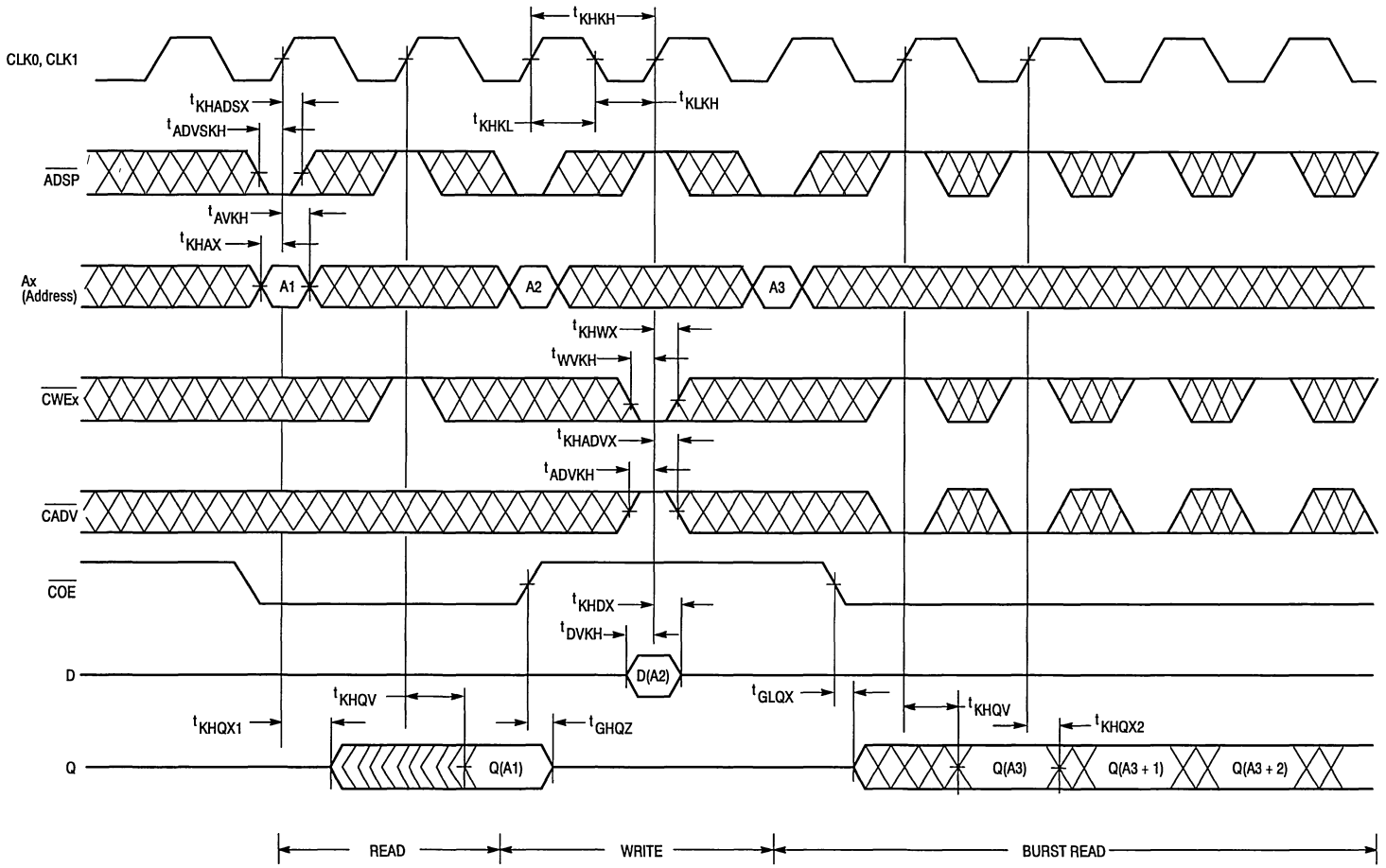
DATA RAMs WRITE CYCLES



DATA RAMs COMBINATION READ/WRITE CYCLES ($\overline{CCS}$ low, $\overline{CADS}$ high)



TAG RAM AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

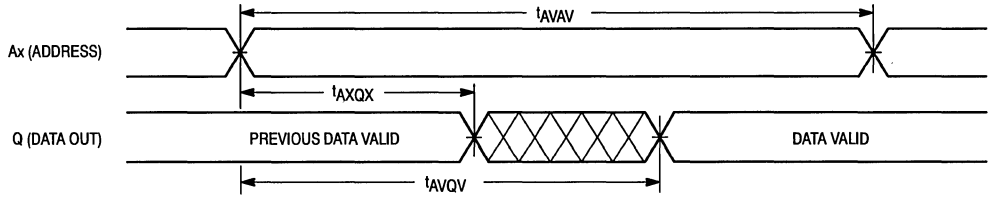
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

TAG RAM READ CYCLE (See Note 1 and 5)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Read Cycle Time	t_{AVAV}	15	—	ns	2
Address Access Time	t_{AVQV}	—	15	ns	
Output Hold from Address Change	t_{AXQX}	4	—	ns	3, 4

NOTES:
1. $\overline{CWE}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first address transition.
3. Transition is measured ±500 mV from steady–state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{COE}$ = V_{IL}).

TAG RAM READ CYCLE (See Note 5)



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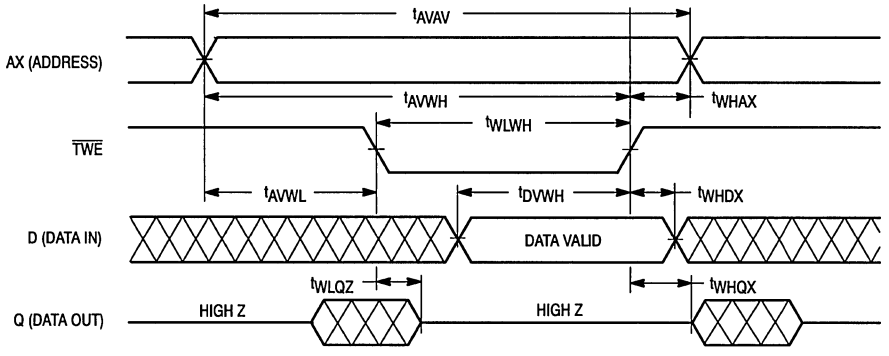
TAG RAM WRITE CYCLE (See Notes 1 and 2)

Parameter	Symbol	–15		Unit	Notes
		Min	Max		
Write Cycle Time	t_{AVAV}	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	ns	
Write Low to Output High–Z	t_{WLQZ}	0	7	ns	5,6,7
Write High to Output Active	t_{WHQX}	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	0	—	ns	

NOTES:
1. A write occurs when $\overline{CWE}$ is low.
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first address transition.
4. If $\overline{COE} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady–state voltage with load of Figure 2B.
7. This parameter is sampled and not 100% tested.

TAG RAM WRITE CYCLE (See Notes 1 and 2)



AC TEST LOADS

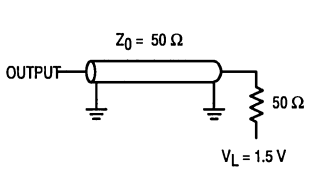


Figure 1A

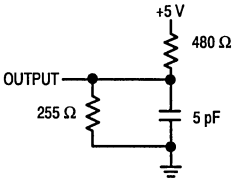


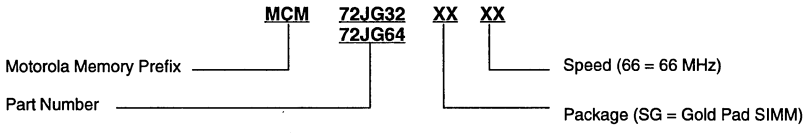
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6

ORDERING INFORMATION
(Order by Full Part Number)

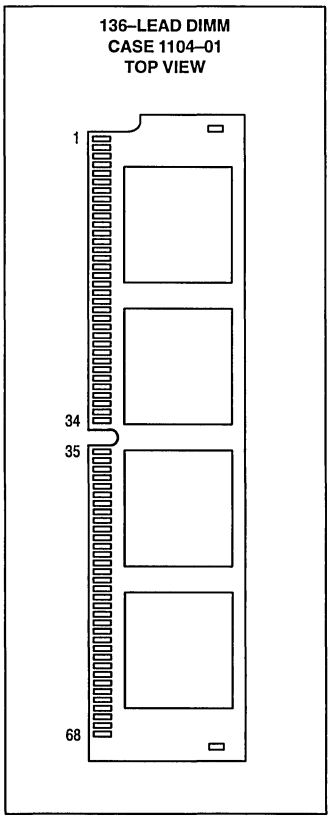


Full Part Numbers — MCM72JG32SG66 MCM72JG64SG66

6

256KB Asynchronous Secondary Cache Module for PowerPC™

MPC2001
(Formerly MCM64AC32)



The MPC2001 is designed to provide asynchronous 256KB L2 cache for the PowerPC 60x processors. The module is configured as 32K x 64 bits in a 136 pin dual readout single inline memory module (DIMM). The module uses eight of Motorola's MCM6206 CMOS RAMs.

Eight write enables are provided for byte write control.

The cache is designed to interface with the PowerPC 60x bus and requires external tag.

PD0 – PD2 are reserved for density and speed identification.

The cache is plug and pin compatible with Motorola's MPC2002 and MPC2003 BurstRAM™ synchronous cache modules.

- Dual Readout SIMM (DIMM) for Circuit Density
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Write Capability
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- Fast SRAM Access Times 12 ns, 15 ns
- Low Cost Asynchronous Solution for MPC105 PCI Bridge/Memory Controller Chip

6

BurstRAM is a trademark of Motorola.
PowerPC and PowerPC 601 are trademarks of International Business Machines Corp.

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PIN ASSIGNMENT
136–LEAD DIMM
CASE 1104–01
TOP VIEW

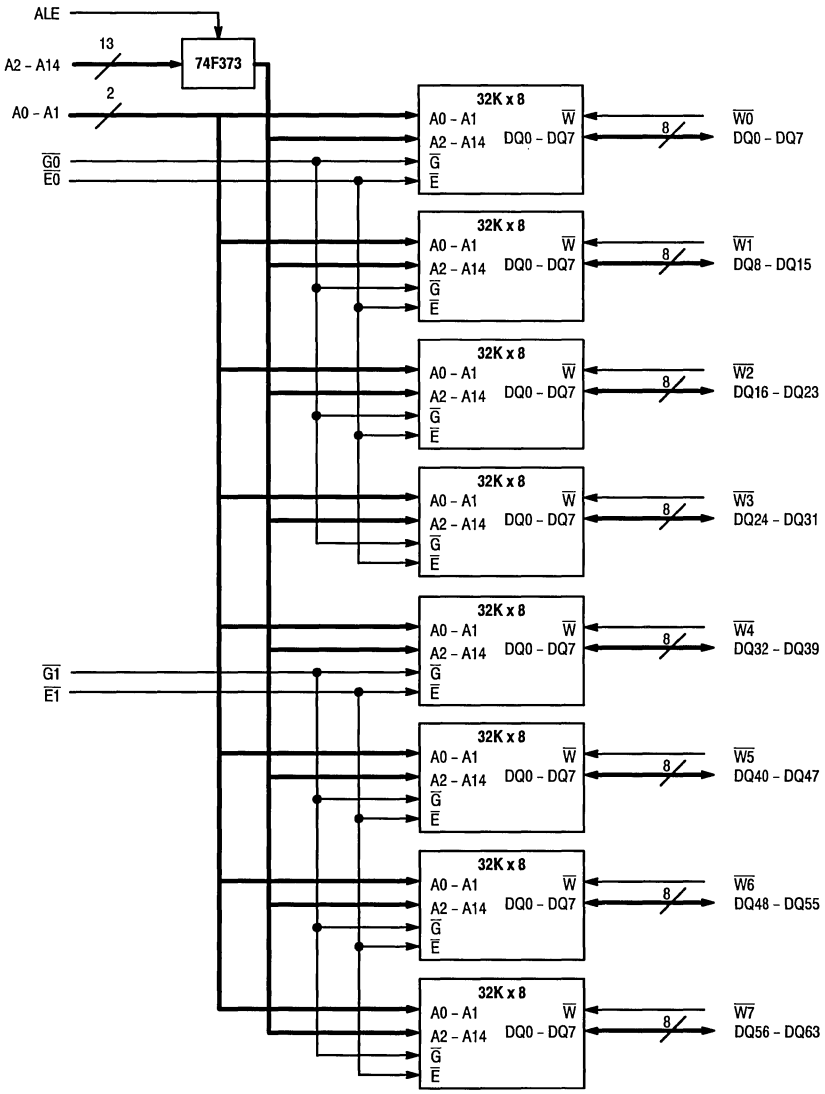
PD0	1	69	V_{SS}	$\overline{W6}$	35	103	$\overline{W7}$
PD1	2	70	PD2	DQ32	36	104	$\overline{E1}$
DQ0	3	71	V_{CC}	DQ33	37	105	DQ34
DQ1	4	72	DQ2	V_{SS}	38	106	DQ35
V_{CC}	5	73	DQ3	DQ36	39	107	DQ37
DQ4	6	74	DQ5	DQ38	40	108	V_{CC}
DQ6	7	75	DQ7	DQ39	41	109	NC
NC	8	76	V_{SS}	DQ40	42	110	DQ41
DQ8	9	77	DQ9	V_{CC}	43	111	DQ42
DQ10	10	78	DQ11	DQ43	44	112	DQ44
V_{SS}	11	79	DQ12	DQ45	45	113	V_{SS}
NC	12	80	V_{SS}	DQ46	46	114	DQ47
V_{SS}	13	81	DQ13	NC	47	115	DQ48
DQ14	14	82	DQ15	V_{SS}	48	116	DQ49
V_{CC}	15	83	NC	NC	49	117	V_{SS}
DQ16	16	84	V_{SS}	V_{SS}	50	118	DQ50
DQ17	17	85	DQ18	DQ52	51	119	DQ51
DQ19	18	86	DQ20	DQ53	52	120	DQ54
DQ21	19	87	DQ22	DQ55	53	121	DQ56
V_{CC}	20	88	DQ23	NC	54	122	V_{SS}
NC	21	89	V_{SS}	V_{CC}	55	123	DQ57
DQ24	22	90	DQ25	DQ58	56	124	DQ59
DQ26	23	91	DQ27	DQ60	57	125	DQ61
DQ28	24	92	DQ29	DQ62	58	126	DQ63
V_{SS}	25	93	DQ30	NC	59	127	V_{CC}
DQ31	26	94	V_{SS}	A0	60	128	A1
NC	27	95	$\overline{E0}$	A2	61	129	A3
V_{SS}	28	96	$\overline{W1}$	A4	62	130	A5
$\overline{W0}$	29	97	$\overline{W3}$	A6	63	131	A7
$\overline{W2}$	30	98	$\overline{G0}$	A8	64	132	ALE
NC	31	99	NC	A10	65	133	A9
NC	32	100	V_{SS}	A12	66	134	A11
V_{CC}	33	101	$\overline{G1}$	A14	67	135	A13
$\overline{W4}$	34	102	$\overline{W5}$	V_{SS}	68	136	NC

PD2	PD1	PD0	Cache Size	Module
NC	V_{SS}	NC	256KB	MPC2001SG12
NC	V_{SS}	V_{SS}	256KB	MPC2001SG15

PIN NAMES

A0 – A14	Address Inputs
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
PD0 – PD2	Presence Detect
V_{CC}	+ 5 V Power Supply
ALE	Address Latch Enable
V_{SS}	Ground
NC	No Connection

MPC2001 BLOCK DIAGRAM
Asynchronous 136 Pin DIMM



ORDERING INFORMATION
(Order by Full Part Number)

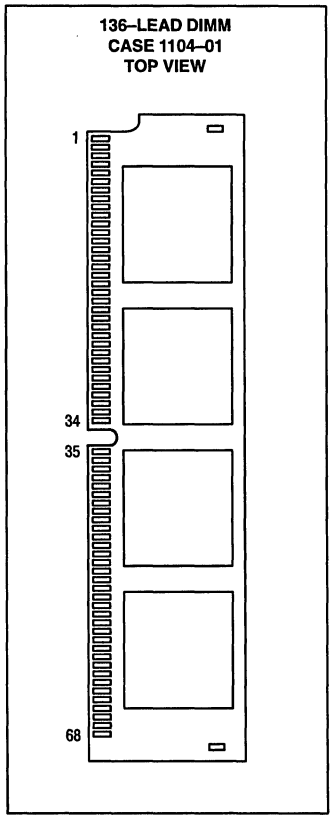
MPC	2001	XX	XX
Motorola Memory Prefix	Part Number		Package (SG = Gold Pad SIMM)
			Speed (12 = 12 ns, 15 = 15 ns)

Full Part Numbers — MPC2001SG12 MPC2001SG15

6

256KB and 512KB BurstRAM™ Secondary Cache Module for PowerPC™ – Based Systems

MPC2002
MPC2003
(Formerly MCM72MS32/64)



The MPC2002SG and MPC2003SG are designed to provide a burstable, high performance, 256K/512K L2 cache for the PowerPC 60x processors. The modules are configured as 32K x 72 and 64K x 72 bits in a 136 pin dual readout single inline memory module (DIMM). The module uses four of Motorola's MCM67M518 or MCM67M618 BiCMOS BurstRAMs.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start controller ($\overline{TSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst address advance ($\overline{BAA}$) pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with the PowerPC 60x bus and requires external tag.

PD0 – PD2 are reserved for density and speed identification.

- PowerPC–style Burst Counter on Board
- Dual Readout SIMM for Circuit Density
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz, 60 MHz, 50MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- I/Os are 3.3 V Compatible

6

BurstRAM is a trademark of Motorola.
PowerPC and PowerPC 601 are trademarks of International Business Machines Corp.

5/95

PIN ASSIGNMENT
136–LEAD DIMM
CASE 1104–01
TOP VIEW

PD0	1	69	V_{SS}	$\overline{W6}$	35	103	$\overline{W7}$
PD1	2	70	PD2	DQ32	36	104	$\overline{E1}$
DQ0	3	71	V_{CC}	DQ33	37	105	DQ34
DQ1	4	72	DQ2	V_{SS}	38	106	DQ35
V_{CC}	5	73	DQ3	DQ36	39	107	DQ37
DQ4	6	74	DQ5	DQ38	40	108	V_{CC}
DQ6	7	75	DQ7	DQ39	41	109	DQP4
DQP0	8	76	V_{SS}	DQ40	42	110	DQ41
DQ8	9	77	DQ9	V_{CC}	43	111	DQ42
DQ10	10	78	DQ11	DQ43	44	112	DQ44
V_{SS}	11	79	DQ12	DQ45	45	113	V_{SS}
K0	12	80	V_{SS}	DQ46	46	114	DQ47
V_{SS}	13	81	DQ13	DQP5	47	115	DQ48
DQ14	14	82	DQ15	V_{SS}	48	116	DQ49
V_{CC}	15	83	DQP1	K1	49	117	V_{SS}
DQ16	16	84	V_{SS}	V_{SS}	50	118	DQ50
DQ17	17	85	DQ18	DQ52	51	119	DQ51
DQ19	18	86	DQ20	DQ53	52	120	DQ54
DQ21	19	87	DQ22	DQ55	53	121	DQ56
V_{CC}	20	88	DQ23	DQP6	54	122	V_{SS}
DQP2	21	89	V_{SS}	V_{CC}	55	123	DQ57
DQ24	22	90	DQ25	DQ58	56	124	DQ59
DQ26	23	91	DQ27	DQ60	57	125	DQ61
DQ28	24	92	DQ29	DQ62	58	126	DQ63
V_{SS}	25	93	DQ30	DQP7	59	127	V_{CC}
DQ31	26	94	V_{SS}	A0	60	128	A1
DQP3	27	95	$\overline{E0}$	A2	61	129	A3
V_{SS}	28	96	$\overline{W1}$	A4	62	130	A5
$\overline{W0}$	29	97	$\overline{W3}$	A6	63	131	A7
$\overline{W2}$	30	98	$\overline{G0}$	A8	64	132	NC
$\overline{TSP}$	31	99	$\overline{TSC}$	A10	65	133	A9
$\overline{BAA}$	32	100	V_{SS}	A12	66	134	A11
V_{CC}	33	101	$\overline{G1}$	A14	67	135	A13
$\overline{W4}$	34	102	$\overline{W5}$	V_{SS}	68	136	A15*

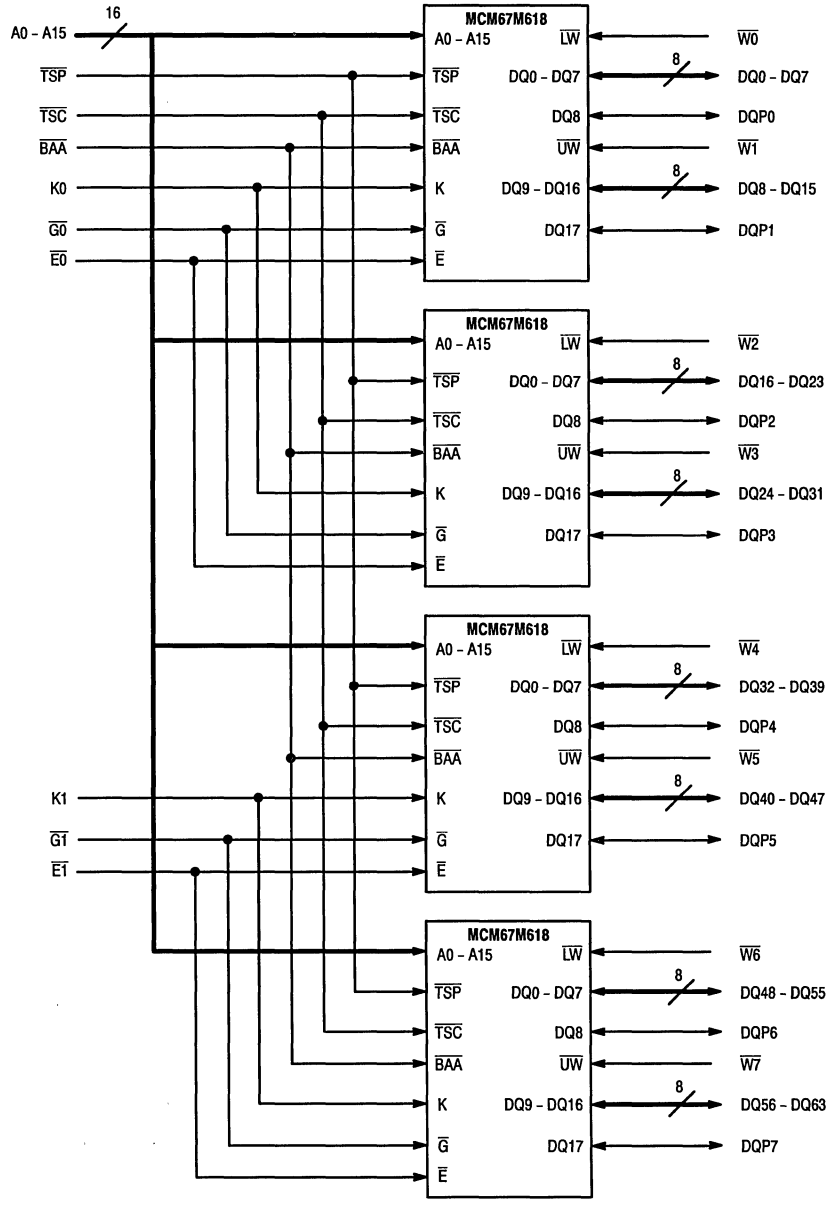
PD2	PD1	PD0	Cache Size	Module
V_{SS}	NC	NC	512KB	MPC2003SG66/60
V_{SS}	NC	V_{SS}	512KB	MPC2003SG50
V_{SS}	V_{SS}	NC	256KB	MPC2002SG66/60
V_{SS}	V_{SS}	V_{SS}	256KB	MPC2002SG50

PIN NAMES	
A0 – A15	Address Inputs
K0, K1	Clock
$\overline{W0}$ – $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 – DQ63	Cache Data Input/Output
DQP0 – DQP7	Data Parity Input/Output
$\overline{TSC}$	Transfer Start Controller
$\overline{TSP}$	Transfer Start Processor
$\overline{BAA}$	Burst Address Advance
PD0 – PD2	Presence Detect
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

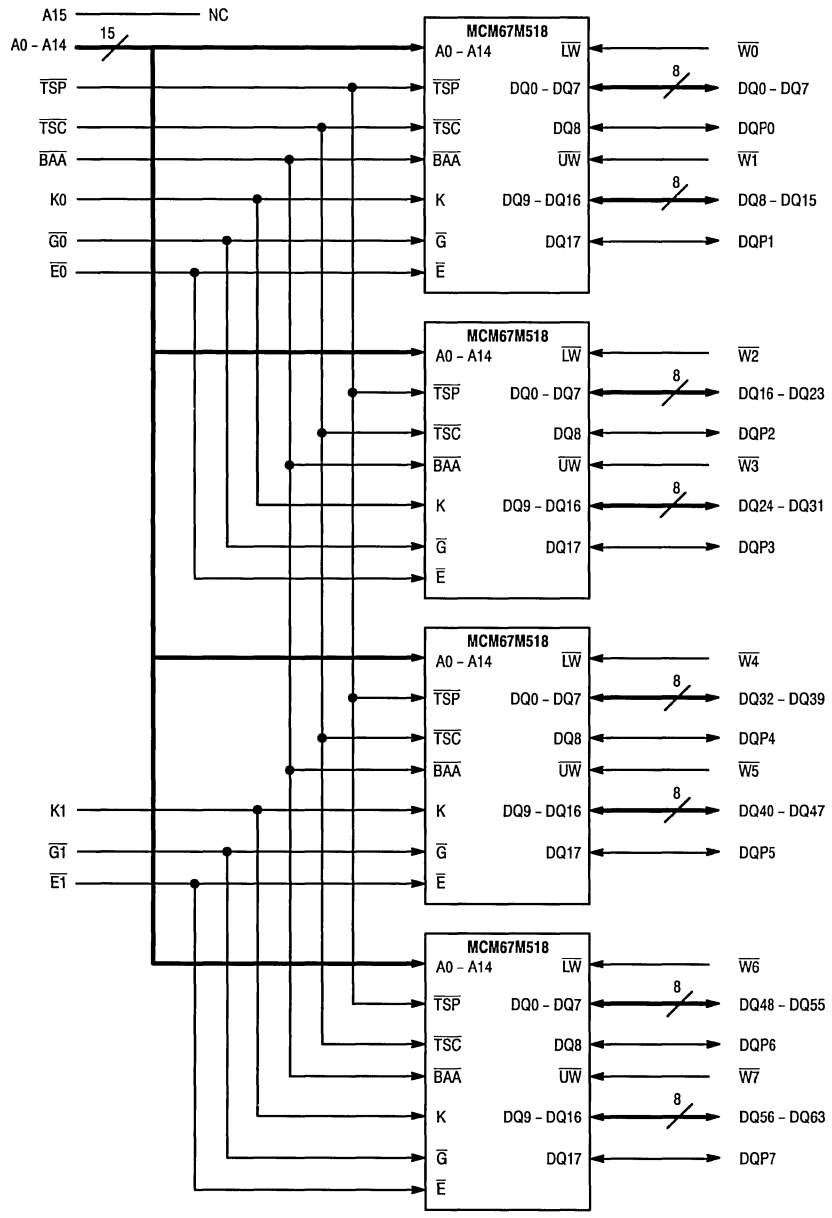
* This pin on the MPC2002 is a No Connect (NC)

6

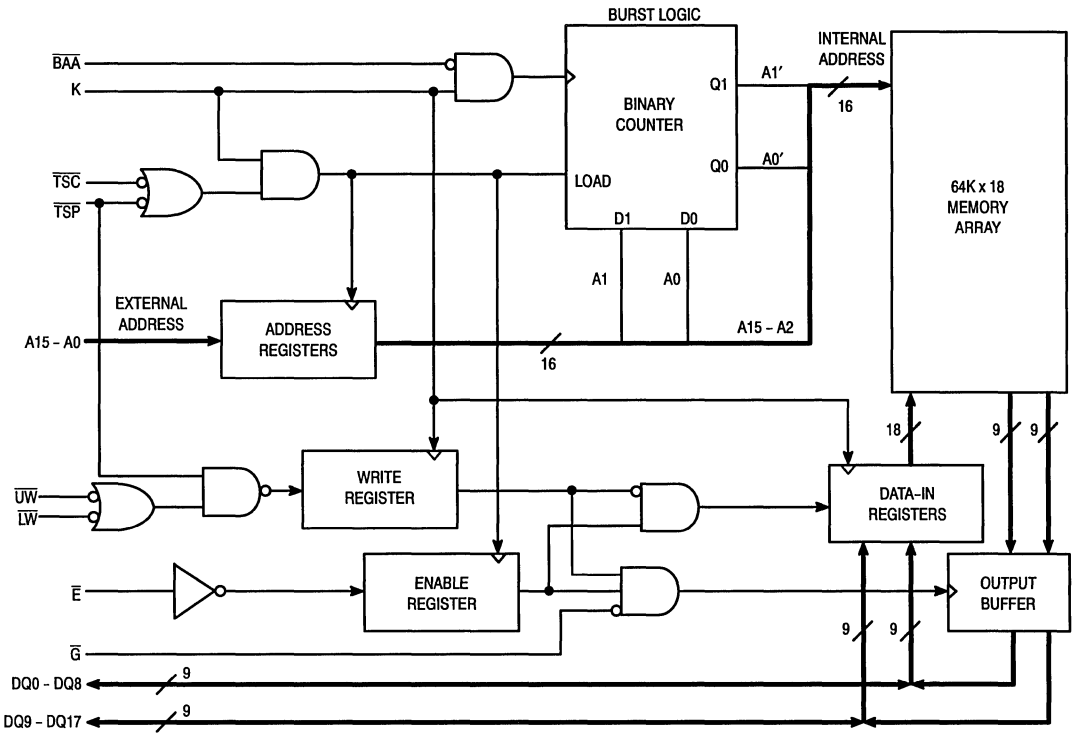
MPC2003 (64K x 72) MODULE BLOCK DIAGRAM



MPC2002 (32K x 72) MODULE BLOCK DIAGRAM

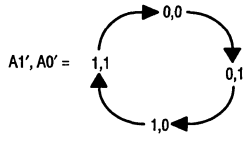


BLOCK DIAGRAM (See Note)



NOTE: All registers are positive–edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. Alternatively, a $\overline{TSP}$–initiated two cycle WRITE can be performed by asserting $\overline{TSP}$ and a valid address on the first cycle, then negating both $\overline{TSP}$ and $\overline{TSC}$ and asserting $\overline{LW}$ and/or $\overline{UW}$ with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram).
When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low–to–high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Write	X	High–Z — Data In
Deselected	X	High–Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	6.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High–Z at power up.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA66} I_{CCA60} I_{CCA50}	—	1160 1100 1000	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	300	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible PowerPC bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	(A0 – A15, $\overline{TSP}$, $\overline{TSC}$, $\overline{BAA}$)	C_{in}	25	32	pF
Input/Output Capacitance	(DQ0 – DQ63, DQP0 – DQP7)	$C_{I/O}$	8	10	pF
Input Capacitance	(Kx, $\overline{Gx}$, $\overline{Ex}$, $\overline{Wx}$)	C_{in}	12	15	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol	MPC2002SG66/ MPC2003SG66		MPC2002SG60/ MPC2003SG60		MPC2002SG50/ MPC2003SG50		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	11	—	14	ns	4
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High–Z	t_{GHQZ}	2	6	2	6	2	6	ns	5
Clock High to Q High–Z	t_{KHQZ}	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{TSVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible PowerPC 60x external bus cycles.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

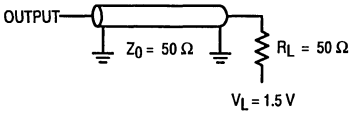


Figure 1A

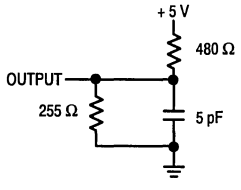
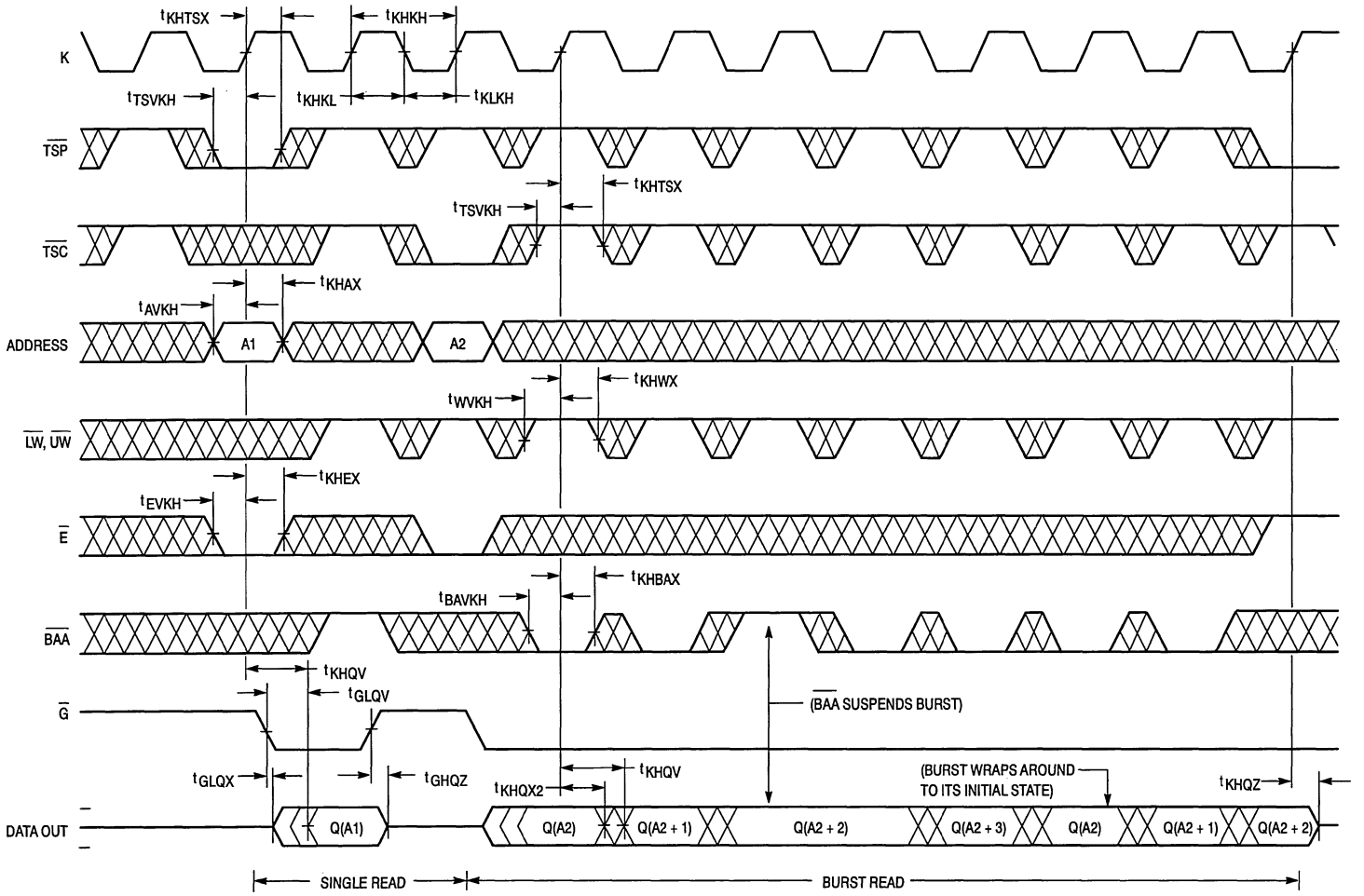


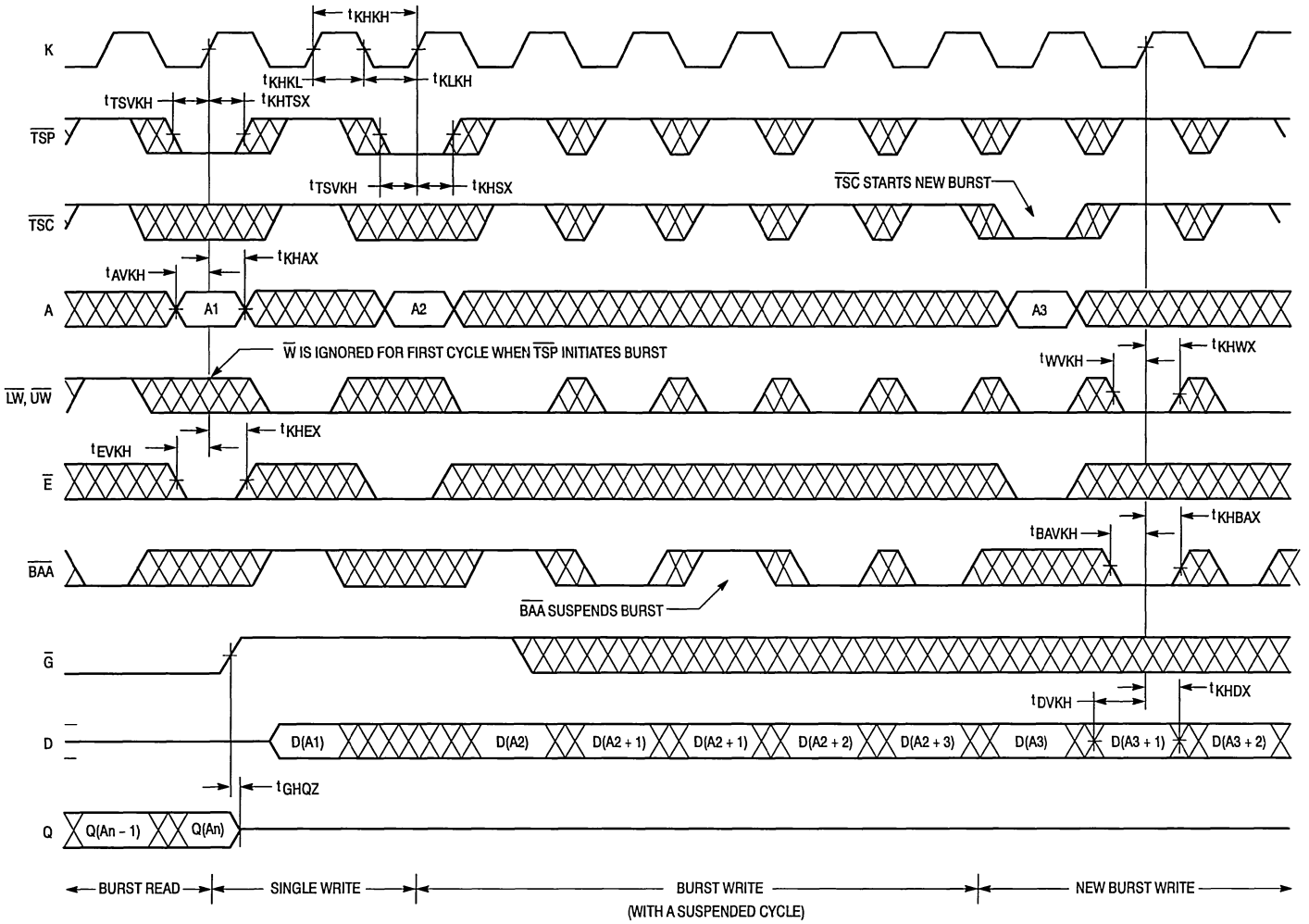
Figure 1B

READ CYCLES

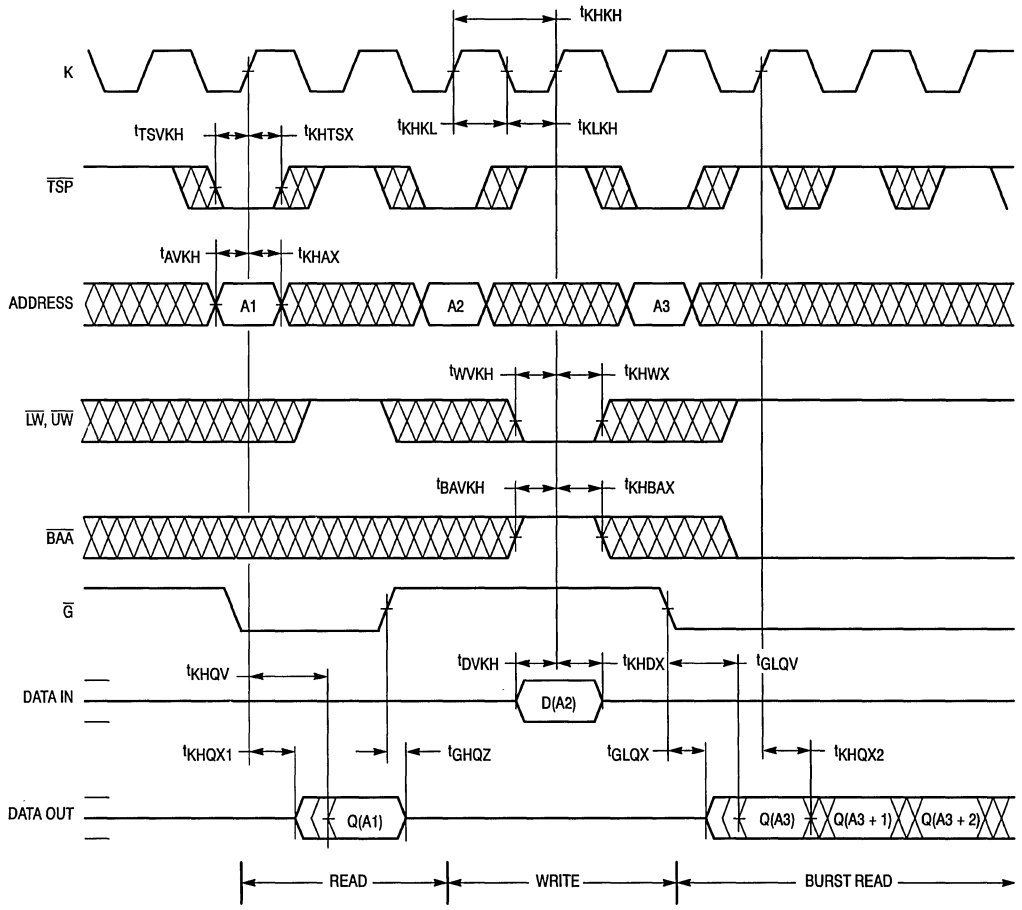


NOTE: Q(A2) represents the first output data from the base address A2; Q(A2 + 1) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE ($\overline{E}$ low, $\overline{TSC}$ high)



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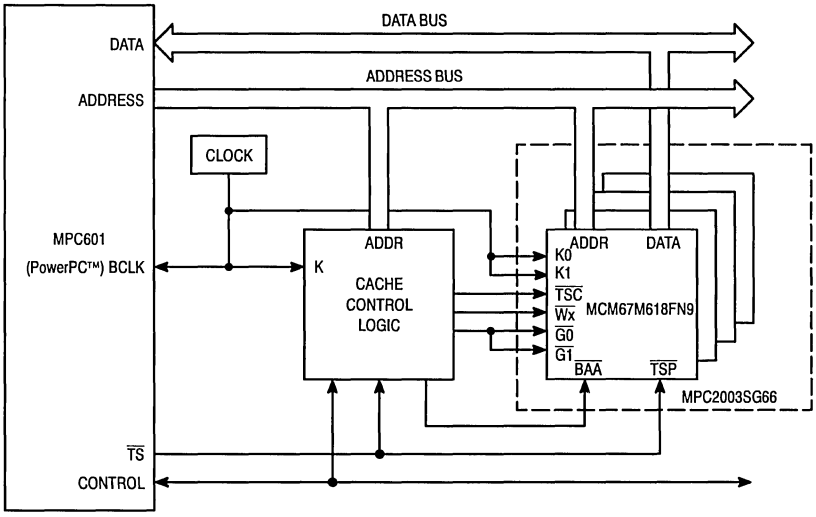
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using MPC2003SG66 with a 66 MHz MPC601 PowerPC™

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)

MPC2002
MCM MPC2003 XX XX

Motorola Memory Prefix
Part Number
Speed (66 = 66 MHz, 60 = 60 MHz, 50 = 50 MHz)
Package (SG = Gold Pad SIMM)

Full Part Numbers —	MPC2002SG66	MPC2002SG60	MPC2002SG50
	MPC2003SG66	MPC2003SG60	MPC2003SG50

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MPC2004
MPC2005

Advance Information

256KB and 512KB BurstRAM™ Secondary Cache Modules for PowerPC™ PReP/CHRP Platforms

The MPC2004 and MPC2005 are designed to provide burstable, high performance 256KB/512KB L2 cache for the PowerPC 60x microprocessor family in conformance with the PowerPC Reference Platform (PReP) and the PowerPC Common Hardware Reference Platform (CHRP) specifications. The modules are configured as 32K x 72 and 64K x 72 bits in a 182 (91 x 2) pin DIMM format. Each module uses four of Motorola's 5 V 32K x 18 or 64K x 18 BurstRAMs and a 5 V cache tag RAM configured as 16K x 12 for tag field plus 16K x 2 for valid and dirty status bits.

Bursts can be initiated with the $\overline{\text{SRAMADS}}$ signal. Subsequent burst addresses are generated internal to the BurstRAM by the $\overline{\text{SRAMCNTEN}}$ signal.

Write cycles are internally self timed and are initiated by the rising edge of the clock (CLKx) inputs. Eight write enables are provided for byte write control.

Presence detect pins are available for auto configuration of the cache control. A serial EEPROM is optional to provide more in–depth description of the cache module.

The module family pinout will support 5 V and 3.3 V components for a clear path to lower voltage and power savings. Both power supplies must be connected.

These cache modules are plug and pin compatible with the MPC2006, a 1MB synchronous module also designed for the PReP and CHRP specifications. They are also compatible with the MPC2007 and MPC2009, 256KB and 1MB respectively, asynchronous cache modules.

- PowerPC–style Burst Counter on Chip
- Flow–Through Data I/O
- Module Requires Both 3.3 V and 5 V Power Supplies
- Multiple Clock Pins for Reduced Loading
- All Cache Data and Tag I/Os are LVTTL (3.3 V) Compatible
- Three State Outputs
- Byte Write Capability
- Fast Module Clock Rates: 66 MHz
- Fast SRAM Access Times: 10 ns for Tag RAM Match
  9 ns for Data RAM
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi–Layer FR4 PWB With Separate Power and Ground Planes
- 182 Pin Card Edge Module
- Burndy Connector, Part Number: ELF182JSC–3Z50

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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PIN ASSIGNMENT
182–LEAD DIMM
TOP VIEW – CASE TBD

GND	92	1	GND
PD1/IDSDATA	93	2	PD0/IDSCLK
PD3	94	3	PD2
DH31	95	4	DH30
DH29	96	5	DH28
DH27	97	6	DH26
DH25	98	7	DH24
$V_{CC}3$	99	8	$V_{CC}3$
$\overline{SRAMWE3}$	100	9	DP3
DH23	101	10	DH22
DH21	102	11	DH20
DH18	103	12	DH19
GND	104	13	GND
DH16	105	14	DH17
$\overline{SRAMWE2}$	106	15	DP2
DH14	107	16	DH15
DH13	108	17	DH12
$V_{CC}5$	109	18	$V_{CC}5$
DH10	110	19	DH11
DH8	111	20	DH9
$\overline{SRAMWE1}$	112	21	DP1
DH6	113	22	DH7
$V_{CC}3$	114	23	$V_{CC}3$
DH4	115	24	DH5
GND	116	25	DH3
CLK0	117	26	DH2
GND	118	27	DH0
DH1	119	28	DP0
$\overline{SRAMWE0}$	120	29	GND
DL31	121	30	CLK1
DL30	122	31	GND
GND	123	32	DL28
DL29	124	33	DL2C
DL27	125	34	DL24
DL25	126	35	DP7
$V_{CC}5$	127	36	$V_{CC}5$
$\overline{SRAMWE7}$	128	37	DL22
DL23	129	38	DL20
DL21	130	39	DL18
DL19	131	40	DL16
GND	132	41	GND
DL17	133	42	DP6
$\overline{SRAMWE6}$	134	43	DL14
DL15	135	44	DL12
DL13	136	45	DL11
GND	137	46	GND
DL10	138	47	DL9
DL8	139	48	DP5
$\overline{SRAMWE5}$	140	49	DL7
DL6	141	50	DL4
$V_{CC}3$	142	51	$V_{CC}3$
DL5	143	52	DL3
DL2	144	53	DL1
GND	145	54	DL0
(CLK3) NC	146	55	GND
GND	147	56	CLK2
(CLK4) NC	148	57	GND
GND	149	58	DP4
$\overline{SRAMWE4}$	150	59	$\overline{SRAMOE0}$
(SRAMALE) NC	151	60	NC (SRAMOE1)
$V_{CC}3$	152	61	$V_{CC}3$
(ADDR1A) NC	153	62	NC (ADDR0A)
(ADDR1B) NC	154	63	NC (ADDR0B)
$\overline{SRAMCNTEN0}$	155	64	$\overline{SRAMADS0}$
(SRAMCNTEN1) NC	156	65	NC ($\overline{SRAMADS1}$)
$V_{CC}5$	157	66	$V_{CC}5$
$V_{CC}5$	158	67	$V_{CC}5$
A27	159	68	A28
A24	160	69	A26
A22	161	70	A25
A20	162	71	A23
GND	163	72	GND
A18	164	73	A21
A16	165	74	A19
A15	166	75	A17
A14	167	76	A13 (See Note 1)
$V_{CC}3$	168	77	$V_{CC}3$
A10	169	78	NC (A12)
A8	170	79	A11
A6	171	80	A9
GND	172	81	GND
A4	173	82	A7
A2	174	83	A5
A1	175	84	A3
RESERVED	176	85	A0
$V_{CC}5$	177	86	$V_{CC}5$
TAG VALID	178	87	$\overline{TAGCLR}$
$\overline{TAGWE}$	179	88	TAG MATCH
STANDBY	180	89	$\overline{TAGOE}$
DIRTYOUT	181	90	DIRTYIN
GND	182	91	GND

NOTES:
1. This pin on the MPC2004 is a No Connect (NC).
2. Signal names in (parentheses) are NC on MPC2004 and MPC2005, but are actual signals on other modules in the MPC200x family.
3. All power pins ($V_{CC}5$, $V_{CC}3$) must be connected to appropriate supplies.

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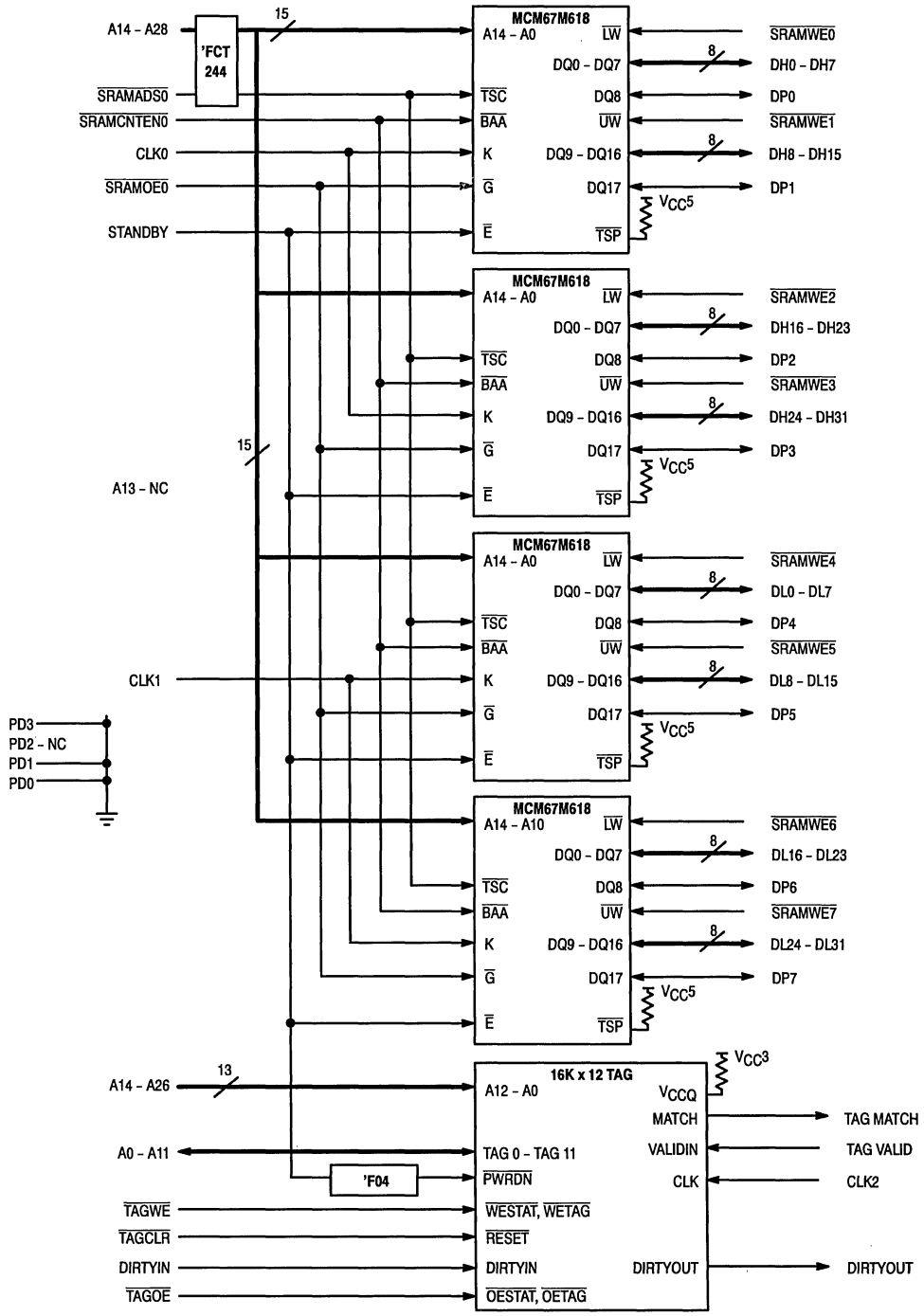
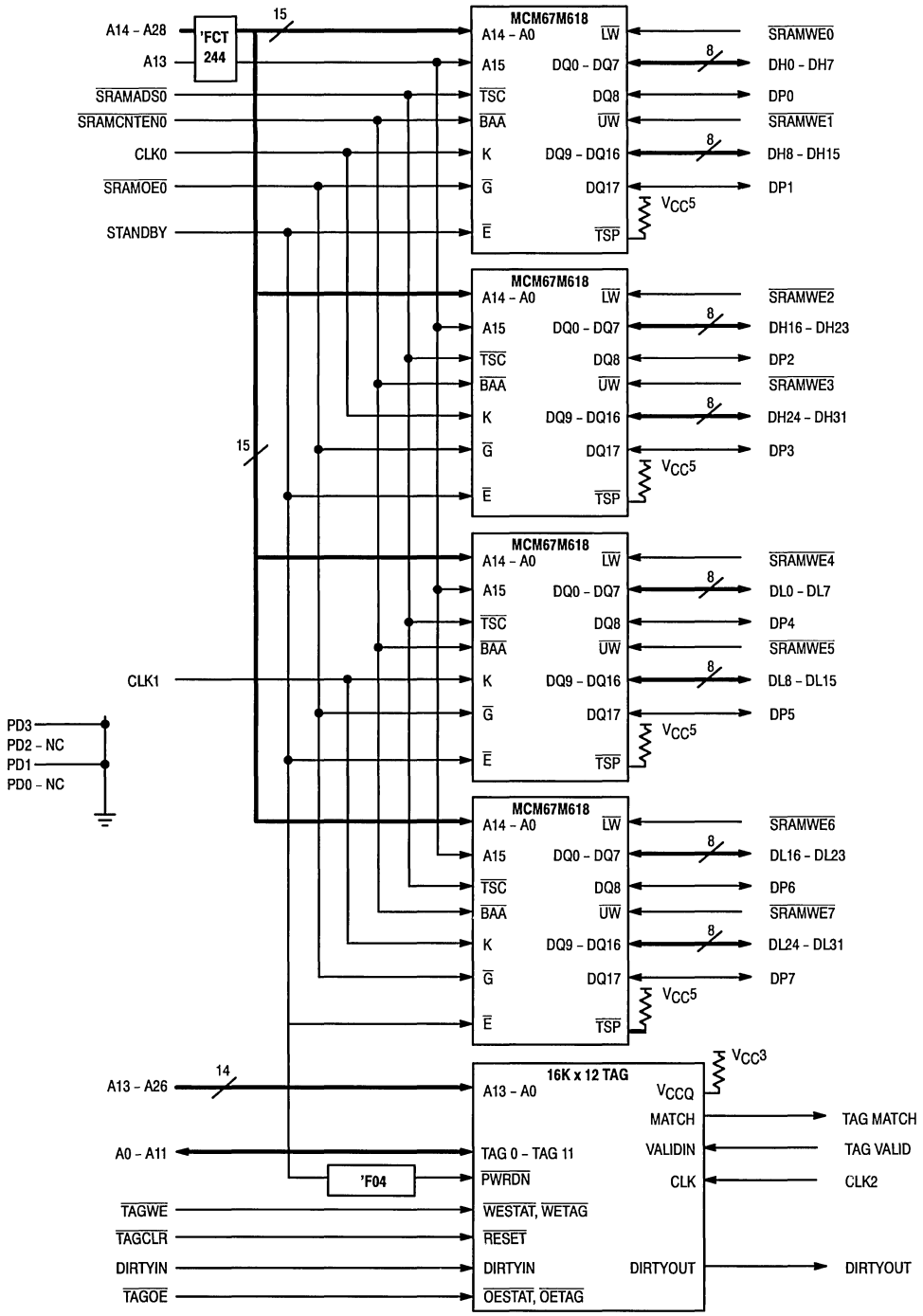
MPC2004 (32K x 72) BurstRAM MEMORY BLOCK DIAGRAM



MPC2005 (64K x 72) BurstRAM MODULE BLOCK DIAGRAM



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PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
68, 69, 70, 71, 73, 74, 75, 76, 78, 79, 80, 82, 83, 84, 85, 159, 160, 161, 162, 164, 165, 166, 167, 169, 170, 171, 173, 174, 175	A0 – A28	Input	Address Inputs – (MSB:0, LSB:28)
62, 63	ADDR0A, ADDR0B	Input	Least significant address bit when asynchronous SRAMs are used.
153, 154	ADDR1A, ADDR1B	Input	Next to least significant address bit when asynchronous SRAMs are used.
30, 56, 117, 146, 148	CLK0 – CLK4	Input	Clock Inputs – CLK2 is for Tag RAM, CLK0, 1, 3, and 4 are for SRAMs. For 1MB use all the clocks. For 512KB or less us CLK0–CLK2 only.
4, 5, 6, 7, 10, 11, 12, 14, 16, 17, 19, 20, 22, 24, 25, 26, 27, 95, 96, 97, 98, 101, 102, 103, 105, 107, 108, 110, 111, 113, 115, 119	DH0 – DH31	I/O	High Data Bus – (MSB:0, LSB:31)
32, 33, 34, 37, 38, 39, 40, 43, 44, 45, 47, 49, 50, 52, 53, 54, 121, 122, 124, 125, 126, 129, 130, 131, 133, 135, 136, 138, 139, 141, 143, 144	DL0 – DL31	I/O	Low Data Bus – (MSB:0, LSB:31)
9, 15, 21, 28, 35, 42, 48, 58	DP0 – DP7	I/O	Data Parity Bus – (MSB:0, LSB:7)
3, 94	PD2, PD3	Output	Presence detect bits 2 and 3.
2	PD0/IDSCLK	Input	Presence detect bit 0/EEPROM serial clock.
93	PD1/IDSDATA	I/O	Presence detect bit 1/EEPROM serial data.
64, 65	$\overline{\text{SRAMADS0}}$, $\overline{\text{SRAMADS1}}$	Input	SRAM Address Strobe – For 512KB or less us $\overline{\text{SRAM}}$ $\overline{\text{ADS0}}$ only.
151	SRAM ALE	Input	SRAM Address Latch Enable – Use for asynchronous SRAM only.
155, 156	$\overline{\text{SRAMCNTEN0}}$, $\overline{\text{SRAMCNTEN1}}$	Input	SRAM Count Enables – For 512KB or less use $\overline{\text{SRAM}}$ $\overline{\text{CNT}}$ $\overline{\text{EN0}}$ only.
59, 60	$\overline{\text{SRAMOE0}}$, $\overline{\text{SRAMOE1}}$	Input	SRAM Output Enables – For 512KB or less use $\overline{\text{SRAM}}$ $\overline{\text{OE0}}$ only.
100, 106, 112, 120, 128, 134, 140, 150	$\overline{\text{SRAMWE0}}$ – $\overline{\text{SRAMWE7}}$	Input	SRAM Write Enables – (MSB:0, LSB:7)
87	$\overline{\text{TAGCLR}}$	Input	Tag RAM clear.
88	TAG MATCH	Output	Tag RAM match indication.
178	TAG VALID	Input	Tag RAM valid bit.
179	$\overline{\text{TAGWE}}$	Input	Tag RAM write enable.
89	$\overline{\text{TAGOE}}$	Input	Tag RAM output enable.
90	DIRTYIN	Input	Dirty input bit.
181	DIRTYOUT	Output	Dirty output bit.
180	STANDBY	Input	Standby pin. Reduces standby power consumption.
176	RESERVED		Reserved pin.
8, 23, 51, 61, 77, 99, 114, 142, 152, 168	$V_{CC}3$	Input	+ 3.3 V power supply.

Pin Locations	Symbol	Type	Description
18, 36, 66, 67, 86, 109, 127, 157, 158, 177	$V_{CC}5$	Input	+ 5 V power supply.
1, 13, 29, 31, 41, 46, 55, 57, 72, 81, 91, 92, 104, 116, 118, 123, 132, 137, 145, 147, 149, 163, 172, 182	GND	Input	Ground

Reliability Information

7

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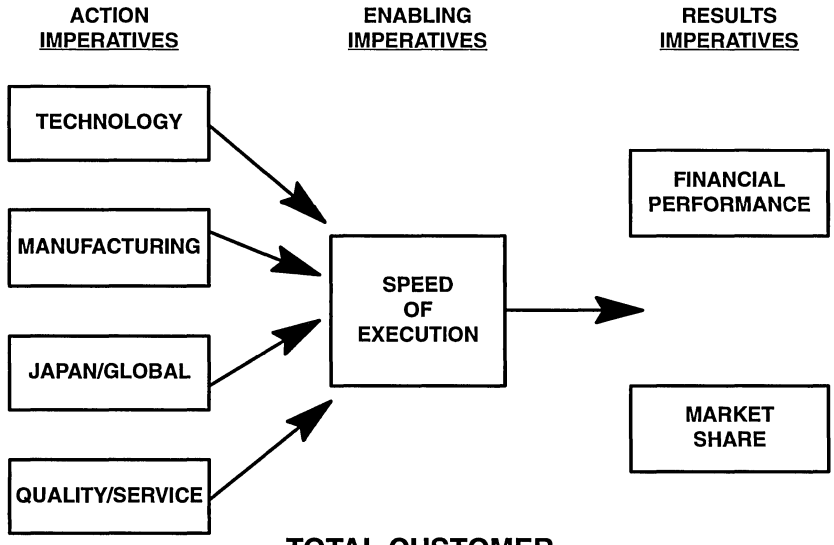
MOTOROLA
SEMICONDUCTOR PRODUCTS SECTOR
IMPERATIVES



TOTAL CUSTOMER SATISFACTION

DIVISION QUALITY STATEMENT

MOTOROLA FAST STATIC RAM PRODUCTS DIVISION

The Fast Static RAM Products Division is committed to being a world class CMOS, BiCMOS, Application Specific, and Module Fast Static RAM supplier. This means the integration of outstanding product and technology designs, linked with excellent manufacturing, cycle time, customer service, and engineering analysis.

This will be accomplished through dedication to a continuous quality improvement culture that will ensure our success in reaching the Motorola Corporate goal of total customer satisfaction.

We trust that you will experience Motorola Fast Static RAM Products Division as the best memory supplier through WORLD CLASS product performance and services.

Thomas Conn
Vice–President and General Manager
Fast Static RAM Division
Microprocessor and Memory Technologies Group

Michael Phillips
Director, Reliability and Quality Assurance
MOS Memory Products
Microprocessor and Memory Technologies Group

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QUALITY SYSTEMS

Motorola Fast Static RAM Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on a timely basis. The Fast Static RAM Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that the Fast Static Ram Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all Fast Static RAM devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proven accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to these criteria and the use of control devices ensure that the test results are valid and meaningful.

New Fast Static RAM devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, design, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola Fast Static RAM products, our customers can benefit from joint qualification activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend the qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero defects. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \bullet (\text{Lot Acceptance Rate}) \bullet (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices*}}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \bullet \text{Lot Size}$$

$$\text{Total Number of Devices} = \text{Sum of all the units in each submitted lot}$$

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

*10^6 = Conversion to parts per million (PPM)

The chart in Figure 1 indicates the product Average Outgoing Quality performance as measured in parts per million.

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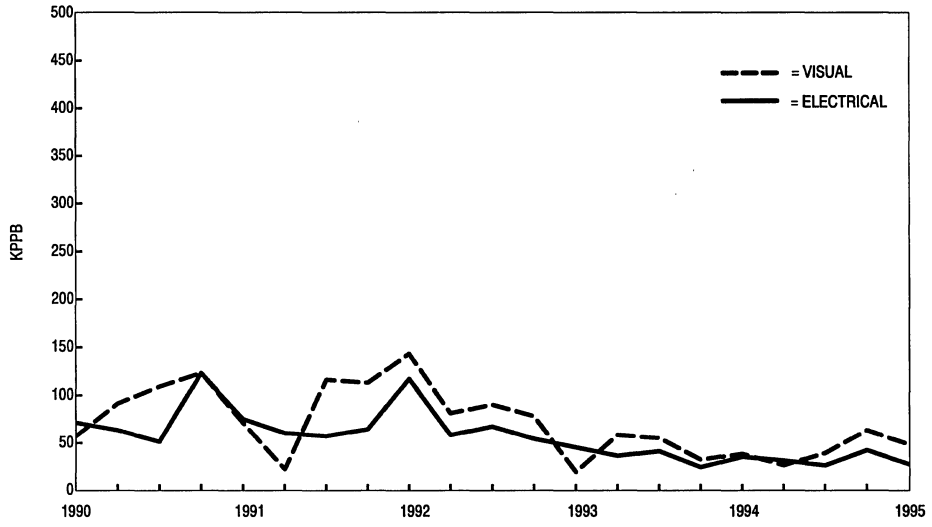

Figure 1. FSRAM AOQ

STATISTICAL PROCESS CONTROL

Motorola's Fast Static RAM Products Division is continually pursuing new ways to improve product quality. Initial design improvement is one method that can be used to produce a superior product. Equally important to outgoing product quality is the ability to produce product that consistently conforms to specification. Process variability is the basic enemy of semiconductor manufacturing since it leads to product variability. Used in all phases of Motorola's product manufacturing, STATISTICAL PROCESS CONTROL (SPC) replaces variability with predictability. The traditional philosophy in the semiconductor industry has been adherence to the data sheet specification. Using SPC methods ensures that the product will meet specific process requirements throughout the manufacturing cycle. The emphasis is on defect prevention, not detection. Predictability through SPC methods requires the manufacturing culture to focus on constant and permanent improvements. Usually, these improvements cannot be bought with state-of-the-art equipment or automated factories. With quality in design, process, and material selection, coupled with manufacturing predictability, Motorola produces world class products.

The immediate effect of SPC manufacturing is predictability through process controls. Product centered and distributed well within the product specification benefits Motorola with fewer rejects, improved yields, and lower cost. The direct benefit to Motorola's customers includes better incoming quality levels, less inspection time, and ship-to-stock capability. Circuit performance is often dependent on the cumulative effect of component variability. Tightly controlled component distributions give the customer greater circuit predictability. Many customers are also converting to just-in-time (JIT) delivery programs. These programs require improvements in cycle time and yield predictability achievable only through SPC techniques. The benefit derived from SPC helps the manufacturer meet the customer's expectations of higher quality and lower cost product.

Ultimately, Motorola will have Six Sigma capability on all products. This means parametric distributions will be centered within the specification limits, with a product distribution of plus or minus Six Sigma about mean. Six Sigma capability, shown graphically in Figure 2, details the benefit in terms of yield and outgoing quality levels. This compares a centered distribution versus a 1.5 sigma worst case distribution shift.

New product development at Motorola requires more robust design features that make them less sensitive to minor variations in processing. These features make the implementation of SPC much easier.

Standard Deviations From Mean

Distribution Centered	Distribution Shifted ± 1.5
At ± 3 σ 2700 ppm defective 99.73% yield	66810 ppm defective 93.32% yield
At ± 4 σ 63 ppm defective 99.9937% yield	6210 ppm defective 99.379% yield
At ± 5 σ 0.57 ppm defective 99.999943% yield	233 ppm defective 99.9767% yield
At ± 6 σ 0.002 ppm defective 99.9999998% yield	3.4 ppm defective 99.99966% yield

Figure 2. Percent Defective and Yield from a Normal Distribution of Product with 6σ Capability

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235 to 260°C solder dip and microscope inspection of the leads.

RELIABILITY STRESS TESTS

The following summary briefly describes the various reliability tests included in the Motorola reliability monitor program.

DYNAMIC EARLY FAIL STUDY

This stress is performed to accelerate infant mortality failure mechanisms, which are defects that occur within the first year of normal device operation. Typical stress is a temperature of 125°C, nominal voltage (6.5 V), and a duration of 72 hours. All devices used in this test are sampled directly after the standard production final test flow with no prior burn-in or other prescreening, unless called out in the normal production flow.

DYNAMIC AND STATIC LONG TERM LIFETEST

Both Dynamic and Static Long Term Lifetests are performed to accelerate failure mechanisms and access parametric shifts, which are voltage and thermally activated. This is done through the application of extreme temperatures and the use of biased operating conditions. Typical stress temperature is 125°C with the bias applied being equal to or greater than the data sheet nominal value. All devices used in the long term lifetest are sampled from the Dynamic Early Fail Study. Testing is either performed with dynamic signals applied to the devices or in a static bias configuration for a test duration of 1008 hours.

TEMPERATURE CYCLE

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of – 65 to + 150°C for a duration of 500 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperature.

THERMAL SHOCK

The objective of this test is the same as that for Temperature Cycle testing: to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress because the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed to minimum and maximum temperatures of – 65 to + 150°C for a duration of 500 cycles. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

TEMPERATURE HUMIDITY BIAS (THB)

This is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Typical stress duration is 1008 hours.

PRESSURE TEMPERATURE HUMIDITY BIAS (PTHB)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions employed during this test are a temperature of 148°C, humidity of 90%, 44 psig, and a nominal static bias voltage. Typical stress duration is 72 hours.

SMT PRECONDITIONING STRESS

The purpose of this test is to simulate the manufacturing steps involved in mounting and reworking a surface mount device used in customer applications. The test consists of simulating ambient moisture absorption by the device followed by exposure to temperatures typical of solder reflow. Devices are exposed to 85°C/85% relative humidity until saturated (non-moisture sensitive devices) or 30°C/60% relative humidity (moisture sensitive devices) followed by four passes of vapor phase reflow (215°C) for 120 seconds per pass. This test method meets all requirements of Jedec A113.

AUTOCLAVE

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 96 hours.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

Applications Information

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TYPICAL OPERATING CURVES

The terminated transmission line (T-line) shown in Figure 1A of the data sheets represents the actual test environment seen by the device under test (DUT). Because these SRAMs have fast edge rates (ranging from 1.0 V/ns to 3.0 V/ns), transmission line effects are encountered in the test environment. For the purpose of maintaining signal integrity, a 50 Ω termination is placed at the far end (tester's input) of the 50 Ω T-line. All of Motorola's Fast SRAM's output buffers have been designed to supply high current (> 50 mA) demanded by both the 50 Ω test environment as well as heavily capacitive system applications.

Although this test load may closely represent the load in your design, you may wish to simulate the SRAM's performance in your system. For this reason, a SPICE output buffer model is available upon request from the factory.

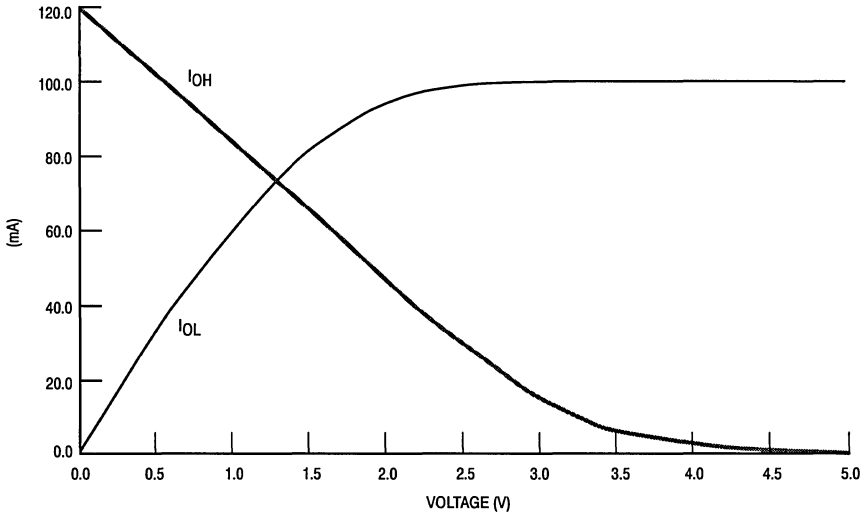

Figure 1. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6226A, MCM6227A, MCM6229A

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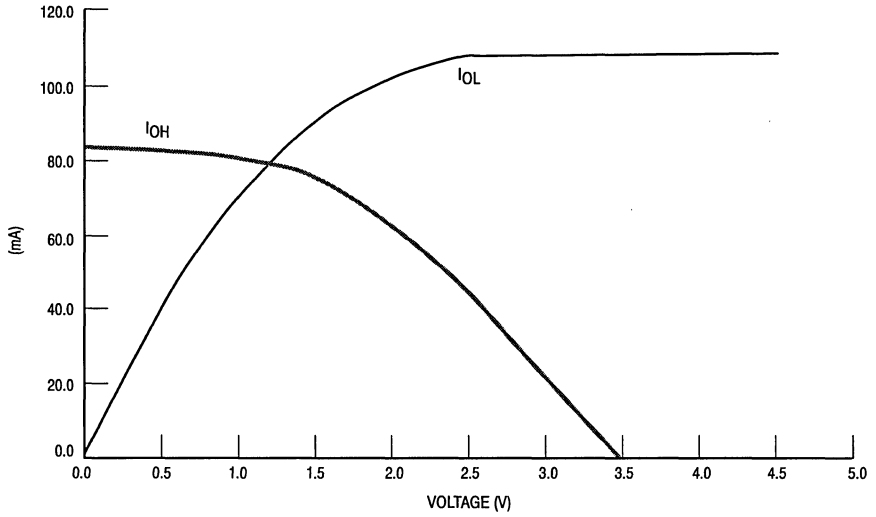

Figure 2. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6726A, MCM6728A, MCM6729A

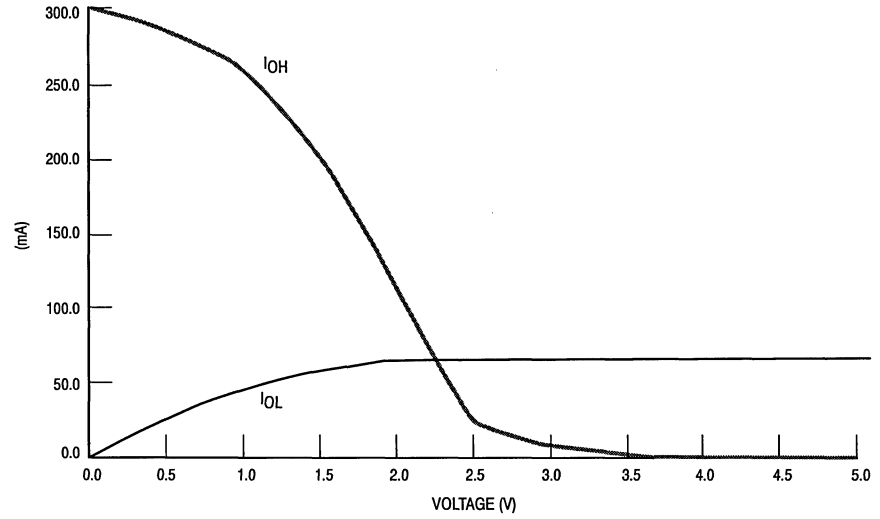

Figure 3. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6705A, MCM6706A, MCM6708A, MCM6709A

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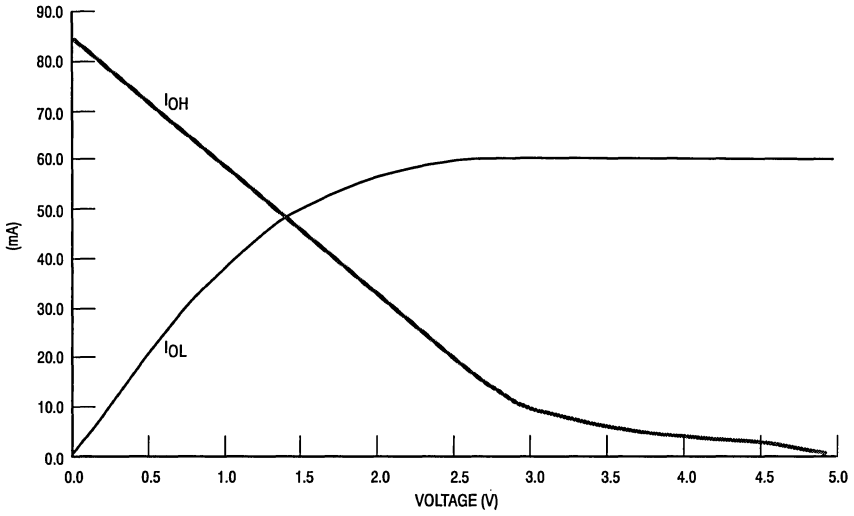

Figure 4. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6208C, MCM6209C, MCM6288C

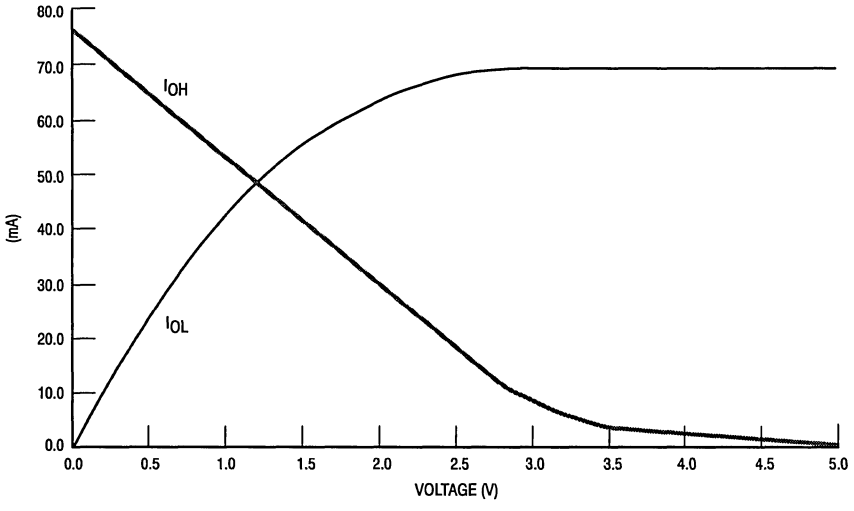

Figure 5. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6205C, MCM6206C, MCM6264C, MCM6265C, MCM56824A, MCM56824AZP

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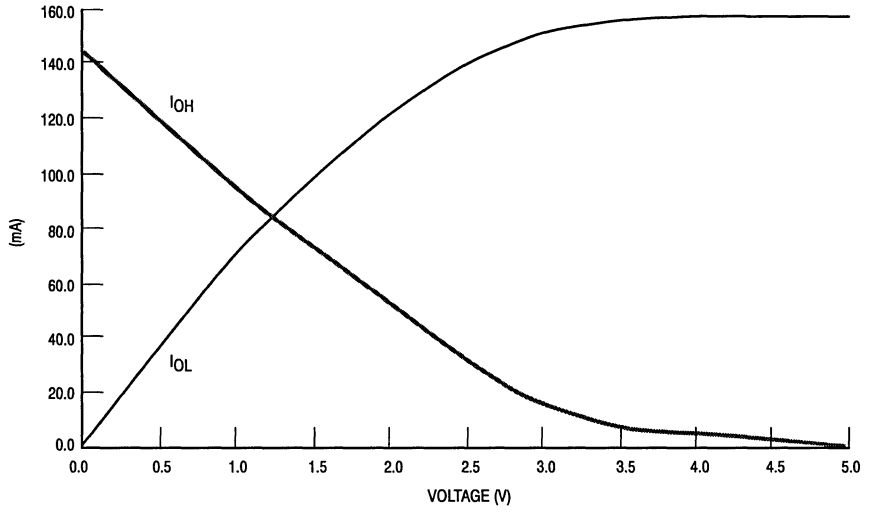

Figure 6. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM62110, MCM62486A, MCM62940A, MCM62990A, MCM62995A, MCM62996

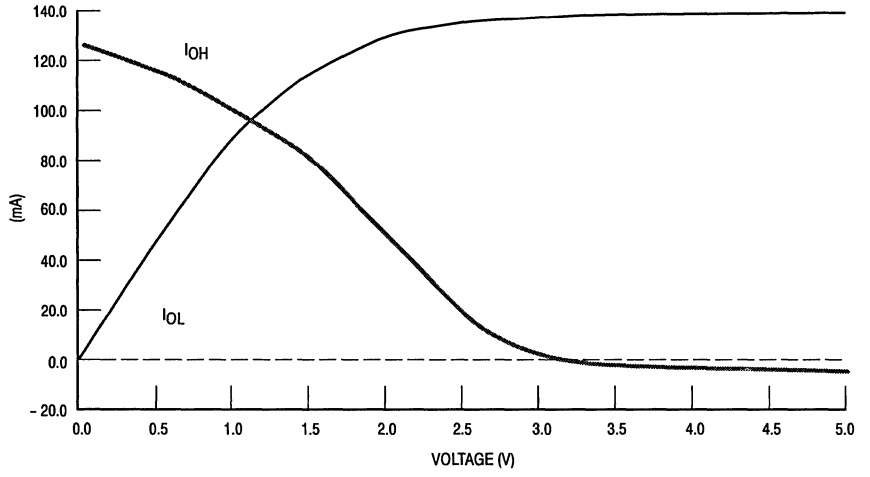

Figure 7. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM67A518, MCM67B518, MCM67C518, MCM67H518, MCM67J518, MCM67M518, MCM67W518 MCM67A618, MCM67B618, MCM67C618, MCM67H618, MCM67J618, MCM67M618, MCM67W618

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THERMAL PERFORMANCE OF FAST STATIC RAM PACKAGES

The following explains the test and simulation methodologies that are used to determine thermal performance. Simulation results are reported for most of Motorola's Fast Static RAM packages currently in use.

JUNCTION TO AMBIENT THERMAL RESISTANCE

The thermal performance of a surface mount integrated circuit package is normally reported as a junction to ambient thermal resistance. Theta JA, θ_{JA}, and $R\theta_{JA}$ are the normal nomenclatures. Theta JA is determined using the methodology of SEMI Standard G38 – 87. To summarize, the package is built with a thermal test die which has resistors for heating the silicon die within the package and one or more diodes to measure the die temperature. A surface mount package is then soldered to a printed circuit board. Naturally, the size and amount of metallization on the board strongly influences the measured thermal performance. The test boards are designed with "minimum" metallization but with all the leads routed. The printed circuit board with the package is placed horizontally in either the wind tunnel for forced convection measurements or in a one cubic foot box for natural convection measurements. The test chip is used to heat the package and determine the die temperature within the package. This die temperature is the "junction" temperature. Then the junction to ambient thermal resistance is determined by

$$\theta_{JA} = \frac{(T_J - T_A)}{P}$$

where T_J is the die temperature, T_A is the ambient temperature, and P is the power dissipated within the package. The ambient temperature is measured below the printed circuit board, one half inch away from the edge of the board and one inch below the plane of the board. This location is a local ambient while avoiding measuring the air temperature after it has been heated by the package. Typically for the SOJ packages, one watt is used for the measurement. The measured value of Theta JA is not a strong function of the measurement power although the measured value will decrease slightly with increasing power. The slight decrease occurs because higher surface temperatures cause a more effective natural convection.

Measurements of test die have been taken on three memory packages for this report: 24 lead, 300 mil wide SOJ; 28 lead, 400 mil wide SOJ; and 52 lead PLCC. This data was used to "calibrate" the thermal simulation tool. After the simulations were completed, measurements were made on the 28 lead 300 mil wide SOJ to provide an error estimate.

With validation obtained from the experimental data, the simulation tool was used to calculate the thermal performance of the packages listed in Table 1. The simulations are expected to be within 20%. The range in thermal performance between the various devices in a given package are primarily a result of the different die and die paddle sizes.

Table 1. Thermal Resistances of Memory Packages

Lead Count	Pkg Width	Part Number	Theta JA, Natural, Measured	Theta JA, Natural, Simulated	Theta JA, 200 LFM, Measured	Theta JA, 200 LFM, Simulated	Theta JC, Measured	Theta JC, Simulated	Theta JA0, Natural, Simulated
36	400 mil	XCM6246WJ		54.06		39.86		5.06	15.61
36	400 mil	XCM67084WJ		57.69		43.35		7.65	21.11
32	400 mil	XCM6249WJ		55.58		40.28		4.23	14.14
32	400 mil	MCM6726WJ		60.48		45.02		7.72	21.55
32	400 mil	MCM6226AWJ		59.69		44.24		7.3	19.43
32	400 mil	Test Chip	56.5	55.53	39.7	40.22		4.25	14.46
32	400 mil	MCM6226BWJ		66.81		51.2		13.7	26.09
28	400 mil	MCM6229AWJ		67.36		49.73		6.8	18.72
28	400 mil	MCM6728WJ		68.34		50.54		7.35	21.41
28	400 mil	MCM6229BWJ		74.86		57.18		13.23	25.83
32	300 mil	MCM6206CJ		72.1		57.37		14.14	27.59
32	300 mil	MCM6206BJ		68.07		53.35		10.36	24.36
28	300 mil	MCM6206CJ		75.27		60.19		15.24	28.99
28	300 mil	MCM6264CJ		92.77		76.93		30.29	49.95
28	300 mil	MCM6229BJ		70.7		55.63		11.01	25.33
28	300 mil	MCM6706AJ		77.35		62.21		17.09	31.23
28	300 mil	Test Chip	65.1*	76.6	48.1	61.45	17.3	16.38	30.69
24	300 mil	MCM6708AJ		80.73		64.19		16.85	31.14
24	300 mil	MCM6290CJ		91.28		74.16		25.29	45.08
24	300 mil	Test Chip	69.7	72.7		56.4		9.95	23.16
52	PLCC	MCM67618FN		45.88		31.85		8.46	14.79
52	PLCC	Test Chip	45.5	50.24	33	35.47	15.4	11.96	18.96
44	PLCC	MCM62486FN		57.1		41.03		14.78	23.35

*Measured value on SOJ with pin 14 and pin 28 connected to "split" flag (die paddle). Simulated value for SOJ with standard flag.

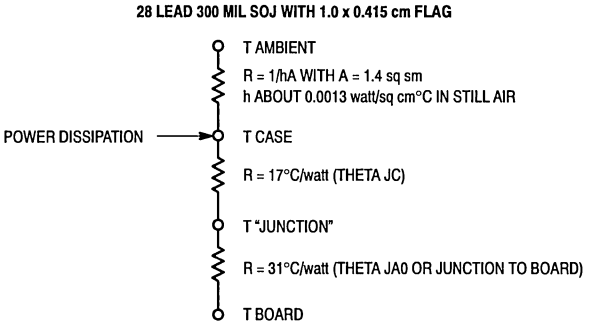
JUNCTION TO CASE THERMAL RESISTANCE

The junction to case thermal resistance, Theta JC or θ_{JC}, has been used in many different ways. The definition that is currently being used by the JEDEC 15.1 committee is the thermal resistance from the junction to the surface of the package. For the SOJ and PLCC package, that would be the thermal resistance from the junction to top surface of the package. Since heat sinks are rarely employed for SOJ packages, the junction to case thermal resistance is not normally used in determining the junction temperature. The enclosed table provides the simulated junction to case thermal resistance as determined by the simulation tool. The values obtained are not very accurate, but have sufficient accuracy in most circumstances. For a critical application, the junction to case thermal resistance should be measured.

Frequently, however, ThetaJC is used for the temperature difference (divided by total package power) between the junction and a thermocouple (or other temperature sensor) attached to top of the case. The JEDEC committee is recommending the nomenclature of *junction to reference* for the measurements relative to a thermocouple at the top of the package. Using the temperature on the top of the package in conjunction with the junction to reference thermal resistance is the best method to determine junction temperature in an actual use condition. In Natural Convection for the memory packages, we recommend using a value of Theta J-ref of 4°C/watt. In forced convection above 400 ft/minute, the recommended value of the Theta J-ref is Theta JC. These values will allow estimation of the junction temperature within 5°C for the normal range of applications provided that the thermocouple is 40 gauge or smaller and is applied correctly.

OVERALL PACKAGE THERMAL MODEL

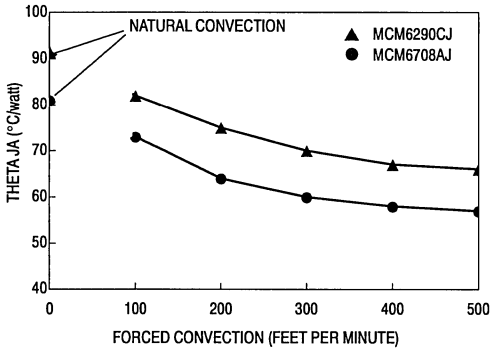
Theta JC is also used for a junction to lead thermal resistance occasionally. From an experimental point of view, it makes more sense to discuss the junction to board (printed circuit board) thermal resistance. The simulation software calculates a thermal resistance that is similar to the junction to board resistance: namely, θ_{JA0} that is defined to be the thermal resistance, with the printed circuit board held at ambient temperature. This is a close approximation of the junction to board thermal resistance since approximately 80% of the heat flows to the board in natural convection. These values can be used to construct a 1-D model of the thermal paths of the package as shown in Figure 1 below. This model can be used in the 2.5-D thermal model of the printed circuit application, if the spreading resistance of the board is treated correctly. Because the junction temperature is so closely coupled to the board temperature, determining the board temperature in the actual application is extremely important if the junction temperature is to be estimated.



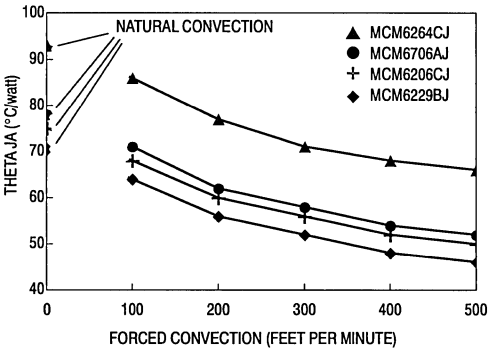
NOTE: Theta JA simulated in Natural Convection 77°C/watt.

Figure 1. One Dimensional Thermal Model

The thermal derating curves for Motorola's Fast Static RAMs are provided below. Although the data represents simulation results, there is a high level of confidence in the data points. In all cases, the manner in which the data is used could have a significant impact upon the validity of your thermal budget.



24 Lead SOJ, 300 mil, Copper Leadframe, Single Layer PCB Simulated Results



28 Lead SOJ, 300 mil, Copper Leadframe, Single Layer PCB Simulated Results

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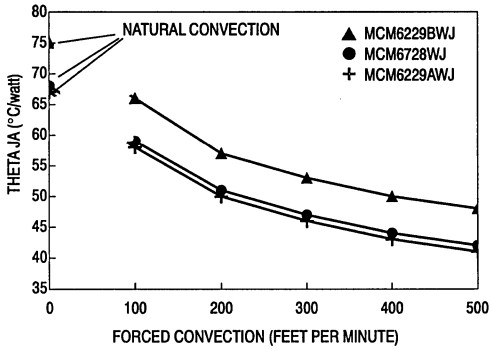
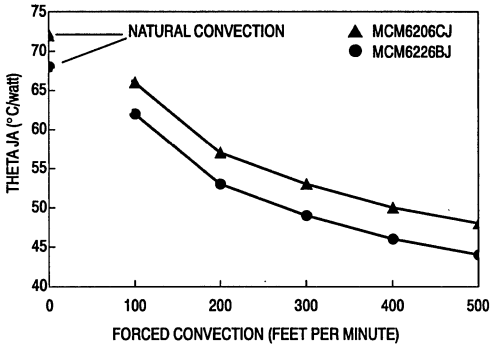
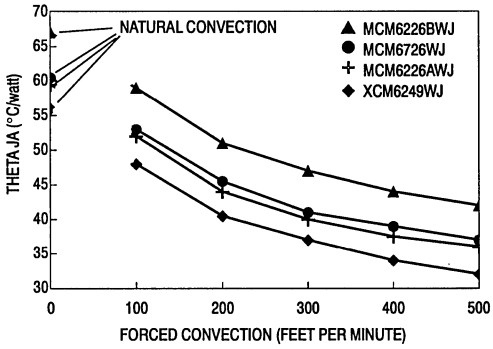


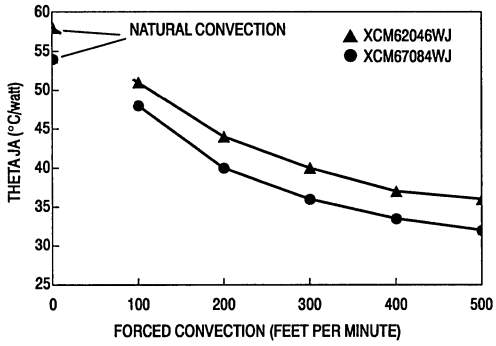
28 Lead SOJ, 400 mil, Copper Leadframe, Single Layer PCB Simulated Results



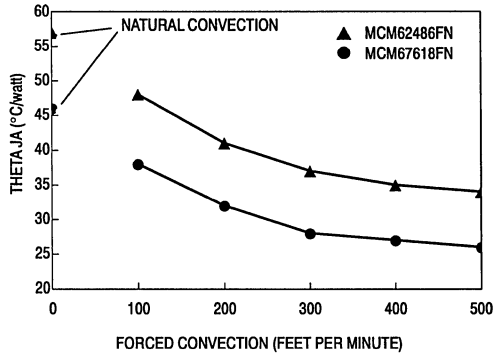
32 Lead SOJ, 300 mil, Copper Leadframe, Single Layer PCB Simulated Results



32 Lead SOJ, 400 mil, Copper Leadframe, Single Layer PCB Simulated Results



36 Lead SOJ, 400 mil, Copper Leadframe, Single Layer PCB Simulated Results



44 and 52 Lead PLCC, Copper Leadframe, Single Layer PCB Simulated Results

8

AN971
REV1

Avoiding Bus Contention in Fast Access RAM Designs

INTRODUCTION

When designing a bus oriented system, the possibility of bus contention must be taken into consideration. Bus contention occurs when two or more devices try to output opposite logic levels on the same common bus line.

This application note points out common causes of bus contention when designing with fast static random access memories and describes ways to eliminate or reduce contention.

WHAT CAUSES BUS CONTENTION?

The most common form of bus contention occurs when one device has not completely turned off (output in a high-impedance state) before another device is turned on (output active). Basically, contention is a timing overlap problem that results in large, transient current spikes. These large current spikes not only generate system noise, but can also affect the long term reliability of the devices on the bus (see Figure 1).

BUS CONTENTION AND FAST STATIC RAMs

Since memory devices are primarily used in bus oriented systems, care must be taken to avoid bus contention in memory designs. Fast static RAMs with common I/O data lines (or any high frequency device with common I/O pins) are the most likely candidates to encounter bus contention. This is due to the tight timing requirements that are needed to achieve high-speed operation. If timing control is not well maintained, bus contention will occur. The most common form of bus contention for memories occurs when switching from a read mode to a write mode or vice versa.

SWITCHING FROM A READ TO WRITE MODE

With $\overline{E}$ low (device selected), on the falling edge of $\overline{W}$ (write asserted) the RAM output driver begins to turn off (high-impedance state). Depending on the input and output logic levels, if sufficient time is not allowed for the output to fully turn off before an input driver turns on, bus contention will occur (see Figure 2a).

Figure 2a shows an example of a RAM trying to drive a bus line low while an input driver is trying to drive the line high. If the situation were reversed (RAM output high and the input driver low), bus contention would still exist.

Of course the obvious way to avoid this type of bus contention is to make sure that the input buffer is not enabled until the write low to output high-impedance (t_{WLQZ}) time is satisfied (see Figure 2b). This specification is usually given on most manufacturers' data sheets.

Another method to eliminate bus contention would be to use $\overline{E}$ to deselect the RAM before asserting $\overline{W}$ (low). This allows the RAM output extra time to go into high-impedance state before the input driver is enabled. $\overline{E}$ and $\overline{W}$ are later asserted low to begin a write cycle (see Figure 2c).

SWITCHING FROM A WRITE TO A READ MODE

With $\overline{E}$ set low (device selected), on the rising edge of $\overline{W}$ (write terminated) the address or data-in changes before the device has had a chance to terminate the write mode. If this should occur, and depending on the input and output logic levels, a bus contention situation could exist (see Figure 3). To avoid address changing type bus contention requires that the address not change till the write recovery specification (t_{WHAX}) is satisfied. To avoid bus contention caused by data changing requires that the data-in remains stable for the duration of the data hold specification (t_{WHDX}). Most of

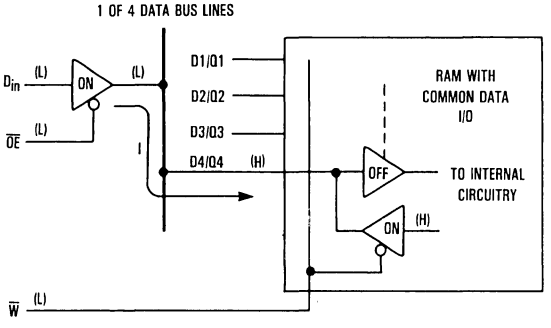


Figure 1. Common I/O Bus Contention

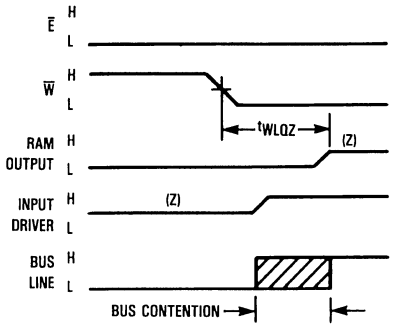


Figure 2a. Input Driver Enabled Prior to Disabling RAM Output

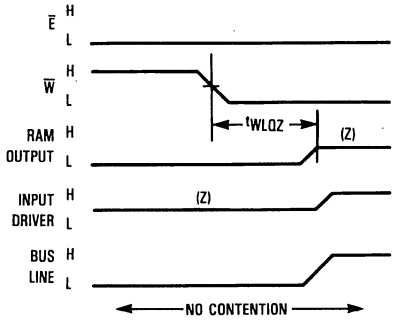


Figure 2b. Input Driver Disabled Prior to Enabling RAM Output

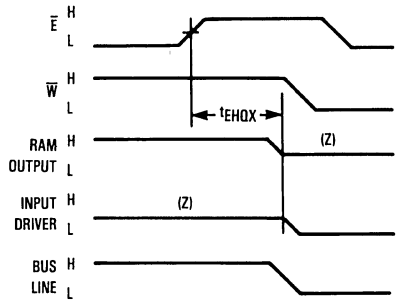


Figure 2c. Using $\overline{E}$ to Avoid Bus Contention

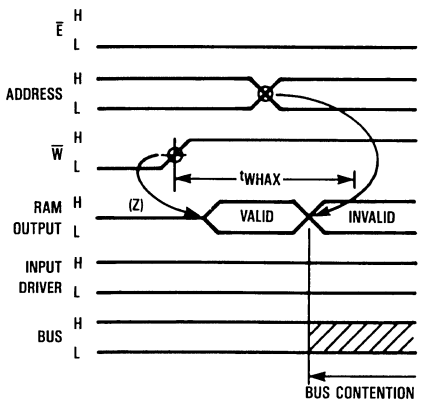


Figure 3a. Data Setup Time Violation

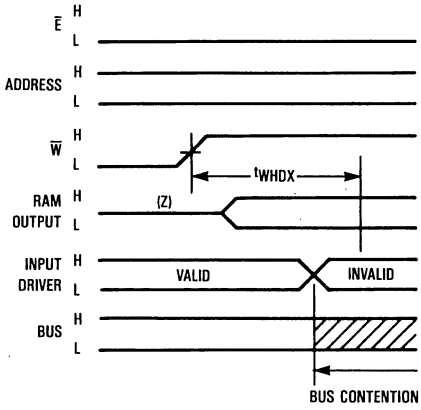


Figure 3b. Data Hold Time Violation

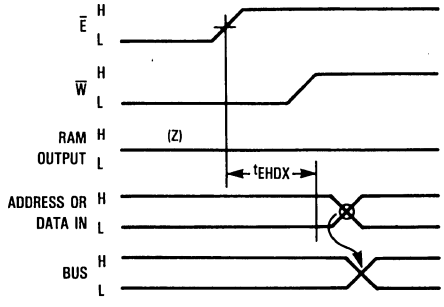


Figure 3c. Using $\overline{E}$ to Avoid Bus Contention

Motorola's fast static RAMs specify write recovery and data hold times of 0 ns. However, it is always a good practice to allow some margin to take care of possible race conditions.

Both of these types of contention could also be avoided by taking $\overline{E}$ high prior to taking $\overline{W}$ high. This will give the RAM output driver time to go to a high-impedance state before $\overline{W}$ goes high. In this case $\overline{E}$ is used to terminate the write cycle instead of $\overline{W}$ (see Figure 3c).

OTHER WAYS TO ELIMINATE BUS CONTENTION

If the RAM has an output enable pin ($\overline{G}$), synchronizing schemes can be incorporated to help eliminate bus contention. Taking $\overline{G}$ high will ensure that even when the RAM is in a read mode the output will be in a high-impedance state. This will allow the input driver to be enabled longer.

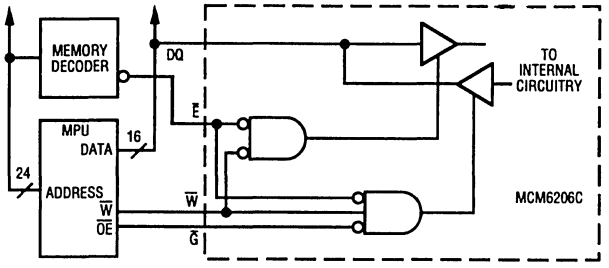


Figure 4a. Using $\overline{G}$ to Avoid Bus Contention

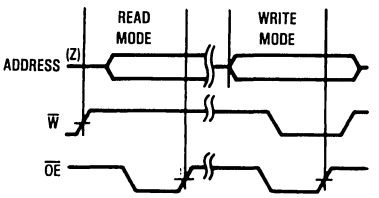


Figure 4b. Timing Diagram of MPU

Most advanced microprocessors have asynchronous bus-control signals that take advantage of fast memory devices with output enable pins. Figure 4 shows one way to avoid bus contention using a microprocessor interfaced to a Motorola 15-ns MCM6206C.

A more obvious way to eliminate bus contention is to use slow memory devices. Slow memories have loose timing requirements that allow devices to fully turn off before another device turns on. Of course this defeats the whole purpose of fast static memory devices.

Another obvious way to eliminate bus contention is to use memory devices that have separate data I/O pins. In this way the $\overline{W}$ signal from the microporcessor can control a buffer device to eliminate bus contention (see Figure 5). However, the industry is demanding RAM with common I/O because these devices cost less and save system real estate.

Common I/O devices reduce package size since fewer pins are needed. Smaller packages result in less PCB space requirement. Common I/O devices also eliminate the need for an extra buffer with its associated expense and space requirement. In general fast static RAMs configured greater than a X1 will have common data I/O pins.

Another popular way to reduce bus contention is to put a current limiting series resistor on each bus line (see Figure 6). The series resistor does not eliminate bus contention, but it helps reduce the large transient currents associated with bus contention. However, series resistors increase access time as well as increasing component count. The added access time depends on the total bus capacitance (including the capacitance of the devices on the bus) and the total bus resistance. The added delay should be added on to the point at which bus contention ceases. The following formulas can be used to determine the added access delay.

$$t_{HL} = R_L \cdot C_L \cdot \ln \frac{V_{in}(initial) - V_{in}(final)}{V_{IL}(max) - V_{in}(final)}$$

$$t_{LH} = R_L \cdot C_L \cdot \ln \frac{V_{in}(final) - V_{in}(initial)}{V_{in}(final) - V_{IH}(min)}$$

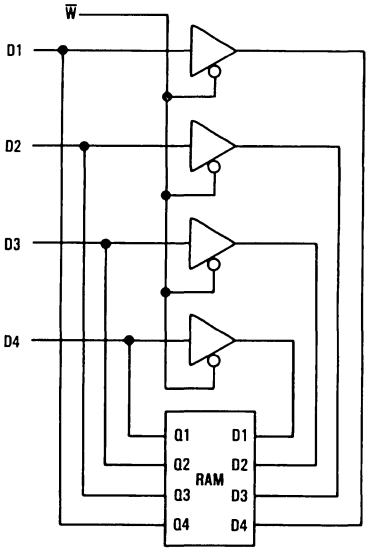


Figure 5. Separate I/O Buffer

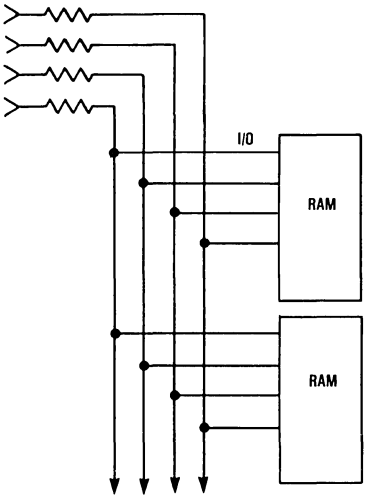


Figure 6. Using Series Terminating Resistors

8

Generally the value of the resistor should be around 50 ohms. The larger the resistor the less the transient current generated, but the greater the delay. Using a 150-ohm resistor will limit the current flow to less than 20 milliamperes while adding approximately 3 nanoseconds extra access time. However, note that even the series resistors bus contention duty cycle must be minimized to reduce EMI and bus ringing.

Although it is very important to reduce bus contention, CMOS memories can tolerate more bus noise generated by bus contention than can bipolar memories, due to the excellent noise immunity advantage of CMOS over bipolar technology. However, even when using CMOS memories, large destructive transient currents generated by bus contention can still occur.

CONCLUSION

Bus contention must be taken into consideration in most bus-oriented system design. The occurrence of bus contention generates large transient currents that produce system noise and could also affect the system's long term reliability.

Fast random access memories with common data I/O pins are very susceptible to bus contention due to tight timing requirements. Although it is almost impossible to totally eliminate bus contention, it must be the goal of the system designer to minimize bus contention.

AN1209

The Motorola BurstRAM™

Prepared by: James Garris

This note introduces the MCM62486 32K x 9 Synchronous BurstRAM. The device was designed to provide a high-performance, secondary cache for the Intel i486™ microprocessor and future microprocessors with burst protocol. Four of these devices can supply a 128K byte direct-mapped bursting cache with parity support.

THE MCM62486

The 62486 is a synchronous device with input registers and address counters surrounding a standard 32K x 9 FSRAM core. The additional circuitry in the periphery enables the memory to uniquely interface with the i486. Like the i486, the timings are referenced to the rising edge of the clock (K). Signals generated by the processor and control logic must be stable during all transitions of clock from low to high. Output enable ($\overline{G}$) on the 62486 is the only asynchronous input.

The 62486 contains three burst-control inputs. They are $\overline{ADV}$, $\overline{ADSC}$, and $\overline{ADSP}$. These inputs are used by the cache controller to control the burst capabilities of the 62486 and to maintain synchronization with the i486 or other logic driving the cache.

USE WITH THE i486 PROCESSOR

The 62486 requires an ASIC or discrete PAL type of cache controller to work with the i486. This cache control logic must also include 8K x 16 of cache-tag comparator RAM and any other buffers needed for system operation.

Control signals are sourced as follows: K is driven by the system clock (CLK); $\overline{ADSP}$ is an output from the microprocessor; and $\overline{ADV}$, $\overline{ADSC}$ are generated from the cache control logic. The data bus and lower address bus may interface directly with the 62486 or the address bus may be buffered to improve its drive to the rest of the system. A simple block diagram of this setup is shown in Figure 2.

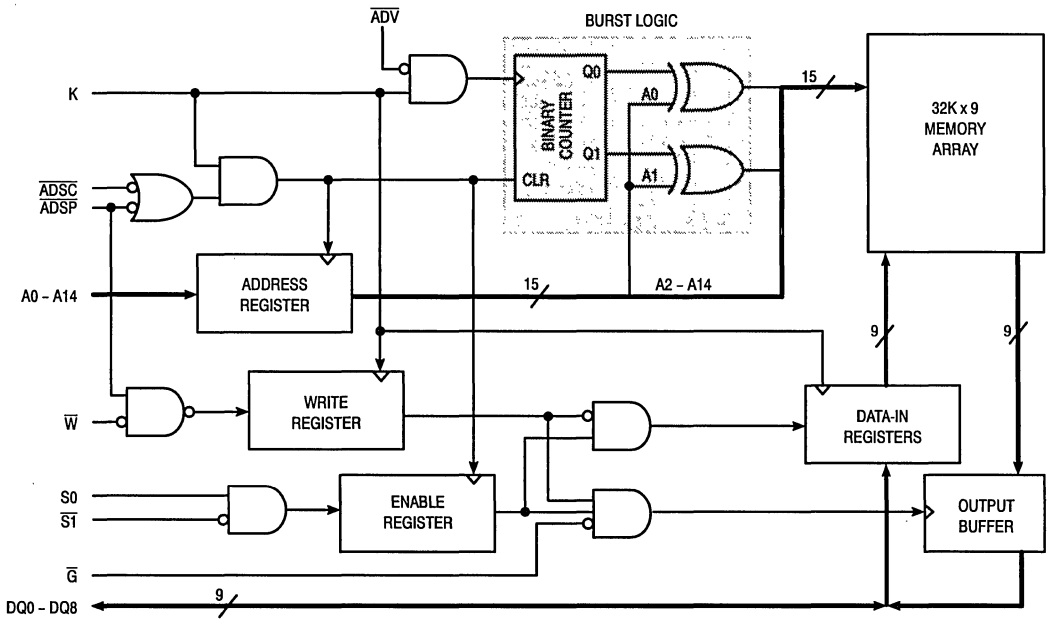


Figure 1. MCM62486 Block Diagram

BurstRAM is a trademark of Motorola, Inc.
i486 is a trademark of Intel Corp.

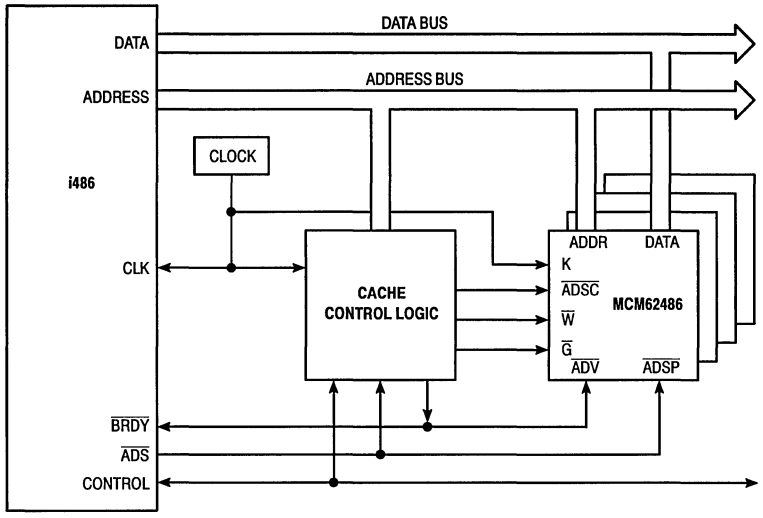


Figure 2. Typical System Block Diagram

INPUT PINS OF THE MCM62486

K is the clock input of the 62486. This should be tied to the system clock.

ADSP is one of two address status input pins that are supplied on the 62486. This input allows the microprocessor to initiate a cache bus cycle. For every processor access, to or from memory, the i486 will assert ADS for one transition of K from low to high. If ADS from the i486 is tied to ADSP on the 62486, the 62486 will register the correct address from the processor. During all "T2" cycles on the i486, ADS and ADSP should not be asserted as described in the i486 processor user manual.

ADSC is the second of two address status input pins supplied on the 62486. This input allows external logic to initiate or continue cache bus cycles. The purpose of this input is to give the cache controller its own input to regulate cache accesses. This gives the 62486 a good deal of system design flexibility. One use of ADSC is for burst extension. After four burst accesses have been generated by the 62486, the cache controller may supply an additional base address to continue the burst. This method works well with 72 bit data buses. This pin can also be used in a similar manner to facilitate a cache fill from other sources.

ADV is the burst advance input pin supplied on the 62486. The purpose of this pin is to acknowledge a successful read-from or write-to memory as determined by the cache control logic. The 62486 may then proceed to the next address. This input is a function of T2 (T2 cycle as defined by the i486 processor manual), KEN (from the processor), MATCH (from the cache tags), READ (from the processor) and MISS (a cacheable read miss from the control logic).

W is the synchronous write input pin supplied on the 62486. This signal must be valid for every clock cycle ADSP is not asserted.

A0 – A14 are the synchronous address pins supplied on the 62486. These must be valid for the transitions of K from low to high. If neither ADSC or ADSP is negated, or if the chip is deselected, the address inputs do not need to meet the required setup/hold times. For all other read/write operations, the setup/hold times **MUST** be met.

S0 and S1 are the synchronous chip selects supplied on the 62486. These must be valid whenever the addresses are required valid. These inputs can be used for address depth expansion without any external logic.

G is the asynchronous output enable supplied on the 62486. This pin changes the outputs from high impedance to active at any time that the SRAM is selected.

CACHE OPERATION

READ CYCLES

Cache operations of the 62486 are initiated with one of the two Address Status Pins mentioned. Figure 3 shows the read cycle timings when ADSP is tied to ADS. During the first cycle (T1) the i486 supplies an address and asserts ADS low. The 62486 responds to ADSP being asserted by registering the lower 15 addresses. The 62486 begins to perform a read access regardless of the state of its W input.3

During the next cycle (T2), the cache controller determines if the read access was a cache hit. If so, the controller should assert G and ADV on the 62486 as well as BRDY on the i486. The assertion of G will allow the 62486 to drive the data onto the data bus while BRDY will inform the processor that the data is correct. The assertion of ADV will cause the 62486 to begin on the next burst access. Subsequent burst access will be available without wait states in a similar fashion.

Single, non-burst reads behave in a similar manner as the first access of a read burst.

Note for timing diagrams: Q1, Q2, Q3, Q4 represent the data output from the first address (base address), second, third and fourth address. For example, if A in Figure 3 was #000C, Q1 would be the data from #000C, Q2 from #0008, Q3 from #0004 and Q4 from #0000. (This is the same burst sequence as in **Table 7.7. Burst Order** in the *i486 Microprocessor Data Book*).

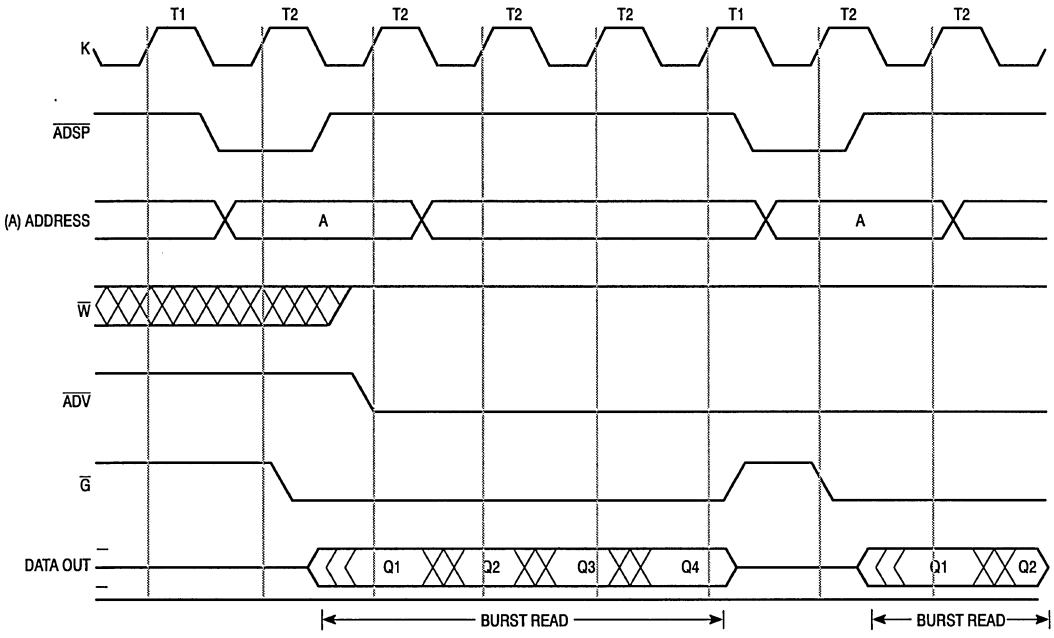


Figure 3. Cache Read Cycles

WRITE CYCLES

For a write to cache access, the initial T1 cycle will be the same as above. During the T2 cycle, the cache controller should assert $\overline{W}$ instead of $\overline{G}$. This will allow the 62486 to receive the data from the i486 and write it to memory. The i486 can burst write for 8 and 16 bit operations. The 62486 can support this action as described in the 62486 data sheet and Figure 4.

ADDRESS BUS LOADING

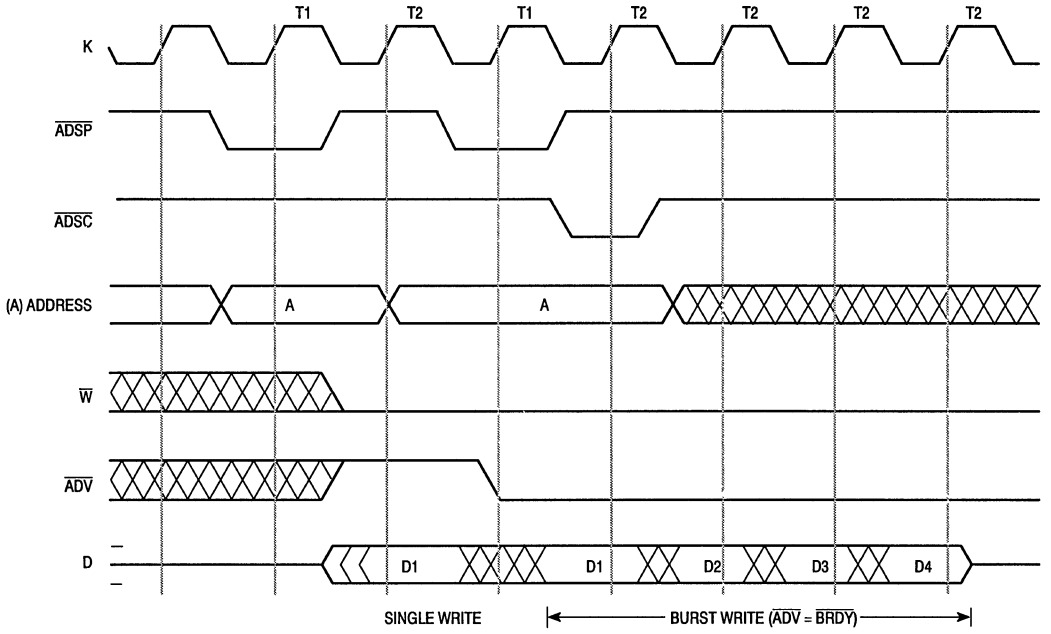
The 62486 has setup and hold timing that allow address buffers to be placed between the SRAM and the processor. The i486 is specified with 50 pF loads. Since the 62486 has a typical input capacitance of 2 pF, the i486 can be run without the buffer assuming the cache tags and other circuitry do not overload the bus.

ADVANTAGES OF THE 62486 OVER OTHER FSRAM SOLUTIONS

The 62486 is meant to replace a standard 32K x 9 FSRAM as well as some external logic. By incorporating this logic and RAM onto one chip, the system designer is given more board space, less power consumption, and most of all, easier design timing requirements. At 33 MHz, a discrete logic/SRAM solution would require a 7 ns PAL (for the burst counter) and an 18 ns SRAM [30 ns (period) – 5 ns (i486 setup) – 7 ns (PAL) = 18 ns].

This timing is even more difficult in write cycles. Closer examination of writes shows that the write signal and data from the processor do not correspond with the requirements of a standard 32K x 9 SRAM. A self-timed write SRAM is essential for high performance systems.

The 62486 represents the JEDEC standard for a 32K x 9 Synchronous SRAM for the i486. This pin-out provides enough power and ground pins to allow these devices to support systems running 50 MHz and faster. Also the 62486 represents the standard functionality descriptions for $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$. These same pins are used in the JEDEC standard 64K x 18 SRAM to be used with the i486 and the "P5".



NOTE: The first T1/T2 cycle is a single write operation. This works the same as the first two cycles of a burst write. In this single write operation, ADV goes high for the T2 cycle, while the RDY signals on the processor must be asserted low. In this operation, the ADV and RDY signals behave differently. To match their behavior, examine the second T1/T2 cycles. This second write operation (the burst write) shows how the ADV signal may behave like the RDY signals. Note that the ADSC is asserted for the first T2 cycle, thereby reloading the base address. Had the ADSC remained high for this cycle, the data (D1) would have been incorrectly written to the second burst address. This second write operation shows both single and burst write operations with ADV and RDY both asserted low for all T2 cycles.

Figure 4. Cache Write Cycles

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AN1210

A Protocol Specific Memory for Burstable Fast Cache Memory Applications

Prepared by: Ron Hanson

Cache memory design has evolved rapidly in recent years, taking full advantage of the specialized cache application specific fast static RAMs that are becoming increasingly available. These advanced designs are driven by several factors: faster processor clock rates, larger on-chip processor caches, larger and faster FSRAMs, more efficient processor bus protocols, and more efficient DRAM interfaces.

CACHE MEMORY DESIGN TRENDS

Six key trends can be observed in this evolution:

1. Larger caches to improved hit rates.
2. Faster caches to maintain the desired no-wait state response.
3. Dominance of direct-mapped cache designs over the number of multiple-way set associative cache designs.
4. Minimization of external cache control logic to increase speed.
5. Users are developing their own cache solutions, even though vendors are offering more and more integrated solutions.
6. An increasing use of Application Specific Memories (ASMs).

LARGER CACHES

The latest CISC and RISC processors all have ample amounts of no-wait state cache on-chip or included in the processor chip set. Frequently this cache responds a full clock cycle or more faster than an external memory cache could because it is connected to the processor's highly efficient internal bus. In the case of the MC68040, this is a full Harvard Bus architecture that is at least twice as efficient as the fastest external memory system.

The hit rates of these internal caches are very impressive too. The i486™ provides 8K bytes of on-chip four-way set associative cache as does the '040. Though a small amount of cache, these caches have read hit rates greater than 80%. In short, it takes a comparatively large external cache to improve on the performance of the processor alone and this trend will continue. However, FSRAMS are also getting larger. 256K bit FSRAMs are now in abundance and 1 Megabit FSRAMs are in production. As has always been the case with memories, these new larger FSRAMs will replace the older smaller ones at about the same price relative to their respective product life cycles. In other words, building a cache with the largest FSRAMs available today is no more expensive that building a cache three years ago with the largest FSRAMs available then.

BurstRAM is a trademark of Motorola, Inc.
SPARC is a registered trademark of SPARC International, Inc.
i486 is a trademark of Intel Corp.

FASTER CACHES

Processor speeds continue to increase and there is no end in sight. There are already 50 MHz production processors. Recently the processors have been designed to be more "cache friendly." Significant protocol improvements were implemented on the '040 versus the '030 and the i486 versus the i386. These include implementing synchronous protocols, adding burst addressing, and reducing the data input set-up times.

However, it still comes down to question of raw speed. Fortunately, the increase in density has also been accompanied by increases in FSRAM speed. Now RAMs with 12 ns access times are available to support the 50 MHz processors. It is increasingly apparent that greater integration will be needed to continue to support the fastest processors. The elimination of logic circuits from the critical cache speed path is being vigorously pursued today.

THE DOMINANCE OF DIRECT-MAPPED CACHE DESIGNS

It has been shown that for any given system, as the size of the external cache increases, the performance advantage of a multiple way set associative cache over a direct mapped cache quickly fades to insignificance.[1] Furthermore, a multiple way set associative cache is always more complex to implement.[2] In a discrete design, this translates to either more cost or a loss in response time, which erodes any performance advantage that might be gained. For an integrated solution, it means relying on a vendor for a purchased proprietary solution. Often, if more performance is sought, it is far simpler and less expensive to just enlarge the cache rather than build in multiple way set associativity.

1 Jeff Leonard, "Clever Cache Designs Required to Pace High-Speed RISCs," *EE Times*, March 19, 1990, pp. 56, 68 – 69.
2 Mark D. Hill, "A Case for Direct-Mapped Caches," *IEEE*, December 1988, pp. 25 – 40.

8

MINIMIZATION OF EXTERNAL LOGIC

This point differs from the comment made on the elimination of logic circuits though integration. The Cache Tag RAM is a good example of integration that eliminated the need for a discrete comparator logic device. This did not minimize the logic required. Synchronous or self timed RAMs accomplish this by greatly reducing the complex logic required during write cycles. This is only the beginning; new protocol-specific memories are on the way that will take their cues from the processor itself and perform the needed RAM functions.

USERS ARE DEVELOPING THEIR OWN SOLUTIONS

There are many reasons why computer companies from the lowest performance to the highest are developing their own circuits rather than purchasing the ready-made solutions. One is competitive pressures. PC manufacturers using the same processor, coprocessor, mass storage devices, etc., must find a way to differentiate their products. They can do this by designing their own circuits. Another reason is value added. Many of these companies desire to develop their own chip technology to increase their own share of the revenue received for each computer.

Nevertheless, there is still a high demand for standardized memories. The sheer volume a memory can generate if it is adopted as a standard will drive its cost down far below what an individual custom memory could accomplish. Thus, though cache designs are using more specialty ICs, they still rely on multi-sourced high volume memories for cache data storage.

USE OF APPLICATION SPECIFIC MEMORIES

Referring back to the problem of supporting the very fastest processors, it is clear that the cache designer must attack this problem on all fronts. What is needed is a smart flexible, integrated, high density, very fast SRAM. Such products do exist, and the following is a description of one of the latest under development by several vendors that combines all of these features.

THE SYNCHRONOUS BURST PROTOCOL

In an effort to overcome the limitations of memory bus bandwidth, many of the high performance microprocessors have implemented burst memory protocols. Rather than transferring a single memory word per bus cycle, the microprocessor will transfer (burst) several consecutive memory words in quick succession. The number of words transferred corresponds to the length of a line in the microprocessor's internal cache. Burst transfers have been shown to greatly improve bus utilization. The MC68030, MC68040, PowerPC™, i486, Pentium™, MC88200, and AM29000 all employ burst memory transfers of one type or another.

Though the on-chip cache(s) can be very effective, system performance frequently can be improved by the addition of a secondary cache memory external to the microprocessor. There are three good possible reasons to add a secondary cache: 1) in multiprocessing systems, the time spent arbitrating for control of a global bus can severely degrade performance; 2) the system bus may run at a significantly slower rate than the microprocessor bus; and 3) the nature of the code itself may be better suited for larger caches than are available on-chip.

Burst protocols provide a new challenge for system designers. To achieve no wait state performance, it is necessary for the cache to count through the burst sequence. This in turn creates a problem during cache update cycles when wait states must be added to account for slower DRAM access times. Clearly, the designer would benefit from the integration of as much of this logic as possible onto the FSRAM. This reduces chip count and eliminates the propagation delay from discrete devices. Furthermore, by using inputs directly from the processor, it is possible to actually minimize the amount of logic required to manage the burst cycle. The inclusion of this logic creates an FSRAM that is not only processor specific, but protocol specific as well.

THE 32K x 9 SYNCHRONOUS BURST FSRAM

Not surprisingly, the original specification proposal for this burst FSRAM came from a user, Compaq Computer (Houston, Texas). It is a Synchronous FSRAM with an on-chip burst counter (see Figure 1) and special logic that enables the RAM to interface directly to the i486 processor as well as a cache controller. This device is being developed by several vendors for the i486 market.

The device is similar to existing synchronous FSRAMs in the market today. All of the address and control signal inputs to the RAM are held in registers on the chip, which are triggered by the rising edge the clock input (K) or the clock input gated by another input signal. These other signals include the $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ signals that qualify the address input.

The burst counter on chip is designed to count in the sequence used by the i486; however, the on chip count avoids the wait state inserted by the i486 at the beginning of a burst read cycle, thus improving cache performance. The $\overline{\text{ADV}}$ signal advances the counter of the rising edge of the clock, prior to the next memory access. The device uses a data input register to clock in the data on write cycles. Writes to the RAM are self-timed, requiring the minimal amount of control logic.

This FSRAM has a special built in wait state on write cycles (see Figure 2). This conforms with the i486 write timing. Furthermore, the RAM only advances its internal counter when told to by the controller, which is simultaneously acknowledging the previous transfer to the processor. The RAM can insert wait states whenever needed and, more importantly, it can hold address and count and switch from read to write mode in the event that a cache read miss occurs.

The real value of the BurstRAM™ is its simple processor interface (see Figures 3 and 4). The on-chip Address Register is controlled by the clock input and the processor's valid address signal. Thus, the RAM only registers the address when told to by the processor.

Using inputs from users on Motorola's MC68040 microprocessor, a similar device for '040 has been developed. This version, the MCM62940A, can also interface with the MPC601 (PowerPC), MC88200 and AM29000 RISC processors.

This version of the BurstRAM naturally has a modulo four burst counter to stay in step with the '040 and MPC601. No-wait state Write Burst Cycles at very high clock rates are attainable on both '040 and PowerPC platforms.

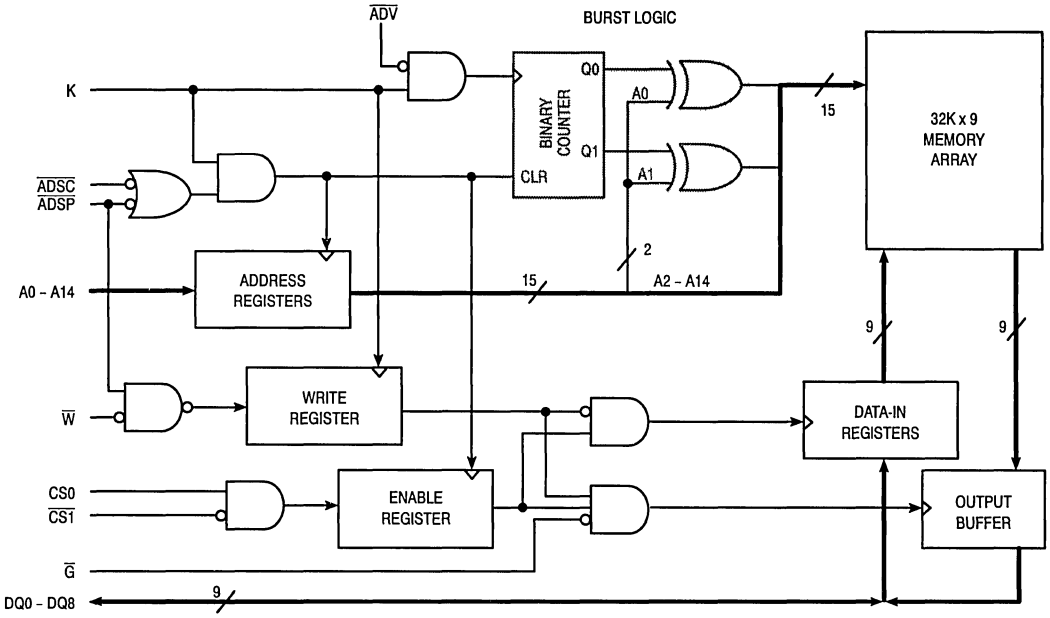

Figure 1. MCM62486A 32K x 9 BurstRAM Block Diagram

The removal of the wait state from the beginning of the write cycle actually simplifies the control logic since the conditions under which the BurstRAMs internal counter is advanced are now identical for both read and write cycles.

The conditional registering of the address input is especially useful when interfacing to a processor with multiplexed address and data buses such as the MC88200 or shared address buses such as the AM29000.

Burst FSRAMs are not a new concept; when the '030 first introduced the burst protocol in a microprocessor environment, a burst protocol FSRAM specification was developed. Unfortunately, the timing constraints of the '030 placed the performance goals of the FSRAM beyond the technology available at the time. The only way to build a no-wait state cache at the higher speeds was to utilize the bus retry cycle to rerun any memory access in the event of a cache miss.[3] To the RAM, this meant having to count backwards in the event of a cache miss and adding pins and logic to control this adjustment. Furthermore, the 15 ns access times needed were not feasible at the time.

THE FUTURE DIRECTION OF PROTOCOL SPECIFIC FSRAMs

Clearly, with the technology being developed today, it will be quite feasible to fully integrate all of the elements of the cache (data storage, address tag storage, and control logic) onto one chip. This will be the least cost approach, and if offered by a vendor, it will represent the least amount of user design resources. However, this approach will severely limit cache options and product differentiation. Furthermore, this approach will never perform as well as on-chip caches, which are growing in size. Thus, discrete FSRAMs of some kind will continue to be used in cache memory design.

Protocol Specific FSRAMs will increase in usage, but they will not completely replace standard products if for no other reasons than the versatility advantage of a standard device and its smaller packages. The densities of both will have to increase, though it appears that wider RAMs will be preferred for the new designs.

[3] Richard Crisp, Brian Branson, and Ron Hanson, "Designing a Cache for a Fast Processor," *Electronic Design*, October 13, 1988, pp. 111 – 118.

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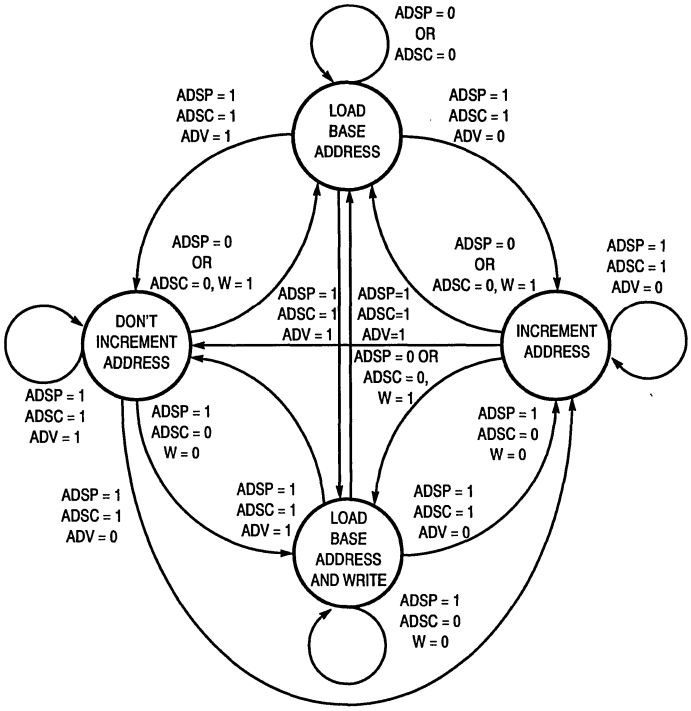

Figure 2. State Diagram for Address Determination on the MCM62486A BurstRAM

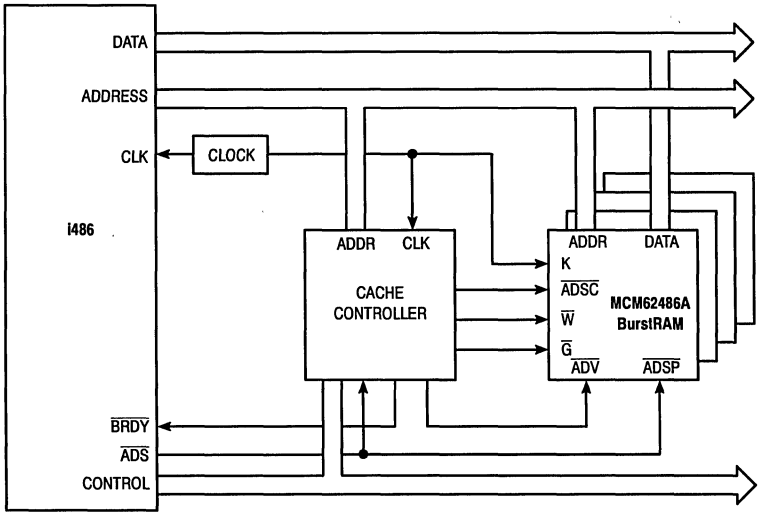

Figure 3. i486 128K Byte Burstable Cache Memory Block Diagram

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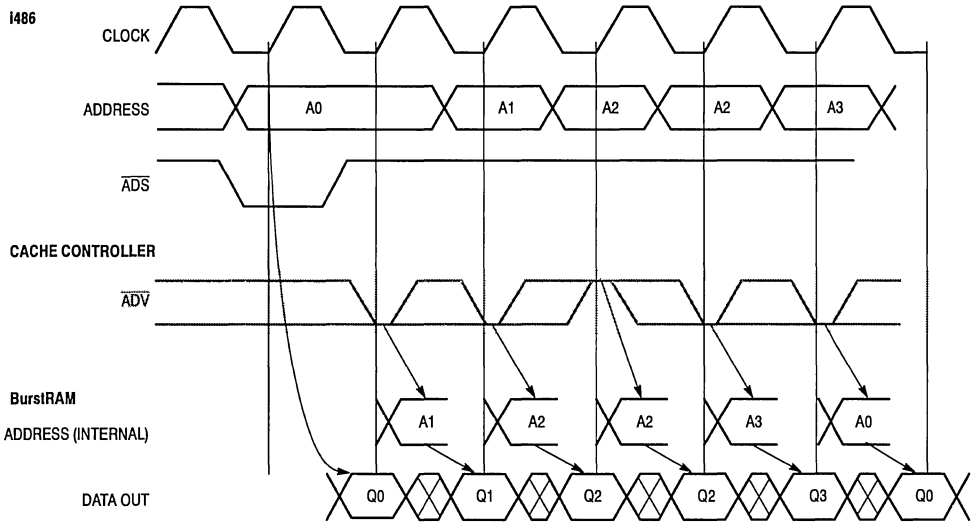

Figure 4. Timing Example of a 2/1/2/1 Burst Read

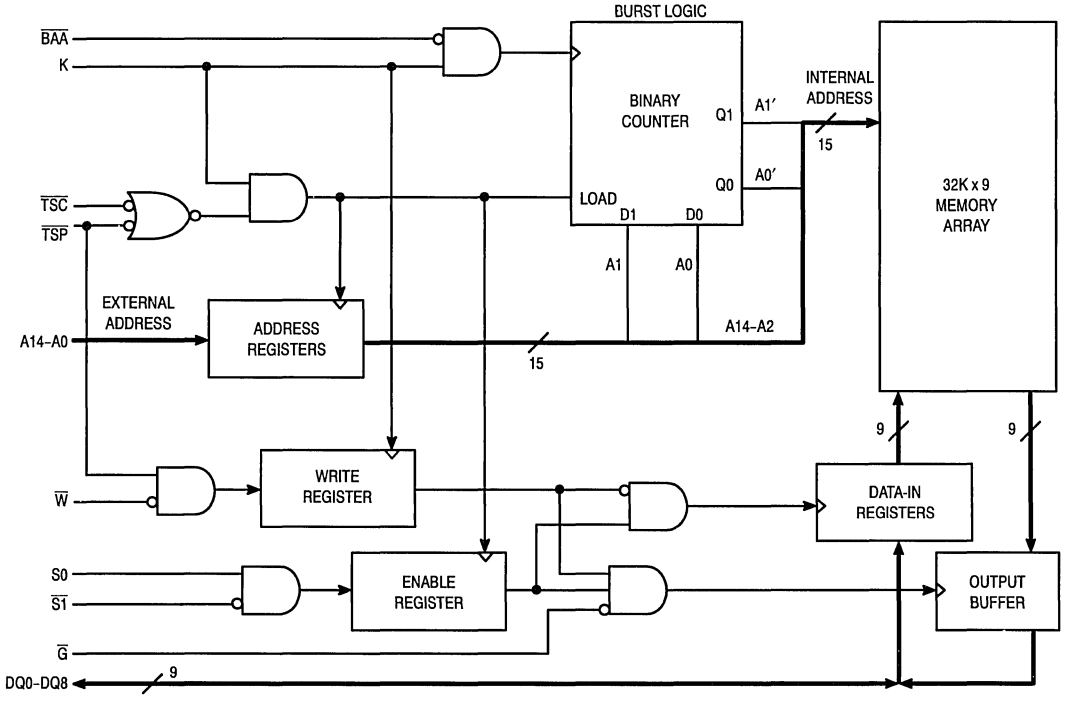

Figure 5. MCM62940A 32K x 9 BurstRAM Block Diagram

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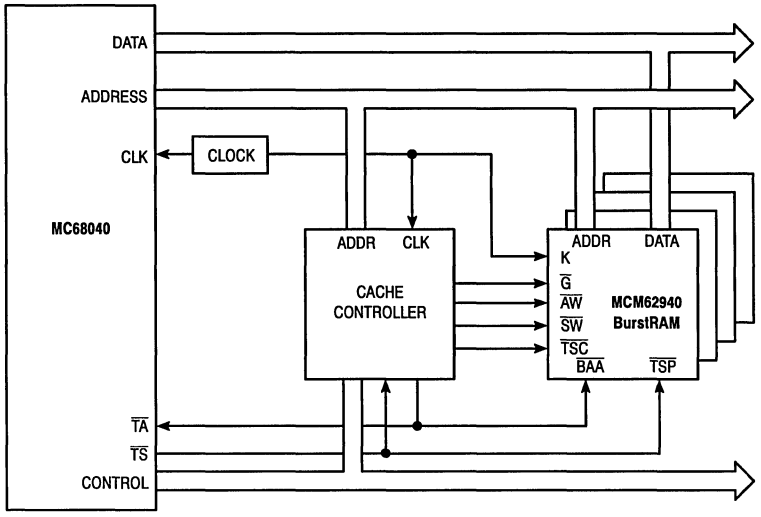

Figure 6. MC68040 128K Byte Burstable Cache Memory Block Diagram

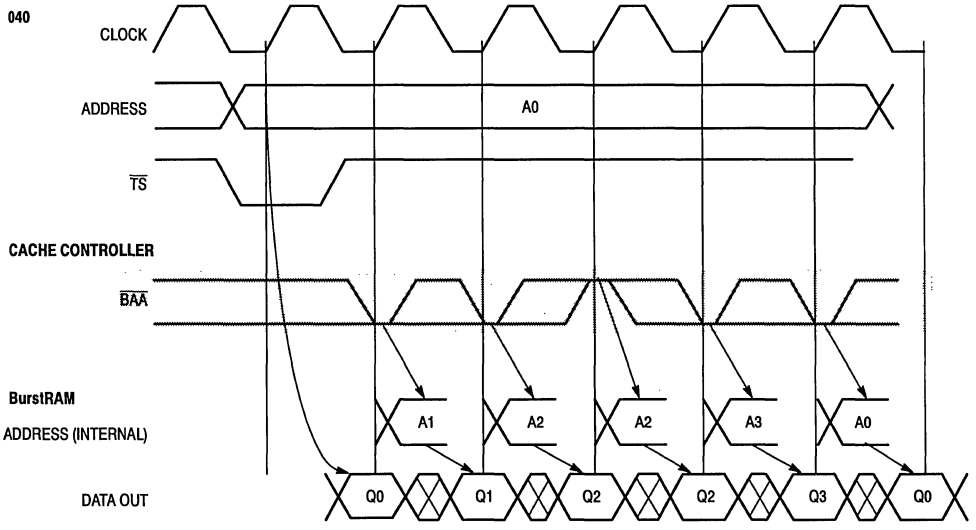

Figure 7. Timing Example of a 2/1/2/1 Burst Read

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AN1223

A Zero Wait State Secondary Cache for Intel's Pentium™

Prepared by: Michael Peters, FSRAM Applications Engineer

Due to the increased complexity and sheer memory size requirements of new and forthcoming operating systems (OS), graphical user interfaces (GUI) and application programs, the demand for ever-increasing performance from the desktop machine continues. Next generation machines require more and faster memory. Microsoft's Windows NT™, for instance, will most likely need 12 to 16 MBytes of main memory. Cache size requirements follow accordingly. And Intel's new Pentium CPU has been introduced with external bus speeds of 60 MHz and 66 MHz.

High performance memory is essential in achieving Pentium's full potential. First level (L1), on-chip cache memory hit rates will suffer as a result of users' migration away from DOS to Windows to Windows NT. It has been shown that L1 cache hit rates decrease mainly due to the increased number and types of references demanded by the newer OS.[1] The CPU designer can only afford relatively small increases in L1 cache size in an effort to keep chip size down. So, second level (L2) cache must make up for the lack of an appropriately sized cache and significantly help to avoid time consuming DRAM accesses. In addition, at 60/66 MHz bus speeds, the L2 cache must be capable of reading and writing data fast enough for Pentium's superscalar design.

Motorola's new families of 64Kx18 and 32Kx18 Fast SRAMs establish a new standard in providing a big enough and fast enough data cache for Pentium designs. These families include five synchronous and two asynchronous devices in each family. All x18 SRAMs feature byte-write capability, 3.3 V I/O compatibility, and asynchronous output enable control. A zero wait state solution is possible using four MCM67B618 (or four MCM67B518) BurstRAMs™. The objective of this note is to explain some of the system level, electrical, and timing issues associated with the design of a zero wait state secondary cache.

BurstRAMs vs. ASYNCHRONOUS SRAMs

Although the i486™ and Pentium CPUs support a burst cache line fill protocol, in most cases building a zero wait state bursting cache with a single bank of ordinary SRAMs is simply not practical. Virtually all cache controllers/chipsets designed to work with the i486 accommodate the burst protocol by using an interleaved scheme of two banks of standard asynchronous SRAMs. The speed requirements for this type of caching arrangement allow the use of 20 ns through 35 ns SRAMs. These speeds accommodate 20 through 33 MHz i486 machines, the bulk of today's IBM-compatible PC market. For the i486's 32-bit bus speeds less than 50 MHz, this hook-up is technically feasible, but somewhat expensive and physically large, and it consumes a good deal of power since as many as eight SRAMs are required. However, Pentium's 64-bit bus and bus cycle rates of 60 MHz and faster only exacerbate the difficulties with single and double bank caches using ordinary asynchronous SRAMs. Most chipset vendors will find that the use of synchronous burstable SRAMs will be the only practical zero wait state solution for Pentium.

A single bank scheme must use either extremely fast RAMs (< 7 ns for a 60 MHz bus) or add wait states. With the added wait states, a single bank 3-2-2-2 (three lead-off clock cycles and two clock cycles for each subsequent read) design might still require 12 ns standard SRAMs.

A double bank scheme can be designed with wait states or for high speed with no wait states. Figure 1 shows the timing for a 3-2-2-2 design using sixteen 15 ns 32Kx8 (or x9) SRAMs in a two bank design.

The cache can be expected to consume about 8.6 W. Two banks of 12 ns standard 32Kx8 (or x9) BiCMOS SRAMs might achieve 3-1-1-1 burst, but at an even greater power premium — nearly 12 W. In two bank schemes, even when one bank is de-selected, it will still draw about 65% of the full operating current.

Double bank designs present other issues that must be considered, including address and data bus loading, physical layout, and socketing devices. Two banks of 32Kx8s will present an 80 pF load (plus routing) to the cache controller's address bus. These heavily loaded lines represent additional signal delay and power dissipation compared to a BurstRAM design. And, one cannot afford a 5 ns buffer delay in the address path. When comparing the BurstRAM's 52-lead PLCC package with a standard 32Kx9 SOJ, direct mounting of these devices on a board will yield roughly four square inches versus eight square inches, respectively. Socketing the SRAMs is ill advised since access time will be pushed out, and signal integrity may be compromised.

Although designing caches with asynchronous SRAMs can be done, the control signal timing is far from easy. Of all timing concerns, write pulse generation may be the biggest issue. Burst writes may be next to impossible to perform since both edges of the write pulse must be positioned precisely to accommodate address set-up and data hold times. One can expect 10 ns minimum write pulse widths for 12 ns asynchronous SRAMs; this does not leave much time for the 15 ns cycle processor bus.

Motorola has developed a series of 256Kbit, 512Kbit, and 1Mbit SRAMs, known collectively as BurstRAMs, to solve these problems.[2]

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.
Windows NT is a trademark of Microsoft Corp.

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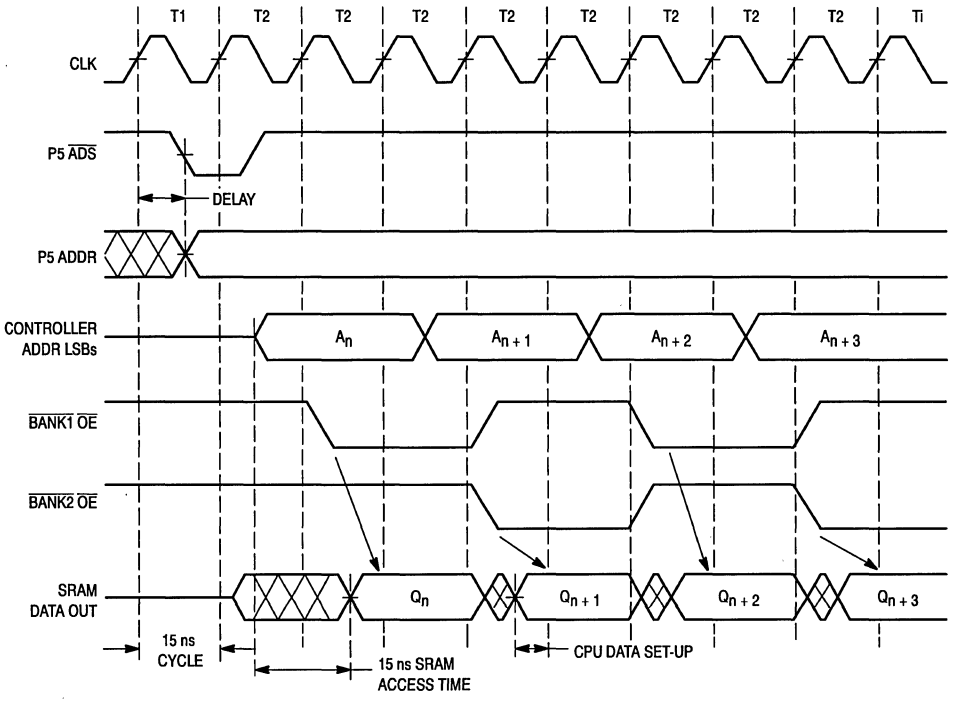

Figure 1. Two Bank Asynchronous SRAMs Performing 3-2-2-2 Burst READ

The MCM62486, a 32Kx9 BurstRAM, was developed for i486 systems. These BurstRAMs are being used in many of the 50 MHz i486 systems built today. The MCM67518, a 32Kx18 device, and the MCM67618, a 64Kx18 device, are the best suited for Pentium-based designs. Key to the success of a zero wait solution is the SRAM's support of Intel's burst protocol. A 2-1-1-1 (zero wait state) burst read cycle can be performed at cycle times of 20 ns and less. Pipelined addressing can further reduce a burst cycle to a 1-1-1-1 count. The MCM67B618 and MCM67B518 are synchronous BiCMOS SRAMs that feature wide x18 data paths, burst reading and writing, byte-write capability, 3.3 V I/O compatibility, and asynchronous output enable control. Note that all BurstRAM operations occur on the rising edge of clock (CLK).

Four (4) MCM67618 devices provide a single bank of 512K byte L2 cache. The interface to the Pentium chip is a direct connection for address and data paths. These new BurstRAMs (MCM67B518, MCM67B618) have been designed to operate at clock rates of up to 66 MHz (15 ns cycle time). They are available in access times of 9/12/18 ns with cycle times of 15/20/30 ns, respectively. The term "access time" is used loosely for synchronous SRAMs and is more accurately, CLK-to-VALID DATA time.

WHAT IS A BurstRAM™ ?

BurstRAMs are synchronous SRAMs that contain input registers for address, write, and enable signals and have an on-chip burst counter that imitates the i486 and Pentium's lower order address burst count. These control signals are registered into the BurstRAM on the rising edge of the CLK input. Three (3) control pins allow complete control of the burst function. $\overline{ADSP}$ (ADS Processor), $\overline{ADSC}$ (ADS Controller), and $\overline{ADV}$ (ADVance) control the burst read/write functions as well as single read/writes. A self-timed write is also provided for the purpose of simpler (and relaxed) write timing. Byte-write capability is provided with the $\overline{UW}$ and $\overline{LW}$ (Upper/Lower byte Write) signals. Note that all control signals are active low. See Figure 2.

THE BURST CYCLE

A burst read cycle is performed as follows (see Figure 3):

1. During the first cycle (T1), the CPU generates ADS and a valid address, and the BurstRAMs register the external address A<18:3> and enable on the rising edge of the system clock (CLK). This address can be considered the base address from which the BurstRAM begins its address counting,

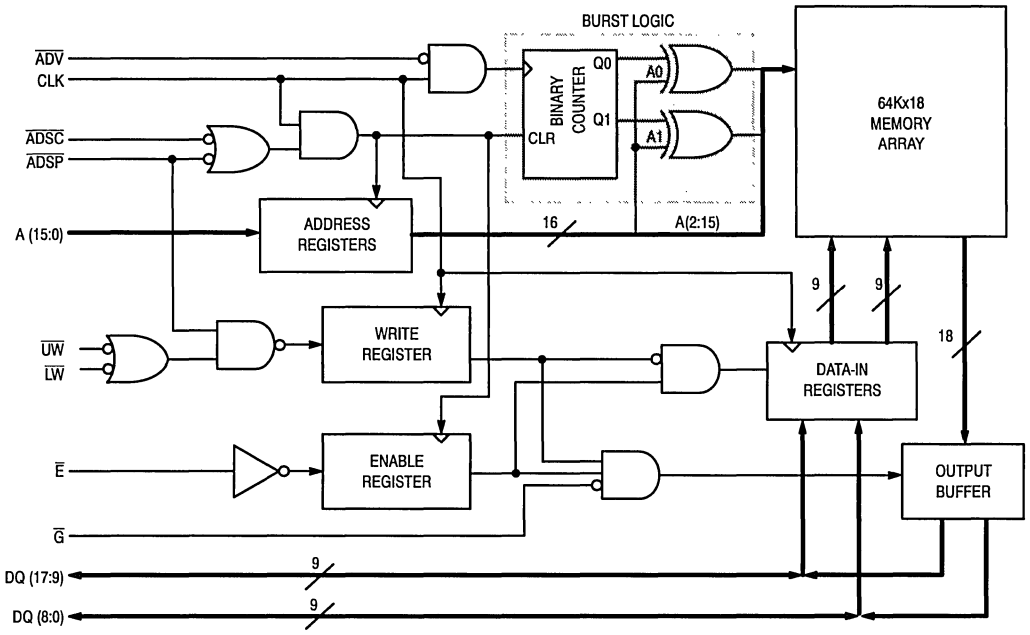

Figure 2. Block Diagram of 64Kx18 BurstRAM

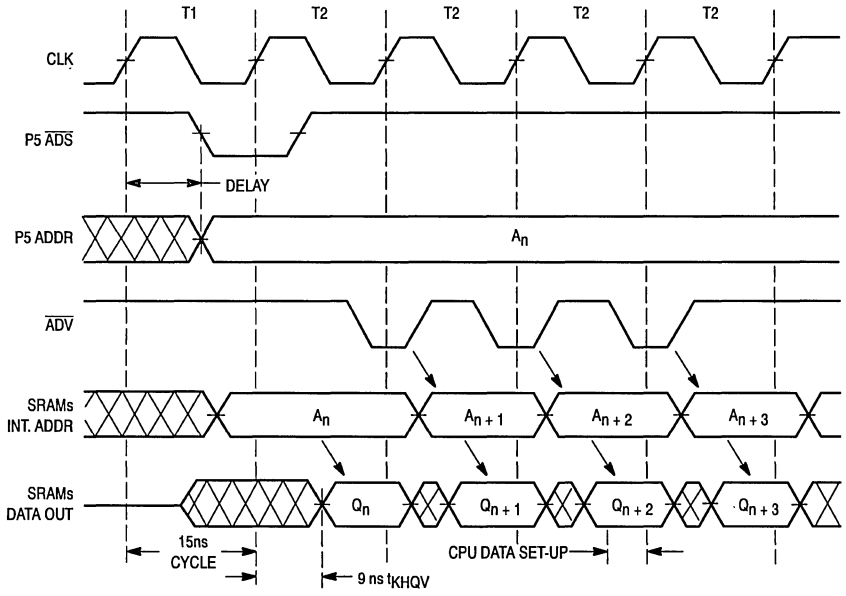

Figure 3. 64Kx18 BurstRAM Performing 2-1-1-1 Burst READ

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2. Assuming the cache controller has determined that the cycle is a cache hit, the first 8 bytes of valid data are driven onto the data bus 9 ns after the second rising clock edge,
3. Subsequent cycles present valid data upon the negation of $\overline{ADS}$ and the assertion of $\overline{ADV}$. An entire 32 byte cache line can be supplied to the CPU in just five cycles. The BurstRAM's output enable ($\overline{G}$) can be asserted well into the 2nd cycle since it is asynchronous and represents only 5 ns delay.

Pentium operates with external bus speeds of 60 MHz and 66 MHz. This corresponds to 16.6 ns and 15 ns cycle times, respectively. Standard asynchronous SRAMs are hard pressed for a zero-wait state application. A look at the timing reveals that sub-12 ns SRAMs would be required since Pentium's data set-up time is about 3 to 4 ns. The inclusion of on-chip logic allows the BurstRAM to be directly connected to the CPU, and avoids the timing penalty associated with glue logic.

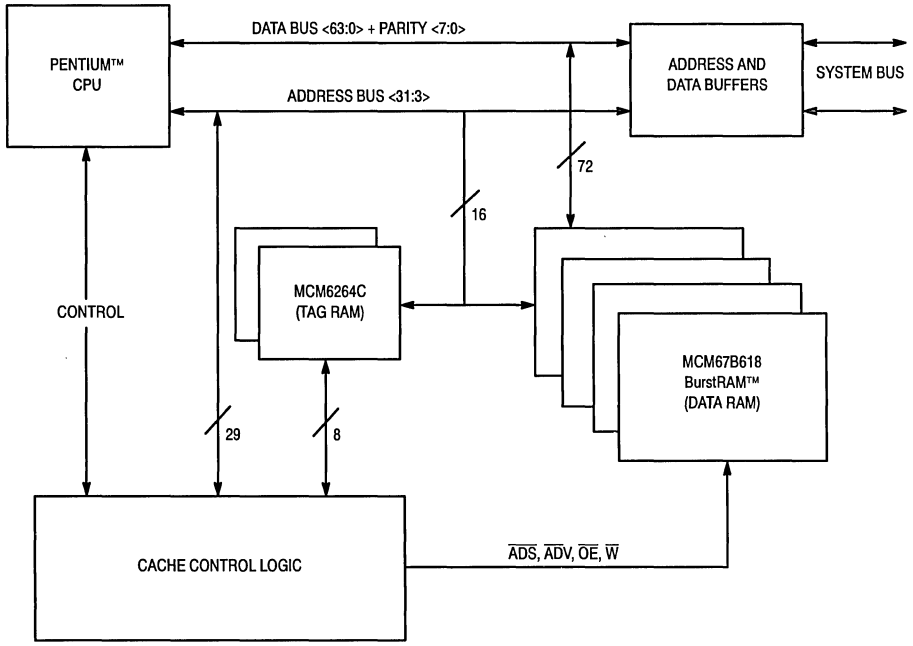
Using the BurstRAM, a zero wait state burst write cycle can be performed as well. Upon the CPU's assertion of $\overline{ADS}$, the BurstRAM begins and completes a burst write cycle with the assertion of $\overline{E}$, $\overline{LW}$, $\overline{UW}$, and $\overline{ADV}$ signals. A burst write cycle can be started using either $\overline{ADSP}$ or $\overline{ADSC}$. If $\overline{ADSC}$ is sampled low (while $\overline{ADSP}$ is high), data can be written immediately to the BurstRAM while $\overline{ADV}$ is asserted on subsequent cycles for the completion of the burst cycle. If $\overline{ADSP}$ is sampled low (while $\overline{ADSC}$ is high), the write register is blocked inside the BurstRAM and consequently only allows A<15:0> and $\overline{E}$ to be registered. On the following cycle ($\overline{ADSP}$ and $\overline{ADSC}$ negated), the burst write operation begins assuming $\overline{LW}$ and $\overline{UW}$ have been asserted. Again, $\overline{ADV}$ must be asserted on subsequent cycles to complete the burst cycle.

The use of a synchronous SRAM makes a design simpler in the sense that address and control signals can have looser timing constraints since they are registered in, and the SRAM does the rest. As long as DQ<17:0>, $\overline{LW}$, and $\overline{UW}$ signals comply with the required set-up (2.5 ns) and hold (0.5 ns) times, complex off-chip write pulse generation can be eliminated. An undue burden will be placed on the controller to provide proper write pulse width and write timing edges relative to address and the CPU's valid data.

SYSTEM CONFIGURATIONS

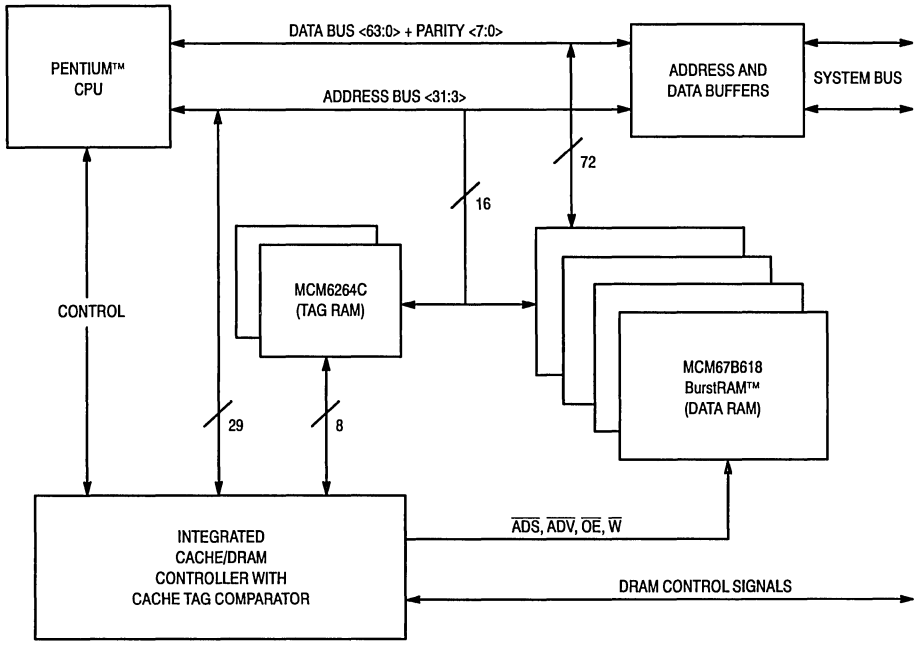
Pentium's 64-bit data path will require four (4) MCM67B618s (or MCM67B518s) to provide a single bank 512K (256K) byte L2 cache. The interface to the Pentium chip is a direct connection for address and data paths. Control signals must come from the cache controller. See Configurations A/B/C of the System Block Diagrams.

Configuration A is the least integrated solution, one that uses external tag RAM and a PAL or ASIC for the cache controller. The DRAM controller would be yet another component in the system.



Configuration A
Secondary Cache Solution for Pentium — 512KByte

Configurations B and C are the most likely approaches taken by chipset vendors in which the tag RAM may or may not be integrated, but will probably integrate the DRAM control. For direct-mapped caches such as these, tag RAM size depends on the controller's mapping of tags (or sectors) to cache lines. Each sector may consist of 1, 2, 4, or more cache lines. Tag RAM depth is then 16K, 8K, 4K, or so, respectively.



Configuration B
Secondary Cache Solution for Pentium — 512KByte

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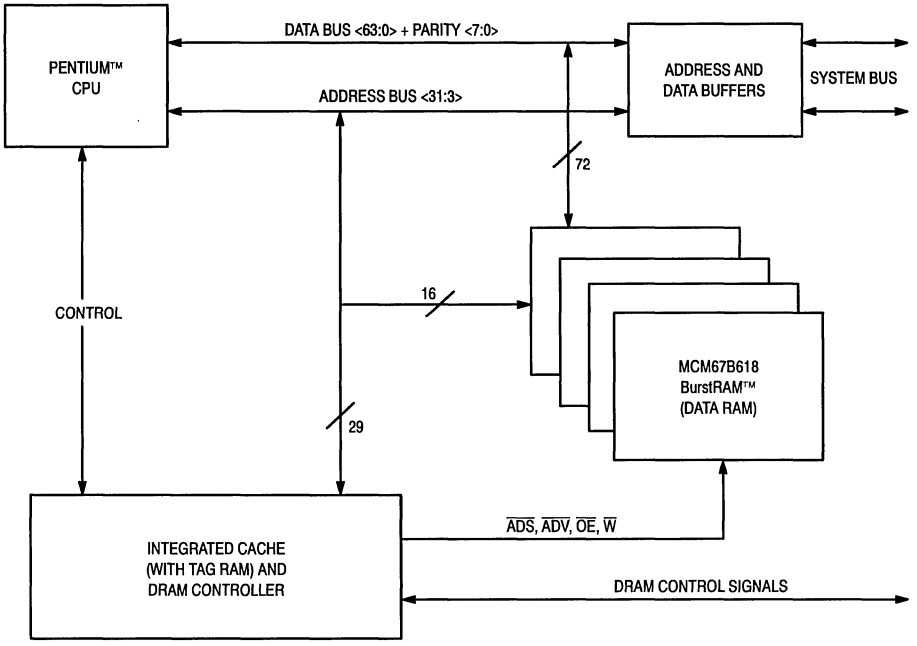
The tag RAM must be at least 10 ns for zero wait state performance; otherwise, a lead-off wait state must be added (3-1-1-1). This is determined by the speed of the controller's tag comparison as well. If the cache line size is 32 bytes and the data RAM depth is 64K, the tag RAM will have to be a 16Kx8/10 or 4Kx8/10 organization. The tag RAM's width (data path) is a function of the system's main memory size. An 8-bit tag will allow a cache size of 512KB to cache 128MB of main memory.



Configuration C
Secondary Cache Solution for Pentium — 512KByte

FEATURES OF 64Kx18

The 64Kx18 SRAMs are fabricated on a BiCMOS process and exhibit less dependence on output loading compared to CMOS devices. These SRAMs are powered on a single 5 V supply (± 5%) and are 3.3 V I/O compatible — no additional power supplies are required. The output buffer is composed of an NPN pull-up and an N-channel MOS pull-down. The pull-up circuitry has been carefully designed to limit the NPN's base drive such that the output pulls up to approximately 3.3 V even under high supply conditions (e.g., 5.25 V). These 3.3 V "friendly" output buffers have controlled 3.3 V output swing and will not overdrive a future 3.3 V controller or processor. This important feature allows one to easily migrate from an all 5 V system to a mixed 5 V – 3.3 V system upon the availability of 3.3 V Pentium and controller chips.

SYSTEM CONSIDERATIONS

The entire 64Kx18 SRAM family makes use of multiple power and ground pins on the 52-lead PLCC package. Five (5) power and five (5) ground pins (6 pairs for the asynchronous devices) have been provided to allow adequate supply decoupling and return current paths for such a fast device. Multiple power and ground pins reduce the effective inductance of theses connections. Since the output buffers swing 3.3 V in 1 to 2 ns (t_r/t_f), significant di/dt currents flow in the V_{CC} and V_{SS} pins. Separate power and ground planes on the printed circuit board are highly recommended and will help improve signal integrity, ground bounce, and in turn the SRAM's access time. The use of a 0.001 µF or 0.01 µF chip capacitor or similar leadless (surface mount) capacitor connected within 0.5 inch or so of each pair of V_{CC}/V_{SS} pins will provide a low impedance path for the fastest transients. A single 1 to 4.7 µF chip or ceramic capacitor per device should be sufficient for dc stability.

The use of standard (asynchronous) SRAMs may prove to be very difficult to use in 50+ MHz systems due to the requirements of carefully controlling the signal integrity, maintaining good noise margins, keeping component count down, and reducing board space. Because the BurstRAM, a synchronous device, registers address and control signals during a very brief moment during the system cycle, noise occurring throughout most of the cycle in the system can be tolerated by the BurstRAM. Component count, and therefore board space, is reduced since these SRAMs integrate the burst counter logic and self-timed write circuitry onto the chip and, in addition, have a wide (x18) data path. Because of the on-chip logic, cache control logic can be simplified and some control signal timing can be relaxed.

In cases that demand detailed timing analysis and a close look at the analog effects of your board design, it is recommended that a board-level (Quad Design/Viewlogic) or SPICE simulator is used. Particularly when PCB routing lengths are about 4 inches or more, transmission line effects become dominant over the lumped circuit equivalent. Since interconnect time-of-flight is approximately 175 to 190 ps/inch, a 4 inch route adds about 0.75 ns to a memory access.

When analyzing the cache data read path, the DQ<17:0> are in their active state and drive the data bus. The characteristics of these output pins are important to know when completing a board's physical layout. Use the information in Table 1 (output buffer I-V data), Table 2 (input I-V data), and Table 3 (package parasitics) to help verify your timing and loading effects. This tabular data may be used directly as input to board level simulators, such as those offered by Quad Design, Integrity Engineering, Quantic Labs, etc. Figure 4 shows how to connect the parasitic package components between the chip (output buffer or input) and package pin. An input pin on the 64Kx18 can be modeled as C die = 4 pF.

Table 1. I-V Characteristics of the 64Kx18 I/O Buffers

V_{OL} (V)	I_{OL} (min) (mA)	I_{OL}(max) (mA)	V_{OH} (V)	I_{OH} (min) (mA)	I_{OH} (max) (mA)
0	0	0	0	– 110	– 145
0.5	38	60	0.5	– 106	– 136
1.0	68	107	1.0	– 96	– 124
1.5	90	137	1.5	– 78	– 102
2.0	104	154	2.0	– 55	– 77
2.5	110	160	2.5	– 29	– 45
3.0	112	162	3.0	– 7	– 13
3.5	113	163	3.5	0.3	0.2
4.0	114	164	4.0	0.7	0.6
4.5	115	164	4.5	1.4	1.3
5.0	115	164	5.0	2.0	2.0

Table 2. I-V Characteristics of the 64Kx18 Inputs (Address and Control)

Diode to GND		Diode to V_{CC}	
V_{in} (V)	I_{in} (mA)	V_{in} (V)	I_{in} (mA)
0	0	5.0	0
– 0.4	0	5.4	0
– 0.5	0	5.5	0
– 0.6	0	5.6	0
– 0.7	– 0.1	5.7	0.1
– 0.8	– 2.0	5.8	2.1
– 0.9	– 25	5.9	20
– 1.0	– 70	6.0	50

Table 3. Packaging Characteristics

	Min	Max	Unit
R package	50	200	mΩ
L package	3	6	nH
C package	0.5	1.0	pF
C die	2	7	pF

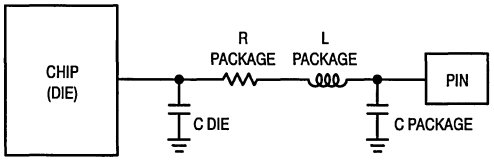


Figure 4. Package Parasitics Schematic

OUTPUT BUFFER CHARACTERISTICS

The access times guaranteed in the datasheet are based on a 50Ω test load and should be derated for unterminated CMOS loads. Refer to the derating curve (Figure 5) for your application. This curve relates the difference in access time between a 50Ω test environment and a lumped capacitive load (no dc load) condition typically found in most applications. The curve is based on worst case conditions, i.e., V_{CC} = 4.75 V and T_A = 70°C. Note that the 50Ω test condition is equivalent to a lumped 10 pF load. For instance, if the BurstRAM outputs see a 30 pF load, derate the access time by about 0.4 ns. So, for a Pentium design that uses the MCM67B618 – 9 ns device, one can expect a worst case access time of 9.4 ns under these conditions.

SUMMARY

For high performance Pentium systems, the use of Motorola's 64Kx18 BurstRAMs provides a straightforward solution to Pentium's secondary cache requirements. Four BiCMOS BurstRAMs support the size and speed required by zero wait state Pentium systems. For equivalent cache size and performance, standard SRAM solutions warrant two bank interleaved approaches that utilize more board space, require more power, and demand a higher performance cache controller.

REFERENCES

1. AP-469: "Cache and Memory Design Considerations for the Intel 486DX2 Microprocessor", Intel Corp.
2. DL156/D: *Fast Static RAM BiCMOS, CMOS, and Module Data*, Motorola, Inc.

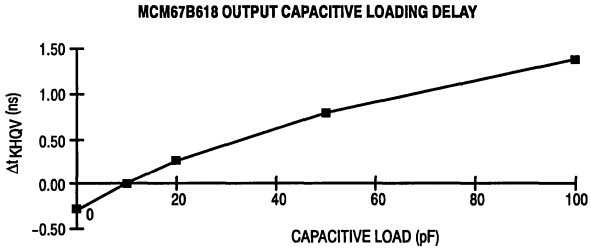


Figure 5. Access Time Derating Curve

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AN1231

Plastic Ball Grid Array (PBGA)

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(MMTG Final Manufacturing Operations)

INTRODUCTION TO THE PBGA

The Plastic Ball Grid Array or PBGA package is the industry description of what is sometimes referred to as Motorola's OverMolded Pad Array Carrier or OMPAC package. It was developed by Motorola in the late 1980's for use in Motorola products with space limitations such as radios, pagers and cellular telephones. Since that time it has grown in popularity within the electronic industry and standard body sizes and pin counts have been adopted by JEDEC and soon by EIAJ. The many benefits of using PBGA over similar lead count leaded devices include:

1. Board space efficiency.
2. Thermal and electrical performance and ease of enhancing both.
3. Excellent surface mount yields when compared to fine pitch leaded devices.
4. Lower profile (i.e., overall thickness).
5. Almost unlimited pin count capability.
6. Compatibility with existing surface mount, test and handling equipment.
7. Potential lower total cost of ownership compared to leaded devices due to reduced scrap, rework and lack of need for fine pitch assembly equipment.

This application note serves to provide general information about the PBGA package as well as provide information about its implementation into products and surface mount assembly.

PACKAGE CONSTRUCTION

The PBGA package is based on a printed circuit board (PCB) substrate or "leadframe" fabricated of Bismaleimide Triazine (BT) epoxy/glass laminate. This material is used over standard and multi-functional FR4 laminates for its high glass transition temperature of 170 – 215°C and heat resistance (230°C exposure for 30 minutes with no degradation). The standard core thickness of this two layer substrate is typically 0.2 mm with 18 μm (half ounce or 0.7 mil) copper on each side. A two mil thick (thickness over epoxy glass) dry or dual pass wet film soldermask is currently used to ensure that all the substrate vias will be completely tented. The silicon chip containing an integrated circuit is die bonded to the top side of the substrate using silver-filled epoxy typical of that found in leaded devices. The chip is then gold wire-bonded to wire bond pads on the circuitized substrate. Traces from the wire bond pads take the signals to vias which carry them to the bottom side of the substrate and then to circular solder pads. The bottomside solder pads are laid out on a square or rectangular grid with either a constant 1.5 mm or 1.27 mm pitch. These two pitches, as well as a 1.0 mm pitch, are prescribed by the JEDEC registration for PBGA which is included in Appendix A. An overmold (or possibly a liquid or "glob-top" encapsulation) is then performed to completely cover the chip, wires and substrate wire bond pads. Typical feature dimensions common to most PBGA configurations, as discussed above, are summarized in Table 1.

Individual preformed 30 mil diameter solder balls are gang dipped in no-clean paste flux using a specially designed pick-up tool then placed on each bottomside solder pad using an internal Motorola developed (by Motorola Manufacturing Systems in Boyton Beach, Florida), but commercially available, robotic bumping cell. To provide somewhat greater fatigue resistance and a finer, more homogeneous solder microstructure, the near-eutectic (62%Sn/36%Pb) solder balls also contain 2% Ag, which results in a solidus temperature of 179°C. The balls are then reflowed onto the solder pads using a conventional forced convection nitrogen reflow oven and a typical surface mount assembly profile with a maximum specified temperature of 230°C. Following reflow, the substrates are centrifugally cleaned in Terpene (CFC-free organic cleaner) to remove flux residue as well as any fibers and particulates from the remainder of the package.

The entire process described above, takes place on a substrate containing several (currently from three to six) PBGA devices. The final step in assembly is the singulation or excise of the individual PBGA devices out of that larger substrate or panel. The resulting device has a body size that now conforms to JEDEC standards, although for the near term some pre-JEDEC devices are included in Motorola's package offerings. The package outline dimensions for several PBGA configurations (86, 119, 169, 225, and 357 pins) currently offered by Motorola are included in Appendix B. The total number of I/Os on the package is obviously determined by the body size and pitch. Additionally, the JEDEC standard allows for any number of balls to be depopulated from a completely populated matrix (i.e, staggered pitch or center balls depopulated). A cross-sectional rendering of a device mounted to a PCB is pictured in Figure 1.

Table 2 provides nominal room temperature values for the physical properties of all the materials that comprise the PBGA package. It is important to note that the properties of many of the PBGA materials have a temperature-dependence that is not included in the table.

Table 1. Typical Nominal Dimensions of Selected PBGA Substrate Features

Feature	Dimension (mil/mm)	Comment
Substrate Thickness (Two Layer)	7.9/0.20 14.1/0.36	BT/glass laminate core thickness. Overall (BT/glass + Cu + soldermask).
Substrate Thickness (Four Layer)	15.7/0.40 24.0/0.60	BT/glass laminate core thickness. Overall (BT/glass + Cu + soldermask).
Copper Thickness	0.71/0.018 1.2/0.030	Clad to BT/glass laminate. Plated on (electroless + electrolytic).
Trace/Space Widths	3.5/0.090	Minimum.
Soldermask Thickness	2/0.05 1.2/0.03	Over BT/glass. Over copper features.
Via ϕ	9.8/0.25 15.7/0.40	Typical Minimum. Normal.
Solder Pad Cu ϕ	35/0.89 30/0.76	Standard. Specific 1.27 mm pitch devices.
Soldermask Opening ϕ	25/0.64 22/0.56	Standard. Specific 1.27 mm pitch devices.

NOTE: ϕ = Diameter. All dimensions are approximate and are for reference only.

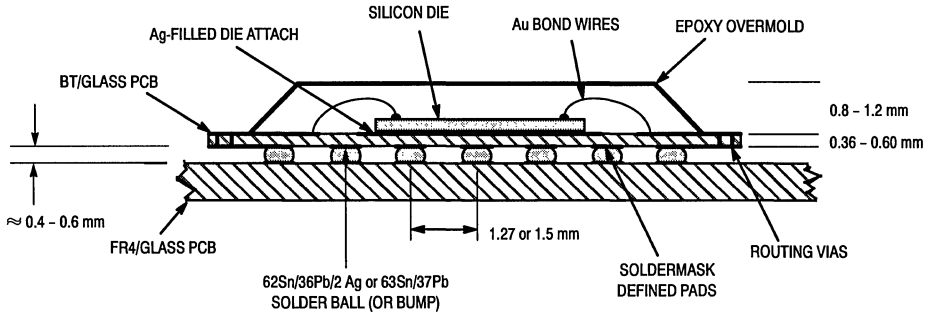

Figure 1. Cross-Sectional View of an PBGA Mounted to a PCB

Table 2. Physical Properties of All Materials Used in the PBGA Package at 23°C

Material	Elastic Modulus (ksi)	Poisson's Ratio (–)	T_g (°C)	CTE – x, y/z < T_g (ppm/°C)	Thermal Cond. (W/m-°K)
Copper (ED/Rolled)	17,500	0.345	1085 (melt)	17	418
62% Sn/36% Pb/2% Ag Solder	4,600	0.4	178 (melt)	21	50
Dry Film soldermask	300	0.45	≈120	50	0.33
BT/Glass Subtrate	2,760	0.195	170 – 230	15/57	0.19
Silicon Die	18,900	0.278	1412 (melt)	2.6	83
Mold Compound	2,200	0.25	196	15	0.67
Ag Filled Epoxy Die Attach	1,070	0.3	77	52	1.38

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MOTHERBOARD LAYOUT

The PBGA package, with its leads or balls in an array configuration, presents some unique challenges to overcome with respect to motherboard routing when compared to peripherally leaded devices. Additionally, the volume of solder in the joint is relatively large and since all of it is molten during reflow, special considerations must be taken when determining appropriate pad geometries.

FOOTPRINT GEOMETRY

A solderable surface defined by soldermask, also called a soldermask defined (SMD) pad, has traditionally been used and recommended by Motorola for the PBGA. This is because the soldermask defined pad provides better adhesion strength to the PCB. This greater adhesion comes from the fact that the copper pad diameter is greater than that of the soldermask opening with the overlapping soldermask providing added strength. Since the strength and compliance of solder balls is far less than that of leads, the copper pad/FR4 laminate adhesion becomes a relatively weaker link than with leaded devices. This extra strength could be important in certain extreme bending and high thermal mismatch-induced stress situations (i.e., large package or die, large and rapid temperature swings).

The diameter of the solderable surface is generally chosen to match that on the PBGA. The standard PBGA soldermask opening is specified at 25 mils for all 1.5 mm pitch devices. As the pitch is reduced to 1.27 mm and the package substrate routing becomes more difficult, some devices have required reducing the soldermask opening and copper pad diameters to a specified 23 and 31 mils, respectively. The copper pad diameter is chosen to allow for the worst case soldermask to artwork misregistration that may be encountered. For the majority of PCB fabricators the tolerance on that misregistration is from ± 2 to ± 4 mils and can be as much as ± 5. Likewise, the soldermask opening has some dimensional variation from overdeveloping and aperture diameter changes to compensate for the same. The tolerance on the soldermask opening should be chosen such that its diameter is never less than that on the PBGA. Having a joint with a larger diameter at the device than at the board may cause it to be more unstable while molten and increase any risk of shorting. Therefore, it may be advantageous, for example, to specify an opening with a 26 mil nominal diameter in the case of a PCB supplier who can guarantee a ± 1 mil tolerance. Figures 2a to 2c give examples of various soldermask defined pads, one of which (Figure 2a) is shown with some possible dimensions. The various routing trade-offs associated with different pads for 1.27 and 1.5 mm pitch packages will be discussed later.

The individual pad geometry also has to incorporate the desired escape method to be used between routing to other board layers with vias or simply routing on the device layer (or typically, a combination). The pads shown in Figures 2a and 2b have integral vias to take the signal immediately to another layer while the Figure 2c and 2d pads have traces exiting them which keep the signal on the component layer. The connection between the via and adjacent via pad can either be with a trace (which forms what is referred to as a dumbbell or dogbone pad) or by simply filling in the entire area between the via pad and solder pad to form a teardrop pad.

Another integral via geometry technique that has been tried is to put a via concentric to the pad or via-in-pad (VIP). Special consideration must be taken with this configuration with regard to the volume of the via and its "thieving" of solder from the joint which results in a much lower device stand-off. Ways to get around this problem are to compensate by screen printing extra solder paste, tent the via with copper, use the minimal cost-effective via diameter possible and/or request completely solder filled vias from the PCB fabricator. It should be stressed that only minimal data exists as to the reliability and processibility of the VIP configuration and it is only mentioned here as an option that requires further investigation.

Non-soldermask (NSMD) or copper defined pads, as shown in Figure 2d, pads have also been used successfully with the PBGA. In this case there is a soldermask clearance area around the copper pad. Due to the large volume of solder present in the PBGA ball, the solder will wet down the sides of the pad in the case of a non-soldermask defined pad. This will result in an effectively greater diameter joint and lower accompanying stand-off (see Figure 3). This lower stand–off can result in a reduced attachment reliability in accelerated thermal cycling.The same considerations as mentioned above with regard to soldermask to artwork registration tolerances have to be applied to a non-soldermask defined pad in determining the diameter of the soldermask opening so that it does not touch or exhibit tangency to the copper pad. In determining which pad to ultimately use, the application environment, the desired board technology/ cost, and the assembly characteristics need to be taken into account.

ESCAPE ROUTING

The main perceived drawback of using BGA is the challenge of routing all the required signal, power and ground pins to the system board without increasing printed circuit board (PCB) complexity and therefore cost. Fortunately, this challenge is easily overcome by Motorola with thoughtful package pin assignment and device configuration considerations (pitch, ball count, ball depopulation methods) in conjunction with the choice of solder pad geometry and board technology (number of layers and line/space widths). If signal pin assignments are made too deeply within the BGA matrix, board level escape using conventional eight mil printed circuit board fabrication technology becomes difficult for large matrices. Current PCB technology with eight mil lines and eight mil spaces typically does not incur any additional cost. For this reason Motorola attempts to perform signal pin assignment such that the outer four rows of the PBGA contain all the signals that must be escaped. The Motorola 68356 chip is an example of such a properly assigned BGA footprint that provides users with easy board–level escape with no cost adders for sub–eight mil line and space board technology or internal signal layers. The 68356 is a Signal Processing Communications Engine with integrated functions such as a 68000 based microprocessor, RISC communications core, 24 bit DSP and a PCMCIA controller. The device is housed in a 25 mm PBGA, using a 1.27 mm or 50.0 mil ball pitch. The balls are in a 19x19 array with the four corner balls depopulated to result in 357 pins.

One of the key features that facilitates the routeability of this package is the location of the power and ground assignments to an 11x11 matrix in the center of the package. Within

this inner matrix, the centermost 9x9 pins form a ground bus and the remaining 40 pins encircle that with what is called a power ring. Those power and ground pins do not need to be escaped as they are dropped straight down using dumbbell or teardrop shaped pads with offset vias to the associated power and ground planes on the circuit board. This leaves the outer four rows containing 236 signal pins around the perimeter of the package that need to be escaped. This package itself has 23 mil diameter solder pads on it and the same solderable surface diameter or only slightly larger is recommended for the PCB. Therefore, using a 23 mil non–soldermask defined pad in conjunction with a 25 mil diameter via pad a board employing eight mil lines and spaces can be used to easily route these four outer rows using two signal layers. The escape routing of the outer two rows can be achieved on the topside of the PCB without using vias and the third and fourth rows from the outside are escaped by dropping down vias and escaping on the bottomside. This example is illustrated in Appendix C, which shows a representative top and bottomside signal layer routing schematic for the 68356.

A similar package design methodology is used on other devices packaged in BGA such as Fast Static RAM devices that utilize a 7x17 and soon a 9x17 array PBGA, the PowerPC 603™, PowerPC 604™ microprocessors as well as the MPC105 PCI Bridge/Memory Controller for PowerPC™ microprocessors that will be available in a ceramic BGA. The fact that this 119 pin FSRAM package only contains seven rows in one direction further simplifies routing since there are a maximum of three buried rows. As can be seen in Table 3, no matter what geometry (diameter and SMD versus NSMD pad configuration) is chosen for 1.5 mm pitch PBGA devices one eight mil trace can always be routed between two solder pads. Only if NSMD pads are used an eight mil trace can be routed between two pads at 1.27 mm pitch. As can be seen in Table 3, a maximum trace width of six mils would be needed to use an SMD pad.

As PBGA pin count and matrix size increase it may be necessary to make signal assignments on more than just the four outer rows. This would require more that one buried row on each of the outer layers to be escaped on a given PCB layer to maintain a two signal layer board. When this becomes the case, trace size will have to decrease further from the standard eight to six. Table 3 also shows how many traces can be routed between two pads for given line and space technologies down to three and three and all the current standard PBGA pad diameters. For example, when and if it becomes necessary to route two signal traces between NSMD pads at 1.27 mm pitch, five mil trace widths will be necessary to avoid adding extra signal layers. If SMD pads were used those traces could only be three mils wide maximum. This example once again underscores the routing advantages of NSMD pads.

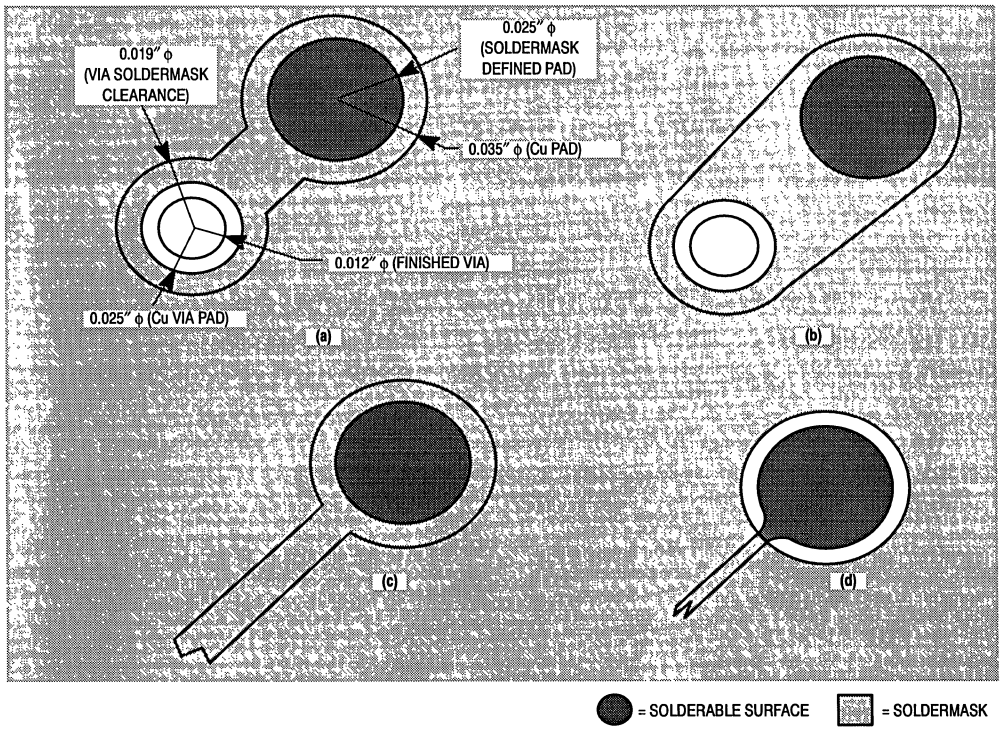

Figure 2. Pad Options for PBGA Motherboard Routing: a) Dumbbell pad shown with typical dimensions, b) Teardrop, c) No integral via for escaping onto top layer, d) PBGA version of standard surface mount pad with soldermask clearance around the solder pad.

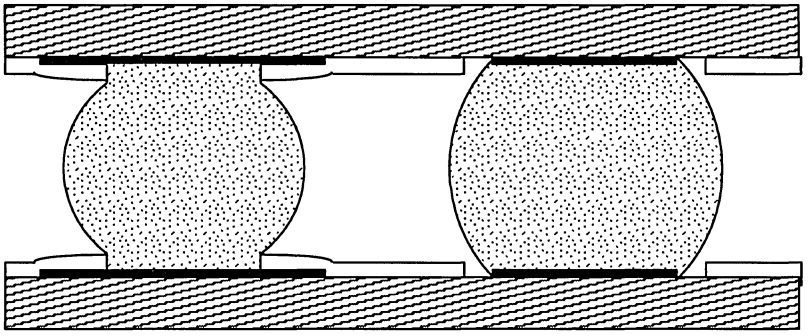

Figure 3. Comparison of PBGA Solder Joints with: a) soldermask-defined pad and b) conventional non-soldermask defined pad. Note the greater volume of solder and greater effective joint diameter for the non-soldermask defined pad to achieve the same stand-off.

Table 3. Number of Escape Traces That Can Be Routed Between PBGA Pads Given Device Pitch, Pad Diameter, and Board Line/Space Widths

Board Technology (Line/Space Widths in Mils)	Number of Escape Traces Routed Between Pads Given Ball Pitch and Pad Diameter in (mms/mils). Shaded Columns Represent NSMD Pads.							
	1.5/23	1.5/25	1.5/31	1.5/35	1.27/23	1.5/25	1.27/31	1.27/35
3/3	5	5	4	3	5	3	2	2
4/4	4	3	3	2	2	2	1	1
5/5	3	2	2	1	2	2	1	1
6/6	2	2	1	1	1	1	1	
8/8	1	1	1	1	1	1		

Note: When encountered, fractions of traces were rounded down.

SURFACE MOUNT ASSEMBLY

One of the greatest advantages of the PBGA package is that it can typically be placed onto printed circuit boards and assembled using existing surface mount equipment. This is not true for many other new and high pin count packaging technologies such as TAB, DCA, fine pitch QFPs, PGA, etc. Most require new or upgraded process equipment and in some cases new processes or manual assembly. It has the added advantage of being completely compatible with existing handling systems. Open tooled handling media, namely trays and tape and reel (heat seal or C-pak) are available for many of the JEDEC PBGA body sizes. Handling damage is significantly reduced by package robustness due to the absence of fragile leads.

FLUXING

Either solder paste (cream), paste flux or liquid flux (i.e., spraying, dispensing, or foaming) must be applied to the PC board solder pads prior to assembly. This is necessary to not only reduce oxides formed on the solder pad, but also on the solder ball. Slight solder ball oxidation may occur during exposure to burn-in, storage, and dry baking in non-inert atmospheres. Typically, the method chosen to apply flux is done to maintain compatibility with current processes. Due to the fact that the solder ball is comprised of eutectic or near-eutectic solder and its entire volume is molten during reflow, it is not necessary to add solder volume to the joint with solder paste. The 30 mil diameter ball provides enough volume to give an 18 to 24 mil average stand-off across the device depending on package and device/board solder pad configuration. This is typically enough stand-off to ensure that no opens will occur due to device or board warpage at elevated temperatures (more discussion on device warpage in the Coplanarity section). Applying an amount of solder paste equal to 14% of the ball volume (i.e., eight mil stencil, 25 mil diameter apertures, final solder volume = 1/2 solder paste volume) will generally increase the stand-off by one to two mils. In some cases additional solder volume may be advantageous to increase stand-off and subsequent device solder joint reliability. However, applying larger amounts of solder paste with the use of thicker stencils and/or larger apertures has the potential to result in joint voiding, especially when combined with fast oven ramp rates and volatile fluxes. Voids are formed when flux volatilizes and is entrapped within the joint. Voids form at the bottom (motherboard interface) of the ball, but end up at the joint/package interface due to buoyancy effects. These voids have been shown not to be a reliability risk. Figure 4 shows a pad from an PBGA test board with eight mils of solder paste screenprinted onto it prior to device

placement. Besides screening solder paste, pin transfer and single point dispense of paste flux have also been used successfully on PBGA within Motorola.

DEVICE PLACEMENT

Due to the large pitches involved relative to fine pitch QFPs, pick and place is much simpler and involves lower required machine accuracies and resolutions. Additionally, due to tight ball pattern to device edge tolerances (better than ± 3 mils) relative to the pitch, placement can be performed off of the body outline. This is the method currently used for much smaller devices in the industry using extremely fast "chip-shooters". Additionally, new equipment with upward looking vision or lasers (dual lasers or better are recommended over a single laser system) that are specifically designed for the ball grid array are becoming available. This equipment centers off the ball array itself and can also check for missing balls and in some cases calculate device coplanarity real-time. Finally, due to the fact that the PBGA is self-centering in the reflow process, a device can be placed up to 50% off pad and still be expected to align itself. The self-centering feature, which is a result of the surface tension of the molten solder, can be easily observed by placing devices deliberately off pad and reflowing.

REFLOW

Surface mount reflow of the PBGA device is similar to that of leaded devices. The process of reflowing a PBGA is sometimes referred to as a Controlled Chip Carrier Collapse Connection or C5 since the solder ball starts with an approximate height of 25 mils (plus paste if any) and collapses down three to seven mils during reflow due to the weight of the package and wetting of the motherboard pad. Devices have been reflowed successfully in IR, convection and mixed heating ovens as well as with vapor phase. Care must obviously be taken that each solder joint is exposed to the solder solidus temperature immediately following a flux-dependent high temperature soak period in which the flux is mobile and active. An example of an IR reflow profile (not optimized) obtained by placing thermocouples under two different devices at the middle and corner of a 4.5″ x 7.5″ four layer test board is presented in Figure 5. The main difference in reflowing the PBGA lies in the fact that the joints are heated more from the package and board as opposed to direct air impingement or IR exposure onto the leads. It is relatively easy to obtain a suitable profile with boards containing a variety of surface mount and through-hole device types along with the PBGA.

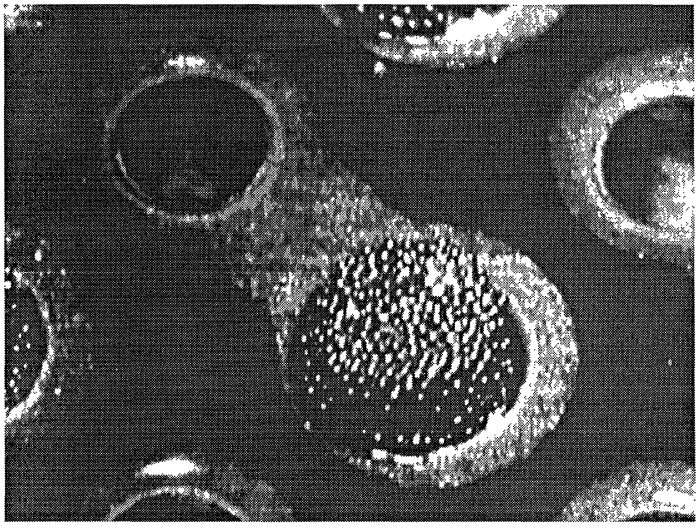

Figure 4. Micrograph of an PBGA Test Board Pad with Eight Mils of Screenprinted Solder Paste (Magnification of Approximately 40X, 45°)

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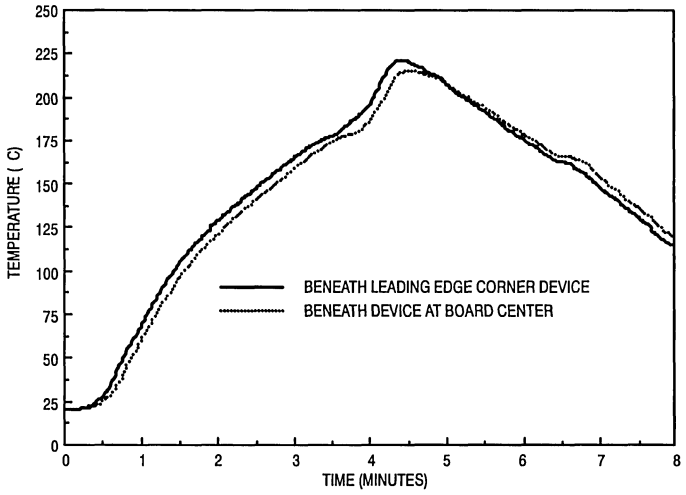


Figure 5. PBGA IR Reflow Profile Obtained by Placing TCs Underneath Devices

Another difference between PBGA and typical leaded devices is in profiling. The profiling thermocouple(s) (TC) must be placed underneath the package and preferably within an actual solder joint. This requires using thinner TC wire than may typically be used as to allow the device to solder to the board almost normally with minimal tilt or non-contacting balls. A suggested procedure for making a profile board is to solder the TC bead to a ball under the device. The center ball is recommended since it is likely to exhibit the minimum peak temperature and is therefore the worst-case position for a cold solder joint. It is advantageous to also TC the outermost ball on the leading edge of the device to obtain worst case maximum temperatures. The device is then hand placed onto a prefluxed board footprint, secured with the minimal amount of polyimide (i.e., Kapton™) tape possible and reflowed. The tape is then removed and the board can be used for repeated profiles, assuming the TC did not break free and that the device reflowed somewhat normally onto the board. An alternate way of more securely fastening a TC is to remove a PBGA ball with a solder sucker or wick and to attach the bead to the site using high-temperature solder or thermally conductive epoxy. Drilling a hole through either the top of the device or the bottom of the board for subsequent thermocouple placement can also be done successfully. Also, inserting a TC with thermal grease on the bead under an already mounted package can sometimes yield sufficient results.

COPLANARITY

The JEDEC standard for maximum allowable noncoplanarity is currently 0.15 mm (5.91 mils), regardless of package size or pin count. This coplanarity is defined in the standard as the maximum distance from the highest ball to a seating plane formed by the three balls that the package would rest on if placed on a perfectly flat surface. Any lack of PBGA coplanarity is a result of two elements, the warpage of the overmolded substrate and differential substrate pad to-solder ball tip heights. The substrate warpage is typically the major contributor to any lack of coplanarity, while the solder ball heights are relatively uniform. At room temperature, the typical PBGA has a slight upward curvature, such that 225 pin PBGAs with a 27 mm body size have been measured to have a worst case coplanarity of around four mils.

Determining the coplanarity per the JEDEC standard requires scanning all the PBGA bumps and determining the relative positions of their tips in space. Software that takes into account the center of mass of the part must then determine which three balls the device would rest on and the distance from the remaining ball tips to a plane formed by these three seating balls. An automated system, the Model 830B, to do this has been developed by View Engineering and is available now (priced in the mid-$100K range). The system also has the capability to determine the coplanarity to a best fit plane, ball volumes, the absence of balls and the deviation of ball tips from the expected x-y grid. A more expensive and flexible system that also performs printed solder paste height inspection is also available from Synthetic Vision Systems, who are affiliated with View. Among others, RVSI is also a potential equipment supplier.

SOLDER JOINT INSPECTION

One of the perceived drawbacks to using PBGA technology is the fact that, as with any array package, the interior joints are not visible to be readily inspected. Perimeter joints, can be readily inspected. High volume users have presented data showing that the 169 and 225 pin PBGA has one to two orders of magnitude fewer solder-related defects that the 208 PQFP.

X–ray inspection is typically used during assembly process development and for failure analysis. Due to the atomic density of the lead in the solder joints, standard resolution real-time x-ray systems may only be useful in determining shorts and missing or double balls, which are readily observable (see Figure 6). More subtle joint assembly defects like voids, total wetting of the motherboard pad (i.e., full or partial opens) and solder splattering/balling require more sophisticated systems to detect. Very costly x-ray laminography systems (i.e., Four Pi Systems) can detect such features,

although their current cost and image acquisition cycle time may be prohibitive for some users. Fein Focus and Imaging Systems International (affiliated with Nicolet) have both developed lower cost systems with the resolution to identify voids and in some cases non-contact failures. Examples imaged with the Fein Focus Model FXS-160.32 and Nicolet Model NXR-1400, are presented in Figures 7 and 8, respectively. Other systems with similar capabilities are available from Lixi, I.R.T. and others.

A pad geometry design change that can allow detection of non-contact failures or opens involves modifying the motherboard pad footprint. A tab or ear is placed in the soldermask defined pad as in Figure 9. During reflow, solder fills the pad and is readily observed by using even inexpensive x-ray systems. If solder plated or HASL motherboards are used or solder paste is screened on prior to reflow, this ear would already be filled with some solder. In these cases, the x-ray would have to be of sufficient resolution to distinguish between an ear filled by solder from the ball and one already filled by plated, HASL'd or stenciled on solder.

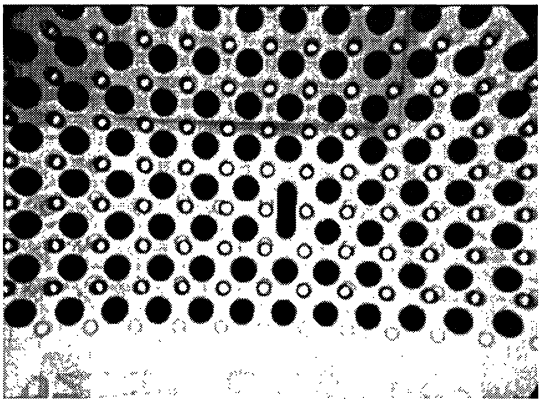


Figure 6. X-ray Micrograph of a Mounted PBGA Showing Solder Shorting

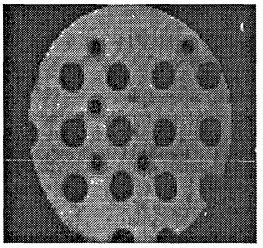


Figure 8. X-ray Micrograph of a Mounted PBGA Showing Solder Splattering/Balling

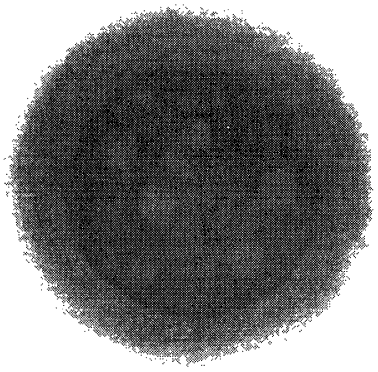


Figure 7. X-ray Micrograph of a Mounted PBGA Showing Voiding in the Solder Joints

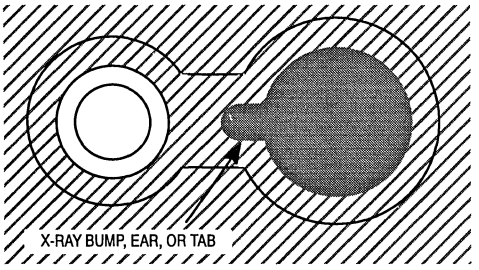


Figure 9. PBGA Pad with Bump to Facilitate X-ray Inspection

REWORK AND REPAIR

The main point that should be stressed when discussing PBGA rework is that since the assembly process gives so much better yields than high pin count, fine pitch leaded devices, that the frequency of rework is greatly reduced. Unfortunately, when one joint is defective the entire package must be replaced since there is no touchup. However, methods and equipment do exist to successfully remove and replace PBGA devices that are found to have assembly or device-related defects.

DEVICE REMOVAL

Typically, PBGA device removal involves simply heating past the solidus temperature of the solder. As opposed to the original surface mount assembly process, no special considerations (assuming the device will be scrapped) need to be taken with respect to ramp-up rates and time over solidus as long as all joints are molten upon device lifting. It may be beneficial to apply a liquid flux beneath the device prior to heating and removal. This flux will facilitate uniform heating and reduce device and board oxidation for subsequent soldering processes. Joints which were not quite molten will appear as "candy kisses" on the board and PBGA after removal. This is a good indication that the device was removed at the earliest possible time, such that the board is being subjected to a minimal amount of temperature-induced damage. If the assembled board has been exposed to out of dry-pack conditions for an extended period of time (24 to 96 or more hours depending on PBGA configuration and ambient conditions) and removal is performed, "popcorning" or die attach delamination will occur. To avoid this the entire assembly must be baked at 125°C for 12 hours. Since the saturation/bake-out curves for PBGA are quite steep, baking for a half to two-thirds of this time will go a long way in preventing popcorning as long as care is taken not to use an excessive ramp-up rate (i.e., > 3°C/min) or maximum temperature (≈ 240 – 250°C).

If other known good PBGAs (or other surface mount devices) are proximate to the device being removed, care must be taken not to overheat them and cause collateral delamination damage. Studies performed by an equipment division of Motorola who are a high volume PBGA user on devices which have body sizes of 19 mm or less indicate that neighboring devices should not exceed 185°C to prevent popcorn at any reasonable saturation level. Also, to minimize temperatures on adjacent devices the nozzle on the rework station should be maintained around 100 mils from the top of the PBGA and heating should be applied only from the top of the device. Additionally, the size of the nozzle should be less than or equal to the device molded body. As opposed to leaded devices which require perimeter heating directly to the leads, reflow of the PBGA is accomplished by heat conducting through the body of the device. Heat can be applied from the bottom also, but as stated earlier, this leads to greater spreading of the heat and an increased chance of damaging or partially reflowing neighboring devices if they are present.

EQUIPMENT

The cost of rework equipment for PBGA, as with leaded devices, varies greatly with features. Some of the features that may be useful to include in rework stations for PBGA are as follows: selectable top and/or bottom heating, selectable IR and/or forced air heating, nitrogen capability, auto-profiling capabilities, split-prism optics manual placement, automated vision placement, and a device removal head or vacuum tool. For the production rework of its smaller PBGA devices, Motorola uses a simple, inexpensive (< $4K) portable rework station made by A.P.E that provides top heating only and has no device placement capabilities. Other PBGA users are known to use the same industry-standard equipment they use for their leaded device rework made by Conceptronics, S.R.T., Air-Vac, Manix, and many others. Prices for these latter machines are ≈ $40K and up without post-removal vision placement capabilities. Of course, special PBGA-specific nozzles need to be bought or made for each of these pieces of equipment. Due to their position as a supplier of rework equipment to Motorola, A.P.E. has nozzles that correspond to most current PBGA body sizes. As PBGA popularity increases, similar nozzles and related tooling will undoubtedly be available from all rework equipment suppliers.

PRE- AND POST-REWORK BOARD CONSIDERATIONS

The principal board consideration during device removal and subsequent replacement lies in the fact that the pad may be soldermask defined and as such damage can occur if the soldermask is subjected to extreme heat and/or has poor initial adhesion to the copper pad. This situation is magnified if the board technology is soldermask over solder (SMOS) which is not recommended. If there are offset vias integral to the tear-drop shaped PBGA pad and they are not filled or tented with soldermask, the web between the usable pad and via pad will be subjected to lifting due to its potential sub 10 mil width. Also, as with reworking all SMT device types, the motherboard itself is subject to other modes of failure such as blistering, delamination and copper/PCB adhesion lifting if overheated or subjected to repeated heat cycles.

SITE PREPARATION AND DEVICE REPLACEMENT

After device removal the pads will typically have a large quantity of solder remaining (approximately half of the ball volume). This solder needs to be removed to allow device placement and facilitate self aligning of the replacement device. Removal can be performed with a solder sucker or more manually with a solder wick. The site should be fluxed prior to replacement with another PBGA device. Generally, solder paste cannot be reapplied due to the interference of a stencil and accompanying fixturing with other devices close to the removal/replacement site. Short of machine replacement with vision, the new device can be placed manually. A board design consideration to aid in this can be a silk-screen or copper pattern on the board that outlines the device body. Split prism optics that allow viewing of the PBGA bump and solder pad patterns simultaneously for alignment prior to device placement are inexpensive and have been used very successfully. The profile that is used to reflow the device should match the initial reflow profile as much as possible, although it is subject to the constraints previously discussed with regard to damaging neighboring devices.

DEVICE TEST, REBUMPING AND POSSIBLE REUSE AFTER REMOVAL

If care was taken in the removal of the device with regard to popcorning, it can ultimately be tested following reballing. If the same amount of solder remains on each pad and it is relatively hemispherical, the device can be tested as is after cleaning with a solvent. The fact that most PBGA test sockets use a pogo pin design that provides several mils (up to ≈ 20) of travel can allow testing even in the presence of smaller or even missing balls. If the bumps after removal exhibit the "candy kiss" shape, it may be necessary to flux, reflow and clean the device prior to test.

Although not recommended by Motorola, costly PBGA devices that are found to be functional can also be reworked for reuse if the process is proven reliable through a full qualification. Such rework would, of course, have to be within the allowable guidelines of the using company. Solder must first be removed from each pad as described above for the motherboard. Without a robotic bumping cell or manual bumping equipment, individual 30 mil diameter solder balls can be dipped in paste flux with tweezers (or paste flux applied to the device), placed on the removed device solder pads and then reflowed. This would definitely allow for test in any socket possibly followed by the normal reuse of the device. Undoubtedly, the time, costs and reliability of doing this need to be weighed with the original device cost to determine feasibility.

SOLDER JOINT RELIABILITY

The decreased compliance of PBGA solder joints as compared to conventional leads has raised concern about its suitability for certain applications where environments are severe (i.e., automotive), required lifetime is long (i.e., telecommunications) or device power is substantial (i.e., microprocessors). This lead compliance is important when a mounted PBGA is subjected to any thermal excursions since the joint typically absorbs the relative device/board expansion and contraction caused by thermal mismatch or temperature gradients. The materials that are used to construct the PBGA, as outlined in the earlier section on package construction, have thermal expansion coefficients that for the most part match that of the FR4/glass PCB to which they are typically mounted. The largest exception to this, for materials which are structurally significant to the package, is the silicon die. It has an expansion coefficient of 2.6 ppm/°C compared to 15 to 17 ppm/°C for other structural materials (see Table 2).

THERMAL CYCLING METHODOLOGY

Assembly-level accelerated thermal cycling is generally used to compare the performance of PBGAs relative to conventional leaded as well as other technologies. It is also used to detect any latent process defects that may be manifested in the first few cycles and to determine a wear-out (i.e., fatigue) failure distribution for the given device and environment. These test conditions are typically accelerated in cycle time as well as temperature extremes when compared to the actual application use environment. This is necessary since, by definition, an accelerated test is meant to decrease time to failure so that the failure characteristics and mechanisms may be known before the prohibitive amount of time it would take for something to fail in an actual application. Temperature extremes chosen could be the worst case expected application conditions or an expansion of that excursion to further accelerate the test. In either situation, the test will be accelerated because the cycle times chosen will probably be less than the application cycle time. A field cycle length depends on the particular application. For example, desktops personal computers are usually considered to cycle one or two times per day, while laptops cycle three to five or more cycles per day. A network server or high-end workstation may only cycle once every month on average to basically never.

The sample size in thermal cycling is generally much smaller than the ultimate population in the field. Therefore, accelerated reliability test results must be statistically analyzed and extrapolated to determine application cycles to fail a small percentage of the population. Also, these differences between cycle duration, form of excitation (i.e., internal device power versus ambient temperature swings) and temperature extremes between the accelerated test and the application field environment may need to be resolved before accurate predictions of field solder joint reliability can be made. These three differences result in a different failure distribution, namely the scale (time to 50% device failure) of that distribution, determined from accelerated testing than would be obtained by cycling to the actual application conditions. Everything involved with accounting for and resolving those differences is beyond the scope of this document, but some basic discussion to that end is included.

TESTING CONFIGURATION

Thermal cycling involves assembling PBGA devices using standard production processes to test boards that approximate the actual application board configuration in thickness, number of layers and pad geometry/layout. Some way of determining when a PBGA has failed must be used in order to gather failure data. The standard way is to use daisy-chain devices where adjacent pads are simply shorted on the PBGA substrate. Motorola has daisy-chain versions of all the PBGA designs that are currently available expressly for this purpose as well as for process studies. Traces directly connecting adjacent pads on the test board complete the chain such that there are one or more independent nets that go through all joints. An entire device can be covered with one net or several nets can be used to determine, for example, how rows fail relative to one another. Figure 10 provides an example of a routing scheme that was used on the 361 pin PBGA with 1.27 mm pitch and a 25 mm body. The rows on the device were divided into four sets: outer, middle, die perimeter, and inner.

The continuity of each net or device is measured either in-situ or every few (50 to 100 recommended) cycles to determine if it has failed. Monitoring in-situ is the preferred method and specialized equipment can be used to automate or simplify the monitoring process. Event detectors made by Anatech are especially made for monitoring solder joints, logging the data to a computer file and calculating the statistical failure parameters (discussed later) in real time. Data loggers with resistance capability may also be used.

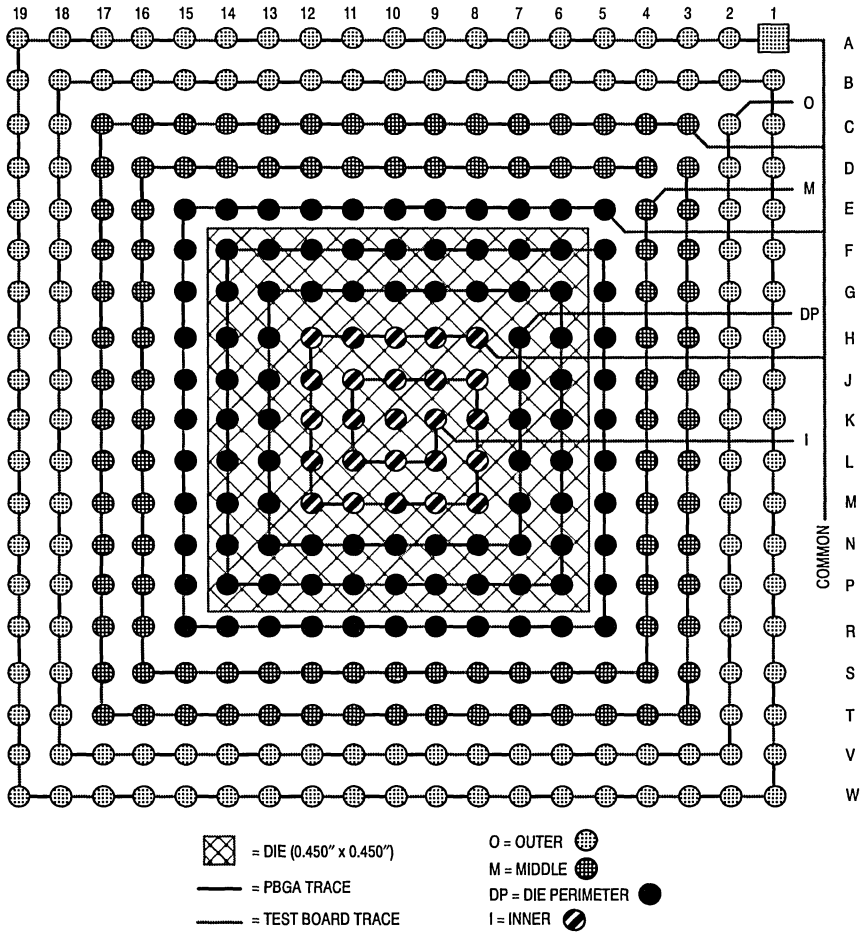


Figure 10. Example of an PBGA/Test Board Daisy-Chain Configuration to Allow Monitoring of Individual Groups of Rows (361 Pin, 19 x 19 Array, 1.27 mm Pitch, Device Bottom View)

Motorola uses two basic thermal cycle conditions. The most severe is a one hour – 40 to 125°C cycle that is mainly used to determine suitability to automotive under the hood applications. The other, more commonly used cycle is tyically 20 minutes in duration and goes from 0 to 100°C. The 20 minutes is made up of five minute ramps where possible and five minute dwell times at each temperature. The ramp time is limited by chamber heating and cooling capacity and sometimes has to be extended to allow the boards to reach the prescribed temperature. It is very important to know what temperature the boards and devices are actually experiencing as opposed to what was programmed or what the chamber air temperature is. This is accomplished through profiling the boards directly by placing thermocouples beneath several devices under which temperatures are expected to show differences. The air and board temperatures for a typical 0 to 100°C profile are shown in Figure 11. The ramp times for this profile had to be extended beyond five minutes to achieve the prescribed endpoint temperatures such that the total cycle time was 25 minutes. Examples of devices that would be expected to see the closest and furthest temperatures from the ambient air are the corner device on the board the most upstream of chamber airflow versus the middle device on the center board, respectively. To minimize these board to board thermal gradients, it is advisable to place boards parallel to the prevailing chamber air flow direction.

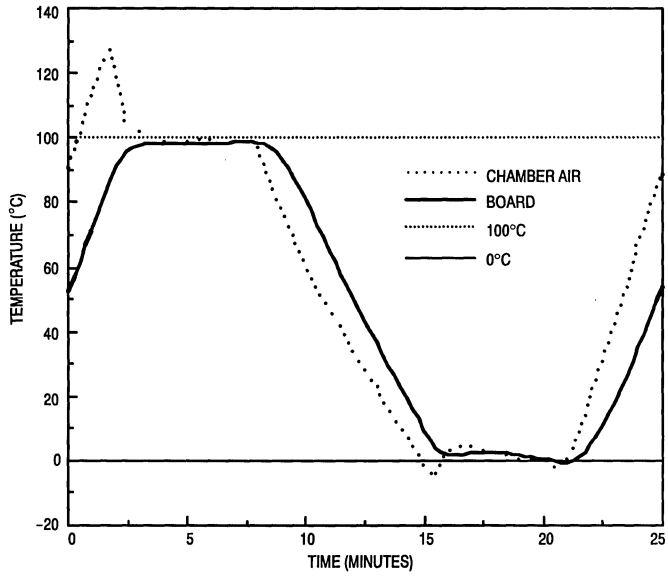


Figure 11. Typical 0 to 100°C Thermal Cycling Profile Showing the Difference Between Chamber Air Temperature and Temperature Seen by the Test Board

FAILURE DATA STATISTICAL ANALYSIS

After the thermal cycling has resulted in a substantial number of PBGA device failures (typically at least 50%, greater than 75% is preferred), the data can be fit to a statistical failure distribution. The two most commonly used for fatigue are the Weibull and the Log Normal distributions. The reliability function that describes failure in the Weibull distribution is as follows:

$$R(t) = e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad (1)$$

In the above equation R is the fraction of devices that have survived and α and β are called the scale and shape parameters, respectively. The scale parameter, α, corresponds to the time at which 63.2% of all devices fail. Time, t, is usually expressed in cycles.

After testing is complete the data consists of a number of data pairs that is equal to the number of devices that failed. Each pair will contain the failure number and the cycles to failure for that specific device. An example of some actual data for a 225 pin PBGA that was subjected to 30 minute thermal cycles from 0 to 100°C is presented in Table 4 on the next page. In this example the sample size was 28 and cycling continued until all devices failed (100% device failure or R = 0). Larger sample sizes such as these on the order of 30 or greater are recommended. The α and β are determined by doing a best fit curve of equation (1). Statistical software packages with Weibull capability can automate the process of determining α and β. One powerful tool to do this is WeibullSmith™ (written by Fulton's Findings) and another is the software that comes with the previously mentioned Anatech event detectors. The Anatech software presents the data in terms of cycles to 50% failure as opposed to 63.2% (α). For the case of the data in Table 4, $N_{50\%}$ was determined to be 7737, α was determined to be 7958 cycles and β, which is dimensionless, was 13.0.

The data can then be plotted on Weibull axes as it is in Figure 12. Note that also plotted on this graph is the 95% lower confidence limit of the data. It is also important to note that each set of data has a correlation coefficient or a measure of its goodness of fit to the particular failure distribution. In this case, the correlation coefficient (R^2 on the graph) was an adequate 0.965.

The Log Normal distribution is similar to the Normal distribution but it operates on the logarithm of the failure data. In other words, if the distribution of the log of the cycles to failure data is normal, the data is Log Normally distributed. The reliability function for the Log Normal distribution cannot be written in closed form and is closely approximated by the following:

$$R(t) = \frac{1}{2}\left\{1 - \text{erf}\left(\frac{\ln(t) - \ln(N_{50\%})}{\sqrt{2}\sigma}\right)\right\} \quad (2)$$

8

Table 4. Sample Failure Data for a 225 Pin, 27 mm Body PBGA Cycled from 0 to 100°C at Two Cycles per Hour (Starting Sample Size, n = 28).

Failure Number	Cycles to Failure (t)
1	6253
2	6438
3	6536
4	6869
5	7105
6	7148
7	7195
8	7246
9	7291
10	7361
11	7405
12	7430
13	7521
14	7698
15	7720
16	7807
17	7819
18	7886
19	7887
20	7945
21	7991
22	8163
23	8197
24	8272
25	8497
26	8772
27	8874
28	9143

Once again, t is expressed in cycles and erf refers to the (Gaussian) error function. The Log Normal scale and shape parameters, $N_{50\%}$ and σ, may be calculated as mentioned previously using a best fit procedure or preferably with a statistical software package. $N_{50\%}$ is simply the mean time to failure or the time at which 50% of the sample has failed. Since 100% of the samples have failed, the Log Normal parameters can be calculated directly as follows from the cycles to failure data, with n being the sample size (Log Normal standard deviation is actually calculated on the log of the cycles to failure data):

$$N_{50\%} = \frac{\Sigma t_i}{n} \quad (3)$$

and

$$\sigma = \sqrt{\frac{\Sigma (t_i - N_{50\%})^2}{n-1}} \quad (4)$$

Taking the same 225 pin PBGA failure data from Table 4 and fitting it to the Log Normal distribution reliability function gives an $N_{50\%}$ of 7628 cycles and a σ of 0.042. The cummulative failure 95% plot is represented in Figure 13 with the lower confidence interval shown once again. Note that for this data set the correlation coefficient (R^2) was 0.985 in the Log Normal distribution, which is better than was achieved with the Weibull distribution. Which failure distribution is used ultimately depends on how it fits the majority of the collected data as well as the availability of statistical software and familiarity with a particular distribution.

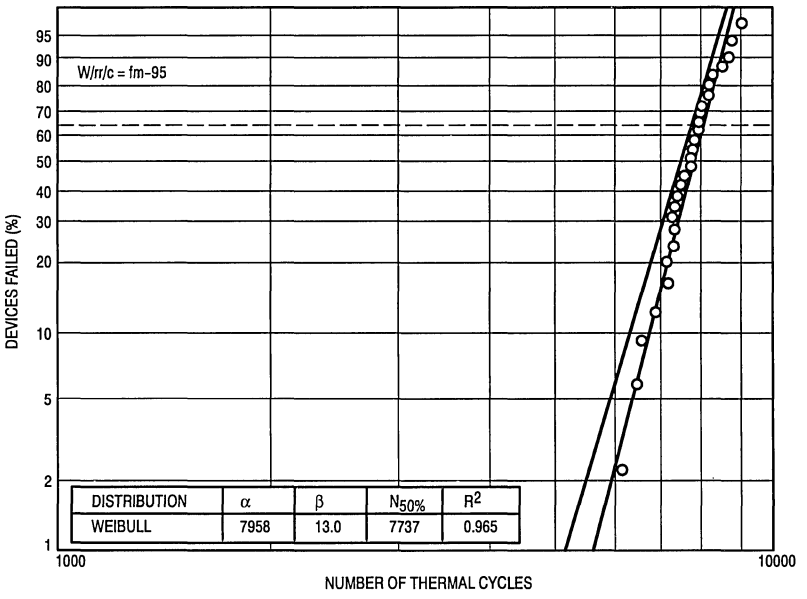


Figure 12. Weibull Failure Distribution of the Data in Table 4

8

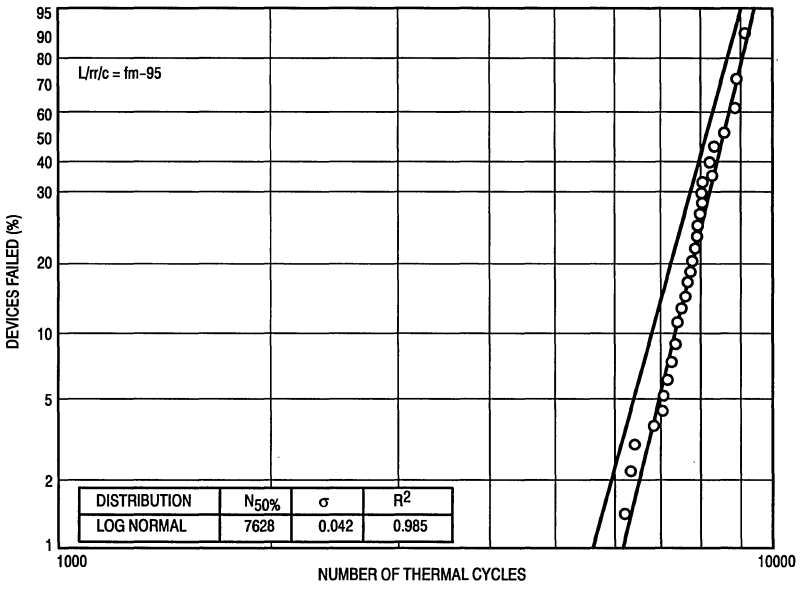


Figure 13. Log Normal Failure Distribution of the Data in Table 4

Extrapolation to Application Failure Data

As mentioned previously, PBGA accelerated reliability data and field failure data are usually different in three ways: 1) the sample size is much smaller in accelerated testing, 2) the cycle duration is greater in the actual application and 3) typical thermal excursions are usually less severe in the application. Additionally, the isothermal temperature excursions associated with thermal cycling are somewhat different than the thermal gradients found in the mounted PBGA in an actual application. The difference in the size of the population (sample size) can generally be accounted for by extrapolating data from the previously mentioned statistical distributions. Due to the highly nonlinear dependence of PBGA solder joint fatigue life on cycle time and severity, these differences generally cannot be accounted for as simply. Typically, nonlinear finite element models employing the viscoplastic temperature–dependent behavior of the solder as it undergoes creep and plastic deformation must be used. The finite element model is provided with accelerated testing and field temperature distributions for a cycle and the solder joint stress and inelastic strain or damage is determined. Crack growth and S–N correlations may then be used to determine the joint and subsequently the device life. The ratio formed by dividing the percentage of the population failing ($N_{xx\%}$) in the field (f) by the accelerated thermal cycling (ATC) testing cycles to failure is called the acceleration factor (AF):

$$AF = \frac{N_{xx\%,f}}{N_{xx\%,ATC}} \quad (5)$$

It has been proposed that a joint's, and therefore the entire package's, mean cycles to failure or $N_{50\%}$ follow a power law of the inelastic strain range seen by a joint during a thermal or application cycle (assuming inelastic strain is dominated by creep as opposed to plastic deformation):

$$N_{50\%} \propto (\Delta\varepsilon_{joint,inelastic})^n \quad (6)$$

The strain exponent (n) has been proposed by Solomon (see reference to Solomon in last section) to be approximately –2 for eutectic or near–eutectic solder. For long cycle dwell times, as would be found in typical field applications, this creep strain range is proportional to the cycle temperature range (ΔT). This temperature range raised to the strain exponent can then also be said to be proportional to the cycles to failure. For accelerated reliability testing, this is not the case unless the dwell times are sufficiently long to allow complete stress relaxation in the joint as stresses are converted to creep deformation. Substituting ΔT for $\Delta\varepsilon$ in equation (6) for both field and accelerated testing, substituting the resulting equations into equation (5) and simplifying results yields an equation of the form:

$$AF \approx \left(\frac{\Delta T_f}{\Delta T_{ATC}}\right)^{-2} \quad (7)$$

This equation has been further modified in an attempt to account for the field and ATC cyclic frequencies and maximum temperature seen during a cycle:

$$AF \approx \left(\frac{\Delta T_f}{\Delta T_{ATC}}\right)^{-1.9} \left(\frac{f_f}{f_{ATC}}\right)^{1/3} \exp\left(1414\left(\frac{1}{T_{max,f}} - \frac{1}{T_{max,ATC}}\right)\right) \quad (8)$$

Where: f, ATC = Subscripts to indicate field and accelerated thermal cycling testing.
$N_{xx\%}$ = Percentage of devices failed.
ΔT = Difference in minimum and maximum cyclic extremes (°C).
f = Cyclic frequency (Note: For purposes of the above equation, f_f minimum is 6 cycles per day).
T_{max} = Maximum during a cycle temperature (°K).

Once again, such an equation should be used as a very rough first–order estimate and could give very erroneous results, but it may be used for a lack of any other more in–depth analysis (such as nonlinear finite element modeling). It is also prudent to obtain an actual acceleration factor from two different testing conditions to verify the validity of equation 8 before its use in predicting field cycles to failure.

After the acceleration factor, scale parameter and shape parameter have been determined, test data may be extrapolated to determine cycles to failure for a much larger sample size such as a population in the field. The acceleration factor is multiplied by the percentage failed in accelerated thermal cycling to determine the percentage failed in the field as follows:

$$N_{xx\%,f} = AF \bullet N_{xx\%,ATC} \quad (9)$$

Then the time for any percentage to fail in the field can simply be calculated by substituting the desired reliability (i.e., fraction failed), the shape parameter and the field scale parameter and solving for time (in cycles) in either equations (1) or (2) above. It also has to be assumed that the field shape parameter (β or σ) is the same as that calculated from testing. This then assumes that the failure mode is the same in both the field and during accelerated testing since the shape parameter is also an indicator of failure mode. For the Weibull distribution, solving equation (1) for time yields:

$$t = \alpha \bullet \{-1n\,[R(t)]\}^{(1/\beta)} \quad (10)$$

It must be determined to what reliability cycles to failure are desired. It is commonly desirable to know the time at which 1,000 devices per million (ppm) would be predicted to fail. This 1,000 ppm corresponds to an R of 0.999 (R = 1 – 1,000/1,000,000=1 – fraction failed). Substituting this R as well as a previously calculated value of α ($N_{63.2\%}$) and known β into equation (10) yields a time to fail 1,000 ppm or $N_{0.1\%}$ of 4685 cycles. Since the Lognormal equation (2) cannot readily be solved for time due to its complexity, an iterative process (with the aid of a spreadsheet that has the erf function) can be performed to determine the $N_{0.1\%}$. Alternately, statistical software with Lognormal capabilities may be used. For this example it was determined to be 5659 cycles. This is slightly higher than what was predicted using the Weibull distribution. This is usually the case, as the Weibull distribution is a more conservative predictor than the Lognormal. However, the Lognormal traditionally results in a better correlation coefficient. The distribution that is used should be whatever the user is most comfortable and has the most experience or history using. Predictions to any given reliability can likewise be made from the two distributions. To illustrate this and to further compare the Weibull and Lognormal distributions, Table 5 shows a range of reliabilities calculated from using the data in Table 4.

It should be noted that to extrapolate the most conservative cycles to failure values for small percentages of a total population, data to a desired confidence interval should be used. In the two reliability plots above (Figures 12 and 13) this would mean using the lines forming the 90% confidence interval (or whatever confidence level was desired) as opposed the scale and shape parameters determined from the best fit of the data. It is only practical to consider the lower confidence limit since using the upper limit of the expected cycles to failure is not useful or prudent for field failure prediction. Table 6 compares the predicted cycles to failure from the best fit line versus those predicted using the upper and lower 95% confidence limits.

PBGA Thermal Cycling Data

Motorola has thermal cycled several configurations of 72, 119, 225, and 361 pin PBGAs while testing of other configurations is ongoing. Additionally, several other companies have thermal cycling testing either underway or completed. Two of those companies are AT&T and Compaq and their published data, along with a sampling of Motorola data are presented in Table 7. Also listed are Motorola data on two leaded devices, the 68 PLCC and the 208 PQFP, both with copper leadframes. The Motorola PBGA data shown shaded in Table 7 represents data that was used as example data for thermal cycling statistics in the previous section.

Table 5. 225 Pin PBGA Reliability Predictions Using the Weibull and Log Normal Distributions (0 to 100°C Thermal Cycling, 20 Minute Cycle)

Reliability (R)	Percentage Failed (%)	Devices Failed Per Million	Predicted Cycles to Failure Using:	
			Weibull	Log Normal
0.999999	0.0001	1	2758	4794
0.99999	0.001	10	3291	5035
0.9999	0.01	100	3926	5317
0.999	0.1	1000	4685	5659
0.99	1.0	10,000	5592	6098
0.9	10.0	100,000	6696	6739
0.84	16.0	160,000	6960	6925
0.5	50.0	500,000	7737	7628
0.368	63.2	632,121	7958	7878

Table 6. Reliability Predictions Using the Lower 95% Confidence Limits for the Weibull and Lognormal Distributions

	Predicted $N_{0.1\%}$ (in Cycles) Using:	
	Weibull	Log Normal
From Best Fit Line	4685	5659
95% Lower Confidence Limit	4121	5239

Table 7. PBGA Accelerated Thermal Cycling Data from Motorola and Others(with Comparisons to PQFP/PLCC)

Company	Device (Die in mils)	Cycle (°C)	$N_{0.1\%}$	$N_{1\%}$	$N_{50\%}$	α ($N_{63\%}$)	β	Source
Motorola	72 PBGA (270x270)	– 40 to 125, 1cph	1058	1363	2171	2260	9.1	Internal
Motorola	72 PBGA (270x270)	0 to 100, 3cph	3013	4034	6895	7222	7.9	Internal
Motorola	119 PBGA (280x437)	0 to 100, 2cph	4459	5848	9683	10113	8.4	Internal
Motorola	225 PBGA (400x400)	0 to 100, 2cph	4685	5592	7737	7958	13.0	Internal
Motorola	361 PBGA (450x450)	0 to 100, 2cph	6319	7804	11495	11886	10.9	Internal
Motorola	68 **PLCC**, Cu Leadframe	– 40 to 125, 1cph	904	1818	6561	7332	3.3	Internal
Motorola	208 **PQFP**, Cu Leadframe	– 40 to 125, 1cph	639	1553	7912	9111	2.6	Internal
AT&T	169 PBGA (364x359)	0 to 100, 2cph	2103	2741	4459	4651	8.7	Semi/HDP-10/93
AT&T	225 PBGA (389x398)	0 to 100, 2cph	1412	1993	3749	3960	6.7	Semi/HDP-10/93
Compaq	72 PBGA (270x270)	– 25 to 100, 2cph	1734	2194	3379	3508	9.8	1993 IEPS
Compaq	165 PBGA (437x437)	– 25 to 100, 2cph	1010	1309	2106	2195	8.9	1993 IEPS
Compaq	225 PBGA (389x398)	– 25 to 100, 2cph	1252	1664	2807	2937	8.1	1993 IEPS

Comparing the cycles to 50% failure for the PBGA and leaded devices reveals that the PQFP and PLCC tend to last longer. For example, $N_{50\%}$ for the 68 PLCC is a factor of three greater (6561 versus 2171 cycles) than the 72 PBGA for identical cycling conditions. But, it can be seen in Table 7 that the β's associated with leaded device data are significantly lower, on average, than those of the PBGA. This greater spread in the leaded device data can be attributed to a greater variation in the factors that influence solder joint reliability such as solder volume and device coplanarity. This β disparity means that there is a greater spread in the leaded data and when subsequent extrapolations are made down to $N_{0.1\%}$ or lower, they tend to become comparable to the same estimates for PBGA. Extrapolating $N_{0.1\%}$ for the 72 PBGA and 68 PLCC mentioned above, yields 1058 and 904 cycles, respectively. The same thing can be done when comparing the 225 PBGA to the 208 PQFP although the thermal cycle on the leaded device was the more severe – 40 to 125°C. The 208 PQFP had a higher α and $N_{50\%}$, but when $N_{0.1\%}$'s are compared there is a much different situation (4685 cycles PBGA versus 639 cycles PQFP).

Another observation from Motorola testing is that rows under and proximate to the die perimeter tend to fail first. This can be seen in Figure 14 which compares the outer, die perimeter, middle, and inner rows of the standard 361 pin PBGA. This gets back to the previously mentioned mismatch between silicon and the other PBGA and FR4 PCB materials. To further prove this point, tests on 72 pin packages without die went for many more cycles without failure than identical packages with die. Another conclusion drawn from Motorola testing is that there is a relative cycle basis acceleration factor of about 3.5 between 0 to 100°C and – 40 to 125°C PBGA testing. This actually results in no relative acceleration on a time basis since the more severe cycle is approximately three times longer than the 0 to 100°C cycle. Also observed from the testing was that underfill (although it causes the devices to be unreworkable) can give up to a 4X increase in cycles to failure and that increased device standoff (obtained through using larger diameter solder balls) improves the fatigue life as would be expected.

Failure Analysis

Analysis of devices that have failed in accelerated thermal cycling or in an application can provide extremely useful information with regard to determining the failure characteristics and mode. Generally, the failure analysis of PBGA devices consists of resistance probing to locate specific failed joints when possible, cross-sectioning and also die penetrant analysis of fractures. Probing of individual joints (actually joint pairs) usually only pertains to daisy-chain devices on test boards that have vias integral to each solder pad which drop down to the bottomside of the board and can be probed. Knowing the schematic of the daisy-chain net, specific via pairs can be probed until a failing pair with atypical or infinite resistance is found.

Care must be taken when preparing cross-sections of PBGAs with solder joint failures. Vibrations and flexure caused by the cutting of a failed device out of a test board, if not performed properly, can further propagate or initiate fractures. High speed diamond blades, abrasive wheels or routers are recommended over band saws. Once the device is removed, setting of the potting compound should optimally take place in a vacuum. Slower curing potting epoxies are also usually better than the quick setting variety to ensure that the PBGA is completely underfilled. After grinding, polishing and etching to reveal the solder structure, fractures

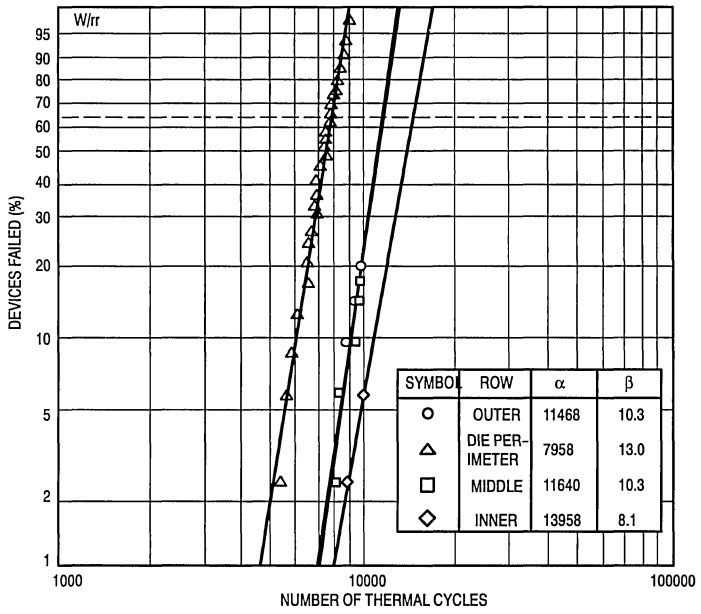


Figure 14. Weibull Failure Distribution by Device Row for a 361 Pin PBGA Cycled from 0 to 100°C at Two Cycles per Hour

can be readily observed. It should be noted that fracture length measurements taken from perpendicular PBGA cross-sections can be erroneous, depending on the row being sectioned, due to the fact that fractures generally propagate in a direction radially from the device center.

A very useful technique in analyzing devices with a multitude of fractured joints is dye penetrant analysis. Dye penetrant analysis can be used to visualize an overall distribution of fractures on all joints. For this procedure to work the best, the mounted device should be cleaned with a solvent prior to the application of a dye penetrant. This cleaning removes any flux residues, soldermask and other particles which are mobile during thermal cycling and may inhibit the flow of the dye into the fracture. There are many dyes available for the specific purpose of penetrating fractures (such as Ardrox Tracer-Tech), however, a machinist's layout dye made by ITW and called Dykem (Steel Red is typically the most visible) has shown excellent results at Motorola and elsewhere. After cleaning, a dropper is used to repeatedly flush the dye underneath the mounted device. The excess dye is then allowed to drain and the remainder is dried. This drying is accelerated by baking at 100°C for 10 to 30 minutes depending on the amount of dye under and around the device. Following removal from the bake oven and cooling, the PBGA is mechanically removed. It can be pried off with a screwdriver or similar, which may damage joints on the outer one or two rows, or the board repeatedly flexed until the device "pops" off. After removal, the board and device can be readily inspected. Fracture surfaces which are dyed were obviously present prior to device removal and presumably caused by the accelerated testing. An example with a fracture approximately one quarter of the way through the joint is presented in Figure 15.

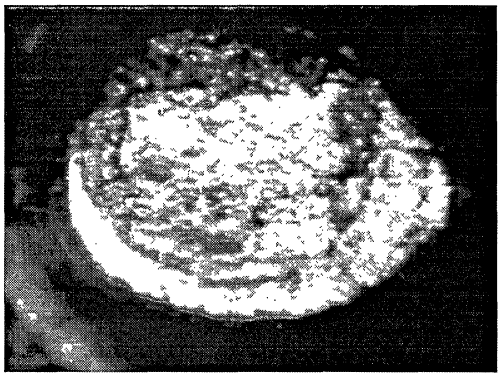


Figure 15. Micrograph of a Solder Joint Partial Fracture Surface Following Application of Dye Penetrant and Removal of a Thermal Cycled PBGA (Magnification of ≈ 50X)

MOISTURE AND POPCORNING

As with all plastic surface mount packages, the PBGA is currently susceptible to moisture induced delamination or popcorning if it is heated to reflow temperatures with excessive moisture content. The moisture weight percentage at which damage can occur is typically 0.15%. The PBGA is currently specified to meet Level 5 of the JEDEC classifications for moisture sensitivity in Test Method A112 (JESD22–A112). Level 5 in this test method, states that the PBGA will not exhibit delamination after exposure to 30°C/60%RH for 30 hours. The accompanying user handling requirements are a 24 hour out or drypack life. Any exposure over this 24 hours will require baking at 125°C for 24 hours. It is recommended, where possible, that this bake be performed in an inert atmosphere such as nitrogen to minimize potential solder ball oxidation.

The mode of moisture-induced failure in the PBGA package is delamination of the die attach from the die flag. This delamination, caused by the vaporization of the trapped moisture, is clearly visible in the form of a bubble in the BT substrate immediately under the die location. If the moisture content is high enough this delamination occurs violently (i.e., popcorning) and the delamination will propagate along the mold compound/BT interface until it is visible around the perimeter of the package. When this occurs, it is likely that an accompanying shorting of solder balls will occur in the area under the die. For this reason, it is advised to bake and dry pack even mechanical samples or daisy-chain devices prior to process assembly experiments.

RELIABILITY STRESS TESTS

The following summary briefly describes the various reliability tests included in the packaging reliability program. This program includes the PBGA.

SMT Preconditioning Stress

The purpose of this test is to simulate the shipping, storage, and solder attach steps involved in mounting and reworking a surface mount device. The preconditioning flow begins with ten temperature cycles at –65 to 150°C, dehydration bake at 125°C for 24 hours and is followed by a moisture soak. The moisture soak may involve simulating a worst case "no dry pack" condition in an 85°C/85% RH environment, a worst case dry pack condition of 85°C/60% RH, or a typical manufacturing environment condition of 30°C/60% RH. The duration of the moisture condition will vary depending on the moisture level tested. Moisture exposure is followed by two passes of infrared reflow (230°C) for 20 seconds per pass. Infrared reflow equipment is capable of heating the top side package body to 230°C with a ramp rate of 2–10°C per second.

Temperature Cycle

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of –65 to 150°C for a duration of 500 or 1000 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at a cold dwell system for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. the system employs a circulating air environment to assure rapid stabilization at the specified temperature.

Thermal Shock

The objective of this test is the same as that for temperature cycle testing: to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress because the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed to a minimum and maximum temperatures of –65 to 150°C for a duration 500 or 1000 cycles. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

Temperature Humidity Bias (THB)

This is an environmental test performed at a temperature of 85°C. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization. Typical stress duration is 1008 hours.

Autoclave

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 96 hours.

Results from a qualification of an 86 pin PBGA are included in Appendix D.

RELATED TECHNICAL ARTICLES AND PAPERS

This section provides only a partial listing of articles that have appeared in trade journals and have been published in conference proceedings that discuss issues related to PBGA. All articles are listed alphabetically by principal author/editor last name. Articles for which there is no copyright may be available informally through Motorola.

R. Boyd-Merritt, "Moto Fields New Package Technology", *Electronic Engineering Times*, March 1, 1993, p. 70.

T. Costlow, "Moto Pact Big for BGAs?", *Electronic Engineering Times*, August 2, 1993, p. 16.

R. Darveaux and K. Banjeri, "Fatigue Analysis of Flip Chip Assemblies Using Thermal Stress Simulations and a Coffin-Manson Relation", Proceedings of ECTC, 1991.

R. Darveaux and K. Banjeri, "Constitutive Relations for Tin Based Solder Joints," IEEE Trans on CHMT, Vol. 15, No. 6, December 1992, pp. 1013 – 1024.

R. Darveaux, "Crack Initiation and Growth in Surface Mount Solder Joints," Proceedings ISHM 25th International Symposium on Microelectronics, Dallas, TX, 1993.

M. Donlin, "Packaging Innovations Help Engineers Break Free from Design Constraints", *Computer Design*, June 1993, pp. 65 – 68.

B. Freyman and R. Pennisi, "Overmolded Plastic Pad Array Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics", Proceedings of the Technical Conference, 1991 ECTC, pp. 176 – 182.

A. Fukuda, Feature Article on BGAs (in Japanese), *Nikkei Electronics*, February 14, 1994, pp. 59 – 73.

D. Hattas, "BGAs Face Production Testing", *Advanced Packaging*, Summer 1993, pp. 44 – 46.

J. Houghten, "New Package Takes on QFP's", *Advanced Packaging*, Winter 1993, pp. 38 – 39.

R. Johnson, A. Mawer et al., "A Feasibility Study of Ball Grid Array Packaging", NEPCON East Proceedings, 1993, pp. 413 – 425.

R. Johnson and D. Cawthon, "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", NEPCON East Proceedings, 1993.

J. Lau et al., "No Clean Mass Reflow of Large Over Molded Plastic Pad Array Carriers (OMPAC)", 1993 IEEE/CHMT International Electronics Manufacturing Technology Symposium Proceedings, pp. 63 – 75.

D. Maliniak, "BGAs Make Transition to Memory Packages", *Electronic Design*, October 14, 1993, pp. 34 – 35.

H. Markstein, "Pad Array Improves Density", *Electronic Packaging & Production*, May 1992, pp. 25 – 26.

F. Martin, "C-5 Solder Sphere Robotic Placement Cell for Overmolded Pad Array Carrier", 1993 International Electronics Packaging (IEPS) Conference Proceedings, pp. 740 – 748.

A. Mawer, R. Darveaux and M. Petrucci, "Calculation of Thermal Cycling and Application Fatigue Life of the Plastic Ball Grid Array (BGA) Package", 1993 International Electronics Packaging (IEPS) Conference, 1993, pp. 718 – 730.

B. Miles and B. Freyman, "The Elimination of the Popcorn Phenomenon in Overmolded Plastic Pad Array Carriers (OMPAC)", 1992 International Electronics Packaging (IEPS) Conference Proceedings, pp. 605 – 614.

K. O'Brien, "Will BGA Live Up to Its Billing", *Surface Mount Technology*, August 1993, p. 40.

B. Nagaraj and M. Mahalingam, "OMPAC Package — Creep Analyses of C5 Solder Pads Using FEM Simulation," APDC Technical Report 15-92, 1992.

J. Shimizu, "Plastic Ball Grid Array Coplanarity", Proceedings of the 1993 Surface Mount International Conference, pp. 86 – 90.

H. Solomon, "Strain-Life Behavior in 60/40 Solder", GE Report #88CRD261, 1988.

C. Trigas, "The OMPAC Package — Assembly to Printed Circuit Board", Proceedings of the 1994 EuPAC Conference, Feb 1 – 3, 1994, Essen, Germany.

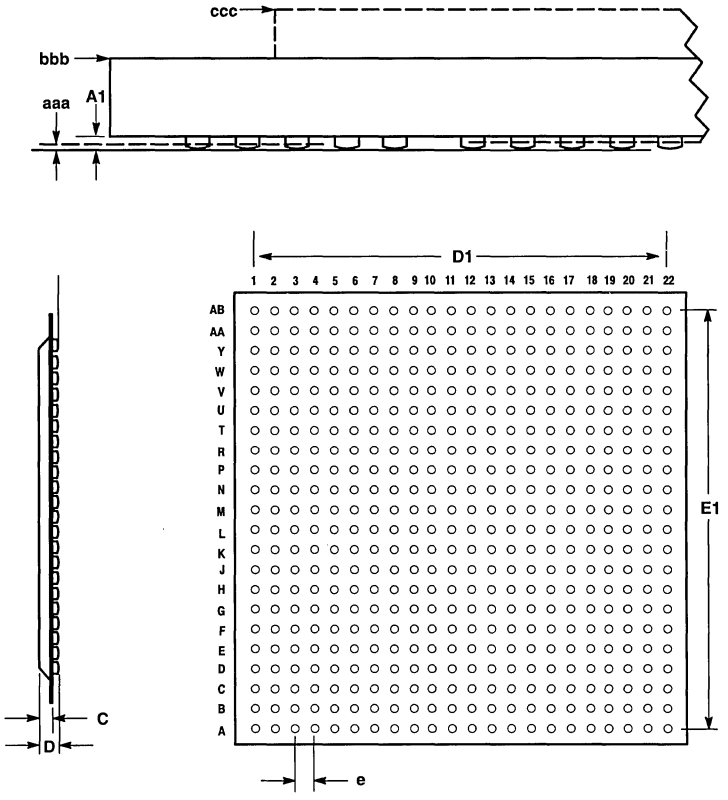
J. Tuck, "BGAs: A Trend in the Making", *Circuits Assembly*, December 1993, pp. 20 – 21.

J. Tuck, "BGAs: The Next Chapter", *Circuits Assembly*, August 1993, pp. 24 – 27.

J. Vardaman, "Ball Grid Array Packaging", TechSearch International, Inc. Consulting Report, January, 1993.

W. Yip and C. Tsai, "Electrical Performance of an Overmolded Pad Array Carrier (OMPAC), 1993 International Electronics Packaging (IEPS) Conference Proceedings, pp. 731 – 739.

APPENDIX A
JEDEC PLASTIC BALL GRID ARRAY FAMILY REGISTRATION



8

Reference Composite of 1.00, 1.27 and 1.50 Pitch Matrices

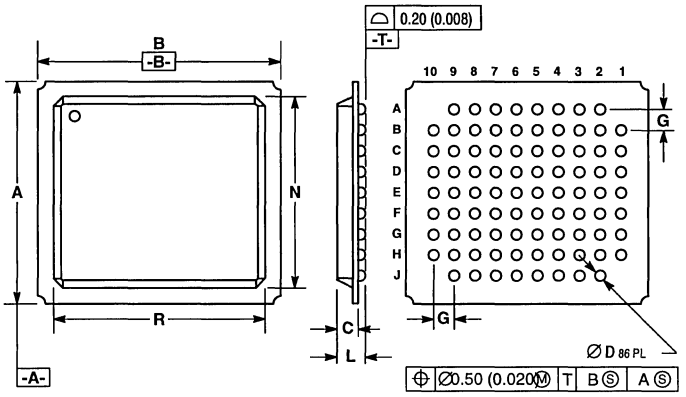
	e = 1.00			e = 1.27			e = 1.50		
		N			N			N	
D/E	M	Full Matrix	Stagger Matrix	M	Full Matrix	Stagger Matrix	M	Full Matrix	Stagger Matrix
7.00	6	36	—	5	25	—	4	16	—
9.00	8	64	—	7	49	—	6	36	—
11.00	10	100	—	8	64	—	7	49	—
13.00	12	144	—	10	100	—	8	64	—
15.00	14	196	—	11	121	—	10	100	—
17.00	16	256	—	13	169	—	11	121	—
19.00	18	324	—	15	225	—	12	144	—
21.00	20	400	—	16	256	—	14	196	—
23.00	22	484	242	18	324	—	15	225	—
25.00	24	576	288	19	361	—	16	256	—
27.00	26	676	338	21	441	221	18	324	—
29.00	28	784	392	22	484	242	19	361	—
31.00	30	900	450	24	576	288	20	400	—
33.00	32	1024	512	26	676	338	22	484	242
35.00	34	1156	578	27	729	365	23	529	265
37.50	37	1369	685	29	841	421	25	625	313
40.00	39	1521	761	31	961	481	26	676	338
42.50	42	1764	882	33	1089	545	28	784	392
45.00	44	1936	968	35	1225	613	30	900	450
47.50	47	2209	1105	37	1369	685	31	961	481
50.00	49	2401	1201	39	1521	761	33	1089	545

Solder Ball Dimensions and Package Coplanarity

	e = 1.00			e = 1.27			e = 1.50		
Dimension	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
aaa	—	—	.15	—	—	.15	—	—	.15
bbb	—	—	.25	—	—	.25	—	—	.25
ccc	—	—	.35	—	—	.35	—	—	.35
b	.50	.60	.70	.60	.75	.90	.60	.75	.90
A1	.40	.50	.60	.50	.60	.70	.50	.60	.70

APPENDIX B
PACKAGE MECHANICAL OUTLINES FOR THE 86, 119, 169, 225, and 357 PIN PBGA

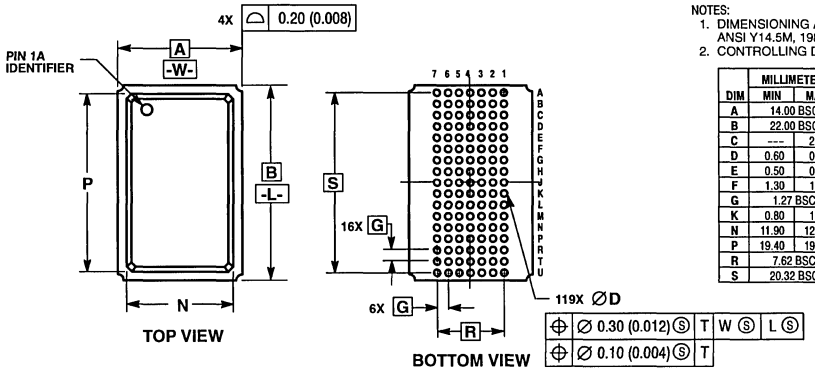
86 PIN PBGA
CASE 896A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

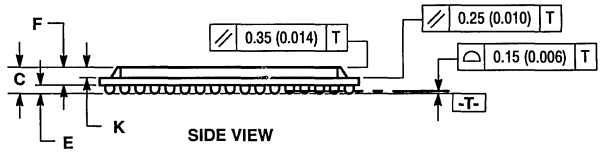
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

119 PIN PBGA
CASE 999-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	---	2.40	---	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	



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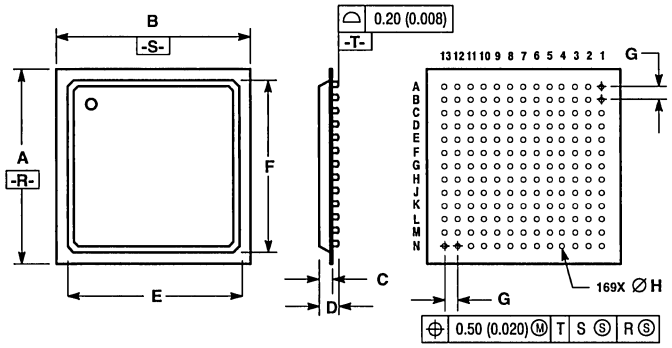
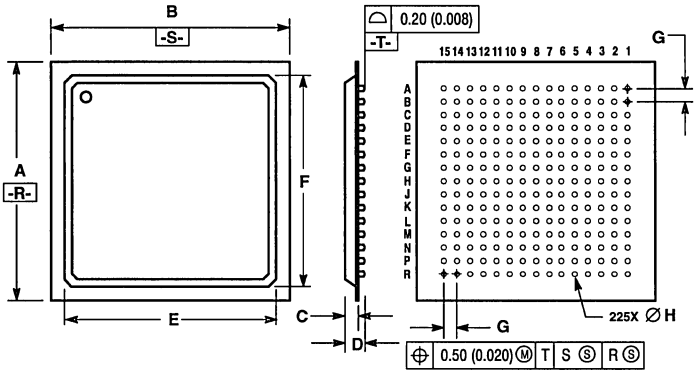
169 PIN PBGA
CASE 938-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.90	22.10	0.8622	0.8700
B	21.90	22.10	0.8622	0.8700
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	19.30	19.70	0.7598	0.7755
F	19.30	19.70	0.7598	0.7755
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318

225 PIN PBGA
CASE 938A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	26.90	27.10	1.0590	1.0669
B	26.90	27.10	1.0590	1.0669
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	23.80	24.20	0.9370	0.9527
F	23.80	24.20	0.9370	0.9527
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318

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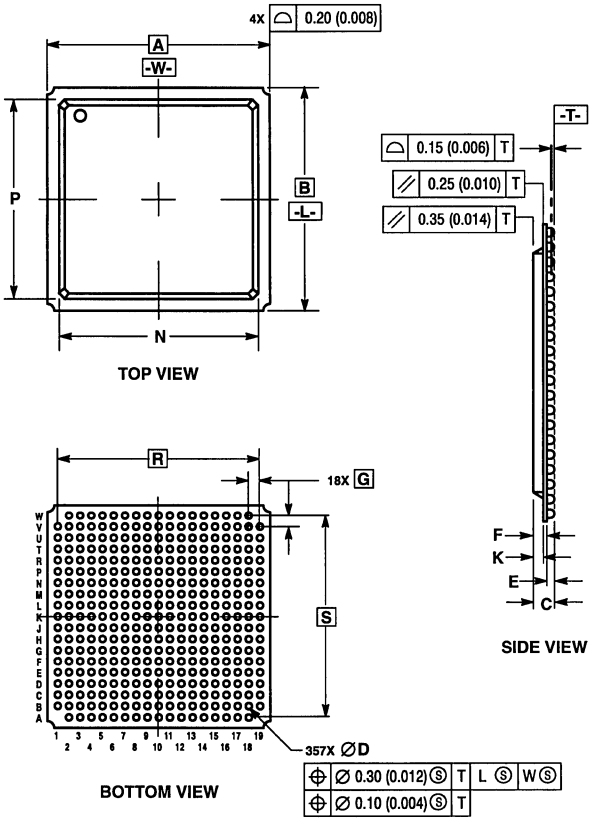
357 PIN PBGA
CASE 1103-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

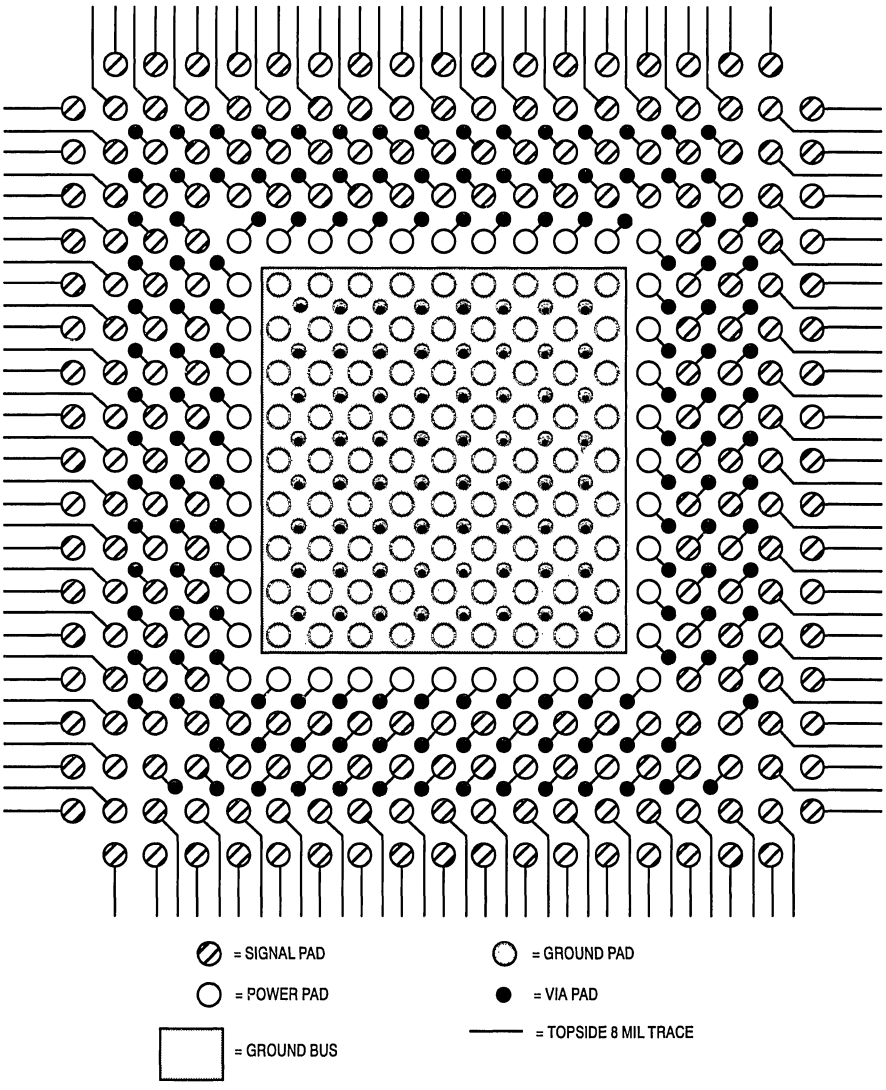
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	---	2.05	---	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

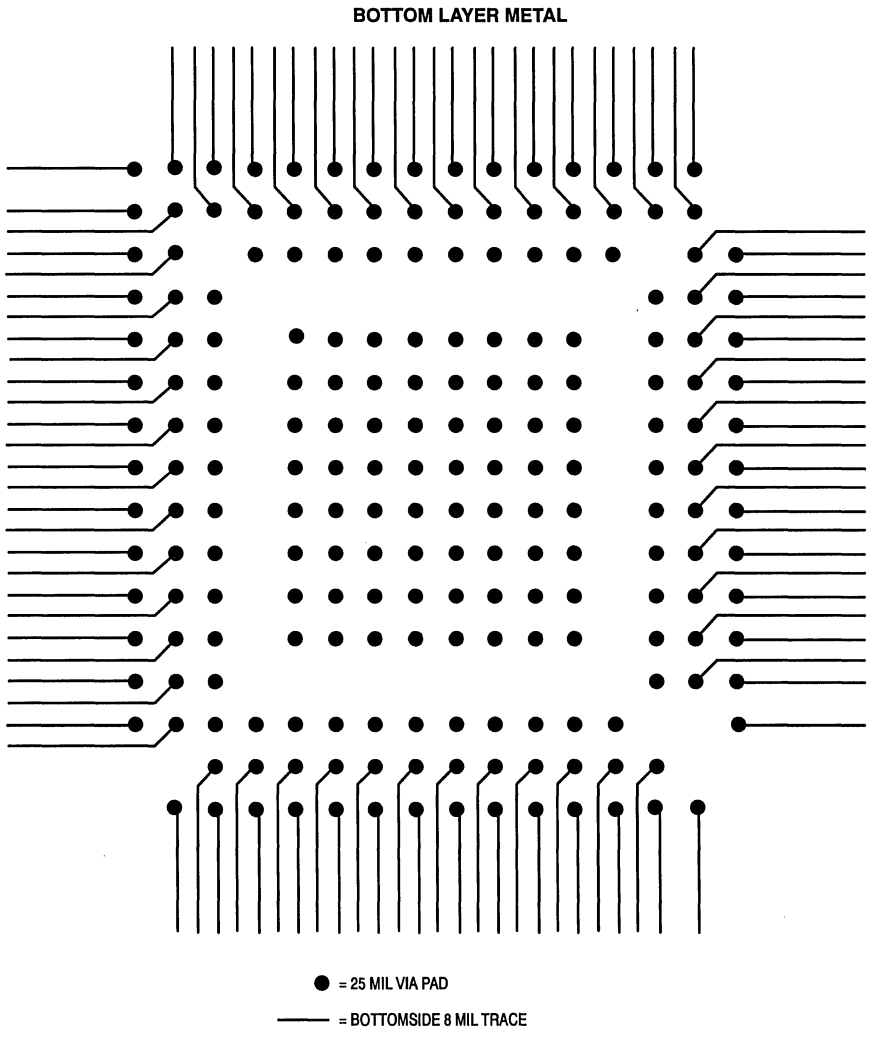
8

APPENDIX C

Example of escape routing for a 19x19 array, 1.27 mm pitch 357 pin PBGA with 23 mil diameter NSMD solder pads on a board with two signal, one power, and one ground plane.

TOP LAYER METAL




BOTTOM LAYER METAL
= 25 MIL VIA PAD
= BOTTOMSIDE 8 MIL TRACE

APPENDIX D

86 PIN PBGA PACKAGE QUALIFICATION SUMMARY SHEET

SOURCE DEVICE:	MCM62C416ZP21	TECHNOLOGY:	0.8 µ CMOS	FABRICATION:	MOS8
SOURCE DEVICE:	MCM56824ZP25	TECHNOLOGY:	0.8 µ CMOS	FABRICATION:	MOS8
		PACKAGE:	9X10 PBGA		
		LEAD COUNT:	86 BUMP	JOINT QUAL SPEC REV:	I

PURPOSE: QUALIFICATION OF 86 BUMP PBGA

PACKAGE RELIABILITY (Preconditioning Temperature Cycle (–65 to +150°C + bake (125°C, 24 hours) + (30°C, 60% RH 48 hours) + infrared reflow (230°C, 20 seconds, two passes)

Stress	Conditions	Results	Hours/Cycle	Next Readout	Pass/Fail
			Actual Data		
Preconditioning	As Above	0/225	2 Passes	Complete	P
Temperature Humidity Bias	85°C/85% RH/5 V	0/45	1008 Hours	Complete	P
Temperature Cycle	–65 to 150°C Air/Air	0/90	500 Cycles	Complete	P
Autoclave	121°C/100% RH 15 PSIG	0/90	96 Hours	Complete	P

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AN1232

Thermal Performance of Plastic Ball Grid Array (PBGA) Packages for Next Generation FSRAM Devices

Prepared by: Shailesh Mulgaonker (APDC, Phoenix, AZ) and Bennett Joiner (APDPL, Austin, TX)

ABSTRACT

Describing the thermal performance of Plastic Ball Grid Array (PBGA) packages by the traditional Theta JA obscures the performance characteristics of the package. When the package is designed with thermal vias and "thermal balls," the package is closely coupled thermally to the printed circuit board to which it is attached. The thermal performance of the package is dominated by the thermal performance, i.e. the temperature, of the printed circuit board. Since the thermal performance of the package is so closely coupled to the board, the thermal performance, $R_{\theta JA}$, should be expressed as a function of the temperature of the board. The thermal performance of the package is modeled as the junction to board and junction to case thermal resistances. Measured data is provided to validate the techniques. Measurements were taken on the 119 lead PBGA package on single component single and 4 layer printed circuit boards and on a simulated system daughter board with 8 or 16 packages in natural and forced convection environments.

INTRODUCTION

The use of wider bus structures for the static memories used for caches is driving the need for higher lead count packages for memory devices. Additionally, the faster clock and associated rise times highlight the need for multiple power and ground leads. As a result, the memory devices used for cache memories are being packaged into the higher lead count packages such as PLCC, QFP, and PBGA packages. For the range of devices that are being considered here, the PLCC package is physically too large to be acceptable. Hence, the packages of choice are the QFP and the PBGA.

The thermal performance of a 100 lead 14 x 14 mm plastic QFP package is compared to a 119 lead 14 x 22 mm PBGA package in Figure 1. Theta JA, $R_{\theta JA}$, is measured using the procedures of SEMI[1] G38–87 using a single layer printed circuit board (76 x 114 mm) as specified in SEMI G42–88 at natural convection. Normally this value is supplemented by the thermal resistance measurements over a range of forced convection. For illustration of the differences between the two parts consider the bar chart in Figure 1 of the thermal resistance at natural convection for the parts mounted on the standard single layer printed circuit board and parts mounted on a four layer printed circuit board which is included as an extension of the SEMI specification. While the two packages have very similar thermal performance as measured on the standard single layer printed circuit board, there is a substantial difference in the performance on the four layer boards. The higher thermal conductivity of the four layer board with two solid 1 oz. planes causes more of the board to act as a heat sink. The effect is enhanced for the PBGA packages because there is metal conduction path from the die pad to the ground plane of the printed circuit board. This path has much lower thermal resistance than the equivalent path for the QFP. Hence, the PBGA package is much more closely coupled to the printed circuit board and is more sensitive to its temperature and to power dissipation in other components on the board.[2,3]

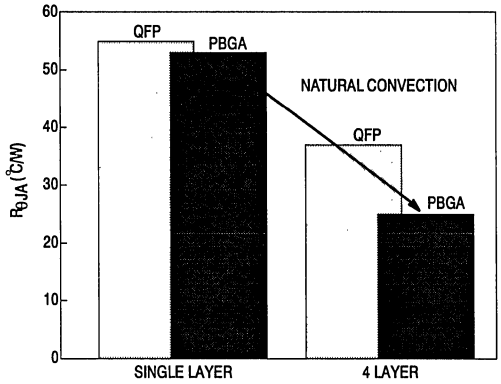

Figure 1. Type of Board on which Package is Mounted

The specific package being considered here is a 119 lead 14 x 22 mm PBGA package which is sketched in Figure 2. The thermal test vehicle packages tested for this characterization activity used a thermal die size of 4.37 x 7.32 mm (172 x 288 mil) mounted on a 7.5 x 11.1 mm die pad. There are 32 vias from the die paddle to the array of 21 thermal balls. The thermal balls are soldered to an array of pads that are connected to the ground plane in the printed circuit board with 32 vias. The planes in the circuit board are solid 1 oz. copper. Allowing the planes to be solid makes simulation easier and reflects the performance of the application boards which will have more than one ground plane.

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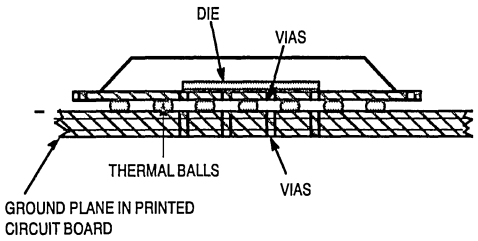

Figure 2.

This paper will address the following questions:
(1) How useful is $R_{\theta JA}$?
(2) Can the customer use the $R_{\theta JA}$ measured on a four layer-board to estimate performance on his multilayer board?
(3) How should the performance of the package be modeled?

Simplified Thermal Models for the PBGA

The heat flow in any package is actually a complicated three dimensional flow in which the path that the heat flow takes is dependent on how each of the surfaces of the package are cooled or heated by adjacent components. There are several approaches to deal with this difficulty including full finite element or finite difference models or the junction to case thermal resistance model of Bar–Cohen.[4] This paper will argue that the additional simplification of the multiple internal resistance models to only the two major thermal paths is valid based on measurement data that fits such a model. The proposed thermal model for a single component on a board is shown in Figure 3.

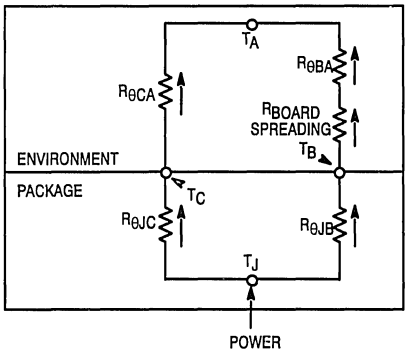

Figure 3.

In this model, the package is modeled as a junction to board thermal resistance, $R_{\theta JB}$, and a junction to case (top of package), $R_{\theta JC}$. These are the two major thermal paths from the package. The heat loss from the package to the environment is represented by the case to ambient thermal resistance, $R_{\theta CA}$; heat loss from the board is represented by a spreading resistance within the board and the board to ambient thermal resistance. For this model, the junction to ambient thermal resistance, $R_{\theta JA}$, can be calculated by series and parallel combinations of the resistance values of the model:

$$\frac{1}{R_{\theta JA}} = \frac{1}{R_{\theta JC} + R_{\theta CA}} + \frac{1}{R_{\theta JB} + R_{BS} + R_{BA}}$$

In most cases, there is not a clear separation between the spreading resistance in the board and the board to ambient thermal resistance. Usually, this equation will just be written in terms of an effective board to ambient thermal resistance.

$$\frac{1}{R_{\theta JA}} = \frac{1}{R_{\theta JC} + R_{\theta CA}} + \frac{1}{R_{\theta JB} + R_{BA}}$$

This analysis works for the single component on the board. If there are other heat sources on the board, the board temperature is not a function of only this one package. For the more general case, the effect of the other components can be represented as the temperature difference, T_{BA}, between the board and the ambient. This term, T_{BA}, is normally referred to as the board temperature rise above ambient. With this addition, the model of the package and board becomes:

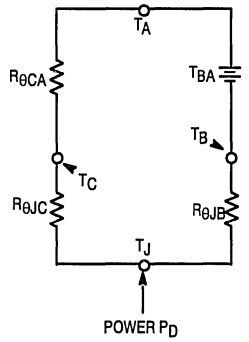

Figure 4.

This model is a simplified version of the model used by Andrews[4] with the junction to header thermal resistance neglected. If one uses this model to solve for the junction to ambient thermal resistance in terms of the thermal resistance values, board to ambient temperature rise, T_{BA}, and power P_d, then the following linear relationship is obtained:

$$R_{\theta JA} = \frac{(R_{\theta JC} + R_{\theta CA})\,R_{\theta JB}}{(R_{\theta JC} + R_{\theta CA}) + R_{\theta JB}} + \frac{(R_{\theta JC} + R_{\theta CA})}{(R_{\theta JC} + R_{\theta CA}) + R_{\theta JB}} \bullet \frac{T_{BA}}{P_D}$$

$$R_{\theta JA} = R_{\theta JA0} + S \bullet \frac{T_{BA}}{P_D}$$

This model predicts that the junction to ambient thermal resistance will be a linear function of the board temperature rise above ambient divided by the power dissipated in the component. The usefulness of the model can be verified by measuring the component thermal performance as function of the board temperature. Experimentally, this is easily accomplished using a silicone rubber heating pad under the printed circuit board. The results are shown in Figure 5.

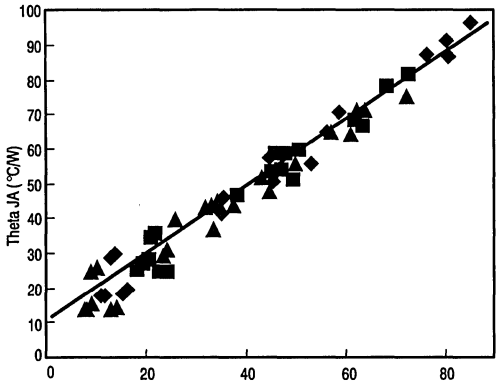

Figure 5. Board Temperature Rise Above Ambient Divided by Package Power

Measurements taken at natural convection, 1 m/s, and 2 m/sec forced convection are shown on the graph with all the data fitted to a single straight line. As predicted by our model, the thermal performance of this package is linearly dependent on the board temperature rise above ambient (divided by package power dissipation). The two resistor model of Figure 4 provides a good description of the thermal performance of the package. When an engineer is first introduced to this concept, one of the first questions is "why is the thermal performance the same at natural convection as at 2 m/s forced convection?" Actually, Theta JA is significantly different between natural convection and 2 m/s because the board temperature is significantly different. What is shown in the Figure 5 is that the junction temperature will be nearly the same at natural convection and at 2 m/s if the board temperature is the same. This would only happen if the power dissipation of the other components on the board forced the additional temperature rise in the board.

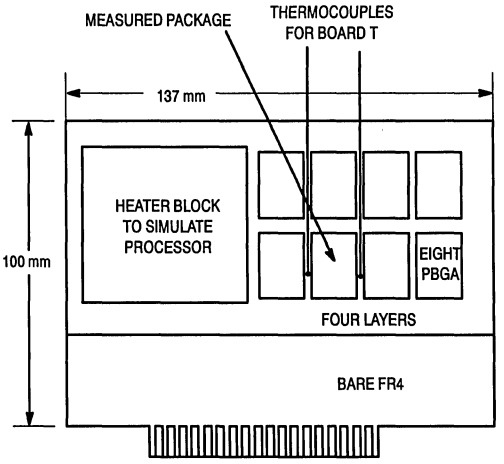

Figure 6.

This data shown above was taken with a single component on the board. The obvious question is: How well this model works in a system application? To answer this question, a simulated system daughter card was designed with an aluminum block with cartridge heaters to simulate a large microprocessor and with provisions for mounting either 8 or 16 PBGA packages. The board has an area of 69 x 137 mm that has four layers with two solid 1 oz planes. Two solid 1 oz. planes are approximately thermally equivalent to a board that would actually be used with perhaps 8 to 12 layers. The layout of the board is shown in Figure 6 with an array of 8 PBGA on one side of the board. The other 8 packages are mounted on the bottom of the board directly under the other ones. The package indicated by the arrow is the one for which data is reported; a package in the "middle" of the array of devices was chosen because it would be representative of a typical package in middle of such an array. Junction temperatures were also measured for the other three devices in that row. The board temperature is measured with a thermocouple on each side of the package soldered into plated through holes which are connected to the ground plane. The thermal balls of the PBGA are connected to the one ground plane.

Results obtained from this board at natural convection, 0.5, 1, and 2 m/s with either 8 PBGA or 16 PBGA packages on the board powered at 1 or 2 watts each are combined with the earlier data taken on single and 4 layer boards and shown in Figure 7.

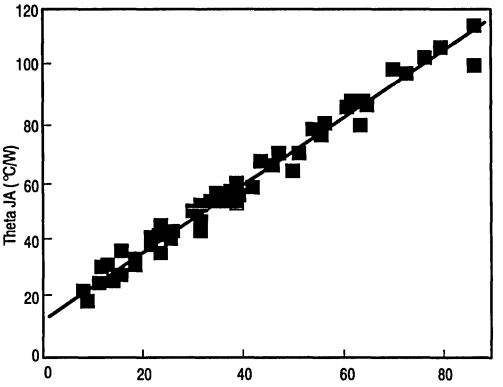

Figure 7. Board Temperature Rise Above Ambient Divided by Package Power

Again, the measured data on a wide variety of environmental conditions fit the linear relationship predicted by the two resistor model. As an example, suppose there is one watt being dissipated in the PBGA package and the board temperature has risen to 30°C above ambient. Then, one could determine from the graph that the Theta JA of the package in that environment would be 40°C/watt. As another example, suppose that the package was dissipating 2 watts and that the board temperature was 60°C above the ambient temperature. Then the board temperature rise divided by the package power would be 30 and the Theta JA would also be 40°C/watt. For an ambient temperature of 25°C, this would result in junction temperatures of 65°C and 105°C for the one and two watt examples, respectively. From this

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discussion, it is evident that good thermal performance will require thermal management of the printed circuit board temperature.

While, the measured Theta JA can be plotted on the same curve for both natural convection and forced convection, a purist would point out that the percentage of heat lost between convection to the air from the package and conducted to the board will change with forced convection. In fact, if the data at natural convection and 1 m/s are separately fitted to a straight line, there will be small differences in the slope and intercept. As an example, the curve fits determined from the results with single component board are given in the following table:

	Intercept	Slope
Natural Convection	9.8	0.997
1 m/s	10.7	0.971
2 m/s	10.7	0.954

As the forced convection increases or a heat sink is placed on the package, a lower percentage of the heat is dissipated to the printed circuit board, and the junction temperature is slightly less coupled to the board temperature. For the typical range of forced convection used in desktop computers, reasonable accuracy for this package is achieved using the simplified expressions combining the results for the various conditions into a single relationship.

A more traditional way to examine the data is to use a table of Theta JA determined by a variety of techniques:

	Theta JA (°C/watt)	
Board Type	Natural Convection	1 m/s Forced Convection
Single Layer Board	52	41
4 Layer Board	24	19
8 Parts at 1 watt (System Board)	56 to 62	46 to 49
8 Parts at 2 watts (System Board)		45 to 49
16 Parts at 1 watt (System Board)	104	84

The junction temperature depends on the environment which includes the conductivity of the board and the power dissipation of surrounding components. The single component on a multilayer board represents one extreme with the other extreme represented by packages mounted closely together on both sides of the board.

The values obtained from the single component on a multilayer board would predict a lower value of the junction temperatures for most applications than would be observed in the typical case with substantial power dissipation in other devices on the board.

The doubling of the observed Theta JA when the packages are mounted on both sides of the board compared to the single sided mounting is a graphic example of the effect of the power density on the board and the resulting board temperature on the junction temperature. Mounting the packages on both sides of the board effectively halves the area available for power dissipation for each package. Incidentally, packages on the bottom of the board had very similar junction temperatures to the packages on top of the board. In natural convection at 1 watt, the package on the top of the board had a junction temperature of 121°C and the bottom package had a junction temperature of 120°C. For all practical purposes, those are identical values. This is explained by the close coupling of the junction temperatures to the board temperature which will be the same for the two packages mounted on opposite sides of the board.

The traditional Theta JA is useful for comparing package performance and as a preliminary estimate to determine whether further analysis is needed. It gives no information to account for the range of thermal performance given as examples in the table above.

The other frequently asked question about this formalism is: How is the board temperature determined? The effective doubling of the Theta JA when the packages are mounted on opposite sides of the board clearly indicates that historical board temperatures could be wrong. The answer to the determination of the board temperature is that a full board level thermal simulation will be required to determine both the thermal performance of the printed circuit board and the performance of each of the packages. There are a number of commercial software codes[6–8] that perform a board level thermal solution with varying degrees of sophistication. These range in sophistication from the 2 1/2 dimensional finite difference or finite element codes to the computational fluid dynamics codes that simultaneously solve the conduction and the fluid flow convection. For all these simulation codes, a simplified thermal model for the package is required. From a component manufacturer's viewpoint, a simple, general purpose model which could be broadly applied would be most helpful. It is our contention that the reduction of the measured data to a single straight line as predicted by the model demonstrates that the two resistor model meets the need for a reasonably accurate description of thermal performance. A proposed method for obtaining that model will be described in the following section.

CONDUCTION MEASUREMENTS TO DETERMINE PACKAGE MODELS

Having determined that the two resistor model will adequately describe the thermal performance, a method for obtaining the values in those models will be discussed. One of the basic premises is that the package model should describe the package behavior. As an example, the package model should not provide a case to ambient thermal resistance because it is not a package characteristic. The case to ambient thermal resistance is a function of whether natural convection can occur in a closed environment, degree of turbulence in forced convection, whether a heat sink is used, etc. Instead, the package model will provide a junction to case thermal resistance. The next level modeling tool can work from that junction to case thermal resistance to determine the total thermal resistance through the top of the case whether a heat sink is used or normal convection environments.

Unfortunately, there are several junction to case formalisms in use. The most confusing is the junction to all surfaces of the case thermal resistance as determined by the junction to a liquid bath measurement which is described in SEMI specification G43–87. One of the board level modeling tools uses this value coupled with the lead resistance as the junction to board measurement. Our position is that this definition is not extensible to the ceramic packages or thermally

enhanced packages on which a heat sink is likely to be used. Instead, the definition taken from the JEDEC[9] committee is used: The junction to case thermal resistance of a package is defined to be "the thermal resistance from the operating portion of a semiconductor device to outside surface of the package (case) closest to the chip mounting area when that same surface is properly heat sunk so as to minimize temperature variation across that surface." Hence, the junction to case thermal resistance is the thermal resistance of the path from the junction to the surface on which a heat sink might be placed. As a result, the junction to case thermal resistance is the thermal resistance from the junction to the top surface of the PBGA. It is determined using a cold plate (infinite heat sink) to force "all" the heat to travel from the junction to the case of the package. The methods for making this measurement are described in the industry specifications: MIL–STD 883D, Method 1012.1 and SEMI G30–88. We deviate from the industry specifications in that the temperature of the cold plate is used instead of the case temperature. All of the techniques to put a thermocouple on the surface of the case using holes or slots in the cold plate or in the case itself will yield a warmer measurement and hence a more optimistic measure of the thermal resistance. Using the cold plate temperature as the "case" temperature creates a slightly conservative result.

A method for determining a junction to board thermal resistance is not defined in the industry. Of the suggestions that have been proposed, the most direct and simple method is the following: The package is soldered to a multilayer printed circuit board with solid power and ground planes to achieve a high thermal conductivity in the x–y plane. The higher thermal conductivity improves the accuracy of the measurement by minimizing the temperature gradients in the vicinity of the package while it is being tested. Any "thermal balls" are connected with vias to the ground plane within the printed circuit board. The printed circuit board is needed for the measurement to provide an easy method to make the necessary electrical connections to the package for the test. The component and printed circuit board are placed on the cold plate as shown in Figure 8 using thermal grease to minimize the thermal resistance between the board and the cold plate.

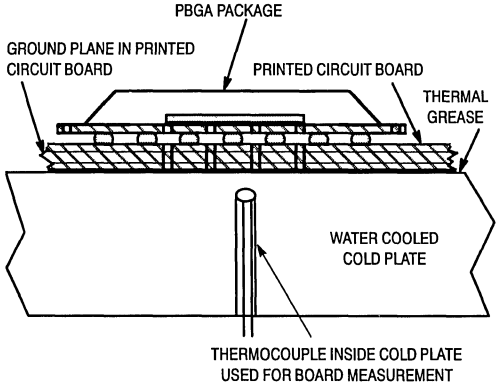

Figure 8.

The junction to board thermal resistance, $R_{\theta JB}$, is then determined by

$$R_{\theta JB} = \frac{(T_J - T_B)}{P}$$

where T_J and T_B are the junction and board temperatures respectively, and P is the power dissipated in the package. Again, a more consistent measurement is obtained by using the cold plate temperature as the board temperature.

The usefulness of the technique can be judged by comparing the junction to board thermal resistance results obtained by the slope and intercept of that data fitted to the two resistor model to the junction to board thermal resistance determined by the cold plate technique. For the two resistor model, the junction to board thermal resistance is determined from the data obtained by the straight line fitted to the data in Figure 7 by the relationship:

$$R_{\theta JB} = \frac{R_{\theta JA0}}{S}$$

To make the judgment easier, the results were compared for the 119 lead 14 x 22 mm, 225 lead 27 x 27mm, and the 357 lead 25 x 25 mm PBGA. The following table gives the junction to board thermal resistance as determined by the two methods for the three different PBGA packages:

Package	Two ResistorModel	Cold Plate
119 Lead	9.8	10.8
225 Lead	8.3	7.4
357 Lead	6.6	7.3

As can be seen, the two methods give a result that is within 1°C/watt. Hence, the choice of techniques should be determined by ease of use except for those cases where testing under the actual heat flow paths is necessary. Testing using actual application environments is appropriate for cases at the conditions of extreme power dissipation or unusual heat sink and convection configurations.

The cold plate method for determining the junction to board thermal resistance is quicker and easier since it is a relatively quick single point measurement instead of requiring some 4 to 8 wind tunnel measurements per sample tested. If it was necessary to test all parts using the two resistor model in the wind tunnel, more wind tunnels would be required within Motorola to meet the package test needs. More importantly, the cold plate technique represents a relatively easy environment to duplicate in simulation to verify the accuracy of simplified models being used in board level simulations. It is also a much easier test environment to explain to a customer.

CONCLUSION

Theta JA determined by the traditional methods provides a comparison of the thermal performance of a package. To be useful to calculate junction temperature, it must be referenced to the board temperature on which the package is mounted. Especially with the PBGA packages, the thermal performance is largely determined by the board temperature to which the package is mounted.

The two resistor thermal model is a simplification of the actual thermal performance of the package, but has been shown to provide an adequate description of the performance of the package over a wide range of environments. The components of the two resistor model can be measured or simulated using the cold plate environment to force essentially all of the heat flow along the path being measured. We are proposing that this two resistor model be made available to designers for use in board level modeling tools for their determination of the board temperatures, Theta JA, and junction temperatures in their application environment.

ACKNOWLEDGEMENTS

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7. Pacific Numerix, Scottsdale, AZ.
8. FLOTHERM, Flomerics, Westborough, MA.
9. JEDEC JC15.1 committee is currently writing specification for thermal characterization of surface mount integrated circuits.

AN1243

Output Loading Effects on Fast Static RAMs

Prepared by: Allan Klaus

INTRODUCTION

This review describes the ac loading used for testing. Component test engineers should pay careful attention to the test conditions and derating curves for deviations from the specified load. This information is also applicable for system engineers calculating required device speed for a given environment. This information will help the user make the appropriate choice of device performance for their needs.

As device access times decrease, so do output transition times. With faster rise and fall times come additional problems associated with output and signal path impedances. In any system running at frequencies where the propagation delay of a signal path (t_{pd}) is greater than 1/2 of the total signal transition time, transmission line effects will be seen on the signal. This results in overshoot and undershoot at the load end of a conductor, which can cause problems in testing, or in actual use of the device. This discussion gives a brief overview of the factors contributing to these effects, and the measures that can be used to predict or eliminate them. For a detailed discussion of both PC board layout considerations and applicable transmission line theory, consult the *MECL System Design Handbook*, publication HB205/D, Motorola, Inc., 1983.

DEFINITION OF TERMS

t_{pd} — Propagation delay in seconds
L_0 — Inductance in henries/meter
C_0 — Capacitance in farads/meter
R_L — Load resistance in ohms
$R_{DS(on)}$ — Resistance from drain to source of a FET device when on
R_O — Output resistance in ohms. For CMOS devices, this is the $R_{DS(on)}$ resistance of the output devices.
R_{OH} — Output resistance for a high, or 1, signal from the device
R_{OL} — Output resistance for a low, or 0, signal from the device
ρ_L — Reflection coefficient of the load end of a signal
ρ_S — Reflection coefficient of the source end of a signal, the device output
V_L — Termination voltage of the load resistor in a transmission line termination network

TRANSMISSION LINE OVERVIEW

What is a transmission line and how does it affect output waveforms? In simple terms, a transmission line is a signal path that exhibits a characteristic impedance. The type of lines discussed in this paper are primarily microstrip (Figure 1) and stripline signal paths (Figure 2) found in most PC boards today. The inductance and capacitance of these lines are a function of the line thickness and width in combination with the dielectric properties of the PC board material and the distance of the line from the ground plane. The impedance of the line is determined by these characteristics and the additional distributed capacitance from other devices on the line.

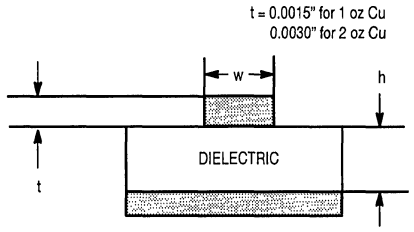

Figure 1. Microstrip Signal Path

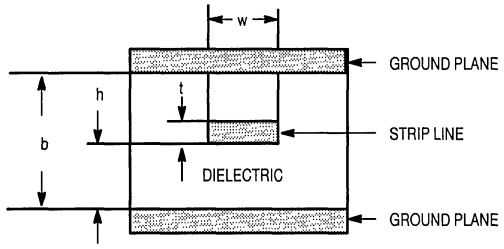

Figure 2. Stripline Signal Path

The characteristic impedance of a microstrip or stripline path is given by the formula $Z_0 = \sqrt{L_0 / C_0}$. The propagation delay of the path, t_{pd}, is $t_{pd} = \sqrt{L_0 / C_0}$ x length = Z_0 C_0 x length. For example, the propagation delay of a microstrip line on G10 epoxy/glass material is approximately 1.76 ns/ft, while the delay for a stripline is about 2.27 ns/ft.

The effect of a transmission line on a device output depends on the electrical length of the line. In all cases, a signal traveling down the line will be affected at the end of the line if it is not terminated with a resistor of the characteristic impedance of the line. The amount of effect is determined by the reflection coefficient of the load, ρ_L, where:

$$\rho_L = \left(\frac{R_L - Z_0}{R_L + Z_0}\right) \quad (1)$$

This reflection occurs at a time t_{pd} after a change at the source of the signal. A similar reflection occurs at $2t_{pd}$ after this new signal has returned from the load to the source, and is determined by the source reflection coefficient, ρ_S, where:

$$\rho_S = \left(\frac{R_O - Z_0}{R_O + Z_0}\right) \quad (2)$$

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R_O is the output resistance of the device. In the case of an electrical line length with t_{pd} less than 1/2 of the rise/fall time of the output signal, the transmission line effects are seen as a delay of the signal transition times. This is caused by the load reflection returning to the source during the actual signal transition and being included in the duration of the signal. For the case of an electrical length with t_{pd} greater than 1/2 of the rise/fall time of the output signal, the reflection effects may be seen directly. In severe cases, signal overshoot or undershoot can cause an invalid level to be seen at the load end at $3t_{pd}$.

The formulas for determining reflection coefficients require knowledge of the output impedance of the device, the characteristic impedance of the signal path, and the termination resistance. The goal of termination is to guarantee that the output signal at the receiving end (load) has enough margin to keep reflection effects from causing a false level to be detected. In an ideal case, the termination resistance is equal to the characteristic impedance of the line, and therefore, no reflection is generated at the load. In that one case, the impedance mismatch at the source is of importance only for signal rise time, V_{OH} and V_{OL} considerations.

The effect of additional distributed capacitance on a transmission line is a reduction in impedance resulting in little change to t_{pd}. This additional capacitance does, however, change the signal transition times resulting in a longer rise and fall time.

OUTPUT BUFFERS

The schematic drawing for a typical CMOS TTL output buffer is shown in Figure 3. Figure 4 shows the equivalent circuit as actually implemented in many devices. The actual values for R_{OH} and R_{OL} vary from design to design but the range of values is similar.

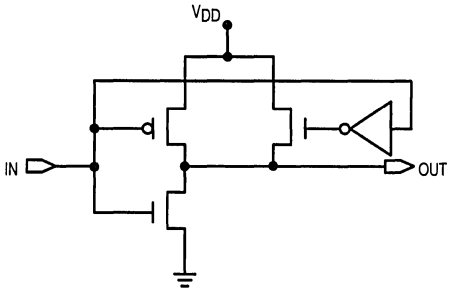

Figure 3. Typical Output Buffer

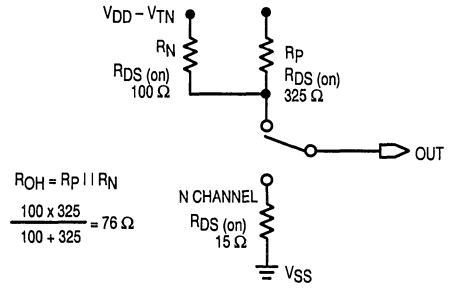

Figure 4. Effective Circuit

As can be seen from Figures 3 and 4, the output impedance of a TTL output buffer is different for high and low output signals. This relation, along with the choice of V_{DD} level, termination resistance, and voltage determine the output high and low levels the part will produce in the system. In a dc condition with $R_L = 50\ \Omega$ = and $V_L = 1.5$ V, the output voltages would be:

$$V_{OL} = V_{SS} + (V_L - V_{SS})\left(\frac{R_{OL}}{R_{OL} + R_L}\right)$$

$$V_{OL} = 0\text{ V} + (1.5\text{ V} - 0\text{ V})\left(\frac{15\ \Omega}{15\ \Omega + 50\ \Omega}\right)$$

$$V_{OL} = 0.35\text{ V} \qquad (3)$$

$$V_{OH} = V_L + \left(V_{DD} - V_L - V_{TN}\ \frac{R_P}{R_P + R_N}\right)\left(\frac{R_L}{R_L + R_{OH}}\right)$$

$$V_{OH} = 1.5\text{ V} + \left(4.4\text{ V} - 1.5\text{ V} - 1.2\text{ V})\ \frac{325\ \Omega}{100\ \Omega + 325\ \Omega}\right)$$

$$\left(\frac{50\ \Omega}{50\ \Omega + 76\ \Omega}\right)$$

$$V_{OH} = 2.33\text{ V} \qquad (4)$$

TRADITIONAL TTL OUTPUT LOAD SPECIFICATIONS

The output loading typically specified in the industry until now is shown in Figure 5. The load consists of a resistor network and capacitance. The values for the network were chosen to present a dc load of 8 mA during an output low condition ($V_{OL} \leq 0.4$ V) and – 4 mA for an output high ($V_{OH} \geq 2.4$ V). A 5 V supply was chosen as the termination supply and a divider network was calculated to provide the specified currents. In addition, a lumped capacitive load of 30 pF was added to the output to represent input loading from other devices. In actual practice during testing, the load used is a Thevenin equivalent as shown in Figure 6, with capacitance being provided by the 50 Ω transmission line connection to the test head and the test fixture capacitance.

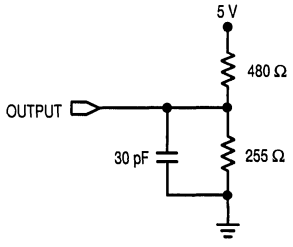

Figure 5. Typical TTL Load

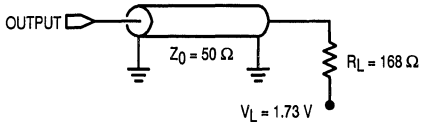

Figure 6. Thevenin Equivalent Test Load

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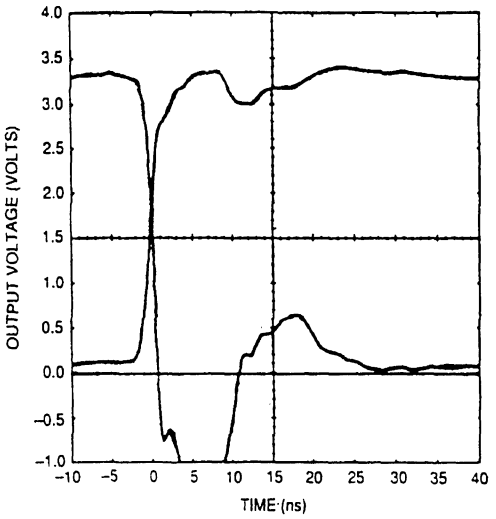

Figure 7. Output Waveforms with Thevenin Equivalent Test Load

The calculated performance of the setup would be that of a transmission line with a Z_0 of 50 Ω terminated to an R_L of 168 Ω at a V_L of 1.73 V. This would be ρ_L = (168 Ω – 50 Ω) / (168 Ω + 50 Ω) = 0.54. This means that the ΔV at the load would be 154% of the source ΔV. Using the example output buffer with V_{DD} = 5.0 V, the dc V_{OL} would be 0.14 V and the incident V_{OH}, using the 50 Ω from Z_0 in place of R_L, would be 2.67 V, giving a ΔV of 2.53 V. The means that for a low to high going signal at the source, at time t_{pd} later, the load would go to V_{OL} + ΔV + (ΔV x 0.54), or 4.01 V.

Figure 7 shows the actual measured waveform at the load end of a test fixture as described in Figure 6. The t_{pd} of the signal path is measured using a TDR (time domain reflectometer) to be approximately 4 ns. Notice the reflection effects at each multiple of t_{pd} on both waveforms. The actual measured waveforms differ from predicted results due to inductance in the ground and V_{DD} path of the device being tested.

In a testing environment, the t_{pd} is subtracted from the time measured to give the actual output delay of the device (access time). Because of this, the distortions at the device output are of no concern. The ringing at the load end, however, can cause severe problems when trying to accurately test the speed of the parts. In the past, the access time has been measured from some mid–level voltage which is centered between the high and low output swing. This has the effect of giving the most noise margin to ringing output signals. However, this maximum noise margin does not guarantee that problems will not arise.

NEW HIGH FREQUENCY AC TEST LOAD

In order to properly test and guarantee the ac performance of these fast static RAMs, it is necessary to change the conditions for ac loading to a load that will allow accurate evaluation of the device parameters. Because of this, the specified ac load is now a transmission line terminated with a resistor of the characteristic impedance of the line to a load voltage (see Figure 8).

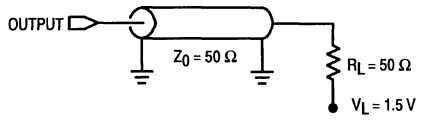

Figure 8. New High Frequency AC Test Load

The calculated performance of this load in a normal test environment would be ρ_L = (50 Ω – 50 Ω) / (50 Ω – 50 Ω) = 0.0. This means that the ΔV at the load would be the same as the source ΔV with no signal reflection.

As seen in Figure 9, using a transmission line terminated to a load supply through a resistor equal to the characteristic impedance of the line produces a load waveform that matches the source signal. Additionally, under ideal conditions, no reflection effects are produced with this load. This results in the maximum possible noise margin for both test and system environments. In this test setup, power supply inductance causes some output noise which is seen at the load.

Figures 10 and 11 are derating curves for calculating the effects of varying C_0 and R_L. These curves are based on typical device performance and are not intended to be absolute worst case specifications.

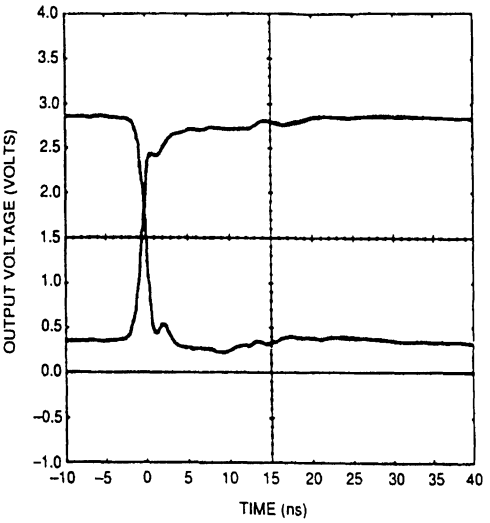

Figure 9. Output Waveforms with High Frequency AC Test Load

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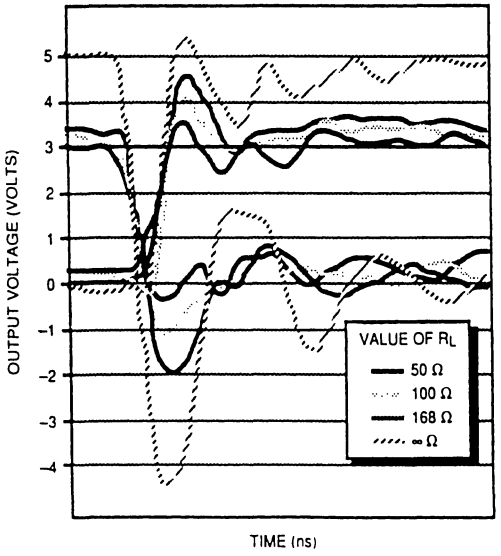

Figure 10. Output Voltage as a Function of R_L

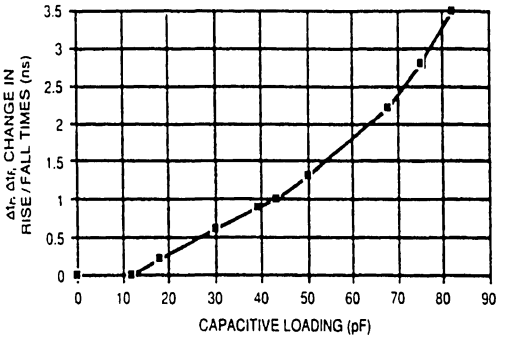

Figure 11. Change in Output Rise and Fall Times for Lumped Capacitive Loads

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NOVEL OVERMOLDED PAD-ARRAY CARRIER MAY OBSOLETE PLASTIC QUAD FLAT PACKS

Until now, the plastic quad flat pack (QFP) has been the package of choice for high-lead-count ICs. But the QFP's successor may have arrived in the form of an overmolded package that uses an array of solder balls for board attachment. Not only does the overmolded pad-array carrier (OMPAC) eliminate worries about lead skew and coplanarity, it also can be handled with the same pick-and-place and soldering equipment used by pc-board manufacturers for low-lead-count components. Furthermore, it's much thinner and may handle more power than an equivalent QFP.

The OMPAC was initially developed by Motorola Inc.'s Land Mobile Products Sector, Plantation, Fla., for its handheld communication products. That group had a need for a high-lead-count package, but wanted to avoid the coplanarity issues surrounding QFPs. Subsequently, the OMPAC was recognized as an attractive vehicle for the high-density CMOS gate arrays produced by Motorola's Semiconductor Products Sector in Phoenix, Ariz. Initially, the OMPAC will come in 169- and 225-contact versions. The former is an alternative to 160-lead QFPs, while the latter can replace 208- or 232-lead QFPs.

The package consists of a thin, BT-epoxy-laminate pc board that's clad with copper *(see the figure)*. BT epoxy is a glass-laminate material similar to FR-4. The top-side metallization carries a die flag and wire-bond pads. The wire-bond pads extend outward to plated through holes located around the board's periphery. These holes provide electrical continuity from the top of the board to the back side. There, the signal path is completed by copper traces routed from the through holes to solder-pad termination sites in a fully populated matrix array. All metal features on the pc board are photodefined, etched, and electroplated with copper, nickel, and gold. A solder mask is photodefined on the back side of the package to contain the flow of solder during infrared (IR) reflow soldering.

Package assembly begins with standard epoxy die-attach and gold-ball-bonding techniques to interconnect the IC to the base. Conventional epoxy transfer-molding procedures are performed to encapsulate the die. After post-mold curing, the packages are solder-bumped, detached from the strip, and electrically tested. The bumps' composition is 62% tin, 36% lead, and 2% silver.

What results is a package that has numerous advantages over conventional QFPs. Because the connections to the board are simple solder balls, no special handling is required. There are no leads to be skewed or knocked out of coplanarity. Motorola's previous answer to QFP lead skew and coplanarity problems was the molded carrier ring, which holds the leads rigid through assembly and test and enables it to guarantee 4-mil coplanarity. With the OMPAC, those problems disappear entirely.

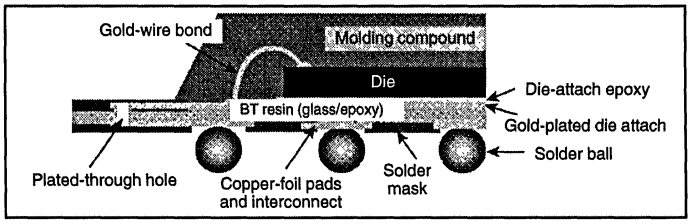
Another advantage is the package's potential power-dissipation capability. Because the OMPAC was adapted for high-performance gate arrays, Motorola addressed thermal enhancements in the form of thermal vias under the die to act as heat pipes through the bottom of the package to lands placed on the pc board. In contrast, QFPs are cooled by forcing air over the mold compound on top of the die. Motorola's measurements indicate that the 225-contact OMPAC with thermal vias delivers a thermal resistance over 20% lower than that of a 208-lead QFP. OMPACs can also be built without thermal vias, in which case their therma performance is roughly equal to that of QFPs.

A key aspect of the OMPAC is how little space it occupies on a board. With a reduced area of about 51% a 169-contact OMPAC will fit inside the body dimensions of a 160-lead QFP That's because of two factors: the lead span of the QFP is eliminated, and the OMPAC's body size is 22 mm versus 28 mm for the QFP. The OMPAC's size advantage also extends to the dimension of height. Both versions stand about 1.5-mm tall from the board. Equivalent QFPs are about 3.65-mm tall.

But even with their smaller size, the 169- and 225-lead OMPACs sport a pitch between solder pads of 1.5 mm, while the 160-lead QFP's leads are pitched at 0.65 mm. At a 1.5-mm pitch, critical circuit-timing traces can be routed directly under the package between the pad rows. This saves board space and shortens critical paths.

In the assembly process, the OMPAC really shines. It can be placed on boards with an alignment tolerance of 12 mils, whereas the QFP needs about a 3-mil registration tolerance. In addition, the OMPAC is more or less self-registering. As the solder balls reflow, the package tends to fall into its lands on the pc board and positions itself. This simplifies the requirement for very-high-precision pick-and-place equipment, thus reducing equipment investments.

For the 225-contact OMPAC user, this translates into IR-reflow attachment of 225 leads. Once again, the OMPAC gives board populators a way to greatly reduce their equipment investment.



Reprinted from ELECTRONIC DESIGN February 1993

The OMPAC, then, represents the attachment of high-lead-count packages at a level that's comparable to devices with much lower lead counts. When the attachment-defect yields are taken into account, the OMPAC becomes even more attractive. In its production trials, Motorola is observing a near-zero-ppm defect yield. At 160 leads, the defect level for QFPs is about 100 ppm, a figure that climbs dramatically at higher lead counts.

Motorola will be offering its HDP Series 1-μm CMOS gate arrays and its H4C Series submicron gate arrays in the 169- and 225-contact OMPACs. Many would-be customers for these devices were unable to handle high-lead-count QFPs, but should be far more comfortable working with the OMPAC.

Production has commenced for the 169-contact package and will begin shortly for the 225-contact package. There is a slight premium for the gate arrays in the OMPAC, but it's anticipated that this will ramp down in time. As for the package's future, Motorola is looking ahead to the OMPAC as a vehicle for multichip modules (MCMs). Developments in this direction could come within the next year.

Motorola's 225-contact OMPAC will be demonstrated in the Universal Instruments booth at next week's Nepcon West show in Anaheim, Calif. This will be the public's first look at the OMPAC.

DAVID MALINIAK

BR1149

Secondary Cache SRAMs for PowerPC™

PowerPC Design Issues

The introduction of high speed PowerPC systems will demand a high performance level two cache solution. In workstation and mid to high end personal computer design, secondary cache is becoming essential and these machines will continue to drive the demand for devices that offer easy design of zero wait state cache performance. Motorola's BurstRAM™ family provides the optimal solution for high performance cache systems. This brief technical overview will focus on Motorola devices that deliver this performance.

High Performance

0 Wait State			
Organization	**V_{CC}**	**I/O**	**Package**
32K x 9	5 V	3.3 V	PLCC
32K x 18	5 V	3.3 V	PLCC
64K x 18	5 V	3.3 V	PLCC
64K x 18	3.3 V	3.3 V	TQFP
32K x 36	3.3 V	3.3 V	TQFP

Moderate Performance

1 Wait State			
Organization	**V_{CC}**	**I/O**	**Package**
32K x 8	5 V / 3.3 V	5 V / 3.3 V	SOJ
32K x 9	5 V	3.3 V	SOJ
128K x 8	5 V	3.3 V	Evo/Revo* SOJ
512K x 8	5 V	5 V	Revo SOJ

* Evo = evolutionary, Revo = revolutionary.

Note that the zero wait state SRAMs have parity bits while the one wait state devices do not. This is mainly due to the fact that the latter will be used in desktop machines and are more cost sensitive. Traditionally, parity checking has not been implemented in this class of machine. Servers, mini-computer class, fault tolerant, and transaction processing machines require parity bits to maintain data integrity.

Microprocessors

Since all 60x (PowerPC) microprocessors feature a common bus interface, all of Motorola's 5 Volt 32K x 9, 32K x 18, and 64K x 18 devices work with these processors. The following is a summary of PowerPC chips.

PowerPC Chips

Processor	Power	Bus Speeds	Comments
MPC601	3.3 V/3.6 V	Up to 66 MHz	3.3 V SRAMs May Need Separate Supply
MPC603	3.3 V	Up to 66 MHz	Notebook/Desktop
MPC604	3.3 V	Up to 66 MHz	Desktop/Server

A Design Note About 3.3 Volt SRAMs and MPC601

Because the PowerPC 601–80 and slower need a 3.6 V power supply, 3.3 V SRAMs may not be well suited for 601 based machines. Most 3.3 V SRAMs limit their supply tolerance to allow operation up to 3.5 V V_{CC}, and may not operate at the upper limit of the 3.6 V supply required by MPC601. If the designer desires to use 3.3 V V_{CC} SRAMs, they may be required to build a machine with three power supply voltages. Therefore, 3.3 V SRAMs do not provide an economically viable solution.

Because other components in the system will require a 5 V V_{CC} for some time to come (e.g. PCI, ISA, DRAMs etc.) 5 V BurstRAMs offer an attractive solution to this dilemma. Motorola's 5 V 32K x 18 and 64K x 18 devices for 601 based machines eliminate the need for a 3.3 V power supply by utilizing the existing 5 V power supply.

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Synchronous SRAMs

A variety of both synchronous, Motorola BurstRAMs and asynchronous fast SRAMs are available to PowerPC system designers. Below is a summary of Motorola's synchronous secondary cache SRAM components with burst mode for PowerPC.

Synchronous BurstRAM Components

Cache Size	Supply Voltage	SRAM Organization	No. of Parts Required	Access Times	Package	Pin Count	Device No.	Pipelined
256K	5 V	32K x 9	8 chips	11/12/14 ns	PLCC(FN)	44	MCM62940B	
		32K x 18	4 chips	9/11/14 ns	PLCC(FN)	52	MCM67M518	
	3.3 V	32K x 36	2 chips	8.5/10/12 ns	TQFP(TQ)	100	MCM69F536	
				5/6/7 ns			MCM69P536	♦
512K	5 V	64K x 18	4 chips	9/11/14 ns	PLCC(FN)	52	MCM67M618	
				9/10/12 ns	PLCC(FN)	52	MCM67M618A	
				5/7 ns	PLCC(FN)	52	MCM67N618A	♦
	3.3 V	64K x 18	4 chips	8.5/10/12 ns	TQFP(TQ)	100	MCM69F618	
				5/6/7 ns			MCM69P618	♦

An Overview of 3.3 V BurstRAM Features

The 3.3 V BurstRAMs (MCM69536/MCM69618) will initially be offered in 64K x 18 and 32K x 36 organizations and have the following features:

- Byte Write and Global Write Capability
- Self-Timed Write
- Pin-Selectable Support for Interleaved (x86) and Linear (PowerPC) Burst Transfers
- 8.5/10/12 ns Access Times (Flow–Through)
- 5/6/7 ns Access Times (Pipelined)
- 100 Pin TQFP Package

Asynchronous SRAMs

If a designer so chooses, it is quite feasible to build a second level cache using asynchronous FSRAMs, although the design requirements are more involved. Below is a summary of devices that may be used as tag and/or data RAMS.

Asynchronous (Standard) SRAMs

Device No.	Organization	Access Time	Pin Count	Package	Comments
MCM6205D	32K x 9	15/20/25 ns	32	SOJ(J)	Tag or Data RAM
MCM6306D	32K x 8	15/20/25 ns	28	SOJ(J)	3.3 V SRAM
MCM6705A	32K x 9	10/12 ns	32	SOJ(J)	Tag or Data RAM
MCM6706B	32K x 8	8/10/12 ns	28	SOJ(J)	Tag or Data RAM
MCM6706R	32K x 8	6/7/8 ns	32	Revo* SOJ(J)	Tag or Data RAM
MCM6706BR	32K x 8	6/7/8 ns	32	Revo SOJ(J)	Tag or Data RAM
MCM6226B	128K x 8	15/20/25 ns	32	Evo* SOJ(J)	Data RAM
MCM6726B	128K x 8	8/10/12 ns	32	Revo SOJ(J)	Data RAM

* Evo = evolutionary, Revo = revolutionary.

Tag RAMs

Although standard asynchronous SRAMs can be used as tag storage, cache designers find the need to integrate the SRAM and compare function on a single chip. Motorola now offers an 8K x 16 Cache Tag RAM designed for the PowerPC market. This device is a single chip solution for 256K caches — two devices can be easily configured to support 512K cache.

Tag RAMs

Device No.	Organization	Access Time	Comments
MCM67T316	8K x 16	10/12 ns	44 PLCC(FN), 5 V power. For use in write through caches. Can be used with MPC105 (Eagle) and MPC106 (Grackle) controllers.

Secondary Cache Modules

Designers can reduce cost and gain flexibility by designing a common motherboard for a variety of products based on a given processor. A simple means of achieving this is to make use of modules as an upgrade option at both the OEM and end user levels. An attractive feature of synchronous second level cache modules is that they provide zero wait state solutions with minimal design effort.

Motorola modules are available in both dual in-line (DIMM) and card edge connector styles. Custom and off-the-shelf solutions are offered.

PowerPC Processor Applications

Description	Chip Set	Functionality	Cache Size	Access Time (Max)	Production	Packaging	Motorola Part Number
PowerPC™	MPC105, MPC106	Flow–Through Burst	512KB	50/60/66 MHz	Now	136 Pin DIMM	MPC2003 (Formerly MCM72MS64)
		Flow–Through Burst	256KB	50/60/66 MHz	Now		MPC2002 (Formerly MCM72MS32)
		Asynchronous	256KB	12/15 ns	Now		MPC2001 (Formerly MCM64AC32)
PowerPC with 16K x 15 CacheTag	MPC105, MPC106	Flow–Through Burst	256KB	60/66 MHz	3Q95	182 Pin Card Edge	MPC2004
		Flow–Through Burst	512KB	60/66 MHz	3Q95		MPC2005
		Flow–Through Burst	1MB	60/66 MHz	3Q95		MPC2006
		Asynchronous	256KB	15 ns	3Q95		MPC2007
		Asynchronous	1MB	15 ns	3Q95		MPC2009

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BR1150

7 x 17 PBGA Sample Preview

GENERAL INFORMATION

MISC7X17THERM — PBGA Thermal Sample
MISC7X17DAISY — PBGA Daisy Chain Sample
MISC7X17MECH — PBGA Mechanical Sample

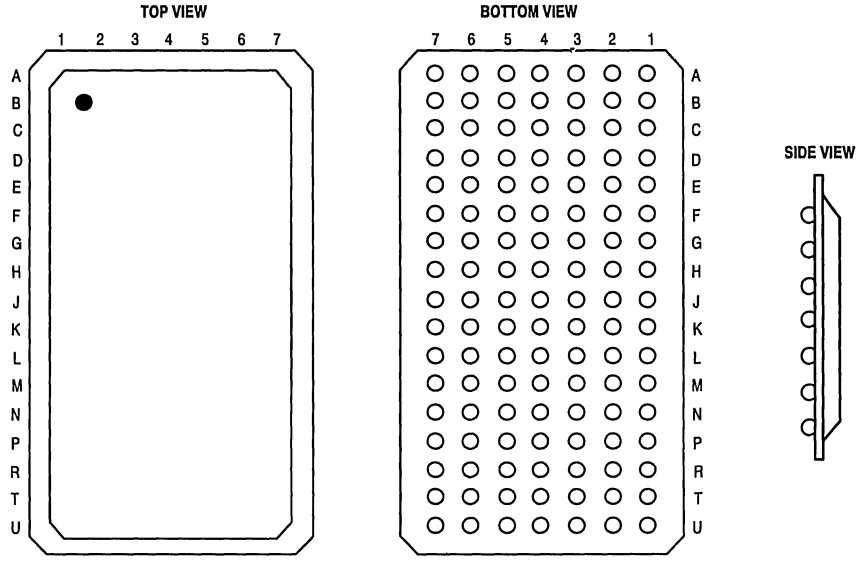
DESCRIPTION

These samples are intended to support Fast SRAM devices that will be packaged in the 7 x 17 PBGA (Plastic Ball Grid Array). Differences in package dimensions and materials may occur between these samples and the actual product.

Thermal Sample: intended for thermal characterization of the package in a system environment. These samples contain a 288 mil x 172 mil Motorola thermal die.

Daisy Chain Sample: intended for solder joint manufacturability and reliability studies. Samples utilize a separate substrate and contain a blank die that is cut to the appropriate size.

Mechanical Sample: intended solely for exercise of customer surface mount processes including: shipping, auto handling, pick and place, reflow, cleaning, rework, and so on. These samples are only guaranteed to meet the case outline physical dimensions. They may not contain a die and should not be used for reliability studies. The materials used in these parts and the nature and content of the marking may vary.



NOTE: Each bump location is identified first by column number and then by row letter. (Drawing not to scale)

Figure 1. 7 x 17 PBGA Layout

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table 8. Bump Assignments and Functions

Bump ID	Bump Name	Description	Comments
6E, 6F, 6G, 6L, 6M	R +	Heater Resistor	Connect all 5 Bumps to (+) Supply
2E, 2F, 2G, 2L, 2M	R –	Heater Resistor	Connect all 5 Bumps to (–) Supply
5A	E_S	Emitter Sense	See Figure 2
3A	E_P	Emitter Power	See Figure 2
3U	C – B_S	Collector – Base Sense	See Figure 2
5U	C – B_P	Collector – Base Power	See Figure 2
7U	Sub	Silicon Substrate	Normally Not Connected
1A, 7A, 1U	—	—	Do Not Connect
2A, 2D, 2H, 2N, 2P, 2U	N/C	N/C	—
6A, 6D, 6K, 6N, 6P, 6U	N/C	N/C	—
6H, 2K	—	—	Shorted Together
3F, 4F, 5F, 3G, 4G, 5G, 3H, 4H, 5H, 3J, 4J, 5J, 3K, 4K, 5K, 3L, 4L, 5L, 3M, 4M, 5M	—	Thermal Bumps	—

NOTE: All other bumps are shorted together.

Typical Electrical Characteristics

- Heater Resistor: 10Ω Nominal Resistance
- Base-Emitter Forward Bias: 700 – 980 mV at 1 mA
  675 – 735 mV at 100 µA
- Base-Emitter Reverse Leakage: < 6 µA at 5 V
- Substrate Leakage: < 30 µA at 20 V
- Base-Emitter K Value: 0.58 – 0.62°C/mV

Maximum Ratings

- Power Dissipation: Dependent on System Environment
- Diode Junction Temperature: 150°C (max)

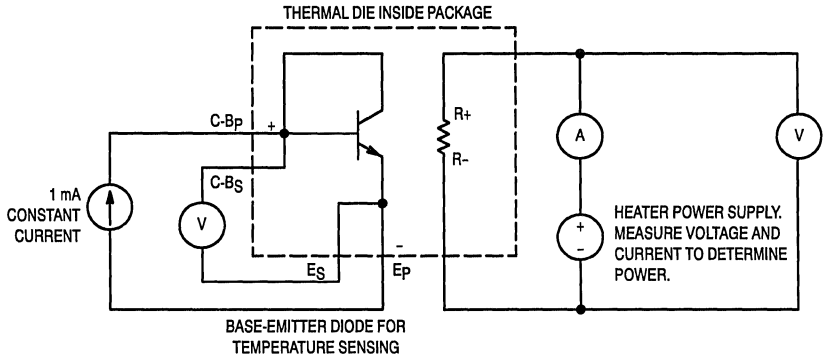
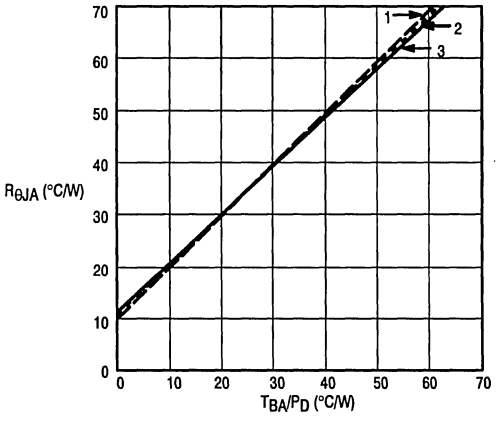


Figure 2. Electrical Hook-Up for Thermal Measurements

8

7 x 17 PBGA Package Thermal Performance

Based on engineering modeling and test data, approximately 90 percent of the heat generated in the package will be dissipated into the motherboard when no heatsink is used. Therefore, plots of junction to ambient resistance ($R_{\theta JA}$)* as a function of airflow are of limited value to the system designer. Instead a plot of measured $R_{\theta JA}$ as a function of the board temperature rise (T_{BA}) divided by the power dissipation (P_D) in the package (T_{BA}/P_D) is provided. The data in Figure 3 was measured at two die power levels, with the packages mounted both on single layer and enhanced four layer boards.



1 — $R_{\theta JA}$, Free Air
2 — $R_{\theta JA}$, 1 m/s
3 — $R_{\theta JA}$, 2 m/s
T_B — Board temperature measured below the package
$R_{\theta JA}$: Junction to ambient resistance ($[T_J - T_A]/P_D$)
T_{BA}: Board temperature rise above ambient ($T_B - T_A$)
P_D: Power dissipated within package $T_J = (R_{\theta JA} * P_D) + T_A$

Figure 3. $R_{\theta JA}$ vs T_{BA}/P_D Characteristics — 119 PBGA Without a Heatsink

As an example in the use of Figure 3, assume a package dissipating 2 W of power in an airflow of 1 m/s. If the ambient temperature (T_A) is 35°C, and the board temperature (T_B) is 85°C, then $T_{BA} = (T_B - T_A) = 50°C$ and T_{BA}/P_D is 25°C/W. Figure 3 provides an $R_{\theta JA}$ value of 35°C/W for these conditions. The junction temperature (T_J) can then be obtained from the equation $T_J = [R_{\theta JA} * P_D] + T_A$ or 105°C for this case. Notice that the junction temperature is largely determined by the board temperature.

Examples (Free Air)

T_B	T_A	P_D (W)	T_{BA}/P_D	$R_{\theta JA}$ (°C/W)	T_J (°C)
50	30	1	20	30	60
50	30	2	10	20	70
80	30	1	50	60	90
80	30	2	25	35	100
80	60	1	20	30	90
80	60	2	10	20	100

$R_{\theta JB}$* and $R_{\theta JC}$* Data

Other relevant measures of package thermal performance are the junction to case thermal resistance ($R_{\theta JC}$) and junction to board thermal resistance ($R_{\theta JB}$). The $R_{\theta JC}$ measurement acquired by the cold plate technique and the $R_{\theta JB}$ data evaluated is as follows.

$R_{\theta JB}$	11.2°C/W
$R_{\theta JC}$	9.7°C/W

For additional information, the user is referred to the detailed Motorola Application Note AN1232/D, *Thermal Performance of the 119 Plastic Ball Grid Array.*

8

* R_θ is a JEDEC standard symbol for thermal resistance.

MISC7X17DAISY

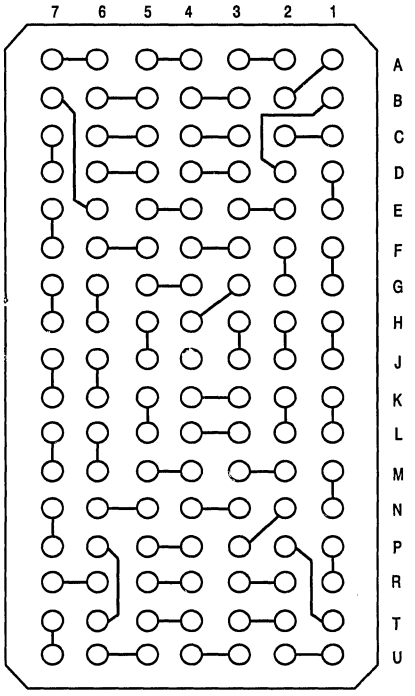


Figure 4. 7 x 17 Daisy Chain Substrate Routing (Bottom View of PBGA)

8

Suggested Motherboard Layout for Daisy Chain Application

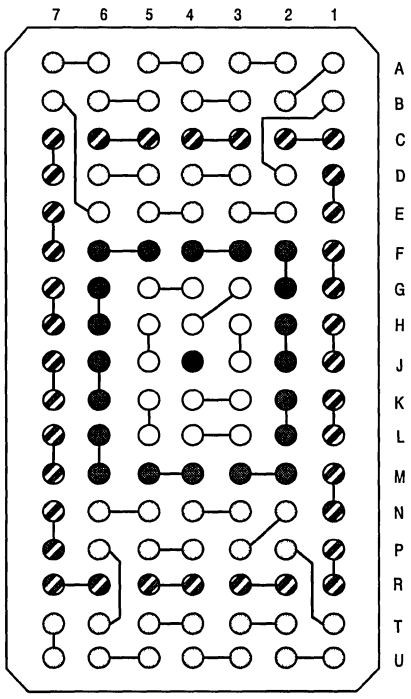


Figure 5. 7 x 17 Daisy Chain Substrate Routing (Bottom View of PBGA)

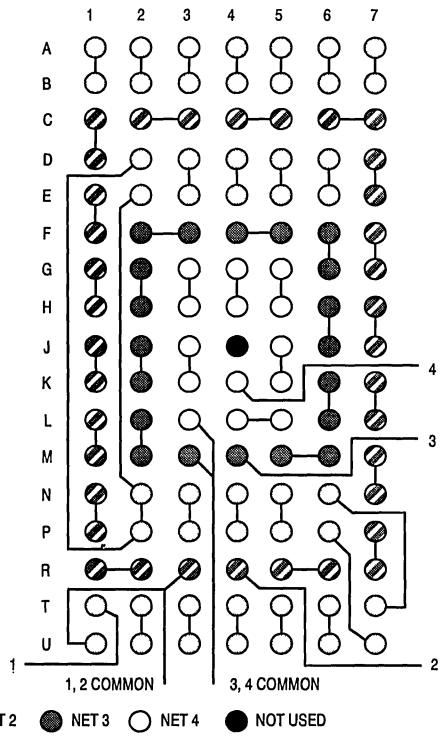


Figure 6. Motherboard Routing

Notes for Suggested Board Layout

Net 1 includes most of the solder joints in the longer ends of the array. This net was designed to include all solder joints that were not part of nets 2, 3, or 4.

Net 2 is a single loop, 7.62 mm x 15.24 mm. This net was designed to correspond with the perimeter of the largest die for this package.

Net 3 is a single loop, 5.08 mm x 7.62 mm. This net was designed to correspond to the perimeter of a typical die for this package.

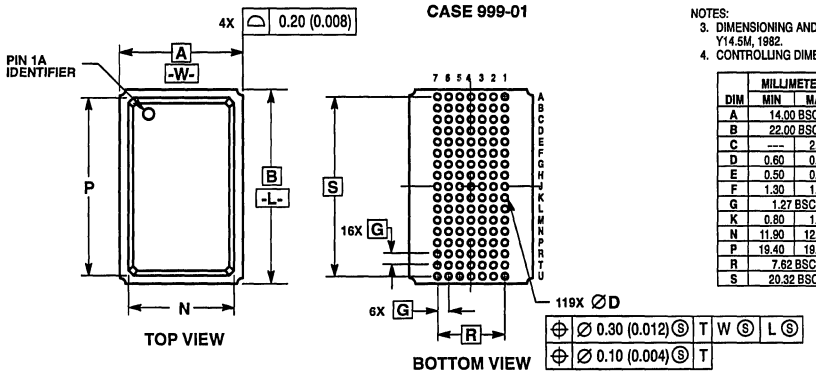
Net 4 is a single loop, 2.54 mm x 5.08 mm. This net was designed to correspond to the perimeter of the smallest die for this package.

To check each net separately, test between the appropriate terminal 1, 2, 3, or 4 and the corresponding common terminal.

To check all joints with a single measurement, do not use the two common terminals. Instead, connect terminals 2 and 3 together and test between terminals 1 and 4.

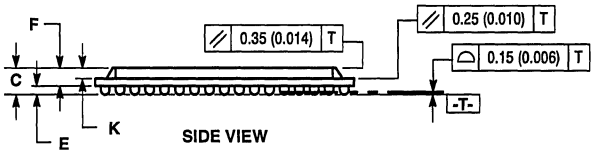
Nets 1 and 2 can be tested together by using only terminals 1 and 2. Likewise, nets 3 and 4 can be tested together by using only terminals 3 and 4.

PACKAGE DIMENSIONS
7 X 17 PBGA
CASE 999-01



NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	---	2.40	---	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	



ORDERING INFORMATION
(Order by Full Part Number)

MISC 7X17 XXXXX XX

- MISC: Miscellaneous Sample
- 7X17: 7 x 17 PBGA
- XXXXX: Sample Type
- XX: Shipping Method (R2 = Tape and Reel, Blank = Waffle Packs)

Full Part Numbers — MISC7X17THERM, MISC7X17THERMR2, MISC7X17DAISY, MISC7X17DAISYR2, MISC7X17MECH, MISC7X17MECHR2

8

BR1152

Secondary Cache SRAMs for Pentium™

Pentium Processor Design Issues

The introduction of high speed Pentium systems will demand a high performance secondary cache solution. In workstation and mid to high end personal computer designs, cache is becoming essential. These machines will continue to drive the demand for devices that offer easy design of zero wait state cache performance. Motorola's BurstRAM™ family provides the optimal solution for high performance cache systems. This brief technical overview will focus on Motorola devices that deliver this performance.

Highest Performance

0 Wait State			
Organization	**V_{CC}**	**I/O**	**Package**
32K x 9	5 V	3.3 V	PLCC
32K x 18	5 V	3.3 V	PLCC
64K x 18	5 V	3.3 V	PLCC
64K x 18	3.3 V	3.3 V	TQFP
32K x 36	3.3 V	3.3 V	TQFP

Moderate Performance

1 Wait State			
Organization	**V_{CC}**	**I/O**	**Package**
32K x 8	5 V / 3.3 V	5 V / 3.3 V	SOJ
32K x 9	5 V	3.3 V	SOJ
128K x 8	5 V	3.3 V	Evo/Revo* SOJ
512K x 8	5 V	5 V	Revo* SOJ

* Evo = evolutionary, Revo = revolutionary.

Note that the zero wait state SRAMs have parity bits while the one wait state devices generally do not. This is mainly due to the fact that the latter will be used in desktop machines which are more cost sensitive. Traditionally, parity checking has not been implemented in this class of machine. Servers, mini-computer class, fault tolerant, and transaction processing machines require parity bits to maintain data integrity.

Microprocessors

Since all x86 microprocessors feature a common bus interface, all of Motorola's 5 Volt synchronous 32K x 9, 32K x 18, and 64K x 18 devices work with all these processors. Pentium bus speeds will likely migrate to 75 MHz, which requires faster access times from the L2 cache RAMs. As a result, pipelined BurstRAMs are required to maintain zero–wait state performance. Although pipelined devices add latency, access times in the 5 to 9 ns range are achieved. The following is a summary of some of the attributes of Pentium processors.

Pentium Microprocessors

Processor	Power	Bus Speeds	Comments
Pentium	5 V / 3.3 V	50/60/66 MHz	64 bit Bus, No new disigns use 5 V Pentiums, 75 MHz bus likely to be added.

BurstRAM is a trademark of Motorola, Inc.
Pentium is a trademark of Intel, Inc.

REV 1
6/95

Synchronous SRAMs

A variety of both synchronous (BurstRAM) and asynchronous fast SRAMs are available to Pentium system designers. Below is a summary of Motorola's synchronous secondary cache SRAM components and modules with burst mode operation for Pentium.

Synchronous BurstRAM Components

Device No.	Organization	Access Time	Pin Count	Package	Pipelined	Comments
MCM62486B	32K x 9	11/12/14/19 ns	44	PLCC(FN)		0.65µ Technology
MCM67B518	32K x 18	9/10/12 ns	52	PLCC(FN)		Flow–Through BurstRAM
MCM67B618	64K x 18	9/10/12 ns	52	PLCC(FN)		Flow–Through BurstRAM
MCM67B618A		9/10/12 ns				
MCM67C518	32K x 18	6/7/9 ns	52	PLCC(FN)	♦	Pipelined BurstRAM
MCM67C618	64K x 18	6/7/9 ns	52	PLCC(FN)	♦	Pipelined BurstRAM
MCM67C618A		5/7 ns			♦	
MCM67H518	32K x 18	9/10/12 ns	52	PLCC(FN)		Flow–Through BurstRAM, supports address pipelining.
MCM67H618A	64K x 18	9/10/12 ns	52	PLCC(FN)		Flow–Through BurstRAM, supports address pipelining.
MCM67J518	32K x 18	6/7/9 ns	52	PLCC(FN)	♦	Pipelined BurstRAM, supports address pipelining.
MCM67J618A	64K x 18	5/7 ns	52	PLCC(FN)	♦	Pipelined BurstRAM, supports address pipelining.
MCM69F618	64K x 18	8.5/10/12 ns	100	TQFP(TQ)		3.3 V Flow–Through BurstRAM
MCM69P618		5/6/7 ns			♦	3.3 V Pipelined BurstRAM
MCM69F536	32K x 36	8.5/10/12 ns	100	TQFP(TQ)		3.3 V Flow–Through BurstRAM
MCM69P536		5/6/7 ns			♦	3.3 V Pipelined BurstRAM

An Overview of 3.3 V BurstRAM Features

The 3.3 V BurstRAMs, the MCM69618/MCM69536, will be offered in 64K x 18 and 32K x 36 organizations and have the following features:

- Byte Write and Global Write Capability
- Self-Timed Write
- Pin-Selectable Support for Intel Burst Transfers
- 8.5/10/12 ns Access Times (Flow–Through)
- 5/6/7 ns Access Times (Pipelined)
- 100 Pin TQFP Package

Asynchronous (Standard) SRAMs

Device No.	Organization	Access Time	Pin Count	Package	Comments
MCM6306D	32K x 8	15/20/25 ns	28	SOJ(J)	3.3 V SRAM
MCM6705A	32K x 9	10/12 ns	32	SOJ(J)	Tag or Data RAM
MCM6706B	32K x 8	8/10/12 ns	28	SOJ(J)	Tag or Data RAM
MCM6706R	32K x 8	6/7/8 ns	32	Revo* SOJ(J)	Tag RAM
MCM6706BR	32K x 8	6/7/8 ns	32	Revo SOJ(J)	Tag RAM
MCM6226B	128K x 8	15/20/25 ns	32	Evo* SOJ(J)	Data RAM
MCM6726B	128K x 8	8/10/12 ns	32	Revo SOJ(J)	Data RAM

* Evo = evolutionary, Revo = revolutionary.

8

Synchronous BurstRAM Modules

Designers can reduce costs and gain flexibility by designing a common motherboard for a variety of products based on a given processor. A simple means of achieving this is to make use of modules as an upgrade option at both the OEM and end user levels. An attractive feature of synchronous second level cache modules is that they provide zero wait state solutions with minimal design effort.

Motorola modules are available in both dual in-line (DIMM) and card edge connector styles. Custom and off-the-shelf solutions are offered.

Pentium and Other x86 Processor Applications

Description	Chip Set	Functionality	Cache Size	Access Time (Max)	Production	Packaging	Device Number
Pentium™ L2 Cache	Intel 82430 FX Triton chip set	Piped Burst	512KB	66 MHz	Now	160 Pin Card Edge	MCM72JG64
			256KB	66 MHz	Now		MCM72JG32
		Asynchronous	256KB	15 ns	2Q95	160 Pin Card Edge	MCM64AF32
Pentium Secondary Cache	Intel 82430 PCI chip set	Flow–Through Burst	512KB	60/66 MHz	Now	136 Pin DIMM Form Factor.	MCM72BA64
			256KB	60/66 MHz	Now		MCM72BA32
	Most Pentium Chip sets	Flow–Through Burst	512KB	60/66 MHz	Now	160 Pin Card Edge	MCM72BB64
			256KB	60/66 MHz	Now		MCM72BB32
		Flow–Through Burst	512KB	60/66 MHz	Now	160 Pin Card Edge	MCM72BF64
	VLSI 82C590	Asynchronous	256KB	15 ns	3Q95	160 Pin Card Edge	MCM64AG32
	Corollary, PeQuR	Piped Burst	512KB	66 MHz	Now	160 Pin Card Edge	MCM72CB64
			256KB	66 MHz	Now		MCM72CB32
i486™ Cache with Tag, Valid, Altered Bit	82420 PCI chip set	Asynchronous	256KB	15 ns	Now	112 Pin Card Edge	MCM32A964
			256KB	15 ns	Now		MCM32N864

8

8

Mechanical Data

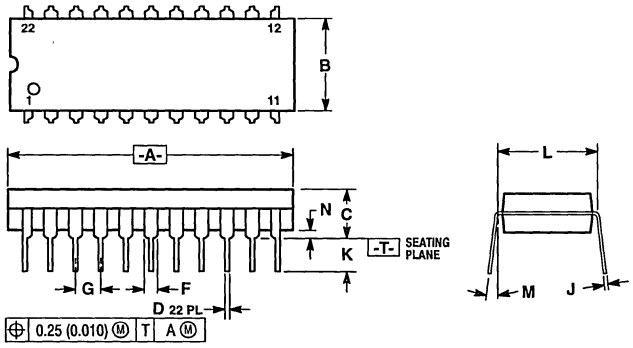
9

9

Package availability and ordering information are given on the individual data sheets.

22–LEAD PACKAGES

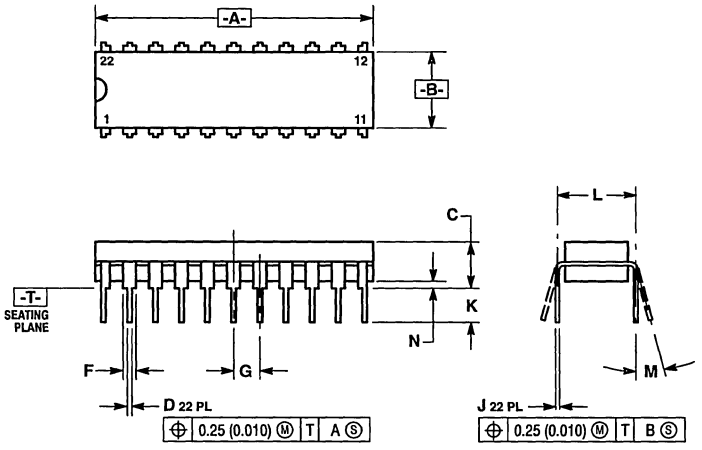
300 MIL PLASTIC
CASE 736A–01



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.65	27.17
B	0.240	0.260	6.10	6.60
C	0.155	0.180	3.74	4.57
D	0.015	0.022	0.38	0.55
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.110	0.140	2.79	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

300 MIL PLASTIC
CASE 736B–01

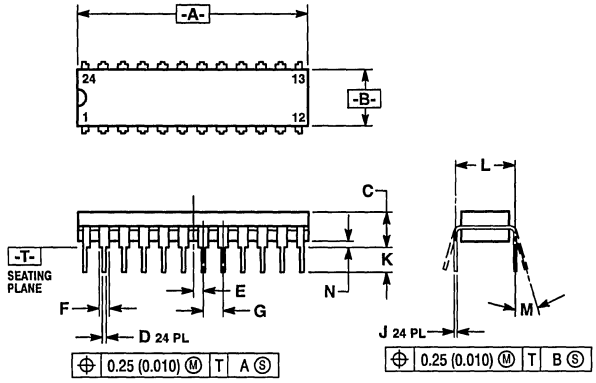


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.070	26.92	27.17
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

9

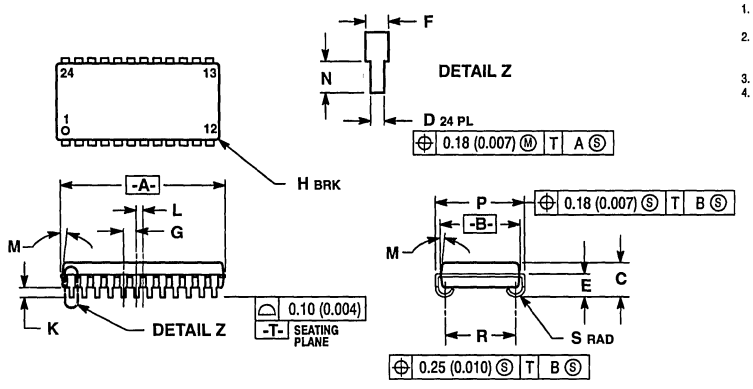
300 MIL PLASTIC
CASE 724A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.160	1.170	29.47	29.71
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

300 MIL SOJ
CASE 810A–02

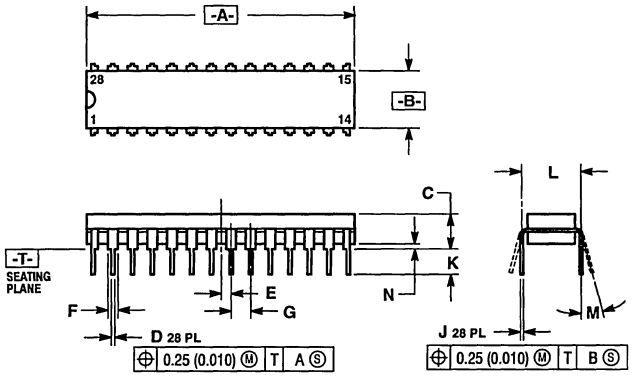


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIMENSION R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.620	0.630	15.75	16.00
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	5°	0°	5°
N	0.030	0.045	0.76	1.14
P	0.335	0.345	8.51	8.76
R	0.260	0.280	6.61	7.11
S	0.030	0.040	0.77	1.01

28–LEAD PACKAGES

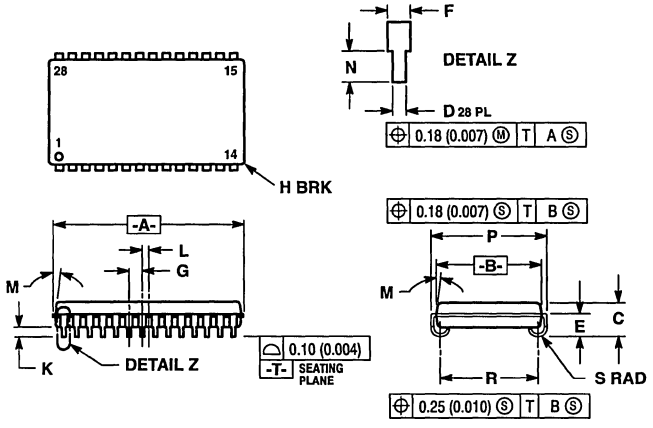
300 MIL PLASTIC
CASE 710B–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.360	1.370	34.55	34.79
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

400 MIL SOJ
CASE 810–03



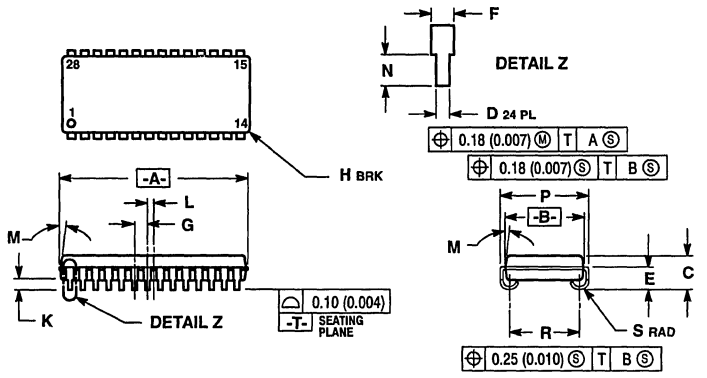
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	5°	0°	5°
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.360	0.380	9.15	9.65
S	0.030	0.040	0.77	1.01

9

28–LEAD PACKAGES (Continued)

300 MIL SOJ
CASE 810B–03

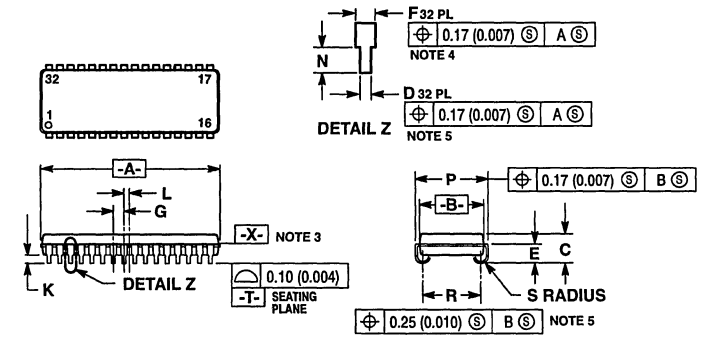


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIMENSION R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	10°	0°	10°
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

32–LEAD PACKAGES

300 MIL SOJ
CASE 857–02



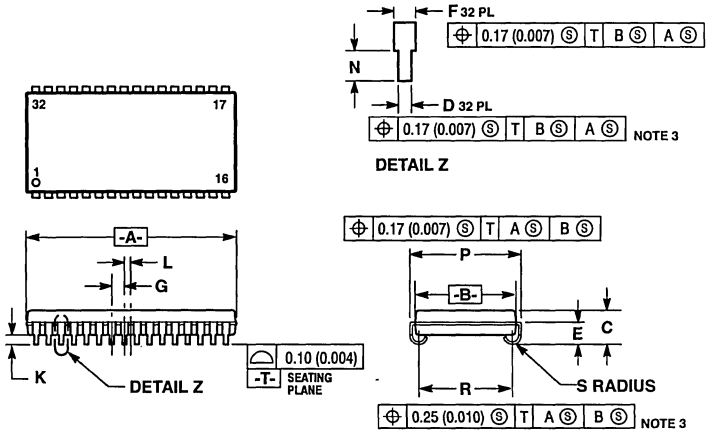
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUM PLANE -X- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
4. TO BE DETERMINED AT PLANE -X-.
5. TO BE DETERMINED AT PLANE -T-.
6. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

9

32–LEAD PACKAGES (Continued)

400 MIL SOJ
CASE 857A–02

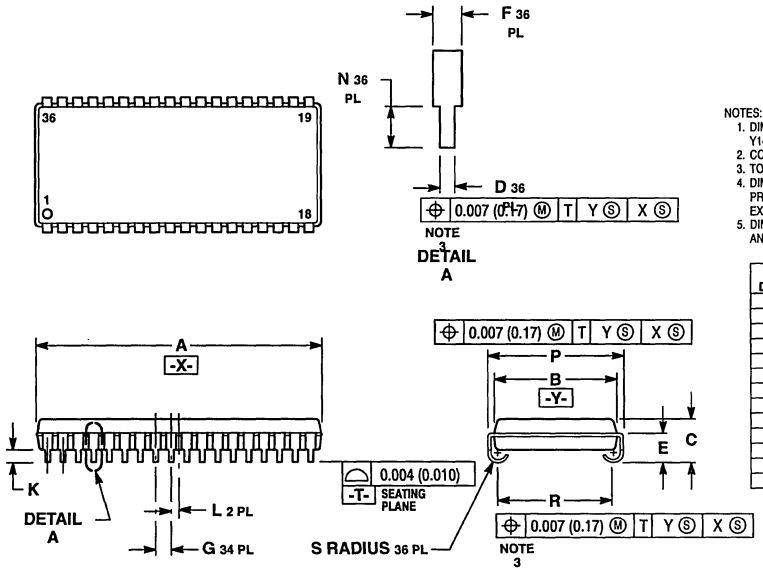


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.27	9.52
S	0.030	0.040	0.77	1.01

36–LEAD PACKAGES

400 MIL SOJ
CASE 893–01

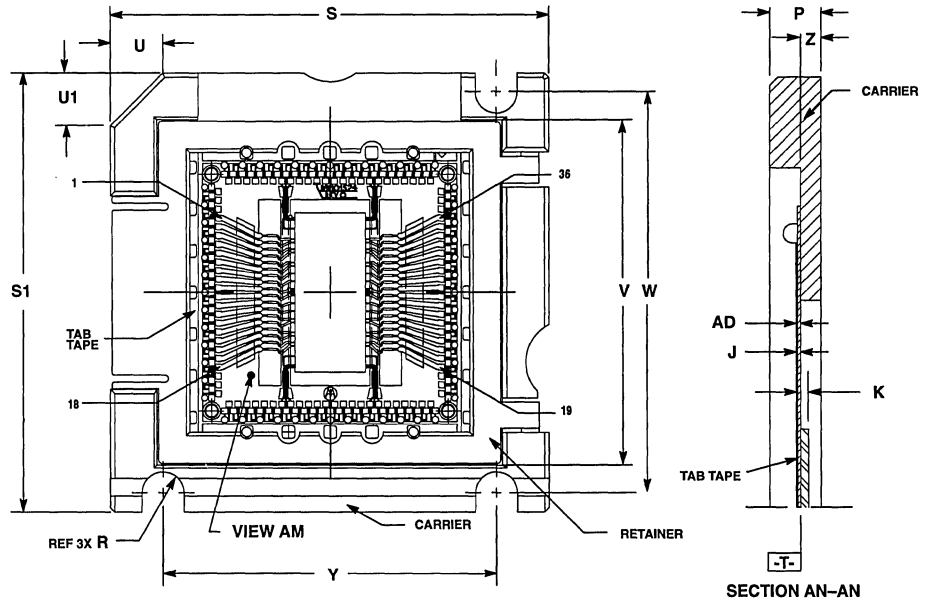


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

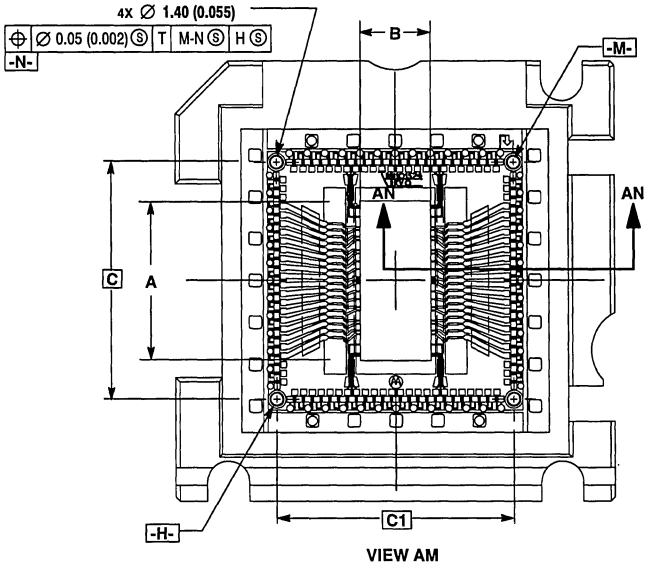
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.035	0.045	0.89	1.14
L	0.025 BASIC		0.64 BASIC	
N	0.030	0.045	0.77	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.28	9.52
S	0.030	0.040	0.77	1.01

9

400 MIL TAB
CASE 984A–01



SECTION AN–AN

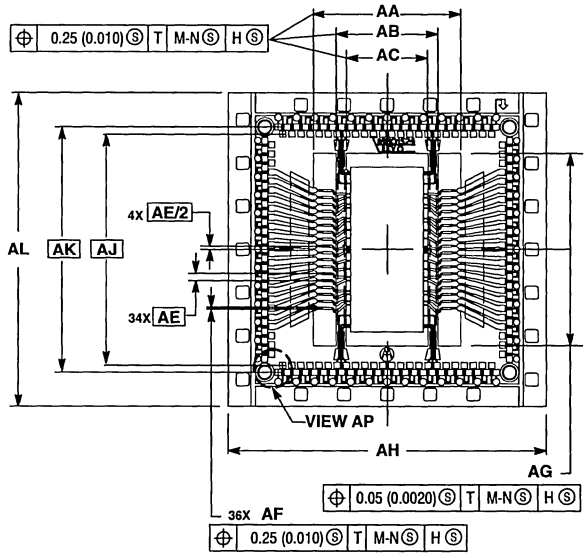


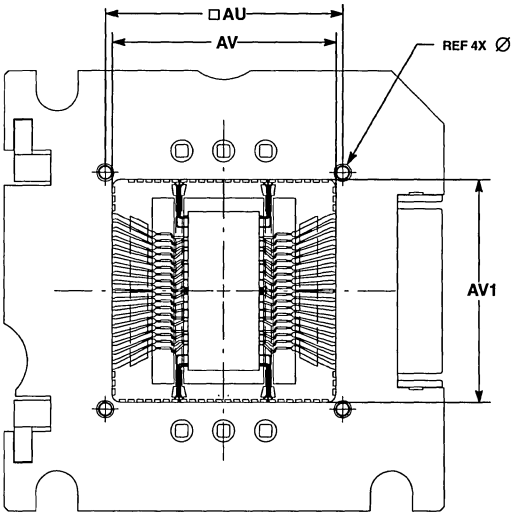
VIEW AM
RETAINER ELIMINATED FROM VIEW FOR CLARITY

NOTES:
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: MILLIMETER.

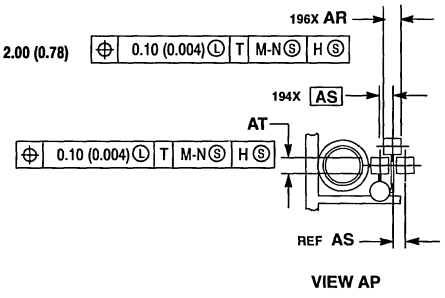
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.14 REF		0.714 REF	
B	8.03 REF		0.316 REF	
C	26.95 BSC		1.061 BSC	
C1	26.95 BSC		1.061 BSC	
J	---	0.25	---	0.010
K	---	0.71	---	0.028
P	3.00 REF		0.118 REF	
R	2.39 REF		0.094 REF	
S	50.00 REF		1.969 REF	
S1	50.00 REF		1.969 REF	
U	6.00 REF		0.236 REF	
U1	6.00 REF		0.236 REF	
V	39.40 REF		1.551 REF	
W	45.68 REF		1.798 REF	
Y	38.00 REF		1.496 REF	
Z	1.15	1.25	0.045	0.049
AA	16.21	16.31	0.638	0.642
AB	11.20	11.30	0.441	0.445
AC	8.99	9.09	0.354	0.358
AD	0.15	0.21	0.006	0.008
AE	0.762 BSC		0.030 BSC	
AF	0.18	0.28	0.007	0.011
AG	21.31	21.24	0.832	0.836
AH	35.00 REF		1.378 REF	
AJ	25.40 REF		1.000 REF	
AK	26.95 BSC		1.061 BSC	
AL	34.98 REF		1.377 REF	
AR	0.65	0.75	0.026	0.030
AS	0.50 BSC		0.020 BSC	
AT	0.60	0.70	0.024	0.028
AU	26.95 REF		1.061 REF	
AV	25.35	25.45	0.998	1.002
AV1	25.35	25.45	0.998	1.002

400 MIL TAB
CASE 984A–01
(CONTINUED)





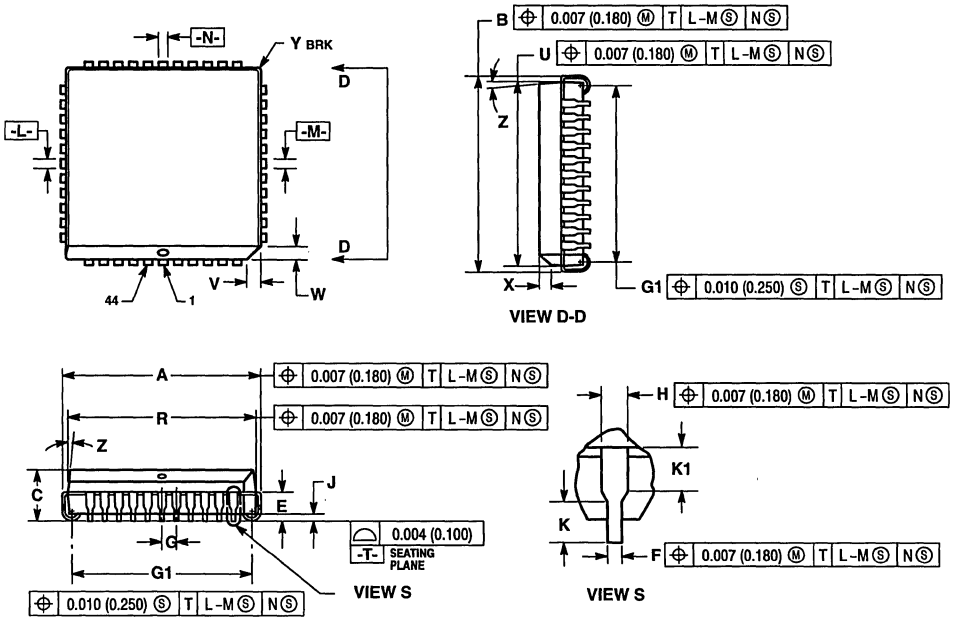
BOTTOM VIEW



VIEW AP

9

PLASTIC CHIP CARRIER
CASE 777–02

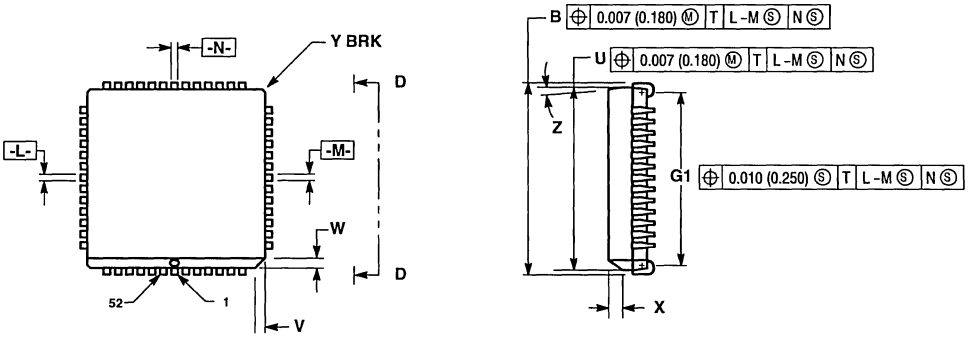


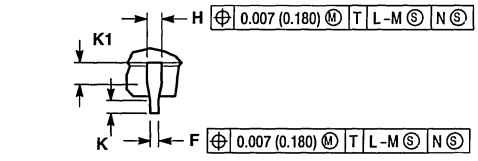
NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

9

PLASTIC CHIP CARRIER
CASE 778–02



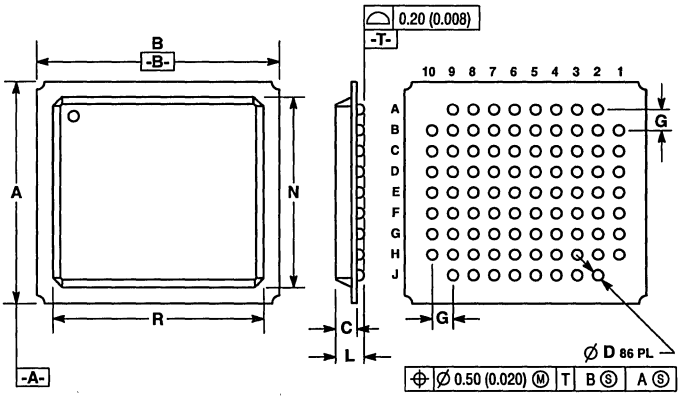


VIEW S

NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

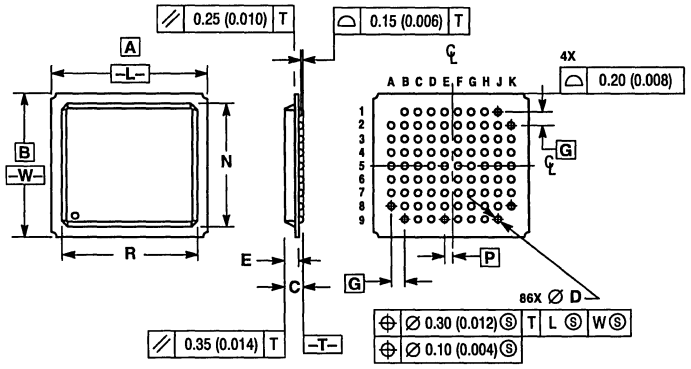
PLASTIC BALL GRID ARRAY
CASE 896A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

PLASTIC BALL GRID ARRAY
CASE 896A–02

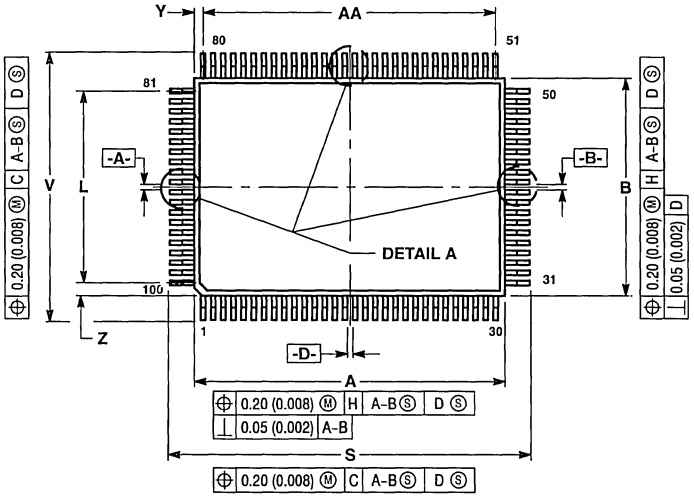


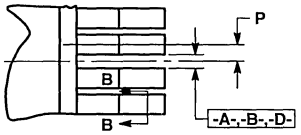
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.78 BSC		0.700 BSC	
B	16.26 BSC		0.640 BSC	
C	1.84	2.44	0.073	0.096
D	0.69	0.81	0.028	0.031
E	1.33	1.73	0.053	0.068
G	1.524 BSC		0.060 BSC	
N	13.80	14.20	0.544	0.559
P	0.762 BSC		0.030 BSC	
R	15.29	15.69	0.602	0.617

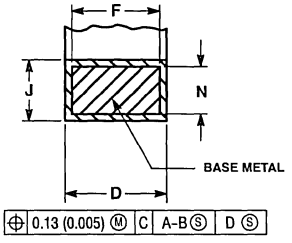
9

TQFP
CASE 983A–01

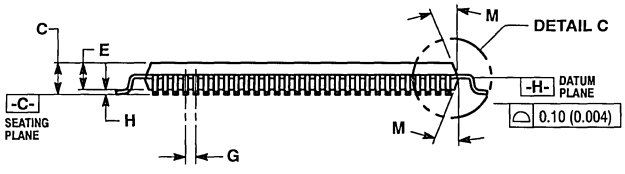


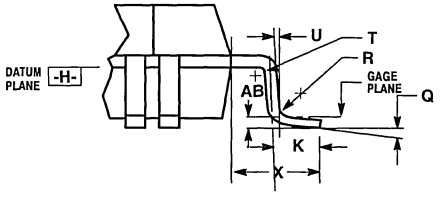


DETAIL A



SECTION B-B
VIEW ROTATED 90° CLOCKWISE



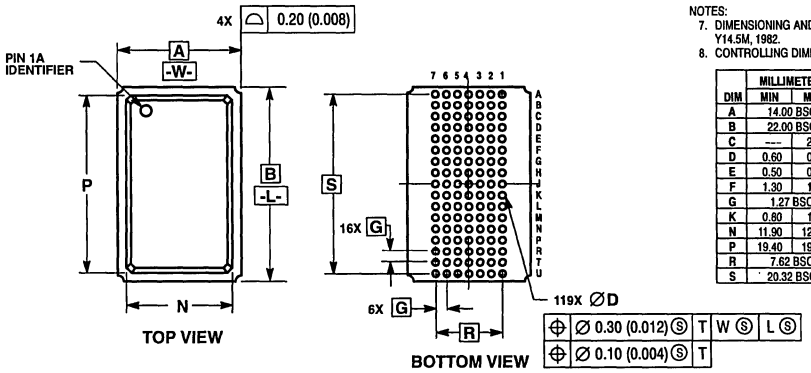


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.460 (0.018). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

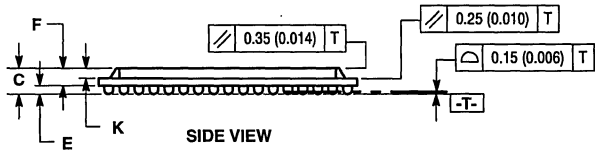
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.90	20.10	0.783	0.791
B	13.90	14.10	0.547	0.555
C	—	1.60	—	0.063
D	TBD	TBD	TBD	TBD
E	1.35	1.45	0.053	0.057
F	2.24 REF		0.088 REF	
G	0.65 BSC		0.026 BSC	
H	0.09	0.20	0.004	0.008
J	TBD	TBD	TBD	TBD
K	0.45	0.75	0.018	0.030
L	12.35 REF		0.486 REF	
M	11°	13°	11°	13°
N	0.35	0.38	0.014	0.015
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.08	0.20	0.003	0.008
S	22.00 BSC		0.866 BSC	
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.00 BSC		0.630 BSC	
X	1.00 REF		0.039 REF	
Y	0.58 REF		0.023 REF	
Z	0.83 REF		0.033 REF	
AA	18.85 REF		0.742 REF	
AB	0.25 BSC		0.010 BSC	

PLASTIC BALL GRID ARRAY
CASE 999–01



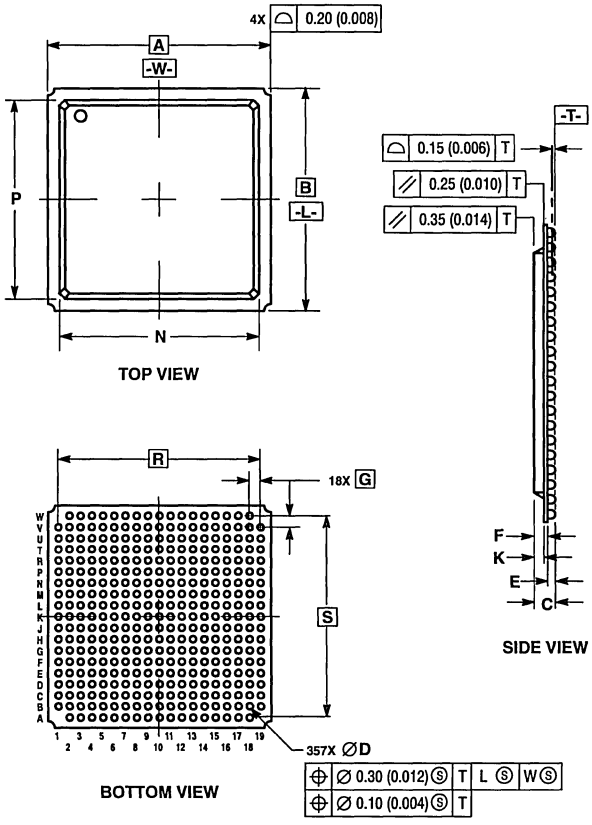
NOTES:
7. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
8. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
B	22.00 BSC		0.866 BSC	
C	---	2.40	---	0.094
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	1.30	1.70	0.051	0.067
G	1.27 BSC		0.050 BSC	
K	0.80	1.00	0.031	0.039
N	11.90	12.10	0.469	0.476
P	19.40	19.60	0.764	0.772
R	7.62 BSC		0.300 BSC	
S	20.32 BSC		0.800 BSC	



9

PLASTIC BALL GRID ARRAY
CASE 1103–01

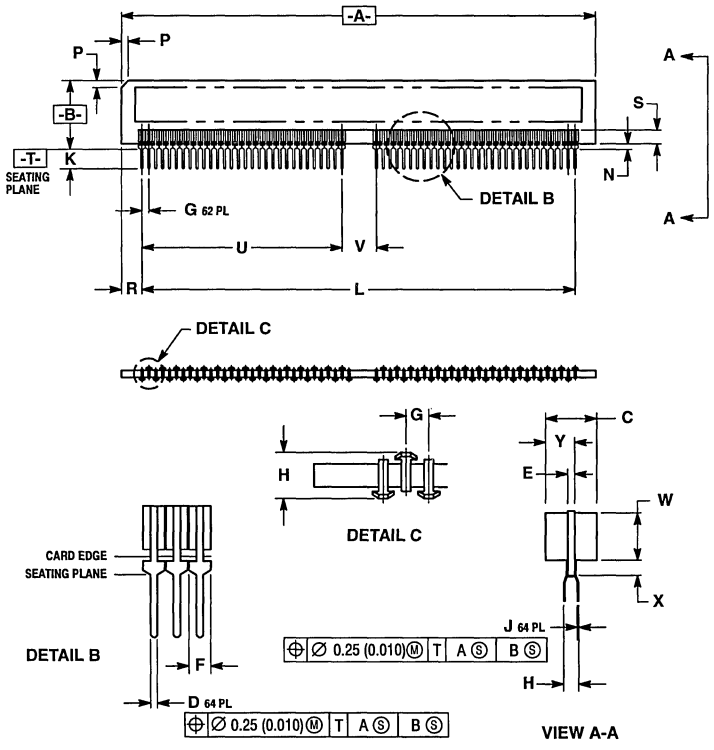


NOTES:
9. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
10. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	---	2.05	---	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

9

64 LEAD
ZIP PACKAGE
CASE 871–01

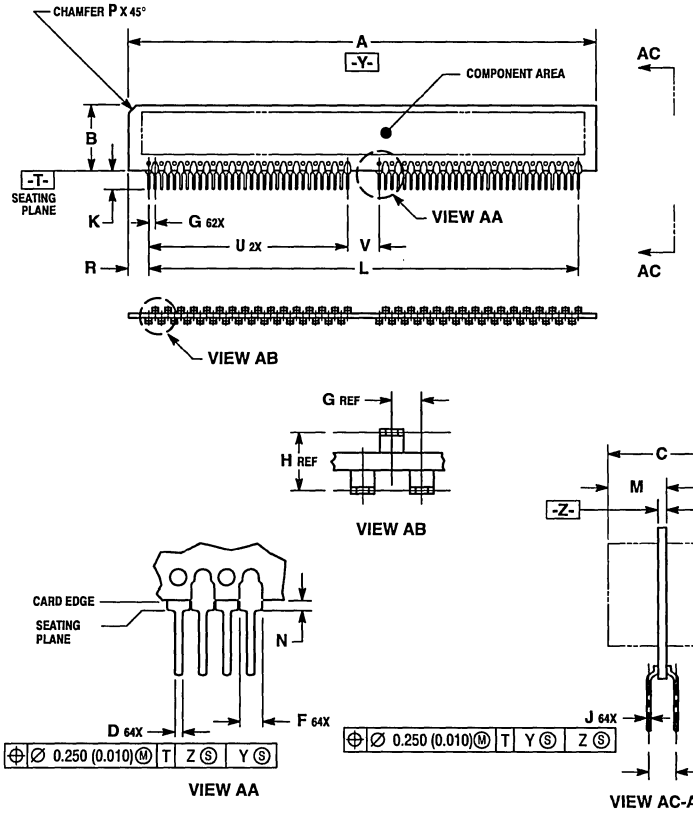


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.640	3.660	92.46	92.96
B	—	0.550	—	13.97
C	—	0.370	—	9.40
D	0.015	0.025	0.38	0.64
E	0.035	0.055	0.89	1.40
F	0.040	0.055	1.02	1.40
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.008	0.014	0.20	0.36
K	0.120	0.160	3.05	4.06
L	3.345	3.355	84.96	85.22
N	0.010	0.055	0.25	1.40
P	0.045	0.055	1.14	1.40
R	0.135	0.165	3.43	4.19
S	—	0.100	—	2.54
U	1.550 REF		39.37 REF	
V	0.250 REF		6.35 REF	
W	—	0.345	—	8.76
X	—	0.150	—	3.81

9

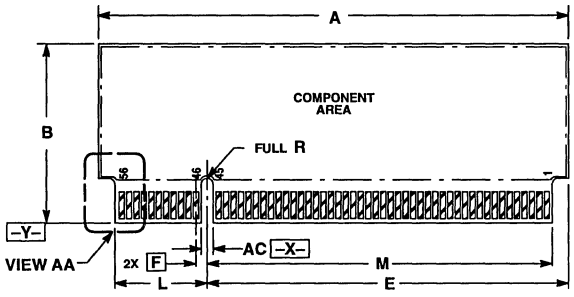
64 LEAD
ZIG ZAG IN–LINE
CASE 871A–01



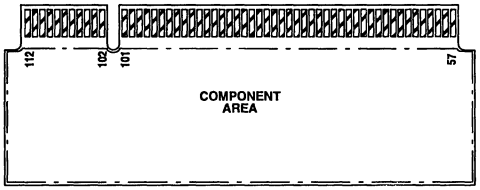
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.640	3.660	92.45	92.963
B	—	0.500	— 7	12.699
C	—	0.370	—	9.397
D	0.015	0.025	0.382	0.634
E	0.035	0.055	0.890	1.396
F	0.040	0.055	1.017	1.396
G	0.050 BSC		1.270 BSC	
H	0.100 BSC		2.540 BSC	
J	0.008	0.014	0.202	0.354
K	0.120	0.160	3.049	4.063
L	3.350 REF		85.090 REF	
M	—	0.240	—	6.096
N	0.010	0.055	0.255	1.396
P	0.045	0.055	1.144	1.396
R	0.135	0.165	3.430	4.190
S	—	0.100	—	2.540
U	1.550 REF		39.371 REF	
V	0.250 BSC		6.351 BSC	
W	—	0.345	—	8.762
X	—	0.150	—	3.809

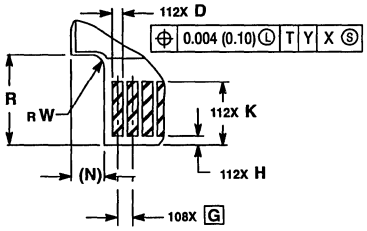
112–LEAD CARD EDGE
CASE 1112–01



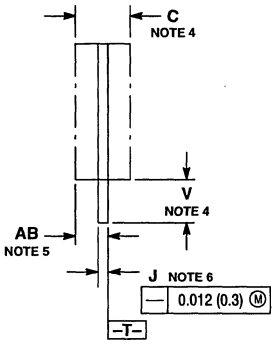
FRONT VIEW



BACK VIEW



VIEW AA



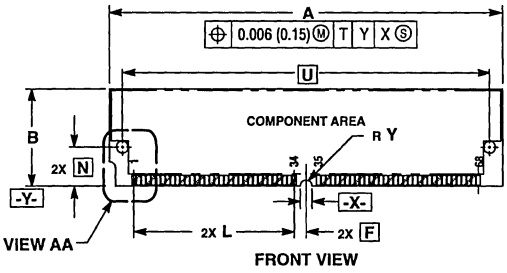
SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

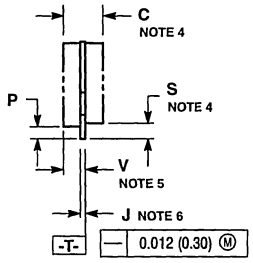
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.130	3.150	79.50	80.01
B	1.190	1.210	30.23	30.73
C	---	0.365	---	9.27
D	0.033	0.037	0.84	0.94
E	2.415	2.425	61.34	61.60
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	---	0.030	---	0.76
J	0.055	0.069	1.40	1.75
K	0.210	---	5.33	---
L	0.605	0.615	15.37	15.62
M	2.305	2.315	58.55	58.80
N	0.110 REF		2.79 REF	
R	0.285	0.305	7.24	7.75
V	0.285	---	7.24	---
W	0.040	0.060	1.02	1.52
AB	---	0.220	---	5.59
AC	0.072	0.076	1.83	1.93

9

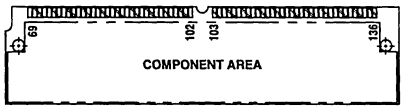
136–LEAD DIMM MODULE
CASE 1104–01



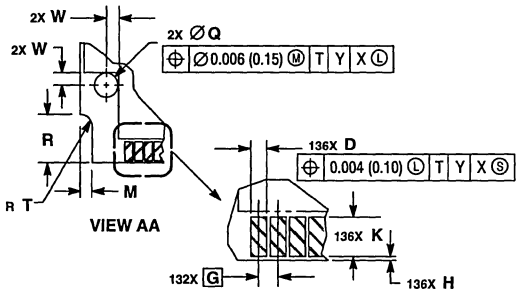
FRONT VIEW



SIDE VIEW



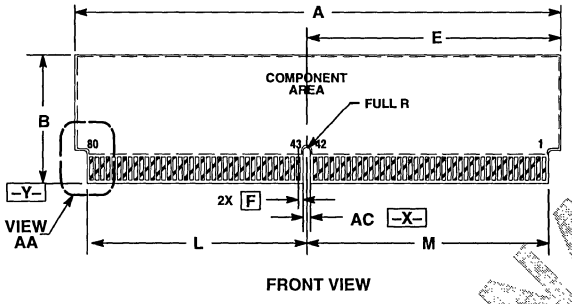
BACK VIEW



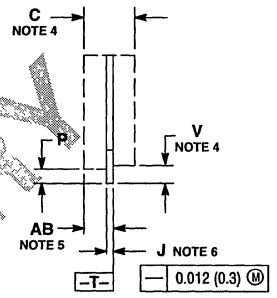
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND S DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.045	4.055	102.74	103.00
B	0.995	1.005	25.27	25.53
C	---	0.413	---	10.50
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	---	0.010	---	0.25
J	0.046	0.054	1.17	1.37
K	0.100	---	2.54	---
L	1.650 BSC		41.91 BSC	
M	0.075	0.085	1.91	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	---	3.18	---
Q	0.123	0.127	3.12	3.22
R	0.245	0.255	6.22	6.48
S	0.157	---	4.00	---
T	0.060	0.064	1.52	1.63
U	3.784 BSC		96.11 BSC	
V	---	0.236	---	6.00
W	0.062	---	1.57	---
Y	0.060	0.064	1.52	1.63

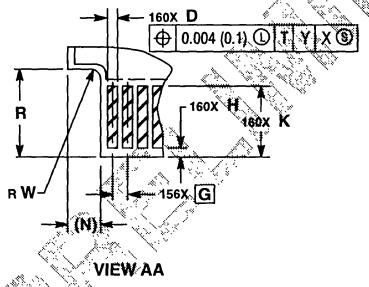
160–LEAD
CARD EDGE MODULE
CASE 1113–01



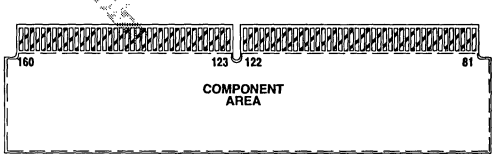
FRONT VIEW



SIDE VIEW



VIEW AA

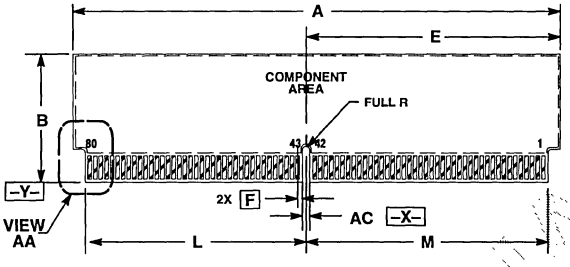


BACK VIEW

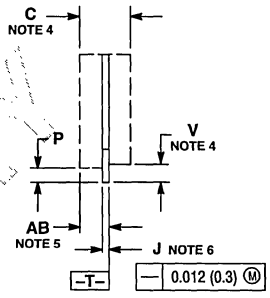
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.330	4.350	109.98	110.49
B	1.290	1.310	32.77	33.27
C	---	0.454	---	11.53
D	0.033	0.037	0.84	0.94
E	2.265	2.275	57.53	57.79
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	---	0.030	---	0.51
J	0.055	0.069	1.40	1.75
K	0.210	---	5.33	---
L	1.955	1.965	49.66	49.91
M	2.155	2.165	54.74	54.99
N	0.110 REF		2.79 REF	
P	0.125	---	3.18	---
R	0.285	0.305	7.24	7.75
V	0.157	---	3.99	---
W	0.040	0.060	1.02	1.52
AB	---	0.262	---	6.66
AC	0.072	0.076	1.83	1.93

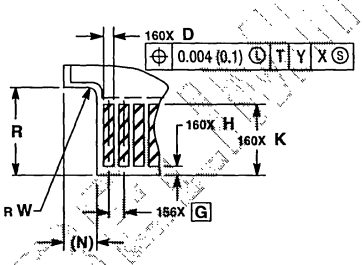
160–LEAD
CARD EDGE MODULE
CASE 1113A–01



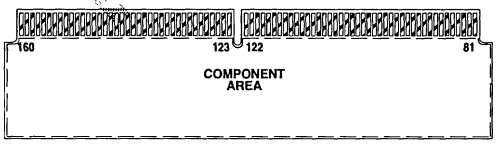
FRONT VIEW



SIDE VIEW



VIEW AA



BACK VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS C AND V DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION AB DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.330	4.350	109.98	110.49
B	1.270	1.310	32.26	33.27
C	---	0.454	---	11.53
D	0.033	0 037	0.84	0.94
E	2.265	2.275	57.53	57.79
F	0.075 BSC		1.91 BSC	
G	0.050 BSC		1.27 BSC	
H	---	0.030	---	0 51
J	0.055	0.069	1.40	1.75
K	0.210	---	5.33	---
L	1.955	1.965	49.66	49.91
M	2.155	2.165	54.74	54.99
N	0.110 REF		2.79 REF	
P	0.125	---	3.18	---
R	0.285	0.305	7.24	7.75
V	0.157	---	3.99	---
W	0.040	0 060	1.02	1.52
AB	---	0.262	---	6.66
AC	0.072	0.076	1.83	1.93

9

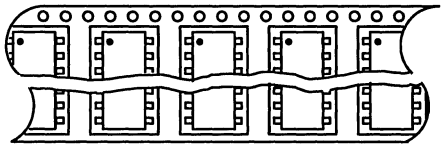
Embossed Tape and Reel

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel-back" cover tape.

- 13-Inch Reel
- Used For Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA-481
- SOJ: 24, 20/26, 24/26, 28, 32
- SOIC: 28, 32
- PLCC: 44, 52

Ordering Information

Use the standard device title and add the required suffix. Note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

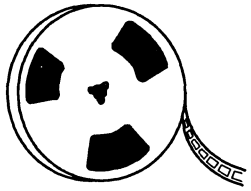


DIRECTION OF FEED

Tape and Reel Data for MOS Memory Surface Mount Devices

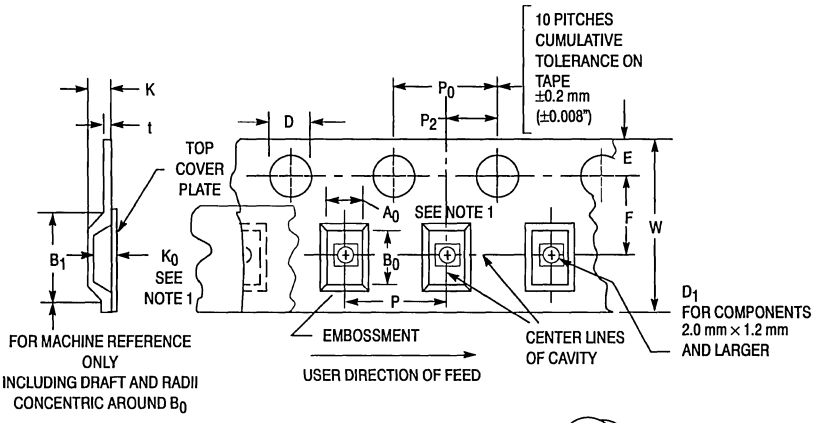
PACKAGES

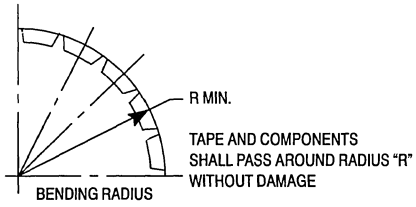
SOJ: 24, 20/26, 24/26, 28, 32
SOIC: 28, 32
PLCC: 44, 52

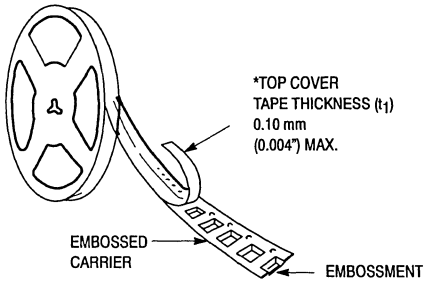


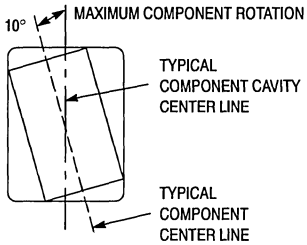
Package	Lead Count	Package Width (mils)	Tape Width (mm)	Reel Size	Devices Per Reel	Minimum Lot Size
SOJ	24	300	24	13"	1000	1000
	20/26	300	24	13"	1000	1000
	20/26	350	24	13"	1000	1000
	24/26	300	24	13"	1000	1000
	28	300	24	13"	1000	1000
	28	400	32	13"	1000	1000
	32	300	32	13"	1000	1000
	32	400	32	13"	1000	1000
SOIC (Gull Wing)	28	350	24	13"	1000	1000
	32	450	32	13"	1000	1000
PLCC	44	650/656	32	13"	450	450
	52	750/756	32	13"	450	450

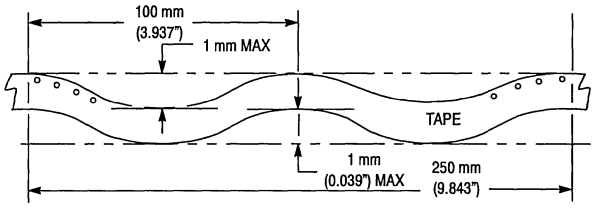
CARRIER TAPE SPECIFICATIONS











CAMBER (TOP VIEW)
ALLOWABLE CAMBER TO BE 1 mm/100 mm NONACCUMULATIVE OVER 250 mm

DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R Min	t Max	W
24 mm	19.4 mm (0.764")	1.5+0.1 mm -0.0 (0.059+0.004" -0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.1 mm (0.453 ±0.004")	4.0 mm (0.157")	12.0–16.0 ±0.10 mm (0.472–0.630 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.400 mm (0.016")	24 ±0.2 mm (0.945 ±0.008")
32 mm	23.0 mm (0.906")	1.5+0.1 mm -0.0 (0.059+0.004" -0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	14.2 ±0.1 mm (0.559 ±0.004")	10.0 mm (0.394")	16.0–24.0 ±0.10 mm (0.630–0.945 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.500 mm (0.020")	32 ±0.3 mm (1.26 ±0.012")

Metric Dimensions Govern–English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by compnent size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

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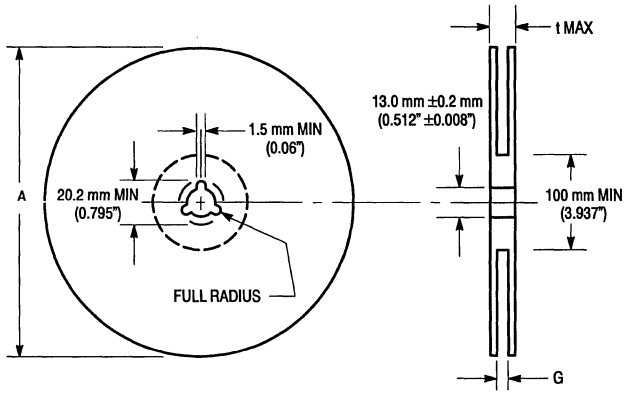
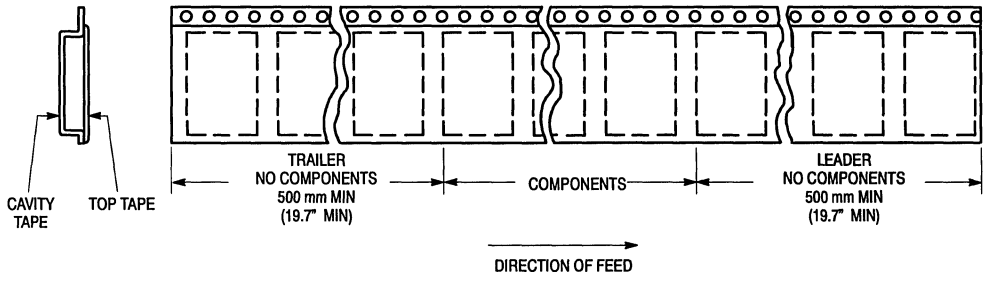
REEL DIMENSIONS

Metric Dimensions Govern–English are in Parentheses for Reference only.



Size	A Max	G	t Max
24 mm	330 mm (12.992")	24.400 mm, +2.0 mm, –0.0 (0.961", +0.079", –0.00)	30.4 mm (1.197")
32 mm	330 mm (12.992")	32.4 mm, +2.0 mm, –0.0 (1.276", +0.079", –0.00)	38.4 mm (1.51")

TAPE ENDS



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