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DL160/D
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Display Products

Device Data

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Device Data

Motorola offers a broad range of semiconductor communications products for a wide variety of applications. The *Motorola Display Products Device Data Book* contains specifications on these parts as well as information on Evaluation Kits, a selection of Application Notes and Technical Literature, a Glossary of related terms, Handling and Design Guidelines, and Reliability and Quality information. A Technical Selection Guide is also included to help you select the appropriate part for your application.

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Selection Guide 1

LCD Driver Product Summary

Segmented LCD Driver for Low MUX Application

Part Number	Description	System	Application Examples	Display Size Examples	Package
MC14LC5003	4 MUX, Total 128 Segments, Serial In	Low MUX, General MCU	Fax Machines, Pager, Digital Meter, Home Appliances	32 x 4	QFP, Bare Die
MC14LC5004	4 MUX, Total 128 Segments, IIC				

DragonKat Series LCD Driver Kits with MC68HC05L10/L11

Part Number	Description	System	Application Examples	Display Size Examples	Package
MC141511A	DragonKat 1+ Slave Driver, 32/41 MUX, 128 Segments	DragonKat 1+ MC68HC05L10	Databank, Pager, Organizer, Games	128 x 32/41, 256 x 32/41	TAB, Bare Die
MC141512	DragonKat 2 Backplane Driver, 146 MUX, 80 Backplanes	DragonKat 2 MC68HC05L11	Translator, Dictionary, Pen-Based Organizer, Low-Cost PDA	160 x 80, 320 x 146, 320 x 160	TAB
MC141514	DragonKat 2 Segment Driver, 146 MUX, 160 Segments				
MC141515	DragonKat 2 Backplane Driver, 146 MUX, 160 Backplanes				
MC141519	DragonKat 2 Segment Driver, 80 MUX, 160 Segments				
MC141516	64 MUX LCD Backplane Driver, 64 Backplane Outputs	DragonKat 2 MC68HC05L11, other MCU with SPI	Pager, Games, Dictionary	80 x 64, 160 x 64, 240 x 64	TQFP, Bare Die
MC141518	64 MUX LCD Segment Driver, 80 Segment Outputs				

TFT LCD Driver Accepts RGB Signal Inputs

Part Number	Description	System	Application Examples	Display Size Examples	Package
MC141522	TFT-LCD Gate (Row) Driver, 120 Row Outputs	Active LCD	Portable TV, Projector	480 x 240, 720 x 480	TAB
MC141524	TFT-LCD Source (Column) Driver, 120 Column Outputs				

MC14153X Series LCD Driver with Commons, Segments, Annunciators "All-in-One" Chip

Part Number	Description	System	Application Examples	Display Size Examples	Package
MC141531	17 Com, 120 Seg, 3 Annunciators	General MCU, 6800, 68K (Parallel Interface)	Mobile Communication Devices, Pager, Cellular, PHS	120 x 17	TAB, Bare Die, Gold Bump Die
MC141532	33 Com, 120 Seg, 4 Annunciators			120 x 33	
MC141533	33 Com, 120 Seg, 4 Annun, Split Common Outputs			120 x 33	
MC141535	17 Com, 161 Seg, 4 Annunciators			161 x 17	
MC141537	16 Com, 120 Seg, 3 Annunciators			120 x 16	
MC141539	32 Com, 120 Seg, 4 Annunciators			120 x 32	

300 MUX LCD Driver without Display DRAM

Part Number	Description	System	Application Examples	Display Size Examples	Package
MC141562	LCD Common Driver, 100 Common Outputs	DragonBall™ MC68328, General MCU with LCD Controller	PDA, Palm-Top, Sub-Notebook	320 x 200, 320 x 240, 640 x 200	TAB, Gold Bump Die
MC141563	LCD Segment Driver, 80 Segment Outputs				

MC14180X Series LCD Driver for Cellular Phone/PHS Applications

Part Number	Description	System	Application Examples	Display Size Examples	Package
MC141800A	65 Common, 128 Segment Outputs	General MCU, 6800, 68K (IIC, SPI, Parallel Interface)	Cellular Phone, PHS Large Display Pager	128 x 65, 128 x 64 Plus One Row for Icons	TAB, Gold Bump Die

LCD Driver Technical Selection Guide

Features	MC14LC5003 MC14LC5004	MC141511A	MC141512	MC141514	MC141515	MC141519
Type	Passive	Passive	Passive	Passive	Passive	Passive
Backplane/Common/Row	4	–	80	–	160	–
Segment/Column	32	128	–	160	–	160
MUX Ratio/Duty	1/4	1/32 or 1/41	1/32 – 1/146	1/32 – 1/146	1/32 – 1/146	1/32 – 1/80
Operating Voltage for Internal Circuit V_{DD} (V)	3 or 5	3 or 5	3 or 5	5	5	3 or 5
Voltage for LCD Drive Circuit VLCD (V)	5	12	25	25	25	16
Typical Current Consumption IDD Display Standby ILCD Display	 30 µA 30 µA 40 µA	 25 µA 15 µA 20 µA	 1 µA 0.5 µA 3 µA	 50 µA 1 µA 10 µA	 2 µA 1 µA 6 µA	 30 µA 1 µA 12 µA
RAM Size	32 x 4	656 x 8	–	146 x 160	–	80 x 160
Package	QFP, Die	TAB, Die	TAB, Die	TAB, Die	TAB	TAB
Target CPU	General	MC68HC05L10	MC68HC05L11	MC68HC05L11	MC68HC05L11	MC68HC05L11
Special Features	Serial Interface or IIC Bus					

Features	MC141516	MC141518	MC141522	MC141524	MC141562	MC141563
Type	Passive	Passive	Active (TFT)	Active (TFT)	Passive	Passive
Backplane/Common/Row	64	–	120	–	100	–
Segment/Column	–	80	–	120	–	80
MUX Ratio/Duty	1/32 – 1/64	1/32 – 1/64	N/A	N/A	1/100 – 1/300	1/100 – 1/300
Operating Voltage for Internal Circuit V_{DD} (V)	3 or 5	3 or 5	5	5	3 or 5	3 or 5
Voltage for LCD Drive Circuit VLCD (V)	13	13	45	15	28	28
Typical Current Consumption IDD Display Standby ILCD Display	 5 µA 2 µA 8 µA	 20 µA 5 µA 30 µA	 100 µA N/A N/A	 10 mA N/A N/A	 40 µA 300 nA 30 µA	 250 µA 1.5 µA 30 µA
RAM Size	–	64 x 80	–	–	–	–
Package	TQFP, Die	TQFP, Die	TAB	TAB	TAB, Die	TAB, Die
Target CPU	MC68HC05L11	MC68HC05L11	–	–	–	–
Special Features					4-Bit/8-Bit Interface	4-Bit/8-Bit Interface

Features	MC141531	MC141535	MC141532 MC141533	MC141537	MC141539	MC141800A
Type	Passive	Passive	Passive	Passive	Passive	Passive
Backplane/Common/Row	17	17	33	16	32	65
Segment/Column	120	161	120	120	120	128
MUX Ratio/Duty	1/16, 1/17	1/17	1/16, 1/17, 1/32, 1/33	1/16	1/16 or 1/32	Direct to 1/65
Operating Voltage for Internal Circuit V_{DD} (V)	2.4 – 3.5	2.4 – 3.5	2.4 – 3.5	2.4 – 3.5	2.4 – 3.5	2.4 – 3.5
Voltage for LCD Drive Circuit VLCD (V)	10.5	10.5	10.5	10.5	10.5	16.5
Typical Current Consumption IDD Display Standby ILCD Display	 75 µA 300 nA 6 µA	 70 µA 300 nA 6 µA	 80 µA 300 nA 6 µA	 70 µA 300 nA 6 µA	 76 µA 300 nA 6 µA	 TBD TBD TBD
RAM Size	17 x 120	17 x 161	33 x 120	16 x 120	32 x 120	65 x 128
Package	TAB, Gold Bump Die	TAB, Gold Bump Die	TAB, Gold Bump Die	TAB, Bare Die	TAB	TAB, Gold Bump Die
Target CPU	General	General	General	General	General	General
Special Features	3 Annunciators, On-Chip DC-DC, Temp. Compensation, Contrast Control, Low-Power Icon	4 Annunciators, On-Chip DC-DC, Temp. Compensation, Contrast Control, Horizontal Scrolling, Low-Power Icon	4 Annunciators, On-Chip DC-DC, Temp. Compensation, Contrast Control, Low-Power Icon	3 Annunciators, On-Chip DC-DC, Temp. Compensation, Contrast Control	4 Annunciators, On-Chip DC-DC, Temp. Compensation, Contrast Control	IIC, SPI, Parallel Interface, On-Chip DC-DC, Temp. Compensation, Contrast Control, Low-Power Icon

MC14153X Series Comparison Table

Features	MC141531	MC141532	MC141533	MC141535	MC141537	MC141539
Max. Display Size	120 x 17	120 x 33	120 x 33	161 x 17	120 x 16	120 x 32
Supply V_{DD}	2.4 – 3.5 V					
Standby Mode Current	Less than 500 nA					
On-Chip DC-DC Converter	2x/3x					
Bias Voltage Generator	On-Chip					
Static Icon	3	4	4	4	3	4
Low-Power Icon Mode	Yes				No	
MUX Ratio	1/16, 1/17	1/16, 1/17, 1/32, 1/33		1/17	1/16	1/16, 1/32
Graphic Display Data RAM	Yes					
Vertical Scrolling	Yes					
Row/Column Remap	Yes					
Master Clear RAM	Yes					
Internal Contrast Control	16 Levels					
External Contrast Control	Yes					
Temperature Compensation	Yes					
Other Features	–	–	Split Common Output	Horizontal Scrolling	–	–
Package	70 mm TAB, Gold Bump Die				35 mm TAB, Bare Die	35 mm TAB

Monitor On-Screen Device Technical Selection Guide

Features	ES Series		AG Series	
	EMOSD Enhance MC141541	**SMOSD Super MC141548/9**	**AMOSD2 Advance MC141546/7**	**GMOSD Graphic MC141542/5**
Display Area	10R x 24C	15R x 30C	15R x 30C	15R x 30C
Color	8	8	8	8
Intensity	High	High/Low	High/Low	High/Low
Windows	3	4	4	4
No. of Characters	128	256	128	256
ROM	120	248	128	288
Mask ROM	**Yes**	**Yes**	**Yes**	**Yes**
Character RAM	**8**	**8**	0	0
Font Matrix	10 x 16	10 x 16	12 x 18	12 x 18
Resolution	EGA	VGA	**SVGA**	**SVGA**
Max. Dot Clock	52.8 MHz	76.8 MHz	92.2 MHz	92.2 MHz
Max. Frequency	110 kHz	120 kHz	120 kHz	120 kHz
ROM-DAC Integration	0	12	12	12
16 DIP, 0 ROM DAC	MC141541P	MC141549P	MC141547P2	MC141545P2
24 DIP, 8 ROM DAC	N/A	MC141548P	MC141546P2	MC141542P2
28 SOIC, 12 ROM DAC	N/A	Custom	Custom	Custom
Special Display Features	Double Height, Double Width, Shadowing, Bordering, 3 Windows	EMOSD Plus: **4 Windows, Windows Shadow, Blinking, Fade-In/Fade-Out, Automatic Height, Icon Intensity, Windows Intensity**	Double Height, Double Width, Shadowing, Bordering, 4 Windows, **Spacing Control, Windows Intensity**	AMOSD2 Plus: **16 Multicolor Font, Color Background, Windows Shadow, Blinking, Fade-In/ Fade-Out, Icon Intensity, Display Clear**
Data Sheet	MC141541/D	MC141548/D	MC141546/D	MC141542/D
Evaluation Kit	MC141541EVK	MC141548EVK	MC141546EVK	MC141542EVK

Part Number Ordering Information

TAB Package

MC141XXX A TX R

1 — 1XXX; 2 — A; 3 — TX; 4 — R

Die

MCC14XXXX Z

5 — C; 1 — XXXX; 6 — Z

Other Packages

MC14XXXX XX

1 — XXXX; 7 — XX

Item	Definition	Representation	Sequence	Notes
1	Four-digit numeral	One particular display IC	1500 – 1599 1800 – 1899 5000 – 5009	
2	One alpha character	Derivative of a particular IC, corresponding to the numeral defined in Item 1	Alphabetical order	Only for derivatives; no such character for original design
3	The letter "T" followed by a one-digit numeral	Device in TAB package	T, T1, T2 ...	No T0 exists
4	The letter "R"	Reel size	With or without "R"	With "R" — 405 mm reel diameter; Without "R" — 330 mm reel diameter
5	The letter "C" or the letter "W"	Device in die form	"C" or "W"	"C" — Die shipped in chip carrier; "W" — Die shipped in wafer form
6	The letter "Z"	Device sold in gold bump die/bare die form	With or without "Z"	With "Z" — Gold bump die; Without "Z" — Bare die
7	One or two alpha character(s)	Package form	"P", "DW", "FU", or "FJ"	"P" — Plastic Dual In-Line Package; "DW" — Small Outline Gull-Wing Package; "FU" — Quad Flat Package; "FJ" — Thin Quad Flat Package

General Information 2

RELIABILITY AND QUALITY ASSURANCE

Prepared by: KY Cheng/Fei Wong
Motorola Semiconductor Hong Kong Ltd

1. Quality Mission

1.1 Quality Policy

"It is the policy of the Motorola Semiconductor Products Sector to produce products and provide services exactly according to CUSTOMER expectations, specifications and delivery schedule. Our system is based on prevention using statistical process control. The standard is a Six Sigma level of error-free performance. These results come from the participative efforts of each employee in conjunction with supportive participation from all levels of management."

1.2 Reliability and Quality Monitor Philosophy

In order to guarantee that the high standards of reliability and quality required by Motorola are met, an ongoing Reliability Audit Program has been established.

Individual product and package monitors are generally developed by identifying a process driver device (in most cases the same device used to qualify a process / product / package family). Once the process driver device is identified, the appropriate stress test programs are put in place to adequately monitor the ongoing process average of the specific family. This process average measurement is made by understanding the reliability and quality results of individual samples from production material. These samples are pulled at the outgoing QA gate portion of the production flow, then randomly sourced into specified reliability tests. These tests include Early Fail Studies, Dynamic Long Term Lifetest (which includes Read and Record Parametric Characterization Samples), Temperature Humidity Bias (THB), Highly Accelerated Stress Test (HAST), and Temperature Cycle, as well as preconditioning stress testing on plastic surface mount packaging technology.

Monitor testing is completed on an ongoing cycle. Test results are subsequently made available quarterly. This report details all test results received for the entire year, outlining the reliability data associated with all process / package family types.

With all of this data, an effective ongoing monitoring method is established which is capable of identifying reliability trends associated with all process / product / package families.

2. Supreme Quality and Reliability

2.1 Quality is defined as:

- Reduction of variability around a target so that conformance to customer requirements and expectations can be achieved in a cost-effective way.
- The probability that a device (equipment, parts) will have performance characteristics within specified limits.
- Fitness for use.

2.2 Reliability is defined as:

- Quality in time and environment (temperature, voltage, etc.).
- The probability that a semiconductor device, which initially has satisfactory performance, will continue to perform its intended function for a given time under actual usage environments.

2.3 Monitorable Reliability and Quality Assurance Program

It is a program to generate on-going data for both reliability and quality for the various product families. Both reliability and quality monitors are performed on the different major categories of semiconductor products. These monitors are designed to test the product's design and material as well as to identify and eliminate potential failure mechanisms to ensure reliable device performance in a "real world" application. Thus, the primary purpose of the program is to identify trends from the data generated, so that if need be, corrective action(s) can be taken toward improved performance. In addition, this reliability and quality data can be utilized by our customers for failure rate predictions.

2.4 Superior Design for Reliability and Quality

Motorola has always stressed reliability and quality considerations in designing any new product. Superior designs with conservative design rules will mean a trouble-free product in the field.

The following rules and guidelines are applied by the various groups to achieve the required reliability and quality goals:

- Testability is a key consideration in new designs.
- Minimum levels of input protection (ESD) are required.
- Minimum levels of latch up protection are required.
- Stress relief design rules have been incorporated in all new large die designs to reduce the effects of package-induced stress.
- All design work is based on simulation across the processing window.
- On future designs the number of bootstrap nodes greater than V_{DD} will be reduced to a minimum to reduce the high E field effect across the new thinner gate oxides.
- Guidelines have been enacted to reduce the effects of hot carrier injection.
- Guidelines have been enacted for maximum current density allowed in metal lines, contacts, and vials to eliminate electromigration concerns.

3. Invincible Quality Assurance System

3.1 Quality Assurance Function at the Development Stage

Excellent quality and reliability of a semiconductor device is determined at the fundamental design stage. In order to assure product quality, design review and reliability tests are performed on prototypes to eliminate design and pilot run problems. While attaining the desired quality and reliability, the process also provides design and process information for future improvement. (See Figure 1.)

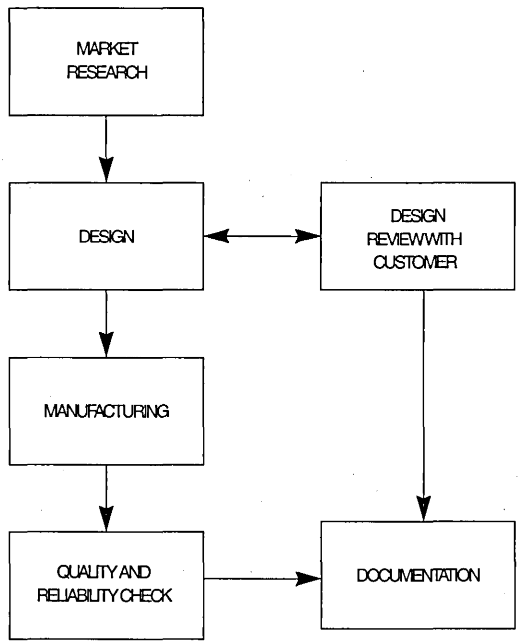

Figure 1. Development Stage Flow Chart

3.2 Quality Assurance in Mass Production

To achieve Motorola's quality objectives, the assurance of product quality is shared among various departments, including the quality department, the manufacturing department, and the test operation department. Each department plays a unique and important role during production, as shown in Figure 2. Key elements including control of material purchasing, manufacturing process, final product control, and an on-going reliability monitoring program are described in this section.

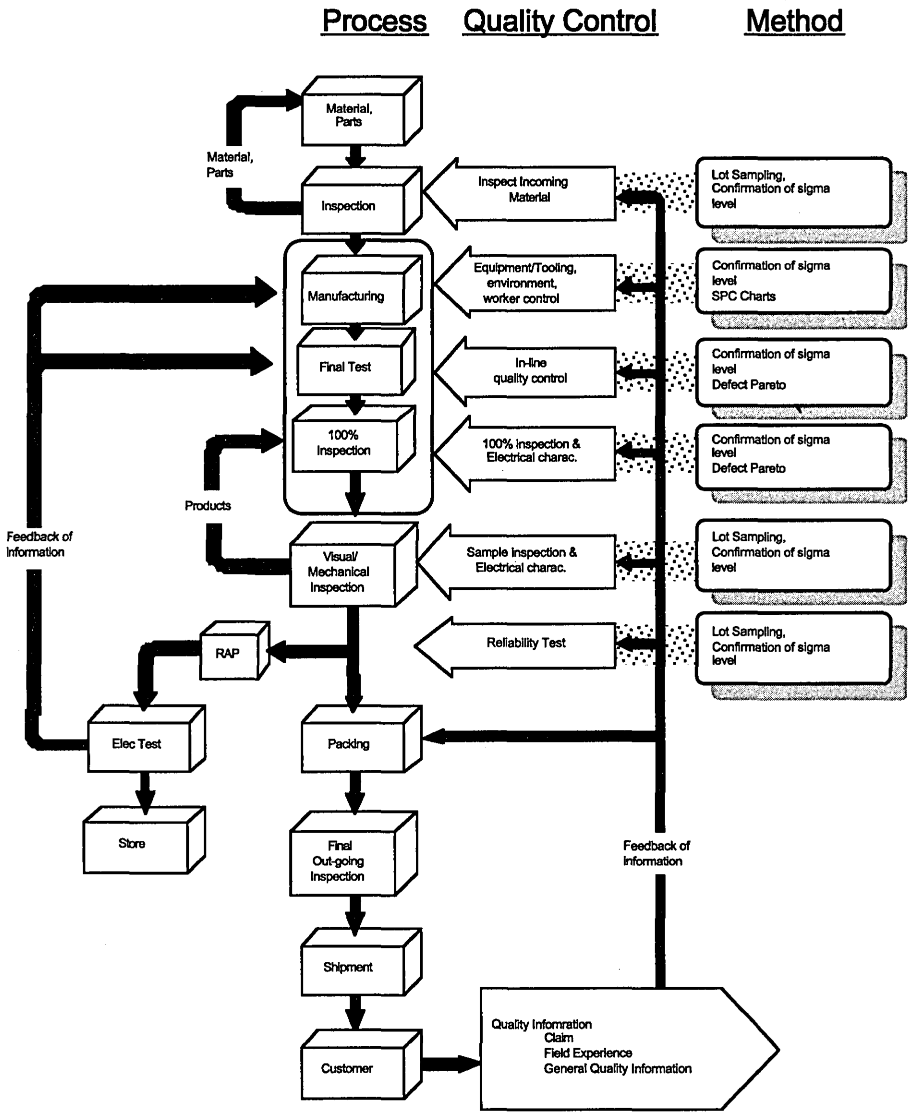

Figure 2. Mass Production Quality Flow Chart

3.2.1. Control of Material Purchasing

In order to maintain and improve the product quality and reliability, the control of materials and parts for manufacturing purpose is essential. The key activities include not only incoming inspection, but also the ensuring of supplier quality systems maintained at levels capable of meeting Motorola's prime objectives of Total Customer Satisfaction and Six Sigma quality. The incoming inspection and sampling method is performed based on Motorola's specifications and drawings.

The other activities of quality assurance are as follows:
1. Qualification and guidance of supplier.
2. Supplier quality system audit.
3. Physical and chemical analysis and test.
4. Technical co-operation with supplier.

Typical checkpoints of materials are shown in the following table.

Material	**Properties**	**Critical Items**
Wafer	Appearance	Damage and contamination, gold bump
TAB Tape	Appearance Dimension Plating Layer	Contamination, scratch, bend, twist All critical dimensions Solderability
Encapsulant	Composition Electrical Characteristics Thermal Characteristics Viscosity	Characteristics of plastic material

3.2.2. Control of the Manufacturing Process

The control of the manufacturing process plays a very important role in quality assurance of the semiconductor devices. This includes the control of in-process and final products, manufacturing equipment and facilities, measuring and inspection equipment, as well as the manufacturing environment. The process control plan in manufacturing is shown in Figure 3. In short, the elements in the manufacturing process control include:

- Prevention and detection of quality problems.
- Continuous improvement in quality.
- Maintenance and improvement of yield.
- Education and on-site training of technical assistants (operators).
- Communication and review of quality information.
- Condition control on equipment and operator.

	OPERATION	CHARACTERISTIC AFFECTED	ANALYSIS METHOD
ASSEMBLY	Recieve Wafer		
	Film & Wafer Mount	Assy Defects	
	Wafer Saw	Assy Defects Wafer Visual Defects	N-P Chart
TAB Tape	Saw Monitor	Resistivity, Bacteria Count Kerf Width	XBar-R
	Inner Lead Bond	Assy Process, Inner Lead Bonding Visual Defects	N-P Chart
	Lead Bond Monitor	Lead Pull	XBar-S
	QA Gate Visual	Wafer/Bonding Visual Defects	
Encapsulant	Encapsulation	Assy Process, Encapsulant Visual Defect	N-P Chart
	Marking	Assy Process, Marking Visual Defects	N-P Chart
	Encapsulant Cure	Assy Process, Marking/Encapsulant Visual Defects	
	QA Gate Visual	Visual Defects, Marking Permanency	Visual 25X Alpha 2100/2110 Test
FINAL TEST	Package Mark Check	Visual Defects	
	Room Temp Test	Electrical Test	Function Test
	QA Gate Inline (Test Temp: RM)	Electrical Test	Function Test Q Program
	Yield Check	Electrical Test	Test Yield
	100% Visual Inspection	Visual Defects	Visual 25X
	QA Gate Visual	Visual Defects	Visual 25X
	Vaccum Pack & Label		
	QA Gate Visual		
	Ship to Warehouse		

Figure 3. Process Control for TAB Package

3.2.3. Control of In-Process and Final Product

With the aim of "Do It Right the First Time" and achieving Six Sigma quality, the semi-final and final product are tightly controlled throughout the manufacturing process. Checkpoints are set up in each manufacturing step, and 100% inspection and screening are executed according to the checkpoints. Product should not be proceeded to the next step if potential failure is found. The potential failure should be removed by the approach of analysis by root cause. An on-going reliability monitoring program is used to monitor the reliability of devices.

3.2.4. Control of Equipment and Facilities

The equipment and facilities developed for semiconductor manufacturing are high performance devices, and they are important in maintaining and improving the process capability. At Motorola, automation equipment is applied in most areas to keep the process variation in the lowest level. All the equipment is maintained on a preventive basis. A periodical preventive maintenance (PM) is carried out for individual equipment. At the PM, the checkpoints listed are checked one by one to avoid any omission. In order to ensure that the manufacturing equipment is under control, statistical process control (SPC) charts are applied. For the measurement and inspection equipment, a periodical calibration scheme is executed to ensure the accuracy, repeatability, and reproducibility.

3.2.5. Control of the Manufacturing Environment

The manufacturing environment (i.e., temperature, humidity and dust) also greatly affects the product quality; therefore, it is controlled as strictly as the other two factors. A periodical process audit is applied to ensure that the environment is in good condition. The prevention of Electrostatic Discharge (ESD) is also a key element in the environment control. Equipment ESD status, clothes, packaging materials, and all the critical points in the manufacturing process are given close attention for ESD protection.

3.2.6. Control of Final Product

After the device has been judged 100% good in test, sampling inspection for electrical characteristics and visual mechanical inspection is carried out by the reliability and quality assurance department. The purpose is to confirm that the product is meeting the customer's expectation, as well as to unmask the potential problems hidden in the manufacturing process. The sampling plan is based on the objective of meeting Six Sigma quality and beyond.

3.2.7. On-Going Reliability Monitoring Program

A reliability audit program (RAP) is executed on the final product to ensure the reliability of the device. Stress tests such as Burn In (B/I), Pressure Temperature and Humidity (PTH), Temperature Cycle (T/C), etc., are done periodically.

4. Innovative Reliability Design

4.1 Reliability Measure

Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period. In other words, reliability is quality over time and environmental conditions. The most frequently used reliability measure for semiconductor devices is the failure rate (λ). The failure rate is obtained by dividing the number of failures observed by the product of the number of devices on test and the interval in hours, usually expressed as percent per thousand hours or failures per billion device hours (FITS). This is called a point estimate because it is obtained from observations on a portion (sample) of the population of devices.

4.2 Reliability Model

To project from the sample to the population in general, one must establish confidence intervals. The application of confidence intervals is a statement of how "confident" one is that the sample failure rate approximates that for the population. To obtain failure rates at different confidence levels, it is necessary to make use of specific probability distributions. The chi-square ($\chi 2$) distribution that relates observed and expected frequencies of an event is frequently used to establish confidence intervals. The relationship between failure rate and the chi-square distribution is as follows:

$$\lambda = \frac{\chi 2\,(\alpha,\ \mathrm{d.f.})}{2t}$$

where:

λ = failure rate

$\chi 2$ = chi-square function

α = (100 – confidence level) / 100

d.f. = degrees of freedom = 2r + 2

r = number of failures

t = device hours

The failure rate of semiconductor devices is inherently low. As a result, the industry uses a technique called accelerated testing to assess the reliability of semiconductors. During accelerated tests, elevated stresses are used to produce, in a short period, the same failure mechanisms as would be observed under normal use conditions. The objective of this testing is to identify these failure mechanisms and eliminate them as a cause of failure during the useful life of the product.

Temperature, relative humidity, and voltage are the most frequently used stresses during accelerated testing. Their relationship to failure rates has been shown to follow an Eyring type of equation of the form:

$$\lambda = A\ \exp(\phi/kT) \bullet \exp(B/RH) \bullet \exp(CE)$$

where A, B, C, ϕ, and k are constants, more specifically B, C, and ϕ are numbers representing the apparent energy at which various failure mechanisms occur. These are called activation energies. T is the temperature, RH is the relative humidity, and E is the electric field.

The most familiar form of this equation deals with the first exponential term which shows an Arrhenius type relationship of the failure rate versus the junction temperature of semiconductors. The junction temperature is related to the ambient temperature through the thermal resistance and power dissipation. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then by applying known acceleration factors, estimate the failure rates for lower junction temperatures.

Arrhenius type of equation:

$$\lambda = A\ \exp\frac{\phi}{kT}$$

where:

λ = failure rate
A = constant
$\varepsilon = 2.72$
ϕ = activation energy, eV
k = Boltzman's constant, 8.62×10^{-5} eV/°K
T = temperature in degrees Kelvin (T_J°C + 273.15)

Temperature acceleration factors for a particular failure mechanism can be expressed as the ratio of the failure rates at two different levels of stress:

$$Fa = \exp(\phi/k) \bullet \frac{1}{Tr} - \frac{1}{Tt}$$

where:

Fa = acceleration factor
ϕ = activation energy
k = Boltzman's constant, 8.62×10^{-5} e/V/°K
Tr = junction temperature, °K at the rated ambient temperature
Tt = junction temperature, °K at the life test ambient temperature

4.3 Reliability Tests

The following summary briefly describes the various reliability tests included in the Motorola reliability monitor program.

Dynamic Early Fail Study

This stress is performed to accelerate infant mortality failure mechanisms, which are defects that occur within the first year of normal device operation. Typical stress is a temperature of 125°C, nominal voltage (6 V), and a duration of 24 or 48 hours. All devices used in this test are sampled directly after the standard production final test flow with no prior burn-in or other prescreening, unless called out in the normal production flow.

Dynamic Long Term Lifetest

Dynamic Long Term Lifetest is performed to accelerate failure mechanisms and access parametric shifts, which are voltage and thermally activated. This is done through the application of extreme temperatures and the use of biased operating conditions. Typical stress temperature is 125°C with the bias applied being equal to or greater than the data sheet nominal value. Testing is performed with dynamic signals applied to the devices for a test duration of 1008 hours.

Temperature Cycle

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of – 65°C to + 150°C for a duration of 500 or 1000 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperature.

Temperature Humidity Bias (THB)

This is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization. Typical stress duration is 1008 hours.

Highly Accelerated Stress Test (HAST)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions employed during this test are a temperature of 130°C, humidity of 85%, 33.5 psia, and a nominal static bias voltage. Typical stress duration is 72 hours.

SMT Preconditioning Stress

The purpose of this test is to simulate the shipping, storage, and solder attach steps involved in mounting and reworking a surface mount device. The preconditioning flow begins with ten temperature cycles (– 65/150°C) and is followed by a moisture soak. The soak may involve simulating a worst case “no Dry Pack” condition in an 85°C/85% RH environment, a worst case Dry Pack condition of 85°C/60% RH, or a typical manufacturing environment condition of 30°C/60% RH. The duration of the moisture condition will vary depending on the moisture level tested. Moisture exposure is followed by multiple passes of vapor phase reflow (215°C) for 120 seconds per pass.

Autoclave

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 240 hours.

Data Retention

Data retention testing or high temperature storage is performed to measure the stability of the programmed EPROM and EEPROM devices during storage at elevated temperatures with no electrical stress applied. The devices are exposed to an ambient of 150°C. An acceleration of charge loss from the storage cell is the expected result. All groups are typically tested to 1008 hours.

EEPROM Write/Erase Cycling

The Write/Erase endurance test measures EEPROM cell operation over an expected life time. All cells are alternately cycled for a minimum of 10,000 cycles between an erased state "1" and a write state "0" at the device high temperature specification of 85°C (some samples are cycled at higher temperatures).

4.4 Reliability Data

The following summary gives a brief description of the various reliability tests included in qualifying and reliability monitoring of LCD drivers.

Operating Life Test, Ea = 0.7eV

Device	Package	Test Condition	Sample Size	Failure
MC141511	128ld QFP	125°C, Bias, 1008hrs	45	0
MC141512	91ld TAB	125°C, Bias, 1008hrs	45	0
MC141514	186ld TAB	125°C, Bias, 1008hrs	45	0

Temperature Cycle

Device	Package	Test Condition	Sample Size	Failure
MC141511	128ld QFP/ 159ld TAB	-65°C to +150°C, 100 cyc	80	0
MC141512	91ld TAB	-65°C to +150°C, 100 cyc	80	0
MC141514	186ld TAB	-65°C to +150°C, 100 cyc	80	0

Temperature Humidity Bias

Device	Package	Test Condition	Sample Size	Failure
MC141512	91ld TAB	85°C/85%RH, 1008hrs	45	0
MC141514	186ld TAB	85°C/85%RH, 1008hrs	45	0

Pressure Temperature Humidity (PTH, Autoclave)

Device	Package	Test Condition	Sample Size	Failure
MC141511	159ld TAB	121°C, 100%RH, 30 PSIA	45	0
MC141512	91ld TAB	121°C, 100%RH, 30 PSIA	45	0
MC141514	186ld TAB	121°C, 100%RH, 30 PSIA	45	0

5. Responsible Field Service

5.1 Mission

Provide "On the Spot" quality professionals to work with our customers to describe our quality initiatives, assist in the resolution of quality problems, and to be proactive in seeking ways to provide total customer satisfaction. Provide technical assistance to our field and headquarters people in developing methods to obtain Six Sigma quality in everything we do. Facilitate cycle time improvements in all processes and procedures in world marketing.

5.2 Responsibilities to the Customer

- Call on all customer departments/organizations in the assigned region to provide resolution of any quality problems discovered or perceived.
- Work with the customer to understand their quality requirements and vendor rating systems and then establish Motorola procedures in our sales and factory organizations to serve our customers' needs and improve our ratings.
- Act as a quality consultant in the field to facilitate the training and implementation of administrative quality systems and programs.

5.3 Measurement

- Overall quality rating improvement with customers.
- Implementation of quality systems that measure and track continuous improvements in quality and reliability of our products and services.
- Reduction in customer returns for administrative quality reasons.
- Support the factory in efforts to provide Total Customer Satisfaction.
- World marketing attention to the "Speed Imperative."

5.4 Field Service Flow

Figure 4 demonstrates Motorola's field service process. As part of the Total Customer Satisfaction (TCS) team, the quality department serves as a medium between sales/field quality and the TCS team for all technical and quality issue support. He or she also acts as a leading function to resolve all quality problems upon customer complaint. Customers can also go through marketers for any inquiry which will be replied to by an active member of the TCS team.

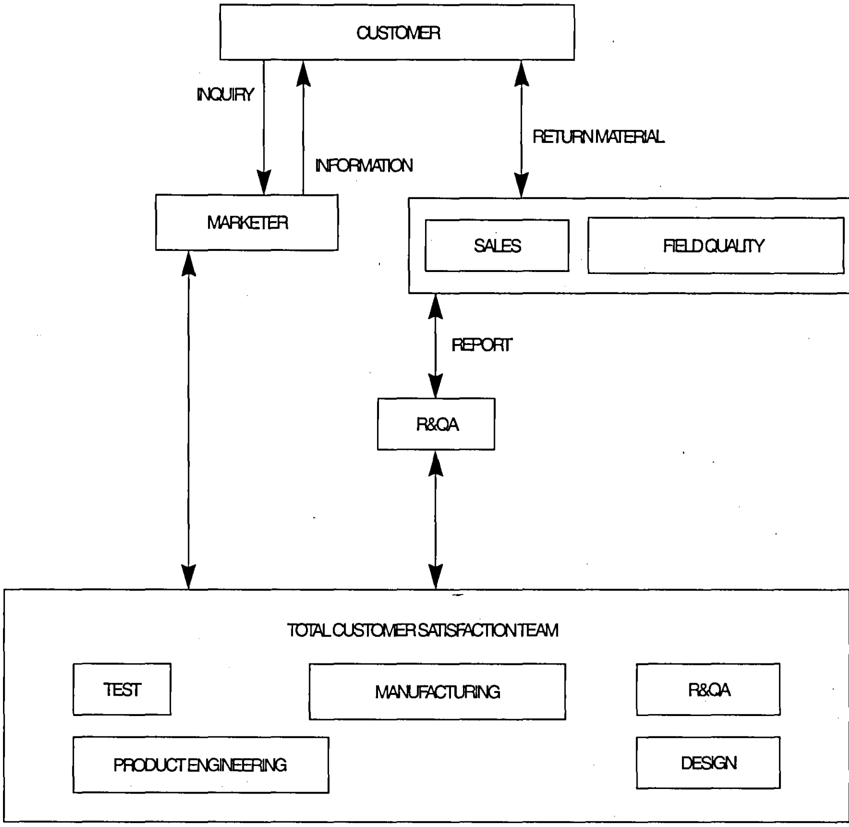

Figure 4. Field Service Process Flow Chart

TAB PACKAGE FOR LCD DRIVER

By O.L. Chau
Motorola Semiconductors Hong Kong Ltd.

Today most products use liquid crystal displays (LCD) for the user interface. The advantage of LCD lies in its small volumetric profile which offers tremendous space saving over cathode ray tube (CRT) display. It has become an increasingly important substitute for CRTs. The proliferation of notebook computers and other portable electronic products have also accelerated the use of LCDs at an incredible rate. As the LCD resolution and capacity increase, more LCD drivers are needed. However, the increase in LCD driving requirement should not offset the advantage of LCD, i.e. slim profile. Therefore, a good choice of LCD driver package should feature high pin count, small form size and cost effectiveness. For such an application, Tape Automated Bonding (TAB) package has been successfully developed as the most preferred package for LCD driver application.

INTRODUCTION TO TAB PACKAGING

A typical TAB package is shown in Fig. 1. The layout is specially designed to meet the application for LCD driver. One side of the package are the output leads for LCD panel terminal connection. These are fine pitch leads to match LCD panel terminal pitch, typical pitch is between 0.07mm to 0.35mm. The opposite side are the input leads for soldering connection to the PCB. The input leads pitch are usually made wide enough for easy alignment, typical pitch is between 0.5mm to 1.2mm. The overall package thickness is around 0.8mm.

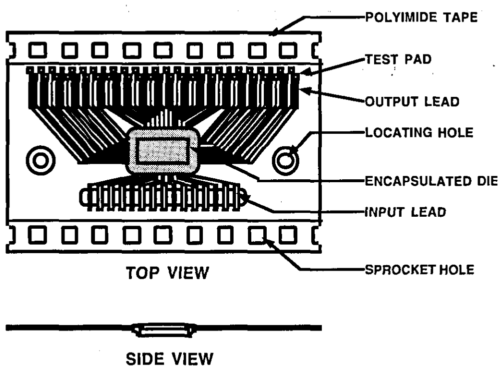

Figure 1. TAB package for LCD driver

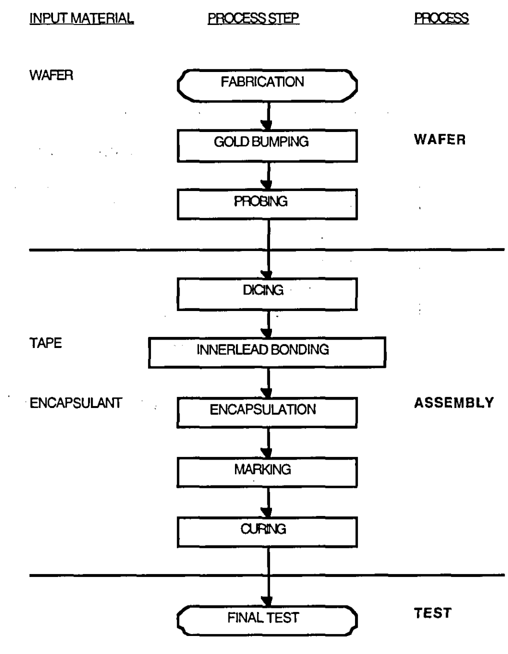

Figure 2. TAB packaging process flow

Fig. 2 shows the TAB packaging process. Instead of using wire bond technology for the inner lead bonding, TAB uses gold bumps to form the connection. Gold bumps are deposited on the bonding pads after wafer fabrication. Several types of bump shape are possible. See Fig. 3.

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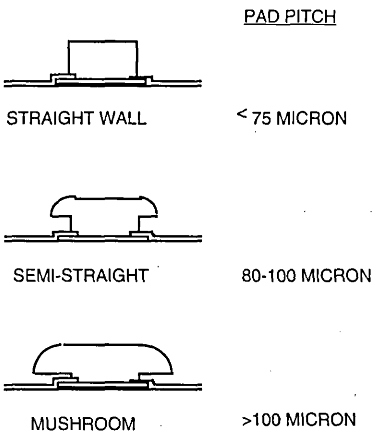


Figure 3. Gold bump shapes

Formation of high reliability gold bumps requires a well controlled series of processes. Motorola uses a proprietary gold bump process to precisely control the bump dimensions so that the straight wall bumps as shown in Fig. 4 can be achieved. With straight wall bumps, bond pads can be placed at closer pitch and the die size can be further reduced.

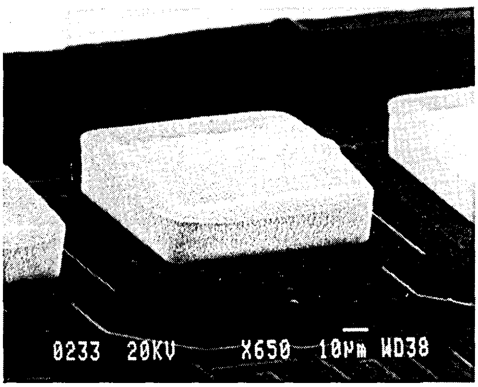


Figure 4. Motorola straight wall bump

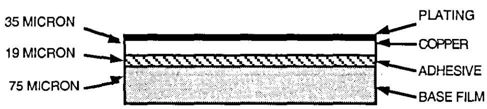


Figure 5. Construction of 3-layer tape

The inexpensive 3-layer tape construction is the usual choice for LCD driver TAB. The 3-layer tape structure consists of a conductive copper foil which is laminated to a polyimide based film using an adhesive. See Fig. 5. With photo-imaging and etching processes, a conductive pattern on the tape is defined to form the interconnection circuitry. The pattern can be designed to match the terminal connection on LCD panel and PCB. Fig. 6 shows the outline of a TAB tape specially designed for LCD driver application.

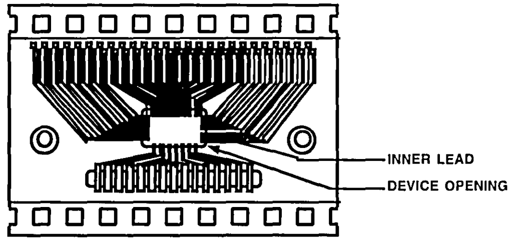


Figure 6. Pattern of a TAB tape

The most common method to connect the tape leads to the gold bumps is by means of a gang bonder. The gang bonder bonds all the leads onto the bumps simultaneously using a thermal compression bonding which provides a strong and reliable mechanical joint. See Fig. 7. Alternatively, the single point bonder can also be used to bond the lead one at a time using thermosonic or laser-based bonding. However, for volume production, the gang bonding is still the most efficient bonding method. After the inner lead bonding, a thin layer of encapsulant is dispensed onto the top surface to provide a protective coating for the chip. The encapsulant is then partially cured in the encapsulator to facilitate handling and marking. At completion of a reel of tape, the reel is transferred to an oven for final cure of the encapsulant. Fig. 8 shows the inner lead gang bonding and encapsulation process for the TAB package.

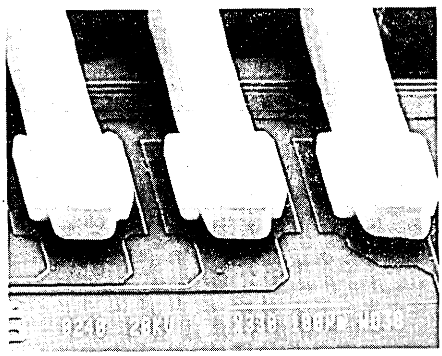


Figure 7. Gang bonded inner leads

PACKAGING REQUIREMENT OF LCD DRIVER

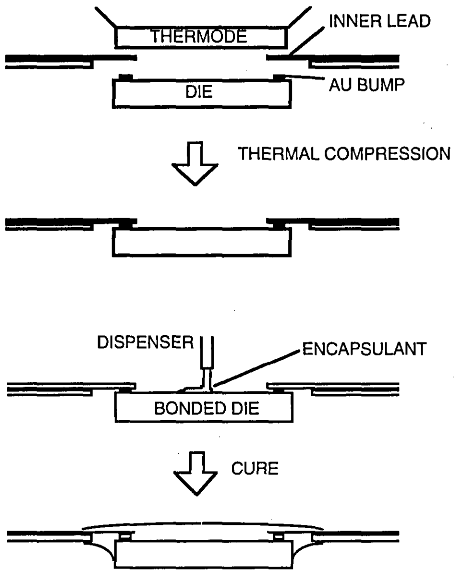


Figure 8. Inner lead bonding and encapsulation

As the display density increases, more driver chips per LCD module are needed and more I/O connections have to be made. Figure 9 shows a typical requirement for the 10" LCD panels. It indicates that use of low pin count chip is impractical. The challenges of building a LCD module are (i) how to accommodate a large number of high pin count chip in a limited mounting area, and (ii) how to connect the large number of terminals on LCD to PCB reliably.

The following are common methods used in the industry to connect the LCD panel to the PCB. See Fig. 10.

(1) Elastomeric connector
Conductive elements are sandwiched between either spongy or solid silicone rubber which is at least 3.5mm thick. By making the pitch sufficiently small, conducting terminals on each surface can be connected through redundant contacts. Silicone rubber is stable and resistant to harsh environmental conditions. However, a permanent clamp frame is required to apply contact pressure, and variation across the length of the rubber has a negative effect on the electrical integrity. Long term contact reliability is also subject to stress relaxation of the silicone rubber in the connection. Connection pitch is usually limited to above 0.4mm.

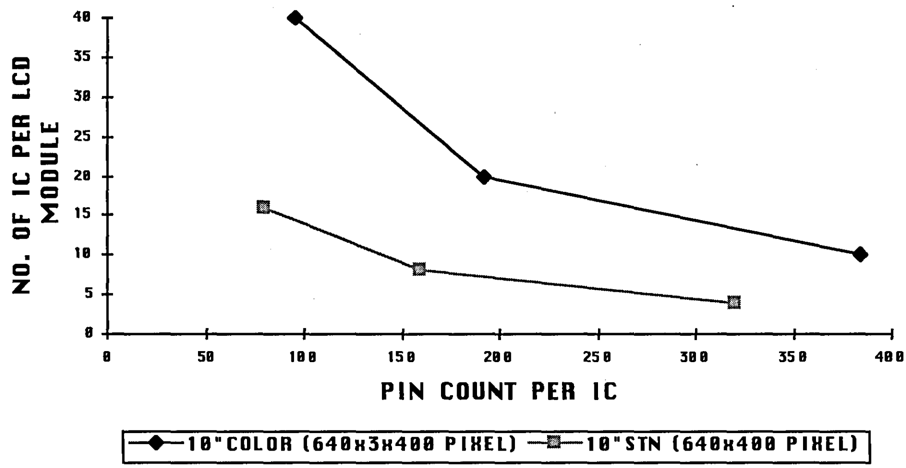


Figure 9. LCD driver requirement

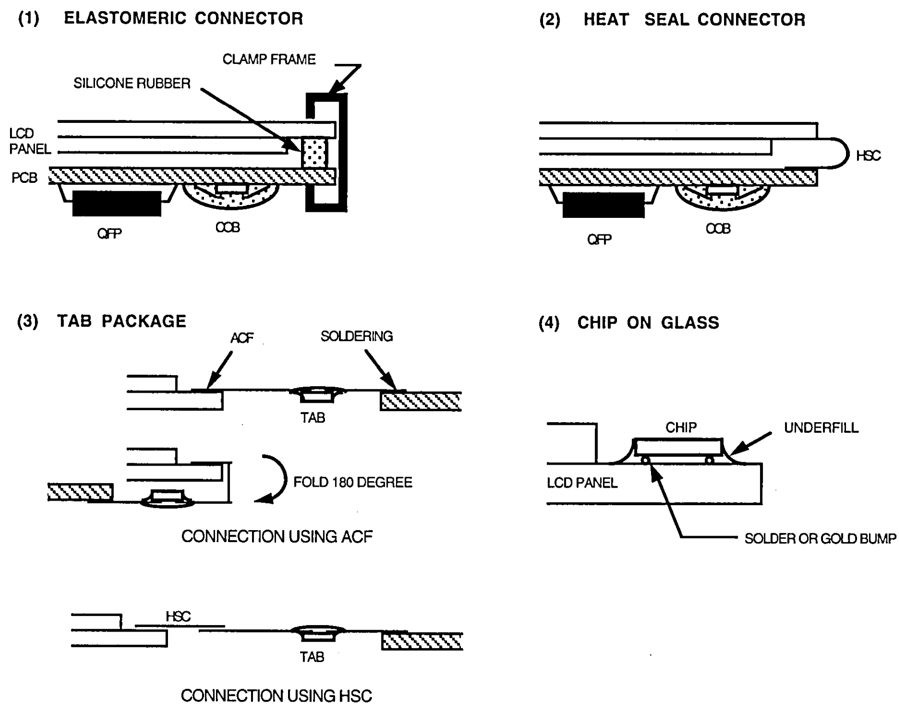


Figure 10. LCD panel terminals connection methods

QFP package is a popular option for the driver chips. The conventional SMT process is a simple process with good cost performance. Use of QFP means that batch reflow soldering with other components is possible. However, for high performance LCD panels, the lead count of the LCD driver is typically around 200. That will require use of a 208 leads QFP package with 0.5mm outer lead pitch. The 208 leads QFP is now a giant 28x28mm package which is almost impossible to be accommodated inside the limited space of a compact product. If outer lead pitch is reduced to below 0.5mm in order to shrink package size, problems with screen printing and solder reflow will require alternative methods of solder application and reflow technique.

Chip on Board (COB) is another popular option for the driver chips. In COB, the bare chip is directly mounted onto the PCB. The signal connection is done via wire bonding. A glob-top coating is generally used for protection of the wire bonded chip. This method used to provide a low cost solution for low lead count devices. However, for high lead count LCD drivers, COB consumes a large fanout area in order to facilitate wire bonding. Unfortunately, a compact product has a very limited PCB area which is to be shared by many other components. In addition, the bonding pad pitch of a high lead count device is usually made as close as possible to save chip cost. With finer pad pitch, more wires and longer wire length, COB would now suffer a higher assembly yield loss.

(2) Heat seal connector (HSC)
HSC is commonly used in small LCD panel for electronic calculators and organizers. It consists of conductive pastes and dielectric thermoset adhesives. The driver chips are mounted to PCB in the same way as the elastomeric connector, i.e. QFP package or COB. HSC is reliable, dimensionally accurate and versatile. However, it is relatively expensive at small pitch even though the pitch can get down to 0.2mm from the latest development. In addition, it will be too messy when applied to a medium or large size LCD panel which requires many drivers and connections.

(3) TAB
In TAB package, the driver chip is packaged into a tape film which provides a high degree of flexibility like a flexible printed circuit (FPC). The tape film can be used as the connector between the LCD panel and the PCB. Anisotropic Conductive Film (ACF) is commercially available for this application. This direct connection method simplifies the

manufacturing process and the end product design. Today most of the large LCD panels in the market use TAB package to serve the dual role of driver and connector. TAB package may also be used in conjunction with HSC for a more flexible connection layout.

(4) Chip on glass (COG)
In COG, the chip is directly mounted onto the LCD panel using a flip chip mounting process. COG offers the smallest form factor which is not possible with packaged chip. Many industry observers predict that COG technology is the trend for LCD driver. However, the trade-off is in terms of cost, yield and reliability issues. It is difficult to do full functional testing and burn-in at the component level. The known good die (KGD) is therefore a well known issue for direct chip mounting process. At present moment, application of COG is limited to medium size panel and matured LCD driver product.

ADVANTAGES OF TAB PACKAGE

Out of the different connection methods, TAB package has appeared to be the best choice for LCD driver. This fact can be evidented from its wide application in most LCD products. The advantages of using TAB package can be summarized as follows:

(1) Slim body profile
The TAB package has a light weight and a thin body profile. These match with the most important characteristics for portable products.

(2) Die size reduction
The main reason to get over this limitation is the cost of silicon. Chip size is very much decided by the lead count, and chip size is proportional to cost. As wire bonding cannot handle pad pitch smaller than 3.0 mil, more and more chips become "pad limited". Use of TAB technology allows closer bonding pad pitch, thus help to reduce chip cost. The following is a comparison of minimum pad pitch requirement between various inner lead bonding technologies.

Innerlead Bonding	Minimum Pad Pitch
TAB	2.0 - 3.0 mil
Wire Bonding (Al wire)	3.0 - 3.5 mil
Wire Bonding (Au wire)	3.5 - 4.0 mil

(3) Flexible connection
TAB package is structured as a thin film and is very flexible. It can be used to form the direct connection between PCB and LCD panel with ACF or HSC. The TAB package virtually does not occupy any space on the PCB. It can be even folded sideway or at the back of the LCD panel to further facilitate space reduction in the product.

(4) Less PCB space consumption
It saves the valuable PCB space and cost since the LCD driver is now an integral part of the PCB/LCD connector.

(5) Simplified manufacturing process
TAB package simplifies the manufacturing process because it combines the mounting of LCD driver and PCB/LCD connection into a single process. Unlike other packages, there is less lead skew or bent lead problem for TAB package. It greatly resolves the handling difficulty for high lead count packages and allows for an automated manufacturing process.

ATTACHMENT OF TAB PACKAGE

There are a number of ways to attach the TAB package. For LCD driver, direct attachment using ACF is very popular. ACF is a high density connecting material serving three purposes at the same time - bonding, conduction and insulation. It is an epoxy based material filled with many tiny conductive particles. The separation between these particles is far enough that they are electrically isolated from each other. Fig. 11 shows the end view of a TAB package, the ACF and a LCD panel ready to be bonded. Heat and pressure are then applied to the parts. Pressure squeezes the excess adhesive out of the conductive path area, leaving deformed conductive particles in close contact with the conductive terminals. The thermoset epoxy hardens under temperature to put the conductive particles in a mechanical bonded state. Conductive particles not in the conductive path do not get compressed and will remain isolated.

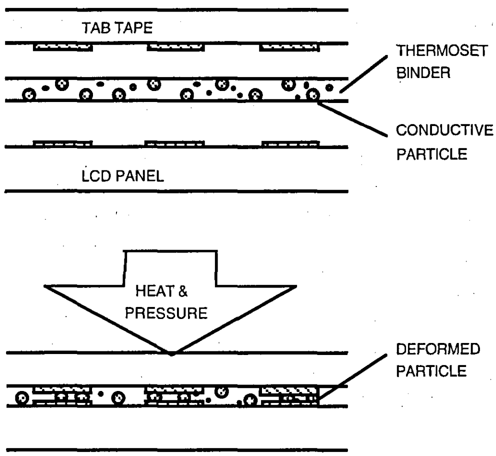


Figure 11. Outer lead bonding using ACF

The application of ACF is simple. Fig. 12 shows the basic steps. After tacking the ACF to LCD panel, the separator on the ACF is removed. Conductive terminals on TAB package and LCD panel are then aligned with vision system. Final sealing is made after more heat and pressure are applied. A number of ACFs are commonly available in the market. Typical minimum connection pitch is 0.15mm to 0.20mm. ACFs with finer connection pitch 0.07mm to 0.10mm are also available from specific suppliers. ACF for COG application at 0.05mm pitch is under development.

Fig. 13 shows the alternative process when HSC is used to bond TAB packages to LCD panel.

For the input leads of the TAB package, the hot bar soldering technique can be applied. The heating tool mechanically presses all the leads down into contact with the PCB connection traces which are usually coated with solder. The solder can be screen printed and reflowed during the precedent SMT process for the other components on the PCB. So flux is needed for soldering with the reflowed solder. Heat is applied to exceed the melting point of the solder. Upon melting the solder, heating is cut off and the solder cools to form the joint. The tool is then lifted and removed from the joint. Sometimes a cooling air jet can be used for faster cooling. As the heating tool is required to follow a pre-programmed heating and cooling sequence, a pulse-heating thermode is preferred for this application.

(1) CLEAN LCD ELECTRODE TERMINALS

(2) TACK ACF

(3) PEEL OFF ACF COVER

(4) ALIGN TAB PACKAGE OUTPUT LEADS TO LCD TERMINALS, APPLY PERMANENT BONDING

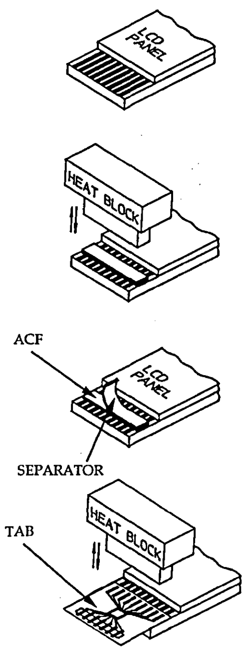


Figure 12. Outer lead bonding using ACF

(1) CLEAN LCD ELECTRODE TERMINALS

(2) ALIGN HSC TO LCD TERMINALS, APPLY BONDING

(3) ALIGN TAB PACKAGE OUTPUT LEADS TO HSC, APPLY BONDING

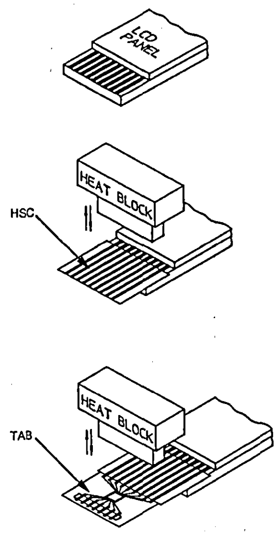


Figure 13. Outer lead bonding using HSC

CUSTOM TAB TAPE DESIGN

TAB tapes are supplied in 35mm, 48mm or 70mm width. They are further classified into STANDARD, WIDE or SUPER format according to size and location of the sprocket holes. The interior area bound by the sprocket holes is the effective user-definable pattern area. The typical dimensions of a 35mm WIDE TAB product is shown in Figure 14. Motorola TAB products use WIDE format which provide an optimum combination of tape handling support and effective pattern area. See Fig. 15.

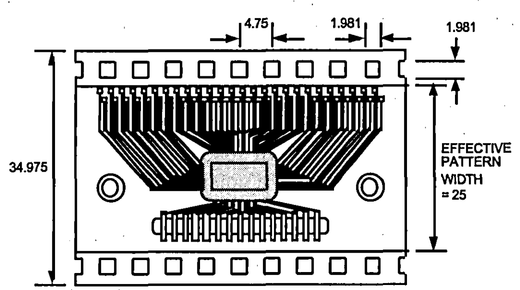


Figure 14. 35mm WIDE format tape

TAPE FORMAT	MAX. A TAPE EFFECTIVE WIDTH	MAX. B TAPE EFFECTIVE LENGTH	MAX. SPROCKET PITCH
35mm WIDE	25.0mm	60.0mm	13
48mm WIDE	38.0mm	66.5mm	15
70mm WIDE	59.0mm	66.5mm	15

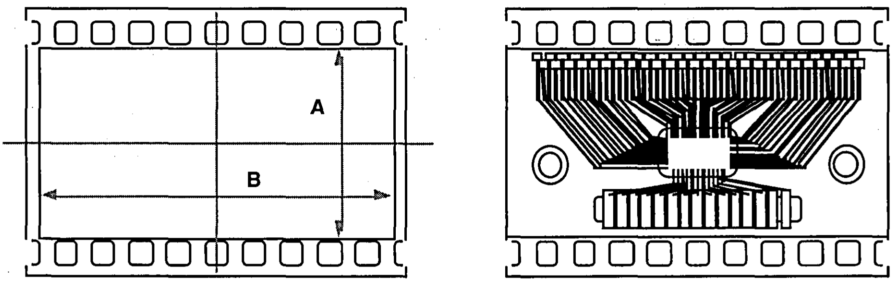


Figure 15. Tape format

For the end user of the TAB product, the considerations in the tape design can be summarized as follows:

(1) Outer lead dimensions
These include the lead pitch, lead width, connection length for both output and input sides. Dummy leads can be added to provide extra protection to the connection.

(2) Polyimide tape opening
Parallel slots can be added to the output side to facilitate folding of the tape after connection to the LCD panel. That is to be determined by the outer lead connection method being used and the components layout requirement in the end product. See Fig. 16.

(3) Alignment marks
Fiducial marks and alignment holes can be added to facilitate alignment of the TAB leads to the LCD panel terminals or the PCB land patterns. See Fig. 17.

(4) Polyimide up or polyimide down design
The chip can be inner lead bonded to either side of the tape leads. The choice can resolve stringent components layout requirement in a compact product.

To drive a large size LCD panel, multiple drivers are needed. Use of slim TAB package can help to eliminate folding of many TAB packages and potential alignment and reliability problem. The length of the slim TAB package is typically between 8.5mm to 12.0mm depending on the lead count. With this short length, slim TAB packages can be mounted along the perimeter

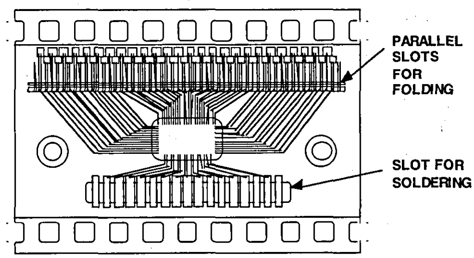


Figure 16. Polyimide tape opening

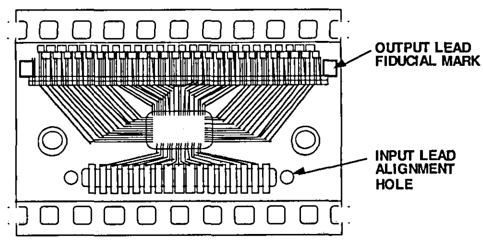


Figure 17. Alignment marks

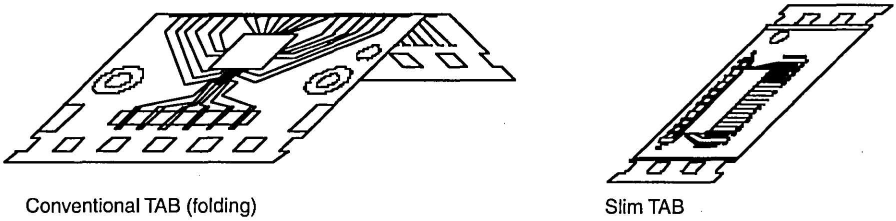


Figure 18. Slim TAB against conventional TAB

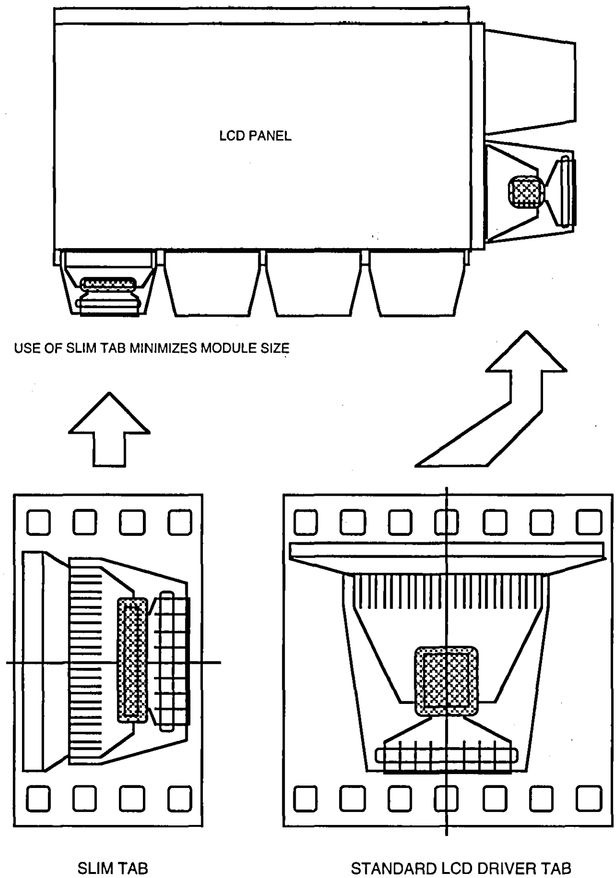


Figure 19. Slim TAB and its application

of the LCD panel without a significant increase in the overall panel size. See Fig. 18 & 19.

TAB HANDLING AND STORAGE CONDITIONS

(1) Delivery

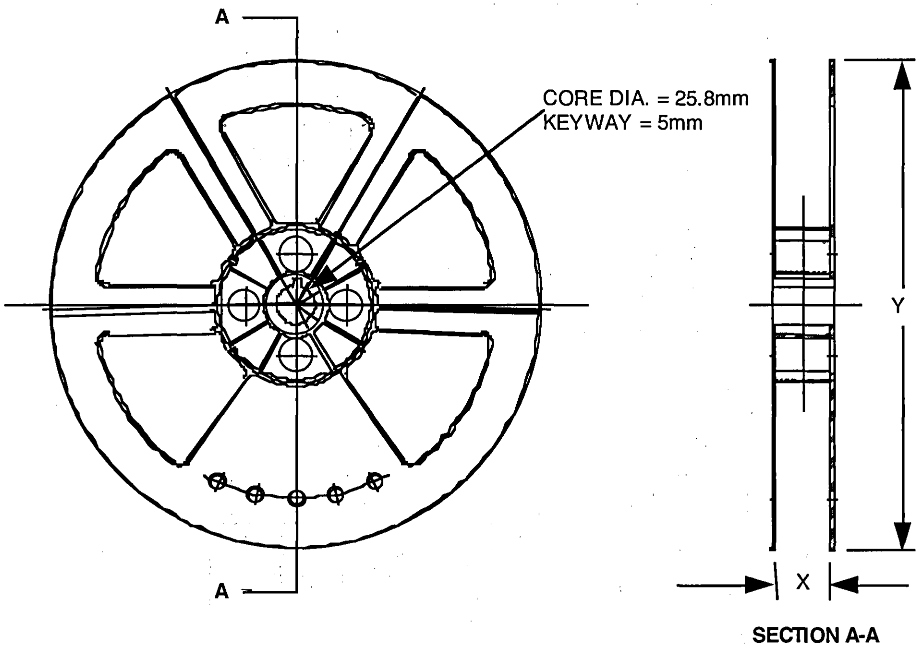
Motorola TAB products are packed in reel. There are two types of reel. The 330mm reel can carry about 20m of tape and the 405mm reel can carry 40m tape. Quantity of TAB product in a reel thus varies according to sprocket pitch of a TAB site. An additional 3m of leading tape and 3m of trailing tape are added to each end of the 20m/40m tape for convenience of handling and protection. Emboss separator tape is used when the TAB tape is wound inside the reel.

Each reel is sealed in a moisture resistant ESD protective bag with desiccant and nitrogen to prevent contamination, corrosion and protection from ESD. Each bag is then packed in a protective box for additional protection. See Fig. 21.

(2) Reject handling

All TAB products will undergo 100% functional test. Inner part of reject site is punched out from the tape. Multiple reject sites are spliced off and reconnected with Kapton adhesive tape.

(3) Mechanical and electrical handling



FORMAT	35mm	48mm	70mm
X (+/- 0.5)	37mm	50mm	72mm

Y	330mm	405mm
TAPE LENGTH	20m	40m

MATERIAL: HIGH IMPACT POLYSTYRENE (HIPS)
SURFACE RESISTIVITY: 1 X 10^5 OHM MIN
1 X 10^9 OHM MAX

Figure 20. Tape Reel

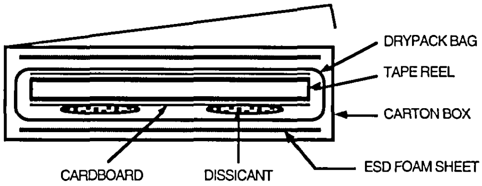


Figure 21. TAB product packing

Prevention of bent lead, contamination, and other forms of mechanical and electrical damage must be observed whenever TAB product is handled. Use of clean room and ESD approved gloves or finger cots are recommended. To prevent ESD damage to the product, proper electrical grounding procedures should be followed.

The outer leads on the TAB product are usually very thin copper foil, so excessive stress should be avoided during mounting of the TAB product. In addition, contamination should be avoided to prevent shorting of the leads. Although the TAB product is structured as a thin film, excessive bending of the film should be avoided to prevent cracking of the solder resist and the encapsulant.

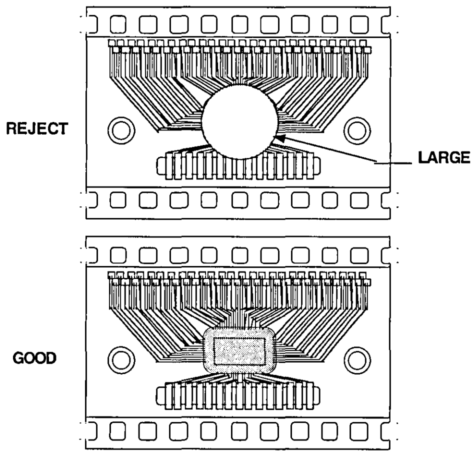


Figure 22. Reject handling

In TAB product, the back side of the chip is exposed. Mechanical or electrical contact with the back side of the chip should be avoided to prevent cracking or ESD damage. Direct exposure to strong ambient light should also be avoided to assure proper electrical characteristics.

(4) Storage conditions
The TAB products should be stored in its original sealed bag in an upright position (stand on diameter end). If products are stored outside of its original sealed bag, then they are recommended to be stored in a nitrogen environment. To assure good solderability, there is a limited time period to use the products once they are removed from the sealed bag. Products stored in ambient conditions, i.e. room temperature at 40% to 50% RH, is recommended to be used within 30 days after opening from the sealed bag. Any unused products stored in the sealed bag after more than one year from date of shipment from Motorola are recommended to be sample tested for solderability.

CONCLUSIONS

TAB package has been gaining wide acceptance in recent years because of its thin body outline and ability to provide high density interconnects in both inner lead bonding and outer lead bonding. It is certainly one of the most important package in the 90's. LCD driver continues to be the major application for TAB packages.

TAB Tape Design Information Checklist

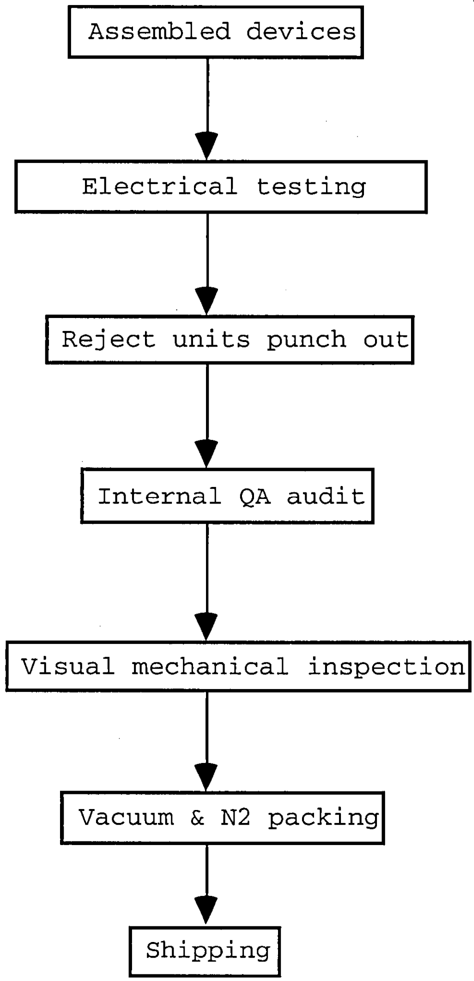
Device name	Example
Final excised size Width Length	 13.5mm 25.4mm
Output side OLB Pitch Width Connection length Dummy lead	 0.23mm 0.11mm 2.835mm min 1, max 2 on each end
Input side OLB Pitch Width Connection length Dummy lead	 1.0mm 0.5mm 1.8mm 1 on each end
Output side alignment mark OD ID Mark to mark distance	2 square marks, one on each end 0.6mm 0.4mm 24.83mm
Input side alignment hole	2 x ϕ 0.5mm on each end
TAB pitch on LCD glass Inter-TAB gap	 3.0mm
No. of sprocket hole	6
Polyimide up/down	Down
Lead coating material Output side Input side	 Tin Tin
OLB connection method Output side Input side	 ACF Soldering
Remark	

FINAL TEST FOR TAB PACKAGE

TEST FLOW

Each lot of TAB devices are 100% tested to confirm the outgoing quality, both of electrical and visual mechanical performance. The manufacturing flow is different from the traditional package in following points:

Continuity of devices - each device within a lot is linked together;
Rejects removal - the die of reject units are punched out from the tape;



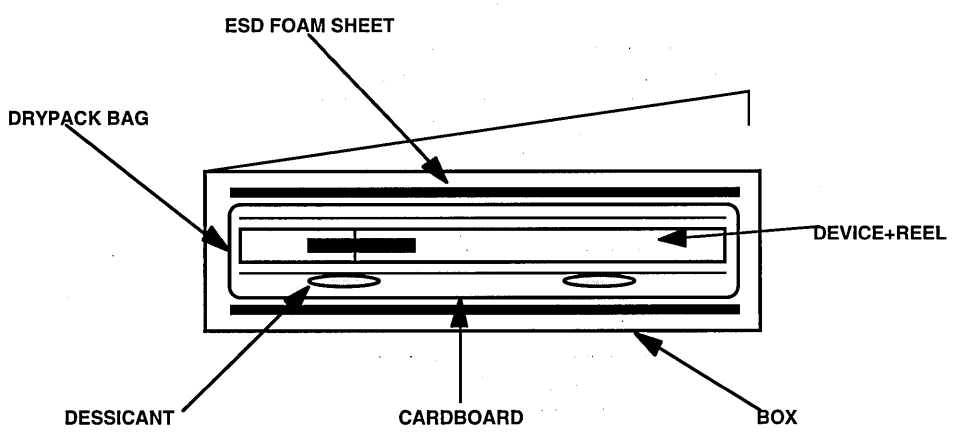
Motorola TAB Package Device Final Test Flow

VACUUM PACK

All TAB devices are passed through the Vacuum Packing process before shipping out. By utilizing the ESD & Moisture protected vacuum packing bag, TAB device can be fully protected from moisture and oxidation on leads. The packing material also protected TAB devices from the damage of mechanical shoot.

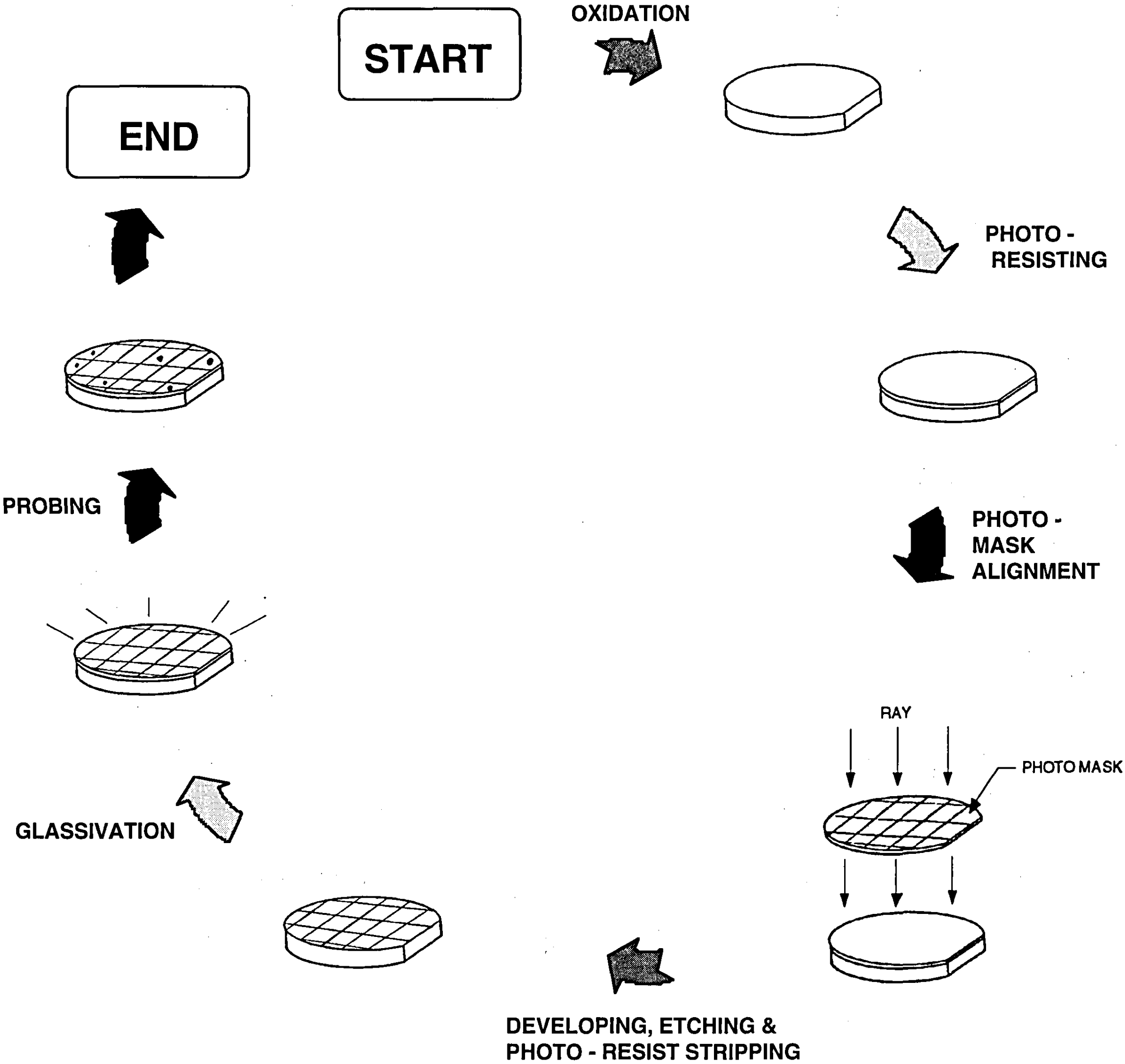
Characteristics of Vacuum Packing:

Vacuum - air is removed from the package to prevent oxidation on leads;
Nitrogen (N2) injection - to balance the pressure for TAB device protection;
Moisture prevention - desiccants are enclosed inside the package to protect the TAB device from moisture damage. Humidity indicator card is also appended with the package for customer inspection.

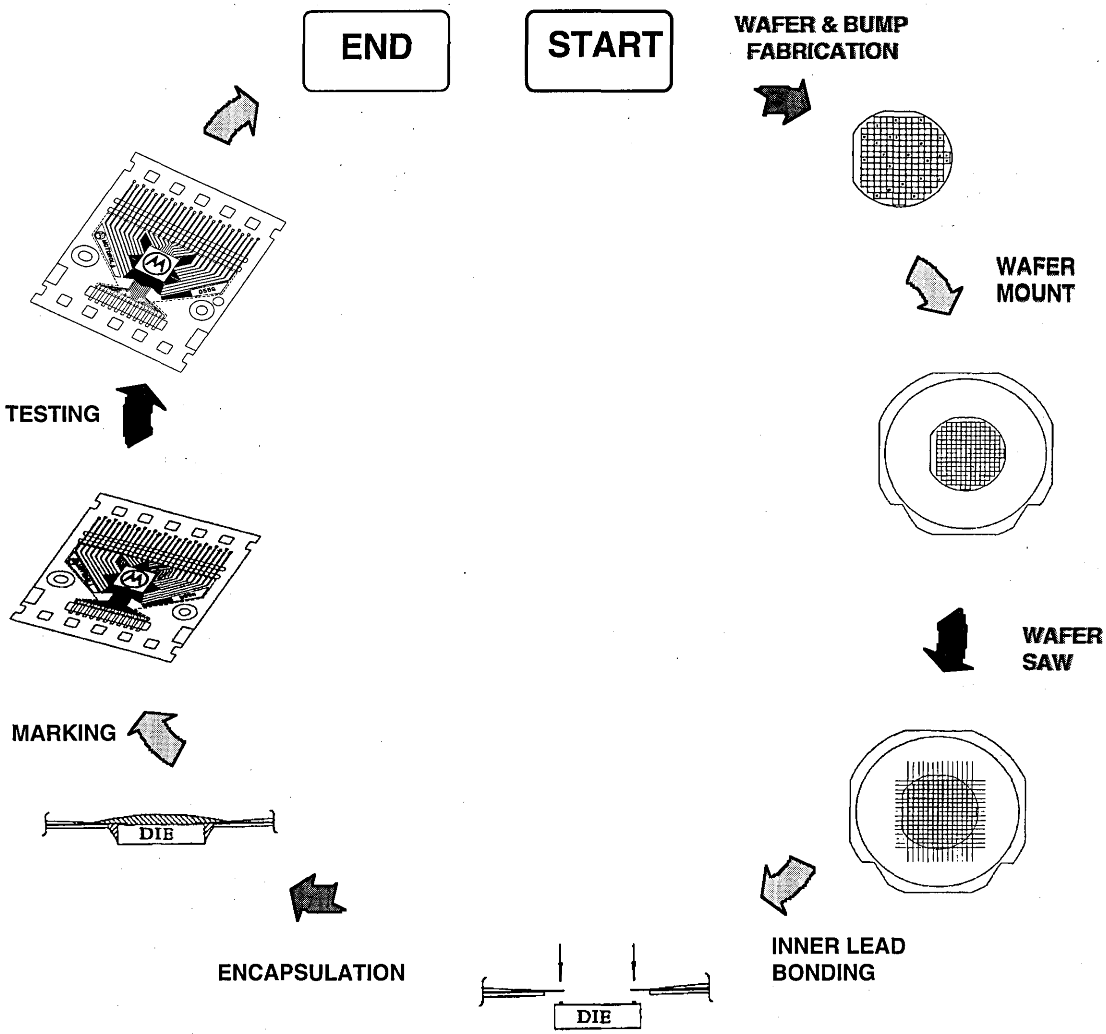


Motorola TAB Package Device Vacuum Pack Appearence

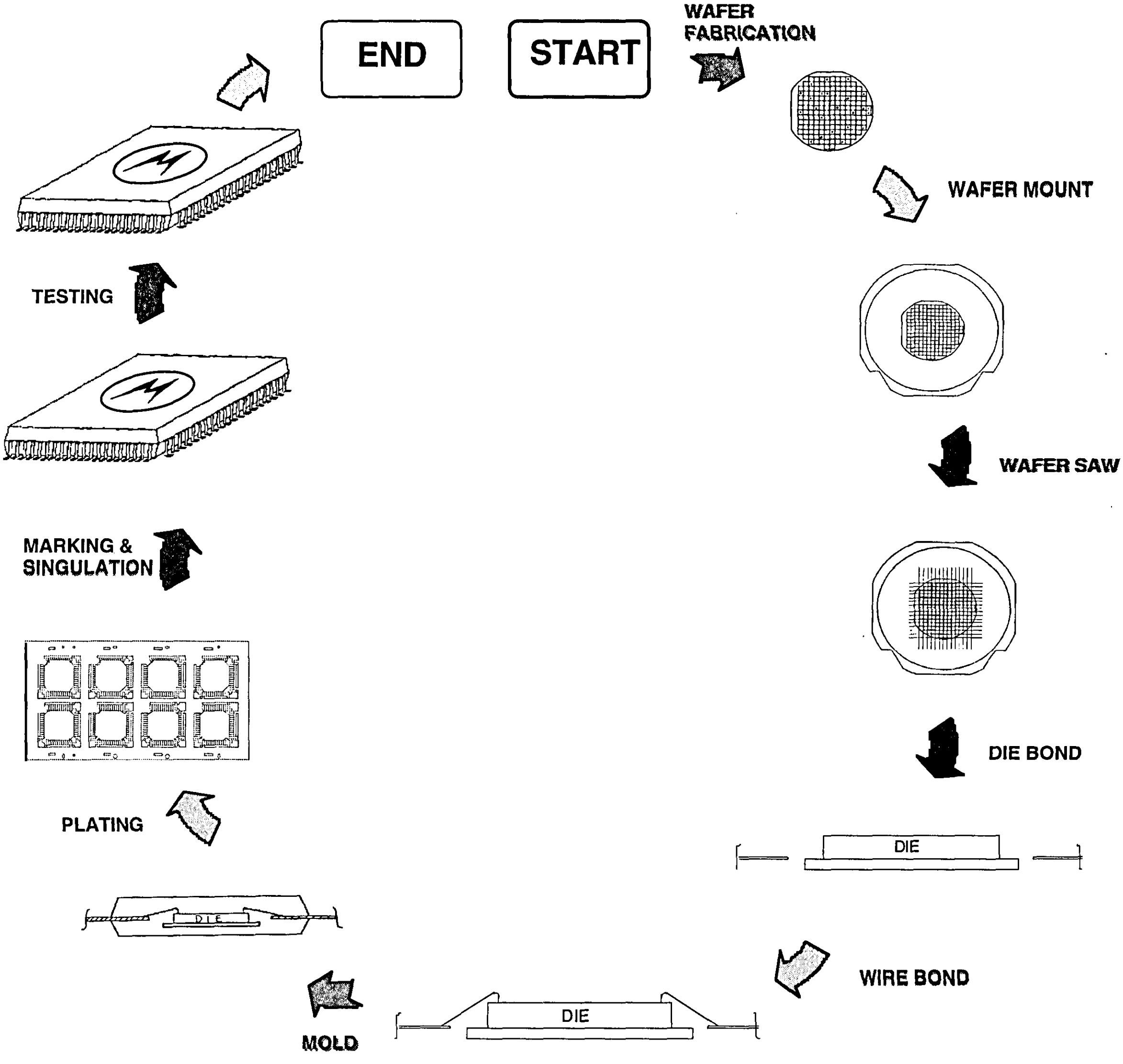
WAFER MANUFACTURING FLOW



TAB MANUFACTURING FLOW



QFP MANUFACTURING FLOW



Liquid Crystal Display Drivers 3

MC14LC5003
MC14LC5004

128 Segment LCD Drivers
CMOS

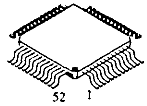
The MC14LC5003/5004 are 128-segment, multiplexed-by-four LCD Drivers. The two devices are functionally the same except for their data input protocols. The MC14LC5003 uses a serial interface data input protocol. The device may be interfaced to the MC68HCXX product families using a minimal amount of software (see example). The MC14LC5004 has a IIC interface and has essentially the same protocol, except that the device sends an acknowledge bit back to the transmitter after each eight-bit byte is received. MC14LC5004 also has a "read mode", whereby data sent to the device may be retrieved via the IIC bus.

The MC14LC5003/MC14LC5004 drives the liquid-crystal displays in a multiplexed-by-four configuration. The device accepts data from a microprocessor or other serial data source to drive one segment per bit. The chip does not have a decoder, allowing for the flexibility of formatting the segment data externally.

Devices are independently addressable via a two-wire (or three-wire) communication link which can be common with other peripheral devices.

The MC14LC5003/MC14LC5004 are low cost version of MC145003 and MC145004 without cascading function.

- Drives 128 Segments Per Package
- May Be Used with the Following LCDs: Segmented Alphanumeric, Bar Graph, Dot Matrix, Custom
- Quiescent Supply Current: 30 μA @ 2.7 V V_{DD}
- Operating Voltage Range: 2.7 to 5.5 V
- Operating Temperature Range: -40 to 85°C
- Separate Access to LCD Drive Section's Supply Voltage to Allow for Temperature Compensation
- See Application Notes AN1066 and AN442

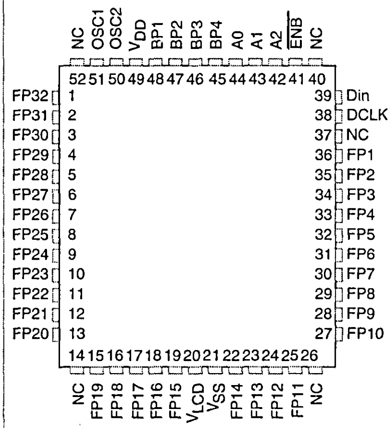


QFP
FU SUFFIX
CASE 848B

ORDERING INFORMATION

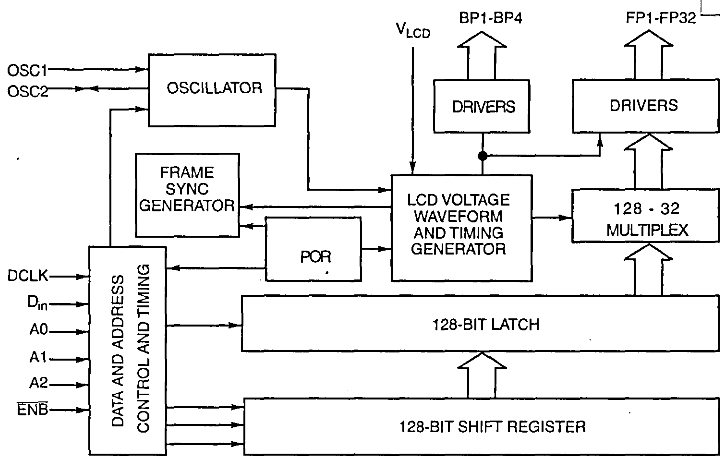
MC14LC5003FU	QFP
MC14LC5004FU	QFP
MCC14LC5003	BARE DIE
MCC14LC5004	BARE DIE

PIN ASSIGNMENT



NC=NO CONNECTION

BLOCK DIAGRAM



REV 2
10/96

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 6.5	V
V_{in}	Input Voltage, D_{in}, and Data Clock	- 0.5 to 15	V
$V_{in\ osc}$	Input Voltage, OSC_{in} of Master	- 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
T_A	Operating Temperature Range	- 40 to + 85	°C
T_{stg}	Storage Temperature Range	- 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A= 25°C)

Characteristic	Symbol	V_{DD} V	V_{LCD} V	Min	Typical	Max	Unit
Output Drive Current — Frontplanes							µA
V_O = 0.15 V	I_{FH}	5	2.7	260	—	—	
	I_{FL}	5	2.7	260	—	—	
V_O = 2.65 V	I_{FH}	5	2.7	-240	—	—	
	I_{FL}	5	2.7	-240	—	—	
V_O = 1.72 V	I_{FH}	5	2.7	-40	—	—	
	I_{FL}	5	2.7	—	—	-1.5	
V_O = 1.08 V	I_{FH}	5	2.7	40	—	—	
	I_{FL}	5	2.7	—	—	2	
V_O = 0.15 V	I_{FH}	5	5.5	600	—	—	
	I_{FL}	5	5.5	600	—	—	
V_O = 5.35 V	I_{FH}	5	5.5	-520	—	—	
	I_{FL}	5	5.5	-520	—	—	
V_O = 3.52 V	I_{FH}	5	5.5	-35	—	—	
	I_{FL}	5	5.5	—	—	-1.5	
V_O = 1.98 V	I_{FH}	5	5.5	55	—	—	
	I_{FL}	5	5.5	—	—	1	
Supply Standby Currents (No Clock)							µA
I_{DD} = Standby @ I_{out} = 0 µA	I_{DDS}	2.7	—	—	—	30	
I_{LCD} = Standby @ I_{out} = 0 µA	I_{LCDS}	—	2.7	—	—	800	
I_{DD} = Standby @ I_{out} = 0 µA	I_{DDS}	5.5	—	—	—	50	
I_{LCD} = Standby @ I_{out} = 0 µA	I_{LCDS}	—	5.5	—	—	1500	
Supply Currents (f_{OSC}) = 110 kHz							µA
I_{DD} = Quiescent @ I_{out} = 0 µA, no loading	I_{DDQ}	2.7	—	—	30	—	
I_{DD} = Quiescent @ loading = 270pF	I_{DDQ}	2.7	—	—	—	70	
I_{DD} = Quiescent @ I_{out} = 0 µA, no loading	I_{DDQ}	5.5	—	—	170	—	
I_{DD} = Quiescent @ loading = 270pF	I_{DDQ}	5.5	—	—	—	400	
I_{LCD} = Quiescent @ I_{out} = 0 µA, no loading	I_{LCDQ}	—	2.7	—	—	40	
I_{LCD} = Quiescent @ I_{out} = 0 µA, no loading	I_{LCDQ}	—	5.5	—	—	70	
Input Current	I_{in}	—	—	-0.1	—	0.1	µA
Input Capacitance	C_{in}	—	—	—	—	7.5	pF

(continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	V_{DD} V	V_{LCD} V	Min	Typical	Max	Unit
Frequencies								
OSC2 Frequency @ R1; R1 = 200 kΩ		f_{OSC2}	5	5	100	—	150	kHz
BP Frequency @ R1		f_{BP}	5	5	100	—	150	Hz
OSC2 Frequency @ R2; R2 = 996 kΩ		f_{OSC2}	5	5	23	—	33	kHz
Average DC Offset Voltage (BP Relative to FP)		V_{OO}	5	2.8	-50	—	+50	mV
Input Voltage	"0" Level	V_{IL}	2.8	5	—	—	0.85	V
		V_{IL}	5.5	5	—	—	1.65	
	"1" Level	V_{IH}	2.8	5	2	—	—	
		V_{IH}	5.5	5	3.85	—	—	
Output Drive Current — Backplanes	V_O = 2.65 V	I_{BH}*	5	2.8	-240	—	—	µA
		I_{BL}	5	2.8	-240	—	—	
	V_O = 0.15 V	I_{BH}	5	2.8	260	—	—	
		I_{BL}	5	2.8	260	—	—	
	V_O = 1.08V	I_{BH}	5	2.8	40	—	—	
		I_{BL}	5	2.8	—	—	2	
	V_O = 1.72 V	I_{BH}	5	2.8	-40	—	—	
		I_{BL}	5	2.8	—	—	-1	
	V_O = 5.35 V	I_{BH}	5	5.5	-520	—	—	
		I_{BL}	5	5.5	-520	—	—	
	V_O = 0.15 V	I_{BH}	5	5.5	600	—	—	
		I_{BL}	5	5.5	600	—	—	
	V_O = 1.98 V	I_{BH}	5	5.5	55	—	—	
		I_{BL}	5	5.5	—	—	1	
	V_O = 3.52 V	I_{BH}	5	5.5	-35	—	—	
		I_{BL}	5	5.5	—	—	-1	
Pulse Width, Data Clock	(Figure 1)	t_w	5		50	—	—	ns
			3		100	—	—	
DCLK Rise/Fall Time	(Figure 1)	t_r, t_f	5		—	—	20	µs
			3		—	—	120	
Setup Time, D_{in} to DCLK	(Figure 2)	t_{su}	5		0	—	—	ns
			3		0	—	—	
Hold Time, D_{in} to DCLK	(Figure 2)	t_h	5		30	—	—	ns
			3		60	—	—	
DCLK Low to $\overline{ENB}$ High	(Figure 3)	t_h	5		10	—	—	ns
			3		20	—	—	
$\overline{ENB}$ High to DCLK High	(Figure 3)	t_{rec}	5		10	—	—	ns
			3		20	—	—	
$\overline{ENB}$ High Pulse Width	(Figure 3)	t_w	5		50	—	—	ns
			3		100	—	—	
$\overline{ENB}$ Low to DCLK High	(Figure 3)	t_{su}	5		10	—	—	ns
			3		20	—	—	

NOTE: Timing for Figures 1, 2, and 3 are design estimates only.

* For a time (t = 4/OSC FREQ.) after the backplane waveform changes to a new voltage level, the circuit is maintained in the high-current state to allow the load capacitances to charge quickly. The circuit is then returned to the low-current state until the next voltage change.

SWITCHING WAVEFORMS

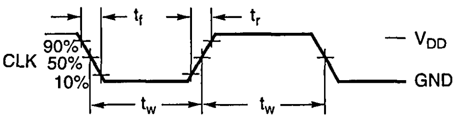


Figure 1.

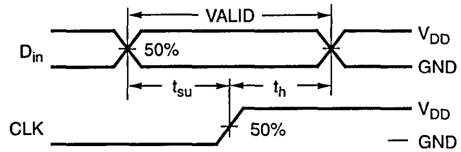


Figure 2.

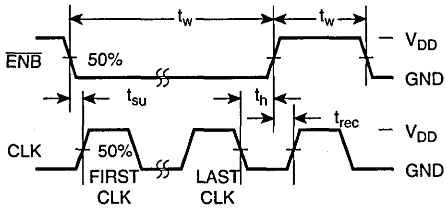


Figure 3.

FUNCTIONAL DESCRIPTION

The MC14LC5003/MC14LC5004 has essentially two sections which operate asynchronously from each other; the data input and storage section and the LCD drive section. The LCD drive and timing is derived from the oscillator, while the data input and storage is controlled by the Data In (D_{in}), Data Clock (DCLK), Address (A0, A1, A2), and Enable ($\overline{ENB}$) pins.

Data is shifted serially into the 128-bit shift register and arranged into four consecutive blocks of 32 parallel data bits. A time-multiplex of the four backplane drivers is made (each backplane driver becoming active then inactive one after another) and, at the start of each backplane active period, the corresponding block of 32 bits is made available at the frontplane drivers. A high input to a plane driver turns the driver on, and a low input turns the driver off.

Figure 4 shows the sequence of backplanes. Figure 5 shows the possible configurations of the frontplanes relative to the backplanes. When a backplane driver is on, its output switches from V_{LCD} to 0 V, and when it is off, it switches from 1/3 V_{LCD} to 2/3 V_{LCD}. When a frontplane driver is on, its output switches from 0 V to V_{LCD}, and when it is off, it switches from 2/3 V_{LCD} to 1/3 V_{LCD}.

The LCD drive and timing section provides the multiplex signals and backplane driver input signals and formats the frontplane and backplane waveforms.

The address pins are used to uniquely distinguish LCD driver from any other chips on the same bus and to define LCD driver as the "master" in the system. There must be one master in any system.

The enable pin may be used as a third control line in the communication bus. It may be used to define the moment when the data is latched. If not used, then the data is latched after 128 bits of data have been received.

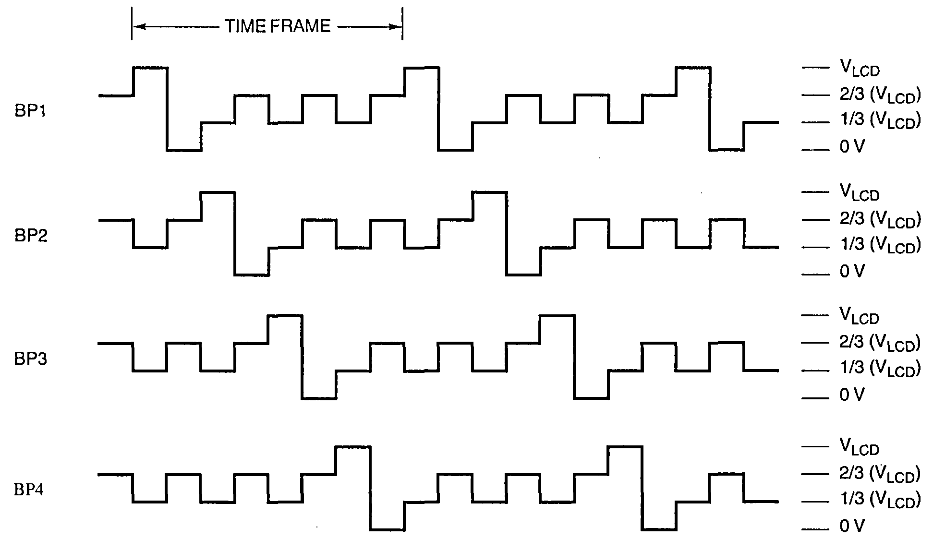


Figure 4. Backplane Sequence

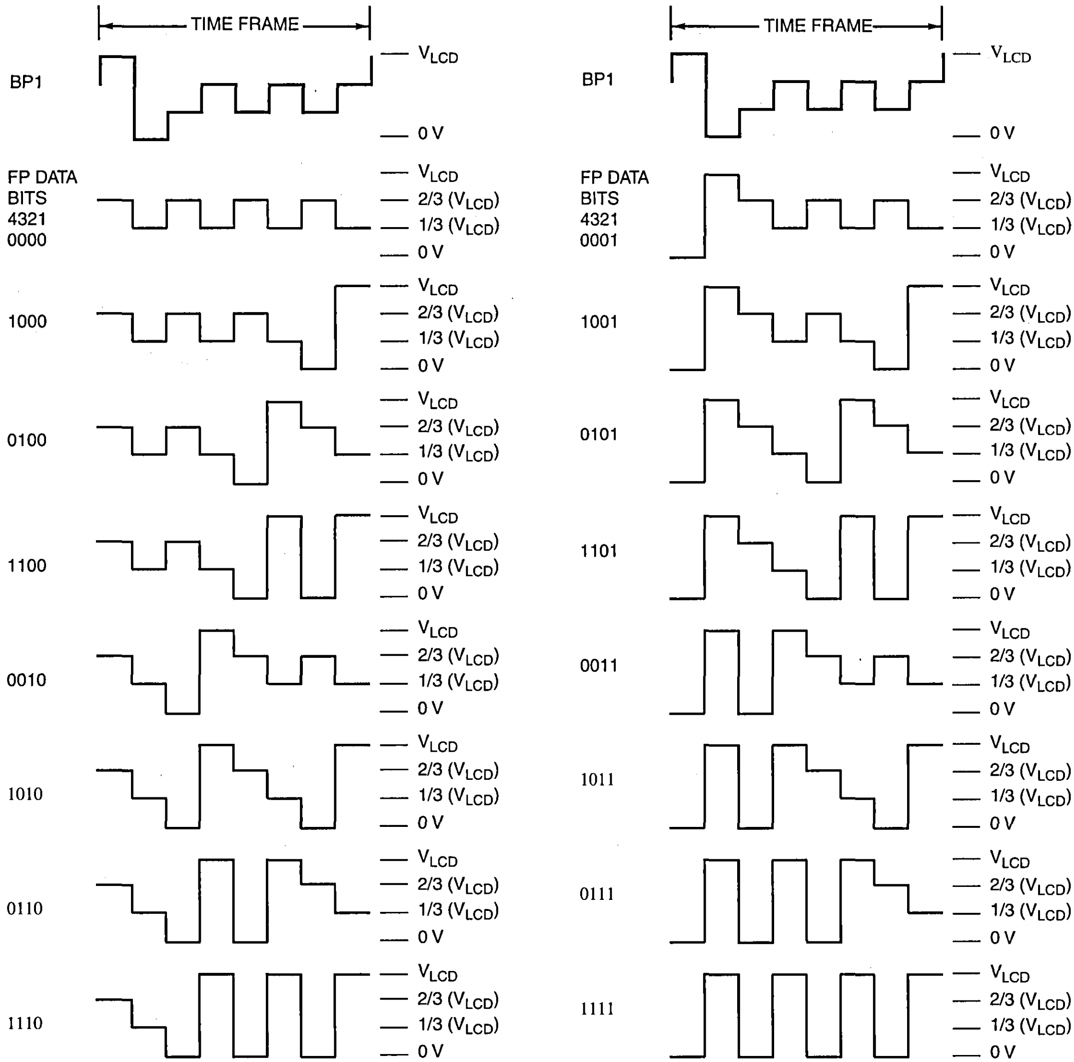


Figure 5. Frontplane Combinations

PIN DESCRIPTIONS

A0-A2
Address Inputs (Pins 42-44)

The devices have to receive a correct address before they will accept data. Three address pins (A2, A1, A0) are used to define the states of the three programmable bits of MC14LC5003/MC14LC5004's 8-bit address.

The address is 0111vwxy where v, w, x represent A2, A1, and A0 respectively. Where v, w, x=0, then A2, A1, and A0 should be tied to 0 V. Where v, w, x=1, then A2, A1, and A0 should be tied to V_{DD}.

The address pins must be tied to V_{DD}. This defines the device as a master.

NOTE

Note: In applications where the circuit will be isolated from external manual interference the system designer may take advantage of the self-programming feature. Upon power-on, address pins which are left open-circuit will be charged to V_{DD}. However, care must be taken not to inadvertently discharge the pins after power-on since the address may then be lost. A similar feature is also available on the $\overline{ENB}$ pin.

CAUTION

The configuration A0, A1, A2 = 000 should not be used. This does not give a valid address and is reserved for Motorola's use only. All three address pins should never be tied to 0 V simultaneously.

$\overline{ENB}$
Enable Input (Pin 41)

If the $\overline{ENB}$ pin is tied to V_{DD}, the MC14LC5003/MC14LC5004 will always latch the data after 128 bits have been received. The latched data is multiplexed and fed to the frontplane drivers for display. If external control of this latching function is required, then the $\overline{ENB}$ pin should be held low, followed by one high pulse on $\overline{ENB}$ when data display is required. (This may be useful in a system where one MC145003/MC145004 is permanently addressed and only the last 128 bits of data sent are required to be latched for display). The pulse on the $\overline{ENB}$ pin must occur while DCLK is high.

DCLK, D_{in}
Data Clock and Data Input (Pins 38, 39)

Address input and data input controls. See **Data Input Protocol** sections for relevant option.

OSC1, OSC2
Oscillator Pins (Pins 51, 50)

To use the on-board oscillator, an external resistor should be connected between OSC1 and OSC2. Optionally, the OSC1 pin may be driven by an externally generated clock signal.

A resistor of 680 kΩ connected between OSC1 and OSC2 pins gives an oscillator frequency of about 30 kHz, giving approximately 30 Hz as seen at the LCD driver outputs. A resistor of 200 kΩ gives about 100 kHz, which results in 100 Hz at the driver outputs. LCD manufacturers recommend an LCD drive frequency of between 30 Hz and 100 Hz. See Figure 6.

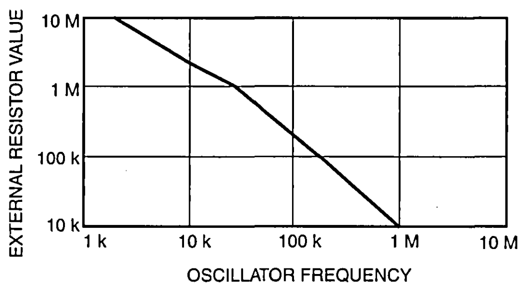


Figure 6. Oscillator Frequency vs. Load Resistance (Approximate)

FP1-FP32
Frontplane Drivers (Pins 36-27, 25-22, 19-15, 13-1)

Frontplane driver outputs.

BP1-BP4
Backplane Drivers (Pins 48-45)

Backplane driver outputs.

V_{LCD}
LCD Driver Supply (Pin 20)

Power supply input for LCD drive outputs. May be used to supply a temperature-compensated voltage to the LCD drive section, which can be separate from the logic voltage supply, V_{DD}.

V_{DD}
Positive Power Supply (Pin 49)

This pin supplies power to the main processor interface and logic portions of the device. The voltage range is 2.7 to 5.5 V with respect to the V_{SS} pin.

For optimum performance, V_{DD} should be bypassed to V_{SS} using a low inductance capacitor mounted very closely to these pins. Lead length on this capacitor should be minimized.

V_{SS}
Ground (Pin 21)

Common ground.

DATA INPUT PROTOCOL

Two-wire communication bus DCLK, D_{in}; three-wire communication bus DCLK, D_{in}, $\overline{ENB}$.

MC14LC5003 — SERIAL INTERFACE DEVICE (FIGURE 7)

Before communication with an MC14LC5003 can begin, a start condition must be set up on the bus by the transmitter. To establish a start condition, the transmitter must pull the data line low while the clock line is high. The "idle" state for the clock line and data line is the high state.

After the start condition has been established, an eight-bit address should be sent by the transmitter. If the address sent corresponds to the address of the MC14LC5003 then on each successive clock pulse, the addressed device will accept a data bit.

If the $\overline{ENB}$ pin is permanently high, then the addressed MC14LC5003's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise, the control of this latch function may be overridden by holding the $\overline{ENB}$ line low until the new data is required to be displayed, then a high pulse should be sent on the $\overline{ENB}$ line. The high pulse must be sent during DCLK high (clock idle).

To end communication with an MC14LC5003, a stop condition should be set up on the bus (or another start condition may be set up if another communication is desired). Note that the communication channel to an addressed device may be left open after the 128 data bits have been sent by not setting up a stop or a start condition. In such a case, the 129th rising DCLK edge, which normally would be used to set up the stop or start condition, is ignored by the MC14LC5003 and data continues to be received on the 130th rising DCLK. The latch function continues to work as normal (i.e., data is be latched either after each block of 128 data bits has been received or under external control as required).

At any time during data transmission, the transfer may be interrupted with a stop condition. Data transmission may be resumed with a start condition and resending the address.

MC14LC5004 — IIC DEVICE (FIGURE 8)

Before communication with an MC14LC5004 can begin, a start condition must be set up on the bus by the controller. To establish a start condition, the controller must pull the data line low while the clock line is high.

After the start condition has been established, an eight-bit address should be sent by the controller followed by an extra clock pulse while the data line is left high. In this option, only the seven most significant bits of the address are used to uniquely define devices on the bus, the least significant bit is used as a read/write control: if the least significant bit is 0, then the controller writes to the LCD driver; if it is 1, then the controller reads from the LCD driver's 128-bit shift register on a first-in first-out basis. If the seven most significant address bits sent correspond to the address of the LCD driver then the addressed LCD driver responds by sending an "acknowledge" bit back to the controller (i.e., the LCD driver pulls the data line low during the extra clock pulse supplied by the controller). If the least significant address bit was 0, then the controller should continue to send data to the LCD driver in blocks of eight bits followed by an extra ninth clock pulse to allow the LCD driver to pull the data line D_{in} low as an acknowledgment. If the least significant address bit was 1, then the LCD driver sends data back to the controller (the clock is supplied by the controller). After each successive group of eight bits sent, the LCD driver leaves the data line high for one pulse.

If the $\overline{ENB}$ pin is permanently high, then the addressed MC14LC5004's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise the control of this latch function may be overridden by holding the $\overline{ENB}$ line low until the new data is required to be displayed, then a high pulse should be sent on the $\overline{ENB}$ line. The high pulse must be sent during DCLK high (clock idle).

To end communication with an MC14LC5004, a stop condition should be set up on the bus (or another start condition may be set up if another communication is desired). Note that the communication channel to an addressed device may be left open after the 128 data bits have been sent by not setting up a stop or a start condition. In such a case the rising DCLK edge which comes after all 128 data bits have been sent and after the last acknowledge-related clock pulse has been made is ignored; data continues to be received on the following DCLK high. The latch function continues to work as normal (i.e., data is latched either after each block of 128 data bits has been received or under external control as required).

At any time during data transmission, the transfer may be interrupted with a stop condition. Data transmission may be resumed with a start condition and resending the address.

Figure 7. MC14LC5003(SERIAL INTERFACE DEVICE)

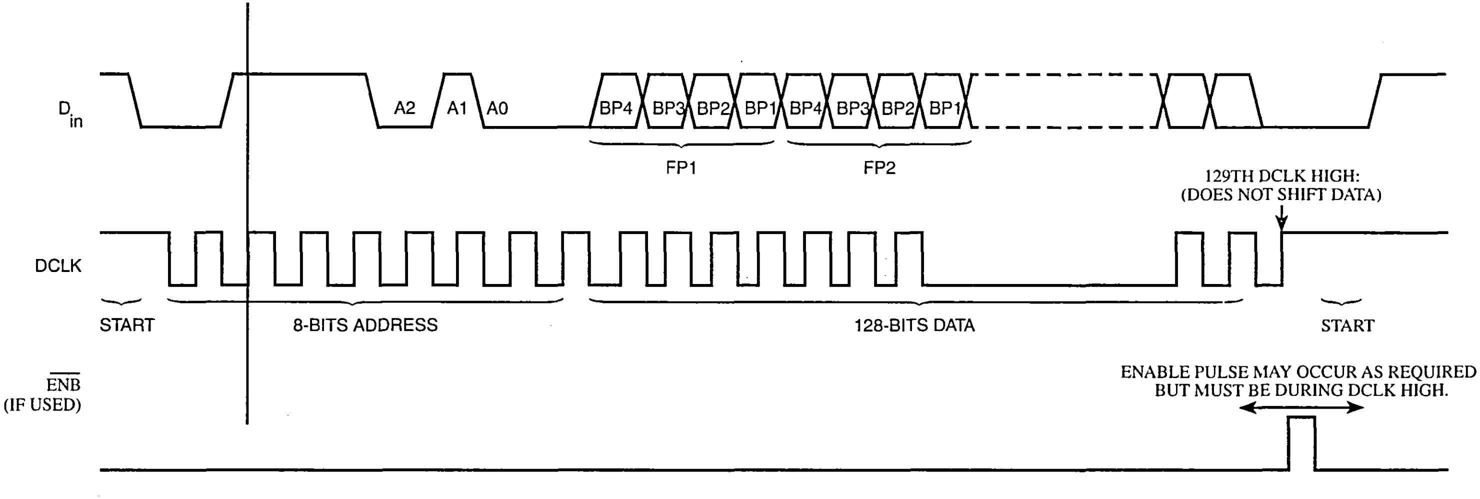


Figure 7a. Data Input—MC14LC5003

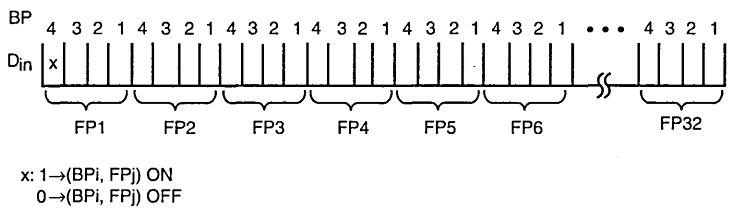


Figure 7b. Serial 128 Bits Data

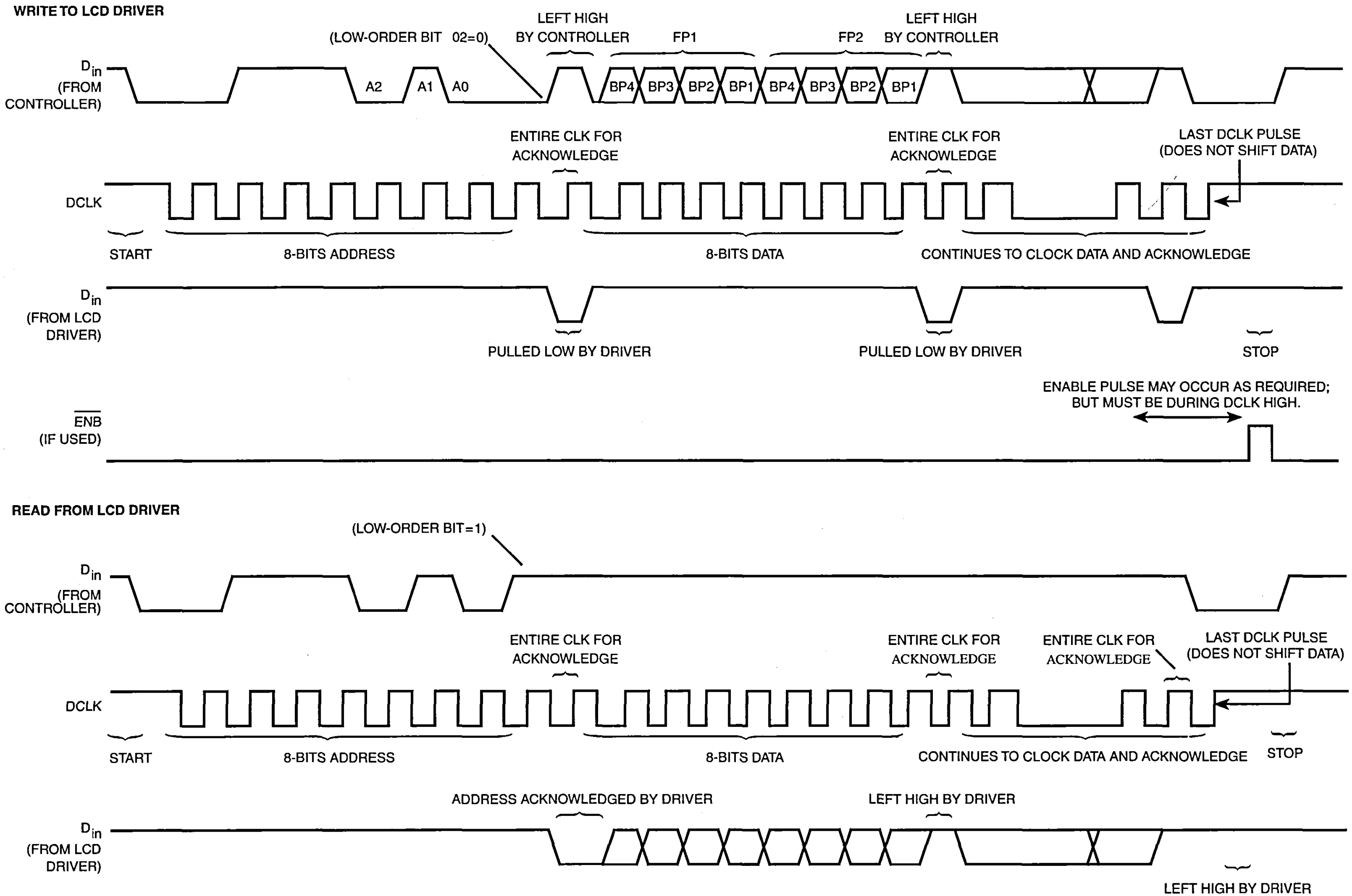


Figure 8. Data Input MC14LC5004 (IIC Device)

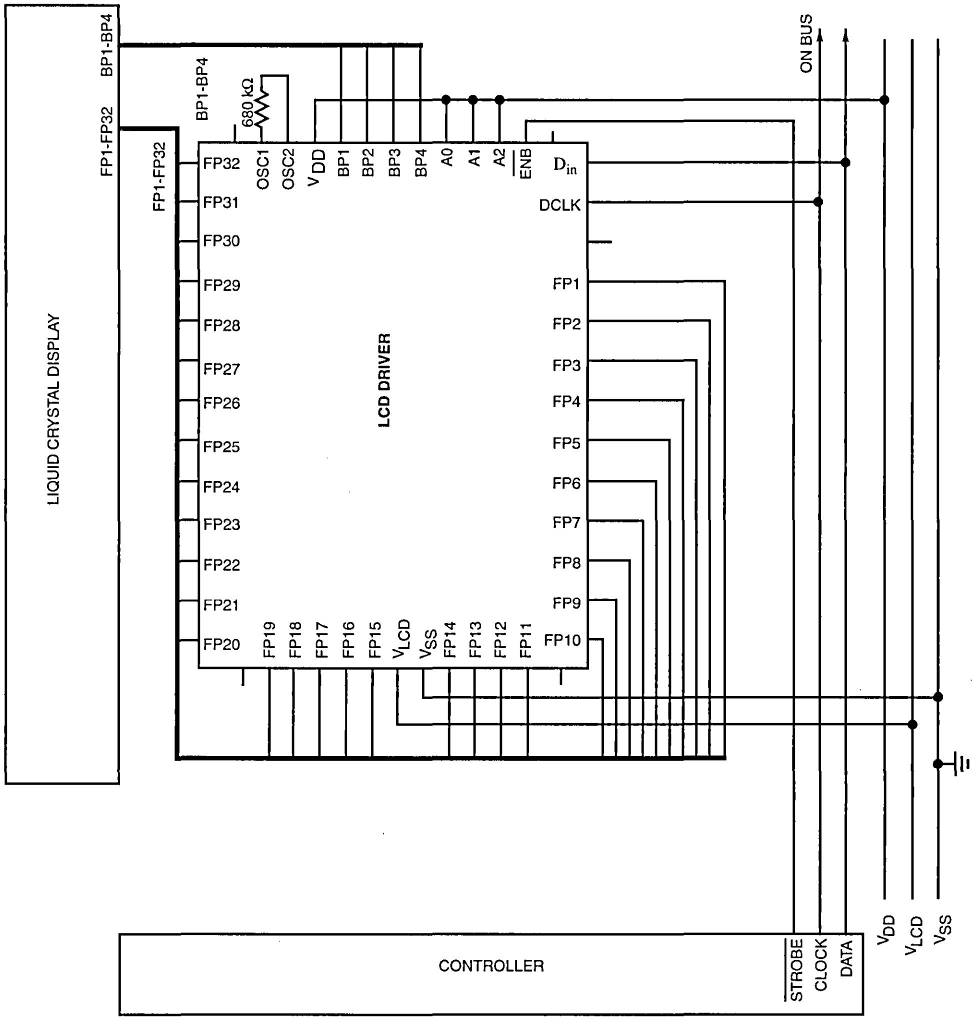


Figure 9. Application Example

APPLICATION INFORMATION

Figure 10 shows an interface example.

Example shows a semi-automatic SPI Mode (only start and stop conditions are done in non-SPI Mode). It contains the software to use HC11 with MC14LC5003 in manual SPI Mode.

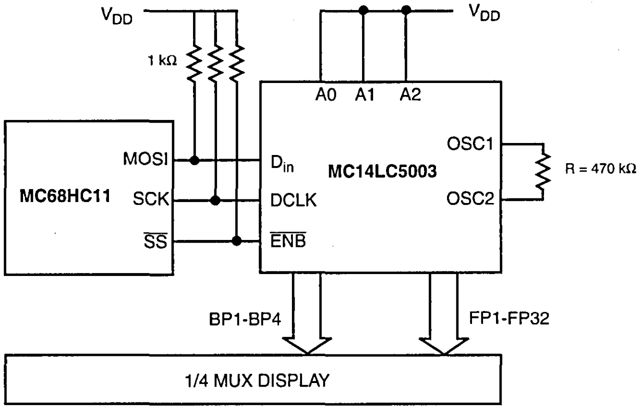


Figure 10. Interface Example Between MC68HC11 and MC14LC5003

```

                    ;=======CONSTANTS==============================================
0000  T             extram     equ        $A000                ;$A000 for 8K RAM
0000  T             stack      equ        $00FF                ;last RAM byte
0000  T             intofs     equ        $1000                ;Internal Registers
0000  T             data       equ        $08
0000  T             clock      equ        $10
0000  T             enable     equ        $20
0000  T             portd      equ        8


                    ;=======PROGRAM BEGIN==========================================
A000  T                        org        extram               ;Program into RAM
A000  N  8E00FF     cold       lds        #stack               ;set stack pointer
A003  M  8638                  ldaa       #$38                 ;set of MOSI,SS,SCK
A005  T  B71009                staa       $1009                ;DDRD
A008  M  C611                  ldab       #17
A00A  N  CEA05E                ldx        #send
A00D  T  BDA010                jsr        spi
A010  T                        end        cold

A010  U  18CE1000   spi        ldy        #intofs
A014  J  181D0820              bclr       portd,y #enable      ;EN = 0
A018  T  BDA031                jsr        start                ;start condition
A01B  X  A600       again      ldaa       0 , x                ;SPI Mode Use
A01D  T  B7102A                staa       $102A                ;SPDR
A020  L  181F2980FB            brclr      $29,y,#$80,*
A025  H  08                    inx                             ;next DATA
A026  H  5A                    decb
A027  R  26F2                  bne        again
A029  J  181C0820              bset       portd,y #enable
A02D  T  BDA04C                jsr        stop                 ;stop condition
A030  H  39                    rts

A031  M  8633       start      ldaa       #$33                 ;Normal Mode
A033  T  B71028                staa       $1028                ;SPCR
```

```
A036  J  181C0808                bset   portd,y #data     ;DATA = 1
A03A  J  181C0810                bset   portd,y #clock    ;CLK = 1
A03E  J  181D0808                bclr   portd,y #data     ;DATA = 0
A042  J  181D0810                bclr   portd,y #clock    ;CLK = 0
A046  M  8673                    ldaa   #$73              ;SPI Mode
A048  T  B71028                  staa   $1028             ;SPCR
A04B  H  39                      rts
A04C  M  8633           stop     ldaa   #$33              ;Normal Mode
A04E  T  B71028                  staa   $1028             ;SPCR
A051  J  181D0808                bclr   portd,y #data     ;DATA = 0
A055  J  181C0810                bset   portd,y #clock    ;CLK = 1
A059  J  181C0808                bset   portd,y #data     ;DATA = 0
A05D  H  39                      rts

A05E  T  7E             send     fcb    $007E             ;LCD Driver Address
A05F  T  F0                      fcb    $00f0             ;Data to sent
A060  T  F0                      fcb    $00f0
A061  T  F0                      fcb    $00f0
A062  T  F0                      fcb    $00f0
A063  T  F0                      fcb    $00f0
A064  T  F0                      fcb    $00f0
A065  T  F0                      fcb    $00f0
A066  T  F0                      fcb    $00f0
A067  T  F0                      fcb    $00f0
A068  T  F0                      fcb    $00f0
A069  T  F0                      fcb    $00f0
A06A  T  F0                      fcb    $00f0
A06B  T  F0                      fcb    $00f0
A06C  T  F0                      fcb    $00f0
A06D  T  F0                      fcb    $00f0
A06E  T  F0                      fcb    $00f0
A06F  H  39                      rts

                        ;=======PROGRAM END==============================================
```

Example 1. Semi-Automatic SPI Method

Figure 11 shows another interface example.
Example 2 contains the software to use HC05 with MC14LC5003 in serial data interface.

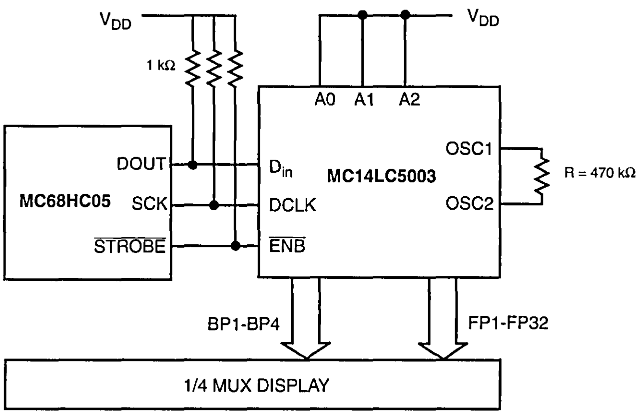


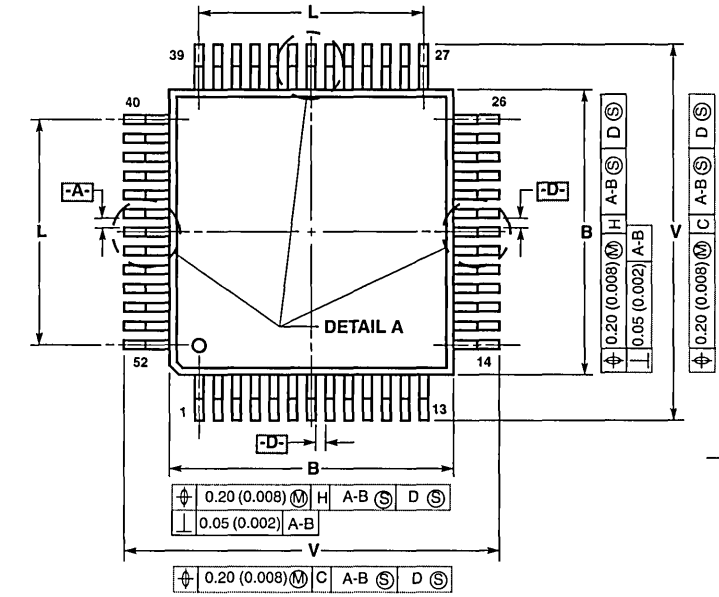
Figure 11. Interface Example Between MC68HC05 and MC14LC5003

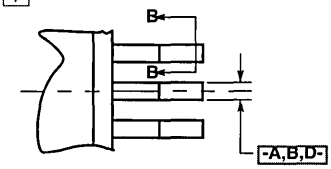
```
PORTC   EQU    $02          PORTC
DDRC    EQU    $06          PORTDC
SEN     EQU    $07          ENABLE PIN, PC7
SCL     EQU    $06          CLOCK PIN, PC6
SDA     EQU    $05          DATA PIN, PC5
DOUT    EQU    $FF          OUTPUT DATA

        ORG    $0050

W1      RMB    1
COUNT   RMB    1

        ORG    $1FFE        ADDRESS OF RESET VECTOR OF MC68HC805C4
        FCB    #$01         RESET VECTOR
        FCB    #$00

*** Main Program start at 0100 ***

        ORG    $0100
START   LDA    #DOUT        SET DATA LINE OUTPUT
        STA    DDRC

AGAIN
        LDX    #$00
        BSET   SDA,PORTC    IDLE STATE
        BSET   SCL,PORTC    CLOCK AND DATA ARE HIGH

READY   BSET   SEN,PORTC    EN=1
        LDA    #$11         SET ADDRESS AND 8 CHARACTERS
        STA    W1
        BCLR   SDA,PORTC    START CONDITION, DATA LOW WHILE CLOCK HIGH

LBYTE   CLC
        LDA    #$08
        STA    COUNT      8 BITS TO SHIFT
        LDA    SEND,X     GET A BYTE
        INCX

LBIT    BCLR   SCL,PORTC    CLOCK LOW
        ROLA
        BCC    DZERO        DATA BIT=0 ?
        BSET   SDA,PORTC    NO, BIT=1 AND DATA HIGH
        JMP    CLKHI
DZERO   BCLR   SDA,PORTC    DATA LOW
CLKHI   BSET   SCL,PORTC    CLOCK HIGH
        DEC    COUNT
        BNE    LBIT
        DEC    W1
        BNE    LBYTE        LAST BYTE ?

STOP    BCLR   SCL,PORTC
        BCLR   SDA,PORTC    STOP CONDITION
        BSET   SCL,PORTC    DATA GOES HIGH WHILE CLOCK HIGH
        BSET   SDA,PORTC
        BCLR   SEN,PORTC    EN=0
        RTS

*** End of Program ***

*** LCD Address and Data ***

SEND
        FCB    $7E                                          LCD DRIVER ADDRESS
        FCB    $FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF       DATA TO SENT
        FCB    $FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF
        RTS
```

Example 2. Serial Data Interface Method

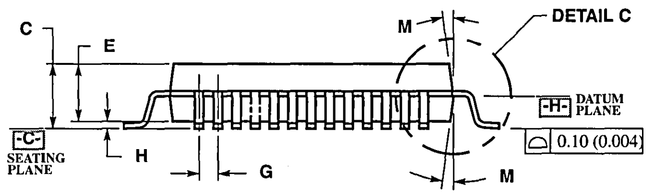
PACKAGE DIMENSIONS

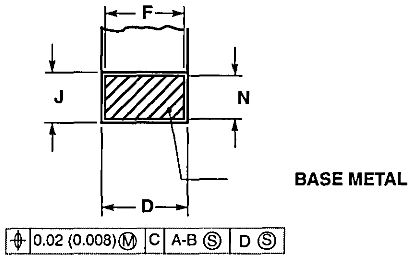
QFP
FU SUFFIX
CASE 848B-02



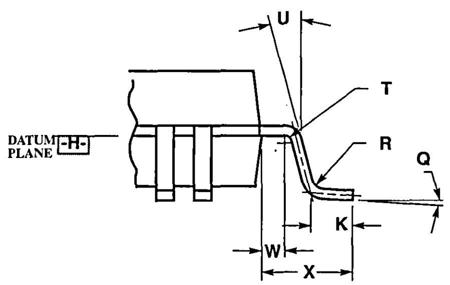


DETAIL A





SECTION B-B

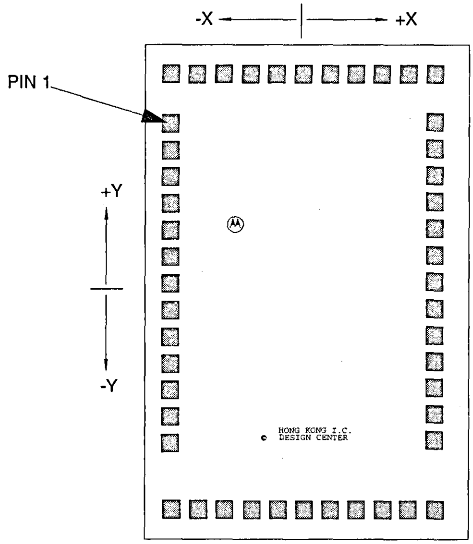


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	--	0.25	--	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	--	0.005	--
U	0°	--	0°	--
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

BOND PAD LAYOUT



Die size : 78 x 119 mil^2

(1 mil ~ 25.4µm)

BOND PAD COORDINATES

PIN NO.	PIN NAME	COORDINATES	
		X	Y
1	FP32	-736.002	929.199
2	FP31	-736.002	781.999
3	FP30	-736.002	634.799
4	FP29	-736.002	487.599
5	FP28	-736.002	340.399
6	FP27	-736.002	193.199
7	FP26	-736.002	45.999
8	FP25	-736.002	-101.201
9	FP24	-736.002	-248.401
10	FP23	-736.002	-395.601
11	FP22	-736.002	-542.801
12	FP21	-736.002	-690.001
13	FP20	-736.002	-837.201
14	NC	N/A	N/A
15	FP19	-736.002	-1205.601
16	FP18	-588.802	-1205.601
17	FP17	-441.602	-1205.601
18	FP16	-294.402	-1205.601
19	FP15	-147.202	-1205.601
20	V_{LCD}	0.000	-1205.600
21	V_{SS}	147.200	-1205.600
22	FP14	294.398	-1205.601
23	FP13	441.598	-1205.601
24	FP12	588.798	-1205.601
25	FP11	735.998	-1205.601
26	NC	N/A	N/A

PIN NO.	PIN NAME	COORDINATES	
		X	Y
27	FP10	735.998	-837.201
28	FP9	735.998	-690.001
29	FP8	735.998	-542.801
30	FP7	735.998	-395.601
31	FP6	735.998	-248.401
32	FP5	735.998	-101.201
33	FP4	735.998	45.999
34	FP3	735.998	193.199
35	FP2	735.998	340.399
36	FP1	735.998	487.599
37	NC	736.000	634.800
38	DCLK	736.000	782.000
39	D_{IN}	736.000	929.200
40	NC	N/A	N/A
41	$\overline{ENB}$	736.000	1205.600
42	A2	588.800	1205.600
43	A1	441.600	1205.600
44	A0	294.400	1205.600
45	BP4	147.198	1205.599
46	BP3	-0.002	1205.599
47	BP2	-147.202	1205.599
48	BP1	-294.402	1205.599
49	V_{DD}	-441.600	1205.600
50	OSC2	-588.800	1205.600
51	OSC1	-736.000	1205.600
52	NC	N/A	N/A

Dimemsions in µm

MC141511A

LCD Segment Driver
CMOS

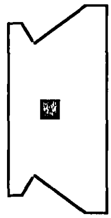
The MC141511A is an LCD frontplane (segment) driver chip which includes a 656 x 8 display RAM. The MC68HC05L10 microcomputer is the companion device which provides the backplane drive.

The MC68HC05L10, together with one MC141511A, may be used to drive a 5248-pixel muxed-by-41 display or a 4096-pixel muxed-by-32 display. Larger displays may be driven by adding additional MC141511A.

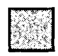
The MC141511A is a low operating voltage version of MC141511. It is pin to pin compatible to the MC141511.

See Application Note AN-HK-13A.

- Operating Supply Voltage Range -
  Control Logic, RAM, and Latch (VDD Pin): 2.7V to 5.5V
  Frontplane Drivers (VLCD Pin): 4.5V to 13.2V
- Operating Temperature Range: -20 to 70˚C
- Direct Interface with the MC68HC05L10
- 656 x 8 Static RAM (Display RAM)
- 128 LCD Segment (Frontplane) Driving Signals
- 10-Bit Address Bus and 8-Bit Bidirectional Data Bus
- Selectable 1:32 or 1:41 Multiplex Ratios
- Available in Two Forms:
  TAB (Tape Automated Bonding), 161 Contacts, 10 sprocket hole device
  Die Form Without Gold Bumps, 159 Pads with 4.5 mil Pads Pitch



MC141511AT2
TAB

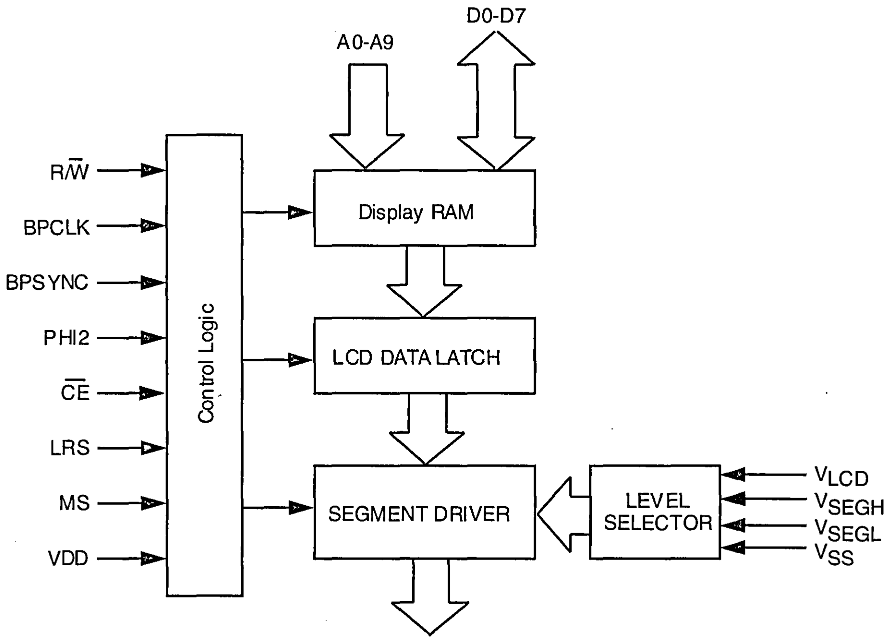


MCC141511A
DIE

ORDERING INFORMATION

MCC141511A	BARE DIE
MC141511AT2	TAB

BLOCK DIAGRAM



REV 3
10/96

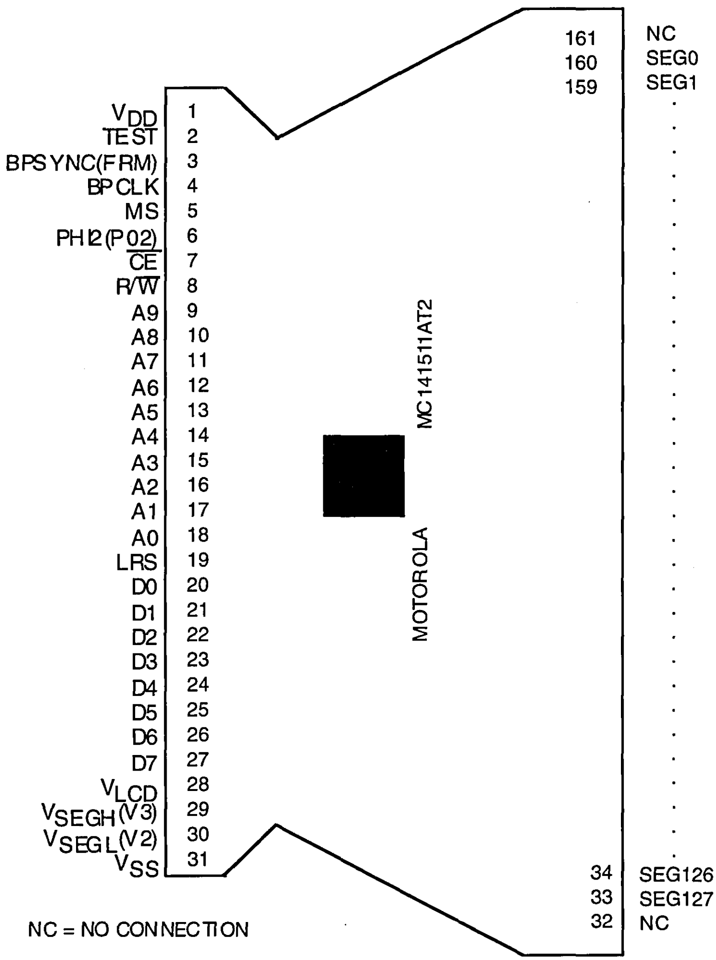


Figure 1A. TAB Package Contact Assignment (Copper View)

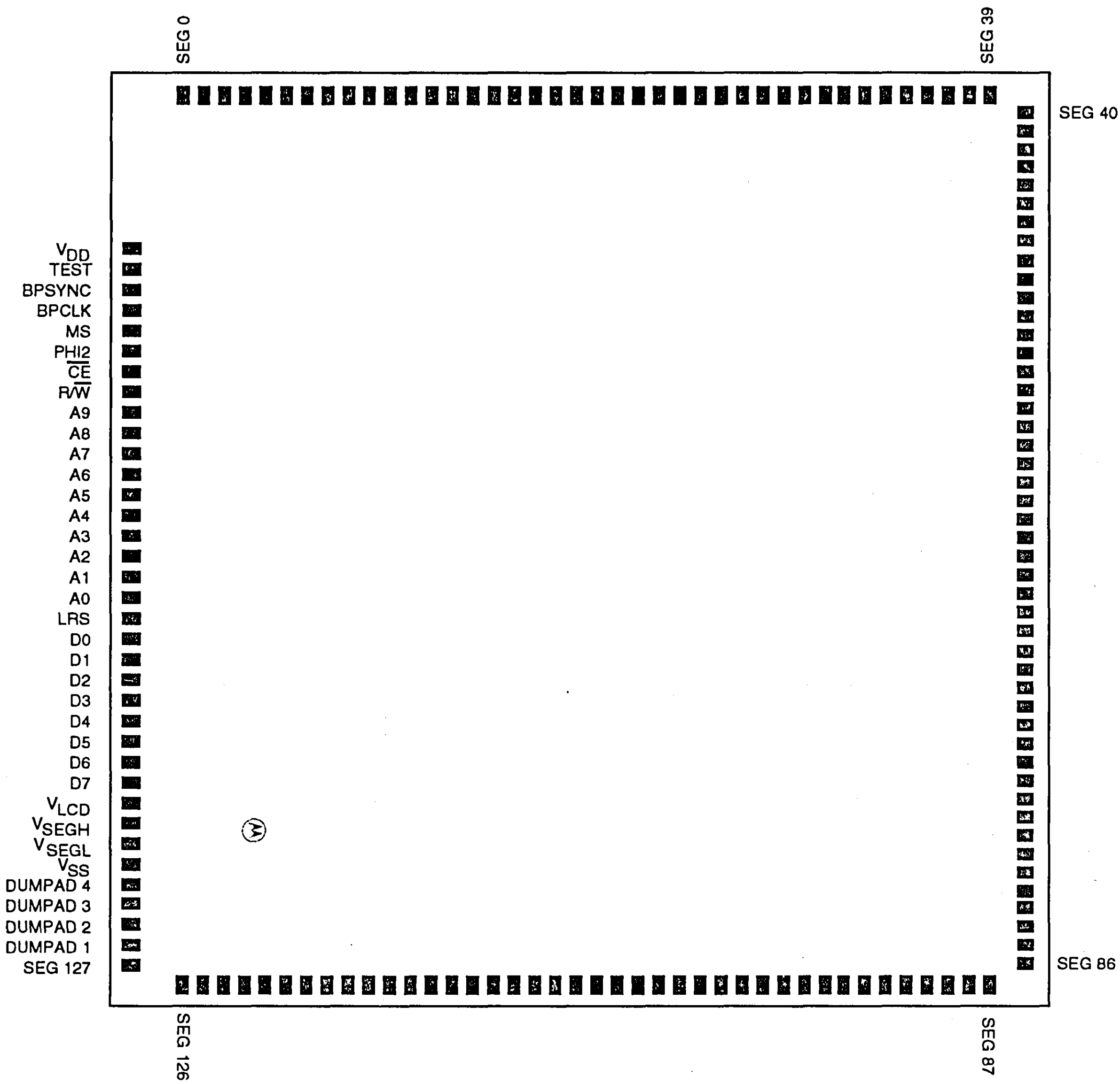


Figure 1B. Chip Pad Assignment

MAXIMUM RATINGS*(Voltages Referenced to V_{SS}, T_A = 25˚C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
V_{LCD}		-0.3 to +14.0	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-20 to +70	˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage *higher than maximum rated voltages to this high* impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left *open. This device may be light sensitive. Caution* should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A = 25˚C)

Symbol	Parameter	Min	Typ	Max	Unit
	Operating Voltage				
V_{DD}	Supply Voltage	2.7	-	5.5	V
V_{LCD}	LCD Voltage	4.5	-	13.2	V
	Supply Current				
	at V_{DD}=5.5V (PHI2=3.685MHz)				
I_{AC}	ACCESS	-	-	200	uA
I_{DP}	DISPLAY	-	25	30	uA
I_{SB}	STANDBY (Using D_{ON} bit of the MCU)	-	15	20	uA
	at V_{DD}=3.0V (PHI2=1.25MHz)				
I_{AC}	ACCESS	-	-	200	uA
I_{DP}	DISPLAY	-	17	30	uA
I_{SB}	STANDBY (Using D_{ON} bit of the MCU)	-	10	20	uA
I_{LCD}	Supply Current at V_{LCD}	-	-	200	uA
V_{OL}	Output Voltage, Iload≤10.0uA	-	-	0.1	V
V_{OH}		V_{LCD}-0.1	-	-	V
V_{OH}	Output High Voltage (Iload=1.6mA) D7-D0	V_{DD}-0.8	-	-	V
V_{OL}	Output Low Voltage (Iload=1.6mA) D7-D0	-	-	0.4	V
V_{IH}	Input High Voltage R/$\overline{W}$, BPCLK, BPSYNC, PHI2, MS, $\overline{CE}$, D7-D0	0.8xV_{DD}	-	V_{DD}	V
V_{IL}	Input Low Voltage R/$\overline{W}$, BPCLK, BPSYNC, PHI2, MS, $\overline{CE}$, D7-D0	V_{SS}	-	0.2xV_{DD}	V
V_R	Data Retention	2.0	-	-	V
I_{in}	Input Current BPCLK, BPSYNC, R/$\overline{W}$, PHI2, D7-D0	-	-	±1	uA
C_{in}	Capacitance R/$\overline{W}$, BPCLK, BPSYNC, PHI2, MS, $\overline{CE}$, D7-D0	-	-	8	pF
I_{OH}	Output current (V_{OH}=4.5V, V_{OL}=0.5V) D7-D0	+20	-	-	uA
I_{OL}		-	-	-20	uA

AC ELECTRICAL CHARACTERISTICS - WRITE CYCLE (V_{DD}=3.0V±10%, V_{SS}=0V)

Symbol	Parameter	Min	Max	Unit
t_{CYCW}	Write Cycle Time	400	-	ns
t_{AS}	Address Set Up Time	100	-	ns
t_{AH}	Address Hold Time	70	-	ns
t_{CS}	Chip Select Pulse Width	260	-	ns
t_{WCS}	Write to Chip Select Delay Time	100	-	ns
t_{DSW}	Data Setup Time	200	-	ns
t_H	Input Hold Time	15	-	ns
t_{WH}	Write Hold Time from Chip Select	70	-	ns

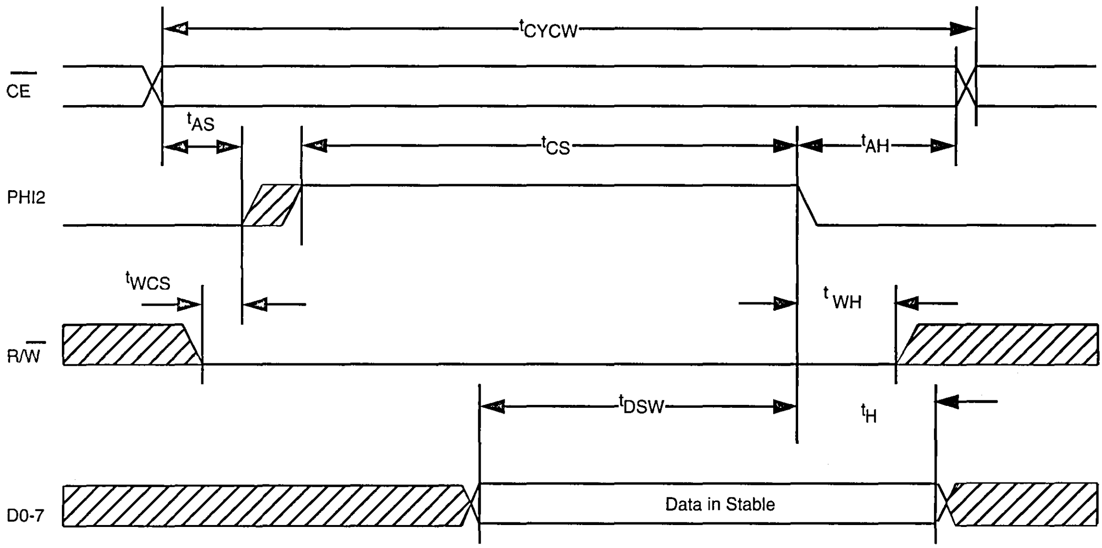


Figure 2. Write Cycle Timing

AC ELECTRICAL CHARACTERISTICS - READ CYCLE (V_{DD}=3.0V±10%, V_{SS}=0V)

Symbol	Parameter	Min	Max	Unit
t_{CYCR}	READ Cycle Time	400	-	ns
t_{AS}	Address Setup Time	100	-	ns
t_{DDR}	Data Delay Time (Read)	-	350	ns
t_H	Output Hold Time	10	-	ns

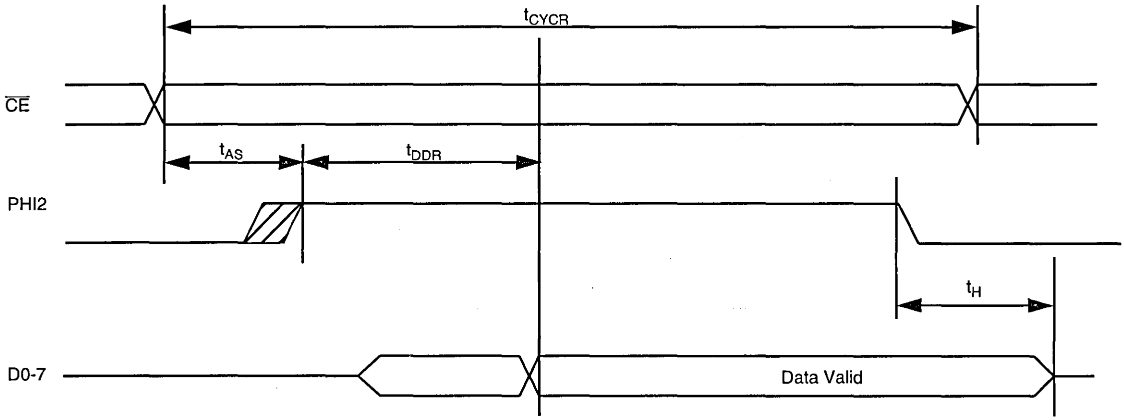


Figure 3. Read Cycle Timing

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

The main dc power is supplied to the part by these two connections. V_{DD} is the most-positive supply level for logic circuitry and V_{SS} is ground.

V_{LCD}

This supply connection provides the voltage level for the segment drivers and is connected to the Vout connection of the MC68HC05L10 MCU.

V_{SEGL}, V_{SEGH}

These inputs are connected to V2 and V3 of an external voltage divider. See Figure 4.

D0 - D7

These connections form an eight bit wide bidirectional data bus which are connected to D0 through D7 of the MC68HC05L10.

A0 - A9

These inputs form a ten-bit wide address bus for addressing the display RAM and are connected to A0 through A9 of the MC68HC05L10.

BPSYNC

This input is a periodic active-low signal from the MC68HC05L10 for timing synchronization. BPSYNC is connected to $\overline{\text{FRM}}$ of MC68HC05L10. See Figure 5.

BPCLK

This input may be run as high as 4.096 kHz (50% duty cycle). It provides the required frame frequency for the segment driver. It is connected to BPCLK of the MC68HC05L10. Thus, the frequency is usually 2.048 kHz. See Figure 5.

PHI2

This input is a bus clock input that is used for data bus timing synchronization. It is connected to P02 of MC68HC05L10.

SEG0 - SEG127

These 128 output lines provide the frontplane drive signals to the LCD panel. These outputs are forced to a low level while display is turned off. Any unused segment outputs should be left open.

$\overline{\text{CE}}$

This is an active low chip enable input and is connected to either $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$ or $\overline{\text{CS4}}$ of the MC68HC05L10.

LRS

The left-right selection input defines the direction of the segment driver display. See Figure 8.
0 or Low = SEG 0 - 127
1 or High = SEG 127 - 0

MS

This input selects how display RAM is addressed. Either a 1:32 or 1:41 multiplex ratio is possible.
0 or Low = 1:32 multiplex addressing
1 or High = 1:41 multiplex addressing

R/$\overline{\text{W}}$

This input indicates which direction the data is to be passed over the data bus. When R/$\overline{\text{W}}$ is low, the LCD driver reads data from the data bus (D0-D7). When R/$\overline{\text{W}}$ is high, the LCD driver writes data to the data bus (D0-D7). This input is connected to R/W of MC68HC05L10.

TEST

Allowing this connection to float or connecting it to VSS (GND) places the part in the normal mode of operation. This input has an on-chip pulldown resistance of approximately 1MΩ.

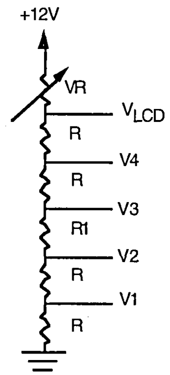


Figure 4. External Voltage Divider

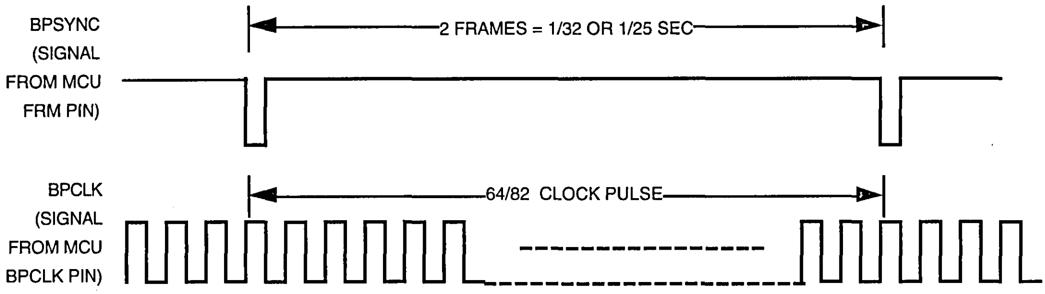


Figure 5. Relationship between BPSYNC and BPCLK

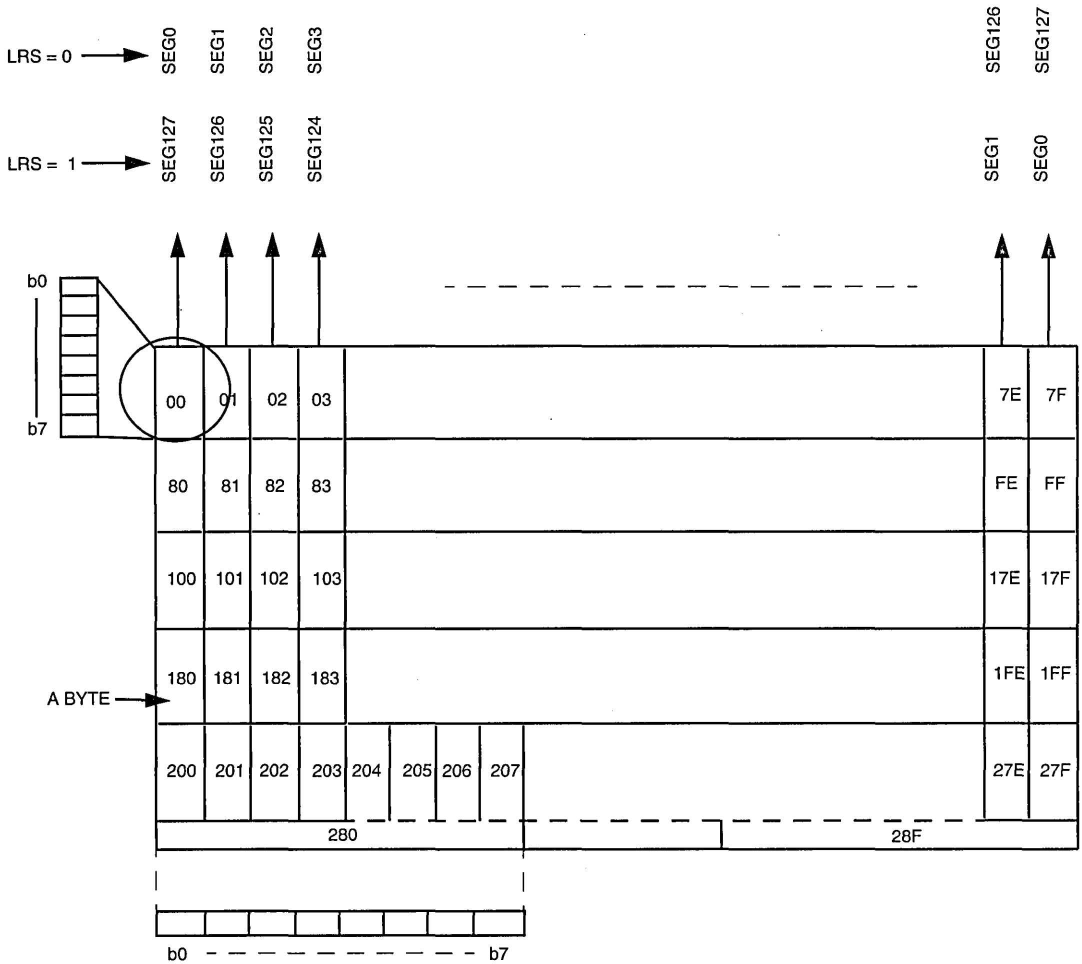


Figure 6. Display RAM Configuration

OPERATION OF LCD DRIVER

INTRODUCTION

The MC141511 is LCD driver with selectable 1: 32 or 1: 41 multiplex ratios. The device consists of the following functional blocks as shown in the Block Diagram.

CONTROL LOGIC - accepts the control signals from the MCU and generates internal signals for synchronisation.

DISPLAY RAM - stores the display data. Each bit of the display RAM has one-to-one correspondence to a pixel of the LCD. The display RAM is in vertical byte oriented format as shown in Figure 6 and the way the display RAM is addressed depends on the multiplexing mode of the LCD (Figure 8). With reference to Figure 6, the display RAM also contains 16 bytes of memory which is in horizontal format ($280-$28F). The display RAM is addressed when backplane reaches 41.

LEVEL SELECTOR - consists of a switching circuit to select appropriate voltage levels from an external voltage divider. See figure 4.

SEGMENT DRIVERS - provides the segment driving signals to the LCD frontplane. See Figure 7.

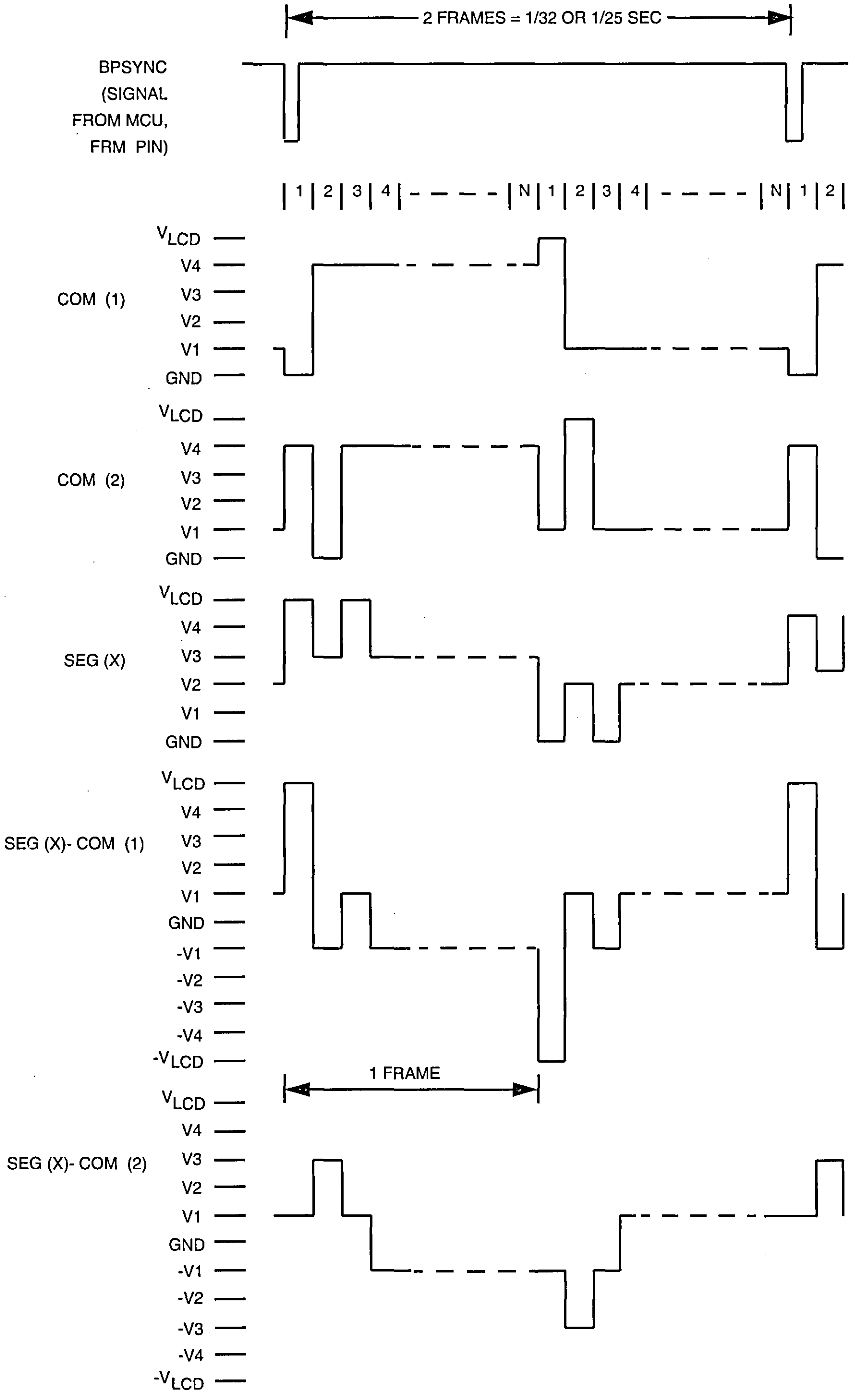
The LCD driver clock is derived from the 2.048KHz BPCLK and frame frequency is 64 Hz for 1:32 multiplex and 50 Hz for 1:41 multiplex ratio. See Figure 5.

GENERATION OF LCD BIAS LEVELS

Refer to Figure 4. In order to obtain optimum contrast for LCD panels, the bias levels should be selected such that

$$BIAS = R/(4R+R1) = 1/(\sqrt{MUX} + 1)$$
$$V1/VLCD = 1/(\sqrt{MUX} + 1)$$
$$V2/VLCD = 2/(\sqrt{MUX} + 1)$$
$$V3/VLCD = (\sqrt{MUX} - 1)/(\sqrt{MUX} + 1)$$
$$V4/VLCD = \sqrt{MUX}/(\sqrt{MUX} + 1)$$

Example: Mux = 41 ----- Bias = 1: 7.4,
R = 10K, R1 = 33K, VR = 100K
Mux = 32 ----- Bias = 1: 6.6,
R = 10K, R1 = 27K, VR = 100K



N = 32, 41

Figure. 7 Driving Waveform of 1:5 Bias, 1:32 or 1:41 Multiplex Ratio

$200 - $27F
$280 - $2FF
$300 - $37F
$380 - $3FF

1 : 32

$1C0 - $1CF
$200 - $27F
$280 - $2FF
$300 - $37F
$380 - $3FF
$400 - $47F

1 : 41

ONE SLAVE

$200 - $27F	$400 - $47F
$280 - $2FF	$480 - $4FF
$300 - $37F	$500 - $57F
$380 - $3FF	$580 - $5FF

1 : 32

$1C0 - $1CF	$1D0 - $1DF
$200 - $27F	$480 - $4FF
$280 - $2FF	$500 - $57F
$300 - $37F	$580 - $5FF
$380 - $3FF	$600 - $67F
$400 - $47F	$680 - $6FF

1 : 41

TWO SLAVES

$200 - $27F	$400 - $47F	$600 - $67F
$280 - $2FF	$480 - $4FF	$680 - $6FF
$300 - $37F	$500 - $57F	$700 - $77F
$380 - $3FF	$580 - $5FF	$780 - $7FF

1 : 32

$1C0 - $1CF	$1D0 - $1DF	$1E0 - $1EF
$200 - $27F	$480 - $4FF	$700 - $77F
$280 - $2FF	$500 - $57F	$780 - $7FF
$300 - $37F	$580 - $5FF	$800 - $87F
$380 - $3FF	$600 - $67F	$880 - $8FF
$400 - $47F	$680 - $6FF	$900 - $97F

1 : 41

THREE SLAVES

$200 - $27F	$400 - $47F	$600 - $67F	$800 - $87F
$280 - $2FF	$480 - $4FF	$680 - $6FF	$880 - $8FF
$300 - $37F	$500 - $57F	$700 - $77F	$900 - $97F
$380 - $3FF	$580 - $5FF	$780 - $7FF	$980 - $9FF

1 : 32

$1C0 - $1CF	$1D0 - $1DF	$1E0 - $1EF	$1F0 - $1FF
$200 - $27F	$480 - $4FF	$700 - $77F	$980 - $9FF
$280 - $2FF	$500 - $57F	$780 - $7FF	$A00 - $A7F
$300 - $37F	$580 - $5FF	$800 - $87F	$A80 - $AFF
$380 - $3FF	$600 - $67F	$880 - $8FF	$B00 - $B7F
$400 - $47F	$680 - $6FF	$900 - $97F	$B80 - $BFF

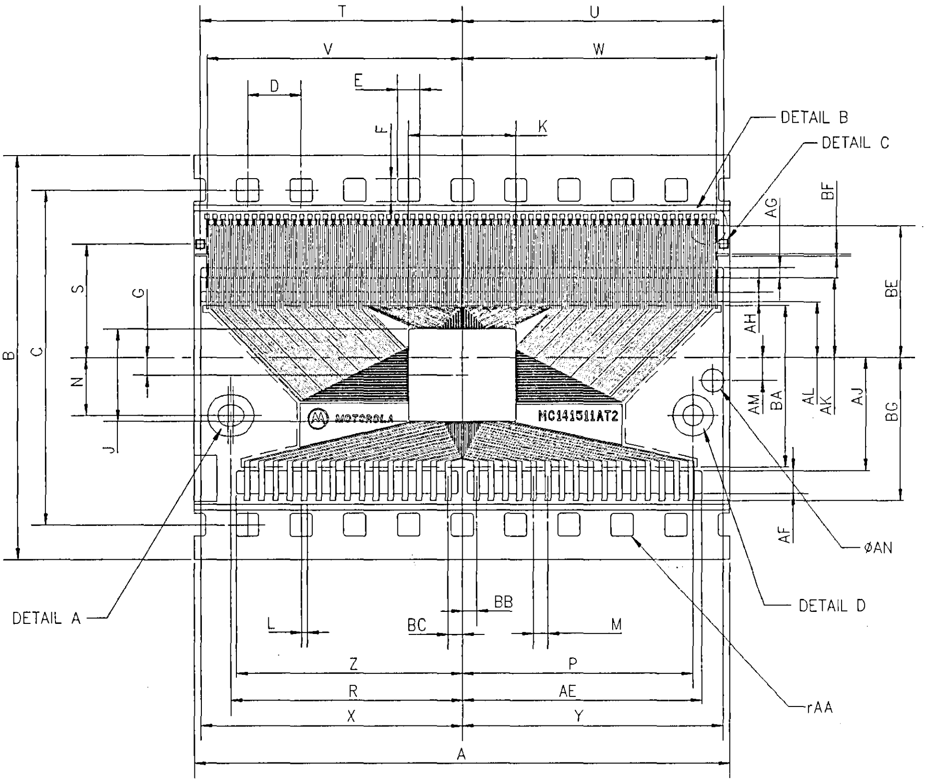
1 : 41

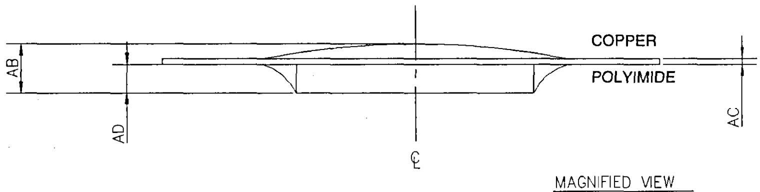
FOUR SLAVES

Figure 8. Display RAM Mapping for 1:32 and 1:41 Multiplex Ratio

PACKAGE DIMENSIONS

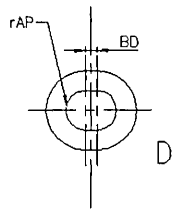
MC141511AT2
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



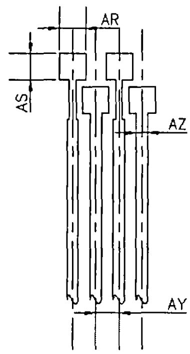


Reference: 98ASL00183A	Issue “A” released on 04/15/96

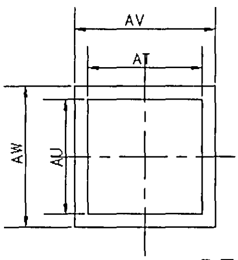
MC141511AT2
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



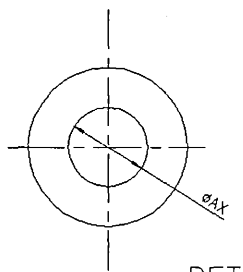
DETAIL "A"



DETAIL "B"



DETAIL "C"



DETAIL "D"

Reference: 98ASL00183A	Issue "A" released on 04/15/96

MC141511AT2 TAB PACKAGE DIMENSION

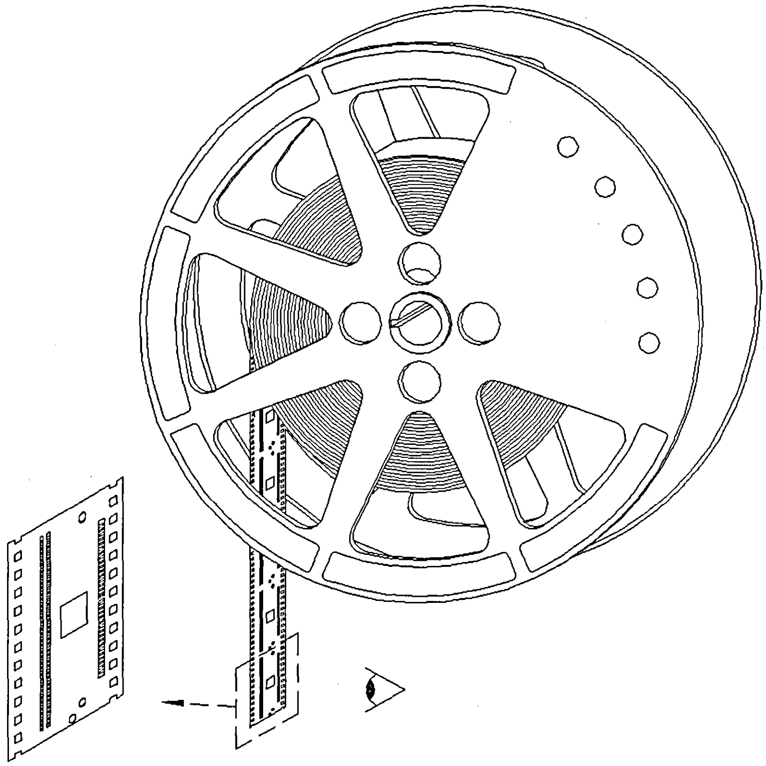
	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	46.55	47.55	1.8327	1.8720	AE	21.25	21.35	0.8366	0.8406
B	34.775	35.175	1.3691	1.3848	AF	1.95	2.05	0.0768	0.0807
C	28.947	29.007	1.1396	1.1420	AG	0.85	0.95	0.0335	0.0374
D	4.72	4.78	0.1858	0.1882	AH	0.85	0.95	0.0335	0.0374
E	1.951	2.011	0.0768	0.0792	AJ	9.75	9.85	0.3839	0.3878
F	1.951	2.011	0.0768	0.0792	AK	6.85	6.95	0.2697	0.2736
G	1	2	0.0394	0.0787	AL	4.75	4.85	0.1870	0.1909
H	-	-	-	-	AM	1.95	2.05	0.0768	0.0807
J	7.469	8.469	0.2941	0.3334	AN	1.95	2.05	0.0768	0.0807
K	9.04	10.04	0.3559	0.3953	AP	0.085	0.095	0.0033	0.0037
L	0.48	0.52	0.0189	0.0205	AR	0.35	0.45	0.0014	0.0177
M	1.26	1.28	0.0496	0.0504	AS	0.35	0.45	0.0014	0.0177
N	4.95	5.05	0.1949	0.1988	AT	0.6	0.7	0.0236	0.0276
P	20.45	20.55	0.8051	0.8091	AU	0.6	0.7	0.0236	0.0276
R	20.45	20.55	0.8051	0.8091	AV	0.75	0.85	0.0295	0.0335
S	9.78	9.88	0.3850	0.3890	AW	0.75	0.85	0.0295	0.0335
T	23.155	23.255	0.9116	0.9156	AX	1.75	1.85	0.0689	0.0728
U	23.155	23.255	0.9116	0.9156	AY	0.34	0.36	0.0134	0.0142
V	22.53	22.62	0.8870	0.8905	AZ	0.15	0.19	0.0059	0.0075
W	22.53	22.62	0.8870	0.8905	BA	13.7	14.3	0.5394	0.5630
X	23.1	23.2	0.9094	0.9134	BB	1.22	1.32	0.0480	0.0520
Y	23.1	23.2	0.9094	0.9134	BC	1.22	1.32	0.0480	0.0520
Z	19.95	20.05	0.7854	0.7894	BD	0.45	0.55	0.0177	0.0217
AA	-	0.2	-	0.0079	BE	11.35	11.45	0.4469	0.4508
AB	0.686	0.838	0.027	0.033	BF	0.12	0.22	0.0047	0.0087
AC	0.068	0.063	0.0027	0.0024	BG	12.35	12.45	0.4862	0.4902
AD	0.579	0.629	0.0227	0.0247					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter
3. Copper thickness: 1 oz

Reference: 98ASL00183A	Issue “A” released on 04/15/96

MC141511AT2

TAB TAPE REEL ORIENTATION



Reference: 98ASL00183A	Issue "A" released on 04/15/96

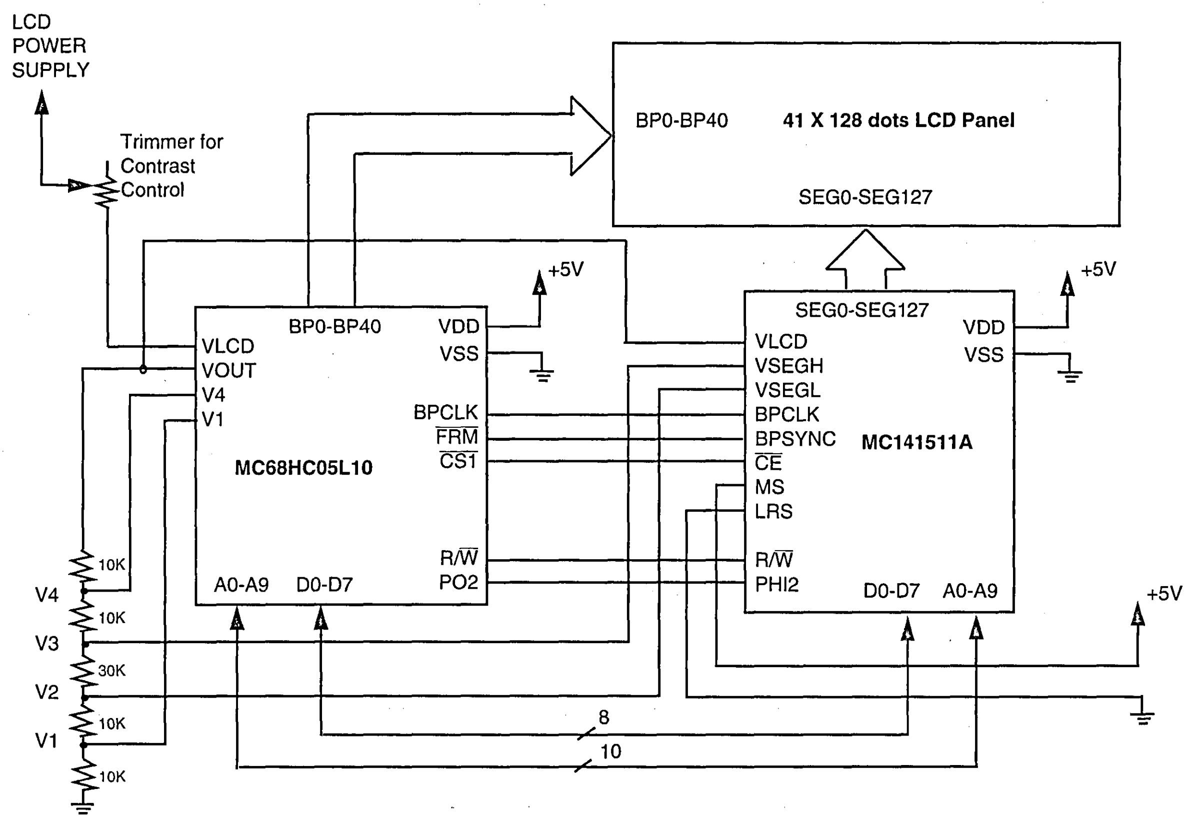
MCC141511A PAD COORDINATES
(UNIT: um)

Pin Name	X	Y	Pin Name	X	Y	Pin Name	X	Y	Pin Name	X	Y
VDD	-1874.62	-2498.76	SEG126	2728.66	-2233.88	SEG86	2630.76	2432.32	SEG39	-2728.66	2227.72
TEST	-1738.66	-2498.76	SEG125	2728.66	-2119.48	SEG85	2516.36	2432.32	SEG38	-2728.66	2113.32
BPSYNC	-1611.06	-2498.76	SEG124	2728.66	-2005.08	SEG84	2401.96	2432.32	SEG37	-2728.66	1998.92
BPCLK	-1483.46	-2498.76	SEG123	2728.66	-1890.68	SEG83	2287.56	2432.32	SEG36	-2728.66	1884.52
MS	-1355.86	-2498.76	SEG122	2728.66	-1776.28	SEG82	2173.16	2432.32	SEG35	-2728.66	1770.12
PHI2	-1228.26	-2498.76	SEG121	2728.66	-1661.88	SEG81	2058.76	2432.32	SEG34	-2728.66	1655.72
$\overline{CE}$	-1100.66	-2498.76	SEG120	2728.66	-1547.48	SEG80	1944.36	2432.32	SEG33	-2728.66	1541.32
R$\overline{W}$	-973.06	-2498.76	SEG119	2728.66	-1433.08	SEG79	1829.96	2432.32	SEG32	-2728.66	1426.92
A9	-845.46	-2498.76	SEG118	2728.66	-1318.68	SEG78	1715.56	2432.32	SEG31	-2728.66	1312.52
A8	-717.86	-2498.76	SEG117	2728.66	-1204.28	SEG77	1601.16	2432.32	SEG30	-2728.66	1198.12
A7	-590.26	-2498.76	SEG116	2728.66	-1089.88	SEG76	1486.76	2432.32	SEG29	-2728.66	1083.72
A6	-462.66	-2498.76	SEG115	2728.66	-975.48	SEG75	1372.36	2432.32	SEG28	-2728.66	969.32
A5	-335.06	-2498.76	SEG114	2728.66	-861.08	SEG74	1257.96	2432.32	SEG27	-2728.66	854.92
A4	-207.46	-2498.76	SEG113	2728.66	-746.68	SEG73	1143.56	2432.32	SEG26	-2728.66	740.52
A3	-79.86	-2498.76	SEG112	2728.66	-632.28	SEG72	1029.16	2432.32	SEG25	-2728.66	626.12
A2	47.74	-2498.76	SEG111	2728.66	-517.88	SEG71	914.76	2432.32	SEG24	-2728.66	511.72
A1	175.34	-2498.76	SEG110	2728.66	-403.48	SEG70	800.36	2432.32	SEG23	-2728.66	397.32
A0	302.94	-2498.76	SEG109	2728.66	-289.08	SEG69	685.96	2432.32	SEG22	-2728.66	282.92
LRS	430.54	-2498.76	SEG108	2728.66	-174.68	SEG68	571.56	2432.32	SEG21	-2728.66	168.52
D0	558.14	-2498.76	SEG107	2728.66	-60.28	SEG67	457.16	2432.32	SEG20	-2728.66	54.12
D1	685.74	-2498.76	SEG106	2728.66	54.12	SEG66	342.76	2432.32	SEG19	-2728.66	-60.28
D2	813.34	-2498.76	SEG105	2728.66	168.52	SEG65	228.36	2432.32	SEG18	-2728.66	-174.68
D3	940.94	-2498.76	SEG104	2728.66	282.92	SEG64	113.96	2432.32	SEG17	-2728.66	-289.08
D4	1068.54	-2498.76	SEG103	2728.66	397.32	SEG63	-0.44	2432.32	SEG16	-2728.66	-403.48
D5	1196.14	-2498.76	SEG102	2728.66	511.72	SEG62	-114.84	2432.32	SEG15	-2728.66	-517.88
D6	1323.74	-2498.76	SEG101	2728.66	626.12	SEG61	-229.24	2432.32	SEG14	-2728.66	-632.28
D7	1451.12	-2498.76	SEG100	2728.66	740.52	SEG60	-343.64	2432.32	SEG13	-2728.66	-746.68
VLCD	1578.94	-2498.76	SEG99	2728.66	854.92	SEG59	-458.04	2432.32	SEG12	-2728.66	-861.08
VSEGH	1706.54	-2498.76	SEG98	2728.66	969.32	SEG58	-572.44	2432.32	SEG11	-2728.66	-975.48
VSEGL	1834.14	-2498.76	SEG97	2728.66	1083.72	SEG57	-686.84	2432.32	SEG10	-2728.66	-1089.88
VSS	1979.78	-2498.76	SEG96	2728.66	1198.12	SEG56	-801.24	2432.32	SEG9	-2728.66	-1204.28
DUMPAD 4	2111.78	-2498.76	SEG95	2728.66	1312.52	SEG55	-915.64	2432.32	SEG8	-2728.66	-1318.68
DUMPAD 3	2239.38	-2498.76	SEG94	2728.66	1426.92	SEG54	-1030.04	2432.32	SEG7	-2728.66	-1433.08
DUMPAD 2	2366.98	-2498.76	SEG93	2728.66	1541.32	SEG53	-1144.44	2432.32	SEG6	-2728.66	-1547.48
DUMPAD 1	2494.58	-2498.76	SEG92	2728.66	1655.72	SEG52	-1258.84	2432.32	SEG5	-2728.66	-1661.88
SEG127	2619.54	-2498.76	SEG91	2728.66	1770.12	SEG51	-1373.24	2432.32	SEG4	-2728.66	-1776.28
			SEG90	2728.66	1884.52	SEG50	-1487.64	2432.32	SEG3	-2728.66	-1890.68
			SEG89	2728.66	1998.92	SEG49	-1602.04	2432.32	SEG2	-2728.66	-2005.08
			SEG88	2728.66	2113.32	SEG48	-1716.44	2432.32	SEG1	-2728.66	-2119.48
			SEG87	2728.66	2227.72	SEG47	-1830.84	2432.32	SEG0	-2728.66	-2233.88
						SEG46	-1945.24	2432.32			
						SEG45	-2059.64	2432.32			
						SEG44	-2174.04	2432.32			
						SEG43	-2288.44	2432.32			
						SEG42	-2402.84	2432.32			
						SEG41	-2517.24	2432.32			
						SEG40	-2631.64	2432.32			

Die Size : 240.0 x 212.0 mil^2
Pad Pitch : 4.5 mil
Note : 1 mil ~ 25.4 µm
DUMPAD 1-4: Dummy pad without connections to internal circuitry

TYPICAL APPLICATIONS

128 X 41 SINGLE PANEL LCD SYSTEM WITH MC68HC05L10



Note : Full capability of MC68HC05L10 can control up to four MC141511A slave LCD drivers with 41 x 512 dots LCD panel. Refer to application note, MC68HC05L10 AN ENHANCED VERSION OF L9 FOR HANDHELD EQUIPMENT APPLICATIONS (AN-HK-13A) for more details.

LCD Backplane Drivers

CMOS

MC141512
MC141515

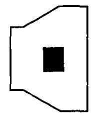
The MC141512 and MC141515 are high voltage passive LCD backplane driver chips. The MC141512 provides 80 high voltage LCD driving signals whereas the MC141515 provides 160 high voltage LCD driving signals.

They are companion chips to the MC141514 and MC141519 LCD segment driver for medium size LCD panels. All these chips are controlled by the MC68HC05L11 microcomputer.

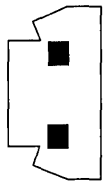
The MC141515T is the twin die version of the MC141512T.

See Application Note AN-HK-15.

- Operating Supply Voltage Range -
  - Control Logic (V_{DD} Pin): 2.7V to 5.5V
  - Backplane Drivers (V_{LCD} Pin): 10V to 25V
- Operating Temperature Range: -25 to 70°C
- Direct Serial Data Interface with the MC68HC05L11
- MC141512 - 80 LCD Backplane Driving Signals
- MC141515 - 160 LCD Backplane Driving Signals
- 1:5 to 1:13 Bias
- Expansion to Higher Driver Count by Cascade
- Available in Three Forms:
  - TAB (Tape Automated Bonding), 91 Contacts - MC141512T1
  - 182 Contacts - MC141515T
  - Die Form Without Gold Bumps, 91 Pads with 4.3 mil Pads Pitch



MC141512T1
TAB



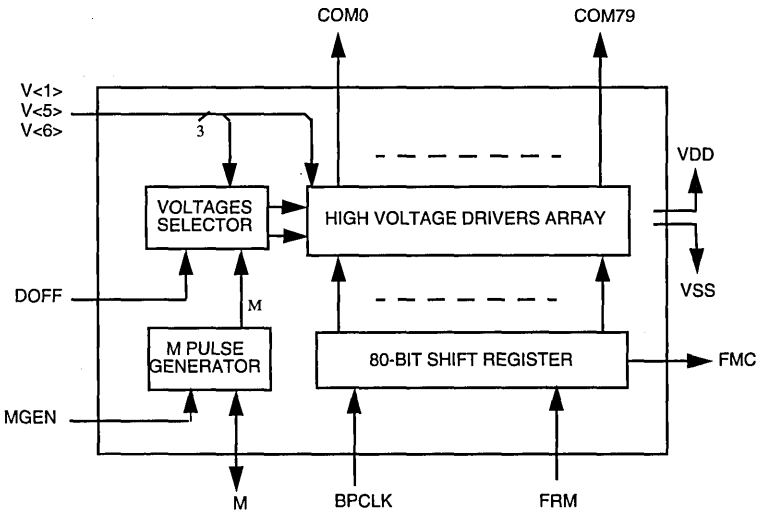
MC141515T
TAB

MCC141512
DIE

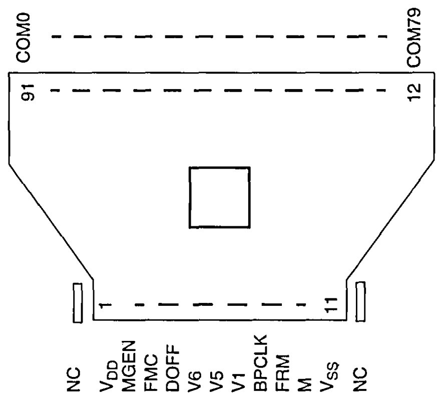
ORDERING INFORMATION

MC141512T1	TAB
MC141515T	TAB
MCC141512	BARE DIE

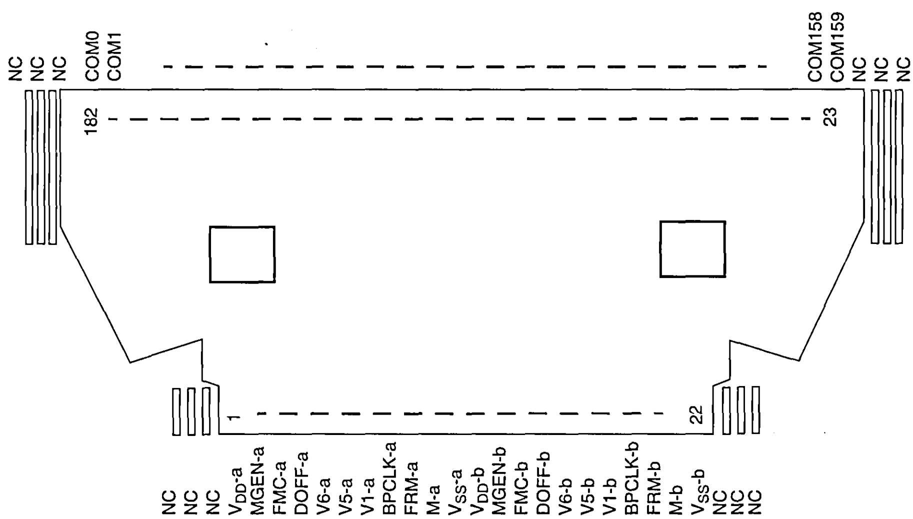
BLOCK DIAGRAM



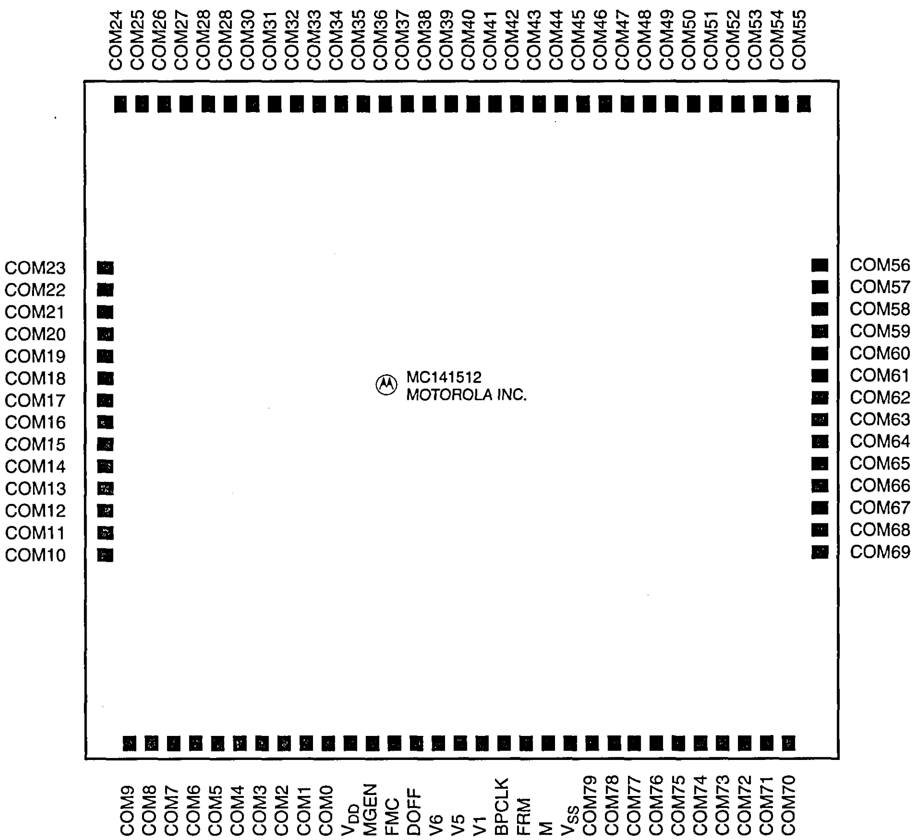
REV 4
10/96



MC141512T1 TAB Package Contact Assignment (Copper View)



MC141515T TAB Package Contact Assignment (Copper View)



Chip Pad Assignment

MAXIMUM RATINGS*(Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
$V_{<1>}$		-0.3 to +27.5	V
V_{in}	Input Voltage	-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-25 to +75	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

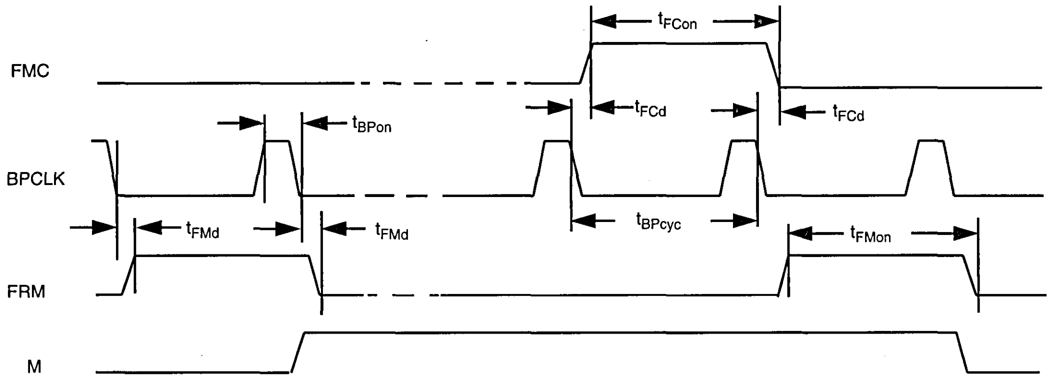
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD} = 5.0V, $V_{<1>}$ = 25V, T_A = -25 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD} $V_{<1>}$	Supply Voltage Range LCD Supply Voltage Range	(Absolute value reference to V_{SS})	2.7 +10.0	- -	5.5 +25.0	V V
I_{DP}	Display Mode Supply Current (V_{DD} Pin)	BPCLK = 8KHz	-	1	10	uA
I_{SB}	Standby Mode Supply Current (V_{DD} Pin)	Using D_{ON} bit of the MCU	-	0.5	1	uA
I_{LDP}	Display Mode Supply Current ($V_{<1>}$ Pin)	BPCLK = 8KHz	-	3	10	uA
I_{LSB}	Standby Mode Supply Current ($V_{<1>}$ Pin)	BPCLK = 8KHz	-	0.5	1	uA
V_{OL} V_{OH}	Output Low Voltage Output High Voltage (M, FMC)	No Load	V_{SS} 0.8 x V_{DD}	- -	0.2 x V_{DD} V_{DD}	V V
V_{IH} V_{IL}	Input High Voltage Input Low Voltage (BPCLK, FRM, M, DOFF, FMC, MGEN)		0.7xV_{DD} V_{SS}	- -	V_{DD} 0.3xV_{DD}	V V
I_{in}	Input Current (BPCLK, FRM, M, DOFF, FMC, MGEN)		-	-	±1	uA
C_{in}	Input Capacitance (BPCLK, FRM, M, DOFF, FMC)		-	-	8	pF
I_{OH} I_{OL}	Output High Current Output Low Current (M, FMC)	V_{OH}= 4.5V V_{OL}= 0.5V	+100 -	- -	- -100	uA uA

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.7 - 5.0V, V_{SS} = 0V, T_A = 25˚C)

Symbol	Parameter	Min	Max	Unit
t_{FCon}	Carry Out Frame On Time	122	-	us
t_{FCd}	Carry Out Frame Delay Time	10	100	ns
t_{BPon}	BPCLK Pulse On Time	61	-	us
t_{BPcyc}	BPCLK Cycle Period	61	-	us
t_{FMd}	Frame Delay Time	10	100	ns
t_{FMon}	Frame Pulse On Time	122	-	us



Timing Diagram

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>, V<5>, V<6>

These are the levels of voltage generated from an external voltages divider (Fig. 1).

DOFF

This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD. If this signal is clear, the backplane driver will supply LCD with driving signal. If this signal is set, the backplane driver outputs will be high-impedanced and LCD display is disabled.

FRM

A periodic active high input to the backplane driver for frame timing synchronization which is connected to FRM of MC68HC05L11.

BPCLK

A periodic output from MC68HC05L11 to backplane driver for timing synchronization. The signal will affect the refreshing time of LCD display.

FMC

This is an output pin of backplane driver which is connected to the FRM of the next backplane driver in case of cascading.

M

This pin is for synchronization between the display driver. When MGEN is set, it will generate an M signal for synchronization. When MGEN is clear, it becomes an input pin and expecting a M signal from other device.

MGEN

An input which is used for program the M pin as an input or output. If MGEN is logic high, M acts as an output. If MGEN is logic low, M becomes an input.

COM 0 - 79

These are the high voltage outputs of the backplane driver which are connected to set of common lines of any LCD panel.

OPERATION OF LCD DRIVER

INTRODUCTION

The LCD backplane driver can support multiplex ratio of a LCD system up to 146 and cascading of more than one driver for expansion is possible. It can be set from 1:5 bias (for 16 mux) to 1:13 bias (for 146 mux), by the voltage divider ratio of Fig.1. The ratio of bias or the contrast ratio (a) is defined as

$$1 : \frac{4 \times R1 + R2}{R1} = 1 : a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a = \sqrt{mux} + 1$$

To set up a multiplex ratio, please refer to MC68HC05L11 technical data Section 10.6.2.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from external voltage divider. (See Fig. 1).

80-BIT SHIFT REGISTER samples the FRM at the falling edge of BPCLK and shifts the sample to the left 80 times before exports to the next backplane driver through FMC.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Com(1) and Com(2)are shown in Figure 2.

POWER UP SYNCHRONIZATION is activated upon the receipt the first M pulse. The M pin of the backplane driver will act as an input when MGEN is connected to Low. When MGEN is Set, this backplane driver will be the master of the synchronization system. M pin will then supply a periodic signal for all LCD drivers.

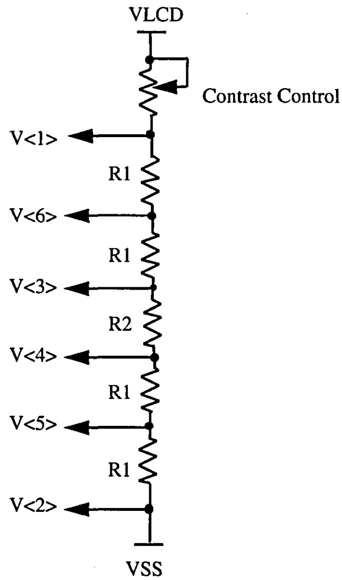


Figure 1. External Voltage Divider

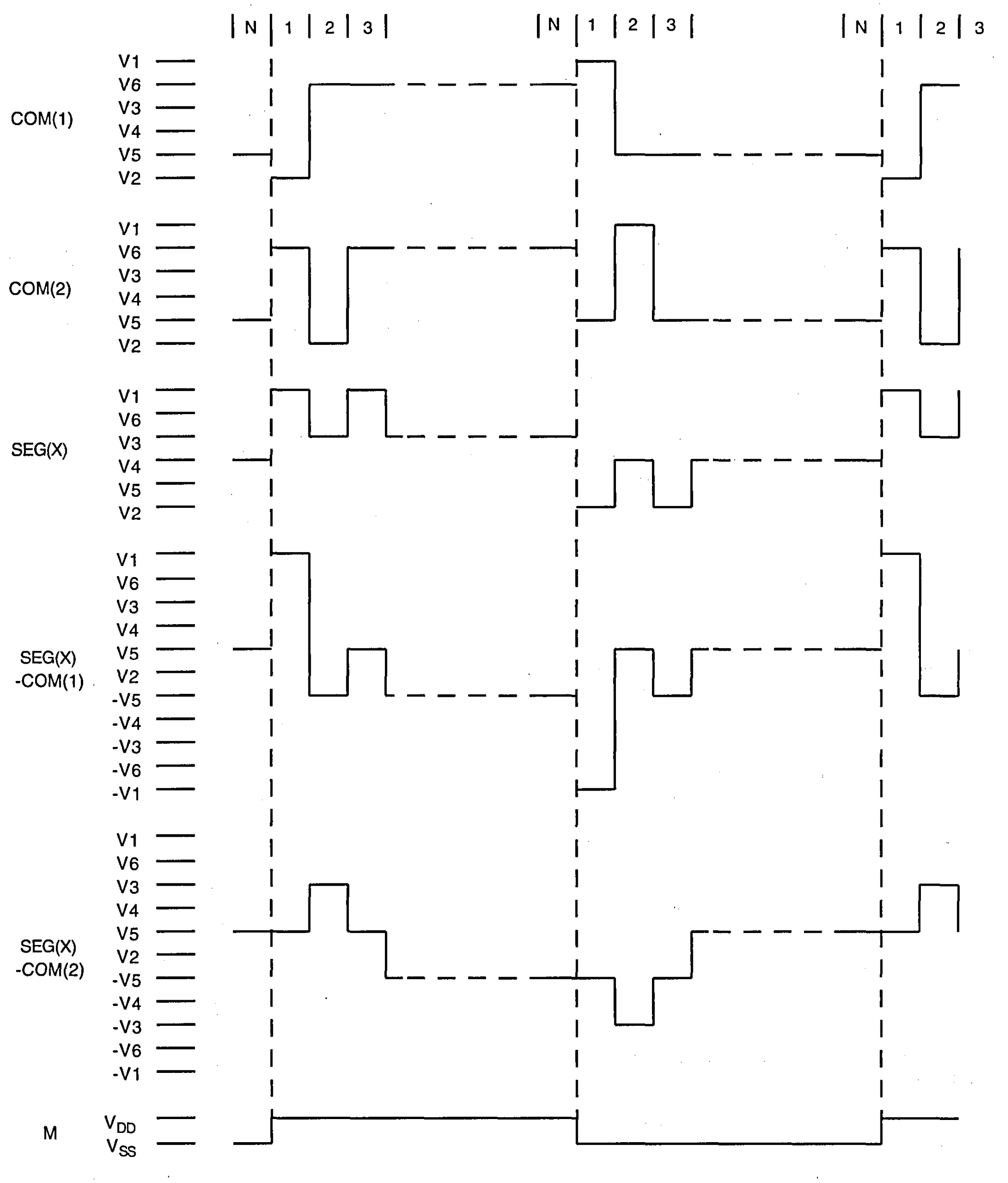
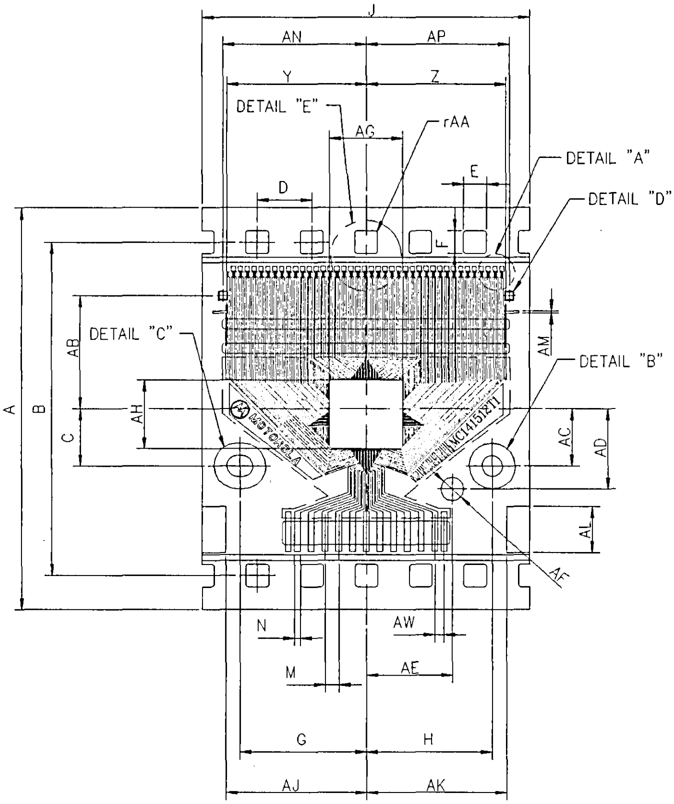
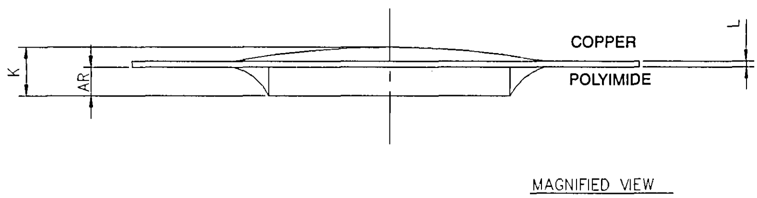


Figure 2. Driving Waveforms of 1:N Multiplex Ratio

PACKAGE DIMENSIONS

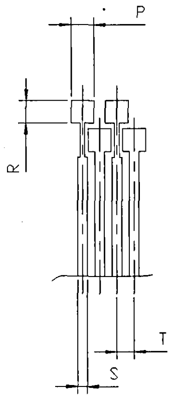
MC141512T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



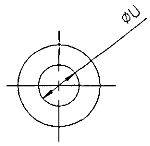


Reference : 98ASL00103A	Issue "A" released on 03/21/94

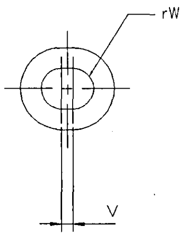
MC141512T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



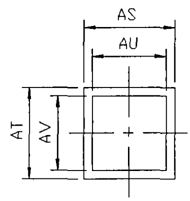
DETAIL "A"



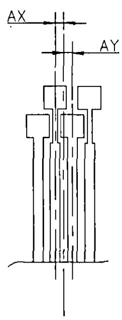
DETAIL "B"



DETAIL "C"



DETAIL "D"



DETAIL "E"

Reference: 98ASL00103A	Issue "A" released on 03/21/94

MC141512T1 TAB PACKAGE DIMENSION

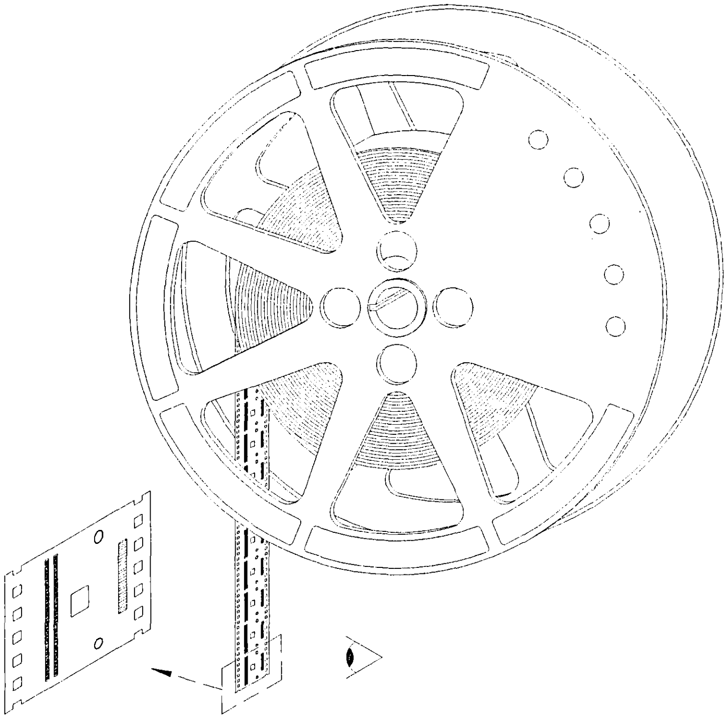
	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	34.775	35.175	1.369	1.385	AE	7.000	8.000	0.2756	0.3150
B	28.907	29.017	1.138	1.142	AF	1.950	2.050	0.0768	0.0807
C	4.950	5.050	0.195	0.199	AG	-	6.410	-	0.2524
D	4.700	4.800	0.185	0.189	AH	-	5.968	-	0.2350
E	1.951	2.011	0.077	0.079	AJ	11.750	12.750	0.4626	0.5020
F	1.951	2.011	0.077	0.079	AK	11.750	12.750	0.4626	0.5020
G	10.950	11.050	0.431	0.435	AL	3.950	4.050	0.1555	0.1594
H	10.950	11.050	0.431	0.435	AM	0.150	0.190	0.0059	0.0075
J	28.00	29.000	1.102	1.142	AN	12.430	12.530	0.4894	0.4933
K	0.686	0.838	0.027	0.033	AP	12.430	12.530	0.4894	0.4933
L	0.0675	0.0825	0.0027	0.0032	AR	0.5794	0.6294	0.0228	0.0248
M	1.190	1.210	0.047	0.048	AS	0.750	0.850	0.0295	0.0335
N	0.480	0.520	0.019	0.020					
P	0.380	0.420	0.015	0.016					
R	0.380	0.420	0.015	0.016					
S	0.150	0.190	0.006	0.007					
T	0.290	0.310	0.011	0.012					
U	1.750	1.850	0.069	0.073					
V	0.480	0.520	0.019	0.020					
W	0.880	0.920	0.035	0.036					
Y	12.100	12.200	0.4764	0.4803					
Z	12.100	12.200	0.4764	0.4803					
AA	-	0.200	-	0.008					
AB	9.778	9.878	0.3850	0.3889					
AC	4.950	5.050	0.1949	0.1988					
AD	6.500	7.500	0.2559	0.2953					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter
3. Cu thickness: 1 oz
4. Tin plating thickness: 0.4μm

Reference: 98ASL00103A	Issue "A" released on 03/21/94

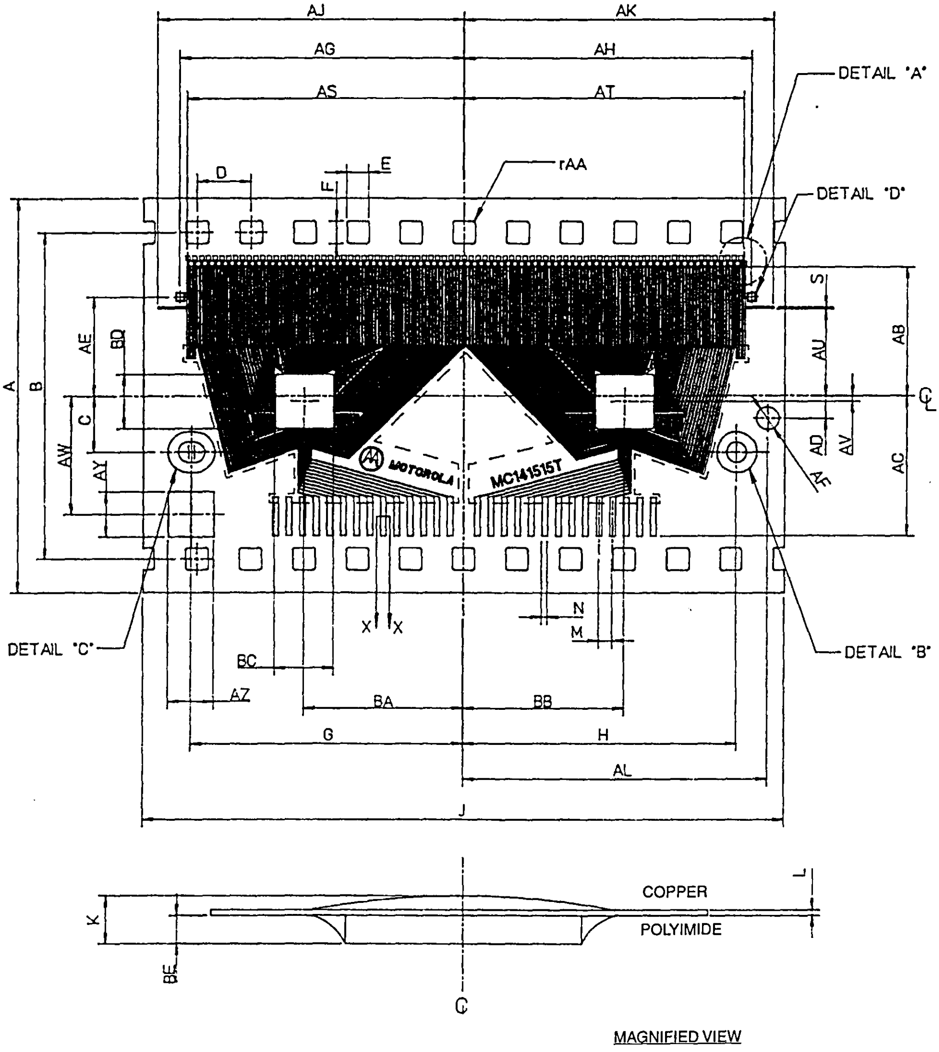
MC141512T1

TAB TAPE REEL ORIENTATION



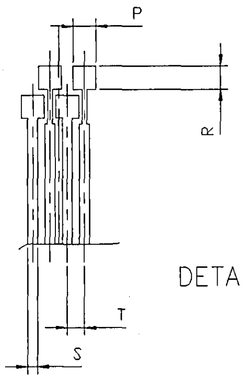
Reference: 98ASL00103A	Issue "A" released on 03/21/94

MC141515T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



Reference: 98ASL00053A	Issue "A" released on 02/28/93

MC141515T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



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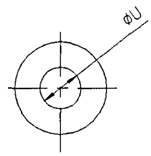

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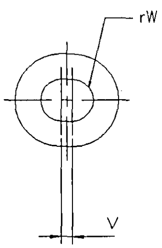
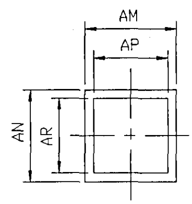
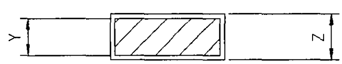


DETAIL "C"



DETAIL "D"



SECTION X–X

Reference: 98ASL00053A	Issue "A" released on 02/28/93

MC141515T TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	34.775	35.175	1.3691	1.3848	AE	8.730	8.750	0.3437	0.3445
B	28.907	29.017	1.1381	1.1424	AF	1.950	2.050	0.0768	0.0807
C	4.950	5.050	0.1949	0.1988	AG	25.250	25.270	0.9941	0.9949
D	4.700	4.800	0.1850	0.1890	AH	25.550	25.570	1.0059	1.0067
E	1.951	2.011	0.0768	0.0792	AJ	27.135	27.235	1.0683	1.0722
F	1.951	2.011	0.0768	0.0792	AK	27.435	27.485	1.0801	1.0821
G	24.200	24.300	0.9528	0.9567	AL	26.950	27.050	1.0610	1.0650
H	24.200	24.300	0.9528	0.9567	AM	0.750	0.850	0.0295	0.0335
J	56.900	57.100	2.2402	2.2480	AN	0.75	0.850	0.0295	0.0335
K	0.686	0.838	0.0270	0.0330	AP	0.600	0.700	0.0236	0.0276
L	0.0675	0.0825	0.0027	0.0033	AR	0.600	0.700	0.0236	0.0276
M	1.190	1.210	0.0469	0.0476	AS	24.590	24.610	0.9681	0.9689
N	0.480	0.520	0.0189	0.0205	AT	24.890	24.910	0.9799	0.9807
P	0.380	0.420	0.0150	0.0165	AU	7.705	7.725	0.3034	0.3041
R	0.380	0.420	0.0150	0.0165	AV	0.450	0.550	0.0177	0.0217
S	0.150	0.190	0.3850	0.3890	AW	10.450	10.550	0.4114	0.4154
T	0.29	0.310	0.0114	0.0122	AY	3.95	4.050	0.1555	0.1595
U	1.780	1.820	0.0701	0.0717	AZ	3.95	4.050	0.1555	0.1595
V	0.480	0.520	0.0189	0.0205	BA	14.200	14.300	0.5591	0.5630
W	0.880	0.920	0.0347	0.0362	BB	14.200	14.300	0.5591	0.5630
Y	0.032	0.038	0.0013	0.0015	BC	-	6.410	-	0.2524
Z	0.032	0.038	0.0013	0.0015	BD	-	5.500	-	0.2165
AA	-	0.2	-	0.0079	BE	0.4326	0.5326	0.0170	0.0210
AB	11.300	11.500	0.4449	0.4527					
AC	12.300	12.500	0.4843	0.4921					
AD	1.950	2.050	0.0768	0.0807					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter
3. Recommended excise area Jx(AB+AC)

Reference: 98ASL00053A	Issue "A" released on 02/28/93

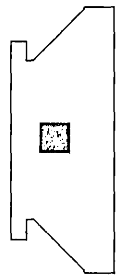
MCC141512 PAD COORDINATES
(UNIT: um)

Pin Name	X	Y	Pin Name	X	Y	Pin Name	X	Y	Pin Name	X	Y
COM9	1687.50	1688.00	COM69	-1841.50	935.00	COM55	-1743.50	-1688.00	COM23	1841.50	-527.50
COM8	1575.00	1688.00	COM68	-1841.50	822.50	COM54	-1631.00	-1688.00	COM22	1841.50	-415.00
COM7	1462.50	1688.00	COM67	-1841.50	710.00	COM53	-1518.50	-1688.00	COM21	1841.50	-302.50
COM6	1350.00	1688.00	COM66	-1841.50	597.50	COM52	-1406.00	-1688.00	COM20	1841.50	-190.00
COM5	1237.50	1688.00	COM65	-1841.50	485.00	COM51	-1293.50	-1688.00	COM19	1841.50	-77.50
COM4	1125.00	1688.00	COM64	-1841.50	372.50	COM50	-1181.00	-1688.00	COM18	1841.50	35.00
COM3	1012.50	1688.00	COM63	-1841.50	260.00	COM49	-1068.50	-1688.00	COM17	1841.50	147.50
COM2	900.00	1688.00	COM62	-1841.50	147.50	COM48	-956.00	-1688.00	COM16	1841.50	260.00
COM1	787.50	1688.00	COM61	-1841.50	35.00	COM47	-843.50	-1688.00	COM15	1841.50	372.50
COM0	675.00	1688.00	COM60	-1841.50	-77.50	COM46	-731.00	-1688.00	COM14	1841.50	485.00
VDD	562.50	1688.00	COM59	-1841.50	-190.00	COM45	-618.50	-1688.00	COM13	1841.50	597.50
MGEN	450.00	1688.00	COM58	-1841.50	-302.50	COM44	-506.00	-1688.00	COM12	1841.50	710.00
FMC	337.50	1688.00	COM57	-1841.50	-415.00	COM43	-393.50	-1688.00	COM11	1841.50	822.50
DOFF	225.00	1688.00	COM56	-1841.50	-527.50	COM42	-281.00	-1688.00	COM10	1841.50	935.00
V6	112.50	1688.00				COM41	-168.50	-1688.00			
V5	0.00	1688.00				COM40	-56.00	-1688.00			
V1	-112.50	1688.00				COM39	56.50	-1688.00			
BPCLK	-225.00	1688.00				COM38	169.00	-1688.00			
FRM	-337.50	1688.00				COM37	281.50	-1688.00			
M	-450.00	1688.00				COM36	394.00	-1688.00			
VSS	-562.50	1688.00				COM35	506.50	-1688.00			
COM79	-675.00	1688.00				COM34	619.00	-1688.00			
COM78	-787.50	1688.00				COM33	731.50	-1688.00			
COM77	-900.00	1688.00				COM32	844.00	-1688.00			
COM76	-1012.50	1688.00				COM31	956.50	-1688.00			
COM75	-1125.00	1688.00				COM30	1069.00	-1688.00			
COM74	-1237.50	1688.00				COM29	1181.50	-1688.00			
COM73	-1350.00	1688.00				COM28	1294.00	-1688.00			
COM72	-1462.50	1688.00				COM27	1406.50	-1688.00			
COM71	-1575.00	1688.00				COM26	1519.00	-1688.00			
COM70	-1687.50	1688.00				COM25	1631.50	-1688.00			
						COM24	1744.00	-1688.00			

Die size : 158.0 x 148.5 mil^2
Pad pitch : 4.43 mil
Note : 1 mil ~ 25.4μm

LCD Segment Driver
CMOS

MC141514



MC141514T1
MC141514T2
TAB

ORDERING INFORMATION

MC141514T1	TAB
MC141514T2	TAB

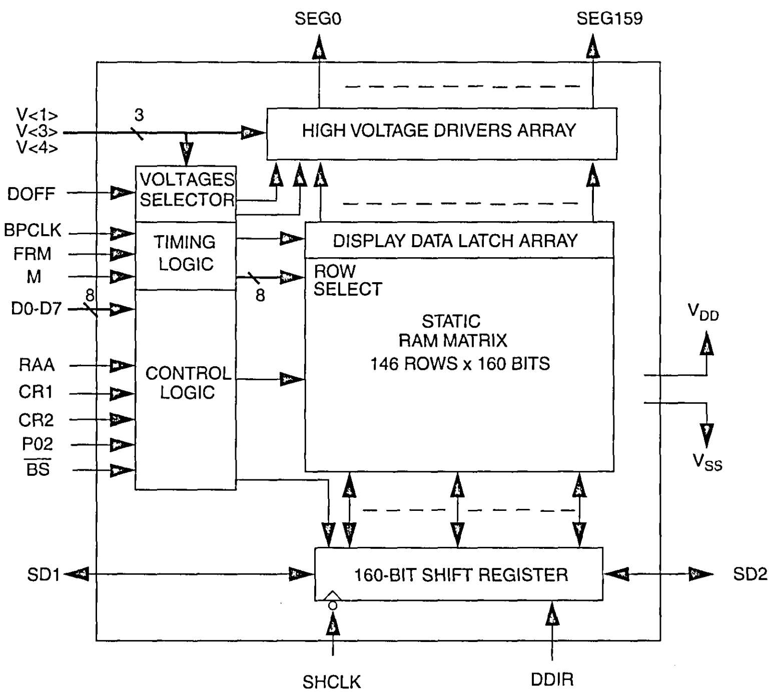
The MC141514 is an LCD segment driver chip which consists of 160x146 static RAM for display storage and provides 160 high voltage LCD driving signals.

It is a companion chip of MC141512 and MC141515 Backplane drivers for medium LCD panels. All these chips are controlled by the MC68HC05L11 microcomputer.

See Application Note AN-HK-15.

- Operating Supply Voltage Range-
  - Control Logic, RAM and Latch (V_{DD} Pin): 4.5V to 5.5V
  - Segment drivers (V_{LCD} Pin): 8.0 to 26V
- Operating Temperature Range: -25 to 70˚C
- Direct Serial Data Interface with the MC68HC05L11
- 160 x146 Static RAM (Display RAM)
- 160 LCD Segment Driving Signals
- Selectable 1:16 to 1:146 Multiplex Ratios
- 1:5 to 1:13 bias
- Expansion to higher driver count by cascade
- Available in TAB Form:
  - TAB (Tape Automated Bonding), 186 contacts

BLOCK DIAGRAM



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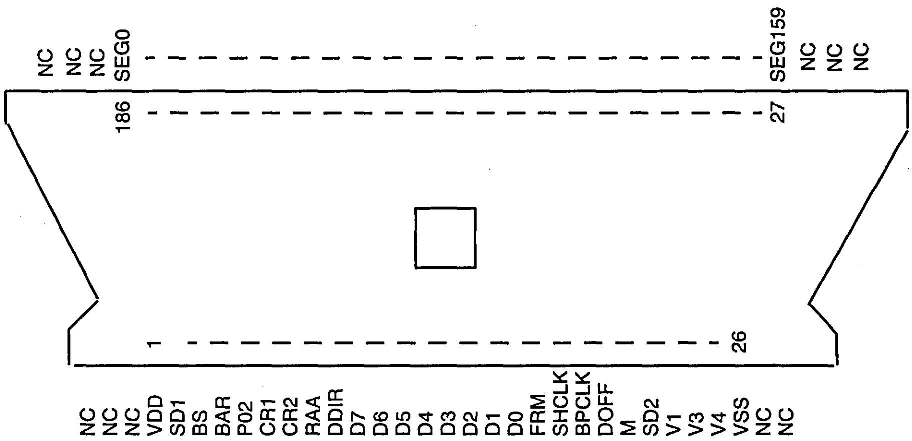


NC=NO CONNECTION

TAB Package Pin Assignment (Copper View)
MC141514T1
MC141514T2

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
$V_{<1>}$		-0.3 to +27.5	V
V_{in}	Input Voltage	-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-25 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

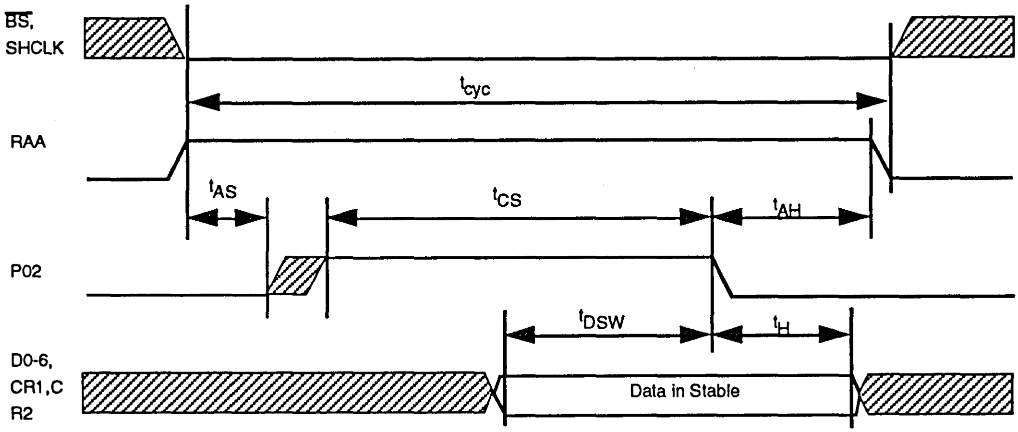
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD} = 5.0V, $V_{<1>}$ = 25V, T_A = 0 to 70°C)

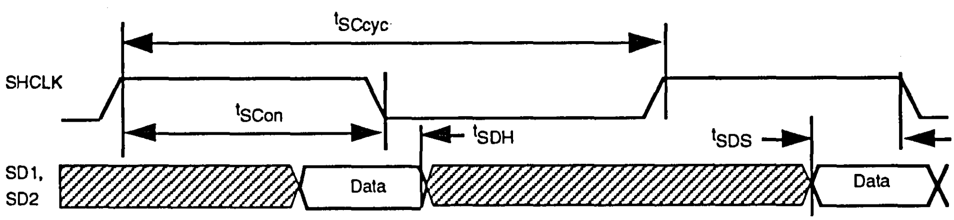
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD} $V_{<1>}$	Supply Voltage Range LCD Supply Voltage Range	(Absolute value reference to V_{SS})	4.5 +8.0	- -	5.5 +26.0	V V
I_{ACC}	Access Mode Supply Current (V_{DD} Pin)		-	100	200	
I_{DP}	Display Mode Supply Current (V_{DD} Pin)		-	50	100	uA
I_{SB}	Standby Mode Supply Current (V_{DD} Pin)	Using D_{ON} bit of the MCU	-	1	10	uA
I_{LDP}	Display Mode Supply Current ($V_{<1>}$ Pin)		-	10	20	uA
I_{LSB}	Standby Mode Supply Current ($V_{<1>}$ Pin)		-	1	10	uA
V_{OL} V_{OH}	Output Low Voltage Output High Voltage (SD1, SD2)	No Load	V_{SS} 0.8 x V_{DD}	- -	0.2 x V_{DD} V_{DD}	V V
V_{IH} V_{IL}	Input High Voltage Input Low Voltage (BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1, SD2, SHCLK, DOFF, M, DIRR)		0.7xV_{DD} V_{SS}	- -	V_{DD} 0.3xV_{DD}	V V
V_R	Data Retention		2.0	-	-	V
I_{in}	Input Current (BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1, SD2, SHCLK, DOFF, M, DIRR)		-	-	±1	uA
C_{in}	Input Capacitance (BPCLK, FRM, P02, RAA, CR1, CR2, $\overline{BS}$, D7-D0, SD1, SD2, SHCLK, DOFF, M, DIRR)		-	-	8	pF
R_{down}	Internal Pull Down Resistance (DOFF)		-	1	-	MΩ

AC ELECTRICAL CHARACTERISTICS(V_{DD}=5.0V, V_{SS}=0, T_A=25°C)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Access Cycle Time	235	-	ns
t_{AS}	Access Set up Time	100	-	ns
t_{AH}	RAA Hold Time	0	-	ns
t_{CS}	Chip Select Pulse Width	135	-	ns
t_{DSW}	Data SetUp Time	100	-	ns
t_H	Input Hold Time	10	-	ns
t_{SCcyc}	Shift Clock Cycle Time	200	-	ns
t_{SCon}	Shift Clock On Time	100	-	ns
t_{SDS}	Serial Data Setup Time	50	-	ns
t_{SDH}	Serial Data Hold Time	10	-	ns



Parallel Access Timing



Serial Access Timing (with $\overline{BS}$ = 0)

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>, V<3>, V<4>

These are the levels of voltage generated from an external voltages divider (Fig. 2). These voltage provide different voltage levels for shaping up the display output waveforms Seg0 - Seg159.

DOFF

This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD.If this pin is clear, the segment driver supplies LCD with driving signal. If this pin is set, the segment driver outputs is high-impedanced and LCD display is disabled.

FRM

A periodic active high input to the segment driver for frame timing synchronization. This pin is connected to the signal FRM of MC68HC05L11. The frequency depends on the MUX ratio and BPCLK signal.

BPCLK

A periodic clock output from MC68HC05L11 to the segment driver for timing synchronization. The signal controls the refresh timing of LCD display.

M

A periodic output from backplane driver. This pin is used for synchronization among display drivers.

D0 - D7

An eight-bit input-only data bus which is connected to the D0 - D7 of MC68HC05L11. These pins are used for address input and data input. Refer to Fig.1 for definition.

P02

A bus clock input that is used for data bus timing synchronization. This pin is connected to P02 of MC68HC05L11.

$\overline{BS}$

This is an active low input for chip select.

RAA

It is a strobe signal from MC68HC05L11 indicating that a valid segment control data is on D0 - D7 for a period of P02.

CR1, CR2

These two control signals from MC68HC05L11 to Segment driver describing the nature of the content in D0 - D7. The effect of CRs are shown on Fig 1.

SD1, SD2

These two pins are two bi-directional data lines connecting to the UD2 or LD2 and UD1 or LD1 respectively. These allow the display data from MC68HC05L11 entering the segment driver in both directions.

SHCLK

This is the shift clock from MC68HC05L11 to segment driver for clocking the serial data on SD1 and SD2. See Timing Diagram (above) for illustration.

DDIR

It is an input pin carrying the signal from MC68HC05L11 to segment driver to control the direction of the serial data. If DDIR is set, the serial data enter the segment driver through SD1 and leave the segment driver through SD2. If DDIR is clear, SD1 and SD2 are redefined as an output and input respectively. See Figure 1A.

SEG0 - SEG159

These 160 output lines provide the segment driving signal to the LCD panel. They are all in high-impedance state while the display is turned off (i.e. DOFF is set).

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

INTRODUCTION

The LCD segment driver can support multiplex ratio of a LCD system up to 256(146 at the present version) and cascading of more than one driver for expansion is possible. It can be set from 1:5 bias (for 16 mux) to 1:13 bias (for 146 mux), by the voltage divider ratio of Fig.2. The ratio of bias or the contrast ratio (a) is defined as

$$1:\frac{4xR1+R2}{R1}=1:a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a=\sqrt{mux}\ +1$$

To set up a multiplex ratio, please refer to MC68HC05L11D/H Technical Data Section 10.

CONTROL LOGIC produces the control signals necessary for display RAM read / write and serial data latching. This Control Logic is directly supervised by the MCU through the Data Bus, i.e. D0 - D7, CR1 and CR2. MCU writing a byte of instruction to the Segment Control Register will cause Segment Driver(s) to fetch this instruction from the Data Bus and the command executed at the next P02 cycle. Fig.1 shows the functions of which the Control Logic will carry out in respond to MCU access through the Segment Control Register.

ROW ADDRESS(WRITE IN) instruction causes Segment driver(s) to load the content of the SHIFT REGISTER into a row of RAM which address is specified by D7 to D0.

ROW ADDRESS(READ FROM) instruction causes Segment driver(s) to copy a row of RAM which address is specified by D7 to D0 into the 160 BIT SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes Segment driver(s) to do a vertical scroll up or down.

The content of D7 to D0 only represents the vertical offset of the new screen to the current screen. This vertical offset presenting in the Data Bus then is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER to generate a new offset. This new offset will then be stored in the VERTICAL SCROLL VECTOR REGISTER. Periodically the content of this register will be fetched and loaded into a presettable counter in the TIMING LOGIC to generate the row addresses for screen refreshing.

RESET	BIT0	Writing an "1" to this bit will set the VERTICAL SCROLL VECTOR REGISTER to zero.
UL	BIT1	If this bit is set, the segment driver serves the upper panel in case of splitted panel. This will cause a swap in signals flow between SD1 and SD2.
CLRSH	BIT2	Writing an "1" to this bit will clear the content of the 160-BIT SHIFT REGISTER.

TIMING LOGIC, according to M, BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix's content periodically starting from the row address specified by the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from the external voltage divider. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 160x146 bits of SRAM cell. The content of these RAM cells can be altered by read/write from/to the shift register with the Segment Control Interface (refer to MC68HC05L11 specification Section 6.2.4).

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Seg(x) in Fig 3.

SHIFT REGISTER is a 160-bit bi-directional register which acts as an input either from SD1 or SD2. The direction of data flow depends on the content of DDIR. And, it can be swapped by setting the UL bit to high. Data enter this shift register in serial. Shift register latches data at the falling edge of the signal SHCLK. See Timing Diagram on Page 4 for illustration.

CR2	CR1	D7	D6	D5	D4	D3	D2	D1	D0
0	0	ROWADDRESS (WRITE IN)							
0	1	ROWADDRESS (READ FROM)							
1	0	SCROLL UP ADVANCE							
1	1	RESER-VED	X	X	X	X	CLR SH	UL	RESET

FIGURE 1 - A Summary of the Control Functions of Segment Driver

DDIR	UL	SD1	SD2
1	0	input	output
0	0	output	input
1	1	output	input
0	1	input	output

FIGURE 1A - Relationship between DDIR, UL, SD1 and SD2

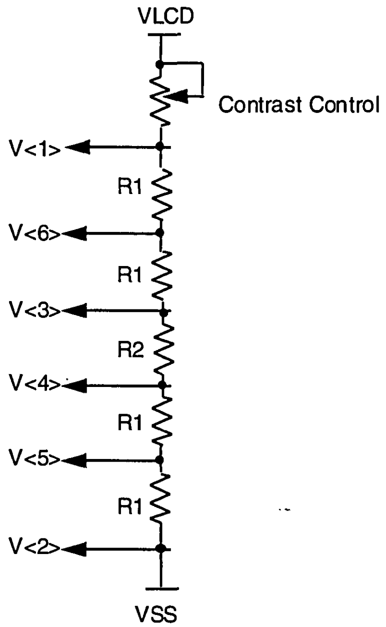


FIGURE 2 - External Voltage Divider

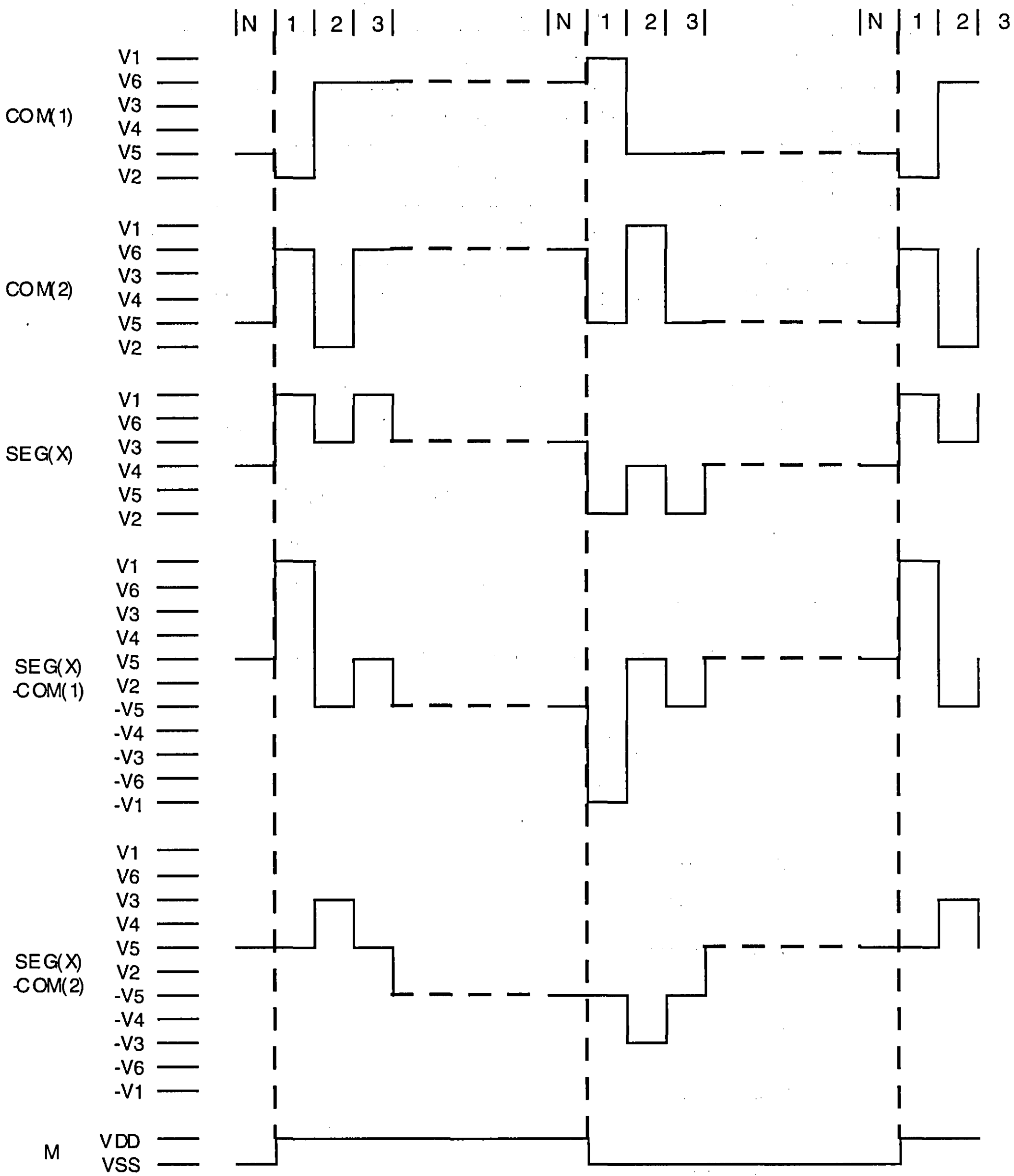
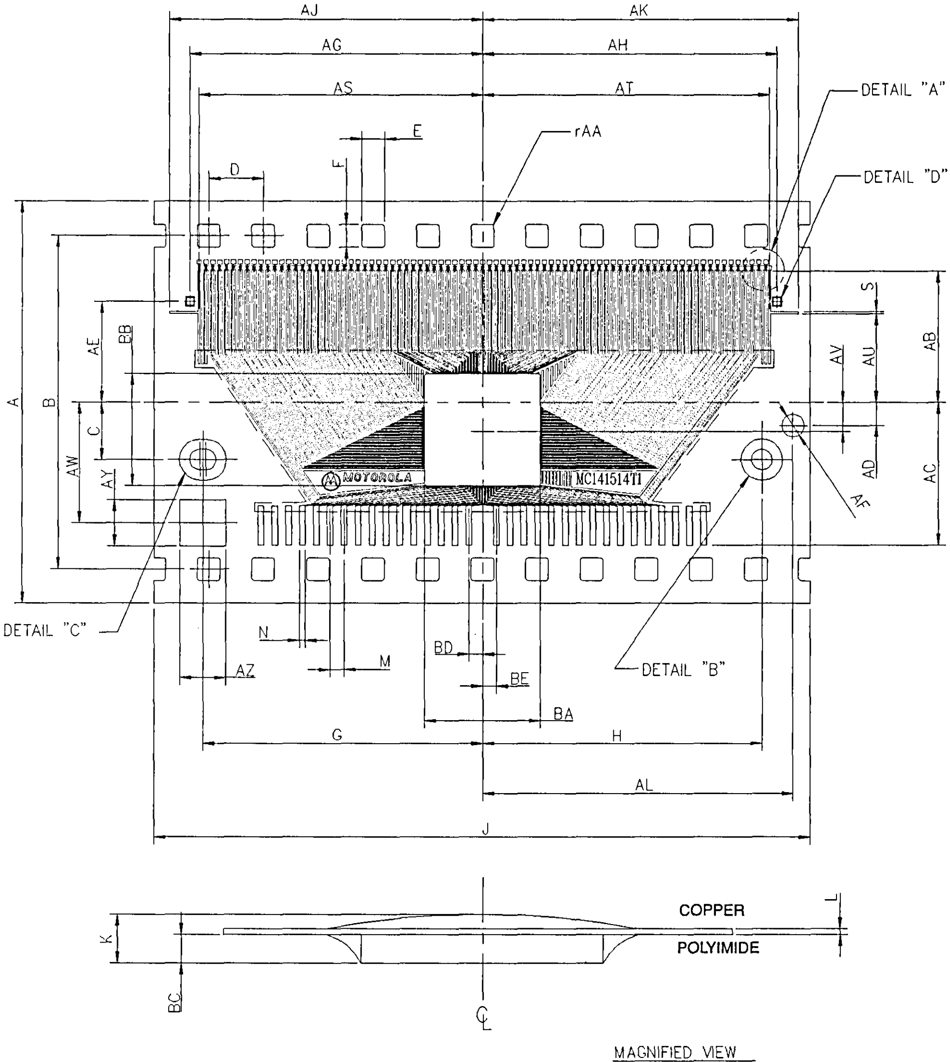


FIGURE 3 - Driving Waveforms of 1:N multiplex

(M is used for timing synchronization)

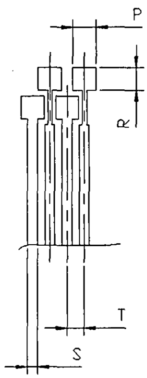
PACKAGE DIMENSIONS

MC141514T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



Reference: 98ASL00052A	Issue "C" released on 11/01/93

MC141514T1
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



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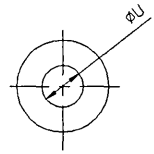
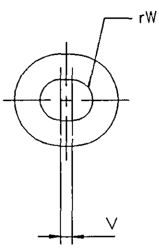
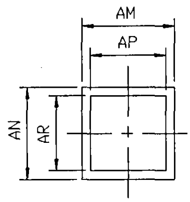


DETAIL "B"



DETAIL "C"



DETAIL "D"

Reference: 98ASL00052A	Issue "C" released on 11/01/93

MC141514T1 TAB PACKAGE DIMENSION

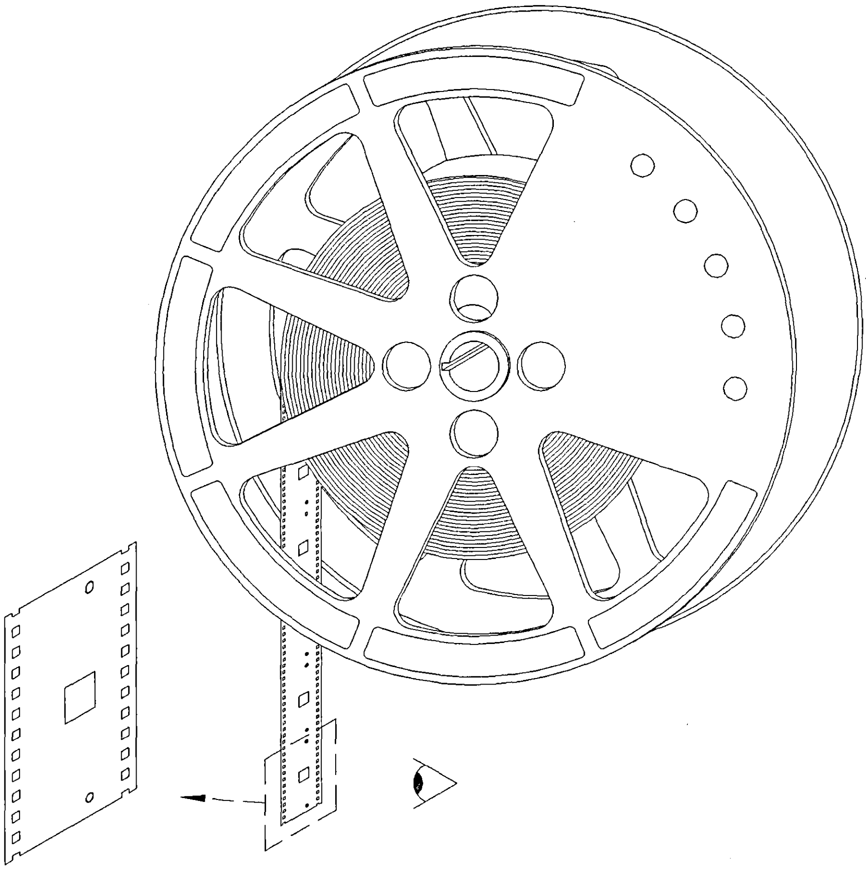
	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	34.775	35.175	1.3691	1.3848	AE	8.690	8.790	0.3421	0.3461
B	28.927	29.027	1.1389	1.1428	AF	1.950	2.050	0.0768	0.0807
C	4.950	5.050	0.1949	0.1988	AG	25.350	25.450	0.9980	1.0020
D	4.720	4.780	0.1858	0.1882	AH	25.510	25.610	1.0043	1.0083
E	1.951	2.011	0.0768	0.0792	AJ	27.130	27.230	1.0681	1.0720
F	1.951	2.011	0.0768	0.0792	AK	27.430	27.530	1.0799	1.0839
G	24.200	24.300	0.9528	0.9567	AL	26.500	27.500	1.0433	1.0827
H	24.200	24.300	0.9528	0.9567	AM	0.750	0.850	0.0295	0.0335
J	56.500	57.500	2.2244	2.2638	AN	0.750	0.850	0.0295	0.0335
K	0.686	0.838	0.0270	0.0330	AP	0.600	0.700	0.0236	0.0276
L	0.0675	0.0825	0.0027	0.0032	AR	0.600	0.700	0.0236	0.0276
M	1.190	1.210	0.0469	0.0476	AS	24.551	24.649	0.9666	0.9704
N	0.480	0.520	0.0189	0.0205	AT	24.850	24.950	0.9784	0.9823
P	0.350	0.450	0.0138	0.0177	AU	7.670	7.770	0.3020	0.3059
R	0.350	0.450	0.0138	0.0177	AV	2.450	2.550	0.0965	0.1004
S	0.150	0.190	0.0059	0.0075	AW	10.000	11.000	0.3937	0.4331
T	0.290	0.310	0.0114	0.0122	AY	3.500	4.500	0.1378	0.1772
U	1.750	1.850	0.0689	0.0728	AZ	3.500	4.500	0.1378	0.1772
V	0.450	0.550	0.0177	0.0217	BA	-	10.062	-	0.3961
W	0.850	0.950	0.0335	0.0374	BB	-	9.747	-	0.3837
AA	-	0.200	-	0.0079	BC	0.5794	0.6294	0.0228	0.0248
AB	10.900	11.900	0.4291	0.4685	BD	1.150	1.250	0.0453	0.0492
AC	11.900	12.900	0.4685	0.5079	BE	1.150	1.250	0.0453	0.0492
AD	1.500	2.500	0.0591	0.0984					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1 oz.
4. Tin plating thickness: 0.4μm.
5. Recommended excise area J x (AB + AC).

Reference: 98ASL00052A	Issue "C" released on 11/01/93

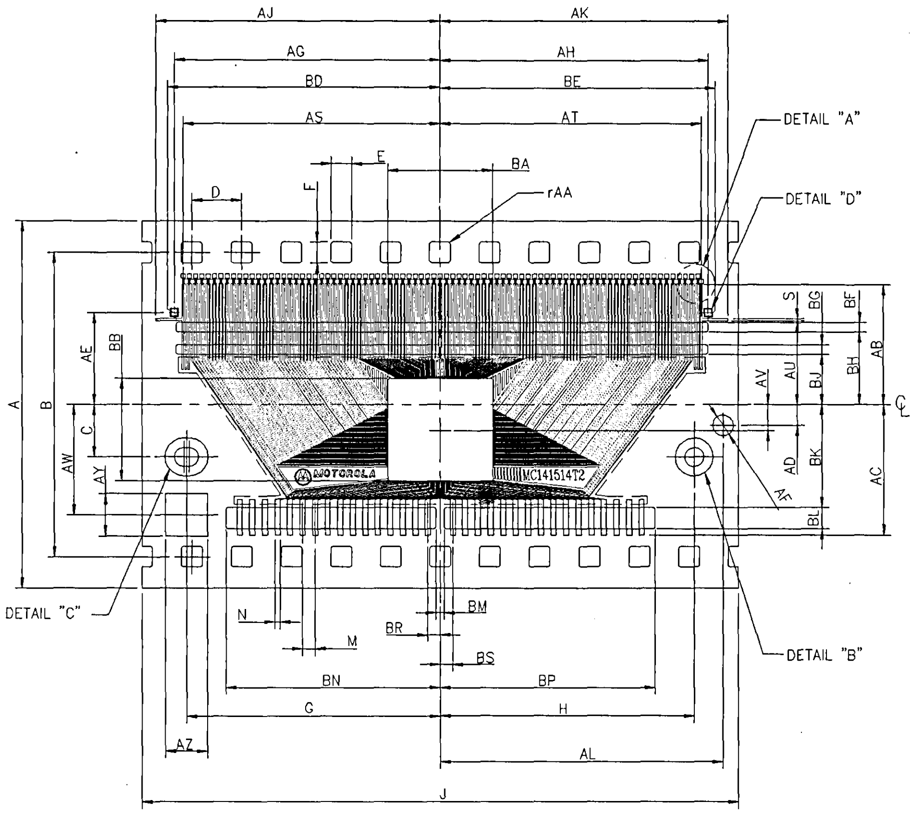
MC141514T1

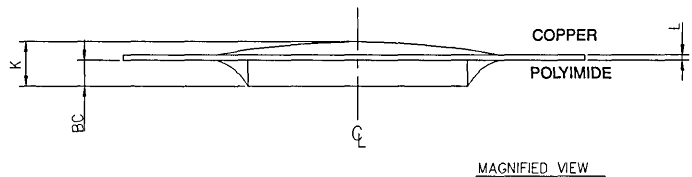
TAB TAPE REEL ORIENTATION



Reference: 98ASL00052A	Issue "C" released on 11/01/93

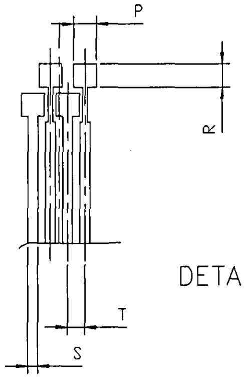
MC141514T2
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)





Reference: 98ASL00100A	Issue “B” released on 09/19/95

MC141514T2
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



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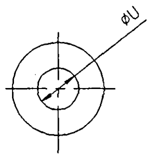

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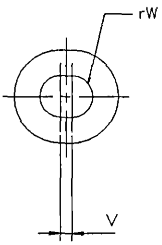

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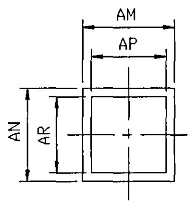


DETAIL "D"

Reference: 98ASL00100A	Issue "B" released on 09/19/95

MC141514T2 TAB PACKAGE DIMENSION

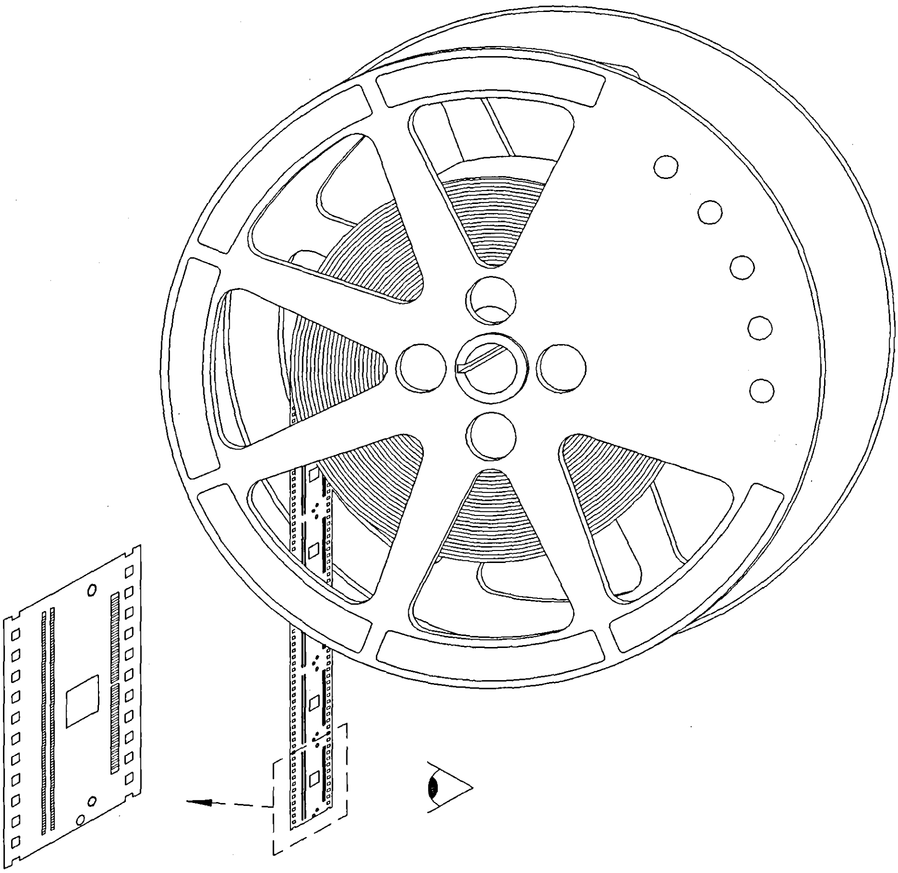
	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	34.775	35.175	1.3691	1.3848	AJ	27.130	27.230	1.0681	1.0720
B	28.927	29.027	1.1389	1.1428	AK	27.430	27.530	1.0799	1.0839
C	4.950	5.050	0.1949	0.1988	AL	26.500	27.500	1.0433	1.0827
D	4.720	4.780	0.1858	0.1882	AM	0.750	0.850	0.0295	0.0335
E	1.951	2.011	0.0768	0.0792	AN	0.750	0.850	0.0295	0.0335
F	1.951	2.011	0.0768	0.0792	AP	0.600	0.700	0.0236	0.0276
G	24.200	24.300	0.9528	0.9567	AR	0.600	0.700	0.0236	0.0276
H	24.200	24.300	0.9528	0.9567	AS	24.551	24.649	0.9666	0.9704
J	56.500	57.500	2.2244	2.2638	AT	24.850	24.950	0.9784	0.9823
K	0.686	0.838	0.0270	0.0330	AU	7.937	8.037	0.3125	0.3164
L	0.0675	0.0825	0.0027	0.0032	AV	2.450	2.550	0.0965	0.1004
M	1.190	1.210	0.0469	0.0476	AW	10.000	11.000	0.3937	0.4331
N	0.480	0.520	0.0189	0.0205	AY	3.500	4.500	0.1378	0.1772
P	0.350	0.450	0.0138	0.0177	AZ	3.500	4.500	0.1378	0.1772
R	0.350	0.450	0.0138	0.0177	BA	-	10.062	-	0.3961
S	0.150	0.190	0.0059	0.0075	BB	-	9.747	-	0.3837
T	0.290	0.310	0.0114	0.0122	BC	0.5794	0.6294	0.0228	0.0248
U	1.750	1.850	0.0689	0.0728	BD	25.200	25.300	0.9921	0.9961
V	0.450	0.550	0.0177	0.0217	BE	25.500	25.600	1.0039	1.0079
W	0.850	0.950	0.0335	0.0374	BF	0.850	0.950	0.0335	0.0374
Y	0.032	0.038	0.0013	0.0015	BG	0.850	0.950	0.0335	0.0374
Z	0.032	0.038	0.0013	0.0015	BH	6.850	6.950	0.2697	0.2736
AA	-	0.200	-	0.0079	BJ	4.750	4.850	0.1870	0.1909
AB	10.900	11.900	0.4291	0.4685	BK	9.750	9.850	0.3839	0.3878
AC	11.900	12.900	0.4685	0.5079	BL	1.950	2.050	0.0768	0.0807
AD	1.500	2.500	0.0591	0.0984	BM	0.750	0.850	0.0295	0.0335
AE	8.690	8.790	0.3421	0.3461	BN	20.450	20.550	0.8051	0.8091
AF	1.950	2.050	0.0768	0.0807	BP	20.450	20.550	0.8051	0.8091
AG	25.350	25.450	0.9980	1.0020	BR	1.150	1.250	0.0453	0.0492
AH	25.510	25.610	1.0043	1.0083	BS	1.150	1.250	0.0453	0.0492

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1 oz (35 micrometer)
4. 12 sprocket hole device

Reference: 98ASL00100A	Issue "B" released on 09/19/95

MC141514T2

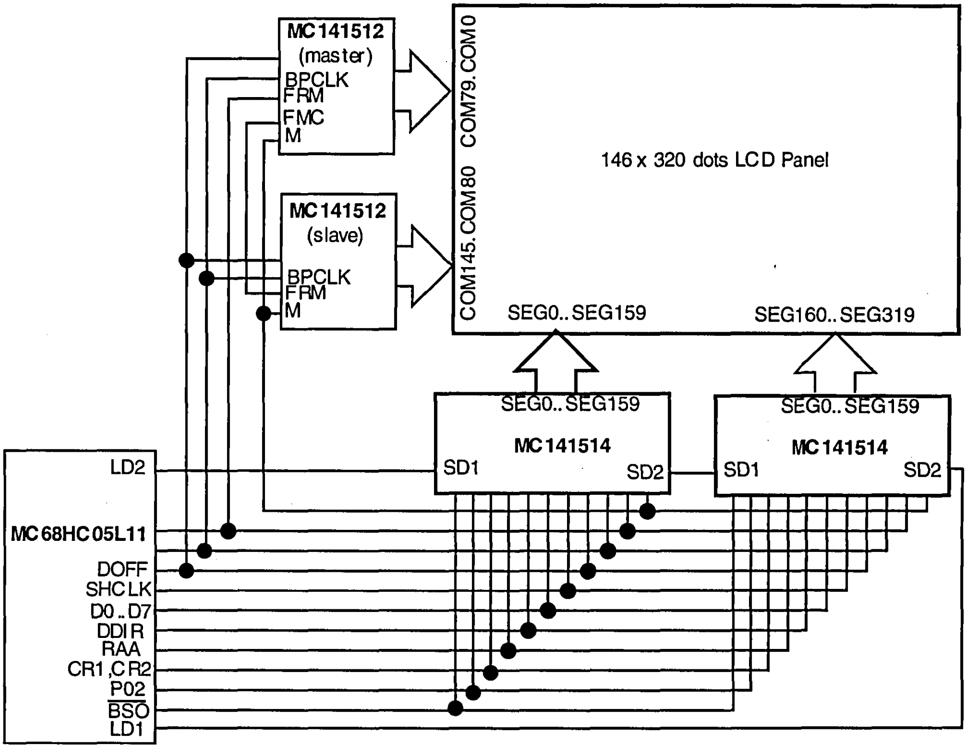
TAB TAPE REEL ORIENTATION



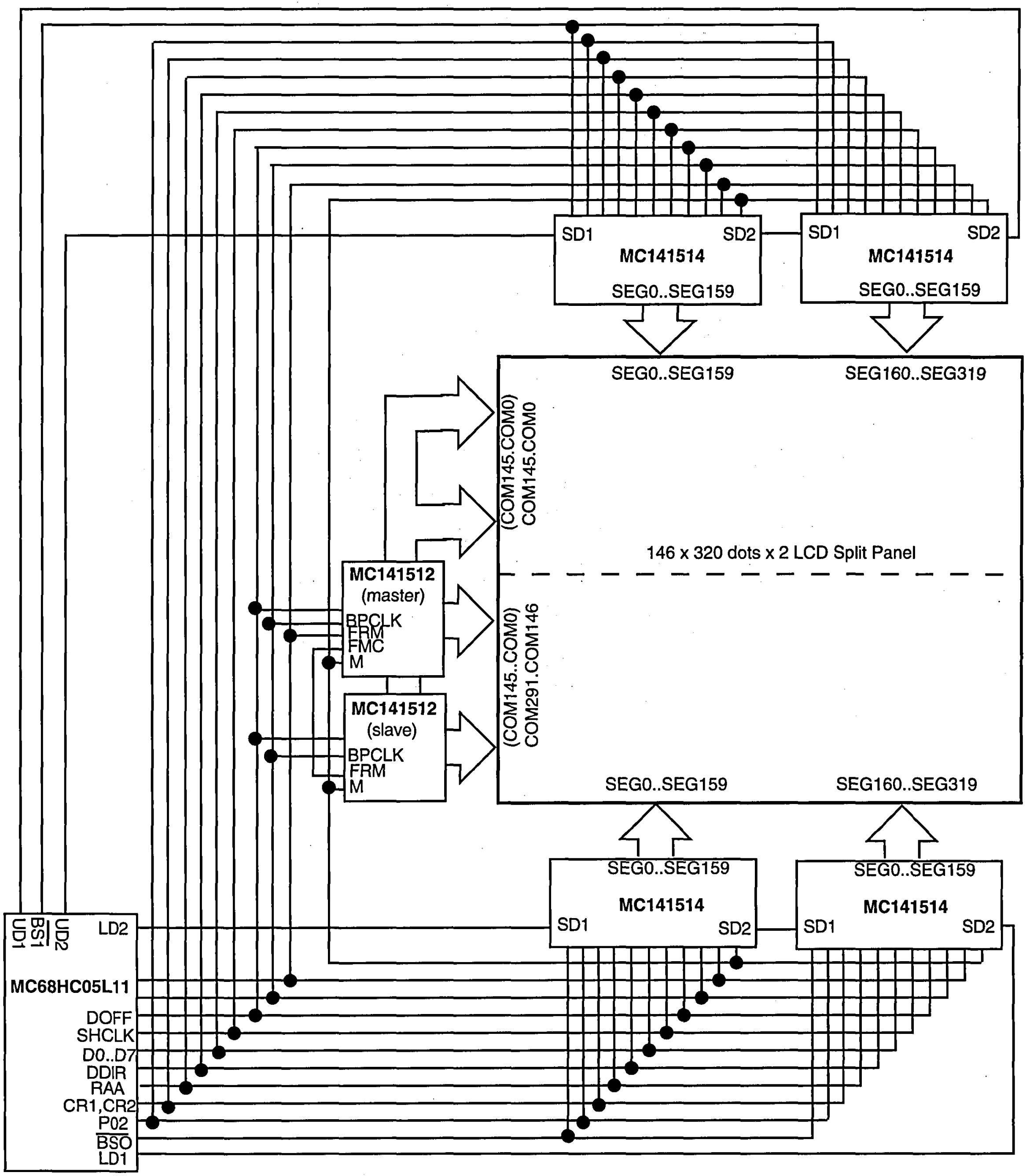
Reference: 98ASL00100A	Issue "B" released on 09/19/95

TYPICAL APPLICATIONS

146 x 320 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11



146 x 320 x 2 SPLIT PANEL LCD SYSTEM WITH MC68HC05L11



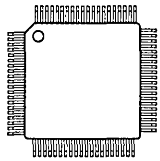
MC141516

LCD Backplane Driver
CMOS

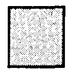
The MC141516 is a high voltage passive LCD Backplane driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 64 backplane driving outputs for 64 MUX or lower LCD panel. The MC141516 is a companion chip of MC141518 (Segment driver).

It has an LCD timing generator which serves the same purpose as the LCD timing generator in a Motorola microcomputer MC68HC05L11. If these drivers are used with MC68HC05L11, its internal LCD timing generator can be disabled. Necessary timing signals are input from MC68HC05L11. Otherwise, the driver's internal LCD timing generator can be activated to provide timing signals for system synchronization.

- Operation Supply Voltage Range-
  - Logic (V_{DD}): 2.7V to 5.5V
  - Backplane drivers (V_{LCD}):6.0V to 13V
- Operation Temperature Range: -20 to 70˚C
- 64 LCD blackplane driving signals
- Driving Duty Cycle (MUX): 1/32 to 1/64
- Optional 32,48 or 64 multiplex ratio if the on-chip RC oscillator is used
- Optional multiplex ratio from 32 to 64 with MC68HC05L11
- 80-pin TQFP (Thin Quad Flat Package)



MC141516FJ
TQFP

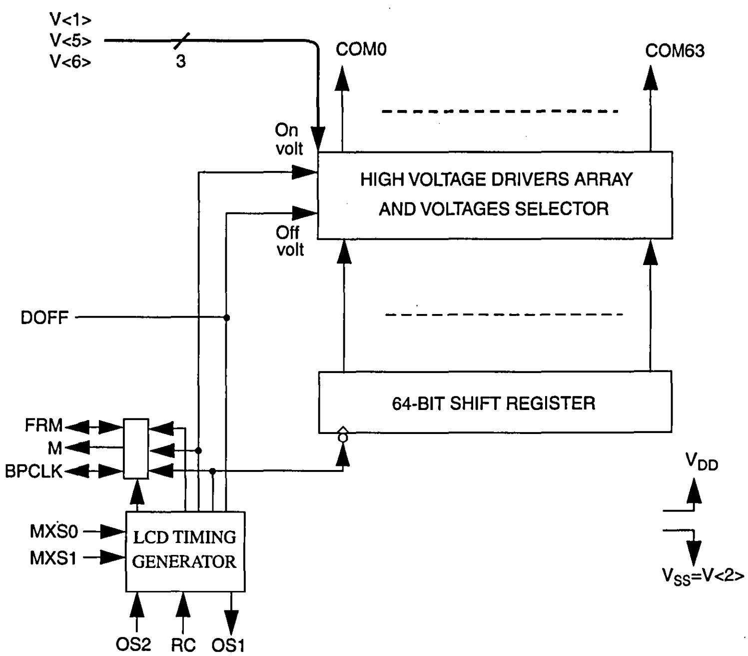


MCC141516
DIE

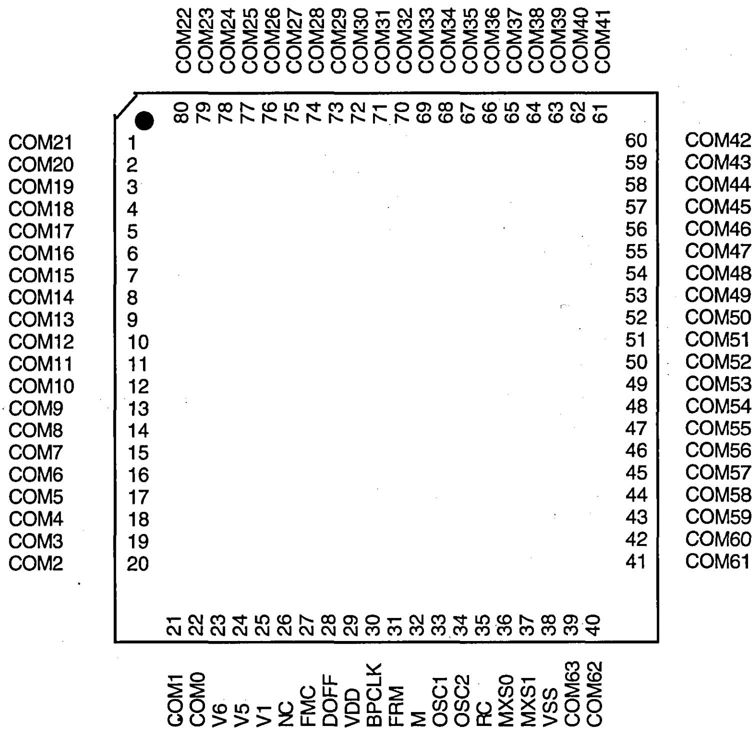
ORDERING INFORMATION

MC141516FJ	TQFP
MCC141516	DIE

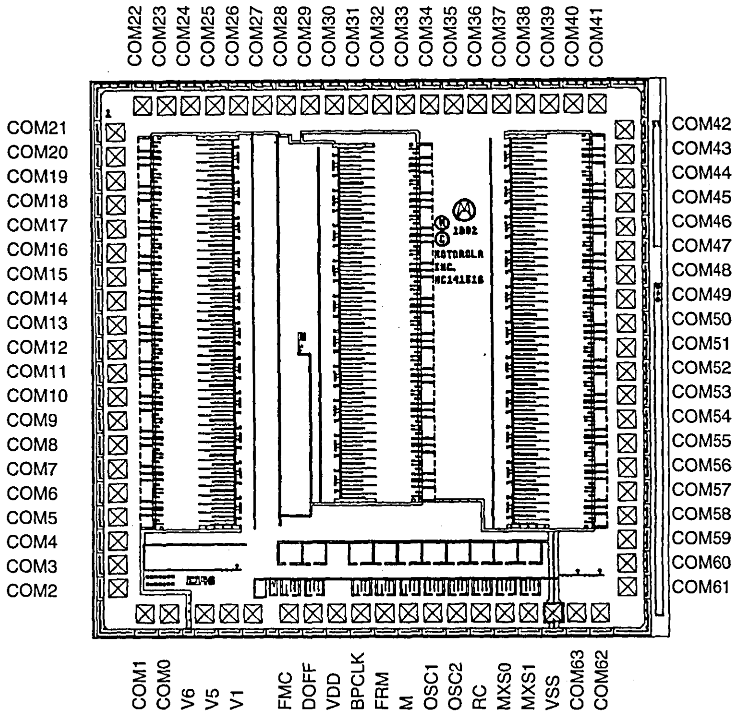
Block Diagram



REV 4
10/96



MC141516FJ Pin Assignment



MCC141516 Pad Assignment

MAXIMUM RATINGS* (Voltages Reference to V_{SS}, T_A=25°C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to + 7.0	V
V<1>		V_{SS} -0.3 to V_{SS} +15	V
V_{in}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
I	Current Drain Per Pin Excluding VDD and Vss	25	mA
T_A	Operating Temperature Range	-20 to +70	°C
T_{stg}	Storage Temperature Range	-65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description Section.

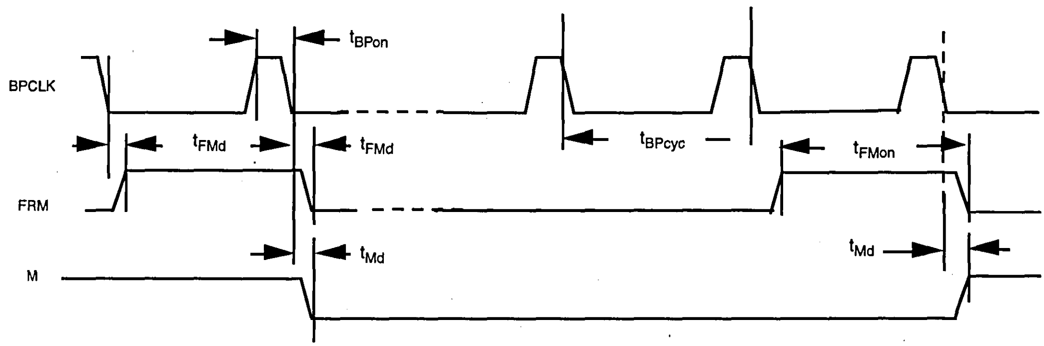
The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range V_{SS} < or = (Vin or Vout) < or = V_{DD}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C, V_{DD}=5.0V, V<1>=13V)

Symbol	Parameter		Min	Max	Unit
V_{IH}	Input High Voltage	BPCLK, FRM, M, DOFF	0.7xV_{DD}	V_{DD}	V
V_{IL}	Input Low Voltage	BPCLK, FRM, M, DOFF	V_{SS}	0.3xV_{DD}	V
C_{in}	Capacitance	BPCLK, FRM, M, DOFF	-	8	pF
	Operating Voltages				
V_{DD}	Supply Voltage (referenced to VSS)		2.7	5.5	V
V<1>	LCD Voltage (referenced to VSS)		6.0	13	V
I_{in}	Input Current (Oscillator OFF)	BPCLK, FRM, M, DOFF, MXS0, MXS1	-	±1	uA
V_{OL}	Output Low Voltage (Oscillator ON)	M, FRM, BPCLK	-	0.2xV_{DD}	V
V_{OH}	Output High Voltage (Oscillator ON)	M, FRM, BCLK	0.8xV_{DD}	-	V
I_{OL}	Output Low Current (Oscillator ON)	M, FRM, BCLK (V_{OL}=0.5V)	-	-100	uA
I_{OH}	Output High Current (Oscillator ON)	M, FRM, BCLK (V_{OH}=4.5V)	100	-	uA
	Operating supply current VDD (VDD=5V, V<1>=13V)				
I_{DP1}	Dynamic Mode (Oscillator ON, BPCLK=4KHz)		-	32	uA
I_{DP2}	(Oscillator OFF, BPCLK=4KHz)		-	5	uA
I_{SB}	Standby Mode		-	2	uA
	Operating supply current V<1> (V<1>=13V)				
I_{LDP}	Display Mode		-	8	uA
I_{LSB}	Standby Mode		-	4.0	uA

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V +/-5%, V_{SS}=0, V<1>=13V, T_A=25°C)

Symbol	Parameter	Min	Max	Unit
t_{BPon}	BPCLK Pulse On Time	61	-	us
t_{BPcyc}	BPCLK Cycle Period	122	-	us
t_{FMd}	Frame Delay Time	5	30	us
t_{FMon}	Frame Pulse On Time	122	-	us
t_{Md}	M Pulse Delay Time	0	30	us



MC141516 Timing Diagram

V_{DD} AND V_{SS}

Power is supplied to the driver using these two pins. VDD is power and VSS is ground.

V<1>, V<5>, V<6>

These input pins provide the voltage levels for the backplane driver and are connected to the V<1>, V<5>, V<6> of the voltages generator as in Figure 2 of the MC141518 Segment driver Product Specification.

DOFF

It is an active-high input for turning off the LCD. If DOFF is set, all high voltage outputs will be turned to high impedance. DOFF will also suppress the on-chip RC oscillator from oscillation when the LCD timing generator is enabled.

OSC1, OSC2, RC

These pins provide connections for external circuitry to the on-chip RC oscillator for frequency selection. The on-chip RC oscillator is part of the internal LCD timing generator. Output of this oscillator will be fed out as BPCLK and further divided down internally to produce signals FRM and M if the LCD timing generator is enabled.

MXS1, MXS0

These pins can be hardwired to select different mux ratios. Table 1 shows the combinations of these signals and their corresponding mux ratios. These four combinations provide selections for 32,48 and 64 mux ratio and a disable state. Except for the disabled state, all other selections will enable the LCD timing generator. With DOFF clear, the periodic signal from the on-chip RC oscillator is fed to the whole LCD system as the BPCLK. BPCLK will then be further divided down through the LCD timing generator to produce signals FRM and M for the whole LCD system.

MXS1, MXS0	MUX RATIO
0,0	DISABLE
0,1	32
1,0	48
1,1	64

Table 1: The Selections of MUX Ratio using MXS1 and MXS0

BPCLK

It is either an input pin connecting to signal BPCLK of the microcomputer MC68HC05L11 or an output pin supplying the synchronization pulse BPCLK to segment drivers. If the LCD timer generator is disabled, this pin is assumed to be input.

FRM

It is either an input pin connecting to signal FRM of the microcomputer MC68HC05L11 or an output pin supplying the synchronization pulse FRM to segment drivers. If the LCD timer generator is disabled, the status of this pin is input.

M

This is an output pin providing the necessary modulation signal to shape up the class B LCD waveform (see Fig.3, Product Specification of MC141518). It is a signal with 50% duty cycle and its frequency is half of FRM.

COM0-COM63

These are the high voltage outputs of the backplane driver which are connected to the common lines of the LCD panel. These high voltage drivers are high impedance if DOFF is set. See Fig.3 "Product Specification of MC141518" for these high voltage outputs waveform.

FMC

This is a test pin. This pin should be left open in application.

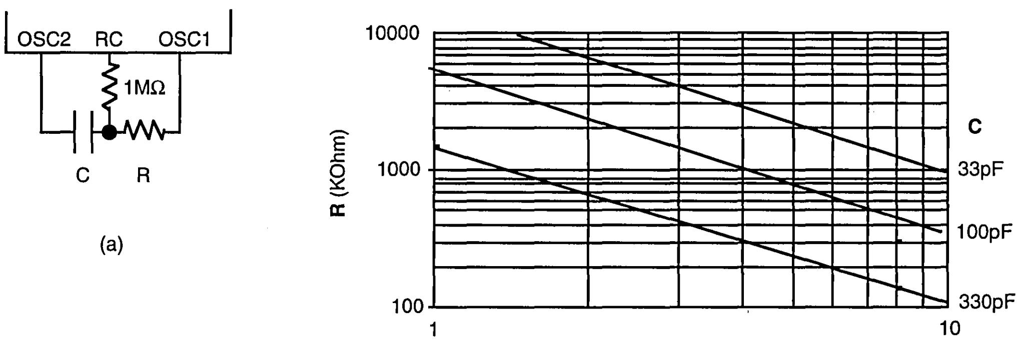
INTRODUCTION

The backplane driver can support multiplex ratio of a LCD system from 32 to 64. Three signals that need to be varied as a result of different mux ratio are BPCLK, FRM and M. The first two can be imported externally (if the microprocessor MC68HC05L11 is used) or the backplane driver generates them internally. In case of internal generation, user has to design the on-chip RC oscillator circuit producing a frequency with respect to desirable mux ratio.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from external voltage divider. See Fig.2, Product Specification of the segment driver MC141518.

64 BIT SHIFT REGISTER samples FRM and shift at the falling edge of BPCLK.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers which outputs are connecting to the backplane (or common) lines of the LCD panel. The waveform of these drivers are shown as Com(1) or Com(2) in Fig. 3, the Product Specification of the segment driver MC141518.



(a)

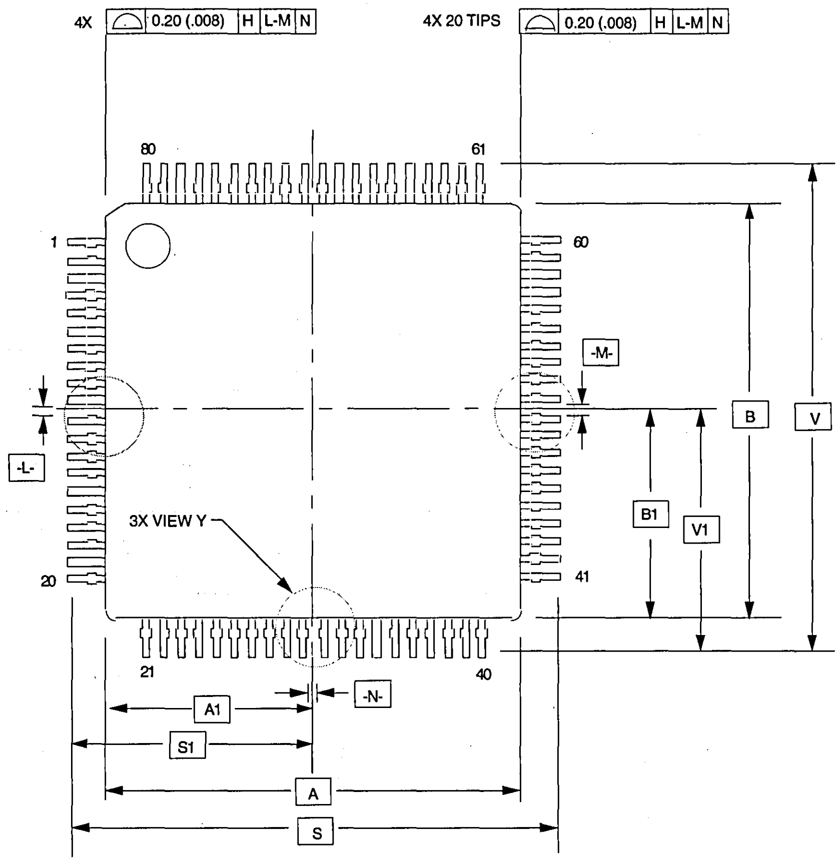
BPCLK Frequency (Khz)
(For reference only)

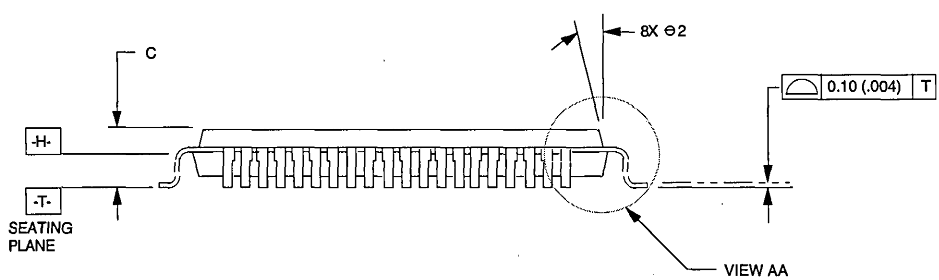
(b)

Figure 1. (a) the external circuit to the on-chip RC oscillator and its (b) frequency relationship with the external resistor and capacitor.

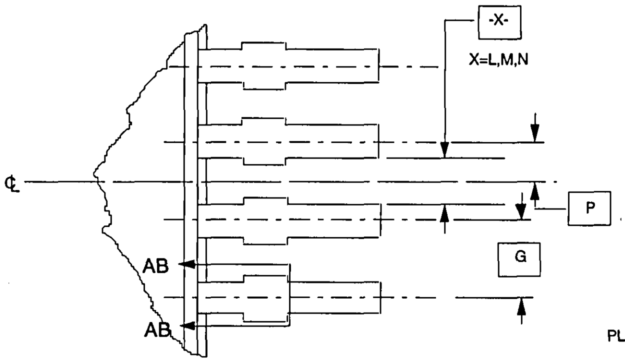
PACKAGE DIMENSIONS

MC141516FJ
TQFP PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)

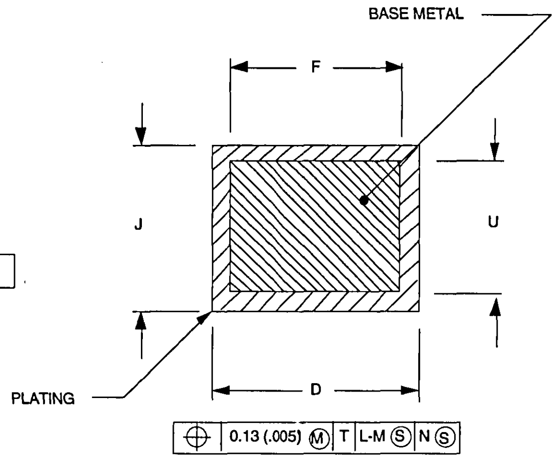




MC141516FJ
TQFP PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)

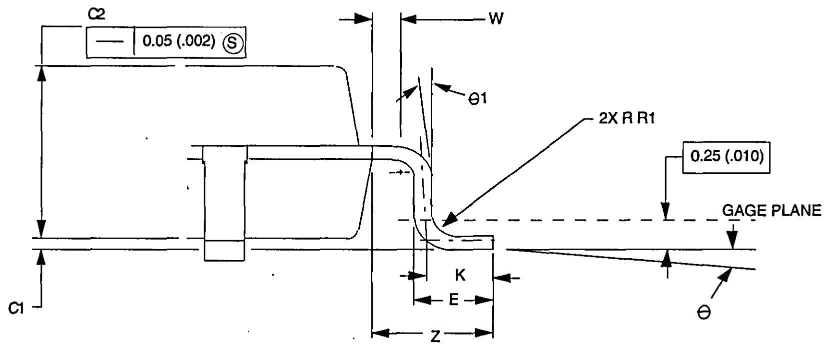


VIEW Y



SECTION AB - AB

ROTATED 90° CLOCKWISE



VIEW AA

MC141516FJ TQFP PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	14.00	BSC	.551	BSC	K	0.50	REF	.020	REF
A1	7.00	BSC	.276	BSC	P	0.325	BSC	.013	REF
B	14.00	BSC	.551	BSC	R1	0.09	0.20	.004	.008
B1	7.00	BSC	.276	BSC	S	16.00	BSC	.630	BSC
C	---	1.74	---	.069	S1	8.00	BSC	.013	BSC
C1	0.04	0.24	.002	.009	U	0.09	0.16	.004	.006
C2	1.30	1.50	.051	.059	V	16.00	BSC	.630	BSC
D	0.22	0.38	.009	.015	V1	8.00	BSC	.315	BSC
E	0.40	0.75	.016	.030	W	0.20	REF	.008	REF
F	0.17	0.33	.007	.013	Z	1.00	REF	.039	REF
G	0.65	BSC	.026	BSC	θ	0°	10°	0°	10°
J	0.09	0.27	.004	.011	θ1	0°	---	0°	---
					θ2	9°	14°	9°	14°

NOTES:

1. Dimensions and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane -H- is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -L- , -M- and -N- to be determined at datum plane -H- .
5. Dimensions S and V to be determined at seating plane -T- .
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.25(.010) per side. Dimensions A and B do include mold mismatch and are determined at datum plane -H- .
7. Dimension D does not include dambar protrusion. dambar protrusion shall not cause the lead width to exceed 0.46 (.018). Minimum space between protrusion and adjacent lead or protrusion 0.07 (.003).

MCC141516 PAD COORDINATES: (UNIT: UM)

PIN NAME	X	Y	PIN NAME	X	Y
COM1	-1330.0	-1481.5	COM61	1489.5	-1331.5
COM0	-1190.0	-1481.5	COM60	1489.5	-1191.5
V6	-982.0	-1481.5	COM59	1489.5	-1051.5
V5	-842.0	-1481.5	COM58	1489.5	-911.5
V1	-702.0	-1481.5	COM57	1489.5	-771.5
FMC	-490.0	-1481.5	COM56	1489.5	-631.5
DOFF	-350.0	-1481.5	COM55	1489.5	-491.5
V_{DD}	-210.0	-1481.5	COM54	1489.5	-351.5
BPCLK	-70.0	-1481.5	COM53	1489.5	-211.5
FRM	70.0	-1481.5	COM52	1489.5	-71.5
M	210.0	-1481.5	COM51	1489.5	68.5
OSC1	350.0	-1481.5	COM50	1489.5	208.5
OSC2	490.0	-1481.5	COM49	1489.5	348.5
RC	630.0	-1481.5	COM48	1489.5	488.5
MXS0	770.0	-1481.5	COM47	1489.5	628.5
MXS1	910.0	-1481.5	COM46	1489.5	768.5
V_{SS}	1050.0	-1481.5	COM45	1489.5	908.5
COM63	1190.0	-1481.5	COM44	1489.5	1048.5
COM62	1330.0	-1481.5	COM43	1489.5	1188.5
			COM42	1489.5	1328.5

PIN NAME	X	Y	PIN NAME	X	Y
COM2	-1489.5	-1331.5	COM22	-1330.0	1481.0
COM3	-1489.5	-1191.5	COM23	-1190.0	1481.0
COM4	-1489.5	-1051.5	COM24	-1050.0	1481.0
COM5	-1489.5	-911.5	COM25	-910.0	1481.0
COM6	-1489.5	-771.5	COM26	-770.0	1481.0
COM7	-1489.5	-631.5	COM27	-630.0	1481.0
COM8	-1489.5	-491.5	COM28	-490.0	1481.0
COM9	-1489.5	-351.5	COM29	-350.0	1481.0
COM10	-1489.5	-211.5	COM30	-210.0	1481.0
COM11	-1489.5	-71.5	COM31	-70.0	1481.0
COM12	-1489.5	68.5	COM32	70.0	1481.0
COM13	-1489.5	208.5	COM33	210.0	1481.0
COM14	-1489.5	348.5	COM34	350.0	1481.0
COM15	-1489.5	488.5	COM35	490.0	1481.0
COM16	-1489.5	628.5	COM36	630.0	1481.0
COM17	-1489.5	768.5	COM37	770.0	1481.0
COM18	-1489.5	908.5	COM38	910.0	1481.0
COM19	-1489.5	1048.5	COM39	1050.0	1481.0
COM20	-1489.5	1188.5	COM40	1190.0	1481.0
COM21	-1489.5	1328.5	COM41	1330.0	1481.0

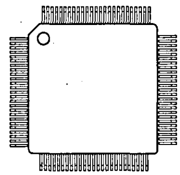
Die Size: 134.0 x 132.5 mil^2
Note: 1 mil ~ 25.4µm

LCD Segment Driver
CMOS

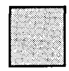
MC141518

The MC141518 is a high voltage passive LCD Segment driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 80 segment driving outputs for 64 MUX or lower LCD panel. The MC141518 is a companion chip of MC141516 (Backplane driver). It can be directly connected to the display controller inside the Motorola microcomputer MC68HC05L11.

- Operating Supply Voltage Range-
  Logic (V_{DD}): 2.7V to 5.5V
  Segment Drivers (V_{LCD}): 6.0V to 13V
- Operating Temperature Range: -20 to 70°C
- 80 LCD segment driving signals
- Driving Duty Cycle (MUX): 1/32 to 1/64
- Casadable for more LCD segment driving outputs
- Serial interface for both display data and control instruction transfers
- 100-pin TQFP (Thin Quad Flat Package)



MC141518FJ
TQFP

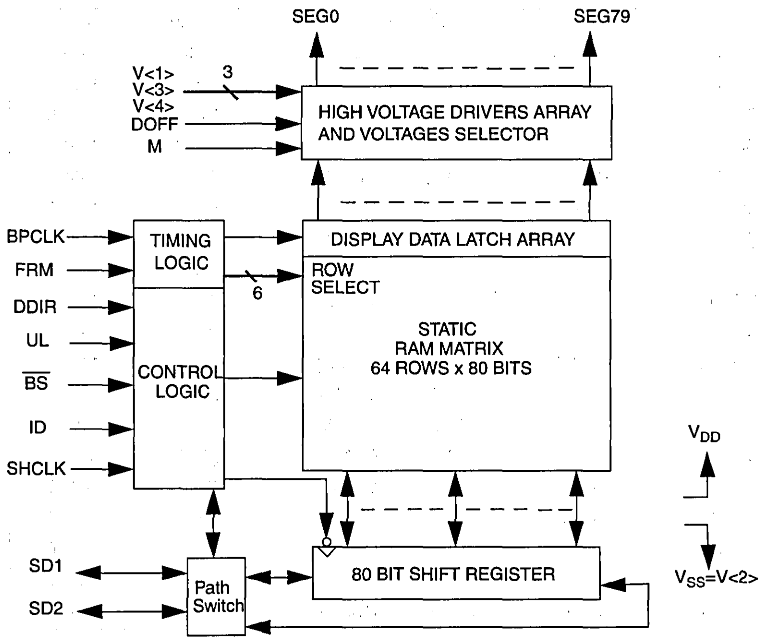


MCC141518
DIE

ORDERING INFORMATION

MC141518FJ	TQFP
MCC141518	DIE

BLOCK DIAGRAM



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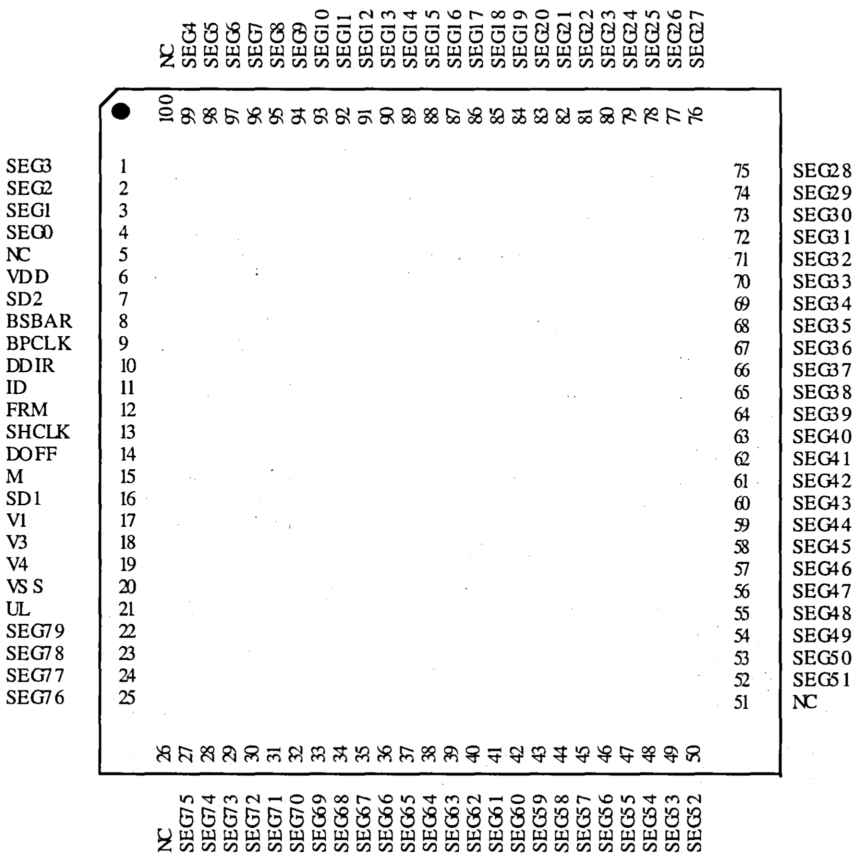
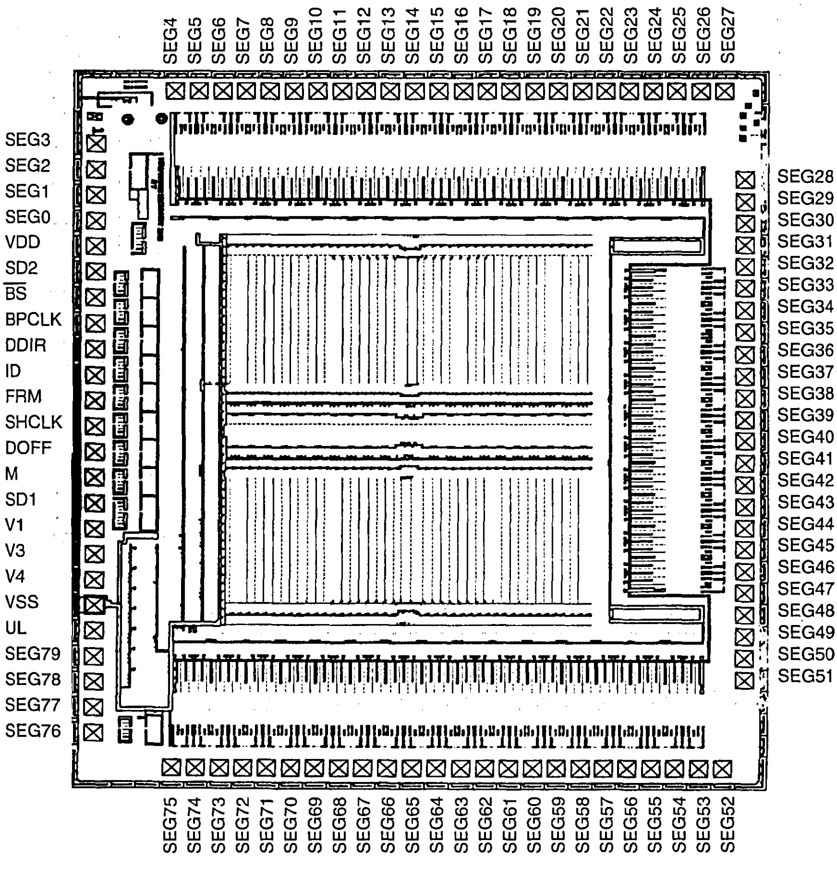


MC141518FJ Pin Assignment



MCC141518 PAD ASSIGNMENT

MAXIMUM RATINGS* (Voltages Reference to V_{SS}, T_A=25 °C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7	V
V<1>		V_{SS} -0.3 to V_{SS} +15	V
V_{in}	Input Voltage	V_{SS} -0.3 to V_{DD} +0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to +70	°C
T_{stg}	Storage Temperature Range	-65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description Section.

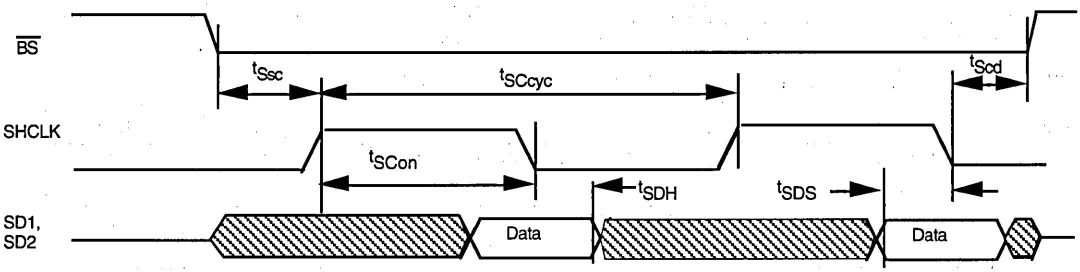
The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either VSS or VDD). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C,V_{DD}=5.0V, V<1>=13V)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage BPCLK, FRM, M, ID, DDIR $\overline{BS}$, SD1, SD2, SHCLK, DOFF	0.7xV_{DD}	V_{DD}	V
V_{IL}	Input Low Voltage BPCLK, FRM, M, ID, DDIR $\overline{BS}$, SD1, SD2, SHCLK, DOFF	V_{SS}	0.3xV_{DD}	V
V_R	Data Retention	2.0	-	V
I_{in}	Input Current BPCLK, FRM, M, ID, DDIR $\overline{BS}$,SD1, SD2, SHCLK, DOFF	-	±1	uA
C_{in}	Capacitance BPCLK, FRM, M, ID, DDIR, $\overline{BS}$,SD1, SD2, SHCLK, DOFF	-	8	pF
V_{OH}	Output High Voltage SD1, SD2	0.8xV_{DD}	V_{DD}	V
V_{OL}	Output Low Voltage SD1, SD2	V_{SS}	0.2xV_{DD}	V
	Operating Voltages			
V_{DD}	Supply Voltage (referenced to V_{SS})	2.7	5.5	V
V<1>	LCD Voltage (referenced to V_{SS})	0.0	+13	V
	Operating supply current V_{DD} (V_{DD}=5V, V<1>=13V, M=2MHz)			
I_{ACC}	Dynamic Mode (Display on, R/W access, BPCLK=4KHz, SHCLK=5MHz)	-	200	uA
I_{DP}	(Display on, R/W disable, BPCLK=4KHz)	-	20	uA
I_{SB}	Standby Mode(Display off, R/W disable)	-	5	uA
	Operating supply current V<1> (V<1>=13V)			
I_{LDP}	Display Mode	-	30	uA
I_{LSB}	Standby Mode	-	2	uA

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V +/-5%, V_{SS}=0, T_A=25°C, V<1>=13V)

Symbol	Parameter	Min	Max	Unit
t_{SCcyc}	Shift Clock Cycle Time	200	-	ns
t_{SCon}	Shift Clock On Time	100	-	ns
t_{SDS}	Serial Data Setup Time	50	-	ns
t_{SDH}	Serial Data Hold Time	10	-	ns
t_{Ssc}	Select to clock on	100	-	ns
t_{Ssc}	Clock on to device disable	10	-	ns



MC141518 Timing Diagram (with $\overline{BS}$ = 0)

PIN DESCRIPTIONS

V_{DD} and V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>,V<3>,V<4>

These are the inputs of voltage levels for the LCD driving signals (Fig. 2).

DOFF

This is an input pin to turn off the LCD. If it is set, all the high voltage drivers are switched off.

FRM

This is an input pin for frame timing synchronisation. This pin is connected either to FRM of the microcomputer MC68HC05L11 or to FRM of the Backplane driver MC141516.

BPCLK

This is an input pin for a periodic signal from the microcomputer to segment driver for timing synchronisation. This pin is connected either to BPCLK of the microcomputer MC68HC05L11 or to BPCLK of the Backplane driver MC141516.

SEG0-SEG79

These 80 output lines provide the segment driving signals to the LCD panel. They are all high impedance while the display is turned off (i.e. DOFF is selected).

$\overline{BS}$

This is the Bank Select pin. It is an active low input for chip enable.

UL

This pin is used to set the segment driver to support the Upper or Lower panel for a split LCD panel system. Since any segment driver to the upper panel will be 180 degree rotated with respect to the lower panel's segment drivers, to maintain easier routing and consistent in data format, the serial data direction has to be reversed. Therefore whenever UL is tied high, the serial data direction inside the segment drivers will be reversed with respect to the serial data direction as UL is ground. Details about the serial data direction can be found in the SD1, SD2 description.

SD1, SD2

These pins are two bidirectional serial data lines connected to either one of the two serial ports of the microcomputer MC68HC05L11 (UD1, UD2 LD1 and LD2) depending on the UL pin. If the segment driver is set to serve the upper panel with its UL tied high, serial data direction between SD1 and SD2 is reversed. In such case, SD1 is connected either to UD1 or to LD1 of MC68HC05L11. SD2 is then connected to UD2 or LD2 of MC68HC05L11. However, if the UL pin is ground, SD1 and SD2 are then connected to UD2 and UD1, or LD2 and LD1 of MC68HC05L11 respectively. SD1 and SD2 allow the display data or instruction from the microcomputer entering the segment driver in both directions. During $\overline{BS}$ high, these two pins are high impedance. In case of an instruction from the microcomputer with ID pin set. SD1 and SD2 are disconnected from the 80-bit shift register and form a transparent loop. Instruction bits entering the segment through a serial port (say SD1) are exported to its cascading device immediately through another serial port (i.e. SD2). In such a way, this instruction from the microcomputer can be broadcasted to a bank of cascading segments. See Typical Application Section for typical system connections.

ID

This is the Instruction/Data pin. If this pin is set, an instruction byte is shifting in from the bidirectional data lines as soon as $\overline{BS}$ goes low. Otherwise, data in the bidirectional lines is the display data. (See SD1 and SD2 definitions). Instructions are described in Table 2. Though each instruction has eight bits, the segment needs 12 SHCLK cycles to complete it. Eight cycles to fill in the internal instruction register and the last four cycles are use for instructions processing. Once the instruction is completed, additional SHCLK is ignored until $\overline{BS}$ signal toggles from high to low again. See Figure 1 for details. <u>Notice that intemal sampling for the instruction register should be as the order of MSB to LSB if DDIR is 0 and LSB to MSB if DDIR is 1, doesn't matter what UL is.</u>

SHCLK

This is the shift clock from the microcomputer MC68HC05L11 to the segment for clocking the serial data on SD1 and SD2.

DDIR

It is an input pin specifying the direction of the serial data. DDIR definition is also affected by UL pin as specified in Table 2. If UL pin is found low and DDIR is set, the serial data enters the segment driver through SD1 and leaves the segment driver through SD2. If both UL and DDIR are zeros, SD1 and SD2 are redefined as output and input respectively. If UL pin is high and DDIR is set, the serial data then enters the segment driver through SD2 and leaves the segment driver through SD1. If UL is high but DDIR is clear, SD2 and SD1 are output and input respectively.

UL	DDIR	Internal Serial Data Direction
0	0	—SD2———bidirectional shifter register———SD1—►
0	1	◄—SD2———bidirectional shifter register———SD1—
1	0	◄—SD2———bidirectional shifter register———SD1—
1	1	—SD2———bidirectional shifter register———SD1—►

Table 1. Summary of Data Direction Flow Responding To DDIR and UL Bit.

OPERATION OF LCD DRIVER

INTRODUCTION

The LCD segment driver is capable of 1:6 bias (for 32 mux) to 1:9 bias (for 64 mux), depending on the voltage divider ratio of Fig.2. The ratio of bias (a) is defined as

$$1:\frac{4xR1+R2}{R1}=1:a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a=\sqrt{mux}\ +1$$

To set up a multiplex ratio, please refer to either Section 10.6.2., the Technical data of MC68HC05L11 or the Advanced Information of the Backplane MC141516.

CONTROL LOGIC produces the control signals necessary for display RAM read/write and serial data latching. This Control Logic can be controlled by the MCU through the serial interface with ID set. MCU writing a byte of instruction (ID7 to ID0) to the Segment Control Register through the serial interface will cause Segment driver(s) to carry functions as shown as Table 2.

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	ROW ADDRESS (WRITE IN)					
0	1	ROW ADDRESS (READ FROM)					
1	0	SCROLL UP ADVANCE					
1	1	X	X	X	CLR SH	X	RESET

TABLE 2. A Summary of the Control Functions of Segment Driver

ROW ADDRESS(WRITE IN) instruction causes the segment driver(s) to load the content of the 80 BITS SHIFT REGISTER into a row of RAM which address is specified by ID5 to ID0.

ROW ADDRESS(READ FROM) instruction causes the segment driver(s) to copy a row of RAM which address is specified by ID5 to ID0 into the 80 BIT SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes the segment driver(s) to do vertically scroll up or down. The content of ID5 to ID0 represents the vertical offset of the new screen to the current screen. This vertical offset is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER. The sum of these is the new offset and will be stored in the VERTICAL SCROLL VECTOR REGISTER. The VERTICAL SCROLL VECTOR REGISTER is default zero during power-on.

RESET BIT0 Writing an "1" to this bit will clear the VERTICAL SCROLL VECTOR REGISTER.

CLRSH BIT2 Writing an "1" to this bit will clear the content of the 80 BIT SHIFT REGISTER.

An instruction (ID7 to ID0) is transferred to the segment driver through the serial interface as Figure 1 demonstrated. Figure 1-a shows a case that the DDIR bit is clear. The most significant bit ID7 of the instruction will come in as the first bit. After 8 SHCLK cycles, a byte of instruction data is kept in an instruction register. However, the instruction needs another 4 cycles to complete, as long as $\overline{BS}$ holds low, segment driver will wait for these 4 cycles to complete the instruction. After the instruction, the segment driver will ignore any coming SHCLK cycle until the signal $\overline{BS}$ toggles from high to low again. Figure 1-b shows in case of DDIR bit set. The UL bit will not affect the order of instruction shifting. For most case, user does not need to worry about the order of shifting if the segment is connected to the display controller in the microcomputer MC68HC05L11.

TIMING LOGIC, according to BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix's content periodically starting from the row address specified in the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels among <V1>, <V3>, <V4> and <V2>. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 64 rows x 80 bits of SRAM cell. The content of these RAM cells can be read from/written to the 80 BIT SHIFT REGISTER.

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as seg(x) in Fig. 3.

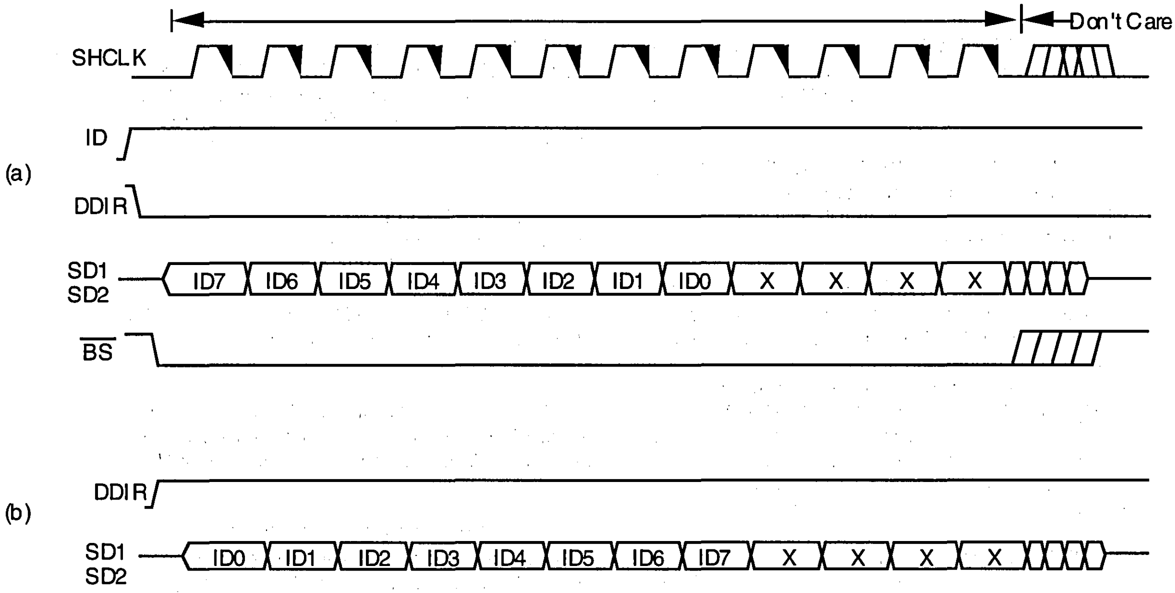


Figure 1. The order of Instruction byte shifted

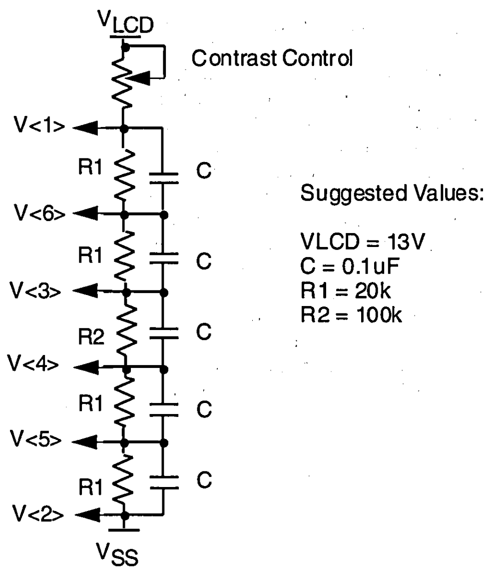


Figure 2. External Voltage Divider

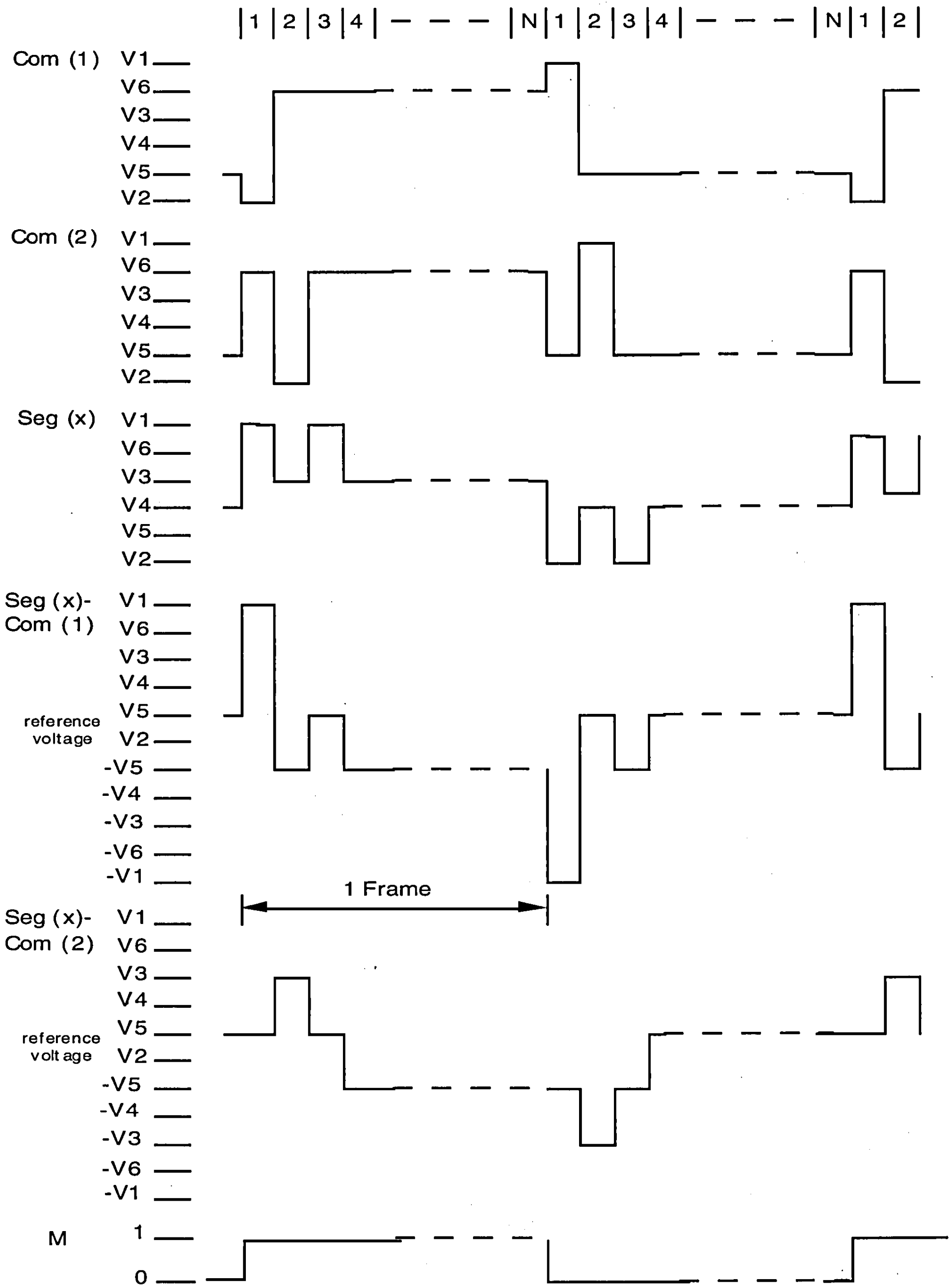
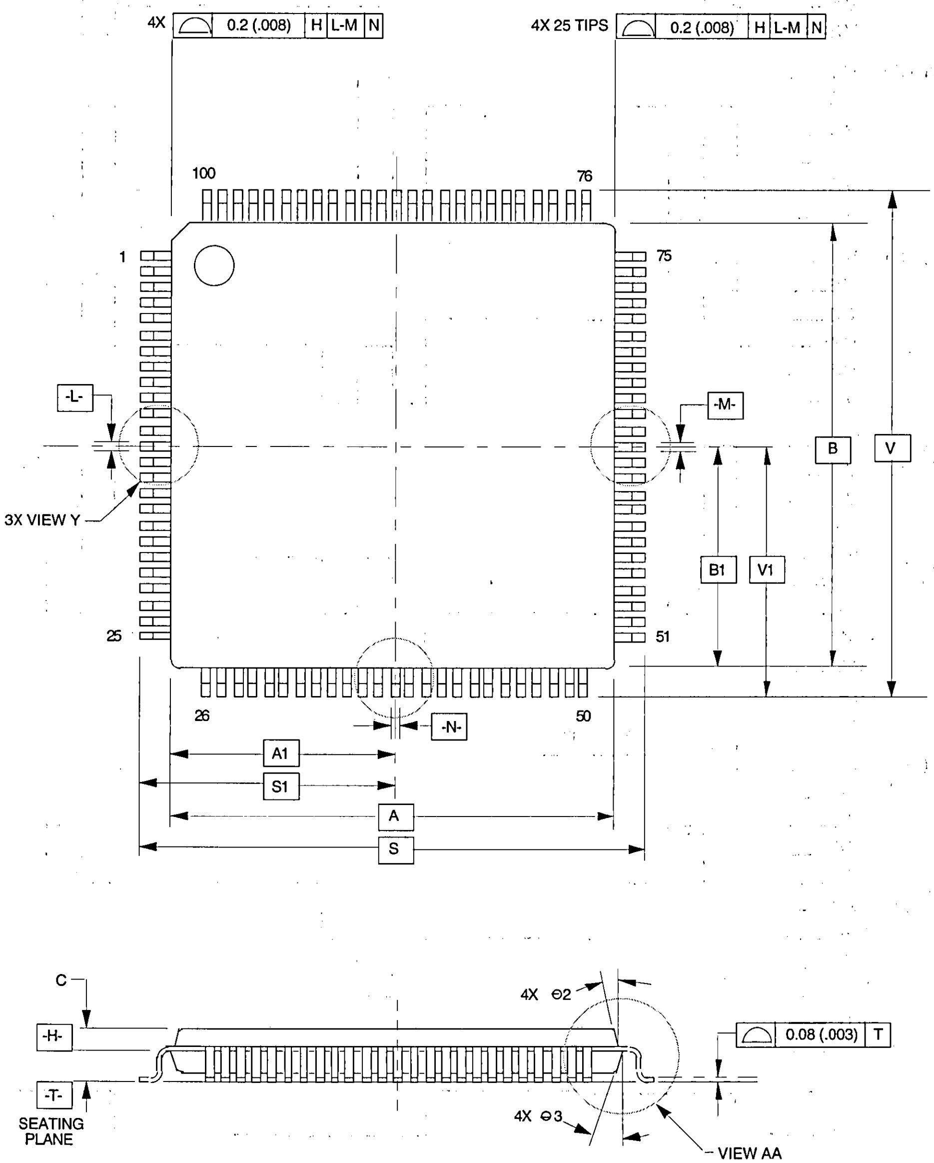


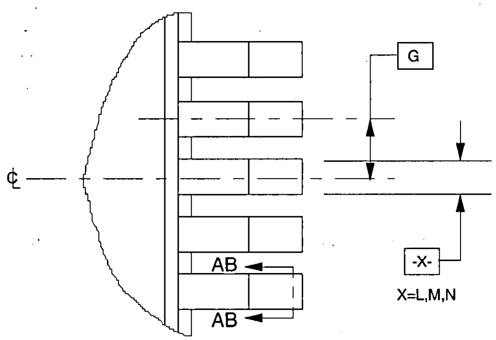
Figure 3. Driving waveforms of 1:N multiplex

PACKAGE DIMENSIONS

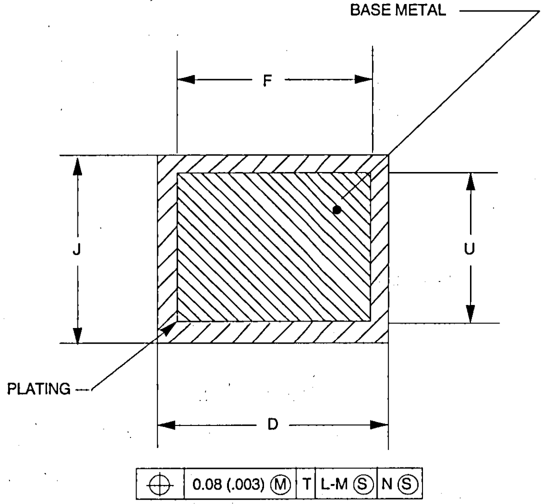
MC141518FJ
TQFP PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



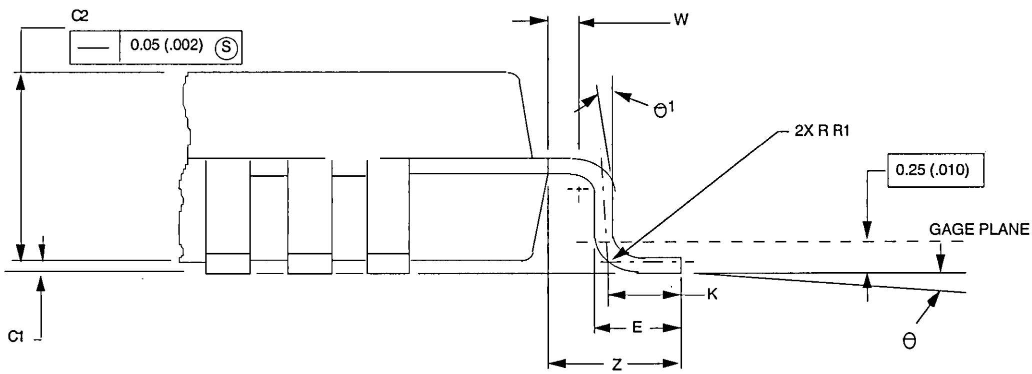
MC141518FJ
TQFP PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



VIEW Y



SECTION AB-AB
ROTATED 90° CLOCKWISE



VIEW AA

MC141518FJ TQFP PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	14.00	BSC	.551	BSC	K	0.50	REF	.020	REF
A1	7.00	BSC	.276	BSC	R1	0.08	0.20	.003	.008
B	14.00	BSC	.551	BSC	S	16.00	BSC	.630	BSC
B1	7.00	BSC	.276	BSC	S1	8.00	BSC	.315	BSC
C	---	1.70	---	.066	U	0.09	0.16	.004	.006
C1	0.05	0.20	.002	.008	V	16.00	BSC	.630	BSC
C2	1.30	1.50	.051	.059	V1	8.00	BSC	.315	BSC
D	0.10	0.30	.004	.012	W	0.20	REF	.008	REF
E	0.45	0.75	.016	.030	Z	1.00	REF	.039	REF
F	0.15	0.23	.006	.009	θ	0°	7°	0°	7°
G	0.50	BSC	.020	BSC	θ1	0°	---	0°	---
J	0.07	0.20	.003	.008	θ2	12°	REF	12°	REF
					θ3	12°	REF	12°	REF

NOTES:

1. Dimensions and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane $\boxed{\text{-H-}}$ is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums $\boxed{\text{-L-}}$, $\boxed{\text{-M-}}$ and $\boxed{\text{-N-}}$ to be determined at datum plane $\boxed{\text{-H-}}$.
5. Dimensions S and V to be determined at seating plane $\boxed{\text{-T-}}$.
6. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.25(.010) per side. Dimensions A and B do include mold mismatch and are determined at datum plane $\boxed{\text{-H-}}$.
7. Dimension D does not include dambar protrusion. Dambar protrusion shall not cause the lead width to exceed 0.46 (.018). Minimum space between protrusion and adjacent lead or protrusion 0.07 (.003).

MCC141518 PAD COORDINATES: (UNIT: μM)

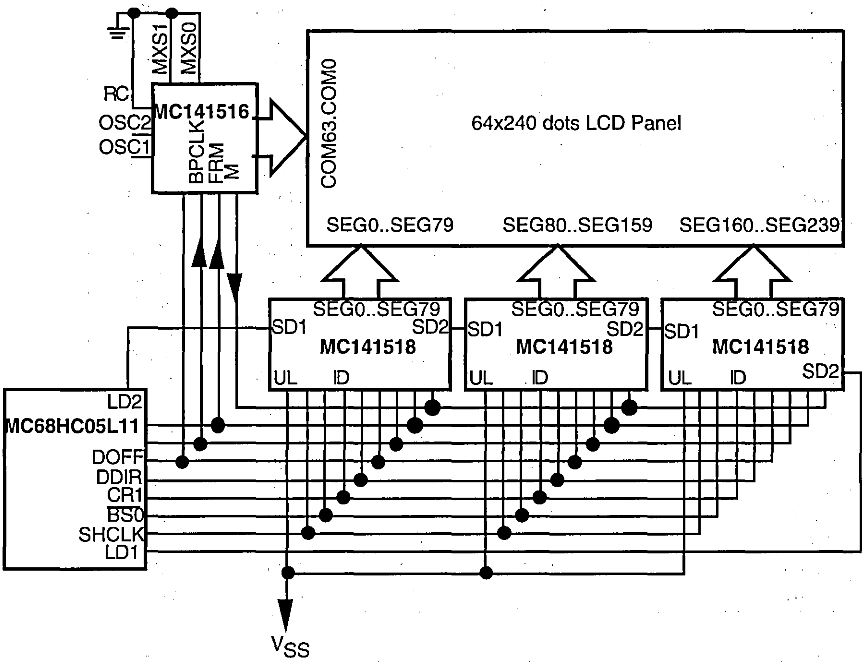
PIN NAME	X	Y	PIN NAME	X	Y
SEG3	-1835.9	-1898.5	SEG75	2180.1	-1442.5
SEG2	-1670.9	-1898.5	SEG74	2180.1	-1302.5
SEG1	-1505.9	-1898.5	SEG73	2180.1	-1162.5
SEG0	-1340.9	-1898.5	SEG72	2180.1	-1022.5
V_{DD}	-1175.9	-1898.5	SEG71	2180.1	-882.5
SD2	-1010.9	-1898.5	SEG70	2180.1	-742.5
$\overline{BS}$	-845.9	-1898.5	SEG69	2180.1	-602.5
BPCLK	-680.9	-1898.5	SEG68	2180.1	-462.5
DDIR	-515.9	-1898.5	SEG67	2180.1	-322.5
ID	-350.9	-1898.5	SEG66	2180.1	-182.5
FRM	-185.9	-1898.5	SEG65	2180.1	-42.5
SHCLK	-20.9	-1898.5	SEG64	2180.1	97.5
DOFF	144.1	-1898.5	SEG63	2180.1	237.5
M	309.1	-1898.5	SEG62	2180.1	377.5
SD1	474.1	-1898.5	SEG61	2180.1	517.5
V1	639.1	-1898.5	SEG60	2180.1	657.5
V3	804.1	-1898.5	SEG59	2180.1	797.5
V4	969.1	-1898.5	SEG58	2180.1	937.5
V_{SS}	1134.1	-1898.5	SEG57	2180.1	1077.5
UL	1299.1	-1898.5	SEG56	2180.1	1217.5
SEG79	1464.1	-1898.5	SEG55	2180.1	1357.5
SEG78	1629.1	-1898.5	SEG54	2180.1	1497.5
SEG77	1794.1	-1898.5	SEG53	2180.1	1637.5
SEG76	1959.1	-1898.5	SEG52	2180.1	1777.5

PIN NAME	X	Y	PIN NAME	X	Y
SEG4	-2179.9	-1442.5	SEG28	-1609.9	1898.5
SEG5	-2179.9	-1302.5	SEG29	-1469.9	1898.5
SEG6	-2179.9	-1162.5	SEG30	-1329.9	1898.5
SEG7	-2179.9	-1022.5	SEG31	-1189.9	1898.5
SEG8	-2179.9	-882.5	SEG32	-1049.9	1898.5
SEG9	-2179.9	-742.5	SEG33	-909.9	1898.5
SEG10	-2179.9	-602.5	SEG34	-769.9	1898.5
SEG11	-2179.9	-462.5	SEG35	-629.9	1898.5
SEG12	-2179.9	-322.5	SEG36	-489.9	1898.5
SEG13	-2179.9	-182.5	SEG37	-349.9	1898.5
SEG14	-2179.9	-42.5	SEG38	-209.9	1898.5
SEG15	-2179.9	97.5	SEG39	-69.9	1898.5
SEG16	-2179.9	237.5	SEG40	70.1	1898.5
SEG17	-2179.9	377.5	SEG41	210.1	1898.5
SEG18	-2179.9	517.5	SEG42	350.1	1898.5
SEG19	-2179.9	657.5	SEG43	490.1	1898.5
SEG20	-2179.9	797.5	SEG44	630.1	1898.5
SEG21	-2179.9	937.5	SEG45	770.1	1898.5
SEG22	-2179.9	1077.5	SEG46	910.1	1898.5
SEG23	-2179.9	1217.5	SEG47	1050.1	1898.5
SEG24	-2179.9	1357.5	SEG48	1190.1	1898.5
SEG25	-2179.9	1497.5	SEG49	1330.1	1898.5
SEG26	-2179.9	1637.5	SEG50	1470.1	1898.5
SEG27	-2179.9	1777.5	SEG51	1610.1	1898.5

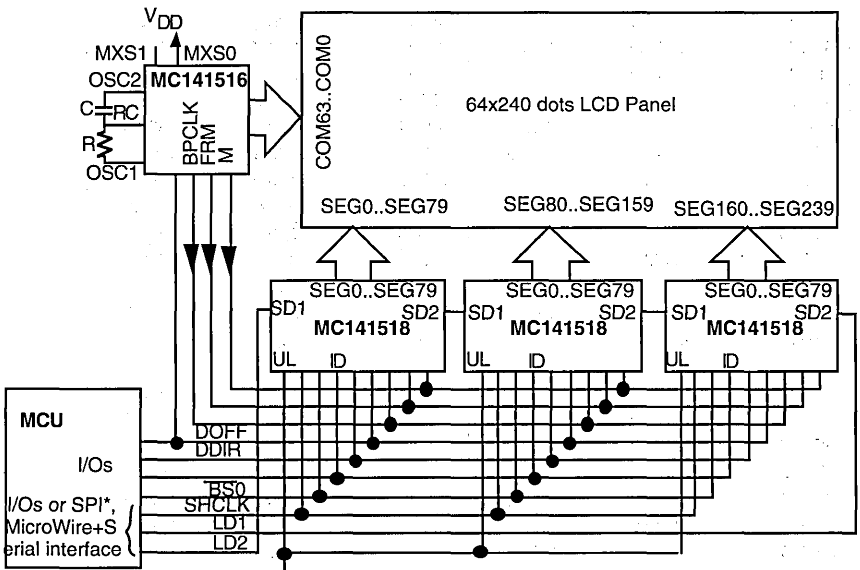
Die size: 193.5 x 167.0 mil^2
Note: 1 mil ~ 25.4μm

TYPICAL APPLICATIONS

64x240 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11

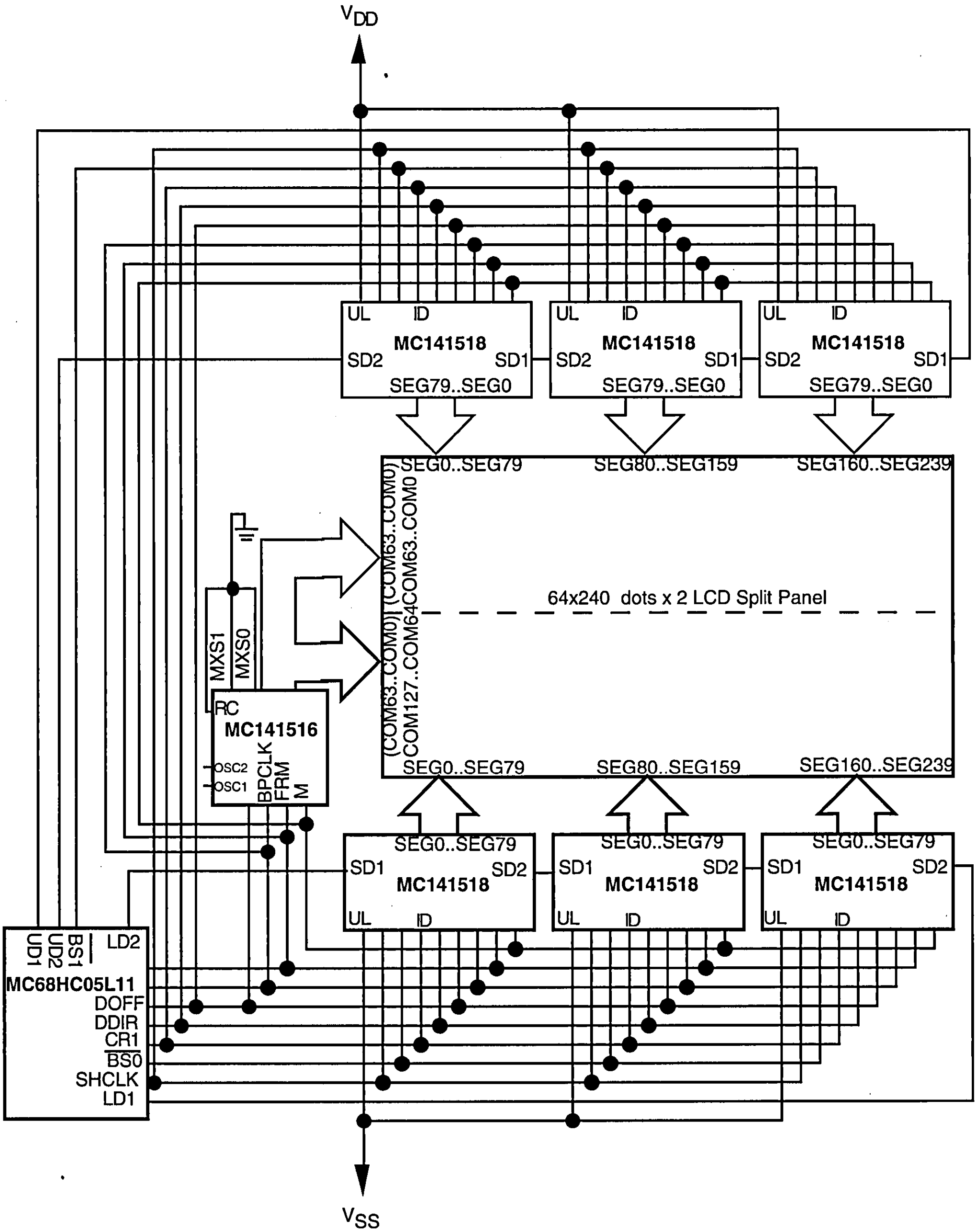


64x240 SINGLE PANEL LCD SYSTEM WITH OTHER MCU



SPI* is Motorola's Serial Peripherial Interface.MicroWire+ is a serial interface from National Semiconductor

64x240x2 SPLIT PANEL LCD SYSTEM



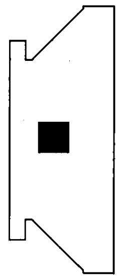
MC141519

LCD Segment Driver
CMOS

The MC141519 is an LCD segment driver chip which consists of 160x80 static RAM for display storage and provides 160 high voltage LCD driving signals.

It is a companion chip of MC141512T Backplane driver for medium LCD panels. All these chips are controlled by the MC68HC05L11 microcomputer.

- Operating Supply Voltage Range-
  - Control Logic, RAM and Latch (V_{DD} Pin): 2.7 to 5.5V
  - Segment drivers (V_{LCD} Pin): 8.0 to 20V
- Operating Temperature Range: -20 to 80˚C
- Direct serial data interface with the MC68HC05L11
- 160 x 80 Static RAM (Display RAM)
- 160 LCD Segment Driving Signals
- Selectable 1:16 to 1:80 Multiplex Ratios
- Expansion to higher driver count by cascade
- Available in TAB Form:
  - TAB (Tape Automated Bonding), 186 contacts

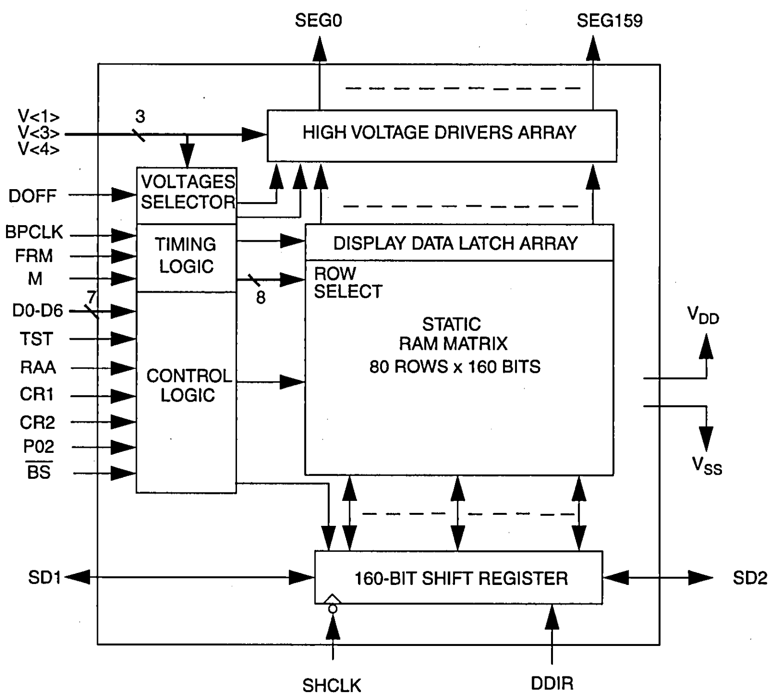


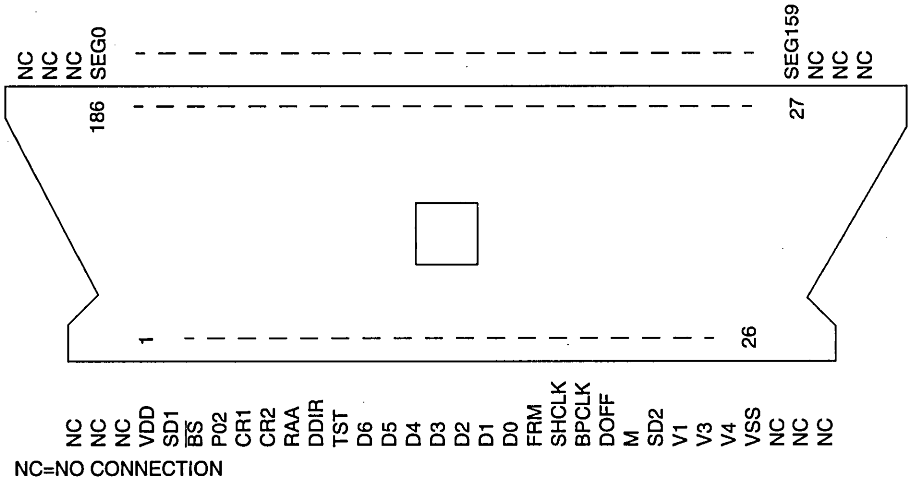
MC141519T
TAB

ORDERING INFORMATION

MC141519T TAB

BLOCK DIAGRAM





TAB Package Pin Assignment (copper view)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +7.0	V
V<1>		V_{SS}-0.3 to V_{SS}+22.0	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to 80	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

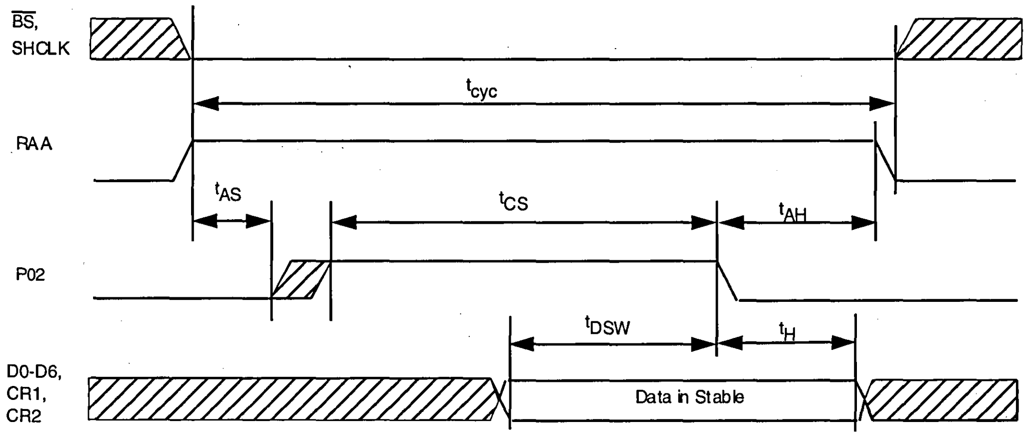
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C, V_{DD} = 5.0V)

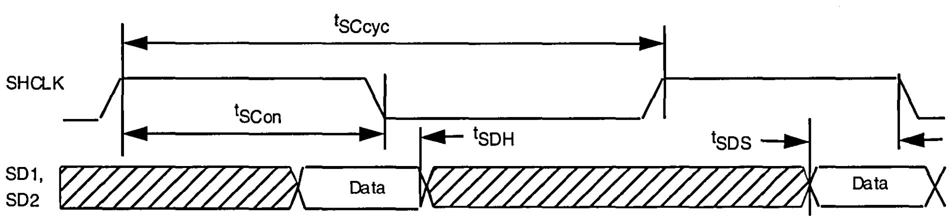
Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input High Voltage BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	0.7xV_{DD}	-	V_{DD}	V
V_{IL}	Input Low Voltage BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	V_{SS}	-	0.3xV_{DD}	V
V_R	Data Retention	2.0	-	-	V
I_{in}	Input Current BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	-	-	±1	uA
C_{in}	Capacitance BPCLK, FRM,P02,RAA,CR1,CR2,$\overline{BS}$, D6-D0,SD1,SD2,SHCLK,DOFF,M,DIRR	-	-	8	pF
V_{OH}	Output High Voltage SD1,SD2	0.8xV_{DD}	-	V_{DD}	V
V_{OL}	Output Low Voltage SD1,SD2	V_{SS}	-	0.2xV_{DD}	V
	Operating Voltages				
V_{DD}	Supply Voltage (referenced to V_{SS})	2.7	-	5.5	V
V<1>	LCD Voltage (referenced to V_{SS})	8.0	-	20.0	V
	Operating supply current (V_{DD})(V_{DD}=5V, referenced to V_{SS})				
I_{ACC}	Access Mode	-	150	200	uA
I_{DP}	Display Mode	-	30	100	uA
I_{SB}	Standby Mode	-	1	10	uA
	Operating supply current (V<1>)(V<1>=20V, referenced to V_{SS})				
I_{LDP}	Display Mode	-	12	20	uA
I_{LSB}	Standby Mode	-	1	10	uA

AC ELECTRICAL CHARACTERISTICS(V_{DD}=2.7V-5.5V, V_{SS}=0, T_A=25°C)

Symbol	Parameter	Min	Max	Unit
t_{cyc}	Access Cycle Time	235	-	ns
t_{AS}	Access Set up Time	100	-	ns
t_{AH}	RAA Hold Time	0	-	ns
t_{CS}	Chip Select Pulse Width	135	-	ns
t_{DSW}	Data SetUp Time	100	-	ns
t_H	Input Hold Time	10	-	ns
t_{SCcyc}	Shift Clock Cycle Time	200	-	ns
t_{SCon}	Shift Clock On Time	100	-	ns
t_{SDS}	Serial Data Setup Time	50	-	ns
t_{SDH}	Serial Data Hold Time	10	-	ns



Parallel Access Timing



Serial Access Timing (with $\overline{BS}$ = 0)

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

Power is supplied to the driver using these two pins. V_{DD} is power and V_{SS} is ground.

V<1>, V<3>, V<4>

These are the levels of voltage generated from an external voltages divider (Fig. 2). These voltage provide different voltage levels for shaping up the display output waveforms Seg0 - Seg159.

DOFF

This is an output from MC68HC05L11 to signal the backplane driver to turn off LCD. If this pin is clear, the segment driver supplies LCD with driving signal. If this pin is set, the segment driver outputs is high-impedance and LCD display is disabled.

FRM

A periodic active high input to the segment driver for frame timing synchronization. This pin is connected to the signal FRM of MC68HC05L11. The frequency depends on the bias ratio and BPCLK signal.

BPCLK

A periodic clock output from MC68HC05L11 to the segment driver for timing synchronization. The signal controls the refresh timing of LCD display.

M

A periodic output from backplane driver. This pin is used for synchronization among display drivers.

D0 - D6

A seven-bit input-only data bus which is connected to the D0 - D6 of MC68HC05L11. These pins are used for address input and control input. Refer to Fig.1 for definition.

TST

The test pin should be pulled-low or connected to D7 of MC68HC05L11 during normal operation.

P02

A bus clock input that is used for data bus timing synchronization. This pin is connected to P02 of MC68HC05L11.

$\overline{BS}$

This is an active low input for chip select.

RAA

It is a strobe signal from MC68HC05L11 indicating that a valid segment control data is on D0 - D6 for a period of P02.

CR1, CR2

These two control signals from MC68HC05L11 to Segment driver describing the nature of the content in D0 - D6. The effect of CRs are shown on Fig 1.

SD1, SD2

These two pins are two bi-directional data lines connecting to the UD2 or LD2 and UD1 or LD1 respectively. These allow the display data from MC68HC05L11 entering the segment driver in both directions.

SHCLK

This is the shift clock from MC68HC05L11 to segment driver for clocking the serial data on SD1 and SD2. See Timing Diagram for illustration.

DDIR

It is an input pin carrying the signal from MC68HC05L11 to segment driver to control the direction of the serial data. In lower panel mode, if DDIR is set, the serial data enters the segment driver through SD1 and leaves the segment driver through SD2. If DDIR is clear, SD1 and SD2 are redefined as an output and input respectively.

SEG0 - SEG159

These 160 output lines provide the segment driving signal to the LCD panel. They are all in high-impedance state while the display is turned off (i.e. DOFF is set).

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

INTRODUCTION

The LCD segment driver can support multiplex ratio of a LCD system up to 80 and cascading of more than one driver for expansion is possible. It can be set from 1:5 bias (for 16 mux) to 1:10 bias (for 80 mux), by the voltage divider ratio of Fig.2. The ratio of bias or the contrast ratio (a) is defined as

$$1:\frac{4xR1 + R2}{R1} = 1:a$$

As the multiplex ratio changes, the ratio of bias has to be changed accordingly. The ratio of bias relates to the multiplex ratio as

$$a = \sqrt{mux} + 1$$

To set up a multiplex ratio, please refer to *MC68HC05L11D/H Technical Data Section 10.*

CONTROL LOGIC produces the control signals necessary for display RAM read / write and serial data latching. This Control Logic is directly supervised by the MCU through the Data Bus, i.e. D0 - D6, CR1 and CR2. MCU writing a byte of instruction to the Segment Control Register will cause Segment Driver(s) to fetch this instruction from the Data Bus and the command executed at the next P02 cycle. Fig.1 shows the *functions of which the Control Logic will carry out in respond to* MCU access through the Segment Control Register.

ROW ADDRESS(WRITE IN) instruction causes Segment driver(s) to load the content of the SHIFT REGISTER into a row of RAM which address is specified by D6 to D0.

ROW ADDRESS(READ FROM) instruction causes Segment driver(s) to copy a row of RAM which address is specified by D6 to D0 into the 160 BIT SHIFT REGISTER.

SCROLL UP ADVANCE instruction causes Segment driver(s) to do a vertical scroll up or down.

The content of D6 to D0 only represents the vertical offset of the new screen to the current screen. This vertical offset presenting in the Data Bus then is added up with an old offset which is stored in a register called the VERTICAL SCROLL VECTOR REGISTER to generate a new offset. This new offset will then be stored in the VERTICAL SCROLL VECTOR REGISTER. Periodically the content of this register will be fetched and loaded into a presettable counter in the TIMING LOGIC to generate the row addresses for screen refreshing.

RESET	BIT0	Writing a "1" to this bit will set the VERTICAL SCROLL VECTOR REGISTER to zero.
UL	BIT1	If this bit is set, the segment driver serves the upper panel in case of splitted panel. This will cause a swap in signals flow between SD1 and SD2.
CLRSH	BIT2	Writing an "1" to this bit will clear the content of the 160-BIT SHIFT REGISTER.

TIMING LOGIC, *according to* M, BPCLK and FRM, fills the DISPLAY DATA LATCH ARRAY with rows of RAM matrix's content periodically starting from the row address specified by the VERTICAL SCROLL VECTOR REGISTER.

VOLTAGES SELECTOR consists of switching circuit to select appropriate voltage levels from the external voltage divider. (See Fig. 2).

DISPLAY DATA LATCH ARRAY is used to buffer up a row of display data from RAM.

STATIC RAM MATRIX consists of 160x80 bits of SRAM cell. The content of these RAM cells can be altered by read/write from/ to the shift register with the Segment Control Interface (refer to MC68HC05L11D/H Technical Data Section 10).

HIGH VOLTAGE DRIVERS ARRAY is a row of high voltage drivers connecting to segment lines of any LCD panel. The output waveform of the high voltage driver is shown as Seg(x) in Fig 3.

SHIFT REGISTER is a 160-bit bi-directional register which acts as an input either from SD1 or SD2. The direction of data flow depends on the content of DDIR. And, it can be swapped by setting the UL bit to high. Data enter this shift register in serial. Shift register latches data at the falling edge of the signal SHCLK. See Timing Diagram for illustration.

CR2	CR1	D6	D5	D4	D3	D2	D1	D0
0	0	ROW ADDRESS (WRITE IN)						
0	1	ROW ADDRESS (READ FROM)						
1	0	SCROLL UP ADVANCE						
1	1	X	X	X	X	CLR SH	UL	RESET

FIGURE 1 - A Summary of the Control Functions of Segment Driver

DDIR	UL	SD1	SD2
1	0	input	output
0	0	output	input
1	1	output	input
0	1	input	output

FIGURE 1A - Relationship between DDIR, UL, SD1 and SD2

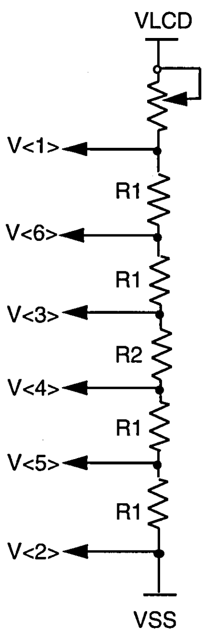


FIGURE 2 - External Voltage Divider

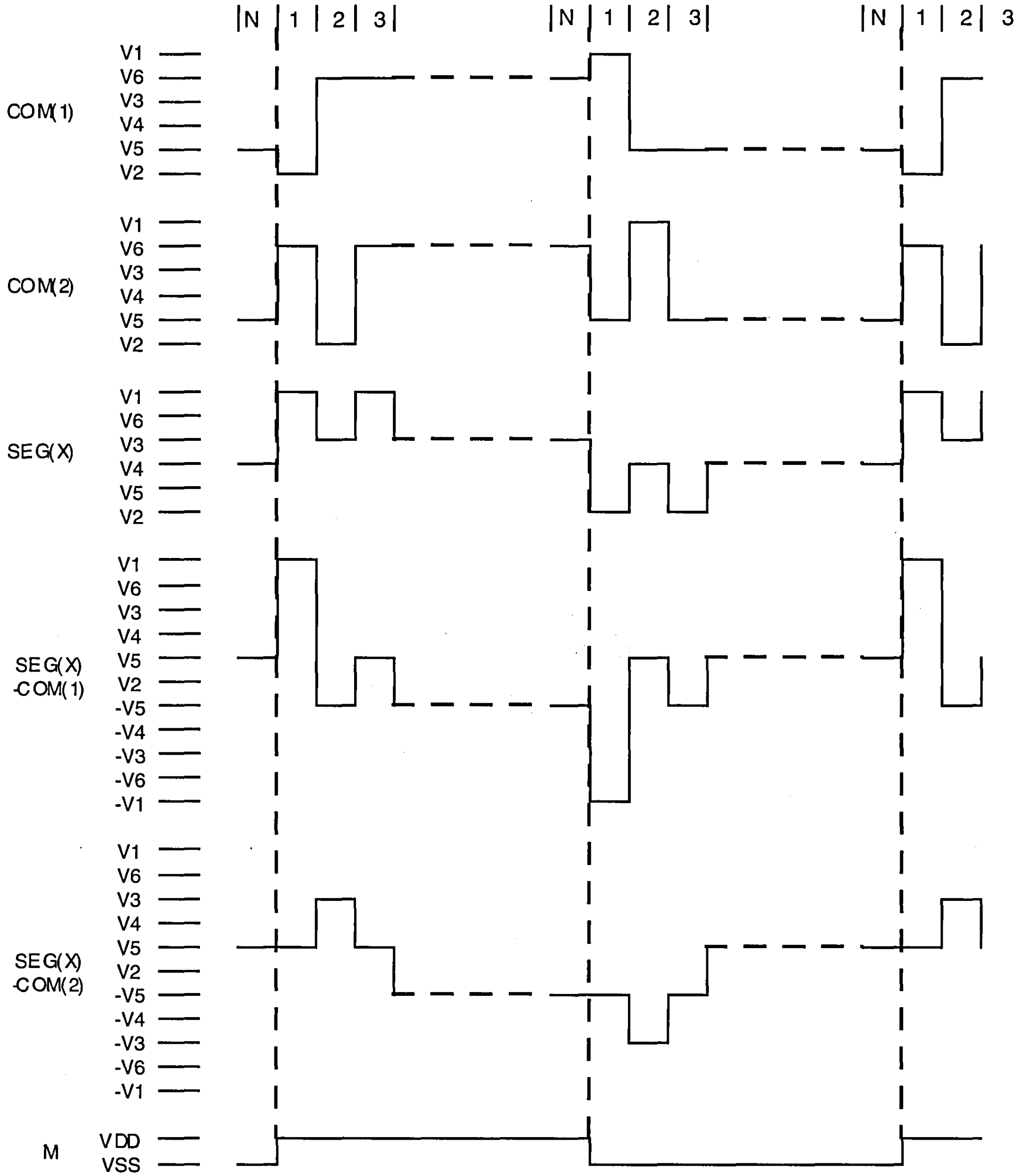
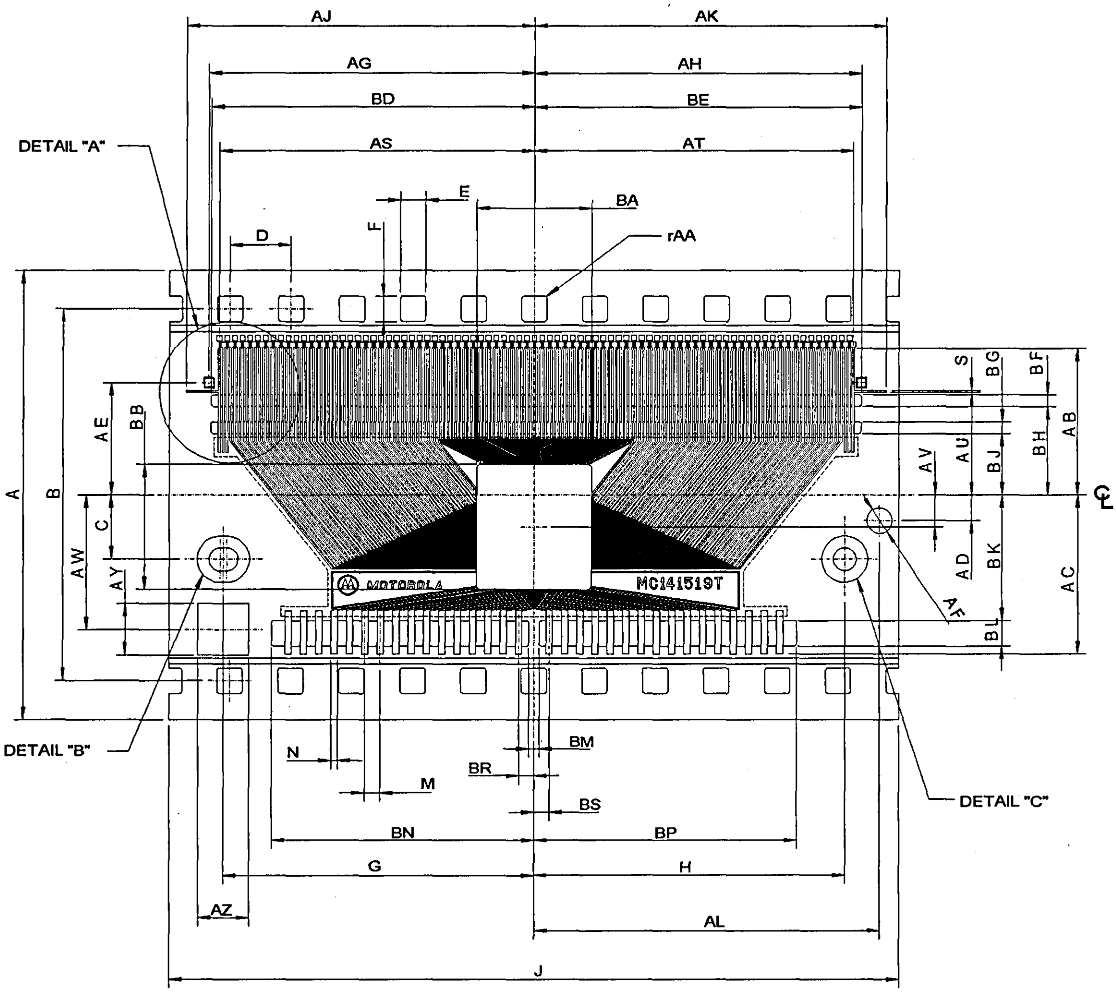
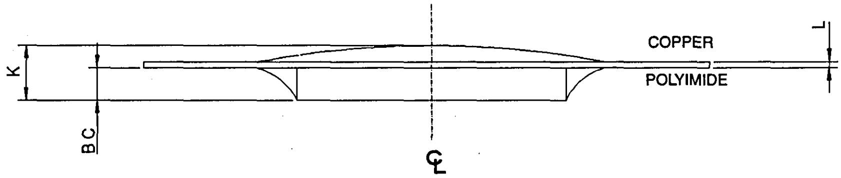


FIGURE 3 - Driving Waveforms of 1:N multiplex
(M is used for timing synchronization)

PACKAGE DIMENSIONS

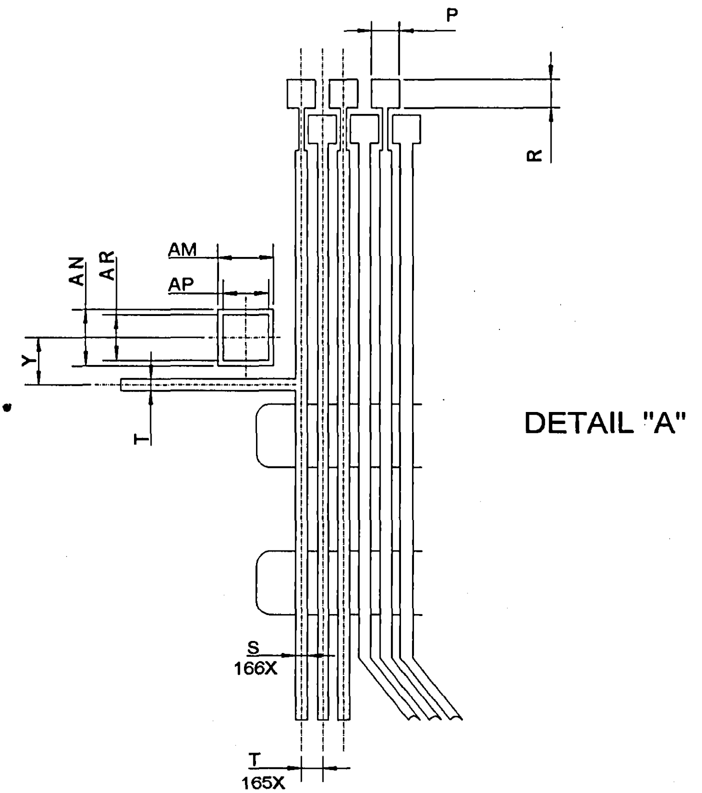
MC141519T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)

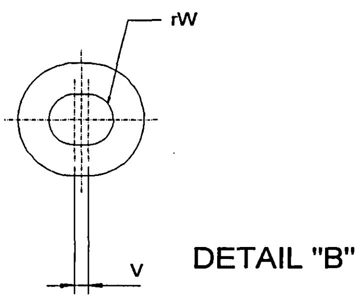


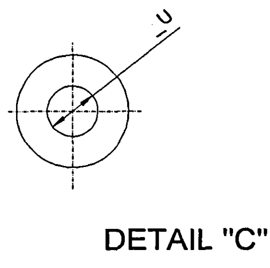


Reference: 98ASL00157A	Issue "0" released on 08/12/94

MC141519T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)







Reference: 98ASL00157A	Issue "0" released on 08/12/94

MC141519T TAB PACKAGE DIMENSION

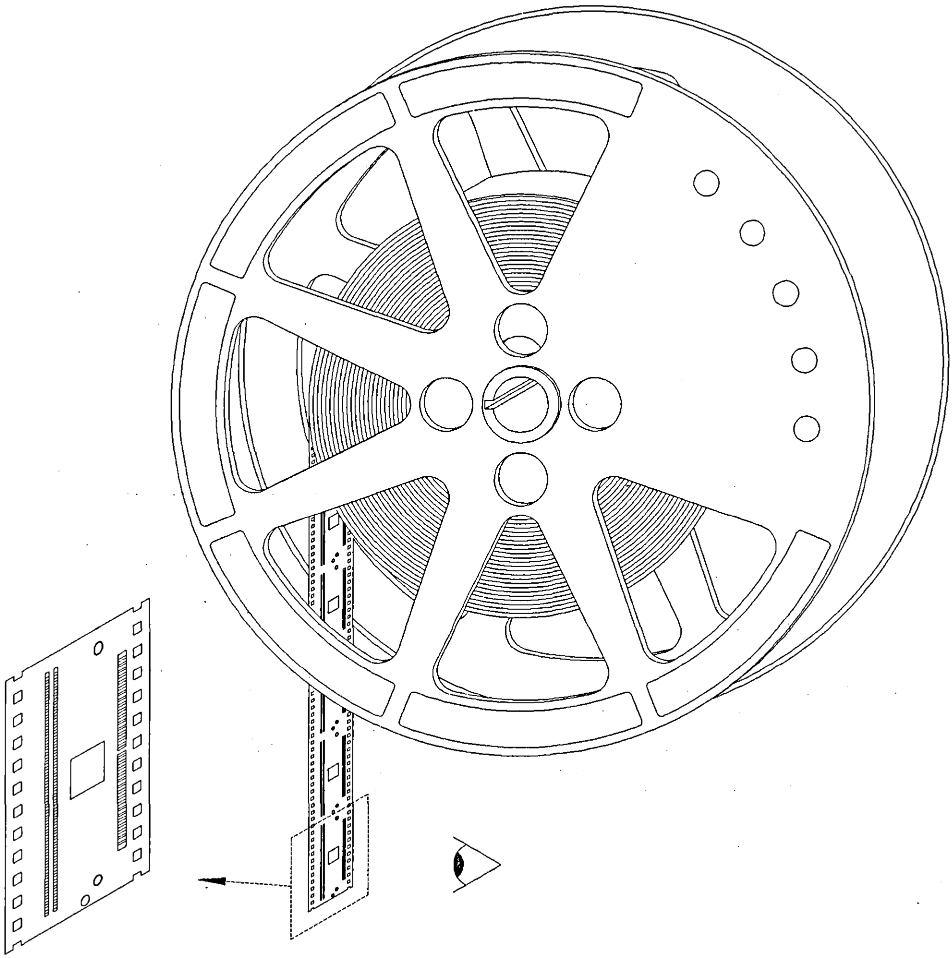
	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	34.775	35.175	1.3691	1.3848	AK	27.430	27.530	1.0799	1.0839
B	28.927	29.027	1.1389	1.1428	AL	26.500	27.500	1.0433	1.0827
C	4.950	5.050	0.1949	0.1988	AM	0.750	0.850	0.0295	0.0335
D	4.720	4.780	0.1858	0.1882	AN	0.750	0.850	0.0295	0.0335
E	1.951	2.011	0.0768	0.0792	AP	0.600	0.700	0.0236	0.0276
F	1.951	2.011	0.0768	0.0792	AR	0.600	0.700	0.0236	0.0276
G	24.200	24.300	0.9528	0.9567	AS	24.551	24.649	0.9666	0.9704
H	24.200	24.300	0.9528	0.9567	AT	24.850	24.950	0.9784	0.9823
J	56.500	57.500	2.2244	2.2638	AU	7.937	8.037	0.3125	0.3164
K	0.686	0.838	0.0270	0.0330	AV	2.450	2.550	0.0965	0.1004
L	0.0675	0.0825	0.0027	0.0033	AW	10.000	11.000	0.3937	0.4331
M	1.190	1.210	0.0469	0.0476	AY	3.500	4.500	0.1378	0.1772
N	0.480	0.520	0.0189	0.0205	AZ	3.500	4.500	0.1378	0.1772
P	0.350	0.450	0.0138	0.0177	BA	-	8.996	-	0.3542
R	0.350	0.450	0.0138	0.0177	BB	-	9.750	-	0.3839
S	0.150	0.190	0.0059	0.0075	BC	0.5794	0.6294	0.0228	0.0248
T	0.290	0.310	0.0114	0.0122	BD	25.200	25.300	0.9921	0.9961
U	1.750	1.850	0.0689	0.0728	BE	25.500	25.600	1.0039	1.0079
V	0.450	0.550	0.0177	0.0217	BF	0.850	0.950	0.0335	0.0374
W	0.850	0.950	0.0335	0.0374	BG	0.850	0.950	0.0335	0.0374
Y	0.622	0.722	0.0245	0.0284	BH	6.850	6.950	0.2697	0.2736
AA	-	0.20	-	0.0079	BJ	4.750	4.850	0.1870	0.1909
AB	10.900	11.900	0.4291	0.4685	BK	9.750	9.850	0.3839	0.3878
AC	12.150	12.650	0.4783	0.4980	BL	1.950	2.050	0.0768	0.0807
AD	1.500	2.500	0.0591	0.0984	BM	0.750	0.850	0.0295	0.0335
AE	8.690	8.790	0.3421	0.3461	BN	20.450	20.550	0.8051	0.8091
AF	1.950	2.050	0.0768	0.0807	BP	20.450	20.550	0.8051	0.8091
AG	25.350	25.450	0.9980	1.0020	BR	1.150	1.250	0.0453	0.0492
AH	25.510	25.610	1.0043	1.0083	BS	1.150	1.250	0.0453	0.0492
AJ	27.130	27.230	1.0681	1.0720					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1oz.
4. Tin plating thickness: 0.4um.
5. 12 sprocket hole device.

Reference: 98ASL00157A	Issue "0" released on 08/12/94

MC141519T

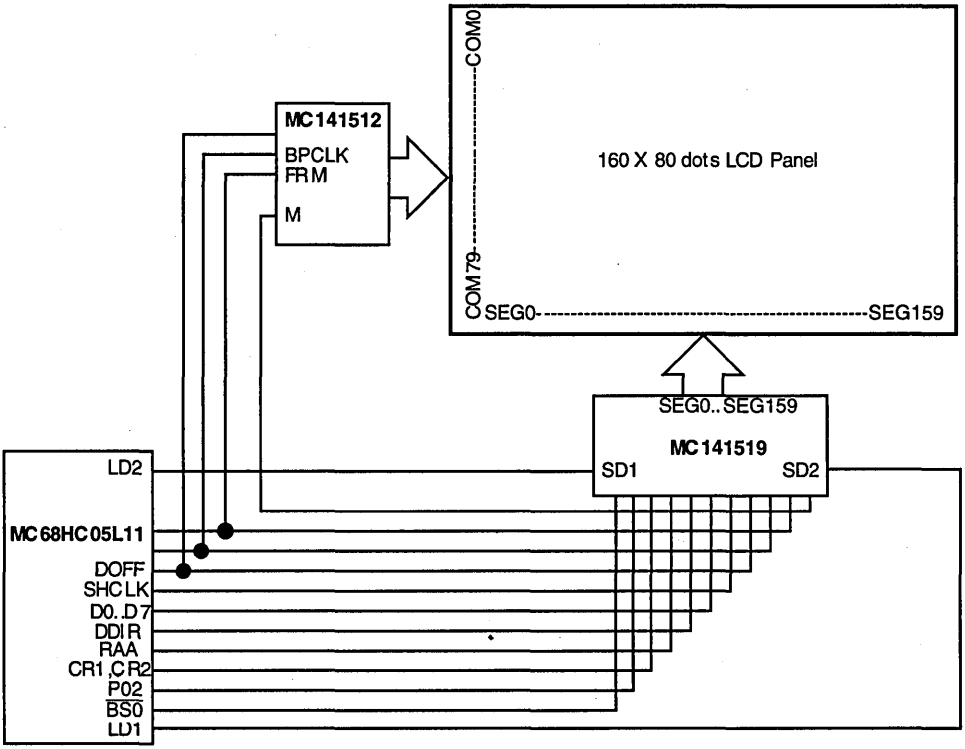
TAB TAPE REEL ORIENTATION



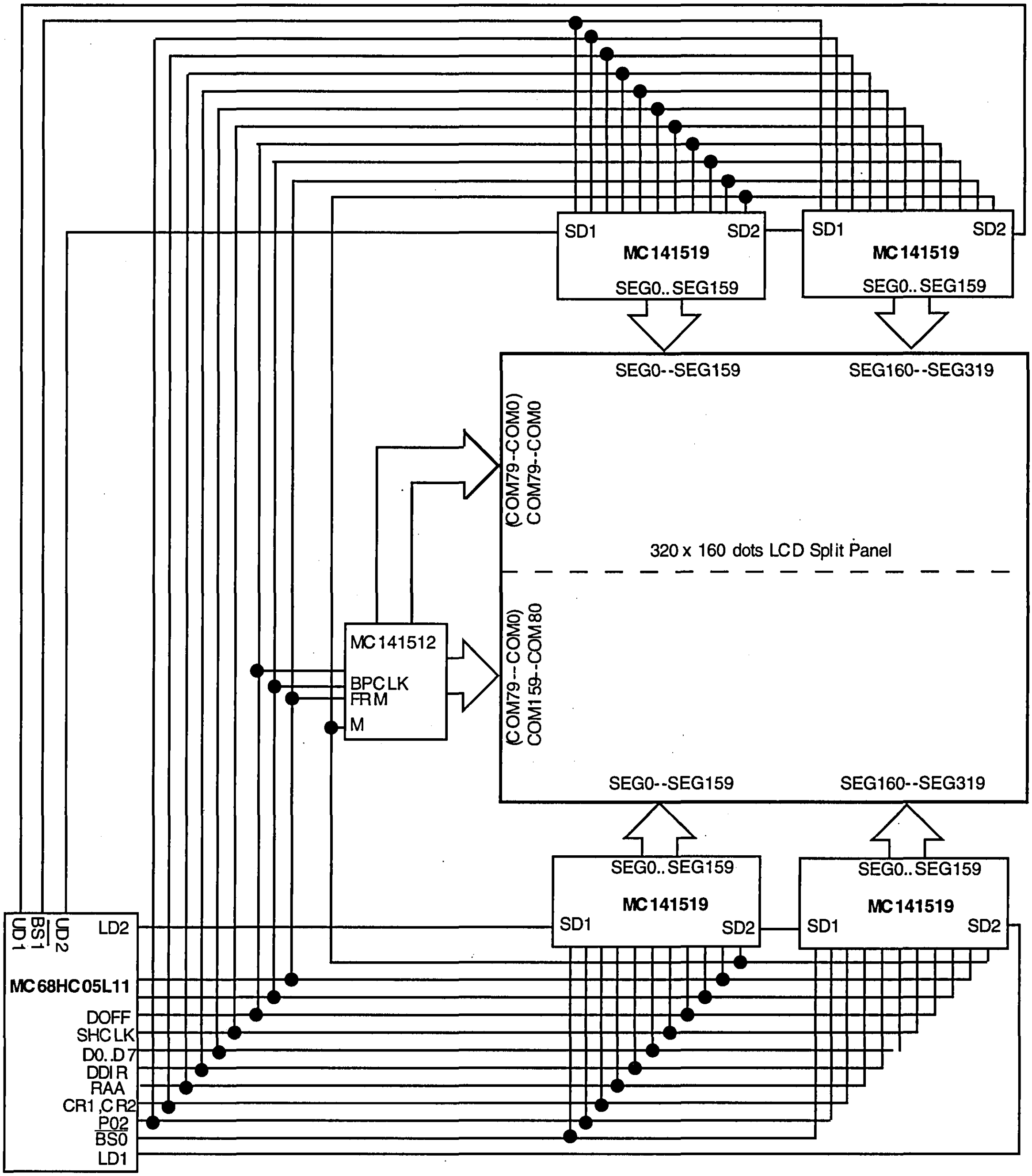
Reference: 98ASL00157A	Issue “0” released on 08/12/94

TYPICAL APPLICATIONS

160 x 80 SINGLE PANEL LCD SYSTEM WITH MC68HC05L11



320 x 160 SPLIT PANEL LCD SYSTEM WITH MC68HC05L11



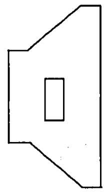
Gate (Row) Driver for TFT Type LCD Panel
CMOS

MC141522

The MC141522 is a high voltage LCD gate driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 120 channels gate drive to provide the row gating function of a TFT (Thin-Film-Transistor) LCD panel.

This chip consists of the low voltage and high voltage part. The low voltage part includes the 122 stages of shift register, level shifter, left/right shift controller. The high voltage part consists of 120 stages level shifters and high voltage output driver buffer with 35 volts output swing capability.

The MC141522 will provide the best performance in combination with the MC141524 (source driver). The two devices can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution by cascading.

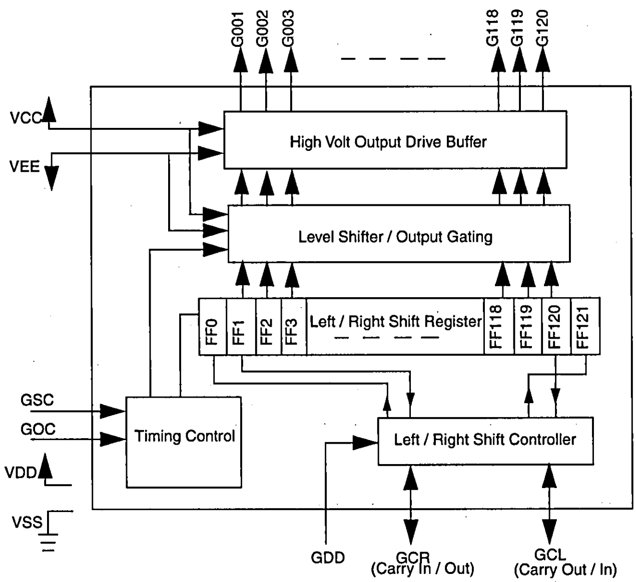


MC141522T1
TAB

ORDERING INFORMATION

MC141522T1 TAB

- Operating Supply Voltage Range
  - Logic (V_{DD} pin): 4.5V to 5.5V
  - Output Drive (V_{CC} - V_{EE}) = 20.0V to 35.0V
- Operating Temperature Range: -30 to 85 °C
- 120 - Row Output Driver
- Split Power Supply
- Output Pulse Width Modulation Control
- Bi-directional Shift Register
- Left / Right Shift Mode Selection
- Maximum Clock Frequency = 100KHz
- Cascadable
- Available in TAB (Tape Automated Bonding), 141 pins



BLOCK DIAGRAM

REV 4
10/96

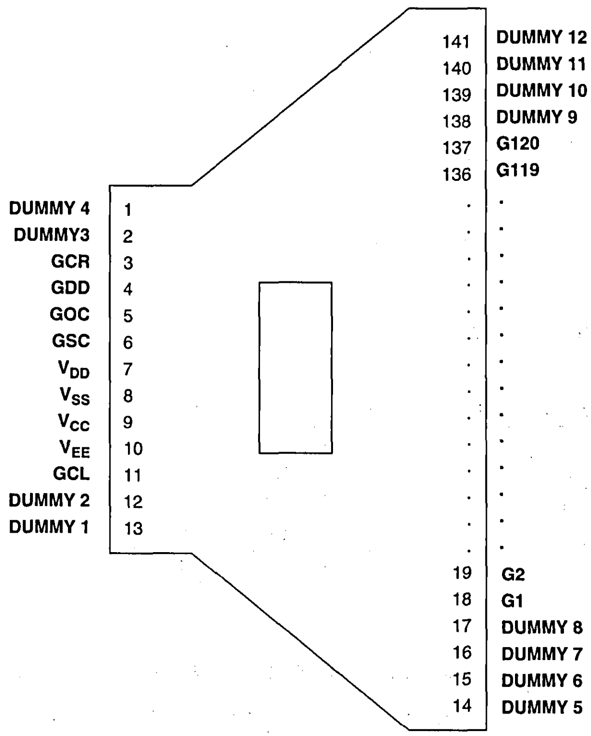


Figure 1A. TAB Package Contact Assignment (Copper View)

ABSOLUTE MAXIMUM RATING (Voltage Referenced to VSS)

Rating	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+7.0 to +17.0	V
Negative Supply Voltage	V_{EE}	-33.0 to - 23.0	V
Logic Supply Voltage	V_{DD}	-0.3 to +6.0	V
DC Supply Voltage	V_{CC} - V_{EE}	+40	V
Logic Input Voltage	V_{in}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Current Drain Per Pin Excluding V_{DD} and V_{SS}	Id	±10	mA
Operating Temp. Range	T_a	-30 to 85	°C
Storage Temp. Range	T_{stg}	-55 to +150	°C

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range VSS < or = (V_{in} or V_{out}) < or = VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either VSS or VDD). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	+5.0	+12.0	+15.0	V
Negative Supply Voltage	V_{EE}	-10.0	-12.0	-30.0	V
Logic Supply Voltage	V_{DD}	+4.5	+5.0	+5.5	V
DC Supply Voltage	V_{CC} - V_{EE}	20	25	35	V
Operating Temperature	T_a	-20	--	+75	°C

AC ELECTRICAL CHARACTERISTICS

V_{DD}=+5.0 V, V_{SS}=0 V, V_{CC}=+15.0 V, V_{EE}=-20 V, T_A=25°C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
High Voltage Driver Output					
Rise Time	tr1	--	--	1.0	us
Fall Time	tf1	--	--	1.0	us
(C_{load}=200pF)					
High Voltage Driver Output					
Rise Time	tr2	--	--	2.5	us
Fall Time	tf2	--	--	2.5	us
(Loading=5KΩ in series with 150pF)					
Propagation Delay Time					
(Carry output from GSC)					
Low to High	tplhc	--	150	250	ns
High to Low	tphlc	--	150	250	ns
Maximum Clock Frequency (GSC)	ø Max	--	15.75	100	KHz

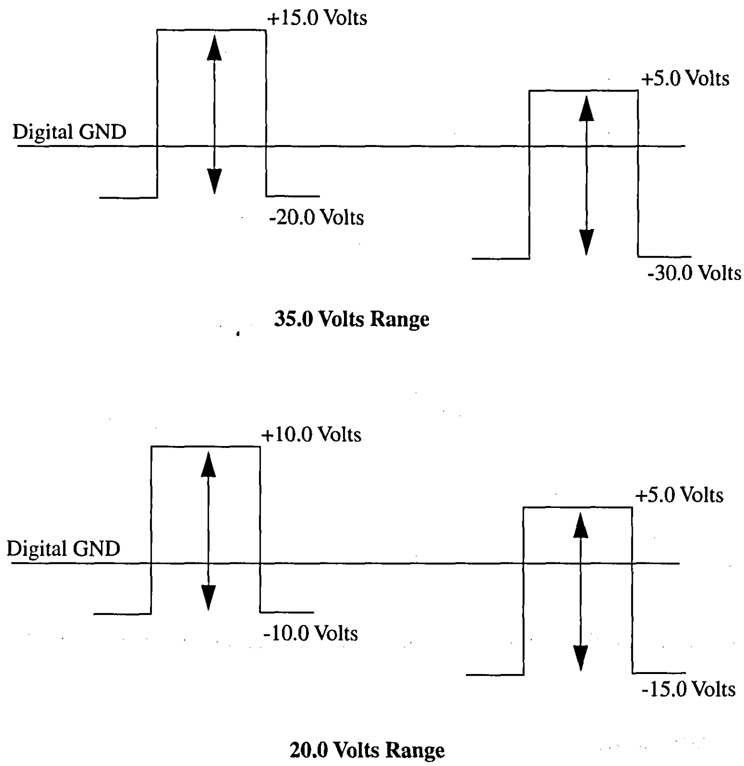


Figure 2. High Voltage Output Buffer Voltage Range

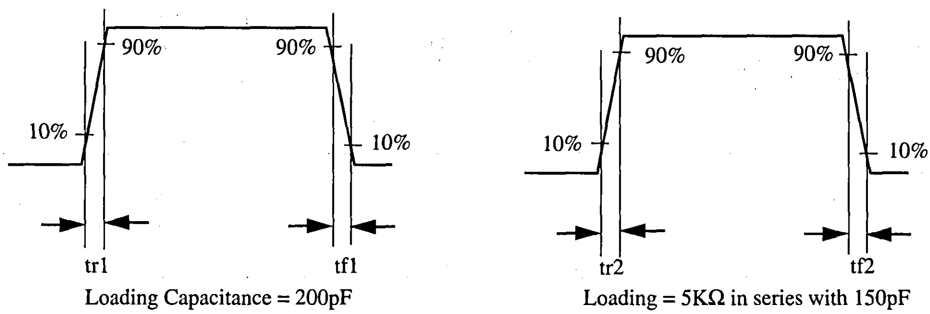


Figure 3. High Voltage Buffer Output Rise and Fall Time

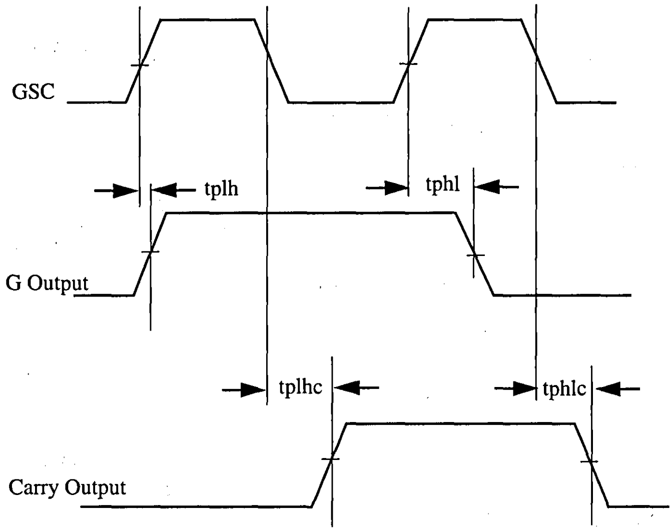


Figure 4. Shift Clock, Gate Driver Output and Carry Output Propagation Delay Timing

DC ELECTRICAL CHARACTERISTICS

V_{DD}=+5.0 V, V_{SS}=0, V_{CC}=+15.0 V, V_{EE}=-20V, T_A =25°C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Control Input Voltage High	V_{IH}	3.2	--	5.5	V
Control Input Voltage Low	V_{IL}	0.0	--	1.2	V
Input Leakage Current					
V_{in} = 0.5V	I_{IL}	-50	--	+50	uA
V_{in} = 3.0V	I_{IH}	-50	--	+50	uA
Driver Output Voltage (G001 - G120)					
High	V_{OH}	Vcc-0.8	--	--	V
Low	V_{OL}	--	--	V_{EE}+0.8	V
Supply Current					
(GSC running at 100kHZ, no loading)	I_{CC}	--	0.5	2.0	mA
	I_{DD}	--	100	200	uA
	I_{EE}	-2.0	0.5	--	mA

PIN DESCRIPTION

V_{SS}
This is the power supply GND connection pin.

V_{DD}
This is the positive 5 V power supply pin for the logic circuitry of the chip.

V_{CC}
This is the power supply pin for the most positive supply voltage.

V_{EE}
This is the power supply pin for the most negative supply voltage.

GSC (Gate Driver Shift Clock)
This input clock signal is to clock the Carry In input ripple through the 122 Stages Shift Register for controlling the Output Scan Gating Sequence.

For normal single scan, the clock frequency is the horizontal frequency of the TV signal. In double scan full resolution mode, the frequency is doubled.

GCL (Gate Driver Carry-Left) / GCR (Carry-Right)
These two input / output pins perform the same function and depends on the GDD (Shift Direction Determination) Operation. In Shift Right mode, the GCL is the Carry input while the GCR is the Carry output for cascading. In shift Left mode, the pin functions and operations are vice versa. See Table 1.

GDD	Shift Direction		GCL	GCR
"0"	G001 to G120	Shift Right Mode	Input	Output
"1"	G120 to G001	Shift Left Mode	Output	Input

Table 1.Carry Shift Direction

GDD (Gate Driver Shift Direction Determination)
This input pin provides the selection of the shift left and right mode of operation.

GDD = "0", the system shift register will shift right.

GDD = "1", the system shift register will shift left.

See Table 1.

GOC (Gate Driver Output Control)
This input pin provides control to the output buffer output pulse width in order to provide the effective gating timing of the TFT.

G001 to G120
These 120 output pins are high voltage buffer for driving the gate of the TFT active matrix LCD panel.

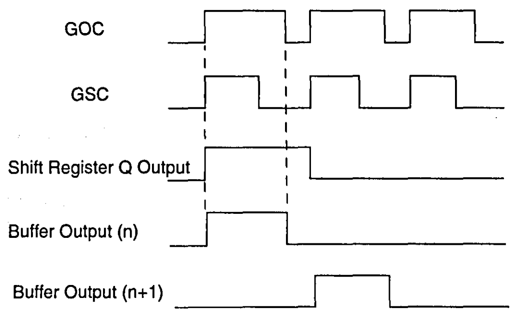


Figure 5. Gate Output Control to Control the Gating Pulse Width

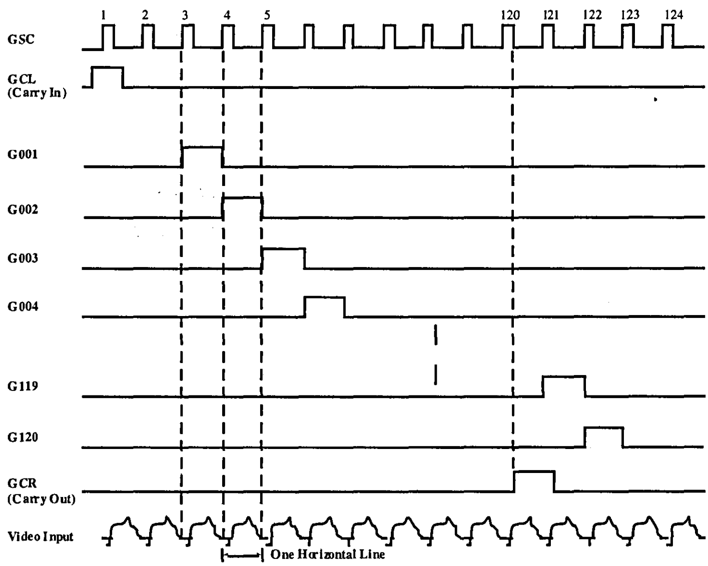
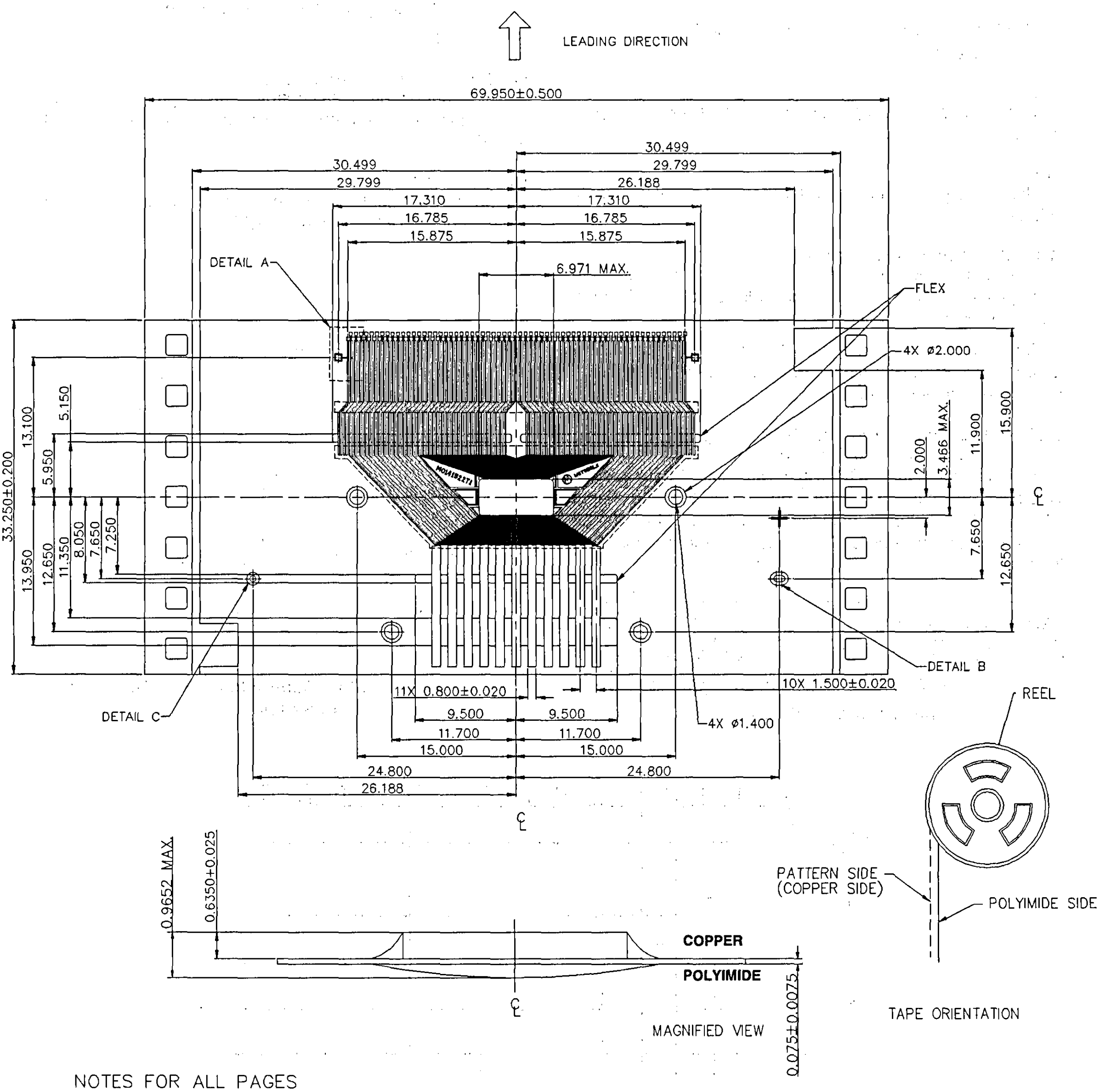


Figure 6. Row Driver Timing Diagram (Shift Right Mode)

MC141522T1

TAB PACKAGE DIMEMSION

(DO NOT SCALE THIS DRAWING)



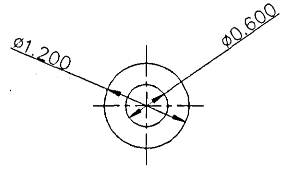
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. 7 SPROCKET HOLES DEVICE
7. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.

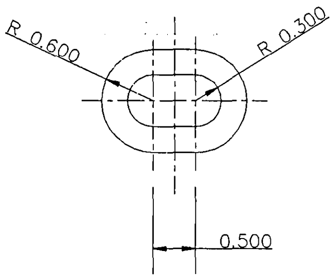
MC141522T1

TAB PACKAGE DIMEMSION

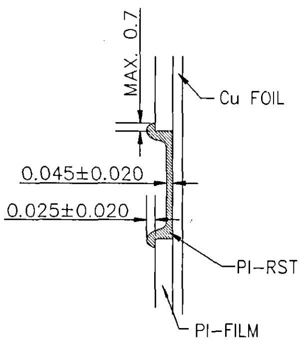
(DO NOT SCALE THIS DRAWING)



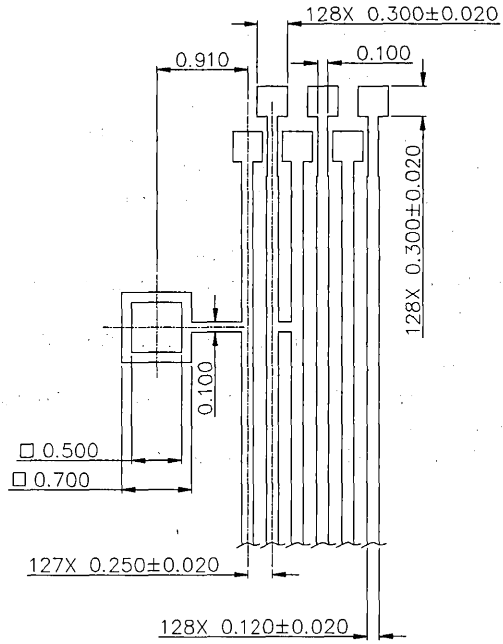
DETAIL C



DETAIL B



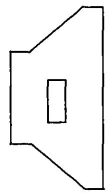
FLEX MATERIAL DETAIL



DETAIL A

Source (Column) Driver for TFT Type LCD Panel
CMOS

MC141524



ORDERING INFORMATION

MC141524T1 TAB

The MC141524 is a high voltage LCD source driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 120 channels source drive to provide the drain bus signal of a TFT (Thin-Film-Transistor) LCD panel.

This chip accepts the three video signals R, G, B. The built-in sample and hold circuitry will sample the video signals and hold these signals before outputting to drive the TFT-LCD panel.

The MC141524 will provide the best performance in combination with the MC141522 (gate driver). The two devices can drive LCD panels from 480 x 240 pixels middle-resolution up to 720 x 480 pixels high-resolution by cascading.

- Operating Supply Voltage Range
  - Logic (V_{DD} pin): 4.5V to 5.5V
  - (V_{EE} pin): -5V to -10V
  - Output Drive (V_{DD} - V_{EE}) = 10V to 15V
- Dynamic Range: 11.0 Volts Peak to Peak
- Operating Temperature Range: -30 to 85 °C
- 120 - Column Output Driver
- 2 Sample & Hold Cells Structure
- Bi-directional Shift Register with Interchanging Carry-Borrow Terminals
- Left / Right Shift Mode Selection
- Maximum Sampling Frequency = 30MHz (Three Phase (3ø)'s Operation)
- Video Bandwidth (-3dB): 5.0MHz
- Programmable Buffer Output Drive with External Resistor
- Cascadable
- Available in TAB (Tape Automated Bonding), 152 pins

REV 4
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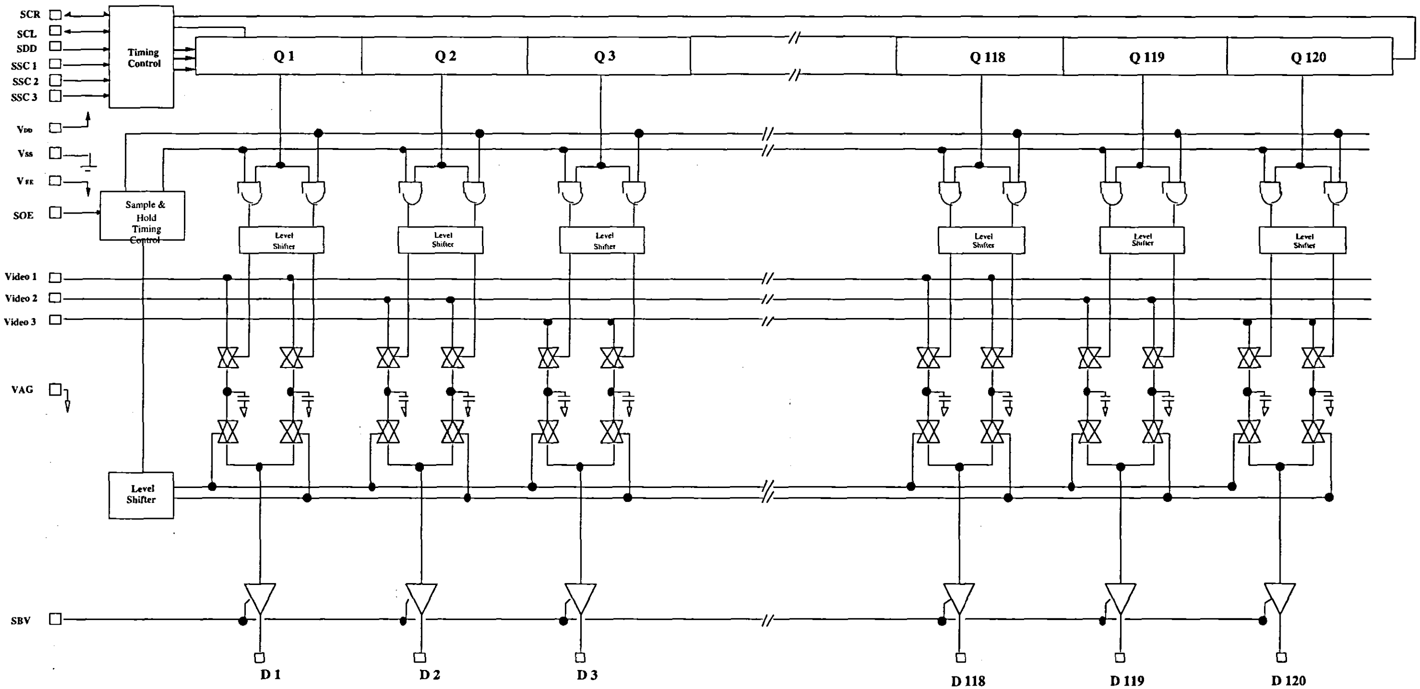
BLOCK DIAGRAM



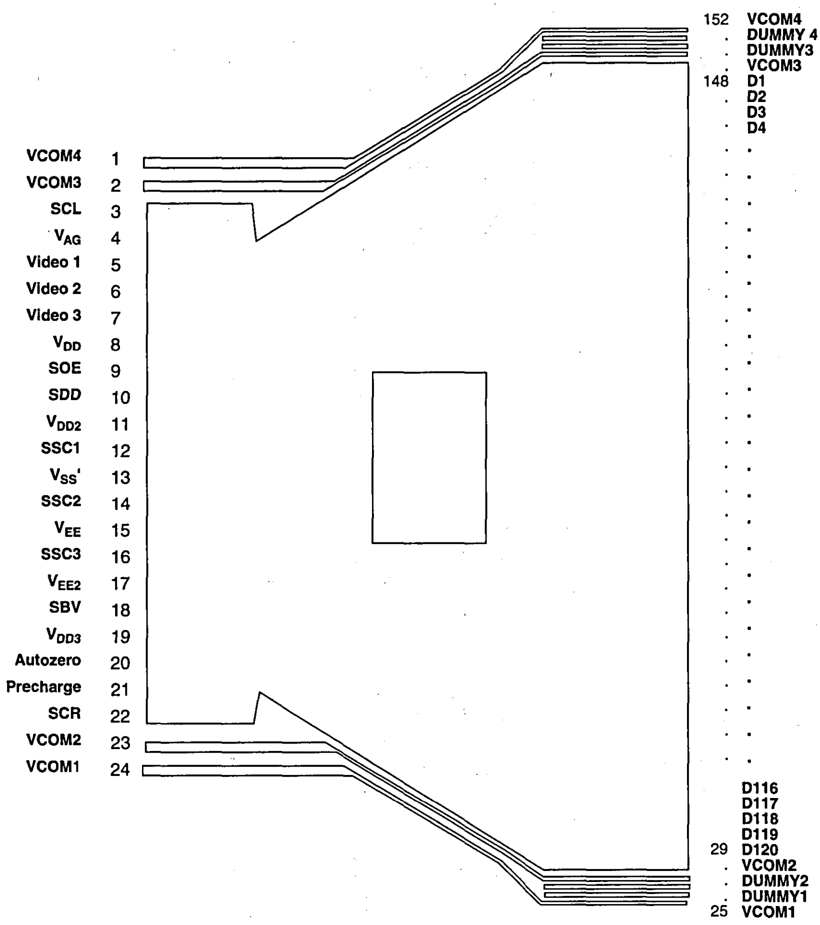


Figure 1A. TAB Package Contact Assignment (Copper View)

ABSOLUTE MAXIMUM RATING (Voltage Referenced to VSS)

RATING	SYMBOL	VALUE	UNIT
Logic Supply Voltage	V_{DD}	+6.0	V
Negative Supply Voltage	V_{EE}	-16.0	V
DC Supply Voltage	V_{DD} - V_{EE}	+22	V
Input Voltage All Digital Input	V_{di}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Input Voltage Analog Video Input	V_{ai}	V_{SS} - 0.5 to V_{DD} + 0.5	V
Operating Temp. Range	T_a	-30 to 85	°C
Storage Temp. Range	T_{stg}	-55 to +150	°C

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that Vin and Vout be constrained to the range VSS < or = (Vin or Vout) < or = VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g. either VSS or VDD). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Logic Supply Voltage	V_{DD}	+4.5	+5	+5.5	V
Negative Supply Voltage	V_{EE}	-5	-8	-10	V
DC Supply Voltage	V_{DD} - V_{EE}	10	--	15	V
Operating Temperature	T_a	-20	--	+75	°C

AC ELECTRICAL CHARACTERISTICS

V_{DD}=5.0 V, V_{SS}= 0V,V_{EE}=-10 V, T_A=25°C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Control Input Rise Time Fall Time (SOE, SCR, SCL, SSC1,2,3)	 t_{TLH} t_{THL}	 -- --	 10 10	 20 20	 ns ns
Shift Clock (SSC) to sampling activated Shift Register Output HIGH Shift Register Output LOW	 t_{PLHR} t_{PLHR}	 -- --	 5 5	 10 10	 ns ns
Carry In to Shift Clock (SSC1) Set Up Time	t_{SUC}	--	20	--	ns
Carry In Pulse Width (SCR/SCL)	t_{WC}	80% of $t_{sø}$	--	--	ns
Shift Clock Cycle (SSC1,2,3)	$t_{sø}$	100	--	1000	ns
Shift Clock Pulse Width HIGH Shift Clock Pulse Width LOW (SSC1,2,3)	t_{SCH} t_{SCL}	40% of $t_{sø}$ 40% of $t_{sø}$	-- --	-- --	ns ns
Shift Clock n to Shift Clock n+1 Phase Delay	t_{SCT}	30	--	--	ns
Propagation Delay Time Low to High Carry Output from SSC High to Low Carry Output from SSC C_L = 100pF	 t_{PLHC} t_{PLHC}	 -- --	 10 10	 30 30	 ns ns

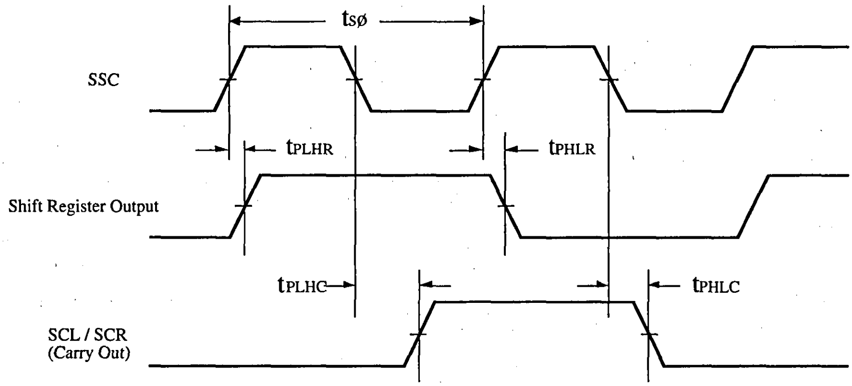


Figure 1. Shift Clock, SR Output and Carry Out Propagation Delay Timing Diagram

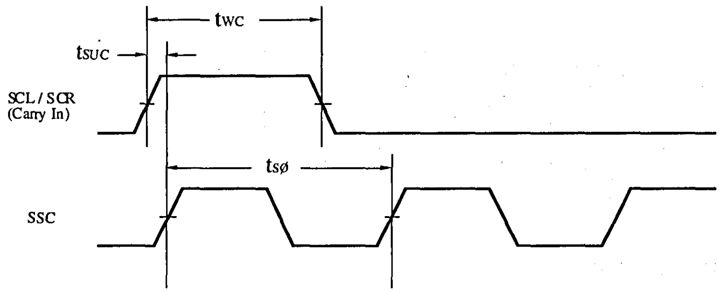


Figure 2. Shift Clock and Carry In Propagation Delay Timing Diagram

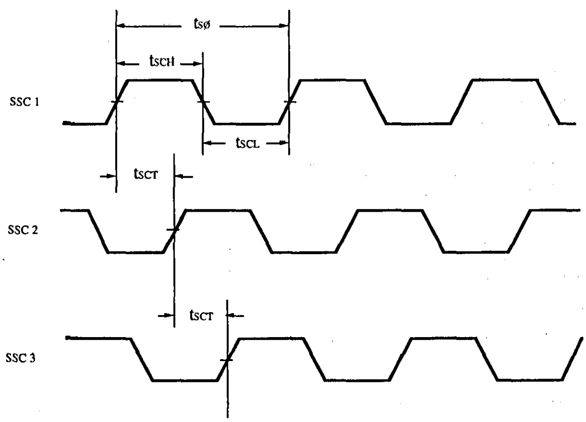


Figure 3. Three Phase Shift Clock Phase Shift Delay Timing Diagram

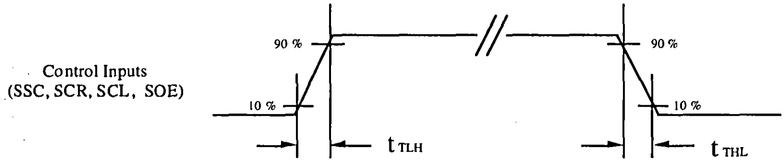


Figure 4. Control Input Rise and Fall Time

DC ELECTRICAL CHARACTERISTICS

V_{DD}=5.0 V, V_{SS}= 0V,V_{EE}=-10 V, T_A=25°C, Voltage referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Unit
Control Input Voltage Level High	V_{IH}	3.2	--	5.5	V
Control Input Voltage Level Low	V_{IL}	0.0	--	1.2	V
SDD Input Voltage High	V_{IHS}	--	--	V_{DD}	V
SDD Input Voltage Low	V_{ILS}	V_{SS}	--	--	V
D_O Output Current High (V_O = V_{DD}-3.0V) Low (V_O = V_{EE}+2.0V)	 I_{OHX} I_{OLX}	 -- 800	 -- --	 800 --	 uA uA
Bias Voltage Resistance Iag=15uA	R_{Ib}	6	7.2	12	KΩ
Input Voltage Range	V_{SG}	V_{EE}+2.0	--	V_{DD}-2.0	V
Input Video Signal Dynamic Range		--	10	11	V_{pp}
Maximum Clock Input Frequency (CLK)	$Ø_{MAX}$	1.0	--	10.0	MHz
Current Consumption Shift Register constantly shifting one V_{DD}=5V, V_{EE}=-10V, Video1,2,3=-8V	I_C	--	10	30	mA
Sample & Hold Cell Gain	$G_{s/h}$	0.95	0.96	1.00	
Driver Output High (Video input = 3V) Driver Output Low (Video input = -8V)	V_{DOH} V_{DOL}	2.8 -8	-- --	3 -7.8	V V

PIN DESCRIPTION

V_{SS}

This is the power supply GND connection pin for the logic circuitry of the chip.

V_{AG}

This is the power supply GND connection pin for the analog circuitry of the chip. Normally it is set to middle between V_{DD} and V_{EE} level.

V_{DD}

This is the positive 5 V power supply pin for both the logic and the analog circuitry of the chip.

V_{EE}

This is the power supply pin for the most negative supply voltage for the analog circuitry of the chip.

Precharge

This logic input pin provides the output reset function. When precharge is held low, all driver o/p will go to the analog group level "VGA". When precharge is set high, all driver o/p is connected to the sample & hold cell (i.e. normal signal output).

Autozero

This is a logic input pin to reset output unity gain buffer before next signal is generated. Normally, it is connected together with precharge pin. User can ignore the Autozero and / or precharge function by tying it to high.

SBV (Source Bias Voltage)

This is the bias voltage supply pin for the unity gain output analog buffer. This bias voltage can control the buffer current driving capability.

The bias voltage is controlled by an external resistor connected between SBV and VEE. The lower resistance will produce higher current driving capability.

SSC1, SSC2, SSC3 (Source Driver Shift Clock 1,2,3)

This input clock signal is divided in Three Phase Operation (3ø) each with frequency of 10.0MHz maximum. Each phase controls the sampling timing of one video line signal. The equivalent operating frequency is 30.0MHz maximum.

Each clock signal will latch the carry signal through the Bi-directional Shift Register to determine the video signal sampling timing for the sample & hold cells.

SCL (Source Driver Carry-Left) / SCR (Carry-Right)

These two input / output pins perform the same function and depends on the SDD (Shift Direction Determination) Operation. In Shift Right mode, the SCL is the Carry input while the SCR is the Carry output for cascading. In shift Left mode, the pin functions and operations are vice versa. See Table 1.

SDD	Shift Direction		SCL	SCR
"0"	D1 to D120	Shift Right Mode	Input	Output
"1"	D120 to D1	Shift Left Mode	Output	Input

Table 1.Carry Shift Direction

SDD (Source Driver Shift Direction Determination)

This input pin determines the shift left / right operation of the Bi-directional Shift Register.

SDD = "0", the system shift register will shift right.

SDD = "1", the system shift register will shift left.

See Table 1.

SOE (Source Driver Output Enable)

This input pin determines the sample and hold output sequence of the unity cell (See Figure 9). It governs the sample and hold alternate timing operation between lines.

D001 to D120

These 120 output pins are sample and hold buffer outputs. These buffers output the sampled video signal and drive the source of the TFT of an active matrix LCD panel.

Bi-directional Shift Register

The 120-stage Bi-directional Shift Register controls the 120 corresponding sample and hold operation of the unity cell connected to each of the LCD driving output buffer. When the shift register bit content is "1", the sample and hold circuit is in sampling state. The shift register is activated by shifting a "1" (Carry In) into the 1st stage of the shift register and the "1" value will latch through the register in turn performs the sample function of the unity cell.

The shift register is driven by a three phase clock. The maximum frequency of each phase clock is 10.0MHz and therefore the minimum sampling window is 100ns. The equivalent sampling rate of the source (common) driver is 30.0MHz. See figure 6, 7, 8, 9.

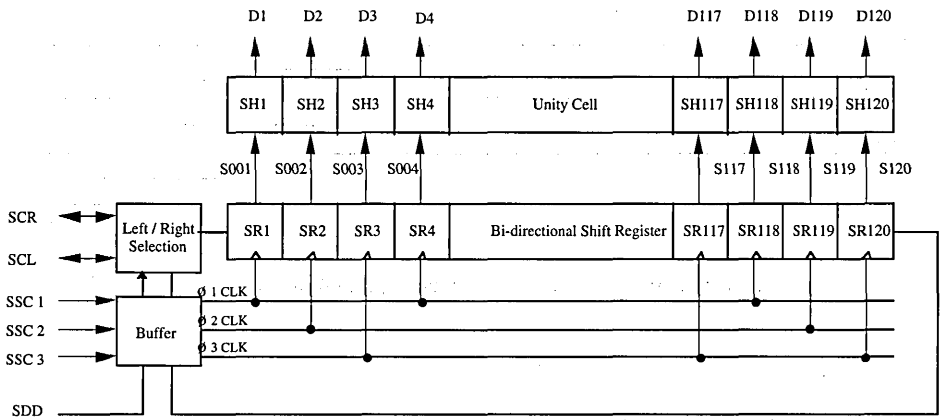


Figure 6. Bi-directional Shift Register Block Diagram

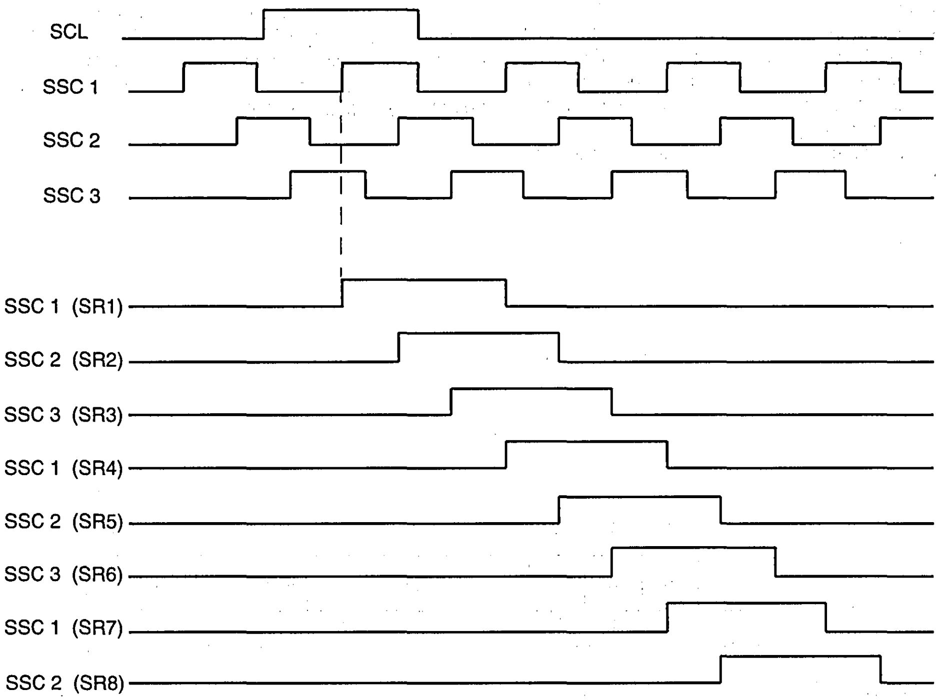


Figure 7. Shift Register Timing Diagram (Shift Right Mode)

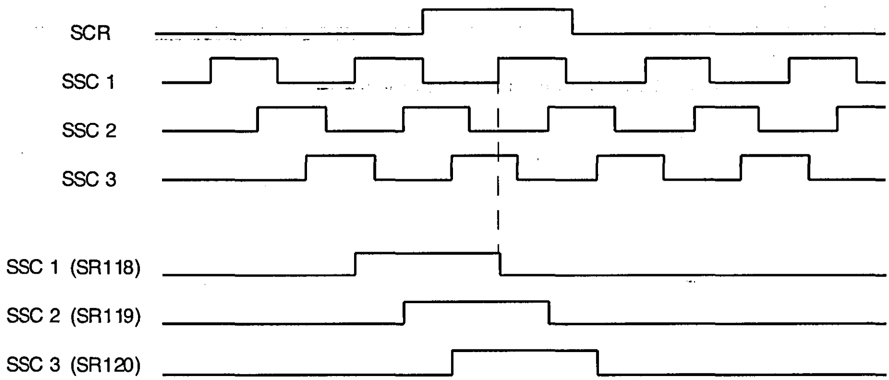


Figure 8. Carry Output Timing Diagram (Shift Right Mode)

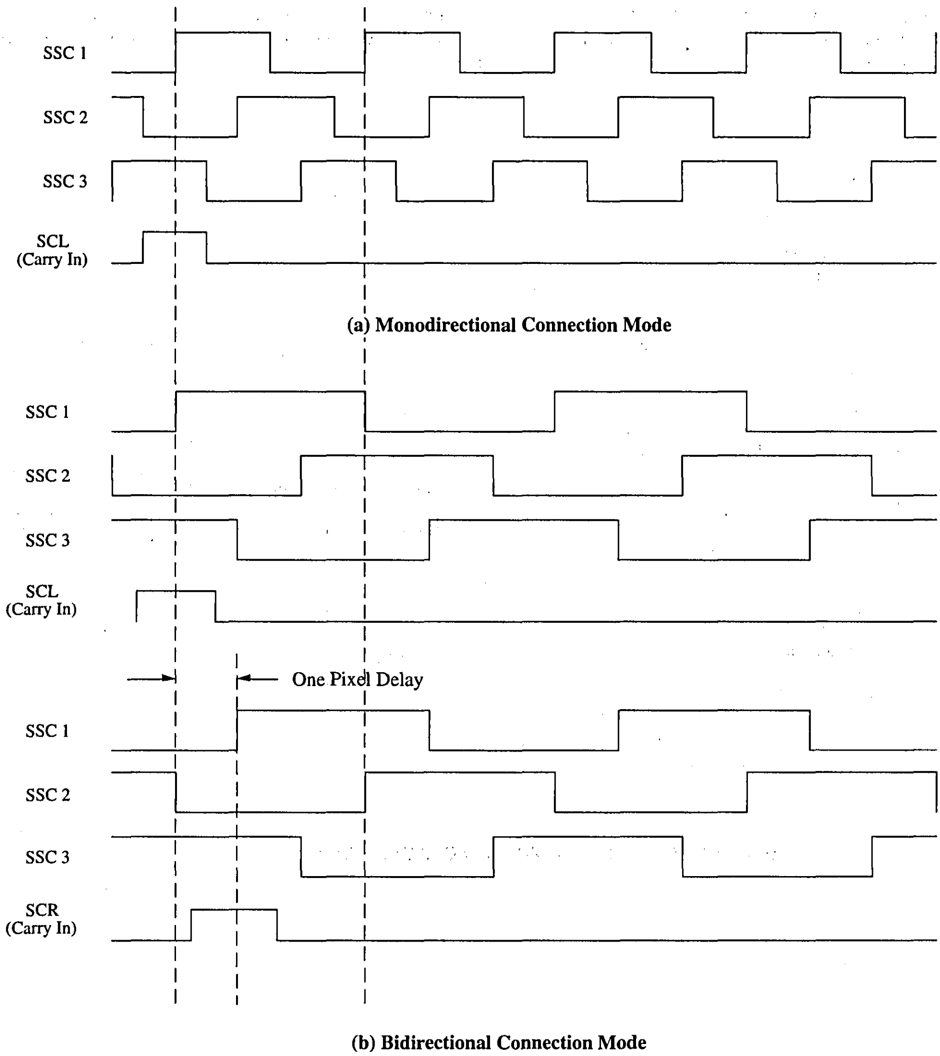


Figure 9. Three Phase Shift Clock Arrangement

SECTION 2

Unity Cell

The unity cell consists of 2 sample and hold circuitry and a unity gain buffer output. The 2 sample and hold cells are arranged in complementary fashion such that one cell is in sampling action while another cell is holding the charge that was sampled previously. The selected sample and hold circuit samples the video signal of one horizontal scan line and read out in the next horizontal line scanning period; while the other selected sample and hold cell samples the video signal of that next scan line. See figure 10, 11, 12, 13.

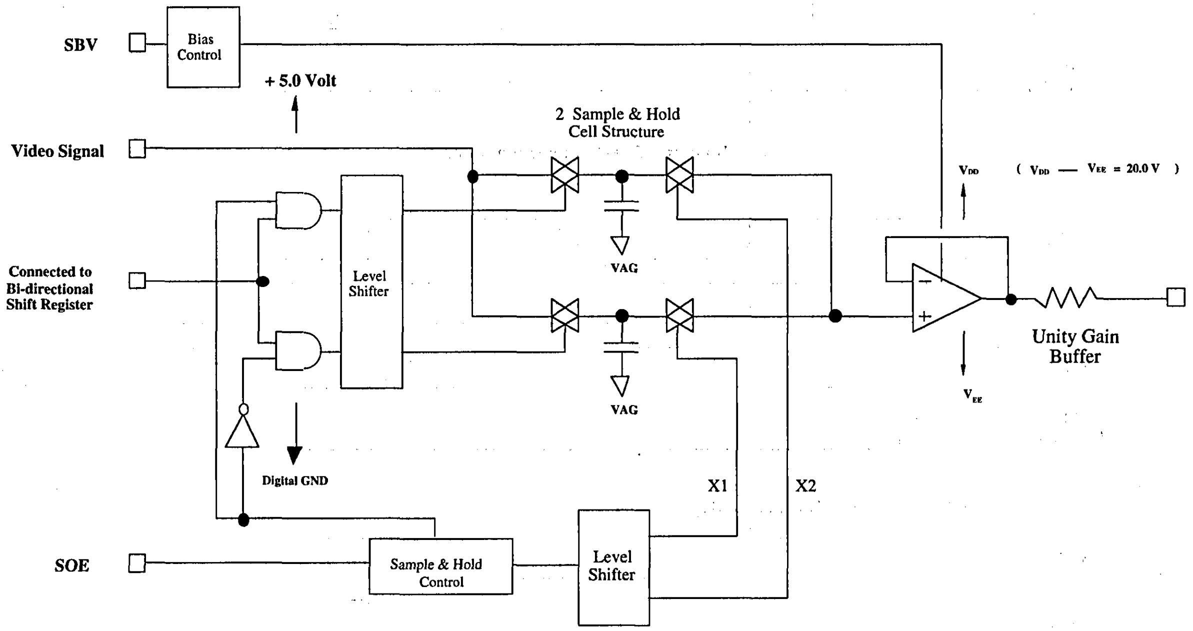


Figure 10. Sample and Hold Unity Cell Block Diagram

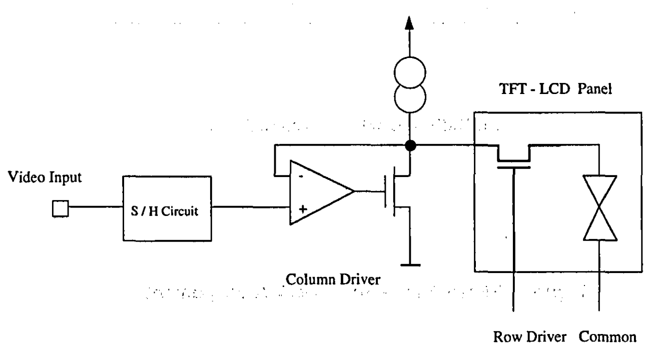


Figure 11. Sample and Hold Schematic

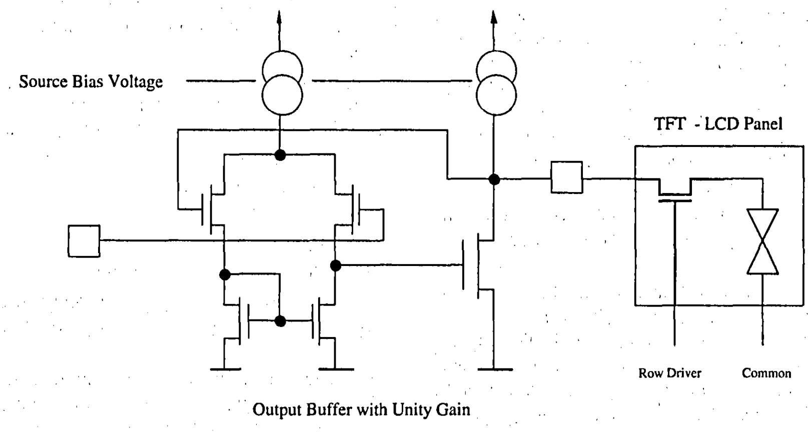


Figure 12. Unity Gain Buffer Schematic

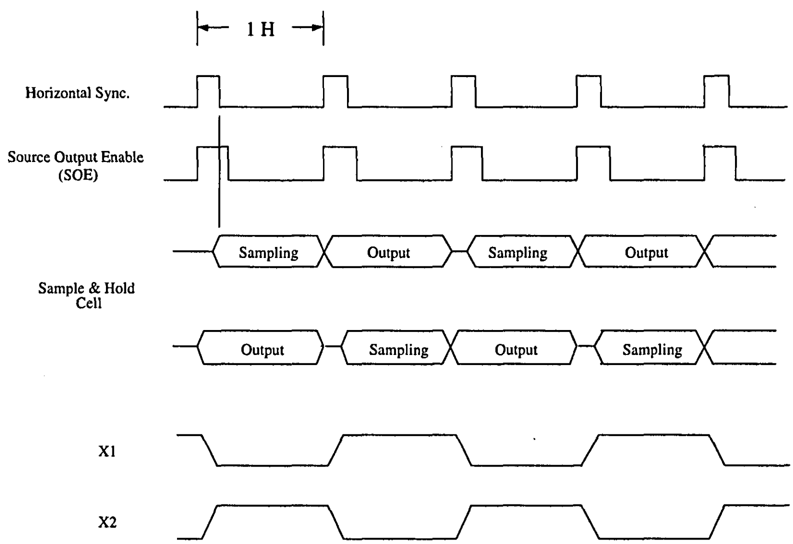


Figure 13. Sample and Hold Timing Diagram

SECTION 3

System Timing

In NTSC TV standard, the vertical synchronization signal period is 16.7ms while the horizontal synchronization signal period is 63.5us. There is about 10us horizontal retrace period in one line of video signal. The effective display period contributes 95% of the rest of valid display period. Therefore, the effective display period for single video line is about 50us. There is an half horizontal period shift between the odd field and even field, the effective display line video signal starts at the 19.0th lines scan after the vertical synchronization signal. The effective display line number for one field is 240 lines for single scan and 480 lines for double scan.

The Output Enable (SOE) control signal governs the sample and hold alternate timing operation between lines.

The driver controller has a VCO running at the required sampling rate to supply the system clock for the controller. The sampling clock is phase locked to the horizontal synchronization cooperated with the vertical synchronization signal. Odd field start and even field start signal are generated inside the controller to provide a timing signal for odd and even field start signal (Carry In). Once the start signal is generated, the column (source) driver starts sampling the video line signal while the row (gate) driver will output the latch signal one line after the start pulse to change the sampled video signal to the LCD panel through the TFT switches on the active matrix panel.

There are 240 row driver outputs for single scan and 480 row driver outputs for double scan "High resolution" panel. However, the sampling frequency of the source (column) driver will be defined by the number of horizontal pixels of the panel.

For example, if the number of horizontal pixel is 720, then the sampling frequency (fs) of the column driver will be defined by the following equation: (singe scan mode)

fs (signal scan)

= (1/effective display period)* (no. of display pixels)

= 720 / (63us*0.95)

= 14.4MHz

= 4.8MHz (using 3 phase clock)

The sampling frequency can be reduced by half if the column driver are placed in the bi-directional connection mode. See figure 6 and figure 12.

However, in the bi-directional connection mode, the controller has to provide a set of upper driver clock signal and lower driver clock signal. The phase shift between the upper and lower driver clock signal must be one pixel delay.

See Figure 14, 15.

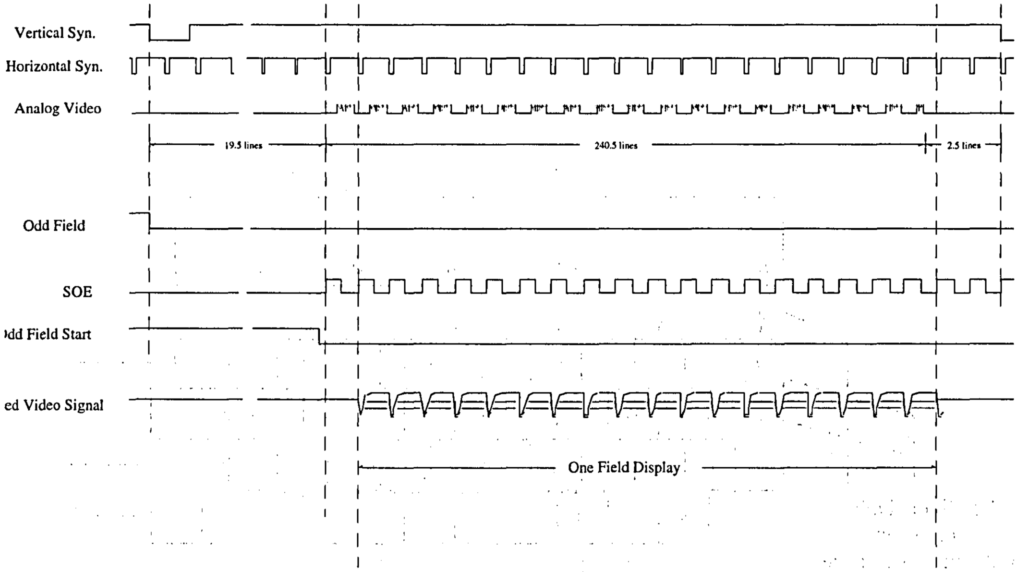


Figure 14. LCD-TV: Odd Field System Timing

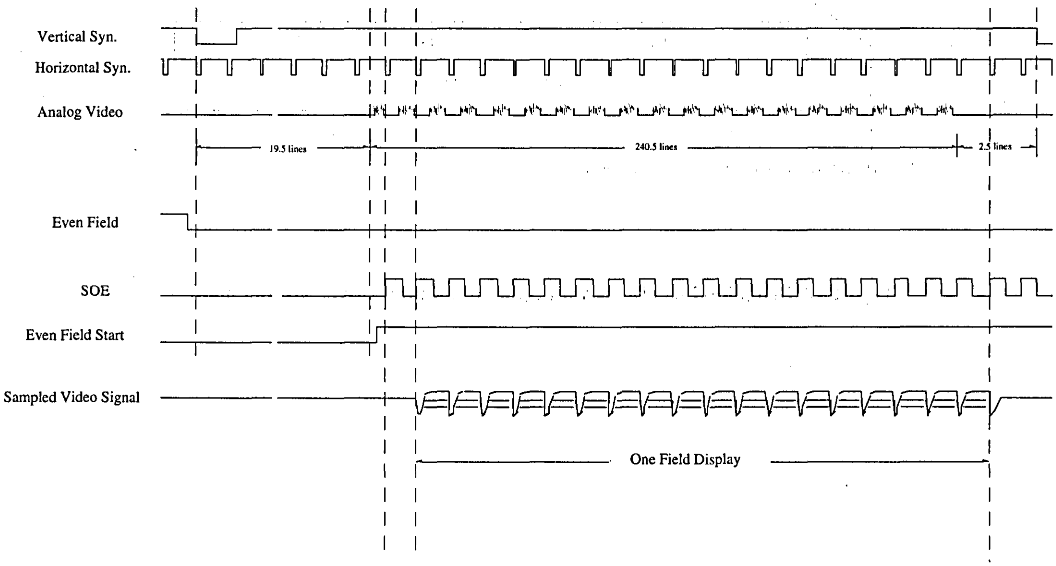


Figure 15. LCD-TV: Even Field System Timing

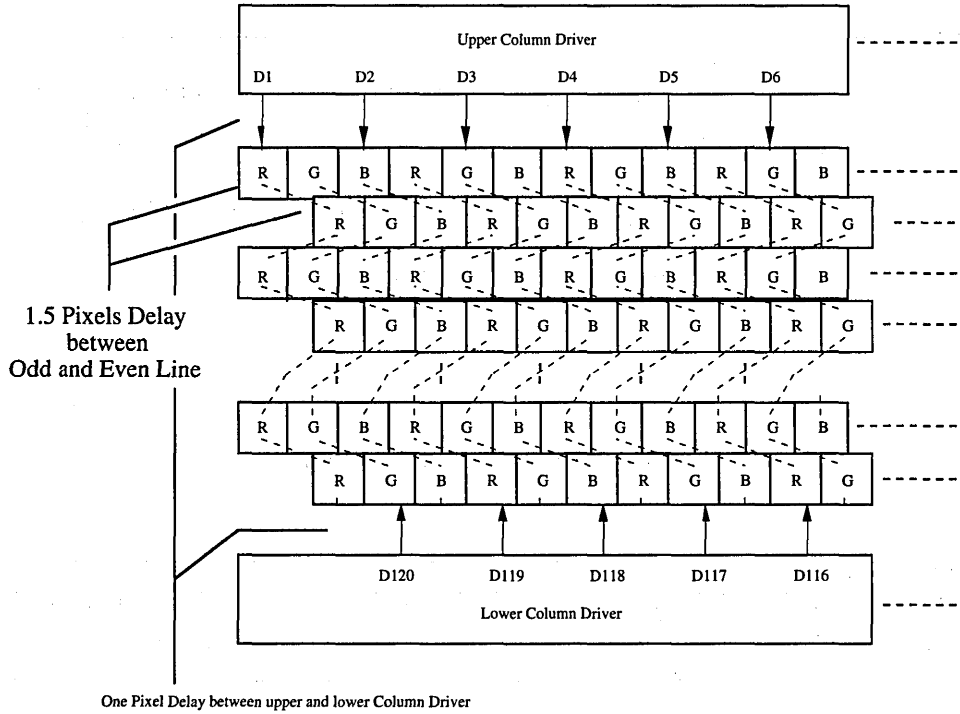


Figure 16. Sampling Pixel Delay with Upper and Lower Driver Arrangement

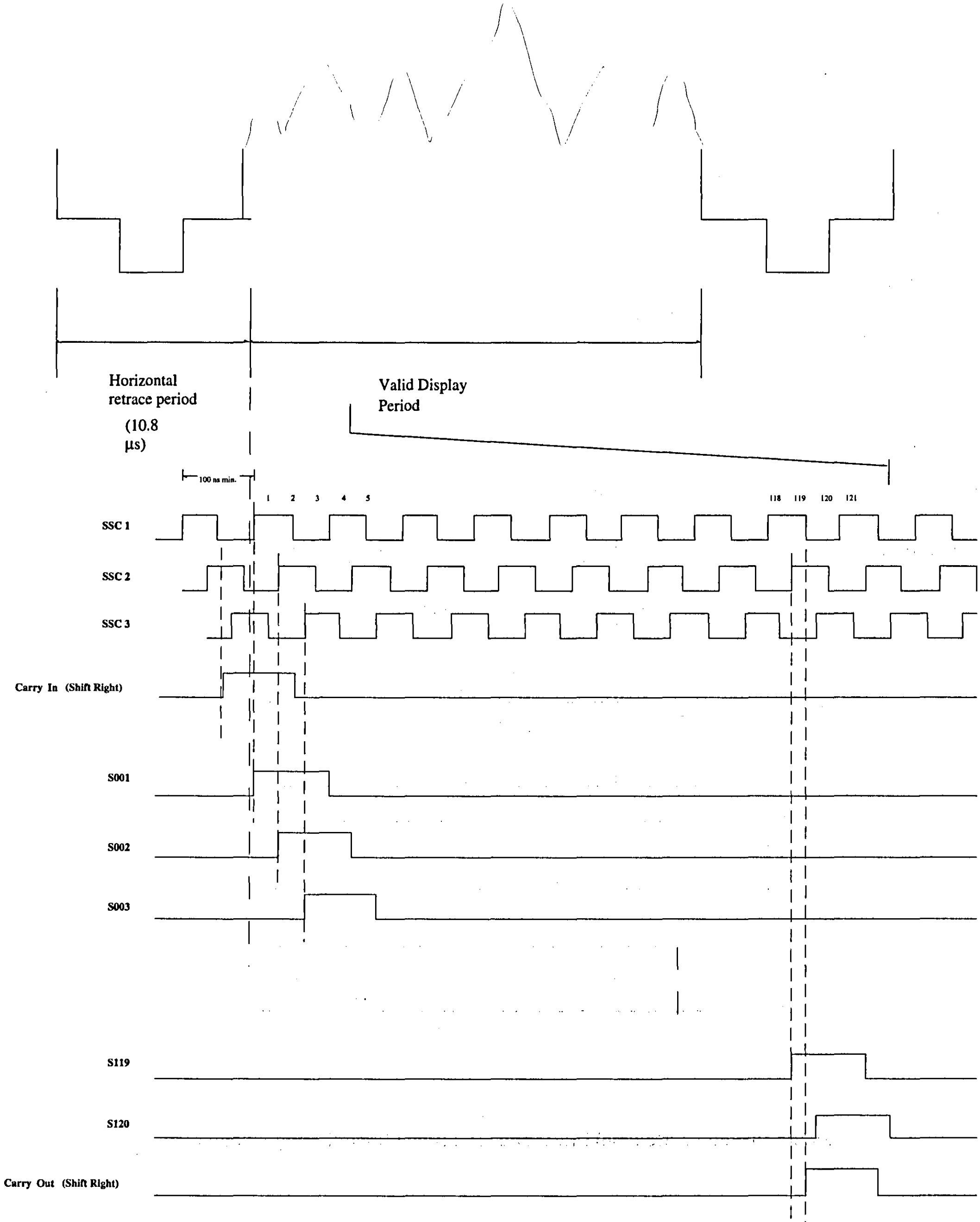


Figure 17. Source (Column) Driver Sampling of Video Line System Timing Diagram

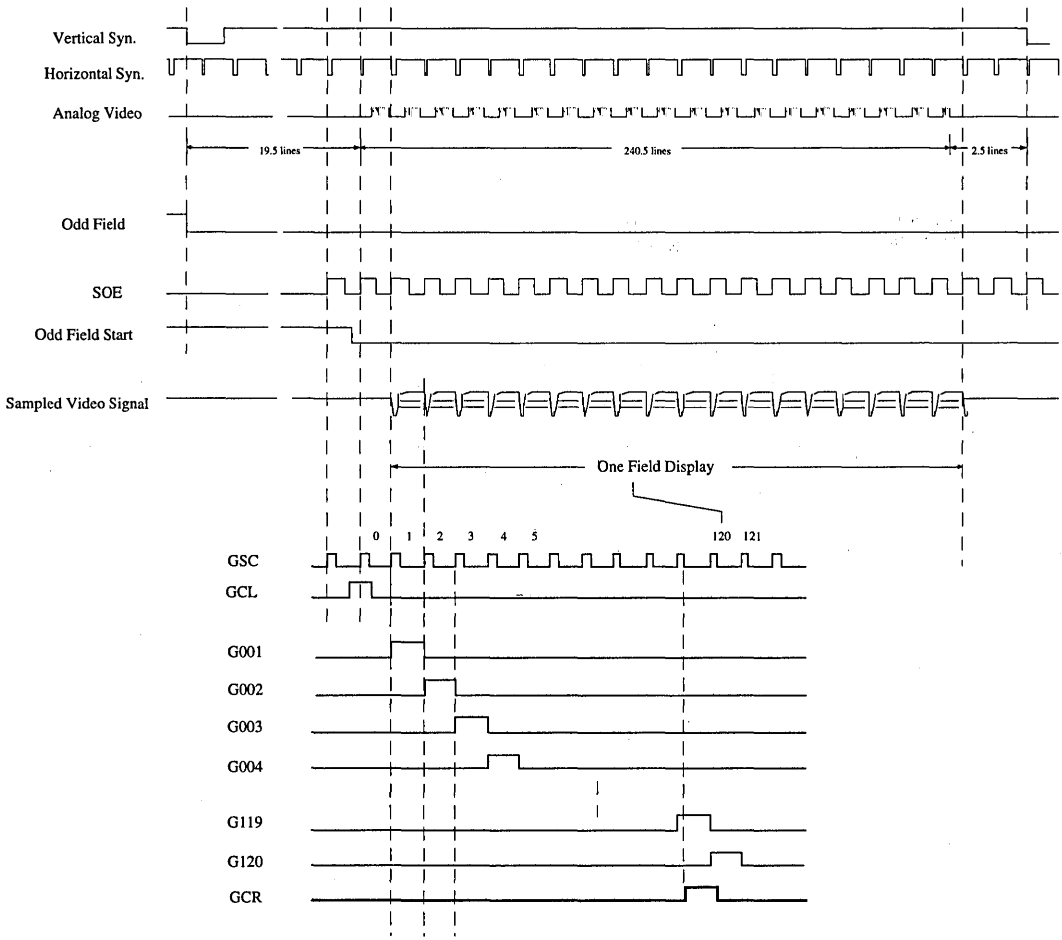
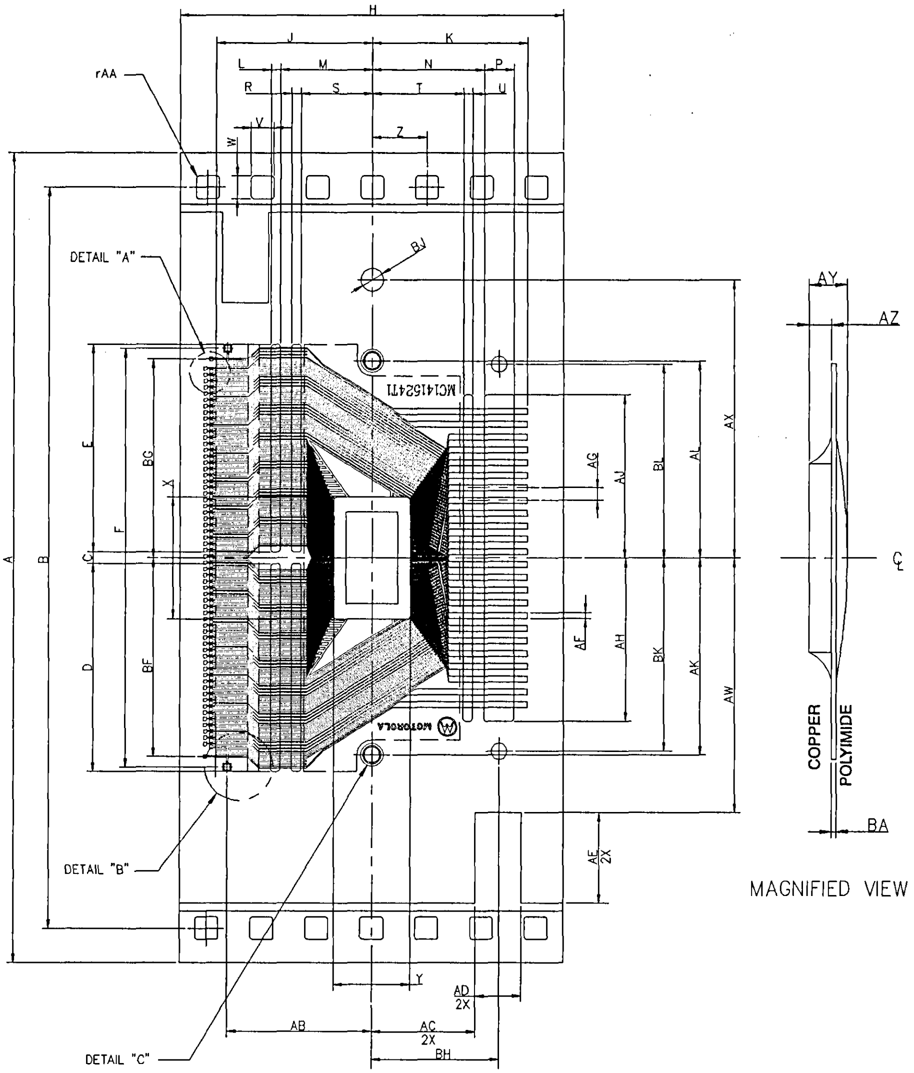


Figure 18. Source (Column) Driver and Gate (Row) Driver Timing Relation

MC141524T1

TAB PACKAGE DIMENSION

(DO NOT SCALE THIS DRAWING)

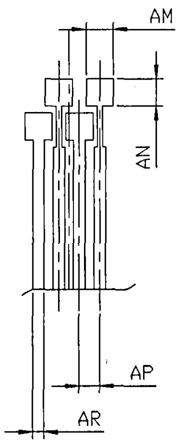


Reference: 98ASL00211A	Issue "0" released on 03/20/96

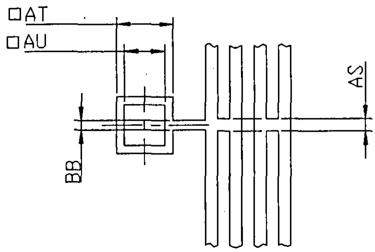
MC141524T1

TAB PACKAGE DIMENSION

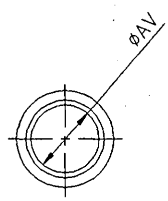
(DO NOT SCALE THIS DRAWING)



DETAIL "A"



DETAIL "B"



DETAIL "C"

Reference: 98ASL00211A	Issue "0" released on 03/20/96

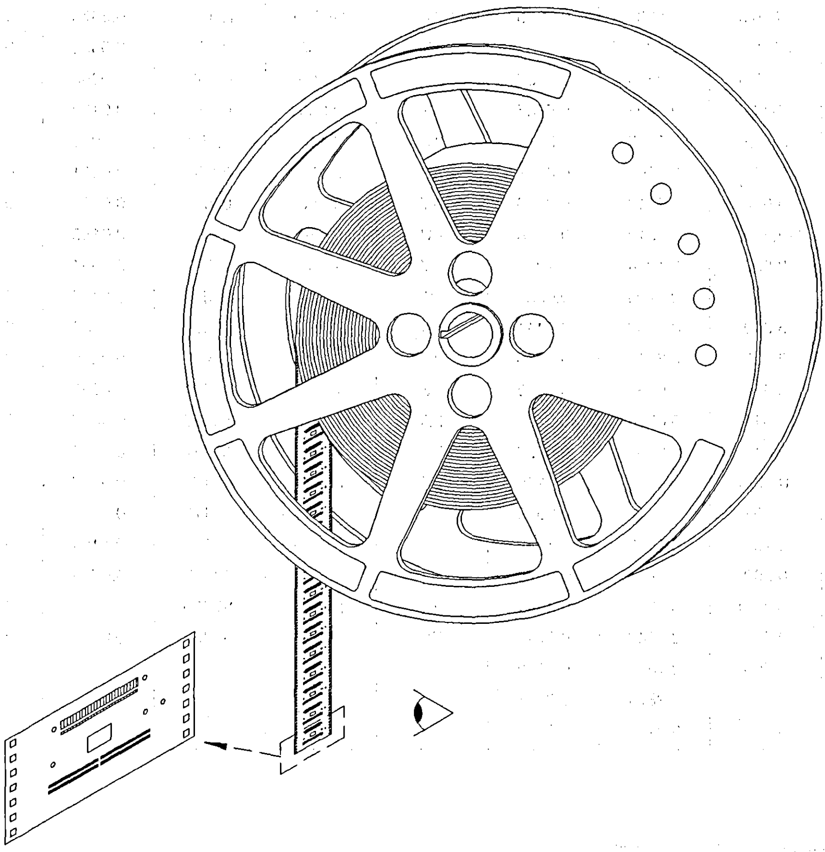
TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	69.750	70.150	2.7461	2.7618	AG	1.090	1.110	0.0429	0.0437
B	63.869	64.029	2.5145	2.5208	AH	14.050	14.115	0.5531	0.5571
C	0.950	1.050	0.0374	0.0413	AJ	14.050	14.115	0.5531	0.5571
D	17.870	17.970	0.7035	0.7075	AK	16.950	17.050	0.6673	0.6713
E	17.870	17.970	0.7035	0.7075	AL	16.950	17.050	0.6673	0.6713
F	36.068	36.212	1.4200	1.4257	AM	0.250	0.350	0.0098	0.0138
H	32.750	33.750	1.2894	1.3287	AN	0.250	0.350	0.0098	0.0138
J	13.450	13.550	0.5295	0.5335	AP	0.260	0.280	0.0102	0.0110
K	13.450	13.550	0.5295	0.5335	AR	0.110	0.150	0.0043	0.0059
L	0.750	0.850	0.0295	0.0335	AS	0.130	0.170	0.0051	0.0067
M	7.900	8.000	0.3110	0.3150	AT	0.680	0.720	0.0268	0.0283
N	9.700	9.800	0.3819	0.3858	AU	0.480	0.520	0.0189	0.0205
P	2.550	2.650	0.1004	0.1043	AV	1.350	1.450	0.0531	0.0571
R	0.750	0.850	0.0295	0.0335	AW	21.500	22.500	0.8465	0.8858
S	6.100	6.200	0.2402	0.2441	AX	23.500	24.500	0.9252	0.9646
T	7.900	8.000	0.3110	0.3150	AY	0.686	0.838	0.0270	0.0330
U	0.750	0.850	0.0295	0.0335	AZ	0.5794	0.6294	0.0228	0.0248
V	1.951	2.011	0.0768	0.0792	BA	0.0675	0.0825	0.0027	0.0032
W	1.951	2.011	0.0768	0.0792	BB	0.080	0.120	0.0031	0.0047
X	-	10.490	-	0.4130	BF	17.111	17.179	0.6737	0.6764
Y	-	6.651	-	0.2619	BG	17.111	17.179	0.6737	0.6764
Z	4.720	4.780	0.1858	0.1882	BH	10.550	11.550	0.4154	0.4547
AA	-	0.200	-	0.0079	BJ	1.950	2.050	0.0768	0.0807
AB	12.450	12.550	0.4902	0.4941	BK	16.650	16.750	0.6555	0.6594
AC	8.500	9.500	0.3347	0.3740	BL	16.650	16.750	0.6555	0.6594
AD	3.500	4.500	0.1378	0.1772					
AE	7.300	8.300	0.2874	0.3268					
AF	0.480	0.520	0.0189	0.0205					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1oz.

Reference: 98ASL00211A	. Issue "0" released on 03/20/96

TAB TAPE REEL ORIENTATION



Reference: 98ASL00211A   Issue "0" released on 03/20/96

MC141531

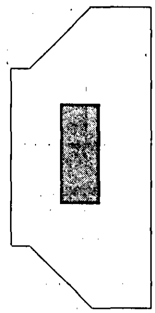
Advance Information

LCD Segment / Common Driver

CMOS

MC141531 is a CMOS LCD Driver which consists of 3 annunciator outputs and 137 high voltage LCD driving signals (17 common and 120 segment). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuits such that limited external component is required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30°C to 85°C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias DC/DC Converter
- 8 bit Parallel Interface
- Graphic Mode Operation
- On Chip 120x17 Graphic Display Data RAM
- Master clear RAM
- 120 Segment Drivers, 17 Common Drivers
- 1/16, 1/17 Multiplex Ratio
- 1:5 bias ratio
- Re-mapping of Row and Column Drivers
- Three Stand Alone Annunciator (Static Icon) Driver Circuits
- Low Power Icon Mode Driven by Com16 in Special Driving Scheme
- Selectable LCD Drive Voltage Temperature Coefficients
- 16 level Internal Contrast Control
- External Contrast Control
- Standard TAB (Tape Automated Bonding) Package, Gold Bump Die



MC141531T
TAB

MCC141531Z
Gold Bump Die

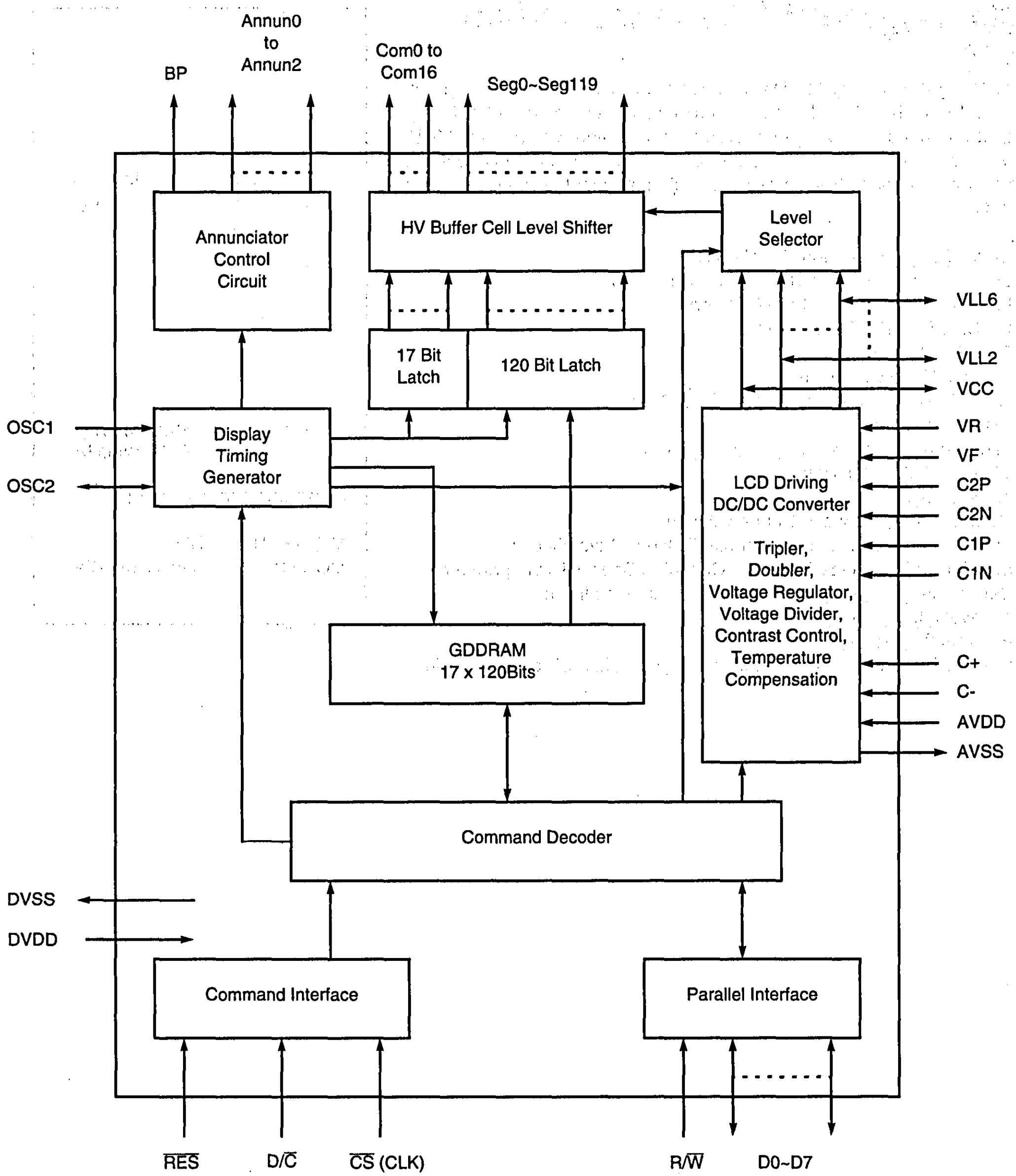
ORDERING INFORMATION

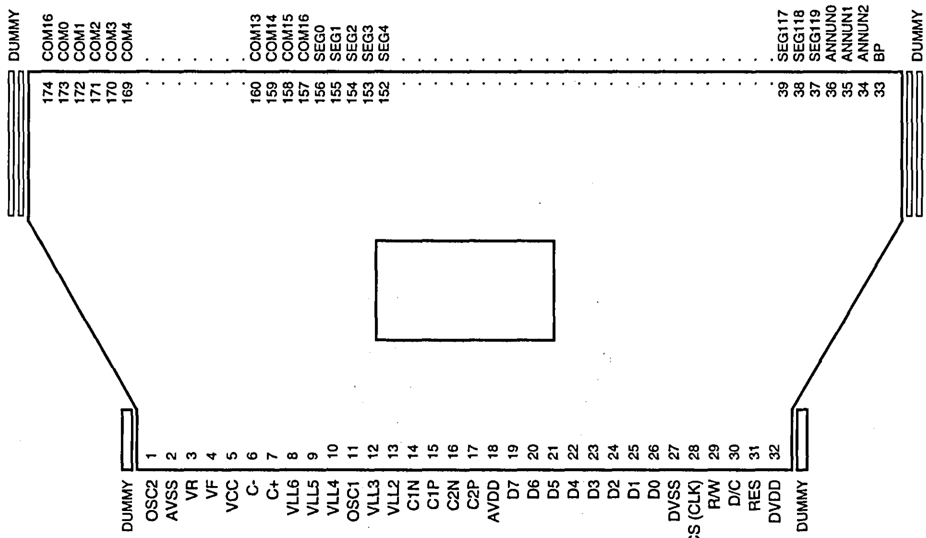
MC141531T	TAB
MCC141531Z	Gold Bump Die

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 4
3/97

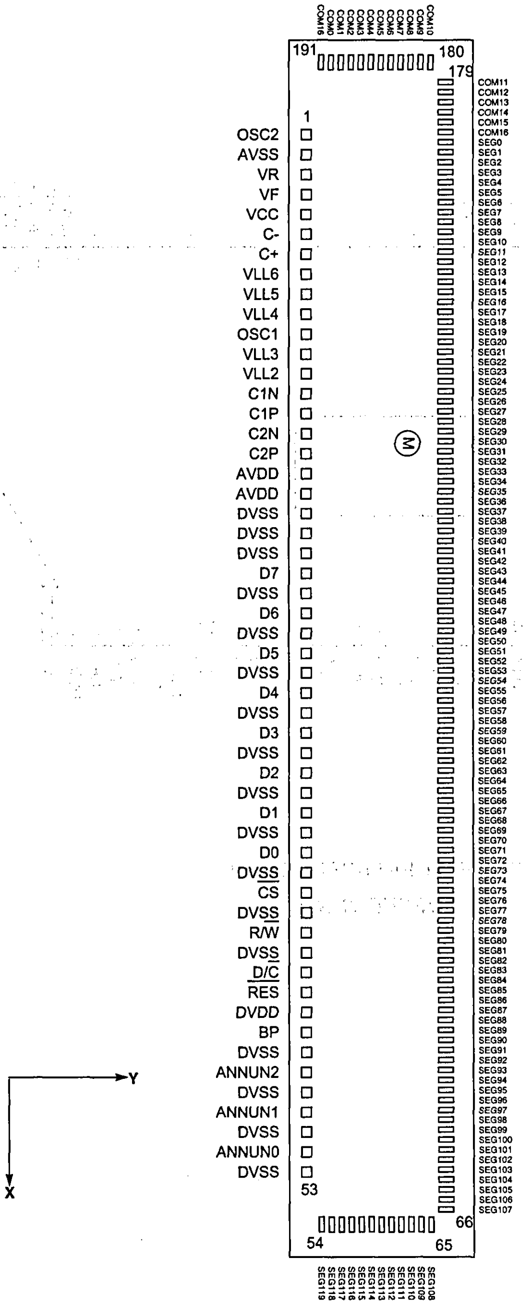
Block Diagram





MC141531T PIN ASSIGNMENT
(COPPER VIEW)

MC141531 Die Pin Assignment



MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
$V_{SS} = AV_{SS} = DV_{SS}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analogue Circuit)
$V_{DD} = AV_{DD} = DV_{DD}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DV_{DD}	Logic Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	2.4	3.0	3.5	V
AV_{DD}	DC/DC Converter Circuit Supply Voltage Range		2.4	-	3.5	V
I_{AC}	Access Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/Off, R/$\overline{W}$ accessing, T_{cyc}=1MHz, Osc. Freq.=38.4kHz, Display On, 1/7 Mux Ratio	0	200	300	µA
I_{DP}	Display Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/Off, R/W halt, Osc. Freq.=38.4kHz, Display On, 1/17Mux Ratio	0	75	165	µA
I_{SB1}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Display off, Oscillator Disabled, R/$\overline{W}$ halt.	0	300	500	nA
I_{SB2}	Annunciator Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Annunciator Mode, Internal Oscillator, Oscillator Enabled, Display Off, R/$\overline{W}$ halt, Int Osc. Freq.=38.4kHz.	0	5	10	µA
I_{SB3}	Icon Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Icon Mode, Internal Oscillator, Oscillator Enabled, Display Off, R/$\overline{W}$ halt, Ext Osc. Freq.=38.4kHz.	0	-	25	µA
V_{CC1}	LCD Driving DC/DC Converter Output (V_{CC} Pin)	Display On, Internal DC/DC Converter Enabled, Tripler Enabled, Osc. Freq.=38.4KHz, Regulator Enabled, Divider Enabled.	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving DC/DC Converter Output (V_{CC} Pin)	Display On, Internal DC/DC Converter Enabled, Doubler Enabled, Osc. Freq.=38.4KHz, Regulator Enabled, Divider Enabled.	-	2*AV_{DD}	7	V
V_{LCD}	LCD Driving Voltage Input (V_{CC} Pin)	Internal DC/DC Converter Disabled.	5	-	10.5	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Input high voltage ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		0	-	0.2*V_{DD}	V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Output (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	Voltage Divider Enabled	- - - - -	V_R 0.8*V_R 0.6*V_R 0.4*V_R 0.2*V_R	- - - - -	V V V V V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Input (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	External DC/DC Converter, Voltage Divider Disable	5 0 0 0 0	- - - - -	V_{CC} V_{LL6} V_{LL5} V_{LL4} V_{LL3}	V V V V V
I_{OH}	Output High Current Source (D0-D7, Annun0-2, BP, OSC2)	V_{out}=V_{DD}-0.4V	50	-	-	μA
I_{OL}	Output Low Current Drain (D0-D7, Annun0-2, BP, OSC2)	V_{out}=0.4V	-	-	-50	μA
I_{OZ}	Output Tri-state Current Drain Source (D0-D7, OSC2)		-1	-	1	μA
I_{IL}/I_{IH}	Input Current ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		-1	-	1	μA
R_{on}	Channel resistance between LCD driving signal pins (SEG and COM) and driving voltage input pins (V_{LL2} to V_{LL6})	During Display on, 0.1V apply between two terminals, VCC within operating voltage range	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD})	Standby mode, retain all internal configuration and RAM data	2	-	-	V
C_{IN}	Input Capacitance (OSC1, OSC2, all logic pins)		-	5	7.5	pF
	Temperature Coefficient Compensation*					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled	-	-0.35	-	%
V_{CN}	Internal Contrast Control (V_R Output Voltage)	Regulator Enabled, Internal Contrast control Enabled. (16 Voltage Levels Controlled by Software. Each level is typically 2.25% of the Regulator Output Voltage.)	-	± 18	-	%

*The formula for the temperature coefficient (TC) is:

$$TC(\%) = \frac{\text{VR at 50°C - VR at 0°C}}{\text{50°C - 0°C}} \times \frac{1}{\text{VR at 25°C}} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, AV_{DD}=DV_{DD}=3V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display timing generator	60Hz Frame Frequency Either External Clock Input or Internal Oscillator Enabled	-	38.4	-	kHz
F_{ANN}	Backplane Frequency of Annunciator (Annun0-3, BP)	50% duty cycle Annunciator on, Fosc=38.4KHz	-	30	-	Hz
F_{FRM}	Frame Frequency	Graphic Display Mode, Timing generator freq. = 38.4kHz Icon Mode, Timing generator freq. = 38.4kHz	-	60 TBD	-	Hz
OSC	Internal Oscillation Frequency with different value of feedback resistor	Internal Oscillator Enabled, V_{DD} within operation range	See Figure 1 for the relationship			

Note: $F_{FRM} = F_{OSC} / 640$
$F_{ANN} = F_{OSC} / 1280$

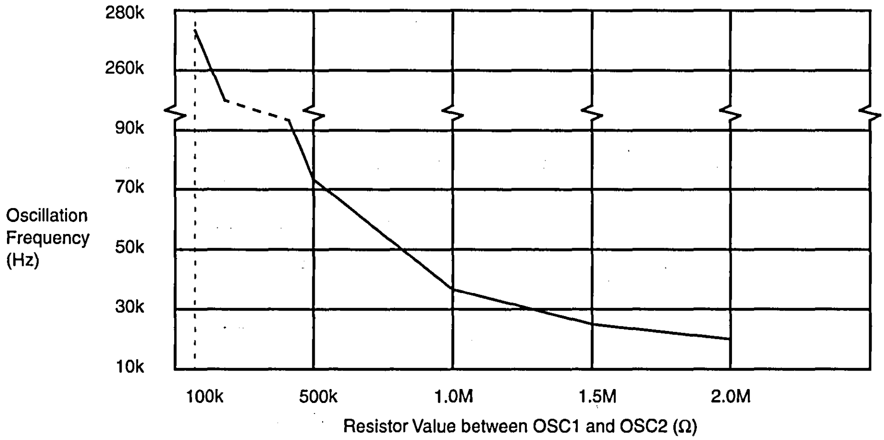


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

TABLE 2a. Parallel Timing Characteristics (Write Cycle) (T_A=-30 to 85˚C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	600	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{DS}	Data Setup Time	290	-	-	ns
t_{DH}	Data Hold Time	20	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns

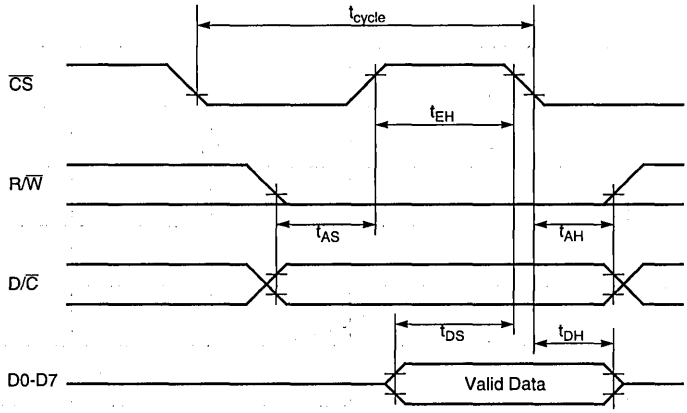


Figure 3. Timing Characteristics (Write Cycle)

TABLE 2b. Parallel Timing Characteristics (Read Cycle) (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	600	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{DS}	Data Setup Time	-	-	290	ns
t_{DH}	Data Hold Time	5	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns

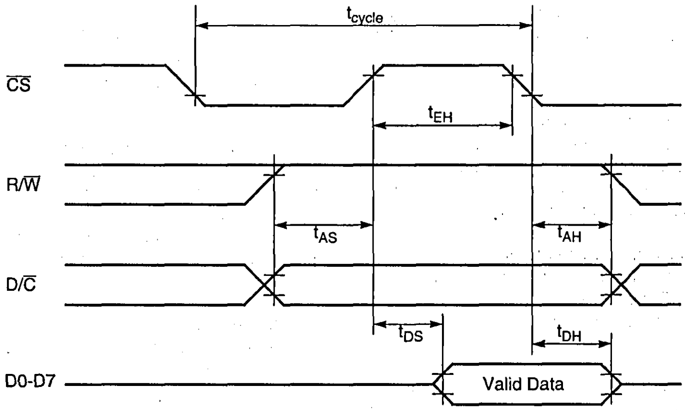


Figure 4. Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)

This input pin tell the LCD driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Input Clock)

This pin is normal Low clock input. Data on D0-D7 are latched at the falling edge of $\overline{CS}$.

$\overline{RES}$ (Reset)

An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

D0-D7 (Data)

This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read / Write)

This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/$\overline{W}$ input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value should be connected between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)

For internal oscillator mode, this is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit if internal divider is enable. For Internal DC/DC Converter enabled, a 0.1 µF capacitor to AV_{SS} is required on each pin.

C1N and C1P

If Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required to connect these two pins.

C2N and C2P

If Internal DC/DC Converter and Tripler are enabled, a 0.1 µF capacitor is required between these two pins. Otherwise, leave these pins open.

C+ and C-

If internal divider circuit is enabled, a 0.1 µF capacitor is required to connect between these two pins.

VR and VF

This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 µF capacitor placed between VR and AVSS. (Refer to the Application Circuit)

COM0-COM16 (Row Drivers)

These pins provide the row driving signal to LCD panel. Output is 0V during display off. COM16 also serves as the common driving signal in the icon mode.

SEG0-SEG119 (Column Drivers)

These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)

This pin combines with Annun0-Annun2 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of 30 Hz. It outputs low when oscillator is disabled.

Annun0 - Annun2 (Annunciator Frontplanes)

These pins are three independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a 30Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave inphase with BP. When all annunciators are disabled, all these pins output 0V.

AVDD and AVSS

AVDD is the positive supply to the LCD bias Internal DC/DC Converter. AVSS is ground.

VCC

For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS

Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (120x17 = 2040 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

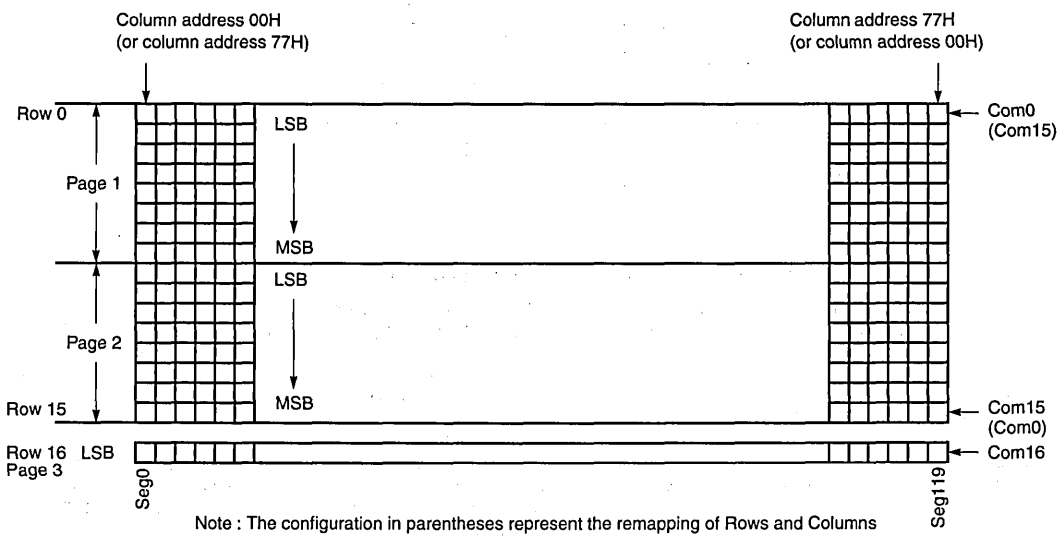


Figure 5. Graphic Display Data RAM (GDDRAM) Address Map

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15kHz to 50kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 3 annunciators and BP are generated by this module. The 3 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit. Before turning the annunciators on, the oscillator must be on in advance. Annunciator output waveform shown in Figure 7.

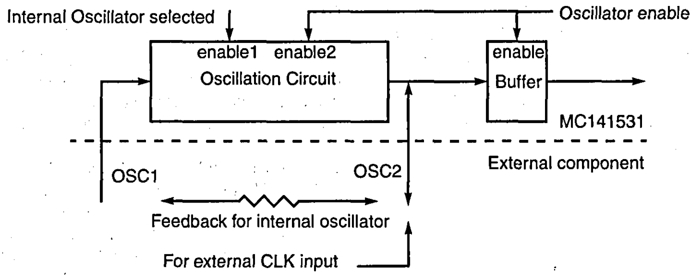


Figure 6. Oscillator Circuitry

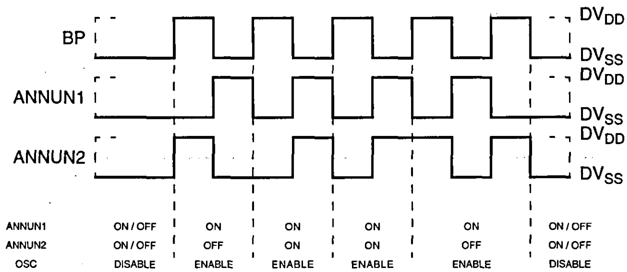


Figure 7. Annunciators and BP Display Waveform

LCD Driving Internal DC/DC Converter and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. It can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
5. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.

All blocks can be individually turned off if external DC/DC Converter is employed.

17 Bit Latch / 120 Bit Latch

A 137 bit long register which carry the display signal information. First 17 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a, 8b and 8c illustrate the desired multiplex scheme.

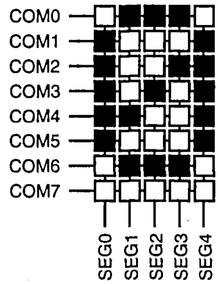


Figure 8a. LCD Display Example "0"

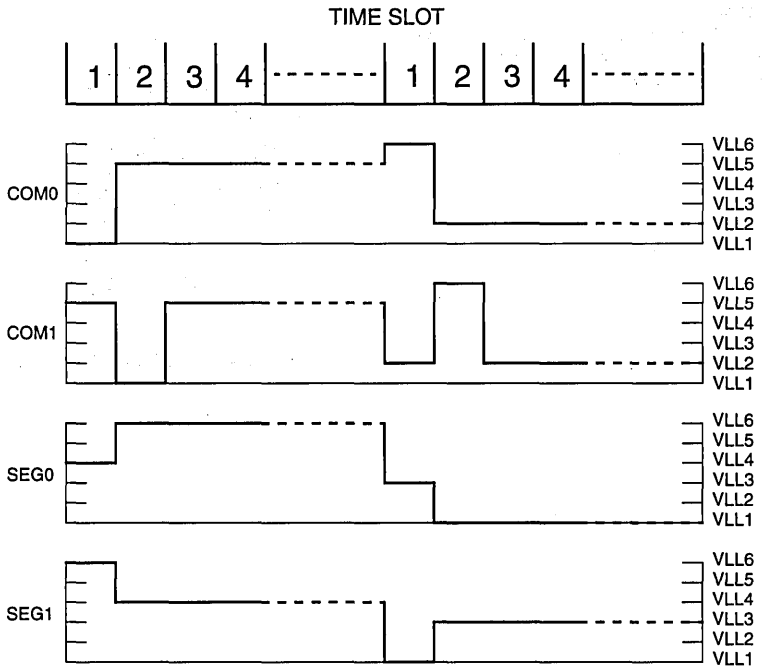


Figure 8b. LCD Driving Signal from MC141531

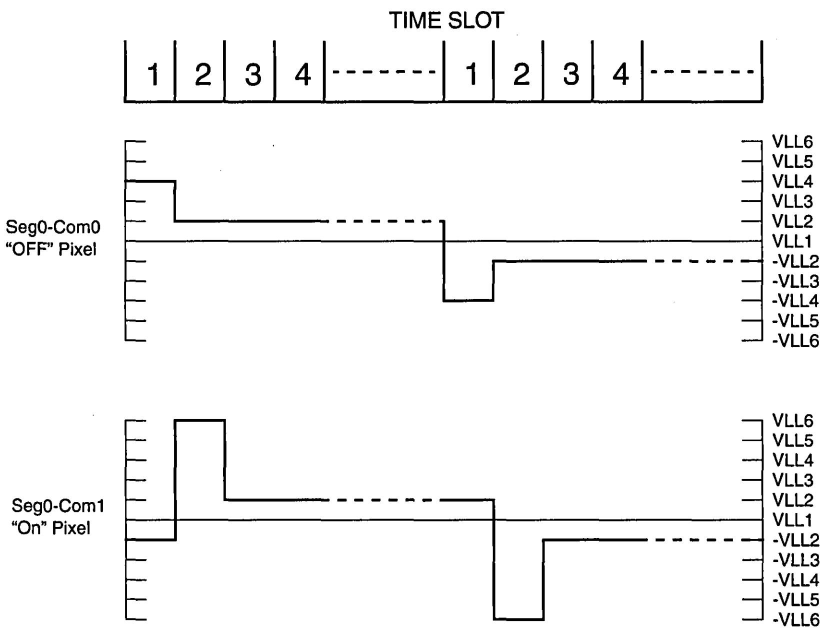


Figure 8c. Effective LCD waveform on LCD pixel

Command Description

Set Display On/Off (Display Mode / Stand-by Mode)

The Display On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command starts the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note: "Set Oscillator On" command should be sent before "Set Display On")

The Display Off command turn the display off and the states of the LCD driver are as follow during display off:

1. The Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Internal DC/DC Converter is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by this command.

Note: DON'T USE ICON DISPLAY MODE DURING DISPLAY OFF.

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-77H (120 columns). The column address will be increased automatically after a read or write operation. Refer to "Address Increment Table" and command "Set GDDRAM Page Address" for further information.

Set GDDRAM Page Address

This command positions the row address to 1 of 3 possible positions in GDDRAM. Refer to figure 5.

Master Clear GDDRAM

This command is to clear the content of page 1 and 2 of the Display Data RAM to zero. Issue this command followed by a dummy write command.

Master Clear Icons

This command is used to clear the data in page 3 of GDDRAM which stores the icon line data. Before using this command, set the page address to Page 3 by the command "Set GDDRAM Page Address". A dummy write data is also needed after this "Master Clear Icons" command to make the clear icon action effective.

Set Display Mode

This command switch the driver to full display mode or low power icon mode. In low power icon mode, only icons (driven by COM16) and annunciators are displayed, and the DC-DC converter, the Internal DC/DC Converter and the regulator are disabled. Do select 1/17 Mux ratio before using the low power icon mode.

Note: DON'T USE ICON DISPLAY MODE DURING DISPLAY OFF.

Set Multiplex Ratio

In normal display mode, the multiplex ratio could be set to be 1/16 or 1/17. For 1/16 Mux Ratio, COM16 signal should not be connected to the panel.

Set Icon Mode A/B

In Icon mode A, on-pixels are stressed by a voltage with root-mean-square value of $0.87xV_{DD}$, whereas off-pixels by $0.5xV_{DD}$. In icon mode B, on-pixels are stressed by a voltage with root-mean-square value of $0.71xV_{DD}$, whereas off-pixels by $0.41xV_{DD}$. This command is used to control the contrast of the icon line (Com16) under icon mode

Set Vertical Scroll Value

This command maps the selected GDDRAM row (00H-0FH) to Com0. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 15 are mapped to Com1 through Com15 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 15 will be mapped to Com1 through Com14 respectively and Row 0 will be mapped to Com15.

Save / Restore Column Address

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 119 of GDDRAM mapped to Seg0-Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119-Seg0 respectively.

Detail information please refer to section "Display Output Description".

Set Row Mapping

This command selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 mappings to select:

1. Row 0 - Row 15 of GDDRAM to Com0 - Com15 respectively;
2. Row 0 - Row 15 of GDDRAM to Com15 - Com0 respectively.

Output of Row 16 (Com16) will not be changed by this command. See section "Display Output Description" for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 3 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on or off the oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command "Set Display On/Off" and "Set Annunciator Control Signal". See command "Set Internal / External Oscillator" for more information

Set Internal / External Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Internal DC/DC Converter On/Off

Use this command to select the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external Vcc is provided.

Set Voltage Doubler / Tripler

Use this command to choose Doubler or Tripler when the Internal DC/DC Converter is enabled.

Set Internal Regulator On/Off

Choose bit option 0 to disable the Internal Regulator. Choose bit option 1 to enable Internal Regulator which consists of the internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is disabled, external bias can be used for V_{LL6} to V_{LL2}. If the Internal Voltage Divider is enabled, the internal circuit will generated the 1:5 bias driving voltage.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after POR.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use. After power-on reset, the contrast level is the lowest.

Set Temperature Coefficient

This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

COMMAND TABLE

Bit Pattern	Command	Comment
$000000X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X_1X_0 as address bits. X_1X_0=00 : page 1 (POR) X_1X_0=01 : page 2 X_1X_0=10 : page 3
$0001X_3X_2X_1X_0$	Set Contrast Level	With $R/\overline{W}$ pin input low, set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR.
$0010000X_0$	Set Voltage Doubler / Tripler	X_0=0 : Set Voltage Tripler (POR) X_0=1 : Set Voltage Doubler
$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
$0010010X_0$	Set Row Mapping	X_0=0 : Row0 to Com0 X_0=1 : Row0 to Com15
$0010100X_0$	Set Display On/Off	X_0=0 : display off (POR) X_0=1 : display on
$0010101X_0$	Set Internal DC/DC Converter On/Off	X_0=0 : Internal DC/DC Converter off(POR) X_0=1 : Internal DC/DC Converter on
$0010110X_0$	Set Internal Regulator On/Off	X_0=0 : Internal Regulator off(POR) X_0=1 : Internal Regulator on When application uses a supply with built-in temperature compensation, the regulator should be disabled.
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0 : Internal Voltage Divider off (POR) X_0=1 : Internal Voltage Divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0 : Internal Contrast Control off (POR) X_0=1 : Internal Contrast Control on Internal contrast circuits can be disabled if external contrast circuits is preferred.
$0011001X_0$	Set Display Mode	X_0=0 : normal display mode (1/16 or 1/17 mux) (POR) X_0=1 : low power icon display mode
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
00110110	Master Clear GDDRAM	Master clear page 1 and 2 of GDDRAM
00110111	Master Clear of Icons	Master Clear of icon line (Com16)
$0011101X_0$	Reserved.	X_0=0: normal operation (POR) X_0=1: test mode (Note: Make sure to set X_0=0 during application)

Bit Pattern	Command	Comment
$0011110X_0$	Set Multiplex Ratio	X_0=0 : 1/16 Mux ratio (POR) X_0=1 : 1/17 Mux ratio
$0011111X_0$	Set Icon Mode A/B	X_0=0 : icon mode A (POR) X_0=1 : icon mode B
$0100X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_3X_2X_1X_0$ as number of lines to scroll. Scroll value = 0 upon POR
$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00 : select annunciator 1 (POR) A_1A_0=01 : select annunciator 2 A_1A_0=10 : select annunciator 3 X_0=0 : turn selected annunciator off (POR) X_0=1 : turn selected annunciator on
01101000	Reserved	
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0= 00 : 0.00% (POR) X_1X_0= 01 : -0.18% X_1X_0= 10 : -0.22% X_1X_0= 11 : -0.35%
$0111000X_0$	Increase / Decrease Contrast Value	X_0=0 : Decrease by one X_0=1 : Increase by one (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.)
$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Make sure to set X_0=0 during application)
$0111101X_0$	Set External / Internal Oscillator	X_0=0: External oscillator (POR) X_0=1: Internal oscillator. For internal oscillator place a resistor between OSC1 and OSC2. For external oscillator mode, feed clock input to OSC2.
$0111111X_0$	Set Oscillator Disable / Enable	X_0=0: oscillator master disable (POR) X_0=1: oscillator master enable. This is the master control for oscillator circuitry. This command should be issued after the "External / Internal Oscillator" command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.

Data Read / Write

To read data from the GDDRAM, input High to $R/\overline{W}$ pin and $D/\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to $R/\overline{W}$ pin and High to $D/\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the "Commands Required for R/W Actions on RAM" Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No (invalid mode)	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.
Remarks : *1. Only data is read from RAM.
*2. If write data is issued after Command Clear RAM, Address increase is not applied.
*3. Column Address will be wrapped round when overflow.

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set External / Internal Oscillator	External	*1
Set Voltage Tripler / Doubler	Tripler	*1
Internal DC/DC Converter On	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast On	Off	*1, *3
Set Contrast Level	Contrast Level = 0	*1, *2, *3
Set Internal Voltage Divider On	Off	*1
Set Column Mapping	Seg. 0 = Col. 0	*1
Set Row Mapping	Com. 0 = Row 0	*1
Set Vertical Scroll Value	Scroll Value = 0	*1
Set Oscillator Enable	Disable	
Set Annunciator Control Signals	Annunciators all off	*1
Master Clear GDDRAM	Random	
Dummy Write Data		
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Normal Display Mode	Set External / Internal Oscillator Set Oscillator Enable, Set Display On.	$(0111101X_0)$* (01111111)* (00101001)*
Icon Display Mode	Set Internal Oscillator Set Oscillator Enable, Set Display Mode to Icon Display Mode Set Display On.	(01111011)* (01111111)* (00110011)* (00101001)*
Annunciator Display	Set External / Internal Oscillator Set Oscillator Enable, Set Annunciator On/Off.	$(0111101X_0)$* (01111111)* $(01100A_1A_0X_0)$*
Standby Mode	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*

Other Related Command with Display Mode: Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

Commands Related to Internal DC/DC Converter:
Set Oscillator Disable / Enable, Set Internal Regulator On/Off, Set Temperature Coefficient, Set Internal Contrast Control On/Off, Increase / Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Display On/Off, Set Internal / External Oscillator, Set Contrast Level, Set Voltage Doubler / Tripler

* No need to resend the command again if it is set previously.

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	$(000000X_1X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	$(0011010X_0)$
Increase GDDRAM Column Address by One	Dummy Read Data	$(X_7X_6X_5X_4X_3X_2X_1X_0)$
Master Clear GDDRAM	Master Clear GDDRAM Dummy Write Data	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$

* No need to resend the command again if it is set previously.
The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed.

Display Output Description

This is an example of output pattern on the LCD panel. The following table is a description of what is inside the CDDRAM, CGRAM and GDDRAM. Figure 9b and 9c are the output pattern on the LCD display with different command enabled.

(Display Mode, Page Swapping, Scrolling, Column Re-map and Row Re-map)

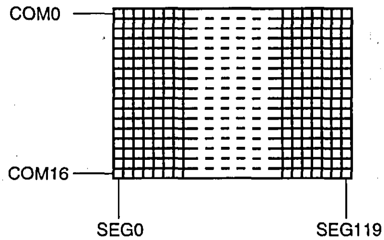
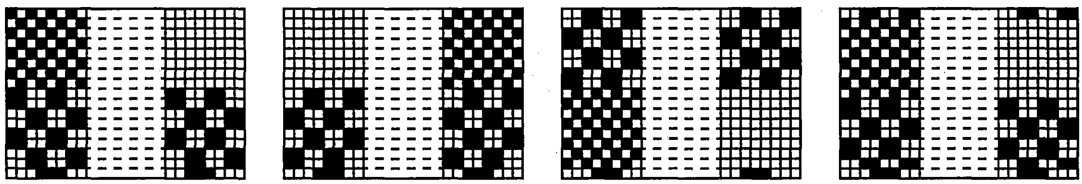


Figure 9a

Content of GDDRAM

PAGE 1	5 A 5 A 5 A 5 A - 0 0 0 0 0 0 0 0 5 A 5 A 5 A 5 A - 0 0 0 0 0 0 0 0
PAGE 2	3 3 C C 3 3 C C - 3 3 C C 3 3 C C 3 3 C C 3 3 C C - 3 3 C C 3 3 C C

Figure 9b



Column remap disable
Row re-map disable

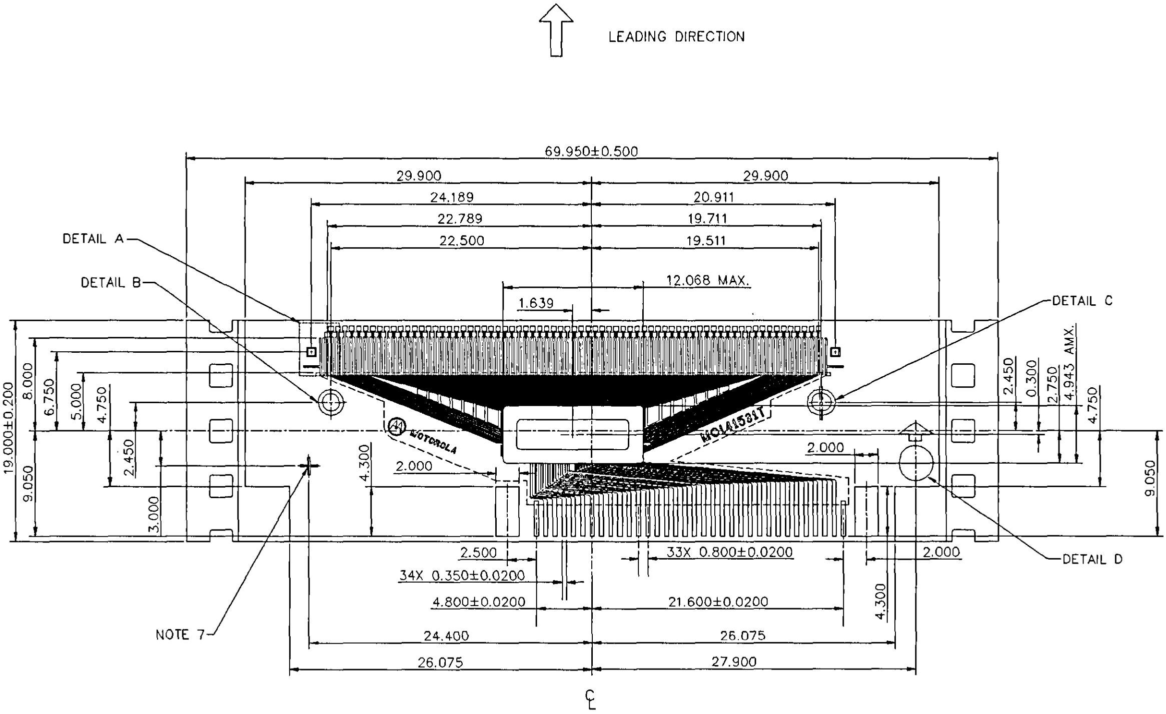
Column remap enable
Row re-map disable

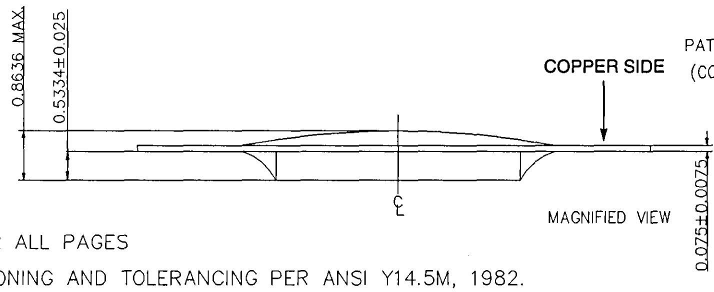
Column remap disable
Row re-map enable

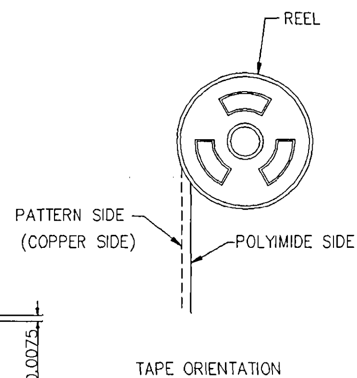
Column remap disable
Row re-map disable
Scroll Value = 0Fh

Figure 9c. Examples of LCD display with different command enabled

PACKAGE DIMENSIONS
MC141531T
TAB PACKAGE DIMENSION - 1
98ASL00247A ISSUE0



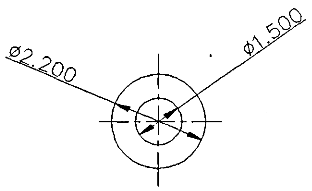




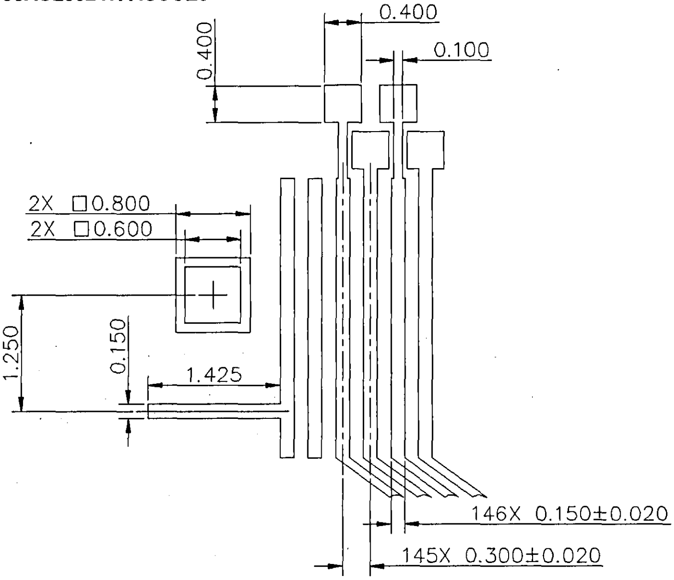
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. 4 SPROCKET HOLES DEVICE
7. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ⌀ 2.0 MM HOLE.

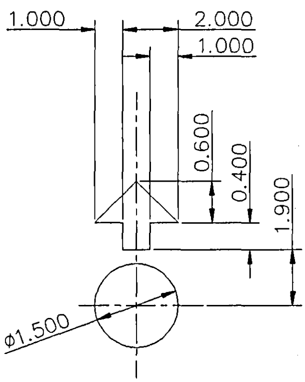
PACKAGE DIMENSIONS
MC141531T
TAB PACKAGE DIMENSION - 2
98ASL00247A ISSUE0



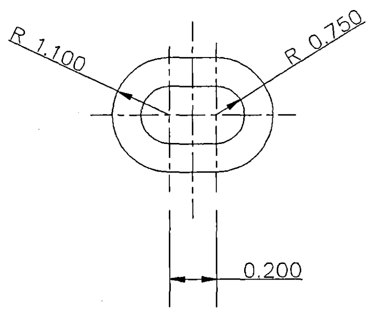
DETAIL B



DETAIL A



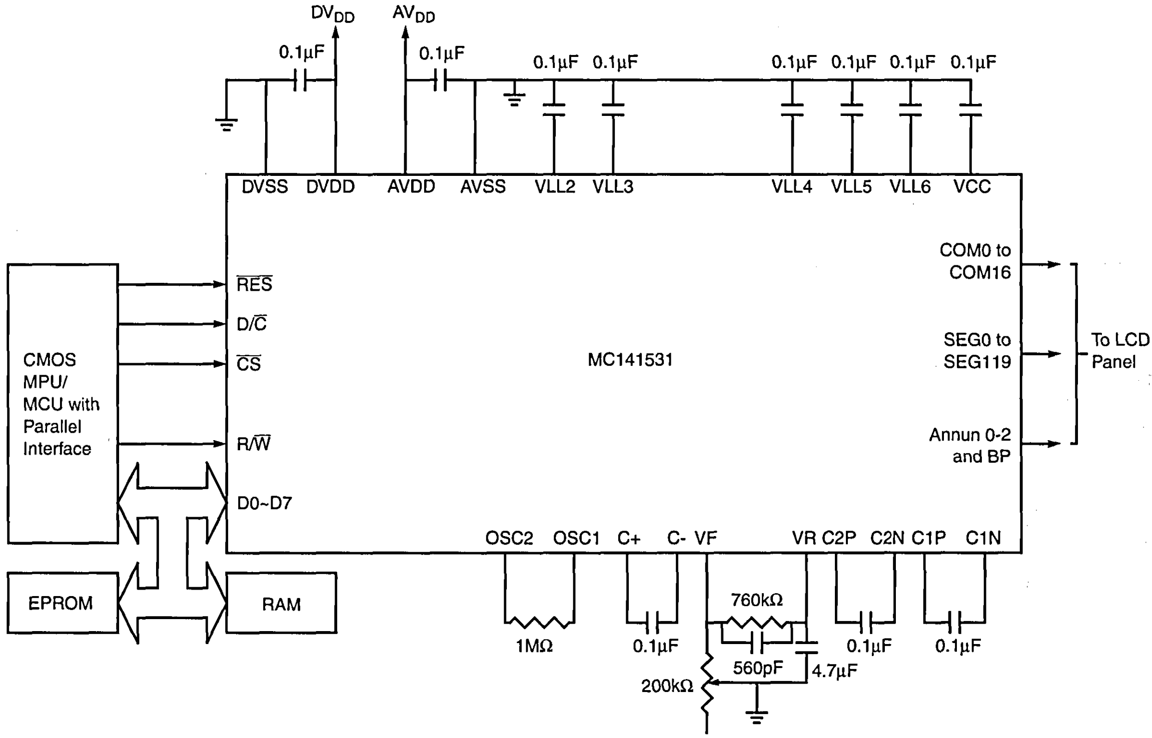
DETAIL D



DETAIL C

Application Circuit

16/17 MUX Display with Analog Circuitry enabled, Tripler enabled and 1:5 bias

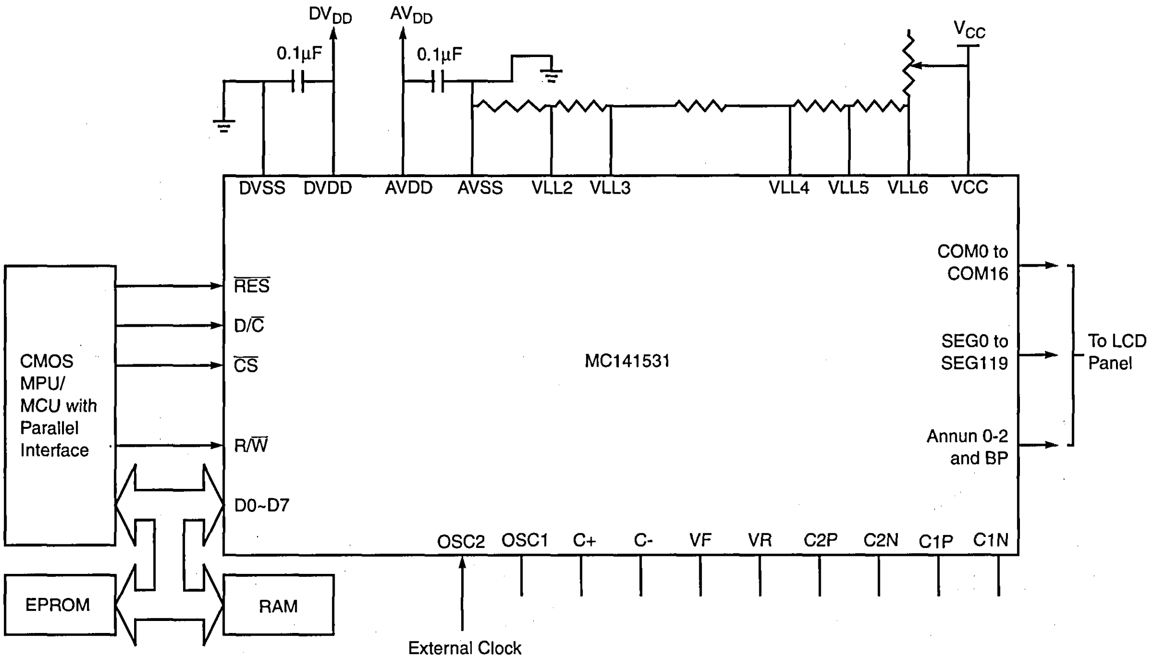


Remark :

1. Capacitor between C2N and C2P can be omitted only if doubler is enable.
2. Resistor across OSC1 and OSC2 can be omitted if external oscillator is used.
3. VR and VF can be left open for Regulator disable, TC = 0% and Contrast Disable.
4. $\overline{\text{RES}}$, $\overline{\text{CS}}$, R/$\overline{\text{W}}$ and D/$\overline{\text{C}}$ should be at a known state.
5. $\overline{\text{CS}}$ line low at Standby Mode.

Application Circuit

16/17 MUX Display with Analog Circuit disabled, External Bias



Remark :

1. Value of the resistors depends on the LCD panel characteristic.
2. $\overline{RES}$, $\overline{CS}$, R/$\overline{W}$ and D/$\overline{C}$ should be at a known state.
3. $\overline{CS}$ line low at Standby Mode.

Die Pad Coordinate of MC141531

Pad	Pin Name	X (um)	Y(um)	Bump Size (um)	Pad	Pin Name	X (um)	Y(um)	Bump Size (um)	Pad	Pin Name	X (um)	Y(um)	Bump Size (um)
1	OSC2	-3685	-762.9	76x76	71	SEG102	3925	631.5	50x108	141	SEG32	-1409	631.5	50x108
2	AVSS	-3487	-762.9	76x76	72	SEG101	3849	631.5	50x108	142	SEG31	-1485	631.5	50x108
3	VR	-3290	-762.9	76x76	73	SEG100	3773	631.5	50x108	143	SEG30	-1561	631.5	50x108
4	VF	-3183	-762.9	76x76	74	SEG99	3697	631.5	50x108	144	SEG29	-1637	631.5	50x108
5	VCC	-2985	-762.9	76x76	75	SEG98	3620	631.5	50x108	145	SEG28	-1714	631.5	50x108
6	C-	-2787	-762.9	76x76	76	SEG97	3544	631.5	50x108	146	SEG27	-1790	631.5	50x108
7	C+	-2590	-762.9	76x76	77	SEG96	3468	631.5	50x108	147	SEG26	-1866	631.5	50x108
8	VLL6	-2392	-762.9	76x76	78	SEG95	3392	631.5	50x108	148	SEG25	-1942	631.5	50x108
9	VLL5	-2194	-762.9	76x76	79	SEG94	3316	631.5	50x108	149	SEG24	-2018	631.5	50x108
10	VLL4	-1997	-762.9	76x76	80	SEG93	3239	631.5	50x108	150	SEG23	-2095	631.5	50x108
11	OSC1	-1789	-762.9	76x76	81	SEG92	3163	631.5	50x108	151	SEG22	-2171	631.5	50x108
12	VLL3	-1682	-762.9	76x76	82	SEG91	3087	631.5	50x108	152	SEG21	-2247	631.5	50x108
13	VLL2	-1485	-763.2	76x76	83	SEG90	3011	631.5	50x108	153	SEG20	-2323	631.5	50x108
14	C1N	-1287	-762.9	76x76	84	SEG89	2935	631.5	50x108	154	SEG19	-2399	631.5	50x108
15	C1P	-1089	-762.9	76x76	85	SEG88	2858	631.5	50x108	155	SEG18	-2476	631.5	50x108
16	C2N	-891.6	-762.9	76x76	86	SEG87	2782	631.5	50x108	156	SEG17	-2552	631.5	50x108
17	C2P	-693.9	-762.9	76x76	87	SEG86	2706	631.5	50x108	157	SEG16	-2628	631.5	50x108
18	AVDD	-496.2	-762.9	76x76	88	SEG85	2630	631.5	50x108	158	SEG15	-2704	631.5	50x108
19	AVDD	-298.5	-762.9	76x76	89	SEG84	2554	631.5	50x108	159	SEG14	-2780	631.5	50x108
20	DVSS	-99	-762.9	76x76	90	SEG83	2477	631.5	50x108	160	SEG13	-2857	631.5	50x108
21	DVSS	18	-762.9	76x76	91	SEG82	2401	631.5	50x108	161	SEG12	-2933	631.5	50x108
22	DVSS	124.8	-762.9	76x76	92	SEG81	2325	631.5	50x108	162	SEG11	-3009	631.5	50x108
23	D7	241.8	-762.9	76x76	93	SEG80	2249	631.5	50x108	163	SEG10	-3085	631.5	50x108
24	DVSS	348.6	-762.9	76x76	94	SEG79	2173	631.5	50x108	164	SEG9	-3161	631.5	50x108
25	D6	465.6	-762.9	76x76	95	SEG78	2096	631.5	50x108	165	SEG8	-3238	631.5	50x108
26	DVSS	572.4	-762.9	76x76	96	SEG77	2020	631.5	50x108	166	SEG7	-3314	631.5	50x108
27	D5	689.4	-762.9	76x76	97	SEG76	1944	631.5	50x108	167	SEG6	-3390	631.5	50x108
28	DVSS	796.2	-762.9	76x76	98	SEG75	1868	631.5	50x108	168	SEG5	-3466	631.5	50x108
29	D4	913.2	-762.9	76x76	99	SEG74	1792	631.5	50x108	169	SEG4	-3542	631.5	50x108
30	DVSS	1020	-762.9	76x76	100	SEG73	1715	631.5	50x108	170	SEG3	-3619	631.5	50x108
31	D3	1137	-762.9	76x76	101	SEG72	1639	631.5	50x108	171	SEG2	-3695	631.5	50x108
32	DVSS	1244	-762.9	76x76	102	SEG71	1563	631.5	50x108	172	SEG1	-3771	631.5	50x108
33	D2	1361	-762.9	76x76	103	SEG70	1487	631.5	50x108	173	SEG0	-3847	631.5	50x108
34	DVSS	1468	-762.9	76x76	104	SEG69	1411	631.5	50x108	174	COM16	-3930	631.5	50x108
35	D1	1585	-762.9	76x76	105	SEG68	1334	631.5	50x108	175	COM15	-4006	631.5	50x108
36	DVSS	1691	-762.9	76x76	106	SEG67	1258	631.5	50x108	176	COM14	-4082	631.5	50x108
37	D0	1808	-762.9	76x76	107	SEG66	1182	631.5	50x108	177	COM13	-4159	631.5	50x108
38	DVSS	1915	-762.9	76x76	108	SEG65	1106	631.5	50x108	178	COM12	-4235	631.5	50x108
39	$\overline{CS}$	2032	-762.9	76x76	109	SEG64	1030	631.5	50x108	179	COM11	-4311	631.5	50x108
40	DVSS	2139	-762.9	76x76	110	SEG63	953.4	631.5	50x108	180	COM10	-4254	140.1	108x50
41	R/$\overline{W}$	2256	-762.9	76x76	111	SEG62	877.2	631.5	50x108	181	COM9	-4254	63.9	108x50
42	DVSS	2363	-762.9	76x76	112	SEG61	801	631.5	50x108	182	COM8	-4254	-12.3	108x50
43	D/$\overline{C}$	2480	-762.9	76x76	113	SEG60	724.8	631.5	50x108	183	COM7	-4254	-88.5	108x50
44	$\overline{RES}$	2587	-762.9	76x76	114	SEG59	648.6	631.5	50x108	184	COM6	-4254	-164.7	108x50
45	DVDD	2794	-762.9	76x76	115	SEG58	572.4	631.5	50x108	185	COM5	-4254	-240.9	108x50
46	BP	2901	-762.9	76x76	116	SEG57	496.2	631.5	50x108	186	COM4	-4254	-317.1	108x50
47	DVSS	3018	-762.9	76x76	117	SEG56	420	631.5	50x108	187	COM3	-4254	-393.3	108x50
48	ANNUN2	3125	-762.9	76x76	118	SEG55	343.8	631.5	50x108	188	COM2	-4254	-469.5	108x50
49	DVSS	3242	-762.9	76x76	119	SEG54	267.6	631.5	50x108	189	COM1	-4254	-545.7	108x50
50	ANNUN1	3348	-762.9	76x76	120	SEG53	191.4	631.5	50x108	190	COM0	-4254	-621.9	108x50
51	DVSS	3465	-762.9	76x76	121	SEG52	115.2	631.5	50x108	191	COM16	-4254	-698.1	108x50
52	ANNUN0	3572	-762.9	76x76	122	SEG51	39	631.5	50x108					
53	DVSS	3689	-762.9	76x76	123	SEG50	-37.2	631.5	50x108					
54	SEG119	4254	-697.2	108x50	124	SEG49	-113.4	631.5	50x108					
55	SEG118	4254	-621	108x50	125	SEG48	-189.6	631.5	50x108					
56	SEG117	4254	-544.8	108x50	126	SEG47	-265.8	631.5	50x108					
57	SEG116	4254	-468.6	108x50	127	SEG46	-342	631.5	50x108					
58	SEG115	4254	-392.4	108x50	128	SEG45	-418.2	631.5	50x108					
59	SEG114	4254	-316.2	108x50	129	SEG44	-494.4	631.5	50x108					
60	SEG113	4254	-240	108x50	130	SEG43	-570.6	631.5	50x108					
61	SEG112	4254	-163.8	108x50	131	SEG42	-646.8	631.5	50x108					
62	SEG111	4254	-87.6	108x50	132	SEG41	-723	631.5	50x108					
63	SEG110	4254	-11.4	108x50	133	SEG40	-799.2	631.5	50x108					
64	SEG109	4254	64.8	108x50	134	SEG39	-875.4	631.5	50x108					
65	SEG108	4254	141	108x50	135	SEG38	-951.6	631.5	50x108					
66	SEG107	4306	631.5	50x108	136	SEG37	-1028	631.5	50x108					
67	SEG106	4230	631.5	50x108	137	SEG36	-1104	631.5	50x108					
68	SEG105	4154	631.5	50x108	138	SEG35	-1180	631.5	50x108					
69	SEG104	4078	631.5	50x108	139	SEG34	-1256	631.5	50x108					
70	SEG103	4001	631.5	50x108	140	SEG33	-1333	631.5	50x108					

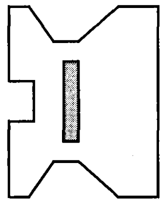
Die Size : 358.5 X 78 mil

MC141532
MC141533

Advance Information

LCD Segment / Common Driver

CMOS



TAB

Die

ORDERING INFORMATION

MC141532T	TAB
MCC141532Z	Gold Bump Die
MC141533T	TAB
MCC141533Z	Gold Bump Die

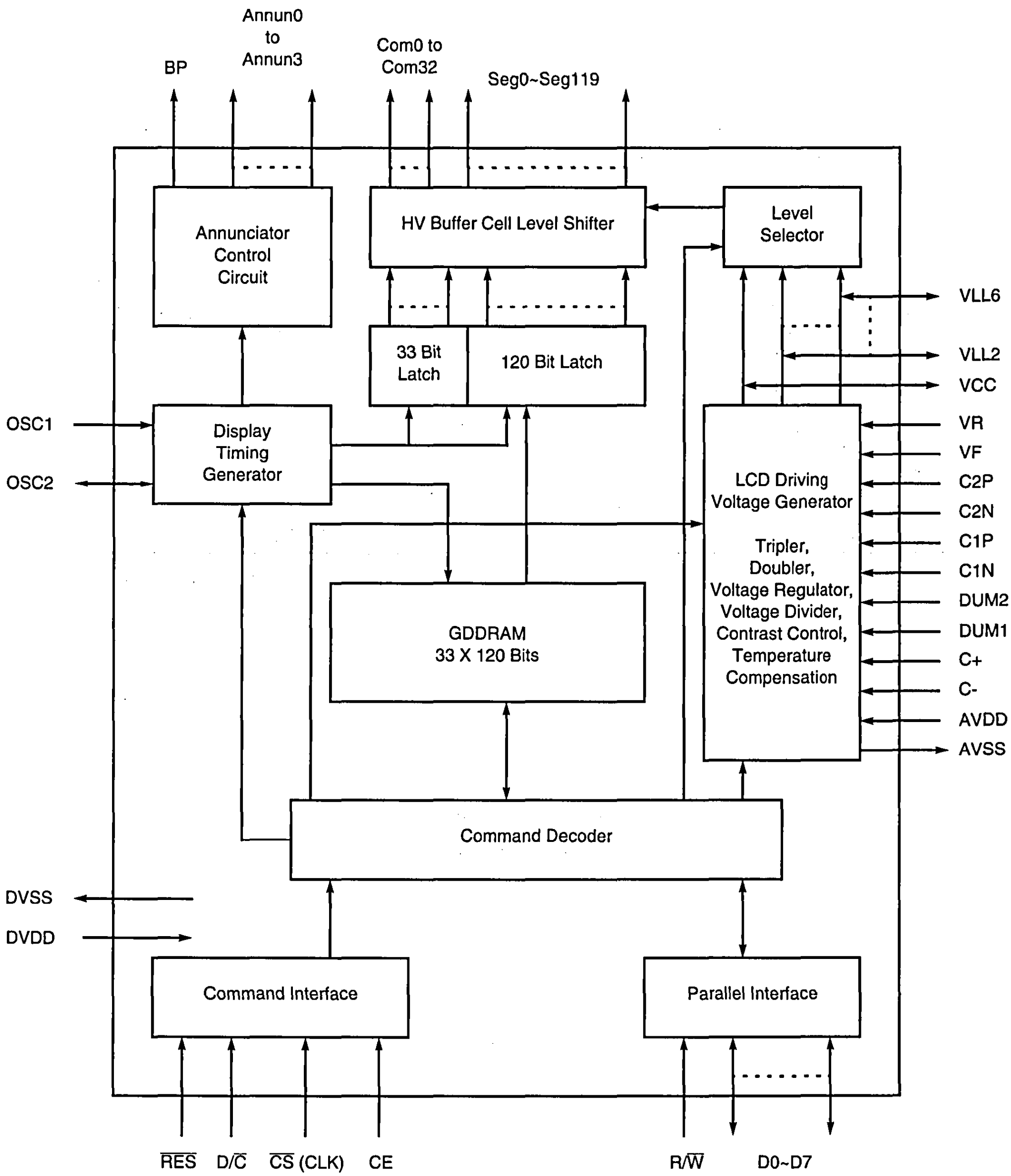
MC141532 / MC141533 is a CMOS LCD Driver which consists of 4 annunciator outputs and 153 high voltage LCD driving signals (33 commons and 120 segments). MC141532 is one sided common output while MC141533 is split common output design. It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has an on chip LCD bias Voltage Generator circuit such that fewer external components are required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30 to 80°C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 Bit Parallel Interface
- Graphic Mode Operation
- On Chip 120 x 33 Graphic Display Data RAM
- 120 Segment Drivers, 33 Common Drivers
- Selectable 1/16, 1/32, 1/33 Multiplex Ratio
- Selectable on Chip Voltage Doubler and Tripler
- Selectable 1:5 or 1:7 Bias Ratio
- Re-mapping of Row and Column Drivers
- Four Stand Alone Annunciator (Static Icon) Driver Circuits
- Low Power Icon Mode Driven by Com32 in Special Driving Scheme
- Selectable LCD Driving Voltage Temperature Coefficients
- 16 Level Internal Contrast Control
- External Contrast Control Provided
- Master Clear RAM
- Standard TAB, Gold Bump Die

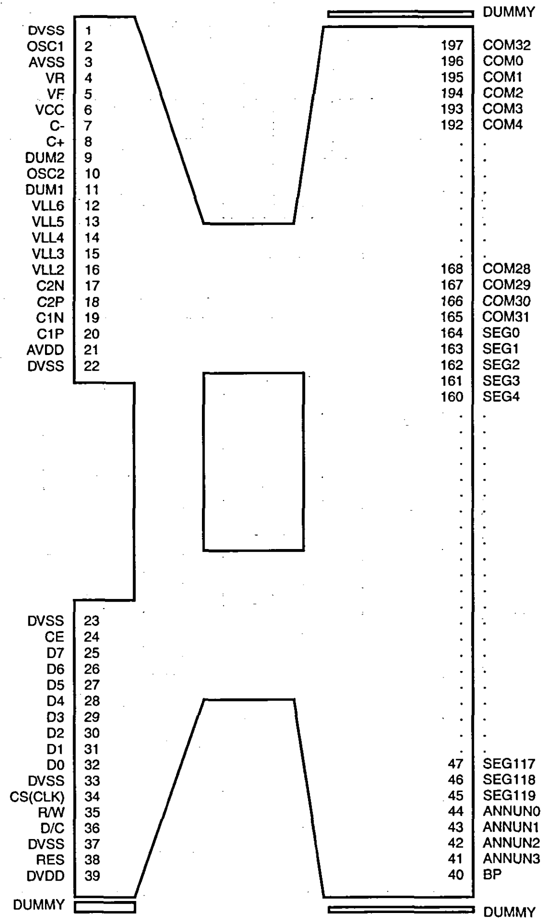
This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 7
3/97

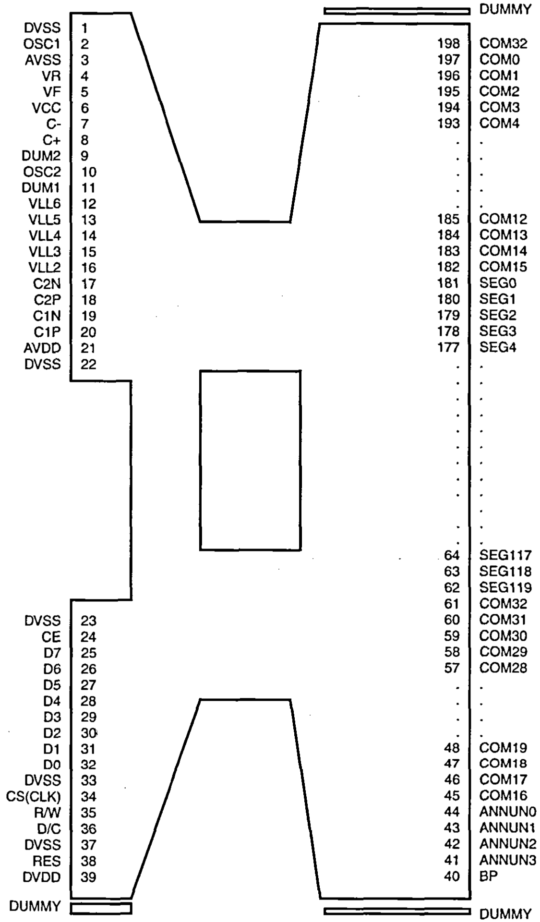
Block Diagram

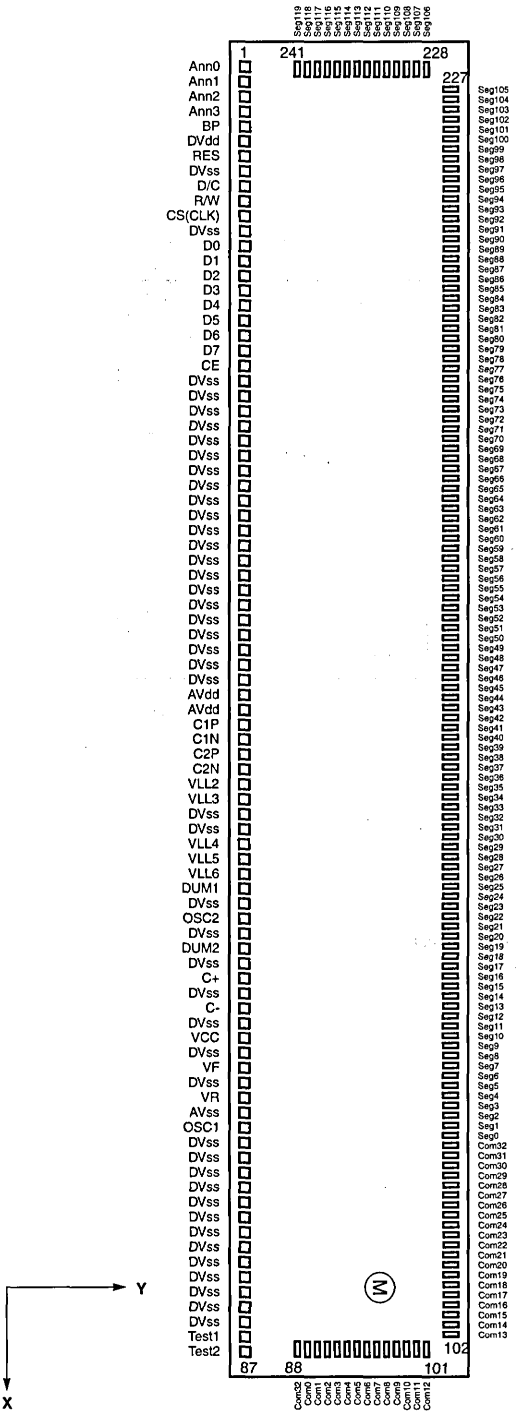


MC141532T PIN ASSIGNMENT
(COPPER VIEW)

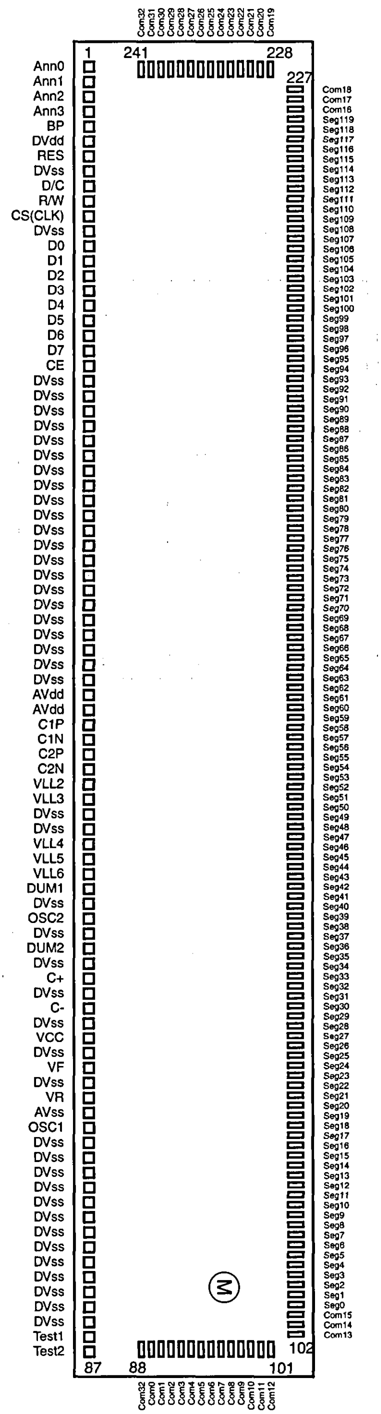


MC141533T PIN ASSIGNMENT
(COPPER VIEW)





MC141532 Die Pin Assignment



MC141533 Die Pin Assignment

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
$V_{SS} = AV_{SS} = DV_{SS}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analogue Circuit)
$V_{DD} = AV_{DD} = DV_{DD}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Supply voltage (Absolute value Referenced to V_{SS})					
DV_{DD}	Operating Range of Logic Circuit Supply DV_{DD}		2.4	3.15	3.5	V
AV_{DD}	Operating Range of Voltage Generator Circuit Supply AV_{DD}		DV_{DD}	3.15	3.5	V
	Supply Current (Measure with V_{DD} fixed at 3.15V)					
I_{AC}	Access Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Accessing, T_{cyc}=1MHz, Osc. Freq.=50kHz, 1/33 Duty Cycle,1/7 Bias.	0	200	300	μA
I_{DP1}	Display Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=50kHz, 1/33 Duty Cycle,1/7 Bias.	0	80	150	μA
I_{DP2}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz, 1/33 Duty Cycle,1/7 Bias.	0	60	100	μA
I_{SB1}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD	Display Off, Oscillator Disabled, R/W Halt	0	300	500	nA
I_{SB2}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, External Oscillator and Frequency = 50kHz.	0	2.5	5	μA
I_{SB3}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 50kHz.	0	5	10	μA
I_{ICON}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD	Low Power Icon Mode, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 50kHz	-	15	25	μA
	VLCD Voltage (Absolute Value Referenced to V_{SS})					
V_{CC1}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Tripler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100μA	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Doubler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100μA	-	2*AV_{DD}	7	V
V_{LCD}	LCD Driving Voltage input at pin V_{CC}.	Internal DC/DC Converter Disabled.	5	-	10.5	V
	Output Voltage					
V_{OH1}	Output High Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100μA	0.8*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100μA	0	-	0.2*V_{DD}	V
V_{R1}	LCD Driving Voltage Source at Pin VR	Regulator Enabled, I_{out}=50μA	0	-	V_{CC}	V
V_{R2}	LCD Driving Voltage Source at Pin VR	Regulator Disabled	-	Floating	-	V
	Input Voltage					
V_{IH1}	Input High Voltage at Pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1 and OSC2.		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage at Pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1 and OSC2.		0	-	0.2*V_{DD}	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, DV_{DD}=2.4-3.15V, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage. (LCD Driving Voltage Output from Pins VLL6, VLL5, VLL4, VLL3 and VLL2.)	1/5 Bias Ratio, Voltage Divider Enabled, Regulator Enabled.	- - - - -	V_R 0.8*V_R 0.6*V_R 0.4*V_R 0.2*V_R	- - - - -	V V V V V
V_{LL6} V_{LL5} V_{LL4} DUM2 DUM1 V_{LL3} V_{LL2}		1/7 Bias Ratio, Internal Voltage Divider Enabled, Regulator Enabled	- - - - - - -	V_R 6/7*V_R 5/7*V_R 4/7*V_R 3/7*V_R 2/7*V_R 1/7*V_R	- - - - - - -	V V V V V V V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}		External Voltage Generator, Internal Voltage Divider Disable	0.5V_{CC} 0.5V_{CC} 0.5V_{CC} V_{SS} V_{SS}	- - - - -	V_{CC} V_{CC} V_{CC} 0.5V_{CC} 0.5V_{CC}	V V V V V
	Output Current					
I_{OH}	Output High Current Source from Pins D0-D7, Annun0-3, BP and OSC2	V_{out}=VDD-0.4V.	100	-	-	μA
I_{OL}	Output Low Current Drain by Pins D0-D7, Annun0-3, BP and OSC2	V_{out}=0.4V.	-	-	-100	μA
I_{OZ}	Output Tri-state Current Drain Source at pins D0-D7 and OSC2		-1	-	1	μA
I_{IL}/I_{IH}	Input Current at pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$ OSC1 and OSC2.		-1	-	1	μA
Ron	On Resistance Channel Resistance between LCD Driving Signal Pins (SEG and COM) and Driving Voltage Input Pins (V_{LL2} to V_{LL6}).	During Display on, 0.1V Apply between Two Terminals, V_{CC} within Operating Voltage Range.	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD}) Standby Mode, Retained All Internal Configuration and RAM Data		1.8	-	-	V
C_{IN}	Input Capacitance All Control Pins		-	5	7.5	pF
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled.	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled.	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled.	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled.	-	-0.35	-	%
V_{CN}	Internal Contrast Control VR Output Voltage with Internal Contrast Control Selected. 16 Voltage Levels Controlled by Software. Each Level is Typical of 2.25% of the Regulator Output Voltage.	Internal Regulator Enabled, Internal Contrast Control Enabled.	-	±18	-	%

* The formula for the temperature coefficient is:

$$TC(\%)= \frac{\text{VR at 50°C - VR at 0°C}}{\text{50°C - 0°C}} \times \frac{1}{\text{VR at 25°C}} \times 100\%$$

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, $AV_{DD}=DV_{DD}$=2.4 to 3.5V, T_A=25°C)

Total variation of VR ΔV_{RT} is affected by the following factors :

Process variation of Regulator ΔV_R

External V_{DD} Variation contributed to Regulator ΔV_{VDD}

External resistor pair Ra/Rf contributed to Regulator ΔV_{res}

where $\Delta V_{RT} = \sqrt{(\Delta V_R)^2 + (\Delta V_{V_{DD}})^2 + (\Delta V_{res})^2}$

Assume external V_{DD} variation is ±6% at 3.15V and 1% variation resistor used at application

	TC Level	ΔV_{VDD} (%)	ΔV_R (%)	ΔV_{res} (%)	ΔV_{RT} (%)
Reference Generator	TC0	±6.0	±2.5	±1.414	±6.652
	TC1	±4.0			±4.924
	TC2	±2.5			±3.805
	TC3	±1.4			±3.195

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, V_{DD}=2.4 to 3.15V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Oscillation Frequency.	Set Clock Frequency to Slow				
F_{OSC1}	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	38.4	-	kHz
F_{ANN1}	Annunciator Display (50% duty cycle) from Pins Annun0-3 and BP		-	18.75	-	Hz
F_{FRM1}	LCD Driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, Either 1/32 or 1/16 Duty Cycle, Graphic Display Mode.	-	66	-	Hz
F_{CON1}	LCD Driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, 1/33 Duty Cycle, Graphic Display Mode.	-	64	-	Hz
	Oscillation Freq.	Set Clock Frequency to Normal				
F_{OSC2}	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	50	-	kHz
F_{ANN2}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	24.4	-	Hz
F_{FRM2}	LCD driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, Either 1/32 or 1/16 Duty Cycle.	-	65	-	Hz
F_{CON2}	LCD driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, 1/33 Duty Cycle.	-	63	-	Hz
OSC	Internal Oscillation Frequency Internal OSC Oscillation Frequency with Different Value of Feedback Resistor.	Internal Oscillator Enabled. V_{DD} within Operation Range.	See Figure 1 for the relationship			

Set Clock Frequency to Slow: $F_{FRM1}=F_{OSC1}/576$

Set Clock Frequency to Normal: $F_{FRM2}=F_{OSC2}/768$

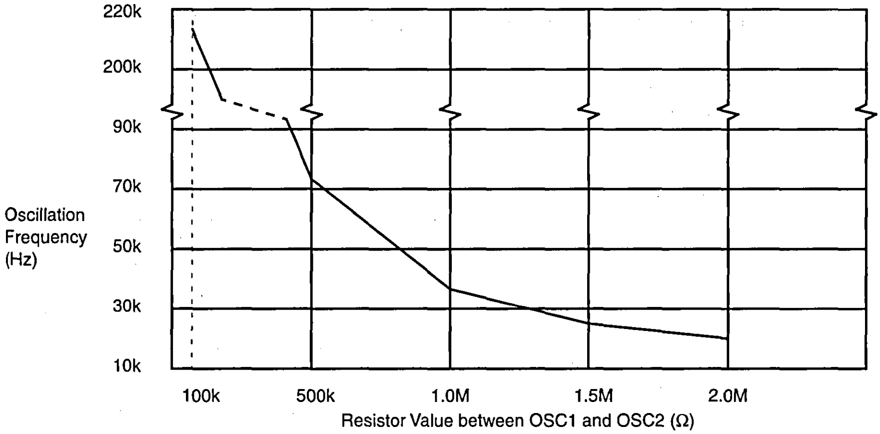


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

AC OPERATION CONDITIONS AND CHARATERISTICS

ELECTRICAL CHARACTERISTICS LCD Panel driving signal timing (T_A=-30 to 85˚C, V_{DD} = 2.4 to 3.5V, V_{SS} = 0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_{Af}	Annunciator Fall Time	-	200	TBD	ns
T_{Ar}	Annunciator Rise Time	-	200	TBD	ns

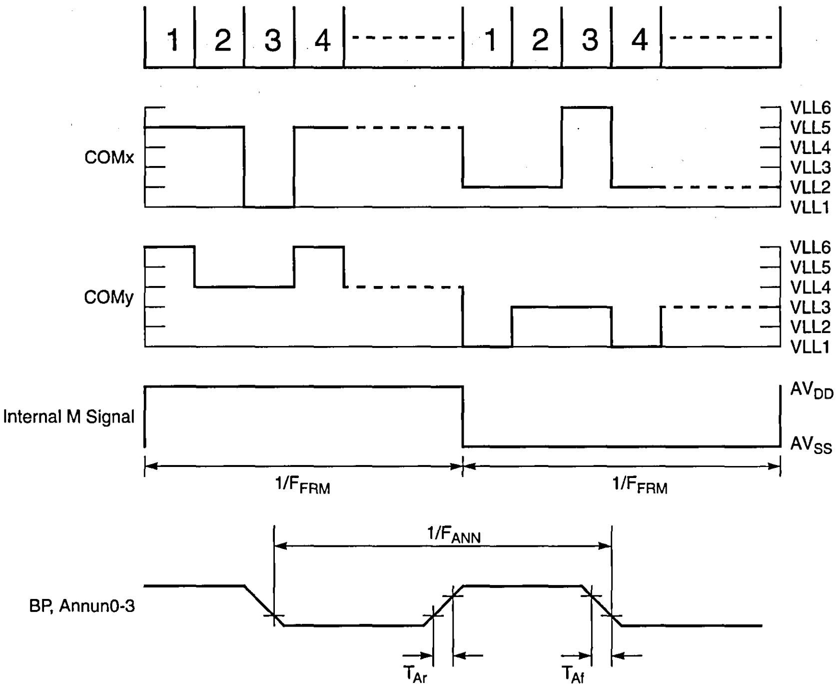


Figure 2. LCD Driving Signal Timing Diagram

TABLE 2a. Parallel Timing Characteristics (Write Cycle) (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	600	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{DS}	Data Setup Time	290	-	-	ns
t_{DH}	Data Hold Time	20	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns

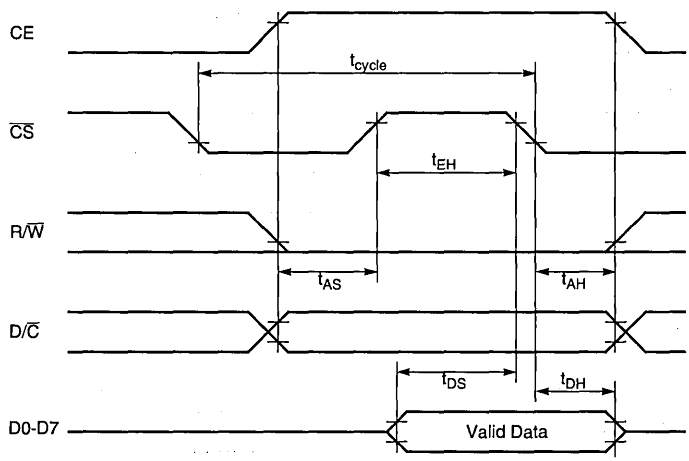


Figure 3. Timing Characteristics (Write Cycle)

TABLE 2b. Parallel Timing Characteristics (Read Cycle) (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	600	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{DS}	Data Setup Time	-	-	290	ns
t_{DH}	Data Hold Time	10	-	-	ns
t_{AH}	Address Hold Time	20	-	-	ns

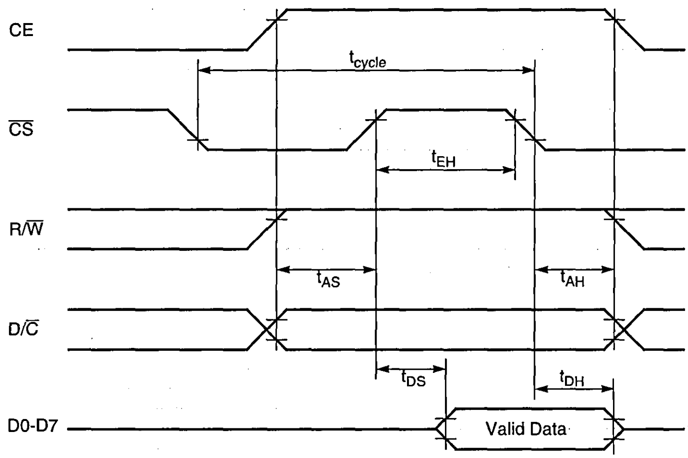


Figure 4. Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)
This input pin let the driver distinguish the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Chip Select / Input Clock)
This pin is normal Low clock input. Data on D0-D7 is latched at the falling edge of $\overline{CS}$.

$\overline{RES}$ (Reset)
An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

CE (Chip Enable)
HIGH input to this pin to enable the control pins on the driver.

D0-D7
This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read/Write)
This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/W input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)
For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)
This is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2
Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal Voltage Divider enabled, a 0.1 µF capacitor to AV_{SS} is required on each pin.

DUM1 and DUM2
If internal Voltage Divider is enabled with 1/7 bias selected, a 0.1 µF capacitor to AV_{SS} is required on each pin. Otherwise, pull these two pin to AV_{SS}

C1N and C1P
If Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required to connect these two pins.

C2N and C2P
If internal Tripler is enabled, a 0.1 µF capacitor is required between these two pins. Otherwise, leave these pin open.

C+ and C-
If internal divider circuit is enabled, a 0.1 µF capacitor is required to connect between these two pins.

VR and VF
This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 µF capacitor placed between VR and AVSS. (Refer to the Application Circuit)

COM0-COM32 (Row Drivers)
These pins provide the row driving signal to LCD panel. Com0-Com31 are used in 32 mux configuration. Com0-Com15 are used in 16 mux configuration. Com32 is used to drive the non-static icons in 33 Mux. They output 0V during display off.

SEG0-SEG119 (Column Drivers)
These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)
This pin combines with Annun0-Annun3 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANNn} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun3 (Annunciator Frontplanes)
These pins are four independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANNn} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When oscillator is disabled, all these pins output 0V.

AVDD and AVSS
AVDD is the positive supply to the noise sensitive circuitry in LCD bias Internal DC/DC Converter. AVSS is ground.

VCC
For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Positive power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS
Power is supplied to the digital control circuit and other circuitry in LCD bias Voltage Generator of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command.

Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

CE is the master chip selection signal. A High input enable the input lines ready to sample signals. Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (120x33 = 3960 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

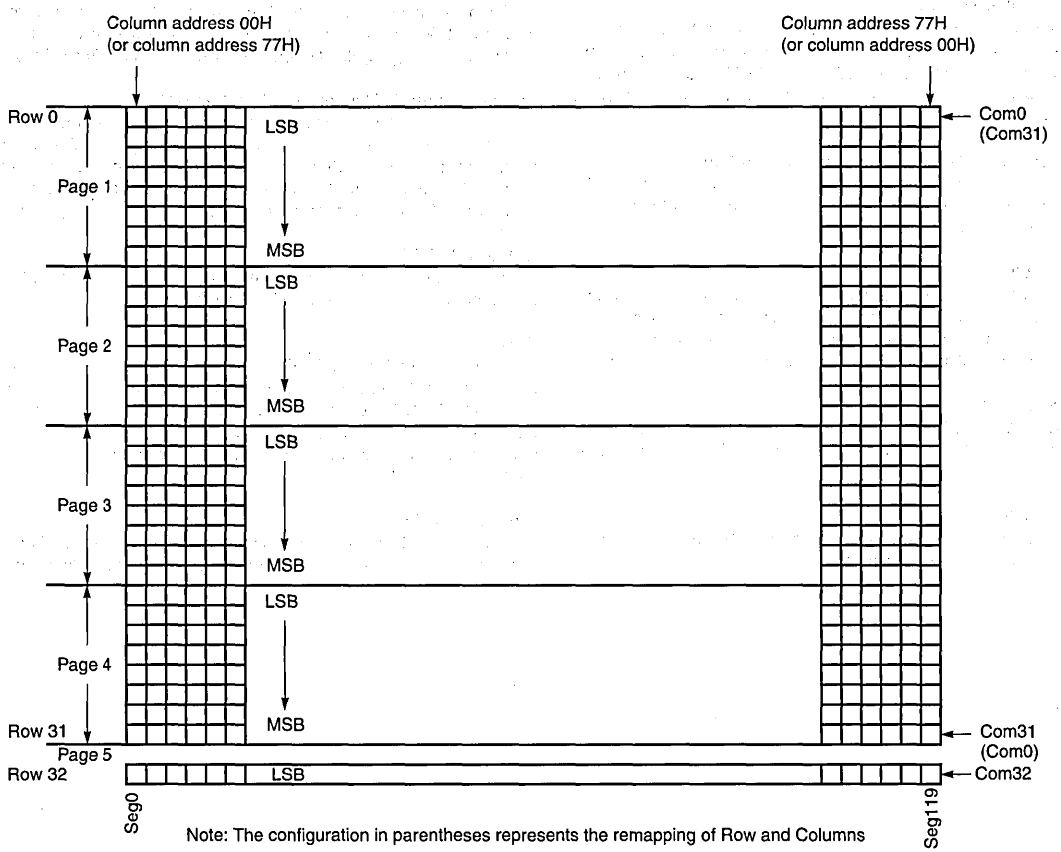


Figure 5. Graphic Display Data RAM (GDDRAM) Address Map

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15 kHz to 50 kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 4 annunciators and BP are generated by this module. The 4 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit too. Annunciator output waveform shown in Figure 7.

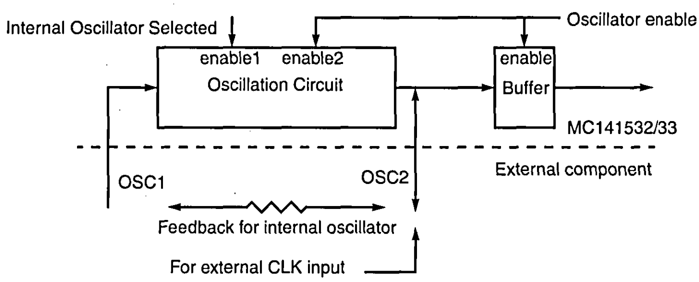


Figure 6. Oscillator Circuitry

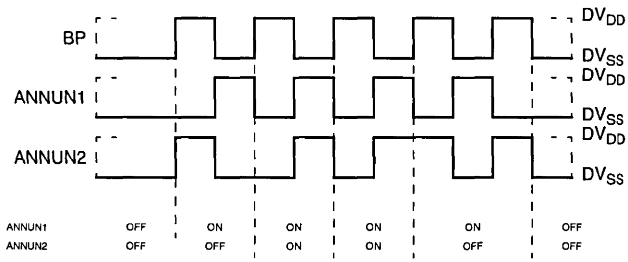


Figure 7. Annunciators and BP Display Waveform

LCD Driving Voltage Generator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. it can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Bias Ratio Selection circuitry
   Software control of 1/5 and 1/7 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
6. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.
7. External Contrast Control
   By adjusting the gain control resistors connected externally, the contrast can be varied. Refer to the application circuit for details.
   All blocks can be individually turned off if external voltage generator is employed.

33 Bit Latch / 120 Bit Latch

A 153 bit long register which carry the display signal information. First 33 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shift-er)

HV Buffer Cell works as a level shift-er which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a, 8b and 8c illustrate the desired multiplex scheme.

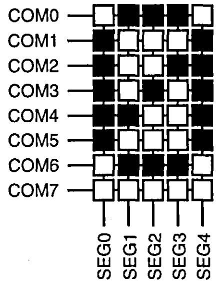


Figure 8a. LCD Display Example "0"

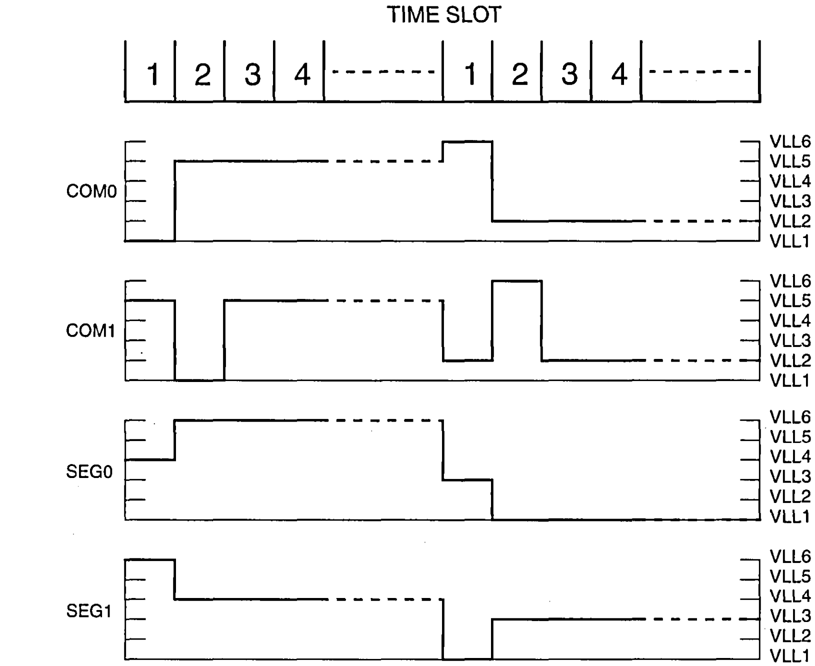


Figure 8b. LCD Driving Signal from MC141532/33

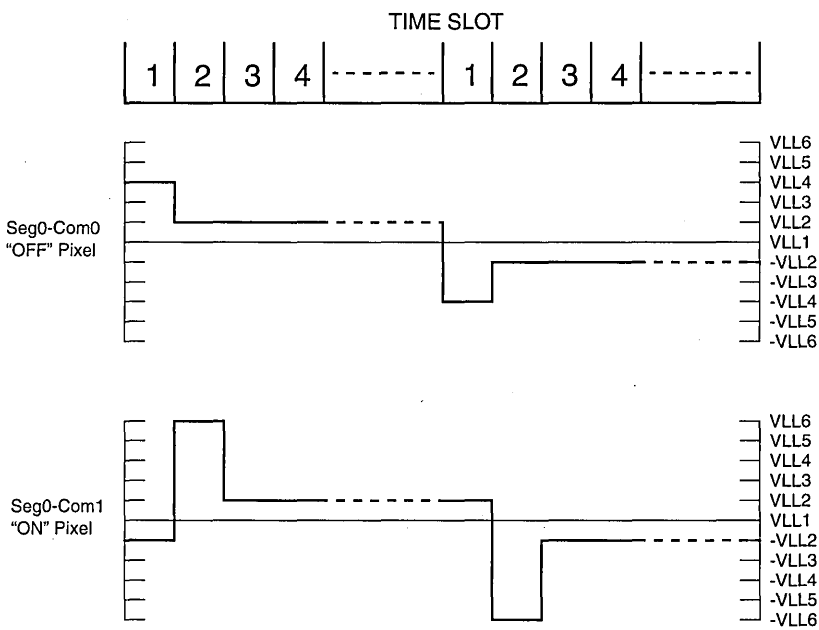


Figure 8c. Effective LCD waveform on LCD pixel

Command Description

Set Display On/Off (Display Mode / Stand-by Mode)

The Display On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command causes the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note: "Oscillator On" command should be sent before "Display On" is selected)

The Display Off command turns the display off and the states of the LCD driver are as follow during display off:

1. The Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by Display Off command.

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-77H (120 columns). The column address will be increased by one automatically after a read or write operation. Refer to "Address Increment Table" and command "Set GDDRAM Page Address".

Set GDDRAM Page Address

This command positions the row address to 1 of 5 possible positions in GDDRAM. Refer to figure 5.

Master Clear GDDRAM

This command is to clear the 480 byte GDDRAM by setting the RAM data to zero. Issue this command followed by a dummy write command. The RAM for icon line will not be affected by this command.

Master Clear Icons

This command is used to clear the data in page 5 of GDDRAM which stores the icon line data. Before using this command, set the page address to Page 5 by the command "Set GDDRAM Page Address". A dummy write data is also needed after this "Master Clear Icons" command to make the clear icon action effective.

Set Display with Icon Line

If 1/32 Mux selected, use this command change to 1/33 Mux for using the Icon LIne. This command can also change Icon Display Mode to Normal Display Mode (1/32 or 1/33 MUX).

Set Icon Display Mode

This command force the output to the icon display mode. Display on Row 0 to Row 31 will be disabled.

Set Icon Line / Annunciator Contrast Level

The contrast of the icon line and annunciators in Icon Mode can be set by this command. There are four levels to select from.

Set Vertical Scroll Value

This command is used to scroll the screen vertically with scroll value 0 to 31. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 31 are mapped to Com1 through Com31 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 31 will be mapped to Com1 through Com30 respectively and Row 0 will be mapped to Com31. Com32 is not affected by this command.

Save / Restore GDDRAM Column Address

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 119 of GDDRAM mapped to Seg0-Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119-Seg0 respectively.

Com32 will not be affected by this command. Detailed information please refer to section "Display Output Description".

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 31 of GDDRAM to Com0 - Com31 respectively;
2. Row 0 - Row 31 of GDDRAM to Com31 - Com0 respectively.

Com32 will not be affected by this command. See section "Display Output Description" for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 4 stand alone annunciator drivers.

Set Oscillator Disable / Enable

This command is used to either disable or enable the Oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command "Set Display On/Off" and "Set Annunciator Control Signal". See command "Set Internal / External Oscillator" for more information

Set Internal / External Oscillator

This command is used to select either internal or external oscillator. When Internal Oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Clock Frequency

Use this command to choose from two different oscillation frequency (50kHz or 38.4kHz) to get the 60 Hz frame frequency. With frequency high, 50 kHz clock frequency is preferred. 38.4kHz clock frequency (low frequency) enable for power saving purpose.

Set DC/DC Converter On/Off

Use this command selects the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external Vcc is provided.

Set Voltage Doubler / Tripler

Use this command to choose Doubler or Tripler when the Internal DC/DC Converter is enabled.

Set Internal Regulator On/Off

Choose bit option 0 to disable the Internal Regulator. Choose bit option 1 to enable Internal Regulator which consists of the internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is disabled, external bias can be used for V_{LL6} to V_{LL2}. If the Internal Voltage Divider is enabled, the internal circuit will automatically select the correct bias level according to the number of multiplex. Refer to command "Bias Ratio Select".

Set Duty Cycle

This command is to select 16 mux or 32 mux display. When 16 mux is enabled, the unused 16 common outputs will be swinging between VLL2 and VLL5 for dummy scan purpose and doubler will be used.

Set Bias Ratio

This command sets the 1/5 bias or 1/7 bias for the divider output. The selection should match the characteristic of LCD Panel.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after POR.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use.

Read Contrast Value

This command allows the user to read the current contrast level value. With R/$\overline{W}$ input high (READ), D/$\overline{C}$ input low (COMMAND) and D7 D6 D5 D4 are equal to 0 0 0 1, the value of the internal contrast value can be read on D0-D3 at the falling edge of CS.

Set Temperature Coefficient

This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

Set I_{DD} Reduction Mode On/Off

By using this command to reduce the display clock frequency by half. Use in Icon Mode to reduce stand-by current.

COMMAND TABLE

Bit Pattern	Command	Comment
$00000X_2X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using $X_2X_1X_0$ as address bits. $X_2X_1X_0$=000 : page 1 (POR) $X_2X_1X_0$=001 : page 2 $X_2X_1X_0$=010 : page 3 $X_2X_1X_0$=011 : page 4 $X_2X_1X_0$=100 : page 5
$000011X_1X_0$	Set Icon Line / Annunciator Contrast Level	Set one of the 4 available values to the icon and annunciator contrast, using X_1X_0 as data bits. X_1X_0=00 at POR
$0001X_3X_2X_1X_0$	Set Contrast Level	Set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ *as data bits. The contrast register is reset to 0000* during POR.
$0001X_3X_2X_1X_0$	Read Contrast Value	With $D/\overline{C}$ pin input Low, $R/\overline{W}$ pin input high, and D7 D6 D5 D4 pins equal to 0001 at the rising edge of $\overline{CS}$, the value of the internal contrast register will be latched out at D3 D2 D1 D0 pins, i.e. $X_3X_2X_1X_0$, at the rising edge of $\overline{CS}$.
$0010000X_0$	Set Voltage Doubler / Tripler	X_0=0: Select Voltage Tripler (POR) X_0=1: Select Voltage Doubler
$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
$0010010X_0$	Set Row Mapping	X_0=0 : Row0 to Com0 (POR) X_0=1: Row0 to Com31
$0010011X_0$	Reserved	
$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
$0010101X_0$	Set DC/DC Converter On/Off	X_0=0: DC/DC Converter off (POR) X_0=1: DC/DC Converter on
$0010110X_0$	Set Internal Regulator On/Off	X_0=0: Internal Regulator off (POR) X_0=1: *Internal Regulator on* When the application employs external contrast control, the internal contrast control, temperature compensation and the Regulator must be enabled.
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: Internal Voltage Divider off (POR) X_0=1: Internal Voltage Divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal Contrast Control off (POR) X_0=1: Internal Contrast Control on Internal contrast circuits can be disabled if external contrast circuits is preferred.
$0011001X_0$	Set Clock Frequency	X_0=0 : low frequency (38.4kHz) (POR) X_0=1 : high frequency (50kHz)
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
00110110	Master Clear GDDRAM	Master clear GDDRAM page 1 to 4
00110111	Master Clear Icons	Master Clear of GDDRAM page 5. GDDRAM page 5 should be selected and dummy write is required
$0011100X_0$	Set Bias Ratio	X_0=0: set 1/7 bias (POR) X_0=1: set 1/5 bias
$0011101X_0$	Reserved.	X_0=0: normal operation (POR) X_0=1: test mode (Note: Make sure to set X_0=0 during application)

Bit Pattern	Command	Comment
$0011110X_0$	Set Display with Icon Line	X_0=0: set display mode without Icon Line X_0=1: set display mode with Icon Line
00111110	Set Icon Display Mode	Power saving icon display mode, Com0 to Com32 will be disabled
$010X_4X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_4X_3X_2X_1X_0$ as number of lines to scroll. Scroll value = 0 upon POR
$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 1 (POR) A_1A_0=01: select annunciator 2 A_1A_0=10: select annunciator 3 A_1A_0=11: select annunciator 4 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on
$0110100X_0$	Set Duty Cycle	X_0=0: 1/32 duty and tripler enabled (POR) X_0=1: 1/16 duty and doubler enabled
$0110101X_0$	Set I_{DD} Reduction Mode	X_0=0: Normal Mode X_0=1: I_{DD} Reduction Mode
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00 : 0.00% (POR) X_1X_0=01 : -0.18% X_1X_0=10 : -0.22% X_1X_0=11 : -0.35%
$0111000X_0$	Increase / Decrease Contrast Value	X_0=0: Decrease by one level X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.
$0111001X_0$	Reserved	
$0111010X_0$	Reserved	
$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Make sure to set X_0=0 during application)
$0111100X_0$	Reserved	
$0111101X_0$	Set Internal / External Oscillator	X_0=0: Internal oscillator (POR) X_0=1: External oscillator. Internal oscillator circuit is automatically enabled if resistors are placed at OSC1 and OSC2. For external oscillator, simply feed clock in OSC2.
$0111110X_0$	Reserved	
$0111111X_0$	Set Oscillator Disable / Enable	X_0=0: oscillator disable (POR) X_0=1: oscillator enable. This is the master control fro oscillator circuitry. This command should be issued after the "External / Internal Oscillator" command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.

Data Read / Write

To read data from the GDDRAM, input High to $R/\overline{W}$ pin and $D/\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to $R/\overline{W}$ pin and High to $D/\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the "Commands Required for R/W Actions on RAM" Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.

Remarks : *1. Refer to the command "Read Contrast Value".
*2. If write data is issued after Command Clear RAM, Address Increase is not applied.
*3. Column Address will be wrapped round when overflow.

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set Clock Frequency	Low	*1
Set Oscillator Enable	Disable	*1
Set Annunciator Control Signals	Annunciator all Off	*1
Set Duty Cycle	1/32 duty	*1
Set Bias Ratio	1/7 bias	*1
Set Internal DC/DC Converter On	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Increase Contrast Level	Contrast Level = 0	*1, *2, *3
Set Internal Voltage Divider On	Off	*1
Set Segment Mapping	Seg. 0 = Col. 0	
Set Common Mapping	Com. 0 = Row 0	
Set Vertical Scroll Value	Scroll Value = 0	
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Display Mode	Set External / Internal Oscillator, Set Oscillator Enable, Set Display On.	$(0111101X_0)$* (01111111)* (00101001)*
Annunciator Display	Set External / Internal Oscillator, Set Oscillator Enable, Set Annunciator Control Signal.	$(0111101X_0)$* (01111111)* $(01100A_1A_0X_0)$*
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator, Set Annunciator Control Signal, Set Display Off, Set Oscillator Enable.	(01111011)* $(01100A_1A_0X_0)$* (00101000)* (01111111)*
Standby Mode 3.	Set Internal Oscillator, Set Annunciator Control Signal, Set Display Off, Set Oscillator Enable.	(01111010)* $(01100A_1A_0X_0)$* (00101000)* (01111111)*

Other Related Command with Display Mode: Set Duty Cycle, Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

Commands Related to Internal DC/DC Converter:
Set Oscillator Disable / Enable, Set Internal Regulator On/Off, Set Duty Cycle, Set Temperature Coefficient, Set Internal Contrast Control On/Off, Increase / Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Bias Ratio, Set Display On/Off, Set Internal / External Oscillator, Set Contrast Level, Set Voltage Doubler / Tripler, Set 33 Mux Display Mode, Set Icon Display Mode

* No need to resend the command again if it is set previously.

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	$(000X_4X_3X_2X_1X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	$(0011010X_0)$
Increase GDDRAM Address by One	Dummy Read Data	$(X_7X_6X_5X_4X_3X_2X_1X_0)$
Master Clear GDDRAM	Master Clear GDDRAM Dummy Write Data	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$

* No need to resend the command again if it is set previously.

Display Output Description

This is an example of output pattern on the LCD panel. Figure 9b and 9c are data map of GDDRAM and the output pattern on the LCD display with different command enabled.

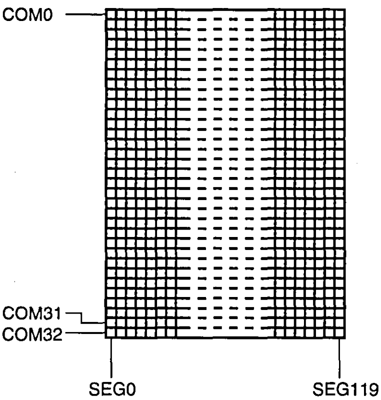
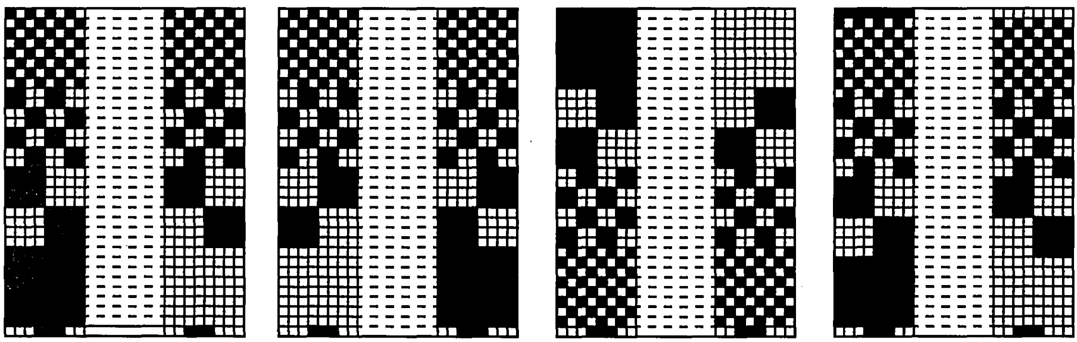


Figure 9a

		Content of GDDRAM
PAGE 1	Upper Nibble	5 A 5 A 5 A 5 A 5 A - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
	Lower Nibble	5 A 5 A 5 A 5 A 5 A - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
PAGE 2	Upper Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - C C 3 3 C C 3 3 C C
	Lower Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - C C 3 3 C C 3 3 C C
PAGE 3	Upper Nibble	0 0 0 0 F F F F 0 0 - - - - - - - - - F F 0 0 0 0 F F F F
	Lower Nibble	F F F F 0 0 0 0 F F - - - - - - - - - 0 0 F F F F 0 0 0 0
PAGE 4	Upper Nibble	F F F F F F F F 0 0 - - - - - - - - - F F 0 0 0 0 0 0 0 0
	Lower Nibble	F F F F F F F F 0 0 - - - - - - - - - F F 0 0 0 0 0 0 0 0
PAGE 5	Upper Nibble	0 0 0 0 0 0 0 0 0 0 - - - - - - - - - 0 0 0 0 0 0 0 0 0 0
	Lower Nibble	0 0 0 1 1 1 0 0 0 0 - - - - - - - - - 0 0 0 0 1 1 1 0 0 0

Figure 9b



Column remap disable
Row re-map disable

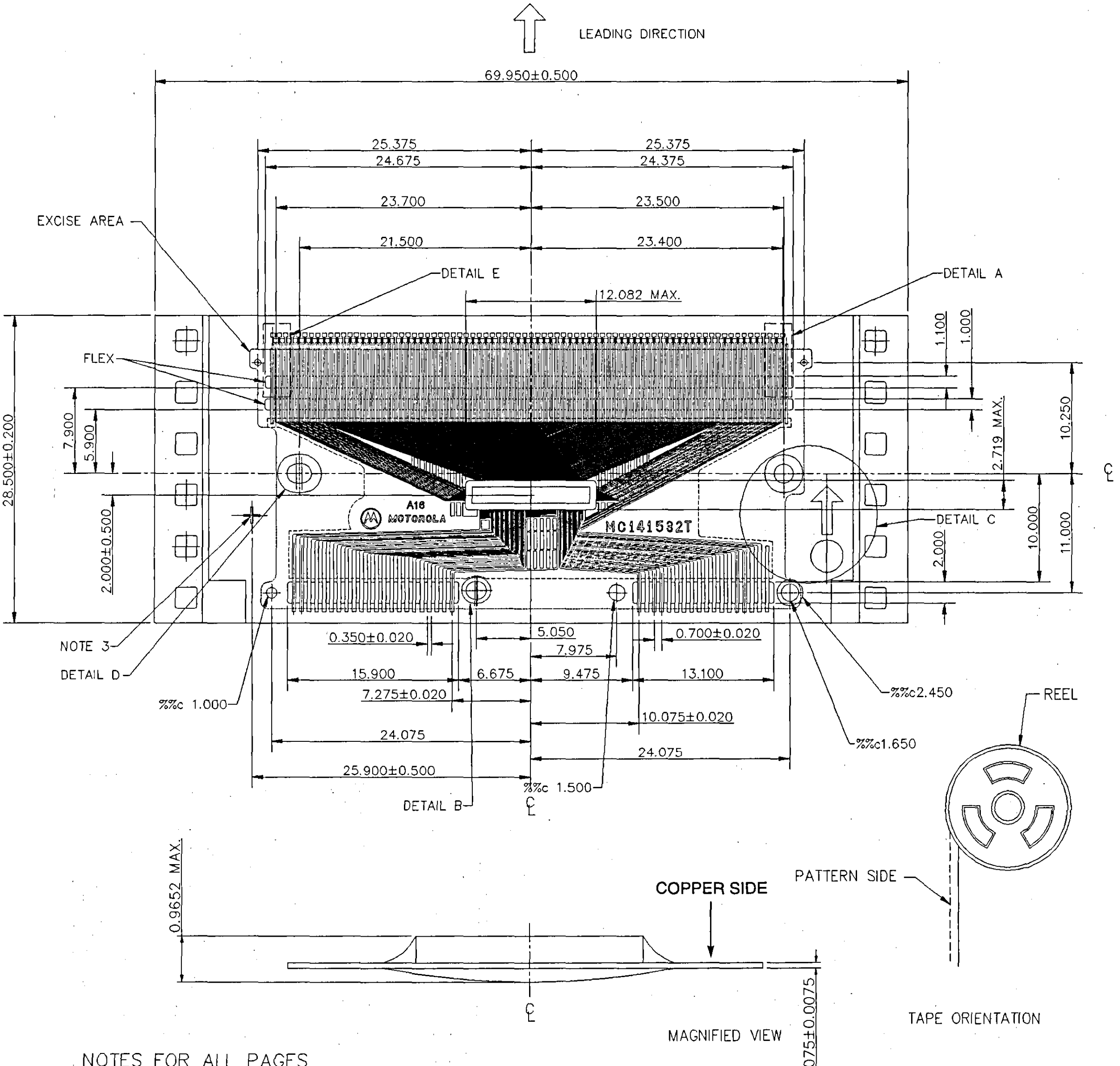
Column remap enable
Row re-map disable

Column remap disable
Row re-map enable

Column remap disable
Row re-map disable
Scroll Value = 31

Figure 9c. Examples of LCD display with different command enabled

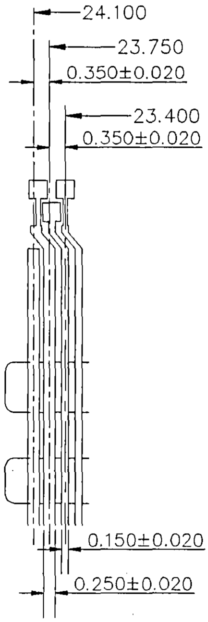
PACKAGE DIMENSIONS
MC141532T
TAB PACKAGE DIMENSION - 1



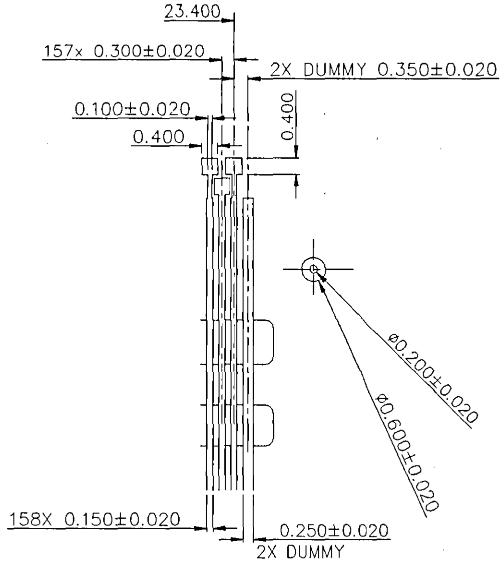
NOTES FOR ALL PAGES

1. BASE MATERIAL: 75 MICRON UPILEX–S
2. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
3. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ∅ 2.0 MM HOLE.
4. IF NOT SPECIFIED, SIZE IN MILLIMETER
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. 6 SPROCKET HOLES DEVICE
7. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05

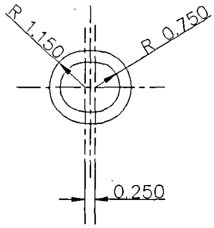
PACKAGE DIMENSIONS
MC141532T
TAB PACKAGE DIMENSION - 2



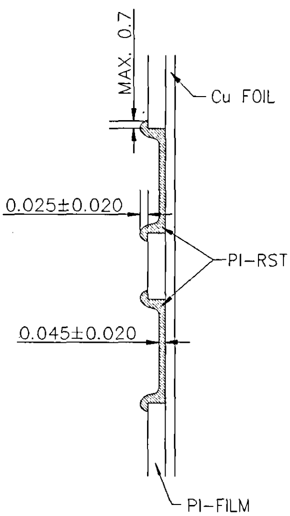
DETAIL E

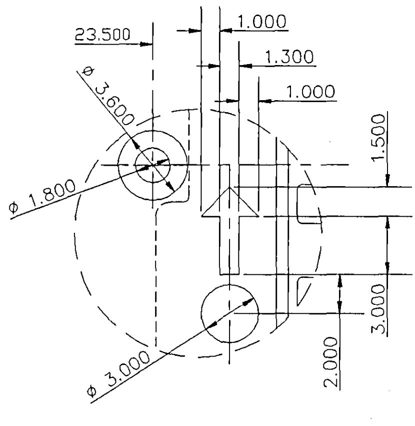


DETAIL A

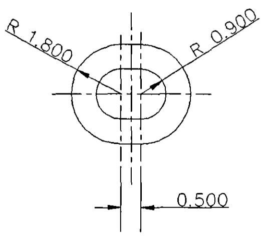


DETAIL B





DETAIL C

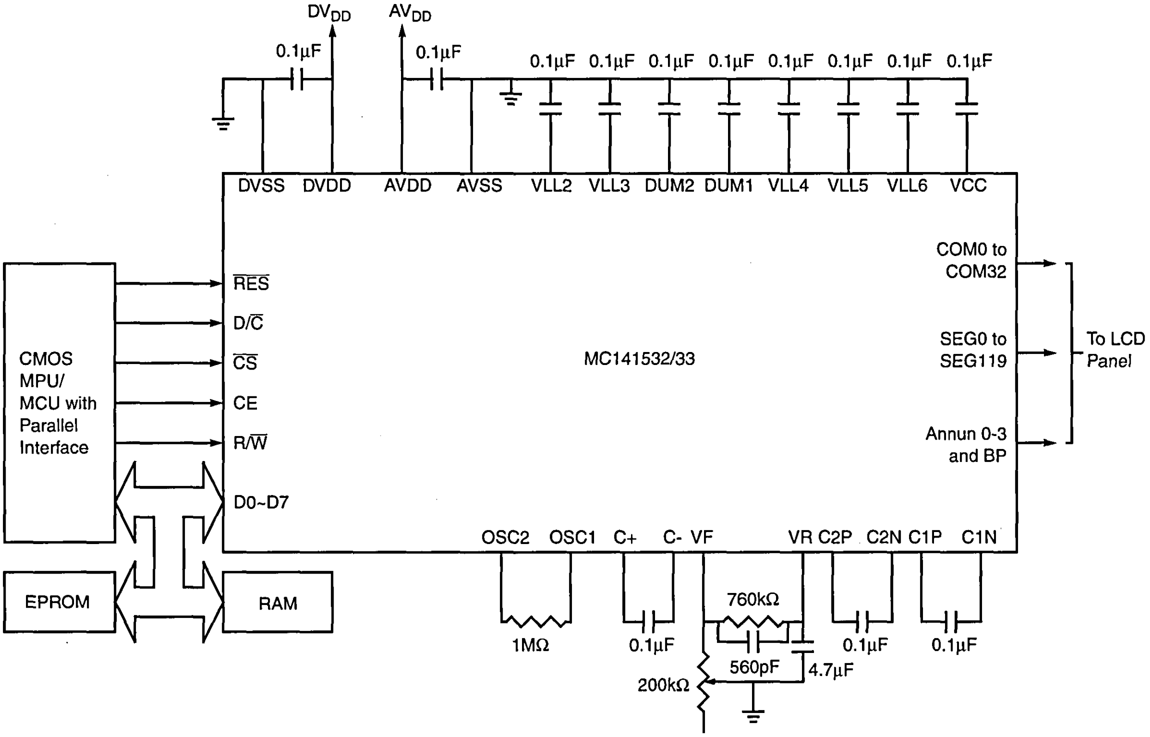


DETAIL D

FLEX MATERIAL DETAIL

Application Circuit

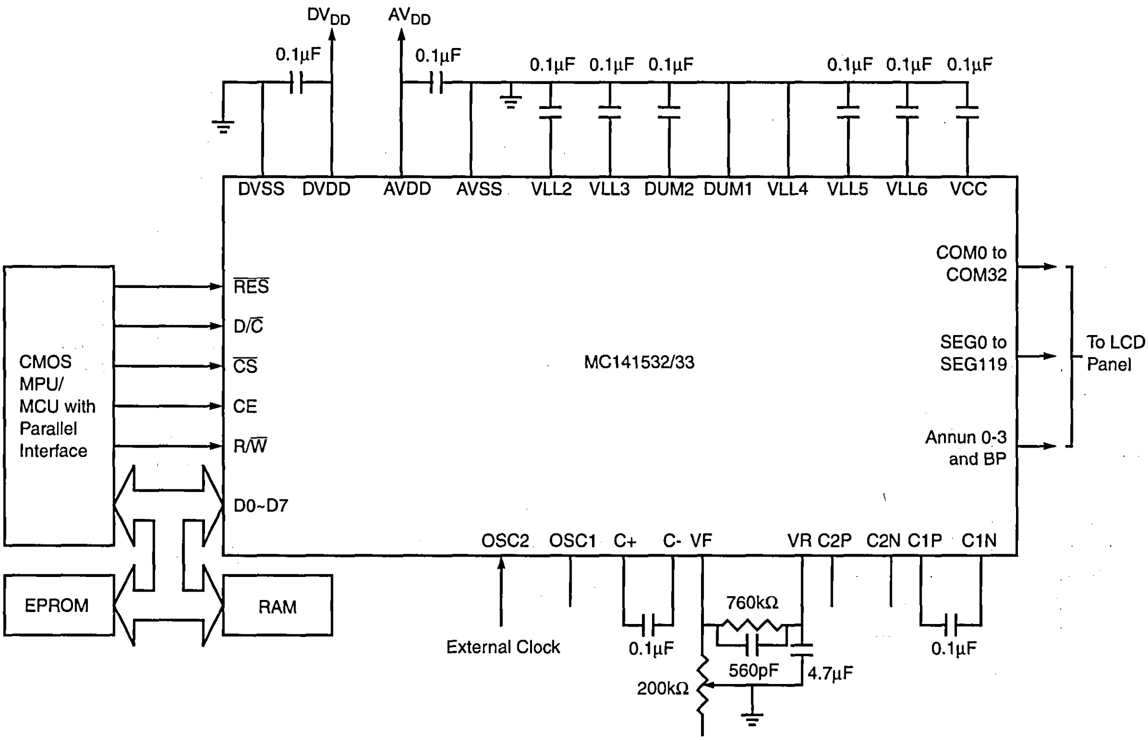
32/33 MUX Display with Analog Circuitry enabled, Tripler enabled and 1/7 bias



Remark :
1. VR and VF can be left open for Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

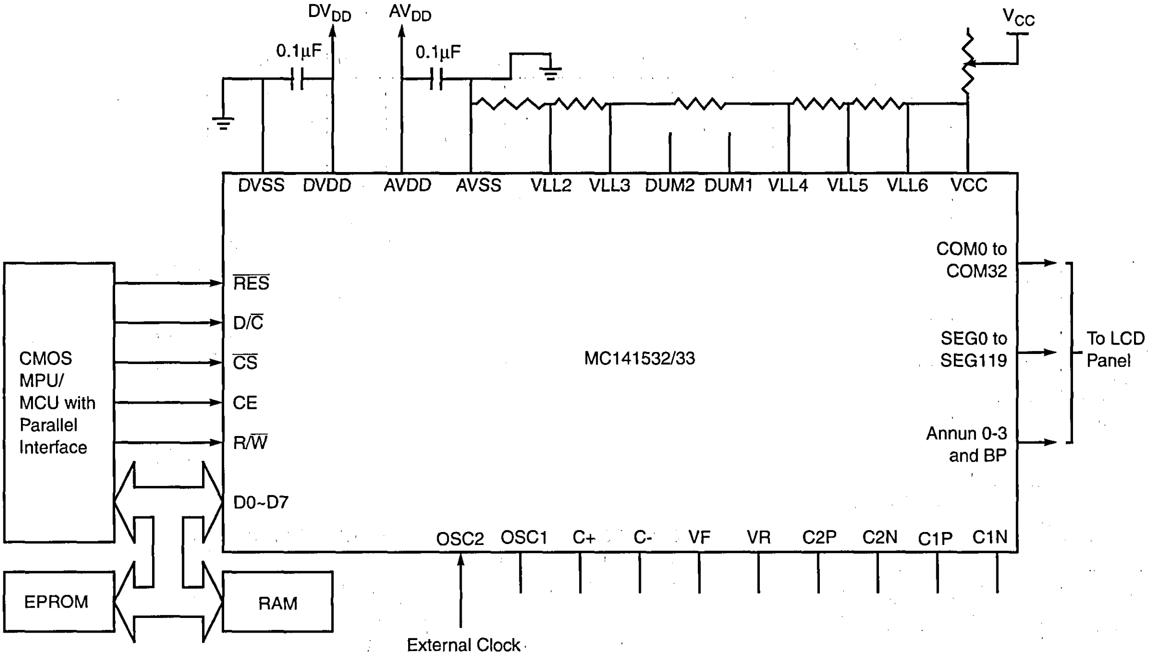
16 MUX Display with Analog Circuitry enabled, Tripler Disabled and 1/5 bias



Remark :
1. VR and VF can be left open for Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

16/32/33 MUX Display with Analog Circuitry disabled



Remark :
1. VR and VF can be left open for Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Die Pad Co-ordinate for MC141532

Pad	Name	X (µm)	Y (µm)	Pad	Name	X (µm)	Y (µm)	Pad	Name	X (µm)	Y (µm)	Pad	Name	X (µm)	Y (µm)
1	Ann0	-4803.6	-526.6	61	DVss	2472.8	-530.4	122	Seg0	3217.4	492.7	181	Seg59	-1266.6	492.7
2	Ann1	-4702.0	-526.6	62	C+	2574.4	-530.4	123	Seg1	3141.4	492.7	182	Seg60	-1342.6	492.7
3	Ann2	-4600.4	-526.6	63	DVss	2676.0	-530.4	124	Seg2	3065.4	492.7	183	Seg61	-1418.6	492.7
4	Ann3	-4498.8	-526.6	64	C-	2777.6	-530.4	125	Seg3	2989.4	492.7	184	Seg62	-1494.6	492.7
5	BP	-4397.2	-526.6	65	DVss	2879.2	-530.4	126	Seg4	2913.4	492.7	185	Seg63	-1570.6	492.7
6	DVdd	-4295.6	-526.6	66	VCC	2980.8	-530.4	127	Seg5	2837.4	492.7	186	Seg64	-1646.6	492.7
7	RES	-4194.0	-526.6	67	DVss	3082.4	-530.4	128	Seg6	2761.4	492.7	187	Seg65	-1722.6	492.7
8	DVss	-4092.4	-526.6	68	VF	3184.0	-530.4	129	Seg7	2685.4	492.7	188	Seg66	-1798.6	492.7
9	D/C	-3990.8	-526.6	69	DVss	3285.6	-530.4	130	Seg8	2609.4	492.7	189	Seg67	-1874.6	492.7
10	R/W	-3889.2	-526.6	70	VR	3387.2	-530.4	131	Seg9	2533.4	492.7	190	Seg68	-1950.6	492.7
11	CS(CLK)	-3787.6	-526.6	71	AVss	3488.8	-530.4	132	Seg10	2457.4	492.7	191	Seg69	-2026.6	492.7
12	DVss	-3686.0	-526.6	72	OSC1	3590.4	-530.4	133	Seg11	2381.4	492.7	192	Seg70	-2102.6	492.7
13	D0	-3584.4	-526.6	73	DVss	3692.0	-530.4	134	Seg12	2305.4	492.7	193	Seg71	-2178.6	492.7
14	D1	-3482.8	-526.6	74	DVss	3793.6	-530.4	135	Seg13	2229.4	492.7	194	Seg72	-2254.6	492.7
15	D2	-3381.2	-526.6	75	DVss	3869.6	-530.4	136	Seg14	2153.4	492.7	195	Seg73	-2330.6	492.7
16	D3	-3279.6	-526.6	76	DVss	3945.6	-530.4	137	Seg15	2077.4	492.7	196	Seg74	-2406.6	492.7
17	D4	-3178.0	-526.6	77	DVss	4021.6	-530.4	138	Seg16	2001.4	492.7	197	Seg75	-2482.6	492.7
18	D5	-3076.4	-526.6	78	DVss	4097.6	-530.4	139	Seg17	1925.4	492.7	198	Seg76	-2558.6	492.7
19	D6	-2974.8	-526.6	79	DVss	4173.6	-530.4	140	Seg18	1849.4	492.7	199	Seg77	-2634.6	492.7
20	D7	-2873.2	-526.6	80	DVss	4249.6	-530.4	141	Seg19	1773.4	492.7	200	Seg78	-2710.6	492.7
21	CE	-2771.6	-526.6	81	DVss	4325.6	-530.4	142	Seg20	1697.4	492.7	201	Seg79	-2786.6	492.7
22	DVss	-2670.0	-526.6	82	DVss	4401.6	-530.4	143	Seg21	1621.4	492.7	202	Seg80	-2862.6	492.7
23	DVss	-2498.3	-526.6	83	DVss	4477.6	-530.4	144	Seg22	1545.4	492.7	203	Seg81	-2938.6	492.7
24	DVss	-873.6	-591.8	84	DVss	4553.6	-530.4	145	Seg23	1469.4	492.7	204	Seg82	-3014.6	492.7
25	DVss	-797.6	-591.8	85	DVss	4629.6	-530.4	146	Seg24	1393.4	492.7	205	Seg83	-3090.6	492.7
26	DVss	-721.6	-591.8	86	Test1	4705.6	-551.0	147	Seg25	1317.4	492.7	206	Seg84	-3166.6	492.7
27	DVss	-645.6	-591.8	87	Test2	4835.2	-550.6	148	Seg26	1241.4	492.7	207	Seg85	-3242.6	492.7
28	DVss	-569.6	-591.8	88	Com32	5174.4	-484.8	149	Seg27	1165.4	492.7	208	Seg86	-3318.6	492.7
29	DVss	-493.6	-591.8	89	Com0	5174.4	-408.8	150	Seg28	1089.4	492.7	209	Seg87	-3394.6	492.7
30	DVss	-417.6	-591.8	90	Com1	5174.4	-332.8	151	Seg29	1013.4	492.7	210	Seg88	-3470.6	492.7
31	DVss	-341.6	-591.8	91	Com2	5174.4	-256.8	152	Seg30	937.4	492.7	211	Seg89	-3546.6	492.7
32	DVss	-265.6	-591.8	92	Com3	5174.4	-180.8	153	Seg31	861.4	492.7	212	Seg90	-3622.6	492.7
33	DVss	-189.6	-591.8	93	Com4	5174.4	-104.8	154	Seg32	785.4	492.7	213	Seg91	-3698.6	492.7
34	DVss	-113.6	-591.8	94	Com5	5174.4	-28.8	155	Seg33	709.4	492.7	214	Seg92	-3774.6	492.7
35	DVss	-37.6	-591.8	95	Com6	5174.4	47.2	156	Seg34	633.4	492.7	215	Seg93	-3850.6	492.7
36	DVss	38.4	-591.8	96	Com7	5174.4	123.2	157	Seg35	557.4	492.7	216	Seg94	-3926.6	492.7
37	DVss	114.4	-591.8	97	Com8	5174.4	199.2	158	Seg36	481.4	492.7	217	Seg95	-4002.6	492.7
38	DVss	190.4	-591.8	98	Com9	5174.4	275.2	159	Seg37	405.4	492.7	218	Seg96	-4078.6	492.7
39	DVss	266.4	-591.8	99	Com10	5174.4	351.2	160	Seg38	329.4	492.7	219	Seg97	-4154.6	492.7
40	DVss	342.4	-591.8	100	Com11	5174.4	427.2	161	Seg39	253.4	492.7	220	Seg98	-4230.6	492.7
41	DVss	418.4	-591.8	101	Com12	5174.4	503.2	162	Seg40	177.4	492.7	221	Seg99	-4306.6	492.7
42	DVss	494.4	-591.8	102	Com13	4771.2	492.7	163	Seg41	101.4	492.7	222	Seg100	-4382.6	492.7
43	AVdd	644.0	-530.4	103	Com14	4695.2	492.7	164	Seg42	25.4	492.7	223	Seg101	-4458.6	492.7
44	AVdd	745.6	-530.4	104	Com15	4619.2	492.7	165	Seg43	-50.6	492.7	224	Seg102	-4534.6	492.7
45	C1P	847.2	-530.4	105	Com16	4518.0	492.7	166	Seg44	-126.6	492.7	225	Seg103	-4619.2	492.7
46	C1N	948.8	-530.4	106	Com17	4442.0	492.7	167	Seg45	-202.6	492.7	226	Seg104	-4695.2	492.7
47	C2P	1050.4	-530.4	107	Com18	4366.0	492.7	168	Seg46	-278.6	492.7	227	Seg105	-4771.2	492.7
48	C2N	1152.0	-530.4	108	Com19	4290.0	492.7	169	Seg47	-354.6	492.7	228	Seg106	-5174.4	503.2
49	VLL2	1253.6	-530.4	109	Com20	4214.0	492.7	170	Seg48	-430.6	492.7	229	Seg107	-5174.4	427.2
50	VLL3	1355.2	-530.4	110	Com21	4138.0	492.7	171	Seg49	-506.6	492.7	230	Seg108	-5174.4	351.2
51	DVss	1456.8	-530.4	111	Com22	4062.0	492.7	172	Seg50	-582.6	492.7	231	Seg109	-5174.4	275.2
52	DVss	1558.4	-530.4	112	Com23	3986.0	492.7	173	Seg51	-658.6	492.7	232	Seg110	-5174.4	199.2
53	VLL4	1660.0	-530.4	113	Com24	3910.0	492.7	174	Seg52	-734.6	492.7	233	Seg111	-5174.4	123.2
54	VLL5	1761.6	-530.4	114	Com25	3834.0	492.7	175	Seg53	-810.6	492.7	234	Seg112	-5174.4	47.2
55	VLL6	1863.2	-530.4	115	Com26	3758.0	492.7	176	Seg54	-886.6	492.7	235	Seg113	-5174.4	-28.8
56	DUM1	1964.8	-530.4	116	Com27	3682.0	492.7	177	Seg55	-962.6	492.7	236	Seg114	-5174.4	-104.8
57	DVss	2066.4	-530.4	117	Com28	3606.0	492.7	178	Seg56	-1038.6	492.7	237	Seg115	-5174.4	-180.8
58	OSC2	2168.0	-530.4	118	Com29	3530.0	492.7	179	Seg57	-1114.6	492.7	238	Seg116	-5174.4	-256.8
59	DVss	2269.6	-530.4	119	Com30	3454.0	492.7	180	Seg58	-1190.6	492.7	239	Seg117	-5174.4	-332.8
60	DUM2	2371.2	-530.4	120	Com31	3378.0	492.7					240	Seg118	-5174.4	-408.8
				121	Com32	3302.0	492.7					241	Seg119	-5174.4	-484.8

Gold Bump Size

Pad	Bump Size X (µm)	Bump Size Y (µm)
1-23	66.5	66.5
24-42	49.0	39.8
43-74	66.5	66.5
75-85	49.0	66.5
86	49.0	107.0
87	No Gold Bump	
88-101	107.0	49.0
102-227	49.0	107.0
228-241	107.0	49.0

Die Size

X (µm)	Y (µm)
10881.0	1522.0

Die Pad Co-ordinate for MC141533

Pad	Name	X (µm)	Y (µm)	Pad	Name	X (µm)	Y (µm)	Pad	Name	X (µm)	Y (µm)	Pad	Name	X (µm)	Y (µm)
1	Ann0	-4803.6	-526.6	61	DVss	2472.8	-530.4	122	Seg17	3217.4	492.7	181	Seg76	-1266.6	492.7
2	Ann1	-4702.0	-526.6	62	C+	2574.4	-530.4	123	Seg18	3141.4	492.7	182	Seg77	-1342.6	492.7
3	Ann2	-4600.4	-526.6	63	DVss	2676.0	-530.4	124	Seg19	3065.4	492.7	183	Seg78	-1418.6	492.7
4	Ann3	-4498.8	-526.6	64	C-	2777.6	-530.4	125	Seg20	2989.4	492.7	184	Seg79	-1494.6	492.7
5	BP	-4397.2	-526.6	65	DVss	2879.2	-530.4	126	Seg21	2913.4	492.7	185	Seg80	-1570.6	492.7
6	DVdd	-4295.6	-526.6	66	VCC	2980.8	-530.4	127	Seg22	2837.4	492.7	186	Seg81	-1646.6	492.7
7	RES	-4194.0	-526.6	67	DVss	3082.4	-530.4	128	Seg23	2761.4	492.7	187	Seg82	-1722.6	492.7
8	DVss	-4092.4	-526.6	68	VF	3184.0	-530.4	129	Seg24	2685.4	492.7	188	Seg83	-1798.6	492.7
9	D/C	-3990.8	-526.6	69	DVss	3285.6	-530.4	130	Seg25	2609.4	492.7	189	Seg84	-1874.6	492.7
10	R/W	-3889.2	-526.6	70	VR	3387.2	-530.4	131	Seg26	2533.4	492.7	190	Seg85	-1950.6	492.7
11	CS(CLK)	-3787.6	-526.6	71	AVss	3488.8	-530.4	132	Seg27	2457.4	492.7	191	Seg86	-2026.6	492.7
12	DVss	-3686.0	-526.6	72	OSC1	3590.4	-530.4	133	Seg28	2381.4	492.7	192	Seg87	-2102.6	492.7
13	D0	-3584.4	-526.6	73	DVss	3692.0	-530.4	134	Seg29	2305.4	492.7	193	Seg88	-2178.6	492.7
14	D1	-3482.8	-526.6	74	DVss	3793.6	-530.4	135	Seg30	2229.4	492.7	194	Seg89	-2254.6	492.7
15	D2	-3381.2	-526.6	75	DVss	3869.6	-530.4	136	Seg31	2153.4	492.7	195	Seg90	-2330.6	492.7
16	D3	-3279.6	-526.6	76	DVss	3945.6	-530.4	137	Seg32	2077.4	492.7	196	Seg91	-2406.6	492.7
17	D4	-3178.0	-526.6	77	DVss	4021.6	-530.4	138	Seg33	2001.4	492.7	197	Seg92	-2482.6	492.7
18	D5	-3076.4	-526.6	78	DVss	4097.6	-530.4	139	Seg34	1925.4	492.7	198	Seg93	-2558.6	492.7
19	D6	-2974.8	-526.6	79	DVss	4173.6	-530.4	140	Seg35	1849.4	492.7	199	Seg94	-2634.6	492.7
20	D7	-2873.2	-526.6	80	DVss	4249.6	-530.4	141	Seg36	1773.4	492.7	200	Seg95	-2710.6	492.7
21	CE	-2771.6	-526.6	81	DVss	4325.6	-530.4	142	Seg37	1697.4	492.7	201	Seg96	-2786.6	492.7
22	DVss	-2670.0	-526.6	82	DVss	4401.6	-530.4	143	Seg38	1621.4	492.7	202	Seg97	-2862.6	492.7
23	DVss	-2498.3	-526.6	83	DVss	4477.6	-530.4	144	Seg39	1545.4	492.7	203	Seg98	-2938.6	492.7
24	DVss	-873.6	-591.8	84	DVss	4553.6	-530.4	145	Seg40	1469.4	492.7	204	Seg99	-3014.6	492.7
25	DVss	-797.6	-591.8	85	DVss	4629.6	-530.4	146	Seg41	1393.4	492.7	205	Seg100	-3090.6	492.7
26	DVss	-721.6	-591.8	86	Test2	4705.6	-551.0	147	Seg42	1317.4	492.7	206	Seg101	-3166.6	492.7
27	DVss	-645.6	-591.8	87	Test1	4835.2	-550.6	148	Seg43	1241.4	492.7	207	Seg102	-3242.6	492.7
28	DVss	-569.6	-591.8	88	Com32	5174.4	-484.8	149	Seg44	1165.4	492.7	208	Seg103	-3318.6	492.7
29	DVss	-493.6	-591.8	89	Com0	5174.4	-408.8	150	Seg45	1089.4	492.7	209	Seg104	-3394.6	492.7
30	DVss	-417.6	-591.8	90	Com1	5174.4	-332.8	151	Seg46	1013.4	492.7	210	Seg105	-3470.6	492.7
31	DVss	-341.6	-591.8	91	Com2	5174.4	-256.8	152	Seg47	937.4	492.7	211	Seg106	-3546.6	492.7
32	DVss	-265.6	-591.8	92	Com3	5174.4	-180.8	153	Seg48	861.4	492.7	212	Seg107	-3622.6	492.7
33	DVss	-189.6	-591.8	93	Com4	5174.4	-104.8	154	Seg49	785.4	492.7	213	Seg108	-3698.6	492.7
34	DVss	-113.6	-591.8	94	Com5	5174.4	-28.8	155	Seg50	709.4	492.7	214	Seg109	-3774.6	492.7
35	DVss	-37.6	-591.8	95	Com6	5174.4	47.2	156	Seg51	633.4	492.7	215	Seg110	-3850.6	492.7
36	DVss	38.4	-591.8	96	Com7	5174.4	123.2	157	Seg52	557.4	492.7	216	Seg111	-3926.6	492.7
37	DVss	114.4	-591.8	97	Com8	5174.4	199.2	158	Seg53	481.4	492.7	217	Seg112	-4002.6	492.7
38	DVss	190.4	-591.8	98	Com9	5174.4	275.2	159	Seg54	405.4	492.7	218	Seg113	-4078.6	492.7
39	DVss	266.4	-591.8	99	Com10	5174.4	351.2	160	Seg55	329.4	492.7	219	Seg114	-4154.6	492.7
40	DVss	342.4	-591.8	100	Com11	5174.4	427.2	161	Seg56	253.4	492.7	220	Seg115	-4230.6	492.7
41	DVss	418.4	-591.8	101	Com12	5174.4	503.2	162	Seg57	177.4	492.7	221	Seg116	-4306.6	492.7
42	DVss	494.4	-591.8	102	Com13	4771.2	492.7	163	Seg58	101.4	492.7	222	Seg117	-4382.6	492.7
43	AVdd	644.0	-530.4	103	Com14	4695.2	492.7	164	Seg59	25.4	492.7	223	Seg118	-4458.6	492.7
44	AVdd	745.6	-530.4	104	Com15	4619.2	492.7	165	Seg60	-50.6	492.7	224	Seg119	-4534.6	492.7
45	C1P	847.2	-530.4	105	Seg0	4518.0	492.7	166	Seg61	-126.6	492.7	225	Com32	-4619.2	492.7
46	C1N	948.8	-530.4	106	Seg1	4442.0	492.7	167	Seg62	-202.6	492.7	226	Com31	-4695.2	492.7
47	C2P	1050.4	-530.4	107	Seg2	4366.0	492.7	168	Seg63	-278.6	492.7	227	Com30	-4771.2	492.7
48	C2N	1152.0	-530.4	108	Seg3	4290.0	492.7	169	Seg64	-354.6	492.7	228	Com29	-5174.4	503.2
49	VLL2	1253.6	-530.4	109	Seg4	4214.0	492.7	170	Seg65	-430.6	492.7	229	Com28	-5174.4	427.2
50	VLL3	1355.2	-530.4	110	Seg5	4138.0	492.7	171	Seg66	-506.6	492.7	230	Com27	-5174.4	351.2
51	DVss	1456.8	-530.4	111	Seg6	4062.0	492.7	172	Seg67	-582.6	492.7	231	Com26	-5174.4	275.2
52	DVss	1558.4	-530.4	112	Seg7	3986.0	492.7	173	Seg68	-658.6	492.7	232	Com25	-5174.4	199.2
53	VLL4	1660.0	-530.4	113	Seg8	3910.0	492.7	174	Seg69	-734.6	492.7	233	Com24	-5174.4	123.2
54	VLL5	1761.6	-530.4	114	Seg9	3834.0	492.7	175	Seg70	-810.6	492.7	234	Com23	-5174.4	47.2
55	VLL6	1863.2	-530.4	115	Seg10	3758.0	492.7	176	Seg71	-886.6	492.7	235	Com22	-5174.4	-28.8
56	DUM1	1964.8	-530.4	116	Seg11	3682.0	492.7	177	Seg72	-962.6	492.7	236	Com21	-5174.4	-104.8
57	DVss	2066.4	-530.4	117	Seg12	3606.0	492.7	178	Seg73	-1038.6	492.7	237	Com20	-5174.4	-180.8
58	OSC2	2168.0	-530.4	118	Seg13	3530.0	492.7	179	Seg74	-1114.6	492.7	238	Com19	-5174.4	-256.8
59	DVss	2269.6	-530.4	119	Seg14	3454.0	492.7	180	Seg75	-1190.6	492.7	239	Com18	-5174.4	-332.8
60	DUM2	2371.2	-530.4	120	Seg15	3378.0	492.7					240	Com17	-5174.4	-408.8
				121	Seg16	3302.0	492.7					241	Com16	-5174.4	-484.8

Gold Bump Size

Pad	Bump Size X (µm)	Bump Size Y (µm)
1-23	66.5	66.5
24-42	49.0	39.8
43-74	66.5	66.5
75-85	49.0	66.5
86	49.0	107.0
87	No Gold Bump	
88-101	107.0	49.0
102-227	49.0	107.0
228-241	107.0	49.0

Die Size

X (µm)	Y (µm)
10881.0	1522.0

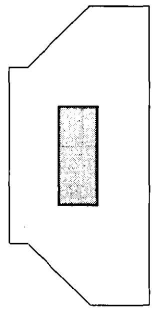
MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

MC141535

LCD Segment / Common Driver
CMOS

MC141535 is a CMOS LCD Driver which consists of 4 annunciator outputs and 178 high voltage LCD driving signals (17 rows and 161 segments). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuit so that limited external components are required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 Bit Parallel Interface
- Graphic Mode Operation
- On Chip Graphic Display Data RAM
- Four Static Annunciator (Icon) Drivers
- Low Power Icon Mode Driven by Com16 in Special Driving Scheme
- 161 Segment Drivers, 17 Row Drivers
- 1:5 Bias Ratio
- 1/17 Multiplex Ratio
- Master Clear RAM (Main Dot Matrix Display / Icons Display)
- Vertical and Horizontal Scrolling for Main Display
- Re-mapping of Row and Column Drivers
- Selectable LCD Driving Voltage Temperature Compensation
- 16 Level Internal Contrast Control
- External Contrast Control
- Standard TAB



TAB

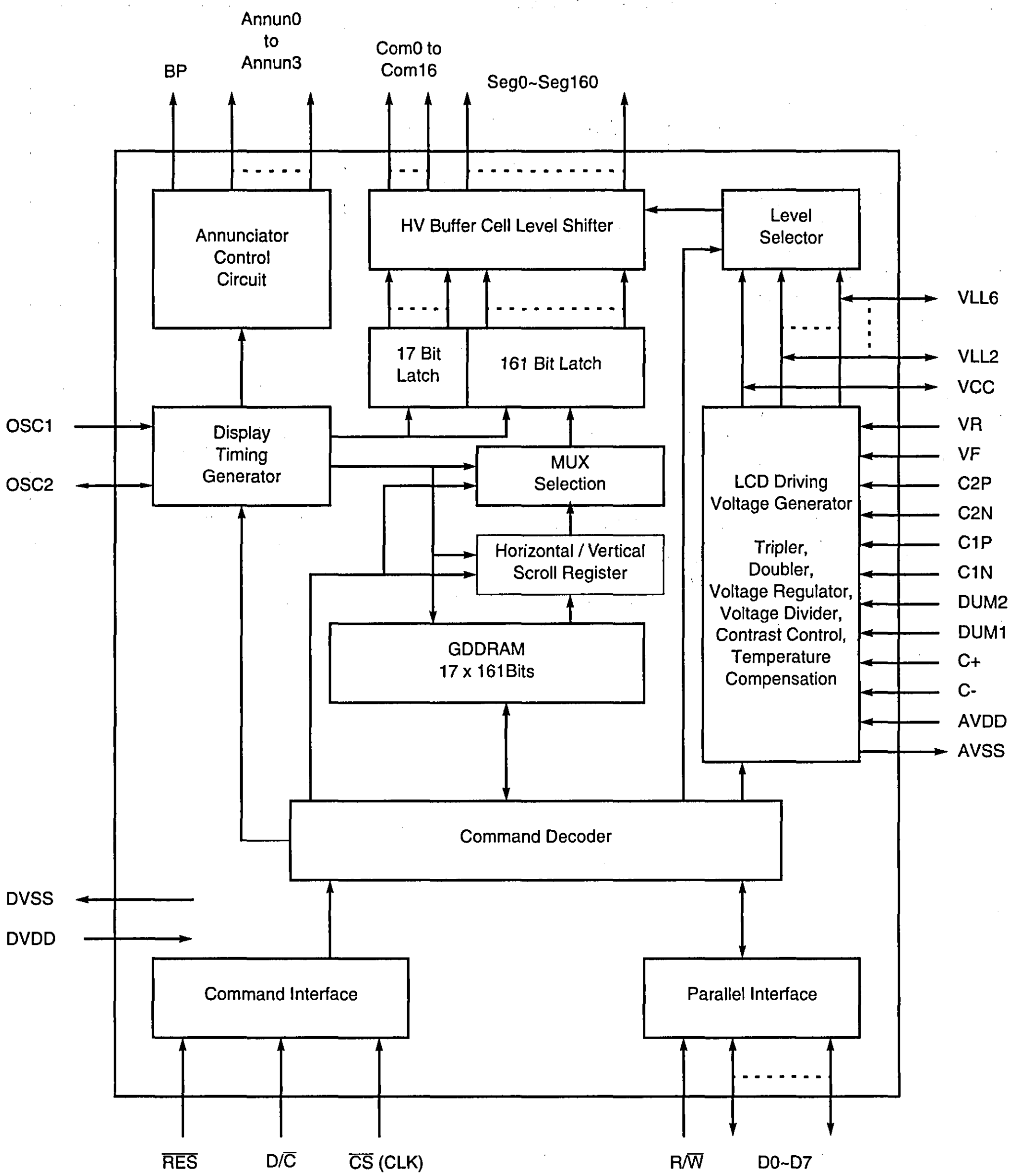
Gold Bump Die

ORDERING INFORMATION

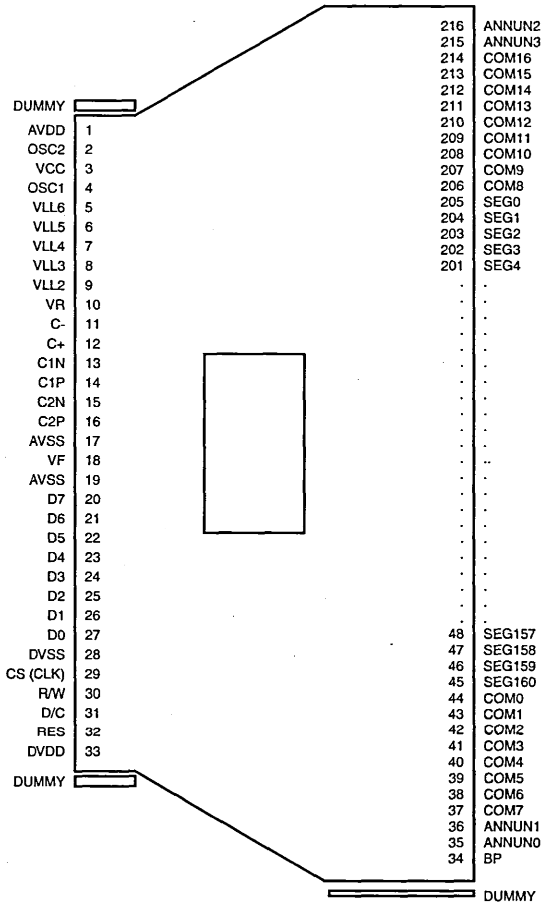
MC141535T	TAB
MCC141535Z	Gold Bump Die

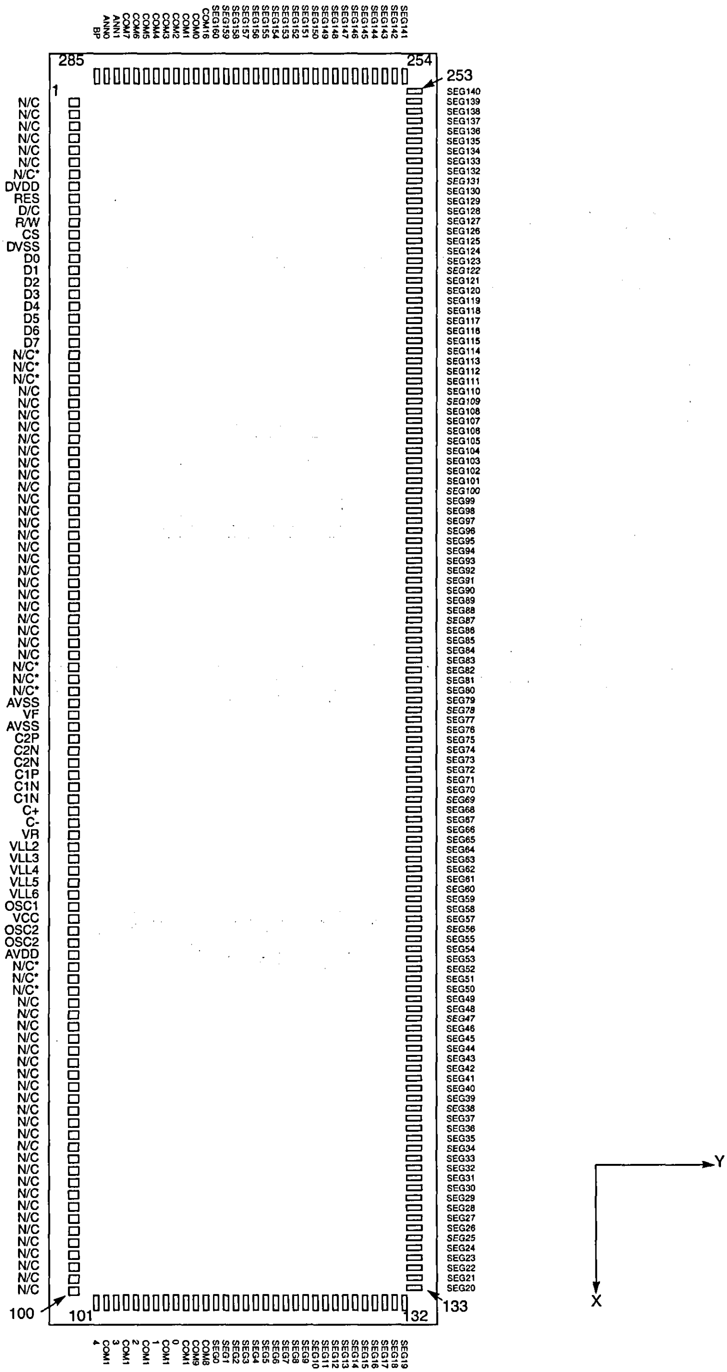
REV 4
3/97

Block Diagram



MC141535T PIN ASSIGNMENT
(COPPER VIEW)





MC141535 Die Pad Assignment

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
 T_{A1} T_{A2}	Operating Temperature For Using Internal Oscillator For Using External Oscillator	 -25 to +85 -30 to +85	 ˚C ˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
$V_{SS} = AV_{SS} = DV_{SS}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analogue Circuit)
$V_{DD} = AV_{DD} = DV_{DD}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analogue Circuit)

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Supply voltage (Absolute value Referenced to V_{SS})					
DV_{DD}	Operating Range of Logic Circuit Supply DV_{DD}		2.4	3.0	3.5	V
AV_{DD}	Operating Range of Voltage Generator Circuit Supply AV_{DD}		2.4	-	3.5	V
	Supply Current (Measure with V_{DD} fixed at 3.0V)					
I_{AC}	Access Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Accessing, T_{cyc}=1MHz, Osc. Freq. =38.4kHz, 1/17 Duty Cycle,1/7 Bias.	0	200	300	µA
I_{DP1}	Display Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Normal Display Mode, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz.	0	70	100	µA
I_{DP2}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Normal Display Mode, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz. Horizontal Scrolling	0	78	110	µA
I_{ICON}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Icon Display Mode, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz.	-	15	30	µA
I_{SB1}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD	Display Off, Oscillator Disabled, R/W Halt	0	300	500	nA
I_{SB2}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, External Oscillator and Frequency = 38.4kHz.	0	2.5	5	µA
I_{SB3}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 38.4kHz.	0	5	7	µA
	VLCD Voltage					
V_{CC1}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Tripler Enable, Osc. Freq. = 38.4kHz, Regulator Enabled, Divider Enabled	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Doubler Enable, Osc. Freq. = 38.4kHz, Regulator Enabled, Divider Enabled	-	2*AV_{DD}	10.5	V
V_{LCD}	LCD Driving Voltage input at pin V_{CC}.	Internal DC/DC Converter Disabled.	AV_{DD}	-	10.5	V
	Output Voltage					
V_{OH1}	Output High Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{R1}	LCD Driving Voltage Source at Pin VR	Regulator Enabled	0	-	V_{CC}-0.5	V
V_{R2}	LCD Driving Voltage Source at Pin VR	Regulator Disabled	-	0	-	V
V_{R3}	Delta of VR Voltage Drop	Regulator Enabled, I_{out}=50µA	0	-	VCC	V
ΔV_R	Variation of V_R Input (V_{DD} is fixed)	Regulator Enabled	-	±1	±2.5	%

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Input Voltage					
V_{IH1}	Input High Voltage at Pins, $\overline{RES}$, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/C, OSC1 and OSC2.		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage at Pins, $\overline{RES}$, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/C, OSC1 and OSC2.		0	-	0.2*V_{DD}	V
	LCD Display Voltage. (LCD Driving Voltage Output from Pins VLL6, VLL5, VLL4, VLL3 and VLL2.)	Voltage Driver Enabled, Regulator Enabled.				
V_{LL6}			-	V_R	-	V
V_{LL5}			-	0.8*V_R	-	V
V_{LL4}			-	0.6*V_R	-	V
V_{LL3}			-	0.4*V_R	-	V
V_{LL2}			-	0.2*V_R	-	V
V_{LL6}		External Voltage Generator, Voltage Divider Disable, Regulator Enabled.	1/2V_{CC}	-	V_{CC}	V
V_{LL5}			1/2V_{CC}	-	V_{CC}	V
V_{LL4}			1/2V_{CC}	-	V_{CC}	V
V_{LL3}			0	-	1/2V_{CC}	V
V_{LL2}			0	-	1/2V_{CC}	V
	Output Current					
I_{OH}	Output High Current Source from Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=VDD-0.4V	50	-	-	μA
I_{OL}	Output Low Current Drain from Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=0.4V	-	-	-50	μA
I_{OZ}	Output Tri-state Current Drain Source at pins D0-D7 and OSC2		-1	-	1	μA
I_{IL}/I_{IH}	Input Current at pins $\overline{RES}$, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$ OSC1 and OSC2.		-1	-	1	μA
Ron	On Resistance Channel Resistance between LCD Driving Signal Pins (SEG and COM) and Driving Voltage Input Pins (V_{LL2} to V_{LL6}).	During Display on, 0.1V Apply between Two Terminals, V_{CC} within Operating Voltage Range.	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD}) Standby Mode, Retained All Internal Configuration and RAM Data		2	-	3.5	V
C_{IN}	Input Capacitance OSC1, OSC2 and All Logic Pins		-	5	7.5	pF

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, DV_{DD}=2.4-3.15V, T_A=25°C)

	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled.	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled.	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled.	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled.	-	-0.35	-	%

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{\text{VR at } 50^\circ C - \text{VR at } 0^\circ C}{50^\circ C - 0^\circ C} \times \frac{1}{\text{VR at } 25^\circ C} \times 100\%$$

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, AV_{DD}=DV_{DD}=2.4 to 3.15V, T_A=25°C)

Total variation of VR ΔV_{RT} is affected by the following factors :

Process variation of Regulator ΔV_R

External V_{DD} Variation contributed to Regulator ΔV_{VDD}

External resistor pair Ra/Rf contributed to Regulator ΔV_{res}

where $\Delta V_{RT} = \sqrt{(\Delta V_R)^2 + (\Delta V_{V_{DD}})^2 + (\Delta V_{res})^2}$

Assume external V_{DD} variation is +/-6% at 3.15V and 1% variation resistor used at application.

	TC Level	ΔV_{VDD} (%)	ΔV_R (%)	ΔV_{res} (%)	ΔV_{RT} (%)
Reference Generator	TC0	±6.0	±2.5	±1.414	±6.652
	TC1	±4.0			±4.924
	TC2	±2.5			±3.805
	TC3	±1.4			±3.195

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, V_{DD}=2.4 to 3.15V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Oscillation Frequency.	Normal Display Frequency Selected				
F_{OSC1}	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	38.4	-	kHz
F_{ANN1}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	18.75	-	Hz
F_{FRM1}	LCD Driving Signal Frame Frequency.	Graphic or Icon Display Mode.	-	60	-	Hz
	Oscillation Frequency.	Slow Display Frequency Selected				
F_{ANN2}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP With Low Display Frequency Enabled		-	9.375	-	Hz
F_{FRM2}	LCD driving Signal Frame Frequency. (Graphic or Icon Display Mode With Low Display Frequency Enabled.)		-	30	-	Hz
OSC	Internal Oscillation Frequency Internal OSC Oscillation Frequency with Different Value of Feedback Resistor. (Internal Oscillator Enabled. V_{DD} within Operation Range.)		See Figure 1 for the relationship			

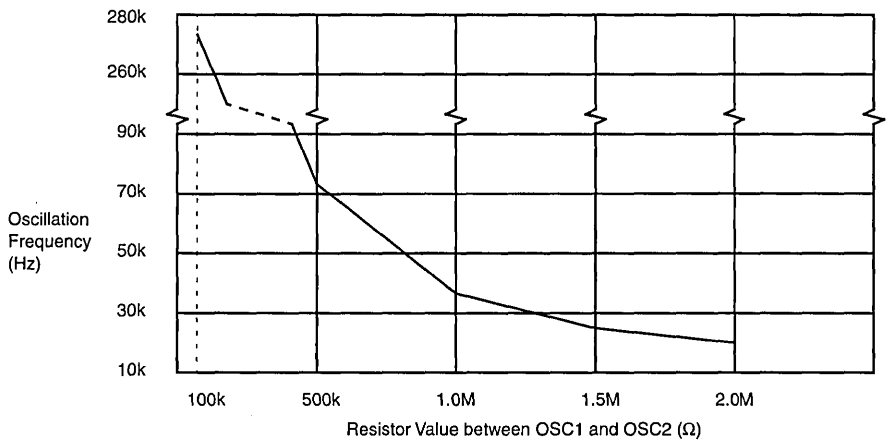


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

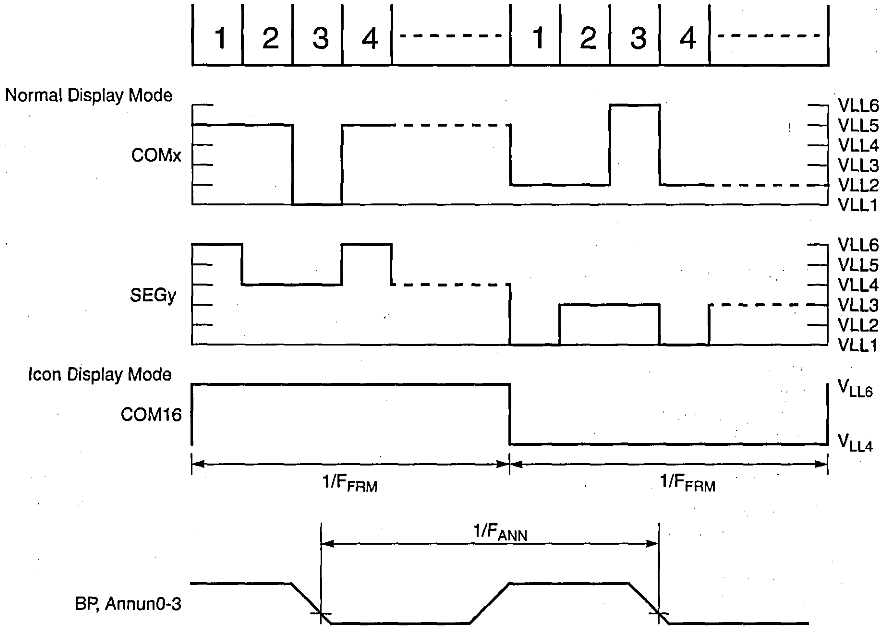


Figure 2. LCD Driving Signal Timing Diagram

TABLE 2a. Parallel Timing Characteristics (Write Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DS}	Data Setup Time	290	-	-	ns
t_{DH}	Data Hold Time	0	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

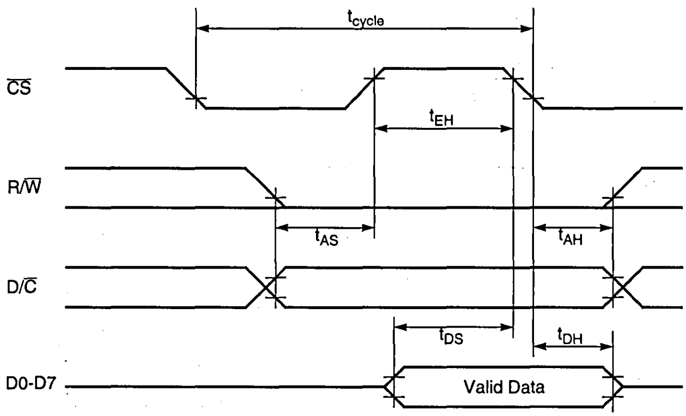


Figure 3. Timing Characteristics (Write Cycle)

TABLE 2b. Parallel Timing Characteristics (Read Cycle) (T_A=-10 to 60°C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	375	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DD}	Data Setup Time	-	-	350	ns
t_{DH}	Data Hold Time	7	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

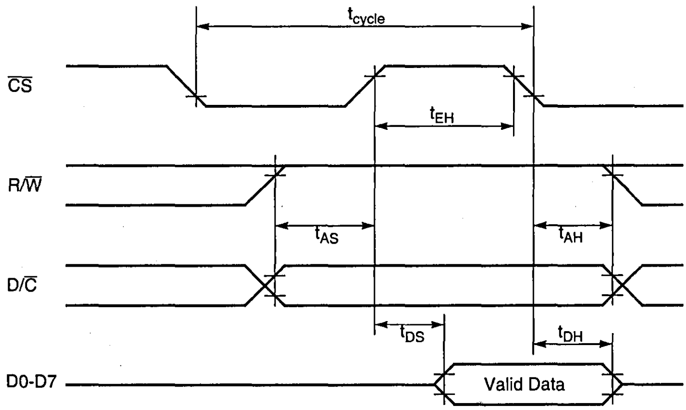


Figure 4. Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)
This input pin tell the LCD driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Chip Select / Input Clock)
This pin is normal Low clock input. Data on D0-D7 is latched at the falling edge of $\overline{CS}$.

$\overline{RES}$ (Reset)
An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

D0-D7 (Data)
This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read / Write)
This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/$\overline{W}$ input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)
For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value should be connected between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)
For internal oscillator mode, this is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2
Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit if internal divider is enable. For Internal DC/DC Converter enabled, a 0.1 µF capacitor to AV_{SS} is required on each pin.

C1N and C1P
If Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required to connect these two pins.

C2N and C2P
If Internal DC/DC Converter and Tripler are enabled, a 0.1 µF capacitor is required between these two pins. Otherwise, leave these pins open.

C+ and C-
If internal divider circuit is enabled, a 0.1 µF capacitor is required to connect between these two pins.

VR and VF
This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 µF capacitor placed between VR and AVSS. (Refer to the Application Circuit)

COM0-COM16 (Row Drivers)
These pins provide the row driving signal to LCD panel. Com0-Com15 are used in 16 mux display. Com16 is used to drive the non-static icons. Output is low during display off.

SEG0-SEG160 (Column Drivers)
These 161 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)
This pin combines with Annun0-Annun3 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANNn} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun3 (Annunciator Frontplanes)
These pins are four independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANNn} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When all annunciators are disabled, all these pins output 0V.

AVDD and AVSS
AVDD is the positive supply to LCD bias voltage generator. AVSS is ground.

VCC
For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS
Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (161x17 = 2737 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

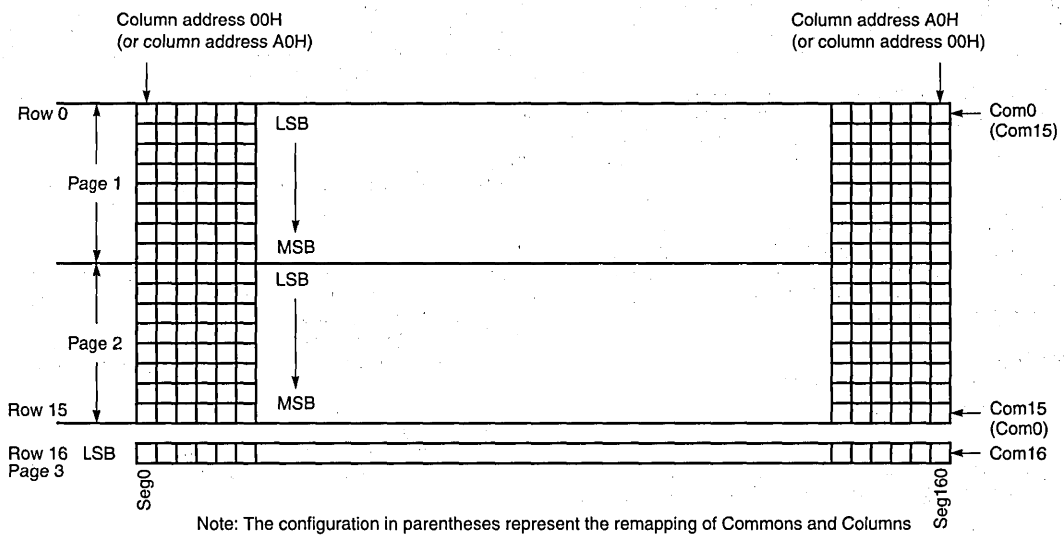


Figure 5. Graphic Display Data RAM (GDDRAM) Address Map

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15kHz to 50kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 4 annunciators and BP are generated by this module. The 4 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit. Before turning the annunciators on, the oscillator must be on in advance. Annunciator output waveform shown in Figure 7.

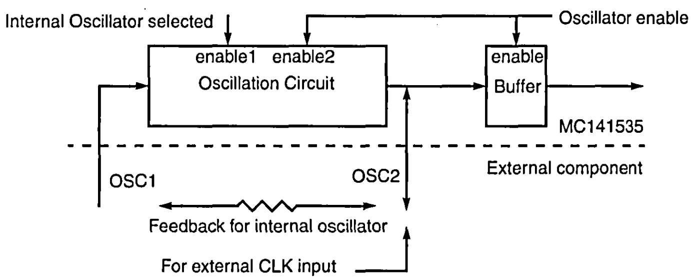


Figure 6. Oscillator Circuitry

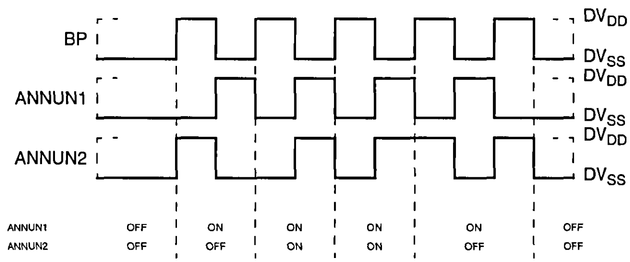


Figure 7. Annunciators and BP Display Waveform

LCD Driving Voltage Generator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. it can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.

All blocks can be individually turned off if external voltage generator is employed.

Voltage Regulator

1. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
2. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.

17 Bit Latch / 161 Bit Latch

A 178 bit long register which carrys the display signal information. First 32 bits are Common driving signals and other 161 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shift-er)

HV Buffer Cell works as a level shift-er which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Horizontal Shifter

This Horizontal Shifter shift the 16 rows of GDDRAM data horizontally according to the value in the Horizontal Scroll register (which is programmable through sending two commands consecutively). Such Horizontal Shifter's output will go to the 161 Bit Latch for display.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a, 8b and 8c illustrate the desired multiplex scheme.

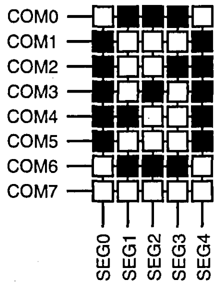


Figure 8a. LCD Display Example "0"

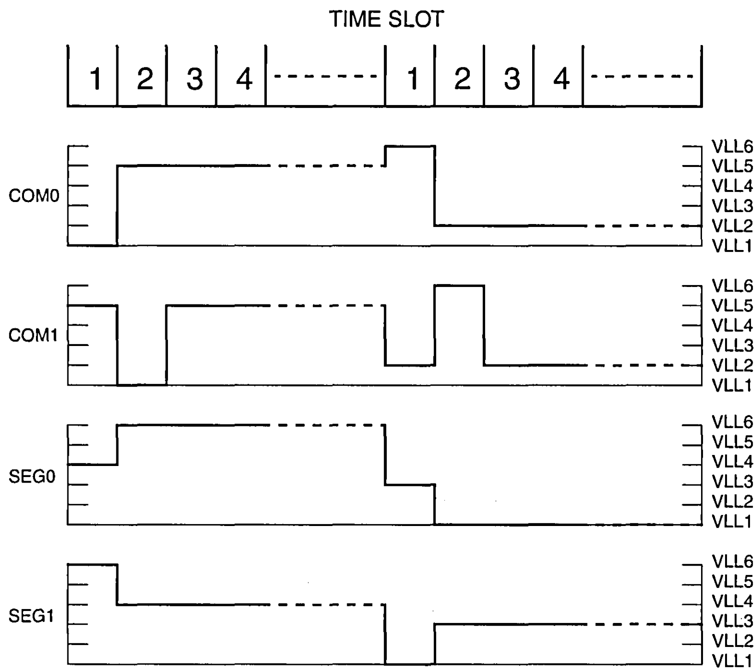


Figure 8b. LCD Driving Signal from MC141535

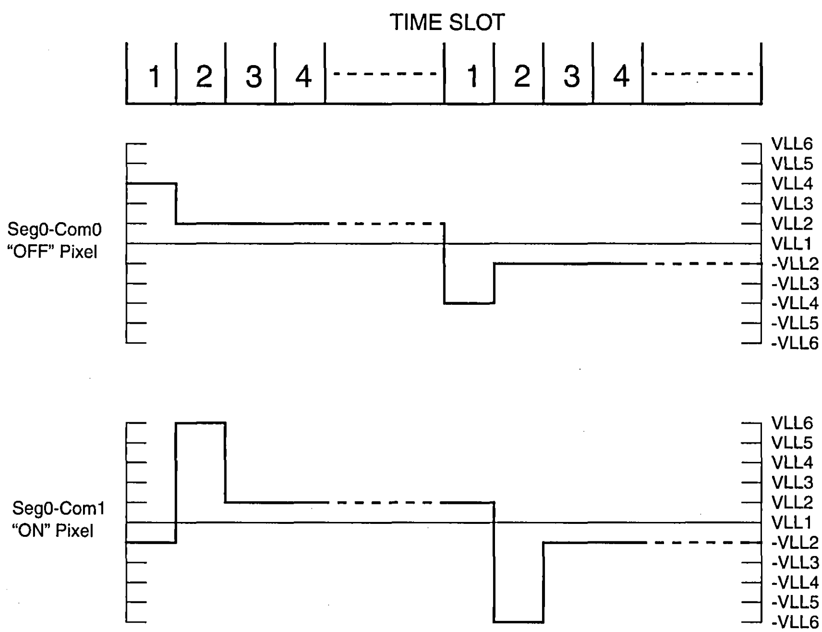


Figure 8c. Effective LCD waveform on LCD pixel

Command Description

Set Display On/Off (Display Mode / Stand-by Mode)

This Display On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command starts the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : "Oscillator On" command should be sent before "Display On" is selected)

The Display Off command turns the display off and the states of the LCD driver are as follow during display off :

1. The Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by this command. The Oscillator is not affected by this command either.

Set Horizontal Scroll

This command is used in combination with "Set Horizontal Scroll Value" to set the LCD driver to scroll the display horizontally. The next input from D0 to D7 is the scroll value. Note that Row16 is not affected by this command.

Set Horizontal Scroll Value

When display is turned on, this command maps the selected GDDRAM column (00H-A0H) to Seg0-Seg160. With scroll value equals to 0, Col 0 of GDDRAM is mapped to Seg0 and Col 1 through Col 160 are mapped to Seg 1 through Seg160 respectively. With Scroll value equals to 1, Col 1 of GDDRAM is mapped to Seg 0, then Col 2 through Col 160 will be mapped to Seg 1 through Seg 159 respectively and Col 0 will be mapped to Seg 160. This command must issue follow command "Set Horizontal Scroll".

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-A0H (161 columns) in combination with the command "Set MSB of GDDRAM Column Address". The column address will be increased automatically after a read or write operation. Refer "Address Increment Table" and command "Set GDDRAM Page Address" for further information.

Set MSB of GDDRAM Column Address

This command set the MSB of the GDDRAM Column address pointer. Set this MSB to 0 for accessing the 00H-7FH address; while set this MSB to 1 for accessing 80H-A0H address

Set GDDRAM Page Address

This command positions the row address to 1 of 3 possible positions in GDDRAM. Refer to figure 5.

Master Clear GDDRAM

This command is to clear the content of page 1 and 2 of the Display Data RAM. Issue this command followed by a dummy write command.

Master Clear Icons

This command is used to clear the data in page 3 of GDDRAM which storing the icon line data. Before using this command, set the page address to page 3 by the command "Set GDDRAM Page Address". A dummy write data operation is also needed after this "Master Clear Icons" command to make the clear icon action effective.

Set Display Mode

This command switch the driver to full display mode or icon display mode. In low power icon mode, only icons (driven by COM16) and annunciators are displayed.

Set Vertical Scroll Value

This command maps the selected GDDRAM row (00H-0FH) to Com0. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 15 are mapped to Com1 through Com15 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 15 will be mapped to Com1 through Com14 respectively and Row 0 will be mapped to Com15.

Save / Restore Column Address

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 160 of GDDRAM mapped to Seg0-Seg160 respectively;
2. Column 0 - Column 160 of GDDRAM mapped to Seg160-Seg0 respectively.

Detail information please refer to section "Display Output Description".

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 15 of GDDRAM to Com0 - Com15 respectively;
2. Row 0 - Row 15 of GDDRAM to Com15 - Com0 respectively.

Output of Row 16 (Com16) will not be changed by this command. See section "Display Output Description" for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 4 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on or off the oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command "Set Display On/Off" and "Set Annunciator Control Signals". See command "Set External / Internal Oscillator" for more information

Set External / Internal Oscillator

This command is used to select either internal or external oscillator. When Internal Oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Internal DC/DC Converter On/Off

Use this command selects the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Turn off the Internal DC/DC Converter if external Vcc is provided.

Set Voltage Doubler / Tripler

Use this command to select Doubler or Tripler when the Internal DC/DC Converter is on.

Set Internal Regulator On/Off

Choose bit option 0 to disable the Internal Regulator. Choose bit option 1 to enables the Internal Regulator which consists of the internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is disabled, external bias can be used for V_{LL6} to V_{LL2}. If the Internal Voltage Divider is enabled, the internal circuit will generated the 1:5 bias driving voltage.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from the lowest value after POR.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use. After power-on reset, the contrast level is the lowest.

Read Contrast Value

This command allows the user to read the current contrast level value. With $R/\overline{W}$ input high (READ), $D/\overline{C}$ input low (COMMAND) and D7 D6 D5 D4 are equal to 0 0 0 1, the value of the internal contrast value can be read on D0-D3 at the falling edge of CS.

Set Temperature Coefficient

A temperature gradient selector circuit controlled by two control bits TC1 and TC2. This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

Set Display Frequency

This command set the LCD panel display to normal frequency or slow frequency.

COMMAND TABLE

Bit Pattern	Command	Comment
$000000X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X_1X_0 as address bits. X_1X_0=00 : page 1 (POR) X_1X_0=01 : page 2 X_1X_0=10 : page 3
$0001X_3X_2X_1X_0$	Set / Read Contrast Level	With $R/\overline{W}$ pin input low, set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR. With $R/\overline{W}$ pin input high, and at the rising edge of $\overline{CS}$, the value of the internal contrast register will be latched out at D3 D2 D1 D0 pins, i.e. $X_3X_2X_1X_0$, at the rising edge of $\overline{CS}$.
$0010000X_0$	Set Voltage Doubler / Tripler	X_0=0: Tripler enable (POR) X_0=1: Doubler enable
$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg160
$0010010X_0$	Set Row Mapping	X_0=0 : Row0 to Com0 X_0=1: Row0 to Com15
$0010011X_0$	Set MSB of GDDRAM Column Address	X_0=0 : MSB = 0 (POR) X_0=1 : MSB = 1
$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
$0010101X_0$	Set Internal DC/DC Converter On/Off	X_0=0: Internal DC/DC Converter off(POR) X_0=1: Internal DC/DC Converter on
$0010110X_0$	Set Internal Regulator Enable	X_0=0: Internal Regulator off (POR) X_0=1: Internal Regulator on When application uses a supply with built-in temperature compensation, the regulator should be disabled .
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: Internal Voltage Divider off(POR) X_0=1: Internal Voltage Divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal Contrast Control off(POR) X_0=1: Internal Contrast Control on Internal contrast circuits can be disabled if external contrast circuits is preferred.

COMMAND TABLE

Bit Pattern	Command	Comment
$0011001X_0$	Set Display Mode	X_0=0 : normal display mode (POR) X_0=1 : icon display mode
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
00110110	Master Clear GDDRAM	Master clear page 1 and 2 of GDDRAM, dummy write is required after this command.
00110111	Master Clear Icons	Master Clear of GDDRAM page 3. GDDRAM page 3 should be selected and dummy write is required
$0011100X_0$	Set Display Frequency	X_0=0: normal display frequency X_0=1: slow display mode
$0011101X_0$	Reserved.	X_0=0: normal operation (POR) X_0=1: test mode (Note: Make sure to set X_0=0 during application)
$0100X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_3X_2X_1X_0$ as number of lines to scroll. Scroll value = 0 upon POR
$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 1 (POR) A_1A_0=01: select annunciator 2 A_1A_0=10: select annunciator 3 A_1A_0=11: select annunciator 4 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on
01101000	Set Horizontal Scrolling	Set horizontal scrolling mode. The next input from D0~D7 will be interpreted as the horizontal shift value.
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=01: -0.18% X_1X_0=10: -0.22% X_1X_0=11: -0.35%
$0111000X_0$	Increase / Decrease Contrast Value	X_0=0: Decrease by one level X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.
$0111001X_0$	Reserved	
$0111010X_0$	Reserved	
$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Make sure to set X_0=0 during application)
$0111100X_0$	Reserved	
$0111101X_0$	Set External / Internal Oscillator	X_0=0: External oscillator (POR) X_0=1: Internal oscillator. For internal oscillator place a resistor between OSC1 and OSC2. For external oscillator mode, feed clock input to OSC2.
$0111110X_0$	Reserved	
$0111111X_0$	Set Oscillator Enable / Disable	X_0=0: oscillator master disable (POR) X_0=1: oscillator master enable. This is the master control fro oscillator circuitry. This command should be issued after the "External / Internal Oscillator" command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.
$X_7X_6X_5X_4X_3X_2X_1X_0$	Set Horizontal Scroll Value	To set the amount of Horizontal scroll

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$ pin and D/$\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to R/$\overline{W}$ pin and High to D/$\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the "Commands Required for R/W Actions on RAM" Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.

Remarks : *1. Refer to the command "Read Contrast Value".
*2. If write data is issued after Command Clear RAM, Address increase is not applied.
*3. Column Address will be wrapped round when overflow.

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Normal Display Mode	Set External / Internal Oscillator Set Oscillator Enable, Set Display Mode (Normal Display) Set Display On.	$(0111101X_0)^*$ (01111111)* (00110010)* (00101001)*
Icon Display Mode	Set External / Internal Oscillator Set Oscillator Enable, Set Display Mode (Icon Display) Set Display On.	$(0111101X_0)^*$ (01111111)* (00110011)* (00101001)*
Annunciator Display	Set External / Internal Oscillator Set Oscillator Enable, Set Annunciator On/Off.	$(0111101X_0)^*$ (01111111)* $(01100A_1A_0X_0)^*$
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator Set Display Off, Set Oscillator Enable. Set Annunciator On / Off,	(01111011)* (00101000)* (01111111)* $(01100A_1A_0X_0)^*$
Standby Mode 3.	Set Internal Oscillator Set Display Off, Set Oscillator Enable. Set Annunciator On / Off,	(01111010)* (00101000)* (01111111)* $(01100A_1A_0X_0)^*$

Other Related Command with Display Mode : Set Segment Mapping, Set Common Mapping, Set Vertical Scroll Value.
Commands Related to Voltage Generator :
Set Oscillator Enable / Disable, Set Internal Regulator On/Off, Set Temperature Coefficient, Set Internal Contrast Control On/Off, Increase / Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Display On/Off, Set Reference Voltage Generator, Set Contrast Level, Set Voltage Doubler / Tripler

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set MSB of GDDRAM Column Address Set GDDRAM Column Address Read/Write Data	$(000000X_1X_0)$* $(0010011X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	$(0011010X_0)$
Increase GDDRAM Address.	Dummy Read Data Set GDDRAM Column Address	$(X_7X_6X_5X_4X_3X_2X_1X_0)$ $(1X_6X_5X_4X_3X_2X_1X_0)$
Master Clear GDDRAM	Master Clear GDDRAM Dummy Write Data	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Master Clear Icons	Set Clear Page 3 of GDDRAM Master Clear Icons Dummy Write Data	(00000010)* (00110111) $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Horizontal Scrolling with Writing GDDRAM	Set GDDRAM Page 1 Set MSB of GDDRAM Column Address Set GDDRAM Column Address Write Data Set GDDRAM Page 1 Set MSB of GDDRAM Column Address Set GDDRAM Column Address Write Data Set Horizontal Scroll Set Scroll Value	(00000000)* $(0010011X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$ (00000001)* $(0010011X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$ (01101000) (00000001)

* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed.

Display Output Description by Working Example

This is an example of output pattern on the LCD panel. The following table is a description of what is inside the CDDRAM, CGRAM and GDDRAM. Figure 9b and 9c are the output pattern on the LCD display with different command enabled.

(Display Mode, Page Swapping, Scrolling, Column Re-map and Row Re-map)

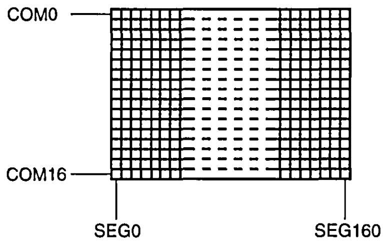
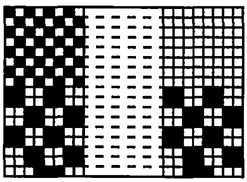


Figure 9a

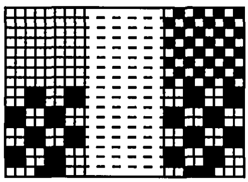
Content of GDDRAM

PAGE 1	5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - - - - 0 0 0 0 0 0 0 0 5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - - - - 0 0 0 0 0 0 0 0
PAGE 2	3 3 C C 3 3 C C - - - - - - - - - - - - - - - - - - 3 3 C C 3 3 C C 3 3 C C 3 3 C C - - - - - - - - - - - - - - - - - - 3 3 C C 3 3 C C
PAGE 3	0 0 0 0 0 0 0 0 - - - - - - - - - - - - - - - - - - 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 - - - - - - - - - - - - - - - - - - 0 0 1 1 1 0 0 0

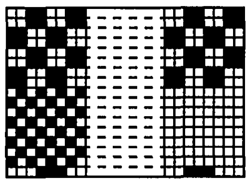
Figure 9b



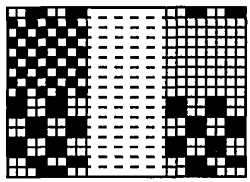
Column remap disable
Row re-map disable



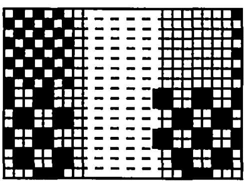
Column remap enable
Row re-map disable



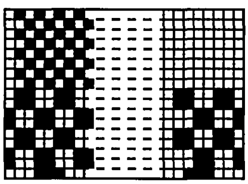
Column remap disable
Row re-map enable



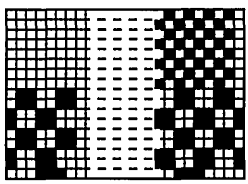
Column remap disable
Row re-map disable
Scroll Value = 0Fh



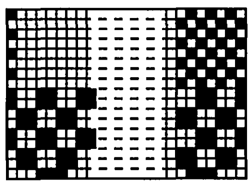
Column remap disable
Row re-map disable
Horizontal scroll = 1



Column remap disable
Row re-map disable
Horizontal scroll = 160



Column remap enable
Row re-map disable
Horizontal scroll = 1

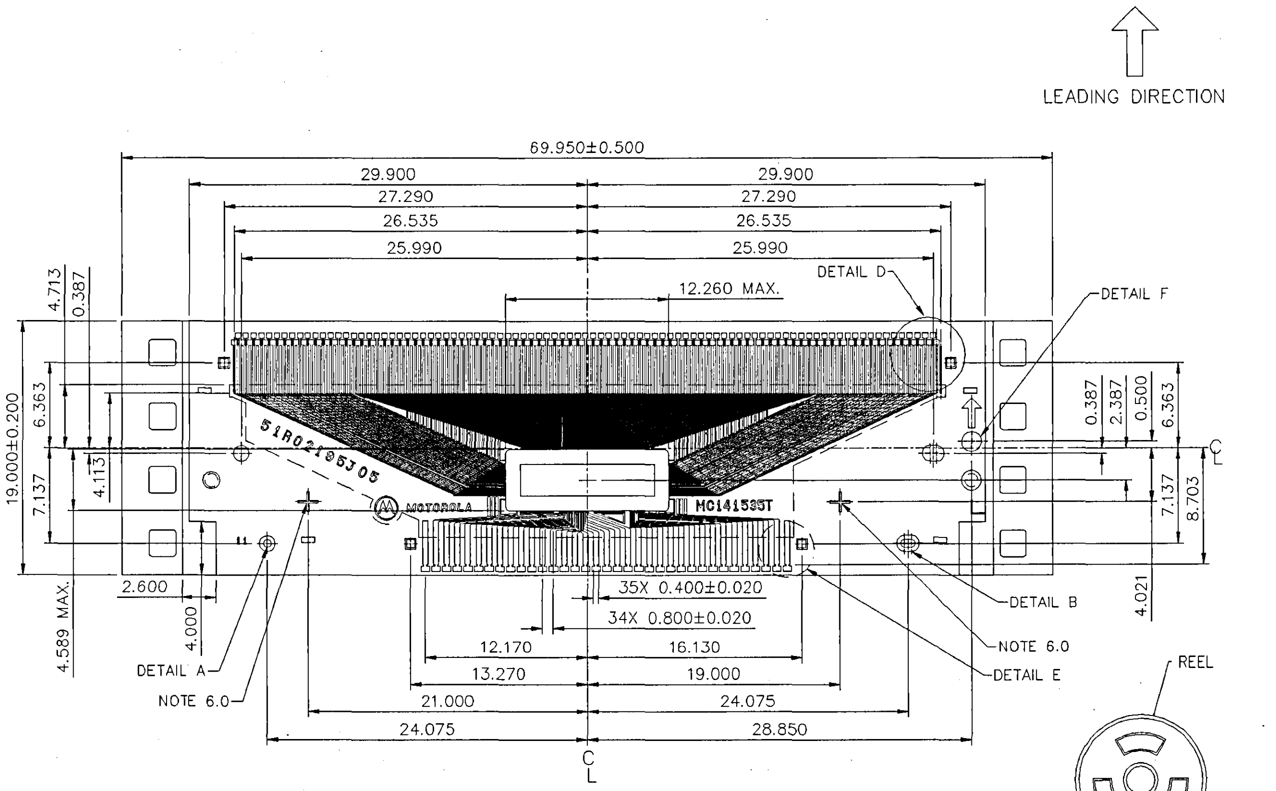


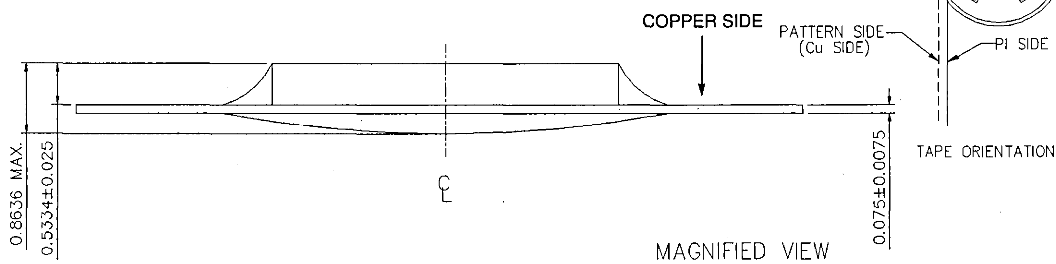
Column remap enable
Row re-map disable
Horizontal scroll = 160

Figure 9c. Examples of LCD display with different command enabled

MC141535T TAB PACKAGE DIMENSION (1 OF 2)
98ASL00248A ISSUE 0

DO NOT SCALE THIS DRAWING



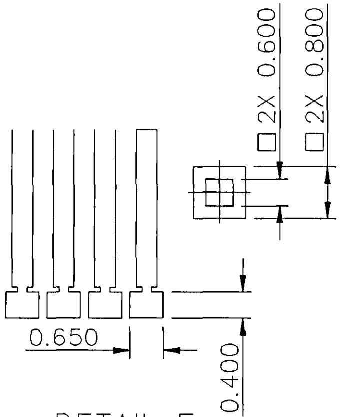


NOTES FOR ALL PAGES

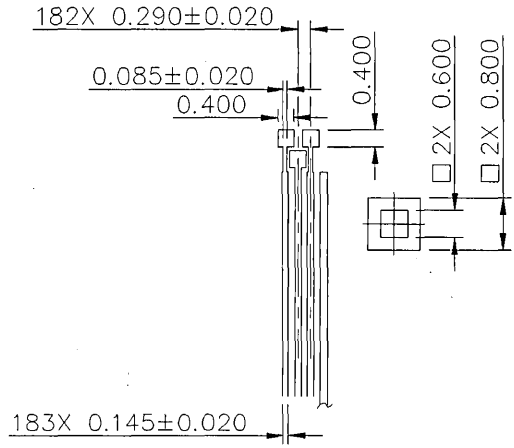
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ø 2.0 MM HOLE.
7. 4 SPROCKET HOLES DEVICE

MC141535T TAB PACKAGE DIMENSION (2 OF 2)
98ASL00248A ISSUE 0

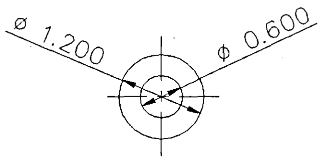
DO NOT SCALE THIS DRAWING



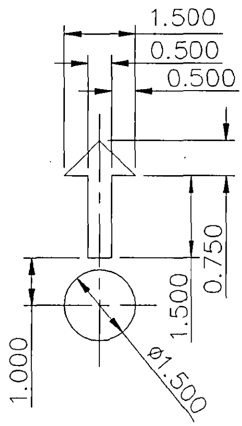
DETAIL E



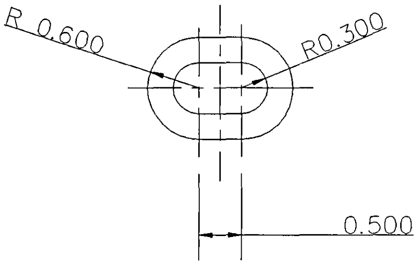
DETAIL D



DETAIL A



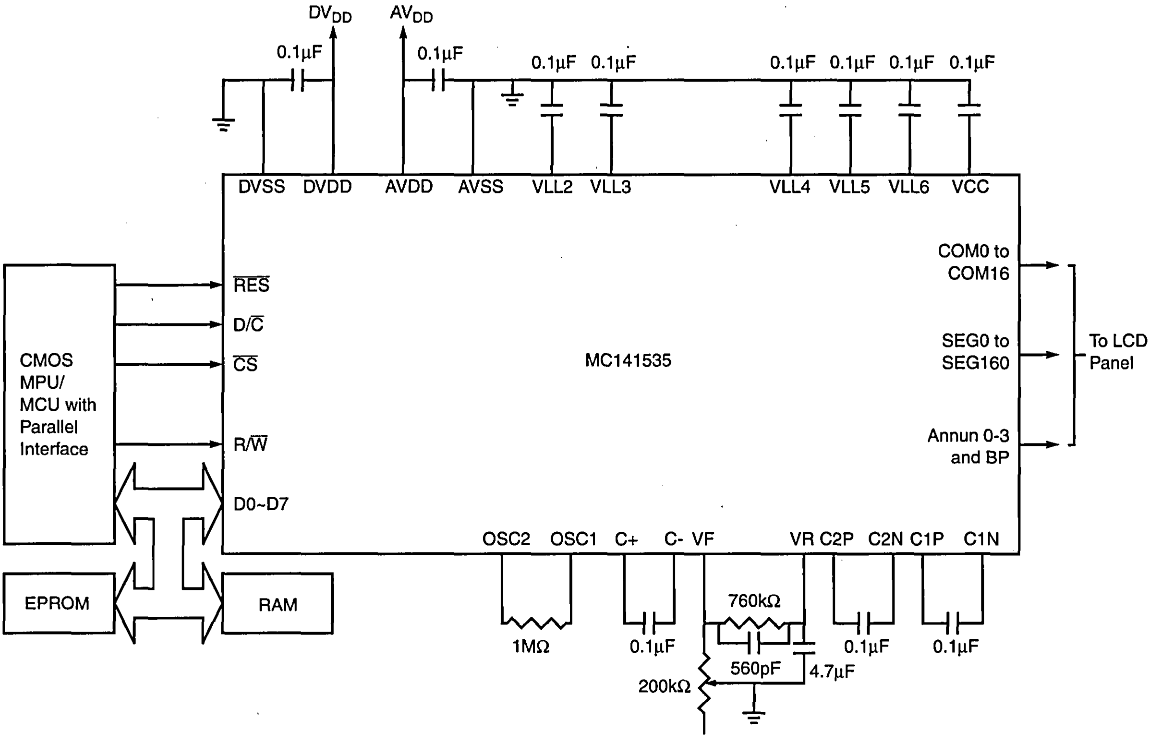
DETAIL F



DETAIL B

Application Circuit

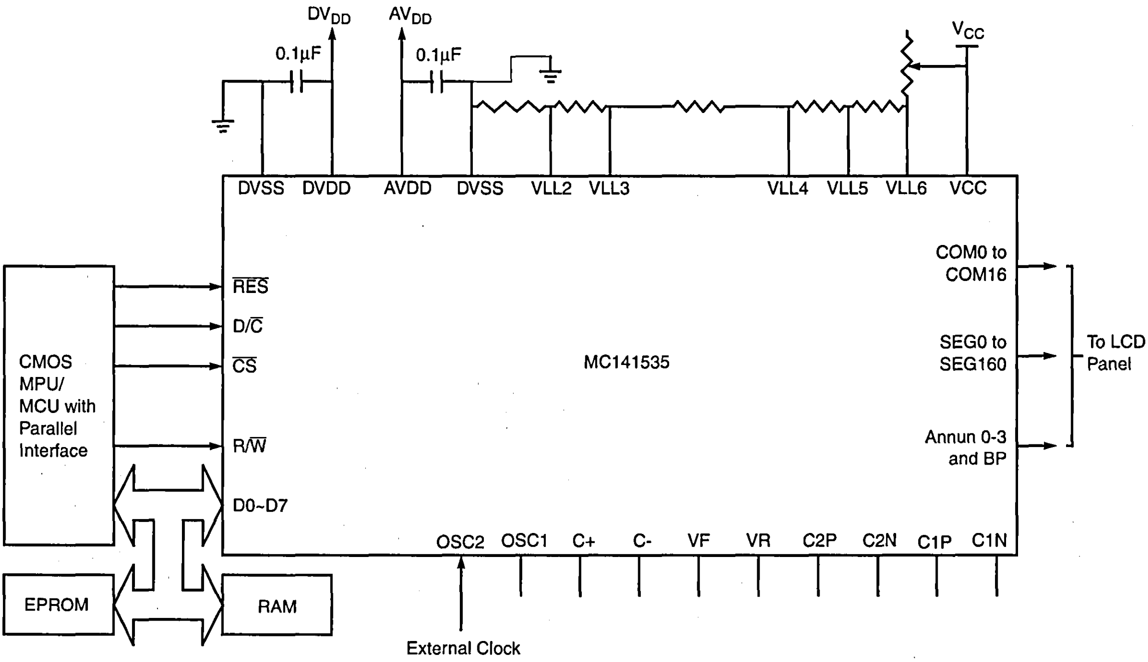
16/17 MUX Display with Analog Circuitry enabled, Tripler enabled and 1:5 bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

16/17 MUX Display with Analog Circuit disabled, External Bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

MC141535 Die Pad Co-ordinate

Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)
1	N/C	-5151.88	-1390.83	71	OSC2	2038.33	-1288.71	141	SEG28	3931.25	1275.76	211	SEG98	-1404.15	1275.76
2	N/C	-5050.13	-1390.83	72	AVDD	2140.08	-1288.71	142	SEG29	3855.03	1275.76	212	SEG99	-1480.37	1275.76
3	N/C	-4948.38	-1390.83	73	N/C	2269.58	-1390.83	143	SEG30	3778.81	1275.76	213	SEG100	-1556.59	1275.76
4	N/C	-4846.63	-1390.83	74	N/C	2371.33	-1390.83	144	SEG31	3702.59	1275.76	214	SEG101	-1632.81	1275.76
5	N/C	-4744.88	-1390.83	75	N/C	2473.08	-1390.83	145	SEG32	3626.37	1275.76	215	SEG102	-1709.03	1275.76
6	N/C	-4643.13	-1390.83	76	N/C	2574.83	-1390.83	146	SEG33	3550.15	1275.76	216	SEG103	-1785.25	1275.76
7	N/C	-4541.38	-1390.83	77	N/C	2676.58	-1390.83	147	SEG34	3473.93	1275.76	217	SEG104	-1861.47	1275.76
8	DVDD	-4264.62	-1307.21	78	N/C	2778.33	-1390.83	148	SEG35	3397.71	1275.76	218	SEG105	-1937.69	1275.76
9	RES	-4183.22	-1307.21	79	N/C	2880.08	-1390.83	149	SEG36	3321.49	1275.76	219	SEG106	-2013.91	1275.76
10	D/C	-4101.82	-1307.21	80	N/C	2981.83	-1390.83	150	SEG37	3245.27	1275.76	220	SEG107	-2090.13	1275.76
11	R/W	-4020.42	-1307.21	81	N/C	3083.58	-1390.83	151	SEG38	3169.05	1275.76	221	SEG108	-2166.35	1275.76
12	CS	-3939.02	-1307.21	82	N/C	3185.33	-1390.83	152	SEG39	3092.83	1275.76	222	SEG109	-2242.57	1275.76
13	DVSS	-3857.62	-1307.21	83	N/C	3287.08	-1390.83	153	SEG40	3016.61	1275.76	223	SEG110	-2318.79	1275.76
14	D0	-3776.22	-1307.21	84	N/C	3388.83	-1390.83	154	SEG41	2940.39	1275.76	224	SEG111	-2395.01	1275.76
15	D1	-3694.82	-1307.21	85	N/C	3490.58	-1390.83	155	SEG42	2864.17	1275.76	225	SEG112	-2471.23	1275.76
16	D2	-3613.42	-1307.21	86	N/C	3592.33	-1390.83	156	SEG43	2787.95	1275.76	226	SEG113	-2547.45	1275.76
17	D3	-3532.02	-1307.21	87	N/C	3694.08	-1390.83	157	SEG44	2711.73	1275.76	227	SEG114	-2623.67	1275.76
18	D4	-3450.62	-1307.21	88	N/C	3795.83	-1390.83	158	SEG45	2635.51	1275.76	228	SEG115	-2699.89	1275.76
19	D5	-3369.22	-1307.21	89	N/C	3897.58	-1390.83	159	SEG46	2559.29	1275.76	229	SEG116	-2776.11	1275.76
20	D6	-3287.82	-1307.21	90	N/C	3999.33	-1390.83	160	SEG47	2483.07	1275.76	230	SEG117	-2852.33	1275.76
21	D7	-3206.42	-1307.21	91	N/C	4101.08	-1390.83	161	SEG48	2406.85	1275.76	231	SEG118	-2928.55	1275.76
22	N/C	-3054.72	-1390.83	92	N/C	4202.83	-1390.83	162	SEG49	2330.63	1275.76	232	SEG119	-3004.77	1275.76
23	N/C	-2952.97	-1390.83	93	N/C	4304.58	-1390.83	163	SEG50	2254.41	1275.76	233	SEG120	-3080.99	1275.76
24	N/C	-2851.22	-1390.83	94	N/C	4406.33	-1390.83	164	SEG51	2178.19	1275.76	234	SEG121	-3157.21	1275.76
25	N/C	-2749.47	-1390.83	95	N/C	4508.08	-1390.83	165	SEG52	2101.97	1275.76	235	SEG122	-3233.43	1275.76
26	N/C	-2647.72	-1390.83	96	N/C	4609.83	-1390.83	166	SEG53	2025.75	1275.76	236	SEG123	-3309.65	1275.76
27	N/C	-2545.97	-1390.83	97	N/C	4711.58	-1390.83	167	SEG54	1949.53	1275.76	237	SEG124	-3385.87	1275.76
28	N/C	-2444.22	-1390.83	98	N/C	4813.33	-1390.83	168	SEG55	1873.31	1275.76	238	SEG125	-3462.09	1275.76
29	N/C	-2342.47	-1390.83	99	N/C	4915.08	-1390.83	169	SEG56	1797.09	1275.76	239	SEG126	-3538.31	1275.76
30	N/C	-2240.72	-1390.83	100	N/C	5016.83	-1390.83	170	SEG57	1720.87	1275.76	240	SEG127	-3614.53	1275.76
31	N/C	-2138.97	-1390.83	101	BP	5163.35	-1160.69	171	SEG58	1644.65	1275.76	241	SEG128	-3690.75	1275.76
32	N/C	-2037.22	-1390.83	102	ANN2	5163.35	-1084.47	172	SEG59	1568.43	1275.76	242	SEG129	-3766.97	1275.76
33	N/C	-1935.47	-1390.83	103	ANN3	5163.35	-1008.25	173	SEG60	1492.21	1275.76	243	SEG130	-3843.19	1275.76
34	N/C	-1833.72	-1390.83	104	COM16	5163.35	-932.03	174	SEG61	1415.99	1275.76	244	SEG131	-3919.41	1275.76
35	N/C	-1731.97	-1390.83	105	COM15	5163.35	-855.81	175	SEG62	1339.77	1275.76	245	SEG132	-3995.63	1275.76
36	N/C	-1630.22	-1390.83	106	COM14	5163.35	-779.59	176	SEG63	1263.55	1275.76	246	SEG133	-4071.85	1275.76
37	N/C	-1528.47	-1390.83	107	COM13	5163.35	-703.37	177	SEG64	1187.33	1275.76	247	SEG134	-4148.07	1275.76
38	N/C	-1426.72	-1390.83	108	COM12	5163.35	-627.15	178	SEG65	1111.11	1275.76	248	SEG135	-4224.29	1275.76
39	N/C	-1324.97	-1390.83	109	COM11	5163.35	-550.93	179	SEG66	1034.89	1275.76	249	SEG136	-4300.51	1275.76
40	N/C	-1223.22	-1390.83	110	COM10	5163.35	-474.71	180	SEG67	958.67	1275.76	250	SEG137	-4376.73	1275.76
41	N/C	-1121.47	-1390.83	111	COM9	5163.35	-398.49	181	SEG68	882.45	1275.76	251	SEG138	-4452.95	1275.76
42	N/C	-1019.72	-1390.83	112	COM8	5163.35	-322.27	182	SEG69	806.23	1275.76	252	SEG139	-4529.17	1275.76
43	N/C	-917.97	-1390.83	113	SEG0	5163.35	-206.09	183	SEG70	730.01	1275.76	253	SEG140	-4605.39	1275.76
44	N/C	-816.22	-1390.83	114	SEG1	5163.35	-129.87	184	SEG71	653.79	1275.76	254	SEG141	-5163.35	1242.09
45	N/C	-714.47	-1390.83	115	SEG2	5163.35	-53.65	185	SEG72	577.57	1275.76	255	SEG142	-5163.35	1165.87
46	N/C	-612.72	-1390.83	116	SEG3	5163.35	22.57	186	SEG73	501.35	1275.76	256	SEG143	-5163.35	1089.65
47	N/C	-510.97	-1390.83	117	SEG4	5163.35	98.79	187	SEG74	425.13	1275.76	257	SEG144	-5163.35	1013.43
48	N/C	-409.22	-1390.83	118	SEG5	5163.35	175.01	188	SEG75	348.91	1275.76	258	SEG145	-5163.35	937.21
49	N/C	-307.47	-1390.83	119	SEG6	5163.35	251.23	189	SEG76	272.69	1275.76	259	SEG146	-5163.35	860.99
50	N/C	-205.72	-1390.83	120	SEG7	5163.35	327.45	190	SEG77	196.47	1275.76	260	SEG147	-5163.35	784.77
51	AVSS	-57.72	-1288.71	121	SEG8	5163.35	403.67	191	SEG78	120.25	1275.76	261	SEG148	-5163.35	708.55
52	VF	44.03	-1288.71	122	SEG9	5163.35	479.89	192	SEG79	44.03	1275.76	262	SEG149	-5163.35	632.33
53	AVSS	145.78	-1288.71	123	SEG10	5163.35	556.11	193	SEG80	-32.19	1275.76	263	SEG150	-5163.35	556.11
54	C2P	247.53	-1288.71	124	SEG11	5163.35	632.33	194	SEG81	-108.41	1275.76	264	SEG151	-5163.35	479.89
55	C2N	349.28	-1288.71	125	SEG12	5163.35	708.55	195	SEG82	-184.63	1275.76	265	SEG152	-5163.35	403.67
56	C2N	451.03	-1288.71	126	SEG13	5163.35	784.77	196	SEG83	-260.85	1275.76	266	SEG153	-5163.35	327.45
57	C1P	552.78	-1288.71	127	SEG14	5163.35	860.99	197	SEG84	-337.07	1275.76	267	SEG154	-5163.35	251.23
58	C1N	654.53	-1288.71	128	SEG15	5163.35	937.21	198	SEG85	-413.29	1275.76	268	SEG155	-5163.35	175.01
59	C1N	756.28	-1288.71	129	SEG16	5163.35	1013.43	199	SEG86	-489.51	1275.76	269	SEG156	-5163.35	98.79
60	C+	858.03	-1288.71	130	SEG17	5163.35	1089.65	200	SEG87	-565.73	1275.76	270	SEG157	-5163.35	22.57
61	C-	959.78	-1288.71	131	SEG18	5163.35	1165.87	201	SEG88	-641.95	1275.76	271	SEG158	-5163.35	-53.65
62	VR	1122.58	-1288.71	132	SEG19	5163.35	1242.09	202	SEG89	-718.17	1275.76	272	SEG159	-5163.35	-129.87
63	VLL2	1224.33	-1288.71	133	SEG20	4541.01	1275.76	203	SEG90	-794.39	1275.76	273	SEG160	-5163.35	-206.09
64	VLL3	1326.08	-1288.71	134	SEG21	4464.79	1275.76	204	SEG91	-870.61	1275.76	274	COM16	-5163.35	-322.27
65	VLL4	1427.83	-1288.71	135	SEG22	4388.57	1275.76	205	SEG92	-946.83	1275.76	275	COM0	-5163.35	-398.49
66	VLL5	1529.58	-1288.71	136	SEG23	4312.35	1275.76	206	SEG93	-1023.05	1275.76	276	COM1	-5163.35	-474.71
67	VLL6	1631.33	-1288.71	137	SEG24	4236.13	1275.76	207	SEG94	-1099.27	1275.76	277	COM2	-5163.35	-550.93
68	OSC1	1733.08	-1288.71	138	SEG25	4159.91	1275.76	208	SEG95	-1175.49	1275.76	278	COM3	-5163.35	-627.15
69	VCC	1834.83	-1288.71	139	SEG26	4083.69	1275.76	209	SEG96	-1251.71	1275.76	279	COM4	-5163.35	-703.37
70	OSC2	1936.58	-1288.71	140	SEG27	4007.47	1275.76	210	SEG97	-1327.93	1275.76	280	COM5	-5163.35	-779.59
												281	COM6	-5163.35	-855.81
												282	COM7	-5163.35	-932.03
												283	ANN1	-5163.35	-1008.25
												284	ANN0	-5163.35	-1084.47
												285	BP	-5163.35	-1160.69

Die Size : 431.5 mil x 129.53 mil

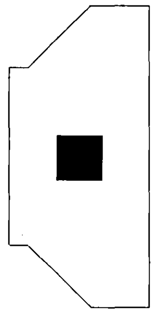
Note : Do not connect the NC pin to external circuit

MC141537

LCD Segment / Common Driver
CMOS

MC141537 is a CMOS LCD Driver which consists of 3 annunciator outputs and 136 high voltage LCD driving signals (16 common and 120 segment). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuit such that limited external component is required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30°C to 85°C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 bit Parallel Interface
- Graphic Mode Operation
- On Chip 240 byte Graphic Display Data RAM
- Master clear RAM
- 120 Segment Drivers, 16 Common Drivers
- 1/16 multiplex ratio
- 1:5 bias ratio
- Re-mapping of Row and Column Drivers
- Three stand alone Annunciator driver circuits
- Selectable LCD Drive Voltage Temperature Coefficients
- 16 level Internal Contrast Control
- External Contrast Control
- Available in TAB (Tape Automated Bonding) Package



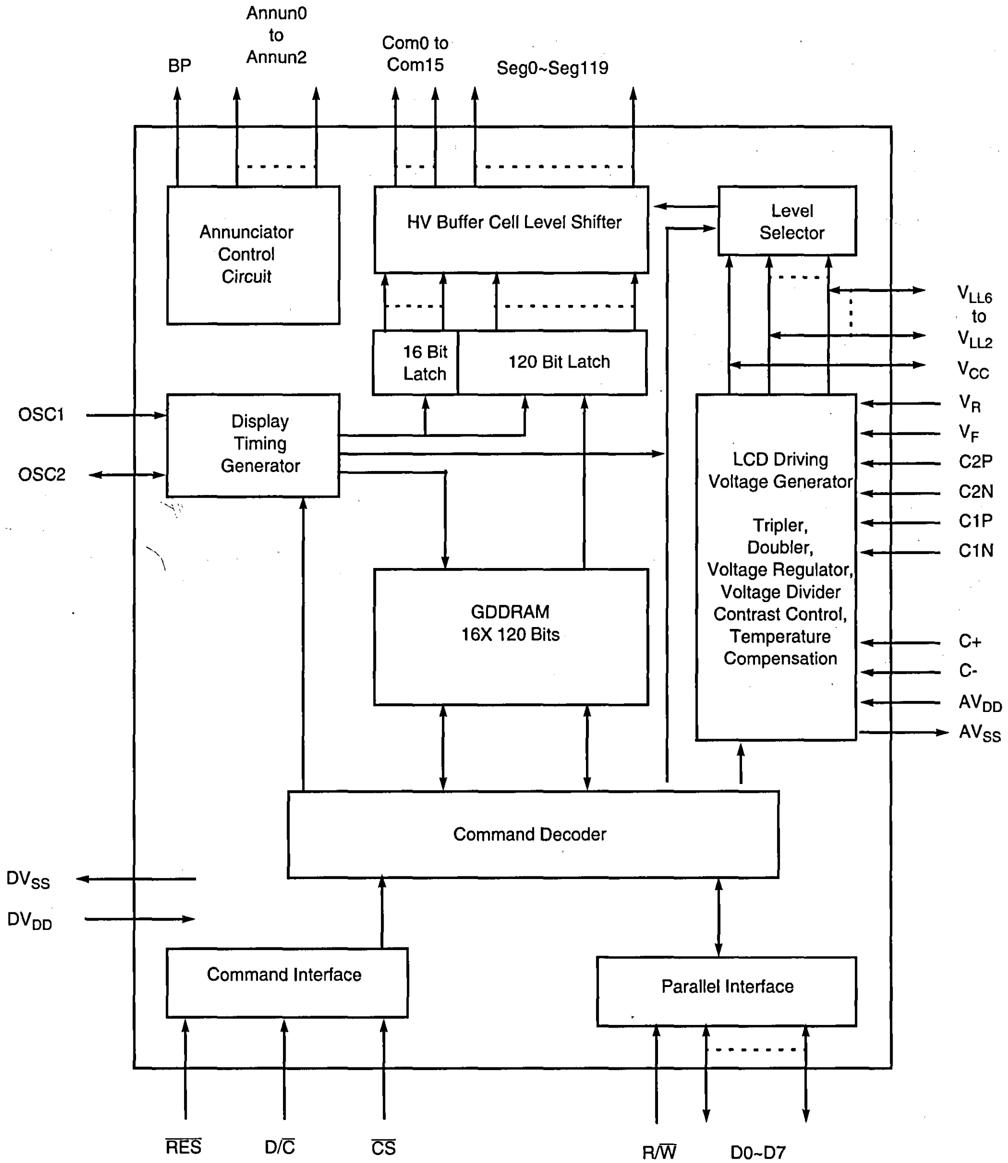
MC141537T1
TAB

ORDERING INFORMATION

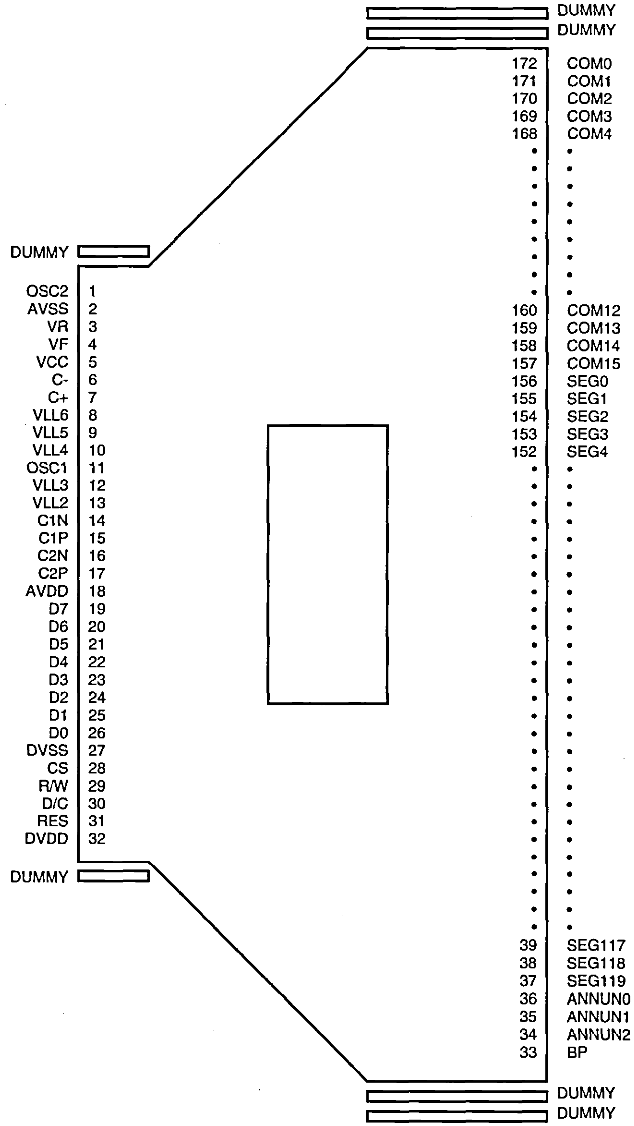
MC141537T1	TAB
MCC141537	Bare Die

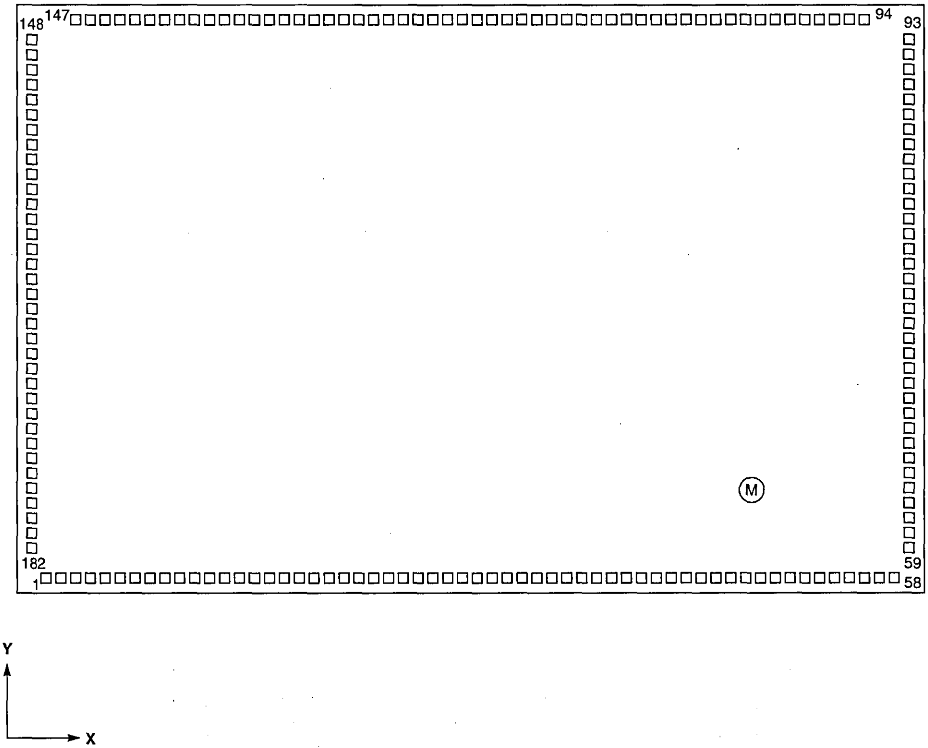
REV 6
3/97

BLOCK DIAGRAM



MC141537T1 PIN ASSIGNMENT
(Copper View)





MCC141537 DIE PIN ASSIGNMENT

Refer to the MC141537 Die Pad Coordinate for Pin Name Assignment

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
 T_{A1} T_{A2}	Operating Temperature For Using Internal Oscillator For Using External Oscillator	 -25 to +85 -30 to +85	 ˚C ˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

$V_{SS} = AV_{SS} = DV_{SS}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analogue Circuit)

$V_{DD} = AV_{DD} = DV_{DD}$ ($DV_{DD} = V_{DD}$of Digital circuit, $AV_{DD} = V_{DD}$ of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DV_{DD} AV_{DD}	Logic Circuit Supply Voltage Range Voltage Generator Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	2.4 2.4	3.0 -	3.5 3.5	V V
I_{AC}	Access Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/Off, R/W accessing, T_{cyc}=1MHz, Osc. Freq.=38.4KHz, Display On.	0	200	300	µA
AI_{DP}	Display Mode Supply Current Drain (AV_{DD} Pin)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/OFF, R/W halt, Osc. Freq.=38.4KHz, Display On.	0	70	150	µA
DI_{DP}	Display Mode Supply Current Drain (DV_{DD} Pin)	V_{DD}=3.0V, Internal DC/DC Converter On, Tripler Enabled, Annunciator On/OFF, R/W halt, Osc. Freq.=38.4KHz, Display On.	0	6	15	µA
I_{SB1}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Display off, Oscillator Disabled, R/W halt.	0	300	500	nA
I_{SB2}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, External Oscillator, Oscillator Enabled, Display Off, R/W halt, Ext Osc. Freq.=38.4KHz.	0	1	2	µA
I_{SB3}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal Oscillator, Oscillator Enabled, Display Off, R/W halt, Int Osc. Freq.=38.4KHz.	0	5	10	µA
V_{CC1}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Internal DC/DC Converter Enabled, Tripler Enabled, Osc. Freq.=38.4KHz, Regulator Enabled, Divider Enabled.	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Internal DC/DC Converter Enabled, Doubler Enabled, Osc. Freq.=38.4KHz, Regulator Enabled, Divider Enabled.	-	2*AV_{DD}	7	V
V_{LCD}	LCD Driving Voltage Input (V_{CC} Pin)	Internal DC/DC Converter Disabled.	AV_{DD}	-	10.5	V
V_{OH1}	Output High Voltage (D0-D7, Annun0-2, BP, OSC2)	I_{out}=100µA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D0-D7, Annun0-2, BP, OSC2)	I_{out}=100µA	0	-	0.1*V_{DD}	V
V_{R1}	LCD Driving Voltage Source (V_R Pin)	Regulator Enabled (V_R voltage depends on TC and Int/Ext Contrast Control)	0	-	V_{CC}	V
V_{R2}	LCD Driving Voltage Source (V_R Pin)	Regulator Disable.	-	Floating	-	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Input high voltage ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		0	-	0.2*V_{DD}	V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Output (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	Voltage Divider Enabled	- - - - -	V_R 0.8*V_R 0.6*V_R 0.4*V_R 0.2*V_R	- - - - -	V V V V V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Input (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	External Voltage Generator, Voltage Divider Disable	0 0 0 0 0	- - - - -	V_{CC} V_{CC} V_{CC} V_{CC} V_{CC}	V V V V V
I_{OH}	Output High Current Source (D0-D7, Annun0-2, BP, OSC2)	V_{out}=V_{DD}-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D0-D7, Annun0-2, BP, OSC2)	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source (D0-D7, OSC2)		-1	-	1	µA
I_{IL}/I_{IH}	Input Current ($\overline{RES}$, OSC2, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$, OSC1)		-1	-	1	µA
R_{on}	Channel resistance between LCD driving signal pins (SEG and COM) and driving voltage input pins (V_{LL2} to V_{LL6})	During Display on, 0.1V apply between two terminals, VCC within operating voltage range	-	-	10	KΩ
V_{SB}	Memory Retention Voltage (DV_{DD})	Standby mode, retain all internal configuration and RAM data	2	-	-	V
C_{IN}	Input Capacitance (OSC1, OSC2, all logic pins)		-	5	7.5	pF
	Temperature Coefficient Compensation*					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled	-	-0.35	-	%
V_{CN}	Internal Contrast Control (V_R Output Voltage)	Regulator Enabled, Internal Contrast control Enabled. (16 Voltage Levels Controlled by Software. Each level is typically 2.25% of the Regulator Output Voltage.)	-	± 18	-	%

*The formula for the temperature coefficient (TC) is:

$$TC(\%) = \frac{V_R \text{ at } 50^\circ C - V_R \text{ at } 0^\circ C}{50^\circ C - 0^\circ C} \times \frac{1}{V_R \text{ at } 25^\circ C} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, AV_{DD}=DV_{DD}=3V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display timing generator	60Hz Frame Frequency Either External Clock Input or Internal Oscillator Enabled	-	38.4	-	KHz
F_{ANN}	Backplane Frequency of Annunciator (Annun0-2, BP)	50% duty cycle Annunciator on, Fosc=38.4KHz	-	30	-	Hz
F_{FRM}	Frame Frequency	Graphic Display Mode, Timing generator freq. within specification	-	60	-	Hz
OSC	Internal Oscillation Frequency with different value of feedback resistor	Internal Oscillator Enabled, V_{DD} within operation range	See Figure 1 for the relationship			

Note: $F_{FRM}=F_{OSC}/640$
$F_{ANN}=F_{OSC}/1280$

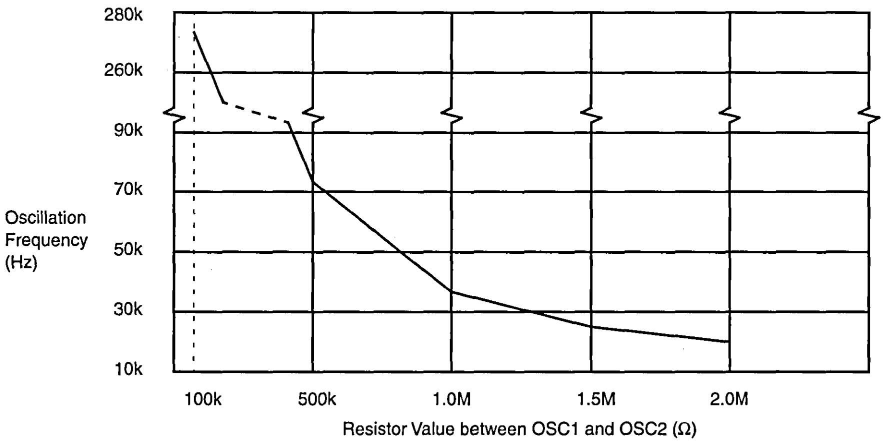


Figure 1. Internal Oscillator Frequency Relationship with External Resistance

TABLE 2. Parallel Timing Characteristics (Write Cycle) (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{DS}	Data Setup Time	350	-	-	ns
t_{DH}	Data Hold Time	30	-	-	ns
t_{AH}	Address Hold Time	30	-	-	ns

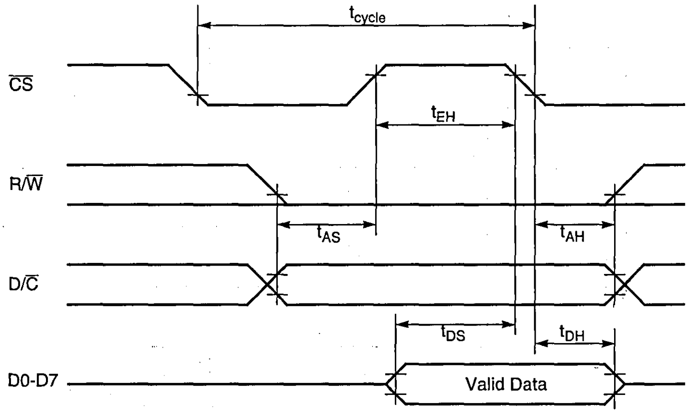


Figure 3a. Parallel Timing Characteristics (Write Cycle)

TABLE 3. Parallel Timing Characteristics (Read Cycle) (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	300	-	-	ns
t_{AS}	Address Setup Time	30	-	-	ns
t_{DS}	Data Setup Time	-	-	350	ns
t_{DH}	Data Hold Time	30	-	-	ns
t_{AH}	Address Hold Time	30	-	-	ns

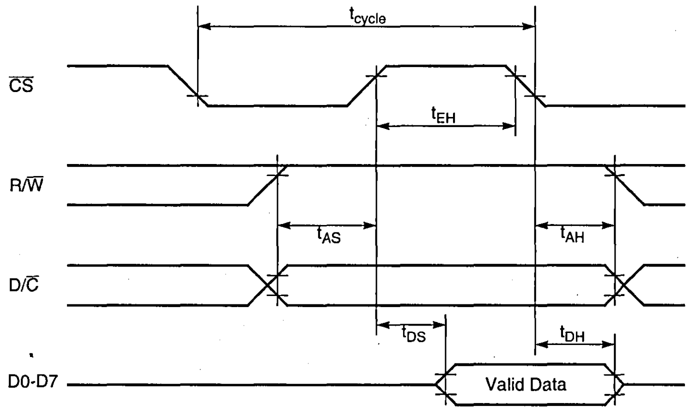


Figure 3b. Parallel Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)

This input pin tell the driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Input Clock)

This pin is normal Low clock input. Input on D0-D7 is latched at the falling edge of CS.

$\overline{RES}$ (Reset)

An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

D0-D7

This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read/Write)

This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/W input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)

This is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal Voltage Divider enabled, a 0.1 µF capacitor to AV_{SS} is required on each pin.

C1N and C1P

If Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required to connect these two pins.

C2N and C2P

If Internal DC/DC Converter is enable with Tripler enable, a 0.1µF capacitor is required to connect between these two pins. Otherwise, it should be left open.

C+ and C-

If internal divider circuit is enabled, a 0.1 µF capacitor is required to connect between these two pins.

VR and VF

This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 µF capacitor placed between VR and AVSS. (Refer to the Application Circuit Section)

COM0-COM15 (Row Drivers)

These pins provide the row driving signal to LCD panel. They output 0V during display off.

SEG0-SEG119 (Column Drivers)

These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)

This pin combines with Annun0-Annun2 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANN} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun2 (Annunciator Frontplanes)

These pins are three independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANN} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When oscillator is disabled, all these pins output 0V.

AVDD and AVSS

AVDD is the positive supply to the LCD bias voltage generator. AVSS is ground.

VCC

For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Positive power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS

Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command.

Data is directed to this module based upon the operating mode of the part and the status of the D/$\overline{C}$ line. If D/$\overline{C}$ High, data is written to Graphic Display Data RAM (GDDRAM). D/$\overline{C}$ Low indicates that the data is interpreted as a Command.

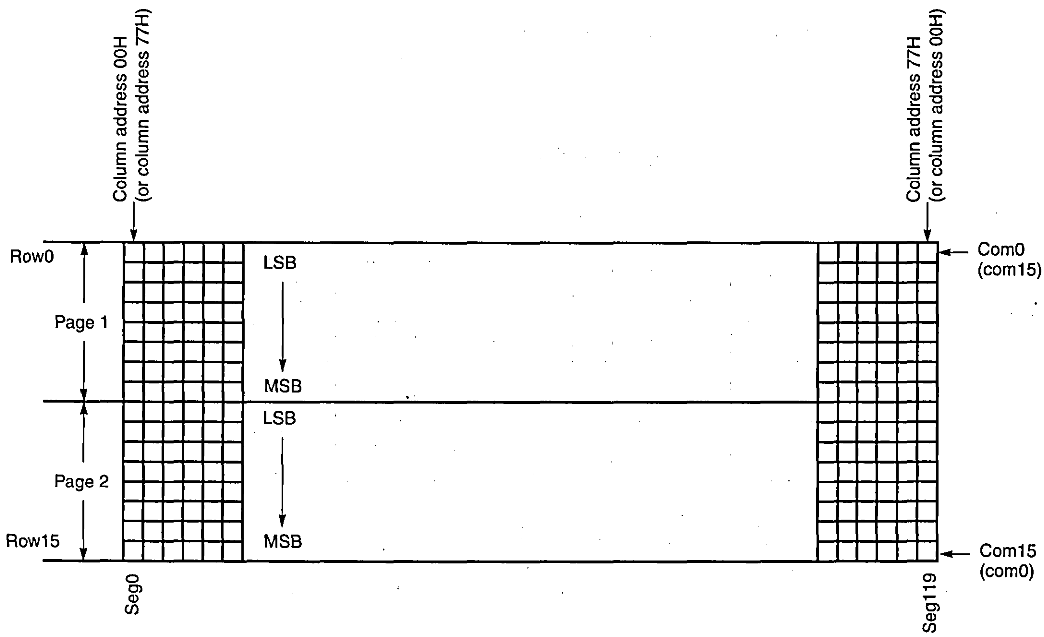
Reset has the same function as Power ON Reset (POR). Once $\overline{RES}$ received the POR pulse, all internal circuitry will reset to its initial status. Refer to Command description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7) plus R/$\overline{W}$ and $\overline{CS}$. The R/$\overline{W}$ line High indicates a read of the Graphic Display Data RAM (GDDRAM). R/$\overline{W}$ line Low indicates a write to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ line. The $\overline{CS}$ line serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM that holds the bit pattern to be displayed at graphic display mode. The size of the RAM is determined by number of row times the number of column drivers (120x16 = 1920 bits). Figure 4 is a description of GDDRAM address map. For mechanical feasibility, re-mapping on both Segment and Common outputs are provided.



Note : The configuration in parentheses represent the remapping of Commons and Columns

Figure 4. Graphic Display Data RAM Address MAP

Display Timing Generator

The part is an on chip low power RC oscillator circuitry (figure 5). The oscillator frequency is selected by external resistor in the range of 15 kHz to 50 kHz. The circuitry can be enabled with software control. For external clock application, feed clock into OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 3 Annunciators and BP are generated by this block. The 3 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit. The Oscillator must be enabled before selecting the annunciator on. Annunciator display waveform is shown in Figure 6.

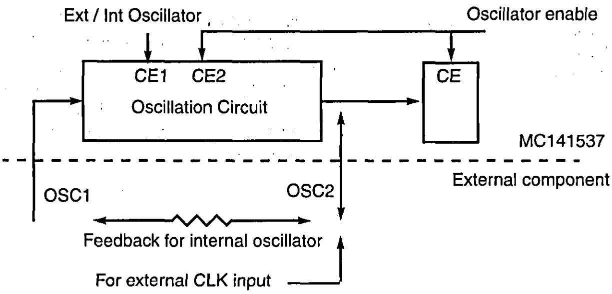
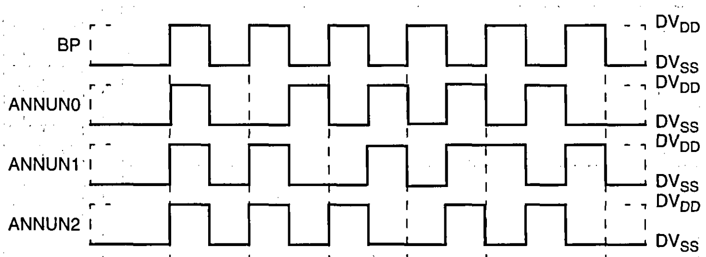


Figure 5. Oscillator Circuitry



Annunciator 0	On / Off	Off	On	On	On	On	On / Off
Annunciator 1	On / Off	Off	Off	On	On	Off	On / Off
Annunciator 2	On / Off	Off	Off	Off	On	On	On / Off
OSC	Disable	Enable	Enable	Enable	Enable	Enable	Disable

Figure 6. Annunciators and BP display waveform

LCD Drive Voltage Generator

This module generates the LCD voltages needed for display output. This section should take a single supply input and generate necessary bias voltage.

It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Doubler is used for LCD panel which needs lower driving voltage for less power consumption. Tripler is used for LCD panel which needs higher driving voltage.
2. Voltage Regulator
   Feedback gain control for initial LCD display voltage. One can also use it as an external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which consumes very little I_{LCD} current compare with traditional resistor ladder method.
4. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. This temperature coefficients can be selected by software control.
5. Contrast Control Block
   Software control of 16 voltage levels of LCD display voltage.

All blocks can be individually turned off if external voltage generator is provided.

16 Bit Latch / 120 Bit Latch

A 136 bit long register which carries the display signal information. First 16 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the Level Shifter for bumping up to the required level.

Level Selector

Level selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycle. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shifter)

HV buffer cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with a internal FRM clock which comes from the Display Timing Generator. The voltage levels are determined by the level selector which is synchronized with the internal M signal.

LCD Panel Driving Waveform

This is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveform shown in figure 7a, 7b and 7c illustrates the desired multiplex scheme.

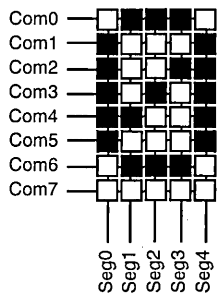


Figure 7a. LCD Display Waveform

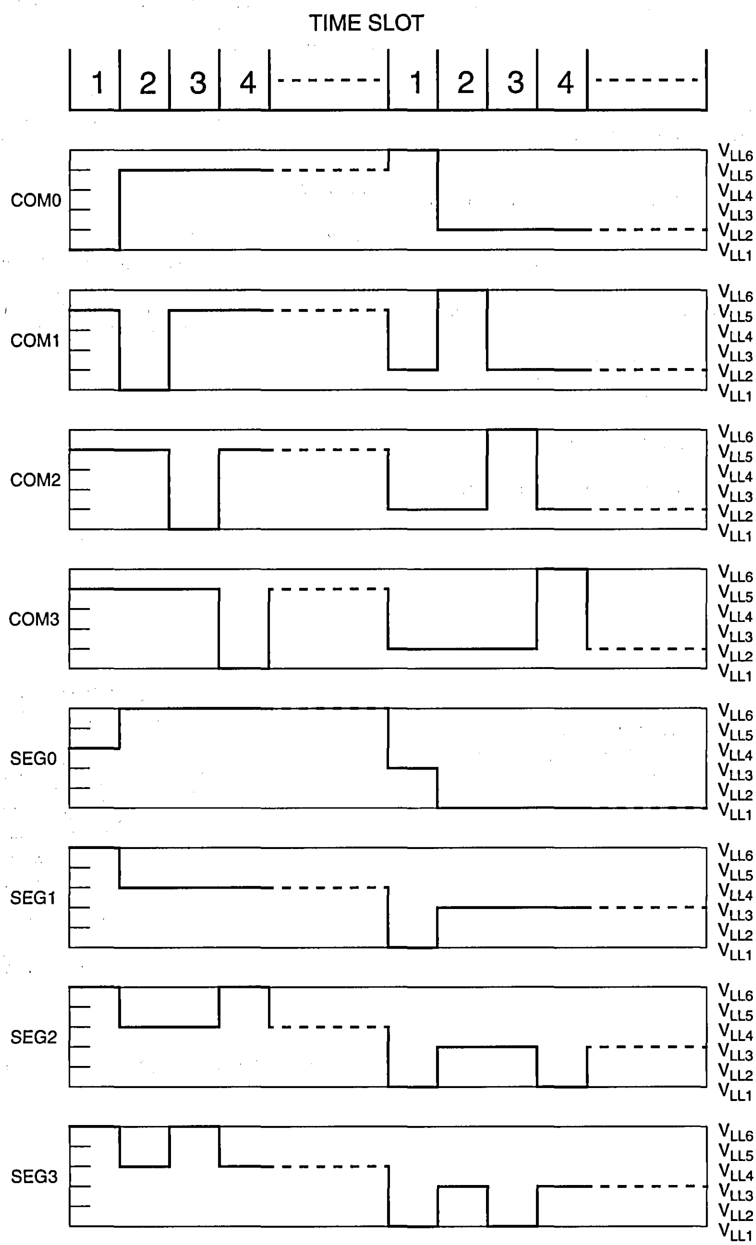


Figure 7b. LCD Driving Signal from MC141537

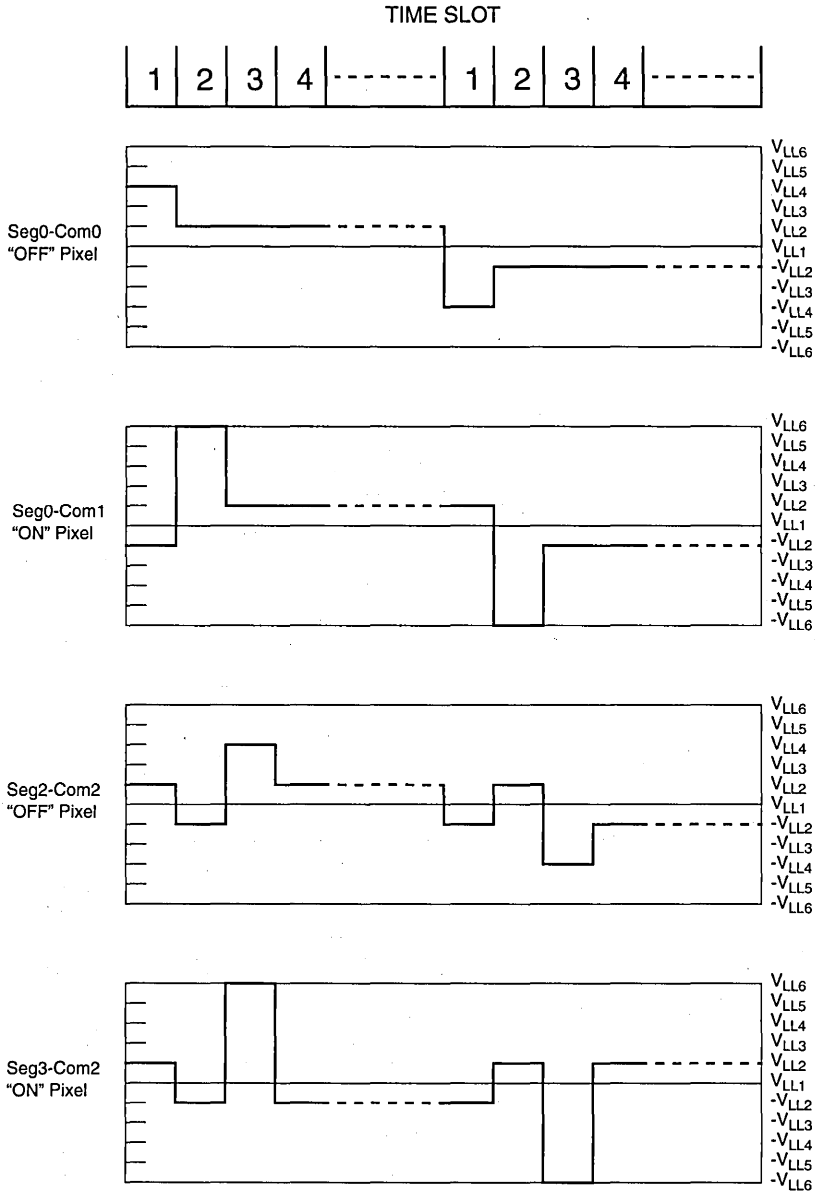


Figure 7c. Effective LCD waveform on LCD pixel

Command Description

Set Display On/Off (Display Mode / Stand-by mode)

The Display On command controls the selecting of the LCD output voltage and has no effect on the annunciator drivers. The Display On command causes the conversion of data in GDDRAM to the necessary waveforms on the Common and Segment driver outputs. It enables the on-chip bias generator. (Note : "Set Oscillator On" command should be issued before "display on")

The Display Off Command turns the display off and the state of the LCD driver are as follow during display off:
1) The Common and Segment driver outputs are fixed at V_{LL1} (V_{SS}).
2) The bias voltage generator is turned off.
3) The content of all registers and RAM are retained.
4) IC will accept new commands and data.
5) Annunciators is not affected by this command.
6) Oscillator is not affected by this command.

Set GDDRAM Column Address

This command positions the address pointer on a column boundary. The address can be set to location 00H-77H (120 columns). The column address will be increased automatically after a read or write operation. Refer to figure 4, "Address Increment Table" and command "Set GDDRAM Page Address" for further information.

Set GDDRAM Page Address

This command positions the row address pointer to 1 of 2 possible positions in GDDRAM. Refer to figure 4.

Master Clear GDDRAM

This command is a MASTER clear of the GDDRAM. The internal RAM data will be set to Zero after the command is issued. The clear RAM action will be taken if a dummy Write follows the "Clear GDDRAM" command.

Set Vertical Scroll Value

When display is turned on, this command maps the selected GDDRAM row (00H-0FH) to Com0-Com15. With scroll value equal to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 15 are mapped to Com1 through Com15 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 15 will be mapped to Com1 through Com14 respectively and Row 0 will be mapped to Com15.

Save / Restore Column Address

With a bit option = 1, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With a bit option = 0, this instruction restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing idle graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment Drivers for mechanically flexibility. There are 2 selected mappings:
1. Column 0 - Column 119 of GDDRAM mapped to Seg0 - Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119 - Seg0 respectively.

See section "Display Output Description by Example" for related information.

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:
1. Row 0 - Row 15 of GDDRAM to Common 0 - Common 15 respectively;
2. Row 0 - Row 15 of GDDRAM to Common 15 - Common 0 respectively.

See section "Display Output Description" for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 3 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on / off Oscillator. For either internal or external oscillator, this command should be executed. This command is not affected by the command " Set Display On/Off" and "Annunciator On/Off". See command "Ext/Int Oscillator" for more information.

Set External / Internal Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is being selected, feedback resistor between OSC1 and OSC2 is needed. For External oscillation circuit, clock should be input to OSC2. OSC1 should be left open.

Set Internal DC/DC Converter On/Off

This command selects the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external V_{CC} is provided.

Set Voltage Doubler / Tripler

This command selects the Voltage Doubler or Tripler when the Internal DC/DC Converter is enabled.

Set Internal Regulator On/Off

With different bit option values, this command either enables or disables the regulator which consists of internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is enabled, an external power supply should be applied to V_{LL6}- V_{LL2}. If the divider is enabled, the internal circuit will automatically generate the 1:5 bias level driving voltage.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage between the bias voltages. If the bit option = 1, the software selected for delta bias voltage control is enabled. If the bit option = 0, the external contrast control through an external resistor is enabled. Note: The software contrast control and the external feedback contrast controls cannot be both enabled at the same time.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use. After power-on reset, the contrast level is the lowest.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from the lowest value after POR.

Set Temperature Coefficient

This instruction selects 4 different LCD drive voltage temperature coefficients allowing for various liquid crystal temperature grades. These temperature coefficients are specified in Electrical Characteristics Tables.

COMMAND TABLE

	Bit Pattern	Command	Comment
1	$0000000X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X0 as address bit. X_0=0: page 1(POR) x_0=1: page 2
30	$0001X_3X_2X_1X_0$	Set Contrast Level	Enable one of the 16 Internal Contrast Value using X3X2X1X0 as data bits. Reset to 0000 during POR.
2	$0010000X_0$	Set Voltage Tripler / Doubler	X_0=0: tripler enabled (POR) X_0=1: doubler enabled
3	$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
4	$0010010X_0$	Set Row Mapping	X_0=0 : Row0 to Com0 (POR) X_0=1: Row0 to Com15
5	$0010011X_0$	Reserved for Expansion	
6	$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
7	$0010101X_0$	Set Internal DC/DC Converter Enable	X_0=0: disable generator(POR) X_0=1: enable generator
8	$0010110X_0$	Set Internal Regulator On/Off	X_0=0: disable regulator (POR) X_0=1: enable regulator When application uses a supply with built-in temperature compensation, the regulator should be disabled .
9	$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: disable voltage divider (POR) X_0=1: enable voltage divider When an external bias network is used, the voltage divider should be disabled.
10	0011000X0	Set Internal Contrast Control On/Off	X_0=0: disable contrast control (POR) X_0=1: enable contrast control Internal contrast circuits should be disabled if external contrast circuits is used.
11	$0011001X_0$	Reserved for Expansion	
12	$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
13	00110110	Master Clear GDDRAM	Master Clear GDDRAM
14	$0011100X_0$	Reserved for Expansion	
15	$0011101X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode (Note: Be sure to set X0=0 during application)
16	$001111X_1X_0$	Reserved for Expansion	
17	$0100X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_3X_2X_1X_0$ as scroll amount. Scroll value = 0 upon POR
18	$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 0(POR) A_1A_0=01: select annunciator 1 A_1A_0=10: select annunciator 2 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on
19	$011010X_1X_0$	Reserved for Expansion	
20	$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=01: -0.18% X_1X_0=10: -0.22% X_1X_0=11: -0.35%

	Bit Pattern	Command	Comment
21	$0111000X_0$	Increment/Decrement Contrast Level	X_0=0: decrement by one level X_0=1: increment by one level (Note: increment/decrement wraps around; total 16 contrast levels. Start at the lowest level when POR.)
22	$0111001X_0$	Reserved for Expansion	
23	$0111010X_0$	Reserved for Expansion	
24	$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Be sure to set X0=0 during application)
25	$0111100X_0$	Reserved for Expansion	
26	$0111101X_0$	Set External / Internal Oscillator	X_0=0: external oscillator (POR) X_0=1: internal oscillator For internal oscillator circuit enabled, place resistor between OSC1 and OSC2. At external oscillator mode, feed clock to OSC2.
27	$0111110X_0$	Reserved For Expansion	
28	$0111111X_0$	Oscillator Enable	X_0=0: oscillator disable (POR) X_0=1: oscillator enable. This is the master control for oscillator circuitry. Issue command 26 before this command.
29	1X6X5X4X3X2X1X0	Set GDDRAM Column Address	Set GDDRAM Column Address. Use X6X5X4X3X2X1X0 as address bits

DATA READ/WRITE TABLE

	Bit Pattern	Command	Comment
1	$X_7X_6X_5X_4X_3X_2X_1X_0$	Data Read / Data Write D/$\overline{C}$ line high	When R/$\overline{W}$ line low, Data write into GDDRAM. RAM column address pointer will have increment automatically. When R/$\overline{W}$ line high, Data read from GDDRAM. RAM column address pointer will have increment automatically. Address Auto increment will not apply if the last command is Clear RAM. This is a dummy write.

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Parallel Mode Write Command	No	
0	1	Parallel Mode Read Command	No (invalid mode)	1
1	0	Parallel Mode Write Data	Yes	2
1	1	Parallel Mode Read Data	Yes	

Address Increment is done automatically after command being sent or data read write. Only the Column address pointer of GDDRAM is affected.

Remark : 1. Under this condition, the data, not command will be read from RAM.
2. If write data is issued after Command Clear RAM, address inc is not applied.
3. Column Address wraps around.

Commands Required for R/W Actions on RAMs

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address, Set GDDRAM Column Address, Read/Write Data.	$(0000000X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	$(0011010X_0)$
Increment GDDRAM Address by one	Dummy Read Data	$(X_7X_6X_5X_4X_3X_2X_1X_0)$
Clear GDDRAM Address.	Master Clear GDDRAM, Dummy Write Data.	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Graphic Mode	Set External / Internal Oscillator, Set Oscillator Enable, Set Display On.	$(0111101X_0)$* (01111111)* (00101001)*
Annunciator Display	Set External / Internal Oscillator, Set Oscillator Enable, Set Annunciator On/Off.	$(0111101X_0)$* (01111111)* $(01100A_1A_0X_0)$*
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator, Set Display Off, Set Oscillator Enable. Set Annunciator On/Off.	(01111010)* (00101000)* (01111111)* $(01100A_1A_0X_0)$*
Standby Mode 3.	Set Internal Oscillator, Set Display Off, Set Oscillator Enable. Set Annunciator On/Off.	(01111011)* (00101000)* (01111111)* $(01100A_1A_0X_0)$*

1. Other Related Command with Graphic Mode :
   Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

2. Commands Related to Voltage Generator :
   Set Oscillator Enable / Disable, Set External / Internal Oscillator, Set Voltage Doubler / Tripler , Set Temperature Coefficient, Set Internal Regulator On/Off, Set Internal Contrast Control On/Off, Increase / Decrease Contrast Level, Set Contrast Level, Set Internal Voltage Divider On/Off, Set Display On/Off.

* No need if set already.

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set External / Internal Oscillator	External	*1
Set Voltage Tripler / Doubler	Tripler	*1
Internal DC/DC Converter Enable	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Set Contrast Level	Contrast Level = 0	*1, *2, *3
Set Internal Voltage Divider On	Off	*1
Set Column Mapping	Seg. 0 = Col. 0	*1
Set Row Mapping	Com. 0 = Row 0	*1
Set Vertical Scroll Value	Scroll Value = 0	*1
Set Oscillator Enable	Disable	
Set Annunciator Control Signals	All Annunciators off	*1
Master Clear RAM	Random	
Dummy Write Data		
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

Display Output Description by Example

This an example of output pattern on the LCD panel. Figure 8a, 8b and 8c are data map of GDDRAM and the output pattern on the LCD display with different command enabled. (Scrolling, Column Re-map and Row Re-map)

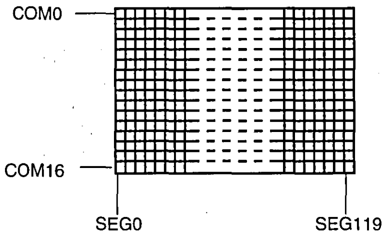
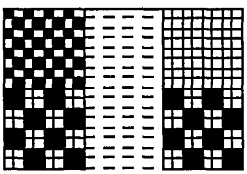


Figure 8a

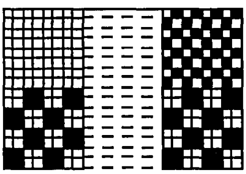
Content of GDDRAM

PAGE 1	5 A 5 A 5 A - - - 0 0 0 0 0 0 5 A 5 A 5 A - - - 0 0 0 0 0 0
PAGE 2	3 3 C C 3 3 - - - C C 3 3 C C 3 3 C C 3 3 - - - C C 3 3 C C

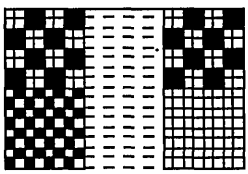
Figure 8b



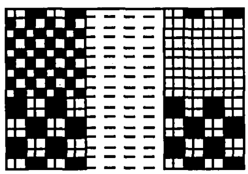
Graphic Mode
Column remap disable
Row remap disable



Graphic Mode
Column remap enable
Row remap disable



Graphic Mode
Column remap disable
Row remap enable

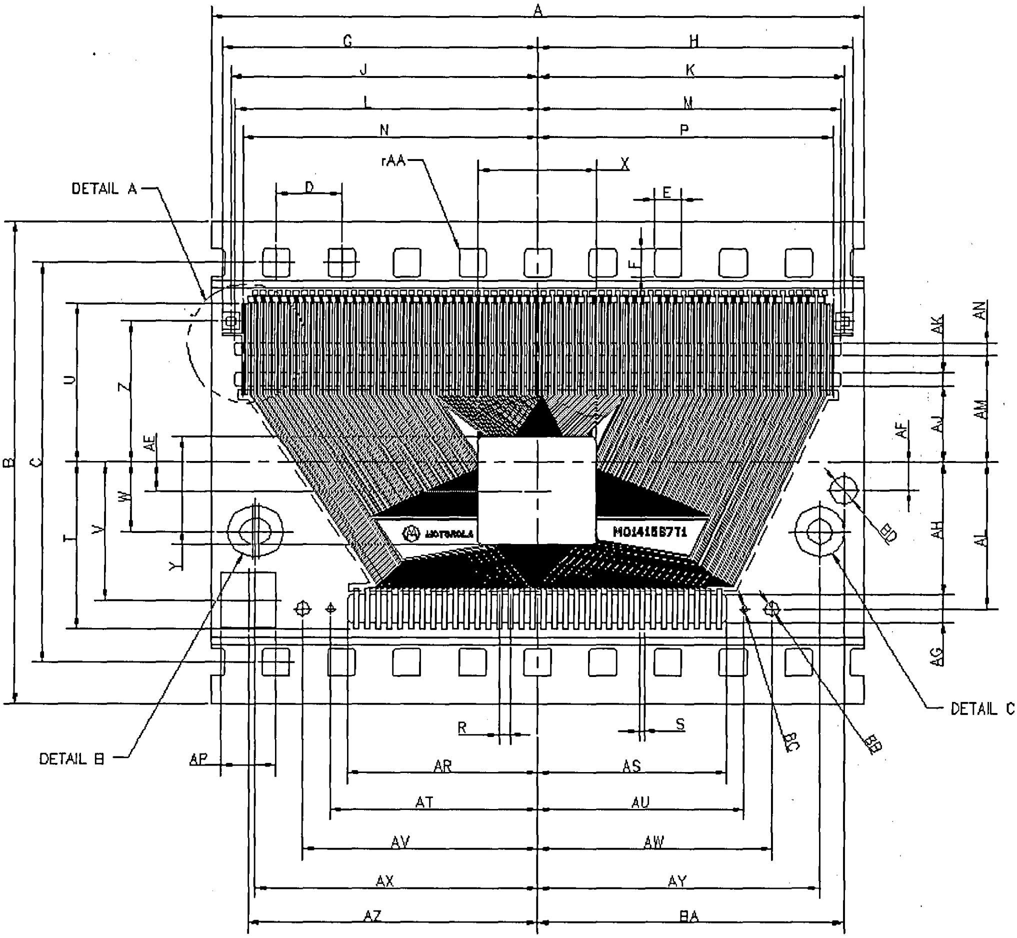


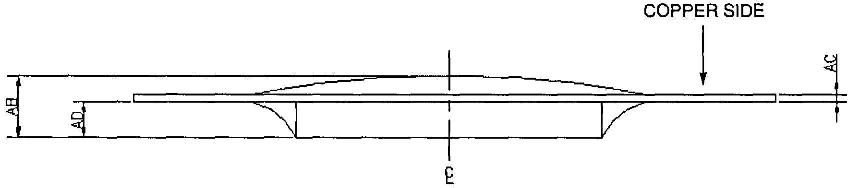
Graphic Mode
Column remap disable
Row remap disable
Scroll Value = 0FH

Figure 8c

PACKAGE DIMENSIONS

MC141537T1
TAB PACKAGE DIMENSION
DO NOT SCALE THIS DRAWING



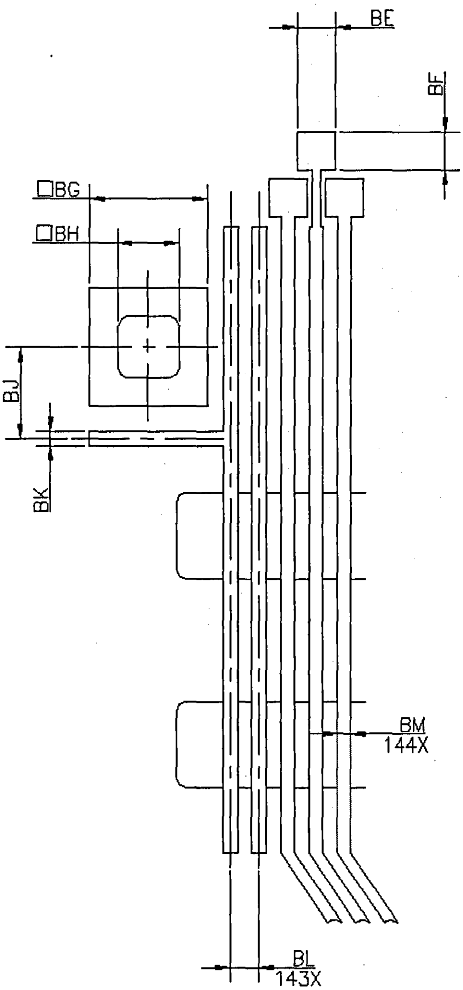


MAGNIFIED VIEW

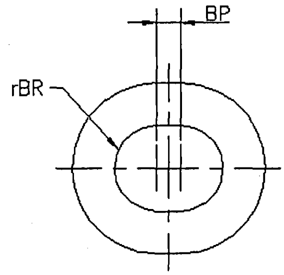
Reference : 98ASL00159A Issue O

MC141537T1 TAB PACKAGE DIMENSION

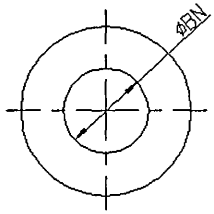
DO NOT SCALE THIS DRAWING



DETAIL "A"



DETAIL "B"



DETAIL "C"

Reference : 98ASL00159A Issue O

MC141537T1 TAB PACKAGE DIMENSION

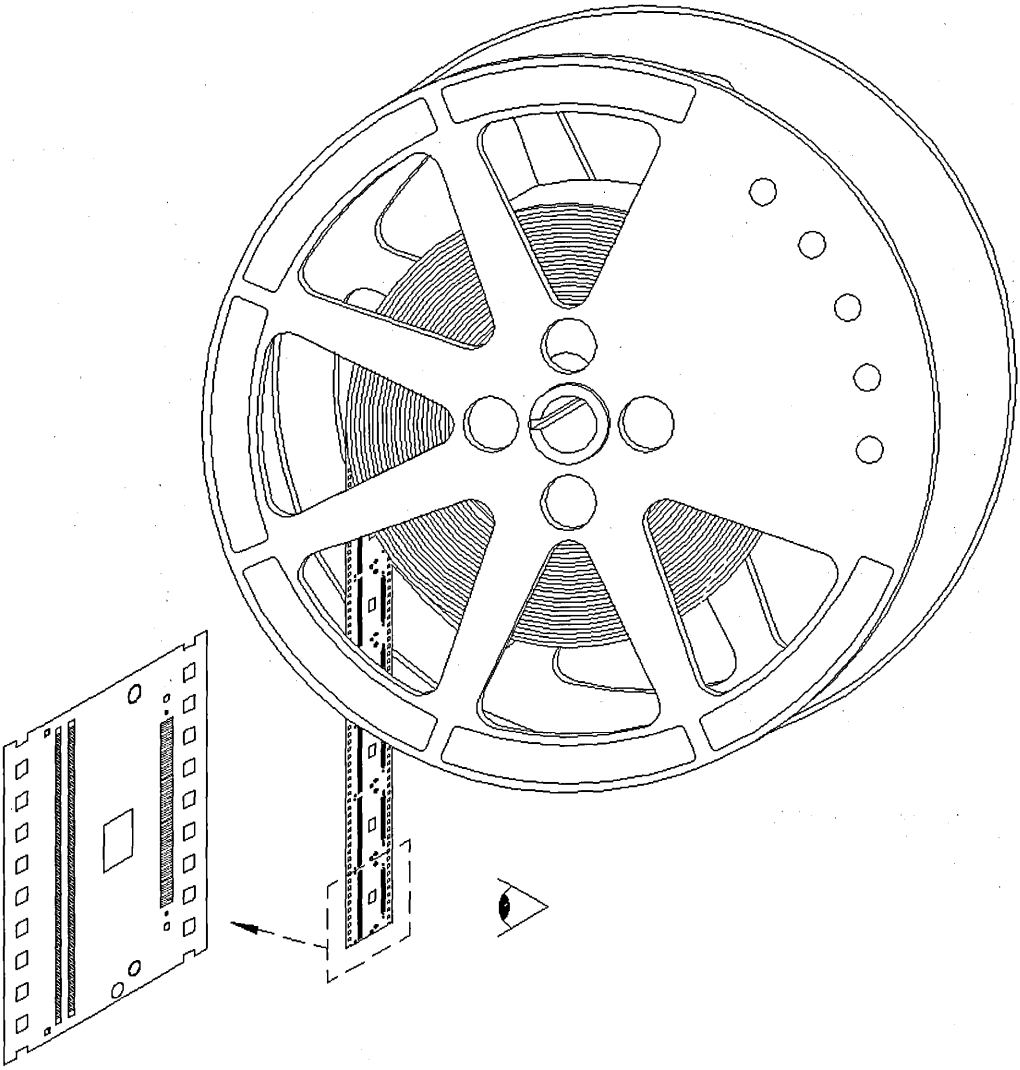
	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	47.000	48.000	1.8504	1.8898	AJ	5.537	5.637	0.2180	0.2219
B	34.775	35.175	1.3691	1.3848	AK	0.850	0.950	0.0335	0.0374
C	28.927	29.027	1.1389	1.1428	AL	10.550	10.650	0.4154	0.4193
D	4.720	4.780	0.1858	0.1882	AM	7.737	7.837	0.3046	0.3085
E	1.951	2.011	0.0768	0.0792	AN	0.850	0.950	0.0335	0.0374
F	1.951	2.011	0.0768	0.0792	AP	3.500	4.500	0.1378	0.1772
G	22.900	23.000	0.9016	0.9055	AR	13.750	13.850	0.5413	0.5453
H	22.900	23.000	0.9016	0.9055	AS	13.750	13.850	0.5413	0.5453
J	22.275	22.375	0.8770	0.8809	AT	15.000	15.100	0.5906	0.5945
K	22.275	22.375	0.8770	0.8809	AU	15.000	15.100	0.5906	0.5945
L	21.975	22.075	0.8652	0.8691	AV	17.000	17.100	0.6693	0.6732
M	21.975	22.075	0.8652	0.8691	AW	17.000	17.100	0.6693	0.6732
N	21.407	21.493	0.8428	0.8462	AX	20.450	20.550	0.8051	0.8091
P	21.407	21.493	0.8428	0.8462	AY	20.450	20.550	0.8051	0.8091
R	0.790	0.810	0.0311	0.0319	AZ	20.500	21.500	0.8071	0.8465
S	0.330	0.370	0.0130	0.0146	BA	21.750	22.750	0.8563	0.8957
T	12.050	12.150	0.4744	0.4783	BB	0.950	1.050	0.0374	0.0413
U	11.450	11.550	0.4508	0.4547	BC	0.450	0.550	0.0177	0.0217
V	9.500	10.500	0.3740	0.4134	BD	1.950	2.050	0.0768	0.0807
W	4.950	5.050	0.1949	0.1988	BE	0.350	0.450	0.0138	0.0177
X	-	8.643	-	0.3403	BF	0.350	0.450	0.0138	0.0177
Y	-	7.814	-	0.3076	BG	1.230	1.270	0.0484	0.0500
Z	10.180	10.280	0.4008	0.4047	BH	0.630	0.670	0.0248	0.0264
AA	-	0.200	-	0.0079	BJ	0.918	1.018	0.0361	0.0401
AB	0.686	0.838	0.0270	0.0330	BK	0.100	0.200	0.0039	0.0079
AC	0.068	0.083	0.0027	0.0032	BL	0.290	0.310	0.0114	0.0122
AD	0.579	0.629	0.0228	0.0248	BM	0.130	0.170	0.0051	0.0067
AE	1.600	2.600	0.0630	0.1024	BN	1.750	1.850	0.0689	0.0728
AF	1.500	2.500	0.0591	0.0984	BP	0.450	0.550	0.0177	0.0217
AG	1.950	2.050	0.0768	0.0807	BR	0.850	0.950	0.0335	0.0374
AH	9.550	9.650	0.3760	0.3799					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper thickness: 1oz.
4. Tin plating thickness: 0.4µm.
5. 10 sprocket hole device.

Reference : 98ASL00159A Issue O

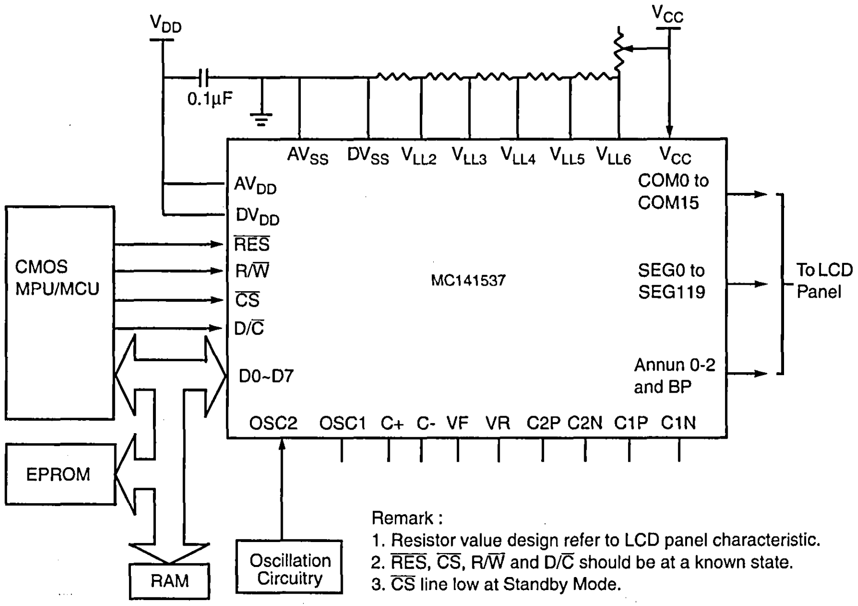
MC141537T1

TAB TAPE REEL ORIENTATION



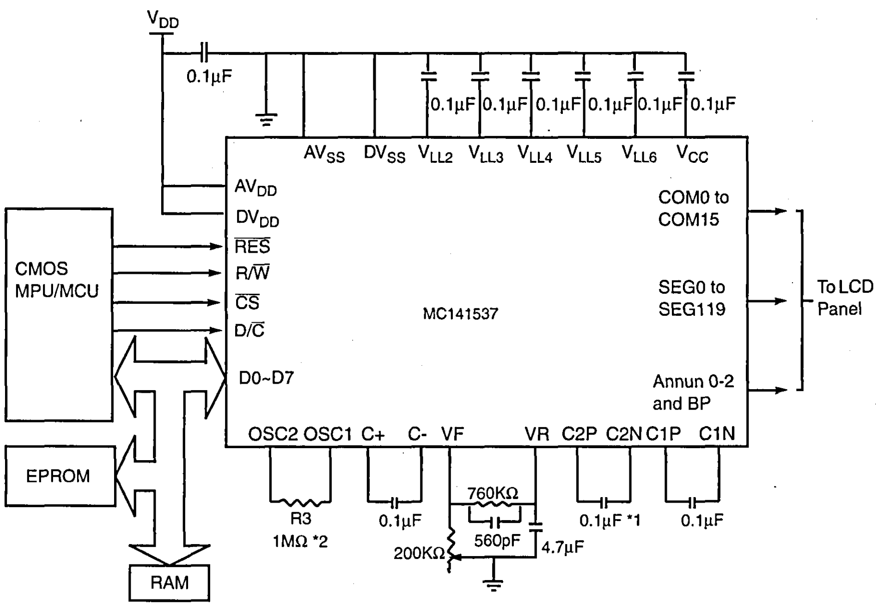
Reference : 98ASL00159A Issue O

Application Circuit: (All Internal Analog Block Disabled, External Voltage Generator used)



Remark :
1. Resistor value design refer to LCD panel characteristic.
2. $\overline{RES}$, $\overline{CS}$, $R/\overline{W}$ and $D/\overline{C}$ should be at a known state.
3. $\overline{CS}$ line low at Standby Mode.

Application Circuit: (All Internal Analog Block Enabled)



Remark :
1. Capacitor between C2N and C2P can be omitted only if doubler is enable.
2. R3 can be omitted for external oscillator.
3. VR and VF can be left open for Regulator disable, TC = 0% and Contrast Disable.
4. $\overline{RES}$, $\overline{CS}$, $R/\overline{W}$ and $D/\overline{C}$ should be at a known state.
5. $\overline{CS}$ line low at Standby Mode.

MC141537 Die Pad Coordinate

Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)	Pin	Name	x (um)	y (um)
1	COM9	-2900.06	-1958.41	59	SEG109	2953.34	-1723.46	94	DUMMY	2705.44	2035.37	148	SEG28	-2953.71	1780.81
2	COM8	-2798.31	-1958.41	60	SEG108	2953.34	-1621.71	95	DUMMY	2603.69	2035.37	149	SEG27	-2953.71	1679.06
3	COM7	-2696.56	-1958.41	61	SEG107	2953.34	-1519.96	96	DUMMY	2501.94	2035.37	150	SEG26	-2953.71	1577.31
4	COM6	-2594.81	-1958.41	62	SEG106	2953.34	-1418.21	97	DUMMY	2400.19	2035.37	151	SEG25	-2953.71	1475.56
5	COM5	-2493.06	-1958.41	63	SEG105	2953.34	-1316.46	98	SEG74	2289.19	1958.41	152	SEG24	-2953.71	1373.81
6	COM4	-2391.31	-1958.41	64	SEG104	2953.34	-1214.71	99	SEG73	2187.44	1958.41	153	SEG23	-2953.71	1272.06
7	COM3	-2289.56	-1958.41	65	SEG103	2953.34	-1068.19	100	SEG72	2085.69	1958.41	154	SEG22	-2953.71	1170.31
8	COM2	-2187.81	-1958.41	66	SEG102	2953.34	-966.44	101	SEG71	1983.94	1958.41	155	SEG21	-2953.71	1068.56
9	COM1	-2086.06	-1958.41	67	SEG101	2953.34	-864.69	102	SEG70	1882.19	1958.41	156	SEG20	-2953.71	966.81
10	COM0	-1984.31	-1958.41	68	SEG100	2953.34	-762.94	103	SEG69	1780.44	1958.41	157	SEG19	-2953.71	865.06
11	DUMMY2	-1882.56	-1958.41	69	SEG99	2953.34	-661.19	104	SEG68	1678.69	1958.41	158	SEG18	-2953.71	763.31
12	OSC2	-1780.81	-1958.41	70	SEG98	2953.34	-559.44	105	SEG67	1576.94	1958.41	159	SEG17	-2953.71	661.56
13	AVSS	-1679.06	-1958.41	71	SEG97	2953.34	-457.69	106	SEG66	1475.19	1958.41	160	SEG16	-2953.71	559.81
14	VR	-1577.31	-1958.41	72	SEG96	2953.34	-355.94	107	SEG65	1373.44	1958.41	161	SEG15	-2953.71	458.06
15	VF	-1475.56	-1958.41	73	SEG95	2953.34	-254.19	108	SEG64	1271.69	1958.41	162	SEG14	-2953.71	356.31
16	VCC	-1373.81	-1958.41	74	SEG94	2953.34	-152.44	109	SEG63	1169.94	1958.41	163	SEG13	-2953.71	254.56
17	C-	-1272.06	-1958.41	75	SEG93	2953.34	-50.69	110	SEG62	1068.19	1958.41	164	SEG12	-2953.71	152.81
18	C+	-1170.31	-1958.41	76	SEG92	2953.34	51.06	111	SEG61	966.44	1958.41	165	SEG11	-2953.71	51.06
19	VLL6	-1068.56	-1958.41	77	SEG91	2953.34	152.81	112	SEG60	864.69	1958.41	166	SEG10	-2953.71	-50.69
20	VLL5	-966.81	-1958.41	78	SEG90	2953.34	254.56	113	SEG59	762.94	1958.41	167	SEG9	-2953.71	-152.44
21	VLL4	-865.06	-1958.41	79	SEG89	2953.34	356.31	114	SEG58	661.19	1958.41	168	SEG8	-2953.71	-254.19
22	OSC1	-763.31	-1958.41	80	SEG88	2953.34	458.06	115	SEG57	559.44	1958.41	169	SEG7	-2953.71	-355.94
23	VLL3	-661.56	-1958.41	81	SEG87	2953.34	559.81	116	SEG56	457.69	1958.41	170	SEG6	-2953.71	-457.69
24	VLL2	-559.81	-1958.41	82	SEG86	2953.34	661.56	117	SEG55	355.94	1958.41	171	SEG5	-2953.71	-559.44
25	C1N	-458.06	-1958.41	83	SEG85	2953.34	763.31	118	SEG54	254.19	1958.41	172	SEG4	-2953.71	-661.19
26	C1P	-356.31	-1958.41	84	SEG84	2953.34	865.06	119	SEG53	152.44	1958.41	173	SEG3	-2953.71	-762.94
27	C2N	-254.56	-1958.41	85	SEG83	2953.34	966.81	120	SEG52	50.69	1958.41	174	SEG2	-2953.71	-864.69
28	C2P	-152.81	-1958.41	86	SEG82	2953.34	1068.56	121	SEG51	-51.06	1958.41	175	SEG1	-2953.71	-966.44
29	AVDD	-51.06	-1958.41	87	SEG81	2953.34	1170.31	122	SEG50	-152.81	1958.41	176	SEG0	-2953.71	-1068.19
30	D7	50.69	-1958.41	88	SEG80	2953.34	1272.06	123	SEG49	-254.56	1958.41	177	COM15	-2953.71	-1214.71
31	D6	152.44	-1958.41	89	SEG79	2953.34	1373.81	124	SEG48	-356.31	1958.41	178	COM14	-2953.71	-1316.46
32	D5	254.19	-1958.41	90	SEG78	2953.34	1475.56	125	SEG47	-458.06	1958.41	179	COM13	-2953.71	-1418.21
33	D4	355.94	-1958.41	91	SEG77	2953.34	1577.31	126	SEG46	-559.81	1958.41	180	COM12	-2953.71	-1519.96
34	D3	457.69	-1958.41	92	SEG76	2953.34	1679.06	127	SEG45	-661.56	1958.41	181	COM11	-2953.71	-1621.71
35	D2	559.44	-1958.41	93	SEG75	2953.34	1780.81	128	SEG44	-763.31	1958.41	182	COM10	-2953.71	-1723.46
36	D1	661.19	-1958.41					129	SEG43	-865.06	1958.41				
37	D0	762.94	-1958.41					130	SEG42	-966.81	1958.41				
38	DVSS	864.69	-1958.41					131	SEG41	-1068.56	1958.41				
39	CS	966.44	-1958.41					132	SEG40	-1170.31	1958.41				
40	R/W	1068.19	-1958.41					133	SEG39	-1272.06	1958.41				
41	D/C	1169.94	-1958.41					134	SEG38	-1373.81	1958.41				
42	RES	1271.69	-1958.41					135	SEG37	-1475.56	1958.41				
43	DVDD	1373.44	-1958.41					136	SEG36	-1577.31	1958.41				
44	BP	1475.19	-1958.41					137	SEG35	-1679.06	1958.41				
45	DUMMY1	1576.94	-1958.41					138	SEG34	-1780.81	1958.41				
46	ANNUN2	1678.69	-1958.41					139	SEG33	-1882.56	1958.41				
47	ANNUN1	1780.44	-1958.41					140	SEG32	-1984.31	1958.41				
48	ANNUN0	1882.19	-1958.41					141	SEG31	-2086.06	1958.41				
49	SEG119	1983.94	-1958.41					142	SEG30	-2187.81	1958.41				
50	SEG118	2085.69	-1958.41					143	SEG29	-2289.56	1958.41				
51	SEG117	2187.44	-1958.41					144	DUMMY	-2400.56	2035.37				
52	SEG116	2289.19	-1958.41					145	DUMMY	-2502.31	2035.37				
53	SEG115	2390.94	-1958.41					146	DUMMY	-2604.06	2035.37				
54	SEG114	2492.69	-1958.41					147	DUMMY	-2705.81	2035.37				
55	SEG113	2594.44	-1958.41												
56	SEG112	2696.19	-1958.41												
57	SEG111	2797.94	-1958.41												
58	SEG110	2899.69	-1958.41												

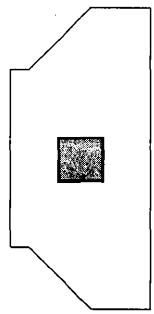
Die Size is 254 mil x 180 mil

MC141539

LCD Segment / Common Driver
CMOS

MC141539 is a CMOS LCD Driver which consists of 4 annunciator outputs and 152 high voltage LCD driving signals (32 commons and 120 segments). It has parallel interface capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD bias voltage generator circuit such that fewer external components are required during application.

- Single Supply Operation, 2.4 V - 3.5 V
- Operating Temperature Range : -30 to 85°C
- Low Current Stand-by Mode (<500nA)
- On Chip Bias Voltage Generator
- 8 Bit Parallel Interface
- Graphic Mode Operation
- On Chip 480 Byte Graphic Display Data RAM
- 120 Segment Drivers, 32 Common Drivers
- Selectable 1/16 or 1/32 Multiplex Ratio
- Selectable on Chip Voltage Doubler and Tripler
- Selectable 1:5 or 1:7 Bias Ratio
- Re-mapping of Row and Column Drivers
- Four Stand Alone Annunciator Driver Circuits
- Selectable LCD Driving Voltage Temperature Coefficients
- 16 Level Internal Contrast Control
- External Contrast Control Provided
- Master Clear RAM
- Standard TAB Package



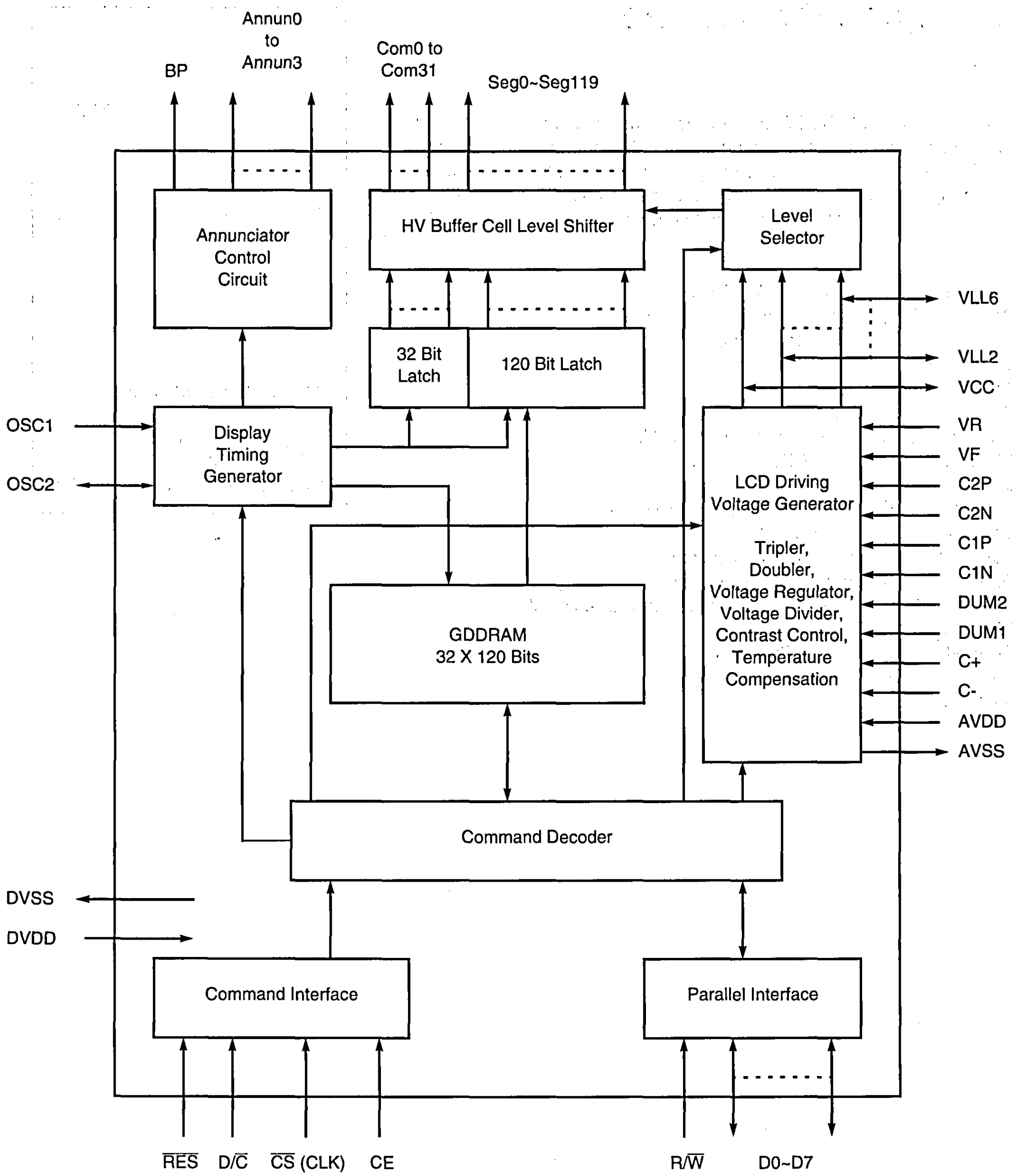
TAB

ORDERING INFORMATION

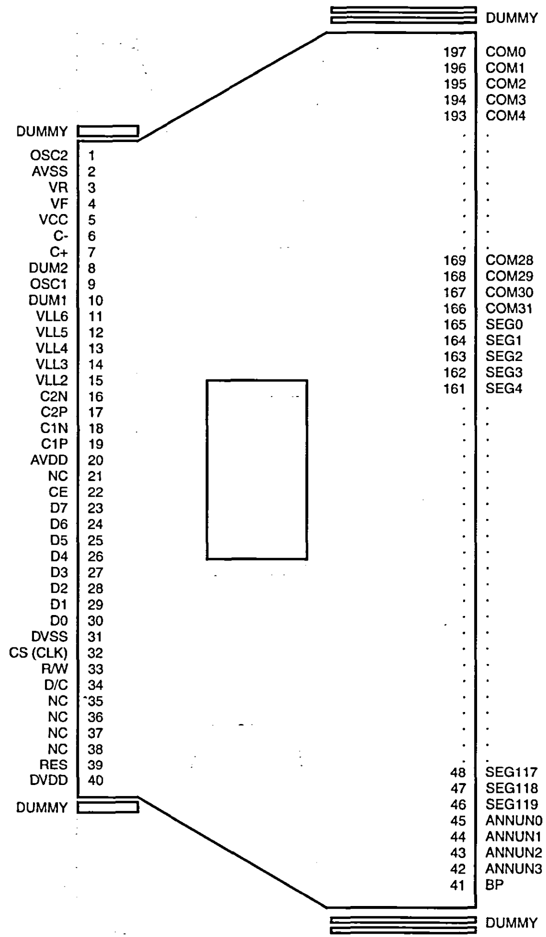
MC141539T1	TAB
MC141539T2	TAB
MCC141539Z	Gold Bump Die

REV 6
3/97

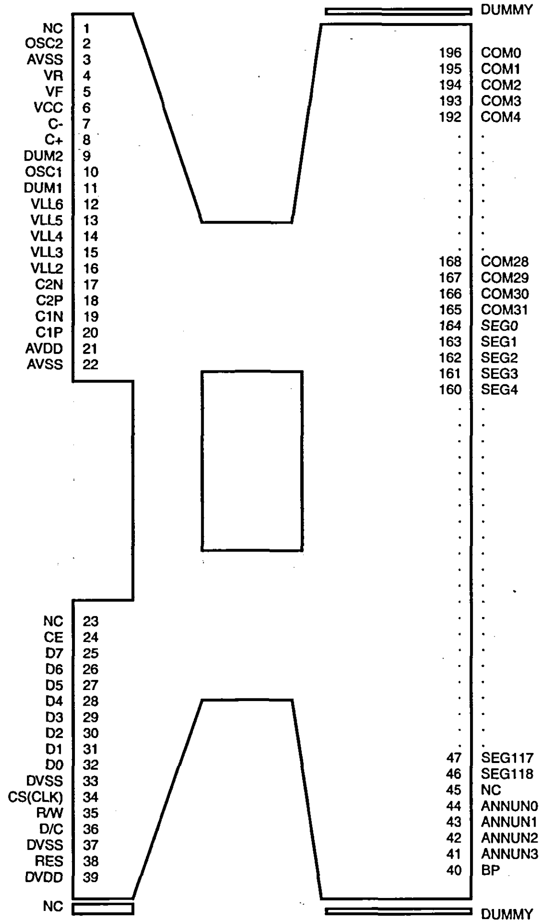
Block Diagram

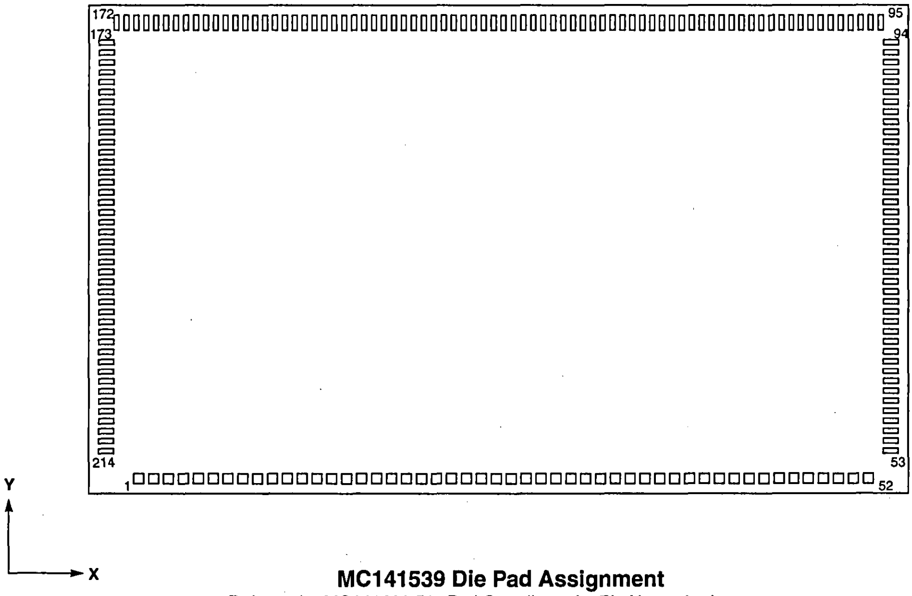


MC141539T1 PIN ASSIGNMENT
(COPPER VIEW)



**MC141539T2R PIN ASSIGNMENT
(COPPER VIEW)**





MC141539 Die Pad Assignment

Refer to the MC141539 Die Pad Coordinate for Pin Name Assignment

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+10.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
 T_{A1} T_{A2}	Operating Temperature For Using Internal Oscillator For Using External Oscillator	 -25 to +85 -30 to +85	 ˚C ˚C
T_{stg}	Storage Temperature Range	-65 to +150	˚C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., *either V_{SS} or V_{DD}). Unused outputs must be left* open.This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
  $V_{SS} = AV_{SS} = DV_{SS}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analogue Circuit)
  $V_{DD} = AV_{DD} = DV_{DD}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analogue Circuit)

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A=25˚C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Supply voltage (Absolute value Referenced to V_{SS})					
DV_{DD}	Operating Range of Logic Circuit Supply DV_{DD}		2.4	3.15	3.5	V
AV_{DD}	Operating Range of Voltage Generator Circuit Supply AV_{DD}		DV_{DD}	3.15	3.5	V
	Supply Current (Measure with V_{DD} fixed at 2.8V)					
I_{AC}	Access Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Accessing, T_{cyc}=1MHz, Osc. Freq.=50kHz, 1/32 Duty Cycle,1/7 Bias.	0	200	300	µA
I_{DP1}	Display Mode Supply Current Drain from Pin AVDD and DVDD.	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=50kHz, 1/32 Duty Cycle,1/7 Bias.	0	76	115	µA
I_{DP2}	Display Mode Supply Current Drain from Pin AVDD and DVDD	Internal DC/DC Converter On, Display On, Tripler Enable, R/W Halt, Osc. Freq.=38.4kHz, 1/32 Duty Cycle,1/7 Bias.	0	55	75	µA
I_{SB1}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD	Display Off, Oscillator Disabled, R/W Halt	0	300	500	nA
I_{SB2}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, External Oscillator and Frequency = 50kHz.	0	2.5	5	µA
I_{SB3}	Stand-by Mode Supply Current Drain from Pin AVDD and DVDD.	Display Off, Oscillator Enable, R/W Halt, Internal Oscillator and Frequency = 50kHz.	0	5	10	µA
	VLCD Voltage (Absolute Value Refer to V_{SS})					
V_{CC1}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Tripler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100µA	-	3*AV_{DD}	10.5	V
V_{CC2}	LCD Driving Voltage Generator Output Voltage at Pin V_{CC}.	Display On, Internal DC/DC Converter Enabled, Doubler Enable, Osc. Freq. = 50kHz, Regulator Enabled, Divider Enabled Iout <= 100µA	-	2*AV_{DD}	7	V
V_{LCD}	LCD Driving Voltage input at pin V_{CC}.	Internal DC/DC Converter Disabled.	AV_{DD}	-	10.5	V
	Output Voltage					
V_{OH1}	Output High Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0.8*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage at Pins D0-D7, Annun0-3, BP and OSC2.	I_{out}=100µA	0	-	0.2*V_{DD}	V
V_{R1}	LCD Driving Voltage Source at Pin VR	Regulator Enabled, I_{out}=50µA	0	-	V_{CC}	V
V_{R2}	LCD Driving Voltage Source at Pin VR	Regulator Disabled, I_{out}=50µA.	-	Floating	-	V
	Input Voltage					
V_{IH1}	Input High Voltage at Pins, $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/C, OSC1 and OSC2.		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage at Pins, $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/C, OSC1 and OSC2.		0	-	0.2*V_{DD}	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, DV_{DD}=2.4-3.15V, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
 V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage. (LCD Driving Voltage Output from Pins VLL6, VLL5, VLL4, VLL3 and VLL2.)	1/5 Bias Ratio, Voltage Divider Enabled, Regulator Enabled.	 - - - - -	 V_R 0.8*V_R 0.6*V_R 0.4*V_R 0.2*V_R	 - - - - -	 V V V V V
V_{LL6} V_{LL5} V_{LL4} DUM2 DUM1 V_{LL3} V_{LL2}		1/7 Bias Ratio, Voltage Divider Enabled, Regulator Enabled	- - - - - - -	V_R 6/7*V_R 5/7*V_R 4/7*V_R 3/7*V_R 2/7*V_R 1/7*V_R	- - - - - - -	V V V V V V V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}		External Voltage Generator, Voltage Divider Disable	0.5V_{CC} 0.5V_{CC} 0.5V_{CC} V_{SS} V_{SS}	- - - - -	V_{CC} V_{CC} V_{CC} 0.5V_{CC} 0.5V_{CC}	V V V V V
	Output Current					
I_{OH}	Output High Current Source from Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=VDD-0.4V	100	-	-	μA
I_{OL}	Output Low Current Drain by Pins D0-D7, Annun0-3, BP and OSC2.	V_{out}=0.4V	-	-	-100	μA
I_{OZ}	Output Tri-state Current Drain Source at pins D0-D7 and OSC2		-1	-	1	μA
I_{IL}/I_{IH}	Input Current at pins $\overline{RES}$, CE, $\overline{CS}$, D0-D7, R/$\overline{W}$, D/$\overline{C}$ OSC1 and OSC2.		-1	-	1	μA
Ron	On Resistance Channel Resistance between LCD Driving Signal Pins (SEG and COM) and Driving Voltage Input Pins (V_{LL2} to V_{LL6}).	During Display on, 0.1V Apply between Two Terminals, V_{CC} within Operating Voltage Range	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD}) Standby Mode, Retained All Internal Configuration and RAM Data		1.8	-	-	V
C_{IN}	Input Capacitance OSC1, OSC2 and All Control Pins		-	5	7.5	pF
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled	-	0.0	-	%
PTC1	Temperature Coefficient 1*	TC1=0, TC2=1, Voltage Regulator Enabled	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	TC1=1, TC2=0, Voltage Regulator Enabled	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled	-	-0.35	-	%
V_{CN}	Internal Contrast Control VR Output Voltage with Internal Contrast Control Selected. 16 Voltage Levels Controlled by Software. Each Level is Typical of 2.25% of the Regulator Output Voltage.	Regulator Enabled, Internal Contrast Control Enabled	-	±18	-	%

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{\text{VR at 50°C - VR at 0°C}}{\text{50°C - 0°C}} \times \frac{1}{\text{VR at 25°C}} \times 100\%$$

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, AV_{DD}=DV_{DD}=2.4 to 3.5V, T_A=25°C)

Total variation of VR ΔV_{RT} is affected by the following factors :

Process variation of Regulator ΔV_R
External V_{DD} Variation contributed to Regulator ΔV_{VDD}
External resistor pair Ra/Rf contributed to Regulator ΔV_{res}

where $\Delta V_{RT} = \sqrt{(\Delta V_R)^2 + (\Delta V_{V_{DD}})^2 + (\Delta V_{res})^2}$

Assume external V_{DD} variation is +/-6% at 3.15V and 1% variation resistor used at application

	TC Level	ΔV_{VDD} (%)	ΔV_R (%)	ΔV_{res} (%)	ΔV_{RT} (%)
Reference Generator	TC0	±6.0	±2.5	±1.414	±6.652
	TC1	±4.0			±4.924
	TC2	±2.5			±3.805
	TC3	±1.4			±3.195

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, V_{DD}=2.4 to 3.15V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
	Oscillation Frequency.	Set Clock Frequency to Low				
F_{OSC1}	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	38.4	-	kHz
F_{ANN1}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	18.75	-	Hz
F_{FRM1}	LCD Driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, Either 1/32 or 1/16 Duty Cycle, Graphic Display Mode	-	66	-	Hz
	Oscillation Freq.	Set Clock Frequency to High				
$Fosc_2$	Oscillation Frequency of Display Timing Generator with 60Hz Frame Frequency.		-	50	-	kHz
F_{ANN2}	Annunciator Display Frequency (with 50% duty cycle) from Pins Annun0-3 and BP		-	24.4	-	Hz
F_{FRM2}	LCD driving Signal Frame Frequency.	Either External Clock Input or Internal Oscillator Enable, Either 1/32 Duty Cycle	-	65	-	Hz
OSC	Internal Oscillation Frequency Internal OSC Oscillation Frequency with Different Value of Feedback Resistor.	Internal Oscillator Enabled. V_{DD} within Operation Range	See Figure 1 for the relationship			

Set Clock Frequency to Slow : F_{FRM1}=F_{OSC1}/576
Set Clock Frequency to Normal : F_{FRM2}=F_{OSC2}/768

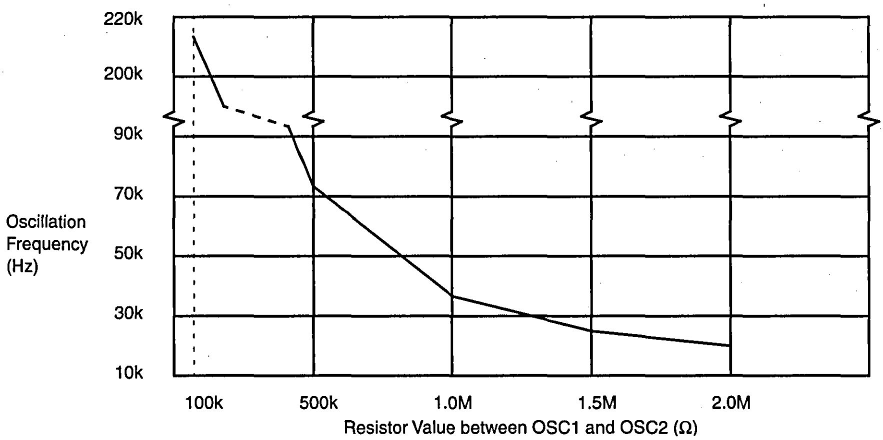


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

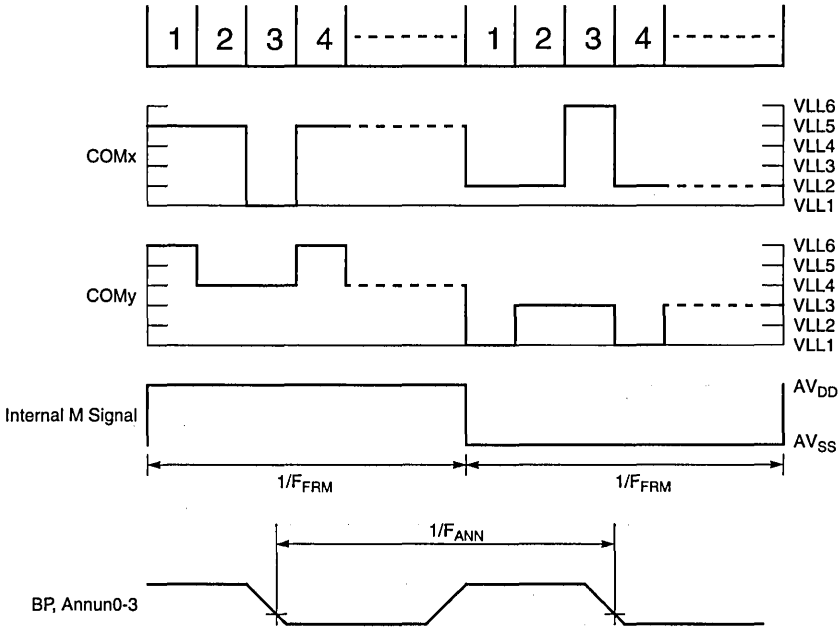


Figure 2. LCD Driving Signal Timing Diagram

TABLE 2a. Parallel Timing Characteristics (Write Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	290	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DS}	Data Setup Time	290	-	-	ns
t_{DH}	Data Hold Time	0	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

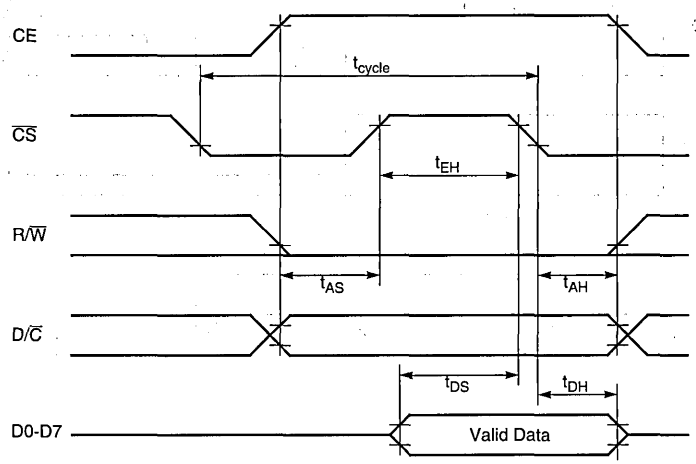


Figure 3. Timing Characteristics (Write Cycle)

TABLE 2b. Parallel Timing Characteristics (Read Cycle) (T_A=-10 to 60˚C, DV_{DD}=2.4 to 3.15V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	375	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{DS}	Data Setup Time	-	-	350	ns
t_{DH}	Data Hold Time	7	-	-	ns
t_{AH}	Address Hold Time	5	-	-	ns

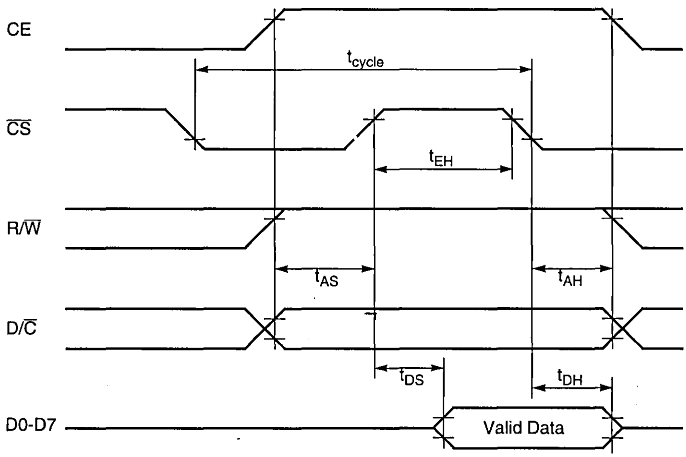


Figure 4. Timing Characteristics (Read Cycle)

PIN DESCRIPTIONS

D/$\overline{C}$ (Data / Command)
This input pin acknowledge the driver the input at D0-D7 is data or command. Input High for data while input Low for command.

$\overline{CS}$ (CLK) (Input Clock)
This pin is normal Low clock input. Data on D0-D7 is latched at the falling edge of CS.

$\overline{RES}$ (Reset)
An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

CE (Chip Enable)
HIGH input to this pin to enable the control pins on the driver.

D0-D7
This bi-directional bus is used for data / command transferring.

R/$\overline{W}$ (Read/Write)
This is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/W input Low indicates a write operation to the display data RAM or to the internal setup registers.

OSC1 (Oscillator Input)
For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value is placed between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)
This is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2
Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit. For internal Voltage Divider enabled, a 0.1 µF capacitor to AV_{SS} is required on each pin.

DUM1 and DUM2
If internal Voltage Divider is enabled with 1/7 bias selected, a 0.1 µF capacitor to AV_{SS} is required on each pin. Otherwise, pull these two pin to AV_{SS}

C1N and C1P
If Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required to connect these two pins.

C2N and C2P
If 32 Mux is selected and Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required between these two pins. Otherwise, leave these pin open.

C+ and C-
If internal divider circuit is enabled, a 0.1 µF capacitor is required to connect between these two pins.

VR and VF
This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between VR and VF, a gain control resistor placed between VF and AVSS, a 10 µF capacitor placed between VR and AVSS. (Refer to the Application Circuit Section)

COM0-COM31 (Row Drivers)
These pins provide the row driving signal to LCD panel. Com0-Com31 are used in 32 mux configuration. Com0-Com15 are used in 16 mux configuration. They output 0V during display off.

SEG0-SEG119 (Column Drivers)
These 120 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

BP (Annunciator Backplane)
This pin combines with Annun0-Annun3 pins to form annunciator driving part. When the annunciator circuit is enabled, it will output square wave of F_{ANNn} Hz. It outputs low when oscillator is disabled.

Annun0 - Annun3 (Annunciator Frontplanes)
These pins are four independent annunciator driving outputs. The enabled annunciator outputs from its corresponding pin a F_{ANNn} Hz square wave which is 180 degrees out of phase with BP. Disabled annunciator output from its corresponding pin an square wave in-phase with BP. When oscillator is disabled, all these pins output 0V.

AVDD and AVSS
AVDD is the positive supply to the LCD bias voltage generator. AVSS is ground.

VCC
For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Positive power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS
Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command.

Data is directed to this module based upon the input of the D/C pin. If D/C high, data is written to Graphic Display Data RAM (GDDRAM). D/C low indicates that the input at D0-D7 is interpreted as a Command.

CE is the master chip selection signal. A High input enable the input lines ready to sample signals. Reset is of same function as Power ON Reset (POR). Once RES received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel Interface

The parallel interface consists of 8 bi-directional data lines (D0-D7), R/W, and the CS. The R/W input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/W input Low indicates a write to Display Data RAM or Internal Command Registers depending on the status of D/C input. The CS input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (120x32 = 3840 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

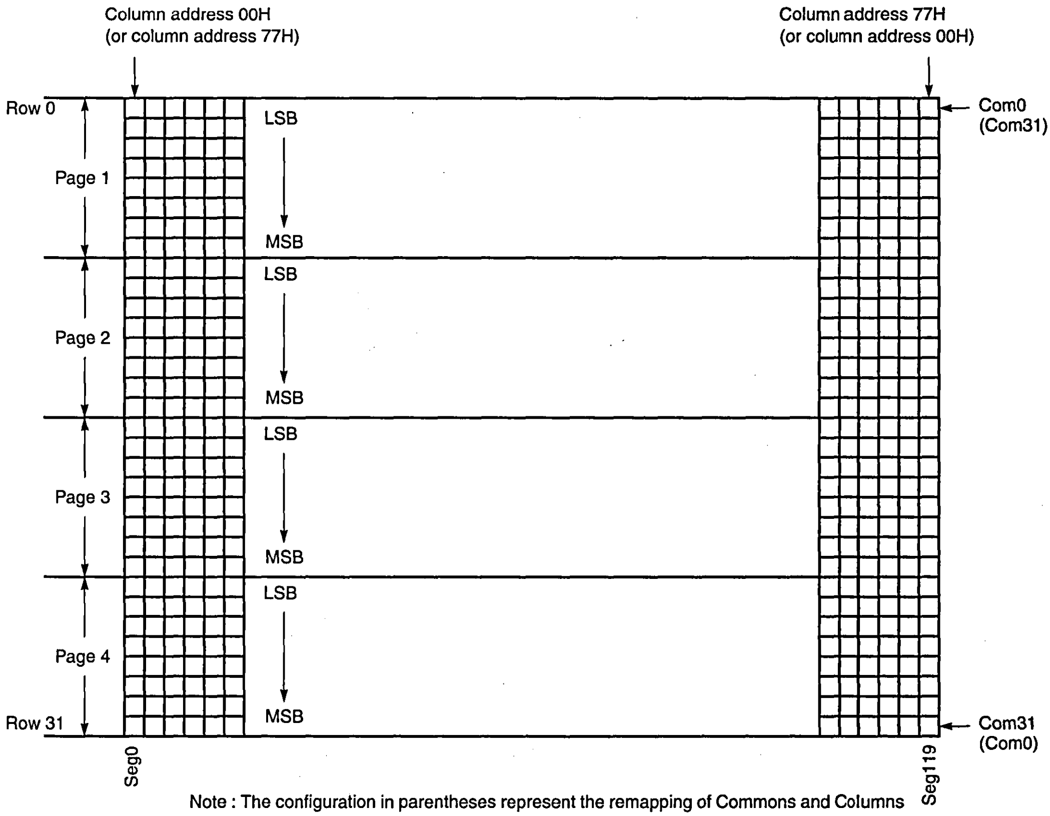


Figure 5. Graphic Display Data RAM (GDDRAM) Address Map

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 15 kHz to 50 kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

Annunciator Control Circuit

The LCD waveform of the 4 annunciators and BP are generated by this module. The 4 independent annunciators are enabled by software command. Annunciator is also controlled by oscillator circuit too. the annunciators pins output 0V when oscillator is disabled. Annunciator output waveform shown in Figure 7.

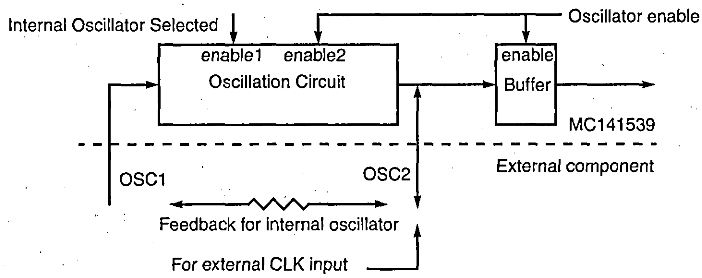


Figure 6. Oscillator Circuitry

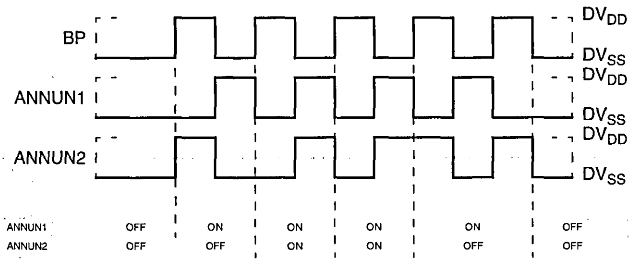


Figure 7. Annunciators and BP Display Waveform

LCD Driving Voltage Generator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. Voltage Doubler and Voltage Tripler
   To generate the Vcc voltage. Either Doubler or Tripler can be enabled.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. It can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
5. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.
6. Bias Ratio Selection circuitry
   Software control of 1/5 and 1/7 bias ratio to match the characteristic of LCD panel.

All blocks can be individually turned off if external voltage generator is employed

32 Bit Latch / 120 Bit Latch

A 152 bit long register which carries the display signal information. First 32 bits are Common driving signals and other 120 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shift-er)

HV Buffer Cell works as a level shift-er which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

Reference Generator

Two reference generators on chip to provide reference voltage to the regulator circuitry. The VR (LCD driving voltage) stability is affected by the performance of the reference voltage. For details on it's performance, please refer to electrical characteristic.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 8a, 8b and 8c illustrate the desired multiplex scheme.

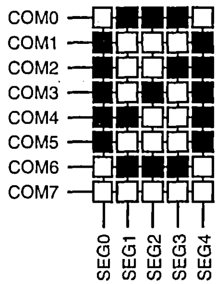


Figure 8a. LCD Display Example "0"

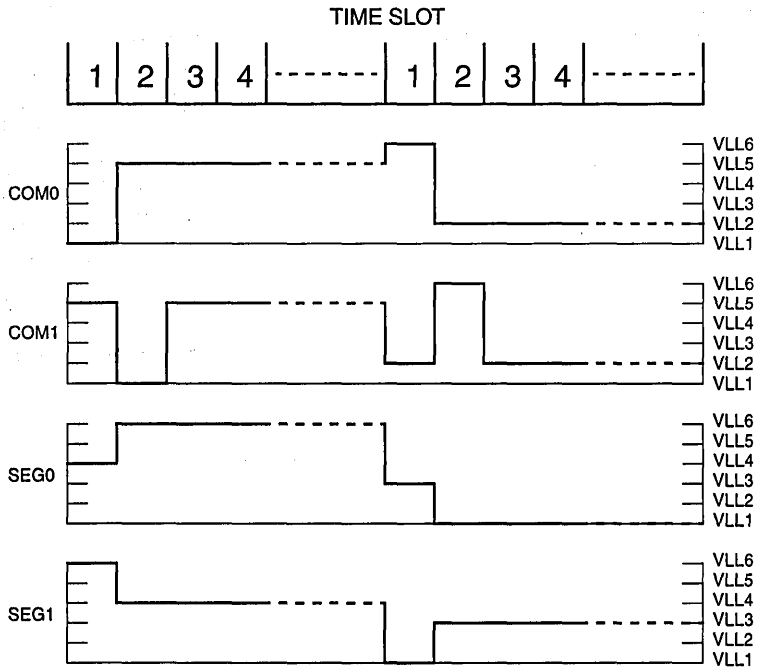


Figure 8b. LCD Driving Signal from MC141539

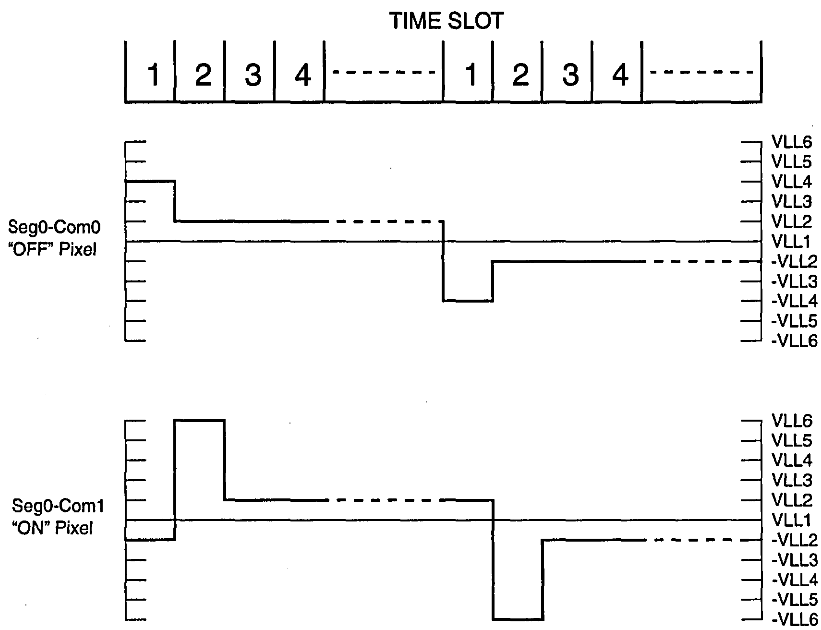


Figure 8c. Effective LCD waveform on LCD pixel

Command Description

Display On/Off (Display Mode / Stand-by Mode)

The Display On command turns the LCD Common and Segment outputs on and has no effect to the annunciator output. This command causes the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : "Oscillator On" command should be sent before "Display On" is selected)

The Display Off command turns the display off and the states of the LCD driver are as follow during display off :

1. The Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The status of the Annunciators and Oscillator are not affected by this command.

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-77H (120 columns). The column address will be increased by one automatically after a read or write operation. Refer "Address Enlacement Table" and command "Set GDDRAM Page Address".

Set GDDRAM Page Address

This command positions the row address to 1 of 4 possible positions in GDDRAM. Refer to figure 5.

Master Clear GDDRAM

This command is to clear the 480 byte Display Data RAM by setting the RAM data to zero. Issue this command followed by a dummy write command.

Set Vertical Scroll Value

This command is used to scroll the screen vertically with scroll value 0 to 31. With scroll value equals to 0, Row 0 of GDDRAM is mapped to Com0 and Row 1 through Row 31 are mapped to Com1 through Com31 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to Com0, then Row 2 through Row 31 will be mapped to Com1 through Com30 respectively and Row 0 will be mapped to Com31.

Save / Restore Column Address

With bit option = 1 in this command, the Save / Restore Column Address command saves a copy of the Column Address of GDDRAM. With bit option = 0, this command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of GDDRAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 119 of GDDRAM mapped to Seg0-Seg119 respectively;
2. Column 0 - Column 119 of GDDRAM mapped to Seg119-Seg0 respectively.

Detail information please refer to section "Display Output Description".

Set Row Mapping

This instruction selects the mapping of GDDRAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row 31 of GDDRAM to Com0 - Com31 respectively;
2. Row 0 - Row 31 of GDDRAM to Com31 - Com0 respectively.

See section "Display Output Description" for related information.

Set Annunciator Control Signals

This command is used to control the active states of the 4 stand alone annunciator drivers.

Set Oscillator Enable / Disable

This command is used to either turn on / off Oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command "Set Display On/Off" and "Set Annunciator On/Off". See command "Ext/Int Oscillator" for more information

Set External / Internal Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Clock Frequency

Use this command to choose from two different oscillation frequencies (50kHz or 38.4kHz) to get the 60 Hz frame frequency. With frequency high, 50 kHz clock frequency is preferred. 38.4kHz clock frequency (low frequency) enable for power saving purpose.

Set Internal DC/DC Converter On/Off

Use this command to select the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external Vcc is provided.

Set Voltage Doubler / Tripler

Use this command to choose Voltage Doubler or Tripler when the Internal DC/DC Converter is enabled.

Set Internal Regulator On/Off

Choose bit option 0 to disable the Internal Regulator. Choose bit option 1 to enable Internal Regulator which consists of the internal contrast control and temperature compensation circuits.

Set Internal Voltage Divider On/Off

If the Internal Voltage Divider is disabled, external bias can be used for V_{LL6} to V_{LL2}. If the Internal Voltage Divider is enabled, the internal circuit will automatically select the correct bias level according to the number of multiplex. Refer to command "Set Bias Ratio ".

Set Duty Cycle

This command is to select 16 mux or 32 mux display. When 16 mux is enabled, the unused 16 common outputs will be swinging between VLL2 and VLL5 for dummy scan purpose and doubler will be used.

Set Bias Ratio

This command sets the 1/5 bias or 1/7 bias for the divider output. The selection should match the characteristic of LCD Panel.

Set Internal Contrast Control On/Off

This command is used to turn on or off the internal control of delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after POR.

Set Contrast Level

This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use.

Read Contrast Value

This command allows the user to read the current contrast level value. With $R/\overline{W}$ input high (READ), $D/\overline{C}$ input low (COMMAND) and D7 D6 D5 D4 are equal to 0 0 0 1, the value of the internal contrast value can be read on D0-D3 at the falling edge of CS.

Set Temperature Coefficient

A temperature gradient selector circuit controlled by two control bits TC1 and TC2. This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

COMMAND TABLE

Bit Pattern	Command	Comment
$000000X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using X_1X_0 as address bits. X_1X_0=00 : page 1 (POR) X_1X_0=01 : page 2 X_1X_0=10 : page 3 X_1X_0=11 : page 4
$0001X_3X_2X_1X_0$	Set Contrast Level	Set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR.
$0001X_3X_2X_1X_0$	Read Contrast Value	With $D/\overline{C}$ pin input Low, $R/\overline{W}$ pin input high, and D7 D6 D5 D4 pins equal to 0001 at the rising edge of $\overline{CS}$, the value of the internal contrast register will be latched out at D3 D2 D1 D0 pins, i.e. $X_3X_2X_1X_0$, at the rising edge of $\overline{CS}$.
$0010000X_0$	Set Voltage Doubler / Tripler	X_0=0: Select Voltage Tripler (POR) X_0=1: Select Voltage Doubler
$0010001X_0$	Set Column Mapping	X_0=0 : Col0 to Seg0 (POR) X_0=1 : Col0 to Seg119
$0010010X_0$	Set Row Mapping	With duty cycle is 1/32 X_0=0 : Row0 to Com0 (POR) X_0=1: Row0 to Com31 With duty cycle is 1/16 X_0=0 : Row0 to Com0 X_0=1:Row0 to Com15
$0010011X_0$	Reserved	
$0010100X_0$	Set Display On/Off	X_0=0: display off (POR) X_0=1: display on
$0010101X_0$	Set Internal DC/DC Converter On/Off	X_0=0: Internal DC/DC Converter off (POR) X_0=1: Internal DC/DC Converter on
$0010110X_0$	Set Internal Regulator On/Off	X_0=0: Internal Regulator off (POR) X_0=1: Internal Regulator on When the application employs external contrast control, the internal contrast control, temperature compensation and the Regulator must be enabled.
$0010111X_0$	Set Internal Voltage Divider On/Off	X_0=0: Internal Voltage Divider off (POR) X_0=1: Internal Voltage Divider on When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal Contrast Control off (POR) X_0=1: Internal Contrast Control on Internal contrast circuits can be disabled if external contrast circuits is preferred.
$0011001X_0$	Set Clock Frequency	X_0=0 : low frequency (38.4kHz) (POR) X_0=1 : high frequency (50kHz)
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
$0011011X_0$	Master Clear GDDRAM	Master clear entire GDDRAM
$0011100X_0$	Set Bias Ratio	X_0=0: set 1/7 bias (POR) X_0=1: set 1/5 bias
$0011101X_0$	Reserved.	X_0=0: normal operation (POR) X_0=1: test mode (Note: Make sure to set X_0=0 during application)
$001110X_1X_0$	Reserved	X_1X_0=00: Reserved X_1X_0=01: Reserved (POR) X_1X_0=10: Reserved X_1X_0=11: Reserved

Bit Pattern	Command	Comment
$010X_4X_3X_2X_1X_0$	Set Vertical Scroll Value	Use $X_4X_3X_2X_1X_0$ as number of lines to scroll. Scroll value = 0 upon POR
$01100A_1A_0X_0$	Set Annunciator Control Signals	A_1A_0=00: select annunciator 1 (POR) A_1A_0=01: select annunciator 2 A_1A_0=10: select annunciator 3 A_1A_0=11: select annunciator 4 X_0=0: turn selected annunciator off (POR) X_0=1: turn selected annunciator on
$0110100X_0$	Set Duty Cycle	X_0=0: 1/32 duty and tripler enabled (POR) X_0=1: 1/16 duty and doubler enabled
$0110101X_0$	Reserved	X_0=0: Reserved X_0=1: Reserved
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=01: -0.18% X_1X_0=10: -0.22% X_1X_0=11: -0.35%
$0111000X_0$	Increase / Decrease Contrast Value	X_0=0: Decrease by one level X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.
$0111001X_0$	Reserved	
$0111010X_0$	Reserved	
$0111011X_0$	Reserved	X_0=0: normal operation (POR) X_0=1: test mode select (Note: Make sure to set X_0=0 during application)
$0111100X_0$	Reserved	
$0111101X_0$	Set Internal / External Oscillator	X_0=0: internal oscillator(POR) X_0=1: external oscillator Internal oscillator circuit is automatically enabled if resistors are placed at OSC1 and OSC2. For external oscillator, simply feed clock in OSC2.
$0111110X_0$	Reserved	
$0111111X_0$	Set Oscillator Disable / Enable	X_0=0: disable oscillator (POR) X_0=1: enable oscillator. This is the master control fro oscillator circuitry. This command should be issued after the "Set External / Internal Oscillator" command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.

Data Read / Write

To read data from the GDDRAM, input High to $R/\overline{W}$ pin and $D/\overline{C}$ pin. Data is valid at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to $R/\overline{W}$ pin and High to $D/\overline{C}$ pin. Data is latched at the falling edge of $\overline{CS}$. And the GDDRAM column address pointer will be increased by one automatically.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the "Commands Required for R/W Actions on RAM" Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.

Remarks : *1. Refer to the command "Read Contrast Value".
*2. If write data is issued after Command Clear RAM, Address increase is not applied.
*3. Column Address will be wrapped round when overflow.

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set Clock Frequency	Low	*1
Set Oscillator Enable	Disable	
Set Annunciator Control Signals	All annunciators off	*1
Set Duty Cycle	1/32 duty	*1
Set Bias Ratio	1/7 bias	*1
Set DC/DC Converter On	Off	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Increase Contrast Value	Contrast Value = 0	*1, *2, *3
Set Internal Voltage Divider On	Off	
Set Segment Mapping	Seg. 0 = Col. 0	
Set Common Mapping	Com. 0 = Row 0	
Set Vertical Scroll Value	Scroll Value = 0	
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Regulator is enabled.

Commands Required for Display Mode Setup

Display Mode	Commands Required	
Display Mode	Set External / Internal Oscillator, Set Oscillator Enable, Set Display On.	(0111101X_0)* (01111111)* (00101001)*
Annunciator Display	Set External / Internal Oscillator, Set Oscillator Enable, Set Annunciator Control Signals.	(0111101X_0)* (01111111)* (01100$A_1A_0X_0$)*
Standby Mode 1.	Set Display Off, Set Oscillator Disable.	(00101000)* (01111110)*
Standby Mode 2.	Set External Oscillator, Set Annunciator Control Signals, Set Display Off, Set Oscillator Enable.	(01111101)* (01100$A_1A_0X_0$)* (00101000)* (01111111)*
Standby Mode 3.	Set Internal Oscillator, Set Annunciator Control Signals, Set Display Off, Set Oscillator Enable.	(01111100)* (01100$A_1A_0X_0$)* (00101000)* (01111111)*

Other Related Command with Display Mode : Set Duty Cycle, Set Column Mapping, Set Row Mapping, Set Vertical Scroll Value.

Commands Related to Voltage Generator :
Set Oscillator Disable/Enable, Set Internal Regulator On/Off, Set Duty Cycle, Set Temperature Coefficient, Set Internal Contrast Control On/Off, Increase/Decrease Contrast Level, Set Internal Voltage Divider On/Off, Set Bias Ratio, Set Display On/Off, Set Reference Voltage Generator, Set VDD Reference, Set Contrast Level

* No need to resend the command again if it is set previously

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data	$(000000X_1X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	$(0011010X_0)$
Increase GDDRAM Address.	Dummy Read Data	$(X_7X_6X_5X_4X_3X_2X_1X_0)$
Master Clear GDDRAM	Master Clear GDDRAM Dummy Write Data	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$

* No need to resend the command again if it is set previously.

Display Output Description by Working Example

This is an example of output pattern on the LCD panel. Figure 9b and 9c are data map of GDDRAM and the output pattern on the LCD display with different command enable.

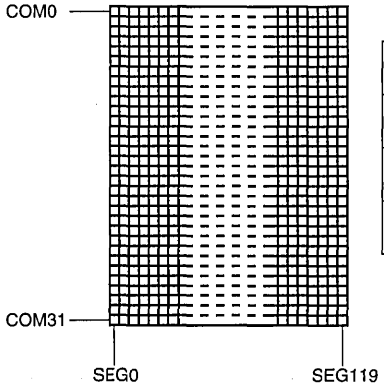
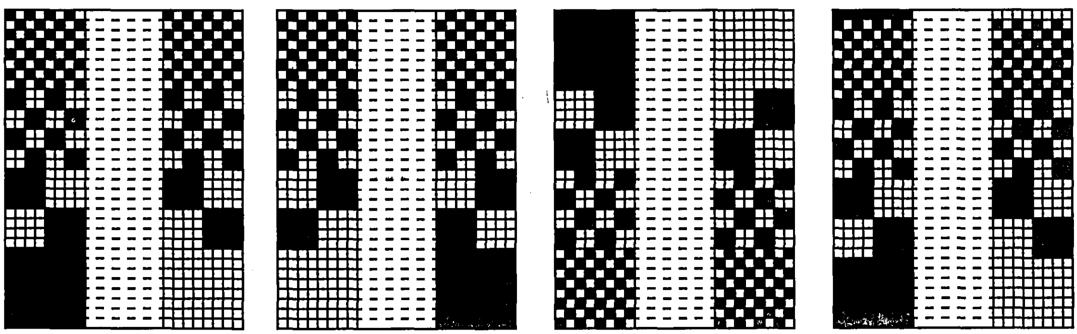


Figure 9a

		Content of GDDRAM
PAGE 1	Upper Nibble	5 A 5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
	Lower Nibble	5 A 5 A 5 A 5 A 5 A - - - - - - - - - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
PAGE 2	Upper Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - - - - - - - - - C C 3 3 C C 3 3 C C
	Lower Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - - - - - - - - - C C 3 3 C C 3 3 C C
PAGE 3	Upper Nibble	0 0 0 0 F F F F 0 0 - - - - - - - - - - - - - - - - - F F 0 0 0 0 F F F F
	Lower Nibble	F F F F 0 0 0 0 F F - - - - - - - - - - - - - - - - - 0 0 F F F F 0 0 0 0
PAGE 4	Upper Nibble	F F F F F F F F 0 0 - - - - - - - - - - - - - - - - - F F 0 0 0 0 0 0 0 0
	Lower Nibble	F F F F F F F F 0 0 - - - - - - - - - - - - - - - - - F F 0 0 0 0 0 0 0 0

Figure 9b



Column remap disable
Row re-map disable

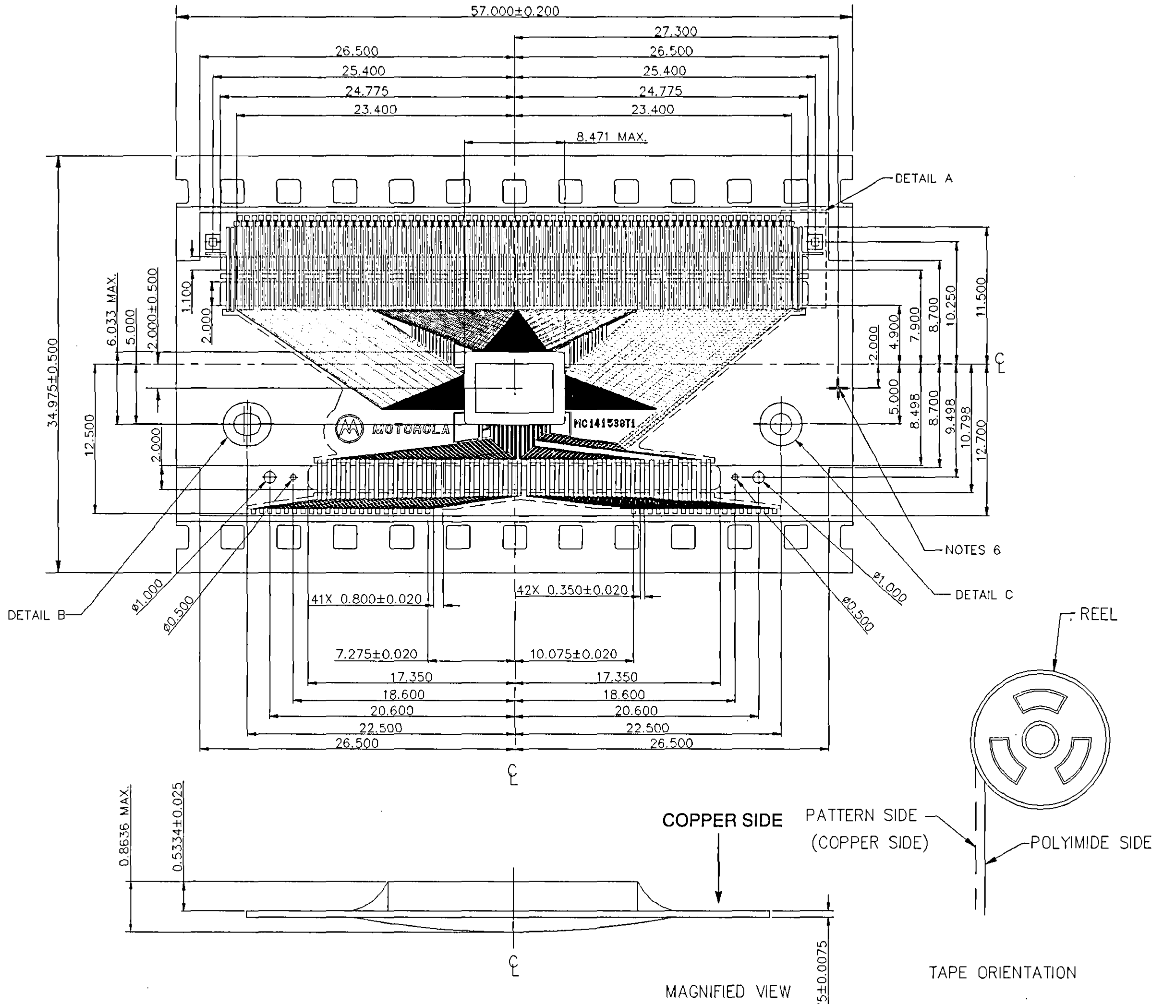
Column remap enable
Row re-map disable

Column remap disable
Row re-map enable

Column remap disable
Row re-map disable
Scroll Value = 31

Figure 9c. Examples of LCD display with different command enabled

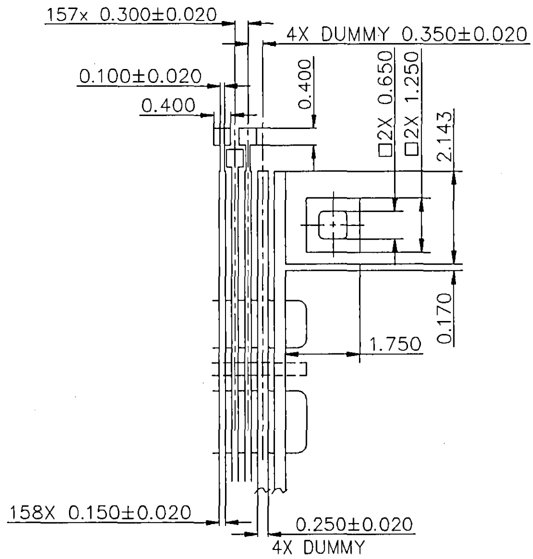
PACKAGE DIMENSIONS
MC141539T1
TAB PACKAGE DIMENSION - 1



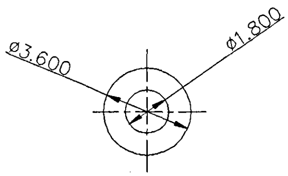
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY Ø 2.0 MM HOLE.
7. 12 SPROCKET HOLES DEVICE

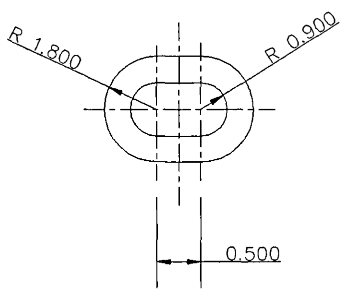
PACKAGE DIMENSIONS
MC141539T1
TAB PACKAGE DIMENSION - 2



DETAIL A

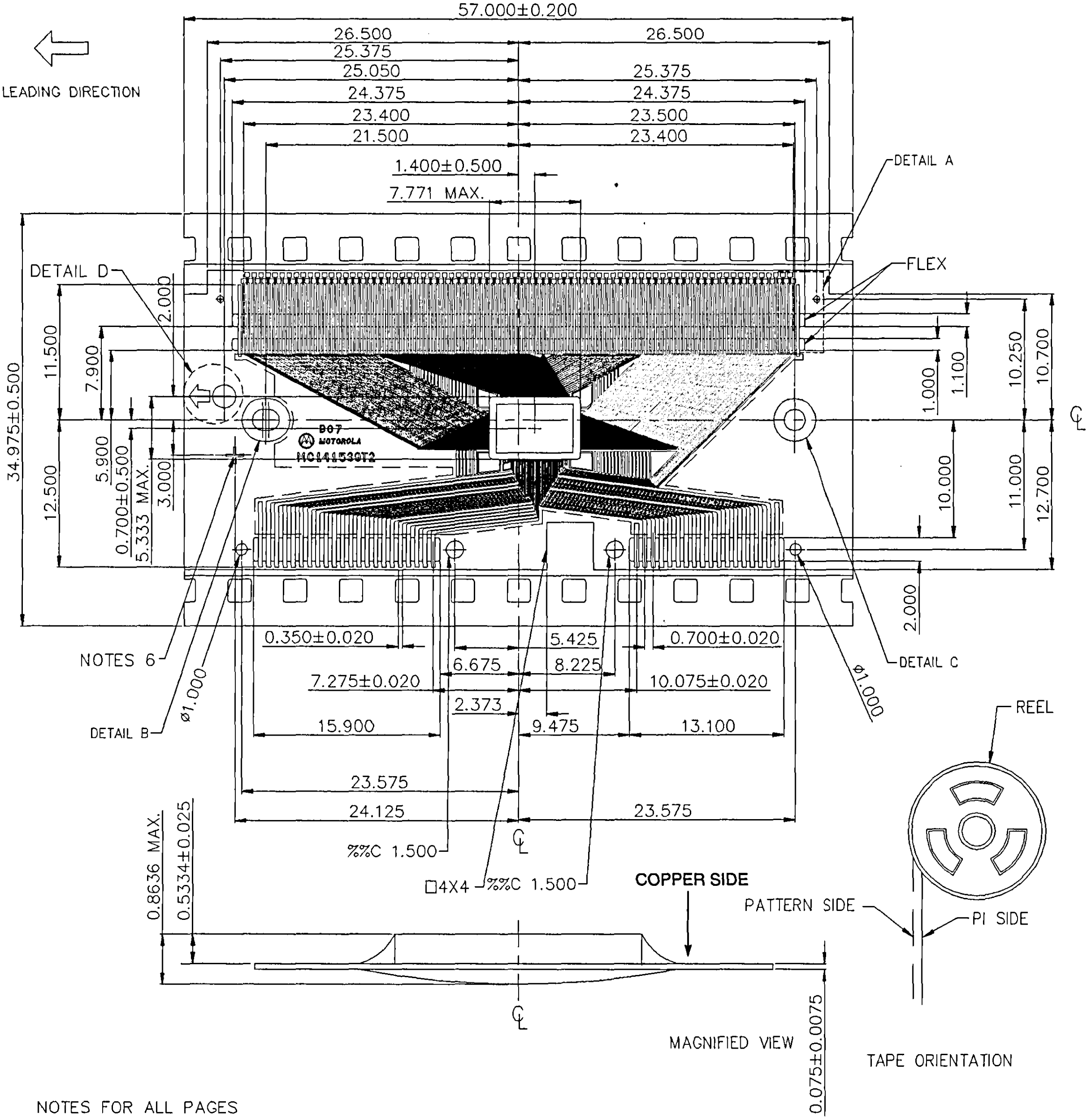


DETAIL C



DETAIL B

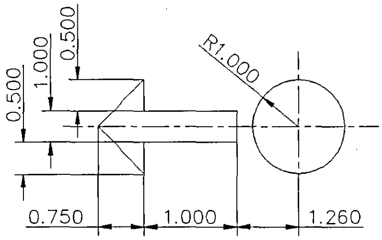
PACKAGE DIMENSIONS
MC141539T2
TAB PACKAGE DIMENSION - 1
98ASL00244A ISSUE0



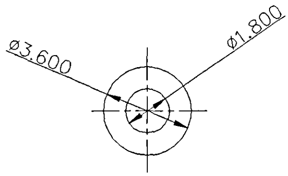
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY Ø 2.0 MM HOLE.
7. 12 SPROCKET HOLES DEVICE

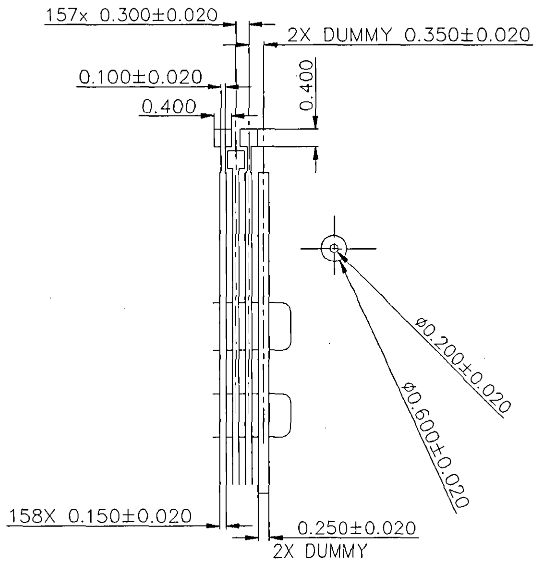
PACKAGE DIMENSIONS
MC141539T2
TAB PACKAGE DIMENSION - 2



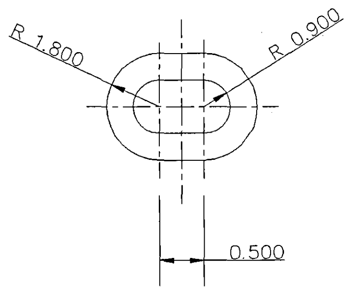
DETAIL D



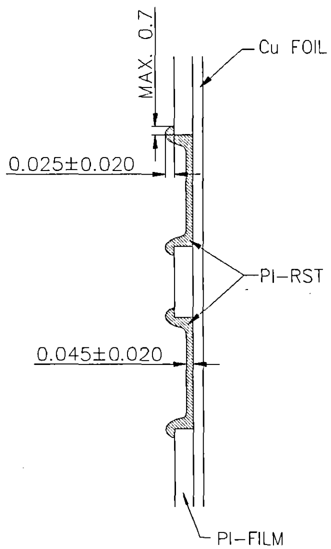
DETAIL C .



DETAIL A



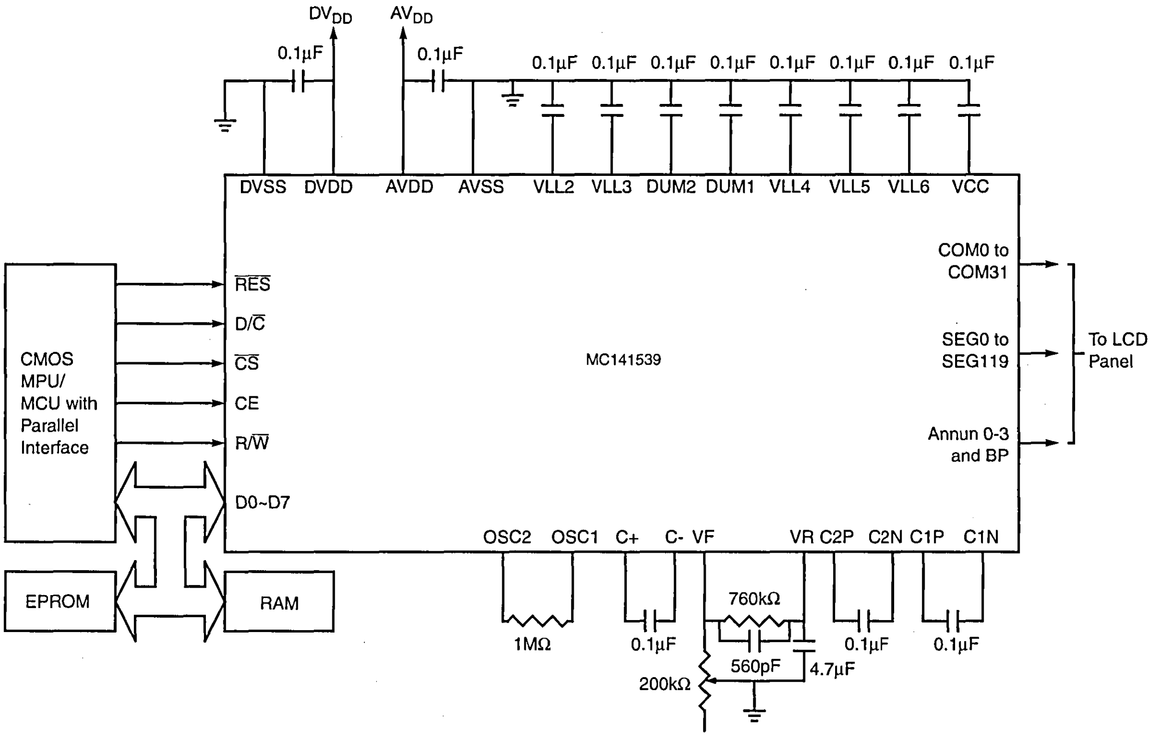
DETAIL B



FLEX MATERIAL DETAIL

Application Circuit

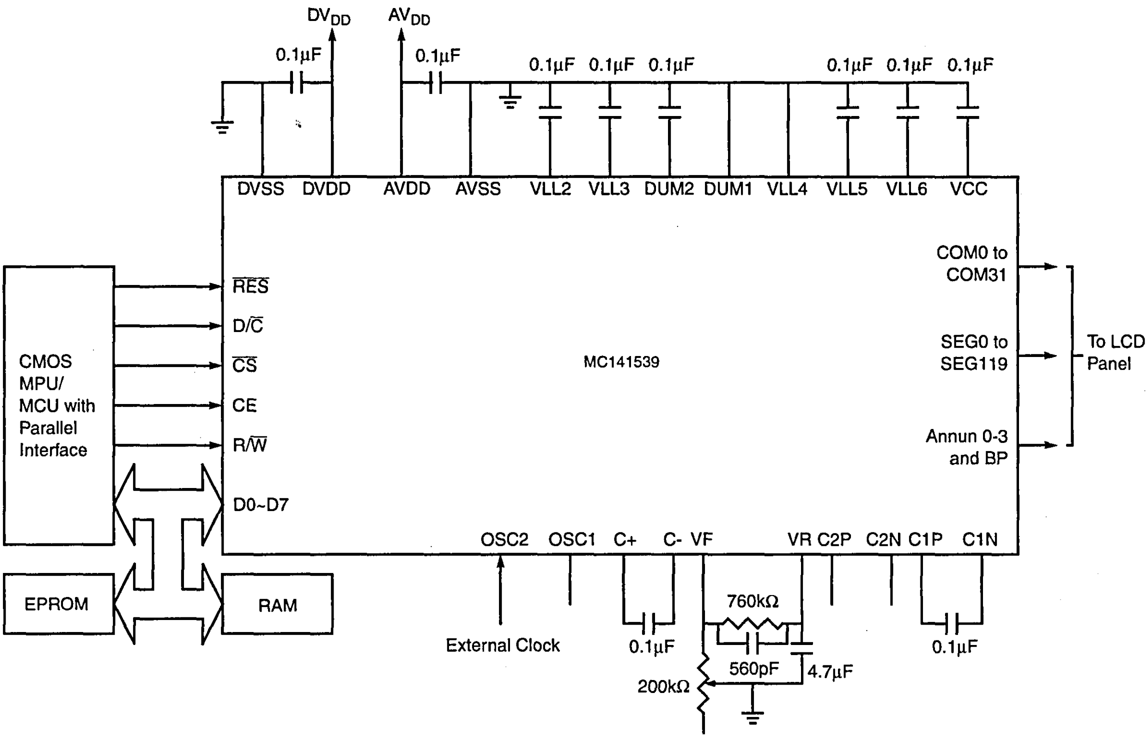
32 MUX Display with Analog Circuitry enabled, Tripler enabled and 1/7 bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

Application Circuit

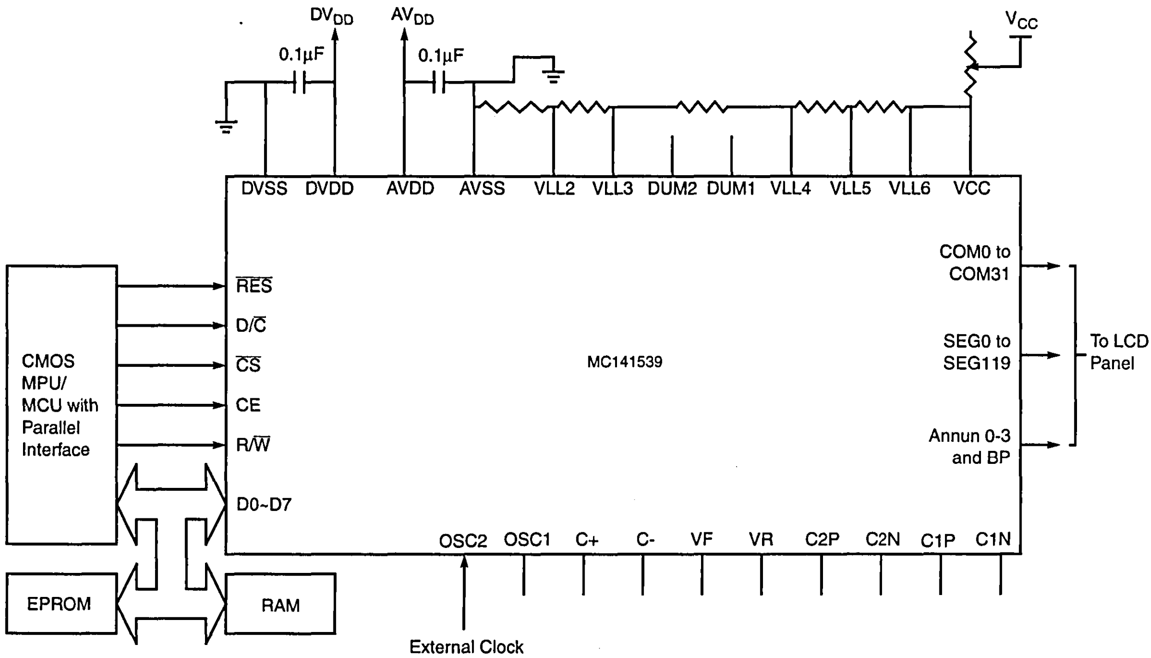
16 MUX Display with Analog Circuitry enabled, Tripler disabled and 1/5 bias



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

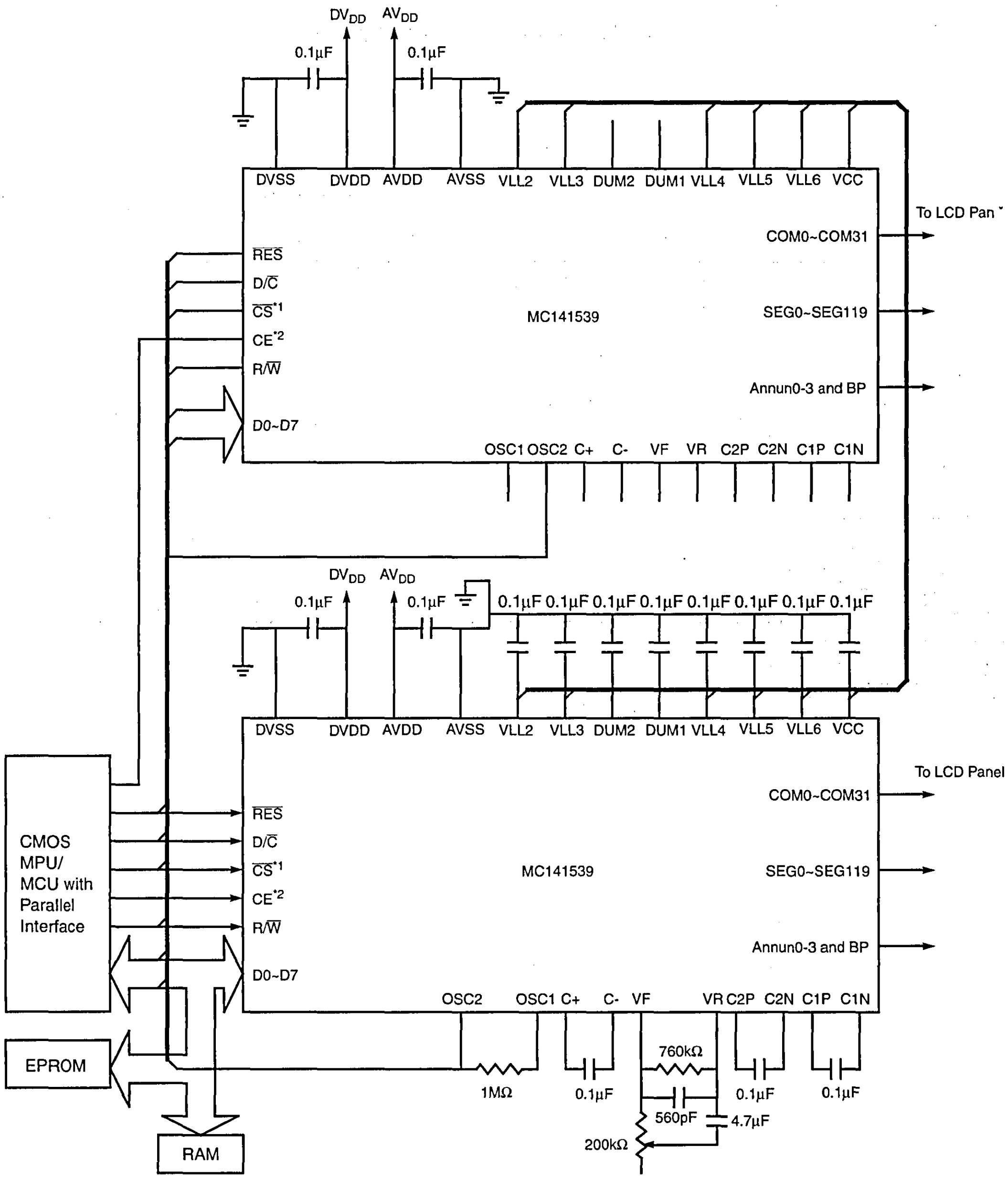
Application Circuit

16/32 MUX Display with Analog Circuitry disabled



Remark :
1. VR and VF can be left open Regulator Disable.
2. $\overline{CS}$ pin low at Standby Mode.

64 Lines 32 MUX Display Application - 1

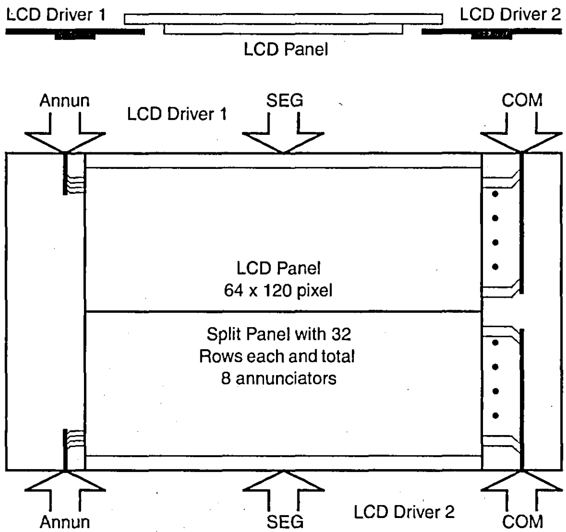


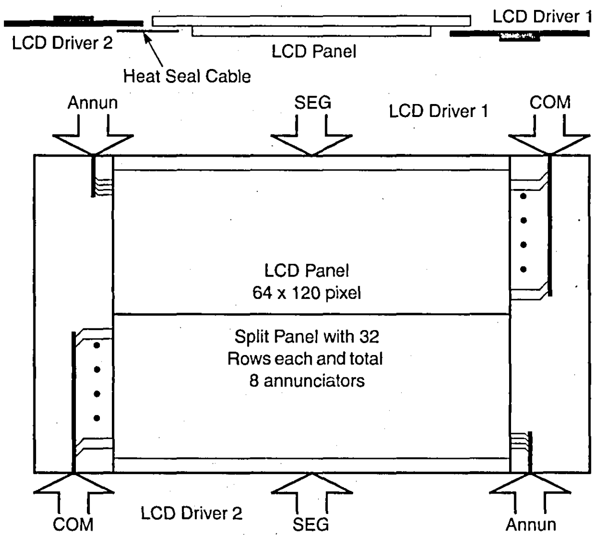
Remark :
1. $\overline{CS}$ pin low at Standby Mode.
2. Two CE signal are needed

64 Lines 32 MUX Display Application - 2

64 lines 32 MUX Display Operation

Master Chip -- analog circuitry enabled,
Slave Chip -- analog circuitry disable.





MC141539 Die Pad Coordinate

Pin	Name	x (um)	y (um)
1	DUMMY	-2730.23	-1862.58
2	DUMMY	-2569.28	-1862.58
3	ANNUN0	-2413.88	-1750.84
4	ANNUN1	-2312.5	-1750.84
5	ANNUN2	-2211.12	-1750.84
6	ANNUN3	-2109.74	-1750.84
7	BP	-2008.36	-1750.84
8	DVDD	-1906.98	-1750.84
9	RESET#	-1805.6	-1750.84
10	DVSS	-1704.22	-1750.84
11	D/C#	-1602.84	-1750.84
12	R/W#	-1501.46	-1750.84
13	CS#	-1400.08	-1750.84
14	DVSS	-1298.7	-1750.84
15	D0	-1197.32	-1750.84
16	D1	-1095.94	-1750.84
17	D2	-994.56	-1750.84
18	D3	-893.18	-1750.84
19	D4	-791.8	-1750.84
20	D5	-690.42	-1750.84
21	D6	-589.04	-1750.84
22	D7	-487.66	-1750.84
23	CE	-386.28	-1750.84
24	AVSS	-284.9	-1750.84
25	AVDD	-183.52	-1750.84
26	C1P	-82.14	-1750.84
27	C1N	19.24	1750.84
28	C2P	120.62	-1750.84
29	C2N	222	-1750.84
30	VLL2	323.38	-1750.84
31	VLL3	424.76	-1750.84
32	AVSS	526.14	-1750.84
33	AVSS	627.52	-1750.84
34	VLL4	728.9	-1750.84
35	VLL5	830.28	-1750.84
36	VLL6	931.66	-1750.84
37	DUM1	1033.04	-1750.84
38	OSC1	1134.42	-1750.84
39	DUM2	1235.8	-1750.84
40	CPLUS	1337.18	-1750.84
41	CMINUS	1438.56	-1750.84
42	VCC	1539.94	-1750.84
43	VF	1641.32	-1750.84
44	VR	1742.7	-1750.84
45	AVSS	1844.08	-1750.84
46	OSC2	1945.46	-1750.84
47	AVSS	2046.84	-1750.84
48	AVSS	2148.22	-1750.84
49	AVSS	2249.6	-1750.84
50	AVSS	2350.98	-1750.84
51	DUMMY	2569.65	-1867.39
52	DUMMY	2730.6	-1867.39

Pin	Name	x (um)	y (um)
53	DUMMY	2986.27	-1763.79
54	COM0	2986.27	-1687.2
55	COM1	2986.27	-1610.98
56	COM2	2986.27	-1534.76
57	COM3	2986.27	-1458.54
58	COM4	2986.27	-1382.32
59	COM5	2986.27	-1306.1
60	COM6	2986.27	-1229.88
61	COM7	2986.27	-1153.66
62	COM8	2986.27	-1077.44
63	COM9	2986.27	-1001.22
64	COM10	2986.27	-925
65	COM11	2986.27	-848.78
66	COM12	2986.27	-772.56
67	COM13	2986.27	-696.34
68	COM14	2986.27	-620.12
69	COM15	2986.27	-543.9
70	COM16	2986.27	-467.68
71	COM17	2986.27	-391.46
72	COM18	2986.27	-315.24
73	COM19	2986.27	-239.02
74	COM20	2986.27	-162.8
75	COM21	2986.27	-86.58
76	COM22	2986.27	-10.36
77	COM23	2986.27	65.86
78	COM24	2986.27	142.08
79	COM25	2986.27	218.3
80	COM26	2986.27	294.52
81	COM27	2986.27	370.74
82	COM28	2986.27	446.96
83	COM29	2986.27	523.18
84	COM30	2986.27	599.4
85	COM31	2986.27	675.62
86	SEG0	2986.27	769.6
87	SEG1	2986.27	845.82
88	SEG2	2986.27	922.04
89	SEG3	2986.27	998.26
90	SEG4	2986.27	1074.48
91	SEG5	2986.27	1150.7
92	DUMMY	3098.75	1275.02
93	DUMMY	3098.75	1351.24
94	DUMMY	3098.75	1470.75

Pin	Name	x (um)	y (um)
95	DUMMY	2943.72	1715.32
96	SEG6	2857.51	1715.32
97	SEG7	2781.29	1715.32
98	SEG8	2705.07	1715.32
99	SEG9	2628.85	1715.32
100	SEG10	2552.63	1715.32
101	SEG11	2476.41	1715.32
102	SEG12	2400.19	1715.32
103	SEG13	2323.97	1715.32
104	SEG14	2247.75	1715.32
105	SEG15	2171.53	1715.32
106	SEG16	2095.31	1715.32
107	SEG17	2019.09	1715.32
108	SEG18	1942.87	1715.32
109	SEG19	1866.65	1715.32
110	SEG20	1790.43	1715.32
111	SEG21	1714.21	1715.32
112	SEG22	1637.99	1715.32
113	SEG23	1561.77	1715.32
114	SEG24	1485.55	1715.32
115	SEG25	1409.33	1715.32
116	SEG26	1333.11	1715.32
117	SEG27	1258.37	1715.32
118	SEG28	1180.67	1715.32
119	SEG29	1104.45	1715.32
120	SEG30	1028.23	1715.32
121	SEG31	952.01	1715.32
122	SEG32	875.79	1715.32
123	SEG33	799.57	1715.32
124	SEG34	723.35	1715.32
125	SEG35	647.13	1715.32
126	SEG36	570.91	1715.32
127	SEG37	494.69	1715.32
128	SEG38	418.47	1715.32
129	SEG39	342.25	1715.32
130	SEG40	266.03	1715.32
131	SEG41	189.81	1715.32
132	SEG42	113.59	1715.32
133	SEG43	37.37	1715.32
134	SEG44	-38.85	1715.32
135	SEG45	-115.07	1715.32
136	SEG46	-191.29	1715.32
137	SEG47	-267.51	1715.32
138	SEG48	-343.73	1715.32
139	SEG49	-419.95	1715.32
140	SEG50	-496.17	1715.32
141	SEG51	-572.39	1715.32
142	SEG52	-648.61	1715.32
143	SEG53	-724.83	1715.32
144	SEG54	-801.05	1715.32
145	SEG55	-877.27	1715.32
146	SEG56	-953.49	1715.32
147	SEG57	-1029.71	1715.32
148	SEG58	-1105.93	1715.32
149	SEG59	-1182.15	1715.32
150	SEG60	-1258.37	1715.32
151	SEG61	-1334.59	1715.32
152	SEG62	-1410.81	1715.32
153	SEG63	-1487.03	1715.32
154	SEG64	-1563.25	1715.32
155	SEG65	-1639.47	1715.32
156	SEG66	-1715.69	1715.32
157	SEG67	-1791.91	1715.32
158	SEG68	-1868.13	1715.32
159	SEG69	-1944.35	1715.32
160	SEG70	-2020.57	1715.32
161	SEG71	-2096.79	1715.32
162	SEG72	-2173.01	1715.32
163	SEG73	-2249.23	1715.32
164	SEG74	-2325.45	1715.32
165	SEG75	-2401.67	1715.32
166	SEG76	-2477.89	1715.32
167	SEG77	-2554.11	1715.32
168	SEG78	-2630.33	1715.32
169	SEG79	-2706.55	1715.32
170	SEG80	-2782.77	1715.32
171	SEG81	-2858.99	1715.32
172	DUMMY	-2943.72	1715.32

Pin	Name	x (um)	y (um)
173	DUMMY	-3098.75	1470.75
174	DUMMY	-3098.75	1351.24
175	DUMMY	-3098.75	1275.02
176	SEG82	-2986.27	1150.7
177	SEG83	-2986.27	1074.48
178	SEG84	-2986.27	998.26
179	SEG85	-2986.27	922.04
180	SEG86	-2986.27	845.82
181	SEG87	-2986.27	769.6
182	SEG88	-2986.27	693.38
183	SEG89	-2986.27	617.16
184	SEG90	-2986.27	540.94
185	SEG91	-2986.27	464.72
186	SEG92	-2986.27	388.5
187	SEG93	-2986.27	312.28
188	SEG94	-2986.27	236.06
189	SEG95	-2986.27	159.84
190	SEG96	-2986.27	83.62
191	SEG97	-2986.27	7.4
192	SEG98	-2986.27	-68.82
193	SEG99	-2986.27	-145.04
194	SEG100	-2986.27	-221.26
195	SEG101	-2986.27	-297.48
196	SEG102	-2986.27	-373.7
197	SEG103	-2986.27	-449.92
198	SEG104	-2986.27	-526.14
199	SEG105	-2986.27	-602.36
200	SEG106	-2986.27	-678.58
201	SEG107	-2986.27	-754.8
202	SEG108	-2986.27	-831.02
203	SEG109	-2986.27	-907.24
204	SEG110	-2986.27	-983.46
205	SEG111	-2986.27	-1059.68
206	SEG112	-2986.27	-1135.9
207	SEG113	-2986.27	-1212.12
208	SEG114	-2986.27	-1288.34
209	SEG115	-2986.27	-1364.56
210	SEG116	-2986.27	-1440.78
211	SEG117	-2986.27	-1517
212	SEG118	-2986.27	-1593.22
213	SEG119	-2986.27	-1669.44
214	DUMMY	-2986.27	-1746.03

Bump Size : 75um x 75 um for 1 - 52
49um x 107um for 95 - 172
107 um x 49 um for 54 - 94, 173 - 214
Die Size : 260 x 164 mil (6604.13 x 4165.60 um)

MC141800A

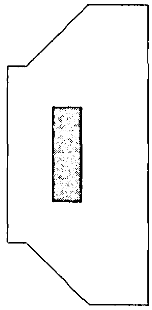
Product Preview

LCD Segment / Common Driver

CMOS

MC141800A is a CMOS LCD Driver which consists of 193 high voltage LCD driving signals to drive 128 Segment and 65 Common display. It has 6800-series parallel, IIC serial interface and Serial Peripheral interface (SPI) capability for operating with general MCU. Besides the general LCD driver features, it has on chip LCD Smart Bias Divider circuit such that minimize external component required in applications.

MC141800AT : TAB (Tape Automated Bonding)
MCC141800AZ : Gold Bump Die



MC141800AT
TAB

MCC141800AZ
Gold bump die

ORDERING INFORMATION

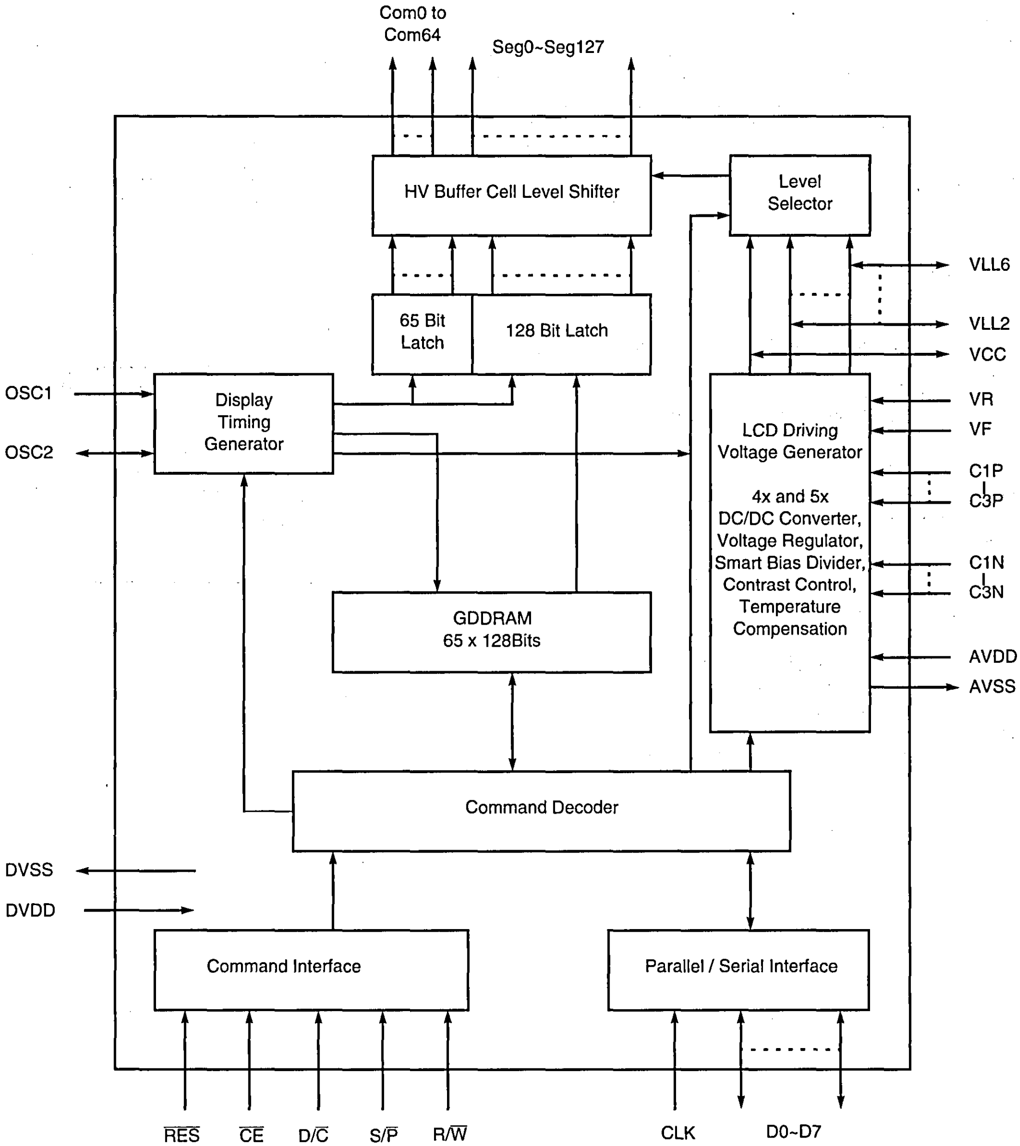
MC141800AT	70 mm TAB
MCC141800AZ	Gold BumpDie

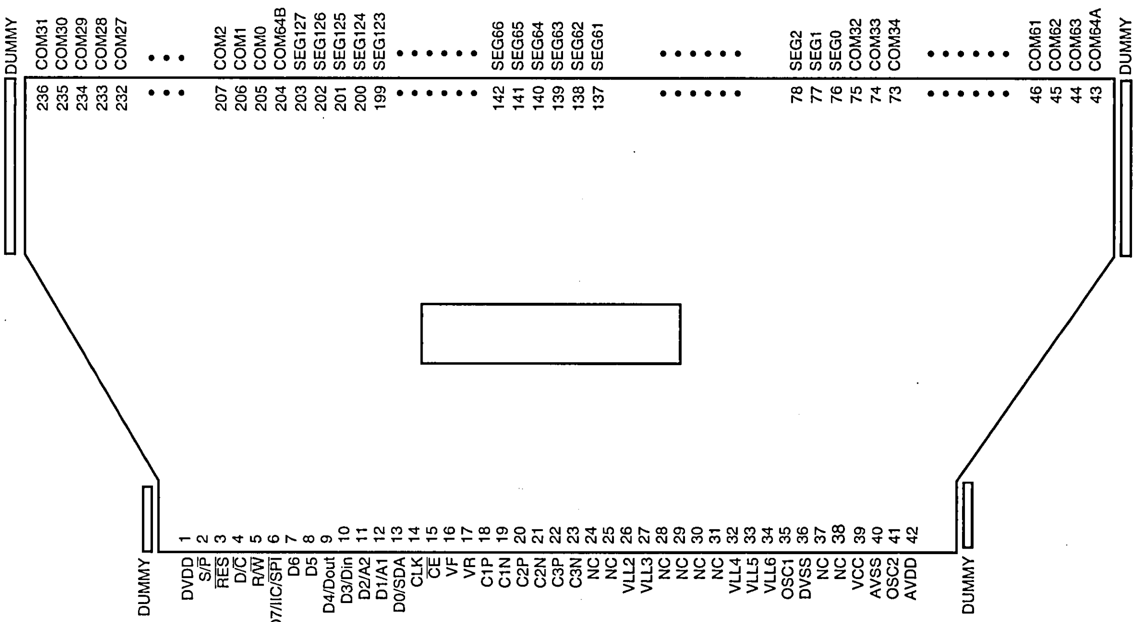
- Single Supply Operation, 2.4 V - 3.5 V
- Maximum 16.5V LCD Driving Output Voltage
- Low Current Stand-by Mode (<1uA)
- On Chip Internal DC/DC Converter / External Power Supply
- Smart Bias Divider
- 4X / 5X DC-DC Converter
- 8 bit 6800-series Parallel Interface, 1MHz IIC Serial Interface and Serial Peripheral Interface (SPI)
- On chip Oscillator
- Graphic Mode Operation
- On Chip 128 x 65 Display Data RAM
- Master Clear RAM
- Low Power Smart Icon Mode (128 icons, <25uA)
- Display Masks for Implementation of Blinking Effect
- 1 to 65 Selectable Multiplex Ratio
- 1:7 / 1:9 Bias Ratio
- Re-mapping of Row and Column Drivers
- 16 level Internal Contrast Control
- External Contrast Control
- Built-in Temperature Compensation Circuit
- Selectable Display Waveform : Type B or Type C Waveform
- 2V Icon Mode Display On

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

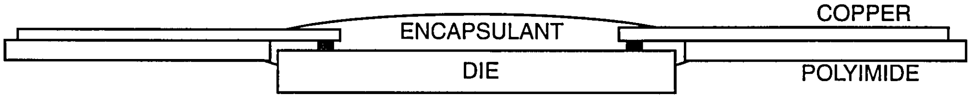
REV 0
2/97

Block Diagram



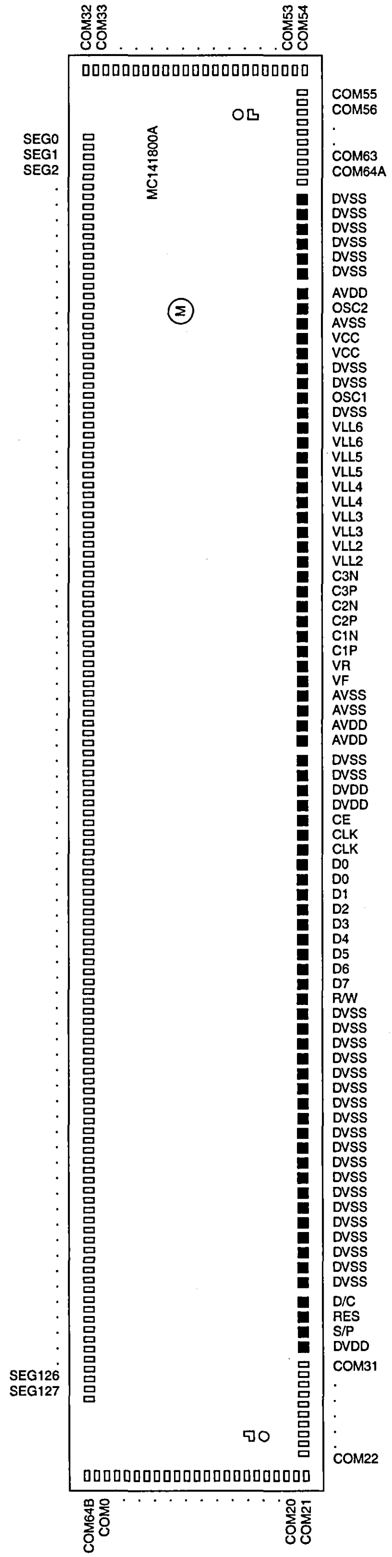


MC141800AT PIN ASSIGNMENT
(COPPER VIEW)



Normal Design TAB

Die Pad Layout for MC141800A



Gold Bump Size :

■ Input Pad, 65 x 65 (um)

▯ Output Pad, 42 x 100 (um)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+16.5	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
V_{SS} = AV_{SS} = DV_{SS} (DV_{SS} = V_{SS} of Digital circuit, AV_{SS} = V_{SS} of Analogue Circuit)
V_{DD} = AV_{DD} = DV_{DD} (DV_{DD} = V_{DD} of Digital circuit, AV_{DD} = V_{DD} of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DV_{DD} AV_{DD}	Logic Circuit Supply Voltage Range Voltage Generator Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	2.4 2.4	3.0 -	3.5 3.5	V V
I_{AC}	Access Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal DC/DC Converter On, 5X DC/DC Converter Enabled, R/$\overline{W}$ accessing, T_{cyc}=1MHz, Osc. Freq.=50KHz, Display On.	-	500	TBD	μA
I_{DP}	Display Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal DC/DC Converter On, 5X Converter Enabled, R/W Halt, Osc. Freq.=50KHz, Display On.	-	300	TBD	μA
I_{SB}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Display off, Oscillator Disabled, R/$\overline{W}$ halt.	-	TBD	1	μA
I_{ICON}	Icon Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal Oscillator, Oscillator Enabled, Display On, Icon On, R/$\overline{W}$ halt, Freq.=50KHz.	-	TBD	25	μA
V_{CC}	LCD Driving Internal DC/DC Converter Output (V_{CC} Pin)	Display On, DC/DC Converter Enabled, Osc. Freq.= 50KHz, Internal Regulator Enabled, Divider Enabled.	7	15	16.5	V
V_{LCD}	LCD Driving Voltage Input (V_{CC} Pin)	Internal DC/DC Converter Disabled.	7	15	16.5	V
V_{ICON}	Low Power Icon mode Voltage		-	2	-	V
V_{OH1}	Output High Voltage (D0-D7, OSC2)	I_{out}=100μA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (D0-D7, OSC2)	I_{out}=100μA	0	-	0.1*V_{DD}	V
V_{R1}	LCD Driving Voltage Source (V_R Pin)	Internal Regulator Enabled (V_R voltage depends on Int/Ext Contrast Control)	0	-	V_{CC}-0.5	V
V_{R2}	LCD Driving Voltage Source (V_R Pin)	Internal Regulator Disable.	-	Floating	-	V

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.4 to 3.5V, T_A=25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Input high voltage (RES, OSC2, CLK, CE, D0-D7,R/W, D/C, S/P, OSC1)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage (RES, OSC2, CLK, CE, D0-D7, R/W, D/C, S/P, OSC1)		0	-	0.2*V_{DD}	V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Output (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	Smart Bias Divider Enabled, 1:9 bias ratio	- - - - -	V_R 8/9*V_R 7/9*V_R 2/9*V_R 1/9*V_R	- - - - -	V V V V V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Output (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	Smart Bias Divider Enabled, 1:7 bias ratio	- - - - -	V_R 6/7*V_R 5/7*V_R 2/7*V_R 1/7*V_R	- - - - -	V V V V V
V_{LL6} V_{LL5} V_{LL4} V_{LL3} V_{LL2}	LCD Display Voltage Input (V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)	External Voltage Generator, Smart Bias Divider Disable	7 0 0 0 0	- - - - -	V_{CC} V_{LL6} V_{LL5} V_{LL4} V_{LL3}	V V V V V
I_{OH}	Output High Current Source (D0-D7, OSC2)	V_{out}=V_{DD}-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (D0-D7, OSC2)	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source (D0-D7, OSC2)		-1	-	1	µA
I_{IL}/I_{IH}	Input Current (RES, OSC2, CLK, D0-D7, R/W, D/C , S/P, OSC1)		-1	-	1	µA
C_{IN}	Input Capacitance (OSC1, OSC2, all logic pins)		-	5	7.5	pF
V_{CN}	Internal Contrast Control (V_R Output Voltage)	Internal Regulator Enabled, Internal Contrast control Enabled. (16 Voltage Levels Controlled by Software. Each level is typically 1.5% of the Internal Regulator Output Voltage.)	-	± 12	-	%
	Temperature Coefficient Compensation					
PTC0	Flat Temperature Coefficient	(TC1=0, TC2=0, Internal Regulator Disabled.)	-	0.0	-	%
PTC1	Temperature Coefficient 1*	(TC1=0, TC2=1, Internal Regulator Enabled.)	-	-0.18	-	%
PTC2	Temperature Coefficient 2*	(TC1=1, TC2=0, Internal Regulator Enabled.)	-	-0.22	-	%
PTC3	Temperature Coefficient 3*	(TC1=1, TC2=1, Internal Regulator Enabled.)	-	-0.35	-	%

* The formula for the temperature coefficient is:

$$TC(\%) = \frac{\text{VR at 50°C - VR at 0°C}}{\text{50°C - 0°C}} \times \frac{1}{\text{VR at 25°C}} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, Voltage referenced to V_{SS}, AV_{DD}=DV_{DD}=3V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display timing generator	60Hz Frame Frequency Either External Clock Input or Internal Oscillator Enabled	45	60	55	KHz
F_{FRM}	Frame Frequency	Graphic Display Mode, Normal Frequency Mode, 65 - 49 MUX	-	$\frac{F_{OSC}}{15 * MUX}$	-	Hz
		Graphic Display Mode, Half Frequency Mode, 65 - 49 MUX	-	$\frac{F_{OSC}}{30 * MUX}$	-	Hz
		Graphic Display Mode, Normal Frequency Mode, 48 - 33 MUX	-	$\frac{F_{OSC}}{23 * MUX}$	-	Hz
		Graphic Display Mode, Half Frequency Mode, 48 - 33 MUX	-	$\frac{F_{OSC}}{46 * MUX}$	-	Hz
		Graphic Display Mode, Normal Frequency Mode, 32 - 2 MUX	-	$\frac{F_{OSC}}{30 * MUX}$	-	Hz
		Graphic Display Mode, Half Frequency Mode, 32 -2 MUX	-	$\frac{F_{OSC}}{60 * MUX}$	-	Hz
		6-Phase Low Power Icon Mode, Normal Frequency Mode	-	$\frac{F_{OSC}}{960}$	-	Hz
		6-Phase Low Power Icon Mode, Half Frequency Mode	-	$\frac{F_{OSC}}{1920}$	-	Hz
		4-Phase Low Power Icon Mode, Normal Frequency Mode	-	$\frac{F_{OSC}}{1024}$	-	Hz
		4-Phase Low Power Icon Mode, Half Frequency Mode	-	$\frac{F_{OSC}}{2048}$	-	Hz
OSC	Internal Oscillation Frequency with different value of feedback resistor	Internal Oscillator Enabled, V_{DD} within operation range	See Figure 1 for the relationship			

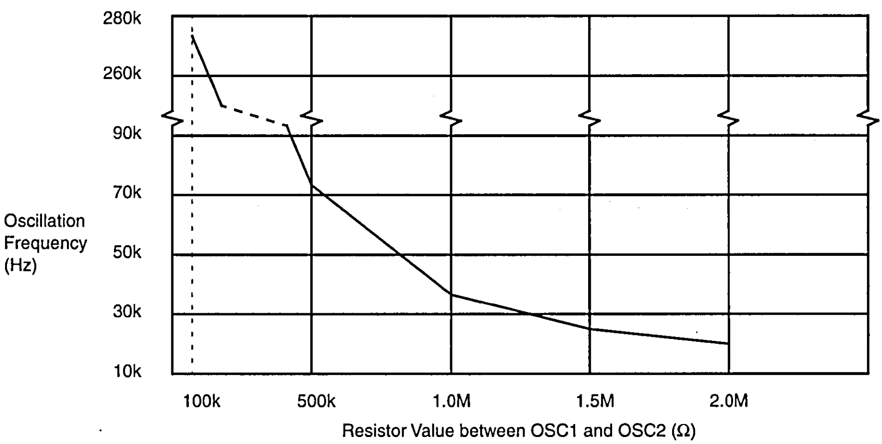


Figure 1. Internal Oscillator Frequency Relationship with External Resistor Value

TABLE 3. Parallel Timing Characteristics (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	1000	-	-	ns
t_{AS}	Address Setup Time	90	-	-	ns
t_{AH}	Address Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	210	-	-	ns
t_{DHW}	Write Data Hold Time	75	-	-	ns
t_{DSR}	Read Data Setup Time	250	-	-	ns
t_{DHR}	Read Data Hold Time	75	-	-	ns
t_{ACC}	Access Time	-	-	250	ns
PW_{EL}	Enable Low Pulse Width	390	-	-	ns
PW_{EH}	Enable High Pulse Width	390	-	-	ns
t_R	Rise Time	-	-	45	ns
t_F	Fall Time	-	-	45	ns

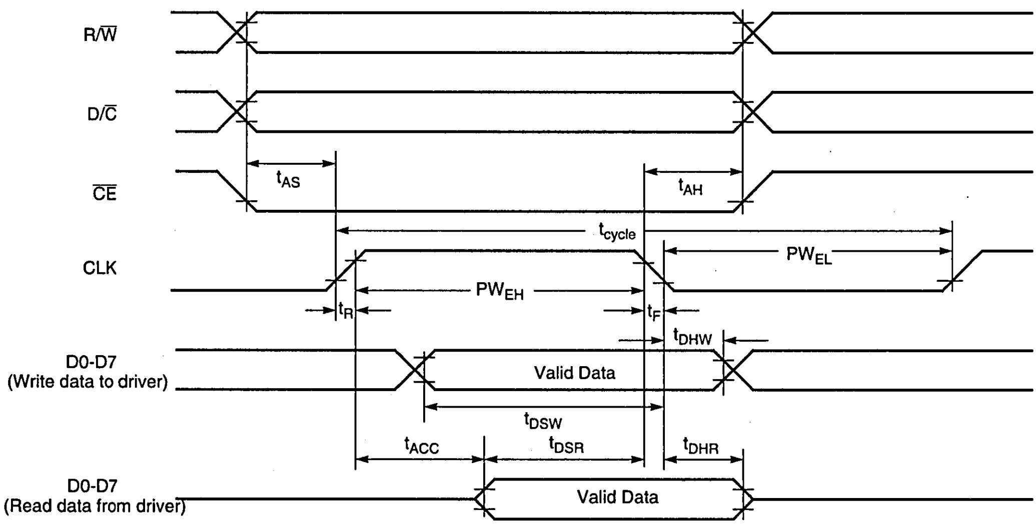


Figure 2. Parallel 6800-series Interface Timing Characteristics

TABLE 4. IIC Serial Timing Characteristics (T_A=-30 to 85˚C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	100kHz			400kHz			1MHz			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{cycle}	Clock Cycle Time	10	-	-	2.5	-	-	1	-	-	µs
t_{HSTART}	Start condition Hold Time	4.0	-	-	0.6	-	-	0.3	-	-	µs
t_{HD}	Data Hold Time	500	-	-	300	-	-	150	-	-	ns
t_{SD}	Data Setup Time	250	-	-	100	-	-	50	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	4.7	-	-	0.6	-	-	0.3	-	-	µs
t_{SSTOP}	Stop condition Setup Time	4.0	-	-	0.6	-	-	0.3	-	-	µs
t_R	Rise Time for data and clock pin	-	-	1000	-	-	300	-	-	150	ns
t_F	Fall Time for data and clock pin	-	-	300	-	-	300	-	-	150	ns
t_{IDLE}	Idle Time before a new transmission can start	4.7	-	-	1.3	-	-	0.6	-	-	µs

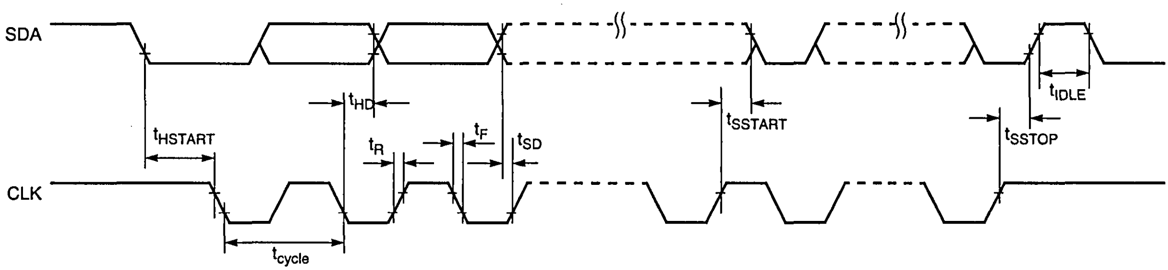


Figure 3. IIC Serial Interface Timing Characteristics

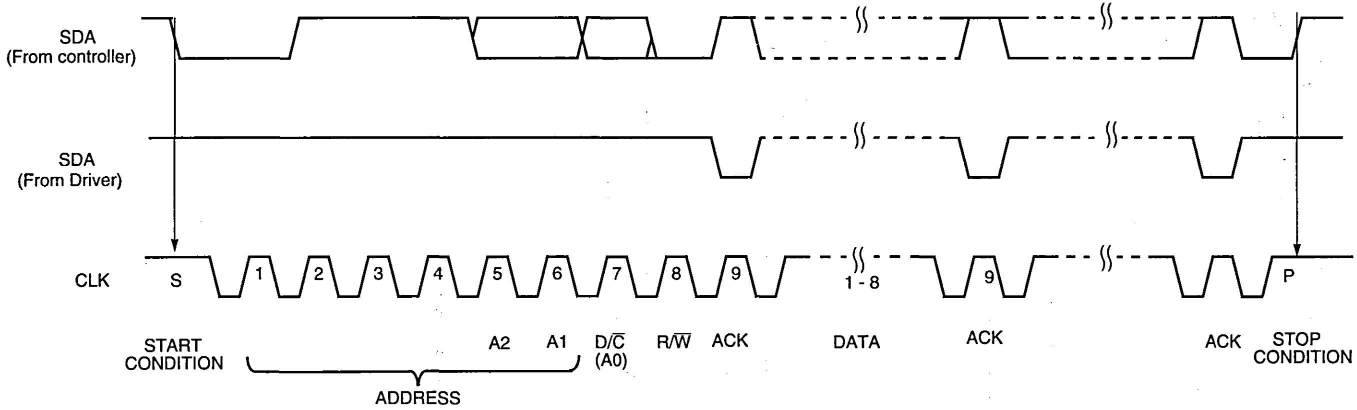


Figure 4. IIC Serial Interface Input Protocol (Write Data to Driver)

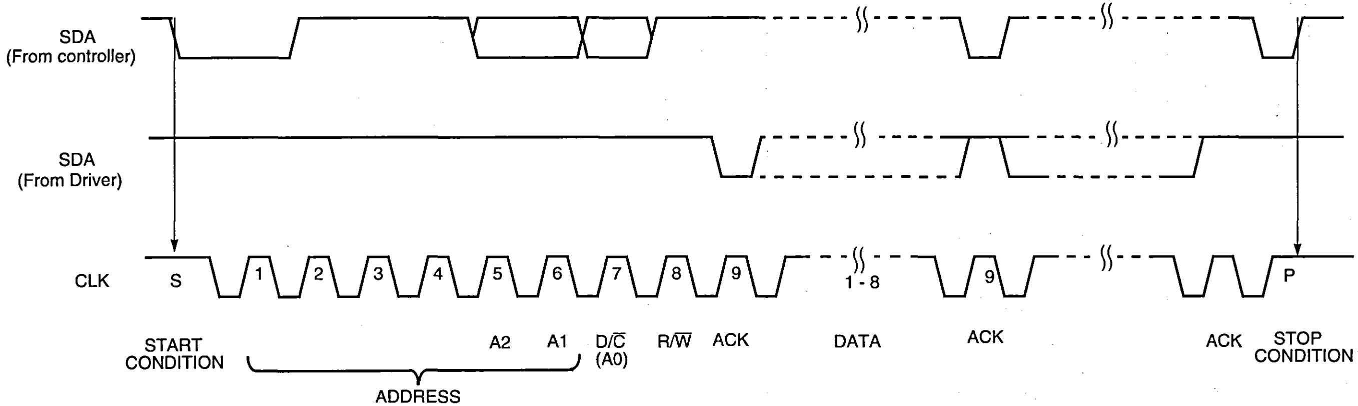


Figure 5. IIC Serial Interface Output Protocol (Read Data from Driver)

TABLE 5. SPI Timing Characteristics (T_A=-30 to 85°C, DV_{DD}=2.4 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	1000	-	-	ns
t_{LEAD}	Enable Lead Time	500	-	-	ns
t_{LAG}	Enable Lag Time	500	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{DVR}	Read Data Valid Time	-	-	240	ns
t_{DHR}	Read Data Hold Time	10	-	-	ns
t_{ACC}	Access Time	-	-	120	ns
t_{DIS}	Disable Time	-	-	240	ns
t_{CLKL}	Clock Low Time	380	-	-	ns
t_{CLKH}	Clock High Time	380	-	-	ns
t_R	Rise Time	-	-	100	ns
t_F	Fall Time	-	-	100	ns

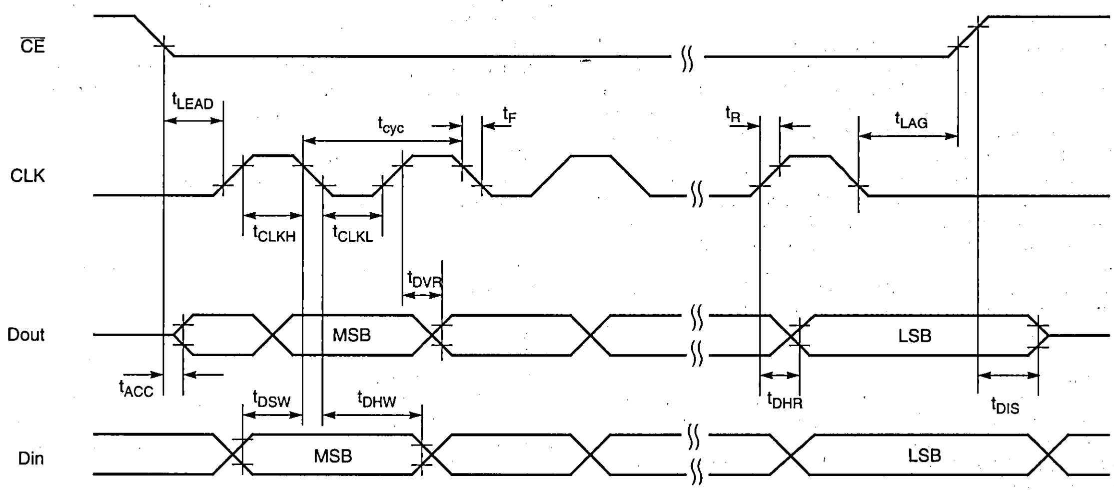


Figure 6. SPI Timing Characteristics

PIN DESCRIPTIONS

S/$\overline{P}$ (Serial / Parallel Interface)

This pin is an input pin. The pin is sampled out when reset to determine what type of interface is desired. The S/$\overline{P}$ pin input HIGH for serial interface while input LOW for parallel interface.

D/$\overline{C}$ (Data / Command)

If parallel interface is selected, this input pin acknowledges the LCD driver the input at D0-D7 is data or command. Input High for data while input Low for command. If serial interface is selected, float this pin.

CLK (Input Clock)

This pin is normal Low clock input. If parallel interface is selected, data on D0-D7 are latched at the falling edge of CLK. If IIC serial interface is selected, data on SDA is latched at the falling edge of CLK. If SPI is selected, data on Din and Dout are latched at the falling edge of CLK.

$\overline{RES}$ (Reset)

A Low input pulse to this pin resets the internal status of the driver (same as power on reset). The minimum pulse width is 10 µs.

$\overline{CE}$ (Chip Enable)

If parallel interface is selected, this input pin is used for chip enable. If IIC serial interface is selected, leave this pin float and it will be internally tied to VDD.

D0 - D7 (Data)

This bi-directional bus is used for data / command transferring. If parallel interface is selected, D0 - D7 are connected directly to MCU for data transfer. When serial interface is selected, D7 (IIC/$\overline{SPI}$) is an input pin to determine which type of serial interface is desired. The IIC/$\overline{SPI}$ pin HIGH indicates IIC interface is used. The IIC/$\overline{SPI}$ pin LOW indicates SPI is used.

When IIC serial interface is selected, D0 (SDA) is connected directly to MCU for data transfer, D1 (A1) and D2 (A2) are used to define the 2 bit programmable address. The address of this device is 0111xyab where x, y, a, b represent A2, A1, D/$\overline{C}$ and R/$\overline{W}$ respectively.

When SPI is selected, D3 (Din) is used to write data / command from MCU to driver and D4 (Dout) is used to read data / command to MCU from driver.

R/$\overline{W}$ (Read / Write)

If parallel interface is selected, this is an input pin. To read the display data RAM or the internal status (Busy / Idle), pull this pin High. The R/$\overline{W}$ input Low indicates a write operation to the display data RAM or to the internal setup registers. If serial interface is selected, let this pin float.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value should be connected between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)

For internal oscillator mode, this is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

VLL6 - VLL2

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit if internal divider is enable.

C1N and C1P, C2N and C2P, C3N and C3P

If Internal DC/DC Converter is enabled, a 0.1 µF capacitor is required to connect these three pair of pins.

V_R and V_F

This is a feedback path for the gain control (external contrast control) of VLL1 to VLL6. For adjusting the LCD driving voltage, it requires a feedback resistor placed between V_R and V_F, a gain control resistor placed between V_F and AVSS, a 10 µF capacitor placed between V_R and AVSS. (Refer to the Application Circuit)

COM0-COM63, COM64A and COM64B (Row Drivers)

These pins provide the row driving signal to LCD panel. Output is 0V during display off. COM64A and COM64B are icon lines with same signal output so as to provide the flexability to have the icon line on top or bottom of panel, or both top and bottom of the panel. COM64A/B also serves as the common driving signal in the icon mode.

COM64A/B is special design icon line (128 icons). There are some special commands to program it separately (e.g. Set Icon Mask, Smart Icon Mode, Low Power Icon Mode)

SEG0-SEG127 (Column Drivers)

These 128 pins provide LCD column driving signal to LCD panel. They output 0V during display off.

AVDD and AVSS

AVDD is the positive supply to the LCD bias Internal DC/DC Converter. AVSS is ground.

VCC

For using the Internal DC/DC Converter, a 0.1 µF capacitor from this pin to AVSS is required. It can also be an external bias input pin if Internal DC/DC Converter is not used. Power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other component.

DVDD and DVSS

Power is supplied to the digital control circuit of the driver using these two pins. DVDD is power and DVSS is ground.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ high, data is written to Graphic Display Data RAM (GDDRAM). D/$\overline{C}$ low indicates that the input at D0-D7 is interpreted as a Command.

Reset is of same function as Power ON Reset (POR). Once $\overline{RES}$ received the reset pulse, all internal circuitry will back to its initial status. Refer to Command Description section for more information.

MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D0-D7), R/$\overline{W}$, D/$\overline{C}$, $\overline{CE}$ and the CLK. The R/$\overline{W}$ input High indicates a read operation from the Graphic Display Data RAM (GDDRAM). R/$\overline{W}$ input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The CLK input serves as data latch signal (clock). Refer to AC operation conditions and characteristics section for Parallel Interface Timing Description.

MPU Serial IIC Interface

The IIC interface consists of two communication bus : data pin SDA and clock pin CLK. The CLK input serves as data latch signal (clock). Before communication begins, a start condition must be setup on the bus by the controller. To establish a start condition, the controller must pull the data pin low while the clock pin is high.

After the start condition has been established for t_{HSTART}, an eight-bit address should be sent. The six most significant bits of the address (0111xy) are used to uniquely define devices on the bus, the 7th bit is used as a data / command control: if it is 0, then the signal on SDA is interpreted as a command; if it is 1, then data SDA is written to GDDRAM. The least significant bit is a data direction read / write control; if it is 0, then the controller writes data / command to the driver; if it is 1, then the controller reads data / command from LCD driver.

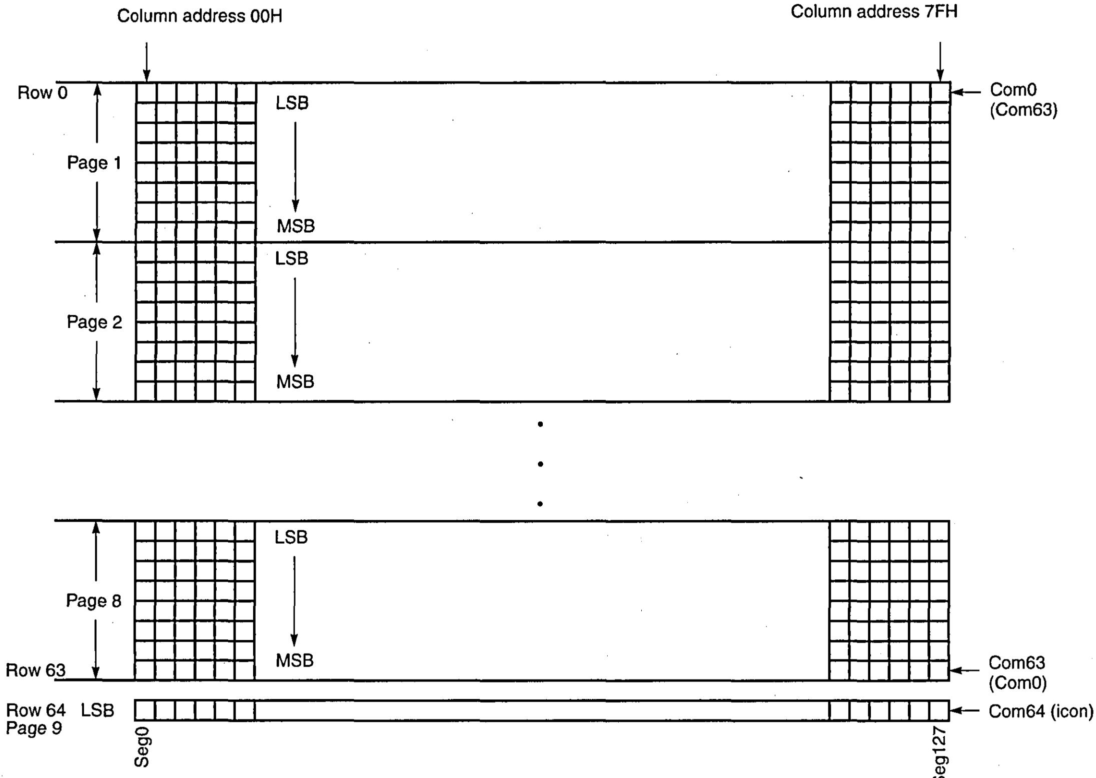
Data is transferred with the most significant bit first. Each byte has to be followed by an acknowledge bit. The transmitter releases the SDA high during the acknowledge clock pulse. The receiver has to pull down the SDA during the acknowledge clock pulse.

To end communication, a stop condition should be set up on the bus. A low to high transition of data pin while the clock pin is high defines a stop condition. However, if a master still wishes to communicate on the bus, another start condition and address can be generated without a stop condition. Refer to AC operation conditions and characteristics section for IIC Serial Interface Timing Description.

MPU Serial Peripheral Interface

The SPI consists of 4 communication bus : data input pin Din, data output pin Dout, clock pin CLK and chip enable pin $\overline{CE}$. The CLK input serves as data latch signal (clock).

Data is transferred serially with most significant bit first, least significant bit last. During the communication, the controller must input Low $\overline{CE}$ before data transactions and must stay low for the rest of the transaction. By default, the LCD driver will receive command from MCU. If messages on the data pin are data rather than command, MCU should send Data Direction command ($0100100X_0$) to control the data direction and then one more command to define the number of data bytes will be read / write. After these two continuous commands are send, the following messages will be data rather than command. For read operation ($X_0 = 1$), MCU reads a group of data from LCD driver through Dout pin. For write opearion ($X_0 = 0$), MCU writes a group of data to the LCD driver through Din pin. Refer to AC operation conditions and characteristics section for Serial Peripheral Interface Timing Description.



Note : The configuration in parentheses represent the remapping of Rows and Columns in 65 MUX mode

Figure 7. Graphic Display Data RAM (GDDRAM) Address Map

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (128x65 = 8320 bits). Figure 7 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 8). The oscillator frequency can be selected in the range of 15kHz to 250kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

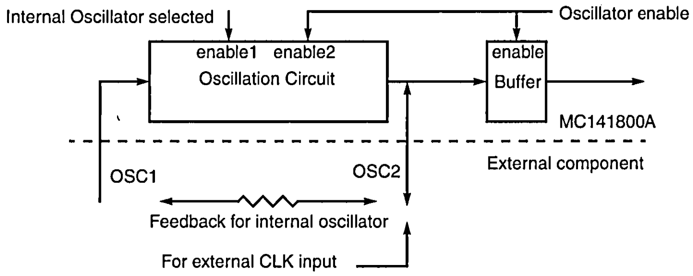


Figure 8. Oscillator Circuitry

LCD Driving Voltage Generator and Internal Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. 4X and 5X DC-DC Converter
   To generate the Vcc voltage. 4X DC-DC converter is used for LCD panel which needs lower driving voltage for less power consumption. 5X DC-DC converter is used for LCD panel which needs higher driving voltage.
2. Internal Regulator
   Feedback gain control for initial LCD voltage. it can also be used with external contrast control.
3. Smart Bias Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the Internal Regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.
   All blocks can be individually turned off if external voltage generator is employed
5. Bias Ratio Selection circuitry
   Software control of 1/7 and 1/9 bias ratio to match the characteristic of LCD panel.
6. Self adjust temperature compensation circuitry
   Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.

65 Bit Latch / 128 Bit Latch

A register carries the display signal information. First 65 bits are Common driving signals and other 128 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

LCD Panel Driving Waveform

The following is an example of how the Common and Segment drivers may be connected to a LCD panel. The waveforms shown in Figure 9a, 9b and 9c illustrate the desired multiplex scheme.

In order to reduce the crosstalk effect, invert the polarities of the pixel-driving waveforms every 2 or 4 or 8 or 65 lines according to the selected waveforms. In the power-up state, the default waveform will be type "B".

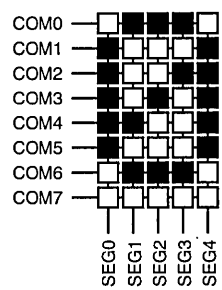


Figure 9a. LCD Display Example "0"

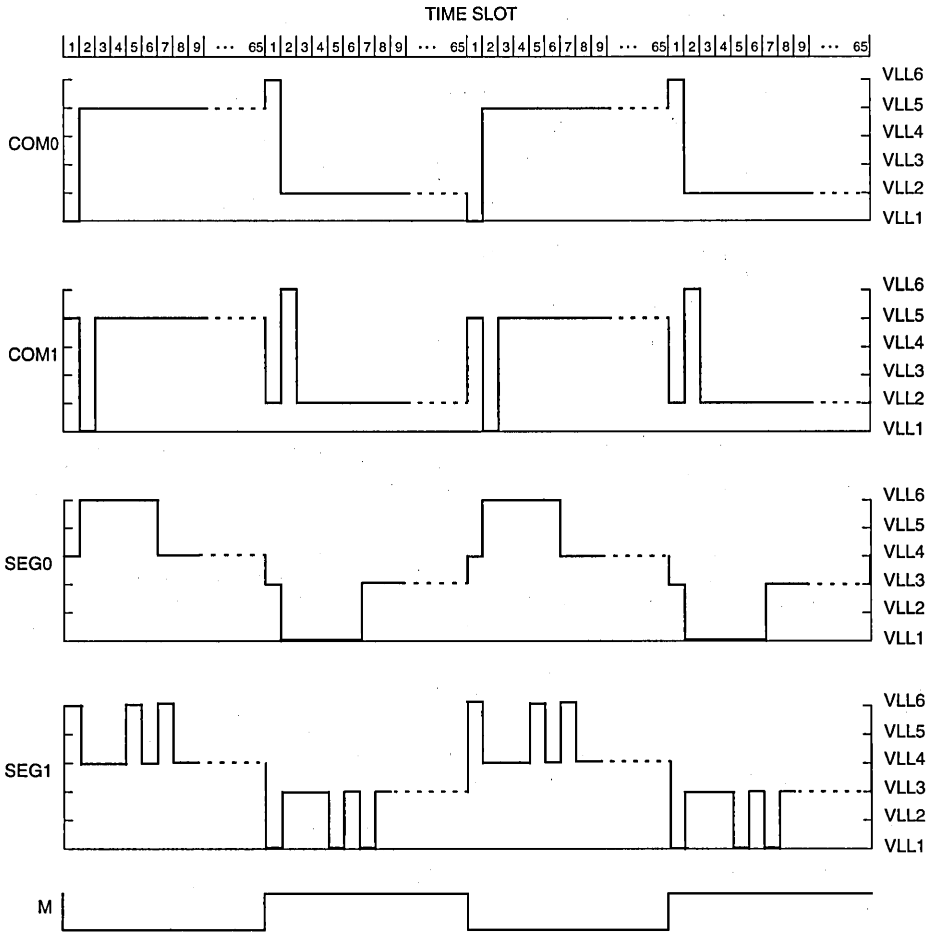


Figure 9b. LCD Driving Signal from MC141800A (Waveform B)

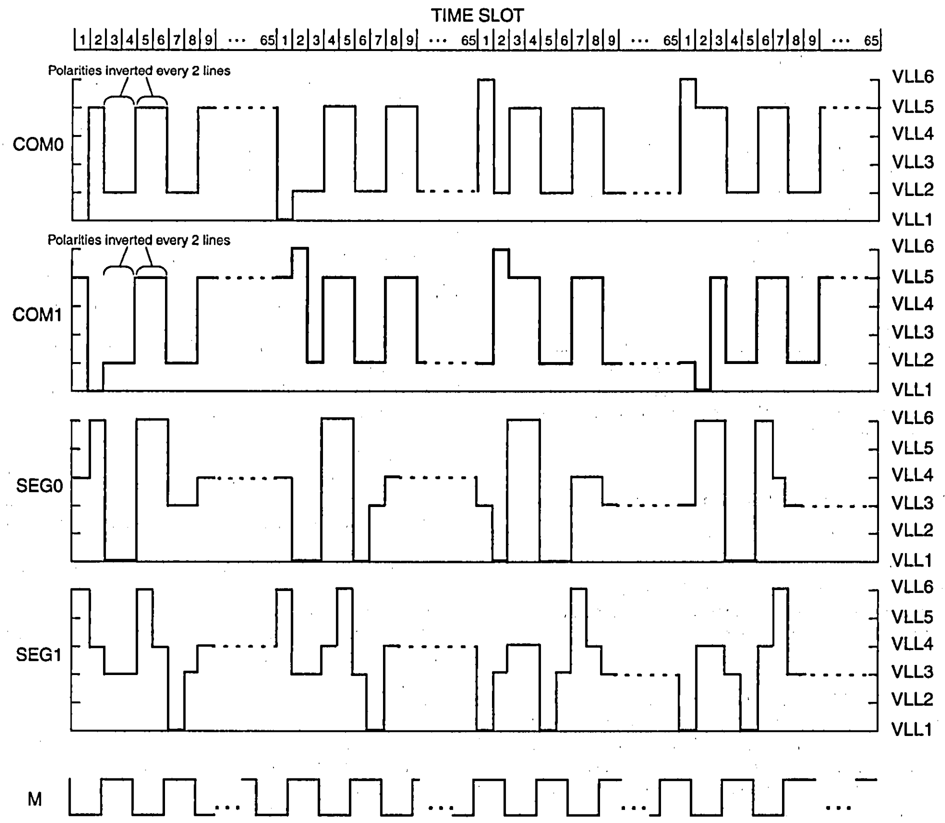


Figure 9c. LCD Driving Signal from MC141800A (Waveform C with polarity inversion every 2 lines)

Command Description

Set Display On / Off (Display Mode / Stand-by Mode)

The Display On command turns the LCD Common and Segment outputs on. This command starts the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : "Oscillator On" command should be sent before "Display On" is selected)

The Display Off command turn the display off and the states of the LCD driver are as follow during display off :

1. All the Common and Segment outputs are fixed at V_{LL1} (V_{SS}).
2. The bias Internal DC/DC Converter is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The Oscillator is not affected by this command.

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-7FH (128 columns). The column address will be increased automatically after a read or write operation. Refer to "Address Increment Table" and command "Set GDDRAM Page Address" for further information.

Set GDDRAM Page Address

This command positions the row address to 1 of 9 possible positions in GDDRAM. Refer to figure 7.

Master Clear GDDRAM

This command is to clear the content of the Display Data RAM to zero. Issue this command followed by a dummy write command. The RAM for icon line will not be affected by this command.

Master Clear Icon

This command is a MASTER clear of the Icon Data RAM. After setting the page pointer to icon page (page 9), the internal icon RAM data will be set to Zero after the command is issued. Before using this command, set the page address to page 9 by the command "Set GDDRAM Page Address". A dummy write data is also needed after the "Master Clear Icon" command to make the clear icon action effective.

Set Page Mask (Display Mask)

The following command will be written to the Page Mask Register. Page Mask is an 8-bit register. Each bit represents one of the 8 pages : page mask bit 0 represents Page 1, page mask bit 1 represents Page 2,...etc.

Page Mask

When the Page Mask is enabled, the display of those pages, with page mask bit set, will be cleared. Meanwhile, the data in the display RAM is retained.

Icon Mask

When the Icon Mask is enabled, the display of the icons will be cleared. Meanwhile, the data in the icon display RAM is retained.

Set Display Mode

This command switch the driver to full display mode or icon display mode. In low power icon mode, only icons (driven by COM64) are displayed. Display on row 0 to row 63 will be disabled. The DC-DC converter and the Internal Regulator are off. All VCC, VLLs pins do not have external bias voltage supply in the low power icon mode. In normal display mode, COM0 to COM64 will be turned on.

Set Display Frequency

In half display frequency mode, the display frame frequency will be halved. Also, the operation frequency of analog circuitries will be halved for power saving purpose.

Save / Restore Column Address

Save Column Address command saves a copy of the Column Address of GDDRAM. Restore Column Address command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Set Column Mapping

This instruction selects the mapping of Display Data RAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 127 of GDDRAM mapped to Seg0-Seg127 respectively;
2. Column 0 - Column 127 of GDDRAM mapped to Seg127-Seg0 respectively.

COM64 will not be affected by this command. Detail information please refer to section "Display Output Description".

Set Row Mapping

This instruction selects the mapping of Display Data RAM to Common Drivers for mechanical flexibility. There are 2 selected mappings:

1. Row 0 - Row x of GDDRAM to Common 0 - Common x respectively;
2. Row 0 - Row x of GDDRAM to Common x - Common 0 respectively.

(x+2 is the multiplex ratio)

COM64 will not be affected by this command. See section "Display Output Description" for related information.

Set MUX Ratio

This command is to select any a ratio from 2 to 65. Row 64 (icon line) is not affected by this command and it would be turned on for normal display. This command contain two commands bytes, the first byte inform the driver that the second byte will be the no. of mux ratio.

e.g. second byte = 0H to turn on Row 0 and 64 (2 MUX)
second byte = 63H to turn on Row 0 to 64 (65 MUX)

The unused common pins output non-scanning signals.

Set Bias Ratio

This command sets the 1/7 bias or 1/9 bias for the divider output. The selection should match the characteristic of LCD Panel.

Set Oscillator Disable / Enable

This command is used to either turn on / off Oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command "Set Display On/Off". See command "Ext/Int Oscillator" for more information.

Set Internal / External Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Set Internal DC/DC Converter Enable

Use this command to select the Internal DC/DC Converter to generate the V_{CC} from AV_{DD}. Disable the Internal DC/DC Converter if external Vcc is provided.

Set 4X / 5X DC/DC Converter
This command selects the usage of 4X or 5X Converter when the Internal DC/DC Converter is enabled.

Set Temperature Coefficient
A temperature gradient selector circuit controlled by two control bits TC1 and TC2. This command can select 4 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades.

Set Internal Regulator On/Off
Choose bit option 0 to disable the on chip Internal Regulator. Choose bit option 1 to enables Internal Regulator which consists of the internal contrast control circuits.

Set Smart Bias Divider On/Off
If the Smart Bias Divider is disabled, external bias can be used for V_{LL6} to V_{LL2}. If the Smart Bias Divider is enabled, the internal circuit will *generated the 1:7 or 1:9 bias driving voltage.*

End of Command
This command is used as extra write end command follows the last byte of data / command written. This command is not available if serial mode is selected.

Set Internal Contrast Control Enable
This command is used to adjust the delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level
If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels. The contrast level starts from lowest value after POR.

Set Contrast Level
This command is to select one of the 16 contrast levels when internal contrast control circuitry is in use. After power-on reset, the contrast level is lowest.

Set Smart Icon Mode
This command is to set 4-Phase or 6-Phase smart icon modes which for lower VDD or higher Von of panel. Refer to Smart Icon Mode Output Description for detail.

Set Display Waveform Type
This command will select the number of lines for the polarity inversion of the driving waveform. Four types of waveform types are available. Refer to Figure 9.

Set Data Direction
This command is used in SPI mode only. It will be two continuous commands, the first byte control the data direction and inform the LCD driver the second byte will be number of data bytes will be read / write. After these two commands sending out, the following messages will be data.

COMMAND TABLE

Bit Pattern	Command	Comment
$0000X_3X_2X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using $X_3X_2X_1X_0$ as address bits. $X_3X_2X_1X_0$=0000 : page 1 (POR) $X_3X_2X_1X_0$=0001 : page 2 $X_3X_2X_1X_0$=0010 : page 3 $X_3X_2X_1X_0$=0011 : page 4 $X_3X_2X_1X_0$=0100 : page 5 $X_3X_2X_1X_0$=0101 : page 6 $X_3X_2X_1X_0$=0110 : page 7 $X_3X_2X_1X_0$=0111 : page 8 $X_3X_2X_1X_0$=1000 : page 9
$0001X_3X_2X_1X_0$	Set Contrast Level	With $R/\overline{W}$ pin input low, set one of the 16 available values to the internal contrast register, using $X_3X_2X_1X_0$ as data bits. The contrast register is reset to 0000 during POR.
$0010000X_0$	Set 4X / 5X DC-DC Converter	X_0=0: enable 4X Converter (POR) X_0=1: enable 5X Converter
$0010001X_0$	Set Segment Mapping	X_0=0: Col0 to Seg0 (POR) X_0=1: Col0 to Seg127
$0010010X_0$	Set Common Mapping	X_0=0: Row0 to Com0 (POR) X_0=1: Row0 to Com63
$0010100X_0$	Set Display on/off	X_0=0: display off (POR) X_0=1: display on
$0010101X_0$	Set Internal DC/DC Converter On/Off	X_0=0: Internal DC/DC Converter Off (POR) X_0=1: Internal DC/DC Converter On
$0010110X_0$	Set Internal Regulator On/Off	X_0=0: Internal Regulator Off(POR) X_0=1: Internal Regulator On
$0010111X_0$	Set Smart Bias Divider On/Off	X_0=0: Smart Bias Divider Off (POR) X_0=1: Smart Bias Divider On When an external bias network is preferred, the Smart Bias Divider should be disabled.

COMMAND TABLE

Bit Pattern	Command	Comment
$0011000X_0$	Set Internal Contrast Control On/Off	X_0=0: Internal Contrast Control Off(POR) X_0=1: Internal Contrast Control On Internal contrast circuits can be disabled if external contrast circuits is preferred.
$0011001X_0$	Set Display Frequency	X_0=0 : normal display frequency (POR) X_0=1 : half display frequency
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : restore address X_0=1 : save address
00110110	Master Clear GDDRAM	Master clear GDDRAM (64 x 128 bits), row 64 (icon line) will not be cleared
00110111	Master Clear Icons	Master Clear of Icons
$0011100X_0$	Set Bias Ratio	X_0=0 : bias = 1 : 9 (POR) X_0=1 : bias = 1 : 7
$0011101X_0$	Reserved	X_0=0 : Normal Operation (POR) X_0=1 : Test Mode 1 Select (Note : Make sure to set X_0=0 during application)
00111100	End of Command	Write commnd to identify end of data frame
$0011111X_0$	Set Display Mode	X_0=0 : low power Icon display mode X_0=1 : normal display mode (POR)
01000000	Set Multiplex Ratio	next command will define no. of MUX, $00X_5X_4X_3X_2X_1X_0$ no. of mux=00111111 upon POR (65 MUX)
01000001	Set Page Mask	next command will be written to page mask register page mask register=0 upon POR
$0100010X_0$	Page Mask	X_0=0 : disable page mask (POR) X_0=1 : enable page mask
$0100011X_0$	Icon Mask	X_0=0 : disable icon mask (POR) X_0=1 : enable icon mask
$0100100X_0$	Set Data Direction (for SPI mode only)	X_0=0 : Write Data (POR) X_0=1 : Read Data next command will define the total number of data bytes will be read / write e.g. no. of data bytes = 01111111 for 128 bytes
$0100101X_0$	Reserved	X_0=0 : Select Switch Resistor as HV divider (POR) X_0=1 : Select Buffer as HV dividier
$0100110X_0$	Reserved	X_0=0 : Select 500ohm in switch resistor divider (POR) X_0=1 : Select 1kohm in switch resistor divider
01010100	Reserved	next command will define Smart Divider value, $000X_4X_3X_2X_1X_0$
$0101001X_0$	Reserved	X_0=0 : Use diode approach for temperature compensation (POR) X_0=1 : Use band gap technique for temperature compensation
$011001X_1X_0$	Set Display Waveform Type	X_1X_0=00 : Waveform Type B (POR) X_1X_0=01 : Waveform Type C with polarity inversion every 8 lines X_1X_0=10 : Waveform Type C with polarity inversion every 4 lines X_1X_0=11 : Waveform Type C with polarity inversion every 2 lines
$0110100X_0$	Set Smart Icon Mode	X_0=1 : 4-Phase Smart Icon X_0=0 : 6-Phase Smart Icon (POR)
$011011X_1X_0$	Set Temperature Coefficient	X_1X_0=: 0.00% (POR) X_1X_0=: -0.18% X_1X_0=: -0.22% X_1X_0=: -0.35%
$0111000X_0$	Increase / Decrease Contrast Level	X_0=0: Decrease by one level X_0=1: Increase by one level (Note: increment/decrement wraps round among the 16 contrast levels. Start at the lowest level when POR.

COMMAND TABLE

Bit Pattern	Command	Comment
$0111011X_0$	Reserved	X_0=0: Normal Operation (POR) X_0=1: Test Mode 2 Select (Note : Make sure to set X_0=0 during application)
$0111101X_0$	Set Internal / External Oscillator	X_0=0: Internal oscillator (POR) X_0=1: External oscillator. For internal oscillator place a resistor between OSC1 and OSC2. For external oscillator mode, feed clock input to OSC2.
$0111111X_0$	Set Oscillator On/Off	X_0=0: oscillator Off (POR) X_0=1: oscillator On. This is the master control for oscillator circuitry. This command should be issued after the "Set Internal / External Oscillator" command.
$1X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address. Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits.

Data Read / Write

To read data from the GDDRAM, input High to R/$\overline{W}$ pin and D/$\overline{C}$ pin in parallel mode or pull high at the 7th and 8th bit of the address in IIC serial mode or send Data Direction command 01001001 in SPI mode. Data is valid at the falling edge of CLK. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to R/$\overline{W}$ pin and High to D/$\overline{C}$ pin in parallel mode or pull low 7th bit and high 8th bit of the address in IIC serial mode or send Data Direction command 01001000 in SPI mode. Data is latched at the falling edge of CLK. And the GDDRAM column address pointer will be increased by one automatically. If parallel interface is selected, End of command should be followed after all data are send out.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the "Commands Required for R/$\overline{W}$ Actions on RAM" Table)

Address Increment Table (Automatic)

D/$\overline{C}$	R/$\overline{W}$	Comment	Address Increment	Remarks
0	0	Write Command	No	
0	1	Read Command	No (invalid mode)	*1
1	0	Write Data	Yes	*2
1	1	Read Data	Yes	

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.

Remarks : *1. Only data is read from RAM.
*2. If write data is issued after Command Clear RAM, Address increase is not applied.
*3. Column Address will wrap round when overflow.

Commands Required for R/W Actions on RAM

R/W Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set GDDRAM Column Address Read/Write Data End of command	$(0000X_3X_2X_1X_0)$* $(1X_6X_5X_4X_3X_2X_1X_0)$* $(X_7X_6X_5X_4X_3X_2X_1X_0)$ (00111100)
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address End of command	$(0011010X_0)$ (00111100)
Master Clear GDDRAM	Set Clear Page GDDRAM (64 x 128 bits) Dummy Write Data	(00110110) $(X_7X_6X_5X_4X_3X_2X_1X_0)$
Master Clear Icon RAM	Set GDDRAM Page Address to Page 9 Master Clear Icon RAM (128 bits, row 64) Dummy Write Data	(00001000) (00110111) $(X_7X_6X_5X_4X_3X_2X_1X_0)$

* No need to resend the command again if it is set previously.

The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed.

Display Output Description

This is an example of output pattern on the LCD panel. Figure 10b and 10c are data map of GDDRAM and the output pattern on the LCD display with different command enabled.

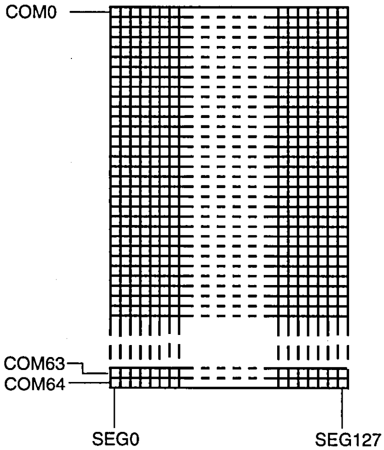


Figure 10a

		Content of GDDRAM
PAGE 1	Upper Nibble	5 A 5 A 5 A 5 A 5 A - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
	Lower Nibble	5 A 5 A 5 A 5 A 5 A - - - - - - - - - 5 A 5 A 5 A 5 A 5 A
PAGE 2	Upper Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - C C 3 3 C C 3 3 C C
	Lower Nibble	3 3 C C 3 3 C C 3 3 - - - - - - - - - C C 3 3 C C 3 3 C C
PAGE 3	Upper Nibble	0 0 0 0 F F F F 0 0 - - - - - - - - - F F 0 0 0 0 F F F F
	Lower Nibble	F F F F 0 0 0 0 F F - - - - - - - - - 0 0 F F F F 0 0 0 0
PAGE 4	Upper Nibble	F F F F F F F F 0 0 - - - - - - - - - F F 0 0 0 0 0 0 0 0
	Lower Nibble	F F F F F F F F 0 0 - - - - - - - - - F F 0 0 0 0 0 0 0 0
. . .	. . .	. . .
PAGE 9	Upper Nibble	0 0 0 0 0 0 0 0 0 0 - - - - - - - - - 0 0 0 0 0 0 0 0 0 0
	Lower Nibble	0 0 0 1 1 1 0 0 0 0 - - - - - - - - - 0 0 0 0 1 1 1 0 0 0

Figure 10b

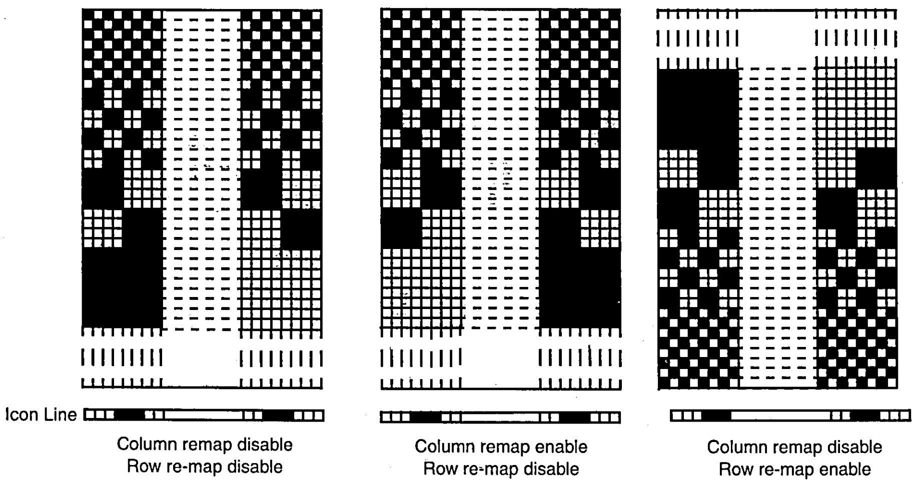


Figure 10c. Examples of LCD display with different command enabled

Power Up Sequence (Commands Required)

Command Required	POR Status	Remarks
Set Display Frequency	Normal	*1
Set Oscillator Enable	Disable	*1
Set MUX Ratio	65 MUX	*1
Set Bias Ratio	1/9 bias	*1
Set Internal DC/DC Converter	4X Converter	*1
Set Internal Regulator On	Off	*1
Set Temperature Coefficient	TC=0%	*1, *3
Set Internal Contrast Control On	Off	*1, *3
Set Contrast Level	Contrast Level = 0	*1, *2, *3
Set Smart Bias Divider On	Off	*1
Set Segment Mapping	Seg. 0 = Col. 0	
Set Common Mapping	Com. 0 = Row 0	
Set Display On	Off	

Remarks :

*1 -- Required only if desired status differ from POR.
*2 -- Effective only if Internal Contrast Control is enabled.
*3 -- Effective only if Internal Regulator is enabled.

Smart Icon Mode Output Description

There are two driving schemes of Smart Icon Mode for panel with different V_{on}/V_{off} or V_{DD} :

1) 4 - Phase Smart Icon : 1/4 ~ 3/4
   $V_{off} > V_{DD}$ * sqrt (1/4)
   $V_{on} < V_{DD}$ * sqrt (3/4)
2) 6 - Phase Smart Icon : 1/6 ~ 3/6
   $V_{off} > V_{DD}$ * sqrt (1/6)
   $V_{on} < V_{DD}$ * sqrt (3/6)

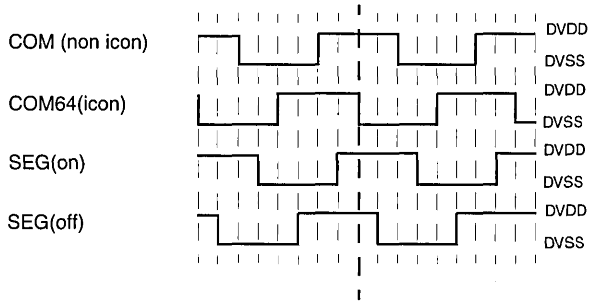


Figure 11a. LCD Driving Signal for 4 - Phase Smart Icon Mode

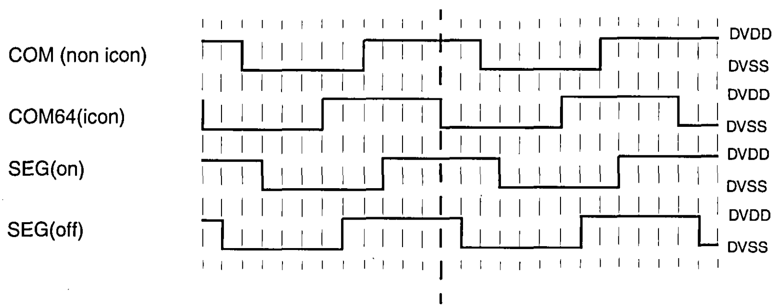
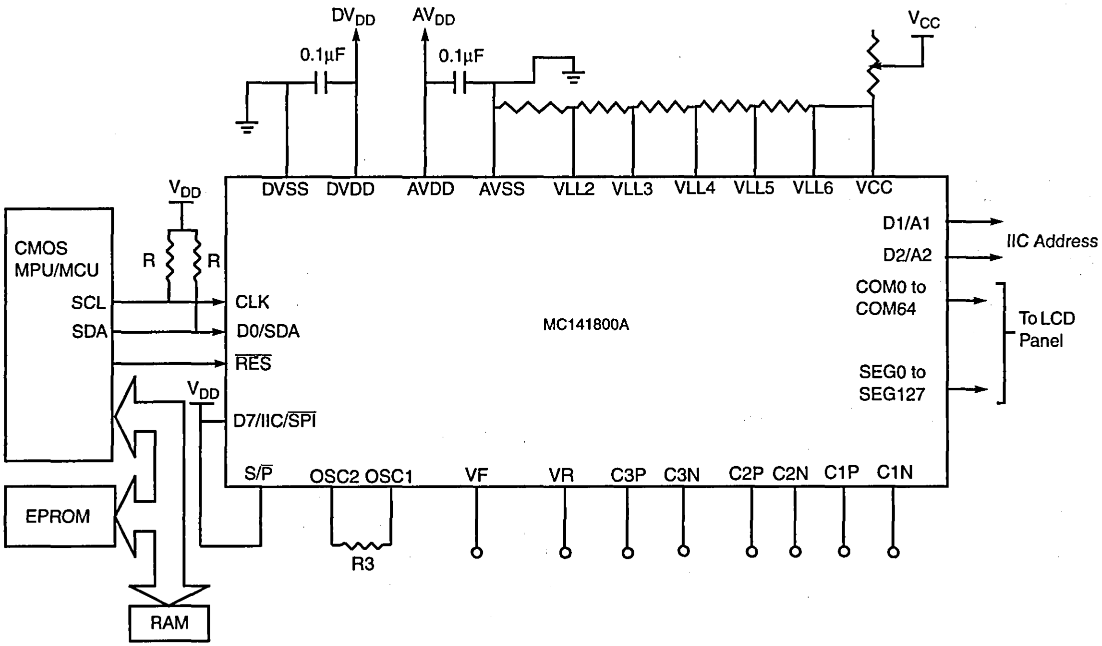


Figure 11b. LCD Driving Signal for 6 - Phase Smart Icon Mode

Application Circuit:

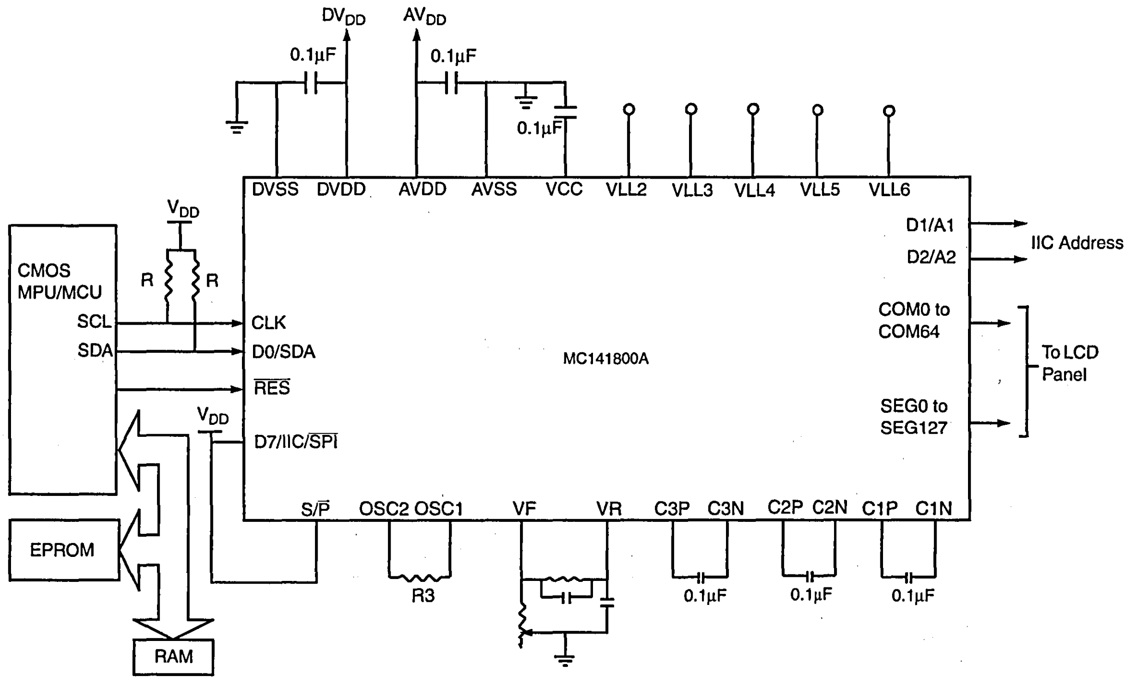
All Internal Analog Circuitry disabled at IIC Serial mode operation



Remark :

1. R3 can be omitted for external oscillator.
2. $\overline{\text{RES}}$ should be at a known state.
3. VLL2 - VLL6 can be left open for internal divider is enable.
4. R/$\overline{\text{W}}$, $\overline{\text{CE}}$, D/$\overline{\text{C}}$ and D3-D6 can be open for IIC serial mode.
5. D1/A1 and D2/A2 should be at predefined state for device identification.
6. R is pull up resistance, $R < \frac{t_r}{2 * C_{bus}}$ (R = 300 ohm for 1MHz, assume C_{bus} = 200pF)

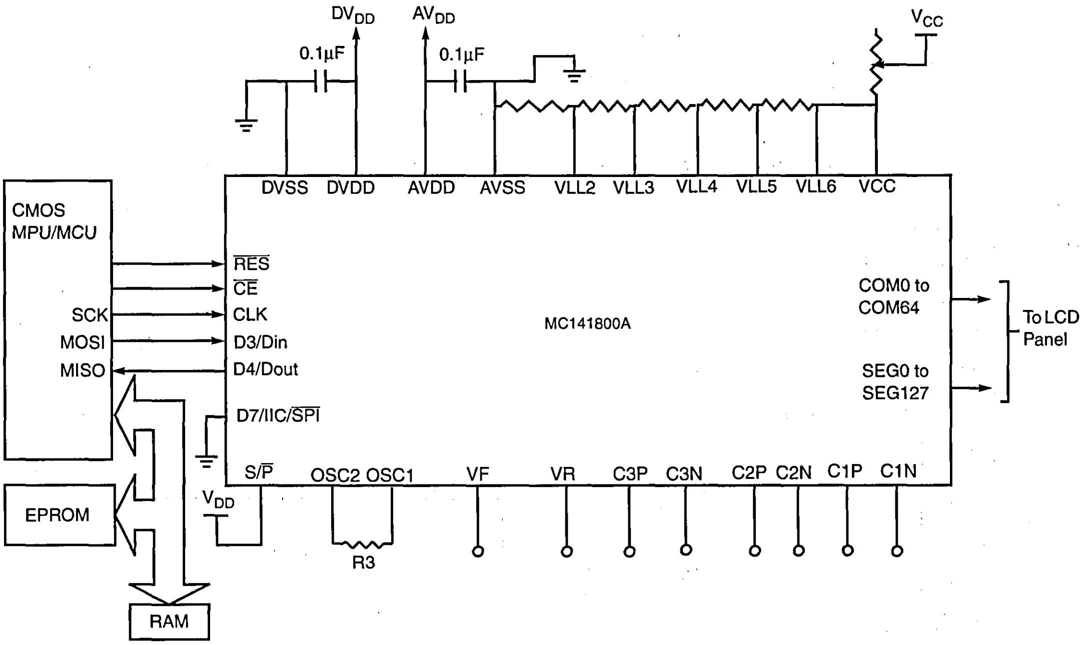
All Internal Analog Circuitry enabled at IIC Serial mode operation



Remark :

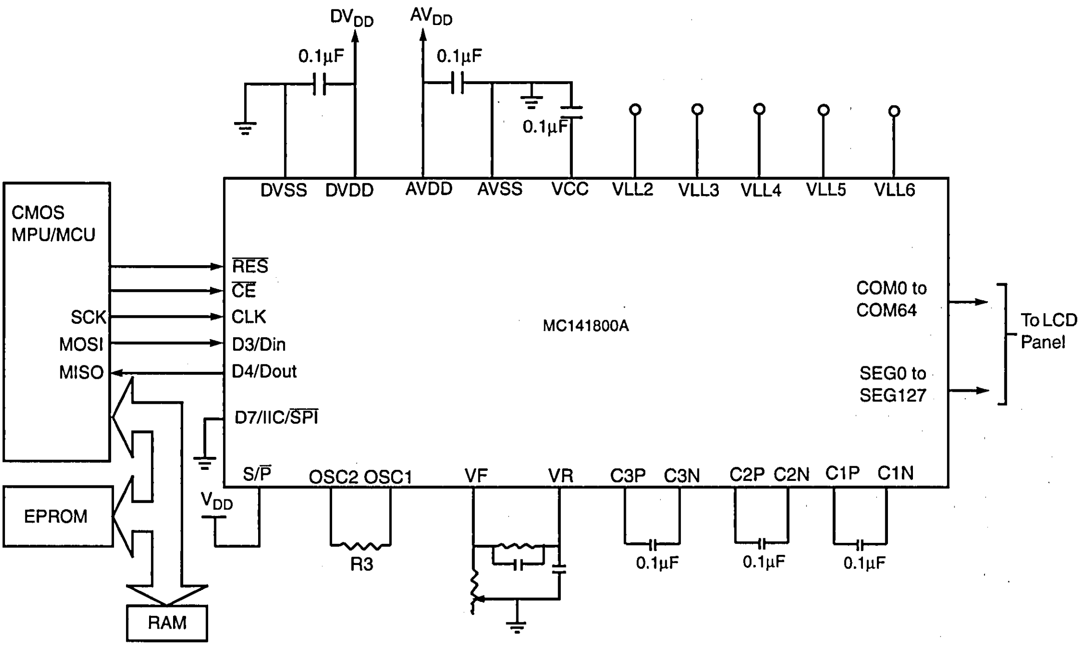
1. R3 can be omitted for external oscillator.
2. VR and VF can be left open for Internal Regulator disable and Contrast Disable.
3. $\overline{\text{RES}}$ should be at a known state.
4. R/$\overline{\text{W}}$, $\overline{\text{CE}}$, D/$\overline{\text{C}}$ and D3-D6 can be open for IIC serial mode.
5. D1/A1 and D2/A2 should be at predefined state for device identification.
6. R is pull up resistance, $R < \frac{t_r}{2 * C_{bus}}$ (R = 300 ohm for 1MHz, assume C_{bus} = 200pF)

All Internal Analog Circuitry disabled at SPI Serial mode operation



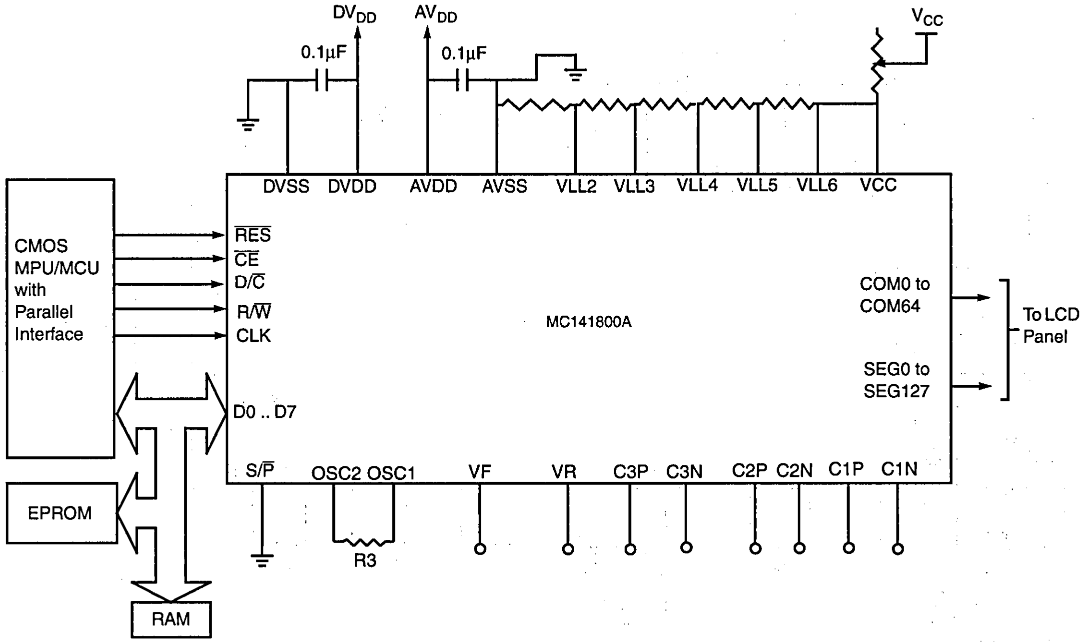
Remark :
1. R3 can be omitted for external oscillator.
2. $\overline{RES}$ should be at a known state.
3. VLL2 - VLL6 *can be left open for internal divider is enable.*
4. R/$\overline{W}$, D/$\overline{C}$, D0-2 and D5-6 can be open for SPI serial mode.

All Internal Analog Circuitry enabled at SPI Serial mode operation



Remark :
1. R3 can be omitted for external oscillator.
2. VR and VF can be left open for Internal Regulator disable and Contrast Disable.
3. $\overline{RES}$ should be at a known state.
4. R/$\overline{W}$, D/$\overline{C}$, D0-2 and D5-6 can be open for SPI serial mode.

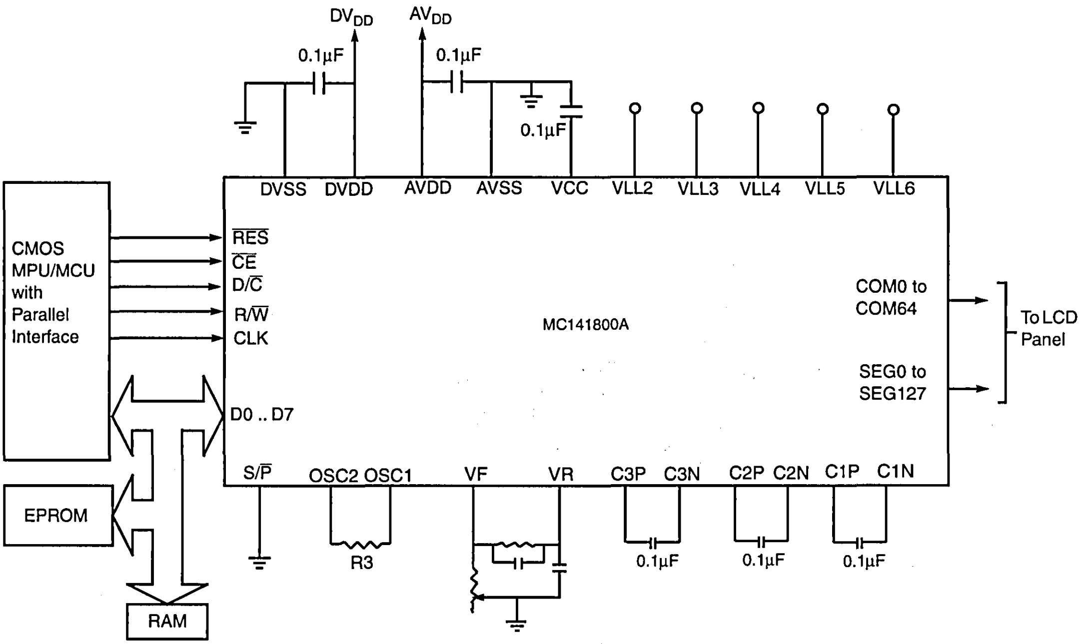
All Internal Analog Circuitry disabled at Parallel mode operation



Remark :

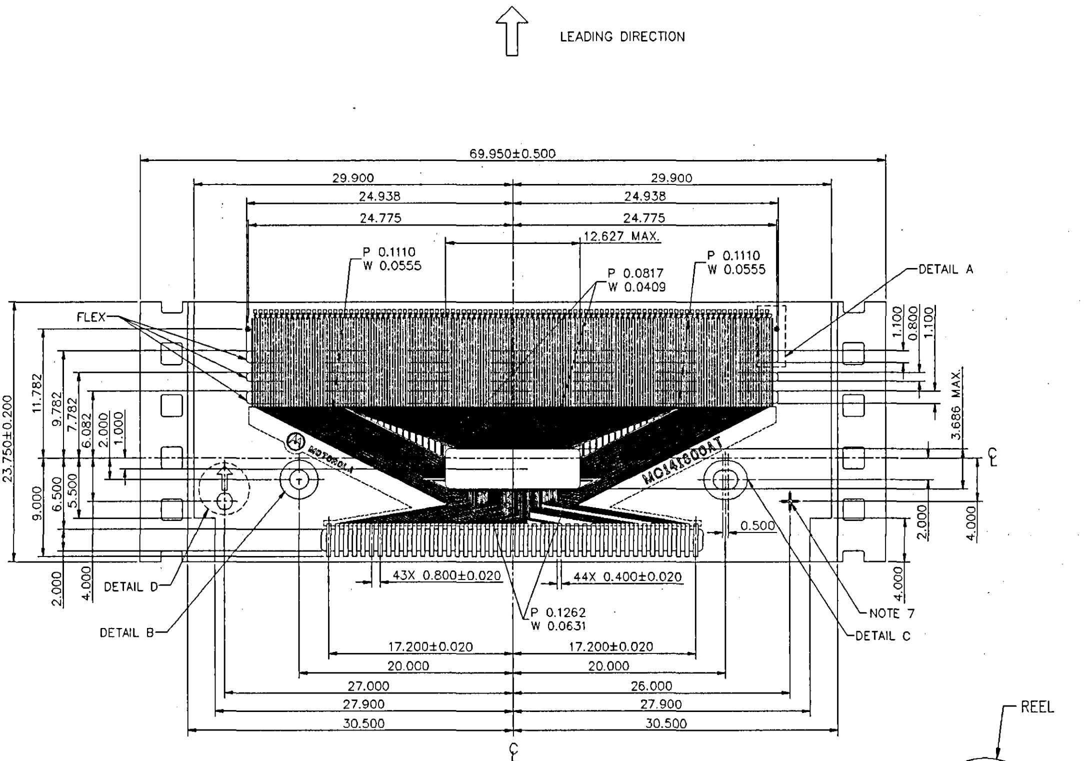
1. R3 can be omitted for external oscillator.
2. $\overline{\text{RES}}$ should be at a known state.
3. VLL2 - VLL6 can be left open for internal divider is enable.

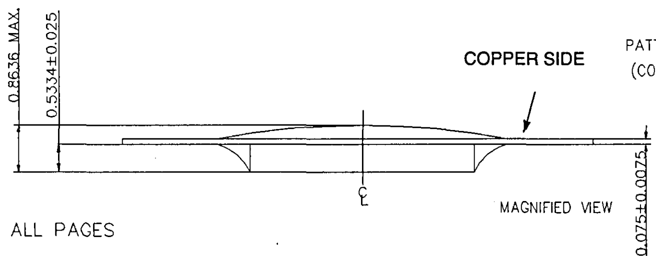
All Internal Analog Circuitry enabled at Parallel mode operation

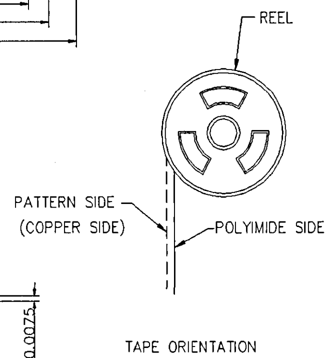


Remark :
1. R3 can be omitted for external oscillator.
2. VR and VF can be left open for Internal Regulator disable and Contrast Disable.
3. $\overline{\text{RES}}$ should be at a known state.

PACKAGE DIMENSIONS
MC141800AT
TAB PACKAGE DIMENSION - 1
(DO NOT SCALE THIS DRAWING)







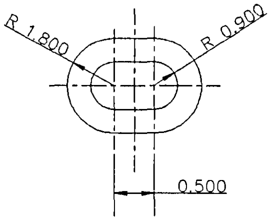
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX–S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. 5 SPROCKET HOLES DEVICE
7. OPTIONAL FEATURE FOR SPS INTERNAL USE ONLY WHICH MAY BE REPLACED BY ⌀ 2.0 MM HOLE.

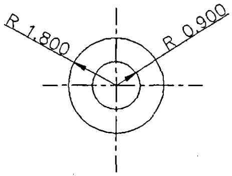
Reference : 98ASL00269A Issue "0" released on 11 Feb 97

PACKAGE DIMENSIONS

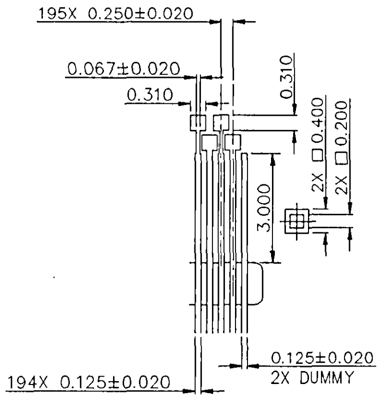
MC141800AT
TAB PACKAGE DIMENSION - 2
(DO NOT SCALE THIS DRAWING)



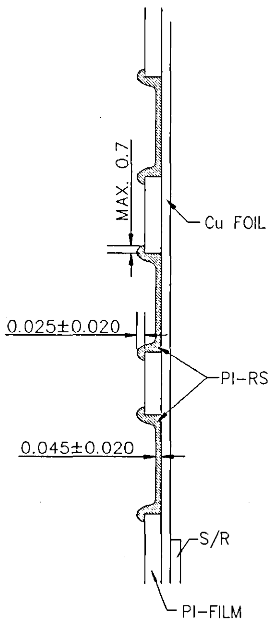
DETAIL C



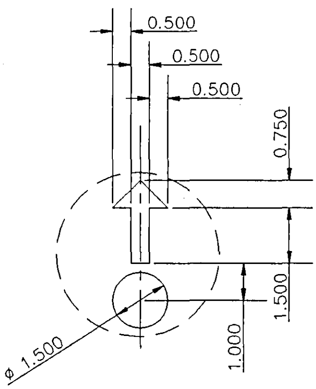
DETAIL B



DETAIL A



FLEX MATERIAL DETAIL



DETAIL D

Reference : 98ASL00269A Issue "0" released on 11 Feb 97

Die Pad Coordinate of MC141800A

Pad	Name	X(um)	Y(um)	Pad	Name	X(um)	Y(um)	Pad	Name	X(um)	Y(um)	Pad	Name	X(um)	Y(um)	Pad	Name	X(um)	Y(um)
1	COM(22)	-4826.0	-807.6	61	C3P	1198.4	-857.8	121	SEG(0)	4826.0	807.6	181	SEG(60)	266.0	807.6	241	SEG(120)	-4294.0	807.6
2	COM(23)	-4750.0	-807.6	62	C3N	1304.4	-857.8	122	SEG(1)	4750.0	807.6	182	SEG(61)	190.0	807.6	242	SEG(121)	-4370.0	807.6
3	COM(24)	-4674.4	-811.8	63	VLL2:	1410.4	-857.8	123	SEG(2)	4674.0	807.6	183	SEG(62)	114.0	807.6	243	SEG(122)	-4446.0	807.6
4	COM(25)	-4598.0	-807.6	64	VLL2:	1516.4	-857.8	124	SEG(3)	4598.0	807.6	184	SEG(63)	38.0	807.6	244	SEG(123)	-4522.0	807.6
5	COM(26)	-4522.0	-807.6	65	VLL3:	1622.4	-857.8	125	SEG(4)	4522.0	807.6	185	SEG(64)	-38.0	807.6	245	SEG(124)	-4598.0	807.6
6	COM(27)	-4446.0	-807.6	66	VLL3:	1728.4	-857.8	126	SEG(5)	4446.0	807.6	186	SEG(65)	-114.0	807.6	246	SEG(125)	-4674.0	807.6
7	COM(28)	-4370.0	-807.6	67	VLL4:	1834.4	-857.8	127	SEG(6)	4370.0	807.6	187	SEG(66)	-190.0	807.6	247	SEG(126)	-4750.0	807.6
8	COM(29)	-4294.0	-807.6	68	VLL4:	1940.4	-857.8	128	SEG(7)	4294.0	807.6	188	SEG(67)	-266.0	807.6	248	SEG(127)	-4826.0	807.6
9	COM(30)	-4218.0	-807.6	69	VLL5:	2046.4	-857.8	129	SEG(8)	4218.0	807.6	189	SEG(68)	-342.0	807.6	249	COM64B	-5328.4	835.4
10	COM(31)	-4142.0	-807.6	70	VLL5:	2152.4	-857.8	130	SEG(9)	4142.0	807.6	190	SEG(69)	-418.0	807.6	250	COM(0)	-5328.4	759.4
11	DVDD:	-4042.2	-857.8	71	VLL6:	2258.4	-857.8	131	SEG(10)	4066.0	807.6	191	SEG(70)	-494.0	807.6	251	COM(1)	-5328.4	683.4
12	S/P	-3940.6	-857.8	72	VLL6:	2364.4	-857.8	132	SEG(11)	3990.0	807.6	192	SEG(71)	-570.0	807.6	252	COM(2)	-5328.4	607.4
13	RES	-3839.0	-857.8	73	DVSS:	2470.4	-857.8	133	SEG(12)	3914.0	807.6	193	SEG(72)	-646.0	807.6	253	COM(3)	-5328.4	531.4
14	D/C	-3737.4	-857.8	74	OSC1	2576.4	-857.8	134	SEG(13)	3838.0	807.6	194	SEG(73)	-722.0	807.6	254	COM(4)	-5328.4	455.4
15	DVSS:	-3569.0	-857.8	75	DVSS:	2682.4	-857.8	135	SEG(14)	3762.0	807.6	195	SEG(74)	-798.0	807.6	255	COM(5)	-5328.4	379.4
16	DVSS:	-3467.4	-857.8	76	DVSS:	2788.4	-857.8	136	SEG(15)	3686.0	807.6	196	SEG(75)	-874.0	807.6	256	COM(6)	-5328.4	303.4
17	DVSS:	-3365.8	-857.8	77	VCC:	2894.4	-857.8	137	SEG(16)	3610.0	807.6	197	SEG(76)	-950.0	807.6	257	COM(7)	-5328.4	227.4
18	DVSS:	-3264.2	-857.8	78	VCC:	3000.4	-857.8	138	SEG(17)	3534.0	807.6	198	SEG(77)	-1026.0	807.6	258	COM(8)	-5328.4	151.4
19	DVSS:	-3162.6	-857.8	79	AVSS:	3106.4	-857.8	139	SEG(18)	3458.0	807.6	199	SEG(78)	-1102.0	807.6	259	COM(9)	-5328.4	75.4
20	DVSS:	-3061.0	-857.8	80	OSC2	3212.4	-857.8	140	SEG(19)	3382.0	807.6	200	SEG(79)	-1178.0	807.6	260	COM(10)	-5328.4	-0.6
21	DVSS:	-2959.4	-857.8	81	AVDD:	3318.4	-857.8	141	SEG(20)	3306.0	807.6	201	SEG(80)	-1254.0	807.6	261	COM(11)	-5328.4	-76.6
22	DVSS:	-2857.8	-857.8	82	DVSS:	3493.0	-857.8	142	SEG(21)	3230.0	807.6	202	SEG(81)	-1330.0	807.6	262	COM(12)	-5328.4	-152.6
23	DVSS:	-2756.2	-857.8	83	DVSS:	3594.6	-857.8	143	SEG(22)	3154.0	807.6	203	SEG(82)	-1406.0	807.6	263	COM(13)	-5328.4	-228.6
24	DVSS:	-2654.6	-857.8	84	DVSS:	3696.2	-857.8	144	SEG(23)	3078.0	807.6	204	SEG(83)	-1482.0	807.6	264	COM(14)	-5328.4	-304.6
25	DVSS:	-2553.0	-857.8	85	DVSS:	3797.8	-857.8	145	SEG(24)	3002.0	807.6	205	SEG(84)	-1558.0	807.6	265	COM(15)	-5328.4	-380.6
26	DVSS:	-2451.4	-857.8	86	DVSS:	3899.4	-857.8	146	SEG(25)	2926.0	807.6	206	SEG(85)	-1634.0	807.6	266	COM(16)	-5328.4	-456.6
27	DVSS:	-2349.8	-857.8	87	DVSS:	4001.0	-857.8	147	SEG(26)	2850.0	807.6	207	SEG(86)	-1710.0	807.6	267	COM(17)	-5328.4	-532.6
28	DVSS:	-2248.2	-857.8	88	COM64A	4142.0	-807.6	148	SEG(27)	2774.0	807.6	208	SEG(87)	-1786.0	807.6	268	COM(18)	-5328.4	-608.6
29	DVSS:	-2146.6	-857.8	89	COM(63)	4217.0	-806.2	149	SEG(28)	2698.0	807.6	209	SEG(88)	-1862.0	807.6	269	COM(19)	-5328.4	-684.6
30	DVSS:	-2045.0	-857.8	90	COM(62)	4293.0	-806.2	150	SEG(29)	2622.0	807.6	210	SEG(89)	-1938.0	807.6	270	COM(20)	-5328.4	-760.6
31	DVSS:	-1943.4	-857.8	91	COM(61)	4369.0	-806.2	151	SEG(30)	2546.0	807.6	211	SEG(90)	-2014.0	807.6	271	COM(21)	-5328.4	-836.6
32	DVSS:	-1841.8	-857.8	92	COM(60)	4445.0	-806.2	152	SEG(31)	2470.0	807.6	212	SEG(91)	-2090.0	807.6				
33	DVSS:	-1740.2	-857.8	93	COM(59)	4521.0	-806.2	153	SEG(32)	2394.0	807.6	213	SEG(92)	-2166.0	807.6				
34	R/W	-1638.6	-857.8	94	COM(58)	4597.0	-806.2	154	SEG(33)	2318.0	807.6	214	SEG(93)	-2242.0	807.6				
35	D7	-1537.0	-857.8	95	COM(57)	4673.0	-806.2	155	SEG(34)	2242.0	807.6	215	SEG(94)	-2318.0	807.6				
36	D6	-1435.4	-857.8	96	COM(56)	4749.0	-806.2	156	SEG(35)	2166.0	807.6	216	SEG(95)	-2394.0	807.6				
37	D5	-1333.8	-857.8	97	COM(55)	4826.0	-807.6	157	SEG(36)	2090.0	807.6	217	SEG(96)	-2470.0	807.6				
38	D4	-1232.2	-857.8	98	COM(54)	5328.4	-836.6	158	SEG(37)	2014.0	807.6	218	SEG(97)	-2546.0	807.6				
39	D3	-1130.6	-857.8	99	COM(53)	5328.4	-760.6	159	SEG(38)	1938.0	807.6	219	SEG(98)	-2622.0	807.6				
40	D2	-1029.0	-857.8	100	COM(52)	5328.4	-684.6	160	SEG(39)	1862.0	807.6	220	SEG(99)	-2698.0	807.6				
41	D1	-927.4	-857.8	101	COM(51)	5328.4	-608.6	161	SEG(40)	1786.0	807.6	221	SEG(100)	-2774.0	807.6				
42	D0	-825.8	-857.8	102	COM(50)	5328.4	-532.6	162	SEG(41)	1710.0	807.6	222	SEG(101)	-2850.0	807.6				
43	D0	-724.2	-857.8	103	COM(49)	5328.4	-456.6	163	SEG(42)	1634.0	807.6	223	SEG(102)	-2926.0	807.6				
44	CLK	-622.6	-857.8	104	COM(48)	5328.4	-380.6	164	SEG(43)	1558.0	807.6	224	SEG(103)	-3002.0	807.6				
45	CLK	-521.0	-857.8	105	COM(47)	5328.4	-304.6	165	SEG(44)	1482.0	807.6	225	SEG(104)	-3078.0	807.6				
46	CE	-419.6	-857.8	106	COM(46)	5328.4	-228.6	166	SEG(45)	1406.0	807.6	226	SEG(105)	-3154.0	807.6				
47	DVDD:	-317.8	-857.8	107	COM(45)	5328.4	-152.6	167	SEG(46)	1330.0	807.6	227	SEG(106)	-3230.0	807.6				
48	DVDD:	-216.2	-857.8	108	COM(44)	5328.4	-76.6	168	SEG(47)	1254.0	807.6	228	SEG(107)	-3306.0	807.6				
49	DVSS:	-114.6	-857.8	109	COM(43)	5328.4	-0.6	169	SEG(48)	1178.0	807.6	229	SEG(108)	-3382.0	807.6				
50	DVSS:	-13.0	-857.8	110	COM(42)	5328.4	75.4	170	SEG(49)	1102.0	807.6	230	SEG(109)	-3458.0	807.6				
51	AVDD:	138.4	-857.8	111	COM(41)	5328.4	151.4	171	SEG(50)	1026.0	807.6	231	SEG(110)	-3534.0	807.6				
52	AVDD:	244.4	-857.8	112	COM(40)	5328.4	227.4	172	SEG(51)	950.0	807.6	232	SEG(111)	-3610.0	807.6				
53	AVSS:	350.4	-857.8	113	COM(39)	5328.4	303.4	173	SEG(52)	874.0	807.6	233	SEG(112)	-3686.0	807.6				
54	AVSS:	456.4	-857.8	114	COM(38)	5328.4	379.4	174	SEG(53)	798.0	807.6	234	SEG(113)	-3762.0	807.6				
55	VF	562.4	-857.8	115	COM(37)	5328.4	455.4	175	SEG(54)	722.0	807.6	235	SEG(114)	-3838.0	807.6				
56	VR	668.4	-857.8	116	COM(36)	5328.4	531.4	176	SEG(55)	646.0	807.6	236	SEG(115)	-3914.0	807.6				
57	C1P	774.4	-857.8	117	COM(35)	5328.4	607.4	177	SEG(56)	570.0	807.6	237	SEG(116)	-3990.0	807.6				
58	C1N	880.4	-857.8	118	COM(34)	5328.4	683.4	178	SEG(57)	494.0	807.6	238	SEG(117)	-4066.0	807.6				
59	C2P	986.4	-857.8	119	COM(33)	5328.4	759.4	179	SEG(58)	418.0	807.6	239	SEG(118)	-4142.0	807.6				
60	C2N	1092.4	-857.8	120	COM(32)	5328.4	835.4	180	SEG(59)	342.0	807.6	240	SEG(119)	-4218.0	807.6				

Note : *Power and ground die pads should be bonded correspondingly in COG application

Die Pad 15 - 33, 43, 45, 47 -54, 64, 66, 68, 70, 72 - 73, 76, 78 and 82 - 87 are multiple pads of critical signal

(Basically, these are D0, CLK, DVDD, DVSS, AVDD, AVSS, VCC and VLL2-VLL6 which special design for COG)

Bump Size :

Pad	X(um)	Y(um)
1-10	42	100
11-87	65	65
88-97	42	100
98-120	100	42
121-248	42	100
249-271	100	42

Die Size (including scribe) : 11226.8 x 2286 (um)

MC141562

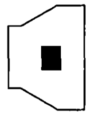
LCD Common (Row) Driver
CMOS

The MC141562 is a high volt, high MUX passive LCD common driver. It is a low power silicon-gate CMOS LCD driver chip which consists of 100-channel common driving outputs for a high MUX (up to 300 MUX) large dot matrix passive LCD panel.

This chip can be configured as 100CH X 1 or 50CH X 2 mode of operation. The 28 V high voltage output driving cells can be controlled by low voltage (3.0 volts) logic input.

The MC141562 will provide the best performance in combination with the MC141563 (segment driver).

- Operating Supply Voltage Range -
  Control Logic, Shift Register (VDD): 2.7V to 5.5V
  Common Drivers (VLCD): 10 V to 28 V
- Operating Temperature Range: -20 to 70°C
- 100 LCD Common Driving Outputs.
- Driving Duty Cycle (MUX) : 1/100 to 1/300.
- Bi-directional Shift Register with 100CH X 1 or 50CH X 2 Mode of Operation.
- Interchangeable Carry-In / Carry-Out Terminals.
- Left / Right Shift Mode Selection.
- Cascadable.
- Maximum Shift Clock Frequency = 1.0 MHz
- Available in TAB (Tape Automated Bonding), 115 pins

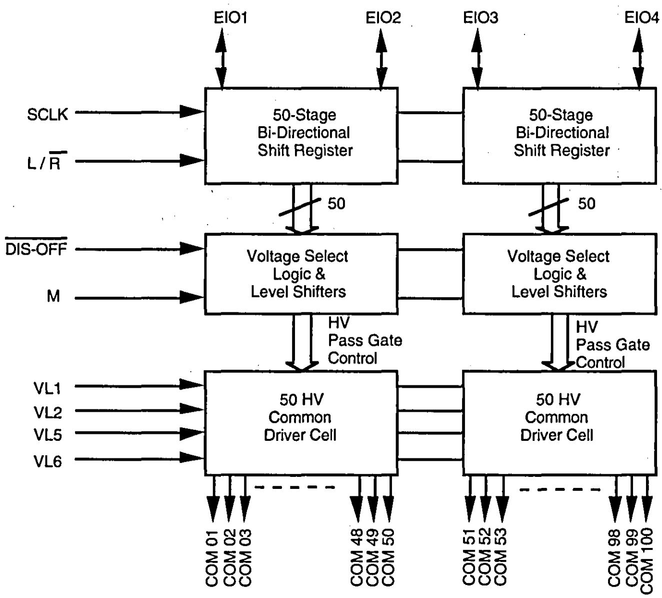


MC141562T
TAB

ORDERING INFORMATION

MC141562T TAB

BLOCK DIAGRAM



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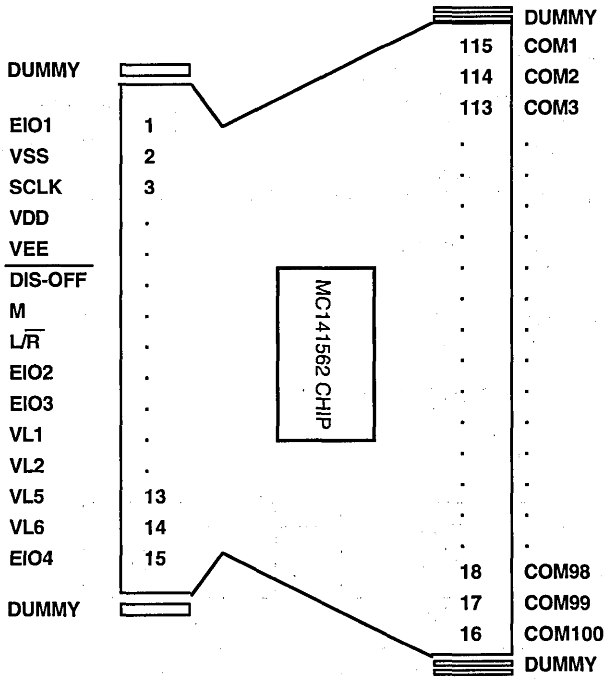


Figure 1. TAB Package Contact Assignment (Copper View)

MAXIMUM RATINGS*(Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6.0	V
V_{EE}		-0.3 to -24.0	V
V_{LCD}	DC Supply Voltage (V_{DD} - V_{EE})	V_{DD} to +30	V
V_{Din} V_{Ain}	Input Voltage All Digital Input V_{LCD} Level Input	 V_{SS}-0.3 to V_{DD}+0.3 V_{EE}-0.3 to V_{DD}+0.3	 V V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to 70	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
 V_{DD} V_{LCD}	Operating Voltage Supply Voltage (reference to V_{SS}) LCD Supply Voltage (V_{DD} - V_{EE})		 2.7 10.0	 - -	 5.5 28.0	V V
 I_{DP} I_{SB}	Supply Current (V_{DD} Pin) Display Mode Standby Mode	V_{DD}=5.5V, V_{EE}=-23V SCLK = 200KHz, M=2KHz	 - -	 40 0.3	 100 2	 µA µA
 I_{DP} I_{SB}	Supply Current (V_{DD} Pin) Display Mode Standby Mode	V_{DD}=2.7V, V_{EE}=-23V SCLK = 200KHz, M=2KHz	 - -	 20 0.3	 - -	 µA µA
I_{EE}	Supply Current at V_{EE}	No Load	-	30	150	µA
 V_{OL} V_{OH}	Common Output Voltage VL5,6=V_{EE} VL1,2=V_{DD} COM1-COM100	Iload = 150µA	 - V_{DD}-0.3	 - -	 V_{EE}+0.3 -	 V V
V_{OH} V_{OL}	Output High Voltage Output Low Voltage EIO1, EIO2, EIO3, EIO4	V_{DD}=5.0V, Iload=1mA	V_{DD}-1.0 -	- -	- V_{SS}+1.0	V V
V_{IH} V_{IL}	Input High Voltage Input Low Voltage SCLK, L/$\overline{R}$, EIO1, EIO2, EIO3, EIO4, M, $\overline{DIS\text{-}OFF}$		0.7xV_{DD} V_{SS}	- -	V_{DD} 0.2xV_{DD}	V V
I_{in}	Input Current SCLK, L/$\overline{R}$, EIO1, EIO2, EIO3, EIO4, M, $\overline{DIS\text{-}OFF}$		-	±0.5	±1	µA
C_{in}	Capacitance SCLK, L/$\overline{R}$, EIO1, EIO2, EIO3, EIO4, M, $\overline{DIS\text{-}OFF}$		-	5	10	pF
I_{OHX}, I_{OLX}	Common Output Current COM1-COM100	V_{OH}= V_{DD} - 0.3V, V_{OL}=V_{EE} +0.3V	±150	-	-	µA
I_{OHC}, I_{OLC}	Carry Output Current EIO1, EIO2, EIO3, EIO4	V_{OH}= V_{DD} - 1.0V, V_{OL}=V_{SS} +1.0V	±1.0	-	-	mA
R_{ON}	Common Output Impedance Common Output Impedance Variance	V_{DD} - V_{EE} =28V, I_{OHX}, I_{OLX}=±150µA	- -	1 ±10	2 ±30	K Ohm %

AC ELECTRICAL CHARACTERISTICS -WRITE CYCLE (V_{DD} =5.0V, V_{SS} = 0V, V_{EE} = -23V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{TLH} t_{THL}	Digital Input Rise and Fall Time SCLK, M, EIO1,2,3,4, $\overline{\text{DIS-OFF}}$	- -	25 25	50 50	ns ns
$t_{SCØ}$	Shift Clock (SCLK) Cycle	1000	-	-	ns
t_{SCH}	Shift Clock (SCLK) Pulse Width HIGH	150	-	-	ns
t_{SCL}	Shift Clock (SCLK) Pulse Width LOW	150	-	-	ns
t_{SUE}	Enable Input (EIO) to Shift Clock (SCLK) Set up Time	100	-	-	ns
t_{he}	Enable Input (EIO) to Shift Clock (SCLK) Hold Time	100	-	-	ns
t_{PEO}	Shift Clock (SCLK) to Enable Output (EIO) Delay Time CL = 25pF	-	-	100	ns

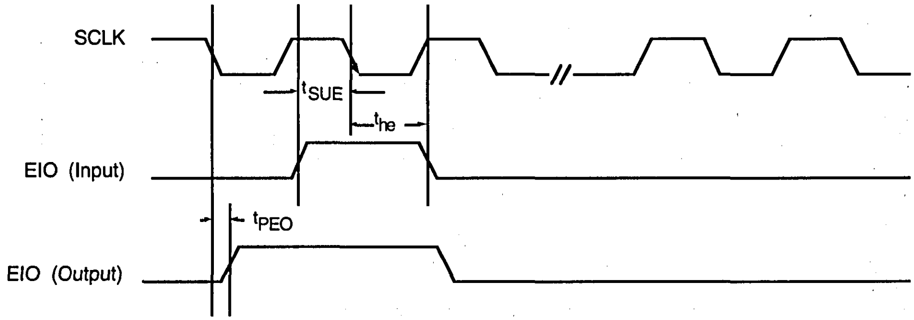


Figure 2. SCLK, EIO Input and Output Propagation Delay Timing Diagram

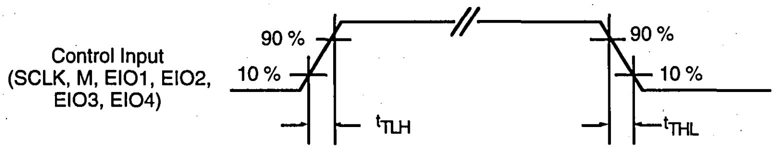


Figure 3. Control Input Rise and Fall Timing Diagram

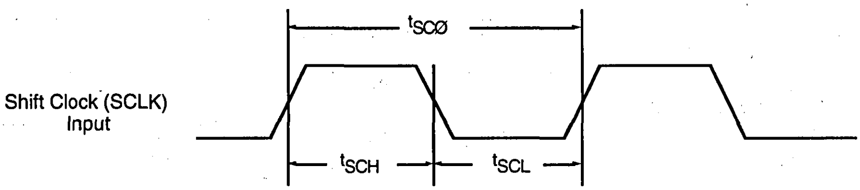


Figure 4. Shift Clock Pulse Width High and Pulse Width Low Timing Diagram

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

The main dc power is supplied to the part by these two connections. V_{DD} is the most-positive supply level and V_{SS} is ground.

VEE

This supply connection provides the negative power supply voltage for the common drivers.

VL1, VL2, VL5, VL6

These input pins are connected to the external voltage divider (See Figure 5).
Voltage supply level for the LCD :
VL1, VL6 : On-level of the LC
VL2, VL5 : Off-level of the LC

Carry Shift Clock (SCLK)

Carry input is strobed into the shift register by the falling edge of the SCLK.

Left / Right Shift Select ($L / \overline{R}$)

This input pin determines the direction of the shift register operation (See Table 1).

$L / \overline{R}$ = "0", the carry will shift right (COM. 1 to COM. 100).
$L / \overline{R}$ = "1", the carry will shift left (COM. 100 to COM. 1).

Carry-In / Carry-Out (EIO1, EIO2, EIO3, EIO4)

These four input / output pins perform the Carry-In and Carry-Out function depending on the shift register direction of operation. EIO1 and EIO2 are used as the I/O pins of the COM1 to COM50 block, while EIO3 and EIO4 are used as I/O pins for the COM51 to COM100 block. In right shift mode ($L / \overline{R}$ = "0"), the EIO1/EIO3 is the Carry-In input while the EIO2/EIO4 will be the Carry-Out output for cascading. In left shift mode ($L / \overline{R}$ = "1"), the pin functions and operation are reversed. In case of 100 CH application, EIO2 and EIO3 should be connected together.

Frame Signal Input (M)

This input signal is the Frame Sync. Signal which provides an frame alternating output format of the output (See Figure 6).

M	1	0	1	0
EIO (Input)	1	0	0	1
Output	VL1	VL2	VL5	VL6

Display-Off Enable ($\overline{\text{DIS-OFF}}$)

This input pin is active low. If set "LOW", all output pins (Common 1 to Common 100) are forced to VL1.

Common Output (Common 1 to Common 100)

These 100 output lines provide the high volt common signal to the LCD panel. They are all at VL1 while display is turned off.

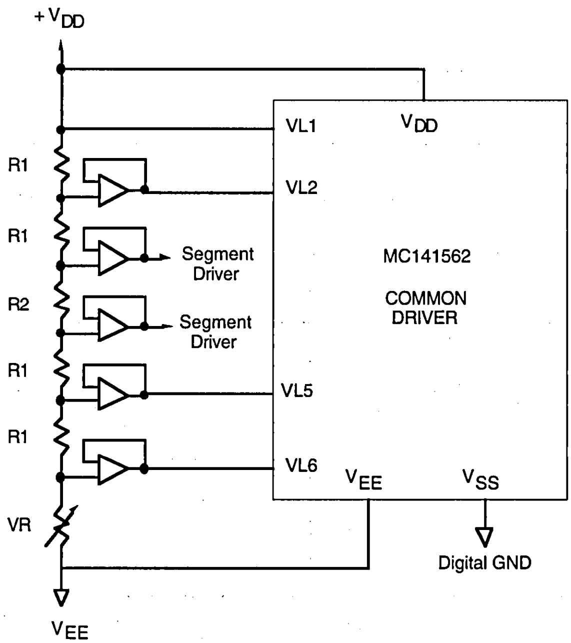


Figure 5. External Voltage Divider

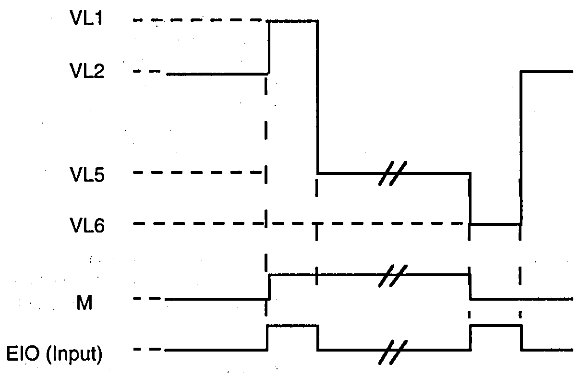


Figure 6. EIO Input, M Signal and Common Output Format

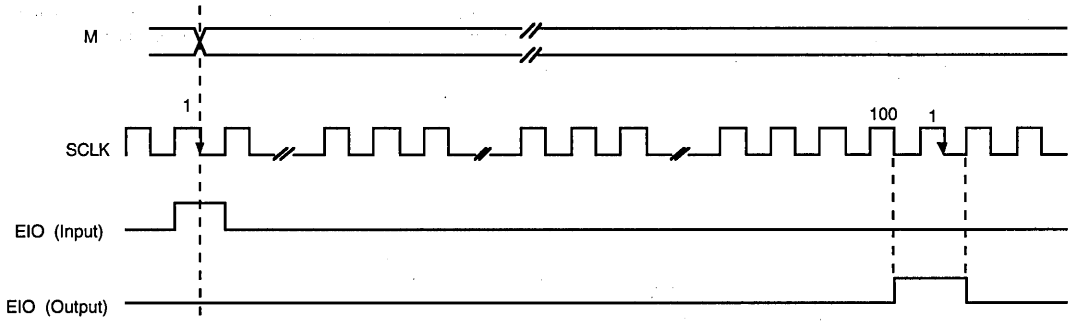


Figure 7. SCLK, M Signal and EIO Input and Output Timing Diagram

	EIO				
L / $\overline{R}$	1	2	3	4	Common Output
H	output			input	COM 100, 99 - - - - - - - - COM 2, 1
	output	input	output	input	COM 100, 99 - - - - - - - -► COM 52, 51 COM 50, 49 - - - - - - - -► COM 2, 1
L	input			output	COM 1, 2 - - - - - - - - COM 99, 100
	input	output	input	output	COM 1, 2 - - - - - - - - -► COM 49, 50 COM 51, 52 - - - - - - - -► COM 99, 100

Table 1. Left / Right Shift Control, EIO and Common Output Relation

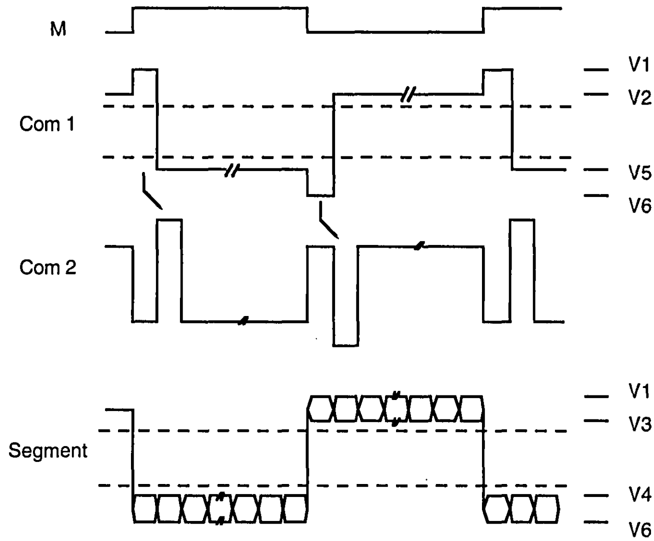
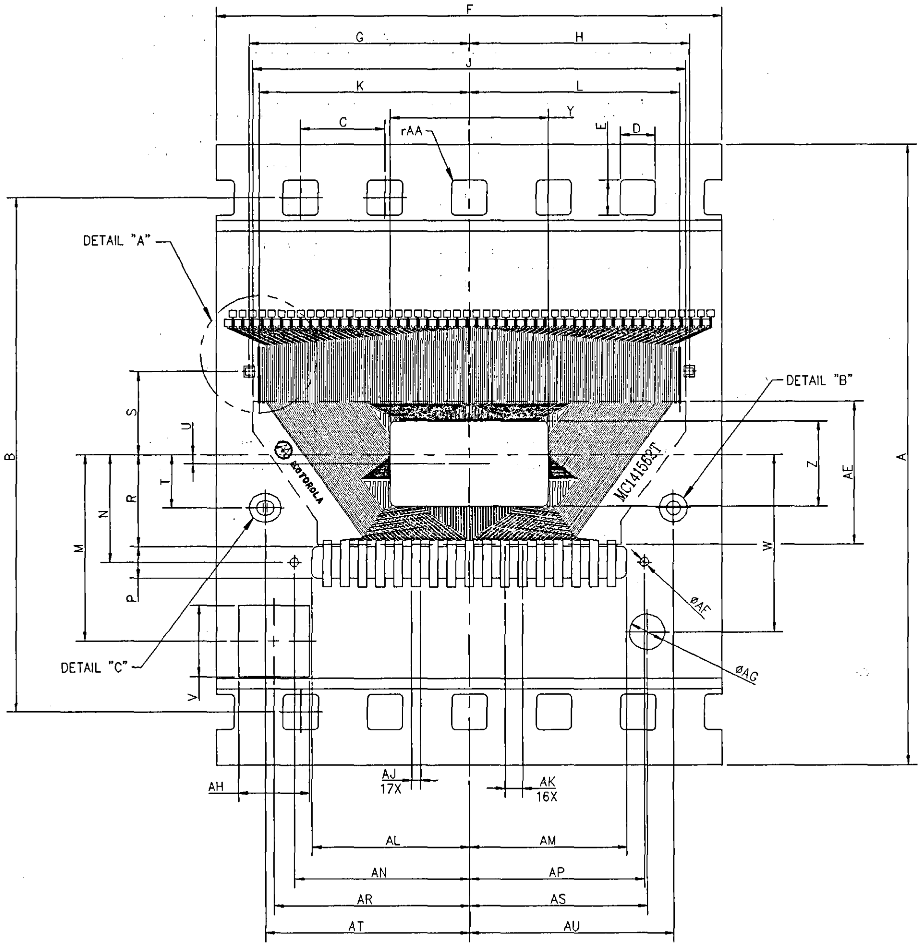
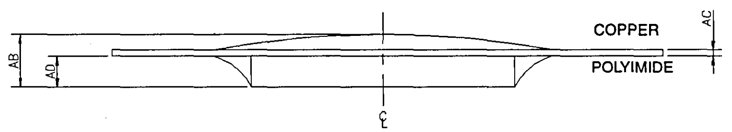


Figure 8. M Signal, Common and Segment Output Format

PACKAGE DIMENSIONS

MC141562T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)

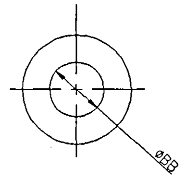




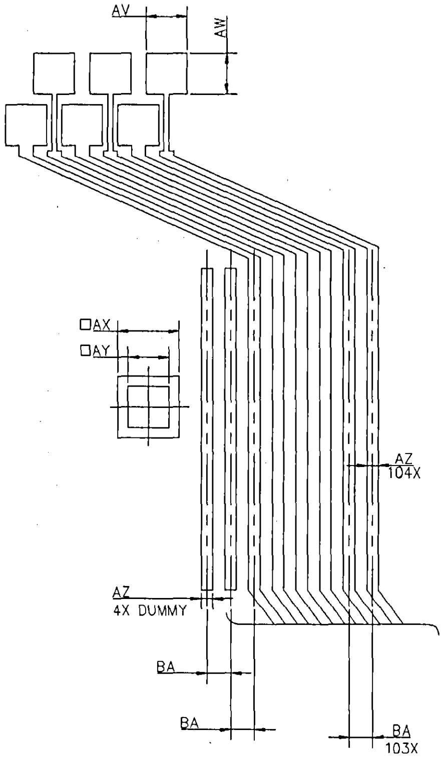
MAGNIFIED VIEW

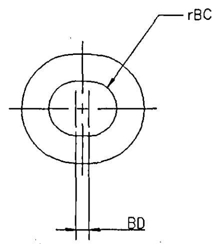
Reference : 98ASL00130A	Issue "0" released on 04/15/94

MC141562T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



DETAIL "B"





DETAIL "C"

DETAIL "A"

Reference : 98ASL00130A	Issue "0" released on 04/15/94

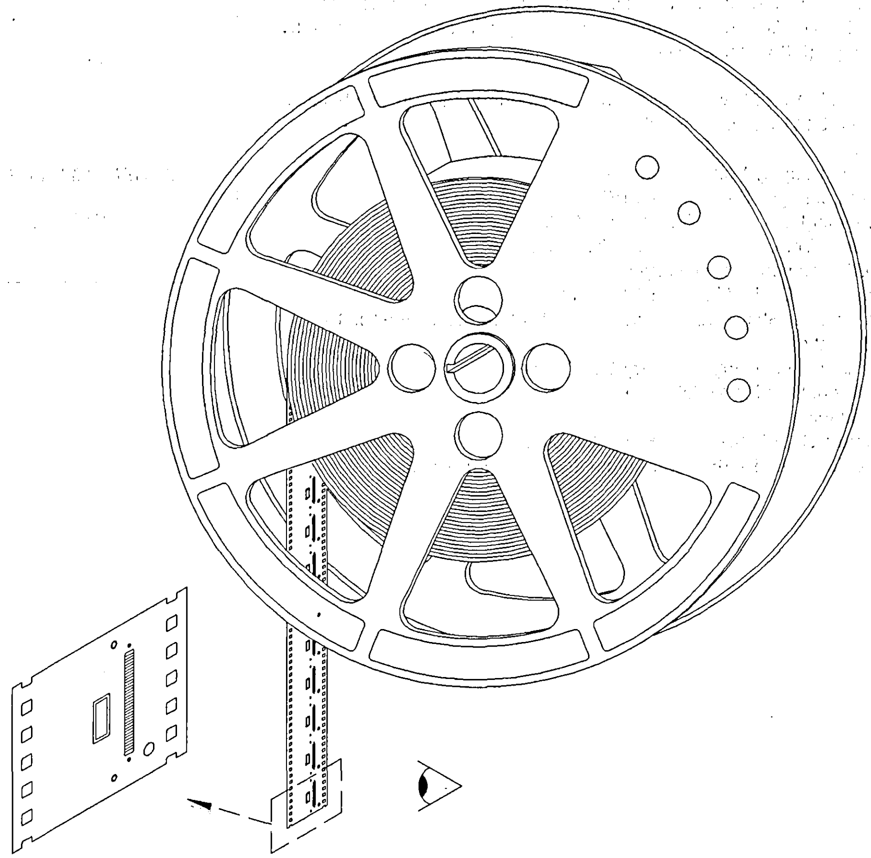
MC141562T TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	**Min**	**Max**	**Min**	**Max**	**Dim**	**Min**	**Max**	**Min**	**Max**
A	34.775	35.175	1.3691	1.3848	AD	0.579	0.629	0.0228	0.0248
B	28.927	29.027	1.1389	1.1428	AE	7.765	8.365	0.3057	0.3293
C	4.720	4.780	0.1858	0.1882	AF	0.450	0.550	0.0177	0.0217
D	1.951	2.011	0.0768	0.0792	AG	1.950	2.050	0.0768	0.0807
E	1.951	2.011	0.0768	0.0792	AH	3.950	4.050	0.1555	0.1594
F	28.000	29.000	1.1024	1.1417	AJ	0.480	0.520	0.0189	0.0205
G	12.365	12.465	0.4868	0.4907	AK	0.990	1.010	0.0390	0.0398
H	12.365	12.465	0.4868	0.4907	AL	8.800	8.900	0.3465	0.3504
J	24.100	24.700	0.9488	0.9724	AM	8.800	8.900	0.3465	0.3504
K	11.821	11.869	0.4654	0.4673	AN	9.800	9.900	0.3858	0.3898
L	11.821	11.869	0.4654	0.4673	AP	9.800	9.900	0.3858	0.3898
M	10.000	11.000	0.3937	0.4331	AR	10.500	11.500	0.4134	0.4528
N	6.005	6.105	0.2364	0.2404	AS	9.500	10.500	0.3740	0.4134
P	1.750	1.850	0.0689	0.0728	AT	11.450	11.550	0.4508	0.4547
R	5.105	5.205	0.2010	0.2049	AU	11.450	11.550	0.4508	0.4547
S	4.643	4.743	0.1828	0.1867	AV	0.350	0.450	0.0138	0.0177
T	2.950	3.050	0.1161	0.1201	AW	0.350	0.450	0.0138	0.0177
U	0.000	1.000	0.0000	0.0394	AX	0.580	0.620	0.0228	0.0244
V	3.950	4.050	0.1555	0.1594	AY	0.380	0.420	0.0150	0.0165
W	9.500	10.500	0.3740	0.4134	AZ	0.090	0.130	0.0035	0.0051
Y	-	8.880	-	0.3496	BA	0.220	0.240	0.0087	0.0094
Z	-	4.820	-	0.1898	BB	0.750	0.850	0.0295	0.0335
AA	-	0.200	-	0.0079	BC	0.350	0.450	0.0138	0.0177
AB	0.686	0.838	0.0270	0.0330	BD	0.150	0.250	0.0059	0.0098
AC	0.068	0.083	0.0027	0.0032					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper Thickness: 1oz.
4. Tin plating thickness: 0.4μm
5. 6 sprocket hole device

Reference : 98ASL00130A	Issue “0” released on 04/15/94

TAB TAPE REEL ORIENTATION



Reference : 98ASL00130A	Issue "0" released on 04/15/94

LCD Segment (Column) Driver
CMOS

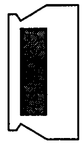
The MC141563 is a high volt, high MUX passive LCD segment driver. It is a CMOS LCD driver chip which consists of 80-channel segment driving outputs for a high MUX (up to 300 MUX) large dot matrix passive LCD panel.

This chip interfaces with 4-bit or 8-bit data bus with bidirectional shift capability. The 28 V high voltage output driving cells can be controlled by low voltage (3.0 Volts) logic input.

The MC141563 will provide the best performance in combination with the MC141562 (common driver).

- Operating Supply Voltage Range -
  Control Logic, Shift Register (VDD): 2.7V to 5.5V
  Segment Drivers (VLCD): 10 V to 28 V
- Operating Temperature Range: -20 to 70°C
- 80 LCD Segment Driving Outputs.
- Driving Duty Cycle (MUX) : 1/64 to 1/300.
- Bi-directional Shift Register Data Bus of 4-bit x 20 or 8-bit x 10 Configuration.
- Interchangeable Carry-In / Carry-Out Terminals.
- Left / Right Shift Mode Selection
- Cascadable.
- Maximum Data Clock Frequency = 8.0 MHz
- Available in SLIM TAB (Tape Automated Bonding), 103 pins

MC141563



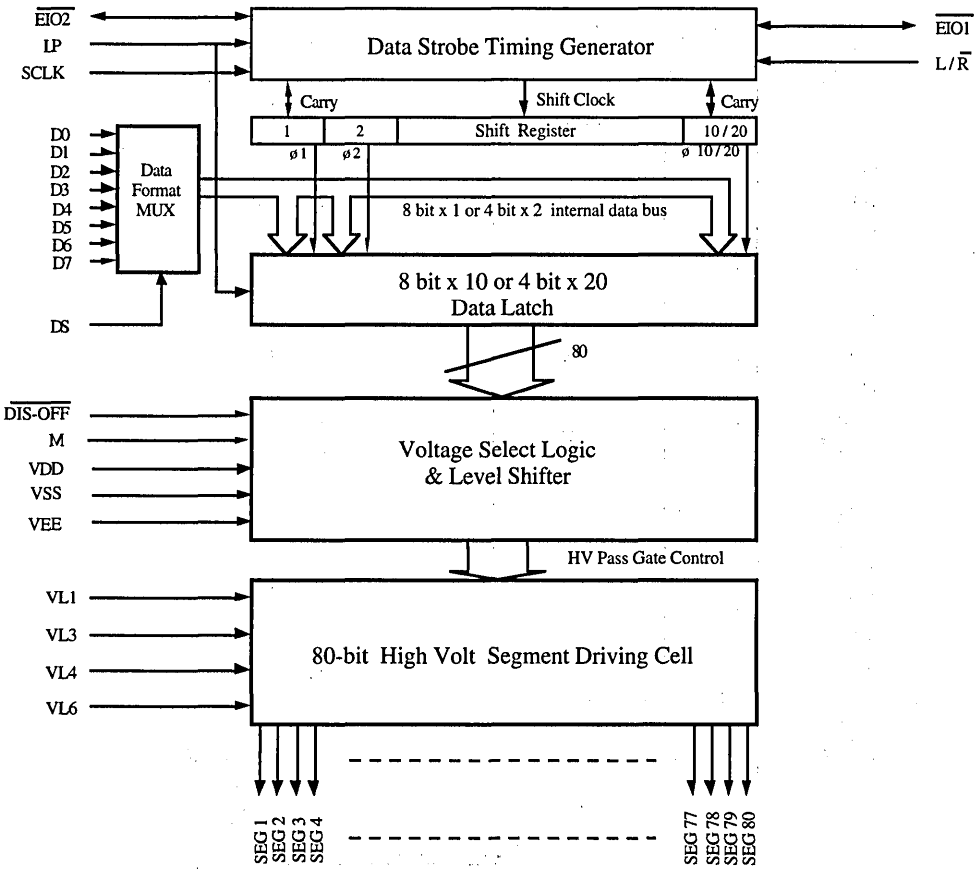
MC141563T
TAB

ORDERING INFORMATION

MC141563T TAB

REV 4
10/96

Figure 1. BLOCK DIAGRAM



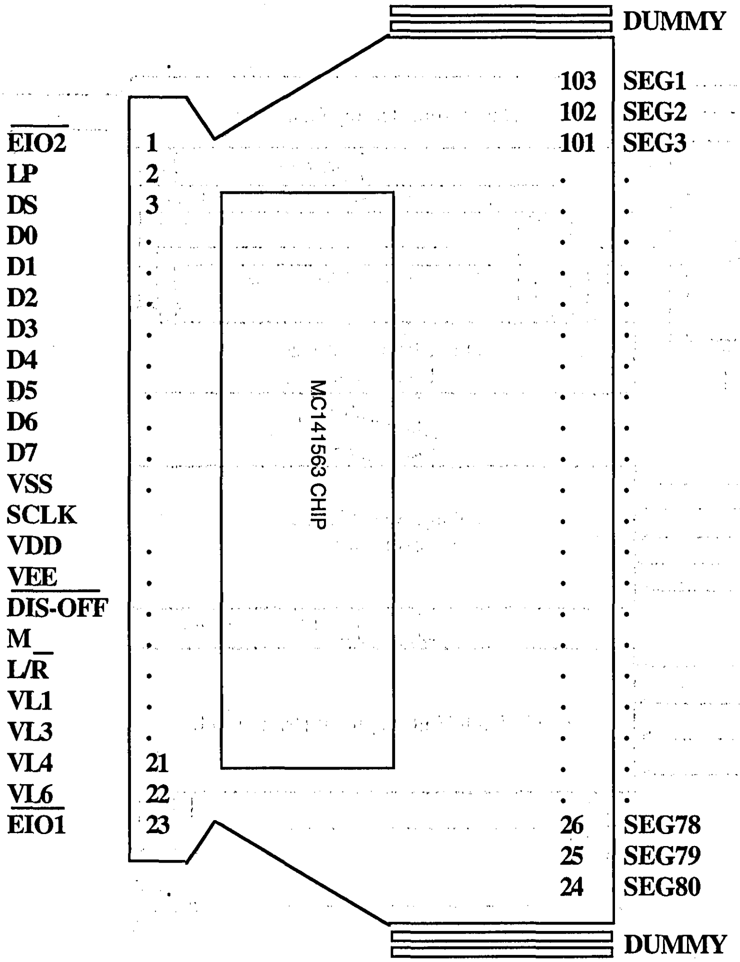


Figure 2. TAB Package Contact Assignment (Copper View)

MAXIMUM RATINGS*(Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +6.0	V
V_{EE}		-0.3 to -24.0	V
V_{LCD}	DC Supply Voltage (V_{DD} - V_{EE})	V_{DD} to +30	V
 V_{Din} V_{Ain}	Input Voltage All Digital Input V_{LCD} Level Input	 V_{SS}-0.3 to V_{DD}+0.3 V_{EE}-0.3 to V_{DD}+0.3	 V V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature Range	-20 to 70	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
 V_{DD} V_{LCD}	Operating Voltage Supply Voltage (reference to V_{SS}) LCD Supply Voltage (V_{DD} - V_{EE})		 2.7 10.0	 - -	 5.5 28.0	V V
 I_{DP} I_{SB}	Supply Current (V_{DD} Pin) Display Mode Standby Mode	V_{DD}=5.5V, V_{EE}=-23V SCLK = 6MHz, LP=15KHz, M=35Hz	 - -	 250 1.5	 600 5.5	 µA µA
 I_{DP} I_{SB}	Supply Current (V_{DD} Pin) Display Mode Standby Mode	V_{DD}=2.7V, V_{EE}=-23V SCLK = 6MHz, LP=15KHz, M=35Hz	 - -	 120 600	 - -	 µA nA
I_{EE}	Supply Current at V_{EE}	No Load	-	30	550	µA
 V_{OL} V_{OH}	Segment Output Voltage VL4,6=V_{EE} VL1,3=V_{DD} SEG1-SEG80	Iload = 100µA	 - V_{DD}-0.3	 - -	 V_{EE}+0.3 -	 V V
V_{OH} V_{OL}	Output High Voltage Output Low Voltage $\overline{EIO1}$, $\overline{EIO2}$	V_{DD}=5.0V, Iload=1mA	V_{DD}-1.0 -	- -	- V_{SS}+1.0	V V
V_{IH} V_{IL}	Input High Voltage Input Low Voltage SCLK, LP, L/$\overline{R}$, $\overline{EIO1}$, $\overline{EIO2}$, D0 to D3, M, $\overline{DIS\text{-}OFF}$		0.7xV_{DD} V_{SS}	- -	V_{DD} 0.2xV_{DD}	V V
I_{in}	Input Current SCLK, LP, L/$\overline{R}$, $\overline{EIO1}$, $\overline{EIO2}$, D0 to D3, M, $\overline{DIS\text{-}OFF}$		-	±0.5	±1.0	µA
C_{in}	Capacitance SCLK, LP, L/$\overline{R}$, $\overline{EIO1}$, $\overline{EIO2}$, D0 to D3, M, $\overline{DIS\text{-}OFF}$		-	5	10	pF
I_{OHX}, I_{OLX}	Segment Output Current SEG1-SEG80	V_{OH}= V_{DD} - 0.3V, V_{OL}=V_{EE} +0.3V	±100	-	-	µA
I_{OHC}, I_{OLC}	Carry Output Current $\overline{EIO1}$, $\overline{EIO2}$	V_{OH}= V_{DD} - 1.0V, V_{OL}=V_{SS} +1.0V	±1.0	-	-	mA
R_{ON}	Segment Output Impedance Segment Output Impedance Variance	V_{DD} - V_{EE} =28V, I_{OHX}, I_{OLX}=±100µA	- -	1.5 ±10	3.0 ±30	K Ohm %

AC ELECTRICAL CHARACTERISTICS -WRITE CYCLE (V_{DD} =5.0V, V_{SS} = 0V, V_{EE} = -23V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SUD}	Data (D0-D3) to Shift Clock (SCLK) Set up Time	50	-	-	ns
t_{hD}	Data (D0-D3) to Shift Clock (SCLK) Hold Time	50	-	-	ns
t_{SULP}	Data Latch (LP) to Shift Clock (SCLK) Set up Time	50	-	-	ns
t_{hLP}	Data Latch (LP) to Shift Clock (SCLK) Hold Time	50	-	-	ns
t_{SUS}	Enable Input ($\overline{EIO}$) to Shift Clock (SCLK) Set up Time	20	-	-	ns
t_{SUE}	Shift Clock (SCLK) to Enable Output ($\overline{EIO}$) Set up Time	20	-	-	ns
	Propagation Delay Time				
t_M	Data Latch (LP) to M	-	-	200	ns
t_{PO}	Data Latch (LP) to Segment Output (n) CL = 100pF	-	-	0.5	µs
t_{PM}	M to Segment Output (n) CL = 100pF	-	-	0.5	µs
t_{PLP}	Data Latch (LP) to $\overline{EIO}$ (Output) CL = 50pF	-	-	50	ns
t_{PE}	Shift Clock (SCLK) to $\overline{EIO}$ (Output) CL = 50pF	-	-	50	ns
t_{TLH}	Control Input Rise and Fall Time	-	10	20	ns
t_{THL}	SCLK, LP, M, $\overline{EIO1}$,$\overline{EIO2}$	-	10	20	ns
$t_{SCØ}$	Shift Clock (SCLK) Cycle V_{DD} = 3.0V	125	-	-	ns
t_{SCH}	Shift Clock (SCLK) Pulse Width HIGH	40	-	-	ns
t_{SCL}	Shift Clock (SCLK) Pulse Width LOW	40	-	-	ns
t_{LPH}	Data Latch (LP) Pulse Width HIGH	50	-	-	ns

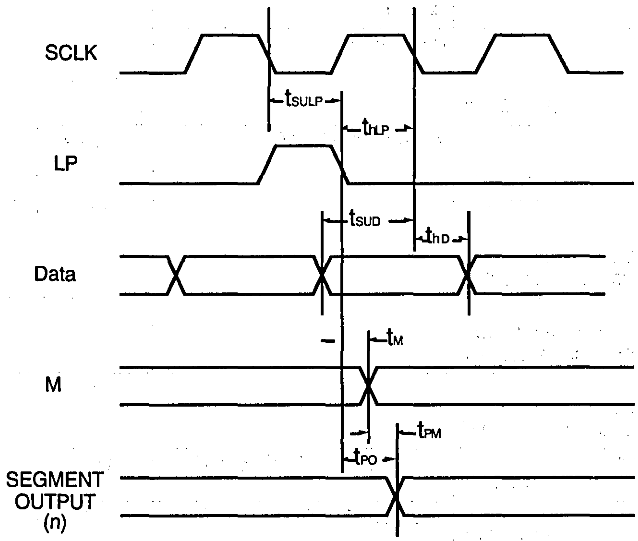


Figure 3. SCLK, LP, Data, M and Segment Output Propagation Delay Timing Diagram

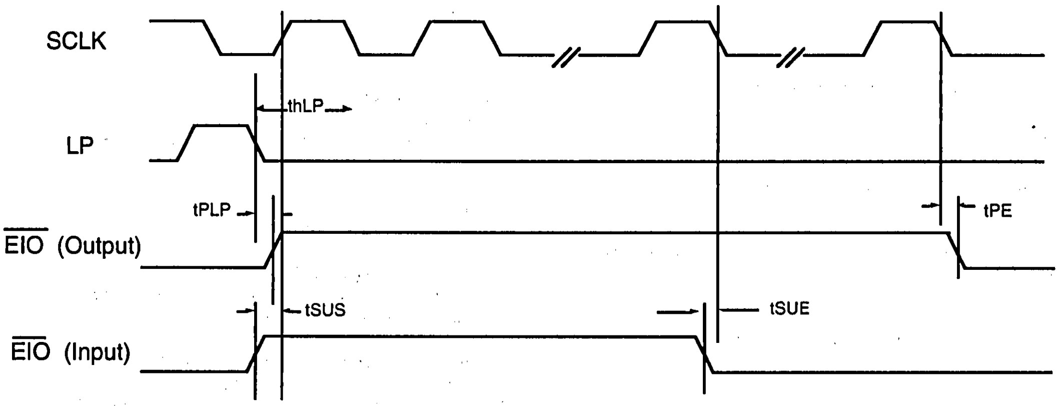


Figure 4. SCLK, LP, EIO (Input/Output) Propagation Delay Timing Diagram

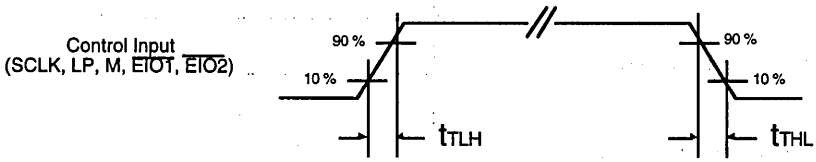


Figure 5. Control Pin Rise and Fall Timing Diagram

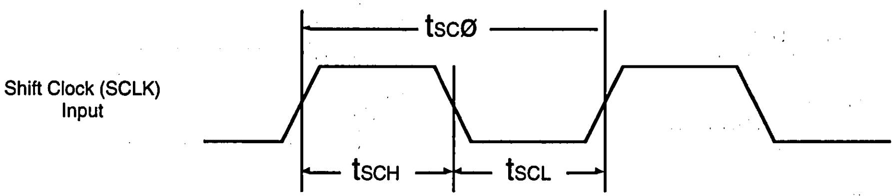


Figure 6. Shift Clock Pulse Width High and Pulse Width Low Timing Diagram

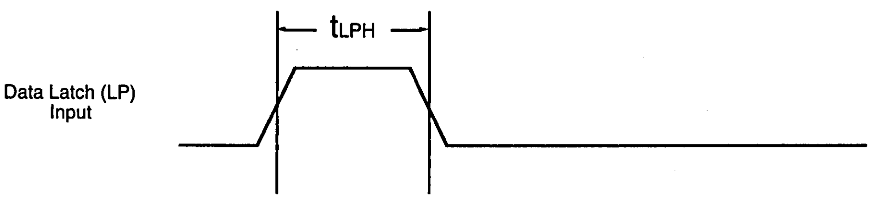


Figure 7. Data Latch Pulse Width High Timing Diagram

PIN DESCRIPTIONS

V_{DD} AND V_{SS}

The main dc power is supplied to the part by these two connections. V_{DD} is the most-positive supply level and V_{SS} is ground.

VEE

This supply connection provides the negative power supply voltage for the common drivers.

VL1, VL3, VL4, VL6

These input pins are connected to the external voltage divider (See Figure 8).
Voltage supply level for the LCD :
VL1, VL6 : On-level of the LC
VL3, VL4 : Off-level of the LC

Data Latch (LP)

Display data (a complete line on display) is acknowledged by the falling edge of the LP signal.

Data Shift Clock (SCLK)

Input data (8 bit or 4 bit) is stored into a 8 bit / 4 bit data latch by the falling edge of SCLK.

Data Input (D0 to D7)

Data Input is either in 8 bit or 4 bit data bus format and is selectable by the DS input.

Data Format Select (DS)

This input is to select the data bus format. If set "Low", the data bus format is 4-bit, if set "High", the data bus format is 8-bit.

Left / Right Shift Select (L / $\overline{R}$)

This input pin provides the selection of the shift register operation (See Table 1).

L / $\overline{R}$ = "1", the data will shift left (LSB of the first input data will be loaded to SEG1).

L / $\overline{R}$ = "0", the data will shift right (LSB of the first input data will be loaded to SEG80).

Carry-In / Carry-Out ($\overline{EIO1}$ / $\overline{EIO2}$)

These two input / output pins perform the same function and depend on the shift register direction of operation. In right shift mode (L / $\overline{R}$ = "0"), the $\overline{EIO1}$ is the Carry-In input while the $\overline{EIO2}$ will be the Carry-Out output for cascading. In Left Mode (L / $\overline{R}$ = "1"), the pin functions and operation are reversed. (See Table 2)

Frame Signal Input (M)

This input signal is the frame sync. signal which provides an frame alternating output format of the segment output (See Figure 9).

M	0	0	1	1
Data	1	0	0	1
Output	VL1	VL3	VL4	VL6

Display-Off Enable ($\overline{\text{DIS-OFF}}$)

This input pin is active low. If set "LOW", all output pins (Segment 1 to Segment 80) are forced to VL1.

Segment Output (Segment 1 to Segment 80)

These 80 output lines provide the high volt segment signal to the LCD panel. They are all at VL1 while display is turned off.

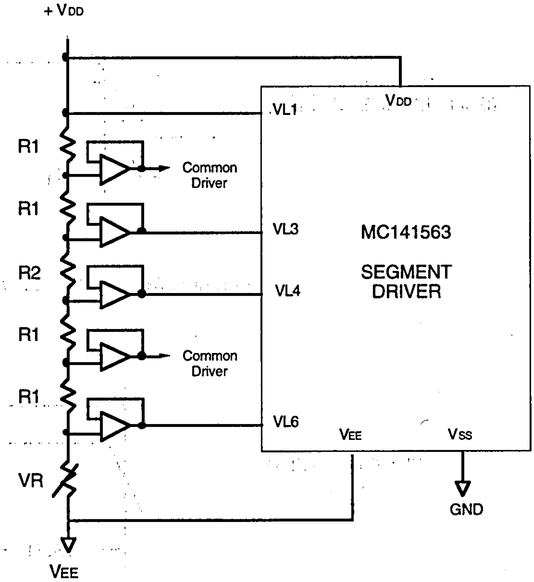


Figure 8. External Voltage Divider

L / $\overline{R}$	SCLK:	1	2	3	4	----	19	20
H	D0	01	05	09	13	----	73	77
	D1	02	06	10	14	----	74	78
	D2	03	07	11	15	----	75	79
	D3	04	08	12	16	----	76	80
L	D0	80	76	72	68	----	08	04
	D1	79	75	71	67	----	07	03
	D2	78	74	70	66	----	06	02
	D3	77	73	69	65	----	05	01

L / $\overline{R}$	SCLK	1	2	----	10
H	D0	01	09	----	73
	D1	02	10	----	74
	D2	03	11	----	75
	D3	04	12	----	76
	D4	05	13	----	77
	D5	06	14	----	78
	D6	07	15	----	79
	D7	08	16	----	80
L	D0	80	72	----	08
	D1	79	71	----	07
	D2	78	70	----	06
	D3	77	69	----	05
	D4	76	68	----	04
	D5	75	67	----	03
	D6	74	66	----	02
	D7	73	65	----	01

Table 1. Left / Right Shift Select and the Associated Data Bit Segment Output Mapping (a) 4 bit interface; (b) 8 bit interface

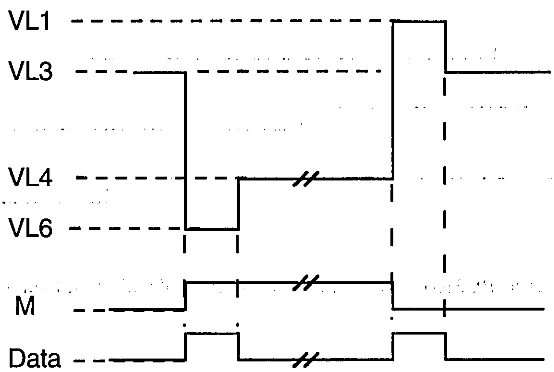


Figure 9. Data, M Inputs and Segment Output Format

L / $\overline{R}$	$\overline{EIO1}$	$\overline{EIO2}$
H	OUT	IN
L	IN	OUT

Table 2. Left / Right Shift Control and $\overline{EIO1}$, $\overline{EIO2}$ Relation

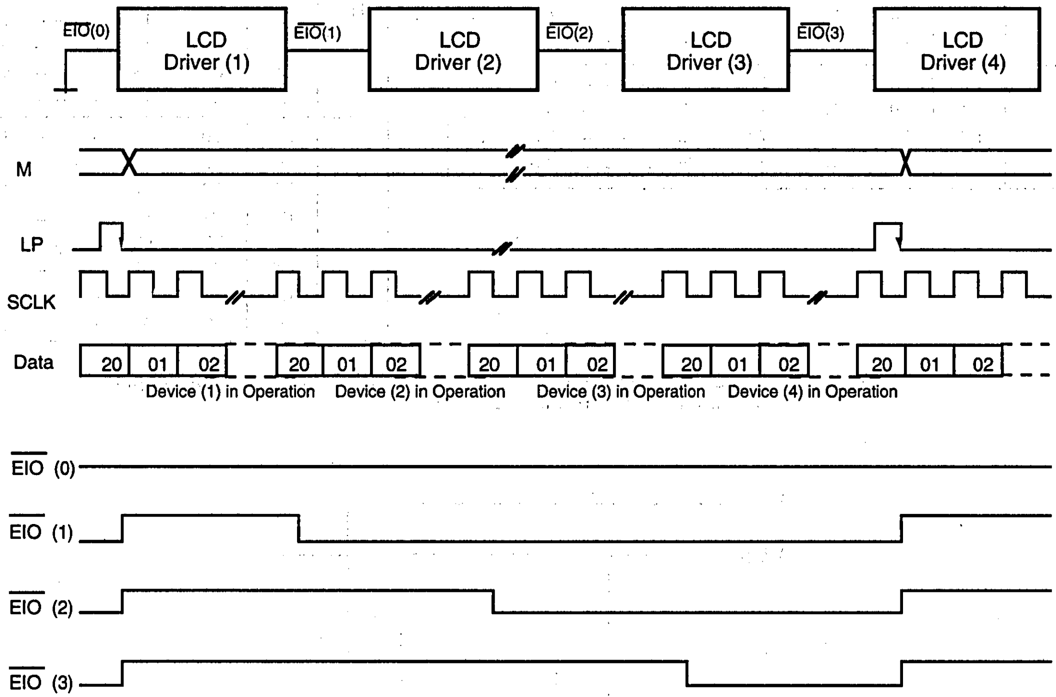


Figure 10. $\overline{\text{EIO1}}$ and $\overline{\text{EIO2}}$ in 4 Data Bit Application and Timing Diagram

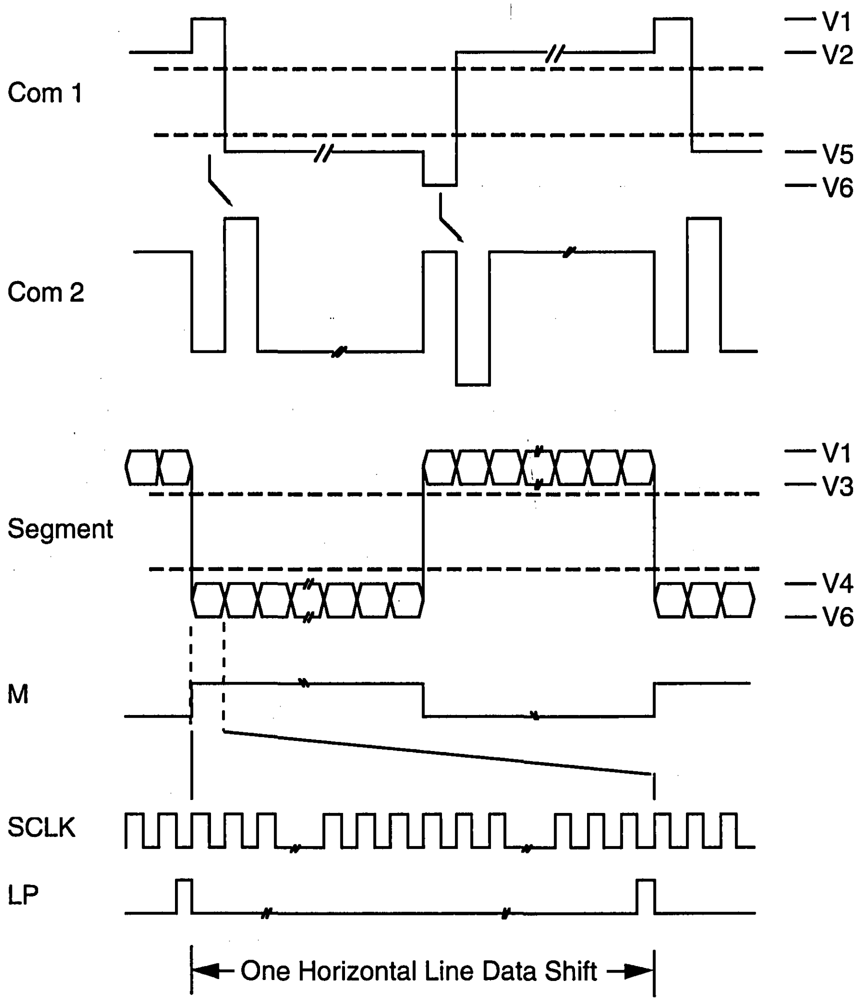
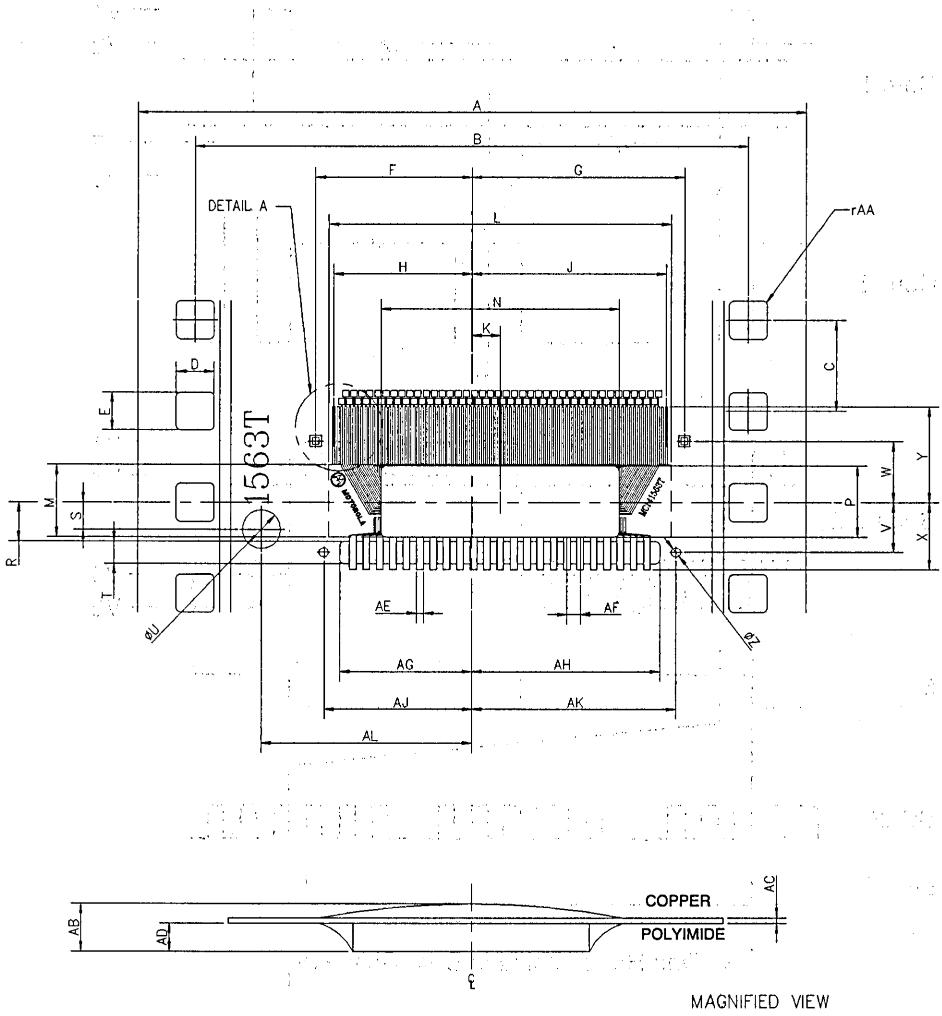


Figure 11. Common and Segment and Input Control Format Timing Diagram

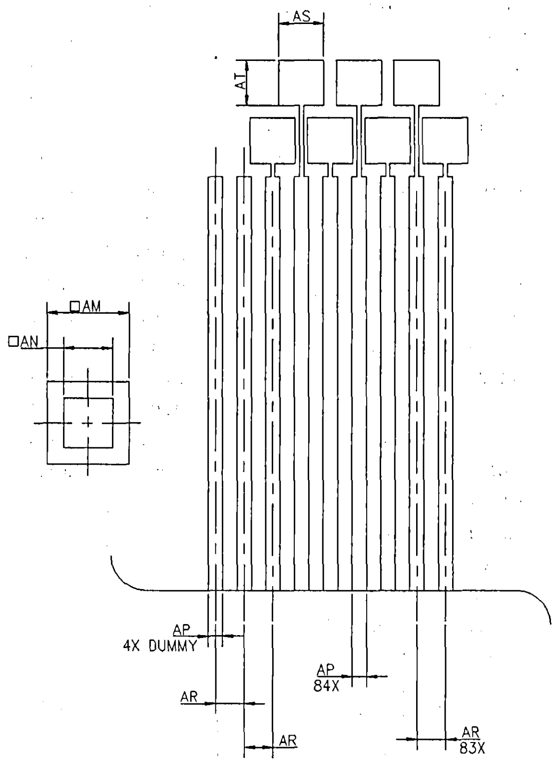
PACKAGE DIMENSIONS

MC141563T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



Reference : 98ASL00131A	Issue "0" released on 03/03/94

MC141563T
TAB PACKAGE DIMENSION
(DO NOT SCALE THIS DRAWING)



DETAIL "A"

Reference : 98ASL00131A	Issue "0" released on 03/03/94

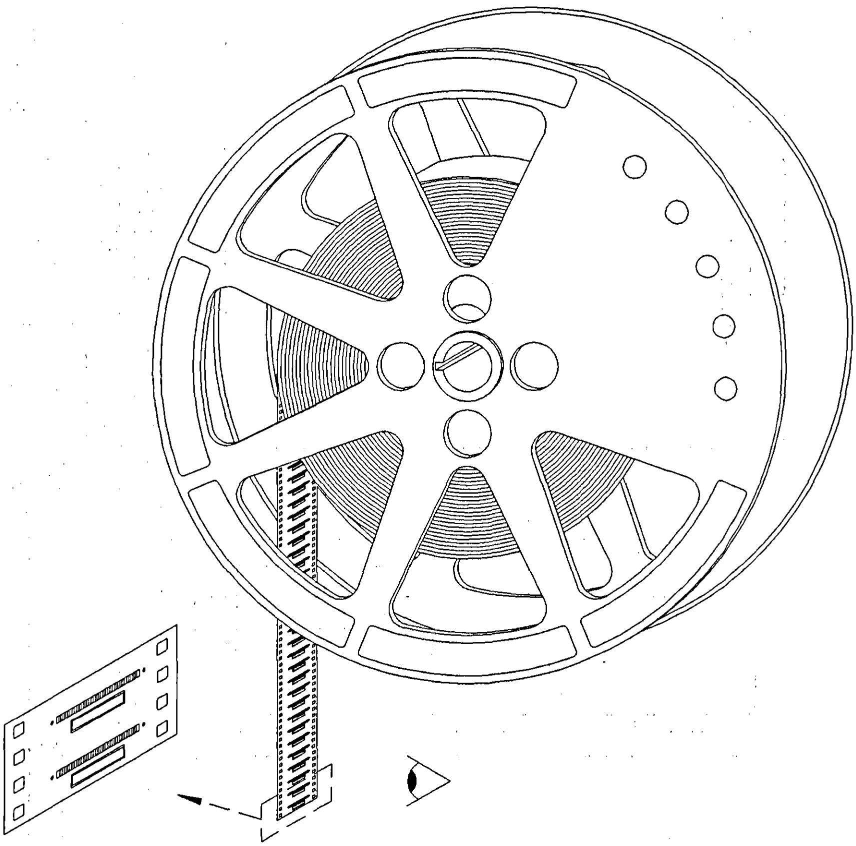
MC141563T TAB PACKAGE DIMENSION

	Millimeters		Inches			Millimeters		Inches	
Dim	Min	Max	Min	Max	Dim	Min	Max	Min	Max
A	34.775	35.175	1.3691	1.3848	AC	0.068	0.083	0.0027	0.0032
B	28.927	29.027	1.1389	1.1428	AD	0.579	0.629	0.0228	0.0248
C	4.720	4.780	0.1858	0.1882	AE	0.330	0.370	0.0130	0.0146
D	1.951	2.011	0.0768	0.0792	AF	0.690	0.710	0.0272	0.0280
E	1.951	2.011	0.0768	0.0792	AG	6.825	6.925	0.2687	0.2726
F	8.100	8.200	0.3189	0.3228	AH	9.825	9.925	0.3868	0.3907
G	11.100	11.200	0.4370	0.4409	AJ	7.675	7.775	0.3022	0.3061
H	7.201	7.229	0.2835	0.2846	AK	10.675	10.775	0.4203	0.4242
J	10.195	10.235	0.4014	0.4030	AL	10.500	11.500	0.4134	0.4528
K	1.000	2.000	0.0394	0.0787	AM	0.580	0.620	0.0228	0.0244
L	17.635	18.235	0.6943	0.7179	AN	0.340	0.380	0.0134	0.0150
M	3.490	4.090	0.1374	0.1610	AP	0.085	0.125	0.0033	0.0049
N	-	12.460	-	0.4906	AR	0.200	0.220	0.0079	0.0087
P	-	3.624	-	0.1427	AS	0.280	0.380	0.0110	0.0150
R	1.962	2.062	0.0772	0.0812	AT	0.280	0.380	0.0110	0.0150
S	0.900	1.900	0.0354	0.0748					
T	1.150	1.250	0.0453	0.0492					
U	1.950	2.050	0.0768	0.0807					
V	2.562	2.662	0.1009	0.1048					
W	3.146	3.246	0.1239	0.1278					
X	3.462	3.562	0.1363	0.1402					
Y	4.938	5.038	0.1944	0.1983					
Z	0.450	0.550	0.0177	0.0217					
AA	-	0.200	-	0.0079					
AB	0.686	0.838	0.0270	0.0330					

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Copper Thickness: 1/2 oz.
4. Tin plating thickness: 0.4µm
5. 2 sprocket hole device

Reference : 98ASL00131A	Issue "0" released on 03/03/94

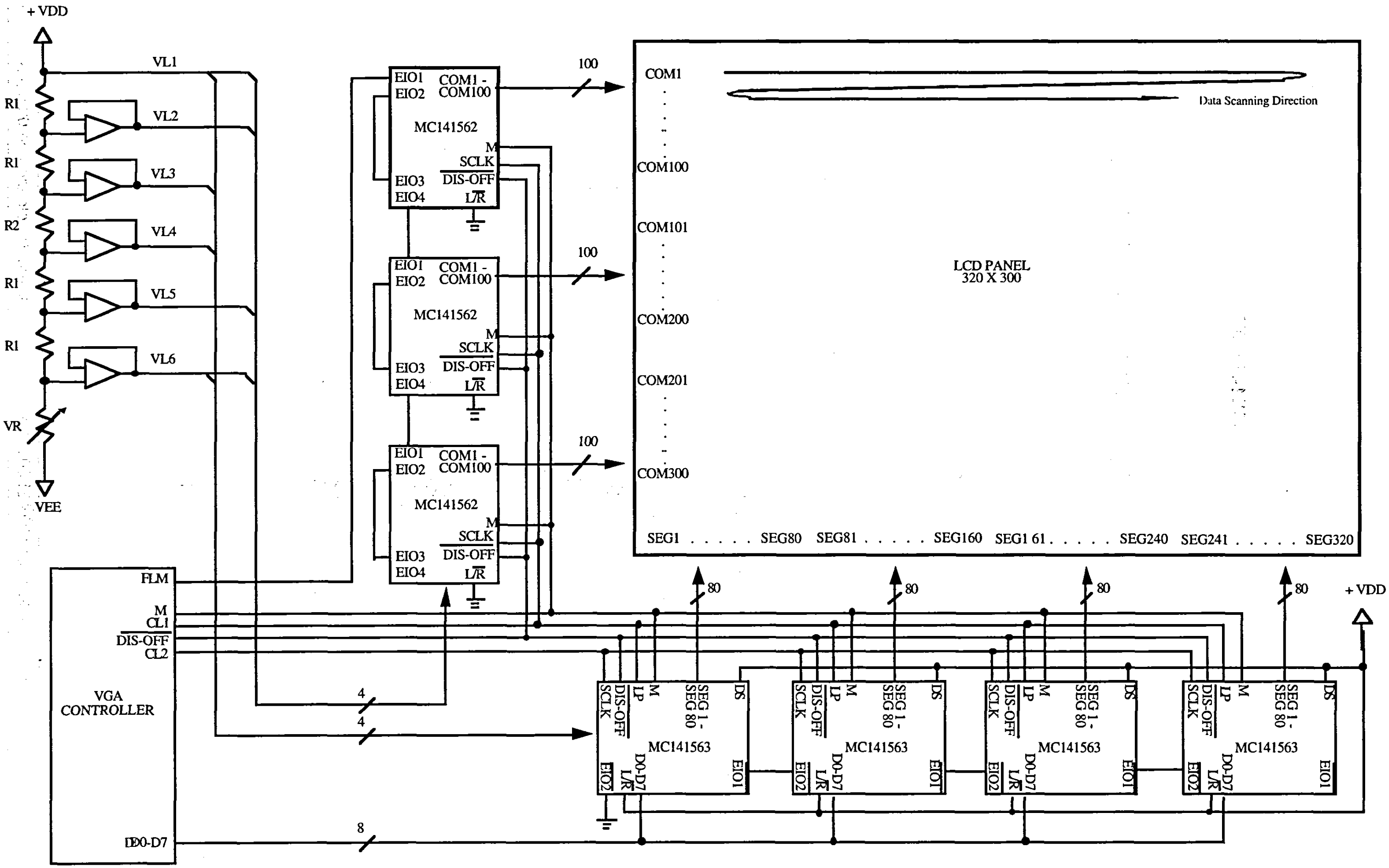
TAB TAPE REEL ORIENTATION



Reference : 98ASL00131A	Issue "0" released on 03/03/94

Application Example

320 x 300

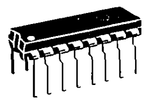


Monitor On-Screen Display Devices

4

MC141541

Enhanced Monitor On-Screen Display
CMOS



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION

MC141541P Plastic Dip

PIN ASSIGNMENT

$V_{SS(A)}$	1	16	V_{SS}
VCO	2	15	R
RP	3	14	G
$V_{DD(A)}$	4	13	B
HFLB	5	12	FBKG
SS	6	11	HTONE/ PWMCK
SDA(MOSI)	7	10	VFLB
SCL(SCK)	8	9	V_{DD}

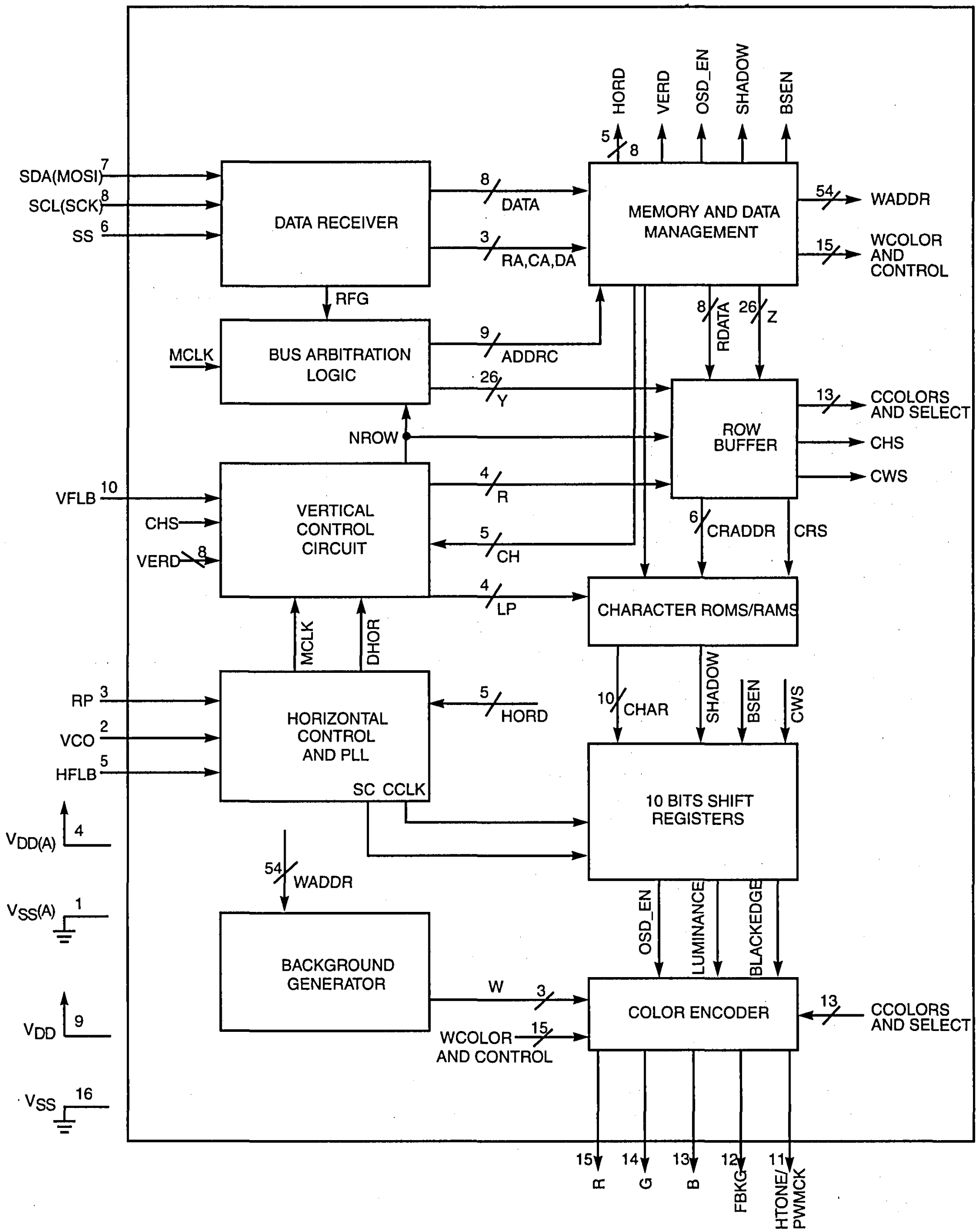
This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto the monitor screen. Its on-chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built-in 273 bytes display/control RAM. By storing a full screen of data and control informations, this device has a capability to carry out 'screen-refresh' without any MCU supervision. Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. Besides, there are two kinds of different character resolution that users can choose. By changing the number of dots per horizontal sync line to 320 or 480, the smaller characters with higher resolution can be easily achieved. Special functions such as character bordering or shadowing, multi-level windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, neither massive information update nor extremely high data transmission rate is expected for normal on screen display operation, serial protocols are implemented in lieu of any parallel formats to achieve the minimum pin count.

And one special feature, character RAM fonts, is implemented in this MOSD enhanced version (EMOSD). Users can download their own fonts pattern and display them at any time once the chip is powered on. Thus, there are two ways for users to build and store their fonts. One is a conventional approach to have their masked ROM fonts. Another new approach is to store the fonts in the EPROM accessed by MCU then download them into the EMOSD character RAM. Under this new technique, users have much flexibility to prepare their fonts and the effective fonts number is increased a lot.

- Two selectable Resolutions: 320 (CGA) and 480 (EGA) Dots per Line
- Fully Programmable Character Array of 10 Rows by 24 Columns
- 273 Bytes Direct Mapping Display RAM Architecture
- Internal PLL Generates a Wide-Ranged System Clock
- For High End Monitor Application, Maximum Horizontal Frequency is 110 KHz (52.8MHz Dot Clock at 480 mode)
- Programmable Vertical Height of Character to Meet Multi-Sync Requirement
- Programmable Vertical and Horizontal Positioning for Display Center
- 120 Characters and Graphic Symbols ROM and 8 programmable character RAM
- 10 x 16 Dot Matrix Character
- Character by Character Color Selection
- A Maximum of Four Selectable Colors per Row
- Double Character Height and Double Character Width
- Character Bordering or Shadowing
- Three Fully Programmable Background Windows with Overlapping Capability
- Provide a Clock Output Synchronous to the Incoming H Sync for External PWM
- M_BUS (IIC) Interface with Address $7A
- Single Positive 5 V Supply

REV 1
12/96

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and HTONE/PWMCK) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	—	—	110K	Hz

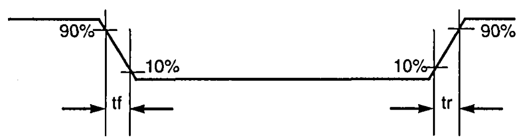


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{Il}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{Il}	Input Current (Not Including RP, VCO, R, G, B, FBKG and HTONE/PWMCK)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 15	mA

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

V_{DD} (Pin 9)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

HTONE/PWMCK (Pin 11)

This is a multiplexed pin. When the PWMCK_EN bit is cleared after power on or by the MCU, this pin is HTONE and outputs a logic high during windowing except when graphics or characters are being displayed. It is used to lower the external R, G, B amplifiers gain to achieve a transparent windowing effect. If the PWMCK_EN bit is set to 1 via M_BUS or SPI, this pin is changed to a mode-dependent clock output with 50/50 duty cycle and synchronous with the input horizontal synchronization signal at Pin 5. The frequency is dependent on the mode in which the EMOSD is currently running. The exact frequencies in the different resolution modes are described below.

Table 1. PWM CLK Frequency

Resolution	Frequency	Duty Cycle
320 dots/line	32 x H_f	50/50
480 dots/line	48 x H_f	50/50

NOTE: H_f is the frequency of the input H sync. on Pin 5.

Typically, this clock is fed into an external pulse width modulation module as its clock source. Because of the synchronization between PWM clock and H sync, a better performance on the PWM controlled functions can be achieved.

FBKG (Pin 12)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13,14,15)

EMOSD color output in TTL level to the host monitor. These three signals are active high output pins which are in high impedance state when EMOSD is disabled.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141541 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: SPI or M_BUS (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer SPI transmission. Parts which offer M_BUS transmission mode have to be specially manufactured as custom parts.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the EMOSD is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the EMOSD functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{\text{HFLB}}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100kbps.The default chip address is $7A, but is hardware changeable by mask set.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the EMOSD circuitry of MC141541, so that the received information can then be displayed.

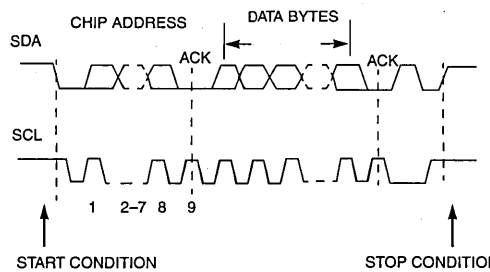


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{\text{SS}}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{\text{SS}}$ pin low by the master device to enable MC141541 to accept data. The $\overline{\text{SS}}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{\text{SS}}$ pin is then pulled high by master to terminate the transmission. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in

M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

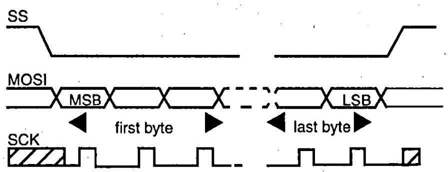


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

In this enhanced version MOSD, both display RAM/control registers and character RAM fonts needed to be programmed after power-on. The arrangement of display RAM/control registers is on the row-column basis, while the character RAM is on the segment-line basis. Although the address basis is different from each other, the data downloading protocols are very similar and will be described in the following sections.

Display RAM and Control Registers

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below. The data train in each sequence consists of row address (R), column address (C), and display information (I), as shown in Figure 4. In format (a), display information data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change which requires a massive information update, or during power up situation, most of the row and column addresses on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the RAM starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

The data transmission formats are:

(a) R – > C– > I –> R – > C – > I – > . . . .

(b) R – > C – > I – > C – > I – > C – > I. . . . . . .

(c) R – > C – > I – > I – > I – > . . . .

To differentiate the row and column addresses when transferring data from master, the MSB (Most Significant Bit) is set as in Figure 5: '1' to represent row, while '0' for column address. Furthermore, to distinguish the column address between format (a), (b) and (c), the sixth bit of the column address is set to '1' which represents format (c), and a '0' for format (a) or (b). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	X	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Row & Column Address Bit Patterns

Character RAM

The structure of 8 character RAM fonts are shown in Figure 6. They occupy the font number from 0 to 7. Because of the 10X16 dot matrix font, we decompose each font into 2 segments in horizontal direction and 16 lines in vertical direction. So, there are 5 dots needed to be defined for each specified segment-line location. This 5-bit data forms the lower 5 bits of the information data byte and the higher 3 bits are ignored. Because there are 16 segments (2 segments per font) and 16 lines, both the segment and line addresses are 4-bit wide.

Basically, the transmission format is very similar with that for display RAM or control registers. The major difference is to replace the row and column address with segment address and line address respectively. After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of segment address (S), line address (L), and font informations (I), as shown in Figure 6. In format (a), each font information data have to be preceded with the corresponding segment address and line address. This format is particular suitable for updating small portion of font pattern. However, if the current information byte has the same segment address as the one before, format (b) is recommended. For a new font pattern change which requires massive information update or during power up situation, most of the segment and column address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the character RAM starting segment and line addresses once only, and then treat all subsequent data as font information. The segment and line addresses will be automatically incremented internally for each RAM font data from the starting location.

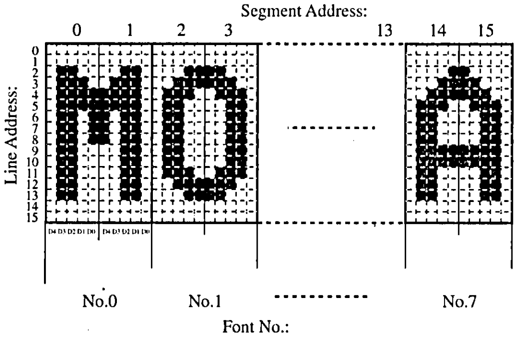
The data transmission formats are:

(a) S - > L - > I -> S - > L - > I - > . . . .

(b) S - > L - > I - > L - > I - > L - > I . . . .

(c) S - > L - > I - > I - > I - > . . . .

To differentiate the segment address from row and line address when transferring data, the bit 7 (MSB) and bit 6 are set to '11' to represent segment address, while '00' for line address used in format (a) or (b) and '01' for line address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).



Segment & Line Address bit Patterns:

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
SEG	1	1	X	X	D	D	D	D	a, b, c
LINE	0	0	X	X	D	D	D	D	a, b
LINE	0	1	X	X	D	D	D	D	c

X: don't care D: valid data

Data Packet:

SEG ADDRESS	LINE ADDRESS	INFORMATION

X	X	X	D4	D3	D2	D1	D0

NOTE: X means don't care bit and D means valid data bit.

Figure 6. Structure of Programmable RAM Fonts and Downloading Format

MEMORY MANAGEMENT

Inside this chip, there are three kinds of RAM, display RAM, control registers and character RAM. For display RAM and control registers, they are addressed with row and column (coln) number in sequence, while the character RAM with segment and line number. The transmission format has been described in the last section. Besides the 8 RAM fonts numbered from $00 to $07, 120 masked ROM fonts numbered from $08 to $7F are also built in this chip.

Display RAM and Control Registers

The space between row 0 and coln 0 to row 9 and coln 23 are called Display registers, with each contains a character RAM/ROM number corresponding to display location on monitor screen. Every data row associate with two control registers, which locate at coln 30 and 31 of their respective rows, to control the characters display format of that row. In addition, three window control registers for each of three windows together with three frame control registers occupy the first 13 columns of row 10 space.

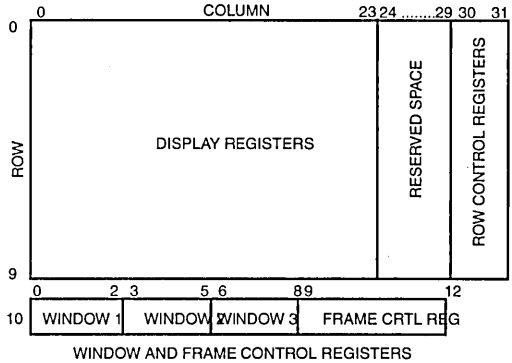


Figure 7. Memory Map

User should handle the internal RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed

Character RAM/ROM

The RAM fonts occupy the font number $00 to $07 and their patterns can be changed at any time via the SPI or MBUS protocol. The masked ROM fonts are fixed and located from number $08 to $7F. See the following Figure for the details.

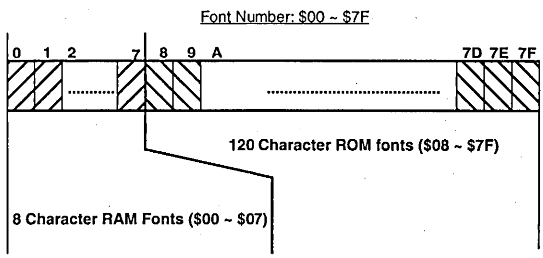


Figure 8. Arrangement of Character RAM/ROM fonts

REGISTERS

Display Register

	7	6	5	4	3	2	1	0
	CCS0							
		← CRADDR →						

Bit 7 CCS0 – This bit defines a specific character color out of the two preset colors. Color 1 is selected if this bit is cleared, and color 2 otherwise.

Bit 6–0 CRADDR – These seven bits address the 128 characters or symbols residing in the character ROM.

Row Control Registers

Coln 30

	7	6	5	4	3	2	1	0
COLN 30	R1	G1	B1	R2	G2	B2	CHS	CWS

Bit 7–2 Color 1 is determined by R1, G1, B1 and color 2 by R2, G2, B2.

Bit 1 CHS – It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS – Similar to bit 1, character is displayed in double width, if this bit is set.

Coln 31

	7	6	5	4	3	2	1	0
COLN 31	R3	G3	B3	R4	G4	B4		

Bit 7–2 Color 3 and 4 are defined by R3, G3, B3, and R4, G4, B4 respectively.

Window 1 Registers

Row 10 Coln 0

	7	6	5	4	3	2	1	0
ROW 10 COLN 0	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 10 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR (MSB … LSB)					WEN	CCS1	HPOL

Bit 2 WEN – It enables the background window 1 generation if this bit is set.

Bit 1 CCS1 – This additional color select bit provides the characters residing within window 1 with two extra color selections, making a total of four selections for that row.

Bit 0 HPOL – This bit selects the polarity of the incoming horizontal sync signal ($\overline{\text{HFLB}}$) on pin 5. If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Row 10 Coln 2

	7	6	5	4	3	2	1	0
ROW 10 COLN 2	COL END ADDR (MSB … LSB)					R	G	B

Bit 2–0 R, G and B – Controls the color of window 1. Window 1 occupies Column 0–2 of Row 10. Window 2 from Column 3–5, and Window 3 from 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 10 Coln 3

	7	6	5	4	3	2	1	0
ROW 10 COLN 3	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 10 Coln 4

	7	6	5	4	3	2	1	0
ROW 10 COLN 4	COL START ADDR (MSB … LSB)					WEN	CCS1	VPOL

Bit 2 WEN – It enables the background window 2 generations if this bit is set.

Bit 1 CCS1 – This additional color select bit provides the characters residing within window 2 with two extra color selections, making a total of four selections for that row.

Bit 0 VPOL – This bit selects the polarity of the incoming vertical sync signal ($\overline{\text{VFLB}}$) on pin 5. If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

Row 10 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR (MSB … LSB)					R	G	B

Bit 2–0 R, G and B – Controls the color of window 2. Window 1 occupies Column 0–2 of Row 10. Window 2 from Column 3–5, and Window 3 from 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 10 Coln 6

	7	6	5	4	3	2	1	0
ROW 10 COLN 6	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 10 Coln 7

	7	6	5	4	3	2	1	0
ROW 10 COLN 7	MSB	COL START ADDR			LSB	WEN	CCS1	PWMCK_EN

Bit 2 WEN – It enables the background window 3 generations if this bit is set.

Bit 1 CCS1 – This additional color select bit provides the characters residing within window 3 with two extra color selections, making a total of four selections for that row.

Bit 0 PWMCK_EN – When this bit is set to 1, HTONE/PWMCK pin will be switched to a clock output which is synchronous to the H sync and used as an external PWM (pulse width modulation) clock source. Refer to the pin description of HTONE/PWMCK for more information. After power on, the default value is 0.

Row 10 Coln 8

	7	6	5	4	3	2	1	0
ROW 10 COLN 8	MSB	COL END ADDR			LSB	R	G	B

Bit 2–0 R, G and B – Controls the color of window 3. Window 1 occupies Column 0–2 of Row 10. Window 2 from Column 3–5, and Window 3 from 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Frame Control Registers

Frame Control Register Row 10 Coln 9

	7	6	5	4	3	2	1	0
COLN 9	MSB	VERTD						LSB

Bit 7–0 VERTD – These eight bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value cannot be zero anytime. The default value is 4.

Frame Control Register Row 10 Coln 10

	7	6	5	4	3	2	1	0
COLN 10	TB	MSB	HORD					LSB

Bit 7 TB – Reserved Test Bit.

Bit 6–0 HORD – Horizontal starting position for character display. Seven bits give a total of 96 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value is 10.

Frame Control Register Coln 11

	7	6	5	4	3	2	1	0
COLN 11	TB	TB	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 TB – Reserved Test Bit.

Bit 6 TB – Reserved Test Bit.

Bit 5–0 CH5–CH0 – These six bits will determine the displayed character height. It is possible to have a proper character height by setting a value greater than or equal to 16 on different horizontal frequency monitor. Setting a value below 16 will not have a predictable result. Figure 9 illustrates how this chip expands the built-in character font to the desired height.

Frame Control Register Coln 12

	7	6	5	4	3	2	1	0
COLN 12	OSD_EN	BSEN	SHADOW	TB	X32B	TB		FBKGC

Bit 7 OSD_EN – OSD circuit is activated when this bit is set.

Bit 6 BSEN – It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW – Character with black-edge shadowing is selected if this bit is set; otherwise bordering prevails.

Bit 4, TB – Reserved Test Bit.

Bit 3, X32B – It determines the number of dots per horizontal line. There are 320 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 480 dots per horizontal sync line is chosen when bit X32B is set to 1. Refer to Table 2 for details.

Bit 2 TB – Reserved Test Bit.

Bit 1 TB – Reserved Test Bit.

Bit 0 FBKGC – It determines the configuration of FBKG output pin. When it is clear, the FBKG pin outputs high while displaying characters or windows; otherwise, the FBKG pin outputs high only while displaying characters.

Table 2. Resolution Setting

Register Setting (32B)	0	1
Dots number per H Sync Line	320	480

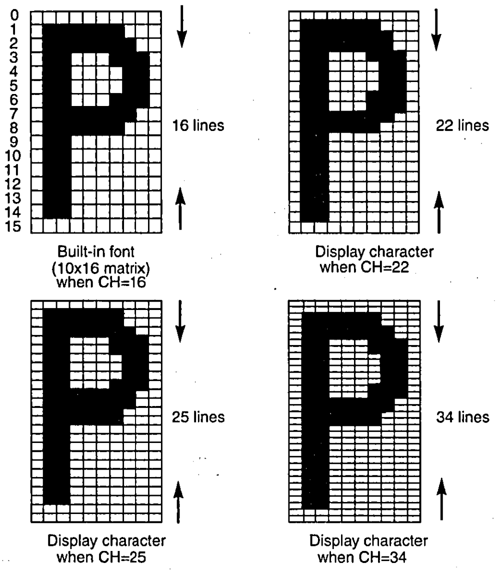


Figure 9. Variable Character Height

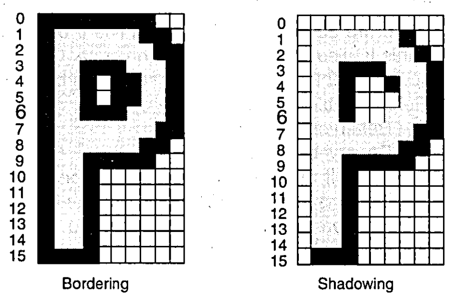


Figure 10. Character Bordering and Shadowing

Frame Format and Timing

Figure 12 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 12 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{HFLB}$ and $\overline{VFLB}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge-up resistor, which is the 330 kΩ resistor in a series with 2 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 320 if the bit X32B is clear and H Freq. x 480 if bit X32B is set to 1 and bit X64 is 0 and H Freq. x 640 if both bit X32B and bit X64 are set to 1. For example, dot frequency is 10.24 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1 and bit X64 is 0, the dot frequency will be 15.36 MHz (one and a half of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{VFLB}$ of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 240, regardless of row character width and the setting of bit X32B.

Although there are 24 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 320 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 480 dots, 24 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 11 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Notice that signal HTONE/PWMCK is active only during window area. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing; it has no effect on the timing of HTONE/PWMCK. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only. Also notice that HTONE/PWMCK has exactly the same waveform as 'window R, G or B'.

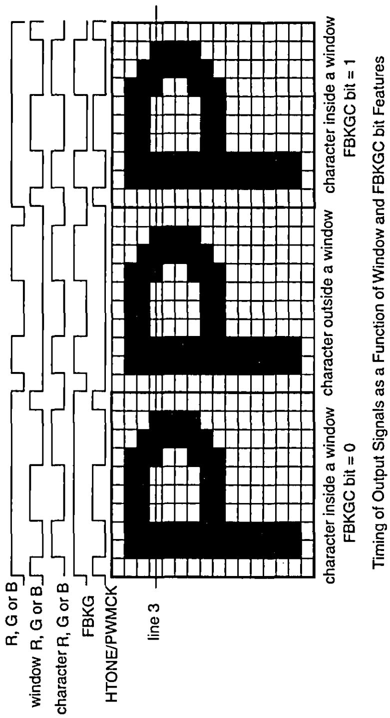


Figure 11. Timing of Output Signals

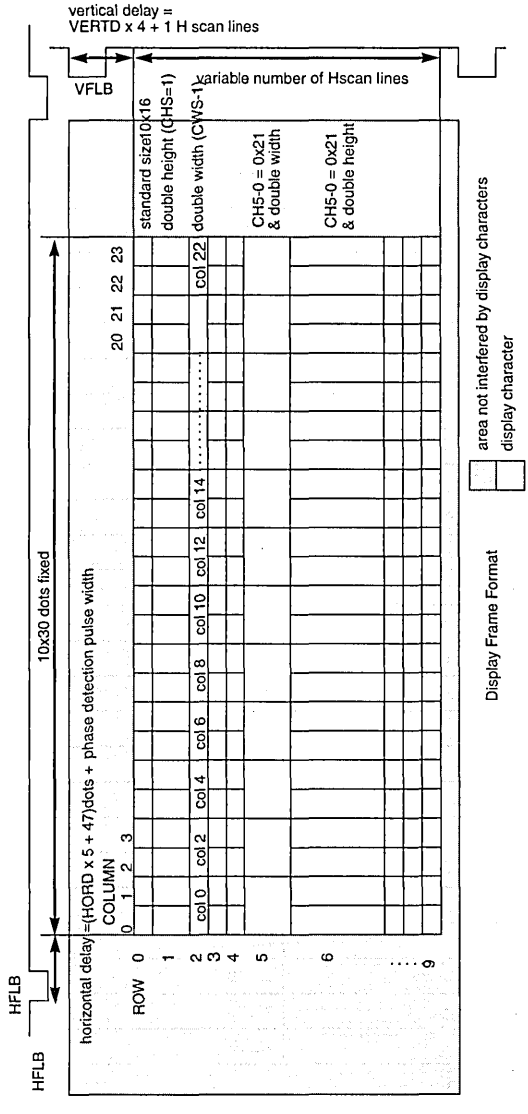


Figure 12. Display Frame Format

FONT

Icon Combination

MC141541 contains 120 character ROM and 8 RAM. The user can create an on-screen menu based on those characters and programmable RAM. Refer to Table 3 for icon combinations.

Table 3. Combination Map

ICON	ROM ADDRESS(HEX)
Volume Bar I	48, 49, 57
Volume Bar II	47
Size	4F, 50
Position	51, 52
Geometry	53, 54, 55, 56
Contrast	58,59
Brightness	5A, 5B
Horizontal Position	5C, 5D
Horizontal Sizing	5E, 5F
Vertical Position	60, 61
Vertical Sizing	62, 63
Pin Cushion	64, 65
Degaussing	66, 67
Trapezoid	6C, 6D, 6E, 6F
Parallelogram	68, 69, 6A, 6B
Color Select	70, 71
Video Level	72, 73
Input Select	74, 75
Recall	76,77
Save	78, 79
Left/Right Arrows	7A, 7B
INC/DEC sign	7C, 7D
Speaker	7E, 7F

ROM CONTENT

Figures 13 – 14 show the ROM content of MC141541.

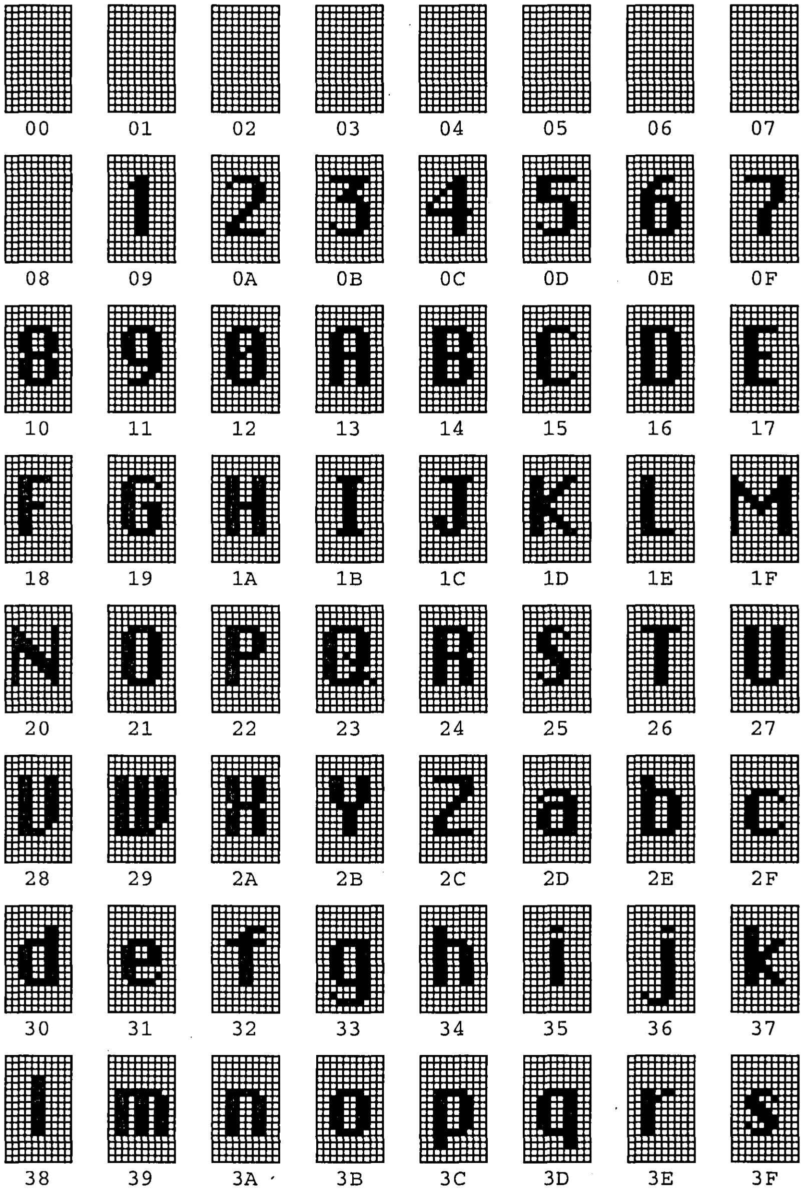


Figure 13. ROM Address ($08 - $3F)

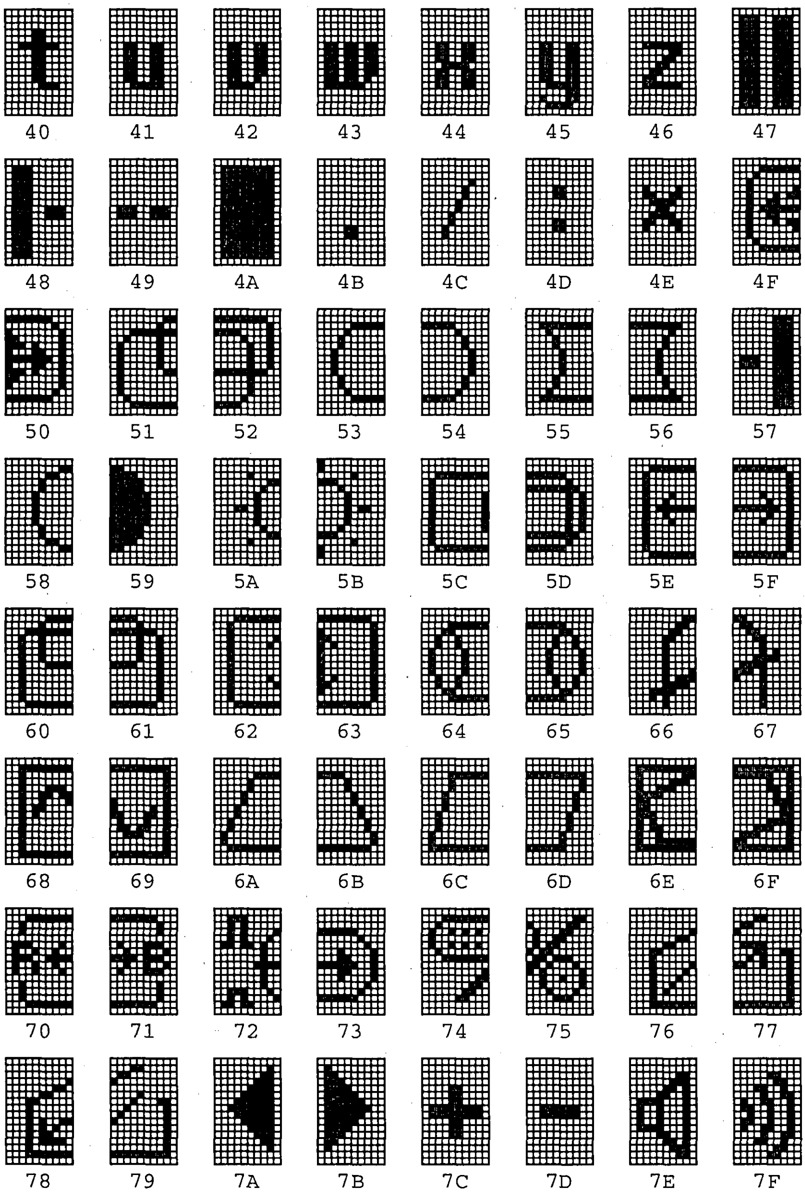


Figure 14. ROM Address ($40 - $7F)

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141541P has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 320/480/640 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating). Refer to the Application Diagram for the ground connections.
- DC supply path for Pin 9 (V_{DD}) should be separated from other switching devices.
- LC filter should be connected between Pin 9 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.

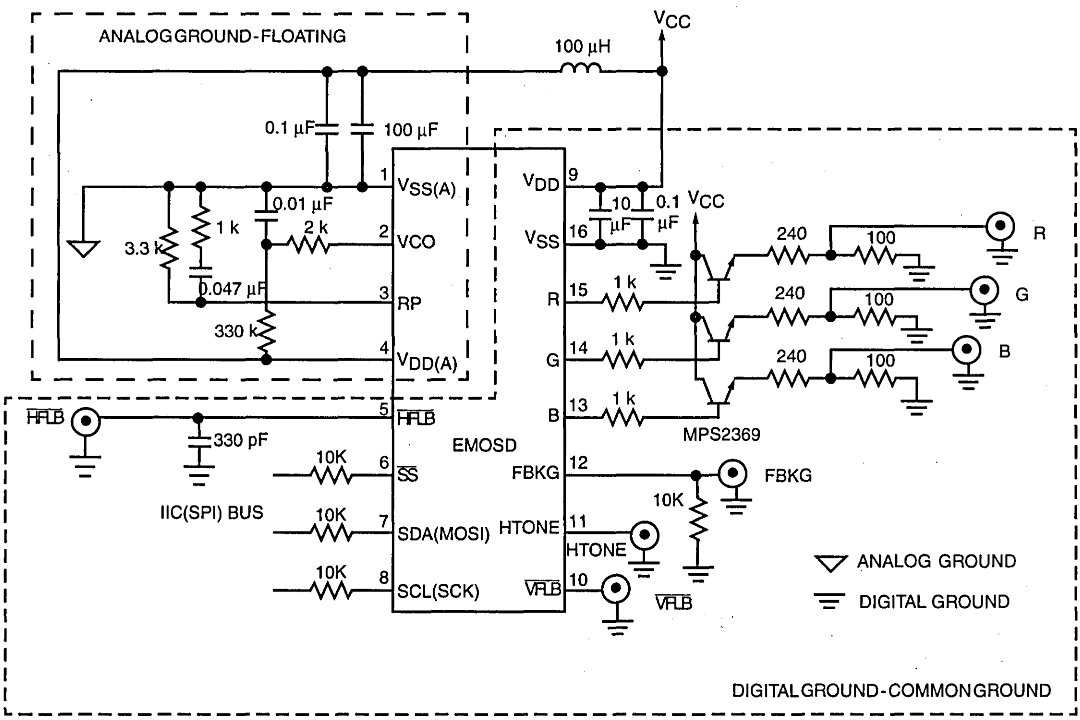
Jittering

Most display jittering is caused by HFLB jittering in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. A small capacitor can be added between Pin 5 – Pin 16 to smooth the signal. Refer to the value used in the Application Diagram.

Display Dancing

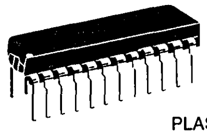
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



Super Monitor On-Screen Display - 24
CMOS

MC141548P

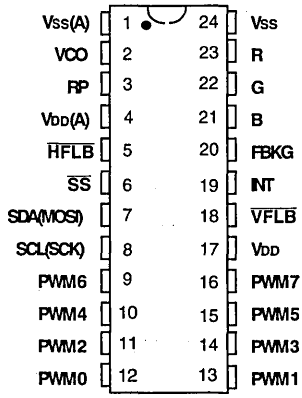


P SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

MC141548P Plastic Dip

PIN ASSIGNMENT



This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto color monitor. Because of the large number of fonts, 256 fonts including the programmable RAM fonts and fixed ROM fonts, SMOSD is suitable to be adopted for the multi-language monitor application especially. Its on-chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. Besides, there are three kinds of different resolutions that users can choose. By changing the number of dots per horizontal line to 320 (CGA), 480 (EGA) or 640 (VGA), smaller characters with higher resolution can be easily achieved.

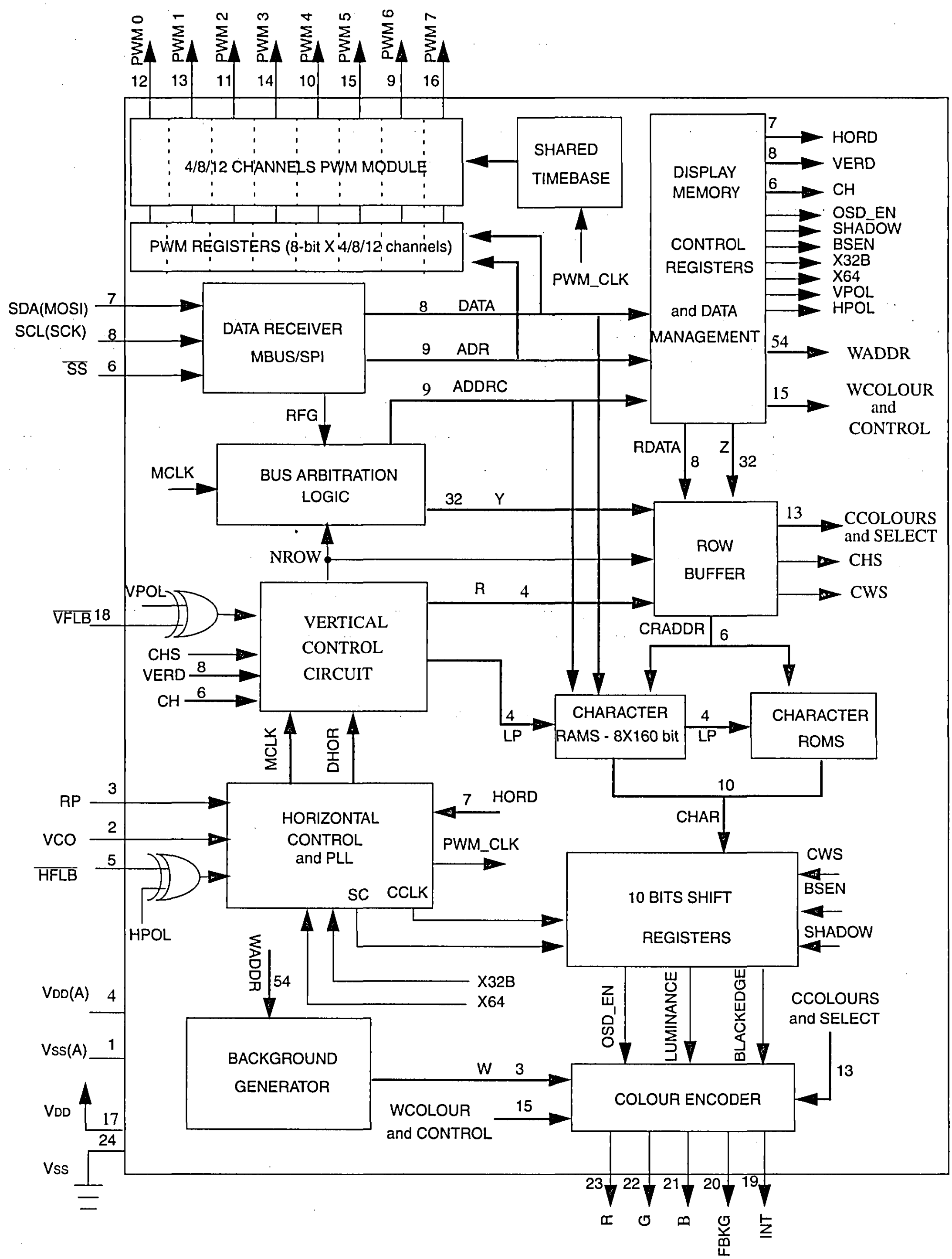
Special functions such as character blinking, automatic height scaling, character/window bordering or character shadowing, four-level windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, 8 programmable character/symbol RAM fonts are also built-in. It is much flexible to create the new symbols, icons and logo. One special attractive application of the RAM fonts is the real-time programming to achieve the dynamic image instead of the static picture as previous.

There are 8 PWM DAC channels for external digital to analog control. Each PWM channel is composed of an 8-bit register which contains a 5-bit PWM in MSB portion and a 3-bit binary rate multiplier(BRM) in LSB portion.

- 8 Channels DAC Synchronous PWMs with 8 bit Resolution
- Totally 256 Characters and Graphic Fonts Including 8 Programmable RAM Fonts and 248 Mask ROM Fonts
- Three Selectable Resolutions: 320 (CGA), 480 (EGA) or 640 (VGA) Dots/Line
- Wide Operating Frequency Range for High End Monitor: 15KHz ~ 120KHz
- Fully Programmable Character Array of 15 Rows by 30 Columns
- True 16-Color Selection for Windows
- Fancy Fade-In/Fade-Out Effects
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- Auto Height Scaling to Keep Constant Height Independent of Display Modes
- Four Programmable Background Windows with Overlapping Capability
- Shadowing on Windows with Programmable Shadow Width/Height
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
- Programmable Vertical Height of Character to Meet Multi-Sync Requirement
- Programmable Vertical and Horizontal Positioning for Display Centre
- Double Character Height and Double Character Width
- Internal PLL Generates a Wide-Ranged System Clock (76.8 MHz)
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

REV 1
12/96

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. *Functional operation should be restricted to the limits in the Electrical Characteristics* tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	—	—	120K	Hz

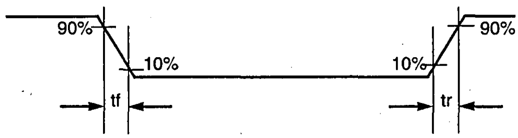


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{II}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{II}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 15	mA

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

PWM 6 (Pin 9)

Channel 6 of the PWM.

PWM 4 (Pin 10)

Channel 4 of the PWM.

PWM 2 (Pin 11)

Channel 2 of the PWM.

PWM 0 (Pin 12)

Channel 0 of the PWM.

PWM 1 (Pin 13)

Channel 1 of the PWM.

PWM 3 (Pin 14)

Channel 3 of the PWM.

PWM 5 (Pin 15)

Channel 5 of the PWM.

PWM 7 (Pin 16)

Channel 7 of the PWM.

V_{DD} (Pin 17)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 18)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT (Pin 19)

This output pin is used to indicate the color intensity. If the intensity control bits are set in the row attribute registers or window control registers, this pin will output a logic high while displaying the specified windows or the characters on the associated rows. Otherwise, it will keep in low state. Please refer to Figure 17 for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

FBKG (Pin 20)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 21, 22, 23)

SMOSD color outputs in TTL level to the host monitor. These three signals are open drain outputs if 3_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 24)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141548 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the SMOSD is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the SMOSD functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{\text{HFLB}}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps.The default chip address is $7A.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the SMOSD circuitry of MC141548, so that the received information can then be displayed.

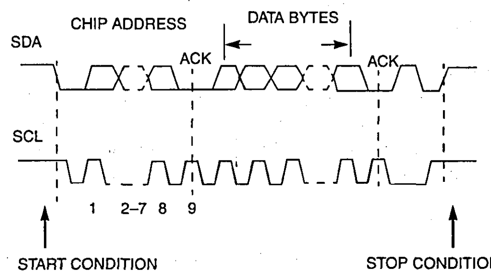


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{\text{SS}}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{\text{SS}}$ pin low by the master device to enable MC141548 to accept data. The $\overline{\text{SS}}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{SS}$ pin is then pulled high by master to terminate the transmission. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

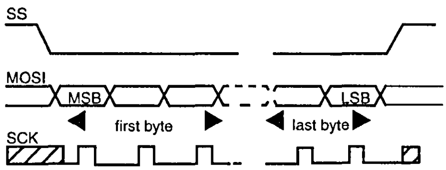


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, three register blocks, display registers, attribute/control registers and RAM fonts, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:

(a) R - > C- > I -> R - > C - > I - > . . . .

(b) R - > C - > I - > C - > I - > C - > I. . . . . . .

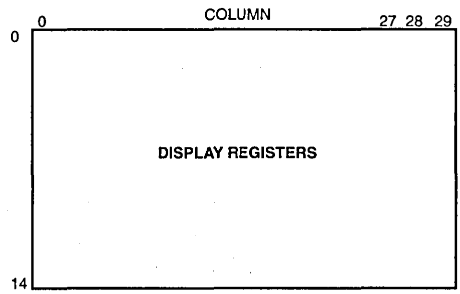
(c) R - > C - > I - > I - > I - > . . . .

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the display row address from attribute/RAM fonts area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet for Display Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:

(a) R - > C- > I -> R - > C - > I - > . . . .

(b) R - > C - > I - > C - > I - > C - > I. . . . . . .

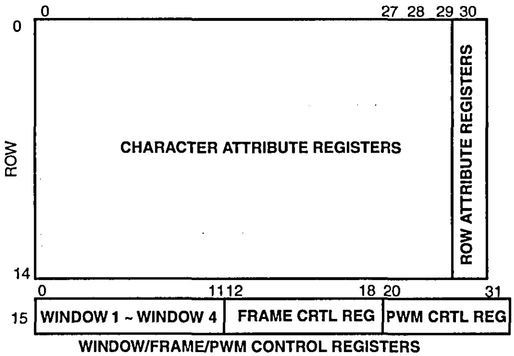
(c) R - > C - > I - > I - > I - > . . . .

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 6. Data Packet for Attribute/Control Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	1	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 7. Address Bit Patterns for Attribute/Control Data

(III) RAM Fonts Programming

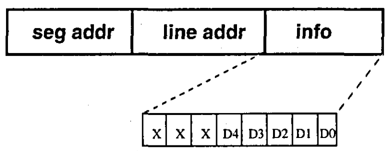
Basically, the transmission format is very similar with that for display RAM or control registers. The major difference is to replace the row and column address with segment address and line address respectively. There are also three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of segment address (S), line address (L), and font informations (I), as shown in Figure 3. In format (a), each font information data have to be preceded with the corresponding segment address and line address. This format is particular suitable for updating small portion of font pattern. However, if the current information byte has the same segment address as the one before, format (b) is recommended. For a new font pattern change which requires massive information update or during power up situation, most of the segment and column address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the character RAM starting segment and line addresses once only, and then treat all subsequent data as font information. The segment and line addresses will be automatically incremented internally for each RAM font data from the starting location.

The transmission formats are shown below:

(a) S - > L - > I -> S - > L - > I - > ....
(b) S - > L - > I - > L - > I - > L - > I.......
(c) S - > L - > I - > I - > I - > ....

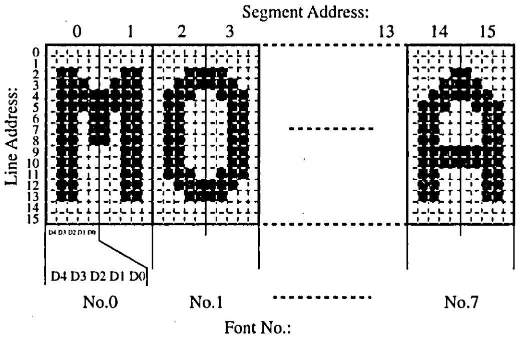
NOTE: S means segment byte.
L means line byte.
I means data byte.

To differentiate the segment address from row and line address when transferring data, the bit 7 (MSB) and bit 6 are set to '11' to represent segment address, while '00' for line address used in format (a) or (b) and '01' for line address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).



NOTE: X means don't care bit and D means valid data bit.

Figure 8. Data Packet for RAM Fonts



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
SEG	1	1	X	X	D	D	D	D	a, b, c
LINE	0	0	X	X	D	D	D	D	a, b
LINE	0	1	X	X	D	D	D	D	c

X: don't care D: valid data

Figure 9. Address Bit Patterns for RAM Fonts

MEMORY MANAGEMENT

All the internal programmable area can be divided into three parts including (1) Display Registers (2) Attribute/Control Registers and (3) Programmable RAM Fonts. Please refer to the following three figures for the corresponding memory map.

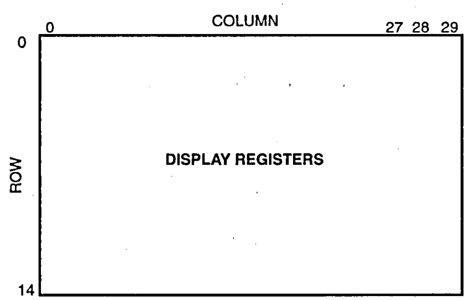


Figure 10. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 RAM/ROM fonts.

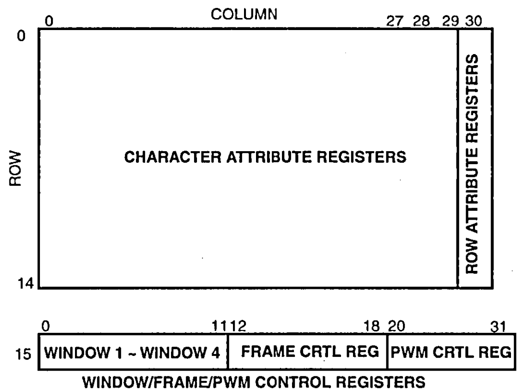


Figure 11. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. Every data row associate with one attribute register, which locate at coln 30 of their respective rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control, frame function control and PWM registers. Three window control registers for each of four windows together with four frame control registers and twelve PWM registers occupy the first 28 columns of row 15 space. These control registers will be described on the "REGISTERS" section.

User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

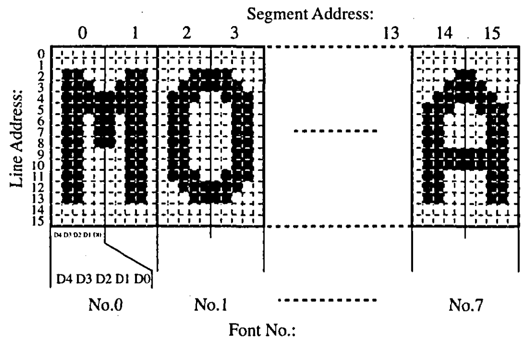


Figure 12. Memory Map of Programmable RAM Fonts

Another programming area is the RAM fonts. Totally, 8 fonts are programmable in SMOSD. The structure of 8 character RAM fonts are shown in Figure 12. They occupy the font number from 0 to 7 while ROM fonts 8 to 255. Because of the 10X16 dot matrix font, we decompose each font into 2 segments in horizontal direction and 16 lines in vertical direction. So, there are 5 dots needed to be defined for each specified segment-line location. This 5-bit data forms the lower 5 bits of the information data byte and the higher 3 bits are ignored. Because there are 16 segments (2 segments per font) and 16 lines, both the segment and line addresses are 4-bit wide.

REGISTERS

(I) Display Register

Display Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
CRADDR							

Bit 7-0 CRADDR - This eight bits address one of the 256 characters or symbols resided in the character RAM/ROM fonts.

(II) Attribute/Window/Control/Frame Registers

Character Attribute Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
				BLINK	R	G	B

Bit 3 BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

Bit 2-0 These three bits are the color attribute to define the color of the associated character/symbol.

Row Attribute Register (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
					R_INT	CHS	CWS

Bit 2 R_INT - Row intensity bit controls the color intensity of the displayed character/symbol on the corresponding row. Setting this bit to 1 means high intensity color and the INT pin will go high while displaying the characters of this row.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

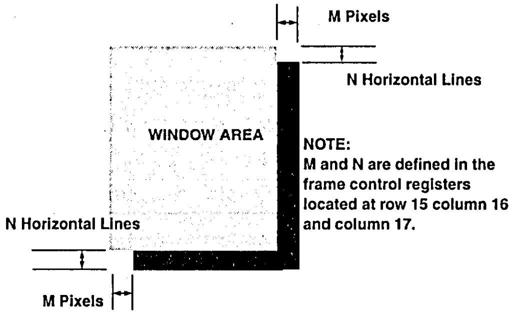
Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 1 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1.The default value is 1 to indicate high intensity..Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output black shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17. See the following figure and the related frame control register for detail.



Window Shadowing

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 2 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2. The default value is 1 to indicate high intensity..Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 2 shadowing.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 2. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 3 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity..Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 3 shadowing.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 3. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 4 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity..Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 4. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
ROW 15 COLN 12	VERTD MSB							LSB

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
ROW 15 COLN 13		HORD MSB						LSB

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Character Height Control Register Row 15 Coln 14

	7	6	5	4	3	2	1	0
ROW 15 COLN 14	HF	AUTO_CH	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance.

Bit 6 AUTO_CH - Auto Character Height Adjustment. If this bit is set, the character height will be controlled internally to keep the fixed ratio in the vertical direction and independent of the display modes. The ratio of character height to the screen is roughly 1/24, 1/36 and 1/48 for 320/480/640 resolution modes respectively. In the meantime, CH5-CH0 are ignored.

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height if AUTO_CH bit is cleared. It is possible to have a proper character height by setting a value greater than or equal to 16 on different horizontal frequency monitor. Setting a value below 16 will not have a predictable result. Figure 13 illustrates how this chip expand the built-in character font to the desired height.

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW	X64	X32B	3_S	FAN	FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 4-3 X64, X32B - It determines the number of dots per horizontal line. There are 320 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 480 dots per horizontal sync line is chosen when bit X64 is clear and 640 dots per horizontal sync line when bit X64 is set to 1. Please refer to the Table 1 for details.

Table 1. Resolution Setting

(X64, X32B)	(0, 0)	(1, 0)	(0, 1)	(1, 1)
Dots / Line	320	320	480	640
Resolution	CGA	CGA	EGA	VGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of characters or windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity characters or windows. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 1 FAN - It enables the fan-in/fan-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

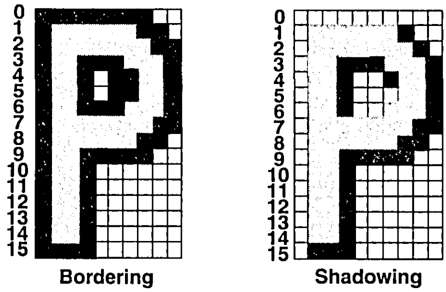


Figure 14. Character Bordering and Shadowing

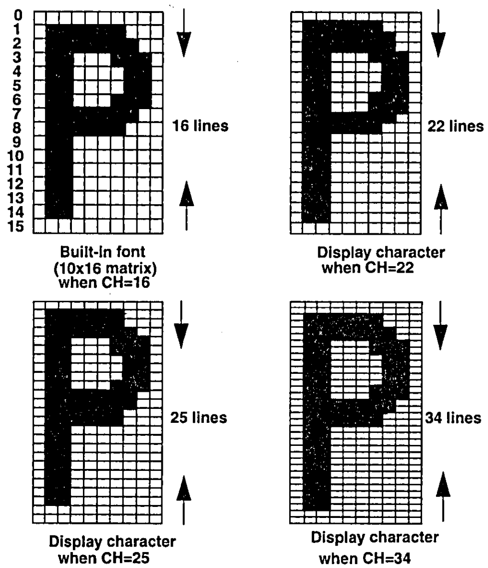
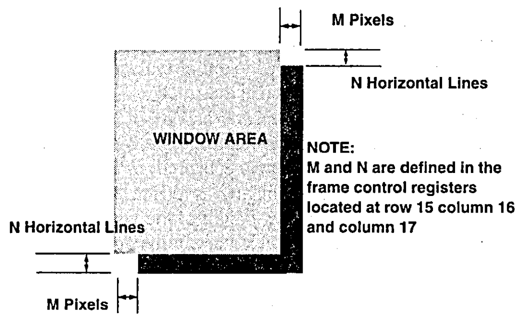


Figure 13. Variable Character Height



Window Shadowing

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
ROW 15 COLN 16	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 2. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 3. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

	7	6	5	4	3	2	1	0
ROW 15 COLN 18						TRIC	HPOL	VPOL

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{\text{HFLB}}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{\text{VFLB}}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

• **NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.**

PWM Control Registers Row 15 Col 20 to Col 31

	7	6	5	4	3	2	1	0
ROW 15 COLN 20-31	MSB			PWM_n				LSB

Bit 7-0 HORD - This eight-bit value decides the output duty cycle and waveforms of PWM. There are maximum 12 channels of PWM. And the corresponding registers are located from column 20 to column 31 respectively on row 15.

The higher five bits (MSB) are used for the conventional PWM and the lower 3 bits (LSB) for the BRM. Please refer to the following figures for more information about BRM algorithm and PWM output waveform.

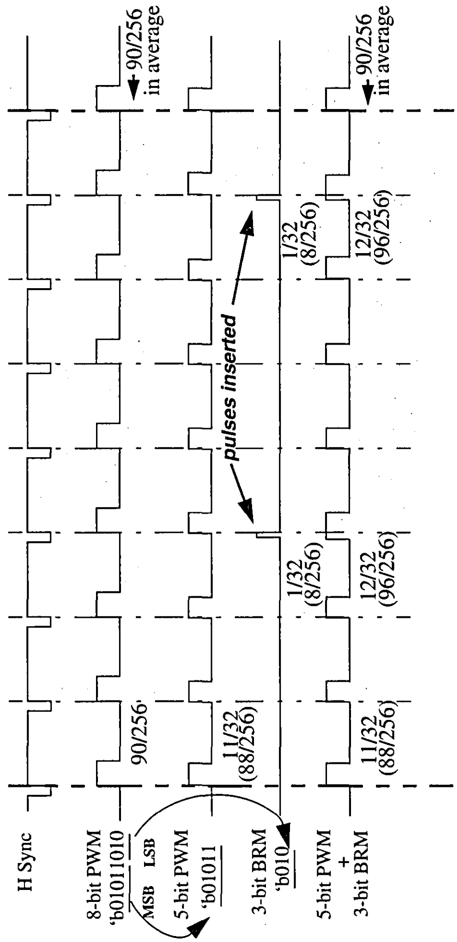


Figure 14. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

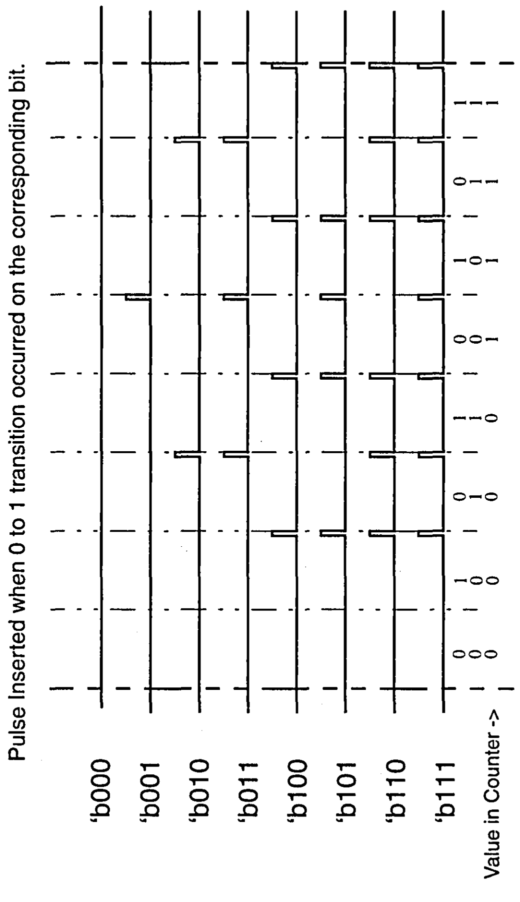


Figure 15. BRM Pulse Insertion Algorithm

A software called SMOSD FONT EDITOR in IBM PC environment was written for MC141548 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141548.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 10x16 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 14 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

Frame Format and Timing

Figure 16 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 16 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{HFLB}$ and $\overline{VFLB}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge-up resistor, which is the 330 kΩ resistor in a series with 2 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 320 if the bit X32B is clear and H Freq. x 480 if bit X32B is set to 1 and bit X64 is 0 and H Freq. x 640 if both bit X32B and bit X64 are set to 1. For example, dot frequency is 10.24 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1 and bit X64 is 0, the dot frequency will be 15.36 MHz (one and a half of the original one). If X32B is 1 and bit X64 is also 1, the dot frequency will be 20.48 MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{VFLB}$ of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 300, regardless of row character width and the setting of bit X32B and X64.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 320 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 480 dots and 640 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 17 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

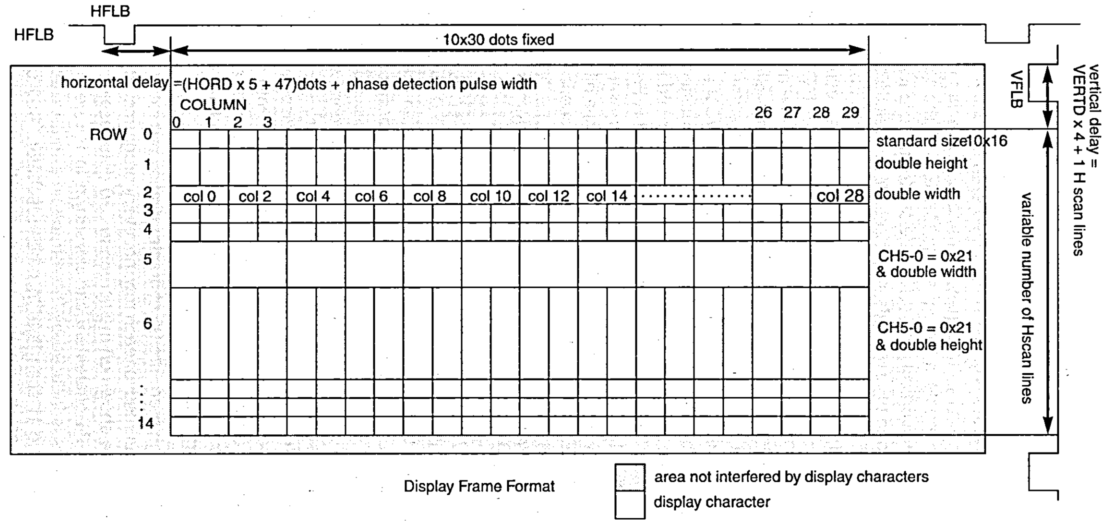
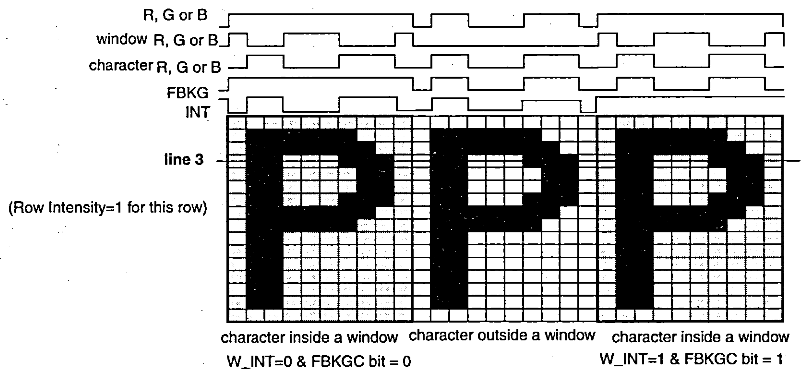


Figure 16. Display Frame Format



Timing of Output Signals as a Function of Window, FBKGC bit and Row Intensity Features

Figure 17. Timing of Output Signals

FONT

MC141548 contains 256 character/symbol fonts including 8 RAM fonts and 248 ROM fonts. The RAM fonts occupy the font number $00 to $07 and their patterns can be changed at any time via the SPI or MBUS protocol described above. The masked ROM fonts are fixed and located from number $08 to $FF. See the figures on the next page for the details fonts mapping.

Icon Combination

User can create On-Screen menu based on those characters and icons. Please refer to Table 4 for Icon combination. Address $00 & $FF are pre-defined characters for testing.

Table 4. Combination Map 1

ICON	ROM ADDRESS(HEX)
RAM CHARACTERS	00-07
ARABIC NUMERALS	09-11
ALPHABET	12-2D
EUROPEAN	2E-48
JAPANESE	48-91
SYMBOLS	82-C4, EF-FE
GEOMETRY	C5-EE

ROM CONTENT

Figures 18 – 21 show the ROM content of MC141548. Mask ROM is optional for custom parts.

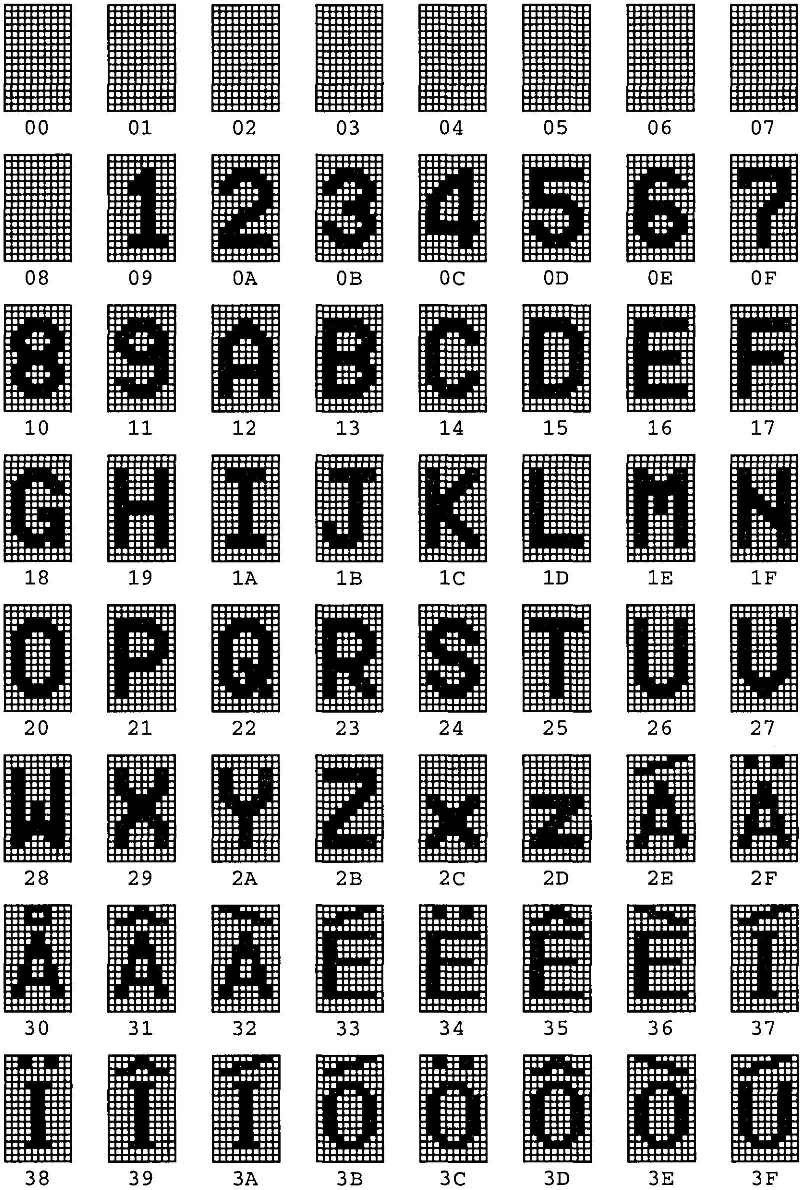


Figure 18. ROM Address ($08 - $3F)

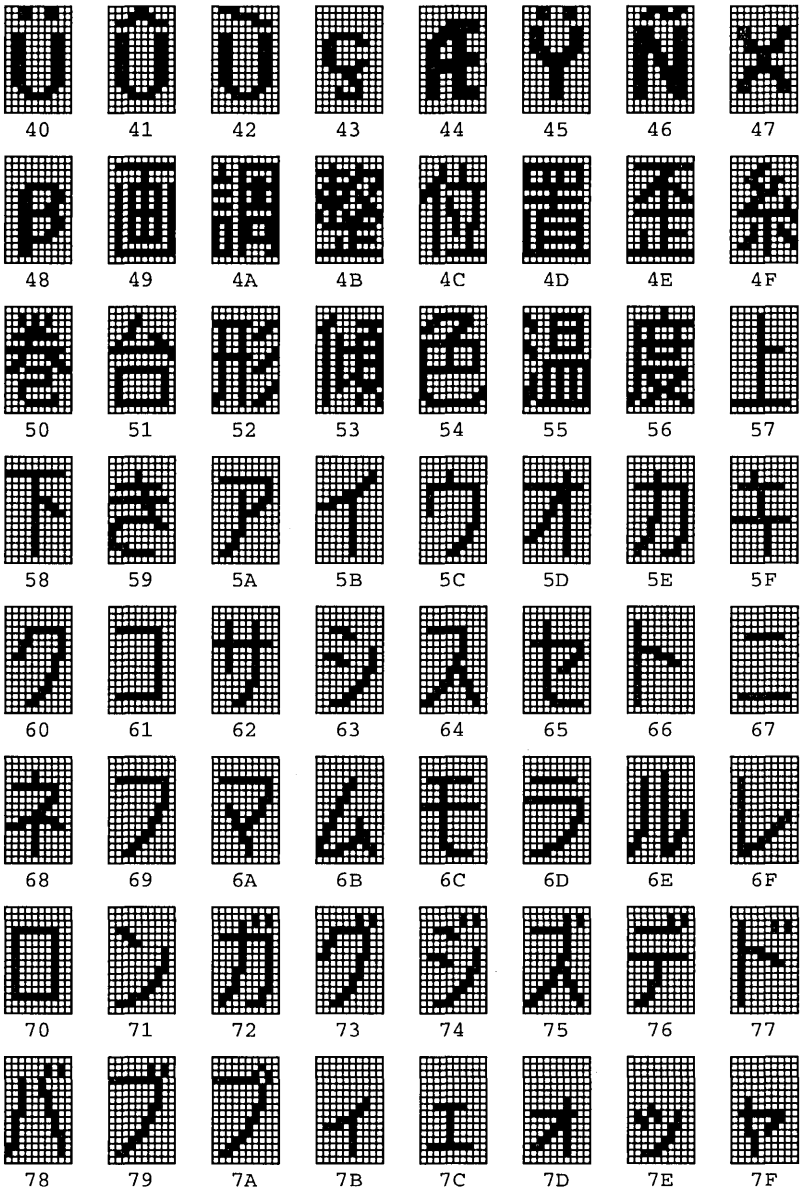


Figure 19. ROM Address ($40 - $7F)

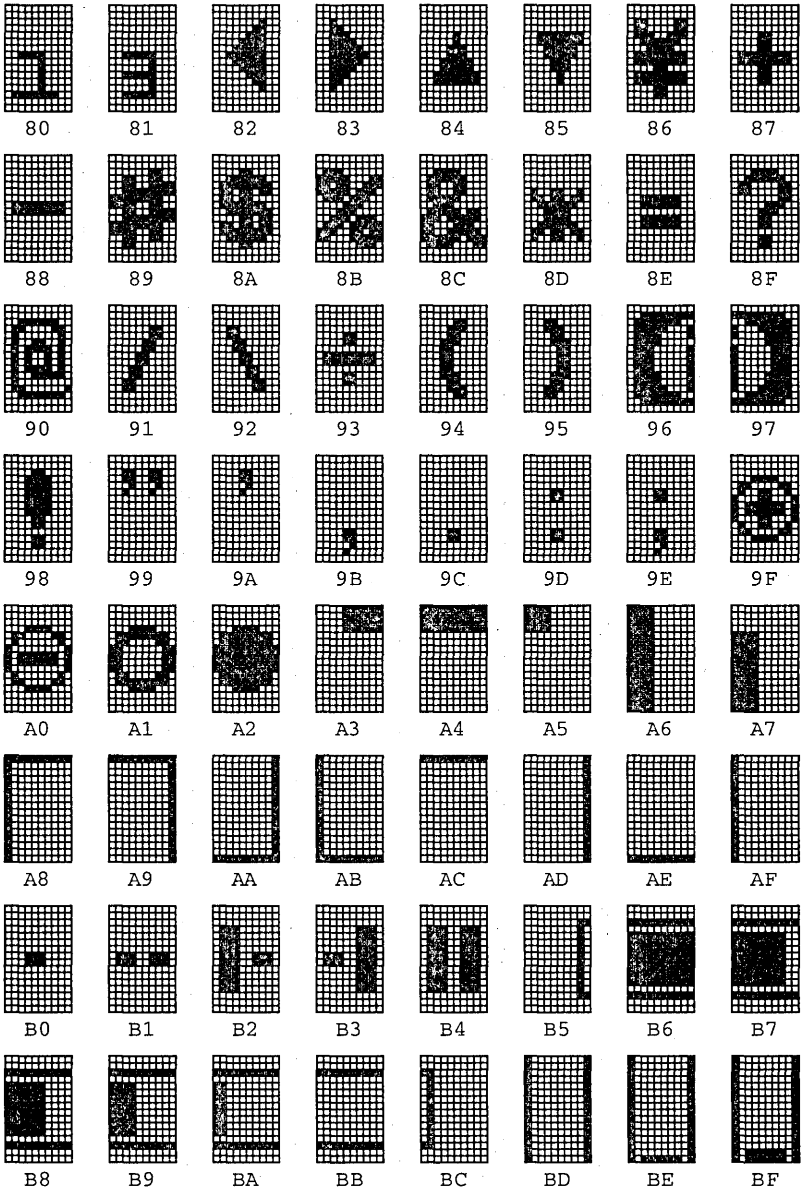


Figure 20. ROM Address ($80 - $BF)

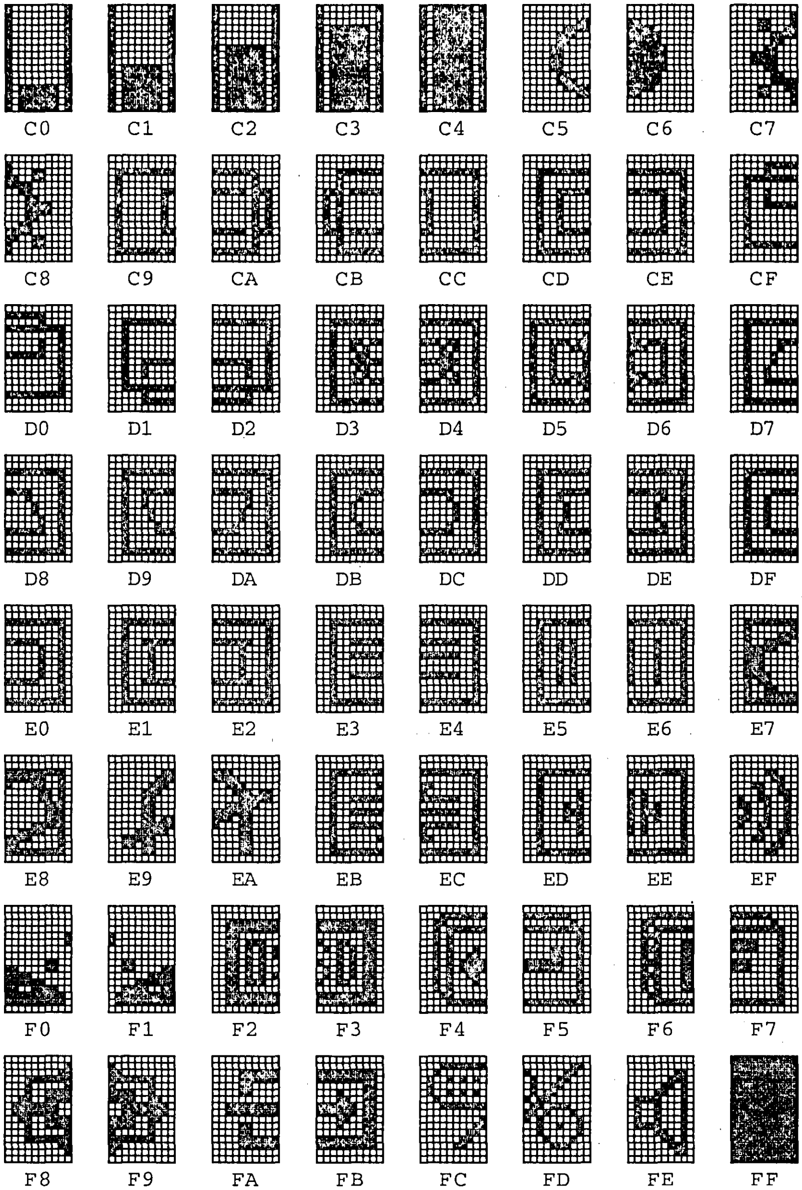


Figure 21. ROM Address ($C0 - $FF)

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141548P has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 320/480/640 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating). Refer to the Application Diagram for the ground connections.
- DC supply path for Pin 17 (V_{DD}) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.

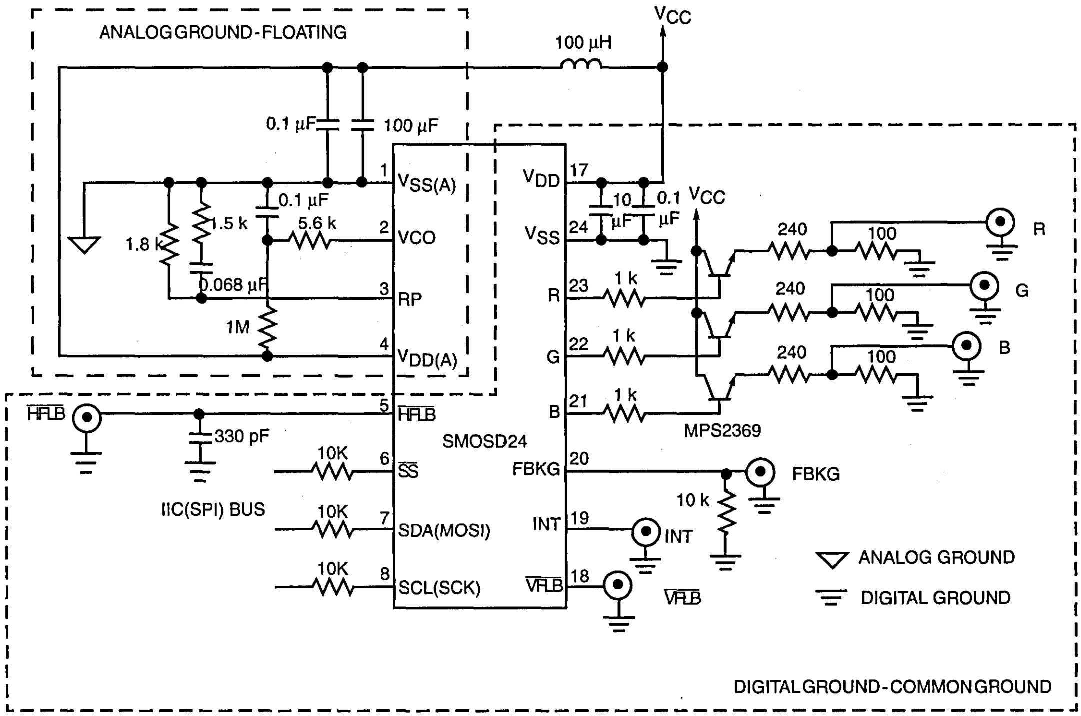
Jittering

Most display jittering is caused by HFLB jittering in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. A small capacitor can be added between Pin 5 – Pin 24 to smooth the signal. Refer to the value used in the Application Diagram.

Display Dancing

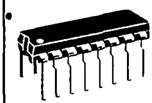
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



Super Monitor On-Screen Display - 16
CMOS

MC141549P



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION

MC141549P   Plastic Dip

PIN ASSIGNMENT

$V_{SS(A)}$	1	16	V_{SS}
VCO	2	15	R
RP	3	14	G
$V_{DD(A)}$	4	13	B
$\overline{HFLB}$	5	12	FBKG
$\overline{SS}$	6	11	INT
SDA(MOSI)	7	10	$\overline{VFLB}$
SCL(SCK)	8	9	V_{DD}

This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto color monitor. Because of the large number of fonts, 256 fonts including the programmable RAM fonts and fixed ROM fonts, SMOSD-16 is suitable to be adopted for the multi-language monitor application especially. Its on-chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

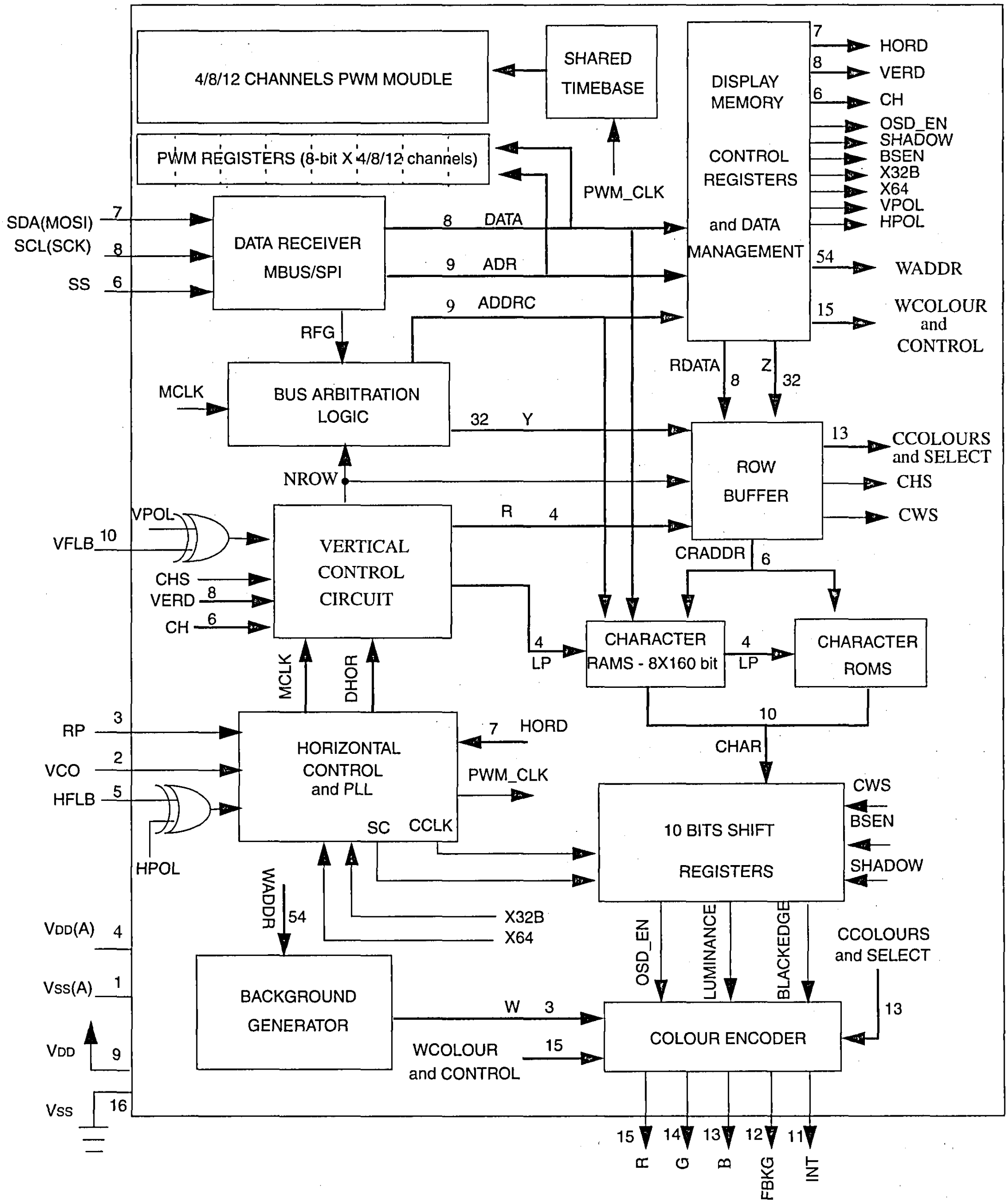
Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. Besides, there are three kinds of different resolutions that users can choose. By changing the number of dots per horizontal line to 320 (CGA), 480 (EGA) or 640 (VGA), smaller characters with higher resolution can be easily achieved.

Special functions such as character blinking, automatic height scaling, character/window bordering or character shadowing, four-level windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, 8 programmable character/symbol RAM fonts are also built-in. It is much flexible to create the new symbols, icons and logo. One special attractive application of the RAM fonts is the real-time programming to achieve the dynamic image instead of the static picture as previous.

- Totally 256 Characters and Graphic Fonts Including 8 Programmable RAM Fonts and 248 Mask ROM Fonts
- Three Selectable Resolutions: 320 (CGA), 480 (EGA) or 640 (VGA) Dots/Line
- Wide Operating Frequency Range for High End Monitor: 15KHz ~ 120KHz
- Fully Programmable Character Array of 15 Rows by 30 Columns
- True 16-Color Selection for Windows
- Fancy Fade-In/Fade-Out Effects
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- Auto Height Scaling to Keep Constant Height Independent of Display Modes
- Four Programmable Background Windows with Overlapping Capability
- Shadowing on Windows with Programmable Shadow Width/Height
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
- Programmable Vertical Height of Character to Meet Multi-Sync Requirement
- Programmable Vertical and Horizontal Positioning for Display Centre
- Double Character Height and Double Character Width
- Internal PLL Generates a Wide-Ranged System Clock (76.8 MHz)
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

REV 1
12/95

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	—	—	120K	Hz

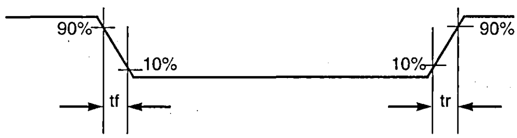


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{Il}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{Il}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 15	mA

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

V_{DD} (Pin 9)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT (Pin 11)

This output pin is used to indicate the color intensity. If the intensity control bits are set in the row attribute registers or window control registers, this pin will output a logic high while displaying the specified windows or the characters on the associated rows. Otherwise, it will keep in low state. Please refer to Figure 17 for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

FBKG (Pin 12)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13, 14, 15)

SMOSD-16 color outputs in TTL level to the host monitor. These three signals are open drain outputs if 3_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141549 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the SMOSD-16 is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the SMOSD-16 functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{\text{HFLB}}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps.The default chip address is $7A.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the SMOSD-16 circuitry of MC141549, so that the received information can then be displayed.

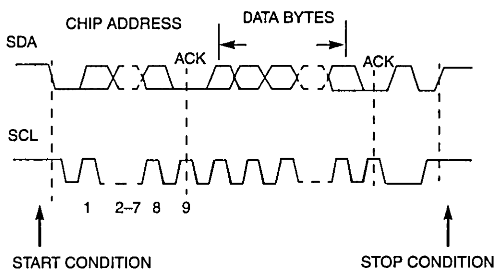


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{\text{SS}}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{\text{SS}}$ pin low by the master device to enable MC141549 to accept data. The $\overline{\text{SS}}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{\text{SS}}$ pin is then pulled high by master to terminate the transmission. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

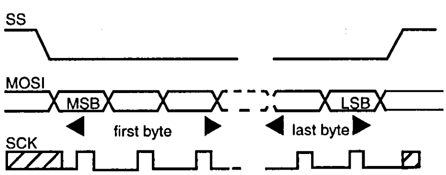


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, three register blocks, display registers, attribute/control registers and RAM fonts, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:

(a) R - > C- > I -> R - > C - > I - > ....

(b) R - > C - > I - > C - > I - > C - > I.......

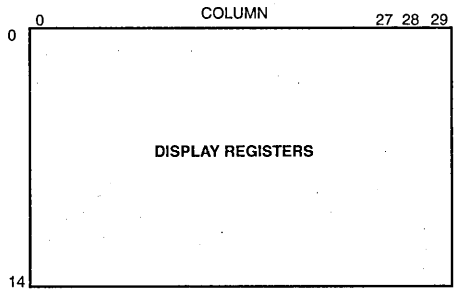
(c) R - > C - > I - > I - > I - > ....

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the display row address from attribute/RAM fonts area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet for Display Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:

(a) R - > C- > I -> R - > C - > I - > ....

(b) R - > C - > I - > C - > I - > C - > I.......

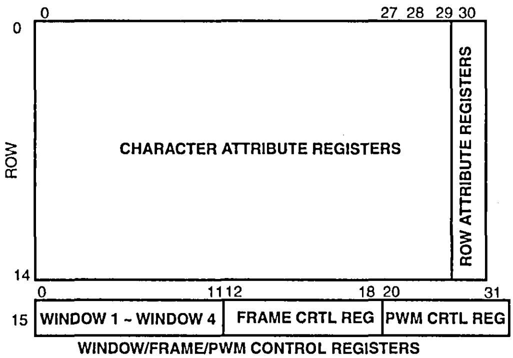
(c) R - > C - > I - > I - > I - > ....

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 6. Data Packet for Attribute/Control Data



ADDRESS	BIT 7	6	5	4	3	2	1	0	FORMAT
ROW	1	0	1	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 7. Address Bit Patterns for Attribute/Control Data

(III) RAM Fonts Programming

Basically, the transmission format is very similar with that for display RAM or control registers. The major difference is to replace the row and column address with segment address and line address respectively. There are also three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of segment address (S), line address (L), and font informations (I), as shown in Figure 3. In format (a), each font information data have to be preceded with the corresponding segment address and line address. This format is particular suitable for updating small portion of font pattern. However, if the current information byte has the same segment address as the one before, format (b) is recommended. For a new font pattern change which requires massive information update or during power up situation, most of the segment and column address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the character RAM starting segment and line addresses once only, and then treat all subsequent data as font information. The segment and line addresses will be automatically incremented internally for each RAM font data from the starting location.

The transmission formats are shown below:

(a) S - > L - > I -> S - > L - > I - > ....

(b) S - > L - > I - > L - > I - > L - > I.......

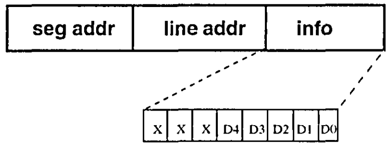
(c) S - > L - > I - > I - > I - > ....

NOTE: S means segment byte.

L means line byte.

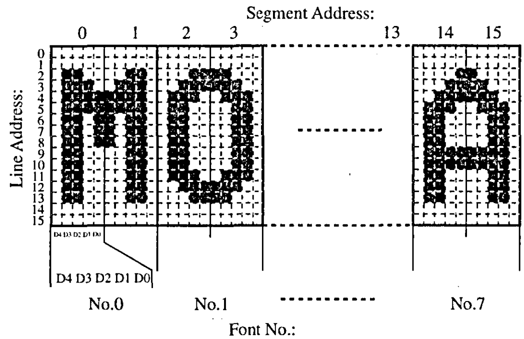
I means data byte.

To differentiate the segment address from row and line address when transferring data, the bit 7 (MSB) and bit 6 are set to '11' to represent segment address, while '00' for line address used in format (a) or (b) and '01' for line address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).



NOTE: X means don't care bit and D means valid data bit.

Figure 8. Data Packet for RAM Fonts



ADDRESS	BIT 7	6	5	4	3	2	1	0	FORMAT
SEG	1	1	X	X	D	D	D	D	a, b, c
LINE	0	0	X	X	D	D	D	D	a, b
LINE	0	1	X	X	D	D	D	D	c

X: don't care D: valid data

Figure 9. Address Bit Patterns for RAM Fonts

MEMORY MANAGEMENT

All the internal programmable area can be divided into three parts including (1) Display Registers (2) Attribute/Control Registers and (3) Programmable RAM Fonts. Please refer to the following three figures for the corresponding memory map.

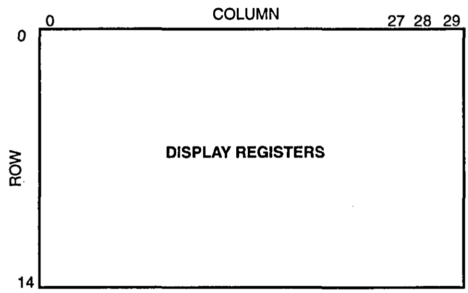


Figure 10. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 RAM/ROM fonts.

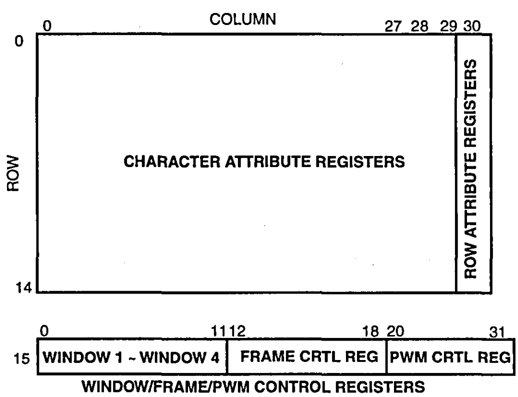


Figure 11. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. Every data row associate with one attribute register, which locate at coln 30 of their respective rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control, frame function control and PWM registers. Three window control registers for each of four windows together with four frame control registers and twelve PWM registers occupy the first 28 columns of row 15 space. These control registers will be described on the "REGISTERS" section.

User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

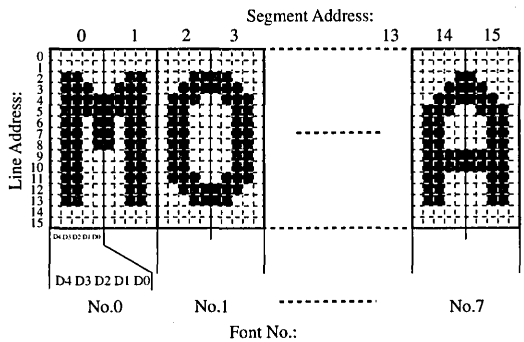


Figure 12. Memory Map of Programmable RAM Fonts

Another programming area is the RAM fonts. Totally, 8 fonts are programmable in SMOSD-16. The structure of 8 character RAM fonts are shown in Figure 12. They occupy the font number from 0 to 7 while ROM fonts 8 to 255. Because of the 10X16 dot matrix font, we decompose each font into 2 segments in horizontal direction and 16 lines in vertical direction. So, there are 5 dots needed to be defined for each specified segment-line location. This 5-bit data forms the lower 5 bits of the information data byte and the higher 3 bits are ignored. Because there are 16 segments (2 segments per font) and 16 lines, both the segment and line addresses are 4-bit wide.

REGISTERS

(I) Display Register

Display Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
←			CRADDR				→

Bit 7-0 CRADDR - This eight bits address one of the 256 characters or symbols resided in the character RAM/ROM fonts.

(II) Attribute/Window/Control/Frame Registers

Character Attribute Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
				BLINK	R	G	B

Bit 3 BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

Bit 2-0 These three bits are the color attribute to define the color of the associated character/symbol.

Row Attribute Register (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
					R_INT	CHS	CWS

Bit 2 R_INT - Row intensity bit controls the color intensity of the displayed character/symbol on the corresponding row. Setting this bit to 1 means high intensity color and the INT pin will go high while displaying the characters of this row.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR (MSB)			(LSB)	ROW END ADDR (MSB)			(LSB)

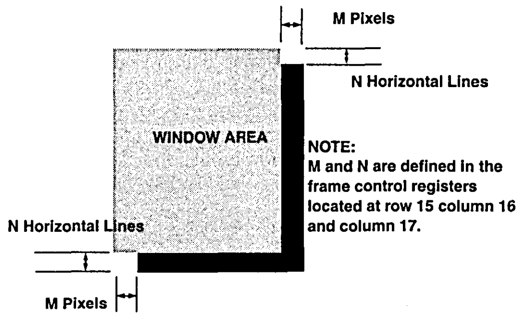
Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR (MSB)				(LSB)	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 1 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output black shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17. See the following figure and the related frame control register for detail.



Window Shadowing

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR (MSB)				(LSB)	R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR (MSB … LSB)					WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 2 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 2 shadowing.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 2. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR (MSB … LSB)					WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 3 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 3 shadowing.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 3. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	COL START ADDR (MSB … LSB)					WEN	W_INT	W_SHD

Bit 2 WEN - It enables the background window 4 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 4. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
ROW 15 COLN 12	MSB			VERTD				LSB

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
ROW 15 COLN 13		MSB			HORD			LSB

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Character Height Control Register Row 15 Coln 14

	7	6	5	4	3	2	1	0
ROW 15 COLN 14	HF	AUTO_CH	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance.

Bit 6 AUTO_CH - Auto Character Height Adjustment. If this bit is set, the character height will be controlled internally to keep the fixed ratio in the vertical direction and independent of the display modes. The ratio of character height to the screen is roughly 1/24, 1/36 and 1/48 for 320/480/640 resolution modes respectively. In the meantime, CH5-CH0 are ignored.

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height if AUTO_CH bit is cleared. It is possible to have a proper character height by setting a value greater than or equal to 16 on different horizontal frequency monitor. Setting a value below 16 will not have a predictable result. Figure 13 illustrates how this chip expand the built-in character font to the desired height.

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW	X64	X32B	3_S	FAN	FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 4-3 X64, X32B - It determines the number of dots per horizontal line. There are 320 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 480 dots per horizontal sync line is chosen when bit X64 is clear and 640 dots per horizontal sync line when bit X64 is set to 1. Please refer to the Table 1 for details.

Table 1. Resolution Setting

(X64, X32B)	(0, 0)	(1, 0)	(0, 1)	(1, 1)
Dots / Line	320	320	480	640
Resolution	CGA	CGA	EGA	VGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of characters or windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity characters or windows. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 1 FAN - It enables the fan-in/fan-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

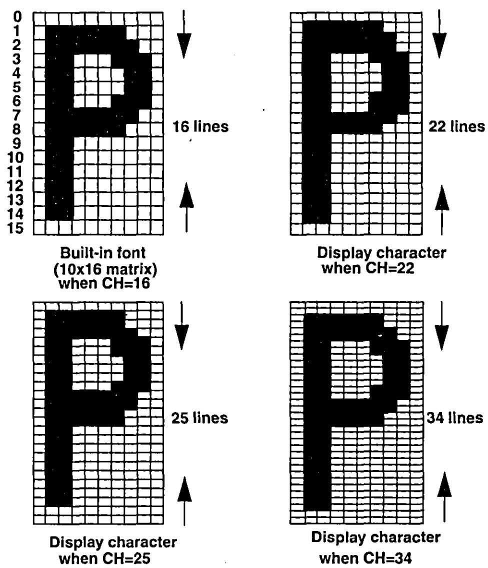


Figure 13. Variable Character Height

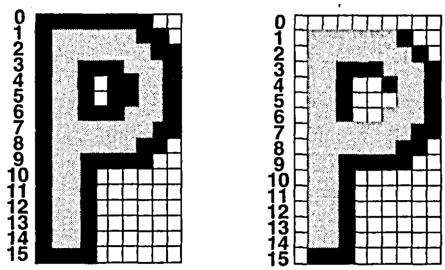
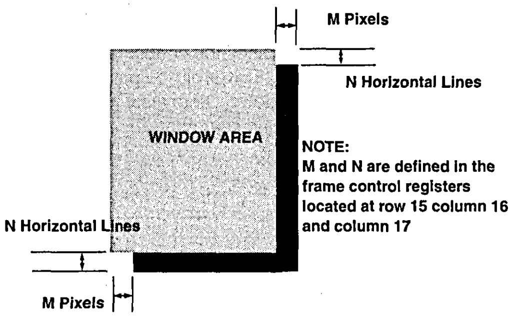


Figure 14. Character Bordering and Shadowing



Window Shadowing

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
ROW 15 COLN 16	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 2. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 3. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

	7	6	5	4	3	2	1	0
ROW 15 COLN 18						TRIC	HPOL	VPOL

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{HFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{VFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

• **NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.**

PWM Control Registers Row 15 Col 20 to Col 31

	7	6	5	4	3	2	1	0
ROW 15 COLN 20-31	MSB			PWM_n				LSB

Bit 7-0 HORD - This eight-bit value decides the output duty cycle and waveforms of PWM. There are maximum 12 channels of PWM. And the corresponding registers are located from column 20 to column 31 respectively on row 15.

The higher five bits (MSB) are used for the conventional PWM and the lower 3 bits (LSB) for the BRM. Please refer to the following figures for more information about BRM algorithm and PWM output waveform.

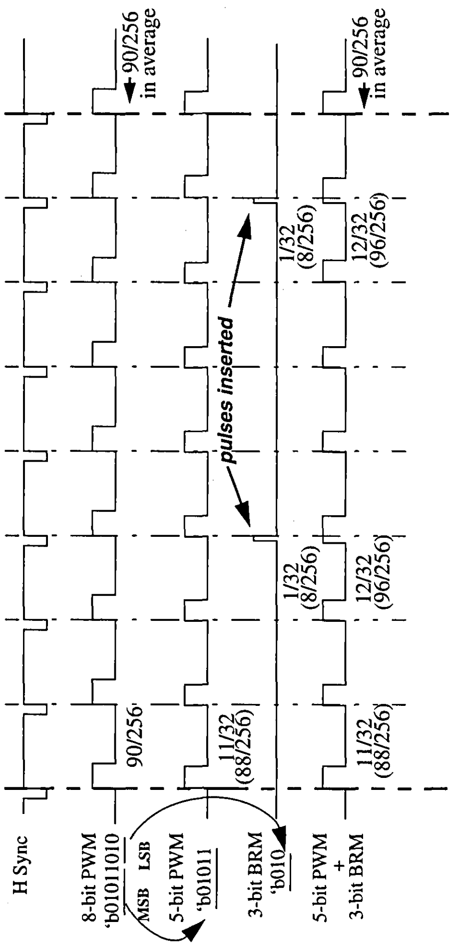


Figure 14. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

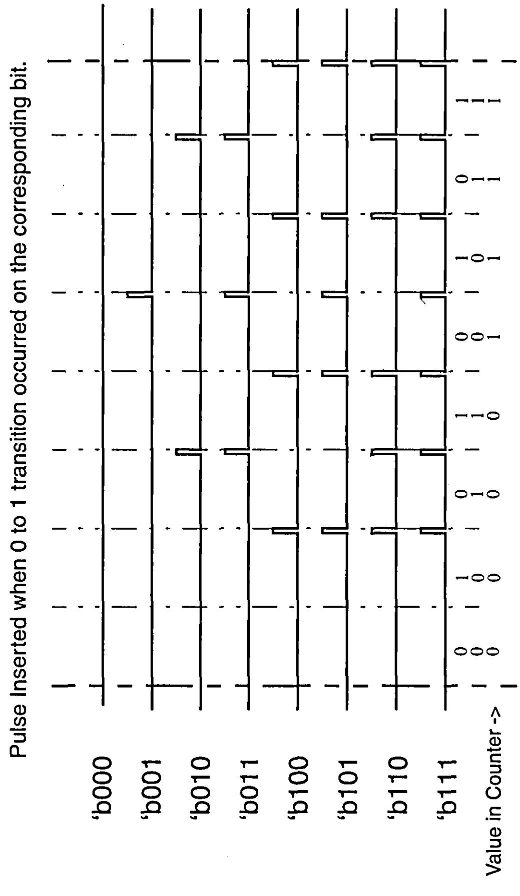


Figure 15. BRM Pulse Insertion Algorithm

A software called SMOSD-16 FONT EDITOR in IBM PC environment was written for MC141548 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141548.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 10x16 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 14 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

Frame Format and Timing

Figure 16 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 16 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{HFLB}$ and $\overline{VFLB}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge-up resistor, which is the 330 kΩ resistor in a series with 2 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 320 if the bit X32B is clear and H Freq. x 480 if bit X32B is set to 1 and bit X64 is 0 and H Freq. x 640 if both bit X32B and bit X64 are set to 1. For example, dot frequency is 10.24 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1 and bit X64 is 0, the dot frequency will be 15.36 MHz (one and a half of the original one). If X32B is 1 and bit X64 is also 1, the dot frequency will be 20.48 MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{VFLB}$ of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 300, regardless of row character width and the setting of bit X32B and X64.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 320 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 480 dots and 640 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 17 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

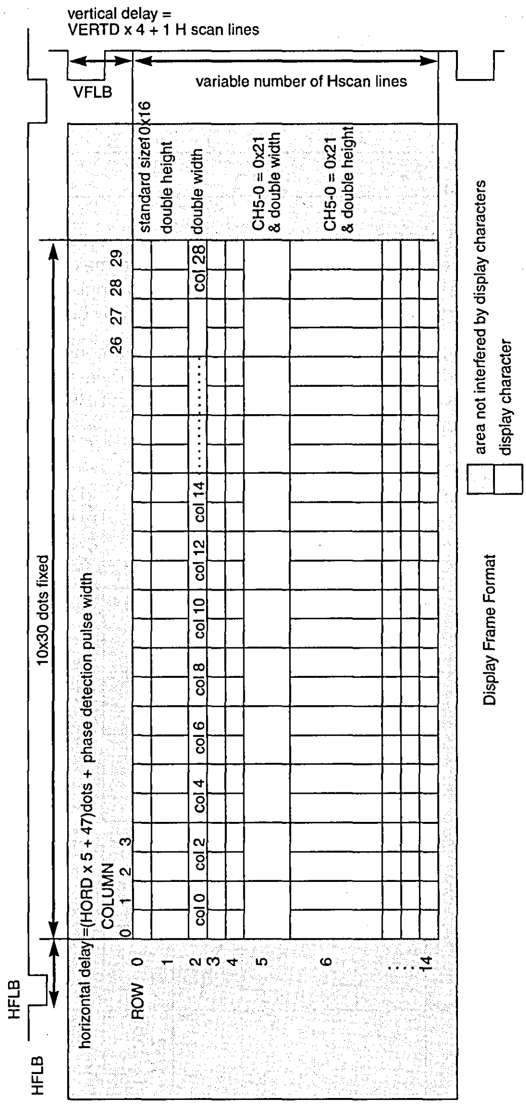


Figure 16. Display Frame Format

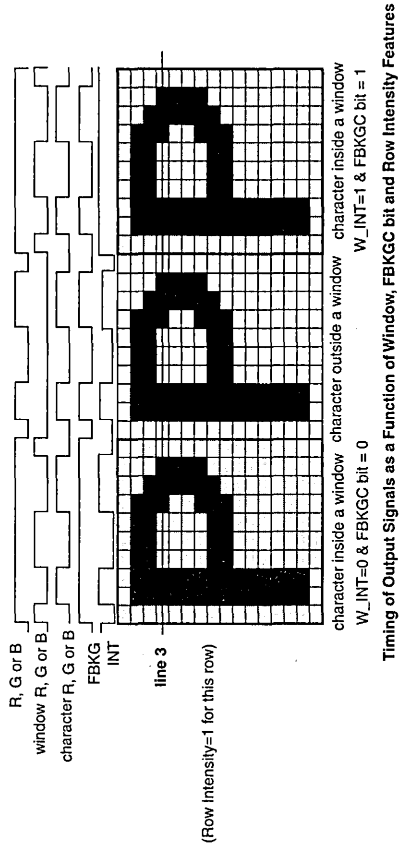


Figure 17. Timing of Output Signals

FONT

MC141549 contains 256 character/symbol fonts including 8 RAM fonts and 248 ROM fonts. The RAM fonts occupy the font number $00 to $07 and their patterns can be changed at any time via the SPI or MBUS protocol described above. The masked ROM fonts are fixed and located from number $08 to $FF. See the figures on the next page for the details fonts mapping.

Icon Combination

User can create On-Screen menu based on those characters and icons. Please refer to Table 4 for Icon combination. Address $00 & $FF are pre-defined characters for testing.

Table 4. Combination Map 1

ICON	ROM ADDRESS(HEX)
RAM CHARACTERS	00-07
ARABIC NUMERALS	09-11
ALPHABET	12-2D
EUROPEAN	2E-48
JAPANESE	49-81
SYMBOLS	82-C4, EF-FE
GEOMETRY	C5-EE

ROM CONTENT

Figures 18 – 21 show the ROM content of MC141549. Mask ROM is optional for custom parts.

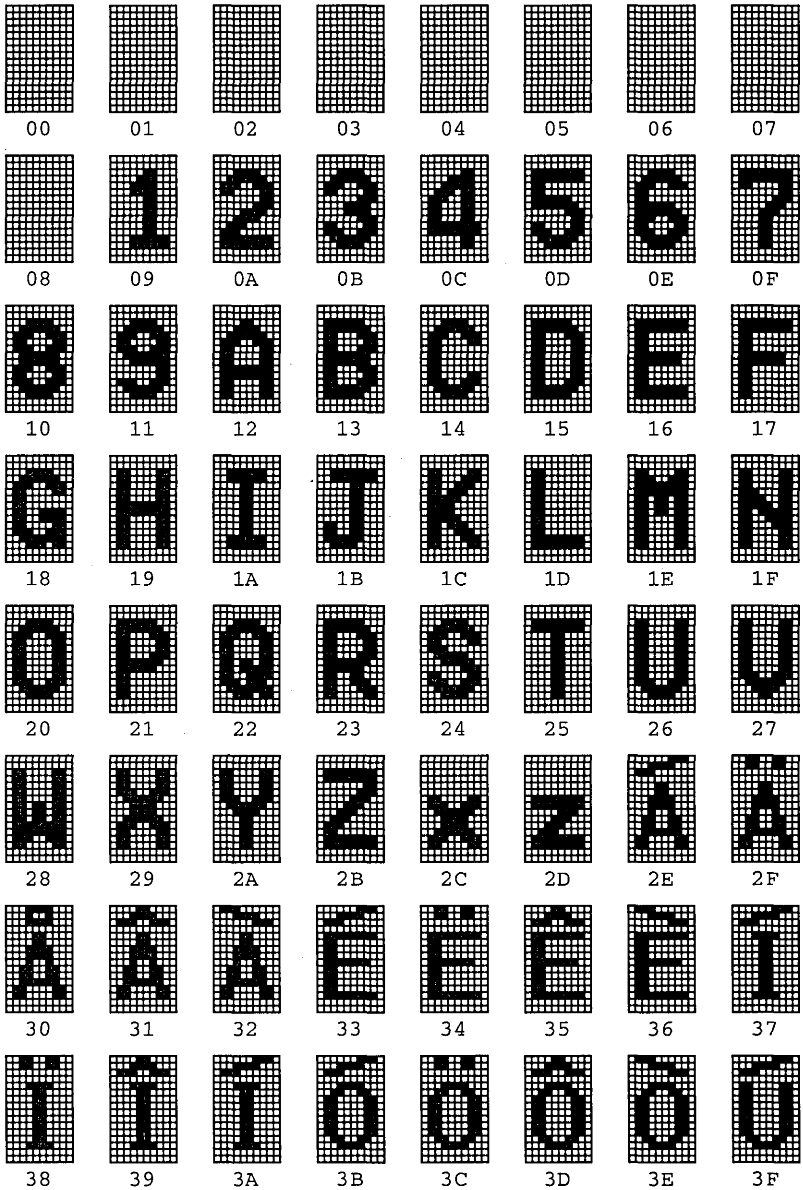


Figure 18. ROM Address ($08 - $3F)

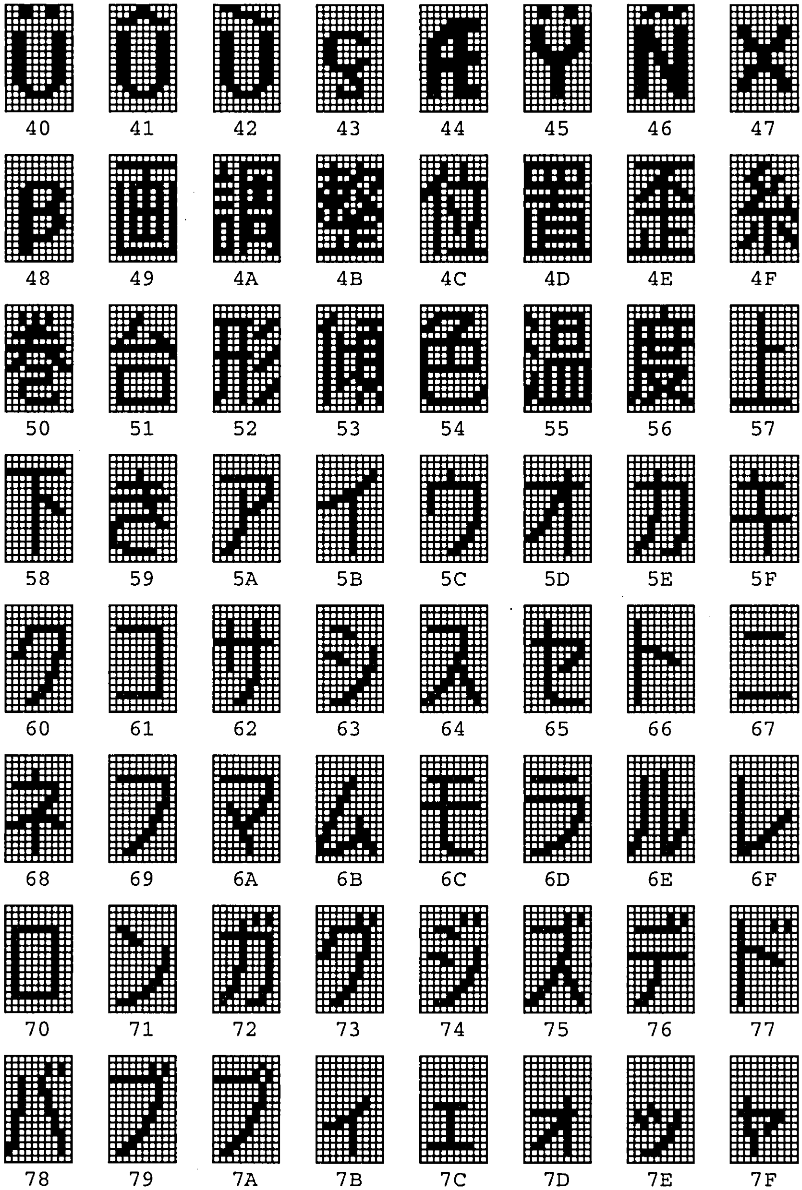


Figure 19. ROM Address ($40 - $7F)

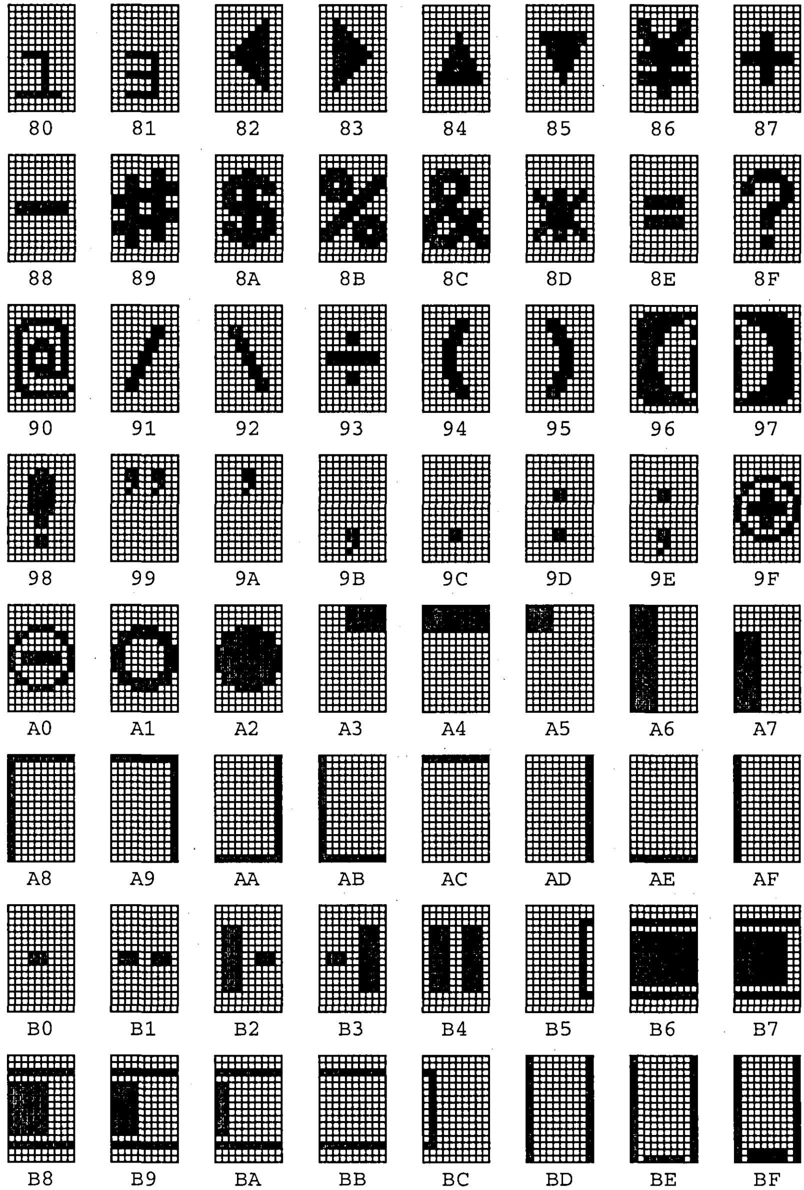


Figure 20. ROM Address ($80 - $BF)

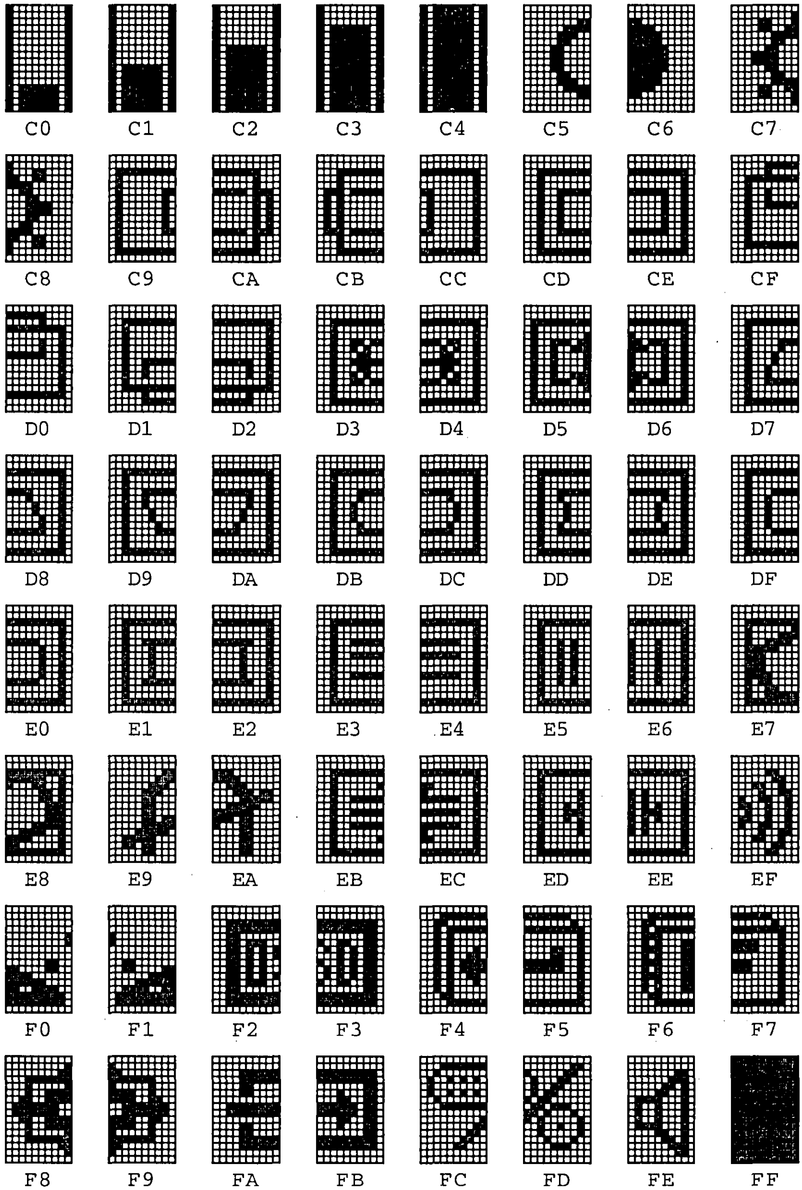


Figure 21. ROM Address ($C0 - $FF)

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141549P has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 320/480/640 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating). Refer to the Application Diagram for the ground connections.
- DC supply path for Pin 9 (V_{DD}) should be separated from other switching devices.
- LC filter should be connected between Pin 9 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.

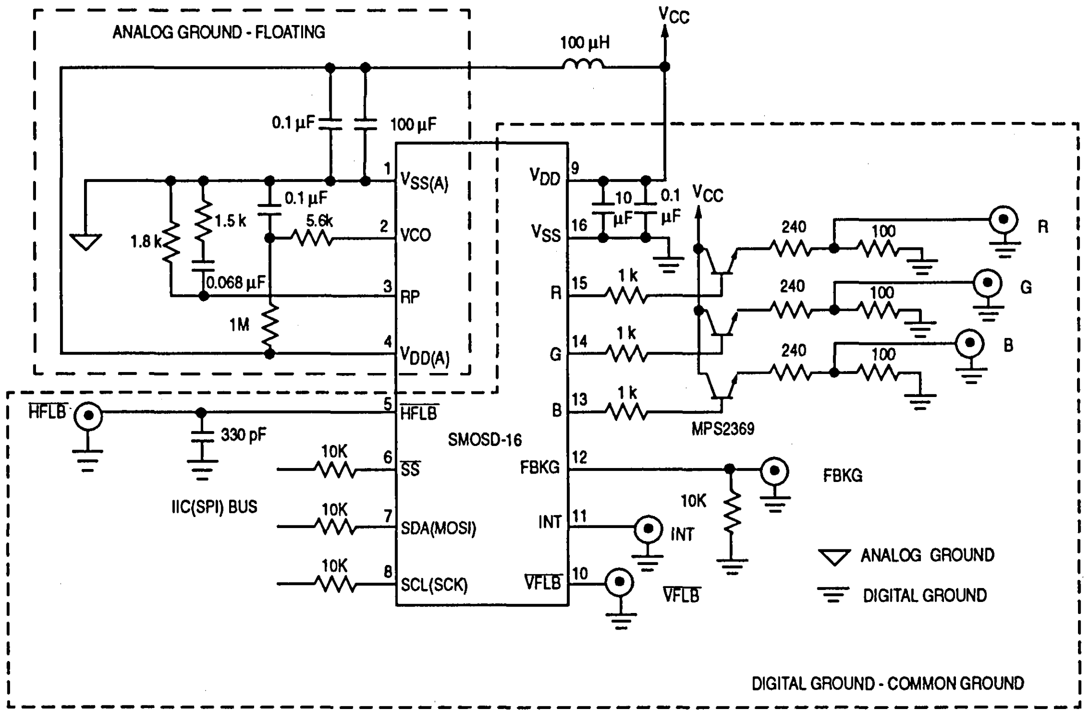
Jittering

Most display jittering is caused by HFLB jittering in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. A small capacitor can be added between Pin 5 – Pin 16 to smooth the signal. Refer to the value used in the Application Diagram.

Display Dancing

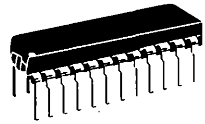
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



MC141546P2

Advanced Monitor On-Screen Display II - 24
CMOS



P SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION
MC141546P2 Plastic Dip

PIN ASSIGNMENT

$V_{SS(A)}$	1	24	V_{SS}
VCO	2	23	R
RP	3	22	G
$V_{DD(A)}$	4	21	B
$\overline{HFLB}$	5	20	FBKG
$\overline{SS}$	6	19	INT/Cout
SDA(MOSI)	7	18	$\overline{VFLB}$
SCL(SCK)	8	17	V_{DD}
PWM 6	9	16	PWM 7
PWM 4	10	15	PWM 5
PWM 2	11	14	PWM 3
PWM 0	12	13	PWM 1

This is a high performance HCMOS device designed to interface with a micro-controller unit to allow colored symbols or characters to be displayed on a color monitor. Its on-chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built-in display and control bytes RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are two different resolutions that users can choose. By changing the number of dots per horizontal line to 384 (CGA) or 768 (VGA), smaller characters with higher resolution can be easily achieved.

Special functions such as character bordering or shadowing, multi-level windows, intensity control for windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, neither massive information update nor extremely high data transmission rate are expected for normal on- screen display operation and serial protocols are implemented in lieu of any parallel formats to achieve the minimum pin count.

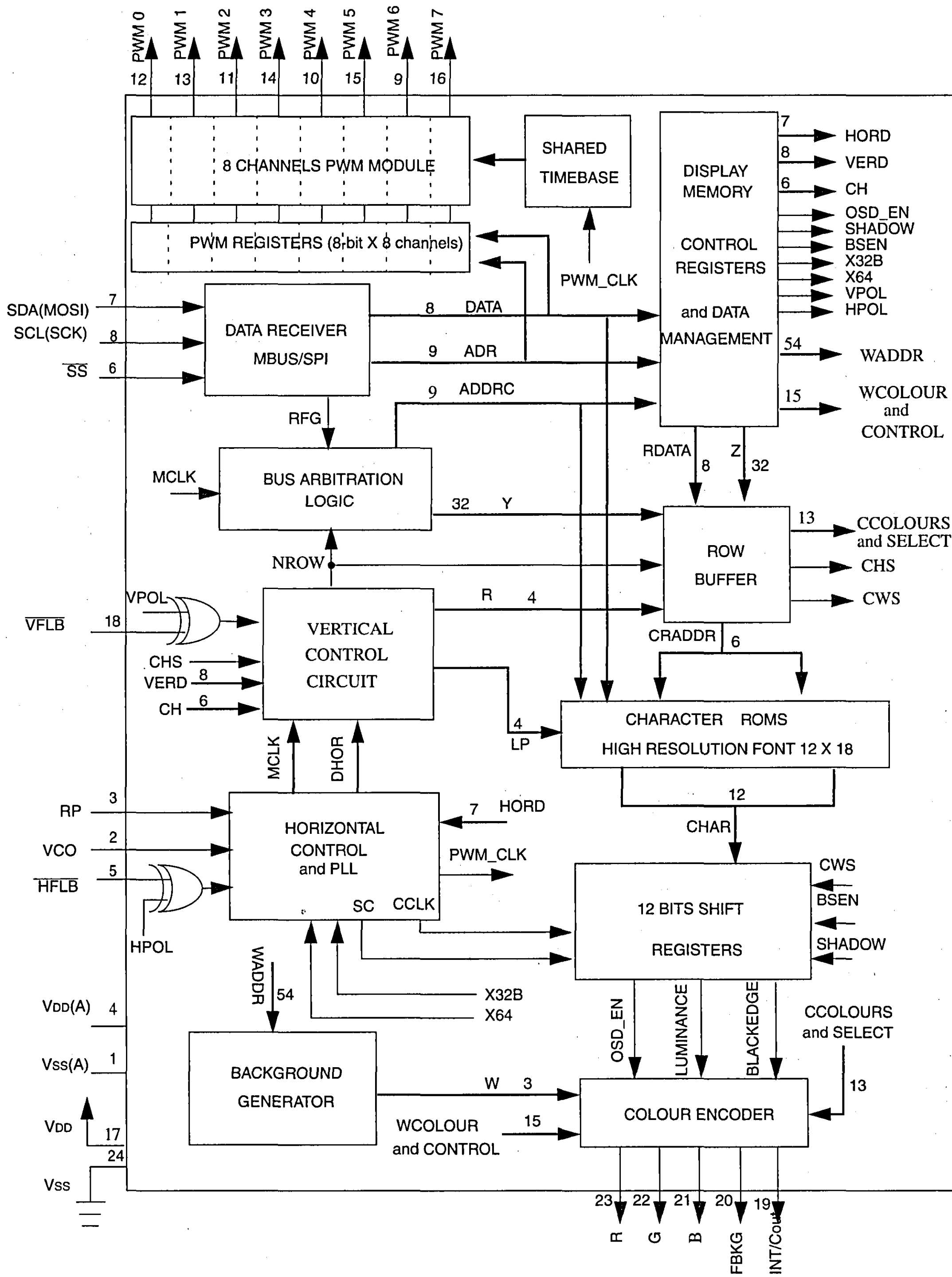
There are 8 PWM DAC channels for external digital to analog control. Each PWM DAC channel is composed of an 8 bit register which contains a 5 bit PWM in MSB portion and a 3 bit binary rate multiplier (BRM) in LSB portion.

Moreover, the font matrix is improved from 10 by 16 to high resolution font matrix, 12 by 18, in this version. In order to maintain the constant menu height in the different display modes, one special register, controlling the row to row spacing, is implemented to avoid the nonuniform extension of BRM algorithm in character height adjustment.

- 8 Channels 8-bit Synchronous PWM DAC with Push-Pull Output
- Two Resolutions: 384 (CGA) or 768 (VGA) Dots per Line
- 12 x 18 Dot Matrix Character
- Maximum Horizontal Frequency is 120 KHz (92.2MHz Dot Clock at 768 mode)
- Four Fully Programmable Background Windows with Intensity Control
- Row to Row Spacing Register to Manipulate the Constant Menu Height
- Programmable Height of Character to Meet Multi-Sync Requirement
- Smooth Menu Movement by Real Time Programming of H/V Delay Registers
- Fully Programmable Character Array of 15 Rows by 30 Columns
- Internal PLL Generates a Wide-Ranged System Clock
- Programmable Vertical and Horizontal Positioning for Display Center
- 128 Characters and Graphic Symbols ROM (Mask ROM is Optional)
- Character by Character Color Selection
- A Maximum of Four Selectable Colors per Row
- Double Character Height and Double Character Width
- Character Bordering or Shadowing
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

REV 1
4/97

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT/Cout) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
	Output Signal (PWM0 - PWM7) C_{load} = 30 pF				
t_r	Rise Time	—	—	20	ns
t_f	Fall Time	—	—	20	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	15K	—	120K	Hz

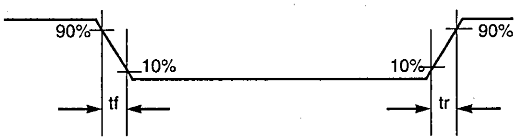


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{Il}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{Il}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 20	mA
LVI	Low Voltage Inhibit for PWM DAC Output	2.7	3.2	3.6	V

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configured as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

PWM 6 (Pin 9)

Channel 6 of the PWM.

PWM 4 (Pin 10)

Channel 4 of the PWM.

PWM 2 (Pin 11)

Channel 2 of the PWM.

PWM 0 (Pin 12)

Channel 0 of the PWM.

PWM 1 (Pin 13)

Channel 1 of the PWM.

PWM 3 (Pin 14)

Channel 3 of the PWM.

PWM 5 (Pin 15)

Channel 5 of the PWM.

PWM 7 (Pin 16)

Channel 7 of the PWM.

V_{DD} (Pin 17)

This is the power pin for the digital logic of the chip.

$\overline{VFLB}$ (Pin 18)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT/ Cout (Pin 19)

This is a multiplexed pin. When the Cout bit is cleared after power on or by the MCU, this pin is INT and this output pin is used to indicate the color intensity. If the associated window intensity control bits are set, this pin will output a logic high while displaying the specified windows. Otherwise, it will keep in low state. Only the windows have the color intensity selection and all displayed characters or symbols are all high intensity. It means that INT pin must be driven high while displaying the characters or symbols.

Please refer to the timing figure for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs for windows' color control. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

If the Cout bit is set to 1 via M_BUS or SPI, this pin is changed to a mode-dependent clock output with 50/50 duty cycle and synchronous with the input horizontal synchronization signal at Pin 5. The frequency is dependent on the mode in which the AMOSD II is currently running. The exact frequencies in the different resolution modes are described below.

Resolution	Frequency	Duty Cycle
384 dots/line	32 x H_f	50/50
768 dots/line	64 x H_f	50/50

NOTE: H_f is the frequency of the input H sync. on Pin 5.

Typically, this clock is fed into an external pulse width modulation module as its clock source. Because of the synchronization between Cout clock and H sync, a better performance on the external PWM controlled functions can be achieved.

FBKG (Pin 20)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 21, 22, 23)

AMOSD II color outputs in TTL level to the host monitor. These three outputs are in high impedance if 3_S bit is set and the color intensity is low. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 24)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141546P2 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the AMOSD II is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the AMOSD II functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{HFLB}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus or SPI bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the HFLB input frequency where the dot clock is equal to 384/768xHFLB in 384/768 modes respectively. In order to have stable operation of M_Bus or SPI bus in the OSD and meet below specifications, HFLB(15k-120k) must be presented and the PLL locks to HFLB properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps.The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the AMOSD II circuitry of MC141546P2, so that the received information can then be displayed.

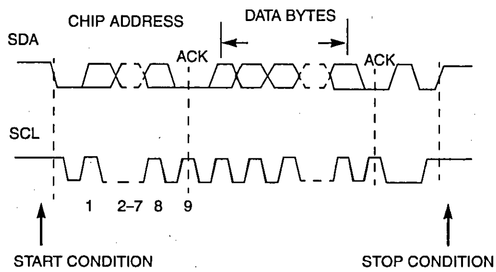


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{SS}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{SS}$ pin low by the master device to enable MC141546P2 to accept data. The $\overline{SS}$ input line must be a logic low prior to occurrence of SCK and remain low until after the last (eighth) SCK cycle. After all data has been sent, the $\overline{SS}$ pin is then pulled high by master to terminate the transmission. Data bit is sent from master to OSD's internal latch during rising edge of SCK and then transmit to internal register during falling edge. Therefore, last falling edge of CLK is needed for proper transmission of last byte data. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

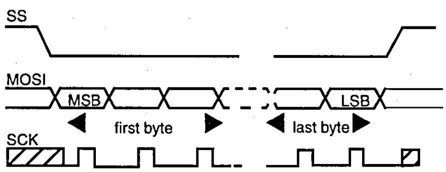


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below. The data train in each sequence consists of row address (R), column address (C), and display information (I), as shown in Figure 4. In format (a), display information data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change which requires a massive information update, or during power up situation, most of the row and column addresses on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the RAM starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

The data transmission formats are:

(a) R – > C– > I –> R – > C – > I – > ....

(b) R – > C – > I – > C – > I – > C – > I.......

(c) R – > C – > I – > I – > I – > ....

To differentiate the row and column addresses when transferring data from master, the MSB (Most Significant Bit) is set as in Figure 5: '1' to represent row, while '0' for column address. Furthermore, to distinguish the column address between format (a), (b) and (c), the sixth bit of the column address is set to '1' which represents format (c), and a '0' for format (a) or (b). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	X	X	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Row & Column Address Bit Patterns

MEMORY MANAGEMENT

Internal RAM are addressed with row and column (coln) number in sequence. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character ROM address corresponding to display location on monitor screen. Every data row associate with two control registers, which locate at coln 30 and 31 of their respective rows, to control the characters display format of that row. In addition, three window control registers for each of three windows together with six frame control registers occupy the first 15 columns of row 15 space. The PWM registers are located from column 20 to 31.

User should handle the internal RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

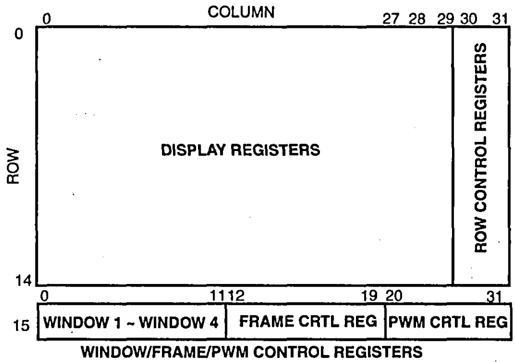


Figure 6. Memory Map

REGISTERS

Display Register

7	6	5	4	3	2	1	0
CCS0	CRADDR						

Bit 7 CCS0 - This bit defines a specific character color out of the two preset colors. Color 1 is selected if this bit is cleared, and color 2 otherwise.

Bit 6-0 CRADDR - This seven bits address the 128 characters or symbols resided in the character ROM.

Row Control Registers

Coln 30

	7	6	5	4	3	2	1	0
COLN 30	R1	G1	B1	R2	G2	B2	CHS	CWS

Bit 7-2 Color 1 is determined by R1, G1, B1 and color 2 by R2, G2, B2. Refer to Table 1 for color selection.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Coln 31

	7	6	5	4	3	2	1	0
COLN 31	R3	G3	B3	R4	G4	B4		

Bit 7-2 Color 3 and 4 are defined by R3, G3, B3, and R4, G4, B4 respectively.

Table 1. The Character/Window Color Selection

	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR (MSB … LSB)					WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 1 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 1 with two extra color selections, making a total of four selection for that row.

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1. The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR (MSB … LSB)					WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 2 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 2 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2. The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 2. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR (MSB … LSB)					WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 3 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 3 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3. The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 3. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	MSB	COL START ADDR			LSB	WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 4 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 4 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	MSB	COL END ADDR			LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 4. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Frame Control Registers

Frame Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
COLN 12	MSB			VERTD				LSB

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Frame Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
COLN 13		MSB		HORD				LSB

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Frame Control Register Coln 14

	7	6	5	4	3	2	1	0
COLN 14			CH5	CH4	CH3	CH2	CH1	CH0

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. AMOSD II adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result. Display character line number is equal to C1 x (18 + C2) where C1 = 1, 2 or 3 defined by CH5-CH4 and C2 = 0-15 defined by CH3-CH0 (BRM).

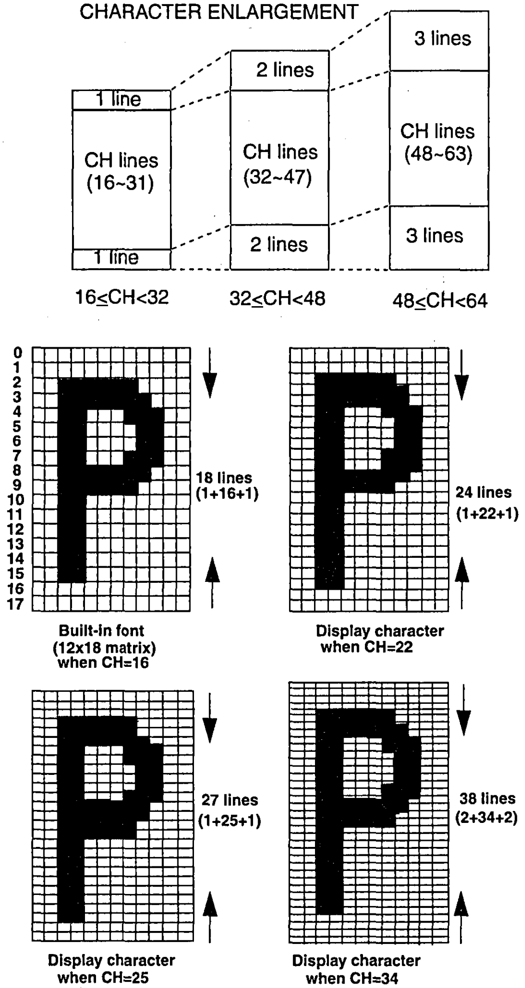


Figure 7. Variable Character Height

Figure 7 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

H = CH + N

Where H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

N = 2 when 16≤CH<32

N = 4 when 32≤CH<48

N = 6 when 48≤CH<64

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW		X32B	3_S		FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 3 X32B - It determines the number of dots per horizontal line. There are 384 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 768 dots per horizontal sync line when bit X32B is set to 1. Please refer to the Table 2 for details.

Table 2. Resolution Setting

X32B	0	1
Dots / Line	**384**	**768**
Resolution	**CGA**	**SVGA**

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity windows which can be implemented by simple external circuit. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
COLN 16				MSB		RSPACE		LSB

Bit 4-0 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on.

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17					HF	TRIC	HPOL	VPOL

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 3 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance. This bit controls gain of internal VCO so that PLL can work for whole range from 15KHz to 120KHz.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{HFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{VFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

Row 15 Col 18 to Col 19

	7	6	5	4	3	2	1	0
ROW 15 COLN 18								

	7	6	5	4	3	2	1	0
ROW 15 COLN 19	Cout							

Bit 7 Cout – When this bit is set to 1,INT/Cout pin will be switched to a clock output which is synchronous to the H sync and used as an external PWM (pulse width modulation) clock source. Refer to the pin description of INT/Cout for more information. After power on, the default value is 0.

PWM Control Registers Row 15 Col 20 to Col 31

	7	6	5	4	3	2	1	0
ROW 15 COLN 20-31	MSB			PWM_n				LSB

Bit 7-0 PWM_n - This eight-bit value decides the output duty cycle and waveforms of PWM. There are maximum 12 channels of PWM. And the corresponding registers are located from column 20 to column 31 respectively on row 15.

The higher five bits (MSB) are used for the conventional PWM and the lower 3 bits (LSB) for the BRM. Please refer to the following figures for more information about BRM algorithm and PWM output waveform.

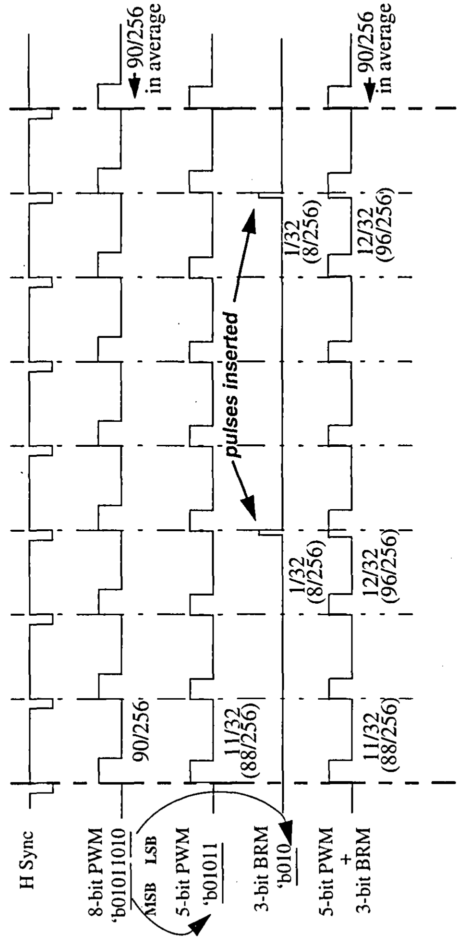


Figure 8. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

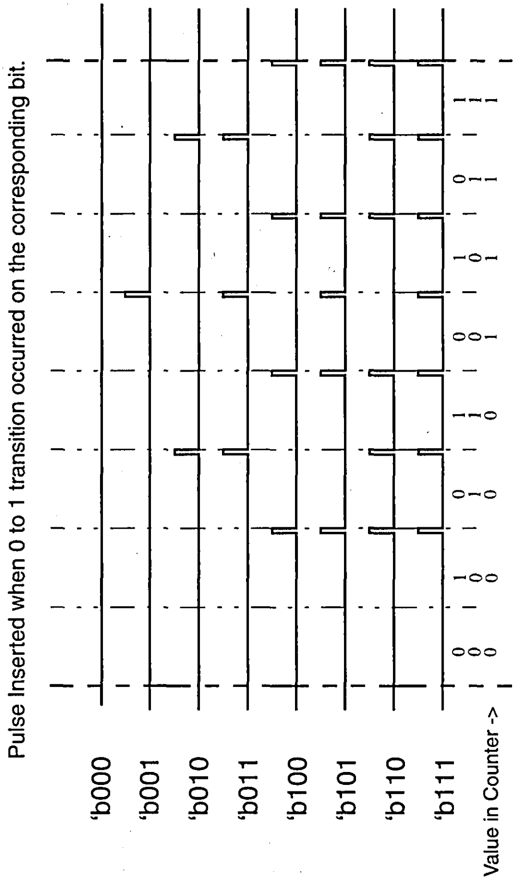


Figure 9. BRM Pulse Insertion Algorithm

Frame Format and Timing

Figure 10 illustrates the relative positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 10 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{\text{HFLB}}$ and $\overline{\text{VFLB}}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Please refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of external charge-up resistor, which is the 1M Ohm resistor in series with 5.6KOhm to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 384 if the bit X32B is clear and H Freq. x 768 if bit X32B is set to 1. For example, dot frequency is 12.288MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1, the dot frequency will be 24.576MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configured each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{\text{VFLB}}$ of next frame to avoid wrapping display characters of the last few rows in current frame into next frame. The number of display dots in a horizontal scan line is always fixed at 360, regardless of row character width and the setting of bit X32B.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 384 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 768 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 11 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters are used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

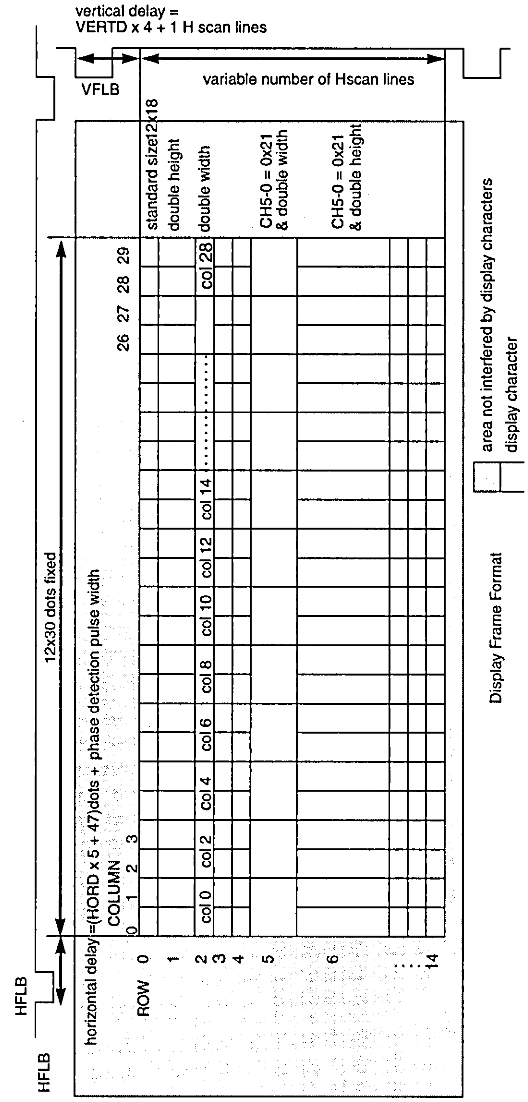


Figure 10. Timing of Output Signals

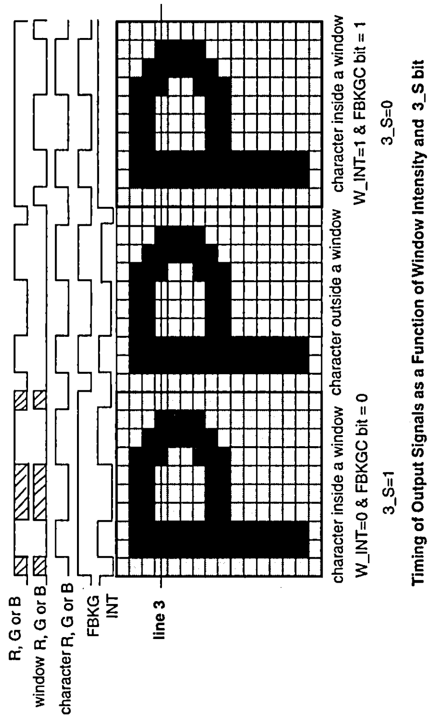


Figure 11. Display Frame Format

A software called AMOSD II FONT EDITOR in IBM PC environment was written for MC141546P2 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141546P2.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 12x18 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 12 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

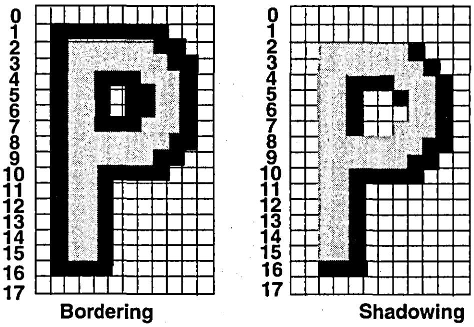


Figure 12. Character Bordering and Shadowing

FONT

Icon Combination

MC141546P2 contains 128 character ROM. The user can create an on-screen menu based on those characters and icons. Refer to Table 3 for icon combinations. Address $00 and $7F are predefined characters. They cannot be modified in any AMOSD II.

Table 3. Combination Map

ICON	ROM ADDRESS(HEX)
ARABIC NUMERALS	01-0A
ALPHABET	0B-26
EUROPEAN	27-41
SYMBOLS	42-61, 7E
GEOMETRY	C5-EE

ROM CONTENT

Figures 13 – 14 show the ROM content of MC141546P2. Mask ROM is optional for custom parts.

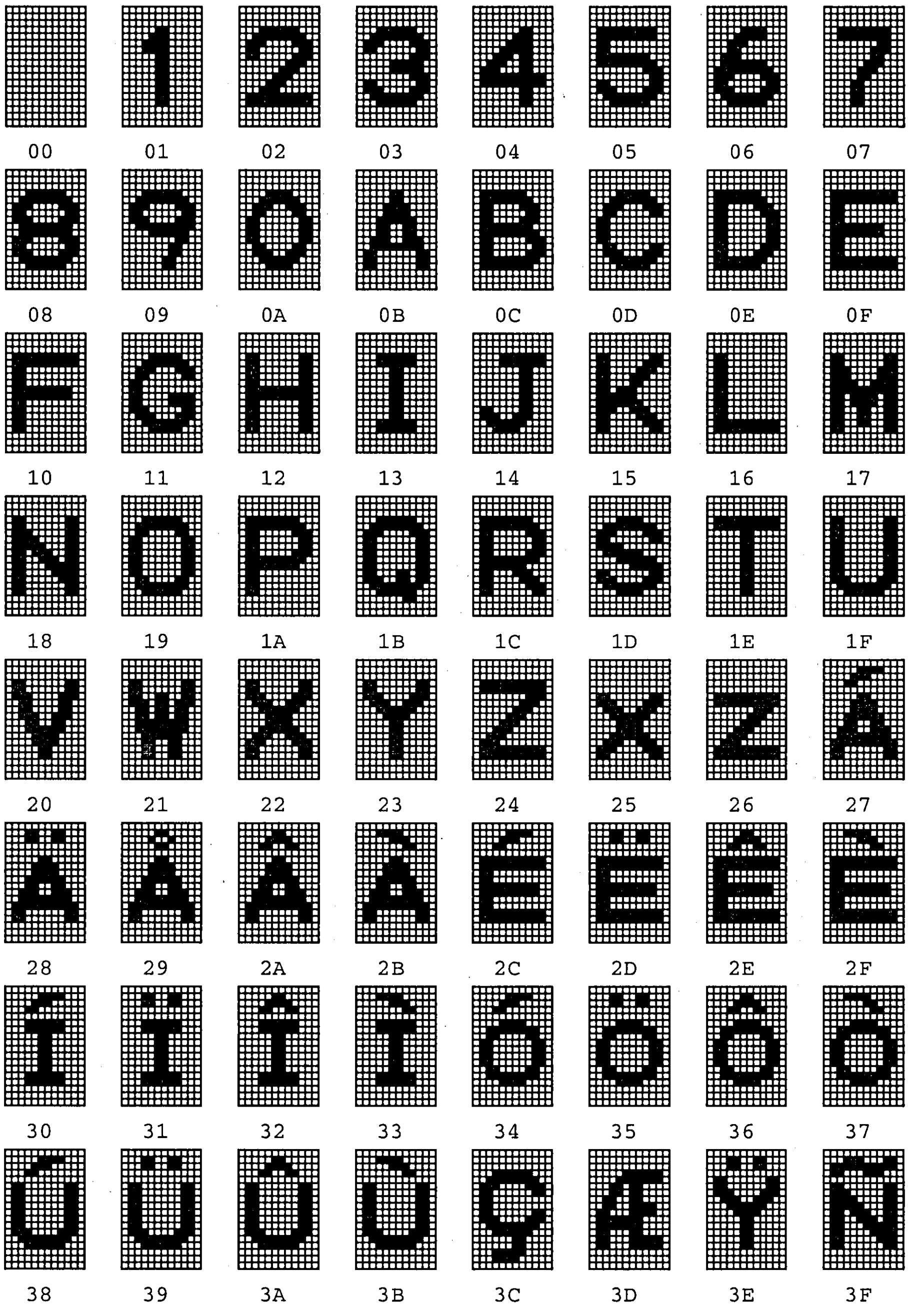


Figure 13. ROM 00 - 3F

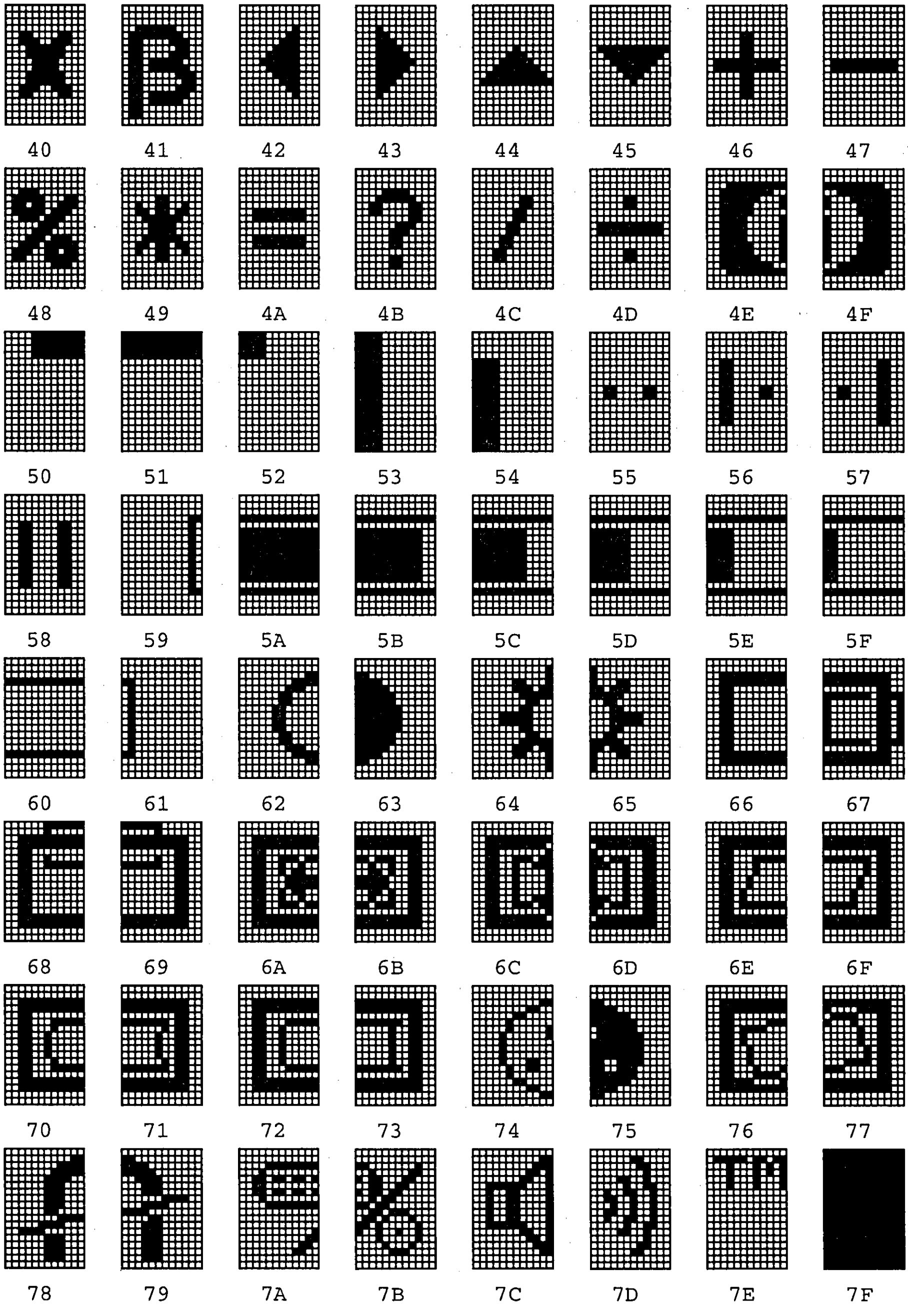


Figure 14. ROM 40 - 7F

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141546P2 has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 384/768 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating outside, they are connected internally). Refer to the Application Diagram for the ground connections.(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be added between Pin1-Pin2 and Pin3-Pin4 to filter VCO noise if necessary. Values should be small enough to avoid picture unlocking caused by temperature variation.

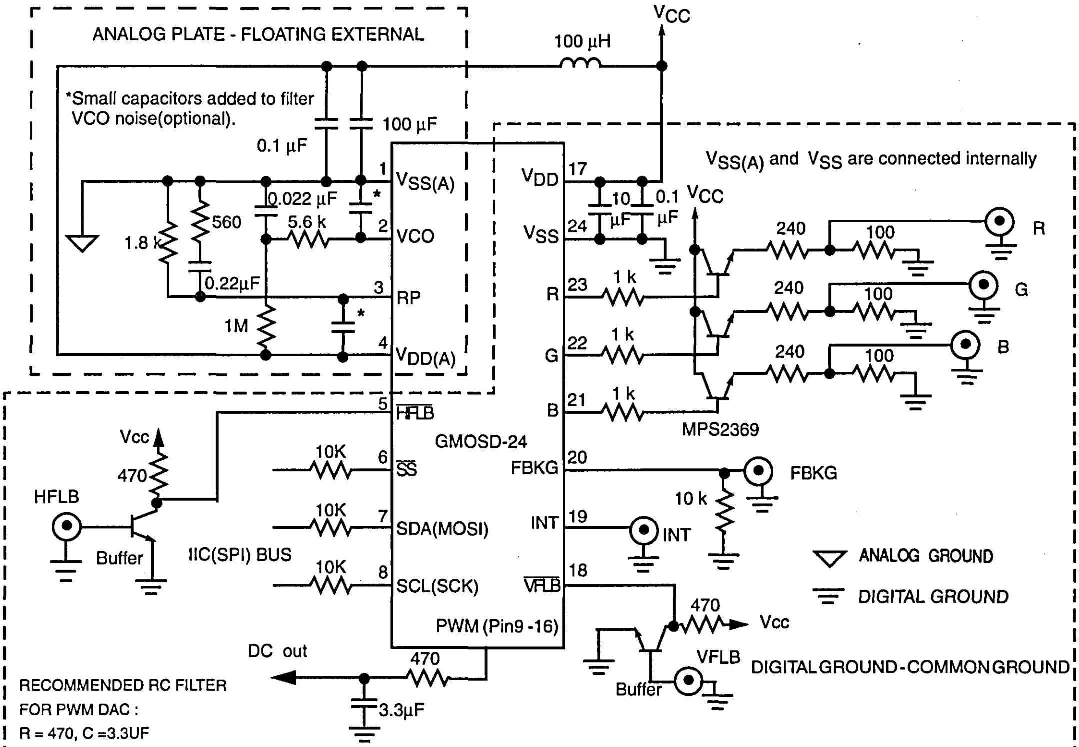
Jittering and Unlocking

Most display jittering and unlocking is caused by HFLB in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both HFLB and VFLB inputs. Refer to the value used in the Application Diagram.

Display Dancing

Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

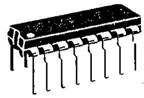
APPLICATION DIAGRAM



Advanced Monitor On-Screen Display II - 16

CMOS

MC141547P2

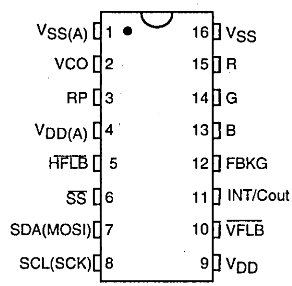


P SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION

MC141547P2 Plastic Dip

PIN ASSIGNMENT



This is a high performance HCMOS device designed to interface with a microcontroller unit to allow colored symbols or characters to be displayed on a color monitor. Its on-chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built-in display and control bytes RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are two different resolutions that users can choose. By changing the number of dots per horizontal line to 384 (CGA) or 768 (VGA), smaller characters with higher resolution can be easily achieved.

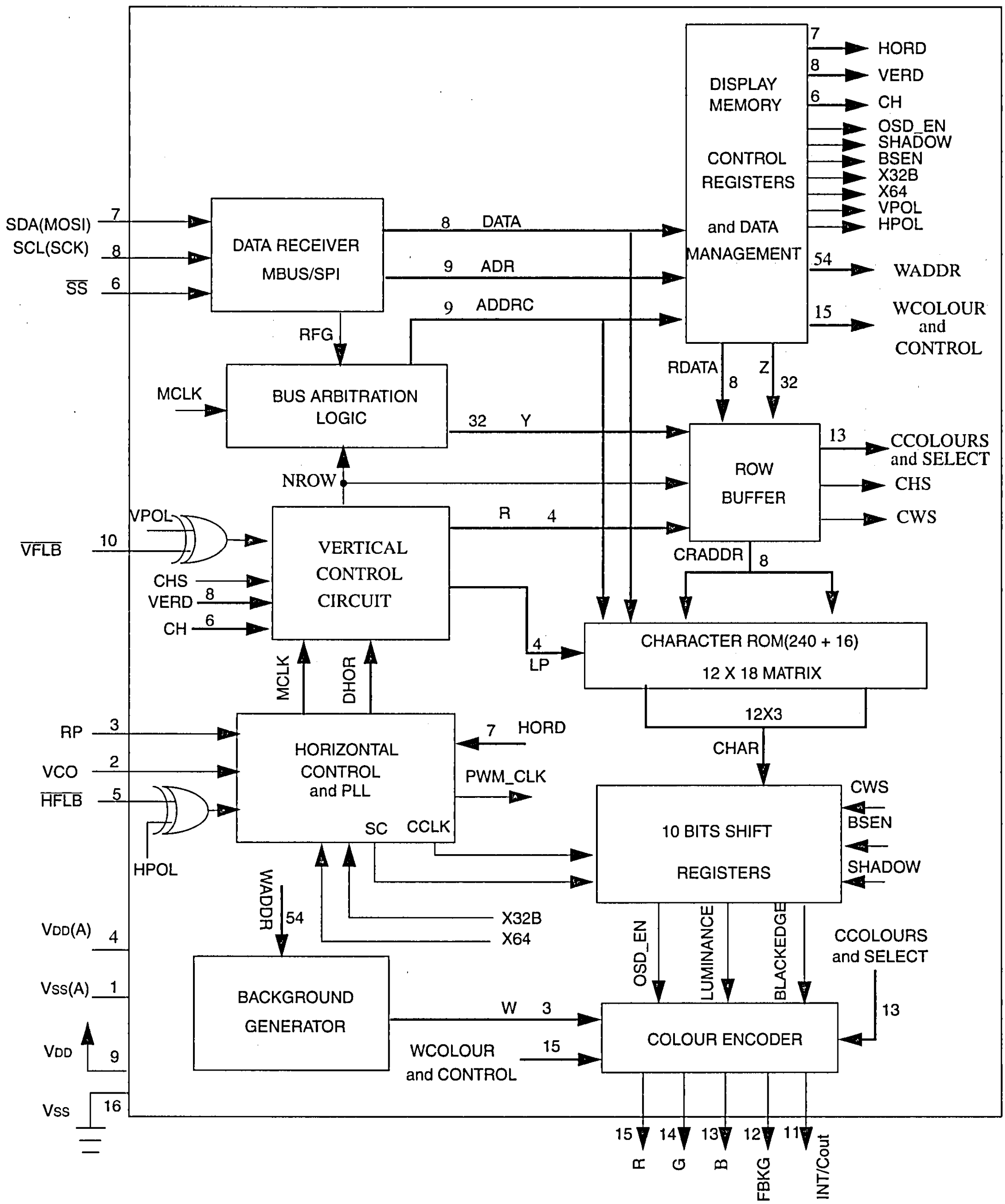
Special functions such as character bordering or shadowing, multi-level windows, intensity control for windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, neither massive information update nor extremely high data transmission rate are expected for normal on- screen display operation and serial protocols are implemented in lieu of any parallel formats to achieve the minimum pin count.

Moreover, the font matrix is improved from 10 by 16 to high resolution font matrix, 12 by 18, in this version. In order to maintain the constant menu height in the different display modes, one special register, controlling the row to row spacing, is implemented to avoid the nonuniform extension of BRM algorithm in character height adjustment.

- Two Resolutions: 384 (CGA) or 768 (VGA) Dots per Line
- 12 x 18 Dot Matrix Character
- Maximum Horizontal Frequency is 120 KHz (92.2MHz Dot Clock at 768 mode)
- Four Fully Programmable Background Windows with Intensity Control
- Row to Row Spacing Register to Manipulate the Constant Menu Height
- Programmable Height of Character to Meet Multi-Sync Requirement
- Smooth Menu Movement by Real Time Programming of H/V Delay Registers
- Fully Programmable Character Array of 15 Rows by 30 Columns
- Internal PLL Generates a Wide-Ranged System Clock
- Programmable Vertical and Horizontal Positioning for Display Center
- 128 Characters and Graphic Symbols ROM (Mask ROM is Optional)
- Character by Character Color Selection
- A Maximum of Four Selectable Colors per Row
- Double Character Height and Double Character Width
- Character Bordering or Shadowing
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

REV 1
4/97

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT/Cout) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	15K	—	120K	Hz

Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{il}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	μA
I_{il}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	μA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 20	mA

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configured as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

V_{DD} (Pin 9)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT/ Cout (Pin 11)

This is a multiplexed pin. When the Cout bit is cleared after power on or by the MCU, this pin is INT and this output pin is used to indicate the color intensity. If the associated window intensity control bits are set, this pin will output a logic high while displaying the specified windows. Otherwise, it will keep in low state. Only the windows have the color intensity selection and all displayed characters or symbols are all high intensity. It means that INT pin must be driven high while displaying the characters or symbols.

Please refer to the timing figure for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs for windows' color control. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

If the Cout bit is set to 1 via M_BUS or SPI, this pin is changed to a mode-dependent clock output with 50/50 duty cycle and synchronous with the input horizontal synchronization signal at Pin 5. The frequency is dependent on the mode in which the AMOSD II is currently running. The exact frequencies in the different resolution modes are described below.

Resolution	Frequency	Duty Cycle
384 dots/line	32 x H_f	50/50
768 dots/line	64 x H_f	50/50

NOTE: H_f is the frequency of the input H sync. on Pin 5.

Typically, this clock is fed into an external pulse width modulation module as its clock source. Because of the synchronization between Cout clock and H sync, a better performance on the external PWM controlled functions can be achieved.

FBKG (Pin 12)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13, 14, 15)

AMOSD II color outputs in TTL level to the host monitor. These three outputs are in high impedance if 3_S bit is set and the color intensity is low. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141547P2 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the AMOSD II is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the AMOSD II functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{\text{HFLB}}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus or SPI bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the HFLB input frequency where the dot clock is equal to 384/768xHFLB in 384/768 modes respectively. In order to have stable operation of M_Bus or SPI bus in the OSD and meet below specifications, HFLB(15k-120k) must be presented and the PLL locks to HFLB properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps. The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the AMOSD II circuitry of MC141547P2, so that the received information can then be displayed.

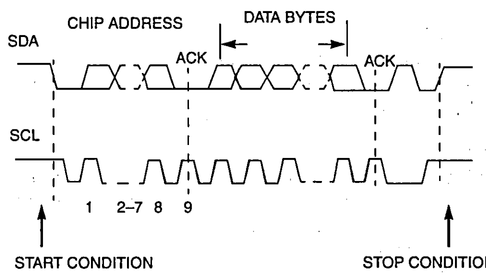


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{SS}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{SS}$ pin low by the master device to enable MC141547P2 to accept data. The $\overline{SS}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{SS}$ pin is then pulled high by master to terminate the transmission. Data bit is sent from master to OSD's internal latch during rising edge of SCK and then transmit to internal register during falling edge. Therefore, last falling edge of CLK is needed for proper transmission of last byte data. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

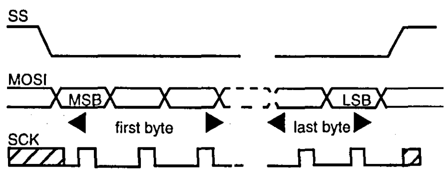


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below. The data train in each sequence consists of row address (R), column address (C), and display information (I), as shown in Figure 4. In format (a), display information data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change which requires a massive information update, or during power up situation, most of the row and column addresses on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the RAM starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

The data transmission formats are:

(a) R – > C– > I –> R – > C – > I – > ....

(b) R – > C – > I – > C – > I – > C – > I.......

(c) R – > C – > I – > I – > I – > ....

To differentiate the row and column addresses when transferring data from master, the MSB (Most Significant Bit) is set as in Figure 5: '1' to represent row, while '0' for column address. Furthermore, to distinguish the column address between format (a), (b) and (c), the sixth bit of the column address is set to '1' which represents format (c), and a '0' for format (a) or (b). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet

ADDRESS	7	6	5	4	3	2	1	0	FORMAT
ROW	1	X	X	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Row & Column Address Bit Patterns

MEMORY MANAGEMENT

Internal RAM are addressed with row and column (coln) number in sequence. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character ROM address corresponding to display location on monitor screen. Every data row associate with two control registers, which locate at coln 30 and 31 of their respective rows, to control the characters display format of that row. In addition, three window control registers for each of three windows together with six frame control registers occupy the first 15 columns of row 15 space. The PWM registers are located from column 20 to 31.

User should handle the internal RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

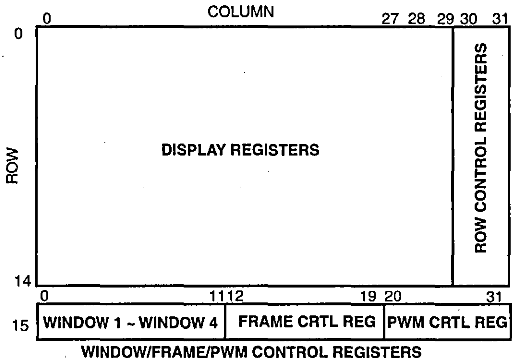


Figure 6. Memory Map

REGISTERS

Display Register

7	6	5	4	3	2	1	0
CCS0							
	CRADDR						

Bit 7 CCS0 - This bit defines a specific character color out of the two preset colors. Color 1 is selected if this bit is cleared, and color 2 otherwise.

Bit 6-0 CRADDR - This seven bits address the 128 characters or symbols resided in the character ROM.

Row Control Registers

Coln 30

	7	6	5	4	3	2	1	0
COLN 30	R1	G1	B1	R2	G2	B2	CHS	CWS

Bit 7-2 Color 1 is determined by R1, G1, B1 and color 2 by R2, G2, B2. Refer to Table 1 for color selection.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Coln 31

	7	6	5	4	3	2	1	0
COLN 31	R3	G3	B3	R4	G4	B4		

Bit 7-2 Color 3 and 4 are defined by R3, G3, B3, and R4, G4, B4 respectively.

Table 1. The Character/Window Color Selection

	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR (MSB … LSB)					WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 1 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 1 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1. The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one,

and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR MSB				LSB	WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 2 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 2 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2. The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 2. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR MSB				LSB	WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 3 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 3 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 3. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	COL START ADDR MSB				LSB	WEN	CCS1	W_INT

Bit 2 WEN - It enables the background window 4 generation if this bit is set.

Bit 1 CCS1 - This additional color select bit provides the characters resided within window 4 with two extra color selections, making a total of four selection for that row

Bit 0 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	COL END ADDR (MSB … LSB)					R	G	B

Bit 2-0 R, G and B - Controls the color of window 4. Refer to Table 1 for color selection. Window 1 Registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Frame Control Registers

Frame Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
COLN 12	VERTD (MSB … LSB)							

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Frame Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
COLN 13		HORD (MSB … LSB)						

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Frame Control Register Coln 14

	7	6	5	4	3	2	1	0
COLN 14			CH5	CH4	CH3	CH2	CH1	CH0

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. AMOSD II adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result. Display character line number is equal to C1 x (18 + C2) where C1 = 1, 2 or 3 defined by CH5-CH4 and C2 = 0-15 defined by CH3-CH0 (BRM).

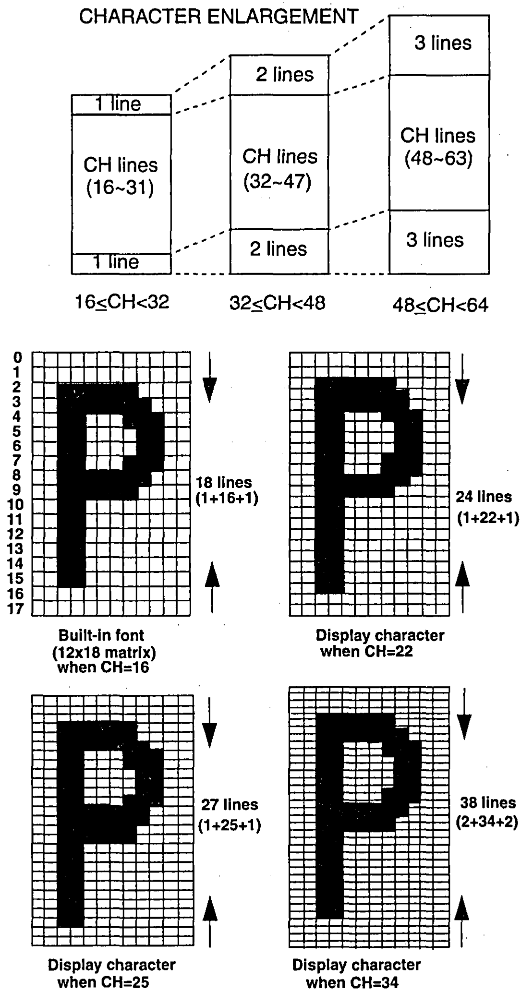


Figure 7. Variable Character Height

Figure 7 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

$H = CH + N$

Where H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

$N = 2$ when $16 \leq CH < 32$

$N = 4$ when $32 \leq CH < 48$

$N = 6$ when $48 \leq CH < 64$

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW		X32B	3_S		FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 3 X32B - It determines the number of dots per horizontal line. There are 384 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 768 dots per horizontal sync line when bit X32B is set to 1. Please refer to the Table 2 for details.

Table 2. Resolution Setting

X32B	0	1
Dots / Line	384	768
Resolution	CGA	SVGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity windows which can be implemented by simple external circuit. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
COLN 16				MSB		RSPACE		LSB

Bit 4-0 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on.

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17					HF	TRIC	HPOL	VPOL

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 3 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance. This bit controls gain of internal VCO so that PLL can work for whole range from 15KHz to 120KHz.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{HFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{VFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

Row 15 Col 18 to Col 19

	7	6	5	4	3	2	1	0
ROW 15 COLN 18								

	7	6	5	4	3	2	1	0
ROW 15 COLN 19	Cout							

Bit 7 Cout – When this bit is set to 1,INT/Cout pin will be switched to a clock output which is synchronous to the H sync and used as an external PWM (pulse width modulation) clock source. Refer to the pin description of INT/Cout for more information. After power on, the default value is 0.

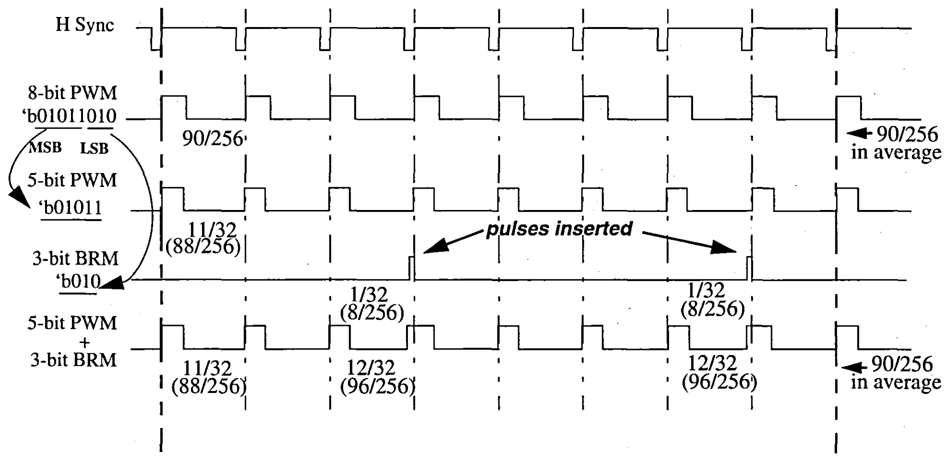


Figure 8. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

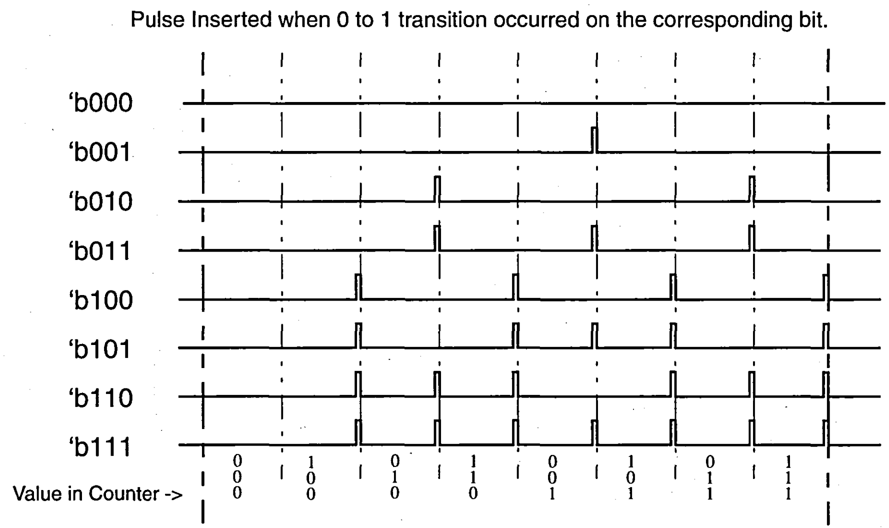


Figure 9. BRM Pulse Insertion Algorithm

Frame Format and Timing

Figure 10 illustrates the relative positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 10 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{HFLB}$ and $\overline{VFLB}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Please refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of external charge-up resistor, which is the 1MOhm resistor in series with 5.6KOhm to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 384 if the bit X32B is clear and H Freq. x 768 if bit X32B is set to 1. For example, dot frequency is 12.288MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1, the dot frequency will be 24.576MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configured each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{VFLB}$ of next frame to avoid wrapping display characters of the last few rows in current frame into next frame. The number of display dots in a horizontal scan line is always fixed at 360, regardless of row character width and the setting of bit X32B.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 384 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 576 dots and 768 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 11 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters are used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

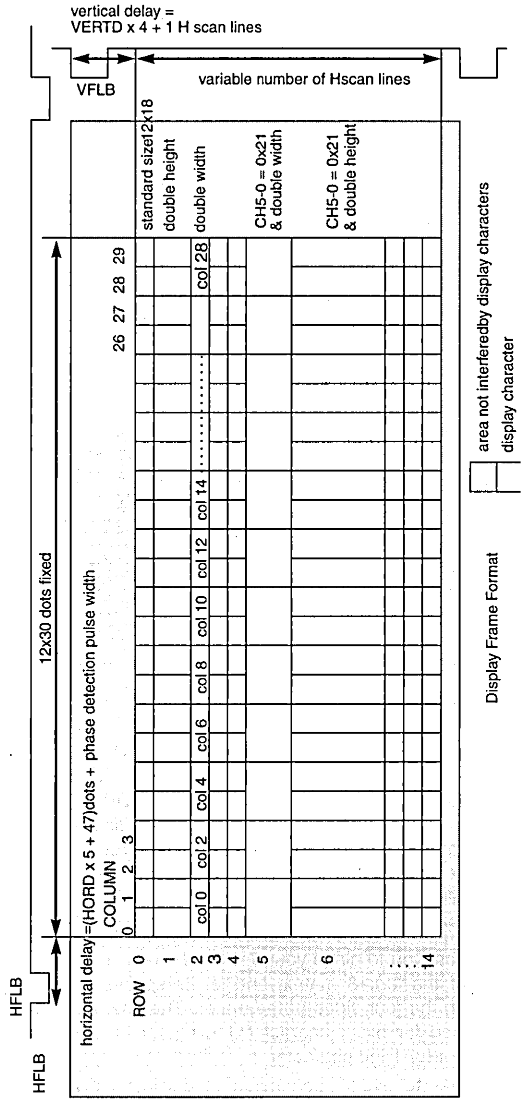


Figure 10. Timing of Output Signals

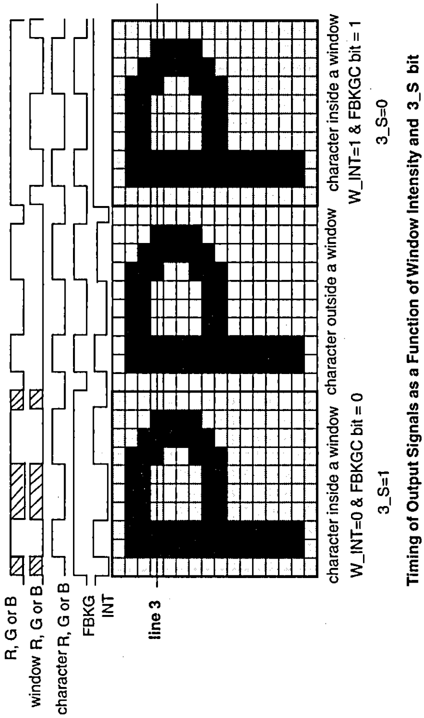


Figure 11. Display Frame Format

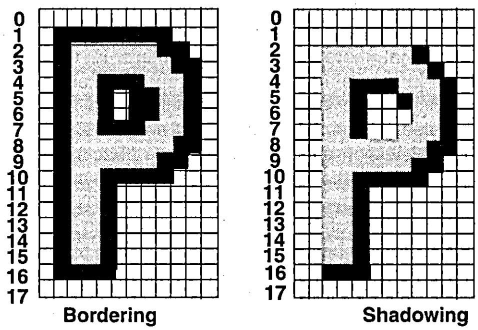


Figure 12. Character Bordering and Shadowing

A software called AMOSD II FONT EDITOR in IBM PC environment was written for MC141547P2 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141547P2.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 12x18 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 12 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

FONT

Icon Combination

MC141547P2 contains 128 character ROM. The user can create an on-screen menu based on those characters and icons. Refer to Table 3 for icon combinations. Address $00 and $7F are predefined characters. They cannot be modified in any AMOSD II.

Table 3. Combination Map

ICON	ROM ADDRESS(HEX)
ARABIC NUMERALS	01-0A
ALPHABET	0B-26
EUROPEAN	27-41
SYMBOLS	42-61, 7E
GEOMETRY	C5-EE

ROM CONTENT

Figures 13 – 14 show the ROM content of MC141547P2. Mask ROM is optional for custom parts.

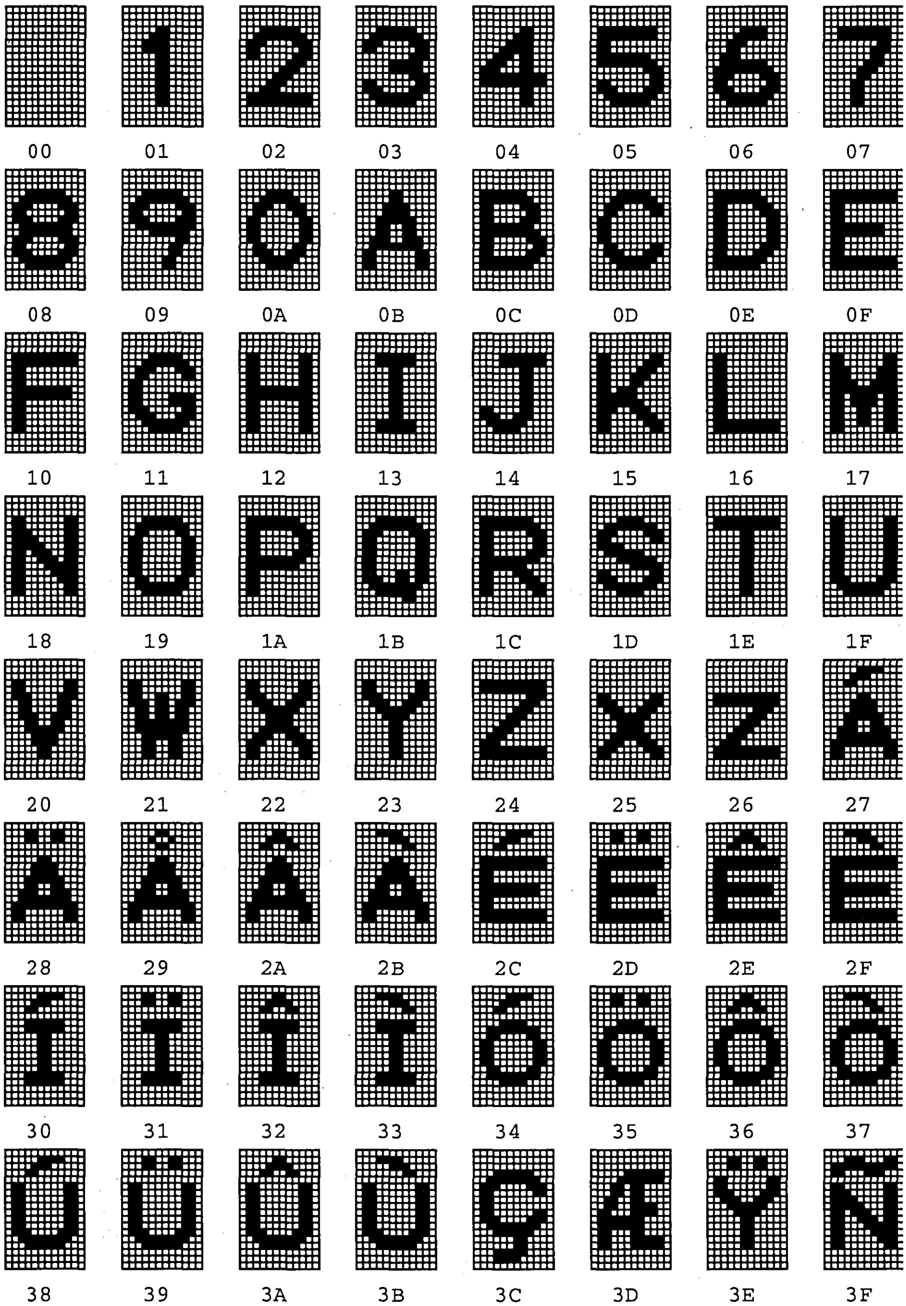


Figure 13. ROM 00 - 3F

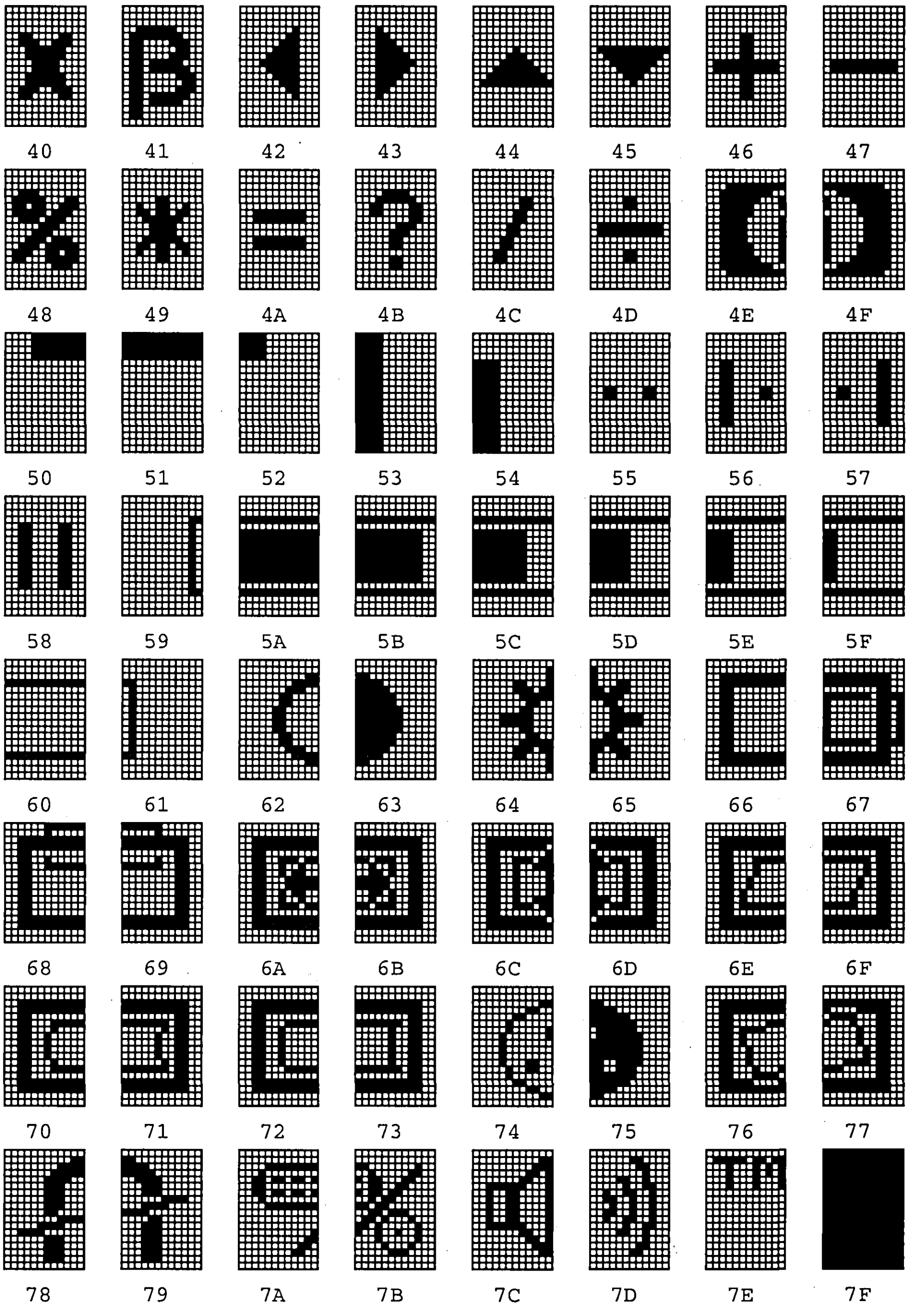


Figure 14. ROM 40 - 7F

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141547P2 has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 384/768 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating outside, they are connected internally). Refer to the Application Diagram for the ground connections.(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be added between Pin1-Pin2 and Pin3-Pin4 to filter VCO noise if necessary. Values should be small enough to avoid picture unlocking caused by temperature variation.

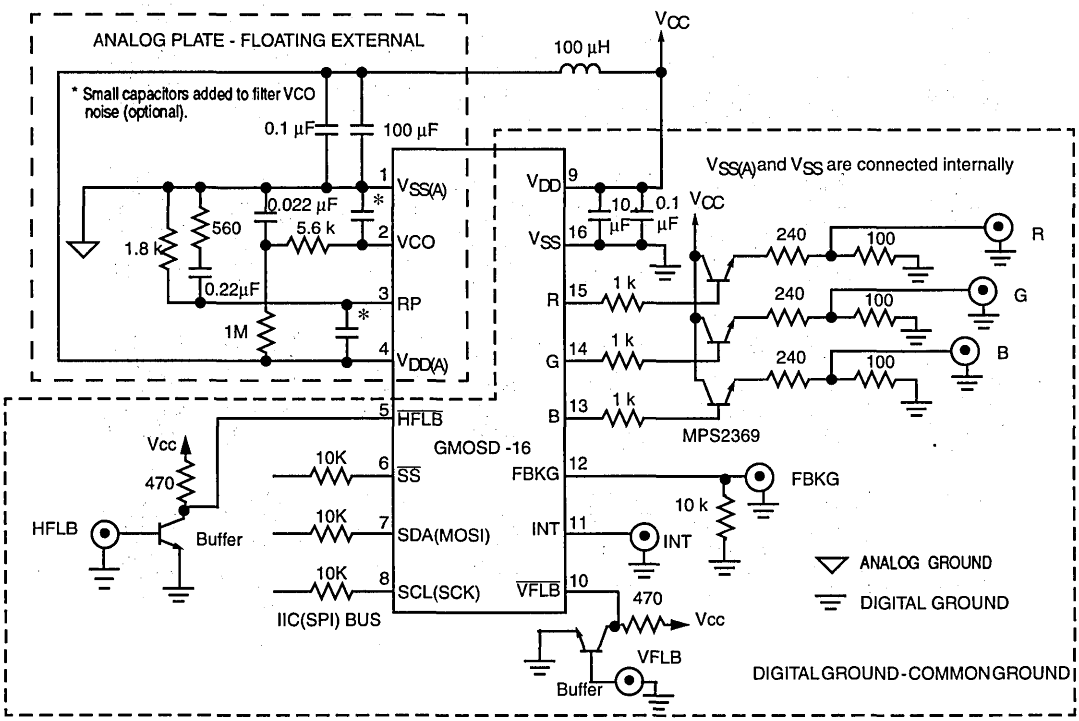
Jittering and Unlocking

Most display jittering and unlocking is caused by HFLB in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both HFLB and VFLB inputs. Refer to the value used in the Application Diagram.

Display Dancing

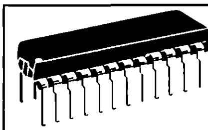
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



Graphic Monitor On-Screen Display - 24
CMOS

MC141542P2



P SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

MC141542P2 Plastic Dip

This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto CRT monitor. Because of the large number of fonts, 256 fonts including 240 standard fonts and 16 multi-color fonts, GMOSD-24 is suitable to be adopted for the multi-language monitor application especially. Its on-chip PLL allows both multiscan operation and self generation of system timing. It also minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are two kinds of resolutions that users can choose. By changing the number of dots per horizontal line to 384 (CGA) or 768 (SVGA), smaller characters with higher resolution can be easily achieved. The full OSD menu is formed of 15 rows x 30 columns which can by freely positioned on anywhere of the monitor screen by changing vertical or horizontal delay.

There are 8 PWM DAC channels for external digital to analog control. Each PWM DAC channel is composed of an 8 bit register which contains a 5 bit PWM in MSB portion and a 3 bit binary rate multiplier (BRM) in LSB portion.

Special functions such as character background color, blinking, bordering or shadowing, four-level windows with programmable shadowing, row double height and double width, programmable vertical height of character and row-to-row spacing, and full-screen erasing and Fade-In/Fade-Out are also incorporated. There are 8 color selections for any individual character display with row intensity attribute and window intensity attribute to expand the color mixture on OSD menu.

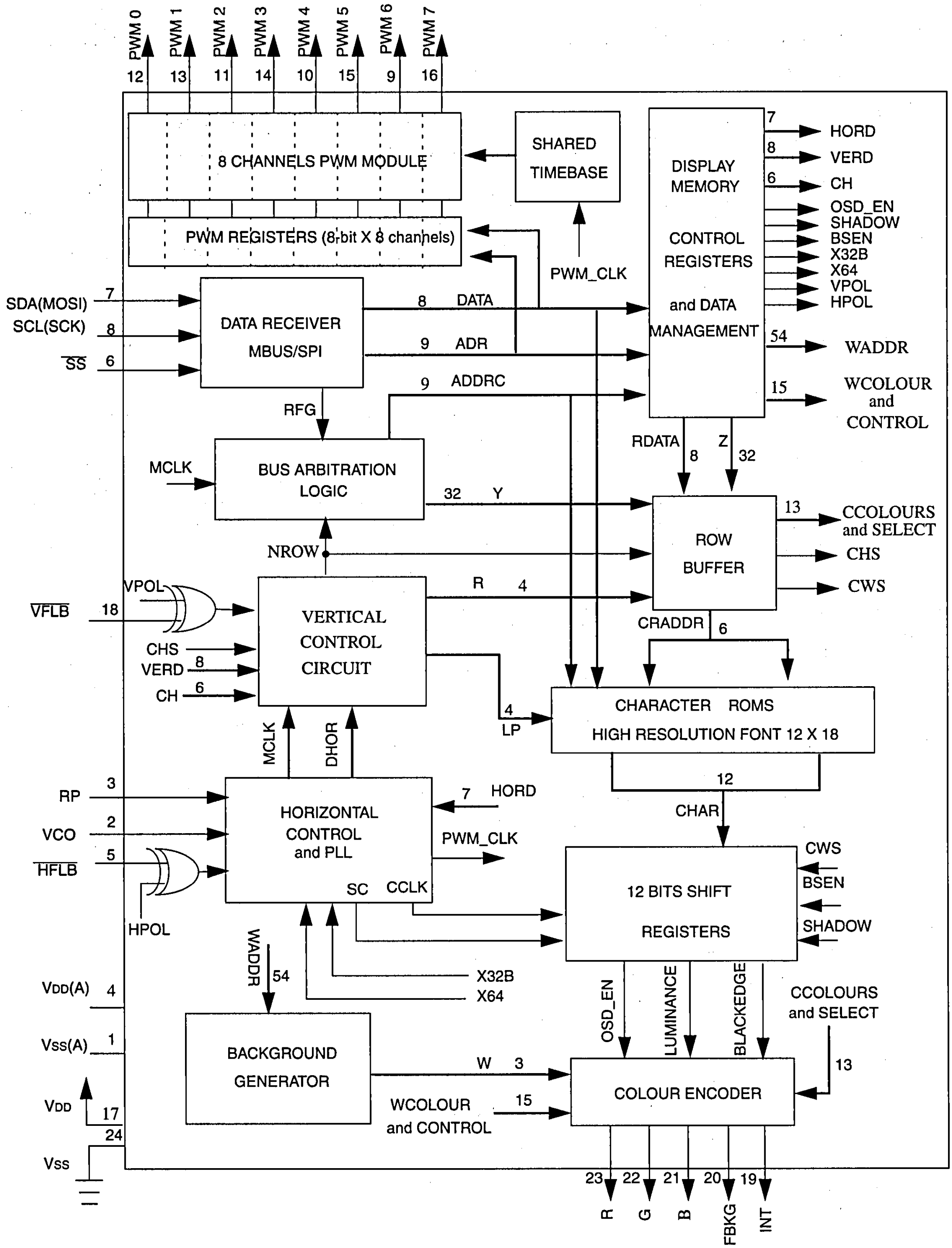
- 8 Channels 8-bit Synchronous PWM DAC with Push-Pull Output
- Totally 256 Fonts Including 240 Standard Fonts and 16 Multi-Color Fonts.
- Two Resolutions: 384 (CGA) or 768 (SVGA) Dots/Line
- Wide Operating Frequency Range for High End Monitor: 15KHz ~ 120KHz
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- 7-Color Selection for Characters background
- True 16-Color Selection for Windows
- Fancy Fade-In/Fade-Out Effects
- Programmable Height of Character to Meet Multi-Sync Requirement
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Shadowing on Windows with Programmable Shadow Width/Height
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
- Programmable Vertical and Horizontal Positioning for Display Centre
- Double Character Height and Double Character Width
- Internal PLL Generates a Wide-Ranged System Clock (92.2 MHz)
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

PIN ASSIGNMENT

$V_{SS(A)}$	1	24	V_{SS}
VCO	2	23	R
RP	3	22	G
$V_{DD(A)}$	4	21	B
$\overline{HFLB}$	5	20	FBKG
$\overline{SS}$	6	19	INT
SDA(MOSI)	7	18	$\overline{VFLB}$
SCL(SCK)	8	17	V_{DD}
PWM 6	9	16	PWM 7
PWM 4	10	15	PWM 5
PWM 2	11	14	PWM 3
PWM 0	12	13	PWM 1

REV 1
4/97

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
	Output Signal (PWM0 - PWM7) C_{load} = 30 pF				
t_r	Rise Time	—	—	20	ns
t_f	Fall Time	—	—	20	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	15K	—	120K	Hz

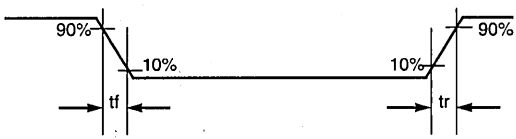


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{Il}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{Il}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output) at V_{DD}=5.0V	—	—	+ 26	mA
LVI	Low Voltage Inhibit for PWM DAC Output	2.7	3.2	3.6	V

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

PWM 6 (Pin 9)

Channel 6 of the PWM.

PWM 4 (Pin 10)

Channel 4 of the PWM.

PWM 2 (Pin 11)

Channel 2 of the PWM.

PWM 0 (Pin 12)

Channel 0 of the PWM.

PWM 1 (Pin 13)

Channel 1 of the PWM.

PWM 3 (Pin 14)

Channel 3 of the PWM.

PWM 5 (Pin 15)

Channel 5 of the PWM.

PWM 7 (Pin 16)

Channel 7 of the PWM.

V_{DD} (Pin 17)

This is the power pin for the digital logic of the chip.

$\overline{VFLB}$ (Pin 18)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT (Pin 19)

This output pin is used to indicate the color intensity. If the intensity control bits are set in the row attribute registers or window control registers, this pin will output a logic high while displaying the specified windows or the characters on the associated rows. Otherwise, it will keep in low state. Please refer to Figure 15 for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

FBKG (Pin 20)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 21, 22, 23)

GMOSD-24 color outputs in TTL level to the host monitor. These three signals are open drain outputs if 3_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 24)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141542P2 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the GMOSD-24 is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the GMOSD-24 functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{HFLB}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus or SPI bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the HFLB input frequency where the dot clock is equal to 384/768xHFLB in 384/768 modes respectively. In order to have stable operation of M_Bus or SPI bus in the OSD and meet below specifications, HFLB(15k-120k) must be presented and the PLL locks to HFLB properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps.The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the GMOSD-24 circuitry of MC141542P2, so that the received information can then be displayed.

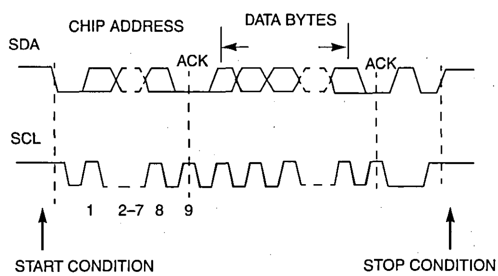


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{SS}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{SS}$ pin low by the master device to enable MC141542P2 to accept data. The $\overline{SS}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{SS}$ pin is then pulled high by master to terminate the transmission. Data bit is sent from master to OSD's internal latch during rising edge of SCK and then transmit to internal register during falling edge. Therefore, last falling edge of CLK is needed for proper transmission of last byte data. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

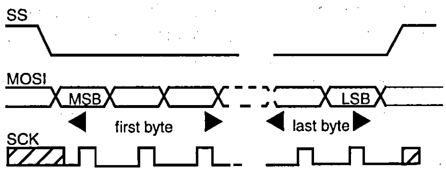


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, two register blocks, display registers, attribute/control registers, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:

(a) R - > C- > I -> R - > C - > I - > ....

(b) R - > C - > I - > C - > I - > C - > I.......

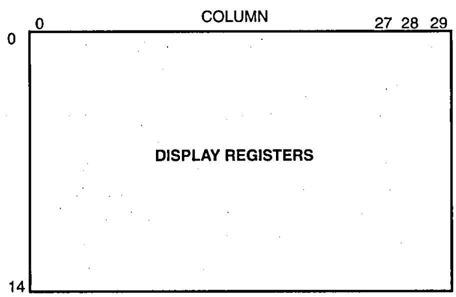
(c) R - > C - > I - > I - > I - > ....

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the display row address from attribute area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet for Display Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care   D: valid data

Figure 5. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:

(a) R - > C- > I -> R - > C - > I - > ....

(b) R - > C - > I - > C - > I - > C - > I.......

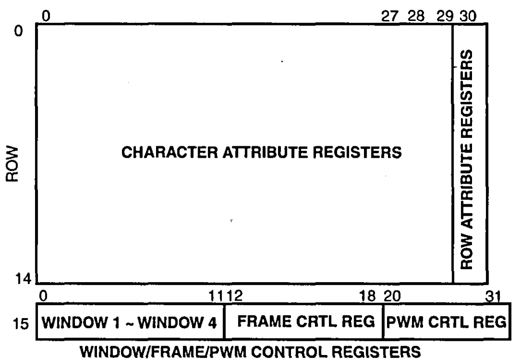
(c) R - > C - > I - > I - > I - > ....

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 6. Data Packet for Attribute/Control Data



ADDRESS	7	6	5	4	3	2	1	0	FORMAT
ROW	1	0	1	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 7. Address Bit Patterns for Attribute/Control Data

MEMORY MANAGEMENT

All the internal programmable area can be divided into two parts including (1) Display Registers (2) Attribute/Control Registers. Please refer to the following two figures for the corresponding memory map.

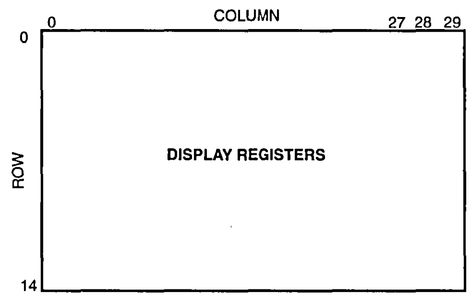


Figure 8. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 ROM fonts.

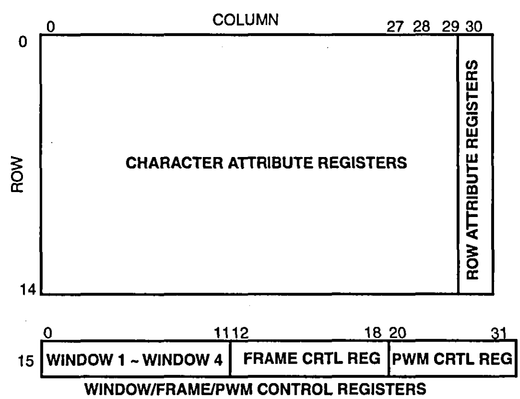


Figure 9. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color and 3-bit to define its background. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. as well as background. Every data row associate with one attribute register, which locate at coln 30 of their respective rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control, frame function control and PWM registers. Four window control registers for each of four windows together with four frame control registers and twelve PWM registers occupy the first 28 columns of row 15 space. These control registers will be described on the "REGISTERS" section.

User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

REGISTERS

(I) Display Register

Display Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
← CRADDR →							

Bit 7-0 CRADDR - This eight bits address one of the 256 characters or symbols resided in the character ROM fonts.

(II) Attribute/Window/Control/Frame Registers

Character Attribute Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
	BGR	BGG	BGB	BLINK	R	G	B

Bit 6-4 These three bits define the color of the background for the correspondent characters. If all three bits are clear, no background will be shown(transparent). Therefore, total seven background colors can be selected.

Bit 3 BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

Bit 2-0 These three bits are the color attribute to define the color of the associated character/symbol.

Table 1. The Character/Window Color Selection

	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Row Attribute Register (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
					R_INT	CHS	CWS

Bit 2 R_INT - Row intensity bit controls the color intensity of the displayed character/symbol on the corresponding row. Setting this bit to 1 means high intensity color and the INT pin will go high while displaying the characters of this row.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

Row 15 Coln 1

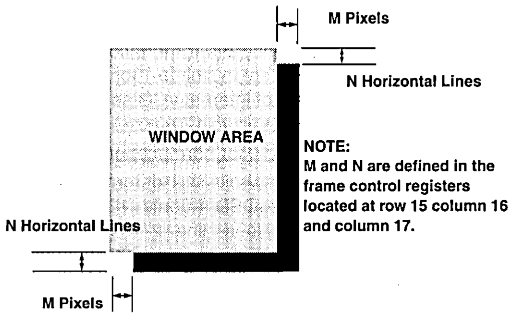
	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR (MSB … LSB)					WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 1 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1. The default value is

1 to indicate high intensity..Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output black shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17. See the following figure and the related frame control register for detail.



Window Shadowing

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 2 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 2 shadowing.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 2.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 3 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 3 shadowing.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 3.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one,

and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 4 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 4.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
ROW 15 COLN 12	VERTD MSB							LSB

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
ROW 15 COLN 13	CLR	HORD MSB						LSB

Bit 7 CLR - Setting this bit to 1 clear all display register from Row 0 to Row 14; Control register will not be erased.

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Character Height Control Register Row 15 Coln 14

	7	6	5	4	3	2	1	0
ROW 15 COLN 14	HF	O	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance. This bit controls gain of internal VCO so that PLL can work for whole range from 15KHz to 120KHz.

Bit 6 Bit reserved. Set to 0 for normal operation.

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. GMOSD adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result. Display character line number is equal to C1 x (18 + C2) where C1 = 1, 2 or 3 defined by CH5-CH4 and C2 = 0-15 defined by CH3-CH0 (BRM).

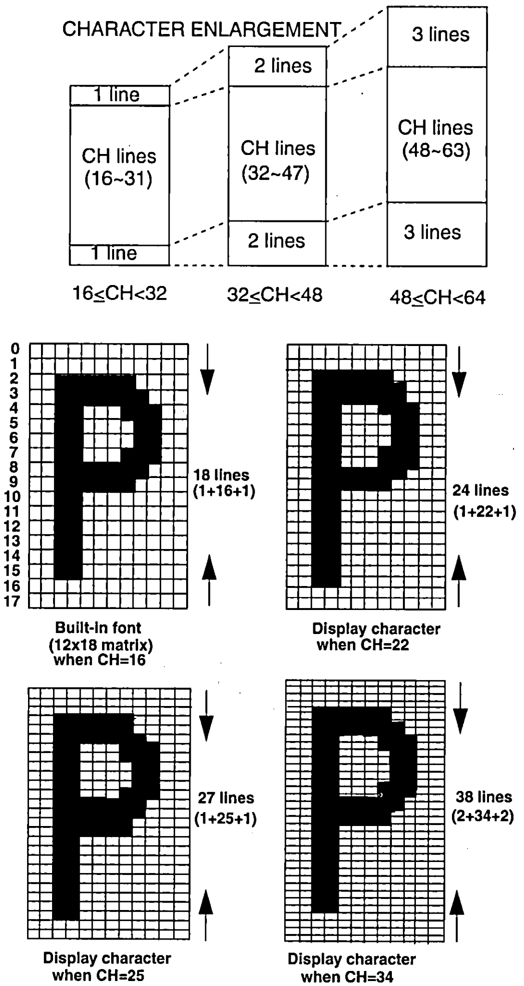


Figure 10. Variable Character Height

Figure 10 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

$H = CH + N$

Where H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

$N = 2$ when $16 \le CH < 32$

$N = 4$ when $32 \le CH < 48$

$N = 6$ when $48 \le CH < 64$

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW		X32B	3_S	FAN	FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 3 X32B - It determines the number of dots per horizontal line. There are 384 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 768 dots per horizontal sync line when bit X32B is set to 1. Please refer to the Table 2 for details.

Table 2. Resolution Setting

X32B	0	1
Dots / Line	384	768
Resolution	CGA	SVGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of characters or windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity characters or windows. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 1 FAN - It enables the fan-in/fan-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

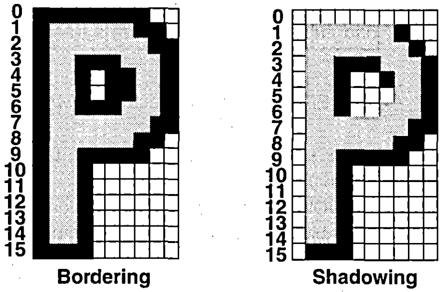
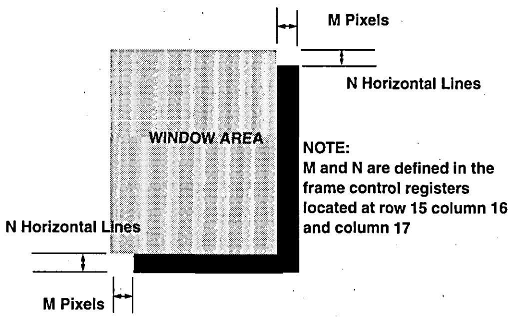


Figure 11. Character Bordering and Shadowing



Window Shadowing

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
ROW 15 COLN 16	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 3. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 4. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

	7	6	5	4	3	2	1	0
ROW 15 COLN 18	MSB		RSPACE		LSB	TRIC	HPOL	VPOL

Bit 7-3 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on. It can be used for Portrait monitor too when icon design is rotated 90 degree.

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{HFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{VFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

- **NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.**

PWM Control Registers Row 15 Col 20 to Col 31

	7	6	5	4	3	2	1	0
ROW 15 COLN 20-31	MSB			PWM_n				LSB

Bit 7-0 PWM_n - This eight-bit value decides the output duty cycle and waveforms of PWM. There are maximum 12 channels of PWM. And the corresponding registers are located from column 20 to column 31 respectively on row 15.

The higher five bits (MSB) are used for the conventional PWM and the lower 3 bits (LSB) for the BRM. Please refer to the following figures for more information about BRM algorithm and PWM output waveform.

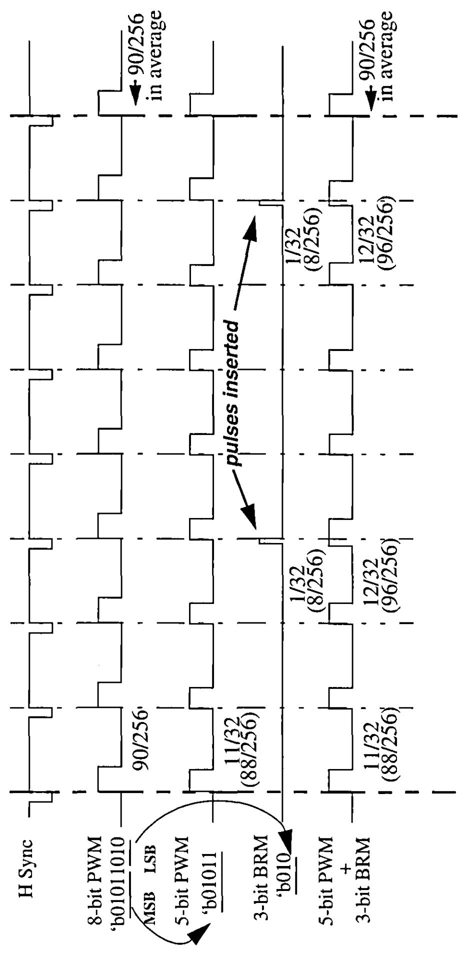


Figure 12. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

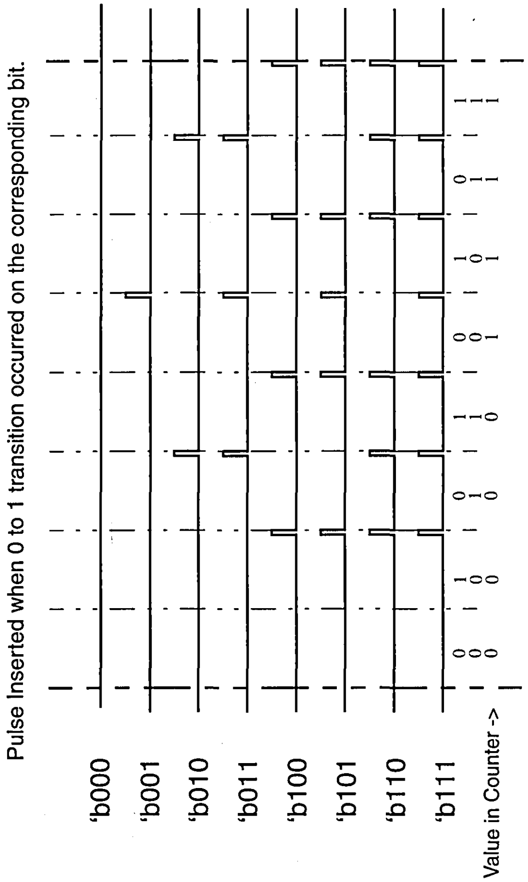


Figure 13. BRM Pulse Insertion Algorithm

A software called GMOSD-24 FONT EDITOR in IBM PC environment was written for MC141542P2 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141542P2.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 12x18 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 11 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

Frame Format and Timing

Figure 14 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 14 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{\text{HFLB}}$ and $\overline{\text{VFLB}}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge-up resistor, which is the 1MΩ resistor in a series with 5.6 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 384 if the bit X32B is clear and H Freq. x 768 if bit X32B is set to 1. For example, dot frequency is 12.28 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1, the dot frequency will be 24.57 MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{\text{VFLB}}$ of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 360, regardless of row character width and the setting of bit X32B.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 384 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 768 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 15 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

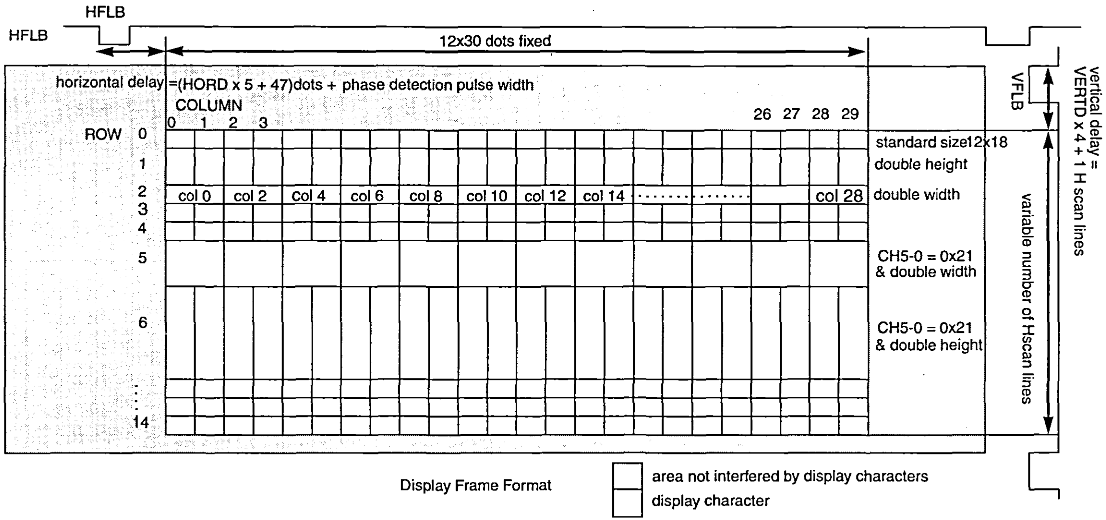
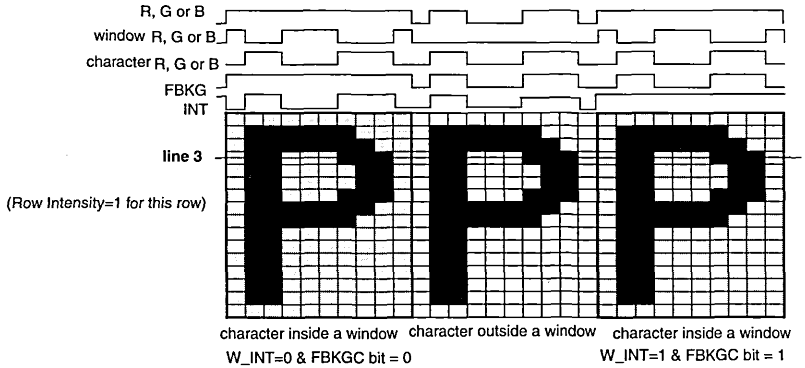


Figure 14. Display Frame Format



Timing of Output Signals as a Function of Window, FBKGC bit and Row Intensity Features

Figure 15. Timing of Output Signals

FONT

MC141542P2 contains 256 character/symbol fonts including 240 normal fonts and 16 multi-color fonts. The normal fonts are located from number $00 to $EF. The 16 multi-color fonts occupy number $F0 to $FF and their patterns can be designed using Font Editor. See the figures on the next page for the details fonts mapping.

Multi-Color Font

The color fonts comprises three different R, G, and B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to the corresponding R/G/B output. See Figure. 16 for the sample displayed color font. No black color can be defined in color font: Black window underline the color font can make the dots(RGB=000) become black in color. It has to be consider during font design stage.

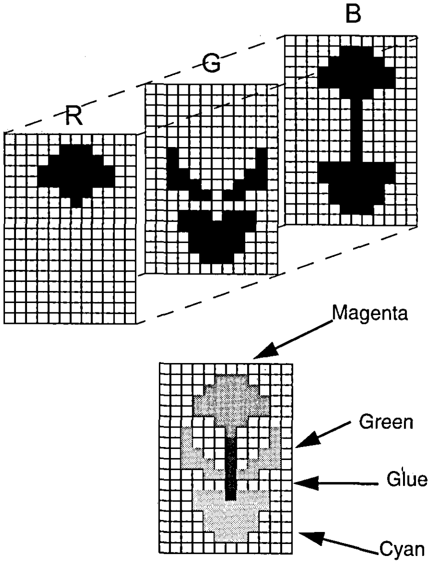


Figure 16. Example of Multi-Color Font

Table 5. The Multi-Color Font Color Selection

	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Icon Combination

User can create On-Screen menu based on those characters and icons. Please refer to Table 6 for Icon combination. Address $00 & $EF are pre-defined characters for testing.

ROM CONTENT

Figures 17 – 20 show the ROM content of MC141542P2. Mask ROM is optional for custom parts.

Table 6. Combination Map

ICON	ROM ADDRESS(HEX)
ARABIC NUMERALS	08-11
ALPHABET	12-2D
EUROPEAN	2E-48
JAPANESE	49-81
SYMOBOLS	01-07, 82-C4
GEOMETRY	C5-EE
COLOR	F0-FF

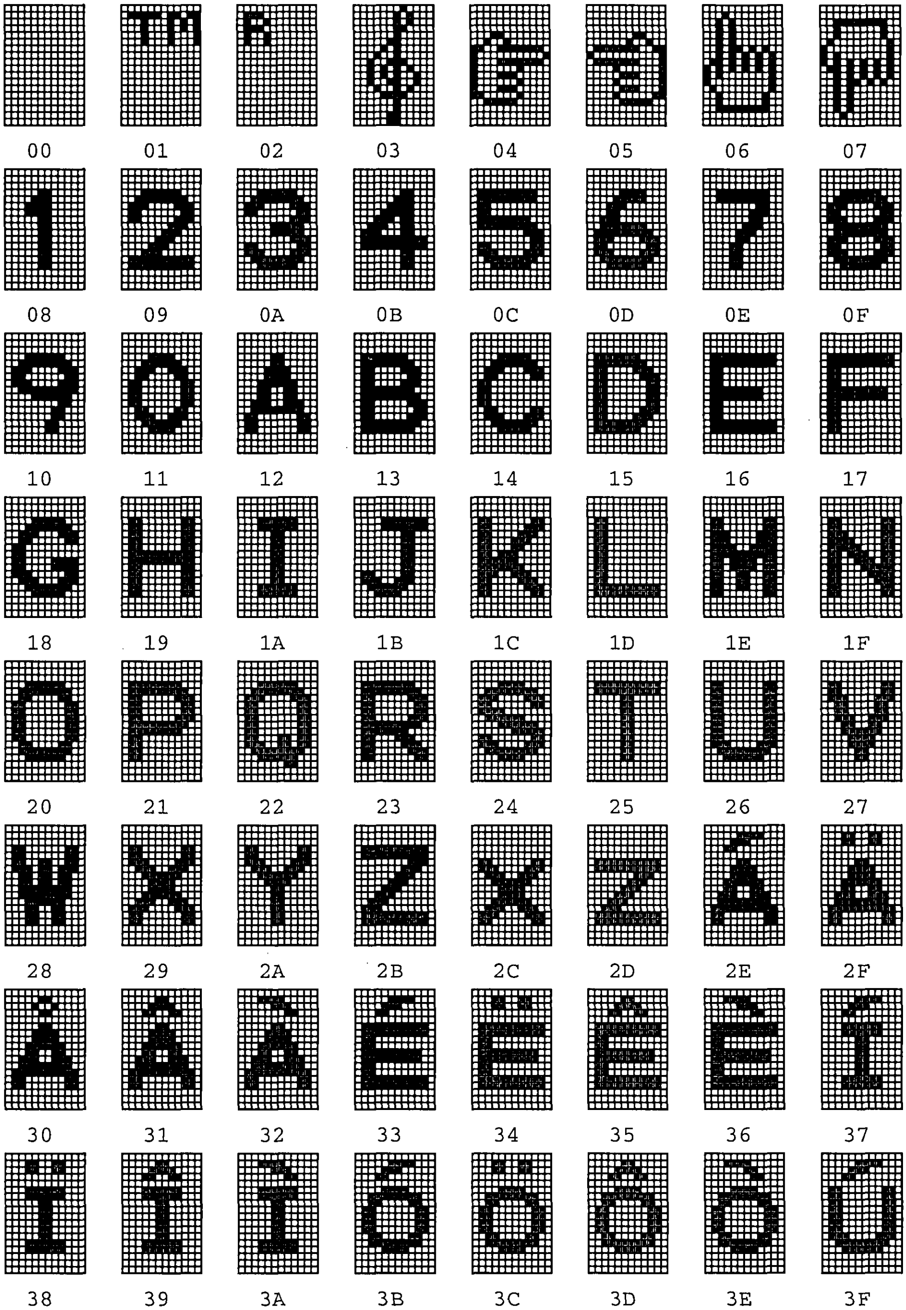


Figure 17. ROM 00 - 3F

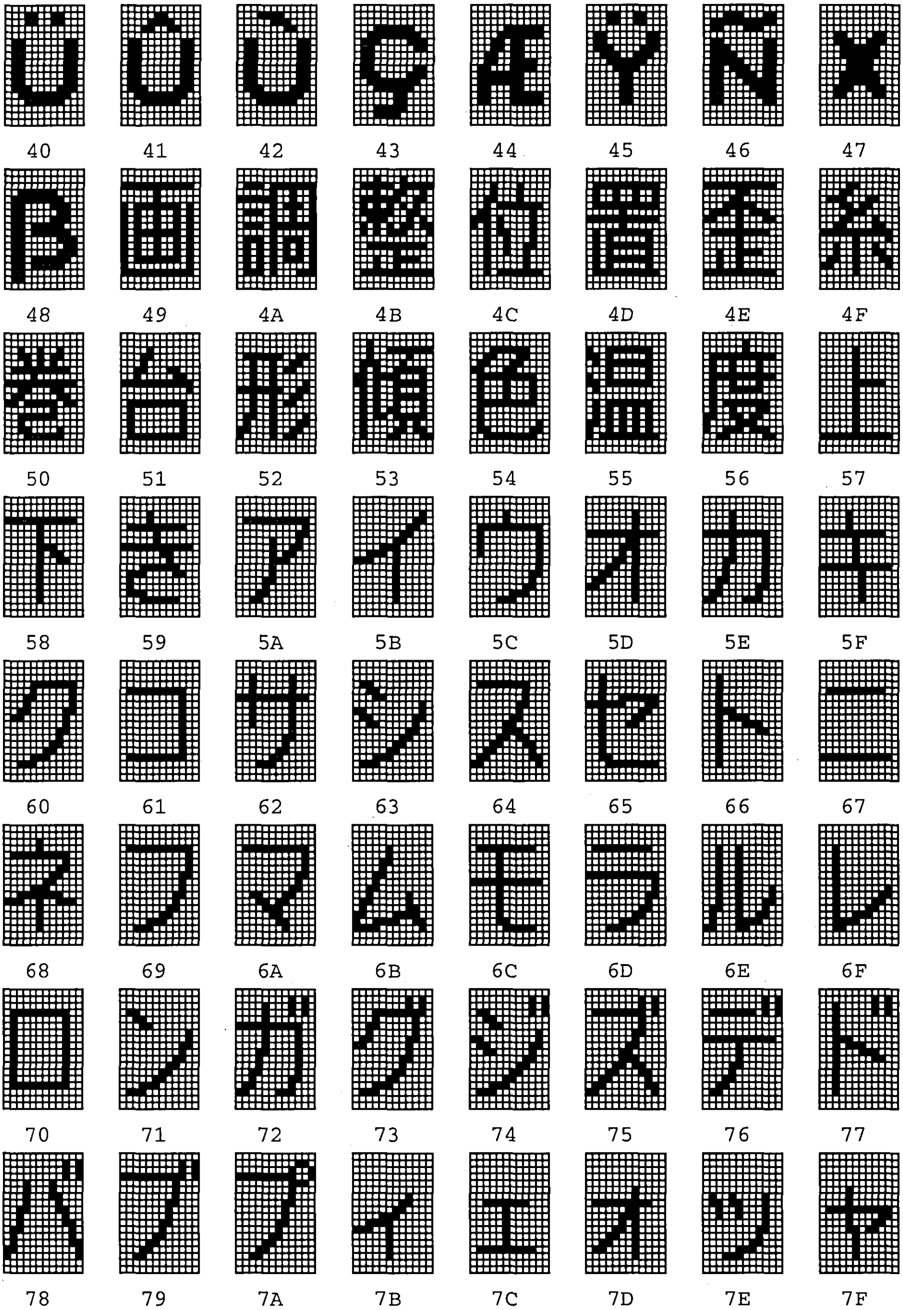


Figure 18. ROM 40 - 7F

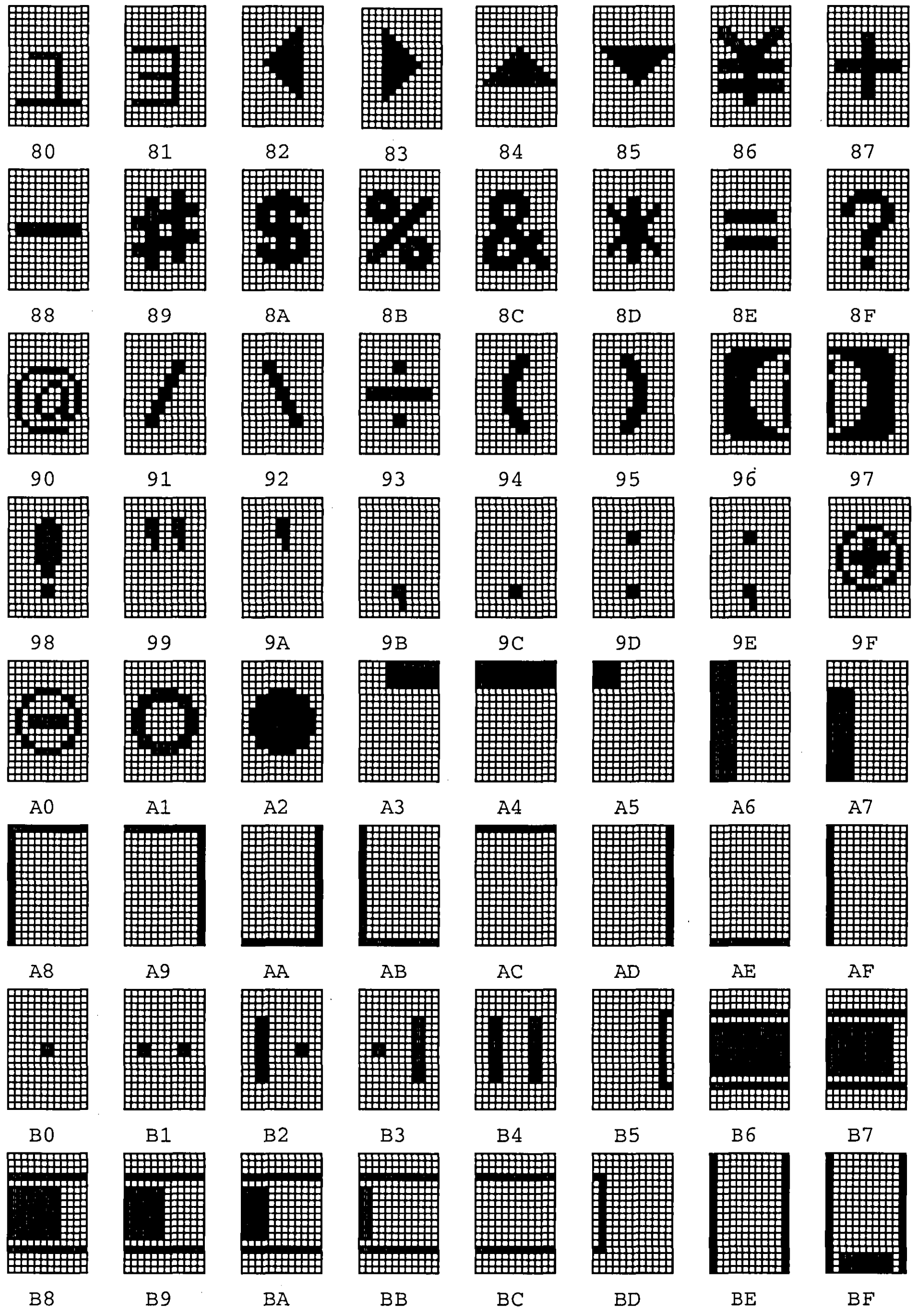


Figure 19. ROM 80 - BF

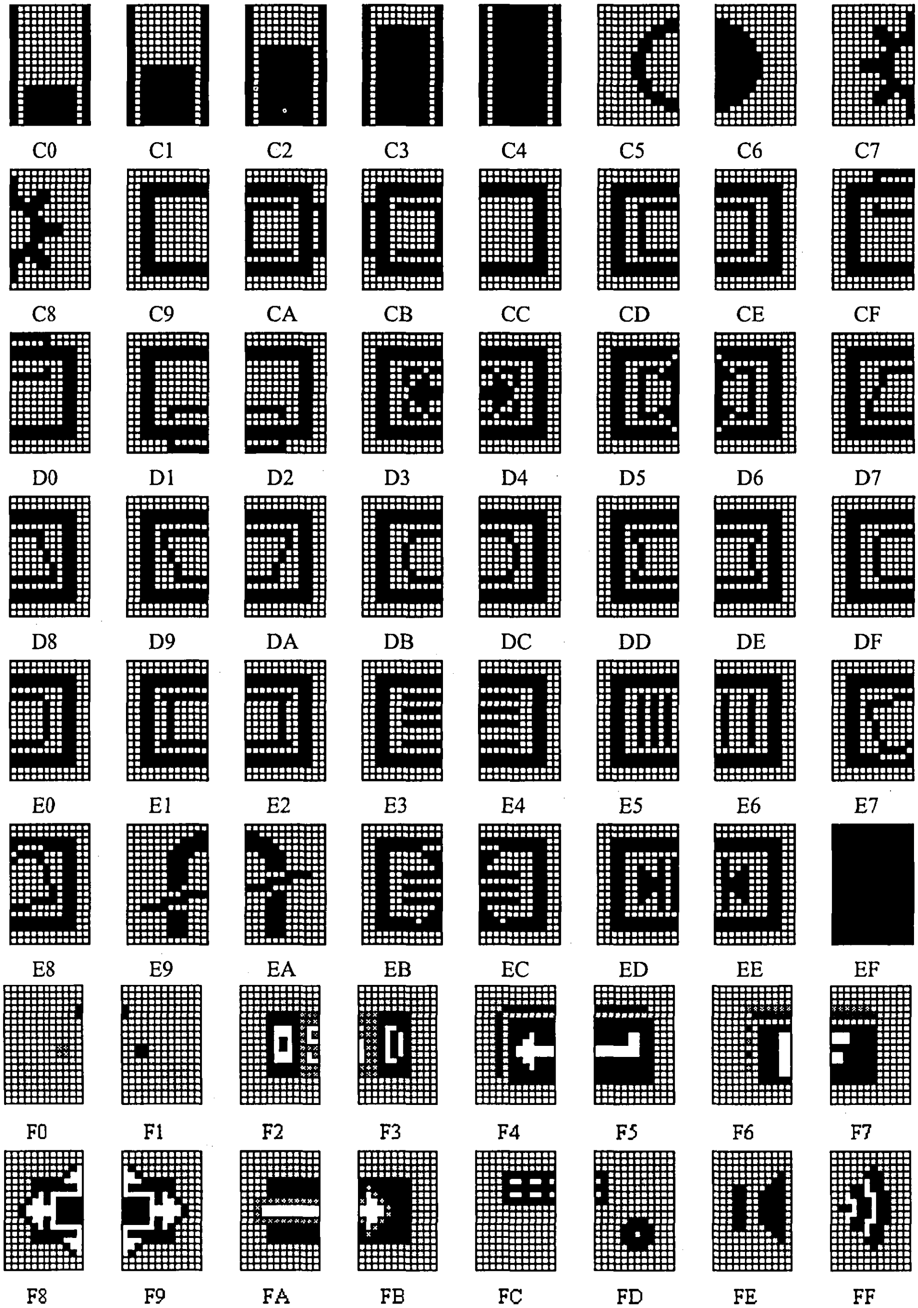


Figure 20. ROM C0 - FF

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141542P2 has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 384/768 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating outside, they are connected internally). Refer to the Application Diagram for the ground connections.(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be added between Pin1-Pin2 and Pin3-Pin4 to filter VCO noise if necessary. Values should be small enough to avoid picture unlocking caused by temperature variation.

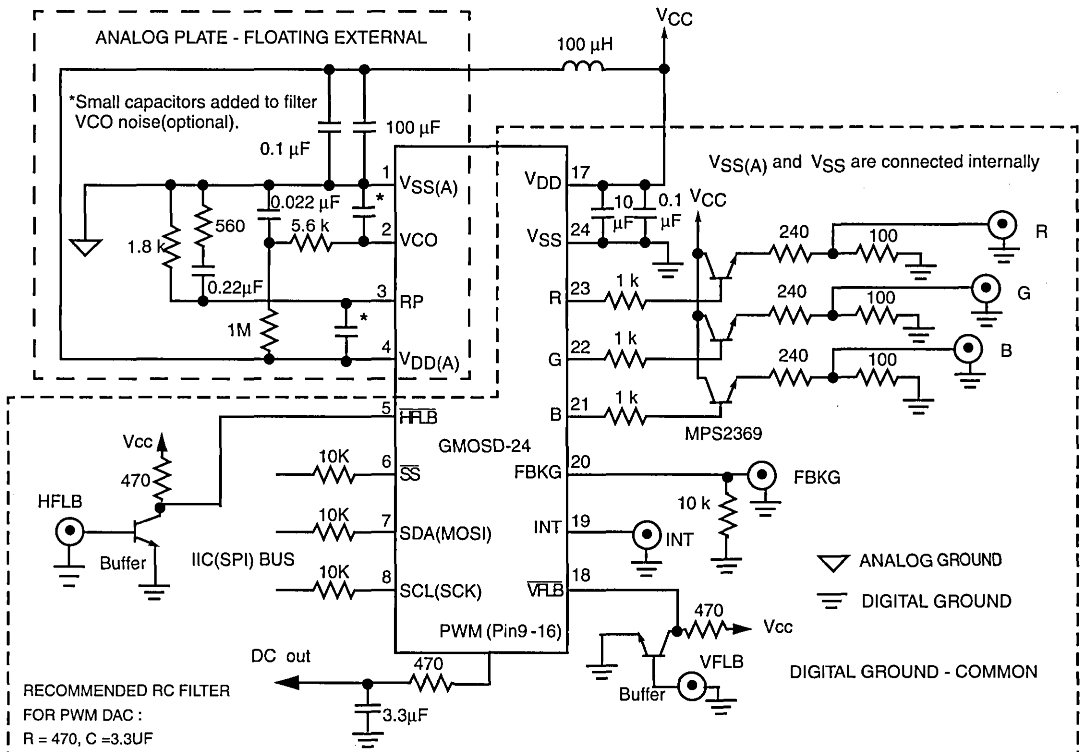
Jittering and Unlocking

Most display jittering and unlocking is caused by HFLB in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both HFLB and VFLB inputs. Refer to the value used in the Application Diagram.

Display Dancing

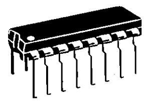
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



Graphic Monitor On-Screen Display - 16
CMOS

MC141545P2



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION
MC141545P2 Plastic Dip

PIN ASSIGNMENT

$V_{SS(A)}$	1	16	V_{SS}
VCO	2	15	R
RP	3	14	G
$V_{DD(A)}$	4	13	B
$\overline{HFLB}$	5	12	FBKG
$\overline{SS}$	6	11	INT
SDA(MOSI)	7	10	$\overline{VFLB}$
SCL(SCK)	8	9	V_{DD}

This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto CRT monitor. Because of the large number of fonts, 256 fonts including 240 standard fonts and 16 multi-color fonts, GMOSD-16 is suitable to be adopted for the multi-language monitor application especially. Its on-chip PLL allows both multiscan operation and self generation of system timing. It also minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

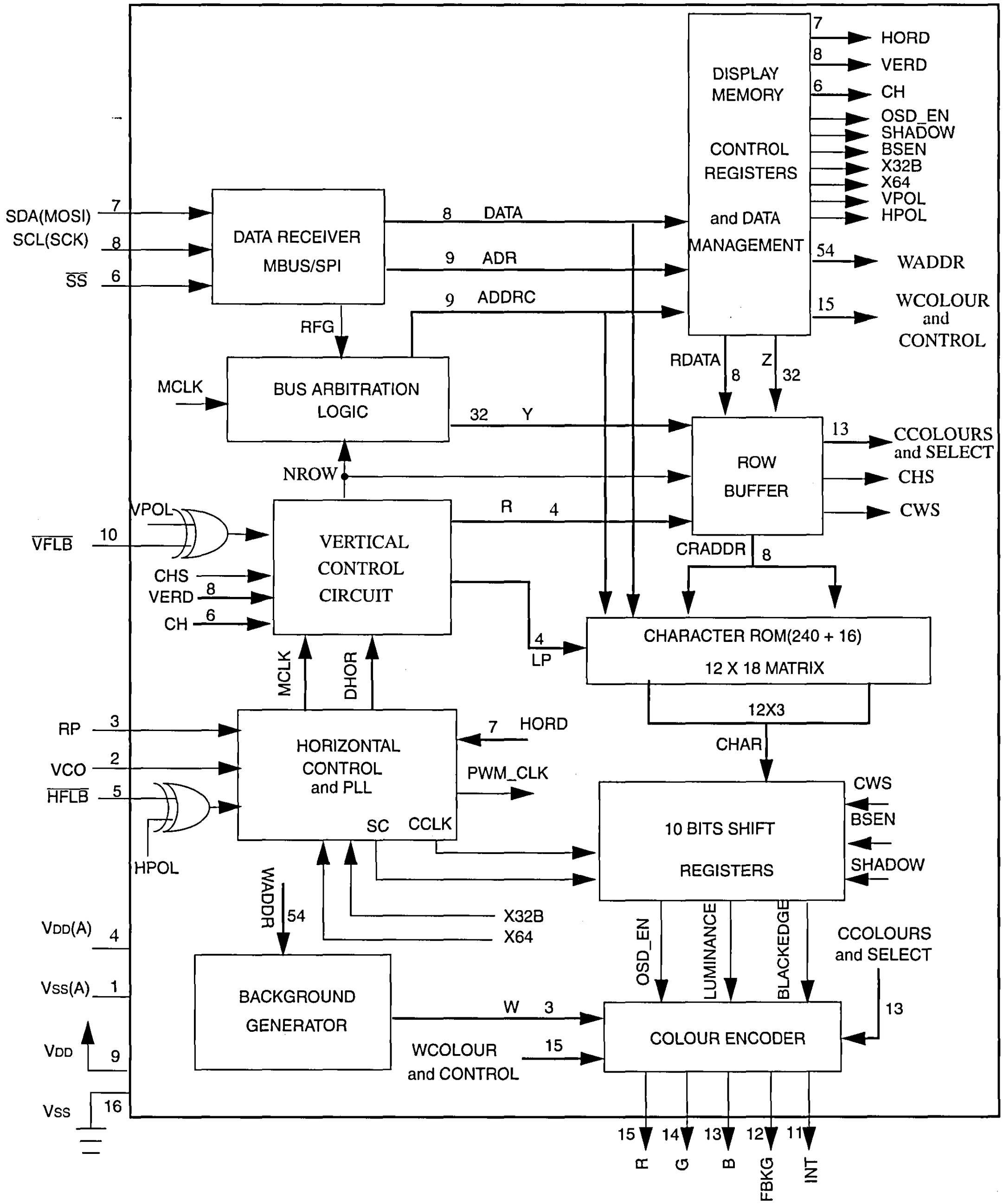
Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are two kinds of resolutions that users can choose. By changing the number of dots per horizontal line to 384 (CGA) or 768 (SVGA), smaller characters with higher resolution can be easily achieved. The full OSD menu is formed of 15 rows x 30 columns which can by freely positioned on anywhere of the monitor screen by changing vertical or horizontal delay.

Special functions such as character background color, blinking, bordering or shadowing, four-level windows with programmable shadowing, row double height and double width, programmable vertical height of character and row-to-row spacing, and full-screen erasing and Fade-In/Fade-Out are also incorporated. There are 8 color selections for any individual character display with row intensity attribute and window intensity attribute to expand the color mixture on OSD menu.

- Totally 256 Fonts Including 240 Standard Fonts and 16 Multi-Color Fonts.
- Two Resolutions: 384 (CGA) or 768 (SVGA) Dots/Line
- Wide Operating Frequency Range for High End Monitor: 15KHz ~ 120KHz
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- 7-Color Selection for Characters background
- True 16-Color Selection for Windows
- Fancy Fade-In/Fade-Out Effects
- Programmable Height of Character to Meet Multi-Sync Requirement
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Shadowing on Windows with Programmable Shadow Width/Height
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
- Programmable Vertical and Horizontal Positioning for Display Centre
- Double Character Height and Double Character Width
- Internal PLL Generates a Wide-Ranged System Clock (92.2 MHz)
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

REV 1
4/97

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT) C_{load} = 30 pF				
t_r	Rise Time	—	—	6	ns
t_f	Fall Time	—	—	6	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	15K	—	120K	Hz

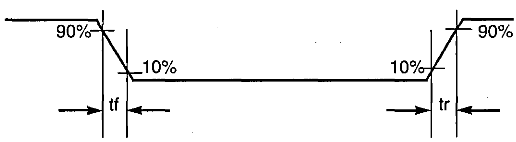


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{II}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{II}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output) at V_{DD}=5.0V	—	—	+ 26	mA

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

V_{DD} (Pin 9)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT (Pin 11)

This output pin is used to indicate the color intensity. If the intensity control bits are set in the row attribute registers or window control registers, this pin will output a logic high while displaying the specified windows or the characters on the associated rows. Otherwise, it will keep in low state. Please refer to Figure 15 for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the "REGISTERS" for more information.

FBKG (Pin 12)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13, 14, 15)

GMOSD-16 color outputs in TTL level to the host monitor. These three signals are open drain outputs if 3_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See "REGISTERS" for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141545P2 is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the GMOSD-16 is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen-refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the GMOSD-16 functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{\text{HFLB}}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus or SPI bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the HFLB input frequency where the dot clock is equal to 384/768xHFLB in 384/768 modes respectively. In order to have stable operation of M_Bus or SPI bus in the OSD and meet below specifications, HFLB(15k-120k) must be presented and the PLL locks to HFLB properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps. The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the GMOSD-16 circuitry of MC141545P2, so that the received information can then be displayed.

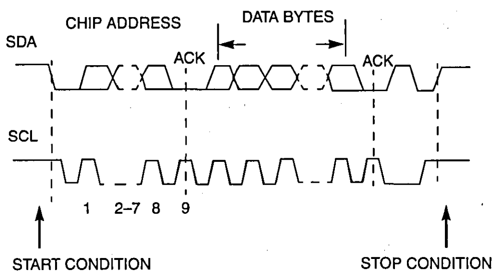


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{\text{SS}}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{\text{SS}}$ pin low by the master device to enable MC141545P2 to accept data. The $\overline{\text{SS}}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{\text{SS}}$ pin is then pulled high by master to terminate the transmission. Data bit is sent from master to OSD's internal latch during rising edge of SCK and then transmit to internal register during falling edge. Therefore, last falling edge of CLK is needed for proper transmission of last byte data. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

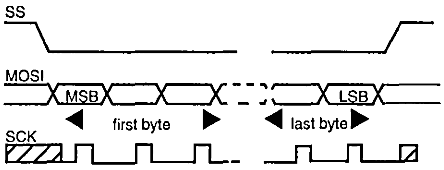


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, two register blocks, display registers, attribute/control registers, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:

(a) R - > C- > I -> R - > C - > I - > ....

(b) R - > C - > I - > C - > I - > C - > I.......

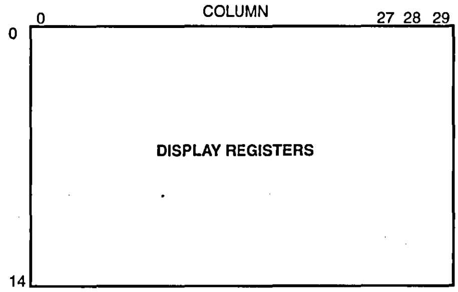
(c) R - > C - > I - > I - > I - > ....

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the display row address from attribute area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 4. Data Packet for Display Data



ADDRESS	BIT 7	6	5	4	3	2	1	0	FORMAT
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:

(a) R - > C- > I -> R - > C - > I - > ....

(b) R - > C - > I - > C - > I - > C - > I.......

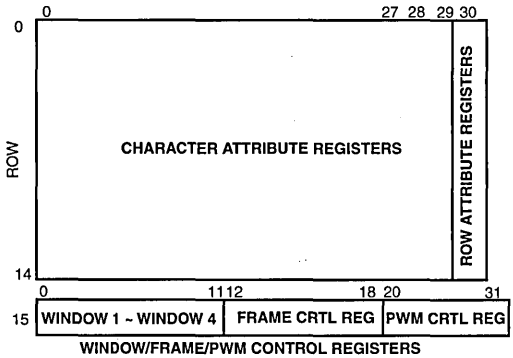
(c) R - > C - > I - > I - > I - > ....

NOTE: R means row byte.
C means column byte.
I means data byte.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

row addr	col addr	info

Figure 6. Data Packet for Attribute/Control Data



ADDRESS	BIT 7	6	5	4	3	2	1	0	FORMAT
ROW	1	0	1	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 7. Address Bit Patterns for Attribute/Control Data

MEMORY MANAGEMENT

All the internal programmable area can be divided into two parts including (1) Display Registers (2) Attribute/Control Registers. Please refer to the following two figures for the corresponding memory map.

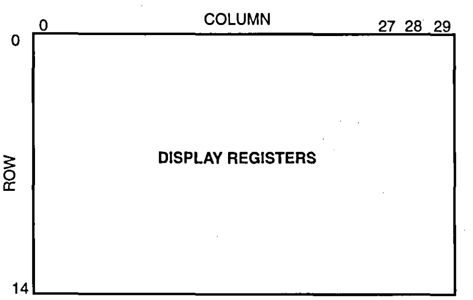


Figure 8. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 ROM fonts.

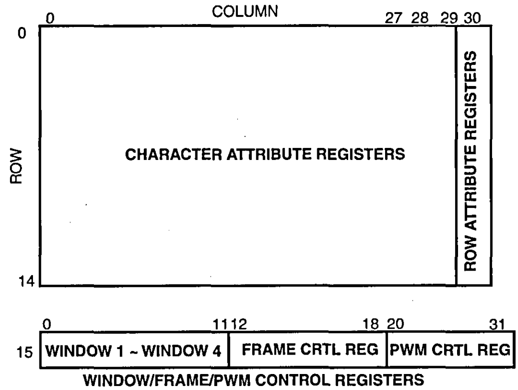


Figure 9. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color and 3-bit to define its background. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. as well as background. Every data row associate with one attribute register, which locate at coln 30 of their respective rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control, frame function control and PWM registers. Four window control registers for each of four windows together with four frame control registers and twelve PWM registers occupy the first 28 columns of row 15 space. These control registers will be described on the "REGISTERS" section.

User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

REGISTERS

(I) Display Register

Display Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
← CRADDR →							

Bit 7-0 CRADDR - This eight bits address one of the 256 characters or symbols resided in the character ROM fonts.

(II) Attribute/Window/Control/Frame Registers

Character Attribute Register (Row 0~14, Coln 0~29)

7	6	5	4	3	2	1	0
	BGR	BGG	BGB	BLINK	R	G	B

Bit 6-4 These three bits define the color of the background for the correspondent characters. If all three bits are clear, no background will be shown(transparent). Therefore, total seven background colors can be selected.

Bit 3 BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

Bit 2-0 These three bits are the color attribute to define the color of the associated character/symbol.

Table 1. The Character/Window Color Selection

	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Row Attribute Register (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
					R_INT	CHS	CWS

Bit 2 R_INT - Row intensity bit controls the color intensity of the displayed character/symbol on the corresponding row. Setting this bit to 1 means high intensity color and the INT pin will go high while displaying the characters of this row.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR (MSB … LSB)				ROW END ADDR (MSB … LSB)			

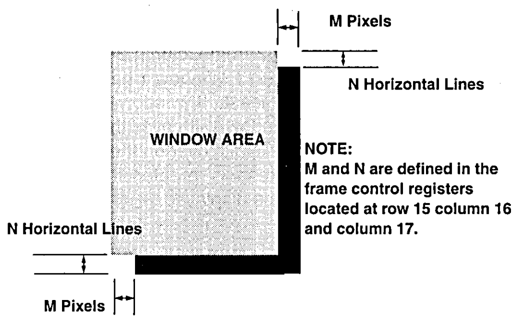
Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR (MSB … LSB)					WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 1 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output black shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17. See the following figure and the related frame control register for detail.



Window Shadowing

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 2 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 2 shadowing.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 2. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 3 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity.Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 3 shadowing.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 3. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9

	7	6	5	4	3	2	1	0
ROW 15 COLN 9	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 10

	7	6	5	4	3	2	1	0
ROW 15 COLN 10	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 4 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11

	7	6	5	4	3	2	1	0
ROW 15 COLN 11	MSB	COL END ADDR			LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 4. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12

	7	6	5	4	3	2	1	0
ROW 15 COLN 12	MSB			VERTD				LSB

Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13

	7	6	5	4	3	2	1	0
ROW 15 COLN 13	CLR	MSB		HORD				LSB

Bit 7 CLR - Setting this bit to 1 will clear all display memory from Row 0 to Row 14; Control register will not be erased.

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Character Height Control Register Row 15 Coln 14

	7	6	5	4	3	2	1	0
ROW 15 COLN 14	HF	O	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance. This bit controls gain of internal VCO so that PLL can work for whole range from 15KHz to 120KHz.

Bit 6 Bit reserved. Set to 0 for normal operation.

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. GMOSD adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result. Display character line number is equal to C1 x (18 + C2) where C1 = 1, 2 or 3 defined by CH5-CH4 and C2 = 0-15 defined by CH3-CH0 (BRM).

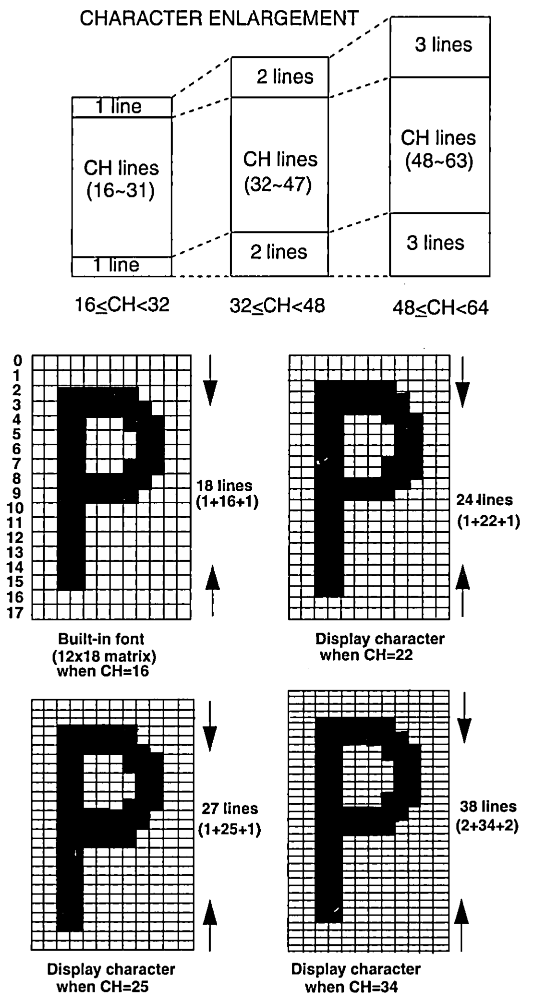


Figure 10. Variable Character Height

Figure 10 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

$H = CH + N$

Where H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

$N = 2$ when $16 \leq CH < 32$

$N = 4$ when $32 \leq CH < 48$

$N = 6$ when $48 \leq CH < 64$

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW		X32B	3_S	FAN	FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 3 X32B - It determines the number of dots per horizontal line. There are 384 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 768 dots per horizontal sync line when bit X32B is set to 1. Please refer to the Table 2 for details.

Table 2. Resolution Setting

X32B	0	1
Dots / Line	384	768
Resolution	CGA	SVGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of characters or windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity characters or windows. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 1 FAN - It enables the fan-in/fan-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

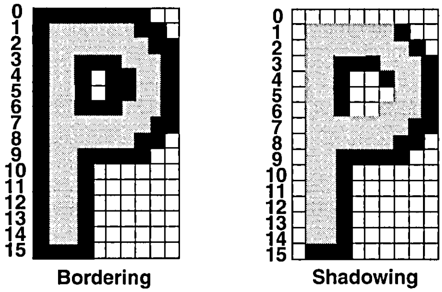
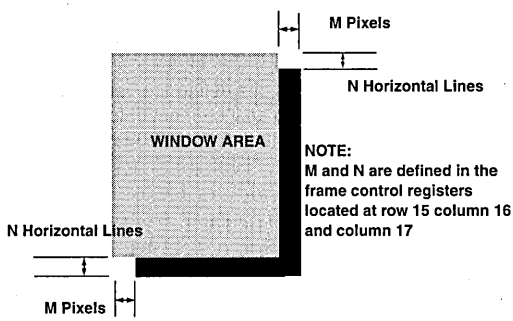


Figure 11. Character Bordering and Shadowing



Window Shadowing

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
ROW 15 COLN 16	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 3. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 4. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

	7	6	5	4	3	2	1	0
ROW 15 COLN 18	MSB		RSPACE		LSB	TRIC	HPOL	VPOL

Bit 7-3 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on. It can be used for Portrait monitor too when icon design is rotated 90 degree.

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal ($\overline{HFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal ($\overline{VFLB}$). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

- **NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.**

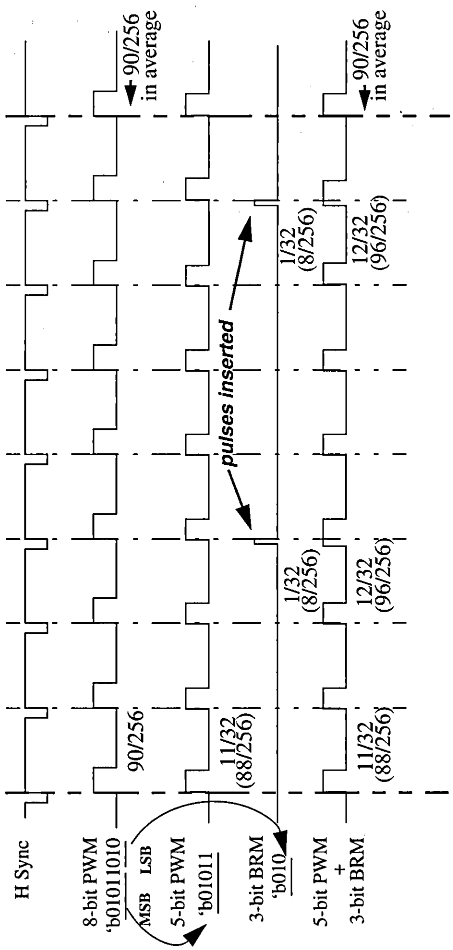


Figure 12. Pure 8-bit PWM v.s. 5-bit PWM + 3-bit BRM

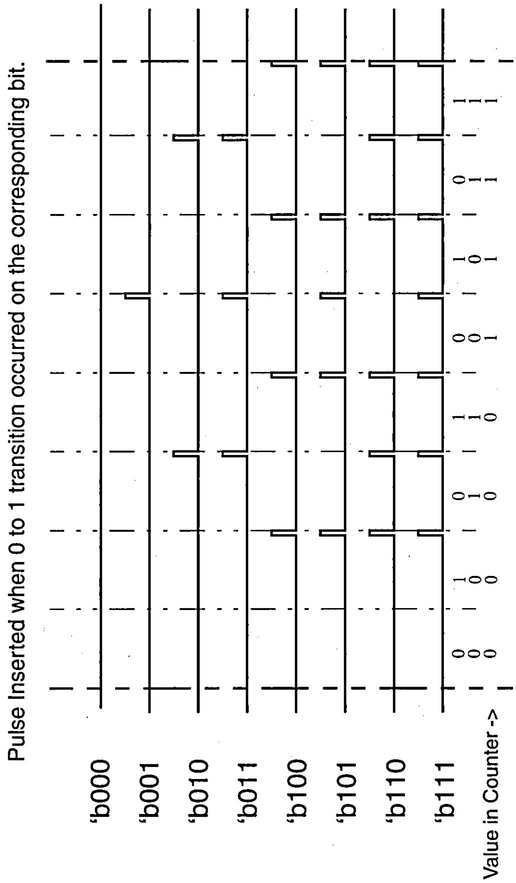


Figure 13. BRM Pulse Insertion Algorithm

A software called GMOSD-16 FONT EDITOR in IBM PC environment was written for MC141545P2 editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141545P2.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 12x18 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 11 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

Frame Format and Timing

Figure 14 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 14 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{HFLB}$ and $\overline{VFLB}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge-up resistor, which is the 1MΩ resistor in a series with 5.6 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 384 if the bit X32B is clear and H Freq. x 768 if bit X32B is set to 1. For example, dot frequency is 12.28 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1, the dot frequency will be 24.57 MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{VFLB}$ of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 360, regardless of row character width and the setting of bit X32B.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 384 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 768 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 15 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

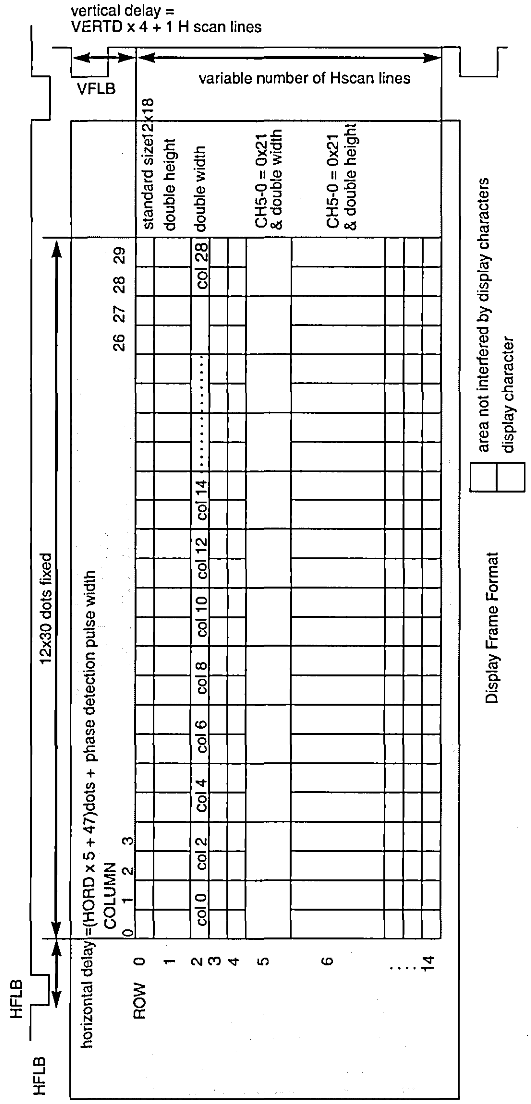


Figure 14. Display Frame Format

FONT

MC141545P2 contains 256 character/symbol fonts including 240 normal fonts and 16 multi-color fonts. The normal fonts are located from number $00 to $EF. The 16 multi-color fonts occupy number $F0 to $FF and their patterns can be designed using Font Editor. See the figures on the next page for the details fonts mapping.

Multi-Color Font

The color fonts comprises three different R, G, and B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to the corresponding R/G/B output. See Figure. 16 for the sample displayed color font. No black color can be defined in color font: Black window underline the color font can make the dots(RGB=000) become black in color. *It has to be consider during font design stage.*

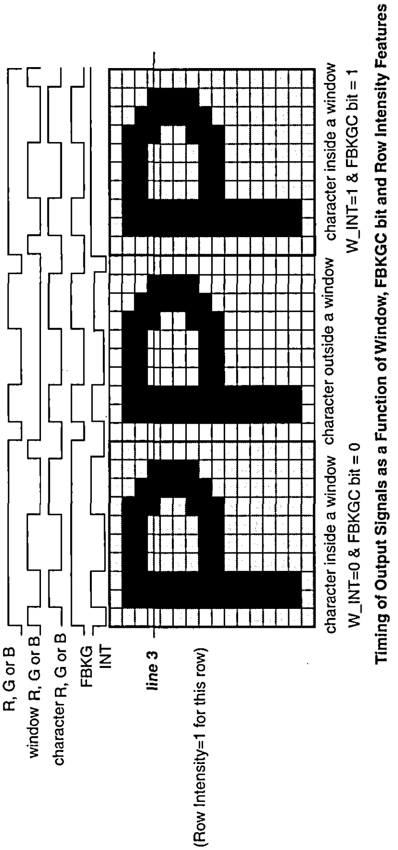


Figure 15. Timing of Output Signals

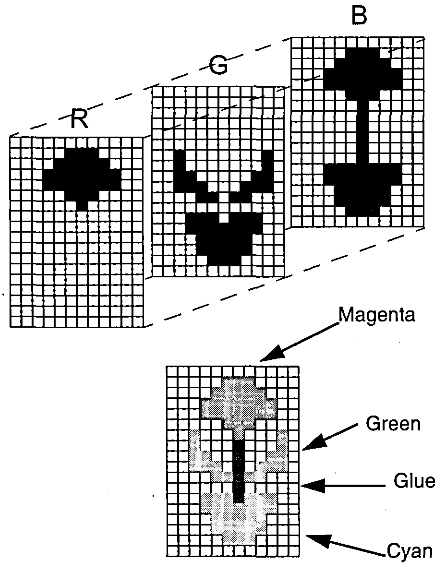


Figure 16. Example of Multi-Color Font

Table 5. The Multi-Color Font Color Selection

	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Icon Combination

User can create On-Screen menu based on those characters and icons. Please refer to Table 6 for Icon combination. Address $00 & $EF are pre-defined characters for testing.

ROM CONTENT

Figures 17 – 20 show the ROM content of MC141545P2. Mask ROM is optional for custom parts.

Table 6. Combination Map

ICON	ROM ADDRESS(HEX)
ARABIC NUMERALS	08-11
ALPHABET	12-2D
EUROPEAN	2E-48
JAPANESE	49-81
SYMBOLS	01-07, 82-C4
GEOMETRY	C5-EE
COLOR	F0-FF

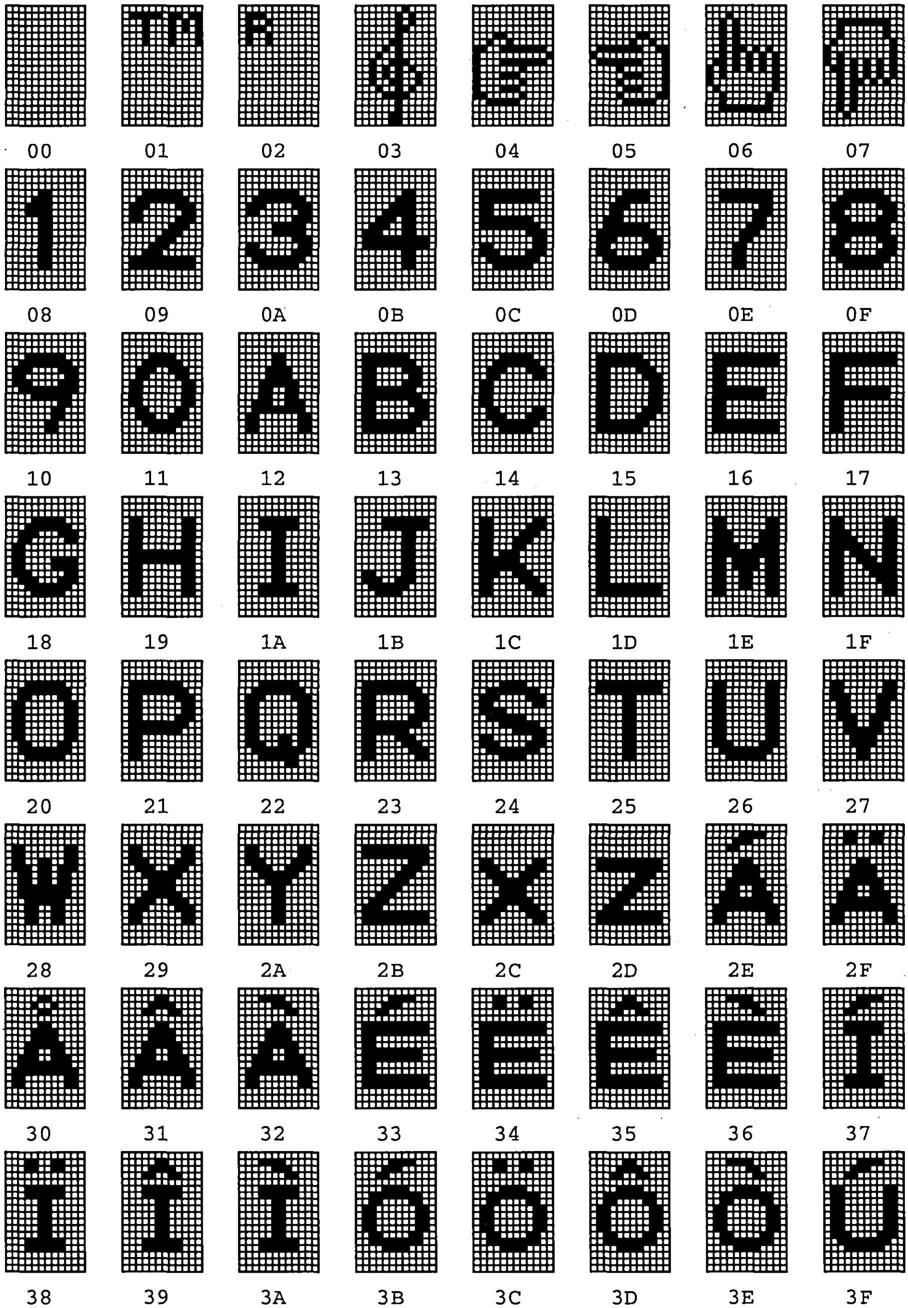


Figure 17. ROM 00 - 3F

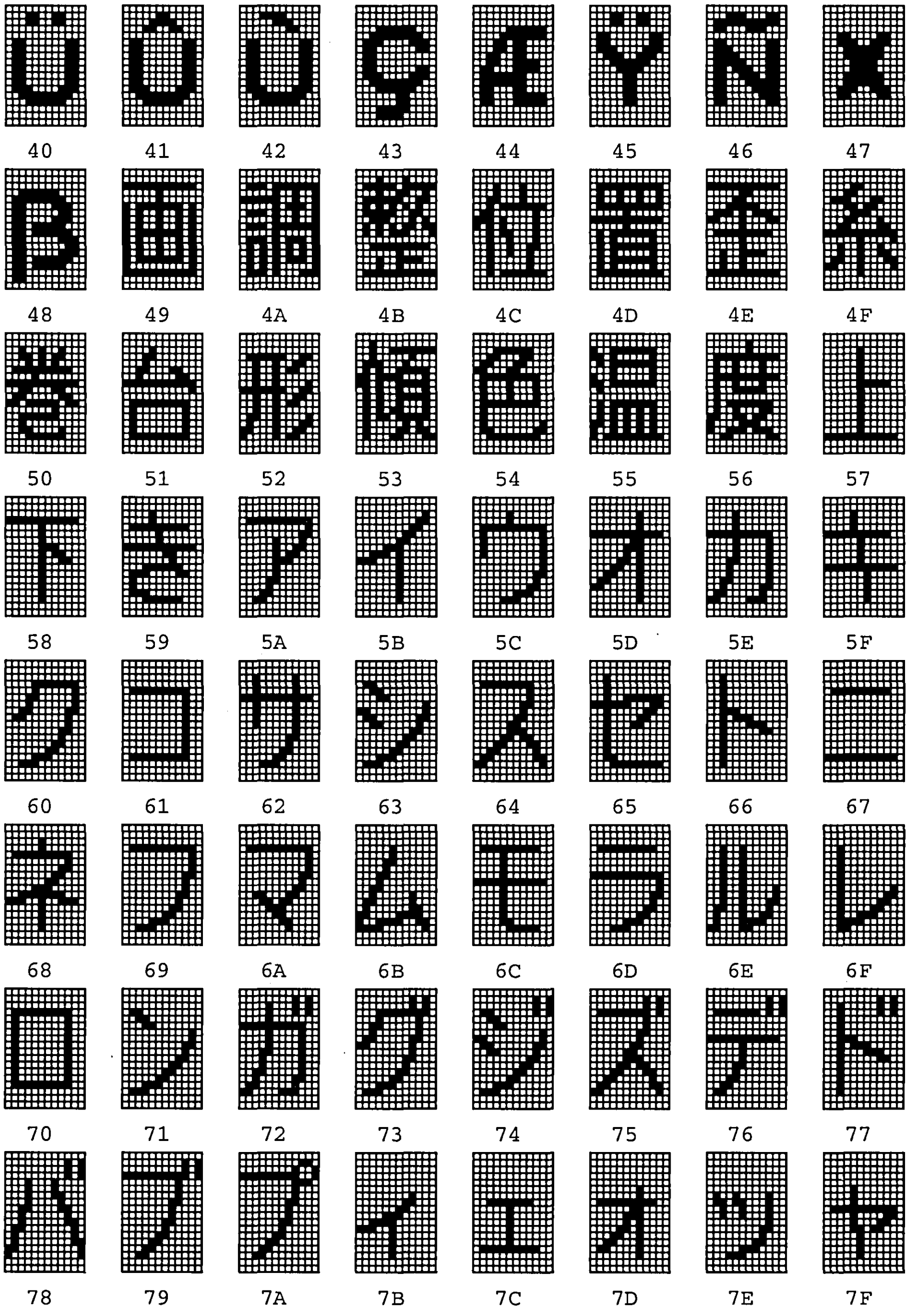


Figure 18. ROM 40 - 7F

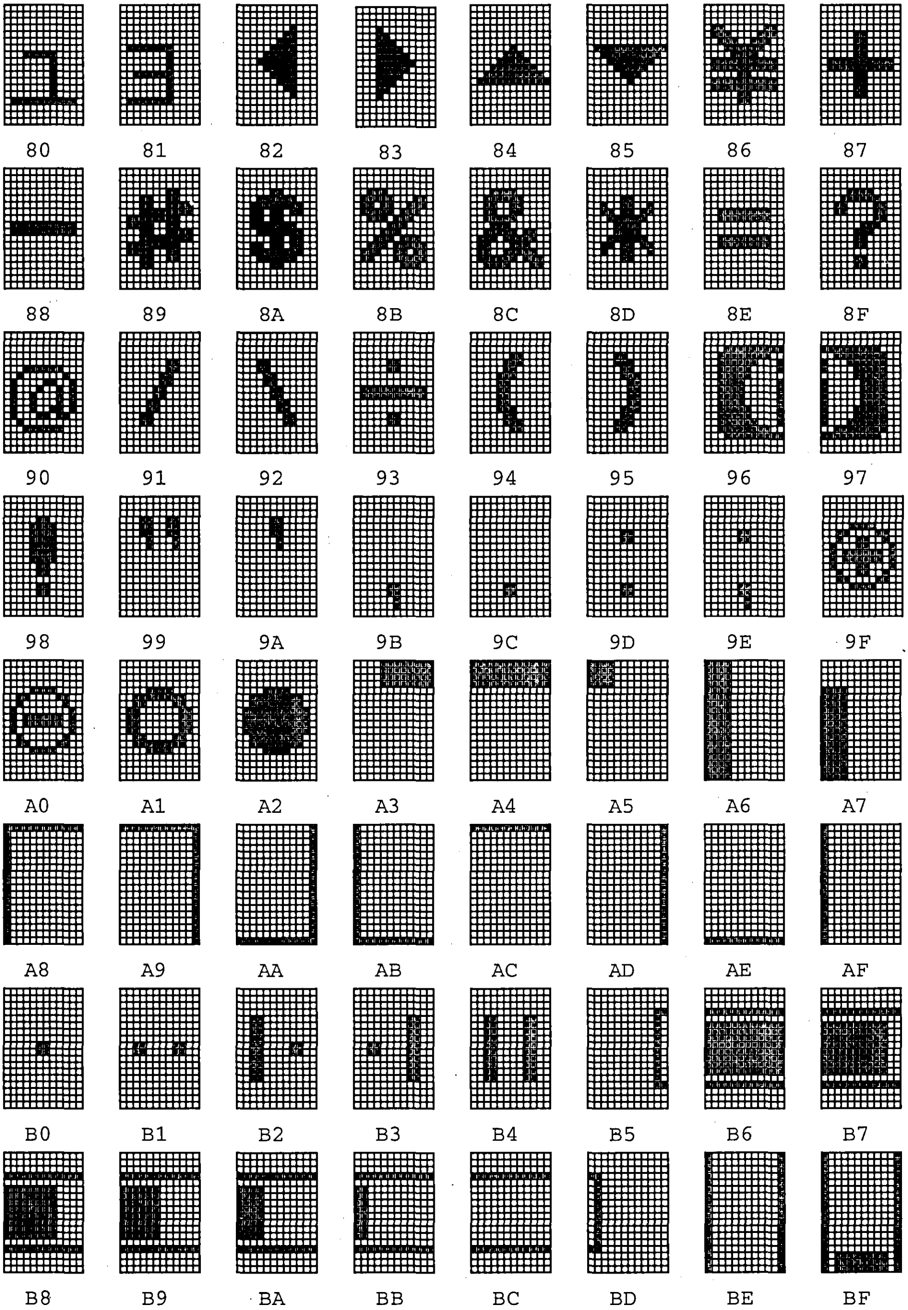


Figure 19. ROM 80 - BF

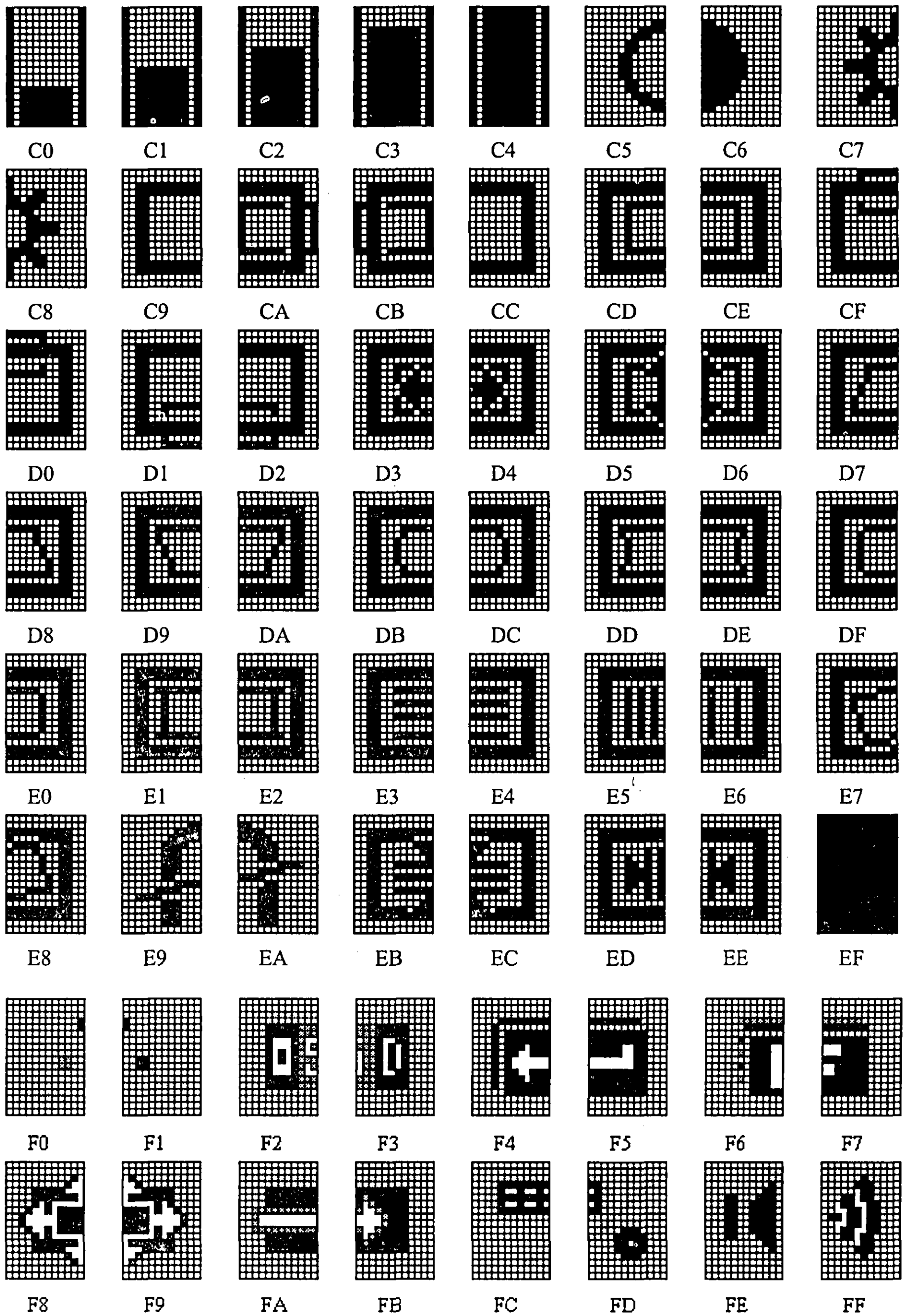


Figure 20. ROM C0 - FF

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141545P2 has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 384/768 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating outside, they are connected internally). Refer to the Application Diagram for the ground connections.(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 17 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be added between Pin1-Pin2 and Pin3-Pin4 to filter VCO noise if necessary. Values should be small enough to avoid picture unlocking caused by temperature variation

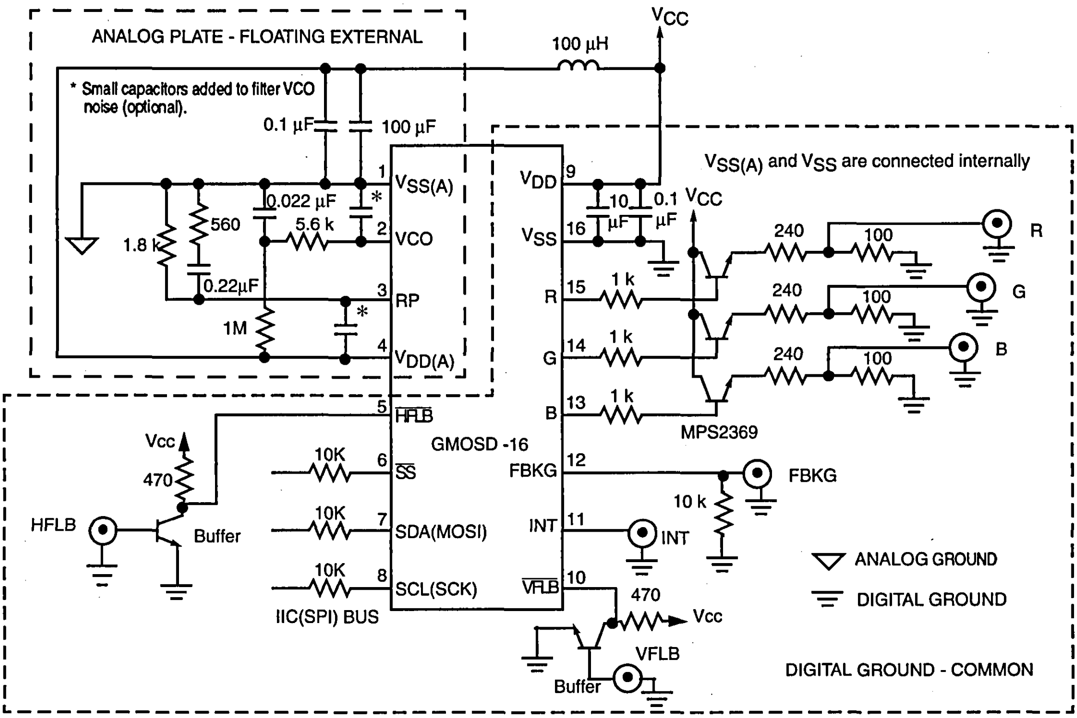
Jittering and Unlocking

Most display jittering and unlocking is caused by HFLB in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both HFLB and VFLB inputs. Refer to the value used in the Application Diagram.

Display Dancing

Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



Evaluation Kits 5

Product Information
MC141511 Evaluation Kit

MC141511EVK1
MC141511EVK2

Introduction

The MC141511EVK is an evaluation board so built that for the development of the application using MC141511. The evaluation board is best to use with the MC68HC05L10EVM so the connection effort is minimal. There is two versions of the evaluation board, MC141511EVK1 is the demo board with two MC141511 and the MC141511EVK2 consist of four MC141511.

The two attached figures which show you the layout of 511 Demo Board and also connection to M68HC05L10EVM.
On the 511 Demo Board, you will find :

Power Supply Jack
Please connect them to +12V, GND and +5V respectively.

P03, P04
These are two 64 way headers to be connected to the EVM. The pin assignment is shown in Figure 2

VR
This is used to adjust the contrast of the LCD EVK.

CS1, CS2, CS3, CS4
The four jumpers are to connect CS1, CS2, CS3, CS4 of MCU to the chip enable pin (CE) of TAB no. 1, 2, 3 and 4.

For MC141511EVK1, the two jumpers on CS2 and CS4 will be closed. For MC141511EVK2, the four jumpers on CS1, CS2, CS3 and CS4 will be closed.

MS
This is to selects how display RAM is addressed, according to 1:32 or 1:41 multiplex ratio.
0 = 1:32 multiplex addressing
1 = 1:41 multiplex addressing

LRS
This is to control the Left-Right Selection pin of the MC141511.

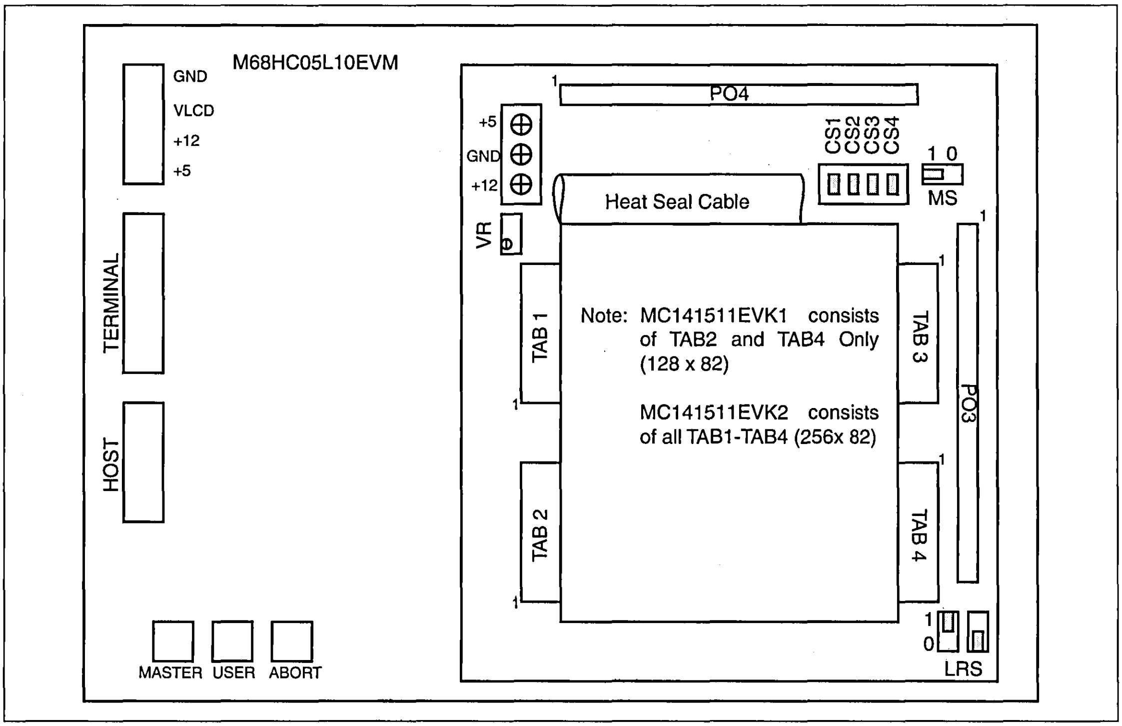


Figure 1. MC141511EVK

REV 1
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There are two jumpers marked LRS on the evaluation board. The left one in Figure 1 is connected to LRS pin of TAB 3 and TAB 4 while the right one is connected to LRS of TAB no. 1 and 2.

The left-right selection pin define the direction of the segment driver display. (Please refer to the figure "Display RAM Configuration" of MC141511 Advance Information)
0 = SEG 0-127
1 = SEG 127 -0

PO3				PO4			
VLCD	1	2	NC	BP0	1	2	BP1
PA7	3	4	PA6	BP2	3	4	BP3
PA5	5	6	PA4	BP4	5	6	BP5
PA3	7	8	PA2	BP6	7	8	BP7
PA1	9	10	PA0	BP8	9	10	BP9
BPCLK	11	12	FRM	BP10	11	12	BP11
CS4	13	14	CS3	BP12	13	14	BP13
CS2	15	16	CS1	BP14	15	16	BP15
AD19	17	18	AD18	BP16	17	18	BP17
AD17	19	20	AD16	BP18	19	20	BP19
AD15	21	22	AD14	BP20	21	22	BP21
AD13	23	24	AD12	BP22	23	24	BP23
AD11	25	26	AD10	BP24	25	26	BP25
AD9	27	28	AD8	BP26	27	28	BP27
AD7	29	30	AD6	BP28	29	30	BP29
AD5	31	32	AD4	BP30	31	32	BP31
AD3	33	34	AD2	BP32	33	34	BP33
AD1	35	36	AD0	BP34	35	36	BP35
PB7	37	38	PB6	BP36	37	38	BP37
PB5	39	40	PB4	BP38	39	40	BP39
PB3	41	42	PB2	BP40	41	42	V1
PB1	43	44	PB0	V4	43	44	VOUT
D7	45	46	D6	PE3	45	46	PE2
D5	47	48	D4	PE1	47	48	PE0
D3	49	50	D2	PD7	49	50	PD6
D1	51	52	D0	PD5	51	52	PD4
IRQ2	53	54	IRQ1	PD3	53	54	PD2
R/W	55	56	PO2	PD1	55	56	PD0
TONE	57	58	RO1S	PC7	57	58	PC6
RESET	59	60	NC	PC5	59	60	PC4
NC	61	62	NC	PC3	61	62	PC2
VDD	63	64	VSS	PC1	63	64	PC0

Figure 2. PO3, PO4 pin assignment

MC141512EVK

Product Information
MC141512 Evaluation Kit

Introduction

The MC141512EVK is an Evaluation Kit for MC141512 & MC141514 LCD drivers evaluation and for prototypes development using these LCD drivers. This module consists of MC141512, MC141514 LCD drivers and a 320 x 146 pixel LCD panel. This EVK board can be connected directly to MC68HC05L11EVM, which is an evaluation module providing control signals and display data from MC68HC05L11 MCU to the LCD Drivers MC141512 & MC141514. Any character or graphic pattern can be displayed on the LCD panel through software control.

Packing List

The package includes:
- an evaluation kit MC141512EVK

Features

- 320 x 146 active display size
- Hardware contrast control
- Two ports for connection to MC68HC05L11EVM
- On board voltage divider provides bias levels to LCD panel

Setup and Operation

Simple Setup
The simple setup is shown in Figure 2.

Supply
The Adapter Board requires two supply voltage : +25V for VLCD, +5V for VDD .

Contrast of LCD panel
The variable resistor, VR1, is used to adjust the contrast of the LCD panel.

Control Signal from MC68HC05L11EVM
The J9 and J10 are used to get control signal and display information from MC68HC05L11EVM. The pin assignment of the two ports is shown in Figure 3.

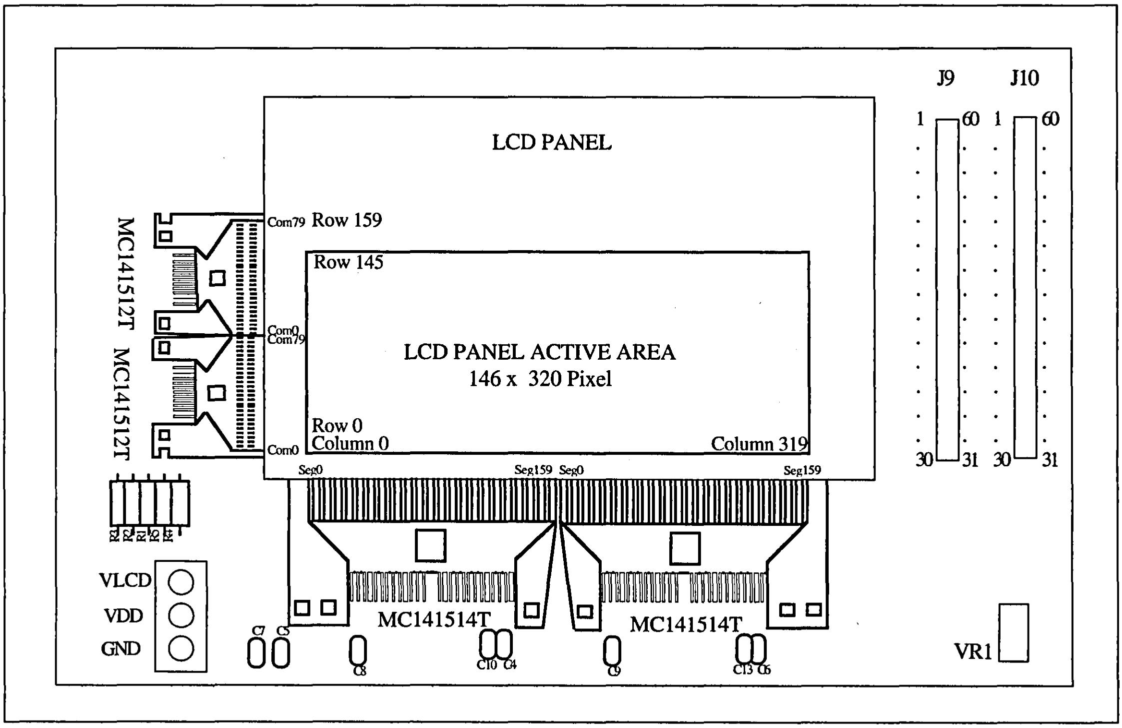

Figure 1. MC141512EVK

REV 2
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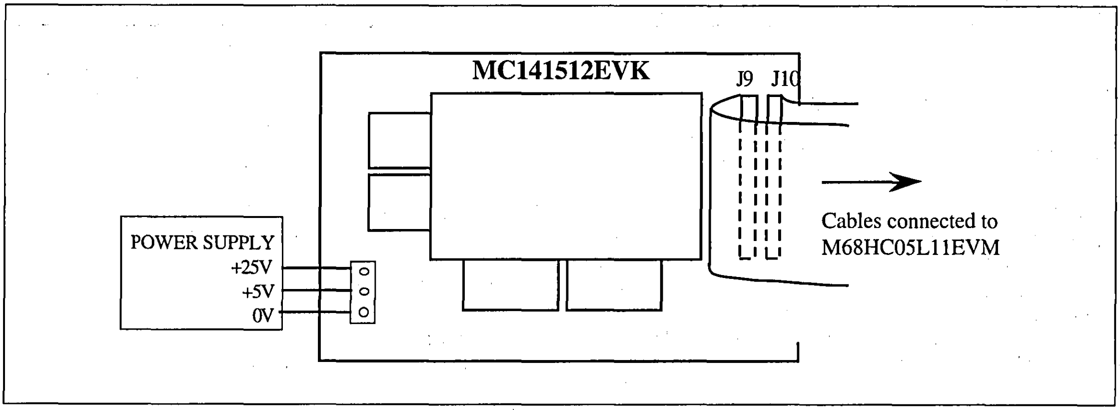

Figure 2 Simple setup of the EVK

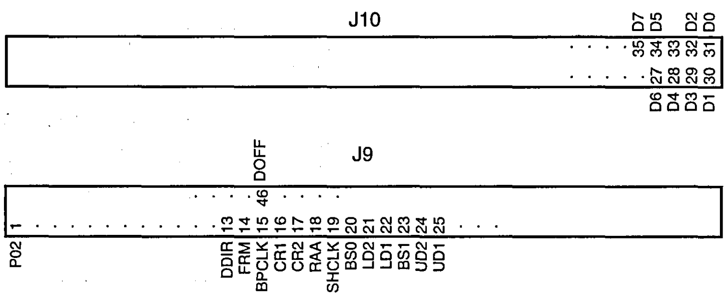

Figure 3 I/O Port Connectors to EVM (only pins with connection are show)

Simple Test Procedure for the Evaluation Board

The following is a simple test procedure which should able to check the functionality of the demo board and also serve as a simple exercise to begin with this EVK:

IBM-PC to EVM Downloading Procedure by using Kermit

MC141512 Evaluation Board power supply condition : VDD = 5V, VSS = 0V, VLCD =0V

Step	Comments
C>KERMIT IBM-PC Kermit-MS VX.XX Type ? for help	IBM-PC prompt. Enter Kermit program
Kermit-MS>SET BUAD 9600	Set IBM-PC baud rate
Kermit-MS>CONNECT	Connect IBM-PC to EVM
(Connecting to host, type Control-] C to return to PC) (RETURN)	
>MM32	Set Control Miscellaneous Register at address $32
=91	Display on, select lower panel segment bank
>MM31	Set MUX Register at address $31
=91	to be 145 (= 146 MUX)
=01	Clear bit 7 of address $32. (Please refer to section 6.2 of MC68HC05L11 Product Preview rev2.0)

After setting up the above steps, maintain the MC141512 Evaluation Board supply condition to : VDD = 5V, VSS = 0V. Then increase the supply to VLCD gradually from 0V to 25V. If the LCD panel is on before reaching 10V, the evaluation module may have problem. The normal operation voltage of VLCD is between 10 - 25V. If the LCD panel does not turn on for VLCD > 25V, the evaluation board is also defective.

If the panel is on in the operation range, do the following steps in Kermit:

>LOAD T
(press [F5] and enter external program file name developed for MC68HC05)
>G XXXX

Check if any line is missing, turn VR1 to get a good contrast.

Reference

Please also refer to the MC68HC05L11 Product Preview, the MC141516 and MC141518 Product Preview and the M68HC05L11EVM Evaluation Module User's Manual for more information.

MC141518EVK

Product Information

MC141516/18 Evaluation Kit

Introduction

The MC141518EVK is an Evaluation Kit for MC141516 & MC141518 LCD drivers evaluation and for prototypes development using these drivers. This module consists of MC141516, MC141518 LCD drivers and a 240 x 60 pixel LCD panel. This EVK board can be connected directly to M68HC05L11EVM,which is an evaluation module providing control signals and display data from MC68HC05L11 MCU to the LCD Drivers MC141516 & MC141518. Any character or graphic pattern can be displayed on the LCD panel through software control.

Packing List

The package includes:
- an evaluation kit MC141518EVK
- an Adapter Board
- a 20 pin cable

Features

- 240x64 display size
- On board voltage divider provides high voltage bias to drive the LCD
- Flexible data loop configuration allows 80 column, 160 column or 240 column display
- Optional on-chip LCD timing generator

Setup and Operation

Simple Setup

The simple setup is shown in Figure 1.

Supply

The Adapter Board requires two supply voltage : +15V for VLCD, +5V for VDD and also a common ground with the EVM supply.

Contrast of LCD panel

The variable resistor, VR1, is used to adjust the contrast of the LCD panel.

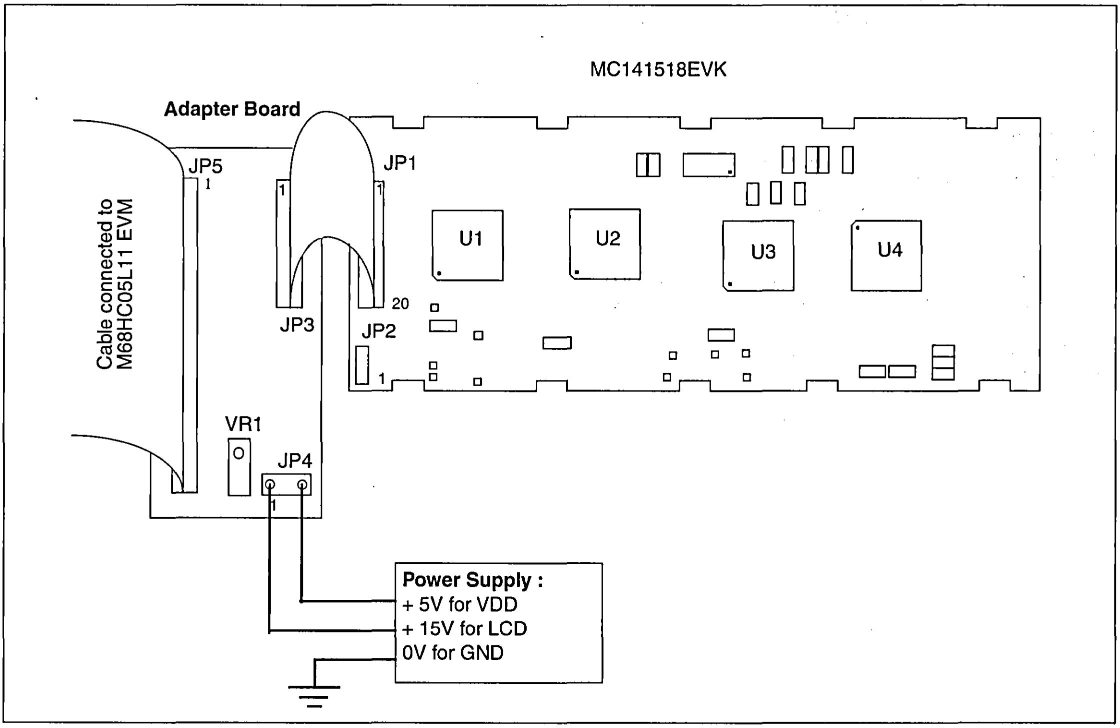

Figure 1. MC141518EVK to MC68HC05L11EVK Setup and Cabling

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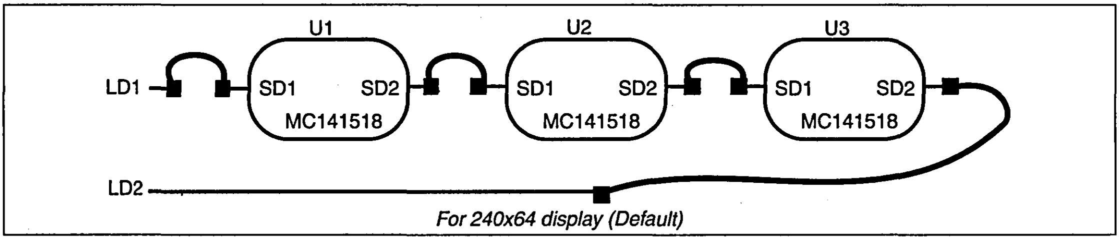

Figure 2a. The hardwire for 240 column

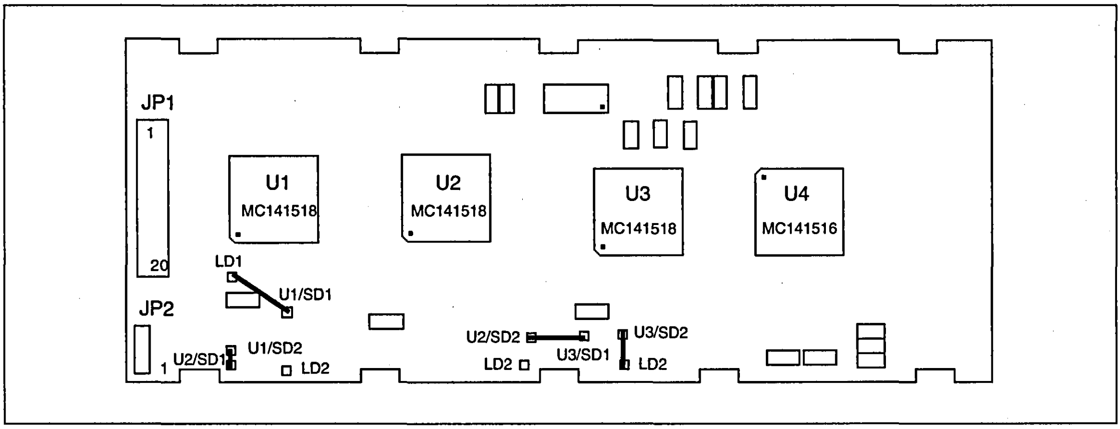

Figure 2b The hardwire for 240 column

Data Loop Configuration

The number of columns of the LCD panel can be altered by re-connecting the data loop using hardwire. By default, the number of columns is 240. However, it can be changed to 160 or 80.

For 240 column configuration, connect the LD1 to U1/SD1, U1/SD2 to U2/SD1, U2/SD2 to U3/SD1 and U3/SD2 to LD2.

For 160 column configuration, connect the LD1 to U1/SD1, U1/SD2 to U2/SD1 and U2/SD2 to LD2.

For 80 column configuration, connect the LD1 to U1/SD1, U1/SD2 to LD2.

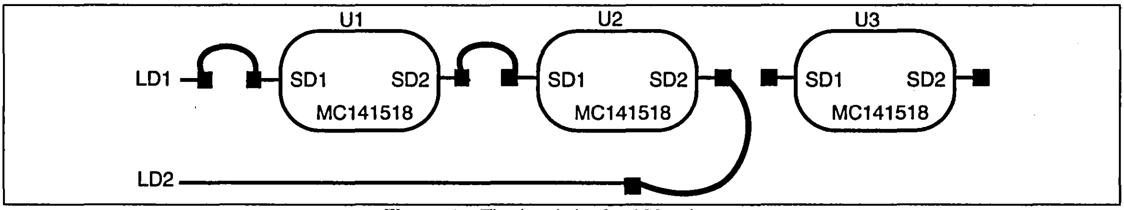

Figure 3a. The hardwire for 160 column

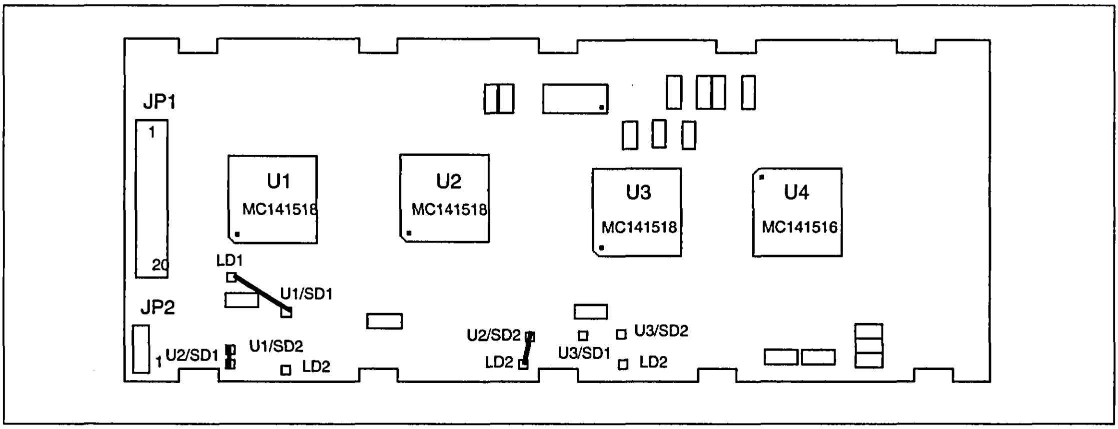

Figure 3b. The hardwire for 160 column

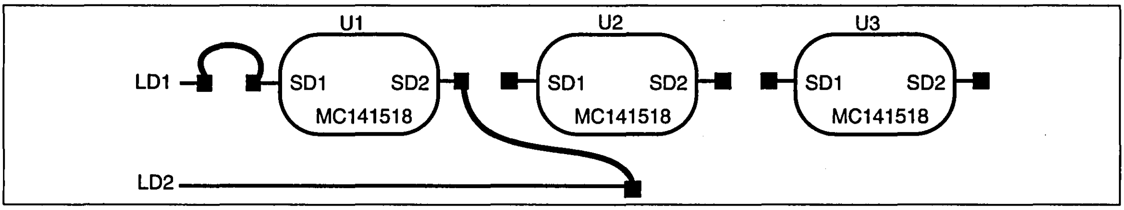

Figure 4a. The hardwire for 80 column

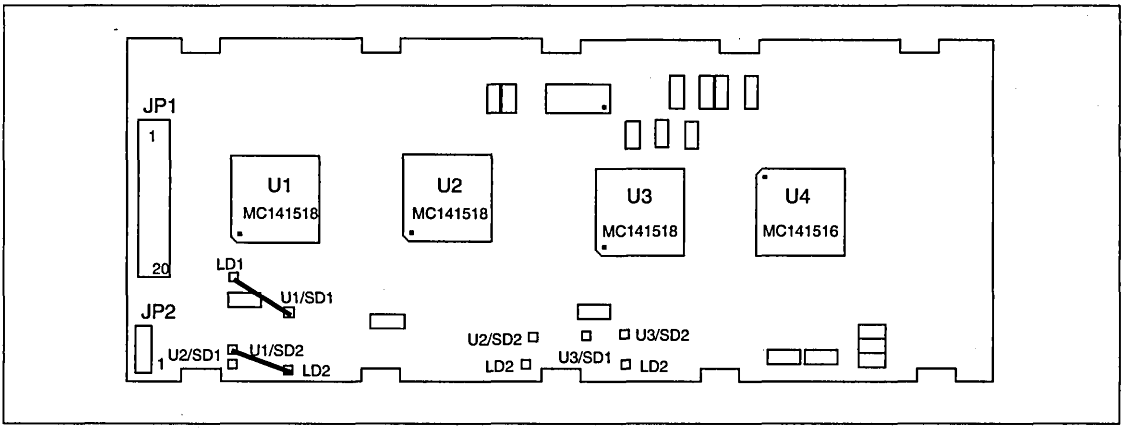

Figure 4b. The hardwire for 80 column

Setup on-chip LCD timing generator

There is a on-chip LCD timing generator on MC141516 which provides the BPCLK, FRM and M for whole LCD system. By default, it is disabled when the EVK works with MC68HC05L11 MCU. However, it can be enabled by setting the jumper JP2 on the MC141518EVK when the EVK works with other MCU through the serial interface.

Disable the LCD timing generator : (Default)

Connect pin 2 & pin 3 of JP2 jumper as shown in Figure 5a.

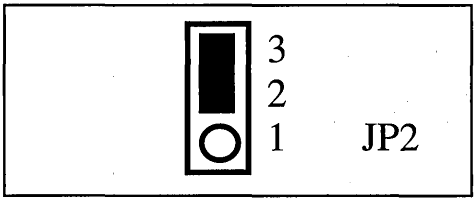

Figure 5a. Disable the LCD timing generator

Enable the LCD timing generator :

Connect pin 1 & pin 2 of JP2 jumper as shown in Figure 4.5b.

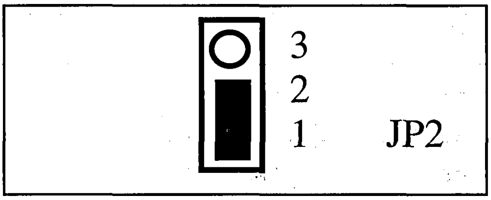

Figure 5b. Enable the LCD timing generator

Simple test for the EVK

The following is a simple test procedure used to check the functionality of the MC141518EVK.

a) Connect the MC141518EVK to the EVM
b) Connect the EVM to the PC
c) Turn on the supply (VDD = 5V, VLCD = 10V)
d) Turn on the LCD by following command :

Command	Description
C:\EVM05> EVM05	Execute the EVM05 in the PC Dos prompt
> MM 32	Modify the Control Miscellaneous Register at $32
= 81.	Set display on
> MM 31	Modify MUX Register at $31
= 3F.	Set the MUX Register to 63

e) Adjust the VLCD gradually from 10V to 15V and observe the LCD
If random pattern displayed, the EVK is OK. If not, check the connection and repeat the procedure (d) to (e).

Reference

Please also refer to the MC68HC05L11 Product Preview, the MC141516 and MC141518 Product Preview and the M68HC05L11EVM Evaluation Module User's Manual for more information.

Hardware Configuration

The hardware configuration of the MC141518EVK is shown in Figure 6a.

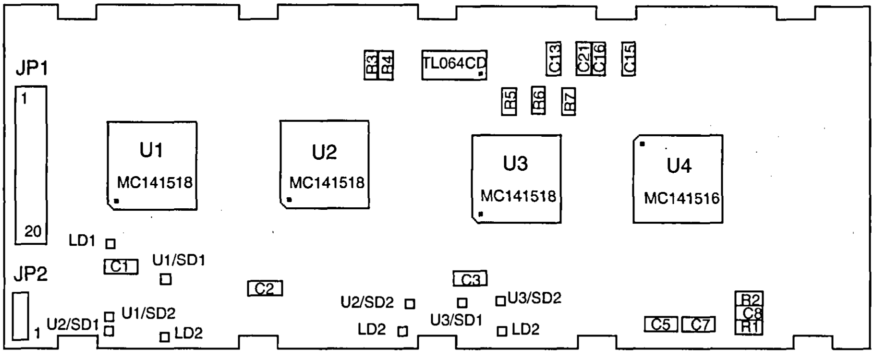

Figure 6a. Hardware configuration of the MC141518EVK

- JP1: Connect to MC141518 Adapter Board for receiving control signal and display data.
- JP2 : Select internal / external LCD timing generator.

The pin assignment of JP1 is shown in Figure 6b

	1	2	V1
	3	4	DOFF
	5	6	SHCLK
	7	8	FRM
	9	10	ID
	11	12	DDIR
	13	14	BPCLK
	15	16	$\overline{\text{BS}}$
VDD	17	18	SD1
GND	19	20	SD2

Figure 6b. Pin assignment of JP1

The hardware configuration of the MC141518 Adapter Board is shown in Figure 6c.

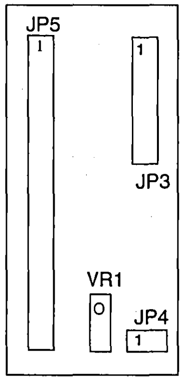

Figure 6c. Hardware configuration of MC141518 Adapter Board

- JP3 : Connect to MC141518 EVK for sending control signals and display data.
- JP4 : Connect to power supply (VLCD).
- JP5 : Connect to M68HC05L11 EVM Evaluation Module.
- VR1: Alter the brightness of the LCD panel.

The pin assignment of JP3 is shown in Figure 6d

	1	2	V1
	3	4	DOFF
	5	6	SHCLK
	7	8	FRM
	9	10	CR1
	11	12	DDIR
	13	14	BPCLK
	15	16	$\overline{BS0}$
VDD	17	18	LD1
GND	19	20	LD2

Figure 6d. Pin assignment of JP3

The pin assignment of JP4 is shown in Figure 6e.

1	2	3
VLCD		VDD

Figure 6e. Pin assignment of JP4

The pin assignment of JP5 is shown in Figure 6f.

	1	60	
	.	.	
	.	.	
	.		
	.		
DDIR	13	48	
FRM	14	47	GND
BPCLK	15	46	DOFF
ID	16	45	GND
	17	.	
	18	.	
SHCLK	19		
$\overline{BS}$	20		
SD1	21		
SD2	22		
	.		
	.		
	.		
	.		
	30	31	

Figure 6f. Pin assignment of JP5

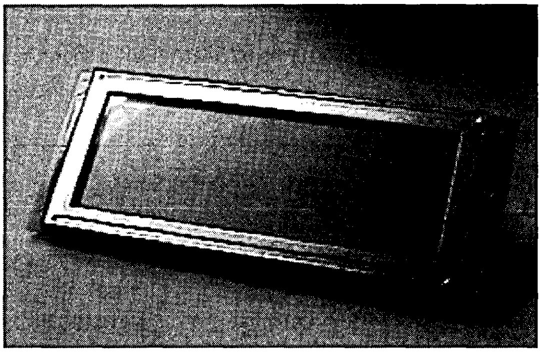

Figure 7. The MC141518EVK Outlook

MC141537EVK

Product Information
MC141537 Evaluation Kit

The MC141537EVK is a demonstration of the MC141537T1 works with a 120 x 16 LCD panel. In addition, three annuciators (icons) can also be seen in the left of the LCD panel. Figure 1 shows the outlook of the EVK.

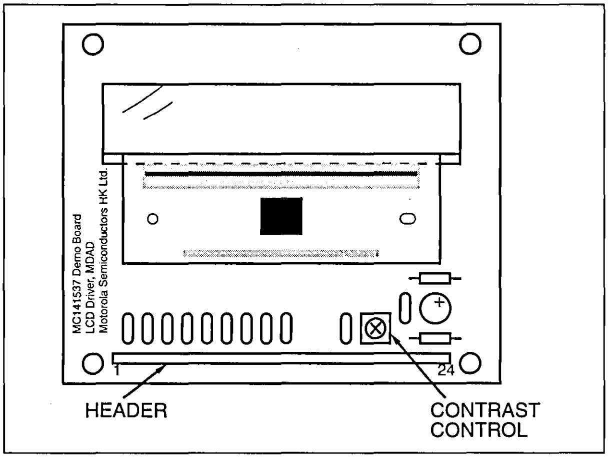

Figure 1 EVK Outlook

The EVK is composed of essential external components of MC141537. There is one contrast control variable resistor indicated in the figure to control the contrast level of the LCD panel. There is a header used to connect the external control from MCU. For the pin assignment of the header, please refer to the EVK Header/Connector section.

EVK Control

Function Control

The header on the EVK is used to control the MC141537 to perform the function desired.

Contrast Control

The contrast control is performed by tuning variable resistor on the upper board as shown in the figure. For lower contrast, turn the VR anti-clockwise; for higher contrast, turn the VR clockwise.

EVK Header/Connector

The header is used to connect the MCU signal to the EVK board. The pin 1 position is marked on Figure 1. The pin assignment of the header is as follow:

Function	DV_{DD}	$\overline{RES}$	NC	$D/\overline{C}$	$R/\overline{W}$	$\overline{CS}$	DV_{SS}	D0	D1	D2	D3	D4	D5	D6	D7	CE	AV_{DD}	AV_{SS}	V_{CC}	NC	NC	NC	NC	NC
Pin Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

The users can use the upper board to build prototype application that matches the pin out stated above.

Troubleshooting

No display

Check the Connection of DVDD, DVSS,AVDD, AVSS

Only icons display

Turn the contrast control VR clockwise to increase the contrast level.

All black display

Turn the contrast control VR anti-clockwise to decrease the contrast level.

Missing Segment

Bad contact from the MC141537T1 TAB to the LCD panel. (Return to factory for replacement)

Caution: Keep the outer leads of the TAB away from touch or they will be damaged.

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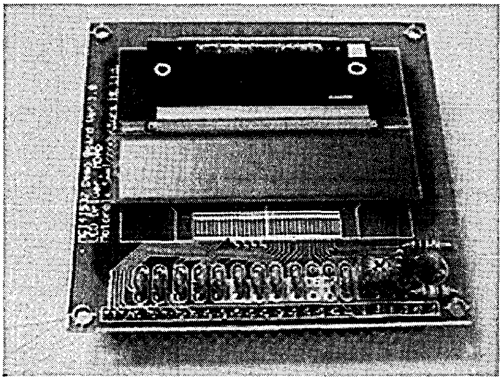

Figure 2a

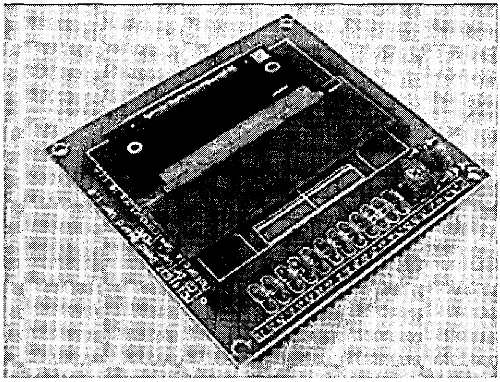

Figure 2b

Figure 2a, 2b The outlook of MC141537EVK (The EVK shipped may have difference)

MC141539EVK

Product Information
MC141539 Evaluation Kit

The MC141539EVK is a demonstration of the MC141539T1 works with a 120 x 32 LCD panel. In addition, four annuciators (icons) can also be seen on the left of the LCD panel. Figure 1 shows the outlook of the EVK.

The EVK is composed of essential external components of MC141539. There is one contrast control variable resistor indicated in the figure to control the contrast level of the LCD panel. There is a header used to connect the external control from MCU. For the pin assignment of the header, refer to the EVK Header/Connector section.

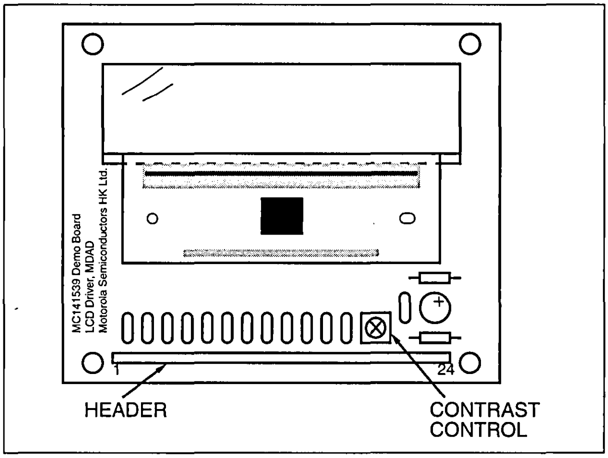

Figure 1 EVK Outlook

EVK Control

Function Control

The header on the EVK is used to control the MC141539 to perform the function desired.

Contrast Control

The contrast control is performed by tuning variable resistor on the board as shown in the figure. For lower contrast, turn the VR anti-clockwise; for higher contrast, turn the VR clockwise.

EVK Header/Connector

The header is used to connect the MCU signal to the EVK board. The pin 1 position is marked on Figure 1. The pin assignment of the header is as follow:

Function	DV_{DD}	$\overline{RES}$	NC	$D/\overline{C}$	$R/\overline{W}$	$\overline{CS}$	DV_{SS}	D0	D1	D2	D3	D4	D5	D6	D7	CE	AV_{DD}	AV_{SS}	V_{CC}	NC	NC	NC	NC	NC
Pin Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

The users can use the board to build prototype application that matches the pin out stated above.

Troubleshooting

No display

Check the Connection of DVDD, DVSS,AVDD, AVSS

Only icons display

Turn the contrast control VR clockwise to increase the contrast level.

All black display

Turn the contrast control VR anti-clockwise to decrease the contrast level.

Missing Segment

Bad contact from the MC141539T1 TAB to the LCD panel. (Return to factory for replacement)

Caution : Keep the outer leads of the TAB away from touch or they will be damage.

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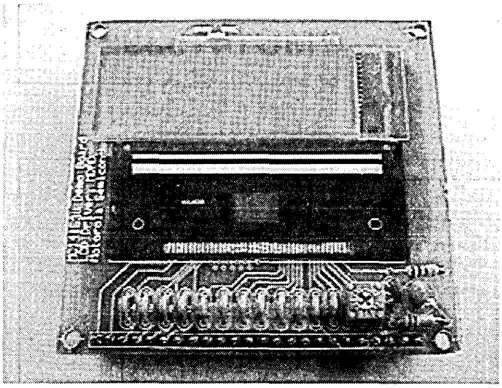

Figure 2a

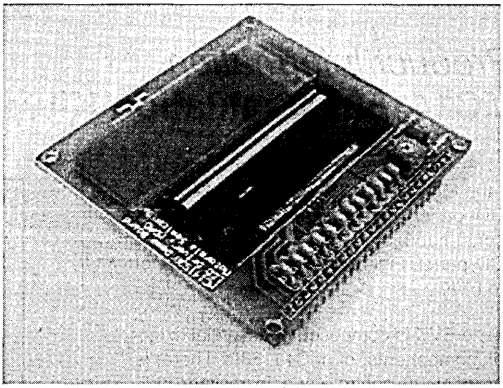

Figure 2b

Figure 2a, 2b The outlook of MC141539EVK (The EVK shipped may have difference)

MC141563EVK

Product Information
MC141562/63 Evaluation Kit

The MC14163EVK is a demonstration of the MC141562 and the MC141563 works with a 320 x 200 LCD panel. Figure 1 shows the layout of the EVK.

The EVK is composed of essential external components of two MC141562 and four MC141563. There are 14 golden pads used to connect the external control from MCU. For the pin assignment, refer to the EVK Control Pin Assignment section.

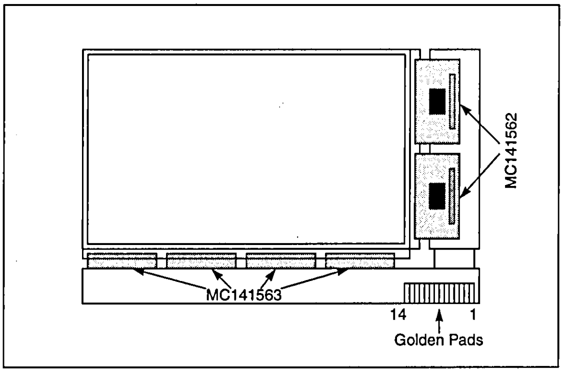

Figure 1 EVK Layout

EVK Control

Function Control

The Control Pins on the EVK is used to control the LCD module to perform the function desired. For the detailed information of the control signals, please refer to the data sheet of MC141562 and MC141563.

Contrast Control

The contrast control is performed by adjusting the VO pin on the LCD module as shown in Figure 2. VO is the voltage supply to the internal LCD bias circuit.

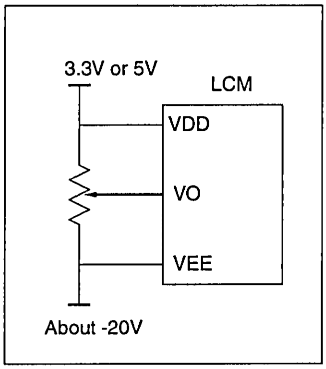

Figure 2 Contrast Control

EVK Control Pin Assignment

There are 14 pads used to connect the MCU signal to the EVK board. The pad 1 and 14 are marked on Figure 1. The assignment of the pads are as follow:

Pin Name	LACD	LFRM	LLP	LCLK	VO	VDD	VSS	VEE	LD3	LD2	LD1	LD0	VSS	$\overline{\text{DISPOFF}}$
Pin Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Connection to MC141562	M	EIO4*	SCLK	-	-	VDD	VSS	VEE	-	-	-	-	VSS	$\overline{\text{DIS-OFF}}$
Connection to MC141563	M	-	LP	SCLK	-	VDD	VSS	VEE	D3	D2	D1	D0	VSS	$\overline{\text{DIS-OFF}}$

The users can use the board to build prototype application that matches the pin out stated above.
* Only connected to the EIO4 of the lower MC141562 indicated in Figure 1.

Troubleshooting

All black display

Try to adjust the contrast to decrease the contrast level.

Missing Segment

Bad contact from the TAB to the LCD panel. (Return to factory for replacement)

REV 0 12/96 **Caution : Keep the outer leads of the TAB away from touch or they will be damage.**

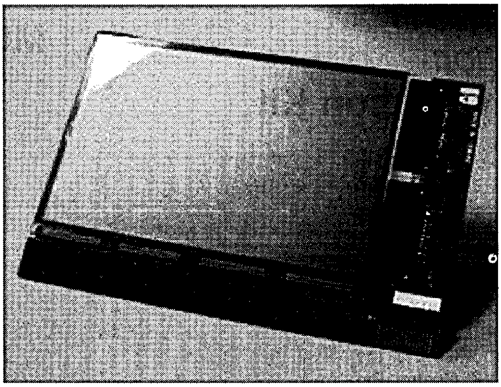

Figure 3 The outlook of MC141563EVK

Application Notes and Technical Articles 6

AN1713

Application Note

LCD Driver for Mobile Application

Advanced Digital Consumer Division - Display Products
Motorola Semiconductors Hong Kong Ltd.

W.M. Lo, Vincent W.S. Wong, Humphrey Leung, Stephen Cheung

Abstract

Traditionally, the LCD driver chip has been playing the simple role of signal driving for LCD panels. However, with the recent trends in mobile applications, such as cellular and pager, moving towards highly integrated, compact, lightweight, with a long-battery life, both the function and package considerations of the LCD driver chips are becoming critical to fulfil the requirements of the new generation mobile communication applications. This paper will present the requirements and design of the LCD driver chip for mobile communication applications.

Introduction

Due to the increasing features and performance of the new generation mobile communication devices, the conventional simple LCD driver design cannot satisfy the requirements. Important features like power saving, small size, light weight, high display quality and a bigger screen should be integrated into the LCD driver chip to increase the performance and lower the cost of the mobile communication device.

Besides the chip design, package design is also important for mobile communication devices. Over the last few years, conventional SMT as a QFP package has emerged as the new generation, high density surface mount solution to the hand held applications. However, for high performance mobile communication applications, the display panel requires 120 segment, 33 common, many icons and other input control pins. The conventional 208 QFP package, which is costly and big in physical size, cannot easily fulfil the application requirement. The TAB (Tape Automated Bond) package is the most suitable solution for LCD driver mobile communication applications. TAB, which is made out of flexible film-type material, can provide a very thin package (<1mm). The TAB package can be folded to the back side of the panel to minimize space. A custom-made TAB package can fully utilize the spacing inside the mobile communication device. The package cost of TAB is low compared to a QFP package for high pin count device.

Due to the increased demand and lower cost in personal communication services, cellular and pager are moving to new generation with more features and usage. The new generation will be commercialized to all classes of people such as students, housewives, doctors, ... etc. Several requirements are important for the new generation mobile communication devices:

- Good display quality
- Long battery life
- Greater portability
- Light weight
- Low Cost

LCD Driver Configuration

The heart of the mobile communication device is a microcontroller which controls the operation of the system. The other components are an LCD screen, decoder, RF block, DC-DC converter, memory chips (RAM/ROM), buttons, and back-light.

Among all the components inside the mobile communication system, the display acts a very important role. End users of the communication products may pick their choice of products mainly because of the quality and the amount of information they can get from the display. A well designed LCD driver not only provides better display quality, but it also increases display features. It provides greater portability to achieve the requirements for a high-performance mobile communication systems. Sophisticated all of which built-in LCD driver designs include low operation voltage, power saving mode, internal oscillator, many icons, DC-DC converter, contrast control, temperature compensation and graphic mode operation. These features all achieve the new generation requirements.
Figure 1 shows the MC141532 LCD driver design which incorporates all the important features in a chip.

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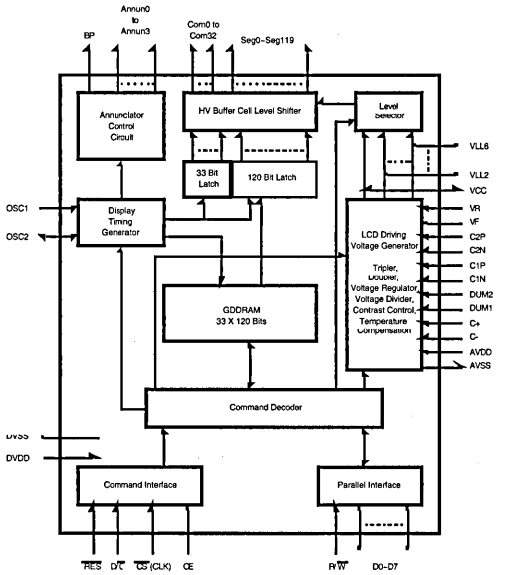

Figure 1. MC141532 LCD Driver Block Diagram

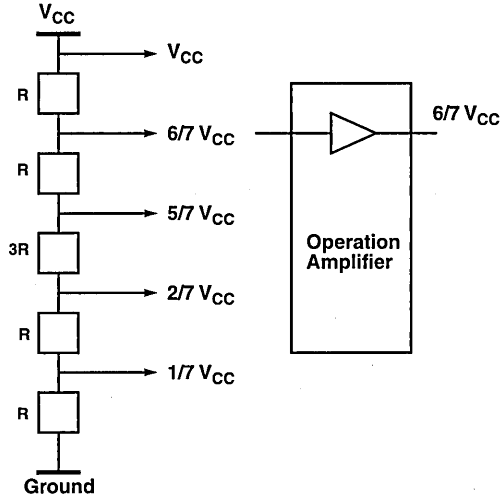

Figure 2. Resister Ladder Voltage Divider

LCD Driver Design Consideration

Voltage Divider

In order to reduce the system cost of the mobile communication system, a DC-DC converter and a voltage divider have to be integrated inside the LCD driver. In order to drive an LCD panels in multiplex ratios of 33, five voltage levels are required for a "1:7 bias" driving scheme. The supply voltage is divided into "1/7", "2/7", "5/7" and "6/7 "of the supply voltage.

To generate five voltage levels, the resistor ladder is the simplest way and is usually used as shown in figure 2. The five voltage levels are used to generate multi-level waveform to charge the capacitance of the LCD pixels. To get a high enough current, the resistance of the resistor ladder must be low. In this way, the D.C. current through the resistor ladder is high. A typical LCD driver supply using resister ladder design in a 120 x 33 pixel panel consumes 200uA D.C. current.

To reduce the D.C. current, an operational amplifier is usually added to the output of the resistor ladder. However, this method fails to reduce the D.C. current. When an operation amplifier is integrated into a chip, it is difficult to make the amplifier stable if the D.C. operating current of the amplifier is too low. Using this design in a 120 x 33 panel consumes about 50uA D.C. current even though a very careful design was used. On the other hand, the CMOS operation amplifier consumes a bigger chip area compared to resistor ladder itself. The chip cost will be higher for bigger chip area.

To overcome the high DC current and high chip cost problem, a design technique using switching capacitors is employed. Under the switching capacitor design techniques, a typical circuit in a 120x33 panel consumes only 5uA DC current.

Temperature Compensation

For highly multiplexed LCD, the operating temperature range may be restricted from 0 to 50°C if the driver voltage is fixed. The purpose of temperature compensation, as shown in figure 3a, is to automatically adjust the level of driving voltage (Vlcd) to the LCD panel under different temperature environments. The threshold voltage of the liquid crystal has a negative temperature coefficient characteristic typically -6mV/°C. The required driving voltage will have to be lowered for higher temperature. In order to maintain the display quality of the LCD panel of different LC material for a wide range of operating temperature, a temperature gradient selection circuit is incorporated in to the voltage generator of the LCD driver circuit, as shown in figure 3b. This provides a negative compensation for different types of liquid crystal glass.

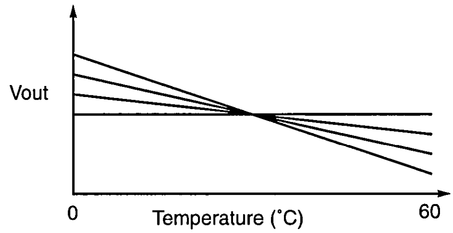

Figure 3a. Temperature Compensation

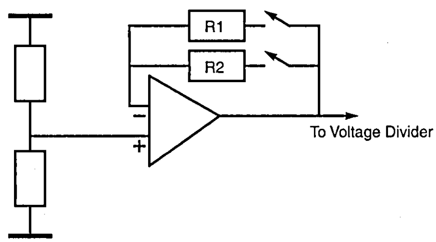

Figure 3b. Concept of Temperature Compensation

Power Saving Mode

For the mobile communication device, it works over 95% of the time in stand by mode. Most of the functional blocks of the device can be turned to stand by mode to save power at this time. What means stand by mode to the LCD is to display limited but sufficient information to the user. So the LCD driver is still displaying and working. To make the "stand-by current" minimum, special icon driving scheme have to be introduced to reduce the current.

1. Static Icon Mode

It is implemented by adding the one common and few segments drivers separated from the main matrix display. Under this mode, all other common and segment outputs will be disabled. Only these additional icon driving pins drive the icons on the screen. This "one Mux" scheme use no high voltage level to drive the LCD icons, and the driving frequency is reduced. So very low power is dissipated by the LCD driver in this mode.

2. Low Power Icon Mode

Unlike Static Icon Mode, this scheme does not employ additional I/O pins. This driving method is to use one of a selected common output from the main matrix display of the LCD driver to drive the icons. And this common output will stay on while other will be off by a special screen off command. The scheme does not need DC/DC converter stay on neither so as to save more power. This Icon Mode is especially useful in higher information content display in the stand by mode, like the clock display, battery level or even signal level. This mode also use no high voltage to drive the icons and the driving frequency is reduced. So the power dissipated is much lower than the running mode.

Using this two special icon modes, designer can implement a two step smart stand-by mode in order to get a larger flexibility in the power saving feature.

TAB Package For Pager LCD driver

QFPs were initially used for LCD drivers, but the TAB package is becoming the mainstream today. The leadcount of LCD panels for a two line alpha numeric Chinese character display is around 120 pins for segment input and 33 pins for common input. The lead pitch of input leads of LCD panels is typically 0.2 - 0.3mm. This application requires the LCD driver of around 200 leadcounts. In order to achieve the low cost and portable target, the conventional big size 208 QFP package is not a suitable candidate for mobile communication applications. The TAB package is a very thin and light package. It is the most suitable package for the application using LCD. The TAB package is expected to grow rapidly in the LCD application because existing QFP packages cannot meet the requirements of high leadcount, small body size and low cost.

The Chip On Board (COB) method is currently used by many manufacturers. In COB, a wire bonding technique is used to make the connection between the LCD driver chip and the PCB. The panel is then connected to the PCB by using a heat seal cable (HSC) as shown in figure 4. This method has been providing a low cost solution for signal connection. The recent applications require a much higher LCD driver leadcount. Under this condition, the pad pitch of the chip is then reduced to become smaller. The fine pad pitch of the chip is becoming a limiting factor for wire bonding the chip on the PCB. The wire bonding of high pin count and fine pad pitch (< 4.0mil) LCD driver chips on PCB will cause assembly yield and quality problems which increases the manufacturing cost. The following is the comparison of minimum pad pitch design between inter-lead bonding (ILB) of TAB technology and wire bonding technology.

	Minimum Pad Pitch
TAB	2.0 - 3.0 mil
Wire Bonding (Al wire)	3.3 - 3.5 mil
Wire Bonding (Au wire)	3.5 - 4.0 mil

Reliable information delivery and robustness of the display is very important for a personal communication device. The TAB package that can provide excellent reliability performance for fine pad pitch and high pin count IC bonding is the most appropriate package for the mobile communication LCD driver application.

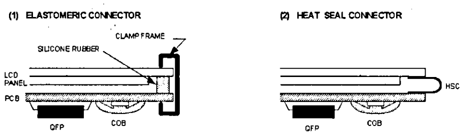

Figure 4. Connection Method for LCD Driver Chip

Advantage of Using TAB

The LCD driver chip is packaged into a tape film, commonly known as the TAB package, figure 5. As the thin film provides a high degree of flexibility like a flexible printed circuit (FPC), it is also used as the connector between the LCD panel and the PCB as shown in figure 6. This direct connection simplifies the manufacturing process and the end product design. The advantages of using the TAB package are:

- Package is light weight and thin,
- High leadcount but small package size,
- Flexibility and foldability (The LCD driver is a TAB package can be folded 90 or 180 degree from the mounting edge of the LCD panel.),
- Less PCB board space and cost (since the driver IC is now part of the PCB / LCD connector.)

Simplified interconnect process (It combines the IC placement and PCB / LCD interconnection processes into a single heat seal process. TAB may also be used in conjunction with HSC for a more flexible connection layout.)

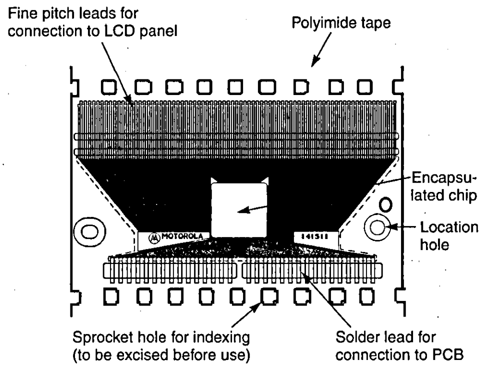

Figure 5. LCD driver in TAB package

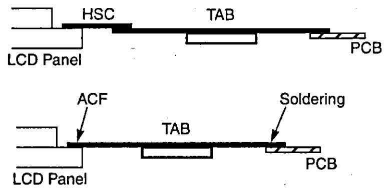

Figure 6. Connection methods for LCD driver TAB

Conclusion

Since the displayed features and display quality of the new generation of mobile communication devices are becoming so important for sales. LCD and the drivers is very important as to differentiate the product. Sophisticated features of LCD driver designs (including low operation voltage, current saving mode, internal oscillator, DC-DC converter, contrast control, temperature compensation, character and graphic mode operation) can achieve the new generation requirements. On the other hand, as the display density increases, like the multiple lines alpha-numeric application, more I/O connections from the driver ICs required. TAB offers a unique combination of high reliability, high packaging density and excellent manufacturability that will result in increased usage on mobile communication LCD driver applications.

Acknowledgment

James Y.S. Lei, William K.W. Wong, K.K. Leung, Jeco Pang, Andrew Kung, Benjamin Liu, George Lien

Reference

[1]O.L Chau, C.N Yan "Dual TAB Application - LCD Driver," Fifth International TAB/Advanced Packaging Symposium., pp.20-24, Feb., 1993.

[2] Motorola Semiconductors Hong Kong Limited, "MC141538 LCD Driver Data Sheet", Oct 1993.

Slim TAB Package for Flat Panel Display Applications

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Abstract

Owing to the fast growing demand of flat panel display on hand held electronic products such as pager, cellular, PHS, PDA, organizer, notebook, LCD-TV, etc., the shift from plastic molded quad flat packages (QFPs) and die bonding, which have been the mainstream package in wire bonding for display driver, to TAB packages is proceeding rapidly. Tape automated bonding (TAB) tape is now widely used for display drivers. TAB is compact, light weight, thin, flexible and idea for a high pin count device.

Cost is being recognized as one of the important factors on the display industry. The cost consideration is not only the display driver itself but also the manufacturing and system cost of the display system. With the appropriate design of TAB package for the application, high performance with a low system cost can be achieved.

Introduction

Nowadays, quality and reliability are a kind of must in each IC package. Regarding to technology, it is highly relied on the development of new material and equipment. More or less, each supplier will provide similar quality, reliability and technology IC package to its customers. The only way to put itself in a better position in the market is to drive down the total system cost of the display system. IC packaging is one of the big areas for cost reduction because packaging can represent a large percentage of the total system cost.

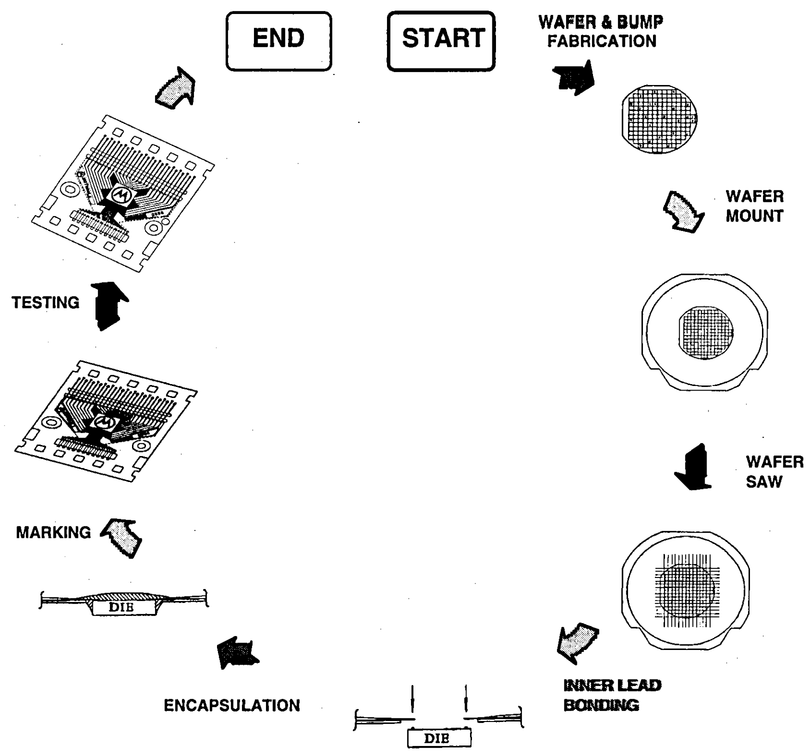

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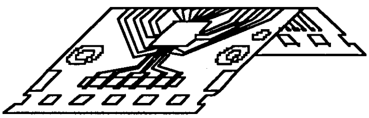
Figure 1. LCD TAB Manufacturing Flow

LCD TAB Manufacturing Process Flow

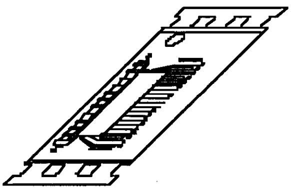
Basically, TAB manufacturing flow, Figure 1, is quite simple when comparing with that of conventional package like PDIP, QFP & so on. It is because the manufacturing steps in semiconductors house are fewer. It only involves wafer mount, wafer saw, inner lead bonding, encapsulation, marking, oven curing and testing. For the wafer mount and saw processes in TAB manufacturing flow, they are the same as those of conventional packages. The inner lead bonding & encapsulation processes can be treated as die bonding plus wire bond processes & molding process respectively. Dejunk, plating, trim & form processes are no more required in TAB manufacturing.

Slim TAB vs. Conventional TAB

The most significant change in the LCD application is the adoption of slim TAB. The TAB LCD driver IC has been modified to minimize the overall size of the display. For example, instead of using a chip that is 5mm x 5mm, a slim rectangular die of size 1.5mm by 17mm is bonded to a TAB tape that has a total width of only 9mm. This greatly reduces the size of the TAB tape bonded to the edge of the glass panel. Conventional TAB with folding window and slim TAB package are shown in Figure 2.



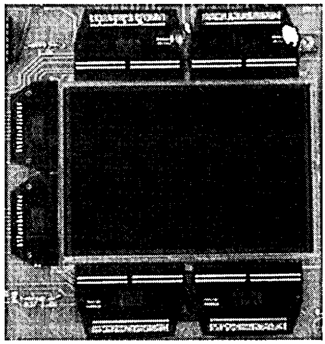
Conventional TAB (folding)



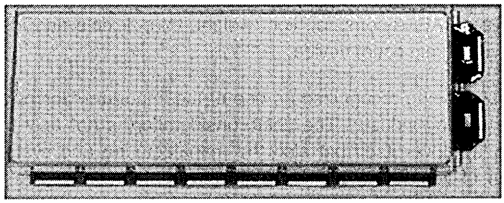
Slim TAB

Figure 2. Different TAB Packages

In applications, the slim TAB provides a narrow width that will reduce the overall size of the LCD module as show in Figure 3. By using a conventional TAB package, the size of the LCD module is increased.



Conventional TAB application



Slim TAB application

Figure 3. Conventional TAB vs. Slim TAB applications

One important effect of slim TAB is reduction in TAB tape material consumption. Slim TAB uses two or three sprocket holes of tape comparing to five or six for conventional TAB. The TAB package cost can also be reduced by using less TAB tape material. Especially for color LCD applications, the use of slim TAB could almost offset the cost increase on three times the number of TAB LCD drivers. As shown in Figure 5, the die of size 6.2 x 6.4mm will consume more TAB tape material that will cost higher. The TAB package cost will decrease when the larger aspect ratio die is employed. However, when the aspect ratio goes up to a certain value, say 1.5mm x 27mm, the TAB tape cost will increase again because the die length exceeds the routable area of the 35mm TAB and 48mm TAB needed to be used will cost higher them.

Concerning the die cost, long aspect ratio die will increase the number of incomplete die on wafer edge. This result in a decrease in the total number of die per wafer as shown in Figure 4. For example, a die size of 4.7mm x 4.7mm (aspect ratio = 1:1) will have 330 pcs of dice per 6 inch wafer comparing to a die size with 1.4mm x 20mm (aspect ratio = 1:20) which has only 290 pcs of dice although they have the same die area.

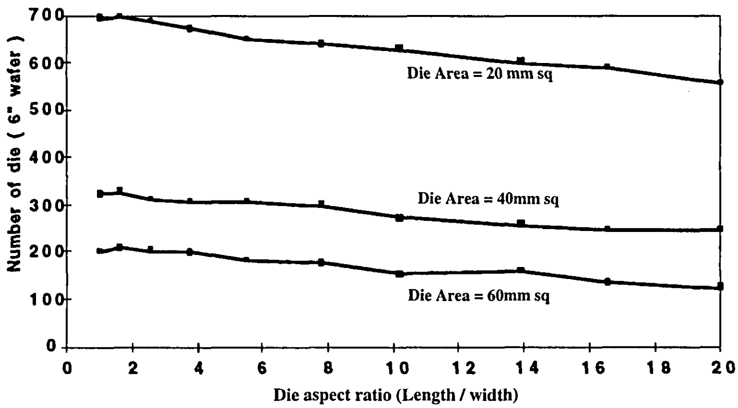


Figure 4. Die Count per 6" wafer vs. Die Aspect Ratio

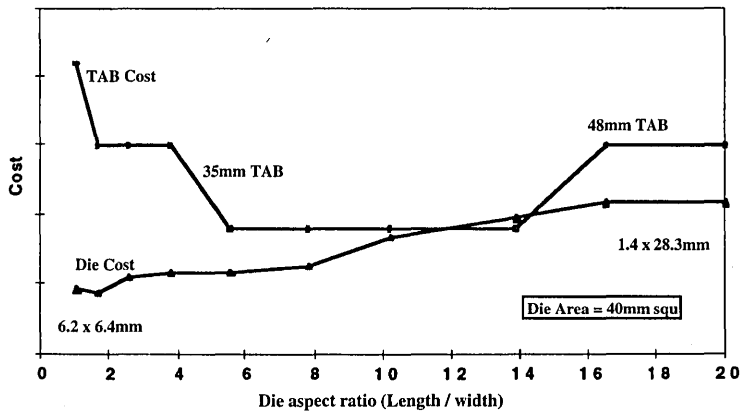


Figure 5. TAB LCD Driver Cost vs. Die Aspect Ratio

The die cost is determined by the total number of good dice per wafer. The higher the die count will decrease the die cost. The decrease in die count per wafer for long aspect ratio die will then increase the die cost of production as shown in Figure 5. Therefore, the aspect ratio of die must be carefully designed so that the total cost of the TAB LCD driver can be optimized.

TAB Design Consideration

It is very important that TAB package design is optimized with the manufacturing process and user applications. The TAB design process begins with the IC design, then progresses through gold bump design, inner lead bonding (ILB) design, outer lead bonding (OLB) design, TAB pattern design. Manufacturability, testing, cost and performance of user applications are the major guiding track on the TAB design process. Some of the main points of each design techniques are explained below:

The TAB design begins with the IC design stage. The chip layout must match with the TAB package design. The chip layout is divided into input terminals and output terminals. The input terminals will be connected to the PCB side and the output terminals will be connected to the LCD glass side. In the conventional TAB design, Figure 6a, the output terminals are placed along three or four sides of the IC chip. The input terminals will place on one side only. For slim TAB design, Figure 6b, in order to minimize the width of the TAB package, the die will have a very long aspect ratio. Many of the output terminals will place at one side and input terminals will place at the opposite side. The pad pitch of the die layout is a key factor to determine the minimum width of a slim TAB design.

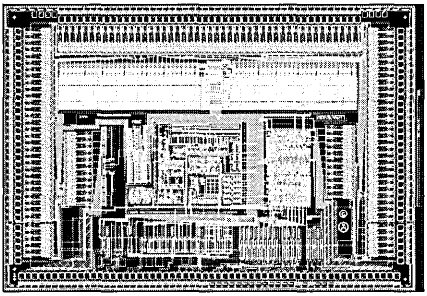


Figure 6a. Die Layout for Conventional TAB Design

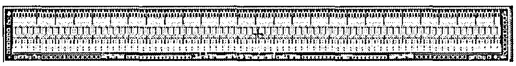


Figure 6b. Die Layout for Slim TAB Design

Also, it is important to design the layout of bond pads on chip and TAB tape for checking the electrical characteristics of the IC on wafer and on final testing stage. Owing to the cost reason, LCD driver that has very high pin count is normally a pad limited design, the smaller the pad pitch will usually consume less silicon and TAB material while the design of a pad size shape must allow accurate probing, the size of pad must be design as big as possible to provide better probing capability during electrical test stage. In order to optimize the manufacturability and cost, stagger bond pad design is used as Figure 7.

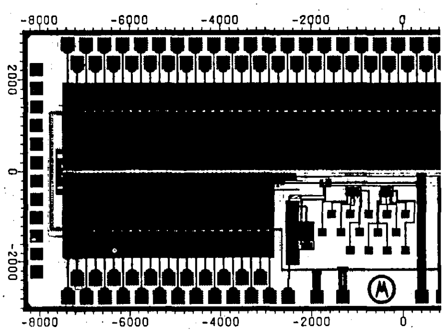


Figure 7. Stagger Pad Design

For gold bump design, Figure 8, the size of aluminum pad and overcoat will determine the optimal size of gold bump. The bump pad must be carefully designed so that it will not have lift bump or short bump problem.

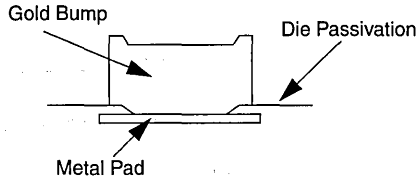


Figure 8. Bump Pad Design

For TAB tape design, the guidelines are as follows:

1) Alignment marks

Alignment marks are very useful to assist operator or vision system to align fine pitch outer lead and the indium thin oxide (ITO) electrode on panel. Normally, they are located at two sides of fine pitch outer leads. The operator or vision system is only required to align corresponding marks so that the connection between the outer lead and the ITO will be accurately formed. Of course, manual alignment and vision system assisted alignment has a little bit difference. The guide line is larger in dimension for operator (normally > 1.0 mm) and smaller in dimension for vision system (normally < 0.8 mm) which are mostly depended on machine accuracy. For vision system, the most desirable shape for alignment marks is circle or square because the center point of the alignment marks will be used as datum for alignment. Therefore, location of the center point of circle or square in shape alignment marks is easier than that of other. Example of alignment mark is showed as Figure 9.

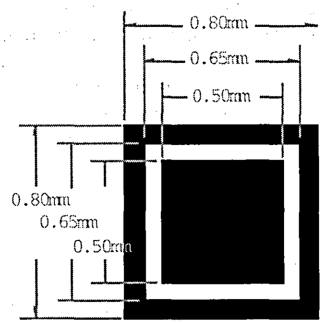


Figure 9. Example of Square Alignment Mark

2) Maximum effective area for pattern routing

Actually, maximum effective area for pattern routing is very important because it will affect the overall design and the cost. Different TAB tape formats will have different effective areas for pattern routing. Incorrect selection of format for its applications will in turn loss money because TAB package cost is heavily dominated by the TAB tape area. In other words, the more the TAB tape material being used, the higher the TAB package cost is. The Figure 10 shows the capability of one of the TAB tape manufacturers about the tape effective width and length for different TAB tape formats.

TAB TAPE FORMAT	MAXIMUM "A"	MAXIMUM "B"	NO. OF SPROCKET
35 mm STD	23.5 mm	60.0 mm	13
35 mm WIDE	25.0 mm	60.0 mm	13
35 mm SUPER	28.6 mm	60.0 mm	13
48 mm WIDE	38.0 mm	66.5 mm	14
48 mm SUPER	41.6 mm	66.5 mm	14
70 mm WIDE5	9.0 mm	66.5 mm	14

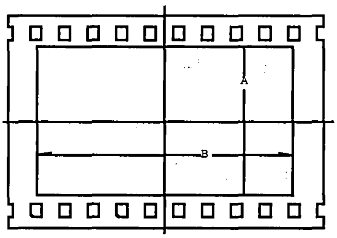


Figure 10. Maximum Effective Area For Pattern Routing

3) Folding slit

The purpose of the folding slit is to increase the flexibility of TAB package, Figure 11. The TAB package can be easily folded after mounted on the LCD panel. The distance between two slits is depended on the thickness of the panel and overall module assembly requirement. However, it should be greater than 1.0 mm and the length of the slit should be max. 42 mm along and 20 mm perpendicular the sprocket hole respectively as a guide line.

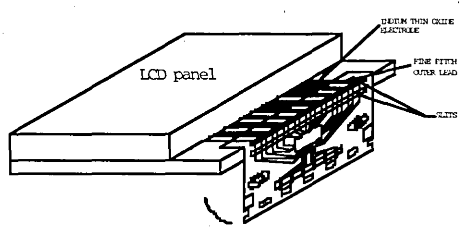


Figure 11. Application of TAB Package with Folding Slit

4) Normal design against Mirror design TAB tape

Since there are two types of inner lead bonding method regarding to the TAB tape orientation, they are named as "normal design TAB tape" and "mirror design TAB tape", Figure 12. In normal design TAB tape, the die surface is facing up and the polyimide (tape) side is facing down (copper pattern is facing up). While in mirror design TAB tape, the die surface is facing up, the polyimide (tape) side is also facing up (copper pattern is facing down). The selection requirement for normal design or mirror design is depended on the real configuration in LCD panel module assembly.

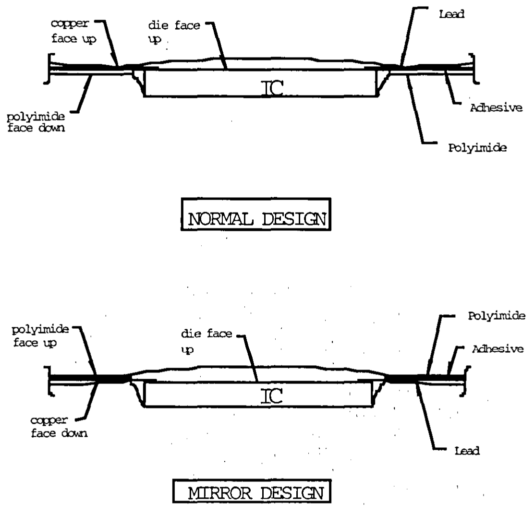


Figure 12. Normal Design vs. Mirror Design TAB Tape

5) Outer lead pitch / width / spacing

For each application, it should have its requirement in outer lead pitch, width and spacing. It is a kind of matching between TAB tape outer lead and the ITO on panel. The pitch size can be from 300 micron down to 70 micron which depends on its application. Of course the min. pitch is highly dependent on the Anisotropic Conductive Film material (ACF) and performance of the outer lead bonder. According to ACF material supplier, 50 micron pitch ACF is now being developed so as to match the min. fine pitch planned capability from some of the best in class TAB tape manufacturers. Figure 13 shows the relationship amongst outer lead pitch, width and spacing.

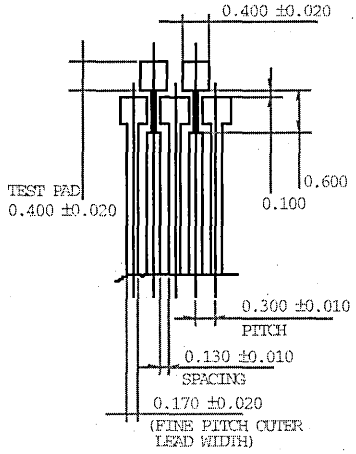


Figure 13 Outer Lead Pitch / Width / Spacing

6) Dummy lead

In order to prevent any external damage to the active outer lead, it is recommended to add some dummy leads to both ends of the outer leads, Figure 14. Even if there is any external shock to the outer leads, dummy leads can act as protection leads.

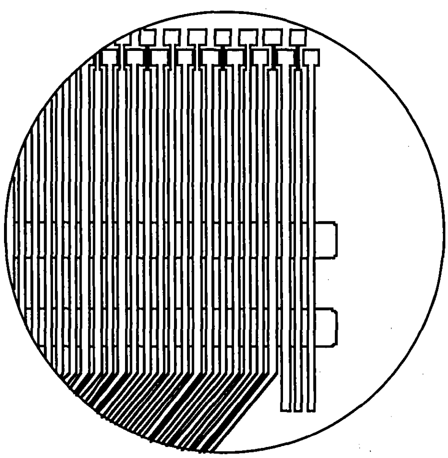


Figure 14 . Dummy Lead

7) Polyimide adhesive material

Talking about the active outer lead protection, a very thin film polyimide adhesive about 10 - 80 micron thick per side can be coated to the folding slit so that the rigidity of the overhanging outer leads can be strengthened significantly. Of course, one side coating and double side coating can be selected according to the requirement. However, the overall price per unit will be higher by 15 - 20% and 30 - 40% for one side and double side coating respectively.

8) Super slim TAB design considerations

Actually, there is no significant difference in design and inner lead bonding between normal TAB tape and super slim TAB tape. However, attention should be paid when you desire to design a super slim TAB tape and to perform inner lead bonding as follows.

a) At least 1 mm spacing is required between the edge of device hole and the slit hole for input outer lead, Figure 15. It is because enough area for copper pattern adhesion is very important especially in the area between the edge of the device hole and the slit hole so as to prevent copper peel off from the polyimide film. Copper pattern routing path and its width in this area should be maximized so as to achieve this requirement.

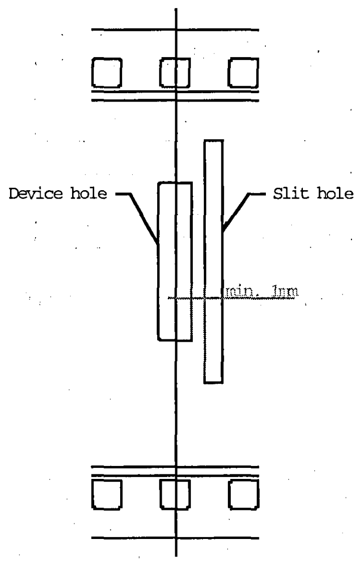


Figure 15. Spacing Requirement for Super Slim TAB Tape

b) In a super slim die, normally all output leads are arranged on top side of the die and the input leads are arranged at bottom side for the sake of easier routing. In order to keep good balance and prevent die tilting during inner lead bonding, dummy leads in input side are recommended to add so as to balance the bonding force. The suggested output leads to input leads ratio is 4: 1.

c) According to some top TAB tape manufacturers, the minimum inner lead pitch is 70 micron for super slim TAB tape in production mode at this moment.

d) In order to make the TAB tape more accurate, the center of the device hole should be located in the center line of the sprocket hole in the rolling direction.

e) Coplanarity is very important in inner lead bonding. In order to get a better bonding quality in super slim TAB package, high temperature lapping inner lead bonding tool should be used during the inner lead bonding so as to achieve enough flatness amongst tool, TAB tape & gold bump.

Future Trend

To be competitive in the display market, it is required to take care of several important things like quality, reliability, technology & total system cost. TAB systems have undergone drastic changes in design, requiring finer feature sizes and dimensions. Therefore, proper design consideration that works closely to customers in the very beginning stage is very important, especially for the IC and package design.

Nowadays, super slim TAB is a kind of new LCD driver market trend. It is because it can lower down the material cost and the overall size of the end product can be reduced. The number of pin count of TAB LCD driver is increasing from 240 to 320. This also pushing the pitch size of OLB from 70um to 50um. The copper thickness on TAB is also required to be reduced to match with the change. Thus, the successful implementation of a fine pitch TAB technology requires materials steady processes, high reliable equipment. Concerning the TAB material, since the TAB package cost is heavily depended on the polyimide tape material, a newly developed polyimide tape or its replacement material should be born so as to significantly cut down the package cost.

Acknowledgement

K.K. Leung, Gary Fung

Reference

[1] O.L Chau, C.N Yan "Dual TAB Application - LCD Driver," Fifth International TAB/Advanced Packaging Symposium., pp.20-24, Feb., 1993.

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AN1714

Application of MC14153X Integrated LCD Segment / Common Driver

Advanced Digital Consumer Division - Display Products
Motorola Semiconductors HK Ltd.

Vincent W.S. Wong

INTRODUCTION

MC14153x is a series of integrated CMOS LCD Drivers which consist of both common and segment driving outputs. It has parallel interface capability for operating with general MCU. In addition to the general LCD driver features, they also have on chip LCD bias voltage generator and temperature compensation circuit so that fewer external components are required in application.

DESIGN CONSIDERATIONS

When making use of the MC14153x series LCD driver, there are some considerations that must pay attention to:

- Display size
- Operation voltage
- Internal or external voltage divider
- Internal or external oscillator
- Internal or external contrast control
- Control signal generation D/$\overline{C}$, R/$\overline{W}$, $\overline{CS}$(CLK), CE
- TAB package

DISPLAY SIZE

The display size is one of the significant factor in choosing which LCD driver is most suitable for a particular application. The driver classified by its display size x by y dots. Note that some of the drivers in the series have multiple mux ratio, that means the driver can turn on full panel, half panel or only icon line. This can be done by issuing command to the LCD driver to change its display mode.

OPERATION VOLTAGE

The operation voltage of the driver can be single supply 2.4-3.5V. The built-in voltage multiplier will generate doubled or even tripled the input voltage (V_{DD}) and will feed it to the on chip voltage divider internally in order to generate the needed LCD driving bias voltage from the input voltage. Under this configuration, only few capacitors are required to connect to the driver to make it works (refer to Figure 1). However, user can build the voltage multiplier and even voltage divider by their own.

INTERNAL OR EXTERNAL VOLTAGE DIVIDER

It is recommended to use the internal voltage divider to generate the required bias voltage to the LCD since it can save more power and use less components. If external voltage divider is employed, the divided voltages should be fed to VLL6, VLL5, VLL4, VLL3, VLL2. These voltages should be set according to the LCD panel specification.

INTERNAL OR EXTERNAL OSCILLATOR

The LCD driver can use both internal or external oscillator. To use the internal oscillator, just connect the OSC1 pin to OSC2 pin by a resistor. The usable value of the resister varies from one driver to the other. Refer to respective data sheet for detailed description. The LCD driver can also use the external oscillator as the clock.

INTERNAL OR EXTERNAL CONTRAST CONTROL

The LCD driver consist of internal contrast control function which is an advanced feature controlled by software command. It is advised that both external and internal contrast control should be implemented during development phase. The reason is that the external contrast control is used to select a suitable contrast which can be further controlled by the internal contrast control.

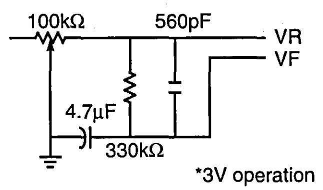

Figure 1. External contrast control

Figure 1 details the implementation of the typical application. Note that the operation voltage of the circuit is 3V and take MC141539 as the example. For other voltage or other driver, the resistor value may be different.

CONTROL SIGNAL GENERATION

The LCD driver can interface to general MPU/MCU. It is easy to control through general I/O ports. For those LCD driver have the CE pin, it can also be used in memory mapped I/O application. (Note: the CE pin of most of

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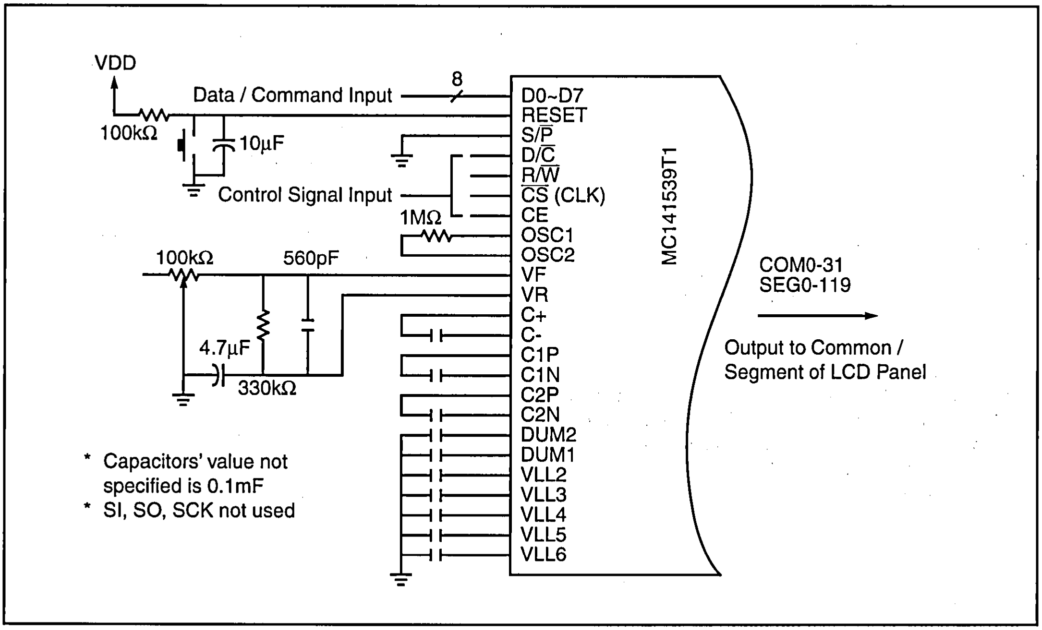

Figure 2. Typical Application of MC141539

the MC driver is active high) For dedicated I/O port control of the LCD driver, the CE can be pulled high during all the time of application. For data bus sharing purpose, CE should be pulled low when not selected as the I/O device and the data pin D0~D7 will be high impedance state. Only pull CE high when the LCD driver is selected to be a device to control.

The D/$\overline{C}$, R/$\overline{W}$, $\overline{CS}$(CLK) combine with the D0~D7 pin to form the control and data I/O block. The detail timing can be obtain in the data sheet. D/$\overline{C}$ input determines the input in D0~D7 is Data or Command. R/$\overline{W}$ input high to read display data or internal status while input low to write data or command to the LCD driver. The $\overline{CS}$(CLK) pin latches the input from D0~D7.

APPLICATION EXAMPLE

The above figure shows the typical application of the LCD driver. This example employed the MC141539T1 and it is configured as 32 MUX and 1:7 bias ratio. Also, internal divider, internal voltage multiplier and internal oscillator are used.

The interface to the MCU is parallel. The user should only take care the control signals and D0~D7 I/O. For direct I/O port control from MCU, pull CE to high. For memory mapped I/O application, the CE, D/$\overline{C}$ and $\overline{CS}$ signals are to be generated by a decoder.

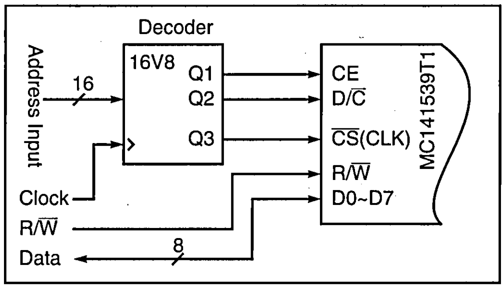

Figure 3. Memory Mapped I/O application using 16V8

In this design, there are two address in the MPU to represent the command write and the data read / write. For example, when $A0 input to the decoder, Q1 and Q2 output 1 and 0 respectively, which is a command write operation. When address input is $A1, the Q1 and Q2 pin of the decoder will both 1s, which is a data read / write operation, depending on the R/$\overline{W}$ input of the LCD driver. The Q3 pin is programmed to go high from low after one clock of Q1 and Q2 generated. And Q3 will go low from high again in next clock to latch the data D0~D7 to / from the LCD driver. Note that the MPU must wait for four clock cycles before issuing new address and data in this case.

	State 1	State 2	State 3	State 4	State 5
Clock	1	2	3	4	5
Address	A0 / A1	A0 / A1	A0 / A1	Don't Care	Ready for new address
Q1, Q2	00	10 / 11	10 / 11	10 / 11	00
Q3	0	0	1	0	0

The table above shows the states of the decoder which is programed as a state machine. The maximum clock input to the decoder depends on the timing of the LCD driver.

TAB PACKAGE

Most of the MC14153x LCD drivers are in TAB package. To use it, direct bonding to LCD panel by ACF (Anisotropic Conductive Film) or bonding to the HSC (Heat Seal Cable) and then to LCD panel are two ways to connect the LCD driver to the LCD panel.

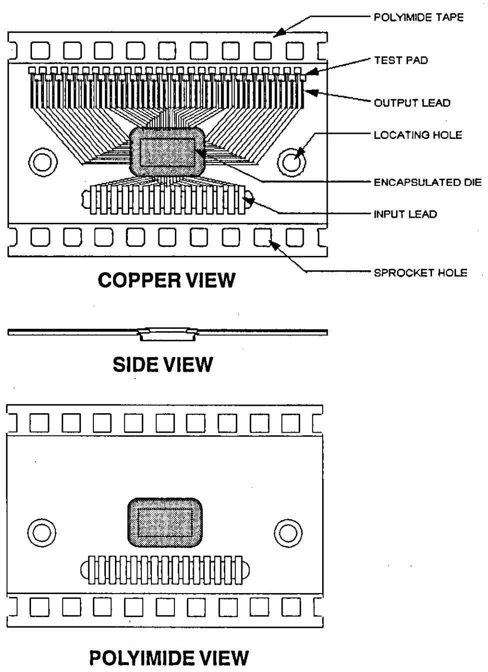

Figure 4. The outlook of TAB package

Figure 4 shows the generic TAB layout of the LCD driver. The polyimide tape is the main carrier of the TAB package. The test pads are just for testing purpose in factory and should be cut off before bonding to LCD panel or HSC. The Common and Segment outputs are on the Output Leads. The Input Leads are the control signal inputs and essential components connections to the LCD driver. The sprocket holes are the square holes on the both sides of the TAB which is used to pull the TAB package from the carrying wheel. And the locating holes are for rough alignment. To align the TAB to the LCD panel or HSC precisely, a square or cross style alignment mark will be marked on the TAB package. (Most likely located besides the both sides of the Output Leads, and not marked on the figure above). This mark will be aligned to the mark previously made on the LCD glass or the HSC.

They can also be simply cascaded to drive a display of any required size. Clearly, the number of chips and interconnections increases directly as the number of segments. This limits the practical size of a display using this arrangement. The output pin to segment connections can be chosen to suit the application. The arrangement used here has been chosen to be compatible with the 4-backplane MC145000 driver used in a later example.

The MC144115 has a three-line serial interface consisting of clock, data, and chip enable. The clock and data lines can be shared with other peripherals, provided that each peripheral has a separate enable line. The enable line can, however, be derived from the clock if no other chips share the clock and data. This method of saving an I/O line is used in application note ANE416. The MC144115 software example (listing 1) has been modified from the routine used in ANE416.

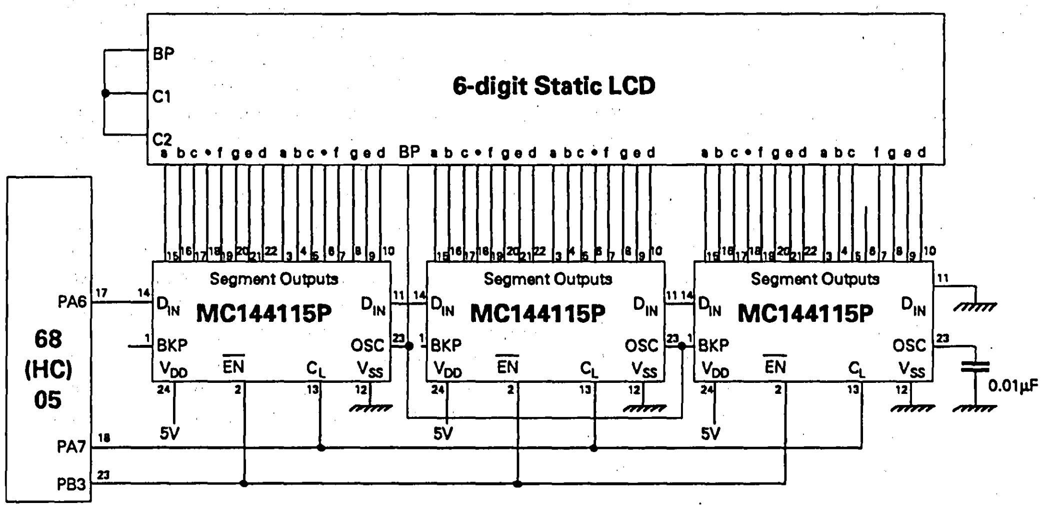

Figure 1. Single-backplane LCD display with MC144115P display drivers

AN442

Driving LCDs with M6805 Microprocessors

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INTRODUCTION

M6805 microprocessors include a wide range of parts with a large diversity of on-chip features. These include A/D and D/A convertors, serial interfaces, timers and display drivers. The display drive capability of the microprocessors range from none beyond I/O pins, through high current ports, to specialised display drivers for LCDs and vacuum fluorescent displays.

The MC68HC05M series have vacuum fluorescent drive capabilities up to 40V. The MC68HC05L series include LCD drivers with capabilities ranging from the MC68HC05L6 (3 or 4 backplanes and 24 frontplanes) through the MC68HC05L7/9 with 8 or 16 backplanes and 60/40 frontplanes. The L9's 40 frontplanes can be expanded to 205 with three MC68HC68L9 expanders.

Microprocessors without special LCD circuitry can be used to drive single backplane LCDs directly but require regular software intervention if the requirement that the display receives only AC drive is to be met. Alternatively display driver chips can be used to interface microprocessors with single and multiple backplane displays.

This application note gives hardware and software examples for these different arrangements. The same methods also apply to other families of microprocessors, eg M6801 and M68HC11. The examples are arranged in the order of the number of backplanes.

SINGLE-BACKPLANE DISPLAYS

Single-backplane displays are commonly used where the number of segments required is limited, usually using the 7-segment format. They have the advantages over multiplexed displays of superior contrast and viewing angle and a wider range of operating voltage and temperature. They can be driven directly by microprocessors with the number of segments limited simply by the number of available pins which are (or can be configured as) outputs. An output pin is required for the backplane together with one for each segment. The ports are loaded with the segment data corresponding to the required display, as with any other peripheral being directly driven by I/O lines. In this case, however, the microprocessor must complement the signals (backplane and frontplanes) at regular intervals, thus satisfying the requirement that the display receives an AC waveform with only a small DC component. It is possible for interrupts to alter the timing of these voltage reversals and the programmer must ensure that the resultant DC component does not exceed that above which the life of the display is reduced.

An alternative method of driving single-backplane displays from microprocessors is to use an LCD driver. Figure 1 shows a 6-digit 7-segment circuit using 3 MC144115P LCD drivers. These chips are driven serially and constitute a simple shift register giving the programmer full control over the display.

LISTING 1

```
                        *****************************************************
                        *                                                   *
                        *       Example program for MC144115 driven         *
                        *       single backplane display.                   *
                        *                                                   *
                        *****************************************************
00000000                PORTA   EQU     $00         PORT A ADDRESS
00000001                PORTB   EQU     $01           "  B    "
                                ORG     $0050
00000050                R       RMB     6           WORKING NUMBER
00000056                TMP1    RMB     1           POSITION OF LSB
00000057                TMP2    RMB     1           POSITION OF MSB
00000058                TMP3    RMB     1
00000059                TMP4    RMB     1
                                ORG     $1000
                        *****************************************************
                        *                                                   *
                        *       First part of the display subroutine        *
                        *       gets the segment codes corresponding to     *
                        *       the BCD data for display.                   *
                        *                                                   *
                        *****************************************************
00001000  a605          DISP    LDA     #$05
00001002  b758                  STA     TMP3
00001004  be56                  LDX     TMP1        LSB
00001006  f6            D3      LDA     0,X
00001007  bf59                  STX     TMP4
00001009  97                    TAX
0000100a  d6103c                LDA     STABL,X     FIND 7 SEGMENT CODE
0000100d  be58                  LDX     TMP3
0000100f  e750                  STA     R,X         PUT IN DISPLAY TABLE
00001011  3a58                  DEC     TMP3
00001013  be59                  LDX     TMP4
00001015  5a                    DECX
00001016  b357                  CPX     TMP2        FINISHED ?
00001018  26ec                  BNE     D3
```

```
                              ****************************************************
                              *                                                  *
                              *       The second part of the  display routine    *
                              *       sends  the  48  bits  required  by  the    *
                              *       display  driver.                           *
                              *                                                  *
                              ****************************************************

0000101a  1701                OUTT    BCLR   3,PORTB  ENABLE LOW

0000101c  ae05                        LDX    #5       SEND DISPLAY TABLE TO 144115
0000101e  e650                DISCHR  LDA    R,X
00001020  bf58                DISPLY  STX    TMP3     SAVE INDEX
00001022  1d00                        BCLR   6,PORTA  CLEAR DATA
00001024  ae08                        LDX    #8
00001026  44                  DIS1    LSRA            SET UP
00001027  2402                        BCC    DIS2     BIT OF
00001029  1c00                        BSET   6,PORTA  ACCUMULATOR
0000102b  1e00                DIS2    BSET   7,PORTA  CLOCK
0000102d  1f00                        BCLR   7,PORTA  IT
0000102f  1d00                        BCLR   6,PORTA  CLEAR DATA
00001031  5a                          DECX            COMPLETE ?
00001032  26f2                        BNE    DIS1     NO
00001034  be58                        LDX    TMP3     RESTORE INDEX
00001036  5a                          DECX
00001037  2ae5                        BPL    DISCHR

00001039  1601                        BSET   3,PORTB  ENABLE HIGH
0000103b  81                          RTS

                              ****************************************************
                              *                                                  *
                              *       LCD segment table.                         *
                              *                                                  *
                              ****************************************************

0000103c  eb                  STABL   FCB    $EB      0   SEGMENT
0000103d  60                          FCB    $60      1
0000103e  c7                          FCB    $C7      2   CODES
0000103f  e5                          FCB    $E5      3
00001040  6c                          FCB    $6C      4   FOR THE
00001041  ad                          FCB    $AD      5
00001042  af                          FCB    $AF      6   MC145000/144115
00001043  e0                          FCB    $E0      7
00001044  ef                          FCB    $EF      8   LCD DRIVER
00001045  ed                          FCB    $ED      9
```

THREE-BACKPLANE DISPLAYS

The MC68HC05L6 can drive 24 frontplanes and either 3 or 4 backplanes, the number of backplanes being selectable in software. The data to be displayed is arranged in the display RAM as shown in figure 2. Note that data sheet for the MC68HC05L6 (ADI1254) shows this relationship wrongly.

It can be seen that each frontplane occupies a nibble in the 12-byte RAM. There is thus a simple relationship between RAM location and displayed digit on a 4-backplane 7-segment display (each 2 frontplane digit corresponds to one byte). With a 3-backplane display, however, each digit corresponds to 3 nibbles (1.5 bytes) so the software required to translate the required segments into display RAM data is more complex. Listing 2 shows a suggested method of doing this.

LCD data latch 00	7	6	5	4	3	2	1	0
($00)	Bp1	Bp2	Bp3	Bp4	Bp1	Bp2	Bp3	Bp4
	Fp 01				Fp 02			

Figure 2. MC68HC05L6 back/frontplane pin to LCD data latch bit relationship

The table which translates the required character into segments contains 2 bytes per character, the middle nibble of the 3 required being repeated. This simplifies the code required to write to the display RAM by using one nibble if the character is intended for an even position in the display and the other for an odd position. Figure 3 shows the L6 – LCD segment arrangement used in this example.

When using a microprocessor without an LCD drive capability a separate display driver can be used to drive a multiplexed display. The example shown in figure 4 and listing 3 uses the ICM7231B 3-backplane driver. The ICM7231B requires each character to be addressed through pins A0, A1 and A2 and the appropriate data written to pins D0, D1, D2 and D3. This parallel control uses more I/O lines than the serial arrangement employed in MC145000/1 and MC144115 drivers.

The fact that data is accepted in HEX and encoded into segments by the driver simplifies the software but reduces the versatility of the display as only the driver's 16 characters are available. The ICM7231B driver displays 0–9,-, E, H, L, P and blank while the ICM7231A displays 0–9, A, B, C, D, E and F.

As with any multiplexed LCD drive, the contrast is dependent on the supply voltage to the driver's multiplexer circuitry. In the case of the ICM7231, contrast can be adjusted using the potentiometer on pin 2 (figure 4).

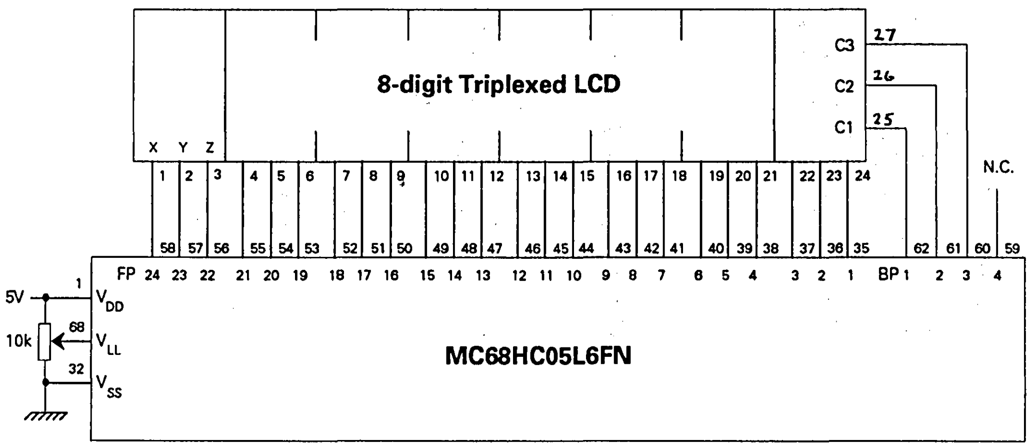

Figure 3. MC68HC05L6 with a 3-backplane LCD

LISTING 2

```
                          ******************************************************
                          *                                                    *
                          *       Example program using the MC68HC05L6         *
                          *       to directly drive a 3-backplane display.     *
                          *                                                    *
                          ******************************************************


00000009                  LADD    EQU     $0009           LCD ADDRESS REGISTER
00000008                  LDAT    EQU     $0008           LCD DATA REGISTER


                                  ORG     $0050

00000050                  Q       RMB     8          DISPLAY REGISTER
00000058                  W1      RMB     1
00000059                  W2      RMB     1


                                  ORG     $0100

                          ******************************************************
                          *                                                    *
                          *       LCD segment look-up table.                   *
                          *                                                    *
                          ******************************************************

00000100  acca            L6TAB   FCB     $AC,$CA         0
00000102  00c0                    FCB     $00,$C0         1
00000104  e48e                    FCB     $E4,$8E         2
00000106  e0ce                    FCB     $E0,$CE         3
00000108  48c4                    FCB     $48,$C4         4
0000010a  e84e                    FCB     $E8,$4E         5
0000010c  ec4e                    FCB     $EC,$4E         6
0000010e  80c8                    FCB     $80,$C8         7
00000110  ecce                    FCB     $EC,$CE         8
00000112  e8ce                    FCB     $E8,$CE         9
00000114  4004                    FCB     $40,$04         -   (A: CC CC)
00000116  ec0e                    FCB     $EC,$0E         E   (B: 6C 46)
00000118  4cc4                    FCB     $4C,$C4         H   (C: AC 0A)
0000011a  2c02                    FCB     $2C,$02         L   (D: 64 C6)
0000011c  cc8c                    FCB     $CC,$8C         P   (E: EC 0E)
0000011e  0000                    FCB     $00,$00             (F: CC 0C)
```

```
                        ********************************************************************
                        *                                                                  *
                        *       Main loop for L6 directly driven LCD.                      *
                        *                                                                  *
                        *       This subroutine assumes that Q contains                    *
                        *       HEX data for display. As each character                    *
                        *       requires 1½ bytes (9 bits contained in                     *
                        *       3 nibbles with 1 bit (backplane) in                        *
                        *       each nibble not used) each execution                       *
                        *       of the loop handles 2 characters.                          *
                        *                                                                  *
                        ********************************************************************

00000120  3f59          START   CLR     W2          Initialise digit pointer.
00000122  a680                  LDA     #$80        First write to $09: Bus/LCD ratio - 256,
00000124  b709                  STA     LADD        4-backplane, fast charge enabled.
00000126  be59          L6OP    LDX     W2
00000128  e650                  LDA     Q,X         Get HEX data.
0000012a  a40f                  AND     #$0F        Only lower nibble is relevant.
0000012c  48                    LSLA                x 2 (two bytes per digit in table).
0000012d  97                    TAX
0000012e  d60100                LDA     L6TAB,X     Get first byte from segment table.
00000131  b708                  STA     LDAT        Send it to LCD data latch.
00000133  3c09                  INC     LADD        Keep LCD on, move to next latch.
00000135  d60101                LDA     L6TAB+1,X   Get second byte of segment data.
00000138  44                    LSRA                From this byte only the
00000139  44                    LSRA                upper nibble is relevant, lower
0000013a  44                    LSRA                nibble is lost as upper nibble
0000013b  44                    LSRA                is shifted down.
0000013c  b758                  STA     W1          Save nibble, to be combined with first
0000013e  3c59                  INC     W2          nibble of next digit.
00000140  be59                  LDX     W2          Address of next digit in Q.
00000142  e650                  LDA     Q,X         Get HEX data.
00000144  a40f                  AND     #$0F        only lower nibble is relevant.
00000146  48                    LSLA                x 2 (two bytes per digit in table).
00000147  97                    TAX
00000148  d60100                LDA     L6TAB,X     Get first byte from segment table.
0000014b  48                    LSLA                From this byte only the
0000014c  48                    LSLA                lower nibble is relevant, upper
0000014d  48                    LSLA                nibble is lost as lower nibble
0000014e  48                    LSLA                is shifted up.
0000014f  bb58                  ADD     W1          Combine nibble with last nibble
00000151  b708                  STA     LDAT        of previous digit and send byte to LCD.
00000153  3c09                  INC     LADD        Next LCD data latch.
00000155  d60101                LDA     L6TAB+1,X   Get second byte from segment table.
00000158  b708                  STA     LDAT        and send it to LCD.
0000015a  3c09                  INC     LADD        Next latch (three per loop).
0000015c  3c59                  INC     W2          Next digit (two per loop).
0000015e  b609                  LDA     LADD
00000160  a10c                  CMP     #12         Finished ?
00000162  26c2                  BNE     L6OP        If not, do next two digits.
00000164  81                    RTS
```

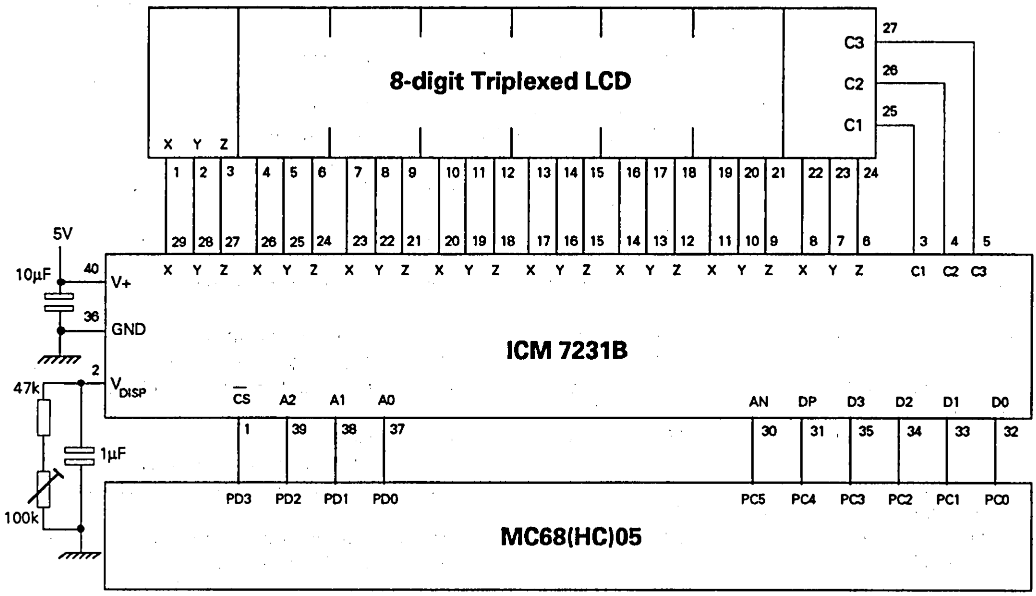

Figure 4. 3-backplane LCD driven by an ICM7321

LISTING 3

```
                          *****************************************************
                          *                                                   *
                          *        Example program using the ICM7231          *
                          *        driver and a 3-backplane display.          *
                          *                                                   *
                          *****************************************************

00000001                  PORTD   EQU     $0001       PORT B DATA
00000002                  PORTC   EQU     $0002       PORT C DATA


                                  ORG     $0050

00000050                  Q       RMB     8           DISPLAY REGISTER


                                  ORG     $0100

                          *****************************************************
                          *                                                   *
                          *        Display contents of Q.                     *
                          *                                                   *
                          *****************************************************

00000100  b601            DISP    LDA     PORTD        CLEAR
00000102  a4f0                    AND     #$F0        LS NIBBLE OF PORTD
00000104  b701                    STA     PORTD       IE DIGIT ADDRESS = 0

00000106  ae08                    LDX     #8

00000108  e64f            AGAIN   LDA     Q-1,X
0000010a  b702                    STA     PORTC
0000010c  1701                    BCLR    3,PORTD     LATCH
0000010e  1601                    BSET    3,PORTD     DIGIT
00000110  5a                      DECX
00000111  2704                    BEQ     OUT         DONE ?
00000113  3c01                    INC     PORTD       NO, GOTO NEXT DIGIT
00000115  20f1                    BRA     AGAIN

00000117  3f02            OUT     CLR     PORTC
00000119  81                      RTS
```

FOUR-BACKPLANE DISPLAYS

As mentioned above, the MC68HC05L6 can drive a 4-backplane display with up to 24 frontplanes directly. The resultant 96 pixels could be used to drive 2 digits of an 5x8 dot matrix display, but with this number of segments most applications will use 7-segment or customised displays. A 7-segment display of up to 12 digits can be used. The software required is similar to, and simpler than, that shown for the L6 with a 3-backplane display. When it is required to drive a 4-backplane display using a microprocessor without an LCD drive capability, the MC145000 offers a versatile solution. Up to 6 digits (12 frontplanes) can be driven directly and more can be driven by the addition of one or more of the 18-pin MC145001 expanders, each adding 11 frontplanes. The example shown in figure 5 and listing 4 drives 6 digits, the software being very similar to that shown for the MC144115 single-backplane driver. This is the result of both chips having the same shift-register/latch architecture despite the actual output signals being quite different. The listing also shows a routine using an SCI rather than port lines.

A difference between the MC145000 and the MC144115 is that the MC145000 has no chip-enable input. It can share its data line with other peripherals but must have a dedicated clock so that the controller can supply data independently of other chips.

For applications requiring more than the 12 frontplanes made available by the MC145000, the MC145003/4 may be appropriate. They provide 32 frontplanes for use with a 4-backplane display, allowing up to 128 segments. The MC145003 and MC145004 are identical except for their serial protocol. The MC145004 has an IIC bus interface incorporating the usual acknowledge procedure associated with the IIC standard. The MC145003 is the same, except that there is no acknowledge and hence no associated clock cycle. The incoming data is automatically latched after 128 bits have been received. If, however, it is required that the data be latched at other times, an enable pin is available.

For applications where Vdd and Vlcd are connected together, the LCD contrast is adjusted by adjusting Vdd. If the data is coming from a chip with a higher supply voltage, the input pins may go higher than the supply voltage of the MC145003/4. This is allowed for the clock and data pins, but not recommended for the enable pin as its input protection circuitry may clamp the input voltage. It is therefore not advisable to use the enable pin if the MC145003/4 has a different Vdd from the chip supplying it with data. In applications not using this pin it can be left floating or tied high.

The example shown in figure 6 does not use the enable pin; the example software sends all 128 bits every time it is executed. The latching is thus performed automatically. The circuit shows 2 6-digit displays, each with 12 frontplanes. Any display or combination of displays with up to 32 frontplanes can be used with the software shown in listing 6, as all 128 bits are always sent. The 6 lines of code (45–50) are commented out for use with the MC145003; they are required for the MC145004.

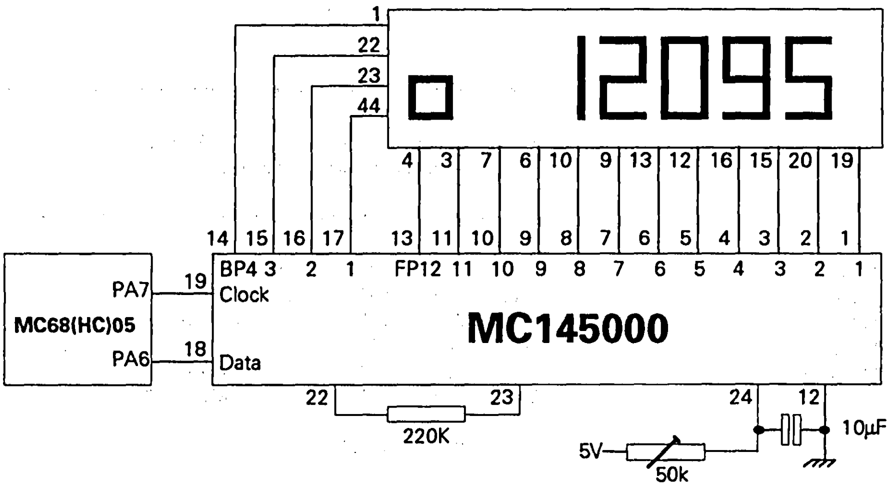

Figure 5. MC145000 driving a 4-backplane LCD

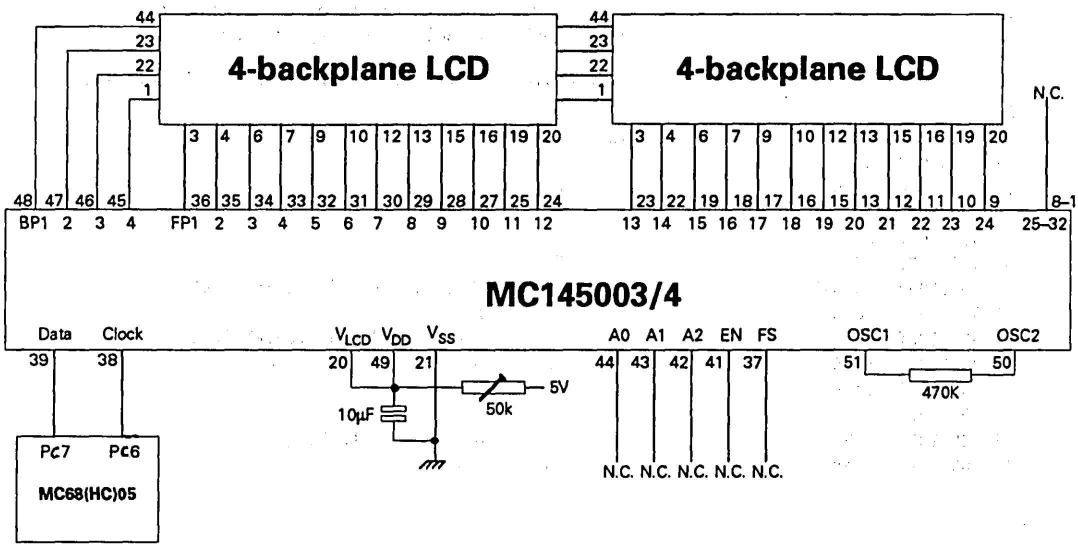

Figure 6. MC145003/4 driving 4-backplane LCDs

LISTING 4

```
                        ****************************************************
                        *                                                  *
                        *     Example program for MC145000 driven          *
                        *     four-backplane display.                      *
                        *                                                  *
                        ****************************************************

00000000                PORTA  EQU    $00      PORT A DATA
0000000d                BAUD   EQU    $0D      SCI BAUD RATE REGISTER
0000000e                SCR1   EQU    $0E       "  CONTROL REG. No. 1
0000000f                SCR2   EQU    $0F       "     "      "   "  2
00000010                SCSR   EQU    $10       "   STATUS  "
00000011                SDAT   EQU    $11       "   DATA    "

                               ORG    $0050

00000050                R      RMB    6        WORKING NUMBER

00000056                W2     RMB    1        POSITION OF LSB
00000057                W3     RMB    1
00000058                W4     RMB    1
00000059                W5     RMB    1
0000005a                W6     RMB    1        POSITION OF MSB


                               ORG    $1000

                        ****************************************************
                        *                                                  *
                        *     First part of  the display  subroutine       *
                        *     replaces  BCD  with  segment codes.          *
                        *                                                  *
                        ****************************************************

00001000  a605          DISP   LDA    #$05
00001002  b758                 STA    W4
00001004  be56                 LDX    W2       LSB
00001006  f6            D3     LDA    0,X
00001007  bf59                 STX    W5
00001009  97                   TAX
0000100a  d61047               LDA    STABL,X  FIND 7 SEGMENT CODE
0000100d  be58                 LDX    W4
0000100f  e750                 STA    R,X      PUT IN DISPLAY TABLE
00001011  3a58                 DEC    W4
00001013  be59                 LDX    W5
00001015  5a                   DECX
00001016  b35a                 CPX    W6       FINISHED ?
00001018  26ec                 BNE    D3
```

```
                       ****************************************************
                       *                                                  *
                       *     The second part of the  display routine      *
                       *     sends  the  48  bits  required  by  the      *
                       *     display  driver.   For  comparison  two      *
                       *     routines are included, one using port A      *
                       *     lines and a second using the SCI.            *
                       *                                                  *
                       ****************************************************

0000101a  ae05         OUTT   LDX    #5       SEND DISPLAY TABLE TO 144115/145000
0000101c  e650         DISCHR LDA    R,X
0000101e  bf57         DISPLY STX    W3       SAVE INDEX
00001020  1d00                BCLR   6,PORTA  CLEAR DATA
00001022  ae08                LDX    #8
00001024  44           DIS1   LSRA            SET UP
00001025  2402                BCC    DIS2     BIT OF
00001027  1c00                BSET   6,PORTA  ACCUMULATOR
00001029  1e00         DIS2   BSET   7,PORTA  CLOCK
0000102b  1f00                BCLR   7,PORTA  IT
0000102d  1d00                BCLR   6,PORTA  CLEAR DATA
0000102f  5a                  DECX            COMPLETE ?
00001030  26f2                BNE    DIS1     NO
00001032  be57                LDX    W3       RESTORE INDEX
00001034  5a                  DECX
00001035  2ae5                BPL    DISCHR

                       ****************************************************
                       *                                                  *
                       *     SCI LCD driver interface.                    *
                       *                                                  *
                       ****************************************************

00001037  ae05                LDX    #5       INITIALISE X
00001039  e650         MORE   LDA    R,X      FETCH DIGIT
0000103b  0f10fd              BRCLR  7,SCSR,* WAIT UNTIL TDRE = 1
0000103e  b711                STA    SDAT     WRITE IT TO SCI TX REG.
00001040  5a                  DECX            NEXT DIGIT
00001041  2af6                BPL    MORE     DONE ?
00001043  0d10fd              BRCLR  6,SCSR,* WAIT UNTIL TC=1
00001046  81                  RTS

00001047  eb           STABL  FCB    $EB      0   SEGMENT
00001048  60                  FCB    $60      1
00001049  c7                  FCB    $C7      2   CODES
0000104a  e5                  FCB    $E5      3
0000104b  6c                  FCB    $6C      4   FOR THE
0000104c  ad                  FCB    $AD      5
0000104d  af                  FCB    $AF      6   MC145000/MC144115
0000104e  e0                  FCB    $E0      7
0000104f  ef                  FCB    $EF      8   LCD DRIVER
00001050  ed                  FCB    $ED      9
```

LISTING 5

```
                          *************************************************************
                          *                                                           *
                          *      Example program using MC145003/4 LCD Drivers.        *
                          *                                                           *
                          *************************************************************

00000002                  IICP     EQU    $02                PORTC
00000006                  IICDD    EQU    $06                PORTCD
00000006                  SCL      EQU    $06                IIC - clock line
00000007                  SDA      EQU    $07                IIC - data line
00000040                  DIN      EQU    $40                INPUT DATA
000000c0                  DOUT     EQU    $C0                OUTPUT DATA

                                   ORG    $0050

00000050                  W1       RMB    1
00000051                  DPNT     RMB    1          IIC WRITE POINTER
00000052                  ADDR     RMB    1          IIC ADDRESS
00000053                  IIC      RMB    16         IIC BUFFER (128 BITS)

                                   ORG    $0B00

00000b00  a67e            START    LDA    #$7E
00000b02  b752                     STA    ADDR
00000b04  a611                     LDA    #17
00000b06  b750                     STA    W1
00000b08  ae52                     LDX    #ADDR
00000b0a  bf51                     STX    DPNT
00000b0c  1f02            SEND2    BCLR   SDA,IICP           START CONDITION
00000b0e  1d02                     BCLR   SCL,IICP           DATA GOES LOW WHILE CLOCK HIGH

00000b10  be51            SLOOP    LDX    DPNT               DATA BUFFER POINTER
00000b12  f6                       LDA    0,X                GET A BYTE
00000b13  ae08                     LDX    #8                 8 BITS TO SHIFT
00000b15  49              SLOP     ROLA
00000b16  2402                     BCC    DZERO              BIT = 0 ?
00000b18  1e02                     BSET   SDA,IICP           NO, BIT = 1
00000b1a  1c02            DZERO    BSET   SCL,IICP           CLOCK HIGH
00000b1c  1d02                     BCLR   SCL,IICP           CLOCK LOW
00000b1e  1f02                     BCLR   SDA,IICP           DATA LOW
00000b20  5a                       DECX
00000b21  26f2                     BNE    SLOP

                          *        LDA    #DIN               DATA LINE AN INPUT
                          *        STA    IICDD
                          *        BSET   SCL,IICP           CLOCK
                          *        BCLR   SCL,IICP           ACKNOWLEDGE BIT
                          *        LDA    #DOUT
                          *        STA    IICDD              BACK TO AN OUTPUT
00000b23  3c51                     INC    DPNT               NEXT BYTE
00000b25  3a50                     DEC    W1
00000b27  26e7                     BNE    SLOOP              LAST BYTE ?

00000b29  1c02            I2CEND   BSET   SCL,IICP           STOP CONDITION
00000b2b  1e02                     BSET   SDA,IICP           DATA GOES HIGH WHILE CLOCK HIGH
00000b2d  81                       RTS
```

8/16-BACKPLANE DISPLAYS

For dot-matrix displays, 8 or 16 backplanes are common. This is the result of the large number of pixels required. A compromise between pin-count and contrast is made to decide the number of backplanes. The minimum pin requirement for a display with N segments would require the number of backplanes to be the square root of N, but with typical requirements of many hundred or thousands of pixels this is not practical as the resultant contrast would not be acceptable. Typical compromises are 8 or 16 backplanes, as this gives acceptable contrast and fits in conveniently with the 8x5 dot-matrix format commonly used for this type of display.

The MC68HC05L7 and L9 are designed to directly drive this type of display. The L7 has 16 backplanes and 60 frontplanes allowing it to drive up to 960 pixels or 24 8x5 dot matrix digits (12 with x 8 multiplexing). The L9 has only 40 frontplanes (16 8x5 digits) but is capable of being used with MC68HC68L9 LCD drive expanders. Each MC68HC68L9, up to 3 of which may be added, contributes 55 frontplanes. An L9 and 3 expanders has thus 205 frontplanes allowing then to drive up to 3280 pixels or 82 8x5 dot matrix digits.

The display RAM contains a 5-bit word for each row of dots in the 8x5 format; thus, 8 locations are used for each digit, allowing easy addressing. The RAM corresponding to the digits driven by expanders is contained in the expanders, but appears in the L9's memory map as the data and address buses from the L9 to external memory are also used by the MC68HC68L9s.

Application note ANHK10/D shows an application using the L9 and also describes a method of extending the display size beyond that normally available using this device.

APPLICATION NOTES

The following application notes give complete applications using the type(s) of display indicated.

ANE404 An extended MC146805E2 CBUG05 system using the MC68HC25.
MC145000-driven 4-backplane, 6-digit and ICM7231B-driven 3-backplane, 8-digit display.

ANE416 MC68HC05B4 Radio Synthesizer.
MC145000-driven 4-backplane, 6-digit and MC144115-driven 1-backplane, 6-digit display.

ANE425 Use of the MC68HC68T1 RTC with M6805 Microprocessors.
ICM7231B-driven 3-backplane, 8-digit display.

ANHK10 The summary of the MC68HC05L9 Micro. App. Demo. Board.
MC68HC05L9/MC68HC68L9-driven dot matrix display.

DRIVER CHIPS

The following list shows some LCD driver devices. They are most suitable for 7-segment, 16-segment and custom displays. The 7SD column shows how many 7-segment digits each device can drive. With the possible exceptions of the MC145000/1 and the MC145003/4, they are not generally suitable for dot-matrix displays which have 35-40 segments per digit.

Device	Back	Front	7SD	Drive	Expan.	Pins	
MC14543	1	7	1	parallel	parallel	16	BCD
MC14544	1	7	1	parallel	parallel	18	ripple blank
MC144115	1	16	2	3-line	yes	24	
MC144117	2	16	4	3-line	no	24	
MC145000	4	12	6	2-line	MC145001	24	
MC145001	(4)	11	5.5	2-line	n/a	18	expander
MC145003	4	32	16	2- or 3-line	parallel	52	2- or 3-line
MC145004	4	32	16	2-line	parallel	52	IIC
MC145453	1	33	4	2-line	parallel	40	also 44-pin
ICM7231	3	24	8	parallel	no	40	BCD

MC68HC05L10 AN ENHANCED VERSION OF L9 FOR HANDHELD EQUIPMENT APPLICATIONS

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INTRODUCTION

The MC68HC05L10 (L10), new member of the DRAGONKAT™ family of Micro-Controllers Unit (MCU), is particularly tailored for application in hand-held equipments, such as organizers, meter readers, inventory checkers, hand-held diagnostic terminals, or personal communication products etc., where low power consumption and system optimization are the main concerns to the product designer. This enhanced version of MC68HC05L9 (L9) has upgraded features to meet the requirements in advanced applications. The similarities and differences between these two MCUs are being highlighted in this application note. In addition, software routines on some new features such as keyscan, LCD (Liquid Crystal Display) and Memory Management Unit (MMU) are also described in detail to guild users in their program development for a specific application.

FEATURE COMPARISON BETWEEN MC68HC05L9 AND MC68HC05L10

Both L10 and L9 belong to the 68HC05 microprocessor family so that they share the same instruction set. Since both of them serve for the same intended application, most of the circuit blocks are the same for ease of use. However, certain features have been added or enhanced in L10 to expand its capability. Their similarities and differences are highlighted in below.

The following on-chip circuits remain unchanged:
* Real time clock and its alarm function
* 16 bit programmable free run timer
* Serial communication interface (SCI)
* Tone generator
* LCD auto-display off
* Keyboard wake-up interrupt
* Separate external data and address bus
* High frequency voltage controlled oscillator with PLL (Phase Lock Loop) locking into reference frequency from 32.768 KHz crystal oscillator.

New Features Added or Features Enhanced to the MC68HC05L10:

* Serial peripheral interface (SPI). It provides a means to interface with other peripherals or MCU in a sophisticated system.

* Memory management unit (MMU). A hardware implementation to extend the memory addressing space from 64KB to 1MB for data storage. The number of address lines is therefore increased to 20.

* External ROM. Internal ROM disabled by hardware pin RDIS which gives the user a choice of using internal or external ROM.

* An additional external interrupt input.

* Two external pins only on PLL. RF pin in L9 PLL system is eliminated by RF resistor on-chip. No VCO (Voltage Controlled Oscillator) center frequency adjustment is required.

* Low voltage inhibit feature deleted. Due to the limitation of achieving high accuracy on internal reference voltage, it is recommended to use external low voltage detection circuit.

* Enhanced LCD driving capability. A programmable 32- or 41-multiplex backplane (or common) drive is built-in to expand the multiplex ratios while minimizing system chip count by fully utilizing the process ability of sustaining voltage. The segments are driven by a separate device (MC141511) which handles up to 128 segments each. The maximum segment driving capability is limited by the display RAM spaced located at $1C0 to $BFF in L10. Up to four MC141511 segment drivers of 41X128X4=20,992 pixels in total on a single LCD display panel or up to two MC141511 segment drivers in a split panel with the same display pixels may be cascaded. The built-in display RAM in MC141511 is organized in 8 bit vertical format. However, the 16 bytes of display RAM for the annunciator in the backplane 40th is arranged horizontally as shown in Figure 3. This configuration of the display RAM significantly eases programming for display of Chinese character in terms of changing the character pitch or performing horizontal scrolling.

* Less interference from bus. During internal memory access, the data bus is at high impedence, address bus at low state, R/W line at high state and P02 switched off. It STOP or WAIT instruction is executed during CPU accessing external memory. the address bus will hold at the location of the instruction following the STOP or WAIT until an interrupt or reset occurs. The interference induced by digital pulses from external bus lines or P02 is, therefore, eliminated during those operations. Furthermore, it also prevents the excess current contributed by the floating data lines and external memory devices during STOP or WAIT mode operation regardless or RIDS pin status.

PROGRAMMING PLL FOR BUS SPEEDS

The PLL system is shown in Figure 1. Upon power on or external reset, the CLKS bit in $1C register is cleared which set the CPU bus directly sourced from 32.768KHz crystal. To change the CPU bus speed from 32.768KHz, follow the sequence shown in flow chart Figure 2. The sampling rate of the PLL is 8KHz or sampling at every 125µs interval. If there is no error occurred at phase detector output after 32 consecutive samplings which equals to 4ms, a PLLI bit in $26 register will be set. It indicates that the PLL stablized at new bus frequency. For operations on those require accurate clock frequency and duty cycle, such as SCI or counter etc., should make sure that the PLLI is set before start execution of the program. The software routine below gives an example:

```
        BCLR    6,$1C            Select 16.384 KHz as internal bus frequency
        BSET    5,$27            Select 1.2288 MHz for PLL
DELAY   LDA     #$9              4.0 msec delay loop for min PLLI settle time
        DECA
        BNE     DELAY
STABLE  BRCLR   6,$26,STABLE     Wait until PLL is stable
        BSET    6,$1C            Select PLL as the internal bus frequency
        JMP     SERVE            Go to service routine
```

INTERFACE BETWEEN MASTER L10 AND SLAVE MC141511 SEGMENT DRIVER

The connection between the L10 and the segment drivers in a single display panel is shown in Figure 4, and the simplified schematic for a split panel in Figure 5. The display RAM in the segment driver is configured in a "WHAT YOU STORE IS WHAT YOU SEE" (WYSIWYS) scheme which is the same as in L9. But the display RAM is to be accessed by the master L10 in 8-bit bytes oriented vertically instead of 5 bit arranged horizontally as in L9. The four segment drivers corresponding to the 2624 bytes (4X41X128) of display RAM located in L10 memory space $1C0 to $BFF are to be selected by four individual chip select pins CS1-CS4. Care should be taken on the system memory address decoding circuit. For details of the address correlation please refer to TABLE 6 "MCU Display Logical & Physical Address Translation", MC68HC05L10 Technical Data and Figure 7 "Display RAM Configuration at 1:32 and 1:41 Multiplex Ratios", of the MC141511Technical Data. For better understanding the relationship an illustration is shown in Figure 6. Notice that the segment driver's data clock rate is 4.096KHz/2 so that there is a time lag of up to 500 usec after DON bit (bit 3 of $26 register) is set before the display data becomes valid.

PROGRAMMING FOR LCD DRIVE AND MMU

The program routine described here demonstrates an LCD driver that has large amount of symbols and font patterns stored in the external memory access via the MMU facility. Users have the flexibility of selecting various display symbols and font patterns or sizes. In this program, a characters in 16X16 pixels, and one row of 21 alphanumerics in 8X6 pixels, the third row of characters is being scrolled softly from right to left. The flow chart of this program is shown in Figure 8a to 8c. It can be divided into three portions: The first portion is to search for the user's required symbol code and its font pattern; the second portion is to locate the display RAM address in L10 to its corresponding display pixel position on LCD; the last portion is to scroll the third character row located at 32nd to 39th backplane in 41 multiplex mode.

The font pattern is organized in a tabular structure so that the user can easily modify the symbols and font patterns to fit their requirements. The number of symbols and font patterns can be extended beyond 64 KB with the on-ship MMU. User can clearly notice from this program how easy it is to access the memory space beyond 64 KB.

PROGRAMMING FOR KEYPAD SCANNING

This KEYSCAN program routine demonstrates a 6X4 matrix in a MXN keypad (M in port A AND N in port B). In order to be versatile the number of keys and the definition of each individual key can be user specified. The flow chart of this program and the associated schematic are shown in Figure 9 and 10 respectively.

To adapt this program to a user specified keypad, user only needs to follow a simple procedure: Firstly. to assign the number of key M in port A and N in port B; secondly, to modify the keypad definition routine as required by the particular application; lastly, to enter the routine entry address into the KEYDEF table. The number of M and N is specified in the section of the program called NUMKEYA and MUNBERB respectively.

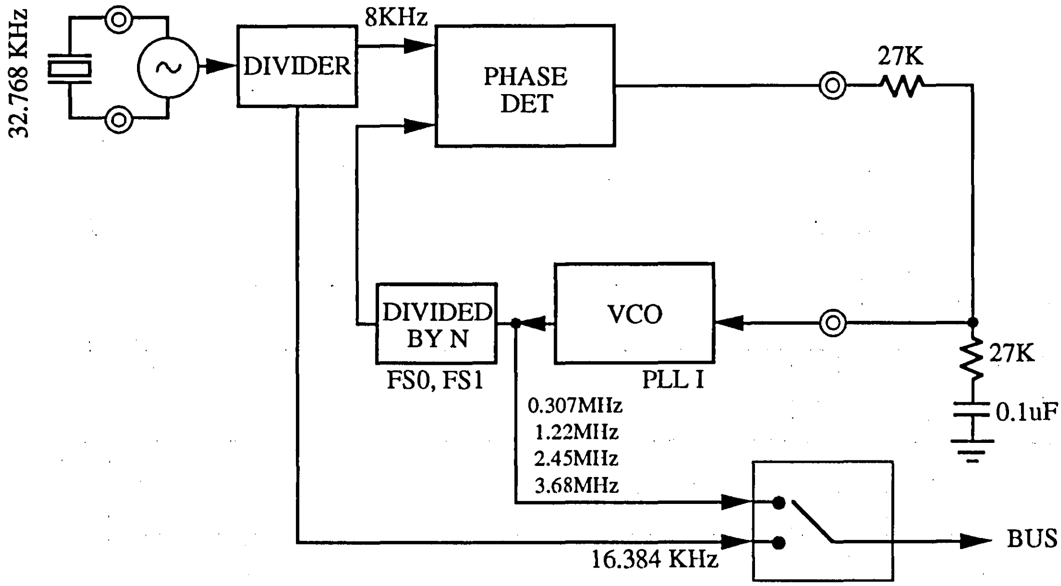
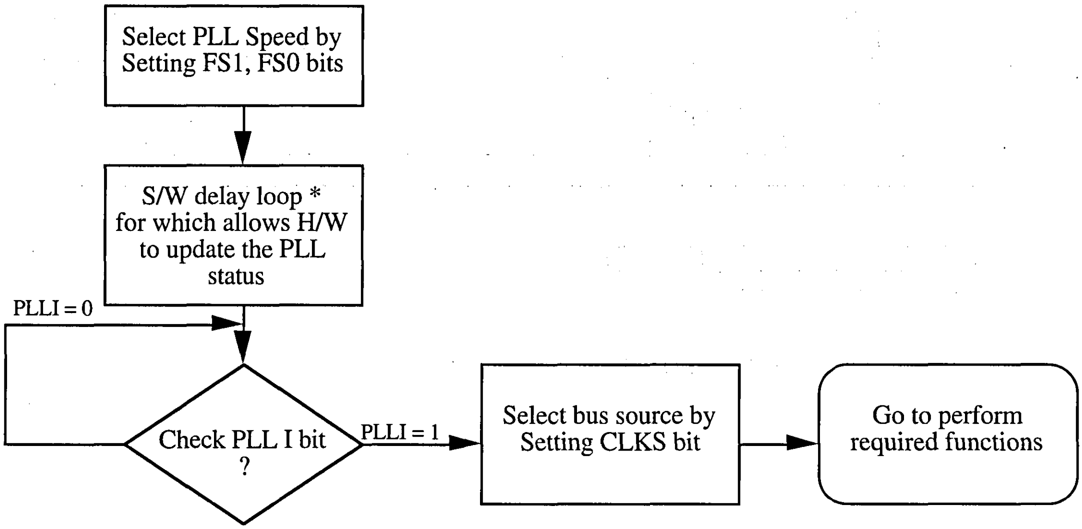


Fig 1 Phase Lock Loop



* L7, L9 need at least 1 msec delay for PLLI to change from 1 to 0 and 16ms from 0 to 1.
L10 needs at least 125 µsec delay for PLLI to change from 1 to 0 and 4ms from 0 to 1.

Fig 2 Flow Chart of Programming PLL for Bus Speed

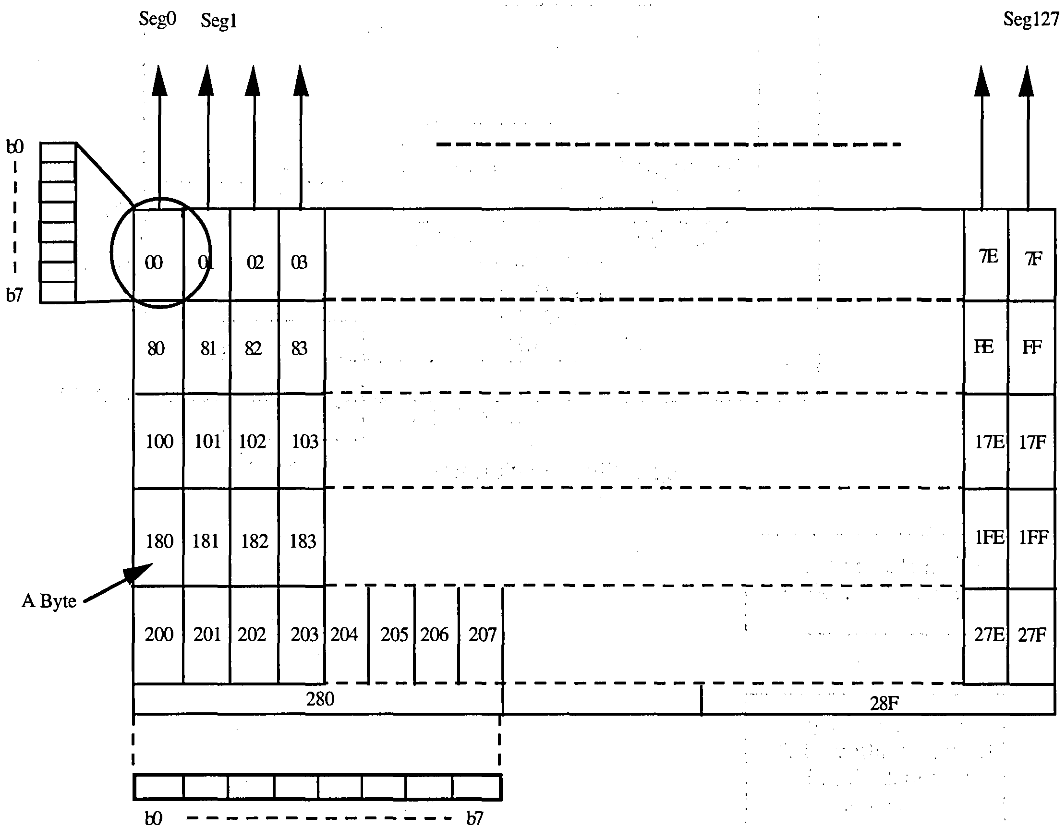


Fig 3 MC141511 Display RAM Configuration

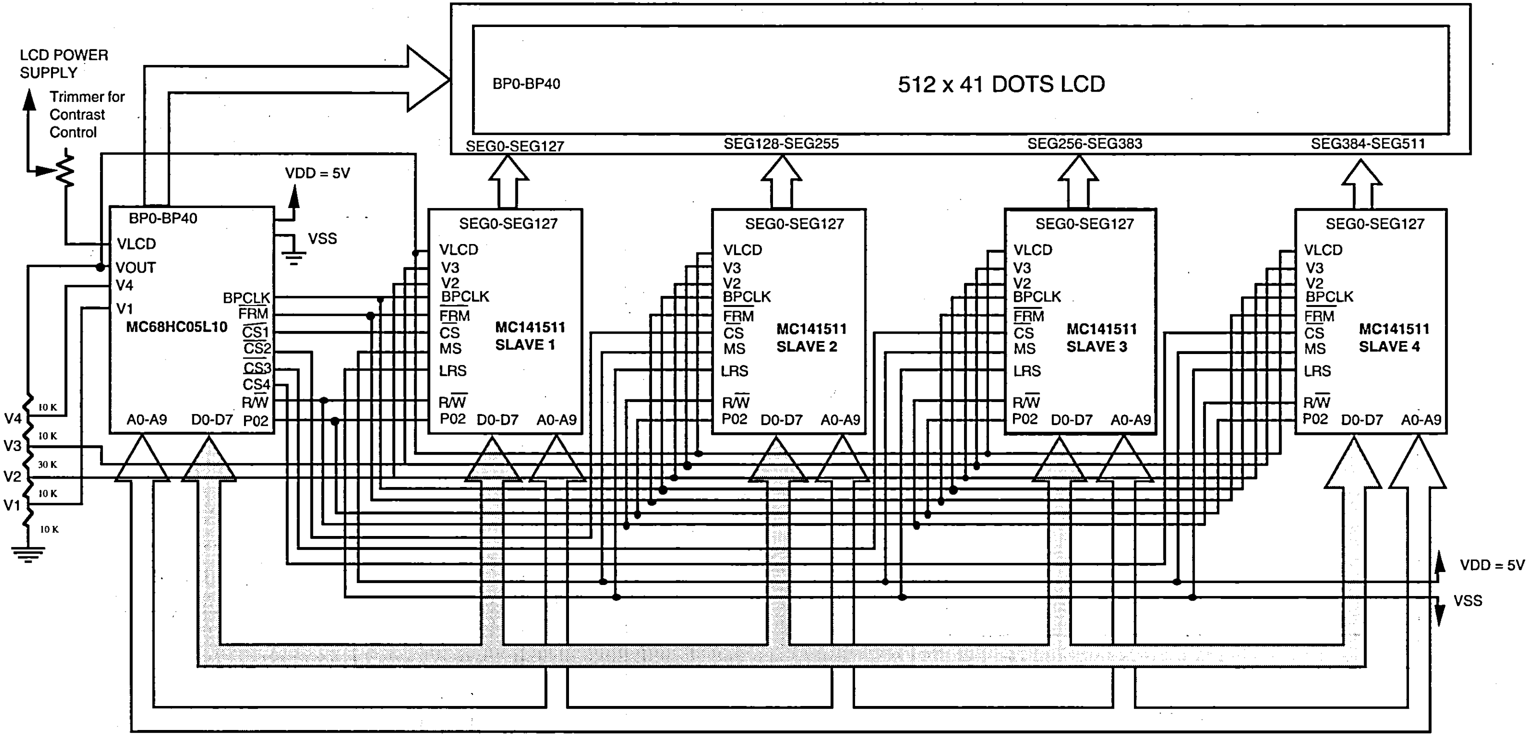


Fig 4 Full Capability of Master MCU and Slave LCD Drivers Pins Connection for 1:41 Mux and Left to Right Display Select

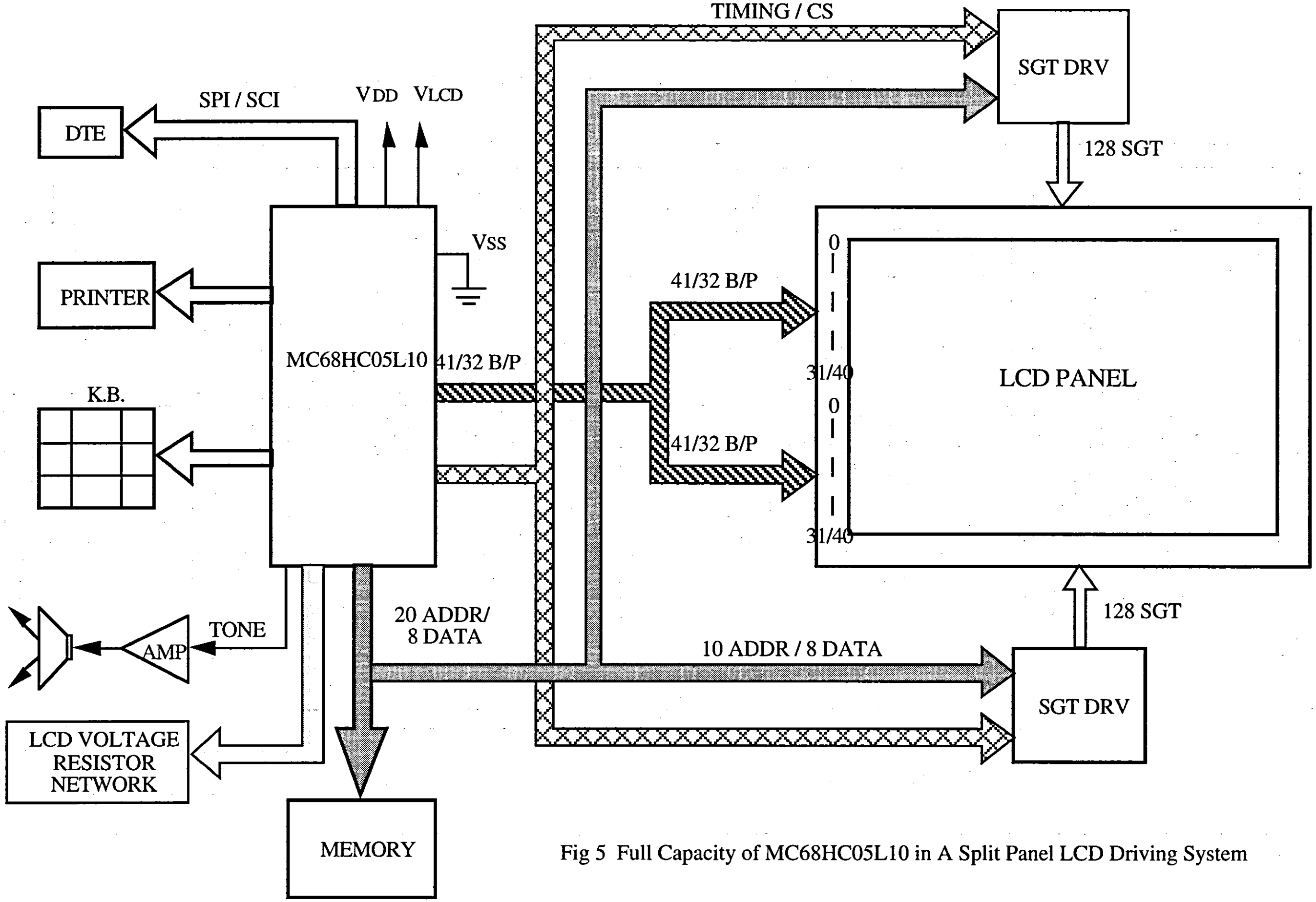
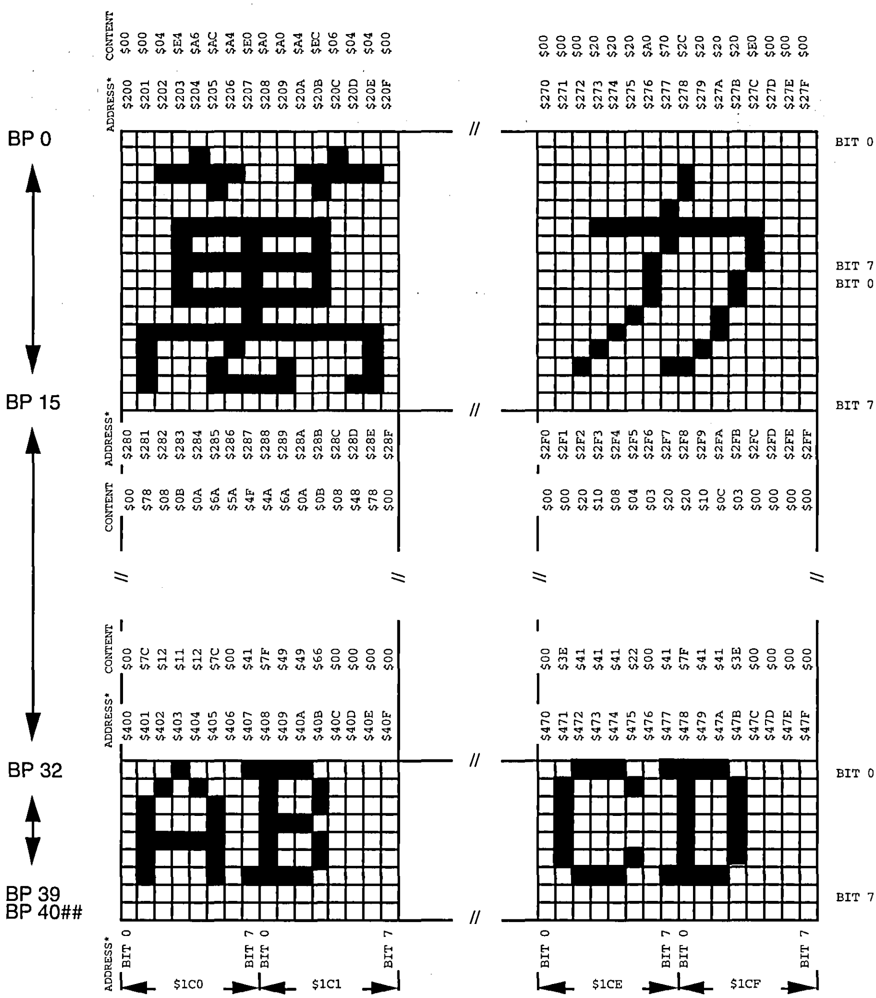


Fig 5 Full Capacity of MC68HC05L10 in A Split Panel LCD Driving System



Note: - * The display RAM address located in L10 for segment selected by $\overline{CS1}$.
- ## For annunciator feature.

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Fig 7 Display Pattern

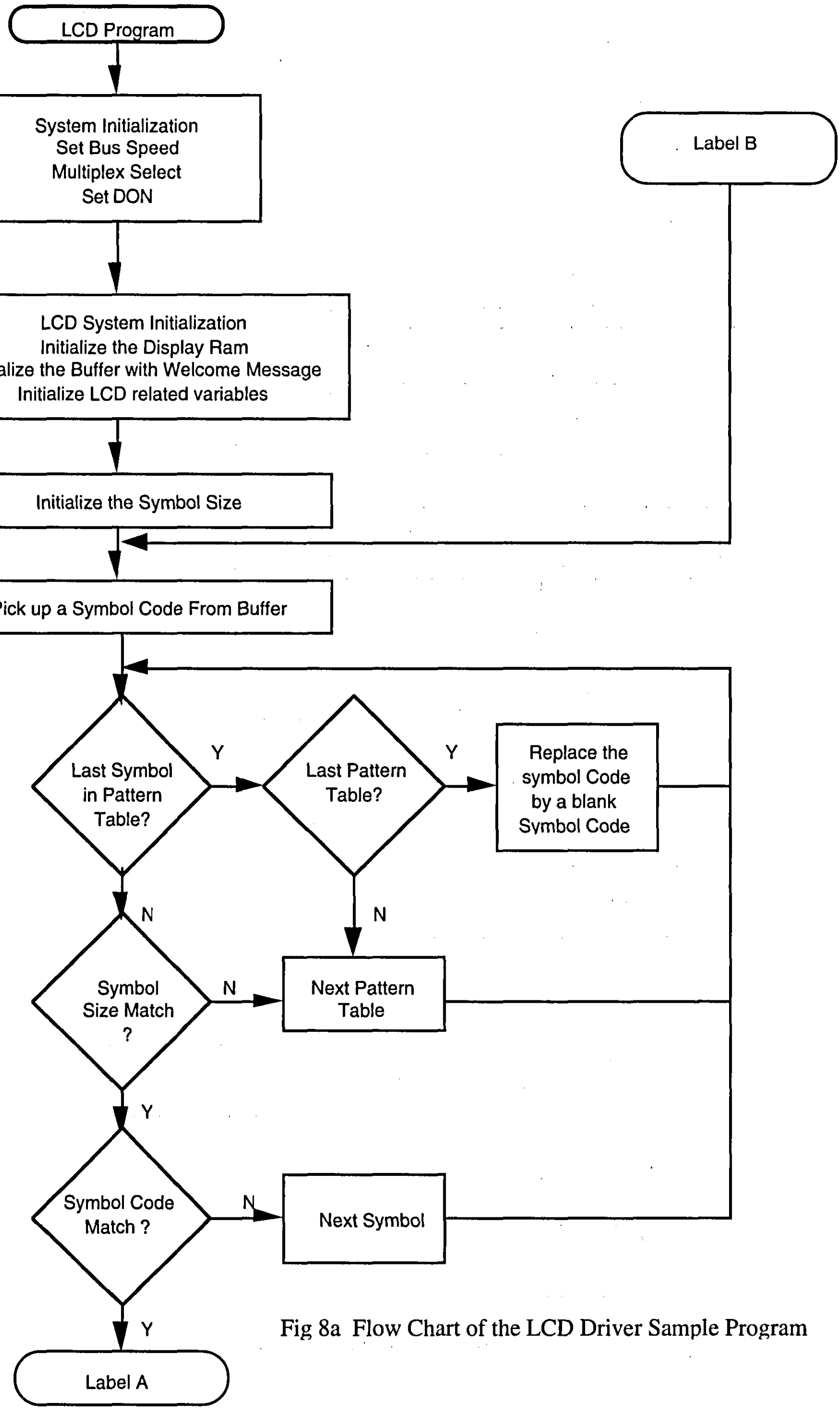

Fig 8a Flow Chart of the LCD Driver Sample Program

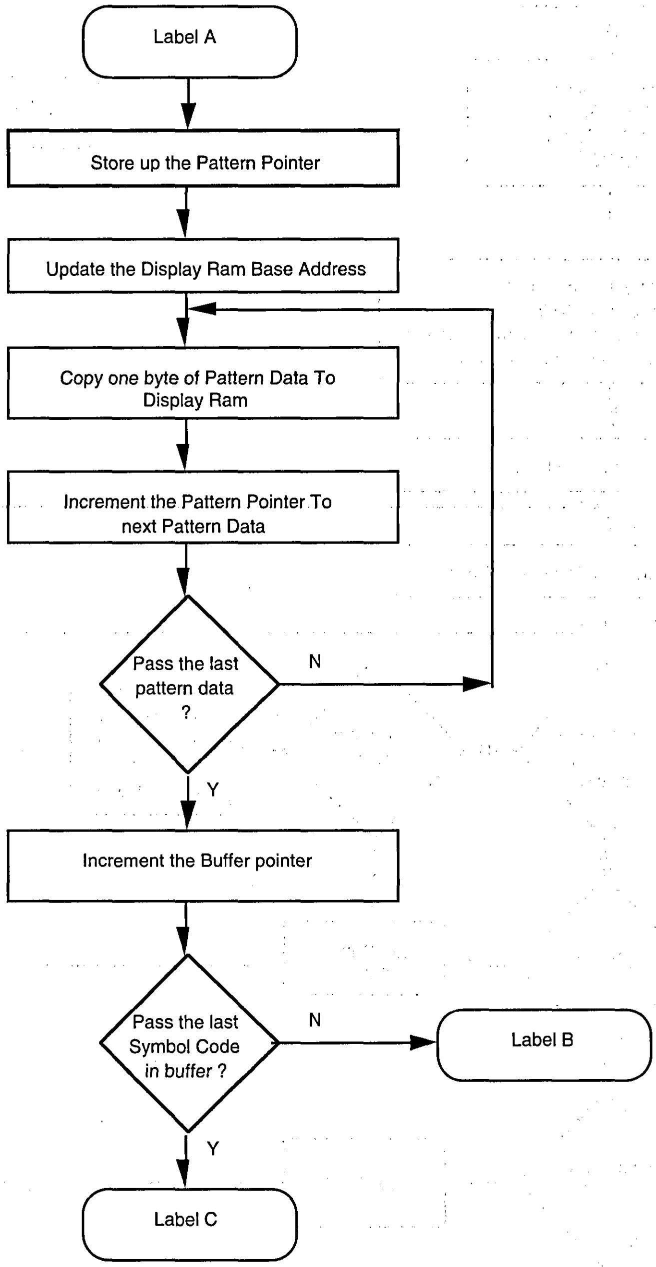

Fig 8b Flow Chart of the LCD Driver Sample Program

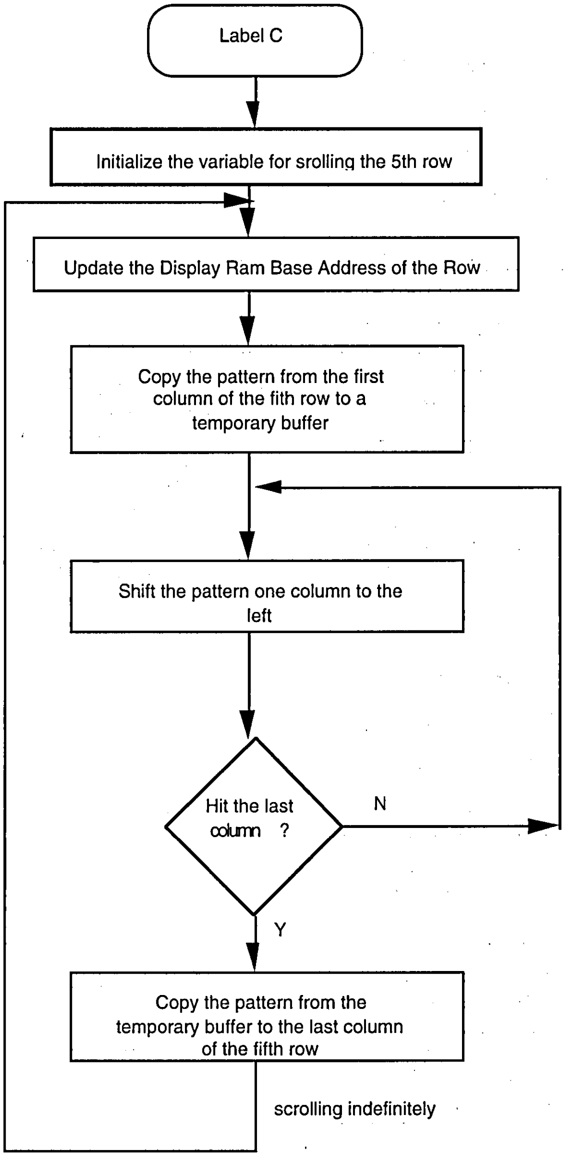

Fig 8c Flow Chart of the LCD Driver Sample Program

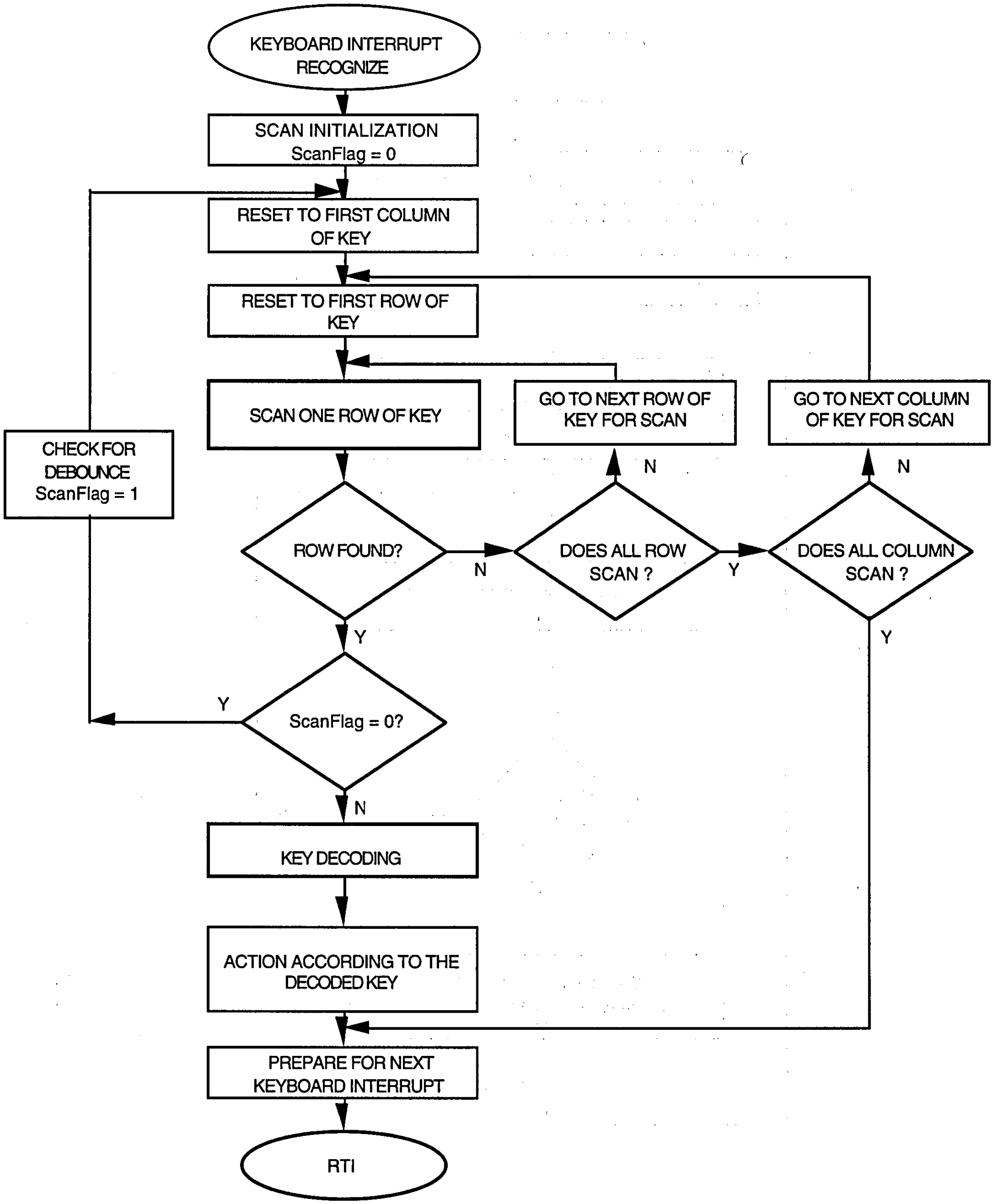

Fig 9 Flow Chart of the Keyscan Sample Progra

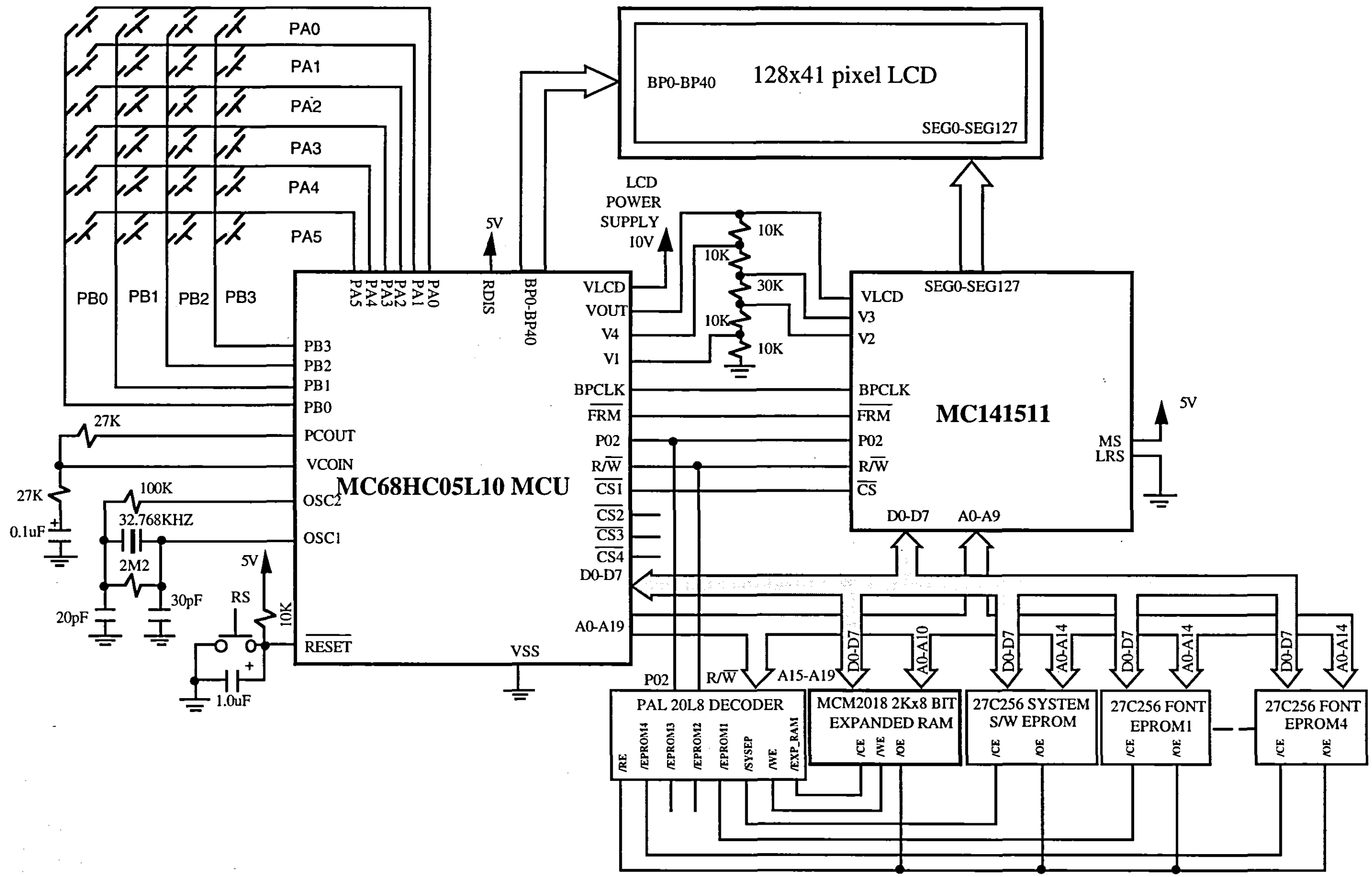

Fig 10 Application Circuitry for Keyscan Program, LCD Driver & Memory Management Unit Program

```
module L10APPLICATION;

title
'PAL20L8
R1.0/MAR26/91
THE ADDRESS DECODER FOR
THE L10 APPLICATION CIRCUITRY.';

L10APP device 'P20L8';


"declarations

    TRUE,FALSE = 1,0;
    H,L = 1,0;
    X,Z,C = .X.,.Z.,.C.;

    GND,VCC
        pin 12,24;

    "Input Port
    A8,A9,A10,A11,A12,A13,A14,A15,A16,A17,A18,A19
        pin 1,2,3,4,5,6,7,8,9,10,11,13;             "Address bus

    P02   pin 14;                                   "System clock

    RW    pin 23; "Read/Write signal


    "Output Port
    _RE   pin 15;                                   "Read Enable

    _WE   pin 16;                                   "Write Enable

    _RAM  pin 17;                                   "Expanded RAM Chip Enable
                                                    "$06000-$067FF

    _SYSEP pin 18;                                  "System S/W Eprom
                                                    "$00C00-$05FFF

    _EPROM1 pin 19;                                 "Eprom 1 $08000-$0FFFF

    _EPROM2 pin 20;                                 "Eprom 2 $10000-$17FFF

    _EPROM3 pin 21;                                 "Eprom 3 $18000-$1FFFF

    _EPROM4 pin 22;                                 "Eprom 4 $20000-$27FFF


    "Identifier Definition
    Address = [A19,A18,A17,A16, A15,A14,A13,A12, A11,A10,A9,A8,
               X,X,X,X,       X,X,X,X];
```

```
equations
    "Output Enable
    !_RE    = RW;


    "Write Enable
    !_WE    = P02 & !RW;


    "Expanded RAM CHIP ENABLE ( 2K x 8 bit RAM )
    !_RAM   = P02 & ( Address >= ^h06000 ) & ( Address <= ^h067FF );


    "_SYSEP  : SYSTEM S/W
    !_SYSEP  = P02 & ( Address >= ^h00C00 ) & ( Address <= ^h05FFF );


    "_EPROM1 : CHIP ENABLE OF FONT/DATA EPROM 1
    !_EPROM1 = P02 & ( Address >= ^h08000 ) & ( Address <= ^h0FFFF );


    "_EPROM2 : CHIP ENABLE OF FONT/DATA EPROM 2
    !_EPROM2 = P02 & ( Address >= ^h10000 ) & ( Address <= ^h17FFF );


    "_EPROM3 : CHIP ENABLE OF FONT/DATA EPROM 3
    !_EPROM3 = P02 & ( Address >= ^h18000 ) & ( Address <= ^h1FFFF );


    "_EPROM4 : CHIP ENABLE OF FONT/DATA EPROM 4
    !_EPROM4 = P02 & ( Address >= ^h20000 ) & ( Address <= ^h27FFF );
```

```
"Test Vectors

"Address Decoding Test Vector
test_vectors (
        [P02,A19,A18,A17,A16,A15,A14,A13,A12,A11,A10,A9,A8]
         ->[_RAM,_SYSEP,_EPROM1,_EPROM2,_EPROM3,_EPROM4]
        )

     "                               ~ ~ ~ ~
     "                              ~ E E E E
     "                               S P P P P
     "                              ~ Y R R R R
     "P A A A A A A A A A A         R S O O O O
     "0 1 1 1 1 1 1 1 1 1 A A     A E M M M M
     "2 9 8 7 6 5 4 3 2 1 0 9 8   M P 1 2 3 4

"RAM CHIP ENABLE : $06000-$067FF
     [H,L,L,L,L,L,H,H,L,L,X,X,X]->[L,H,H,H,H,H];

"SYSTEM EPROM CHIP ENABLE : $00C00-$06FFF
     [H,L,L,L,L,L,L,L,L,H,H,X,X]->[H,L,H,H,H,H];    "$00C00-$00FFF
     [H,L,L,L,L,L,L,L,H,X,X,X,X]->[H,L,H,H,H,H];    "$01000-$01FFF
     [H,L,L,L,L,L,L,H,L,X,X,X,X]->[H,L,H,H,H,H];    "$02000-$03FFF
     [H,L,L,L,L,L,H,L,X,X,X,X,X]->[H,L,H,H,H,H];    "$04000-$05FFF

"EPROM 1 CHIP ENABLE : $08000-$0FFFF
     [H,L,L,L,L,H,X,X,X,X,X,X,X]->[H,H,L,H,H,H];

"EPROM 2 CHIP ENABLE : $10000-$17FFF
     [H,L,L,L,H,L,X,X,X,X,X,X,X]->[H,H,H,L,H,H];

"EPROM 3 CHIP ENABLE : $18000-$1FFFF
     [H,L,L,L,H,H,X,X,X,X,X,X,X]->[H,H,H,H,L,H];

"EPROM 4 CHIP ENABLE : $20000-$27FFF
     [H,L,L,H,L,L,X,X,X,X,X,X,X]->[H,H,H,H,H,L];

"CHIP UN-SELECT
     [L,X,X,X,X,X,X,X,X,X,X,X,X]->[H,H,H,H,H,H];


"Read and Write Enable
test_vectors ( [RW,P02] ->[_RE,_WE] )
        [ H,  H] ->[  L,  H];
        [ H,  L] ->[  L,  H];
        [ L,  H] ->[  H,  L];
        [ L,  L] ->[  H,  H];


end L10APPLICATION;
```

M6805 Portable Cross Assembler 0.05 MS-DOS/PC-DOS Page 1
Mon Sep 09 11:26:57 1991
Command line:
C:\PASM\PASM05.EXE -EQSUX -L keyscan.LST -O keyscan.OBJ keyscan.ASM
Options list:
ON - b - Printing of macro definitions
ON - c - Printing of macro calls
OFF - d - Placing of symbolic debugging information in COFF
ON - e - Printing of macro expansions (changed)
ON - f - Printing of conditional directives
OFF - g - Printing of generated constants list
ON - q - Expanding and printing of structured syntax (changed)
ON - s - Printing of symbol table (changed)
ON - u - Printing of conditional unassembled source (changed)
ON - x - Printing of cross reference table (changed)
OFF - m - Suppress printing of error messages
ON - w - Printing of warning messages
OFF - v - Suppress printing of updated status
OFF - y - Enabling of sgs extensions
ON - o - Create object code
ON - - Formatting of source line listing
Create listing file - l - keyscan.LST
Change object file name - o - keyscan.OBJ

Xdefs:
NONE

Xrefs:

RC00	RC01	RC02	RC03	RC10	RC11	RC12	RC13	RC20	RC21	RC22
RC23	RC30	RC31	RC32	RC33	RC40	RC41	RC42	RC43	RC50	RC51
RC52	RC53									

Input file(s): keyscan.ASM (280 lines)

Output file: keyscan.OBJ
Listing file: keyscan.LST

```
S PC    OPCO OPERANDS S LABEL   MNEMO OPERANDS COMMENT
                        *****************************************************************************
                        *
                        *         FILE NAME:  KEYSCAN.ASM          DATE: 27th Jan., 1991
                        *
                        *         FILE DESCRIPTION: KEYSCAN PROGRAM FOR MC68HC05L10
                        *                KEYSCAN PROGRAM FOR M x N KEY PAD by PORTA and PORTB
                        *                This program can be used for any M x N (8 x 8 max )
                        *                keypad detection. User can run his/her own
                        *                decoding scheme for his/her own application.
                        *
                        *         REVISION: 1.0
                        *
                        *         AUTHOR: JAMSON CHEUNG
                        *
                        *         Remark: This application is fully compiled by MOTOROLA PASM05
                        *                 cross compiler
                        *
                        *         Program Latest Update:
                        *         Rev 1.0      Date: 30th Jan., 1991
                        *                           ORGINIAL RELEASE
                        *
                        *****************************************************************************
                        *
                        *
                                  OPT  NOP    SET NO PAGE HEADER FOR EACH PAGE
                        *                             *
                        * KEYSCAN FOR THE MC68HC05L10 MCU
                        *                             *
                                  OPT  MUL
                        *
                        *
                        *
                                  XREF  RC00,RC01,RC02,RC03
                                  XREF  RC10,RC11,RC12,RC13
                                  XREF  RC20,RC21,RC22,RC23
                                  XREF  RC30,RC31,RC32,RC33
                                  XREF  RC40,RC41,RC42,RC43
                                  XREF  RC50,RC51,RC52,RC53

                        *
                        *         KEY PAD DEFINITION TABLE
                        *
A 3000                            ORG  $3000
                        KEYDEF
A 3000  00000000 X                FDB  RC00,RC01,RC02,RC03
A 3008  00000000 X                FDB  RC10,RC11,RC12,RC13
A 3010  00000000 X                FDB  RC20,RC21,RC22,RC23
A 3018  00000000 X                FDB  RC30,RC31,RC32,RC33
A 3020  00000000 X                FDB  RC40,RC41,RC42,RC43
A 3028  00000000 X        FDB  RC50,RC51,RC52,RC53
                        *
                        * SYSTEM EQUATES
                        *
```

```
A 3030  0007  A BIT7    EQU  $07
A 3030  0006  A BIT6    EQU  $06
A 3030  0005  A BIT5    EQU  $05
A 3030  0004  A BIT4    EQU  $04
A 3030  0003  A BIT3    EQU  $03
A 3030  0002  A BIT2    EQU  $02
A 3030  0001  A BIT1    EQU  $01
A 3030  0000  A BIT0    EQU  $00
              *
              *
              **********************************************************************************
              *
              *  I/O REGISTER DEFINITIONS
              *
A 3030  0000  A PORTA   EQU  $00   I/O PORT A OFFSET
A 3030  0001  A PORTB   EQU  $01   I/O PORT B OFFSET
A 3030  0002  A PORTC   EQU  $02   I/O PORT C OFFSET
A 3030  0003  A PORTD   EQU  $03   I/0 PORT D OFFSET
A 3030  0004  A PORTE   EQU  $04   I/O PORT E OFFSET
A 3030  0005  A DDR     EQU  $05   DATA DIRECTION REGISTER OFFSET
A 3030  0005  A DDRA    EQU  PORTA+DDR PORTA DDR
A 3030  0006  A DDRB    EQU  PORTB+DDR PORTB DDR
A 3030  0007  A DDRC    EQU  PORTC+DDR PORTC DDR
A 3030  0009  A DDRE    EQU  PORTE+DDR PORTE DDR
              *
              *
              *  CONTROL REGISTERS
              *
A 3030  001c  A CTRL$1C EQU  $1C   CONTROL REGISTER $1C
A 3030  0007  A TIMI    EQU  BIT7
A 3030  0006  A CLKS    EQU  BIT6
A 3030  0005  A IR1F    EQU  BIT5
A 3030  0004  A IR2F    EQU  BIT4
A 3030  0003  A PORTI   EQU  BIT3
A 3030  0002  A SECF    EQU  BIT2
A 3030  0001  A ALF     EQU  BIT1
A 3030  0000  A RTCF    EQU  BIT0

A 3030  0026  A CTRL$26 EQU  $26   CONTROL REGISTER $26
A 3030  0007  A TONE    EQU  BIT7
A 3030  0006  A PLLI    EQU  BIT6
A 3030  0005  A IR1O    EQU  BIT5
A 3030  0004  A IR2O    EQU  BIT4
A 3030  0003  A DON     EQU  BIT3
A 3030  0002  A AUTO    EQU  BIT2
A 3030  0001  A TONS    EQU  BIT1
A 3030  0000  A MS      EQU  BIT0

A 3030  0027  A CTRL$27 EQU  $27   CONTROL REGISTER $27
A 3030  0006  A FS1     EQU  BIT6
A 3030  0005  A FS0     EQU  BIT5
A 3030  0004  A KEYE    EQU  BIT4
A 3030  0002  A SECE    EQU  BIT2
A 3030  0001  A ALE     EQU  BIT1
A 3030  0000  A RTCE    EQU  BIT0

              *********************************************************************
              *********************************************************************
A 0050              org  $50    Variable Segment
```

```
A 0050 cd  ffff   A KEYSUB        JSR  $FFFF
A 0053     0051   A KEYADD        EQU  *-2
A 0053 81                RTS

A 0054     01     A KEYFLAG       RMB  1     Keyboard flag
A 0055     01     A KEYA          RMB  1
A 0056     01     A KEYB          RMB  1
A 0057     01     A COLX          RMB  1
A 0058     01     A ROWX          RMB  1

                         *
                         * KEYPAD DEFINITION
                         * THE MAX. NUMBER OF DEFINITION FOR THIS KEYPAD IS 64
                         * SUPPOSE ALL THE LOWER ORDER OF THE PORT ARE USED UP FIRST
                         *
A 0059     0005   A KEYNUMA       EQU  5     NUMBER OF PORT A ARE USED FOR KEYPAD
A 0059     0004   A KEYNUMB       EQU  4     NUMBER OF PORT B ARE USED FOR KEYPAD
A 0059     001f   A MASKPA        EQU  $FF!>(8-KEYNUMA) MASK FOR MASKING PORTA DATA
A 0059     000f   A MASKPB        EQU  $FF!>(8-KEYNUMB) MASK FOR MASKING PORTB DATA



                  *********************************************************************
                  *********************************************************************
A 0de2                            ORG  $0DE2
A 0de2 ad  06  0dea      MAIN     BSR  INIT
A 0de4 ad  10  0df6               BSR  KBINIT
A 0de6 9a                         CLI
A 0de7 8e                STOP     STOP
A 0de8 20  fd  0de7               BRA  STOP

                         *
                         * System Initialization
                         *
A 0dea 1c  1c    A       INIT     BSET CLKS,CTRL$1C SELECT PLL CLOCK FOR CPU
A 0dec 1c  27    A                BSET FS1,CTRL$27 SELECT 7.3728 MHz PLL OUTPUT CLOCK FREQ
A 0dee 1a  27    A                BSET FS0,CTRL$27
A 0df0 0d  26fd 0df0              BRCLR PLLI,CTRL$26,* WAIT UNTIL PLL CLOCK IS STABLE
A 0df3 3f  00    A                CLR  PORTA   CLEAR ANY UNNECCESSARY KEYBOARD INTERRUPT
A 0df5 81                         RTS


                         *
                         * Keyboard System Initialization
                         *
A 0df6 3f  05    A       KBINIT   CLR  DDRA    SELECT PORTA AS INPUT PORT
A 0df8 3f  00    A                CLR  PORTA   PREPARE FOR KEYBOARD INTERRUPT
A 0dfa a6  0f    A                LDA  #MASKPB
A 0dfc b7  06    A                STA  DDRB    SELECT PORTB AS OUTPUT PORT
A 0dfe 3f  01    A                CLR  PORTB
A 0e00 81                         RTS

                         *********************************************************************
                         *********************************************************************
                         *
                         * Keyboard Interrupt Service Routine
                         *
                         KEYISR
```

```
A 0e01 3f  54     A                    CLR  KEYFLAG
A 0e03 a6  ff     A                    KEYSCAN LDA  #$FF
A 0e05 b7  01     A                    STA  PORTB
A 0e07 17  01     A                    BCLR  KEYNUMB-1,PORTB START CHECKING FROM KEYPAD WITH
                                       HIGHEST PORTB
A 0e09 b6  00     A                    REPEAT  LDA  PORTA   START SCANNING FROM THE BOTTOM ROW
A 0e0b a4  1f     A                    AND  #MASKPA
A 0e0d a1  1f     A                    CMP  #MASKPA
A 0e0f 26  06     0e17                 BNE  GOTIT   KEY FOUND IS Z=1
A 0e11 34  01     A                    LSR  PORTB   OTHERWISE, FOR NEXT COLUMN
A 0e13 25  f4     0e09                 BCS  REPEAT
A 0e15 20  1b     0e32                 BRA  DONE
A 0e17 00  5414   0e2e     GOTIT       BRSET BIT0,KEYFLAG,NOSAVE
A 0e1a a6  0f     A                    LDA  #MASKPB
A 0e1c 43                              COMA
A 0e1d ba  56 A                        ORA  KEYB
A 0e1f b7  56     A                    STA  KEYB    SAVE KEYB
A 0e21 a6  1f     A                    LDA  #MASKPA
A 0e23 43                              COMA
A 0e24 ba  55     A                    ORA  KEYA
A 0e26 b7  55     A                    STA  KEYA    SAVE KEYA
A 0e28 ad  0b     0e35                 BSR  DBOUNC  CHECK FOR NOISE
A 0e2a 10  54     A                    BSET BIT0,KEYFLAG SET KEYBOARD FLAG
A 0e2c 20  d5     0e03                 BRA  KEYSCAN
A 0e2e ad  05     0e35     NOSAVE      BSR  DBOUNC  PAUSE
A 0e30 ad  0e     0e40                 BSR  DECODE  GO TO USER KEY DECODE ROUTINE
A 0e32 ad  c2     0df6     DONE        BSR  KBINIT  PREPARE THE SCAN LINES FOR NEXT INTERRUPT
A 0e34 80                              RTI
                           *
                           * DEBOUNCE ROUTINE
                           * DELAY FOR A SHORT PERIOD OF TIME
                           *
A 0e35 a6  5a     A        DBOUNC      LDA  #90
A 0e37 ae  ff     A        AGAIN1      LDX  #$FF
A 0e39 5a                  AGAIN       DECX
A 0e3a 26  fd     0e39                 BNE     AGAIN
A 0e3c 4a                              DECA
A 0e3d 26  f8     0e37                 BNE  AGAIN1
A 0e3f 81                              RTS
                           *
                           * DECODE ROUTINE
                           *
                           DECODE
A 0e40 b6  55     A                    LDA  KEYA    DETERMINE WHICH COLUMN IS DETECTED
A 0e42 ae  ff     A                    LDX  #$FF
A 0e44 5c                  CHKA        INCX
A 0e45 44                              LSRA
A 0e46 25  fc     0e44                 BCS  CHKA
```

```
A 0e48 bf  58    A                  STX  ROWX    ROWX <= 7
A 0e4a b6  56    A                  LDA  KEYB    DETERMINE WHICH ROW IS DETECTED
A 0e4c ae  ff    A                  LDX  #$FF
A 0e4e 5c                 CHKB      INCX
A 0e4f 44                           LSRA
A 0e50 25  fc    0e4e               BCS  CHKB
A 0e52 bf  57    A                  STX  COLX    COLX <= 7
                          * CALCULATE THE OFFSET FROM KEYDEF TABLE WHICH IS EQUAL TO
                          * (ROWX * NUMBER OF COLUMN * 2) + (COLX * 2)
A 0e54 b6  58    A                  LDA  ROWX
A 0e56 ae  04    A                  LDX  #KEYNUMB
A 0e58 58                           LSLX         MULTIPLE BY 2
A 0e59 42                           MUL          PRODUCT <= 128 ( FOR 8 x 8 PAD )
A 0e5a bb  57    A                  ADD  COLX
A 0e5c bb  57    A                  ADD  COLX    2 BYTE ADDRESS IN THE KEYDEF TABLE
                          *                  A = OFFSET OF THE ADDRESS FROM BEGINNING OF
                          *                  THE KEYDEF TABLE
A 0e5e 97                           TAX
A 0e5f d6  3000  A                  LDA  KEYDEF,X LOAD THE UPPER BYTE OF THE ADDRESS
A 0e62 b7  51    A                  STA  KEYADD
A 0e64 d6  3001  A                  LDA  KEYDEF+1,X LOAD THE LOWER BYTE OF THE ADDRESS
A 0e67 b7  52    A                  STA  KEYADD+1
A 0e69 bd  50    A                  JSR  KEYSUB  EXECUTE RAM SUBROUTINE
A 0e6b 81                           RTS
                          *
                          * DUMMY INTERRUPT SERVICE ROUTINE
                          *
                          SPIISR
                          RTCISR
                          SCIISR
                          TIMISR
                          EIRQISR
A 0e6c 80                 SWIISR    RTI
A 0c00                              ORG  $0C00
A 0c00      0e6c          A SPIIRQ  FDB  SPIISR  SPI INTERRUPT VECTOR
A 0c02      0e6c          A RTCIRQ  FDB  RTCISR  REAL TIME CLOCK INTERRUPT VECTOR
A 0c04      0e6c          A SCIIRQ  FDB  SCIISR  SCI INTERRUPT VECTOR
A 0c06      0e6c          A TIMIRQ  FDB  TIMISR  TIMER INTERRUPT VECTOR
A 0c08      0e01          A KEYIRQ  FDB  KEYISR  KEYBOARD INTERRUPT VECTOR
A 0c0a      0e6c          A EIRQ    FDB  EIRQISR EXTERNAL INTERRUPT VECTOR
A 0c0c      0e6c          A SWIVCT  FDB  SWIISR  SOFTWARE INTERRUPT VECTOR
A 0c0e      0de2          A         FDB  MAIN    RESET INTERRUPT VECTOR
                                    END
```

Total number of errors: 0
Total number of warnings: 0
Total number of lines: 280

Number of bytes in section ASCT: 212

Number of bytes in program: 212

CROSS REFERENCE TABLE

NAME	ATTRB S VALUE	P:LINE LINE1....N
RC00	XREF X 0000	45
RC01	XREF X 0000	45
RC02	XREF X 0000	45
RC03	XREF X 0000	45
RC10	XREF X 0000	46
RC11	XREF X 0000	46
RC12	XREF X 0000	46
RC13	XREF X 0000	46
RC20	XREF X 0000	47
RC21	XREF X 0000	47
RC22	XREF X 0000	47
RC23	XREF X 0000	47
RC30	XREF X 0000	48
RC31	XREF X 0000	48
RC32	XREF X 0000	48
RC33	XREF X 0000	48
RC40	XREF X 0000	49
RC41	XREF X 0000	49
RC42	XREF X 0000	49
RC43	XREF X 0000	49
RC50	XREF X 0000	50
RC51	XREF X 0000	50
RC52	XREF X 0000	50
RC53	XREF X 0000	50

M6805 Portable Cross Assembler 0.05 MS-DOS/PC-DOS Page 1
Tue Sep 10 16:30:55 1991
Command line:
C:\PASM\PASM05.EXE -EQSUX -L DPROG.LST -O DPROG.OBJ DPROG.ASM
Options list:
ON - b - Printing of macro definitions
ON - c - Printing of macro calls
OFF - d - Placing of symbolic debugging information in COFF
ON - e - Printing of macro expansions (changed)
ON - f - Printing of conditional directives
OFF - g - Printing of generated constants list
ON - q - Expanding and printing of structured syntax (changed)
ON - s - Printing of symbol table (changed)
ON - u - Printing of conditional unassembled source (changed)
ON - x - Printing of cross reference table (changed)
OFF - m - Suppress printing of error messages
ON - w - Printing of warning messages
OFF - v - Suppress printing of updated status
OFF - y - Enabling of sgs extensions
ON - o - Create object code
ON - - Formatting of source line listing
Create listing file - l - DPROG.LST
Change object file name - o - DPROG.OBJ

Xdefs:
NONE

Xrefs:
NONE

Input file(s): DPROG.ASM (821 lines)

Output file: DPROG.OBJ
Listing file: DPROG.LST

```
M6805 Portable Cross Assembler  0.05  DPROG.ASM  Page 2
 Tue Sep 10 116:30:55 1991
Options - MD,MC,NOG,U,W,MEX,CL,FMT,O

LINE   S PC   OPCO OPERANDS S LABEL    MNEMO OPERANDS COMMENT
                    ******************************************************************************
                    *
                    * FILE NAME:  DPROG.ASM                  DATE: 8th Feb., 1991
                    *
                    * FILE DESCRIPTION: MC68HC05L10 MCU DEMONSTRATION PROGRAM
                    *               a) ONE SLAVE LCD DRIVER PROGRAM
                    *               b) USING MMU TO ACCESS THE MEMORY MAP THAT
                    *                 GREATER THAN 64KByte MEMORY
                    *
                    * REVISION: 1.0
                    *
                    * AUTHOR: JAMSON CHEUNG
                    *
                    * REMARK: THIS FILE CONTAINS THE SOURCE PROGRAM AND SOME BUFFERS
                    *        THIS PROGRAM MUST BE LOCATED IN BANK 0
                    *        THE SYMBOL PATTERN DATA FILES ARE
                    *              a) DROM1.ASM
                    *              b) DROM2.ASM
                    *
                    ******************************************************************************
                    *
                    *
                          OPT   NOP     SET NO PAGE HEADER FOR EACH PAGE
                    *
                    * ADDRESS LOCATION EQUATE
                    *
                    *
                    *     EXTERNAL EXPANDED RAM SECTION   $6000 - $67FF
                    *
      P 0000   6000     A EXTRAM   EQU   $6000
                    *
                    *
                    * INTERNAL DATA/PROGRAMMING ROM   $0DE2 - $3FFF
                    *
      P 0000   0de2     A INTROM   EQU   $0DE2

                    *
                    * EXTERNAL FONT DATA ROM region        $10000-$14FFF
                    *
      P 0000   8000     A OFF6x8   EQU   $8000   COMBINE WITH MMU (PHYSICAL ADD=$10000)
      P 0000   c000     A OFF16x16 EQU   $C000   COMBINE WITH MMU (PHYSICAL ADD=$14000)

      P 0000   8000     A TAB1     EQU   OFF6x8
      P 0000   8100     A TAB2     EQU   OFF6x8+$100
      P 0000   c000     A TAB3     EQU   OFF16x16
      P 0000   c100     A TAB4     EQU   OFF16x16+$100
                    *
                    * SYSTEM EQUATES
                    *
```

```
P 0000    0007   A BIT7    EQU  $07
P 0000    0006   A BIT6    EQU  $06
P 0000    0005   A BIT5    EQU  $05
P 0000    0004   A BIT4    EQU  $04
P 0000    0003   A BIT3    EQU  $03
P 0000    0002   A BIT2    EQU  $02
P 0000    0001   A BIT1    EQU  $01
P 0000    0000   A BIT0    EQU  $00
                 *
                 *  CONTROL REGISTERS
                 *
P 0000    001c   A CTRL$1C EQU  $1C     CONTROL REGISTER $1C
P 0000    0007   A TIMI    EQU  BIT7
P 0000    0006   A CLKS    EQU  BIT6
P 0000    0005   A IR1F    EQU  BIT5
P 0000    0004   A IR2F    EQU  BIT4
P 0000    0003   A PORTI   EQU  BIT3
P 0000    0002   A SECF    EQU  BIT2
P 0000    0001   A ALF     EQU  BIT1
P 0000    0000   A RTCF    EQU  BIT0

P 0000    0026   A CTRL$26 EQU  $26     CONTROL REGISTER $26
P 0000    0007   A TONE    EQU  BIT7
P 0000    0006   A PLLI    EQU  BIT6
P 0000    0005   A IR1O    EQU  BIT5
P 0000    0004   A IR2O    EQU  BIT4
P 0000    0003   A DON     EQU  BIT3
P 0000    0002   A AUTO    EQU  BIT2
P 0000    0001   A TONS    EQU  BIT1
P 0000    0000   A MS      EQU  BIT0

P 0000    0027   A CTRL$27 EQU  $27     CONTROL REGISTER $27
P 0000    0006   A FS1     EQU  BIT6
P 0000    0005   A FS0     EQU  BIT5
P 0000    0004   A KEYE    EQU  BIT4
P 0000    0002   A SECE    EQU  BIT2
P 0000    0001   A ALE     EQU  BIT1
P 0000    0000   A RTCE    EQU  BIT0

                 *
                 *  MMU REGISTERS
                 *
P 0000    0022   A MMUCB   EQU  $22     MMU COMMON BANK REGISTER
P 0000    0020   A MMUPA1  EQU  $20     MMU BANK 1 OFFSET REGISTER
P 0000    0021   A MMUPA2  EQU  $21     MMU BANK 2 OFFSET REGISTER
                 *
                 *
P 0000    0080   A LCDCOL  EQU  128     LCD SIZE = LCDCOL x LCDROW = 128 x 40
P 0000    0028   A M41LCDR EQU  40      LCDROW = M41LCDR (41 mux) or M32LCDR (32 mux)
P 0000    0020   A M32LCDR EQU  32
P 0000    00fa   A BUFSIZE EQU  (LCDCOL/5)*(M41LCDR/8)*2
P 0000    0020   A BLANK   EQU  $20     BLANK CODE
```

```
                  ***********************************************************************
                  ***********************************************************************
                  **
                  **     VARIOUS TABLE/DATA BUFFER DEFINITION
                  **
                  ***********************************************************************

                  ***********************************************************************
                  **
                  **    SYMBOL PATTERN TABLE OFFSET DEFINITION
                  **
                  ***********************************************************************
P 0000    0000    A XSIZE    EQU  0
P 0000    0001    A YSIZE    EQU  1
P 0000    0003    A TABRECSIZE EQU 3     2 BYTE SYMBOL CODE, 1 BYTE OFFSET

                  ***********************************************************************
A 0de2                 ORG  INTROM
                  ***********************************************************************
                  **
                  **    P_TAB - TABLE OF PATTERN SYMBOL PATTERN TABLE POINTER
                  **
                  **    EACH RECORD HAS 5 BYTE (P_TABRECSIZE)
                  **
                  **    P_TAB RECORD FORMAT
                  **        FIRST 2 BYTE : SYMBOL PATTERN TABLE POINTER
                  **        3rd BYTE    : CORRESPONDING MMU COMMON BANK DATA
                  **        4th BYTE    : CORRESPONDING MMU OFFSET REGISTER 1 DATA
                  **        5th BYTE    : CORRESPONDING MMU OFFSET REGISTER 2 DATA
                  **
                  ***************************************************************************
                  P_TAB
A 0de2    8000  A  P_REC0   FDB   TAB1        RECORD #0
A 0de4    c8    A           FCB   $C8         COMMON BANK VALUE
A 0de5    08    A           FCB   8           POSA1 VALUE
A 0de6    00    A           FCB   0           POSA2 VALUE
                   E_REC0
A 0de7    8100  A  P_REC1   FDB   TAB2        RECORD #1
A 0de9    c8    A           FCB   $C8         COMMON BANK VALUE
A 0dea    08    A           FCB   8           POSA1 VALUE
A 0deb    00    A           FCB   0           POSA2 VALUE
                   E_REC1
A 0dec    c000  A  P_REC2   FDB   TAB3        RECORD #2
A 0dee    c8    A           FCB   $C8         COMMON BANK VALUE
A 0def    00    A           FCB   0           POSA1 VALUE
A 0df0    08    A           FCB   8           POSA2 VALUE
                   E_REC2
A 0df1    c100  A  P_REC3   FDB   TAB4        RECORD #3
A 0df3    c8    A           FCB   $C8         COMMON BANK VALUE
A 0df4    00    A           FCB   0           POSA1 VALUE
A 0df5    08    A           FCB   8           POSA2 VALUE
                   E_REC3
A 0df6    60fa  A  P_RECB   FDB   TABLANK     RECORD BLANK
A 0df8    ff    A           FCB   $FF         COMMON BANK VALUE
```

```
A 0df9   00     A           FCB   0            POSA1 VALUE
A 0dfa   00     A           FCB   0            POSA2 VALUE
                  E_RECB
A 0dfb   0000 A P_RECE     FDB   00           LAST RECORD INDICATOR
A 0dfd   00     A           FCB   00           COMMON BANK VALUE
A 0dfe   00     A           FCB   0            POSA1 VALUE
A 0dff   00     A           FCB   0            POSA2 VALUE
                  E_RECE
A 0e00   0e00 A P_END      EQU   *
              ******************************************************************
              **
              **     P_TAB TABLE OFFSET DEFINITION
              **
              ******************************************************************
A 0e00   0002   A P_OFFCB  EQU  2      P_TAB COMMON BANK DATA POINTER
A 0e00   0003   A P_OFFPA1 EQU  3      P_TAB OFFSET REGISTER 1 DATA POINTER
A 0e00   0004   A P_OFFPA2 EQU  4      P_TAB OFFSET REGISTER 2 DATA POINTER
A 0e00   0005   A P_RECSIZE EQU  E_REC0-P_REC0
              ******************************************************************
              **
              **    WELCOME BUFFER
              **
              ******************************************************************
A 0e00   a140a140 A WELCOME  FDB   $A140,$A140,$C577,$AAEF,$BB59,$C17B,$A140,$A140
A 0e10   a140b855 A          FDB   $A140,$B855,$A44F,$AABF,$B4E4,$A4A4,$A4DF,$A140
A 0e20   00200057 A          FDB   ' ','W','E','L','C','O','M','E',' ','T','O',' '
A 0e38   004d004f A          FDB   'M','O','T','O','R','O','L','A',' ',
A 0e4c   0000   A       FDB   $00
A 0e4e   0e4e   A WELEND   EQU   *
              ******************************************************************
              **
              **     EXTERNAL RAM REGION - BUFFER DEFINITIONS
              **
              ******************************************************************
A 6000                ORG   EXTRAM
A 6000   fa     A BUF     RMB   BUFSIZE
A 60fa   00     A TABLANK FCB   0
A 60fb   00     A         FCB   0
A 60fc   0020   A         FDB   BLANK    BLANK CODE NUMBER
A 60fe   05     A         FCB   SYMBLANK-TABLANK
              SYMBLANK
A 60ff   fb     A         RMB   $100-(*-TABLANK)
A 61fa   61fa   A TABLKE  EQU   *
```

```
                 ************************************************************************
                 ************************************************************************
                 **
                 **    RAM SECTION - VARIABLE DEFINITIONS
                 **
                 ************************************************************************
A 0050                      ORG   $50
A 0050 d6  ffff    A LDD    LDA   $FFFF,X
A 0053 81                   RTS
A 0054 d6  ffff    A MVV    LDA   $FFFF,X
A 0057 d7  ffff    A STT    STA   $FFFF,X
A 005a 81                   RTS

A 005b    0051   A SOURCE   EQU  LDD+1   THE 2-BYTE INDEX OF LDD RAM SUBROUTINE
A 005b    0055   A MSRC     EQU  MVV+1   THE 2-BYTE INDEX OF MVV RAM SUBROUTINE
A 005b    0058   A DESTINE  EQU  STT+1   THE 2-BYTE INDEX OF STT RAM SUBROUTINE

A 005b   01   A BUFPTR   RMB  1    BUFFER POINTER
A 005c   01   A LCDPTR   RMB  1    LCD COLUMN POINTER
A 005d   01   A TABPTR   RMB  1    SYMBOL PATTERN POINTER
A 005e   01   A CHARROW  RMB  1    CHARSIZE = CHARROW x CHARCOL
A 005f   01   A CHARCOL  RMB  1
A 0060   01   A CHARBYT  RMB  1    NUMBER OF BYTE TO REPRESENT ONE SYMBOL
A 0061   01   A COUNT    RMB  1    SYMBOL PATTERN SIZE COUNTER
A 0062   02   A DEST     RMB  2    TEMPORARY 2 BYTE INDEX STORAGE
A 0064   01   A TPTR     RMB  1    TEMPORARY SYMBOL PATTERN POINTER
A 0065   01   A FOUND    RMB  1    FLAG FOR LOCATING THE SYMBOL PATTERN
A 0066   01   A P_TPTR   RMB  1    SYMBOL PATTERN TABLE POINTER
A 0067   02   A CHAR     RMB  2    CURRENT SYMBOL CODE
A 0069   01   A TEMP     RMB  1    TEMPORARY VARIABLE 1
A 006a   02   A TABCODE  RMB  2    TEMPORARY VARIABLE 2
A 006c   03   A MMU      RMB  3    TEMPORARY STORAGE FOR MMU REGISTER
A 006f   01   A DISPROW  RMB  1    CURRENT DISPLAY ROW
                 *                 (0..4 for 41 MUX;0..3 for 32 MUX )
A 0070   01   A LCDROW   RMB  1    EQUAL TO 40 FOR 41 MUX; 32 FOR 32 MUX

                 ************************************************************************
                 ************************************************************************
                 **
                 **    Name:  BLOCK - TEMPORARY BUFFER FOR SCROLLING
                 **
                 ************************************************************************
A 0100                      ORG   $0100
A 0100   20   A BLOCK    RMB  32   TEMPORARY BUFFER ( 32 BYTE )

                 ***************************************************************************
A 1c30                      ORG   INTROM+WELEND
                 ***************************************************************************
                 **
                 **    Name:  RESET - MAIN PROGRAM
```

```
                 **
                 ****************************************************************************
A 1c30 ad  0a   1c3c RESET   BSR  SYSINIT
A 1c32 ad  1d   1c51         BSR  LCDINIT
A 1c34 cd  1cc0   A          JSR  DISPBUF  DISPLAY 2 LINE OF CHINESE CHARACTERS
                 *                         AND THEN A LINE OF ENGLISH MESSAGE
A 1c37 cd  1e20   A KEEP_S   JSR  SCROLL5  SCROLLING THE 5th ROW
A 1c3a 20  fb   1c37         BRA  KEEP_S   KEEP SCROLLING


                 ****************************************************************************
                 **
                 **     Name:  SYSINIT - SYSTEM INITIALIZATION
                 **
                 **     Return: A and X will be destroyed
                 **
                 ****************************************************************************
                 SYSINIT

                 * SET UP BUS FREQUENCY

A 1c3c 1d  1c     A         BCLR  CLKS,CTRL$1C SELECT 32KHz CLOCK FOR CPU
A 1c3e 1c  27     A         BSET  FS1,CTRL$27 SELECT 2.4576 MHz FOR PLL
A 1c40 1b  27     A         BCLR  FS0,CTRL$27

                 *     2 msec delay loop is necessary for
                 *         1) clearing the previous PLLI bit and
                 *         2) setting the current PLLI if PLL is locked
                 *
                 *     Current Bus speed is 16KHz
                 *     2 msec is equivalent to 32 bus cycle = 2 + 5*(3+3) cycle
                 *
A 1c42 a6  05     A         LDA   #$5      2 cycle
A 1c44 4a          PLLD     DECA           3 cycle
A 1c45 26  fd   1c44        BNE   PLLD     DELAY COUNTER, 3 cycle

A 1c47 0d  26fd 1c47        BRCLR PLLI,CTRL$26,* WAIT UNTIL PLL CLOCK IS STABLE
A 1c4a 1c  1c     A         BSET  CLKS,CTRL$1C SET THE BUS CLOCK = PLL

A 1c4c 16  26     A         BSET  DON,CTRL$26 TURN ON LCD
A 1c4e 10  26     A         BSET  MS,CTRL$26 SELECT 1:41 MUX

A 1c50 81                   RTS

                 ****************************************************************************
                 **
                 **     Name:  LCDINIT - LCD SUBSYSTEM INITIALIZATION
                 **
                 **     Return: A and X will be destroyed
                 **
                 ****************************************************************************
                 LCDINIT
A 1c51 a6  10     A         LDA   #16      DISPLAY THE WELCOME MESSAGE
A 1c53 b7  5f     A         STA   CHARCOL  FIRST TWO LINES ARE CHINESE CHARACTERS
```

```
A 1c55 a6  02    A       LDA  #2     LAST LINE IS A ENGLISH MESSAGE
A 1c57 b7  5e    A       STA  CHARROW
A 1c59 a6  02    A       LDA  #2
A 1c5b b7  60    A       STA  CHARBYT  2 BYTE SYMBOL CODE

A 1c5d 5f                CLRX
A 1c5e d6  0e01  A NEXTWEL LDA  WELCOME+1,X INITIALIZE THE BUFFER WITH THE
A 1c61 26  05  1c68      BNE  FILL   WELCOME MESSAGE UNTIL THE END OF THE
A 1c63 d6  0e00  A       LDA  WELCOME,X RECORD IS DETECTED
A 1c66 27  10  1c78      BEQ  FILLSP

A 1c68 d6  0e00  A FILL  LDA  WELCOME,X
A 1c6b d7  6000  A       STA  BUF,X
A 1c6e d6  0e01  A       LDA  WELCOME+1,X
A 1c71 d7  6001  A       STA  BUF+1,X
A 1c74 5c                INCX
A 1c75 5c                INCX
A 1c76 20  e6  1c5e      BRA  NEXTWEL

A 1c78 a3  fa    A FILLSP CPX  #BUFSIZE FILL THE REST OF THE BUFFER SPACE
A 1c7a 24  0e  1c8a      BHS  FILLDONE WITH SYMBOL BLANK CODE
A 1c7c a6  00    A       LDA  #(BLANK!>8)!.$FF LOAD UPPER BYTE OF THE BLANK CODE
A 1c7e d7  6000  A       STA  BUF,X
A 1c81 a6  20    A       LDA  #BLANK!.$FF LOAD LOWER BYTE OF THE BLANK CODE
A 1c83 d7  6001  A       STA  BUF+1,X
A 1c86 5c                INCX
A 1c87 5c                INCX
A 1c88 20  ee  1c78      BRA  FILLSP

                 FILLDONE
A 1c8a 01  260d 1c9a     BRCLR MS,CTRL$26,MUX32 CHECK 32 MUX ? OR 41 MUX ?

A 1c8d 4f          MUX41   CLRA
A 1c8e ae  0f    A       LDX  #$F
A 1c90 d7  01c0  A R41INIT STA  $1C0,X   CLEAR THE DATA IF THE BACKPLANE 40th
A 1c93 5a                DECX
A 1c94 2a  fa  1c90      BPL  R41INIT

A 1c96 a6  05    A       LDA  #M41LCDR/8 5 BYTE ROW AVAILABLE
A 1c98 20  02  1c9c      BRA  MUXINIT

A 1c9a a6  04    A MUX32  LDA  #M32LCDR/8 4 BYTE ROW AVAILABLE

A 1c9c b7  70    A MUXINIT STA  LCDROW   INITIALIZE THE # OF ROW AVAILABLE

A 1c9e b7  69    A       STA  TEMP    TEMP = ROW COUNTER

A 1ca0 a6  02    A CLRLCD  LDA  #2     INITIALIZE THE DISPLAY RAM BASE ADDRESS
A 1ca2 b7  58    A       STA  DESTINE
A 1ca4 3f  59    A       CLR  DESTINE+1

A 1ca6 4f          NXTCOL  CLRA
A 1ca7 5f                CLRX
A 1ca8 bd  57    A NXTCLR  JSR  STT     CLEAR THE LCD PANEL ROW BY ROW
```

```
A 1caa 5c            INCX
A 1cab a3  80    A     CPX  #LCDCOL
A 1cad 26  f9   1ca8   BNE  NXTCLR
A 1caf b6  59    A     LDA  DESTINE+1
A 1cb1 ab  80    A     ADD  #LCDCOL
A 1cb3 b7  59    A     STA  DESTINE+1
A 1cb5 b6  58    A     LDA  DESTINE
A 1cb7 a9  00    A     ADC  #$0
A 1cb9 b7  58    A     STA  DESTINE

A 1cbb 3a  69    A     DEC  TEMP
A 1cbd 26  e7   1ca6   BNE  NXTCOL  EXIT WHEN IT HITS THE LAST ROW
A 1cbf 81            RTS

                 ************************************************************************
                 ************************************************************************
                 **
                 **      Name:  DISPBUF -
                 **              GET EACH SYMBOL FROM THE BUFFER,
                 **              LOCATE THE THE CORRESPONDING SYMBOL PATTERN AND
                 **              COPY TO DISPLAY RAM
                 **
                 **      Return: A and X will be destroyed
                 **
                 ************************************************************************
                 DISPBUF
A 1cc0 3f  6f    A     CLR  DISPROW  INITIALIZE ALL THE VARIABLES
A 1cc2 3f  5b    A     CLR  BUFPTR
A 1cc4 3f  5c    A     CLR  LCDPTR
A 1cc6 3f  5d    A     CLR  TABPTR
A 1cc8 3f  59    A     CLR  DESTINE+1 INITIALIZE THE STT RAM SUBROUTINE
A 1cca a6  02    A     LDA  #2      2-BYTE INDEX IS SET TO FIRST BYTE
A 1ccc b7  58    A     STA  DESTINE  OF DISPLAY RAM

                 NEXTBUF
A 1cce b6  6f    A     LDA  DISPROW  HIT THE 5th ROW ?
A 1cd0 a1  04    A     CMP  #4
A 1cd2 25  08   1cdc   BLO  C_DISP  DISPLAY A ROW OF 6x8 ENGLISH MESSAGE
A 1cd4 a6  06    A     LDA  #6      AT THE 5th ROW
A 1cd6 b7  5f    A     STA  CHARCOL
A 1cd8 a6  01    A     LDA  #1
A 1cda b7  5e    A     STA  CHARROW

A 1cdc be  5b    A C_DISP  LDX  BUFPTR   LOAD THE SYMBOL CODE TO VARIABLE CHAR
A 1cde d6  6000  A     LDA  BUF,X
A 1ce1 b7  67    A     STA  CHAR
A 1ce3 d6  6001  A     LDA  BUF+1,X
A 1ce6 b7  68    A     STA  CHAR+1

A 1ce8 ad  2a   1d14   BSR  FPTOLCD  FIND PATTERN AND DISPLAY TO LCD

A 1cea b6  5c    A     LDA  LCDPTR  CHECK WHETHER ENOUGH LCD COLUMN SPACE
A 1cec bb  5f    A     ADD  CHARCOL  FOR ANOTHER SYMBOL
A 1cee a1  80    A     CMP  #LCDCOL
A 1cf0 23  15   1d07   BLS  NOADJ
```

```
A 1cf2 3f  5c    A       CLR  LCDPTR  INITIALIZE TO FIRST COLUMN OF NEXT ROW

A 1cf4 be  5e    A       LDX  CHARROW
A 1cf6 3c  6f    A NEXTROW  INC  DISPROW  UPDATE THE STT RAM SUBROUTINE BASE
A 1cf8 b6  59    A       LDA  DESTINE+1 ADDRESS OFFSET AND UPDATE THE ROW
A 1cfa ab  80    A       ADD  #LCDCOL  COUNTER
A 1cfc b7  59    A       STA  DESTINE+1
A 1cfe b6  58    A       LDA  DESTINE
A 1d00 a9  00    A       ADC  #0
A 1d02 b7  58    A       STA  DESTINE

A 1d04 5a                DECX
A 1d05 26  ef  1cf6      BNE  NEXTROW

A 1d07 b6  5b    A NOADJ  LDA  BUFPTR  UPDATE THE BUFFER POINTER AND POINTING
A 1d09 bb  60    A       ADD  CHARBYT  TO NEXT SYMBOL CODE
A 1d0b b7  5b    A       STA  BUFPTR

A 1d0d b6  6f    A       LDA  DISPROW  HIT THE LAST ROW ?
A 1d0f b1  70    A       CMP  LCDROW
A 1d11 25  bb  1cce      BLO  NEXTBUF
A 1d13 81                RTS

                 *************************************************************************
                 *************************************************************************
                 **
                 **     Name:  FPTOLCD -
                 **            FIND SYMBOL LOCATION AND COPY THE PATTERN TO DISPLAY
                 **            RAM
                 **            IF SYMBOL CODE FAILS TO LOCATE, A EQUIVALENT SIZE
                 **            OF SPACE WILL BE COPIED TO DISPLAY RAM
                 **
                 **     Return: A and X will be destroyed
                 **
                 *************************************************************************
                 FPTOLCD
A 1d14 b6  22    A       LDA  MMUCB   THE SYMBOL PATTERN MIGHT BE LOCATED
                 *                    IN NON BANK 0
A 1d16 b7  6c    A       STA  MMU     SAVE UP THE MMU REGISTERS BEFORE
A 1d18 b6  20    A       LDA  MMUPA1  SEARCHING START
A 1d1a b7  6d    A       STA  MMU+1
A 1d1c b6  21    A       LDA  MMUPA2
A 1d1e b7  6e    A       STA  MMU+2

A 1d20 cd  1d92   A TRY2   JSR  FINDPAT  SEARCH AND FIND THE LOCATION OF
                 *                    SYMBOL ROM PATTERN
A 1d23 27  18  1d3d      BEQ  DISP    FOUND THE SYMBOL PATTERN ?

                 * IF THE PATTERN IS NOT FOUND, SKIP WITH A BLANK SYMBOL

A 1d25 a6  00    A SKIPB  LDA  #(BLANK!>8)!.$FF LOAD THE UPPER BYTE OF THE BLANK CODE
A 1d27 b7  67    A       STA  CHAR
A 1d29 a6  20    A       LDA  #BLANK!.$FF LOAD THE LOWR BYTE OF THE BLANK CODE
A 1d2b b7  68    A       STA  CHAR+1

A 1d2d b6  5f    A       LDA  CHARCOL  BUILD THE BLANK WITH THE EQUIVALENT
```

```
A 1d2f ae  00     A      LDX  #XSIZE  SIZE
A 1d31 d7  60fa   A      STA  TABLANK,X
A 1d34 b6  5e     A      LDA  CHARROW
A 1d36 ae  01     A      LDX  #YSIZE
A 1d38 d7  60fa   A      STA  TABLANK,X
A 1d3b 20  e3  1d20      BRA  TRY2

A 1d3d cd  1d4d   A DISP    JSR  DISPLAY  COPY TO DISPLAY RAM

A 1d40 b6  6c     A      LDA  MMU     RESTORE THE MMU REGISTERS
A 1d42 b7  22     A      STA  MMUCB
A 1d44 b6  6d     A      LDA  MMU+1
A 1d46 b7  20     A      STA  MMUPA1
A 1d48 b6  6e     A      LDA  MMU+2
A 1d4a b7  21     A      STA  MMUPA2
A 1d4c 81                RTS

                  ******************************************************************************
                  ******************************************************************************
                  **
                  **     Name:  DISPLAY -
                  **                COPY THE FOUND SYMBOL PATTERN TO DISPLAY RAM
                  **
                  **     Return: A and X will be destroyed
                  **
                  ******************************************************************************
                  DISPLAY
A 1d4d b6  5f     A      LDA  CHARCOL
A 1d4f b7  61     A      STA  COUNT   INITIALIZE THE SYMBOL PATTERN SIZE
A 1d51 b6  58     A      LDA  DESTINE  COUNT
A 1d53 b7  62     A      STA  DEST    SAVE UP THE CURRENT DISPLAY RAM ROW
A 1d55 b6  59     A      LDA  DESTINE+1 BASE ADDRESS IN CASE OF PATTERN SIZE
A 1d57 b7  63     A      STA  DEST+1  OTHER THAN 1 BYTE HEIGHT

A 1d59 b6  5e     A N_COL  LDA  CHARROW
A 1d5b b7  69     A      STA  TEMP    INITIALIZE VARIABLE FOR CURRENT ROW
A 1d5d b6  5d     A      LDA  TABPTR
A 1d5f b7  64     A      STA  TPTR    INITIALIZE VARIABLE FOR PATTERN
                  *                  POINTER
A 1d61 be  64     A N_ROW  LDX  TPTR
A 1d63 bd  50     A      JSR  LDD     LOAD THE SYMBOL PATTERN BYTE BY BYTE
A 1d65 be  5c     A      LDX  LCDPTR
A 1d67 bd  57     A      JSR  STT     COPY THE SYMBOL PATTERN BYTE TO DISPLAY
A 1d69 3a  69     A      DEC  TEMP    RAM
A 1d6b 27  14  1d81      BEQ  COL_UP  EXIT IF SIGNLE ROW SYMBOL PATTERN

A 1d6d b6  64     A      LDA  TPTR
A 1d6f bb  5f     A      ADD  CHARCOL
A 1d71 b7  64     A      STA  TPTR

A 1d73 b6  59     A      LDA  DESTINE+1 UPDATE THE DISPLAY RAM ADDRESS TO NEXT
A 1d75 ab  80     A      ADD  #LCDCOL  ROW
A 1d77 b7  59     A      STA  DESTINE+1
A 1d79 b6  58     A      LDA  DESTINE
A 1d7b a9  00     A      ADC  #0
A 1d7d b7  58     A      STA  DESTINE
```

```
A 1d7f 20  e0   1d61       BRA  N_ROW   GO TO ANOTHER ROW IF NECESSARY
A 1d81 b6  62        A COL_UP  LDA  DEST    RESTORE THE DISPLAY RAM ADDRESS BACK
A 1d83 b7  58        A     STA  DESTINE  TO THE ORGINAL ADDRESS
A 1d85 b6  63        A     LDA  DEST+1
A 1d87 b7  59        A     STA  DESTINE+1
A 1d89 3c  5d        A     INC  TABPTR  UPDATE THE POINTER TO NEXT SYMBOL
                     *              PATTERN BYTE
A 1d8b 3c  5c        A     INC  LCDPTR  UPDATE THE DISPLAY RAM COLUMN POINTER
A 1d8d 3a  61        A     DEC  COUNT   DECREMENT THE COLUMN COUNT BY 1
A 1d8f 26  c8   1d59       BNE  N_COL
A 1d91 81                  RTS
                     ***************************************************************************
                     ***************************************************************************
                     **
                     **     Name:  FINDPAT -
                     **
                     **     SEARCH ALL SYMBOL PATTERN ROM MEMORY UNTIL THE RIGHT PATTERN IS FOUND
                     **     EACH PAGE OF SYMBOL PATTERN ROM MEMORY IS STORE IN THE P_TAB.
                     **     EACH RECORD OF THE P_TAB CONTAINS
                     **         ADDRESS OF THE SYMBOL PATTERN ROM TABLE
                     **         CORRESPONDING MMU COMMON BANK VALUE
                     **         CORRESPONDING MMU POSA1 VALUE
                     **         CORRESPONDING MMU POSA2 VALUE
                     **     THE LAST RECORD HAS ALL ZERO ENTRY
                     **
                     **     RETURN  : A DESTROY
                     **               X DESTROY
                     **               Z = 1 IF FOUND
                     **               Z = 0 IF NOT FOUND
                     **
                     ***************************************************************************
                     FINDPAT
A 1d92 3f  66        A     CLR  P_TPTR  INITIALIZE THE P_TAB POINTER
A 1d94 10  65        A     BSET 0,FOUND  INITIALIZE THE FLAG
                     NEXT_PTAB
A 1d96 be  66        A     LDX  P_TPTR  CHECK FOR NULL RECORD
A 1d98 d6  0de2      A     LDA  P_TAB,X
A 1d9b 26  14   1db1       BNE  LDSET
A 1d9d d6  0de3      A     LDA  P_TAB+1,X
A 1da0 26  0f   1db1       BNE  LDSET
A 1da2 d6  0de4      A     LDA  P_TAB+P_OFFCB,X
A 1da5 26  0a   1db1       BNE  LDSET
A 1da7 d6  0de5      A     LDA  P_TAB+P_OFFPA1,X
A 1daa 26  05   1db1       BNE  LDSET
A 1dac d6  0de6      A     LDA  P_TAB+P_OFFPA2,X
A 1daf 27  26   1dd7       BEQ  P_EXIT  EXIT IF NULL RECORD IS FOUND
A 1db1 d6  0de2      A LDSET   LDA  P_TAB,X  INITIALIZE THE BASE ADDRESS TO THE
```

```
A 1db4 b7  51     A       STA  SOURCE  PAGE COINTAINS THE FOUND SYMBOL
A 1db6 d6  0de3   A       LDA  P_TAB+1,X PATTERN
A 1db9 b7  52     A       STA  SOURCE+1
A 1dbb d6  0de4   A       LDA  P_TAB+P_OFFCB,X SET THE MMU REGISTERS
A 1dbe b7  22     A       STA  MMUCB
A 1dc0 d6  0de5   A       LDA  P_TAB+P_OFFPA1,X
A 1dc3 b7  20     A       STA  MMUPA1
A 1dc5 d6  0de6   A       LDA  P_TAB+P_OFFPA2,X
A 1dc8 b7  21     A       STA  MMUPA2

A 1dca cd  1dda   A CHKPTAB JSR  FOUNDTAB SEARCH THE PAGE OF SYMBOL CODES WHICH
                  *                 DEFINES IN P_TAB
A 1dcd 27  08  1dd7       BEQ  P_EXIT  FOUND IF Z = 1; EXIT IF Z = 0
A 1dcf b6  66     A       LDA  P_TPTR
A 1dd1 ab  05     A       ADD  #P_RECSIZE GO TO NEXT P_TAB RECORD
A 1dd3 b7  66     A       STA  P_TPTR
A 1dd5 20  bf  1d96       BRA  NEXT_PTAB

A 1dd7 3d  65     A P_EXIT  TST  FOUND   RETURN Z=1
A 1dd9 81                 RTS

                  ****************************************************************************
                  ****************************************************************************
                  **
                  **     Name:  FOUNDTAB -
                  **
                  **     LOCATE THE SYMBOL PATTERN ROM WITH THE SYMBOL CODE DEFINED IN
                  **     VARIABLE CHAR
                  **     ALL THE SYMBOL PATTERN ENTRIES ARE STORE IN A TABLE AND WITH THE
                  **     FOLLOWING FORMAT
                  **     FIRST TWO BYTE DEFINES THE SYMBOL PATTERN SIZE ( X bits x Y byte)
                  **     EACH ENTRY OF THIS TABLE CONTAINS
                  **          TWO BYTE CODE REPRESENT THE SYMBOL/CHARACTER CODE
                  **          PATTERN OFFSET FROM THE BEGINNING OF THE PAGE
                  **     THE LAST RECORD HAS ALL ZERO ENTRY
                  **
                  **
                  **
                  **     RETURN  : A DESTROY
                  **             X DESTROY
                  **             Z = 1 FOUND IF THE PATTERN SIZE AND CODE ARE MATCHED
                  **             Z = 0 OTHERWISE
                  **
                  ****************************************************************************
                  FOUNDTAB
A 1dda ae  00     A       LDX  #XSIZE  LOAD THE PATTERN WIDTH SIZE TO CHECK
A 1ddc bd  50     A       JSR  LDD
A 1dde b1  5f     A       CMP  CHARCOL
A 1de0 26  3b  1e1d       BNE  RECEXIT  EXIT IF NOT MATCH
A 1de2 ae  01     A       LDX  #YSIZE  LOAD THE PATTERB HEIGHT SIZE TO CHECK
A 1de4 bd  50     A       JSR  LDD
A 1de6 b1  5e     A       CMP  CHARROW
A 1de8 26  33  1e1d       BNE  RECEXIT  EXIT IF NOT MATCH

A 1dea ae  02     A       LDX  #2     IF MATCH, UPDATE THE SYMBOL PATTERN
A 1dec bf  5d     A       STX  TABPTR  POINTER AND START SEARCHING
```

```
A 1dee be 5d    A CHKTAB  LDX  TABPTR  LOAD THE 2-BYTE SYMBOL CODE FROM TABLE
A 1df0 bd 50    A         JSR  LDD
A 1df2 b7 6a    A         STA  TABCODE
A 1df4 5c               INCX
A 1df5 bd 50    A         JSR  LDD
A 1df7 b7 6b    A         STA  TABCODE+1

A 1df9 3d 6a    A         TST  TABCODE
A 1dfb 26 04  1e01        BNE  C_CHKTAB
A 1dfd 3d 6b    A         TST  TABCODE+1
A 1dff 27 1c  1e1d        BEQ  RECEXIT  EXIT IF HIT THE NULL ENTRY

              C_CHKTAB
A 1e01 b1 68    A         CMP  CHAR+1   SYMBOL CODE MATCH ?
A 1e03 26 10  1e15        BNE  N_REC
A 1e05 b6 6a    A         LDA  TABCODE
A 1e07 b1 67    A         CMP  CHAR
A 1e09 26 0a  1e15        BNE  N_REC    GO TO NEXT SYMBOL CODE IF NOT MATCH

A 1e0b 5c               INCX        SYMBOL CODE MATCH
A 1e0c bd 50    A         JSR  LDD
A 1e0e 97               TAX
A 1e0f b7 5d    A         STA  TABPTR   SET TABPTR TO THE PAGE OFFSET
A 1e11 3f 65    A         CLR  FOUND    CLEAR THE FLAG AND EXIT
A 1e13 20 08  1e1d        BRA  RECEXIT

A 1e15 b6 5d    A N_REC   LDA  TABPTR   TRY NEXT SYMBOL CODE
A 1e17 ab 03    A         ADD  #TABRECSIZE
A 1e19 b7 5d    A         STA  TABPTR
A 1e1b 20 d1  1dee        BRA  CHKTAB

A 1e1d 3d 65    A RECEXIT TST  FOUND
A 1e1f 81               RTS


              ******************************************************************************
              ******************************************************************************
              **
              **     Name:  SCROLL5 -
              **              SCROLLING THE 5th ROW OF DISPLAY RAM TO LEFT
              **              SIX COLUMN
              **
              **     Return: A and X will be destroyed
              **
              ******************************************************************************
              SCROLL5
A 1e20 a6 04    A         LDA  #4     INITIALIZE THE VARIABLES
A 1e22 b7 6f    A         STA  DISPROW
A 1e24 a6 06    A         LDA  #6
A 1e26 b7 5f    A         STA  CHARCOL
A 1e28 a6 01    A         LDA  #1
A 1e2a b7 5e    A         STA  CHARROW
A 1e2c ad 04  1e32        BSR  SCROLLEFT SCROLLING THE ROW OF DISPLAY RAM TO
              *                    LEFT BY A COLUMN
A 1e2e cd 1e6c  A         JSR  PAUSE    PAUSE FOR EACH SYMBOL PATTERN MOVE
```

```
A 1e31 81            RTS

                     ****************************************************************************
                     ****************************************************************************
                     **
                     **    Name:  SCROLLEFT -
                     **           SCROLLING THE SPECIFIED ROW (SINGLE ROW) BY THE NUMBER
                     **           OF COLUMN STATED IN VARIABLE CHARCOL
                     **
                     **    Return: A and X will be destroyed
                     **
                     ****************************************************************************
                     SCROLLEFT
A 1e32 a6  02     A        LDA  #2      CALCULATE THE LCD ADDRESS OF THE ROW
A 1e34 b7  51     A        STA  SOURCE
A 1e36 3f  52     A        CLR  SOURCE+1

A 1e38 be  6f     A        LDX  DISPROW
A 1e3a b6  52     A INCR   LDA  SOURCE+1 UPDATE THE BASE DISPLAY RAM ADDRESS
A 1e3c ab  80     A        ADD  #LCDCOL  ACCORDING TO THE VARIABLE DISPROW
A 1e3e b7  52     A        STA  SOURCE+1
A 1e40 b6  51     A        LDA  SOURCE
A 1e42 a9  00     A        ADC  #0
A 1e44 b7  51     A        STA  SOURCE
A 1e46 5a                  DECX
A 1e47 26  f1  1e3a        BNE  INCR

A 1e49 b6  52     A        LDA  SOURCE+1 DUPLICATE THE DISPLAY RAM ADDRESS
A 1e4b b7  59     A        STA  DESTINE+1 TO DESTINE
A 1e4d ab  01     A        ADD  #1      INCREMENT THE DISPLAY RAM ADDRESS
A 1e4f b7  56     A        STA  MSRC+1   1 AND STORE TO MSRC

A 1e51 b6  51     A        LDA  SOURCE
A 1e53 b7  58     A        STA  DESTINE
A 1e55 a9  00     A        ADC  #0
A 1e57 b7  55     A        STA  MSRC

A 1e59 bd  50     A PICKBYT JSR  LDD     MOVE THE COLUME 0th DATA TO A BUFFER
A 1e5b c7  0100   A        STA  BLOCK

A 1e5e 5f                  CLRX
A 1e5f bd  54     A MVVLCD  JSR  MVV     SHIFT ALL THE DATA PATTERN BY
A 1e61 5c                  INCX         A COLUMN UNTIL THE LAST COLUMN IS HIT
A 1e62 a3  7f     A        CPX  #$7F
A 1e64 26  f9  1e5f        BNE  MVVLCD

A 1e66 c6  0100   A        LDA  BLOCK   MOVE THE DATA FROM COLUME 0TH BEFORE
A 1e69 bd  57     A        JSR  STT     TO THE LAST COLUMN

A 1e6b 81                  RTS



                     ************************************************************************
                     **
                     **    Name:  PAUSE() -- PAUSE FOR ONE SECOND
```

```
                **
                ****************************************************************************
                PAUSE

A 1e6c 5f               CLRX
                PAUSE0
A 1e6d a6  d0     A       LDA  #$D0
A 1e6f 5c           PAUSE1  INCX
A 1e70 26  fd   1e6f      BNE  PAUSE1
A 1e72 4a                 DECA
A 1e73 26  fa   1e6f      BNE  PAUSE1
A 1e75 81                 RTS

                ****************************************************************************
                ****************************************************************************
                **
                **    Name:  DUMINT() -- DUMMY INTERRUPT SERVICE ROUTINE
                **
                ****************************************************************************
                DUMINT

A 1e76 80                 RTI




                ****************************************************************************
                ****************************************************************************
                **
                **    SYSTEM RESET VECTOR
                **
                ****************************************************************************
A 0c00                  ORG  $0C00
A 0c00    1e76   A SPIIRQ  FDB  DUMINT  SPI INTERRUPT VECTOR
A 0c02    1e76   A RTCIRQ  FDB  DUMINT  REAL TIME CLOCK INTERRUPT VECTOR
A 0c04    1e76   A SCIIRQ  FDB  DUMINT  SCI INTERRUPT VECTOR
A 0c06    1e76   A TIMIRQ  FDB  DUMINT  TIMER INTERRUPT VECTOR
A 0c08    1e76   A KEYIRQ  FDB  DUMINT  KEYBOARD INTERRUPT VECTOR
A 0c0a    1e76   A EIRQ    FDB  DUMINT  EXTERNAL INTERRUPT VECTOR
A 0c0c    1e76   A SWIVCT  FDB  DUMINT  SOFTWARE INTERRUPT VECTOR
A 0c0e    1c30   A         FDB  RESET   RESET INTERRUPT VECTOR
                       END
```

Total number of errors: 0
Total number of warnings: 0
Total number of lines: 821

Number of bytes in section ASCT: 1278

Number of bytes in program: 1278

M6805 mber of bytes in section ASCT: 1278

Number of bytes in program: 1278
M6805 Portable Cross Assembler 0.05 MS-DOS/PC-DOS Page 1
Mon Sep 09 10:43:21 1991
Command line:
C:\PASM\PASM05.EXE -EQSUX -L DROM1.LST -O DROM1.OBJ DROM1.ASM
Options list:
ON - b - Printing of macro definitions
ON - c - Printing of macro calls
OFF - d - Placing of symbolic debugging information in COFF
ON - e - Printing of macro expansions (changed)
ON - f - Printing of conditional directives
OFF - g - Printing of generated constants list
ON - q - Expanding and printing of structured syntax (changed)
ON - s - Printing of symbol table (changed)
ON - u - Printing of conditional unassembled source (changed)
ON - x - Printing of cross reference table (changed)
OFF - m - Suppress printing of error messages
ON - w - Printing of warning messages
OFF - v - Suppress printing of updated status
OFF - y - Enabling of sgs extensions
ON - o - Create object code
ON - - Formatting of source line listing
Create listing file - l - DROM1.LST
Change object file name - o - DROM1.OBJ

Xdefs:
NONE

Xrefs:
NONE

Input file(s): DROM1.ASM (189 lines)

Output file: DROM1.OBJ
Listing file: DROM1.LST

```
LINE  S PC  OPCO OPERANDS S LABEL   MNEMO OPERANDS COMMENT
*****************************************************************************
               *
               * FILE NAME:  DROM1.ASM              DATE: 8th Feb., 1991
               *
               * FILE DESCRIPTION: MC68HC05L10 MCU DEMONSTRATION SYMBOL PATTERN
               *            DATA FILE 1
               *
               * REVISION: 1.0
               *
               * AUTHOR: JAMSON CHEUNG
               *
               * REMARK: THIS FILE MUST BE IN CONJUCTION WITH THE PROGRAM DPROG.ASM
               *      THIS FILE CONTAINS TWO SYMBOL PATTERN TABLES. BOTH SYMBOL
               *      PATTERN ARE 8 x 6 DOTS SYMBOLS.
               *
               ***************************************************************************
               ***************************************************************************
               *
               *    SYMBOL PATTERN TABLE FORMAT
               *         FIRST TWO BYTE: PATTERN SIZE
               *                FIRST  BYTE : NUMBER OF DOTS IN X-AXIS
               *               SECOND BYTE : NUMBER OF BYTES IN Y-AXIS
               *                    ( 8 DOTS A BYTE )
               *
               *         3 BYTE RECORD FOLLOWING:
               *                1st TWO BYTE: SYMBOL CODE
               *               3rd    BYTE: PATTERN OFFSET FROM THE
               *                    BEGINNING OF THE TABLE
               *
               *         THE RECORD ENDING WITH A NULL RECORD
               *
               *         THE BYTE FOLLOWING THE NULL RECORD ARE THE SYMBOL PATTERN
               *         DATA LOCATION
               *
               **************************************************************************
               *
               *
                    OPT  NOP     COMPILER - LISTING OPTION
               *
               * SYMBOL PATTERN TABLE ADDRESS EQUATE
               *
      P 0000   8000   A OFFSET  EQU  $8000

      P 0000   8000   A TAB1LOC  EQU  OFFSET+$000
      P 0000   8100   A TAB2LOC  EQU  OFFSET+$100

               * NB :  PHYSCIAL ADDRESS = LOGICAL ADDRESS + POSAx * $1000
               *
               *         LOGICAL ADDRESS       PHYSICAL ADDRESS   CB  POSA1  POSA2
```

```
                 * TAB1LOC     $8000          $10000       C8  8   0
                 * TAB2LOC     $8100          $11000       C8  8   0
                 *
                 *
                 * SYMBOL PATTERN TABLE 1
                 *
A 8000                  ORG   TAB1LOC
A 8000    06        A TAB1   FCB  SYMEXCL-SYMSP8 NUMBER OF DOTS IN X-AXIS
A 8001    01        A        FCB  1     NUMBER OF BYTES IN Y-AXIS
                 *
                 * SYMBOL CODE AND SYMBOL PATTERN DATA OFFSET RECORD
                 *
A 8002    002053  A      FCB  $00,' ',SYMSP8-TAB1
A 8005    002159  A      FCB  $00,'!,SYMEXCL-TAB1
A 8008    00225f  A      FCB  $00,'",SYMDQUO-TAB1
A 800b    002365  A      FCB  $00,'#,SYMSQ-TAB1
A 800e    00246b  A      FCB  $00,'$,SYMDOL-TAB1
A 8011    002571  A      FCB  $00,'%,SYMPER-TAB1
A 8014    002677  A      FCB  $00,'&,SYMAMP-TAB1
A 8017    00277d  A      FCB  $00,$27,SYMSQUO-TAB1
A 801a    002883  A      FCB  $00,'(,SYMOPBK-TAB1
A 801d    002989  A      FCB  $00,'),SYMCLBK-TAB1
A 8020    002a8f  A      FCB  $00,'*,SYMAST-TAB1
A 8023    002b95  A      FCB  $00,'+,SYMPLUS-TAB1
A 8026    002c9b  A      FCB  $00,$2C,SYMCOMA-TAB1
A 8029    002da1  A      FCB  $00,'-,SYMMINU-TAB1
A 802c    002ea7  A      FCB  $00,'.,SYMDOT-TAB1
A 802f    0030ad  A      FCB  $00,'0,SYM0-TAB1
A 8032    0031b3  A      FCB  $00,'1,SYM1-TAB1
A 8035    0032b9  A      FCB  $00,'2,SYM2-TAB1
A 8038    0033bf  A      FCB  $00,'3,SYM3-TAB1
A 803b    0034c5  A      FCB  $00,'4,SYM4-TAB1
A 803e    0035cb  A      FCB  $00,'5,SYM5-TAB1
A 8041    0036d1  A      FCB  $00,'6,SYM6-TAB1
A 8044    0037d7  A      FCB  $00,'7,SYM7-TAB1
A 8047    0038dd  A      FCB  $00,'8,SYM8-TAB1
A 804a    0039e3  A      FCB  $00,'9,SYM9-TAB1
A 804d    003ae9  A      FCB  $00,':,SYMCOL-TAB1
A 8050    000000  A      FCB  $00,$00,$00 NULL RECORD OF TAB1
                 *
                 * SYMBOL PATTERN DATA
                 *
A 8053    00000000 A SYMSP8   FCB  $00,$00,$00,$00,$00,$00 SPACE
A 8059    0000004f A SYMEXCL  FCB  $00,$00,$00,$4F,$00,$00 !
A 805f    00000700 A SYMDQUO  FCB  $00,$00,$07,$00,$07,$00 "
A 8065    00147f14 A SYMSQ    FCB  $00,$14,$7F,$14,$7F,$14 #
A 806b    00242a7f A SYMDOL   FCB  $00,$24,$2A,$7F,$2A,$12 $
A 8071    00231308 A SYMPER   FCB  $00,$23,$13,$08,$64,$62 %
A 8077    00364956 A SYMAMP   FCB  $00,$36,$49,$56,$20,$58 &
A 807d    00000503 A SYMSQUO  FCB  $00,$00,$05,$03,$00,$00 '
A 8083    00001c22 A SYMOPBK  FCB  $00,$00,$1C,$22,$41,$00 (
A 8089    00004122 A SYMCLBK  FCB  $00,$00,$41,$22,$1C,$00 )
```

```
A 808f   0022147f A SYMAST   FCB  $00,$22,$14,$7F,$14,$22 *
A 8095   0008083e A SYMPLUS  FCB  $00,$08,$08,$3E,$08,$08 +
A 809b   00000050 A SYMCOMA  FCB  $00,$00,$00,$50,$30,$00 ,
A 80a1   00080808 A SYMMINU  FCB  $00,$08,$08,$08,$08,$08 -
A 80a7   00000060 A SYMDOT   FCB  $00,$00,$00,$60,$60,$00 .
A 80ad   003e5149 A SYM0     FCB  $00,$3E,$51,$49,$45,$3E 0
A 80b3   0000427f A SYM1     FCB  $00,$00,$42,$7F,$40,$00 1
A 80b9   00426151 A SYM2     FCB  $00,$42,$61,$51,$49,$46 2
A 80bf   00214145 A SYM3     FCB  $00,$21,$41,$45,$4B,$31 3
A 80c5   00181412 A SYM4     FCB  $00,$18,$14,$12,$7F,$10 4
A 80cb   00274545 A SYM5     FCB  $00,$27,$45,$45,$45,$39 5
A 80d1   003c4a49 A SYM6     FCB  $00,$3C,$4A,$49,$49,$30 6
A 80d7   0001f109 A SYM7     FCB  $00,$01,$F1,$09,$05,$03 7
A 80dd   00364949 A SYM8     FCB  $00,$36,$49,$49,$49,$36 8
A 80e3   00064949 A SYM9     FCB  $00,$06,$49,$49,$29,$1E 9
A 80e9   00000024 A SYMCOL   FCB  $00,$00,$00,$24,$00,$00 :


                   *
                   * SYMBOL PATTERN 2
                   *
A 8100                      ORG  TAB2LOC
A 8100   06      A TAB2   FCB  SYMB-SYMA NUMBER OF DOTS IN X-AXIS
A 8101   01      A        FCB  1     NUMBER OF BYTES IN Y-AXIS
                   *
                   * SYMBOL CODE AND SYMBOL PATTERN DATA OFFSET RECORD
                   *
A 8102   004153  A        FCB  $00,'A,SYMA-TAB2
A 8105   004259  A        FCB  $00,'B,SYMB-TAB2
A 8108   00435f  A        FCB  $00,'C,SYMC-TAB2
A 810b   004465  A        FCB  $00,'D,SYMD-TAB2
A 810e   00456b  A        FCB  $00,'E,SYME-TAB2
A 8111   004671  A        FCB  $00,'F,SYMF-TAB2
A 8114   004777  A        FCB  $00,'G,SYMG-TAB2
A 8117   00487d  A        FCB  $00,'H,SYMH-TAB2
A 811a   004983  A        FCB  $00,'I,SYMI-TAB2
A 811d   004a89  A        FCB  $00,'J,SYMJ-TAB2
A 8120   004b8f  A        FCB  $00,'K,SYMK-TAB2
A 8123   004c95  A        FCB  $00,'L,SYML-TAB2
A 8126   004d9b  A        FCB  $00,'M,SYMM-TAB2
A 8129   004ea1  A        FCB  $00,'N,SYMN-TAB2
A 812c   004fa7  A        FCB  $00,'O,SYMO-TAB2
A 812f   0050ad  A        FCB  $00,'P,SYMP-TAB2
A 8132   0051b3  A        FCB  $00,'Q,SYMQ-TAB2
A 8135   0052b9  A        FCB  $00,'R,SYMR-TAB2
A 8138   0053bf  A        FCB  $00,'S,SYMS-TAB2
A 813b   0054c5  A        FCB  $00,'T,SYMT-TAB2
A 813e   0055cb  A        FCB  $00,'U,SYMU-TAB2
A 8141   0056d1  A        FCB  $00,'V,SYMV-TAB2
A 8144   0057d7  A        FCB  $00,'W,SYMW-TAB2
A 8147   0058dd  A        FCB  $00,'X,SYMX-TAB2
A 814a   0059e3  A        FCB  $00,'Y,SYMY-TAB2
A 814d   005ae9  A        FCB  $00,'Z,SYMZ-TAB2
A 8150   000000  A        FCB  $00,$00,$00 NULL RECORD OF TAB2
```

```
                         *
                         * SYMBOL PATTERN DATA
                         *
A 8153   007c1211 A SYMA   FCB  $00,$7C,$12,$11,$12,$7C A
A 8159   00417f49 A SYMB   FCB  $00,$41,$7F,$49,$49,$36 B
A 815f   003e4141 A SYMC   FCB  $00,$3E,$41,$41,$41,$22 C
A 8165   007f4141 A SYMD   FCB  $00,$7F,$41,$41,$41,$3E D
A 816b   007f4949 A SYME   FCB  $00,$7F,$49,$49,$49,$41 E
A 8171   00ff0909 A SYMF   FCB  $00,$FF,$09,$09,$09,$01 F
A 8177   003e4149 A SYMG   FCB  $00,$3E,$41,$49,$49,$3A G
A 817d   007f0808 A SYMH   FCB  $00,$7F,$08,$08,$08,$7F H
A 8183   0000417f A SYMI   FCB  $00,$00,$41,$7F,$41,$00 I
A 8189   00204041 A SYMJ   FCB  $00,$20,$40,$41,$3F,$01 J
A 818f   007f0814 A SYMK   FCB  $00,$7F,$08,$14,$22,$41 K
A 8195   007f4040 A SYML   FCB  $00,$7F,$40,$40,$40,$40 L
A 819b   007f020c A SYMM   FCB  $00,$7F,$02,$0C,$02,$7F M
A 81a1   007f0408 A SYMN   FCB  $00,$7F,$04,$08,$10,$7F N
A 81a7   003e4141 A SYMO   FCB  $00,$3E,$41,$41,$41,$3E O
A 81ad   007f0909 A SYMP   FCB  $00,$7F,$09,$09,$09,$06 P
A 81b3   003e4151 A SYMQ   FCB  $00,$3E,$41,$51,$21,$5E Q
A 81b9   007f0919 A SYMR   FCB  $00,$7F,$09,$19,$29,$46 R
A 81bf   00464949 A SYMS   FCB  $00,$46,$49,$49,$49,$31 S
A 81c5   0001017f A SYMT   FCB  $00,$01,$01,$7F,$01,$01 T
A 81cb   003f4040 A SYMU   FCB  $00,$3F,$40,$40,$40,$3F U
A 81d1   001f2040 A SYMV   FCB  $00,$1F,$20,$40,$20,$1F V
A 81d7   003f4038 A SYMW   FCB  $00,$3F,$40,$38,$40,$3F W
A 81dd   00631408 A SYMX   FCB  $00,$63,$14,$08,$14,$63 X
A 81e3   00070870 A SYMY   FCB  $00,$07,$08,$70,$08,$07 Y
A 81e9   00615149 A SYMZ   FCB  $00,$61,$51,$49,$45,$43 Z

                              END

```

Total number of errors: 0
Total number of warnings: 0
Total number of lines: 189

Number of bytes in section ASCT: 478

Number of bytes in program: 478

M6805 Portable Cross Assembler 0.05 MS-DOS/PC-DOS Page 1
Mon Sep 09 10:43:45 1991
Command line:
C:\PASM\PASM05.EXE -EQSUX -L DROM2.LST -O DROM2.OBJ DROM2.ASM
Options list:
ON - b - Printing of macro definitions
ON -- c - Printing of macro calls
OFF - d - Placing of symbolic debugging information in COFF
ON - e - Printing of macro expansions (changed)
ON - f - Printing of conditional directives
OFF - g - Printing of generated constants list
ON - q - Expanding and printing of structured syntax (changed)
ON - s - Printing of symbol table (changed)
ON - u - Printing of conditional unassembled source (changed)
ON - x - Printing of cross reference table (changed)
OFF - m - Suppress printing of error messages
ON - w - Printing of warning messages
OFF - v - Suppress printing of updated status
OFF - y - Enabling of sgs extensions
ON - o - Create object code
ON - - Formatting of source line listing
Create listing file - l - DROM2.LST
Change object file name - o - DROM2.OBJ

Xdefs:
NONE

Xrefs:
NONE

Input file(s): DROM2.ASM (157 lines)

Output file: DROM2.OBJ
Listing file: DROM2.LST

Options - MD,MC,NOG,U,W,,MEX,CL,FMT,O

```
LINE  S PC   OPCO OPERANDS S LABEL  MNEMO OPERANDS COMMENT
                  ***********************************************************************
                  *
                  * FILE NAME:  DROM2.ASM              DATE: 8th Feb., 1991
                  *
                  * FILE DESCRIPTION: MC68HC05L10 MCU DEMONSTRATION SYMBOL PATTERN
                  *            DATA FILE 2
                  *
                  * REVISION: 1.0
                  *
                  * AUTHOR: JAMSON CHEUNG
                  *
                  * REMARK: THIS FILE MUST BE IN CONJUCTION WITH THE PROGRAM DPROG.ASM
                  *      THIS FILE CONTAINS TWO SYMBOL PATTERN TABLES. BOTH SYMBOL
                  *      PATTERN ARE 16x16 DOTS SYMBOLS.
                  *
                  ***********************************************************************
                  ***********************************************************************
                  *
                  *     SYMBOL PATTERN TABLE FORMAT
                  *          FIRST TWO BYTE: PATTERN SIZE
                  *                   FIRST  BYTE : NUMBER OF DOTS IN X-AXIS
                  *               SECOND BYTE : NUMBER OF BYTES IN Y-AXIS
                  *                       ( 8 DOTS A BYTE )
                  *
                  *          3 BYTE RECORD FOLLOWING:
                  *                   1st TWO BYTE: SYMBOL CODE
                  *               3rd    BYTE: PATTERN OFFSET FROM THE
                  *                       BEGINNING OF THE TABLE
                  *
                  *          THE RECORD ENDING WITH A NULL RECORD
                  *
                  *          THE BYTE FOLLOWING THE NULL RECORD ARE THE SYMBOL PATTERN
                  *          DATA LOCATION
                  *
                  ***********************************************************************
                  *
                  *
                       OPT   NOP     COMPILER - LISTING OPTION
                  *
                  *
                  * SYMBOL PATTERN TABLE ADDRESS EQUATE
                  *
      P 0000  c000   A OFFSET   EQU   $C000

      P 0000  c000   A TAB3LOC  EQU   OFFSET
      P 0000  c100   A TAB4LOC  EQU   OFFSET+$100

                  *
                  * NB :   PHYSCIAL ADDRESS = LOGICAL ADDRESS + POSAx * $1000
```

```
            *
            *         LOGICAL ADDRESS     PHYSICAL ADDRESS   CB POSA1 POSA2
            * TAB3LOC     $C000           $14000          C8  0     8
            * TAB4LOC     $C100           $14100          C8  0     8
            *

            *
            * SYMBOL PATTERN TABLE 3
            *
A c000               ORG  TAB3LOC
A c000  10      A TAB3   FCB  (YEN-FU)/2 NUMBER OF DOTS IN X-AXIS
A c001  02      A        FCB  2     NUMBER OF BYTE IN Y-AXIS
A c002  c577    A        FDB  $C577
A c004  17      A        FCB  FU-TAB3
A c005  aaef    A        FDB  $AAEF
A c007  37      A        FCB  YEN-TAB3
A c008  bb59    A        FDB  $BB59
A c00a  57      A        FCB  EI-TAB3
A c00b  c17b    A        FDB  $C17B
A c00d  77      A        FCB  LEM-TAB3
A c00e  b855    A        FDB  $B855
A c010  97      A        FCB  MAN-TAB3
A c011  a44f    A        FDB  $A44F
A c013  b7      A        FCB  LEK-TAB3
A c014  0000    A        FDB  $00    NULL RECORD OF TAB3
A c016  00      A        FCB  $00
            *
            * SYMBOL CODE AND SYMBOL PATTERN DATA OFFSET RECORD
            *
A c017  00745e74 A FU    FCB  $00,$74,$5E,$74,$80,$74,$5E,$74
A c01f  0010080c A       FCB  $00,$10,$08,$0C,$F8,$08,$18,$00
A c027  0004027f A       FCB  $00,$04,$02,$7F,$55,$7F,$55,$00
A c02f  40300804 A       FCB  $40,$30,$08,$04,$03,$0E,$78,$00

A c037  00009080 A YEN   FCB  $00,$00,$90,$80,$00,$F8,$04,$02
A c03f  0000fc04 A       FCB  $00,$00,$FC,$04,$04,$FC,$00,$00
A c047  00003e31 A       FCB  $00,$00,$3E,$31,$60,$6F,$68,$64
A c04f  62405f40 A       FCB  $62,$40,$5F,$40,$41,$41,$00,$00

A c057  00102404 A EI    FCB  $00,$10,$24,$04,$86,$4C,$E4,$14
A c05f  0000c40c A       FCB  $00,$00,$C4,$0C,$06,$04,$00,$00
A c067  00412110 A       FCB  $00,$41,$21,$10,$00,$00,$7F,$20
A c06f  25292129 A       FCB  $25,$29,$21,$29,$25,$21,$20,$00

A c077  00fc243c A LEM   FCB  $00,$FC,$24,$3C,$24,$E4,$00,$20
A c07f  100cea28 A       FCB  $10,$0C,$EA,$28,$E8,$08,$00,$00
A c087  007f243c A       FCB  $00,$7F,$24,$3C,$24,$27,$20,$00
A c08f  3c243d01 A       FCB  $3C,$24,$3D,$01,$3D,$24,$3C,$00

A c097  000004e4 A MAN   FCB  $00,$00,$04,$E4,$A6,$AC,$A4,$E0
A c09f  a0a0a4ec A       FCB  $A0,$A0,$A4,$EC,$06,$04,$04,$00
A c0a7  0078080b A       FCB  $00,$78,$08,$0B,$0A,$6A,$5A,$4F
A c0af  4a6a0a0b A       FCB  $4A,$6A,$0A,$0B,$08,$48,$78,$00
```

```
A c0b7   00000020 A LEK    FCB  $00,$00,$00,$20,$20,$20,$A0,$70
A c0bf   2c202020 A        FCB  $2C,$20,$20,$20,$E0,$00,$00,$00
A c0c7   00002010 A        FCB  $00,$00,$20,$10,$08,$04,$03,$20
A c0cf   20100c03 A        FCB  $20,$10,$0C,$03,$00,$00,$00,$00


              *
              * SYMBOL PATTERN 4
              *
A c100                   ORG  TAB4LOC
A c100   10     A TAB4   FCB  (KON-GI)/2 NUMBER OF DOTS IN X-AXIS
A c101   02     A        FCB  2      NUMBER OF BYTES IN Y-AXIS
A c102   aabf   A        FDB  $AABF
A c104   14     A        FCB  GI-TAB4
A c105   b4e4   A        FDB  $B4E4
A c107   34     A        FCB  KON-TAB4
A c108   a4a4   A        FDB  $A4A4
A c10a   54     A        FCB  CHUN-TAB4
A c10b   a4df   A        FDB  $A4DF
A c10d   74     A        FCB  SIN-TAB4
A c10e   a140   A SYMSP16 FDB $A140
A c110   94     A        FCB  WHITE-TAB4
A c111   0000   A        FDB  $00    NULL RECORD OF TAB2
A c113   00     A        FCB  $00
              *
              * SYMBOL PATTERN DATA
              *
A c114   00008848 A GI     FCB  $00,$00,$88,$48,$28,$18,$08,$08
A c11c   8040a030 A        FCB  $80,$40,$A0,$30,$28,$A0,$60,$00
A c124   0001001f A        FCB  $00,$01,$00,$1F,$11,$11,$1F,$40
A c12c   20100805 A        FCB  $20,$10,$08,$05,$02,$05,$00,$00

A c134   00224488 A KON    FCB  $00,$22,$44,$88,$00,$20,$A0,$64
A c13c   3e247ea4 A        FCB  $3E,$24,$7E,$A4,$24,$20,$20,$00
A c144   00201008 A        FCB  $00,$20,$10,$08,$04,$01,$00,$7F
A c14c   41414547 A        FCB  $41,$41,$45,$47,$71,$02,$00,$00

A c154   0000e010 A CHUN   FCB  $00,$00,$E0,$10,$10,$10,$10,$FE
A c15c   10101010 A        FCB  $10,$10,$10,$10,$E0,$00,$00,$00
A c164   00000302 A        FCB  $00,$00,$03,$02,$02,$02,$02,$7F
A c16c   02020202 A        FCB  $02,$02,$02,$02,$03,$00,$00,$00

A c174   00008040 A SIN    FCB  $00,$00,$80,$40,$A0,$00,$00,$60
A c17c   30000000 A        FCB  $30,$00,$00,$00,$00,$80,$40,$00
A c184   00010000 A        FCB  $00,$01,$00,$00,$01,$02,$06,$0C
A c18c   08080804 A        FCB  $08,$08,$08,$04,$00,$01,$00,$00

A c194   00000000 A WHITE  FCB  $00,$00,$00,$00,$00,$00,$00,$00
A c19c   00000000 A        FCB  $00,$00,$00,$00,$00,$00,$00,$00
A c1a4   00000000 A        FCB  $00,$00,$00,$00,$00,$00,$00,$00
A c1ac   00000000 A        FCB  $00,$00,$00,$00,$00,$00,$00,$00

END

```

Total number of errors: 0
Total number of warnings: 0
Total number of lines: 157

Number of bytes in section ASCT: 395

Number of bytes in program: 395

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN-HK-15

USING DRAGONKAT II LCD CHIP-SET IN HAND-WRITING APPLICATIONS

Prepared by Harvey Wong
Motorola Semiconductors Hong Kong Ltd.

INTRODUCTION

DragonKat II is a chip-set solution offered by Motorola for high density graphic LCD systems (with 146 mux and more than 160 segments). It includes a microcontroller (MCU) MC68HC05L11, a cascadable LCD backplane (or common) driver MC141512 and a cascadable LCD segment (or column) driver MC141514. When linked up to a touch sensitive panel, the system can accept and display handwriting inputs. The purpose of this document is to illustrate a pen-based system using this chip set. First the display output unit will be described. Then follows the hand-writing input system. Finally, they are integrated and a demonstration software for doing handwriting/erasing will be presented.

USING DRAGONKAT II LCD CHIP-SET TO BUILD A 164 x 320 LCD SYSTEM

MC68HC05L11 is a fully static single chip CMOS microcomputer. It has 448 bytes of RAM of which 64 bytes are for stack, 3584 bytes of ROM, one crystal oscillator generating clock for a real time clock and one PLL frequency synthesizer for MCU's system clock, 38 bidirectional I/O lines, 2 serial communication interfaces (an SCI[1] and an SPI[2]), one 16-bit timer, a memory management unit to page in as much as 8 Mega-bytes logical address into a 64k physical address and a special LCD Control Unit. This MCU has all the features that make it an ideal part for electronic organizer, personal data bank, dictionary, game and other hand-held terminal or measurement equipment applications.

The segment driver MC141514, as in Figure 1, is designed to generate segment-driving waveforms[3] for passive LCD panels. (It is customary to name the vertical lines of a LCD panel as segments and its horizontal lines as backplanes. Pixels are positioned at where these lines intercept.) MC141514 has 160 outputs and is cascadable for higher segment count. Inside there is a Static RAM matrix of 146 rows by 160 bits for image storage.

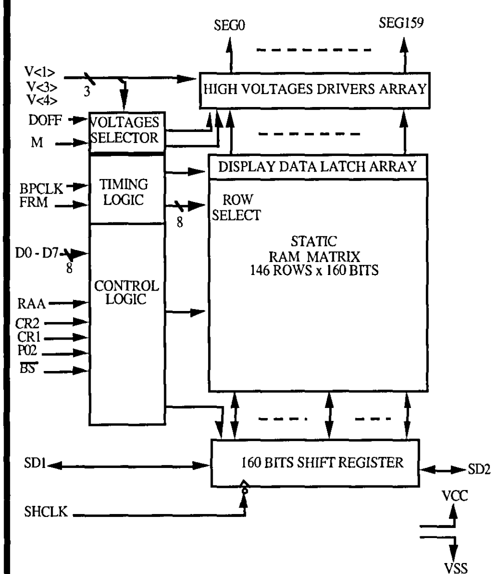

Figure 1. The Segment Driver MC141514

1. Serial Communications Interface (SCI) supports full-duplex asynchronous communication with standard NRZ format in number of standard baud rates.
2. Serial Peripherals Interface (SPI)is a Motorola's proprietary standard for synchronous communication.
3. See MC141514 Product Specification.

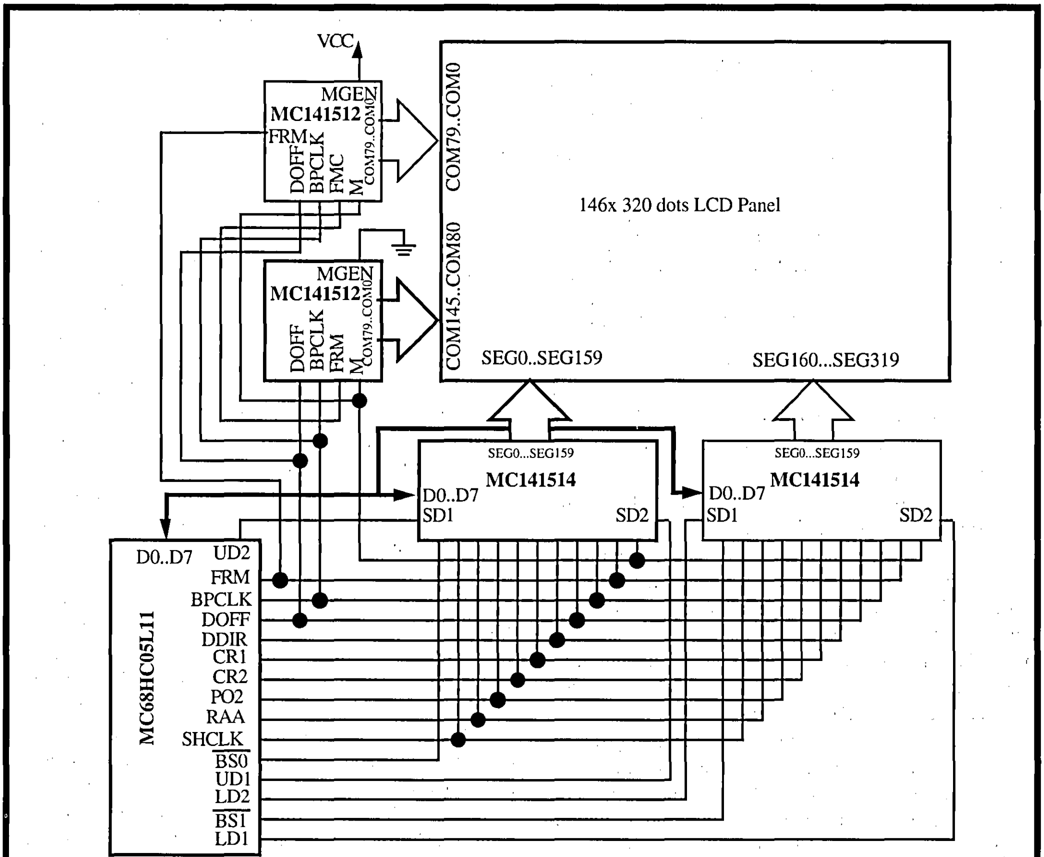

Figure 2. A 146x320 LCD SYSTEM

Any of these rows can be selected and its contents fetched for segment output display or transferred to a 160-bit wide bidirectional shift register in a parallel fashion. Conversely, the content of the 160-bit bidirectional shift register can be stored in any of the 146 rows. The bidirectional shift register serves as the gateway for transporting video data between the MCU and segment drivers. Since the content is stored in the segment driver(s), the LCD screen refresh is handled automatically by an internal wrap-around counter that sequentially scans each row for segment output in a repetitive manner. The MCU is required to access the segment driver(s) only if the screen content is to be altered.

The backplane driver MC141512 is designed to supply the backplane waveforms to a passive LCD panel. The mechanism is driven by a marching "1" along 80-bit shift register. At the start of a refresh cycle, the Frame signal (FRM) feeds a logic one momentarily into the first bit of the shift register. The lone "1" is shifted to the next higher order bit successively on each BPCLK pulse. Effectively each row of pixels on the LCD screen is sequentially selected during a refresh cycle.

Figure 2 shows an LCD system built with the DragonKat II chip-set. It consists of two backplane drivers, two segment drivers, one MCU and an LCD panel. The MCU communicates with the drivers through a special circuit block, the LCD Control Unit, as shown on Figure 3. This unit is designed to facilitate graphic manipulations such as smooth scrolling in "x" or "y" directions, variable pitch editing and window partitioning. However, it must work with the two drivers (the backplane driver MC141512 and the segment driver MC141514) in order to perform graphic functions. It can be divided into three functional blocks: a serial data interface, a parallel control interface and a timing generator as shown in Figure 3. The timing generator provides the necessary signals for system synchronization. The unit, most of the time, communicates with its drivers through the serial and parallel interfaces. Which are designed for different purposes: the serial interface is for video data transfer while the parallel one is for issuing commands. It is vital to have a serial transfer mechanism because of

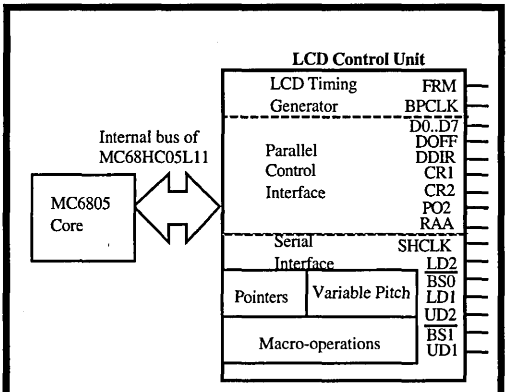

Figure 3. The LCD Control Unit

its capability to shift data bit by bit. Also, it can shift to the left or right so as to allow smooth horizontal scroll in either directions. Figure 2 also shows the physical connections between the serial interface and the bidirectional shift registers of the segment drivers. As mentioned before the bidirectional shift register is a gateway for transporting video data, it can also serve as a parallel dump for a row of video content. Its length is same as the width of the video RAM. In our case here, the segment driver MC141516 has 160 bits per row of video RAM, therefore, the bidirectional shift register is 160 bits long. It can be easily observed that the serial connections are closed to form a loop. In Figure 2, there are two of these loops. Usually, only one loop is enough to support a long single LCD panel because more than one segment drivers can be cascaded to form a longer loop. However, the system shown uses two loops to support a single panel (one segment driver per loop) to shorten the loop path so as to increase the accessing speed. In the normal case, a separate loop drives each half of a split panel.

Other than serial data transfer operations, the serial port has a few more supporting circuits built-in i.e. the pointers, the variable pitch access logic and a macro-operations block. The macro-operations block can do four macro-operations while the pointers and variable pitch access block set up boundary conditions and access pitch respectively for these macro-operations. Macro-operations are either on a sequential (SEQ) or on a one-shot (OSH) access basis. Two sequential access options allow the MCU to either read from or write into the bidirectional shift register(s) of the segment driver(s) within a specified window boundary and at various pitch widths sequentially. For instance, a sequential-write at a 10-bit pitch width allows the MCU to write into the serial stream a 10-bit word at a time which is then shifted serially into the segment drivers. The transfer is automatically carried out as soon as a 10-bit word has been written into a register of the LCD Control Unit. After the transfer, the interface will stop for the next 10-bit word from the processor. This transfer-and-wait process is repeated within a window which is specified by the left and right pointers of the LCD Control Unit. These two pointers can be flexibly adjusted to fit in window of any size. The width can be as wide as the whole screen or just a pixel. For data outside this window, the interface will carry out a non-stop shift until the specified end-point. With this interface a row of display data can then be composed in the bidirectional shift register loop before the MCU orders the segment drivers to copy this row of data into their internal Static RAM in a parallel fashion. The MCU does it by issuing a command, encrypted with a row address, to the segment drivers through the parallel interface. It is a typical cycle that a row of display data is loaded into the bidirectional shift register and written back to the same row after it has been edited by the processor. This cycle can be viewed as accessing some part of the screen in rectangular coordinates - the row address as the Y-coordinate and the location pointed by one of the two pointers as the X-coordinate, particularly if the macro-operation "One-Shot Replace" is used. "One-Shot Replace" will replace a number of dots as specified by the variable pitch register after the first pointer with the new content prepared by the MCU. The transfer is one-shot and the loop will stop only after it has reverted back to its original position. Such an LCD system allows for a natural way of manipulating graphics on the LCD panel via a rectangular coordinating system. Unlike some conventional LCD systems which coordinations are somehow tied with the 8-bit RAM structure, it eases much effort when only a bit of content needs to be changed, which is most often the case in handwriting applications.

The Handwriting Input Mechanism

An input device for handwriting is a touch sensitive panel. It is transparent and can be laid on top of the LCD panel. With the appropriate setup, the points of touch can be located by an A/D converter (MC1415150). Detected points expressed in rectangular coordinates are brought to the processor for scaling and transformation and put on the LCD. If the sampling is fast enough, one would see a continuous trace on the LCD screen recording the movement of the touch.

This panel is a passive device and it needs both a hardware and a software driver for handwriting purpose. Figure 4 shows the hardware driver of the touch sensitive panel system. The panel shown is coupled to a transistor ladder which is responsible for configuring the circuit for different sampling set-ups. The ladder circuit is controlled by I/O port C. After the establishment of the right circuit configuration, the MCU through the Serial Peripheral Interface commands the A/D converter to translate an analog voltage into a digital numeric.

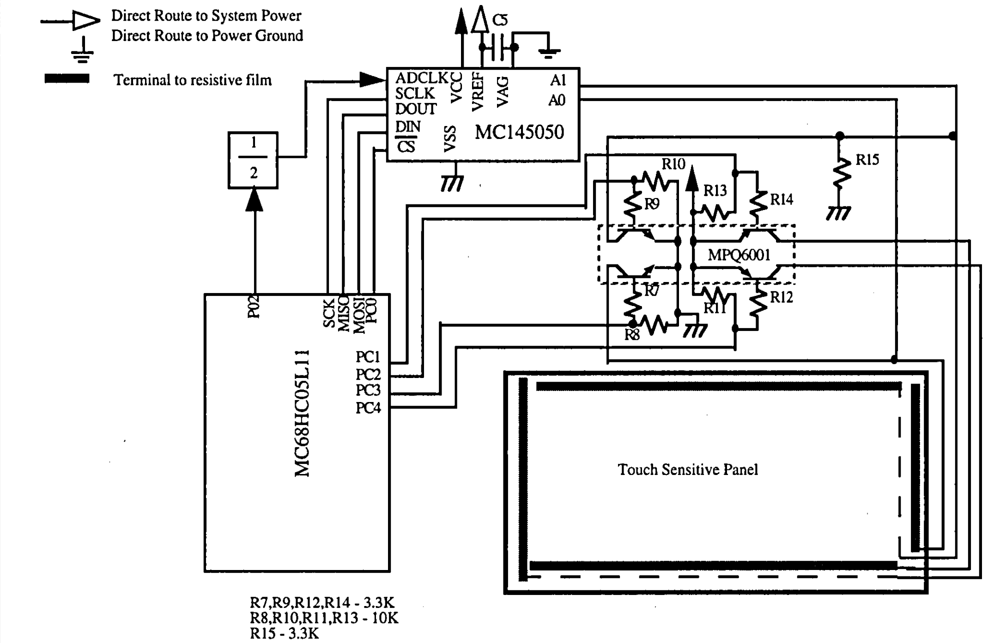

Figure 4. The Hardware Support Of The Touch Sensitive Panel

The touch sensitive panel has two layers of transparent, evenly doped resistive film sandwiching a thin spacer and mounted on a supporting glass. There are four terminals located along the four edges of the panel. A pair of terminals connects to opposite sides the upper film (e.g. in the horizontal direction) while another pair connects similarly to the lower film (e.g. in the vertical direction). Separated by a thin spacer, these films are electrically isolated from each other in the idle state. However, if a pressure is applied with a sharp pen, the stylus will push the upper film down to make contact with the lower film. Also, if a reference voltage is applied across the terminals of the upper film while the other pair remains in high impedance, the voltage should drop linearly across the upper film in vertical direction. The point of contact of the two films transforms the terminals of the lower film to become the wiper of a potentiometer. Because the resistance across the layer is uniform, the voltage at the contact point should be proportional to its distance from the ground-referenced edge. As a result, the voltage at either terminal of the lower film carries information about the Y coordinate of the stylus. The same procedure can be applied to measure the X coordinate of the stylus by role-swapping the two pairs of terminals. The mechanism is simple and its accuracy depends on the linearity of the resistive film and the resolution of the A/D converter. However, there is another problem. Like most mechanical devices (e.g. a keyboard), the touch sensitive panel suffers from contact bounce. To verify good contact closure, the system has to switch one pair of terminals to the reference voltage source and then connect one of the terminals of the other pair to a high value pull-down resistor (but not too high in order to overcome the capacitive effect across the films). A good contact is ensured if the voltage across this resistor is greater than a threshold. In Figure 5, the software checks for a good contact before sampling the X and Y coordinates. However, the process is not ended until a reconfirmation for a good contact is done after polling in X and Y because of the fact that a good contact might be lost during sampling for X and Y. Valid samples will be further processed and then sent to the LCD system for output.

A PROTOTYPE FOR HAND-WRITING APPLICATION

It is relatively straight-forward to implement handwriting input in a DragonKat II- based system. Figure 5 shows the circuit diagram of such a system. It is just the combination of the Figure 1 and 3 with the touch sensi-

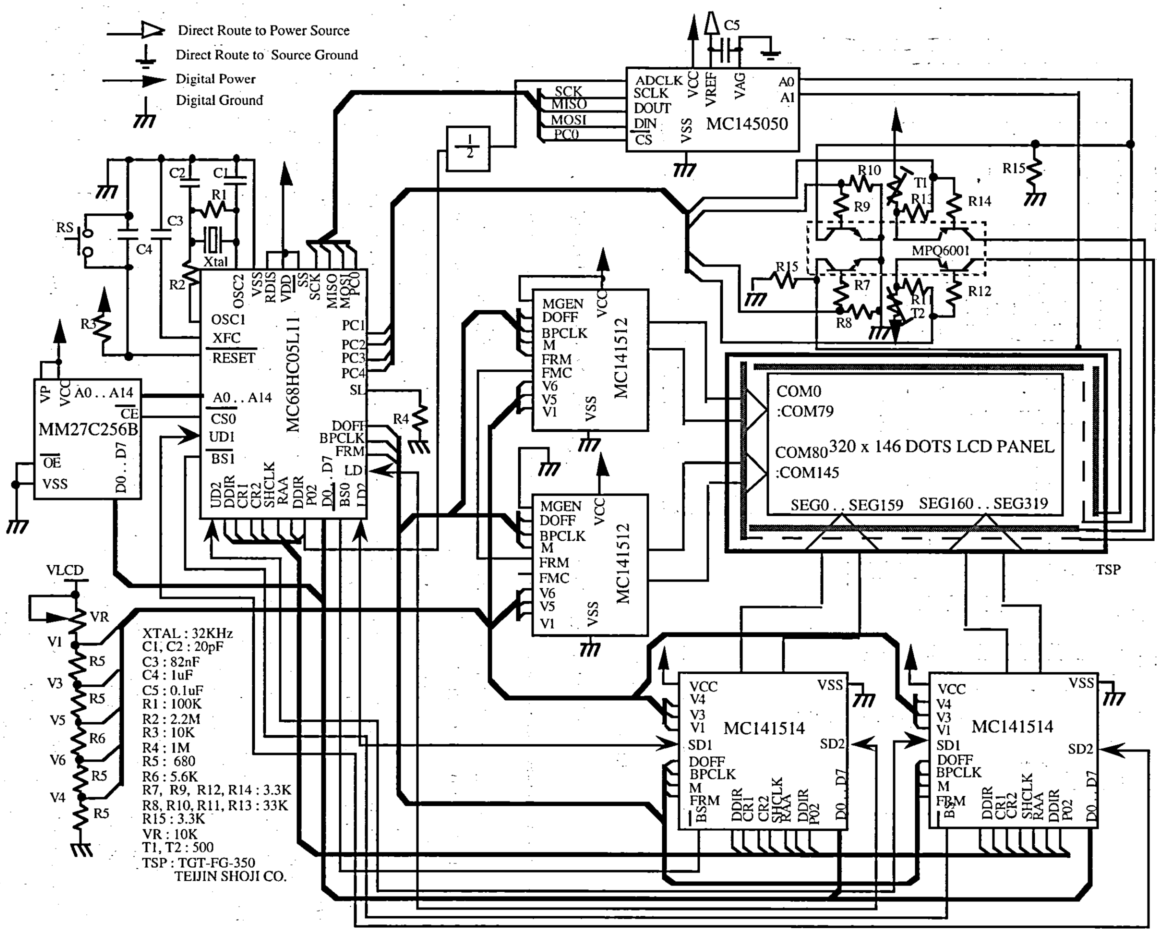

Figure 5. Schematic Of An LCD Display System With Handwriting Input

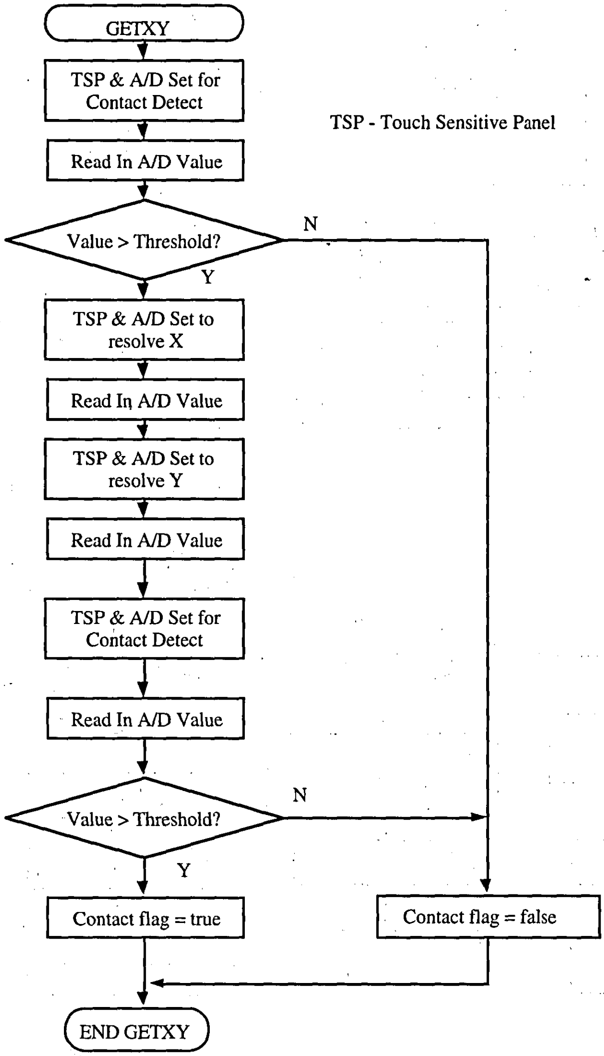

Figure 6. The Software Driver For The Touch Sensitive Panel System

tive tablet overlaid on the top of the LCD panel. The MCU samples the touch sensitive tablet for handwriting input. If a valid contact is found, after a sample conversion, the dot can be transferred to the LCD system for display. Furthermore, the user can intercept the software flow for different interpretations on the pen-based inputs in applications such as straight-lines drawing, polygon building and even pattern hatching. The large effective area of the tablet allows icons to be displayed for pen selections. A touch-and-execute procedure makes the system very user-friendly and obviates the need for an elaborate keyboard in a pocket equipment.

SOFTWARE OF THE PROTOTYPE

Figure 7 shows the flow chart of a sample program which emulates a blank paper and an eraser. The system routine DRAWRUB starts up to do hand-writing with its Eraser Flag disabled. It will first clean the screen and pops up an Eraser Icon at the upper right-hand corner of the screen. It then enables a 16-bit timer interrupt before it goes to WAIT[4]. The Timer will then periodically call up the processor to scan for user inputs. The main part

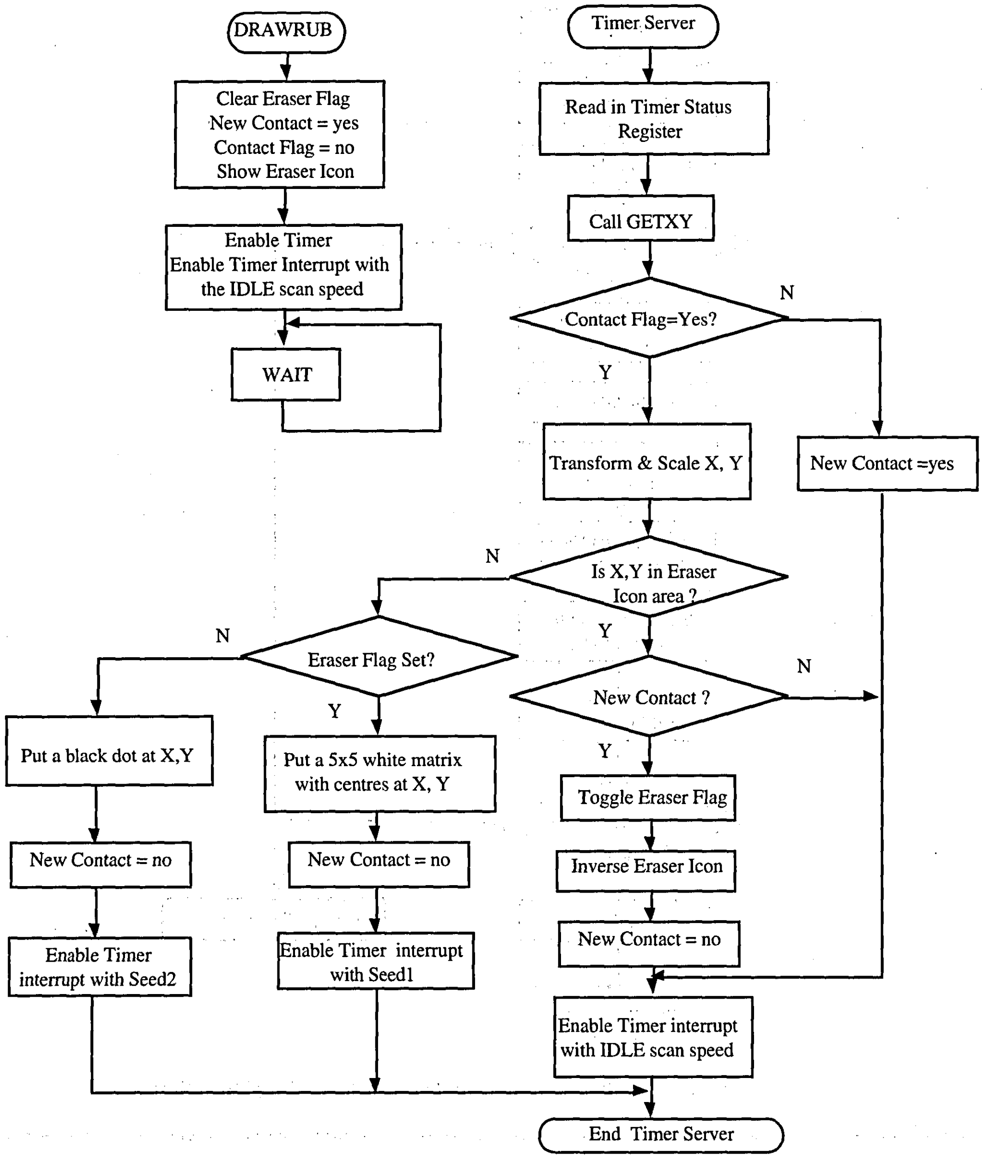

Figure 7. The Software For Electronic Handwriting And Erasing

of the scan-and-print job is resident in the Timer Server routine. The Timer Server is the routine to where the processor will branch as soon as it is waken up by a timer interrupt. It will first access the timer status register. The Timer Output Compare flag will be cleared as it writes a next interrupt count into the Output Compare Register. Otherwise the same interrupt request may keep on interrupting the processor as soon as it is out of the Timer Server. Then the MCU branches to scan for contact closures. It simply calls the routine GETXY as shown as Figure 6. Out of GETXY, the processor examines the Contact Flag. If a good contact is found, the processor resolves the X,Y coordinates on the LCD panel and then checks if the stylus is pointing to the area within the Eraser Icon. If so, it further examines the New Contact flag to determine whether it is a fresh

4. A power saving mode of MC68HC05.

touch. Only a fresh touch can trigger the Eraser Icon. This trigger will cause the processor to inverse the Eraser Icon and toggle the Eraser Flag. However if the coordinates are out of Eraser Icon, the routine will either carry out the erasing routine or the writing routine depending on the Eraser Flag. The writing routine is listed in Figure 6 which just puts a black dot at the X,Y location while the erasing routine will clean up a square of an effective area around to the stylus. Both routines end with Enabling the Timer with different speed settings for the fact that writing and erasing might have different repetitive rates. Also if no good contact is found, the Timer Server will be exited with the New Contact flag asserted and the timer interrupt is enabled with the IDLE speed set. As a result, the system may have different scan rates for erasing, for writing and for idle scanning. On exiting the Server, the processor loops back to WAIT and repeats the same procedure. The attached appendix lists the source code for the software and it starts up with the screen as shown in Figure 8. A 16x16 eraser icon is located at the upper right hand corner of the LCD panel.

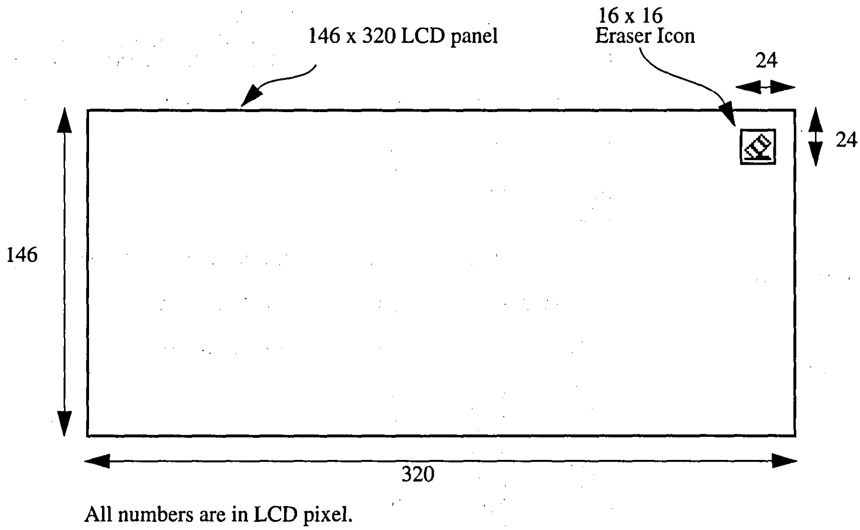

Figure 8. The Start Up Screen Of The Demonstration Software

APPENDIX : THE LISTING OF THE DEMONSTRATION SOFTWARE

```
                    ***************** LCD CONTROL REGISTER ********************
0028                    MODE    EQU     $28     MODE AND ATTRIBUTE REGISTER
0000                    SEQ     EQU     0
0001                    OSH     EQU     1
0002                    S0      EQU     2
0003                    S1      EQU     3
0004                    INVA    EQU     4
0005                    INVB    EQU     5
0006                    MOD     EQU     6
0007                    RSW     EQU     7       REGISTER SWITCH

0029                    LFTPTR  EQU     $29     LEFT POINTER
002B                    RGTPTR  EQU     $2B     RIGHT POINTER
002D                    SHTREG  EQU     $2D     SHIFT REGISTER
002D                    LOOP    EQU     $2D     LOOP SIZE REGISTER
002F                    HP      EQU     $2F     HORIZONTAL PITCH REGISTER

0030                    STATUS  EQU     $30     STATUS REGISTER AND ITS BITS
DEFINITION
0000                    RDY     EQU     0
0001                    ACT     EQU     1
0002                    HPOF    EQU     2
0003                    RGST    EQU     3

0030                    PSCALAR EQU     $30     PRESCALAR REGISTER FOR MUX
RATIO SELECTION
0031                    SEGMENT EQU     $31     SEGMENT CONTROL REGISTER

0032                    LCDMREG EQU     $32     LCD MODE REGISTER AND ITS BITS
DEFINITION
0000                    DON     EQU     0
0001                    CR1     EQU     1
0002                    CR2     EQU     2
0003                    DDIR    EQU     3
0004                    BS0     EQU     4
0005                    BS1     EQU     5
0006                    DPAN    EQU     6
0007                    MSW     EQU     7

                    ***************** SYSTEM CLOCK REGISTERS ******************
0021                    CTL21   EQU     $21     CONTROL REGISTER $21
0004                    PLLI    EQU     4
0005                    FS0     EQU     5
0006                    FS1     EQU     6

0025                    CTL25   EQU     $25     CONTROL REGISTER $25
0000                    CLKS    EQU     0
0003                    PORTI   EQU     3
0007                    TIMI    EQU     7

                    ***************** TIMER REGISTERS ************************
0012                    TCR     EQU     $12     TIMER CONTROL REGISTER
0000                    OLVL1   EQU     0
0001                    IEDG    EQU     1
0002                    OLVL2   EQU     2
0004                    OCIE2   EQU     4
0005                    TOIE    EQU     5
0006                    OCIE1   EQU     6
0007                    ICIE    EQU     7

0013                    TSR     EQU     $13     TIMER STATUS REGISTER
0004                    OCF2    EQU     4
```

```
0005            TOF     EQU     5
0006            OCF1    EQU     6
0007            ICF     EQU     7

0016            OUTCMP1 EQU     $16     TIMER OUTPUT COMPARE1 REGISTER

0018            TIMER   EQU     $18     TIMER COUNT REGISTER

001A            ATIMER  EQU     $1A     ALTERNATE COUNT REGISTER

001C            OUTCMP2 EQU     $1C     TIMER OUTPUT COMPARE2 REGISTER

              ***************** SPI REGISTERS **************************
0022            SPCR    EQU     $22     SPI CONTROL REGISTER
0000            SPR0    EQU     0
0001            SPR1    EQU     1
0002            CPHA    EQU     2
0003            CPOL    EQU     3
0004            MSTR    EQU     4
0006            SPE     EQU     6
0007            SPIE    EQU     7

0023            SPSR    EQU     $23     SPI STATUS REGISTER
0004            MODF    EQU     4
0006            WCOL    EQU     6
0007            SPIF    EQU     7

0024            SPDR    EQU     $24     SPI DATA I/O REGISTER

              ***************** CONTROL PORTS **************************
0008            PORTCDR EQU     $08     PORTC DATA DIRECTION REGISTER
0002            PORTC   EQU     $02     PORTC DATA REGISTER
0000            ADSEL_  EQU     0       SELECT A TO D CONVERTER
0001            UPVREF_ EQU     1       DISCONNECT/CONNECT THE VREF
FOR UPPER FILM
0002            UPGND   EQU     2       CONNECT/DISCONNECT THE GND FOR
UPPER FILM
0004            LWVREF_ EQU     4       DISCONNECT/CONNECT THE VREF
FOR LOW FILM
0003            LWGND   EQU     3       CONNECT/DISCONNECT THE GND FOR
LOW FILM

              ***************** CONSTANTS ******************************
0028            SEED1H  EQU     $28
0000            SEED1L  EQU     $00
001F            SEED2H  EQU     $1F
0000            SEED2L  EQU     $00
00FF            IDLEH   EQU     $FF
0000            IDLEL   EQU     $00
00C0            TRIGGERH EQU    $C0
0000            TRIGGERL EQU $00
0001            WICONX1H EQU$01
0028            WICONX1L EQU$28
0001            WICONX2H EQU$01
0037            WICONX2L EQU$37
0008            WICONY1 EQU     $8
0017            WICONY2 EQU     $17
0000            LFTBDH  EQU$00
0060            LFTBDL  EQU     $60
0000            TOPBDH  EQU     $00
0090            TOPBDL  EQU     $90

0001            FLLOOPH EQU     $1
003F            FLLOOPL EQU     $3F
009F            HFLOOP  EQU     $9F
0091            SCNHGT  EQU     145
```

```
                     ****************** VARIABLES AND FLAGS ********************
0050                     TSPFLGS EQU     $50
0000                     CONTACT EQU     0       GOOD/BAD CONTACT - CONTACT FLAG
0001                     NEWCONT EQU     1       NEW/OLD CONTACT - NEW CONTACT
FLAG
0002                     ERASER  EQU     2       ON/OFF ERASER - ERASER FLAG

0052                     X       EQU     $52     STORAGE OF X COORDINATE
0054                     Y       EQU     $54     STORAGE OF Y COORDINATE
0056                     YD      EQU     $56     DUMMY VARIABLE
0057                     FN      EQU     $57     FOR LONG OPERATIONS
0059                     SN      EQU     $59     FOR LONG OPERATIONS

0200                             ORG     $200
                     ***************** DRAWRUB *********************************
0200 10 25               DRAWRUB BSET    CLKS,CTL25       SELECT PLL CLOCK
0202 1B 21                       BCLR    FS0,CTL21        SET SYSTEM CLOCK TO
2.44MHZ
0204 1C 21                       BSET    FS1,CTL21
0206 08 21 FD                    BRSET   PLLI,CTL21,*
0209 09 21 FD                    BRCLR   PLLI,CTL21,*     WAIT FOR PLL STABLE

                     **************** SET UP CONTROL PORTS ********************
020C 10 08                       BSET    ADSEL_,PORTCDR
020E 12 08                       BSET    UPVREF_,PORTCDR
0210 14 08                       BSET    UPGND,PORTCDR
0212 18 08                       BSET    LWVREF_,PORTCDR
0214 16 08                       BSET    LWGND,PORTCDR
0216 10 02                       BSET    ADSEL_,PORTC

                         * SET TRANSISTORS LADDER TO IDLE *
0218 12 02                       BSET    UPVREF_,PORTC
021A 15 02                       BCLR    UPGND,PORTC
021C 18 02                       BSET    LWVREF_,PORTC
021E 17 02                       BCLR    LWGND,PORTC

                         * SET UP LCD SYSTEM *
0220 1E 32                       BSET    MSW,LCDMREG
0222 A6 91                       LDA     #SCNHGT
0224 B7 31                       STA     SEGMENT
0226 A6 20                       LDA     #$20
0228 B7 30                       STA     PSCALAR
022A 1F 32                       BCLR    MSW,LCDMREG
022C 10 32                       BSET    DON,LCDMREG
022E 12 32                       BSET    CR1,LCDMREG
0230 14 32                       BSET    CR2,LCDMREG
0232 18 32                       BSET    BS0,LCDMREG
0234 1A 32                       BSET    BS1,LCDMREG
0236 1C 32                       BSET    DPAN,LCDMREG
0238 A6 04                       LDA     #%00000100
023A B7 31                       STA     SEGMENT
023C 13 32                       BCLR    CR1,LCDMREG
023E 15 32                       BCLR    CR2,LCDMREG
0240 A6 92                       LDA     #SCNHGT+1
0242 4A                  CLRROW  DECA
0243 B7 31                       STA     SEGMENT
0245 26 FB                       BNE     CLRROW
0247 3F 29                       CLR     LFTPTR
0249 3F 2A                       CLR     LFTPTR+1

024B 3F 50                       CLR     TSPFLGS          CLEAR ALL FLAGS
024D 12 50                       BSET    NEWCONT,TSPFLGS  NEXT CONTACT IS NEW
024F CD 05 3A                    JSR     PUTICON

                         * CHECK A/D CIRCUIT *
0252 1C 22                       BSET    SPE,SPCR
```

```
0254 11 02              A_DCHK  BCLR    ADSEL_,PORTC
0256 A6 B0                      LDA     #$B0
0258 B7 24                      STA     SPDR
025A 0F 23 FD                   BRCLR   SPIF,SPSR,*
025D B6 24                      LDA     SPDR
025F B7 57                      STA     FN
0261 3F 24                      CLR     SPDR
0263 0F 23 FD                   BRCLR   SPIF,SPSR,*
0266 10 02                      BSET    ADSEL_,PORTC
0268 B6 24                      LDA     SPDR
026A B7 58                      STA     FN+1
026C A6 80                      LDA     #$80
026E B7 59                      STA     SN
0270 4F                         CLRA
0271 B7 5A                      STA     SN+1
0273 CD 02 B0                   JSR     LONGCMP
0276 27 07                      BEQ     A_DOK
0278 A6 20                      LDA     #$20
027A 4A                 A_DWAIT DECA
027B 26 FD                      BNE     A_DWAIT
027D 20 D5                      BRA     A_DCHK
                        A_DOK

                        * ENABLE TIMER INTERRUPT *

027F 16 25                      BSET    PORTI,CTL25       ENABLING TIMER
0281 B6 18                      LDA     TIMER
0283 B7 57                      STA     FN
0285 B6 19                      LDA     TIMER+1
0287 B7 58                      STA     FN+1
0289 A6 FF                      LDA     #IDLEH
028B B7 59                      STA     SN
028D A6 00                      LDA     #IDLEL
028F B7 5A                      STA     SN+1
0291 CD 02 A3                   JSR     LONGADD
0294 B6 13                      LDA     TSR     CLEAR OCF2 FOR SYSTEM SECURITY
0296 B6 57                      LDA     FN
0298 B7 16                      STA     OUTCMP1
029A B6 58                      LDA     FN+1
029C B7 17                      STA     OUTCMP1+1
029E 1C 12                      BSET    OCIE1,TCR         ENABLING OUTPUT
COMPARE1 INTERRUPT

                        * ENTER WAIT *
02A0 8F                 TOWAIT  WAIT
02A1 20 FD                      BRA     TOWAIT
                     **************** END OF DRAWRUB ***************************

                     **************** LONG CALCULATIONS SUBROUTINES ************
                     **********************************************************
                        *       LONGADD - DOUBLE BYTE ADDITION
                        *               FN:FN+1 = MSB,LSB OF THE FISRT NUMBER
                        *               SN:SN+1 = MSB,LSB OF THE SECOND NUMBER
                        *       FORMULA FN = FN + SN
                     **********************************************************

02A3 B6 58              LONGADD LDA     FN+1
02A5 BB 5A                      ADD     SN+1
02A7 B7 58                      STA     FN+1
02A9 B6 57                      LDA     FN
02AB B9 59                      ADC     SN
02AD B7 57                      STA     FN
02AF 81                         RTS


                     **********************************************************
                       *      LONGCMP - COMPARE TWO UNSIGNED DOUBLE BYTE NUMBERS
```

```
                    *                FN:FN+1 = MSB,LSB OF FIRST NUMBER
                    *                SN:SN+1 = MSB,LSB OF SECOND NUMBER
               ***********************************************************

02B0 B6 57          LONGCMP LDA      FN
02B2 B1 59                  CMP      SN
02B4 26 04                  BNE      LCMPQT
02B6 B6 58                  LDA      FN+1
02B8 B1 5A                  CMP      SN+1
02BA 81             LCMPQT  RTS

               ***********************************************************
                    *       LONGSUB - DOUBLE BYTE SUBTRACTION
                    *                FN:FN+1 = MSB,LSB OF THE FIRST NUMBER
                    *                SN:SN+1 = MSB,LSB OF THE SECOND NUMBER
                    *       FORMULA FN = FN - SN
               ***********************************************************

02BB B6 58          LONGSUB LDA      FN+1
02BD B0 5A                  SUB      SN+1
02BF B7 58                  STA      FN+1
02C1 B6 57                  LDA      FN
02C3 B2 59                  SBC      SN
02C5 B7 57                  STA      FN
02C7 81                     RTS
                ***************** END OF CALCULATIONS SUBROUTINES *********

               ***************** TIMERSERVER ******************************
                    TIMERSERVER
02C8 B6 13                  LDA      TSR      NEXT ACCESS TO OUTCMP1 WILL
CLEAR FLAG
02CA CD 04 2C               JSR      GETXY
02CD 00 50 04               BRSET    CONTACT,TSPFLGS,GOODCONTACTIF GOOD
CONTACT
02D0 12 50                  BSET     NEWCONT,TSPFLGS         NEXT CONTACT
IS NEW
02D2 20 65                  BRA      IDLING
                    GOODCONTACT
02D4 34 52                  LSR      X
02D6 36 53                  ROR      X+1
02D8 B6 53                  LDA      X+1
02DA B7 58                  STA      FN+1
02DC B6 52                  LDA      X
02DE B7 57                  STA      FN

02E0 A6 00                  LDA      #LFTBDH
02E2 B7 59                  STA      SN
02E4 A6 60                  LDA      #LFTBDL
02E6 B7 5A                  STA      SN+1
02E8 CD 02 BB               JSR      LONGSUB
02EB 25 3D                  BCS      SETRATE
                    INLFTBOUND
02ED A6 01                  LDA      #FLLOOPH
02EF B7 59                  STA      SN
02F1 A6 3F                  LDA      #FLLOOPL
02F3 B7 5A                  STA      SN+1
02F5 CD 02 B0               JSR      LONGCMP
02F8 22 30                  BHI      SETRATE

                    INRGTBOUND
02FA B6 57                  LDA      FN
02FC B7 52                  STA      X
02FE B6 58                  LDA      FN+1
0300 B7 53                  STA      X+1

0302 34 54                  LSR      Y
0304 36 55                  ROR      Y+1
```

```
0306 34 54                       LSR     Y
0308 36 55                       ROR     Y+1
030A B6 54                       LDA     Y
030C B7 57                       STA     FN
030E B6 55                       LDA     Y+1
0310 B7 58                       STA     FN+1
0312 A6 00                       LDA     #TOPBDH
0314 B7 59                       STA     SN
0316 A6 90                       LDA     #TOPBDL
0318 B7 5A                       STA     SN+1
031A CD 02 BB                    JSR     LONGSUB
031D 25 0B                       BCS     SETRATE

031F 3F 59                       CLR     SN
0321 A6 91                       LDA     #SCNHGT
0323 B7 5A                       STA     SN+1
0325 CD 02 B0                    JSR     LONGCMP
0328 23 15                       BLS     PASS2

                         SETRATE
032A 04 50 06                    BRSET   ERASER,TSPFLGS,SETRATE1
032D A6 1F                       LDA     #SEED2H
032F AE 00                       LDX     #SEED2L
0331 20 41                       BRA     GENRATE
                         SETRATE1
0333 A6 28                       LDA     #SEED1H
0335 AE 00                       LDX     #SEED1L
0337 20 3B                       BRA     GENRATE
                         IDLING
0339 A6 00                       LDA     #IDLEL
033B AE FF                       LDX     #IDLEH
033D 20 35                       BRA     GENRATE
                         PASS2
033F B6 58                       LDA     FN+1
0341 B7 54                       STA     Y                 Y BECOMES ONE BYTE
VARIABLE NOW

                         * CHECK X,Y IN ERASER ICON *
0343 B6 54                       LDA     Y
0345 A1 08                       CMP     #WICONY1
0347 25 4E                       BLO     NOTICON
0349 A1 17                       CMP     #WICONY2
034B 22 4A                       BHI     NOTICON
034D B6 52                       LDA     X
034F B7 57                       STA     FN
0351 B6 53                       LDA     X+1
0353 B7 58                       STA     FN+1
0355 A6 28                       LDA     #WICONX1L
0357 B7 59                       STA     SN
0359 A6 01                       LDA     #WICONX1H
035B B7 5A                       STA     SN+1
035D CD 02 B0                    JSR     LONGCMP
0360 25 35                       BLO     NOTICON
0362 A6 37                       LDA     #WICONX2L
0364 B7 59                       STA     SN
0366 A6 01                       LDA     #WICONX2H
0368 B7 5A                       STA     SN+1
036A CD 02 B0                    JSR     LONGCMP
036D 22 28                       BHI     NOTICON
036F 02 50 1A                    BRSET   NEWCONT,TSPFLGS,ICON
0372 20 C5                       BRA     IDLING
                         GENRATE
0374 B7 59                       STA     SN
0376 BF 5A                       STX     SN+1
0378 B6 18                       LDA     TIMER
037A B7 57                       STA     FN
037C B6 19                       LDA     TIMER+1
```

```
037E B7 58                 STA    FN+1
0380 CD 02 A3              JSR    LONGADD
0383 B6 57                 LDA    FN
0385 B7 16                 STA    OUTCMP1
0387 B6 58                 LDA    FN+1
0389 B7 17                 STA    OUTCMP1+1
038B 80                    RTI

038C A6 04        ICON     LDA#$04
038E B8 50                 EOR    TSPFLGS          TOGGLING ERASER FLAG
0390 CD 05 03              JSR    INVERSE
0393 13 50                 BCLR   NEWCONT,TSPFLGS
0395 20 A2                 BRA    IDLING

                  NOTICON
0397 04 50 4F              BRSET  ERASER,TSPFLGS,DOERASE
039A B6 52                 LDA    X
039C B7 57                 STA    FN
039E B6 53                 LDA    X+1
03A0 B7 58                 STA    FN+1
03A2 A6 9F                 LDA    #HFLOOP
03A4 B7 5A                 STA    SN+1
03A6 3F 59                 CLR    SN
03A8 CD 02 BB              JSR    LONGSUB
03AB 25 06                 BCS    RGTHFSCREEN
03AD 19 32                 BCLR   BS0,LCDMREG
03AF 1A 32                 BSET   BS1,LCDMREG
03B1 20 04                 BRA    PUTDOT

                  RGTHFSCREEN
03B3 18 32                 BSET   BS0,LCDMREG
03B5 1B 32                 BCLR   BS1,LCDMREG
                  PUTDOT
03B7 B6 57                 LDA    FN
03B9 B7 2B                 STA    RGTPTR
03BB B6 58                 LDA    FN+1
03BD B7 2C                 STA    RGTPTR+1
03BF 12 32                 BSET   CR1,LCDMREG
03C1 15 32                 BCLR   CR2,LCDMREG
03C3 B6 54                 LDA    Y
03C5 B7 31                 STA    SEGMENT
03C7 1E 28                 BSET   RSW,MODE
03C9 3F 2E                 CLR    LOOP+1
03CB A6 9F                 LDA    #HFLOOP
03CD B7 2D                 STA    LOOP
03CF 1F 28                 BCLR   RSW,MODE
03D1 A6 01                 LDA    #$01
03D3 B7 2E                 STA    SHTREG+1
03D5 3F 2F                 CLR    HP
03D7 A6 42                 LDA    #%01000010
03D9 B7 28                 STA    MODE
03DB 06 30 FD              BRSET  RGST,STATUS,*
03DE 12 32                 BSET   CR1,LCDMREG
03E0 B6 54                 LDA    Y
03E2 B7 31                 STA    SEGMENT
03E4 13 50                 BCLR   NEWCONT,TSPFLGS
03E6 CC 03 2A              JMP    SETRATE

                  DOERASE
03E9 1A 32                 BSET   BS1,LCDMREG
03EB 18 32                 BSET   BS0,LCDMREG
03ED A6 05                 LDA    #5
03EF B7 56                 STA    YD
03F1 B6 52                 LDA    X
03F3 B7 2B                 STA    RGTPTR
03F5 B6 53                 LDA    X+1
03F7 B7 2C                 STA    RGTPTR+1
```

```
03F9 1E 28                    BSET    RSW,MODE
03FB A6 01                    LDA     #FLLOOPH
03FD B7 2D                    STA     LOOP
03FF A6 3F                    LDA     #FLLOOPL
0401 B7 2E                    STA     LOOP+1
0403 1F 28                    BCLR    RSW,MODE
0405 A6 04                    LDA     #4
0407 B7 2F                    STA     HP
0409 15 32                    BCLR    CR2,LCDMREG
040B B6 54                    LDA     Y
                      REDO
040D 12 32                    BSET    CR1,LCDMREG
040F B7 31                    STA     SEGMENT
0411 3F 2E                    CLR     SHTREG+1
0413 AE 42                    LDX     #%01000010
0415 BF 28                    STX     MODE

0417 06 30 FD                 BRSET   RGST,STATUS,*
041A 13 32                    BCLR    CR1,LCDMREG
041C B7 31                    STA     SEGMENT
041E 4C                       INCA
041F A1 91                    CMP     #SCNHGT
0421 22 04                    BHI     EQUIP
0423 3A 56                    DEC     YD
0425 26 E6                    BNE     REDO
                      EQUIP
0427 13 50                    BCLR    NEWCONT,TSPFLGS
0429 CC 03 2A                 JMP     SETRATE


                 **************** GETXY **********************************
042C 18 02            GETXY   BSET    LWVREF_,PORTC    NOW THE LOWER FILM IS
ENERGIZED
                      * CONTACT DETECTION *
042E 11 02                    BCLR    ADSEL_,PORTC
0430 A6 10                    LDA     #$10             CONTACT DETECTION
0432 B7 24                    STA     SPDR
0434 0F 23 FD                 BRCLR   SPIF,SPSR,*
0437 3F 24                    CLR     SPDR
0439 0F 23 FD                 BRCLR   SPIF,SPSR,*
043C 10 02                    BSET    ADSEL_,PORTC
043E 18 02                    BSET    LWVREF_,PORTC
0440 A6 0A                    LDA     #10      A TO D NEEDS >=88 CYCLES FOR
CONVERSION
                      CYCLES88
0442 4A                       DECA
0443 26 FD                    BNE     CYCLES88

                      * GET CONTACT AND COMMAND FOR CONVERTING X *
0445 19 02                    BCLR    LWVREF_,PORTC
0447 16 02                    BSET    LWGND,PORTC
0449 11 02                    BCLR    ADSEL_,PORTC
044B A6 10                    LDA     #$10     GET CONTACT LEVEL
044D B7 24                    STA     SPDR
044F 0F 23 FD                 BRCLR   SPIF,SPSR,*
0452 B6 24                    LDA     SPDR
0454 B7 57                    STA     FN
0456 3F 24                    CLR     SPDR
0458 0F 23 FD                 BRCLR   SPIF,SPSR,*
045B B6 24                    LDA     SPDR
045D B7 58                    STA     FN+1
045F 10 02                    BSET    ADSEL_,PORTC
0461 18 02                    BSET    LWVREF_,PORTC
0463 17 02                    BCLR    LWGND,PORTC
                      * CHECK CONTACT LEVEL IN FN IS LARGER THAN TRIGGER *
0465 A6 C0                    LDA     #TRIGGERH        PROCESS TAKES 35
CYCLES
```

```
0467 B7 59                   STA     SN
0469 A6 00                   LDA     #TRIGGERL
046B B7 5A                   STA     SN+1
046D CD 02 B0                JSR     LONGCMP
0470 24 03                   BHS     PASSCONT1
                     FAILEXIT
0472 11 50                   BCLR    CONTACT,TSPFLGS
0474 81                      RTS
                     PASSCONT1
                     * NEEDS EXTRA 53 CYCLES
0475 A6 09                   LDA     #$9
0477 4A              CYC53   DECA
0478 26 FD                   BNE     CYC53

                     * GET X AND COMMAND FOR CONVERTING Y *
047A 13 02                   BCLR    UPVREF_,PORTC
047C 14 02                   BSET    UPGND,PORTC
047E 11 02                   BCLR    ADSEL_,PORTC
0480 A6 00                   LDA     #$00            GET X, CONVERTING Y
0482 B7 24                   STA     SPDR
0484 0F 23 FD                BRCLR   SPIF,SPSR,*
0487 B6 24                   LDA     SPDR
0489 B7 53                   STA     X+1
048B 3F 24                   CLR     SPDR
048D 0F 23 FD                BRCLR   SPIF,SPSR,*
0490 B6 24                   LDA     SPDR
0492 A4 C0                   AND     #$C0
0494 B7 52                   STA     X
0496 10 02                   BSET    ADSEL_,PORTC
0498 12 02                   BSET    UPVREF_,PORTC
049A 15 02                   BCLR    UPGND,PORTC
049C 38 52                   LSL     X           PROCESS TAKES 25 CYCLES
049E 39 53                   ROL     X+1
04A0 39 52                   ROL     X
04A2 39 53                   ROL     X+1
04A4 39 52                   ROL     X
                     * A TO D NEEDS EXTRA 63 CYCLES
04A6 A6 0A                   LDA     #$A             A TO D NEEDS >=88
CYCLES FOR CONVERSION
                     CYCLES63
04A8 4A                      DECA
04A9 26 FD                   BNE     CYCLES63
                     * GET Y AND COMMAND FOR ANOTHER CONTACT *
04AB 19 02                   BCLR    LWVREF_,PORTC
04AD 11 02                   BCLR    ADSEL_,PORTC
04AF A6 10                   LDA     #$10            GET Y
04B1 B7 24                   STA     SPDR
04B3 0F 23 FD                BRCLR   SPIF,SPSR,*
04B6 B6 24                   LDA     SPDR
04B8 B7 55                   STA     Y+1
04BA 3F 24                   CLR     SPDR
04BC 0F 23 FD                BRCLR   SPIF,SPSR,*
04BF B6 24                   LDA     SPDR
04C1 A4 C0                   AND     #$C0
04C3 B7 54                   STA     Y
04C5 10 02                   BSET    ADSEL_,PORTC
04C7 18 02                   BSET    LWVREF_,PORTC
04C9 38 54                   LSL     Y               PROCESS TAKES 25
CYCLES
04CB 39 55                   ROL     Y+1
04CD 39 54                   ROL     Y
04CF 39 55                   ROL     Y+1
04D1 39 54                   ROL     Y

                     * A TO D NEEDS EXTRA 63 CYCLES
04D3 A6 0A                   LDA     #$A             A TO D NEEDS >=88
CYCLES FOR CONVERSION
```

```
                         CYC53_2
04D5 4A                          DECA
04D6 26 FD                       BNE     CYC53_2

                         * GET ANOTHER CONTACT *
04D8 11 02                       BCLR    ADSEL_,PORTC
04DA A6 10                       LDA     #$10            GET CONTACT
04DC B7 24                       STA     SPDR
04DE 0F 23 FD                    BRCLR   SPIF,SPSR,*
04E1 B6 24                       LDA     SPDR
04E3 B7 57                       STA     FN
04E5 3F 24                       CLR     SPDR
04E7 0F 23 FD                    BRCLR   SPIF,SPSR,*
04EA B6 24                       LDA     SPDR
04EC B7 58                       STA     FN+1
04EE 10 02                       BSET    ADSEL_,PORTC
                         * CHECK CONTACT LEVEL IN FN IS LARGER THAN TRIGGER *
04F0 A6 C0                       LDA     #TRIGGERH
04F2 B7 59                       STA     SN
04F4 A6 00                       LDA     #TRIGGERL
04F6 B7 5A                       STA     SN+1
04F8 CD 02 B0                    JSR     LONGCMP
04FB 24 03                       BHS     SUCCESS
04FD CC 04 72                    JMP     FAILEXIT
                         SUCCESS
0500 10 50                       BSET    CONTACT,TSPFLGS
0502 81                          RTS

                    **************** INVERSE **********************************
                         INVERSE
0503 1B 32                       BCLR    BS1,LCDMREG
0505 18 32                       BSET    BS0,LCDMREG
0507 3F 2B                       CLR     RGTPTR
0509 A6 97                       LDA     #$97
050B B7 2C                       STA     RGTPTR+1
050D 1E 28                       BSET    RSW,MODE
050F A6 9F                       LDA     #HFLOOP
0511 B7 2E                       STA     LOOP+1
0513 3F 2D                       CLR     LOOP
0515 1F 28                       BCLR    RSW,MODE
0517 A6 88                       LDA     #$88
0519 B7 2A                       STA     LFTPTR+1
051B A6 0F                       LDA     #$F
051D B7 2F                       STA     HP
051F 15 32                       BCLR    CR2,LCDMREG
0521 AE 08                       LDX     #WICONY1
                         NEXTROW1
0523 12 32                       BSET    CR1,LCDMREG
0525 BF 31                       STX     SEGMENT
0527 A6 61                       LDA     #%01100001
0529 B7 28                       STA     MODE
052B 06 30 FD                    BRSET   RGST,STATUS,*
052E 13 32                       BCLR    CR1,LCDMREG
0530 BF 31                       STX     SEGMENT
0532 5C                          INCX
0533 A3 17                       CPX     #WICONY2
0535 23 EC                       BLS     NEXTROW1
0537 3F 2A                       CLR     LFTPTR+1
0539 81                          RTS

                    **************** PUTICON **********************************
                         PUTICON
053A 1B 32                       BCLR    BS1,LCDMREG
053C 18 32                       BSET    BS0,LCDMREG
053E 3F 2B                       CLR     RGTPTR
0540 A6 87                       LDA     #$87
0542 B7 2C                       STA     RGTPTR+1
```

```
0544 1E 28                    BSET   RSW,MODE
0546 A6 9F                    LDA    #HFLOOP
0548 B7 2E                    STA    LOOP+1
054A 3F 2D                    CLR    LOOP
054C 1F 28                    BCLR   RSW,MODE
054E A6 0F                    LDA    #$F
0550 B7 2F                    STA    HP
0552 15 32                    BCLR   CR2,LCDMREG
0554 5F                       CLRX
0555 A6 08                    LDA    #WICONY1
                      NEXTROW
0557 B7 56                    STA    YD
0559 12 32                    BSET   CR1,LCDMREG
055B B7 31                    STA    SEGMENT
055D D6 05 7C                 LDA    ICONBASE,X
0560 B7 2D                    STA    SHTREG
0562 5C                       INCX
0563 D6 05 7C                 LDA    ICONBASE,X
0566 B7 2E                    STA    SHTREG+1
0568 A6 42                    LDA    #%01000010
056A B7 28                    STA    MODE
056C 5C                       INCX
056D 06 30 FD                 BRSET  RGST,STATUS,*
0570 13 32                    BCLR   CR1,LCDMREG
0572 B6 56                    LDA    YD
0574 B7 31                    STA    SEGMENT
0576 4C                       INCA
0577 A1 10                    CMP    #$10
0579 26 DC                    BNE    NEXTROW
057B 81                       RTS
                      ICONBASE
057C FF FF 80 01 80 41        FCB    $FF,$FF,$80,$01,$80,$41,$80,$A1
     80 A1
0584 81 91 82 C9 84 65        FCB    $81,$91,$82,$C9,$84,$65,$8C,$39
     8C 39
058C 96 11 A3 21 91 C1        FCB    $96,$11,$A3,$21,$91,$C1,$88,$C1
     88 C1
0594 85 F9 BF FD 80 01        FCB    $85,$F9,$BF,$FD,$80,$01,$FF,$FF
     FF FF

7FF6                          ORG    $7FF6
7FF6 02 C8            VTIMER  FDB    TIMERSERVER

7FFE                          ORG    $7FFE
7FFE 02 00            VRESET  FDB    DRAWRUB
```

Using MC141562, MC141563 LCD Driver with MC68328 DragonBall™ in PDA Application

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INTRODUCTION

MC141562 and MC141563 are a kit of LCD driver ICs offered by Motorola for medium to large LCD systems. The MC141562 is a 100-channel LCD Common Driver and the MC141563 is a 80-channel LCD Segment Driver. They can be directly used with the Motorola processor MC68328 DragonBall™ for PDA or other application. Both LCD Drivers are cascadable for driving different LCD sizes. This application note illustrates a PDA LCD module design using this kit with MC68328 and gives hardware example for different arrangements.

LCD MODULE DESIGN

There are several things to be taken care of when designing LCD module with this chip-set:

- Operating voltage
- LCD bias levels
- M signal generation
- Display size
- Data shift direction
- TAB (Tape Automated Bonding) package

In this application note, a typical PDA display size 320 x 240 is chosen as example.

OPERATION VOLTAGE

Two supply voltages are required. VDD is for the IC's control logic and shift register, it is from 2.7V to 5.5V; VLCD (V<1> - V<6>) is for the high voltage common or segment driving cell and is a DC supply voltage from 10V to 28V. The VLCD voltage required is defined by the LCD characteristics. User should refer to threshold voltage for turning on/off LCD pixels in LCD specification. Typically for 320 x 240 pixels LCD, VLCD = 21V, VDD = 5.0V, VEE = -20V.

LCD BIAS LEVELS

LCD Driver requires six voltage bias level for the high voltage common or segment driver outputs. It can be generated by external voltage divider, see figure 1. In order to obtain optimum contrast for LCD panels, the bias levels should be selected such that

$BIAS = R1/(4R1+R2) = 1/(\sqrt{MUX} + 1)$

$V1/VLCD = 1/(\sqrt{MUX} + 1)$

$V2/VLCD = 2/(\sqrt{MUX} + 1)$

$V3/VLCD = (\sqrt{MUX} - 1)/(\sqrt{MUX} + 1)$

$V4/VLCD = \sqrt{MUX} /(\sqrt{MUX} + 1)$

Example: Mux = 240 ----- Bias = 1:16.5,

R1 = 6.8K, R2 = 75K, VR = 100K

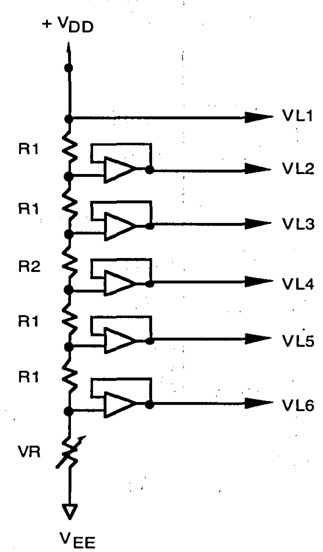


Figure 1. External Voltage Divider

User should also refer to the biasing recommendation in the LCD specifications.

REV 1
10/96

M SIGNAL GENERATION

M signal can be provided directly from MC68328 DragonBall™ or generated externally using the FLM frequency. See figure 2.

Example:
Use a J K Flip-Flop MC14027B.

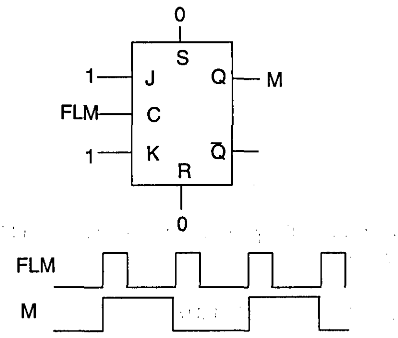


Figure 2. M Signal Generation

DISPLAY SIZE

For typical 320 x 240 display size, 3 x MC141562 and 4 x MC141563 are required. Simply define the display size by setting LCD screen format (screen width register and screen height register) in MC68328 DragonBall™. Depending on the Carry In / Carry Out (EIO1, EIO2, EIO3, EIO4) shift register direction of operation, the last 60 channels of common driver output are unused and left opened. See figure 3.

DIRECTION OF DATA SHIFT

There are 20 SCLK (shift clock) for 4 bit data shifting of total 80 bit data. Direction of data shift is defined by L/$\overline{R}$ pin on MC141563. User has to carefully define the data shift direction so as to obtain correct data sequence displayed. Physical arrangement of the TAB package is also needed to be taken into considerations. See figure 4 & 6.

DISPLAY OFF

A display off pin $\overline{\text{DIS-OFF}}$ is provided in both MC141562 and MC141563 for turning off the whole LCD display and save power.

$\overline{\text{DIS-OFF}}$ must pull high to turn on the display.

See figure 5.

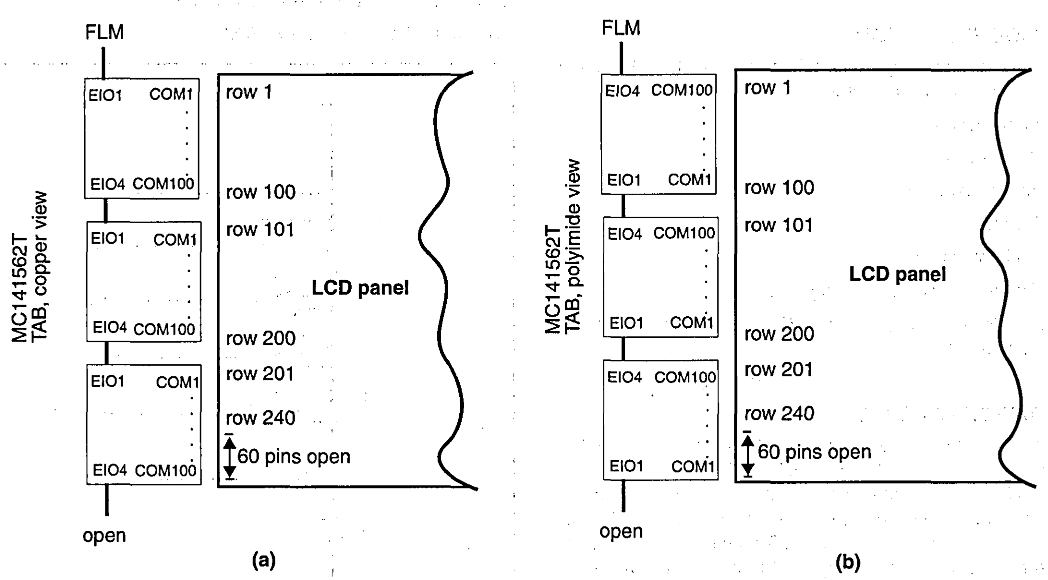
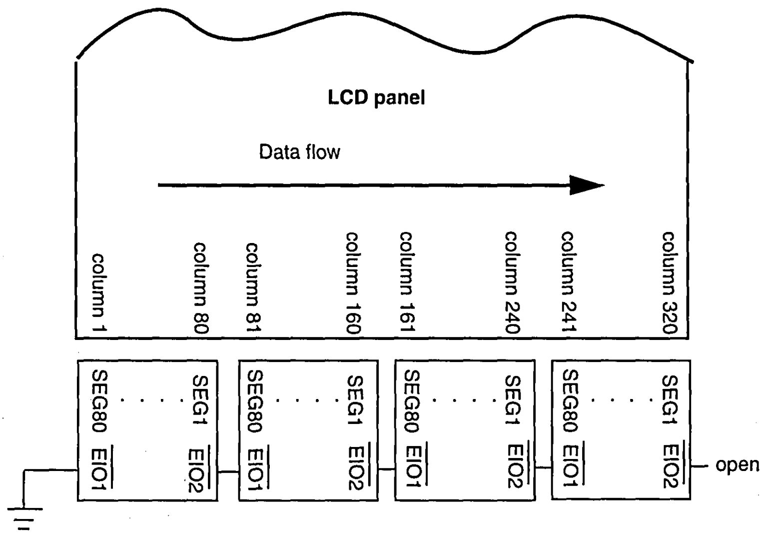
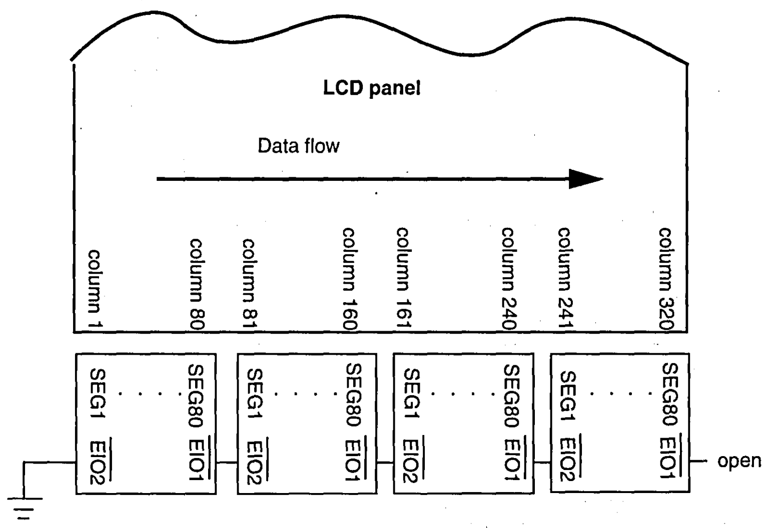


Figure 3. Common LCD Driver Arrangement for 240 rows
(a) Copper view of MC141562T, L/$\overline{R}$ = 0
(b) Polyimide view of MC141562T, L/$\overline{R}$ = 1



(a)



(b)

Figure 4. Segment LCD Driver Arrangement for 320 Columns
(a) Polyimide view of MC141563T, $L/\overline{R} = 0$
(b) Copper view of MC141563T, $L/\overline{R} = 1$

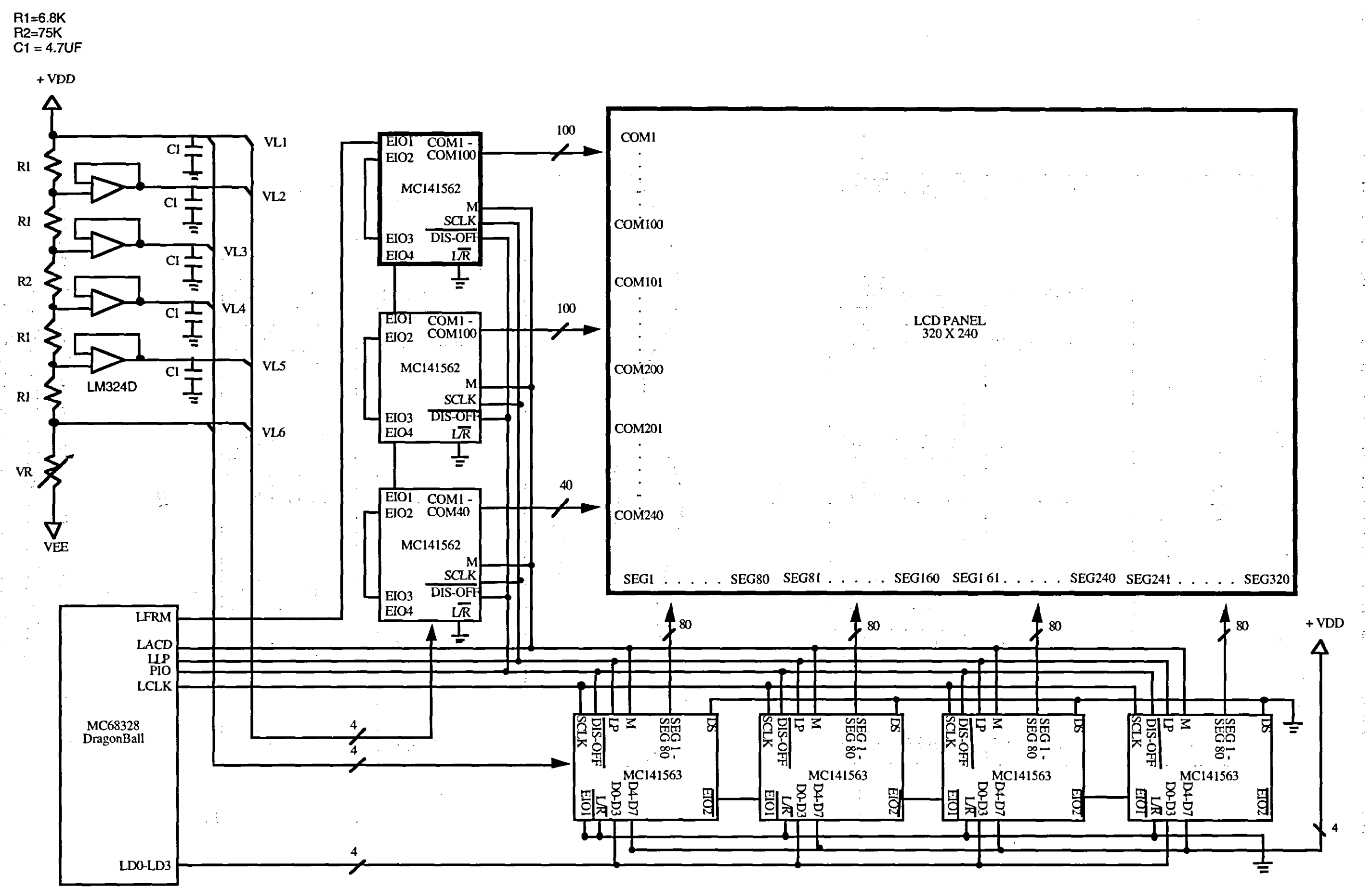


Figure 5. Application Example 320 x 240

TAB PACKAGE

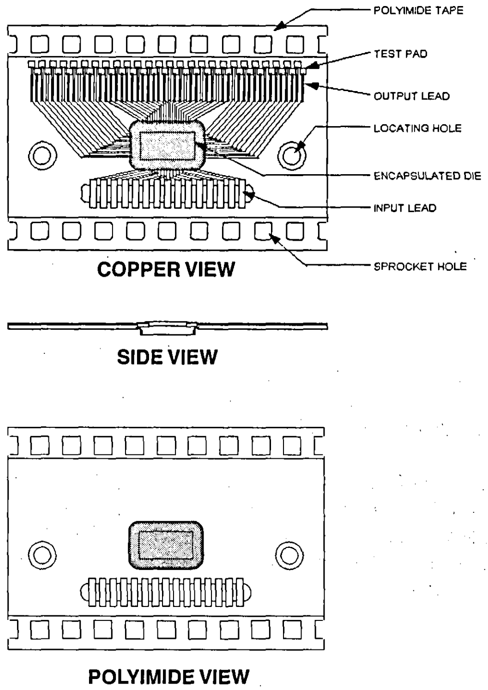


Figure 6. TAB Package

REFERENCE

MC141562 Technical Data, Advanced Information Rev 3.

MC141563 Technical Data, Advanced Information Rev 3.

MC68328 User's Manual, MC68328UM/D.

MC68328 Application Development System MC68328ADS Product Brief, MC68328ADS/D.

MOTOROLA

Microprocessor and Memory
Technologies Group

MC68328
MC68328V

Product Brief
Integrated Portable System Processor—DragonBall™

As the portable consumer market grows in full speed, the system requirements are becoming more rigorous than ever. Minimum components, small board space, low power consumption, and low system cost are several minimum criteria to a successful product. To address these needs, Motorola designed a new processor MC68328 DragonBall™. By providing 3.3V, fully static operation in an efficient package, the MC68328 delivers cost-effective performance to satisfy the extensive requirements of today's portable consumer market.

The MC68328 (shown in Figure 1) is the first integrated processor of the 68K Family to include a LCD controller, which demonstrates Motorola's focus on the portable market. With addition to the LCD controller, MC68328 provides key features that are suitable for many portable applications. Modules like RTC, PWM, Timers, Master SPI, Slave SPI, UART, and the System Integration Module (SIM28) facilitate the system engineer with more flexibility and resources to design efficient and innovative products.

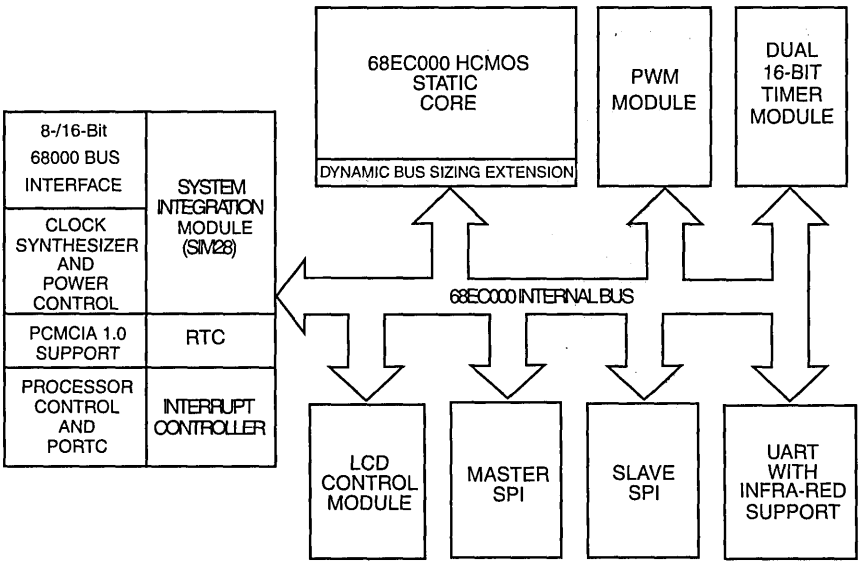


Figure 1. MC68328 Block Diagram

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

KEY FEATURES

The primary features of the MC68328 are as follows:

- Static 68EC000 Core Processor—Identical to MC68EC000 Microprocessor
  - — Full Compatibility with MC68000 and MC68EC000
  - — 32-Bit both External and Internal Address Bus capable of addressing 4GB Space
  - — 16-Bit On-Chip Data Bus for MC68000 Bus Operations
  - — Static Design Allows Processor Clock to be Stopped Providing Dramatic Power Savings
  - — 2.7 MIPS Performance at 16.67-MHz Processor Clock
- External M68000 Bus Interface with Dynamic Bus Sizing for 8-bit and 16-bit Data Ports
- System Integration Module (SIM28), Incorporating Many Functions Typically Relegated to External Array Logic, such as:
  - — System Configuration, Programmable Address Mapping
  - — Glueless Interface to SRAM, EPROM, FLASH Memory
  - — Sixteen Programmable Peripheral Chip Selects with Wait State Generation Logic
  - — Interrupt Controller with 13 flexible inputs
  - — Programmable Interrupt Vector Response for On-Chip Peripheral Modules
  - — Hardware Watchdog Timer
  - — Software Watchdog Timer
  - — Low-Power Mode Control
  - — Up to 78-Bit Individually Programmable Parallel I/O Ports
  - — PCMCIA 1.0 Support
- UART
  - — Support IrDA Physical Layer Protocol
  - — 8 Bytes FIFO on Rx and Tx
- Two Separated Serial Peripheral Interface Ports (Master and Slave)
  - — Support for External POCSAG Decoder (Slave)
  - — Support for Digitizer from A/D Input or EEPROM (Master)
- Dual Channel 16-Bit General Purpose Counter/timer
  - — Multimode Operation, Independent Capture/Compare Registers
  - — Automatic Interrupt Generation
  - — 240-ns Resolution at 16.67-MHz System Clock
  - — Each Timer has an Input and an Output Pin for Capture and Compare
- Pulse Width Modulation Output for Sound Generation
  - — Programmable Frame rate
  - — 16 Bit programmable
  - — Supports Motor Control
- Real Time Clock
  - — 24 Hour Time
  - — One Programmable Alarm
- Power Management
  - — 5 V or 3.3 V Operation
  - — Fully Static HCMOS Technology
  - — Programmable Clock Synthesizer for Full Frequency Control
  - — Low Power Stop Capabilities
  - — Modules can be Individually Shut-down
  - — Lowest Power Mode Control (Shut Down CPU and Peripherals)

- LCD Control Module
  - — Software Programmable Screen Size to Support Single (Non-Split) Monochrome/ STN Panels
  - — Capable Of Direct Driving Popular LCD Drivers/Modules from Motorola, Sharp, Hitachi, Toshiba etc.
  - — Support Up To 4 Grey Levels
  - — Utilize System Memory as Display Memory
- IEEE 1149.1 Boundary Scan Test Access Port (JTAG)
- Operation from DC To 16.67 MHz (Processor Clock)
- Operating Voltages of 3.3V ± 0.3V and 5V ± 0.5V
- Compact 144-Lead Thin Quad Flat Pack (TQFP) Package

SYSTEM INTEGRATION MODULE

The MC68328 system integration module (SIM28) consists of several functions that control the system start-up, initialization, configuration, and the external bus with a minimum of external devices. The memory interface allows the user to interface gluelessly with the popular SRAM, EPROM as well as PCMCIA 1.0 memory cards, with the assistance of chip-select logic, wait states can be programmable. The hardware and software watchdog timers help the user to do system protections. The interrupt controller accepts and resolves the priority from internal modules and external generated interrupts and also handles the masking and wake-up selection control for power control. The low-power logic can be used to control the CPU power dissipation by altering the frequency or stopping it. The SIM28 is also capable of configuring the pin to allow the user to select either dedicated I/O or parallel I/O. This feature helps to increase the number of available I/O ports by reclaiming when the dedicated function is not in used

System Configuration

The MC68328 system configuration logic consists of a system control register (SCR) and which allows the user to configure operation of the following major functions:

- System Status and Control Logic
- Register Double Mapping
- Bus Error Generation Control
- Protecting the module control registers from access by user programs

VCO/PLL Clock Synthesizer

The clock synthesizer can operate with either an external crystal or an external oscillator for reference, using the internal phase-locked loop (PLL) and voltage-controlled oscillator (VCO), or an external clock can directly drive the clock signal at the operating frequency.

Chip Select Logic

The MC68328 provides sixteen programmable general purpose chip-select signals. For a given chip-select block, the user may choose whether the chip-select allows read-only, or both read and write accesses, whether the chip-select should match only one function code value or all values, whether a $\overline{\text{DTACK}}$ is automatically generated for this chip-select, and after how many wait states (from zero to six) the $\overline{\text{DTACK}}$ will be generated.

External Bus Interface

The external bus interface handles the transfer of information between the internal 68EC000 core and the memory, peripherals, or other processing elements in the external address space. It consists of a 16-bit 68000 bus interface for internal and a selectable 8-bit or 16-bit interface to outside.

Interrupt Controller

The interrupt controller accepts and prioritizes both internal and external interrupt requests and generates a vector number during the CPU interrupt acknowledge cycle. Interrupt nesting is also provided so that an interrupt service routine of a lower priority interrupt may be suspended by a higher priority interrupt request. The on-chip interrupt controller has the following major features:

- Prioritized Interrupt Sources (Internal and External)
- A Fully Nested Interrupt Environment
- Programmable Vector Generation
- Interrupt Masking
- Wake-up interrupt Masking

Parallel General-Purpose I/O Ports

The MC68328 supports up to 78-bit general-purpose I/O ports, which can be configured as general-purpose I/O pins or as dedicated peripheral interface pins of the on-chip modules.

Each port pin can be independently programmed as general-purpose I/O pins, even when other pins related to the same on-chip peripheral are used as dedicated pins. Even if all the pins for a particular peripheral are configured as general-purpose I/O, the peripheral will still operate normally, although this is only useful in the case of the RTC and timer modules.

Software Watchdog

A software watchdog timer is used to protect against system failures by providing a means to escape from unexpected input conditions, external events, or programming errors. Once started, the software watchdog timer must be cleared by software on a regular basis so that it never reaches its time-out value. Upon reaching the time-out value, the assumption is made that a system failure has occurred, and the software watchdog logic resets or interrupts the 68EC000 core.

Low-Power Stop Logic

Various options for power-saving are available: turning off unused peripherals, reducing processor clock speed, disabling the processor altogether or a combination of these.

A wake-up from low-power mode can be achieved by causing an interrupt at the interrupt controller logic which runs throughout the period of processor low-power. Selectable interrupt will cause a wake-up of the EC000 core followed by processing of that interrupt.

The on-chip peripherals can initiate a wake-up; for example, the timer can be set to wake-up after a certain elapsed time, or number of external events.

LCD Controller

- Interfaces with Monochrome STN LCD Modules
- Up to 4 Levels of Gray Scale through Frame Rate Control
- Utilize system RAM for display memory
- Screen Refresh through DMA

UART and Infra-red Communication Support

The UART supports standard asynchronous serial communications at normal baud rates and is compatible with HPSIR/IrDA Physical Communication Protocol

Real Time Clock

Real Time Clock in MC68328 is driven by a 32.76KHz/38.4kHz Crystal which is the same as the Clock Synthesizer Clock source. It also provides interrupt for alarm.

JTAG Test Access Port

To aid in system diagnostics the MC68328 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as JTAG (Joint Test Action Group).

ORDERING INFORMATION

Table 1 identifies the packages and operating frequencies available for the MC68328.

Table 1. MC68328 Package/Frequency Availability

Package Type	V_{CC}	Frequency (MHz)	Temperature	Order Number
144-Lead TQFP	5V 3.3V	16.67 16.67	0°C to 70°C	MC68328

The documents listed in Table 2 contain detailed information on the MC68328. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Table 2. Documentation

Document Title	Order Number	Contents
MC68328 User's Manual	MC68328UM/AD	LDC Stocking est. 2Q95
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set

Effects of Bond Temperature and Pressure on Microstructures of Tape Automated Bonding(TAB) Inner Lead Bonds(ILB) with Thin Tape Metallization

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Abstract -- In view of the advantages of low cost, simple manufacturing process and significant miniaturization in size, Tape Automated Bonding(TAB) technology is important to the future development of consumer electronic products. Inner lead bonding(ILB) process is especially crucial for the production of high quality TAB packages and components. In this investigation, the effects of two critical bonding parameters: bond temperature and bond pressure on the final ILBs integrity and microstructures have been studied. The possibility of gang bonding 0.4 μm Sn-plated Cu lead beams with straight wall gold bumps to form reliable TAB inner lead bonds is demonstrated in this study.

The variations in microstructure of ILB joints have been studied by microsectioning, metallography, Scanning Electron Microscopy(SEM) and Energy Dispersive X-ray(EDX) Spectroscopy. The gold rich Au/Sn(80/20 wt.%) eutectic structure and ζ phase have been observed. However, it was found that the Au/Sn eutectic exhibit different structures as the bond temperature and pressure were changed. Binary Au/Sn and ternary Au/Sn/Cu intermetallic compounds have also been detected. The adhesion of the bonded interface has been studied by mechanical pull test. Lead pull values and the failure modes obtained are discussed with the result of microstructral evaluations.

INTRODUCTION

Tape Automated Bonding(TAB) is an electronic packaging technique for providing mechanical support, thermal dissipation & electrical connections to an integrated circuit chip or die which is connected to a substrate through the metal leads carried by a polymer tape. Having the advantages of low production cost, small in size and simple manufacturing process, TAB has been widely used in consumer electronic products such as LCD driver, pager, portable phone and others. Application of TAB in high performance, high pin-count chips also tends to increase. The success of TAB technology for a particular application is largely determined by the success of inner lead bonding to form reliable inner lead bonds(ILB) as it is the first step in TAB assembly process, which connect the chip to the tape.

In order to obtain high quality inner lead bonds, the bonding parameters must be optimized. Important bonding parameters for a given set of mating surface metallizations for leads and bumps are bonding temperature, pressure, dwell time and stage temperature. The bond quality greatly depends on the bonding temperature and pressure since the bonds formed by the action of them. The possible ranges of bonding parameter settings to produce quality ILBs is so-called process window. The process window for the bonding is narrow and difficult to identify, little changes on each individual bonding parameter may causes a great variety on the integrity and structure of the ILBs.

Thermocompression bonding of Au/Au and eutectic bonding of Au/Sn are two common methods of inner lead bonding. For thermocompression bonding, gold-plated lead beams are bonded with gold-bump. The quality of the bonds depends solely on solid-state diffusion of Au/Au. It is known that high bonding pressure and temperature can ensure adequate solid-state diffusion. However, such operating condition may cause cracks on pad structure and damages to the circuit devices which are sensitive to high processing temperature[1]. Another way to provide good quality of diffusion with lower bonding temperature and pressure is by eutectic Au/Sn bonding. Tin-plated lead beams are bonded with gold bump. The Au/Sn alloy is formed by the action of liquid tin and the solid gold during the bonding. Therefore, it is suitable for inner lead bonding those delicate devices. The desired structure of the inner lead bonds is eutectic Au/Sn for it has the advantages of relatively low melting temperature, high strength, free from thermal fatigue and low Young's modulus[2].

However, the formation of Au/Sn alloy during ILB is extremely dynamic[3]. Intermediate phases such as AuSn(δ phase), $AuSn_2$(ε phase) and $AuSn_4$(η phase) may result.

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All these phases are brittle in nature and may cause embrittlement of the ILBs. Ternary Au/Sn/Cu intermetallic compound may also form which may cause strong degradation of pull forces due to the formation of Kirkendall void[4].

The primary goal of this investigation is to obtain a fundamental understanding of the influence of bonding temperature and pressure on the dynamic alloy formation of Au/Sn system. In order to obtain the structural and compositional information on the ILBs, metallographic examination was employed to observe the microstructures formed on the boned zone. Besides, the possibility of bonding reduced tin-plating(0.4 μm) on gold bump is presented in this paper.

EXPERIMENTAL METHOD

Materials

TAB component devices of 97 lead counts and 3-layer tape were used. The lead beam material is electrodeposited(ED) copper and plated with thin tin of low roughness. The thickness of the tin plating is 0.4 μm. Straight wall gold bumps are deposited on the circuit devices. Characteristics of the TAB components are summarized and shown on Table I.

Table I. Characteristic data of the TAB component

Tape:	3-layer tape
Pin count:	97
Die size:	4.01 x 3.77 mm
Lead width:	60 μm
Bump material:	straight wall gold bump
Bump size:	22.5 x 22.5 x 20mm
Lead material:	ED copper
Lead plating material:	immersion tin with 0.4 μm thick

Bonding Process

Inner lead bonds(ILB) were obtained by gang bonding. The bonder first picked up a die onto the stage for pre-heating. Almost at the same time, a TAB tape was moved to bonding position for pattern recognization and lead location check. The thermode was then slowly move down onto the lead. Heat and force were supplied by the thermode to the leads and bumps. The liquid tin reacted with solid gold to form Au/Sn alloy by the action of the temperature and pressure during the bond time. The alloy solidified after the heat and the force was released. The most critical bonding parameters of the bonding process are bonding temperature, bond pressure as they determine the final integrity of ILBs.

In order to investigate the dynamic influence of bond temperature and bond pressure on the formation of microstructures of the ILBs, we only varied both of the parameters, while the stage temperature for pre-heating and the bond time were kept constant at 0.5 second and 150°C respectively. Preliminary studies indicated that stage temperature and bond time have little effect on degradating the quality of the bonds.

Table II. Bonding Parameters Setting

Setting	Bonding temperature / °C	Bonding pressure /unit
A	370	30
B	395	25
C	420	20
D	470	10
E	520	0
F	420	0
G	520	20

The applied thermode temperature were set within the range 370°C to 520°C.

Since the bond force required for bonding may vary as the number of lead beams and the contact area of the thermode on individual lead are changed for different manufacturers or bonders, we only present the variations of the pressure (the force applied divided by the contact area of the thermode and the lead) applied to each lead in a relative sense of arbitrary unit. The range of the thermode force applied in our investigation, 10cN/pad to 40cN/pad, has been used successfully by previous researcher[4] for inner lead bonding.

The variations of the bonding parameter setting is illustrated in Fig. 1. The applied pressure decreased as the bonding temperature is increased. The setting is named in alphabetical order with decreasing bonding pressure and increasing temperature except setting F & G. ILBs were bonded according to the setting.

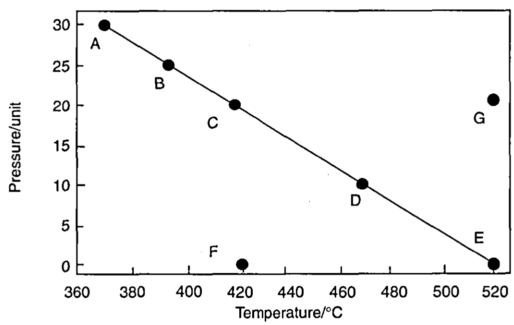


Fig. 1 Variations of bonding parameters.

Analytical Method

Metallographic examination techniques were used to investigate the microstructures and integrity of the formed ILBs. Samples of the TAB components bonded at different parameter settings were mounted using low temperature curing epoxy resins. Normal grinding and polishing procedures were followed to obtain a smooth surface for further analysis.

The micro-sectionings of samples were then examined by a Scanning Electron Microscopy(SEM) which was operated in conjuction with a Back-scattered electron(BSE) detector. The microstructures and the phases were revealed by the detector. The observed phases were identified by an Energy Dispersive X-ray(EDX) Spectroscopy Since the dimensions of ILBs was so small, it was difficult to determine the exact composition of the phases. Thus only semi-qualitative analysis was carried out.

From the obtained micrographs, the deformation characteristics of the formed ILBs were hence determined. The strain of each parameter setting were estimated by comparing the dimensional changes of the leads and bumps.

Parallel to the metallography examination, mechanical lead pull test was carried out to access the quality of the ILBs. The adhesion strength of the contact interface is indicated by the averaged lead pull test values. The failure modes of the test were also used to interpret the data recorded.

RESULTS AND DISCUSSION

Thin Tape Metallization

Reduced tin-plating was used to form ILBs to check the possibility of obtaining reliable bonds. 0.4 μm thick tin was plated on ED copper lead beams instead of 0.5 μm with low roughness. As indicated in Fig. 2, ILBs bonded at various bonding parameter settings have acceptable lead pull values. Besides, the observed failure mode of all the settings is lead break. These directly show that all the ILBs have sufficiently high strength and this adhesive strength of the bonded interface is higher than the fracture strength of the copper lead which is explained by wire theory[5].

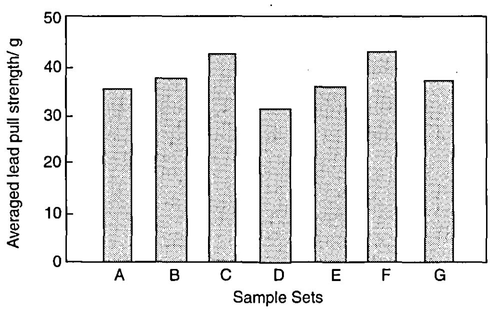


Fig. 2 Averaged lead pull strength of ILBs bonded at various settings.

Since the metallization of the lead beams was reduced, there was limited free tin available for Au/Sn bonding. This not only limited the formation of Au/Sn alloy at the gold-rich region or at the left portion of the Au-Sn phase diagram (Fig. 3) but also excluded the formation of two brittle intermetallic compounds: AuSn2(ε phase) and AuSn4(η phase). However, the formation of the Cu/Sn intermetallic compounds, Cu_3Sn and Cu_6Sn_5, between the tin-plating and the copper lead may reduced the shelf life of the leads and free tin available for alloying as they have relatively high rate of formation at room temperature and form even more rapidly at higher temperature.

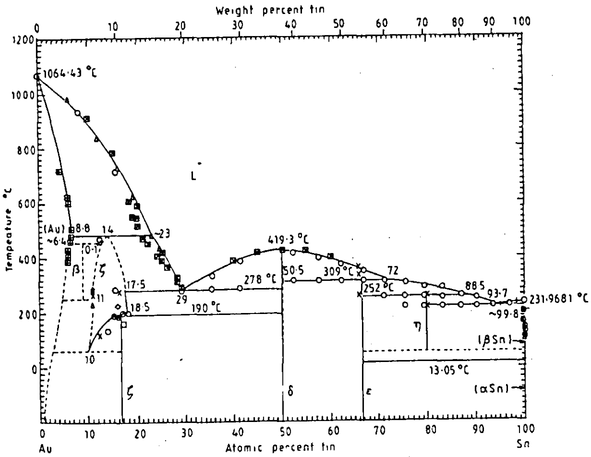


Fig. 3 Au-Sn equilibrium phase diagram [2].

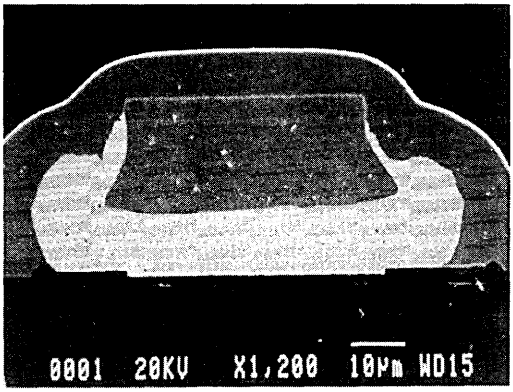
Microstructural Variations

In order to study the bonding mechanism, the microstructures and the alloy composition, samples bonded at different bonding parameters were cut into cross-sections and longitudinal sections. Fig. 4 (a) and (b) show the typical micrographs of the micro-sectioning. They were examined by a back-scattered electrons (BSE) detector in operating with a scanning electronic microscope(SEM) to differentiate the compositional differences of the microstructures.

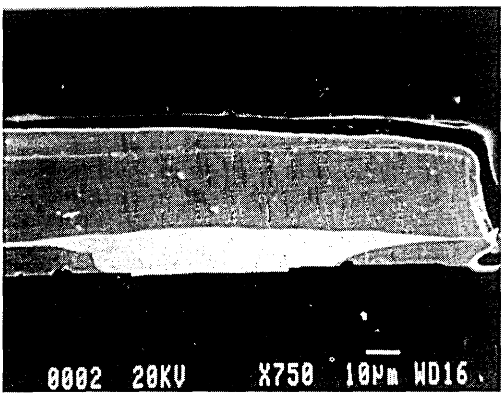
It is observed that ILBs bonded at setting A & B exhibit the same microstructural features. Fig. 5 shows the BSE image of the cross-section of the ILBs bonded at setting A. Rather uniform contact interface was observed with thickness less than 1μm. As we can see, the contrast of the BSE image indicate that the interfacial layer has higher Sn content than the gold-rich eutectic compositon(70 at.%Au, 30 at.% Sn). This alloy did not wet the adjacent Cu-lead beam. Extensive accumulation of eutectic Au/Sn(70/30 at.%) alloy was also found at the contact interface as illustrated in Fig. 6. Cracks were also observed to be initiated from those region.

It should be pointed out that the eutectic Au/Sn found outside the contact interface has two distinguish structures. From Fig. 7(a), it is observed that rather regular coarser columnar layer and fine lamellar co-exist. EDX results indicate that these two structures has the same composition 70 at.% Au and 30 at.% Sn. Thus these phases are identified as eutectic Au/Sn alloy. Formation of eutectic Au/Sn lies on the fact that molten tin flow to the joint region and react with solid gold-bump forming a pool of Au/Sn alloy of eutectic composition and then solidified. The lamellae tend to grow perpendicular to the liquid-solid interface and its spacing would probably adjust so as to minimize the undercooling at the interface. The case is similar to the well known casting-metal structure. The dommed layer between the gold bump and the columnar eutectic was identified as ζ phase with 15 at.% Sn.

A layer of ternary Au/Sn/Cu intermetallic was found at the copper lead beam. For the thickness of the layer is out of the detection limit of EDX, the composition of the compound was not determined. However, it is belief that it is due to the preference of diffusion of Cu atoms to eutectic Au/Sn region to form ternary Au/Sn/Cu intermetallic compounds[4]. The growth of this intermetallic layer is highly temperature dependent.



(a)



(b)

Fig. 4 (a) Cross-section micrograph of ILB.
(b) Longitudinal-section micrograph of ILB.

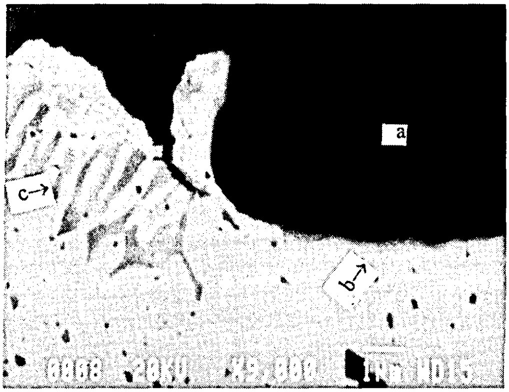


Fig. 5 BSE image of the cross-sectional view ILB bonded at setting A. (a)CU-lead beam b) contact interface c) eutectic region. The thickness of the interface is less than 1µm. The contrast of the image indicate that the layer may have higher Sn content than the eutectic phase(30 at.% Sn).

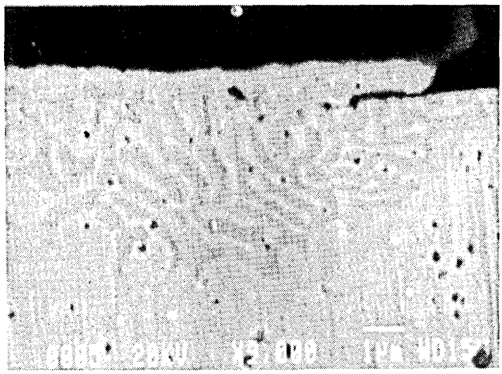
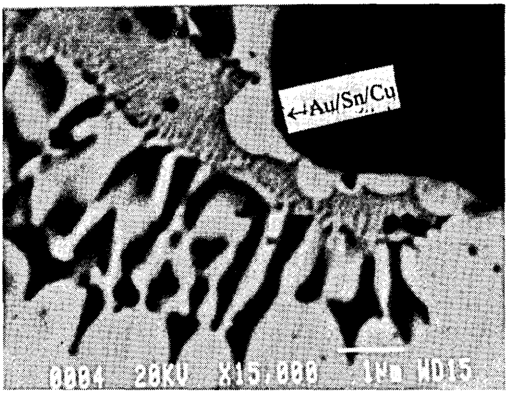


Fig. 6 Cross-sectional SEM micrograph show the accumulation of the eutectic Au/Sn at the contact interface and the initiation of a crack from that region.

Besides the cross-sectional evaluation of the ILBs, longitudinal-section metallographic examination was employed. Fig. 8 (a) show the network structure of the alloy accumulated at the heel. The alloy does not wet the copper lead beam. EDX measurements identified it is a mixture of AuSn (50 at.% Au & 50 at.% Sn) intermetallic or δ phase and gold-rich eutectic (70Au/30Sn at.%). This mixture was observed accumulated at the interface (Fig. 8(b)). Non-uniform interface and cracks were found within the region. Fig. 9 (a) and (b) depict the BSE images of the microstructure of setting A found at the heel and outside the contact interface respectively.

The copper lead beam and the gold bump bonded at setting A & B remain rigid after bonding, i.e. undeformed, as indicated by the strain measurements of the ILBs (Fig. 10). Thus the strength of AuSn phase and gold-rich eutectic mixture which made up the bonded zone determined the interfacial strength of the ILBs. Moreover, the beam and the bump could be deformed if the applied pressure is increased.

(a)

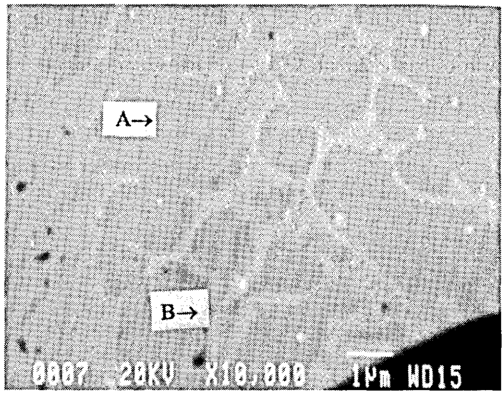


(b)

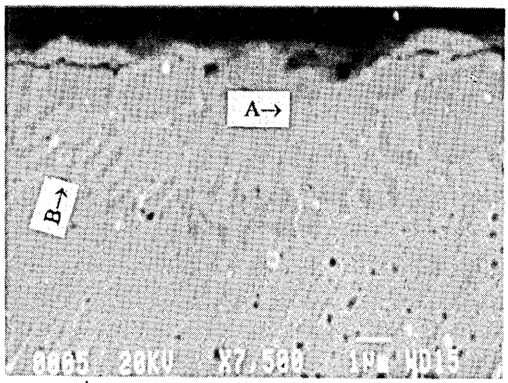
Fig. 7 (a) Microstructure of the accumulated eutectic Au/Sn outside the contact interface. The content of the eutectic phase is 70 at.% Au and 30 at.% Sn. Two distinguish structure of Au/Sn co-exist. They are A) coarser Au/Sn eutectic layer(0.5µm/layer) and B) fine Au/Sn lamellar(0.1µm/layer). The dark region is tin-rich while the lighter one is gold rich. C)ζ phase is found at the perimeter of the gold bump with 15 at.% Sn.

(b) A closer look on the interface. Au/Sn/Cu ternary intermetallic formed at the Cu-beam caused by the diffusion of Cu-atoms to the eutectic Au/Sn zone.

As the bonding temperature exceeded 420°C, the wetting behavior of the formed Au/Sn alloy was observed to be improved as the bonding temperature was increased. The microstructure of the fillet of setting C, D & F was determined to be gold-rich eutectic Au/Sn. No AuSn phase was found as it melts at 419.3 °C. While, for setting E & G, the bonding temperature was 520°C, meniscus of mixture of fine lamellae and small grains are observed. Fig. 11 shows the cross-section of ILBs bonded at setting E. EDX results indicated that the fine lamellae of random orientation has the eutectic Au/Sn composition(70/30 at.%) and the grains has 84 at.% Au and 16 at.% Sn. These two phases hence identified as eutectic Au/Sn and z phase respectively. Indicated by the Au-Sn phase diagram, peritectic reaction $[L + \beta(Au_{10}Sn)] \leftrightarrow \zeta$ occurs at 521 °C [2]. This reaction is likely to happen as the bonding temperature closed to the reaction temperature and with sufficiently high content of gold. This explain the formation of grains of z phase within the eutectic alloy and is termed as hyperetutectic structure.



(a)

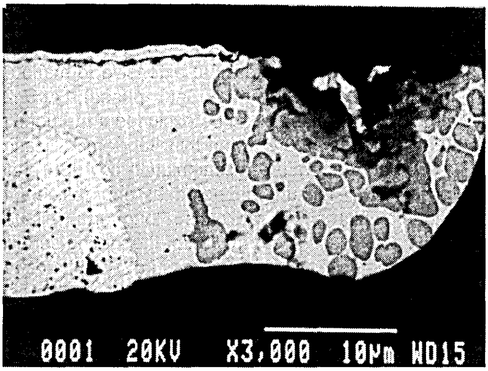


(b)

Fig. 8 (a) Longitudinal-section of ILB bonded at 395°C (SE image) showing the network like structure of the Au/Sn alloy accumulated at the heel. There are 2 phases: A) AuSn (50/50 at.%) phase and B) eutectic Au/Sn (70/30 at.%)

(b) A) AuSn(50/50 at.%) intermetallic and B) eutectic Au/Sn (70/30 at.%) at the contact interface. Cracks are observed to be initiated from the region of AuSn intermetallic.

From Fig. 14 and Fig. 15, we can see that the gold-bump undergone plastic deformation at the perimeter of gold bump. It is obvious to see that the bump deformed by means of grain-boundary sliding under the action of bonding temperature and pressure. More gold solid solution dissolved into the liquid tin, which favored the forming of ζ phase during cooling. Random lamellae formed as solidification. Same kind of microstructures were found at longitudinal sections of the bonds. Due to the effects of high bonding temperature of the settings, thicker layer of ternary Au/Sn/Cu intermetallic compound was expected and was actually observed (Fig. 16). It is well known that the rate of diffusion of Cu is a function of temperature and thus the formation of the ternay intermetallic.



(a)

(b)

Fig. 9 BSE images of the mixture of AuSn phase and eutectic phase found at (a)the heel (b)the adjacent of the lead beam of ILBs bonded at A.

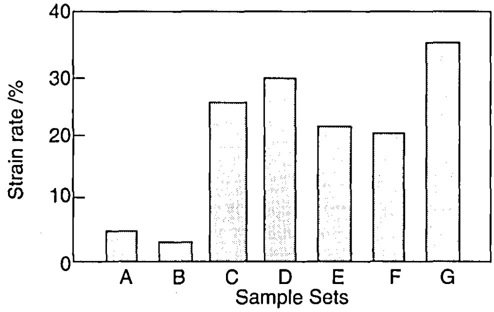


Fig. 10 Strain rate of the ILBs bonded at various setting.

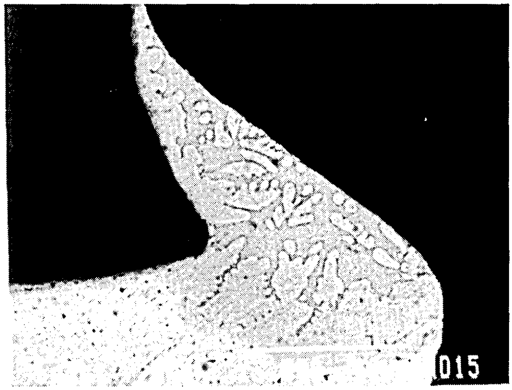


Fig. 11 BSE image reveals the Au/Sn alloy formed at the fillet. The formed meniscus is composed of fine lamellar eutectic Au/Sn and gains of ζ phase with 16 at.% Sn.

Fig. 12 A close look on the meniscus (BSE image) show the fine lamellar Au/Sn grew from different cooling cores and grains of ζ phase formed in the direction bump deformation.

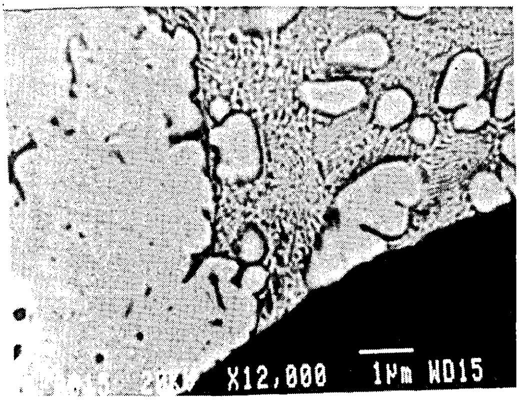


Fig. 13 BSE images of longitudinal-section show the meniscus formed at the heel of setting E.

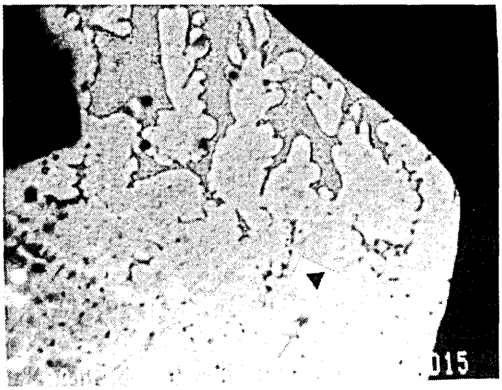


Fig. 14 BSE images shows cross-sectional view of the ILB bonded at setting E. The contrast of the BSE image indicate the diffusion of the Sn atoms to that region through grain boundaries. The Sn content at that region is 11 at.%.
(X6000)

Deformation

As the bond pressure used for setting C, D,E, F & G were all less than setting A & B, the deformation of ILBs are obviously due to the influence of the increasing temperature. Temperature has the predominant role of initiating the deformation of both Cu lead beam and gold-bump. As the bonding temperature increased, more energies are available for the bonding process and for the deforming process. In co-operation with the applied pressure, molten tin was squeezed out with little remaining on the contact interface which facilitate the joining of the interface. The possible bonding mechanism was identified as the interdiffusion of matters of the bonded regions, plastic deformation of surface asperities and power law creep deformation[6]. Therefore, plastic deformation of the surface of Cu lead and Au-bump has the effect of pushing excess molten tin out of the bonded zone. Fig. 17 (a), (b) and (c) show the BSE image of the interfaces of ILBs bonded at setting C, F and G respectively. In addition, this flow would certainly help to wet the alloy to the beam lead. Thus no accumulation of Au/Sn alloy at the interface occurs once deformation has been initiated. However, if temperature and pressure applied further, bulb deformation may result and lead to the degradation of Cu lead beam and gold-bump, that is the case of setting D (Fig. 18).

By comparing the results of strain measurement and lead pull test, highest and lowest pull test values are obtained which are corresponding to the deformation of ILBs at 25% and 30%. It suggest that the bulb deformation occurs as the strain exceed 30%.

The influence of Bonding Temperature and Pressure

In order not to causing any kinds of damaging to the component devices during inner lead bonding, the bonding temperature and pressure should be kept as low as possible. The results obtained so far indicated that extensive formation of Au/Sn intermetallics, including AuSn(δ phase), AuSn2(ε phase) and AuSn4(η phase), can be excluded if the bonding temperature exceeds 420°C with thin tape metallization. While below that temperature, accumulation of AuSn phase and eutectic Au/Sn mixture observed at and outside the bonded zone, which intuitively cause long-term reliability problem. Besides, plastic deformation of the mating surfaces can also be obtained with reducing pressure. The microstructure of the fillet formed at the heel and adjacent to the lead beam is found to be gold-rich eutectic with good and easy wetting to the beam lead. Hypereutectic structure, i.e. mixture of gold-rich eutectic Au/Sn and ζ grains, is obtained as the bonding temperature exceed 470°C. However, the rate of formation of ternary Au/Sn/Cu intermetallics is accelerated due to the increased bonding temperature may lead to long term degradation problem.

It is evident that for TAB Au/Sn eutectic inner lead bonding, bonding temperature is responsible for determining the metallurgical structure of the bonded zone and deforming the contact interfaces with the assistance of applied pressure. The growth of binary An/Sn intermetallic compounds and ternary Au/Sn/Cu intermetallics can be limited by optimizing the bonding temperature within the range 420°C and 470°C. Excellent wetting can also be achieved. The optimum deformation was found to be at 25% strain rate of highest lead pull strength, which indicate that the bonding pressure is sufficient to deform the bonded interfaces without causing bulb deformation.

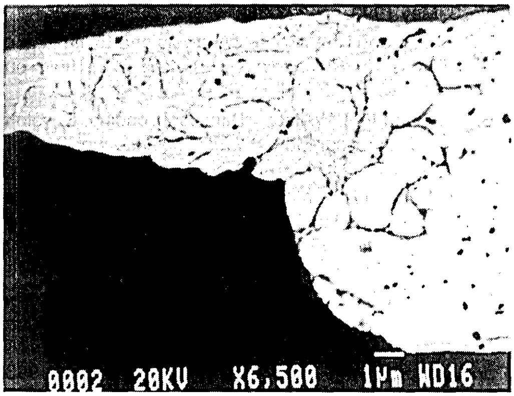


Fig. 15 BSE images of the heel of the ILBs bonded at setting E.

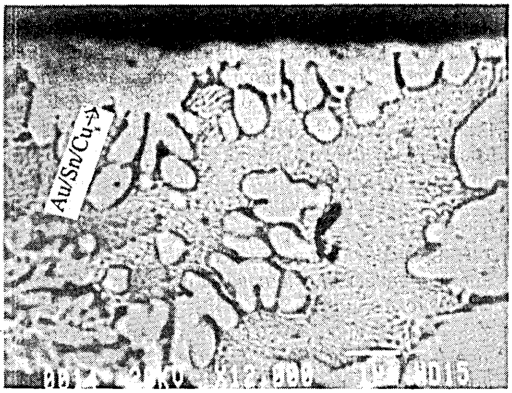
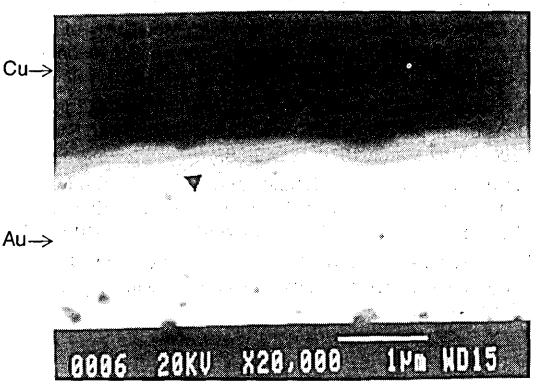
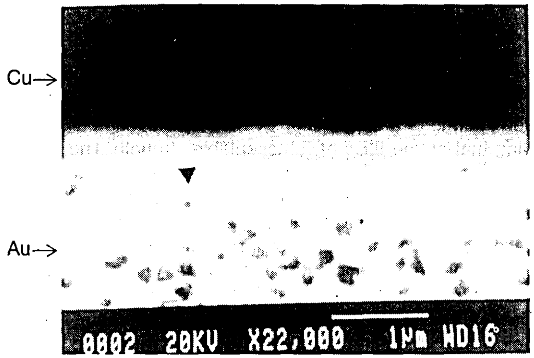


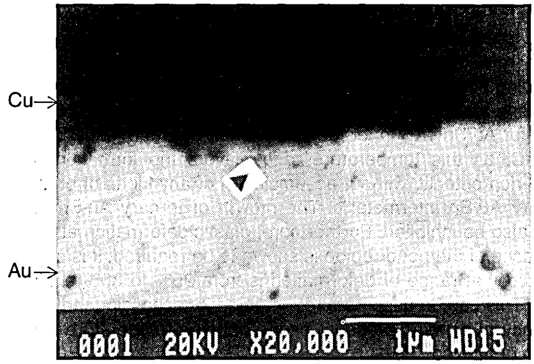
Fig. 16 BSE images of longitudinal-section show ternary Au/Sn/Cu intermetallic formed under the lead beam and grew in the direction of the applied temperature gradient. The content of the ternary phase is 52 at.%Au, 13 at.%Sn and 35 at.%Cu.



(a)



(b)



(c)

Fig. 17 BSE images of the interfacial layer formed at setting a) C, b) F and c) G. The micrographs indicate that the higher the applied pressure, the thinner is the interficial layer.

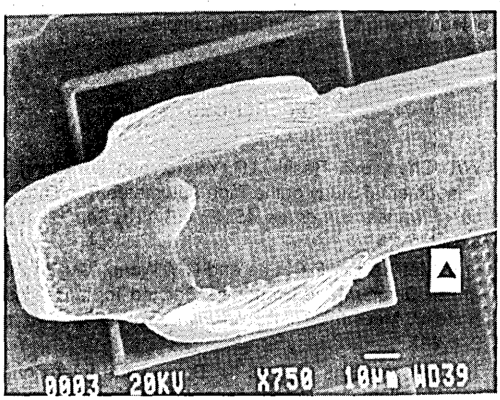


Fig. 18 SEM photograph show the cracks formed at the ILBs bonded at setting G.

CONCLUSION

Reduced tape metallization, 0.4 μm tin-plating, was used to form ILBs in our investigation. The adhesive strength of the bonded interface were examined by mechanical lead pull test showing that all the ILBs have acceptable strength. The failure mode is lead break. The strength of the bonded interface is higher than the fracture strength of the ED copper lead beam. By means of micro-sectioning and metallographic examination, the microstructures of the formed Au/Sn system were investigated. The microstructures of the Au/Sn alloy fillet was a mixture of AuSn intermetallic phase & gold-rich eutectic(70at.%Au & 30at.%Sn) as the bonding temperature was set below 420°C, desirable gold-rich eutectic with good and easy wetting was obtained as bonded in between 420°C and 470°C and a mixture of ζ grains & the eutectic, i.e. hypereutectic composition, was found at 520°C.

It is evident that bonding temperature take the predominant role of establishing the metallurgical structure while bonding pressure assists the plastic deformation of the bonded zone and aids the wetting. The optimum bonding temperature for Au/Sn TAB inner lead bonding is between 420°C and 470°C, as this temperature range favors the formation of gold-rich eutectic without accumulation of any kinds of brittle binary Au/Sn intermetallic. The growth of ternary Au/Sn/Cu can also be inhibited. Furthermore, plastic deformation at the surfaces of the bond region is shown to be required. It is suggested that range of deformation is from 25% to 30% strain rate. This can be used as a rough guide for accessing the adequacy of bonding pressure as the bonding temperature has been optimized.

ACKNOWLEDGEMENTS

The authors would like to express their gratitude to Dr.L.M.C.Wu in City University of Hong Kong for his useful discussion, Caety Tse and Alfred Ho in Motorola Semiconductors H.K. Ltd. for their supports on preparing the TAB components, T.F. Hung and K.F. Liang in MTU of City University of Hong Kong for coating SEM samples.

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Testing LCD Drivers in TAB package

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Contact method for testing TAB package

Owing to the special nature of the TAB package[1], traditional contact method for rigid body packages, such as PLCC and QFP, cannot be used. A different kind of interface should be used between the handler and the test system.

The most commonly used interfaces are probe card and conductive rubbers.

Probe Card

What is probe card

Probe card, in simple words is a PCB board with probes attached in which matches the pin layout of the TAB package under test.

The probe card in Fig. 1 is an Epoxy Ring Type probe card. It is composed of four parts which are:

1. Probe/Sensor
2. Ring
3. Epoxy
4. Printed circuit board

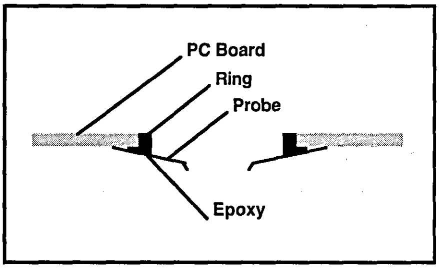


Fig. 1 Epoxy Ring Type Probe Card

The most important parameter within a probe card should be the material of the probes. The material used contributes directly to the contact resistance and the life of the probe card. Three commonly used probe materials are listed below[2]:

1. Tungsten

The most widely used. Exhibits excellent fatigue resistance but higher contact resistance over use due to aluminum oxide build-up on the probe tip. Requires periodic sanding with ceramic wafer.

2. Beryllium Copper

Recommended for high speed high or low power devices because of its lower contact resistance but has a much shorter life than tungsten.

3. Palladium

Recommended for gold pad. Shows stable contact resistance but has a much shorter life than the above materials.

As a result, which material should be used depends upon which device is under test. Below is a table of their characteristics:

CHARACTERISTICS	MATERIALS		
	Tungsten	BeCu	Palladium
Volume Resistivity ($\mu\Omega$cm at 20°C)	5.7	6.8	34.2
Modulus of Elasticity (kg/cm^2)	4.13×10^6	1.33×10^6	1.18×10^6
Hardness (Rockwell C)	7.0	3.0	4.8

[1] The TAB mentioned here is of reel to reel type.

[2] From JEM America Corp.

REV 0
9/96

Conductive Rubber

Conductive Rubber is a collective name for many silicone base "rubber" with conductive materials embedded within. Below are two commonly used conductive rubber: PCR and MOE.

What is PCR

The full name of PCR is Pressure Conductive Rubber. Fig.2 shows a piece of PCR together with its cross section. As seen from the figure PCR looks like a TAB unit with special windows which match the pins on the TAB unit. Within the windows are contact areas, silicone, filled with conductive particles, usually nickel. Once under pressure, current can go through those particles and thus the material conducts.

Below is a table of its characteristics:

Contact Resistance	150 mΩ
Current Carrying Capacity	500mA
Substrate Material	Nickel
Life Time	10000 contacts (30% shrinkage)
Resistivity between conduction areas	10^6 Ω
Temperature Tolerance	-55°C to 150°C

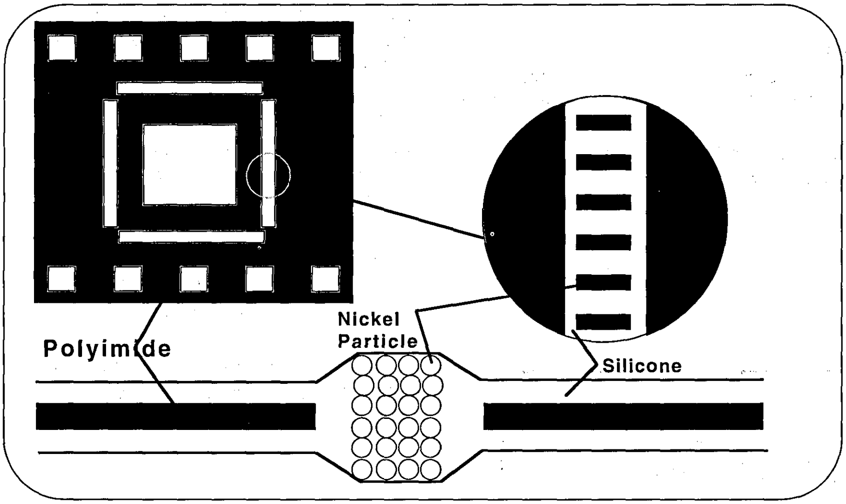


Fig. 2 Pressure Conductive Rubber (PCR)

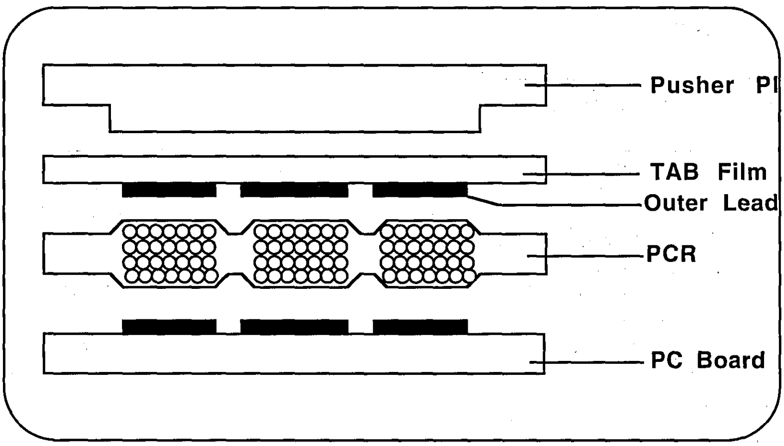


Fig. 3 Application of PCR with TAB

Fig. 3 shows a simplified diagram on the application of PCR. The PCR is placed in between the unit and a PC board. A pusher plate is then placed over the TAB unit to apply pressure in order for the PCR to conduct.

What is MOE

The full name for MOE is Metal On Elastomer. Fig. 4 shows a diagram for a MOE strip. As seen from the diagram, MOE consists of metal traces inserted precisely within electrically insulated silicone rubber to allow conduction in the z-axis. The substrate of the metal traces is usually gold.

Fig. 5 shows a typical application of MOE. Noticed that a special socket housing is needed to allocate the MOE strips. The TAB unit, when placed on top of the socket, can then make contact with the PC board through the MOE strips.

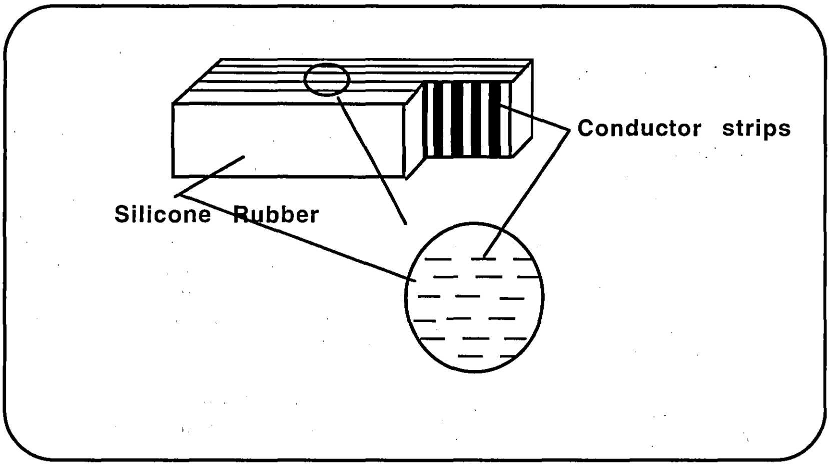


Fig. 4 Metal On Elastomer

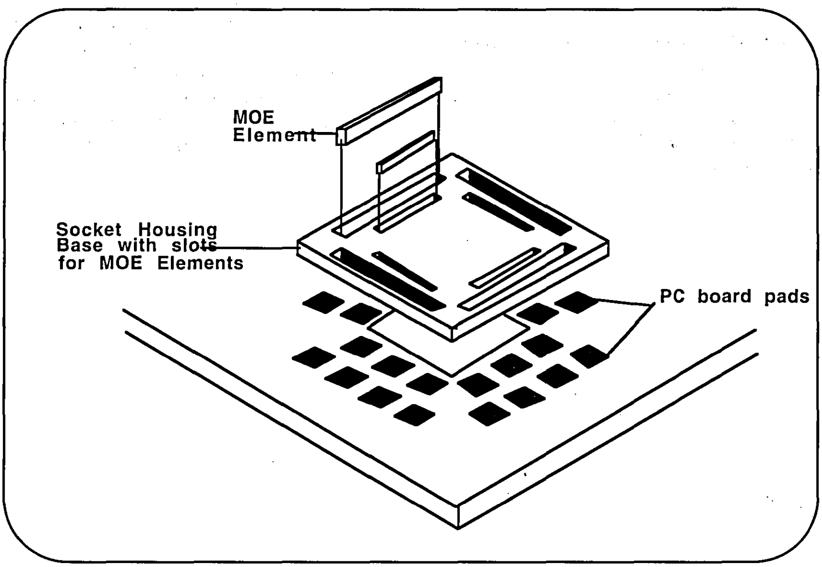


Fig. 5 A typical application of MOE

Below is a table of its characteristics:

Contact Resistance	0.005 Ω
Current Carrying Capacity	3 A
Substrate Material	Silicone rubber
Trace Metallurgy	Gold
Temperature Range	-45°C to150°C
Dielectric constant	3.0
Resistance between traces	10^{12} Ω

Drawbacks of Probe Card and Conductive Rubber methods

One of the advantages of TAB lies in its freedom of pins layout. It will be quite difficult for conductive rubber type of contact to apply on an irregular shaped TAB package due to the high cost for developing the tooling. For conductive rubber each different layout needs a different tooling for the conductive material and sockets. The costs for that would be high.

In addition, owing to their "rubber-like" nature, frequent cleanings are required or the contacts will be contaminated.

Probe card, on the other hand, has complication in maintenance. Besides periodic cleaning of probes, there will be times that the probes will be damaged. Repairing of probes depends totally on the skillful workmanship together with a special repairing station.

Advantages of Probe Card over Conductive Rubber for Mass Production

Despite the above drawback on probe cards, they suit the irregular shaped TAB very well because the probes are laid by human hands. The costs of probe cards are thus comparatively lower than that of conductive rubbers.

Another side advantage of probe cards is that the probes can induce slight scratches on the test pads when pressure is applied. This allows better contact during testing because the probes can scratch away the oxide which may form on the test pads. Probe cards can also handle finer pitch TAB units than conductive rubbers.

As for LCD drivers, which are mixed-signal devices, a controlled impedance test fixture can reduce much noise influences. To achieve that, we want to minimize the layer of contacts from handler to tester. Probe cards with probes built right on the PC board can meet this requirement. Conductive rubber, on the contrary, increases the layer of contacts.

Precautions during testing TAB LCD

ESD protection

No matter what type of method you use to test TAB packaged devices, ESD will be generated due to the nature of the package itself. Besides any usual ESD precautions, ionizers should be installed along the path of the TAB device tape. TAB package can generate as high as 10 kilo volt ESD under a non-ionized environment.

Signal Distortion

LCD drivers are mixed-signal devices which have their own distinctive test problems from those of digital or analog signal devices. Fixturing, or the connection between the test hardware and the device under test (DUT), contributes to this in the form of noise, crosstalk, and corruption of signal integrity. Grounding shields separating the digital and analog signals can assist in maintaining signal integrity. Proper decoupling of the power sources can reduce noise. Suitable design of interface between the device and the test system can also minimize crosstalk[3].

[3] Electronics Engineering, Feb 1994, Vol. 7 Number 10, Joseph A. Mielke, pp 104-107

Glossary 7

Abbreviations

ACF	Anisotropic Conductive Films.
BP	Backplane
COB	Chip On Board
COG	Chip On Glass
DKAT	Dragonkat
ILB	Inner Lead Bonding
LCD	Liquid Crystal Display
MUX	Multiplex
OLB	Outer Lead Bonding
SEG	Segment
STN	Super Twisted Nematic
TAB	Tape Automated Bonding
TCP	Tape Carrier Package
TFT	Thin-Film Transistor
TN	Twisted Nematic

Glossary

ACF
It is for connecting LCD drivers in TAB directly to LCD glass.

Active / Passive
Active (TFT) and Passive (STN) are two categories of LCD technology.

Announciator
Name for the static icon display commonly found on pager application.

BP / Backplane / Row / Common
Horizontal rows in a matrix LCD display.

Bias Levels
Bias = 1 / (√ MUX + 1). It defines the voltage values should be obtained in a voltage divider in order to obtain an optimum contrast for LCD panel.

COG
Chip on glass. The gold bump die directly bond to the LCD panel glass by ACF

DKAT Dragonkat
Motorola's Dragonkat is a MCU Family of C05 core where:
DKAT IMC68HC05L9 + MC68HC68L9
DKAT I +MC68HC05L10 + MC141511A
DKAT IIMC68HC05L11 + MC141512 & MC141514

Gold Bump Process
The unique gold bump technology of Motorola is an Industry leader. Our "Straight Wall Bumps" enable us to use finer spacing of leads and optimum chip sizes.

ILB / Inner Lead Bonding
Process of bonding a die to a TAB.

LCD / Liquid Crystal Display
One of the electronic display technologies.

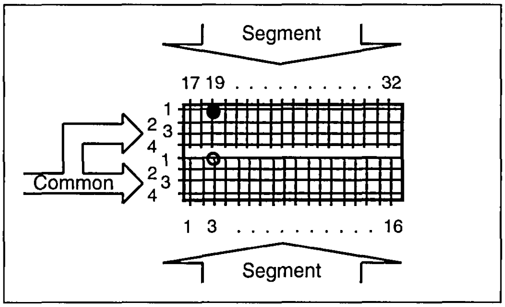
SEG / Segment / Column
Vertical rows in a matrix LCD display.

MUX Multiplex
The multiplex ratio (MUX ratio) is defined as 1: N, where N is the number of Backplanes / Common. It is one of the key factor in defining a LCD Driver.

OLB / Outer Lead Bonding
Process of bonding TAB to LCD glass either directly with ACF or indirectly with heat seal connectors.

POCSEC™
POCSEC™ stands for Pocket Secretary. It represents a chip set where a complete solution of a pen-based, multi-features organizer is provided.

Split Panel
It is a LCD panel which doubles the number of rows with the same MUX ratio by allowing addressing of two segments with one Common signal.



e.g. Point o is of segment 3 and
Point ● is of segment 19, they are both addressed by Common 1.
(MUX ratio is 1: 4 in this example, display size is 8x16)

TAB Tape Automated Bonding /
TCP Tape Carrier Package
A film like package of polyimide substrate with copper leads.

TFT / Thin-Film Transistor
An LCD technology applied in active matrix display.

TN / Twisted Nematic / STN / Super Twisted Nematic
Basic Passive LCD Technologies.

VLCD
LCD driving voltage.

Handling and Design Guidelines 8

Handling and Design Guidelines

HANDLING PRECAUTIONS

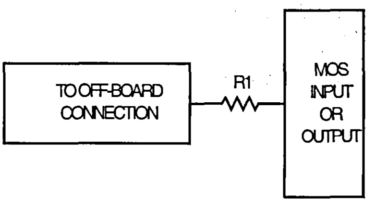
All CMOS devices have an insulated gate that is subject to voltage breakdown. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

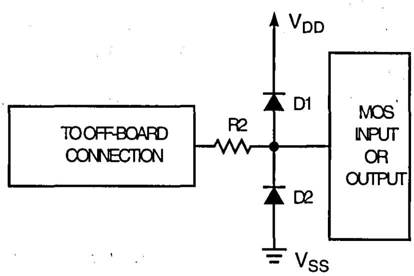
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or devices is merely an extension of the device and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

Figure 1. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility



Advantage: Requires minimal board area.

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:

A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 - PROPAGATION DELAY VS. SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 0.7 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

EQUATION 2 - RISE TIME VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 2.3 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.

RECOMMENDED READING

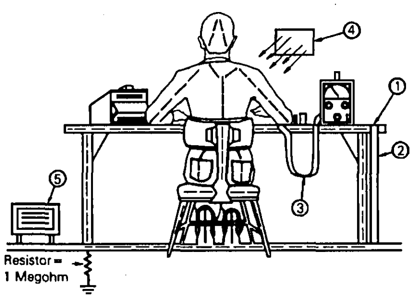
"Total Control of the Static in Your Business"
Available by writing to:

3M
Static Control Systems
Building A145-3N-01
P.O. Box 2963
Austin, TX 78769-2963

Or calling:

1-800-328-1368

Figure 2. Typical Manufacturing Work Station



NOTES:
1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than - 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Ensure that inputs and outputs are limited to the maximum rated values, as follows:
   $-0.5 \le V_{in} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $-0.5 \le V_{out} \le V_{DD} + 0.5$ Vdc referenced to V_{SS}
   $|I_{in}| \le 10$ mA
   $|I_{out}| \le 10$ mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values (see Figure 1).
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of I_{in} = 10 mA (see Figure 1).
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

Figure 3. CMOS Wafer Cross Section

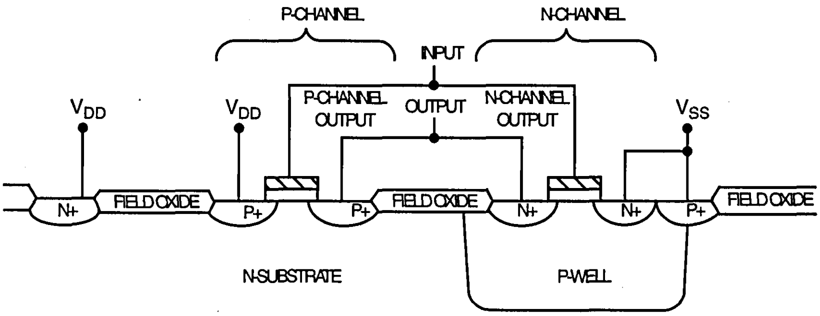
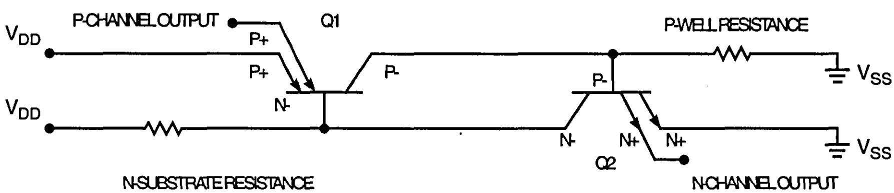


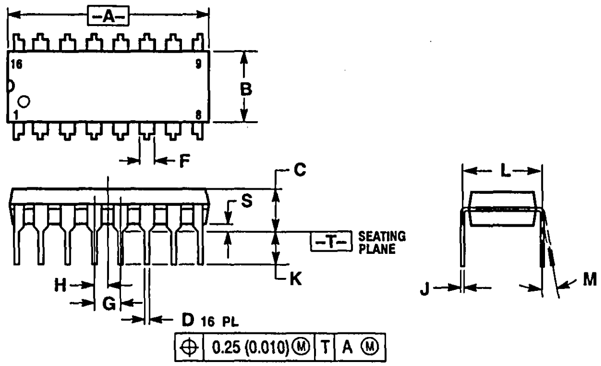
Figure 4. Latch Up Circuit Schematic



Mechanical Data 9

Package availability for each device is indicated on the front page of the individual data sheets.
Dimensions for the packages are given in this chapter.

P SUFFIX
PLASTIC DIP (DUAL IN-LINE PACKAGE)
CASE 648-08

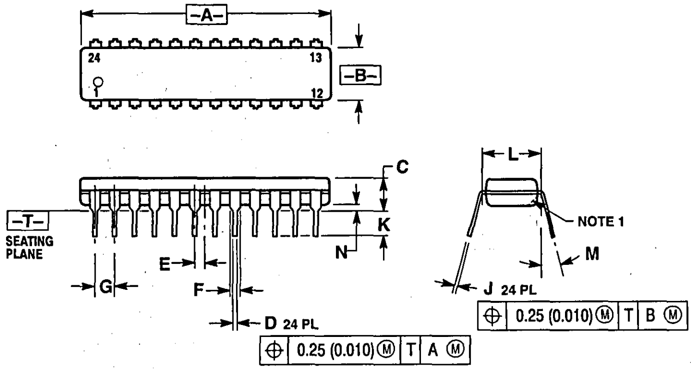


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

STYLE 1:		STYLE 2:	
PIN 1.	CATHODE	PIN 1.	COMMON DRAIN
2.	CATHODE	2.	COMMON DRAIN
3.	CATHODE	3.	COMMON DRAIN
4.	CATHODE	4.	COMMON DRAIN
5.	CATHODE	5.	COMMON DRAIN
6.	CATHODE	6.	COMMON DRAIN
7.	CATHODE	7.	COMMON DRAIN
8.	CATHODE	8.	COMMON DRAIN
9.	ANODE	9.	GATE
10.	ANODE	10.	SOURCE
11.	ANODE	11.	GATE
12.	ANODE	12.	SOURCE
13.	ANODE	13.	GATE
14.	ANODE	14.	SOURCE
15.	ANODE	15.	GATE
16.	ANODE	16.	SOURCE

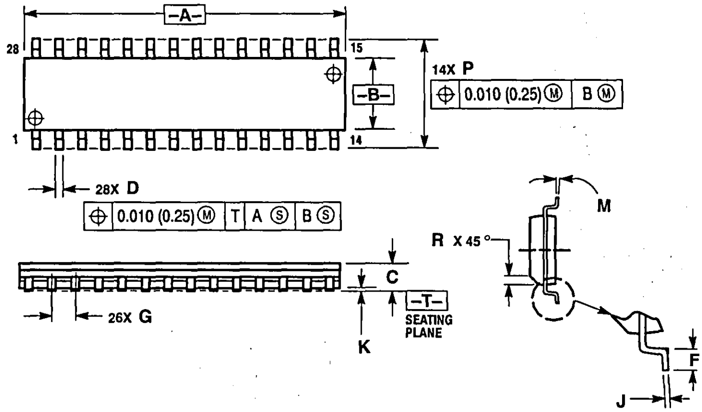
P SUFFIX
PLASTIC DIP (DUAL IN-LINE PACKAGE)
CASE 724-03



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

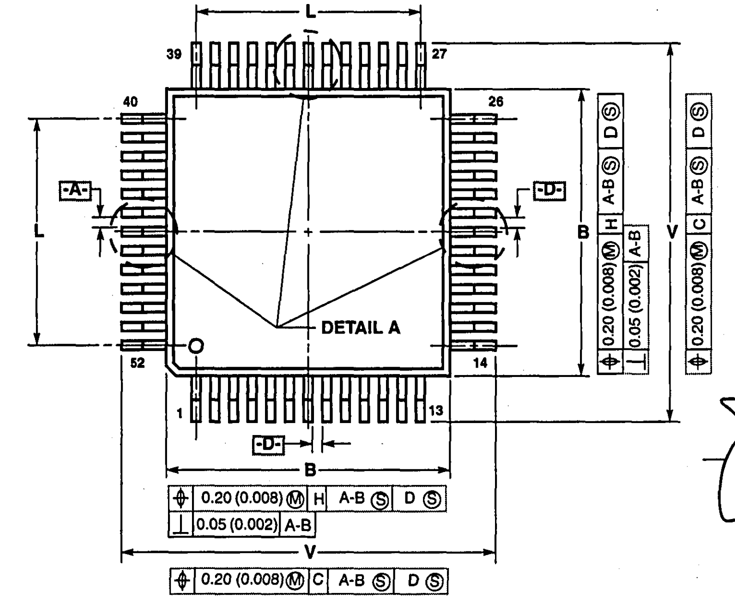
DW SUFFIX
SOG (SMALL OUTLINE GULL-WING) PACKAGE
CASE 751F-04

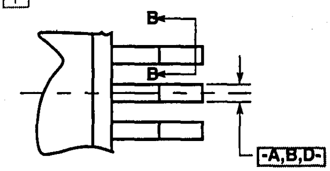


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

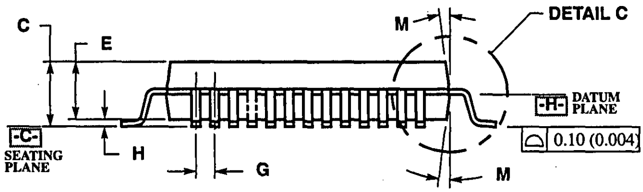
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

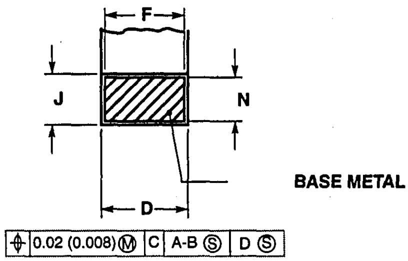
FU SUFFIX
QFP (QUAD FLAT PACKAGE)
CASE 848B-04



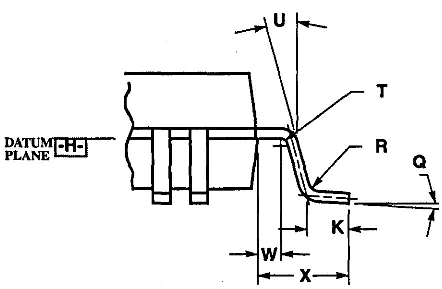


DETAIL A





SECTION B-B



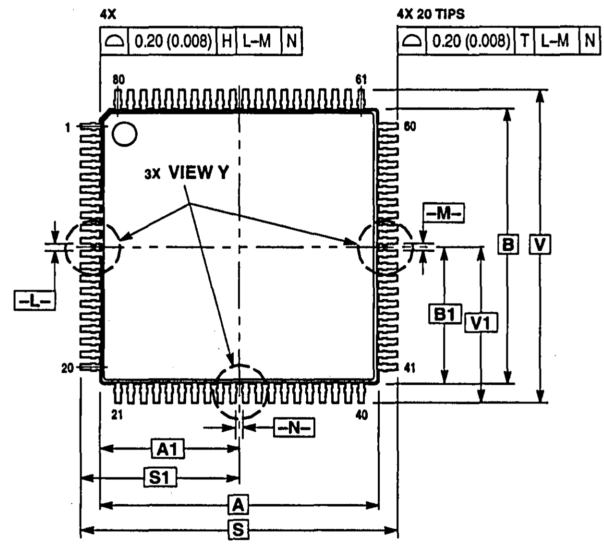
DETAIL C

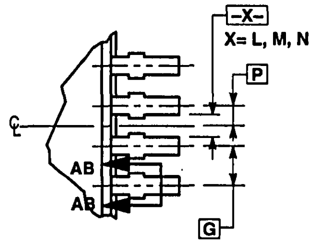
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

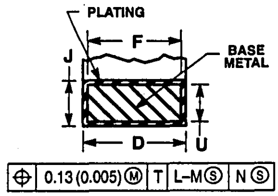
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	--	0.25	--	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	--	0.005	--
U	0°	--	0°	--
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

FJ SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 917A-02

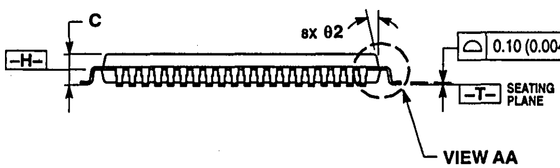


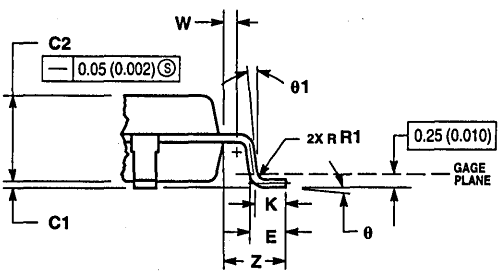


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE



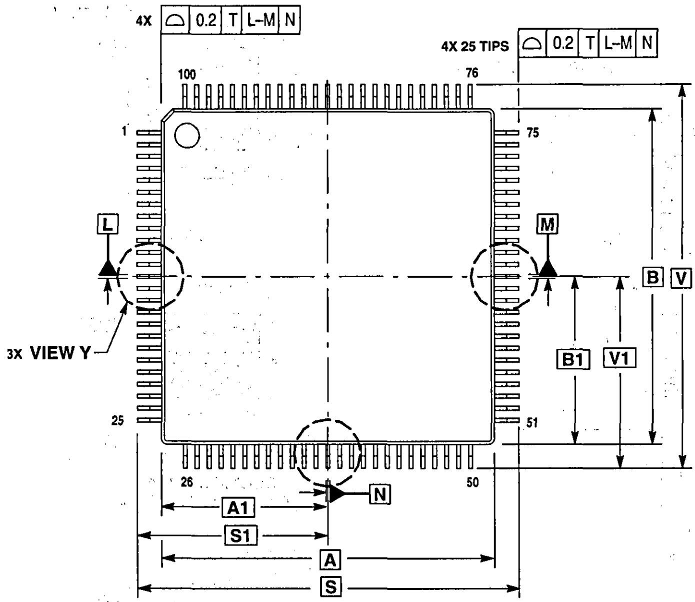


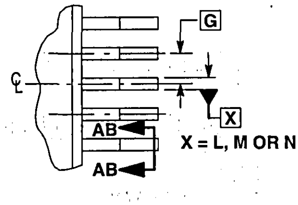
VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.460 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

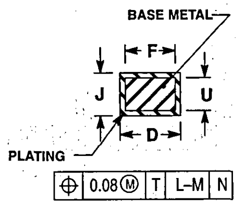
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.00 BSC		0.551 BSC	
A1	7.00 BSC		0.276 BSC	
B	14.00 BSC		0.551 BSC	
B1	7.00 BSC		0.276 BSC	
C	—	1.74	—	0.069
C1	0.04	0.24	0.002	0.009
C2	1.30	1.50	0.051	0.059
D	0.22	0.38	0.009	0.015
E	0.40	0.75	0.016	0.030
F	0.17	0.33	0.007	0.013
G	0.65 BSC		0.026 BSC	
J	0.09	0.27	0.004	0.011
K	0.50 REF		0.020 REF	
P	0.325 BSC		0.013 REF	
R1	0.09	0.20	0.004	0.008
S	16.00 BSC		0.630 BSC	
S1	8.00 BSC		0.315 BSC	
U	0.09	0.16	0.004	0.006
V	16.00 BSC		0.630 BSC	
V1	8.00 BSC		0.315 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	10°	0°	10°
θ1	0°	—	0°	—
θ2	9°	14°	9°	14°

FJ SUFFIX
TQFP (THIN QUAD FLAT PACKAGE)
CASE 983-02

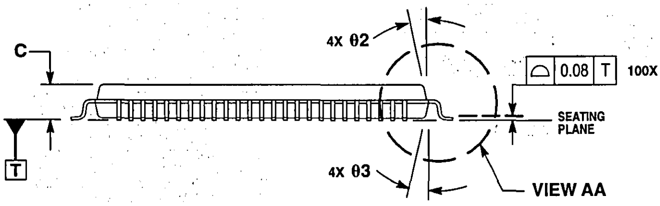


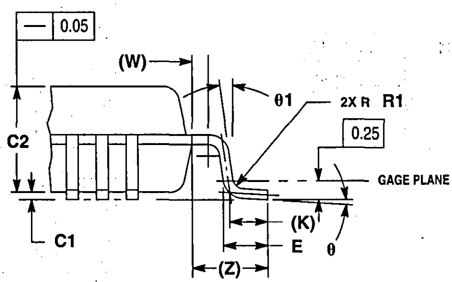


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	14.00 BSC	
A1	7.00 BSC	
B	14.00 BSC	
B1	7.00 BSC	
C	—	1.70
C1	0.05	0.20
C2	1.30	1.50
D	0.10	0.30
E	0.45	0.75
F	0.15	0.23
G	0.50 BSC	
J	0.07	0.20
K	0.50 REF	
R1	0.08	0.20
S	16.00 BSC	
S1	8.00 BSC	
U	0.09	0.16
V	16.00 BSC	
V1	8.00 BSC	
W	0.20 REF	
Z	1.00 REF	
θ	0°	7°
θ1	0°	—
θ2	12° REF	
θ3	12° REF	

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