MECL POCKET BOOK

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Description • Pin-out • Major parameters

The 30 ... to 1600 MHz standard logic family

MECL POCKET BOOK

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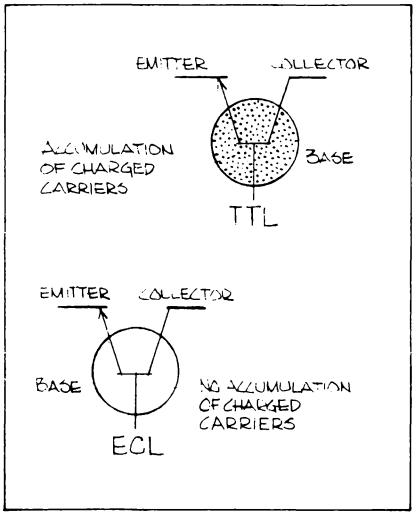
contents

introduction

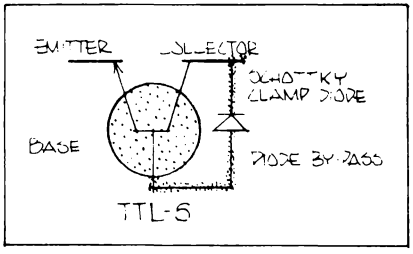
This brochure aims to quickly show you in brief, understandable language, the key advantages of MECL, why it should be easy to use and what Motorola literature is available to make your job that much easier.
There are a lot of applications for high speed MECL logic — way beyond mainframe computer and sophisticated high speed instruments.
Make more on MECL — that's our suggestion. MECL is AVAILABLE. MECL is on the move!

At the present time, there are only two popular types of very high speed integrated circuit logic families available.
One is emitter-coupled logic, labeled ECL. The other is Schottky-clamped TTL logic, designated "TTL-S." It is a higher speed version of the widely used TTL logic family (7400 design series).

TTL stands for "Transistor-Transistor Logic." Presently, perhaps 80% of logic applications employ basic, standard TTL. However, in the constant quest for high speed, there is an inevitable trend away from TTL logic.
The prime reason TTL is not the highest speed logic today and why it cannot increase in speed later is that it is a SATURATED form of logic.
This means that the transistors it employs must be driven into their "saturated" state. The saturated mode substantially slows on-off response in the total system since the transistors require a finite time to come out of saturation — in order to dissipate the accumulation of charged carriers in the base region as a result of the device having been "turned on" electrically. Thus there is a delay in turning the transistor off. Such a time lag is called "storage time."



Schottky-clamped TTL logic reduces the storage time by making use of Schottky diodes. The diodes tend to keep the transistors out of saturation.



The diodes, however, tend to increase input capacitance. Thus there is a significant trade-off. Yes, addition of the diodes permits TTL-S to be faster than TTL... to accomplish speeds of close to 100 MHz, shorter delays of 3 ns. — but at a cost of a 2-to-1 increase in power over the 7400 device series.

The negative point is that TTL-S is self-limited from ever achieving speeds faster than around 100 MHz — and power dissipation above 30 to 50 MHz is prohibitive.

Emitter-coupled logic, on the other hand is the epitome of high speed. Today, MECL is fulfilling a larger percentage of logic appli-

cations as electronic systems have become increasingly sophisticated and demanding — a trend that will step up even more in the future. For MECL offers unique capabilities for communications and high speed signal processing.

This is so because ECL is non-saturated logic. It avoids transistor storage time— without the speed limitation trade-off inherent in TTL-S.

Putting things in perspective, Motorola was, and still is, the pioneer in high speed digital ICs.

It all started back in 1962 when MECL I (MC300/MC350 series) was introduced.

Then four years later, Motorola brought out a faster version — MECL II (MC1000/MC1200 series).

Subsequently, in 1968, Motorola unveiled the fastest form of logic available today in a standard product line -- MECL III. (MC1600 series).

For some time, high speed ICs typically meant high power dissipation, unfamiliar design restrictions, relatively high costs and few useful MSI and LSI complex functions. Motorola set out to hurdle these problems ... helped along by the experience of solving many ECL problems for many custom customers whose need for higher and higher speed systems — without serious trade-offs — were strongly evident.

The net result — in 1971 Motorola introduced MECL 10,000 which, for the first time, combined VERY HIGH SPEED & LOW POWER.

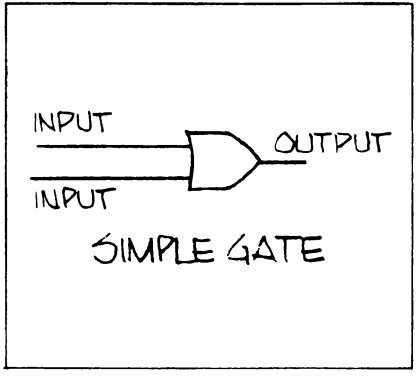
Short-cutting a lot of detail that only a very knowledgeable engineer would comprehend, the two major factors govering high speed are:

... propagation delay of the gates
... and
. . toggle rate of the flip-flops.

In plain language, just what do these two performances characteristics refer to?

Well, a "gate" is one of the basic building blocks of a digital logic system. Its circuit uses one output and a varying number of inputs. The function of a gate is to "gate,"

or passs, data information on receipt of a specified electronic signal.



So "gate propagation delay" refers to the time length between application of a signal and its appearance at the output. This differential is measured in nanoseconds (This is one-billionth of a second. In 1 nanosecond, current moves through a wire the distance of 1/2 foot).

Let us now compare MECL 10,000 to SCHOTTKY TTL in regard to gate propagation delay:

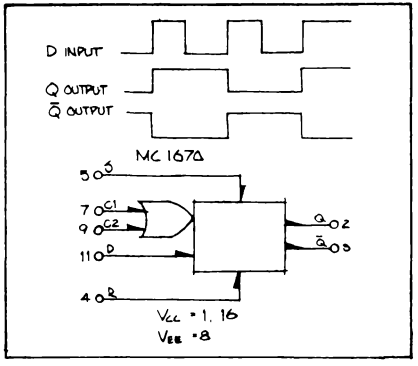
30% faster with MECL!

GATE PROPAGATION DELAY (ns)

TEMP	MECL 10,000	TTL S
25°C	2ns (typ), 2.9ns (max)	3ns (typ), 5ns (max)
-30 and +85°C Standard	3.3ns (max)	*
-55 and +125°C (Military	3.7ns (max)	*

*Schottky TTL data sheets do not guarantee performance over the operating temperature range

Another key building block in a logic system is a "flip-flop." This is a digital circuit used to store information.It has two alternate stable states – "0" and "1," – the two elements of binary language (which we'll talk about in more detail later). The application of a control signal will "flip-flop" it from one state to the other. The number of changes per second is the "toggle rate," as measured in MHz.



As for toggle rate, MECL 10,000 flip-flops have a significant speed advantage over Schottky TTL flip-flops!

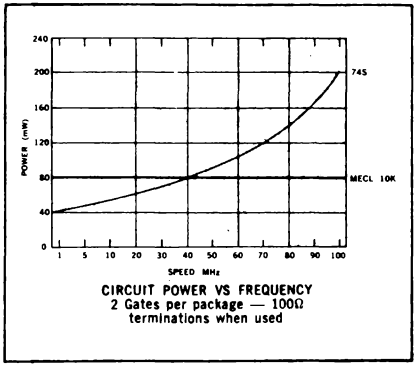
MECL averages 50% faster

TOGGLE RATES (MHz)

CIRCUIT	SPEC	MECL	TTL S
Dual "D" Flip Flop	MIN	125/200	
	TYP	160/225	90
Dual J-K Flip Flop	MIN	125	80
	TYP	140	125
4-Bit Shift Register*	MIN	150	75
	TYP	200	110

*(A shift register is a storage circuit which uses a chain of flip-flops)

MECL has low power along with highest speed! Normally, power requirements increase with frequency for saturated logic — and rapidly become a limiting factor at high-speeds with all saturated logic such as TTL. For example, note the abrupt up-curve for Schottky TTL above 50 MHz.



CIRCUIT POWER VS FREQUENCY
2 Gates per package — 100Ω terminations when used

Measured System Power for MECL 10,000 and Schottky TTL (as a function of frequency).

Contrariwise, the power dissipation of non-saturated, emitter-coupled logic (MECL) is not only low — it is *constant* with frequency — 25 milliwatts per gate, excluding load, in small-scale integration, as low as 8 milliwatts in MSI.

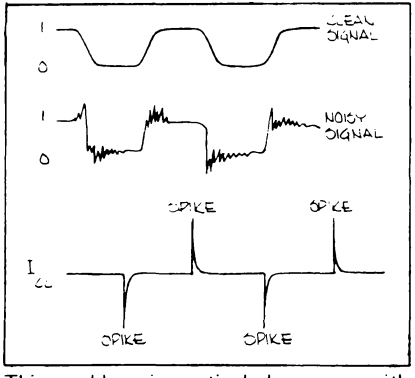
True, Schottky gates, as you can see, use less power at low frequencies — but the advantage clearly swings to MECL 10,000 beyond approximately 35 MHz. And even below 35 MHz, the system power dissipation of MECL 10,000 can be made close to Schottky TTL if MECL complementary outputs and Wire-OR capabilities are used to reduce package count (more on this later).

In a total system, it is true that MECL often will use more power than Schottky. (This assumes the MECL design calls for the use of either pull-down or termination resistors). However, this differential is reduced dramatically if MSI circuits are used.

The gist of all this is that MECL 10,000's total system performance more than offsets any power advantage of Schottky TTL.

Noise in a logic system is generally caused by two factors.

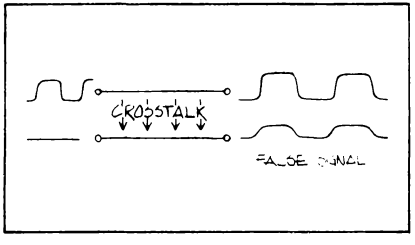
The first one is noise from current spikes on power supply lines.



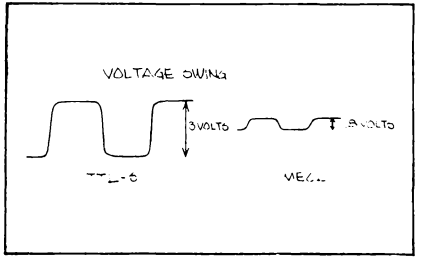
This problem is particularly severe with Schottky TTL because of its totem pole output configuration.

However, with MECL 10,000, with emitter-follower outputs — current spikes are minimal.

"Crosstalk" is the second major factor causing noise — non-desired signals caused by energy spilling over from one signal line to an adjacent signal line. This disruption causes false information to be transmitted. MECL has the advantage over Schottky TTL in this regard because the logic swing of MECL is typically 800 millivolts compared to 3 volts for Schottky. Logic swing is the voltage difference between the two levels representing logical "1" and "0."

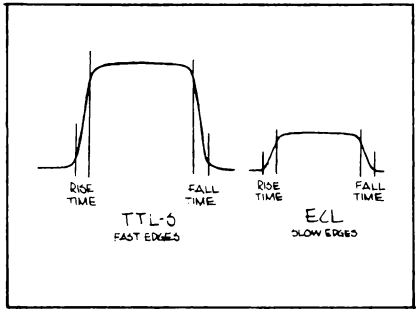


With a lower amount of logic swing there is less tendency for one line to spill over to another line — to crosstalk to the line. Therefore, MECL with its smaller logic swing does not tend to generate as much noise as Schottky TTL's 3 volts of logic swing.



Besides signal amplitude, another factor in limiting crosstalk is what is called "edge speed". The slower the edge speed, the better. On an oscilloscope, the signal waveform shows up visually as an up-slope, a rounded top, and a down-slope. The measure of the time for the up-slope (rise time) or down-slope (fall time) to occur is edge speed. Slower edge speeds are desirable because they are easier to design with — easier to use.

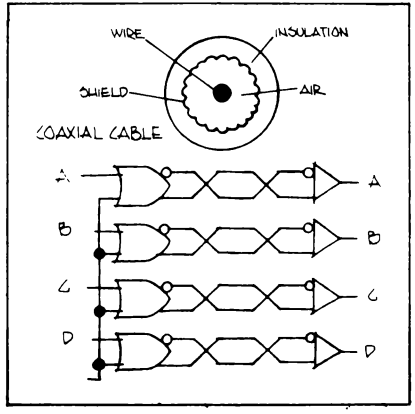
All right — on the basis of edge speed, Schottky TTL circuits generate more than four times the system noise as compared with MECL 10,000!



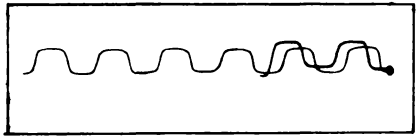
They generate more noise because they are swinging a much larger amount of voltage in about the same time. Therefore, more noise is generated because the signal edges are actually moving faster.

Wiring rules are not much of a problem with very small systems or on circuit boards with only a few high speed devices.

It's a different matter with longer interconnections and larger circuit boards. Techniques such as twisted-pair lines and coaxial cable are used to maintain good signals. High speed circuits usually require a certain amount of these transmission line interconnects to protect the signal from noise.



However, with the longer lines and larger boards there is a problem of signal distortion caused by a phenomena called "reflection".



The system must maintain the integrity of the waveform pattern right down the line — from one end of the wire to its interconnected terminal. Only this way can it maintain proper data transmission, without false trigering due to waveform distortion.

This integrity is not a problem with slow speed logics because the circuit speed is lower than the amount of time a signal is on the line.

Two ways to maintain this integrity are to design with short interconnect lines or to use high speed termination techniques.

With Schottky TTL, the designer is restricted to using short lines because the circuits are not capable of driving terminated lines.

The MECL 10,000 designer can use either technique because MECL 10,000 circuits are specified for use in a transmission line environment.

On MECL data sheets, both AC and DC specs are given for a worst-case 50-ohm load (higher impedance signal lines may also be used).

Because of this capability, you will find no general need for line driving devices in MECL 10,000 — because every output is, in fact, a line driver!

No Schottky parts have MECL's transmission line capabilities. Even the Schottky line driver can only drive 95 ohm line and so is not compatible with ribbon cable, common coaxial cable, and multi-layer interconnects.

Virtually all logic systems today are based on binary language which uses only two symbols, "O" and "1", to transmit all types of information. These symbols are signalled electrically by two voltage levels

– high and low. Usually the high voltage is used to signal "1", and vice versa.

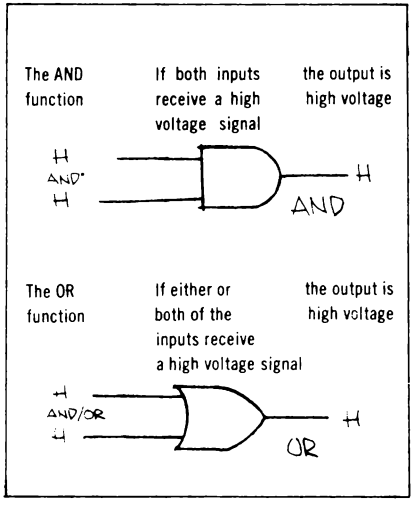
MECL employs a negative supply voltage. SO the two voltage levels are negative:

– 0.9 volts – high level
– 1.7 volts – low level

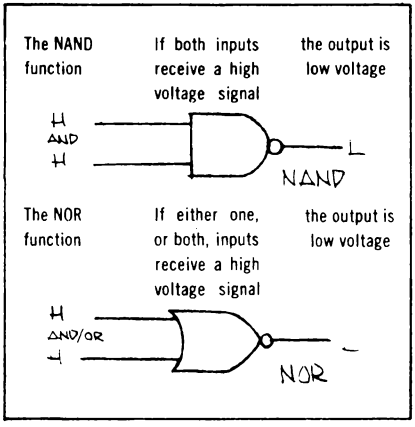
Note the difference between the two is a little less than 1 volt – 800 millivolts.

All right, then – using "0" and "1" voltage signals, data transmission is achieved by using variations of three elementary logic functions – "AND", "OR" and "NOT". All three are in the form of gate devices. They open or close the door on electronic signals trying to pass through inter-related circuits.

For easier understanding, let us greatly simplify matters as to how a logic system uses these logic functions. For illustration, we will show a basic gate diagram with two inputs and one output. Keep in mind that each input must receive either a high or a low level signal.



The NOT function is used by MECL in either of two ways – either inverting the AND function, or inverting the OR function.



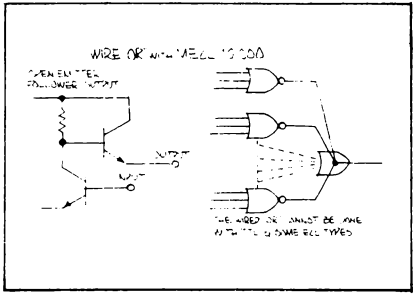
As you no doubt know, in actual operation all this gets extremely complicated. Just the theory behind binary language takes a sizable book to explain. And when you get down to putting it all into action in a computer, or other electronic system there are many varieties of each type of function to consider — and many other types of devices to fill in the block diagrams of a particular system. In total, they make up all devices listed for a logic family like MECL.

Perhaps this very brief description will throw some light on how data language is transmitted by any logic system.

It will also help you understand one of the important advantages of MECL.

MECL Permits Wired-OR Techniques.

This is a logic shortcut which enables the designer to wire together two outputs so that the combination of their outputs results in an OR function.



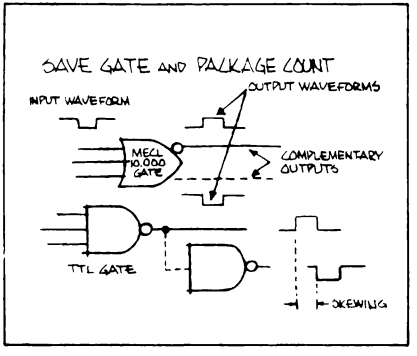
Wire-ORing eliminates adding another gate device because the point at which the separate circuits are wired together will be "1" if any, or all, of the circuits feeding into this point are "1".

The other way to work this goal is to add an additional gate. This causes more delay and higher package count, higher power requirements, and higher cost.

In short, Wire-ORing reduces the number of logic devices required in a design by as much as 30% by producing additional OR gate functions with only an interconnection.

Schottky TTL cannot use the Wire-OR technique!

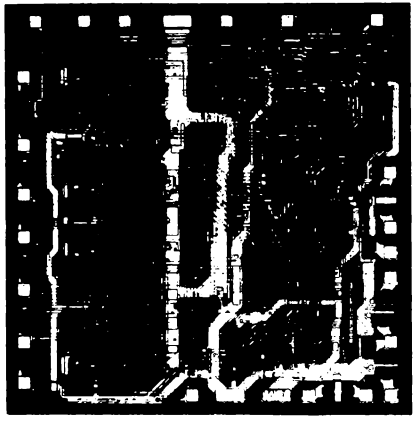
The complementary outputs on most MECL gates and many complex functions are a big advantage to the system designer. With this capability, a logic function and its complement appear simultaneously at the device outputs. The complementary outputs are inherent in the circuit design and both have equal propagation delay.



This feature avoids adding an extra device, an inverter, to get a complementary signal, again reducing package count, cost, and power requirements. It also avoids what is called "skewing". This is a time delay, or offset between two signals which can occur when an inverter is used, causing system timing problems.

Of all standard ECL types, only MECL 10,000 can really be designated a "complex function logic family". Low power and

advanced circuit design techniques, in fact, have permitted extremely sophisticated



This is a photograph of the MC10181 4-bit ALU die. This is the most complex part in the 10,000 family and it is produced using the double layer metallization process. Addition time for 4 bits is 7 ns, and equivalent gate power dissipation is 8 mW.

MECL complex functions. They number some 30 as of now and the number is constantly growing.

A complex function is a highly integrated function which contains the equivalent circuit complexity of 10, or more, logic gates. Depending on the number of gates, they are designated as medium-scale integration (MSI), or large-scale integration (LSI).

These MECL 10,000 functions both reduce package count and cost. They cut down on the number of separate gate packages. They reduce system power requirements. They lessen noise because of reduced wiring and fewer connections. And they increase reliability.

MECL 10,000 logic levels are fully compatible with super-speed MECL III. The designer can use both families in the same system — a bonus when ultra high speed sub-systems are required.

Most MECL 10,000 functions are to be had in the military temperature range ... −55°C

to – 125°C. They are identical to their commercial temperature range equivalents except for temperature rating and their capability to drive 100 ohm (min) transmission lines. Commercial temperature range devices are specified for 50 ohms.

There's some misconception that Schottky TTL can virtually be plugged into TTL designs. BUT THAT'S NOT TRUE. High speed systems inevitably require a little bit more care at the initial design stage and during operation. The particular problems in using high speed logic are essentially the same for emitter-coupled logic as for TTL-S. And once designed in, MECL 10,000 gives you more performance advantages in all applications. Plus a MECL system is open-ended as far as upgrading speed at a later date with minor design modifications. No easy upgrade options exist with Schottky TTL – except a move to ECL.

MECL is the only standard ECL logic family with multiple second sources – Signetics, Fairchild, T.I. and Philips. 82 popular MECL 10,000 device types are now available in the low-priced, dual in-line package.

Over 10,000,000 operating device hours have been accumulated so far in a continuing MECL 10,000 reliability evaluation program by Motorola. These studies project an estimated failure rate of only 0,0013%/1000 hours for circuits operating at 25°C. Almost 70,000,000 device hours – without failure – must be accumulated to verify the estimate.

When we identify a logic system as operating at 100 MHz, or the like, we are referring to the speed at which the system can be operated successfully as a unit – in other words, its signal output speed.

At first glance, it might seem strange to talk about "speed" in terms of "frequency" (MHz) rather than as a measure of "time" (like nanoseconds).

The fact is that frequency – which refers to the number of cycles per second – is actually an inverse of time. For example, 1 MHz amounts to 1 million cycles per second.

Now, there is another type of speed we get

involved in when referring to a logic system. It is "clock rate" – and it, too, is measured in MHz.

Clock rate is the rate at which data is synchronized or moved from one device, or circuit, to the next – inside a logic system. The logic system could be compared to a series of interconnected water pipes, each with a faucet outlet where you are switching water from coming out of one faucet to coming out of another. Each time you switch you slow things down.

If you replace the water pipe system with an electronic logic system, these intermittent delays amount to dividing down the frequency – or slowing down the system. In other words, the rate at which you switch is the clock rate – the speed, in terms of frequency, at which bits, or words, are transferred from one internal logic element to another to carry on a data transfer or logic function. So the output (system speed) is usually slower than the internal speed (clock rate). The devices or circuits must operate, as a minimum, at or above this internal clock rate.

In brief, to oversimplify "system speed" ... "clock rate", – say a man is walking down the street. The rate at which he is walking can be compared to system speed and the speed of his heartbeat, or his pulse rate, could be compared to clock rate.

Clearly, what logic speed you need depends on what you're doing logicwise.

Here are two clues then:

1. If you have system speed needs as low as 4 MHz, you qualify for MECL 10,000.

2. If you need a clock rate of about 10 MHz, or more, you qualify for MECL 10,000.

Then there is a third clue:

3. Whether there is a "high burden of processing" required of a system in relation to the *time available* for processing.

And what does this mean? In any system you need to get a signal from one point to another in a given time frame. For instance, if you're operating at a clock frequency of 100 MHz and you have a basic gate delay

of 2 ns, the best you can do is 5 logic levels of work (5 gates) since you have just 10 nanoseconds to do it in. In other words, if a system is crowded for time, MECL 10,000 is called for.

And here is the fourth and final clue:

4. Do you want to hold open the options for future upgrading of a system.

If a designer has a system in mind that, presently, does not necessarily need the performance advantages of MECL 10,000 — but he envisages that it will need to be up-graded in the future as to system speed, or clock rate, or as to a greater amount of processing — then here, too, MECL 10,000 becomes a natural choice.

1. System speed of 4 MHz, or more
2. Clock rate of 10 MHz, or more
3. Lots of system processing to do in minimum time
4. Future upgrading of system in any of the above three areas.

general information

For the purposes of this discussion, high speed logic has either or both of two characteristics:

a) toggle rates over 50 MHz

b) gate propagation delays under 6 ns

Only two types of standard high speed logic integrated circuits are commonly available in the marketplace: Schottky-clamped TTL logic (TTL-S). and non-saturating emitter-coupled logic (ECL).

Schottky-clamped TTL logic is similar to conventional TTL logic in its circuit configuration and operating characteristics. Conventional TTL is a saturated from of logic; that is, during turn-on, both the emitter-base and collector-base junctions of a transistor are forward biased, causing an accumulation of charged carriers in the base regions. Then, when the transistor is turned off, this charge must discharge through the collector. The finite time required for this charge to dissipate causes a delay in turning the transistor off. This "storage time" delay is clamped TTL logic reduces storage time by means of Schottky-diodes between base-collector junctions. These diodes tend to keep the transistor out of capacitance of the Schottky-clamped transistor. Thus, while the speed of TTL-S is greater than that of TTL, due to a reduction of the transistor input. Emitter-Coupled Logic, being non-saturating by design, completely avoids transistor storage time and its attendent speed limitation without the tradeoffs inherent in TTL-S. Gate delays of less than a nanosecond and operating frequencies approaching a gigahertz are currently feasible, and even these are not ultimate limits.

MECL PRODUCTS

Motorola offers four ECL logic families under its MECL trademark: MECL I, MECL II, MECL III, and MECL 10,000.

The MECL I family, introduced by Motorola in 1962, was the first monolithic intergrated circuit line of emitter-coupled logic. Its propagation delay time of 8 ns and toggle rate of 30 MHz, though no longer considered state of the art, still places it above the speed capabilities of most saturated logic lines. It is still being produced in quantity for use in existing equipment designs, but several features of the more advanced MECL II, III, and MECL 10,000 families favor the use of these families in new designs.

In 1966, Motorola introduced MECL II with gate propagation delays of 4 ns, and flip-flop toggle rates of over 70MHz. Speeds were later increased first to 120 MHz (typical) for the MC1027/MC1227 J-K flip-flop circuit, and then to 180 MHz (min.) for the MC1034 type D flip-flop.

Complex functions became available in MECL II when production capabilities shifted toward more complicated circuits. The family now has adders, data selectors, multiplexers, decoders, and a gas display tube decoder/driver.

Continuing development of MECL made possible an even faster logic family As a result, MECL III was introduced in 1968. Its 1 ns gate propagation delays and greater than 1000 MHz flip-flop toggle rates remain the industry leaders. For the moment, the very high speed capabilities to MECL III appear to have outstripped the general speed requirements of today's computer systems, however they are being utilized extensively in special high-speed sections of computers and high speed test and communication equipment. Motorola is continuing to develop and expand this product line.

For general purpose computer applications, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10,000 is

its compatibility with MECL III to facilitate using both families in the same system. A second important feature is the significant power economy – MECL 10,000 gates use less than one-half the power of MECL III or high speed MECL II gates. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL circuits. For example, complexity of the MC10181 four bit arithmetic unit compares favorably to that of any bipolar integrated circuit on the market.

The basic MECL 10,000 Series has recently been expanded by a subset of devices with even greater speed. This additional series

FIGURE 1 – MECL FAMILY COMPARISONS
General Characteristics

Feature	MECL 10,000		MECL III
	10,100 Series 10,500 Series	10,200 Series 10,600 Series	
1. Gate Propagation Delay	2 ns	1.5 ns	1 ns
2. Gate Edge Speed	3.5 ns	2.5 ns	1 ns
3. Flip-Flop Toggle Speed (min)	125 MHz	200 MHz	1.5 GHz
4. Gate Power	25 mW	25 mW	60 mW
5. Speed-Power Product	50 pJ	37 pJ	60 pJ
6. Transmission Line Capability	Yes	Yes	Yes
7. Wire-Wrap Capability	Yes	Yes	No
8. Output Pulldown Resistors	No	No	No
9. Input Pulldown Resistors	50 k Ω	50 k Ω	50 k Ω

provides a selection of MECL 10,000 logic functions with flip-flop repetition rates up to 200 MHz min. The MECL 10,200 Series is meant for use in critical timing chains, and for clock distribution circuits. MECL 10,200 parts are otherwise identical to their 10,000 Series counterparts (subtract 100 from the MECL 10,200 part number to obtain the equivalent standard MECL 10,000 part number).

Although the basic design of all MECL families is the same, there are differences other than the speed and power capabilities. Comparisons of the key characteristics of each family are given in the table of Figure 1.

MECL IN PERSPECTIVE

In evaluating a logic line, speed and power requirements are the obvious primary considerations. In Figure 2, today's major logic families are compared on the basis of these characteristics. But these are only the start of any comparative analysis. While the chart clearly shows that MECL and other ECL-type families are without peer in the speed category, with low power levels that rival some of the TTL lines, there are a number of other characteristics that make MECL highly desirable for systems implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Significant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

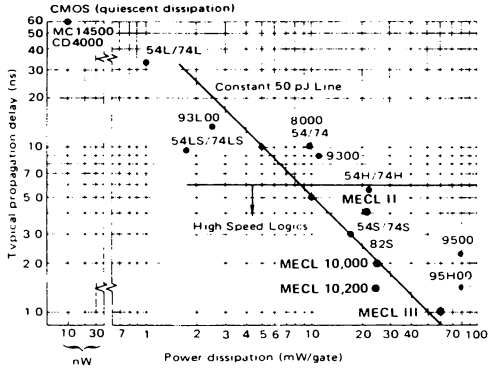


Figure 2a — Speed-Power Characteristics of Major Logic Lines

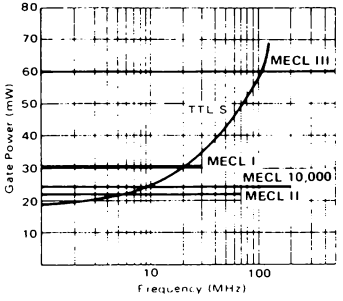


Figure 2b — Power Dissipation versus Frequency (MECL versus TTL-S)

FIGURE 2

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10,000 series). A basic MECL 10,000 gate con-

sumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

MECL APPLICATIONS

The graduated speed ranges of the various MECL Families satisfy many digital system requirements. MECL 10,000 is a general-purpose, high-speed logic family specifically designed for smaller digital systems and peripherals as well as large computers. MECL III is recommended where its exceptionally high speed can buy needed system performance. It is used frequently in counter pre-scalers, high-speed digital communication systems, UHF phase-locked loops, high-speed digital processors, and high-speed timing chains in computers.

The compatibility among MECL families provides a bridge between system performance and system cost. Thus, the many functions and complex circuit members of the MECL 10,000 line can be conveniently mixed with the very-high-speed functions of MECL III, in judicious combinations for system optimization.

BASIC CONSIDERATIONS FOR HIGH SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.

2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.

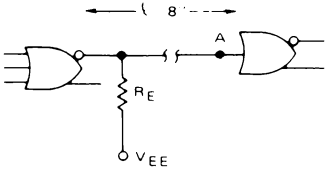
3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high speed systems.

4. Electrical noise generation and pickup are more detrimental at higher speeds.

In general, these four characteristics are speed-and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10,000 Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At extreme speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 3). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*



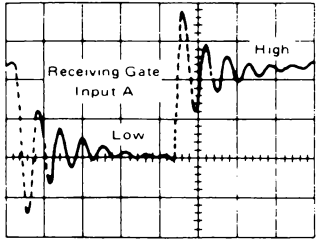
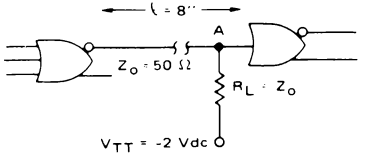


Figure 3a — Unterminated Transmission Line
(No Ground Plane Used)



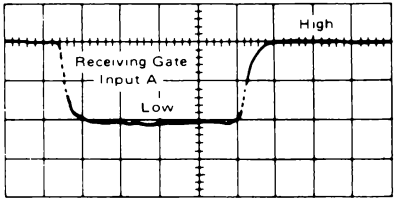


Figure 3b — Properly Terminated
Transmission Line
(Ground Plane Added)

FIGURE 3

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10,000, the rise and fall times of the gate waveforms have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.* From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

CIRCUIT DESCRIPTION

The typical MECL circuit, Figure 4, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections – Any of the power supply levels, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ to -1.3 V (depending on the specific MECL family), $V_{EE} = -5.2$ V.

System Logic Specifications – The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of $V_L = -1.75$ V to a HIGH state of $V_H = -0.9$ V with respect to ground. (These logic levels are valid for the MECL 10,000 and MECL III families.

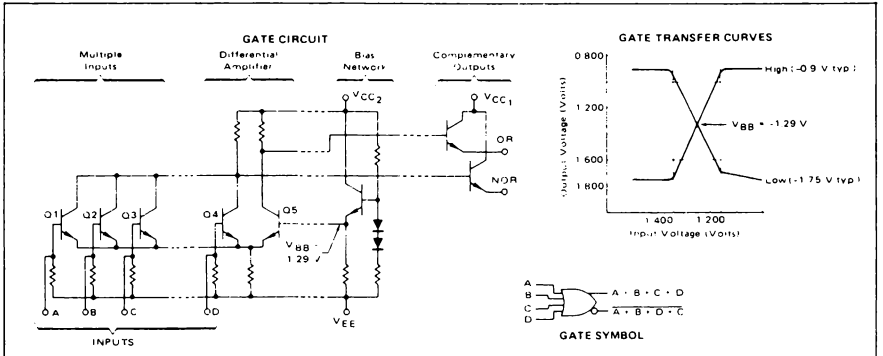


FIGURE 4 – MECL GATE STRUCTURE AND SWITCHING BEHAVIOR

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = −1.75 V = LOW
typical
"1" = −0.9 V = HIGH

Circuit Operation – Beginning with all logic inputs LOW (nominal −1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at −1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or −2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The

base-to-emitter differential across Q1 – Q4 is then the difference between the common emitter voltage (–2.09 V) and the LOW logic level (–1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) or the logic inputs are shifted upward from the –1.75 V LOW state to the –0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from –2.09 V to –1.7 (one diode drop below the –0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at –1.29 V, the base-emitter voltage of Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

VARIATIONS AMONG MECL FAMILIES

The basic gate circuits of the four MECL families are illustrated in Figure 5. From these diagrams, it is evident that some variations were employed as technology advanced. The first of these is that the bias driver for the MECL I Line is not included on the chip, whereas all subsequent lines have this as an internal feature.

Second, most corresponding resistor values differ among all MECL Lines. This difference is necessary to achieve the varying speed and power improvements of the different lines. Of cours, speed is not determined by resistor values alone. Transistor geometries, while not represented on a schematic, are a major determinant. The

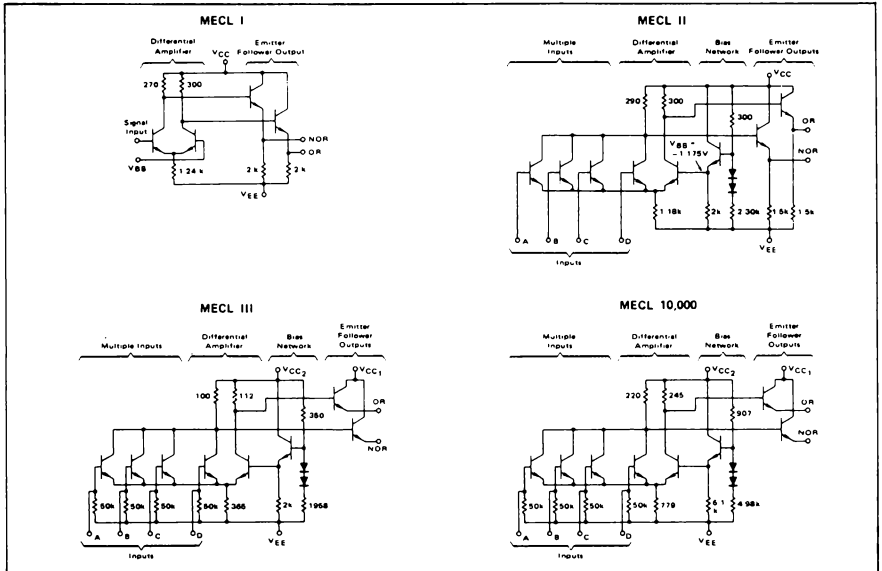


FIGURE 5 — BASIC GATE DIAGRAMS FOR THE MECL FAMILIES

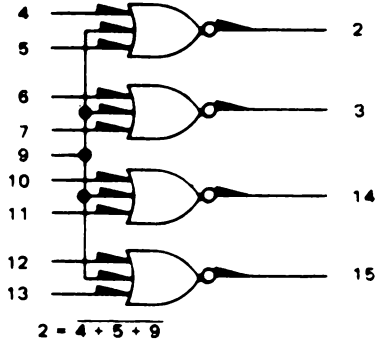
transistor geometries in conjunction with the resistor values provide the speed and power characteristics of the different families.

Third, it will be noted that MECL 10,000 and MECL III gates are supplied with base pull-down resistors ($R_p = 50{,}000\Omega$) in each of the input transistors while the other two families are not. These resistors provide a path for base leakage current to unused input bases, causing them to be well turned off. Where these resistors are not used, any unused inputs must be externally tied to a suitable negative potential, e.g., V_{EE}.

A final significant difference among the families is in the output circuits. MECL I circuits normally are supplied with output pull-down resistors on the chip. MECL II circuits can be obtained with or without output resistors. MECL III and MECL 10,000 circuits have open outputs.

The use of on-chip output resistors has both advantages and limitations. On the plus side is the obvious advantage that fewer external components are required. On the minus side is the fact that wire-ORing capability with on-chip pulldown resistors is limited. Moreover, with open outputs the designer can choose both the value and location of his termination to meet the system requirements. And finally, the use of external resistors reduces onchip heating and power dissipation, allowing more complex LSI and increasing chip life and reliability.

MECL 10,000 compatible functions

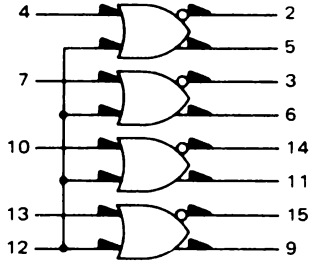


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

Quad 2-input NOR Gate with Strobe

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates. Input pulldown resistors eliminate the need to tie inused inputs to a voltage supply. Open emitter outputs permit wire-ORing and direct connection to busses.



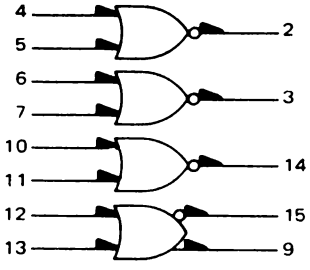
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

Quad OR/NOR Gate

The MC10101 is a quad 2-input OR/NOR gate which one input from each common to pin 12. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

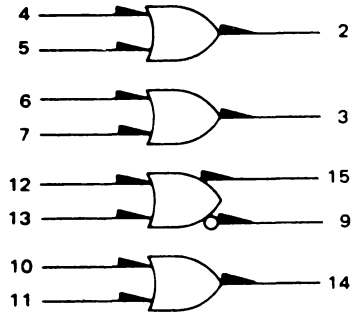
Quad 2-input NOR Gate



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 25 mW typ/gate (No Load)
tpd = 2.0 ns typ

The MC10102 is a quad 2-input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

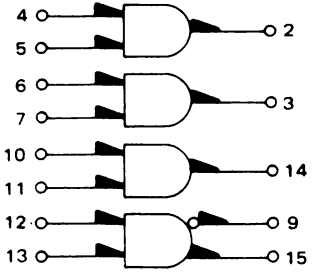


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 25 mW typ/gate (No Load)
tpd = 2.0 ns typ

Quad 2-input OR Gate

The MC10103 is a high-speed, low-power quad 2-input OR gate. One of the gates has both OR and NOR outputs. Input pull-down resistors eliminate the need to tie down unused inputs.

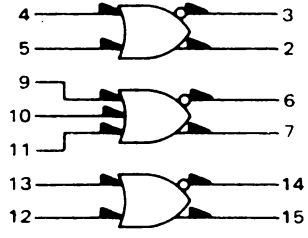


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 35 mW typ/gate (No Load)
tpd = 2.7 ns typ

Quad 2-input AND gate

The MC10104 provides a very useful low power, high speed logic AND function. High Z input pulldown resistors allow high dc and ac fanouts and eliminate the need to tie unused inputs to an external supply. The open emitter outputs allow maximum flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines. Open emitter outputs also allow wire-ORing capability.

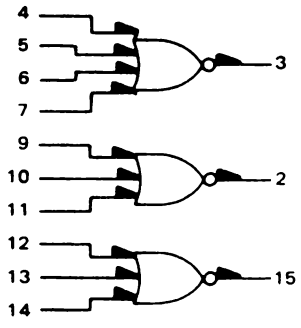


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

Triple 2-3-2 input OR/NOR Gate

The MC10105 is a triple 2-3-2 input OR/-NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

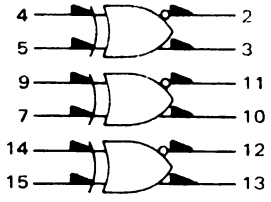


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

Triple 4-3-3 input NOR Gate

The MC10106 is a triple 4-3-3 input NOR gate. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.



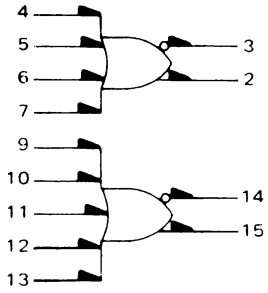
$3 = (4 \bullet \bar{5}) + (\bar{4} \bullet 5)$
$2 = (\bar{4} \bullet \bar{5}) + (4 \bullet 5)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.5 ns typ

Triple 2-input exclusive OR/Exclusive NOR

This three gate array is designed to provide the positive logic Exclusive OR and Exclusive NOR functions in high speed applications. Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

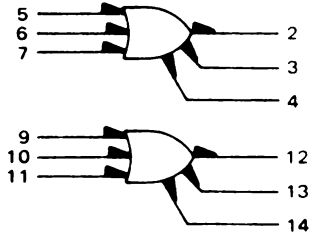


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 2.0 ns typ
P_D = 30 mW typ/gate (No Load)

Dual 4-5-input OR/NOR Gate

The MC10109 is a dual 4-5 input OR-NOR gate which is pin compatible with the MECL III MC1660L dual OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to V_{EE} eliminating the need to tie unused inputs low.



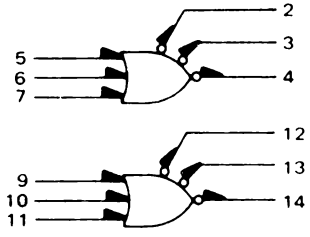
V_{CC1} = 1, 15
V_{CC2} = 16
V_{EE} = 8

P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)

Dual 3-input 3-output OR Gate

The MC10110 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10110 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.



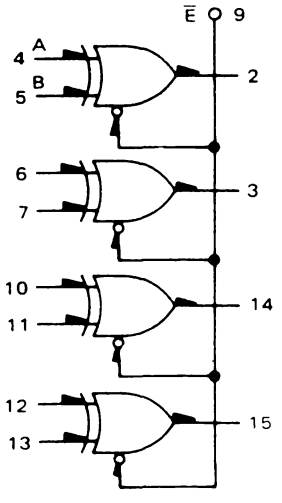
V_{CC1} = 1, 15
V_{CC2} = 16
VEE = 8

P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)

Dual 3-input 3-output NOR Gate

The MC10111 is designed to drive up to three transmission lines simultaneously. The multiple outputs of this device also allow the wire-"OR"-ing of severak levels of gating for minimization of gate and package count.

The ability to control three parallel lines from a single point makes the MC10111 particularly useful in clock distribution applications where minimum clock skew is desired. Three V_{CC} pins are provided and each one should be used.



TRUTH TABLE

A	B	$\overline{E}$	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

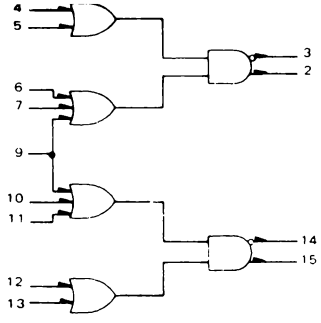
ϕ = Don't Care

V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

Quad Exclusive OR Gate

The MC10113 is a quad Exclusive OR gate, with an enable common to all four gataes. All four outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active low. Input pulldown resistors included in the circuit make it unnecessary to tie down unused inputs. Open emitter outputs permit direct connection of outputs to busses.



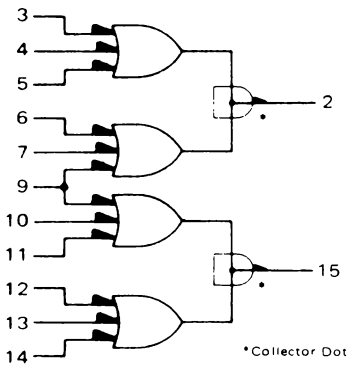
$$2 = \overline{(4 + 5) \bullet (6 + 7 + 9)}$$
$$3 = (4 + 5) \bullet (6 + 7 + 9)$$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

Dual 2-Wide 2-3-input OR-AND/OR-AND-INVERT Gate

The MC10117 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

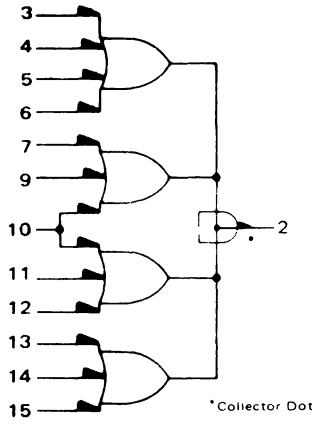


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

Dual 2-Wide 3-input OR-AND Gate

The MC10118 is a basic logic building block providing the OR-AND function, useful in data control and digital multiplexing applications.

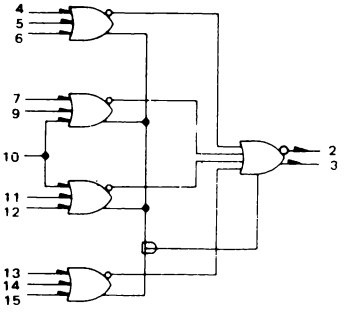


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

4-Wide 4-3-3-3 input OR-AND Gate

The MC10119 is a 4-Wide 4-3-3-3 Input OR-AND gate with one input from two gates common to pin 10. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.



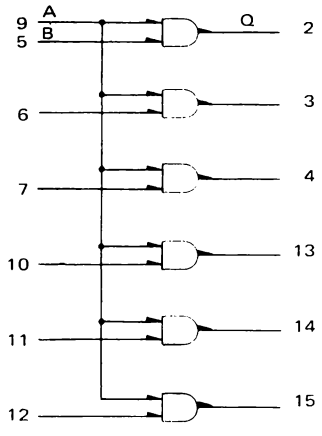
$$2 \quad (4 + 5 + 6) \cdot (7 + 9 + 10) \cdot (10 + 11 + 12) \cdot (13 + 14 + 15)$$
$$3 \quad \overline{(4 + 5 + 6) \cdot (7 + 9 + 10) \cdot (10 + 11 + 12) \cdot (13 + 14 + 15)}$$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ

4-Wide OR-AND/OR-AND-INVERT Gate

The MC10121 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.



TRUTH TABLE

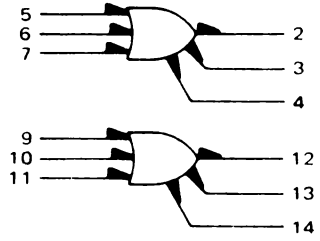
Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ

Hex AND Gate

The MC10197 provides a high speed hex AND function with strobe capability. Open emitter outputs allow wire"OR"-ing. This high density function is useful in control, bussing, communications in high speed central processors, high speed peripherals, digital communications systems, minicomputers, and instrumentation.



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8

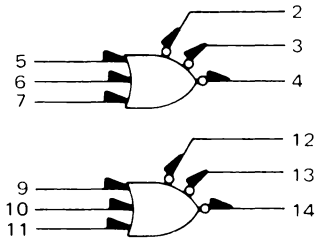
P_D = 160 mW typ/pkg (No load)
t_{pd} = 1.5 ns typ (All Output Loaded)

High Speed Dual 3-input 3-output OR Gate

The MC10210 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10210 particularly useful in clock distribution applications where minimum clock skew is desired.

The MC10210 is a higher speed version of the MC10110. It is a pin-for-pin replacement for the device. Three V_{CC} pins are provided and each one should be used.



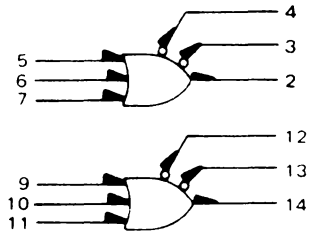
V_{CC1} = 1, 15
V_{CC2} = 16
V_{EE} = 8

P_D = 75 mW typ/gate (Outputs Open)
t_{pd} = 1.5 ns typ (All Outputs Loaded)

High Speed Dual 3-input 3-output NOR Gate

The MC10211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.



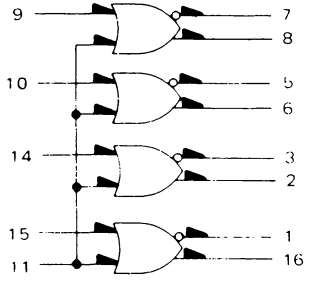
V_{CC1} = 1, 15
V_{CC2} = 16
V_{EE} = 8

P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)

High Speed Dual 3-input 3-output OR/NOR Gate

The MC10212 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10212 particularly useful in clock distribution applications where minimum clock skew is desired.

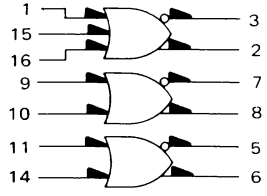


V_{CC} = Pin 4
V_{EE1} = Pin 12
V_{EE2} = Pin 13

t_{pd} = 0.75 ns typ
t+, t− = 0.75 ns typ
P_D = 600 mW typ/pkg. (No Load)
BW = 600 mV @ 500 MHz typ

High Bandwidth Quad 2-input OR/NOR Gate

The MC1601 is a quad OR/NOR gate designed for use in systems requiring up to a 500 MHz bandwidth. Each gate has one independent input, and one input common to all four gates. Outputs may not be wire-ORed.

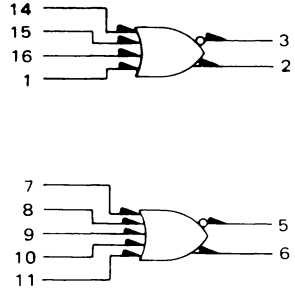


V_{CC} = Pin 4
V_{EE1} = Pin 12
V_{EE2} = Pin 13

t_{pd} = 0.75 ns typ
t+, t− = 0.75 ns typ
P_D = 460 mW typ/pkg (No Load)
BW = 600 mV @ 500 MHz (typ)

High Bandwidth Triple 2-2-3-input OR/NOR Gate

The MC1602 is a triple 2-2-3-input OR/-NOR gate designed for use in systems requiring up to a 500 MHz bandwidth. Outputs may not be wire-ORed.

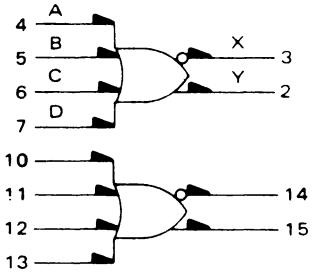


V_{CC} = Pin 4
V_{EE1} = Pin 12
V_{EE2} = Pin 13

t_{pd} = 0.75 ns typ
t+, t− = 0.75 ns typ
P_D = 320 mW typ/pkg. (No Load)
BW = 600 mV @ 500 MHz (typ)

High Bandwidth
4-5-input OR/NOR Gate

The MC1603 is a 4-5-input OR/NOR gate designed for use in systems requiring up to a 500 MHz bandwidth. Outputs may not be wire-ORed.



$X = \overline{A + B + C + D}$

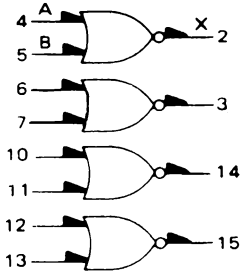
$Y = A + B + C + D$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510 ohm load)
= 1.1 ns typ (50 ohm load)
P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max

Dual 4-input Gate

MC1660 provides simultanous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point is always in the center of the transition region over the temperature range (−30° to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.



$X = \overline{A + B}$

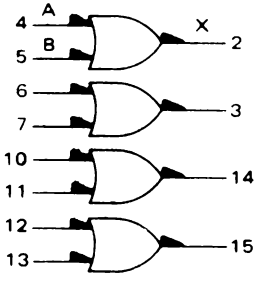
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max

Quad 2-input NOR Gate

Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (−30 to +85°C).
Input pulldown resistors eliminate the need to the unused inputs to V_{EE}.



X = A + B

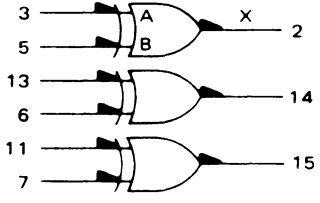
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = −25 mAdc max

Quad 2-input OR Gate

Four 2-input OR to AND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range −30 to +85°C.
Input pulldown resistors eliminate the need to the unused inputs to V_{EE}.



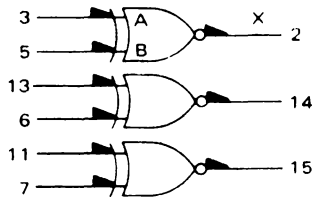
$X = A \bullet \overline{B} + \overline{A} \bullet B$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, $I_L = -25$ mAdc max

Triple 2-input Exclusive-OR Gate

This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30^oC to $+85^oC$). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.



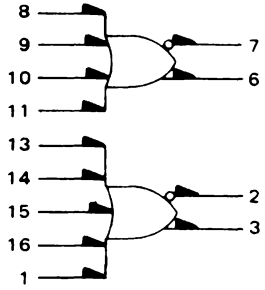
$X = A \bullet B + \bar{A} \bullet B$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = −25 mAdc max

Triple 2-input Exclusive-NOR Gate

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (−30° to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

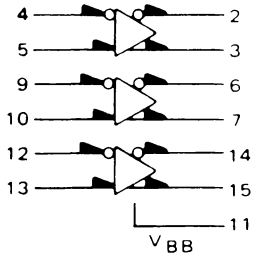


V_{CC1} = 4
V_{CC2} = 5
V_{EE} = 12

t_{pd} = 0.8 ns typ
P_D = 125 mW typ/pkg (No Load)
Output Rise and Fall Times
(10%/o to 90%/o) 1.7 ns
(20%/o to 80%/o) 1.1 ns

Dual 4-5-input OR/NOR Gate

The MC1688 is a dual 4-5 input OR-NOR gate. All inputs are terminated by a 50 k ohm resistor to V_{EE} eliminating the need to tie unused inputs low.



V_{CC1} = 1
V_{CC2} = 16
V_{EF} = 8

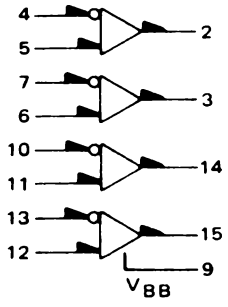
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg

Triple Line Receiver

The MC10114 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative position. This allows a large amount of common mode noise immunity for extra long lines. Another feature of the MC10114 is that the OR outputs (pins 3, 7, 15) go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, digital communication systems, testing and instrumentation systems. The MC10114 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the MC10114 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.



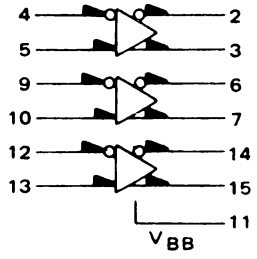
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 2.0 ns typ
P_D = 110 mW typ/pkg (No Load)

Quad Line Receiver

The MC10115 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10115 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

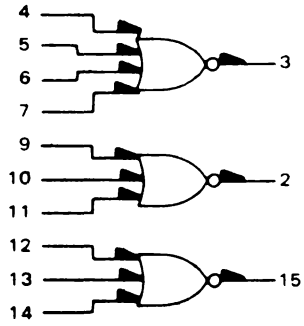
t_{pd} = 2.0 ns typ
P_D = 85 mW typ/pkg (No Load)

Triple Line Receiver

The MC10116 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10116 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

Triple 4-3-3 input
Bus Driver

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leq$ -2.0 Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off". This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part.

Bus Driver

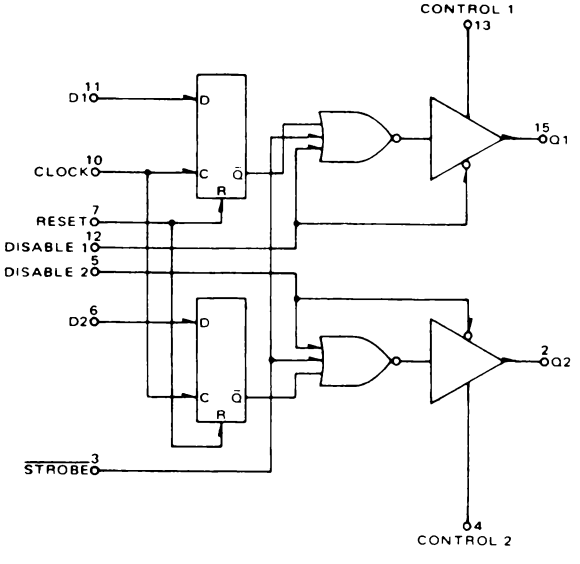
The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

The operating mode IBM or TTL is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data to the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

The MC10128 is useful in interfacing and bus applictions in central processors, minicomputers, and peripheral equipment.



V_{CC} = Pin 14
Gnd 1 = Pin 16
Gnd 2 = Pin 1
Gnd 3 = Pin 9
V_{EE} = Pin 8

P_D = 700 mW pkg/typ (No Load)
t_{pd} = 12 ns typ

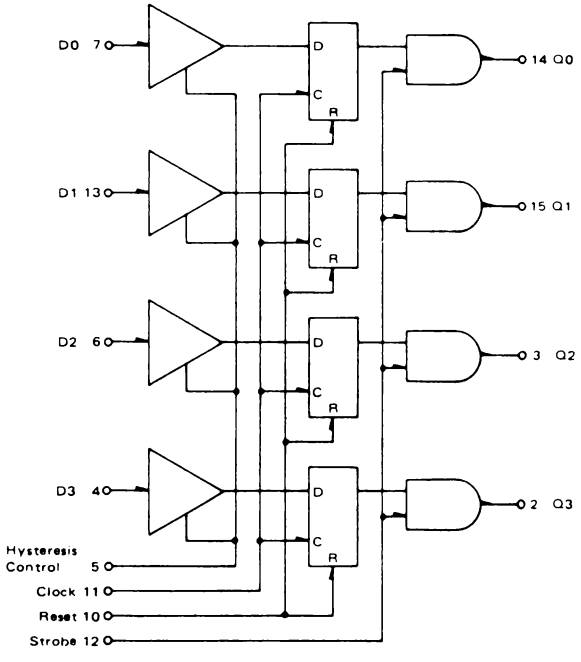
Quad Bus Receiver

The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept MTTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs accept the bus levels, and storage elements are provided to yield temporary latch storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50 k ohm pull-down resistors to V_{EE}. They may be left floating, if not used.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The MC10129 is especially useful in interface applications for central processors, mini-computers, and peripheral equipement.



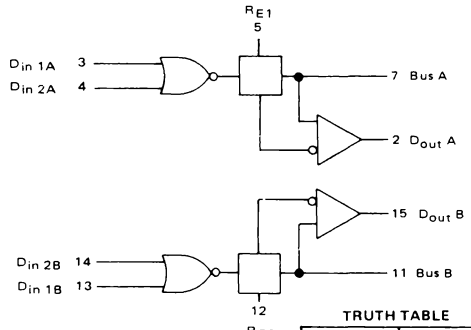
TRUTH TABLE

D	C	STROBE	RESET	Q_{n+1}
Φ	Φ	L	Φ	L
Φ	H	L	H	L
L	L	H	Φ	L
Φ	H	H	L	Q_n
H	L	H	Φ	H

Φ = Don't Care

V_{CC} = Pin 9
Gnd = Pins 1 and 16
V_{EE} = Pin 8

P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ



TRUTH TABLE

Inputs		Outputs	
D_{in} 1	D_{in} 2	Bus	D_{out}
L	L	V_{BusO}	H
H	L	V_{BusH}	H
L	H	V_{BusH}	H
H	H	V_{BusH}	H
L	L	V_{BusH}	L
H	L	V_{BusL}	L
L	H	V_{BusL}	L
H	H	V_{BusL}	L

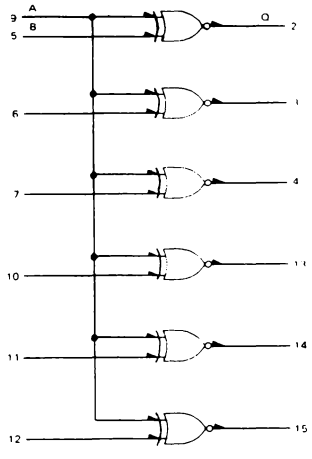
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 405 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

Dual Simultaneous Bus Transceiver

The MC10194 is a dual line driver/receiver which is capable of transmitting and receiving full duplex digital signals on a high speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

The MC10194 is designed to work with a wide range of line impedances by connecting a resistor equal to one half the line impedance between the R_{E1} and R_{E2} inputs and V_{EE}. Each driver in the circuit will drive lines down to 75 ohms or the two drivers may be operated in parallel for lines down to 37 ohms. The data inputs and outputs on the MC10194 are fully compatible with other MECL 10,000 circuits.



TRUTH TABLE

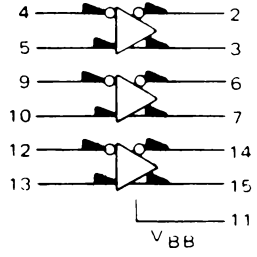
Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ

Hex Inverter/Buffer

The MC10195 is a Hex Buffer Inverter which is built using six EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters. With the common input connected to a high logic level the MC10195 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

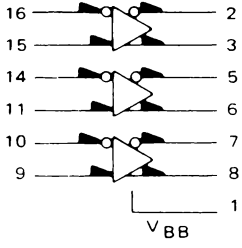
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)

High Speed Triple Line Receiver

The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connectet to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

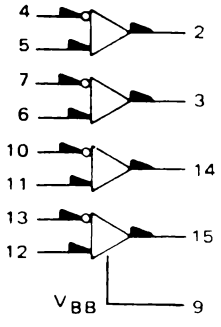


V_{CC} = Pin 4
V_{EE1} = Pin 12
V_{EE2} = Pin 13

t_{pd} = 0.75 ns typ
t+, t− = 0.75 ns typ
P_D = 460 mW typ/pkg. (No Load)
BW = 600 mV @ 500 MHz typ

High Bandwidth Triple Line Receiver

The MC1604 is a triple line receiver designed for use in systems requiring up to a 500 MHz bandwidth. Both OR and NOR outputs are provided on each of the three receivers. V_{BB} is available at pin one. Outputs may not be wire-ORed.

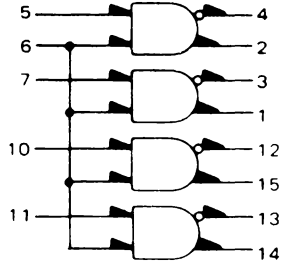


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)
Full Load Current, I_L = −25 mAdc max

Quad Line Receiver

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

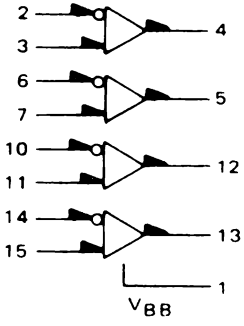
P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50%/o out)

Quad MTTL to MECL Translator

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level "O", it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and −5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

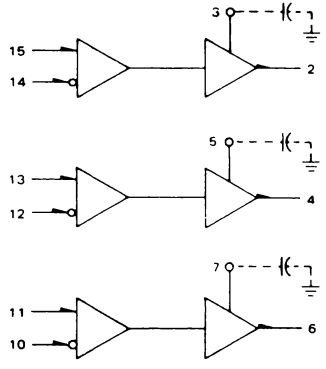
P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

Quad MECL to MTTL Translator

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky MTTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and −5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

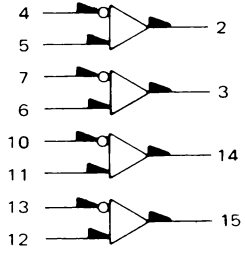


V_{CC} = Gnd = Pins 1,16
V_{EE} = Pin 8 = −5.2 Vdc ± 5o/o
V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc ± 10o/o

Max Load: 350 pF
P_D = 1.0 W typ/pkg @ 5.0 MHz
Operating Rate: 5.0 MHz typ.
(all 3 translators in use simultaneously)

Triple MECL to NMOS Translator

The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It many also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to V_{SS} or to an external capacitor (0.01 to 0.05μF to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, V_{SS} line fluctuations due to transient currents are also reduced.

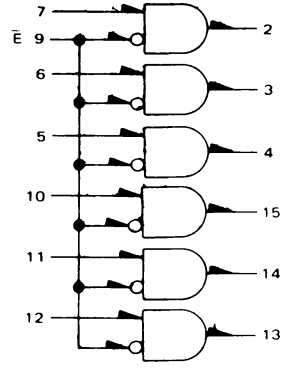


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
V_{SS} = Pin 9 Translator
V_{CC} = Pin 9 Receiver

P_D = 215 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (50% to − 1.5 Vdc out)

Quad MST to MECL 10,000 Translator

The MC10190 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10,000 logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tieing one of the inputs to ground. Since the MC10190 is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} the circuit becomes a line receiver for MECL signals.



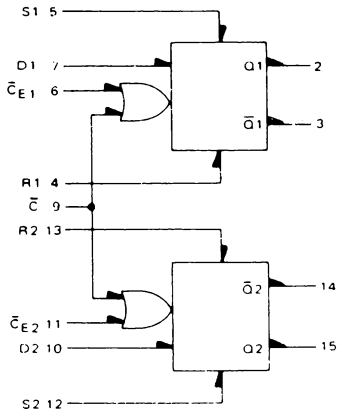
7	9	2
L	L	L
L	H	L
H	L	H
H	H	L

V_{CC1} = Pin 1 = −1.25 Vdc
V_{CC2} = Pin 16 = Gnd
V_{EE} = Pin 8 = −5.2 Vdc

P_D = 145 mW typ/pkg (No Load)
t_{pd} = 2.2 ns typ input to Output
= 3.3 ns typ Enable to Output

Hex MECL 10,000 to MST Translator

The MC10191 is a hex MECL 10,000 to IBM MST type logic translator. A common enable (active low) is provided for gating. Open emitter outputs are provided to permit direct transmission line driving.
The MC10191 is useful for interfacing to both MST-II and MST-IV systems.



TRUTH TABLE

D	$\overline{C}$	$\overline{C}E$	Q_{n+1}
L	L	L	L
H	L	L	H
Φ	L	H	Q_n
Φ	H	L	Q_n
Φ	H	H	Q_n

Φ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

Dual Latch

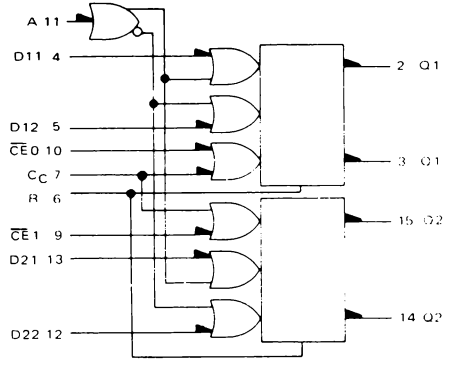
The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{C}E$ or both are high.



TRUTH TABLE

R	D	C_C	$\overline{CE}$	Q_{n+1}
L	L	↑	L	L
L	H	↑	L	H
L	X	L	L	Q_n
L	X	H	L	Q_n
L	X	X	H	Q_n
H	X	X	X	L

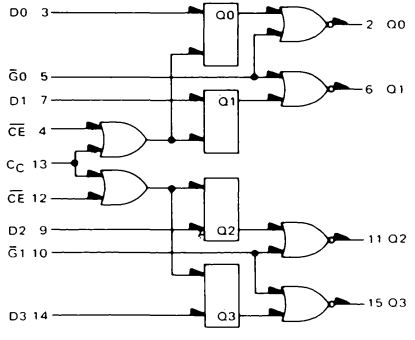
$D = (\bar{A} \bullet D11) + (A \bullet D12)$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

Dual Multiplexer with Latch and Common Reset

The MC10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.



TRUTH TABLE

$\bar{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

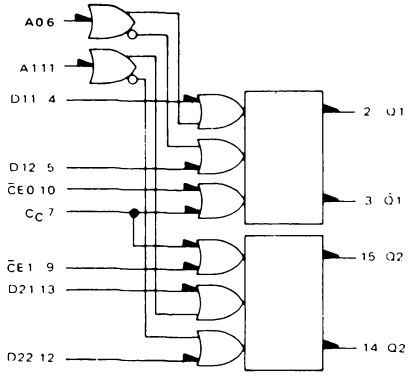
ϕ = Don't Care
C = $\bar{C}_C$ + CE

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Quad Latch

The MC10133 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on negative going transition of the clock.



TRUTH TABLE

C	A0	D11	D12	Q_{n+1}
L	L	L	Φ	L
L	L	H	Φ	H
L	H	Φ	L	L
L	H	Φ	H	H
H	Φ	Φ	Φ	Q_n

Φ = Don't Care
C = $\overline{CE}$ + C_C

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

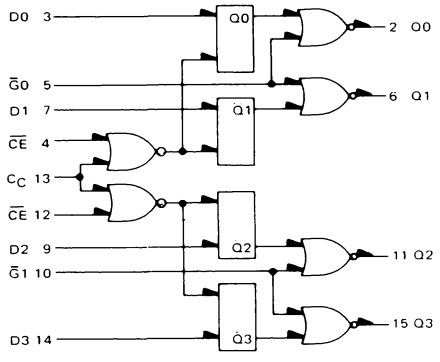
Dual Multiplexer with Latch

The MC10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

Output rise and fall times have been optimized to provide relaxation of system layout and design criteria.



TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

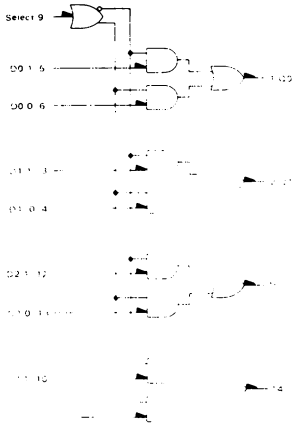
ϕ = Don't Care
$C = C_C + \overline{CE}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Quad Latch

The MC10153 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-O Red together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on positive going transition of the clock. The MC10153 provides the same logic function as the MC10133, except for inversion of the clock.



TRUTH TABLE

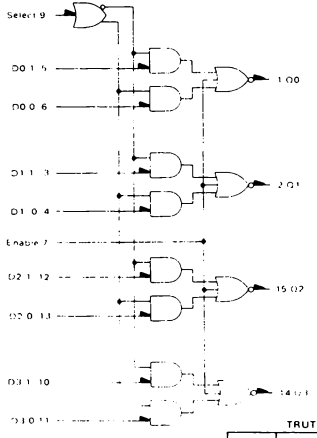
Select	D0	D1	Q

V_{CC} = Pin 16
V_{EE} = Pin 8

P_D = 197 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)

Quad 2-Input Multiplexer (Non-Inverting)

The MC10158 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs (D0 0, D1 0, D2 0, and D3 0 and a low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1.



TRUTH TABLE

Enable	Select	D0	D1	Q
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L
H	X	X	X	L

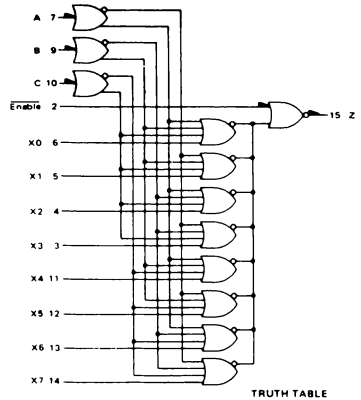
X = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8

P_D = 218 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)

Quad 2-Input Multiplexer (Inverting)

The MC10159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0. A low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.



TRUTH TABLE

ENABLE	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	Φ	Φ	Φ	L

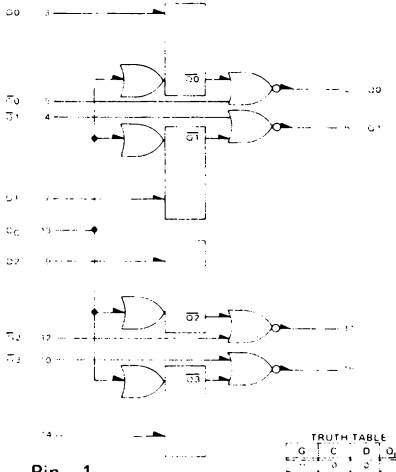
Φ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Data to output)

8-Line Multiplexer

The MC10164 is a high speed, low power eight-channel data selector which routes data present at one of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.



TRUTH TABLE

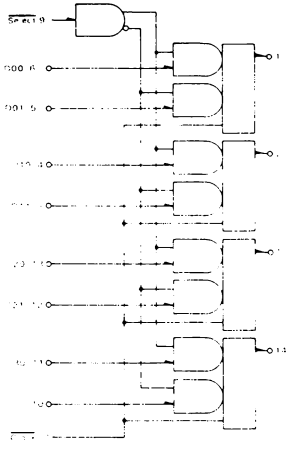
G	C	D	Q_{n+1}
0	1	1	1
0	1	0	0
1	X	X	Q_n
X	0	X	Q_n

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 310 mW typ/pkg (No Load)
t_{pd}: $\overline{G}$ to Q = 2 ns typ
D to Q = 3 ns typ
C to Q = 4 ns typ

Quad Latch

The MC10168 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.



TRUTH TABLE

SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
	H	D01
	X	$Q0_n$

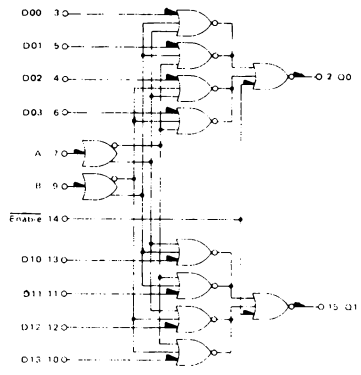
X = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8

P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

Quad 2-input Multiplexer/Latch

The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.



TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
Ē	B	A	Q0	Q1
H	ø	ø	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13

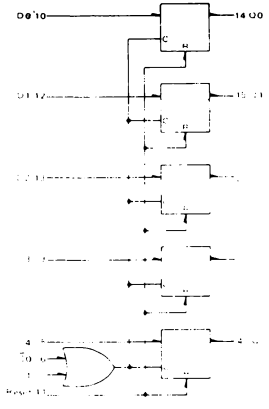
ø = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

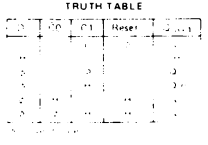
P_D = 305 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (data to output)

Dual 4 to 1 Multiplexer

The MC10174 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state. The enable is also useful in wire-ORing several multiplexers to achieve additional channel capability. Delay from data input to output is typically 3.5 nanoseconds.



TRUTH TABLE



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

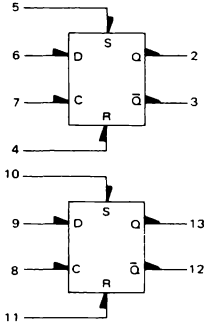
P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to output)

Quint Latch

The MC10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR" ed together. Propagation delays are typically 2.5 nanoseconds from each data input to the output.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

The MC10175 allows storage of five bits of information, and it is useful in temporary storage applications in high speed central processors, accumulators, register files, digital communication systems, instrumentation, and test equipment.



TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	0	0	Q_n
1	0	0	0	1
0	1	0	0	0
1	1	0	0	**
0	0	0	1	0
0	0	1	1	1

**Output state not defined X = Don't Care

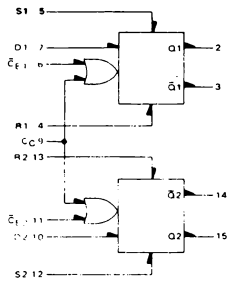
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

Dual Clocked Latch

This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

Dual Type D Master-Slave Flip-Flop



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

X Don't Care
C C_E - C_C
A clock H is a clock transition from a low to a high state

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N D

N D Not Defined

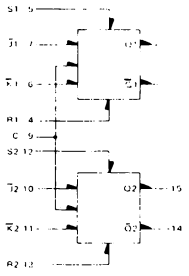
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 235 mW typ/pkg (No Load)
f_{Tog} = 160 MHz typ

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.



CLOCK J-K TRUTH TABLE*

J	K	Q_{n+1}
L	L	Q_n
H	L	L
L	H	H
H	H	$\overline{Q}_n$

*Output states change on positive transition of clock for J-K input combination present

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. Not Defined

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 280 mW typ/pkg (No Load)
f_{Tog} = 140 MHz typ

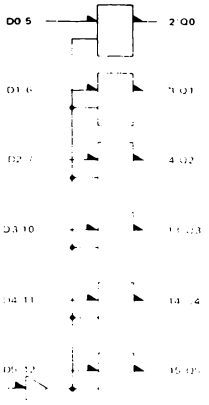
Dual J-K Master-Slave Flip-Flop

The MC10135 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs overide the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
↑	0	0
↑	1	1
0	X	Q_n
1	X	Q_n

X = Don't Care

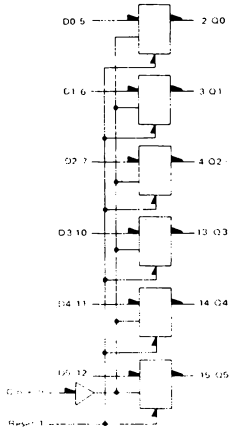
↑ = Clock C goes from a low to a high state

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 460 mW typ/pkg (No Load)
f_{toggle} 150 MHz (typ)

Hex D Master-Slave Flip-Flop

The MC10176 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.



CLOCKED TRUTH TABLE

R	C	Q	Qn+1
L	L	Ø	Qn
L	H	L	L
L	H	H	H
H	L	Ø	L

Ø Don't Care
* A clock H is a clock transition from a low to a high state

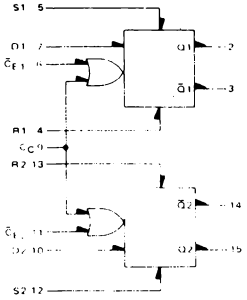
V_{CC} = Pin 16
V_{EE} = Pin 8

P_D = 460 mW typ/pkg (No Load)
f_{toggle} 150 MHz (typ)

Hex "D" Master-Slave Flip-Flop/With Reset

The MC10186 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. Reset only functions when clock is low.

High Speed Dual Type D Master-Slave Flip-Flop



CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	↑	Q_n
H	L	L
H	H	H

ϕ = Don't Care
C = C_E • C_C
A clock H is a clock transition from a low to a high state

R-S TRUTH TABLE

R	S	Q_{n+1}
L	↓	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

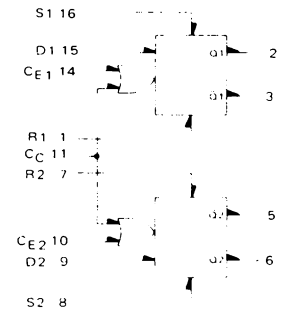
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 270 mW typ/pkg (No Load)
f_{Tog} = 225 MHz typ

The MC10231 is a dual master-slave type D flip-flop. Asynchronouse Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times allow high frequency operation over 200 MHz.



TRUTH TABLE

Inputs					Outputs	
R	S	D	C_E	C_C	Q	$\overline{Q}$
L	H	◌	◌	◌	H	L
H	L	◌	◌	◌	L	H
L	L	H	⌐	⌐	H	L
L	L	H	L	⌐	H	L
L	L	H	⌐	L	H	L
L	L	H	L	L	Q	$\overline{Q}$
L	L	L	⌐	⌐	L	H
L	L	L	L	⌐	L	H
L	L	L	⌐	L	L	H
L	L	L	L	L	Q	$\overline{Q}$

R S cannot be High at the same time
◌ Don't Care
⌐ Low to High Transition

V_{CC} = Pin 4
V_{EE1} = Pin 12
V_{EE2} = Pin 13

P_D = 525 mW typ/pkg. (No Load)
f_{tog} = 500 MHz typ.

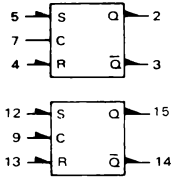
Dual Type D Master-Slave Flip-Flop

The MC1605 is a high speed dual master-slave type D flip-flop. It is designed for use in high bandwidth systems. Each flip-flop has its own clock input in addition to a common clock enable input. Each flip-flop has a Q and $\overline{Q}$ output. The outputs may not be wire-ORed.

Data is transferred to the output with the rising edge of the clock. Each flip-flop has its own set and reset input, and they override the clock input.

Dual Clocked R-S Flip-Flop

This device consists of two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage.
The device is useful as a high-speed dual storage element.



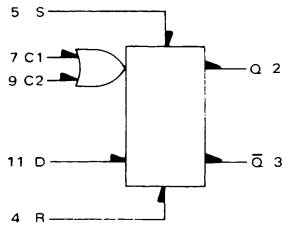
TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)



TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	◇	◇	H
H	L	◇	◇	L
H	H	◇	◇	ND
L	L	L	L	Q_n
L	L	L	⌐	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	⌐	H
L	L	H	H	Q_n

◇ Don't Care
ND = Not Defined
C = C1 • C2

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

Master-Slave
Type D Flip-Flop

The MC1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

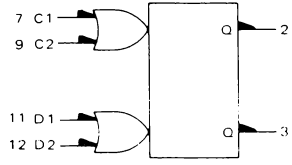
When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

UHF Prescaler
Type D Flip-Flop



TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	X	Q_n
⌐	L	L
⌐	H	H

C = C1 • C2 X = Don't Care
D = D1 • D2

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 200 mW typ/pkg (No Load)
f_{tog} = 500 MHz min

The MC1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary Q and $\overline{Q}$ outputs. It is a higher frequency replacement for the MC1670 (350 MHz) D flip-flop. There are no set or reset inputs and an extra data input is provided.

When used with the MC1678, the MC1690 provides a decade counter capable of 500 MHz operation.

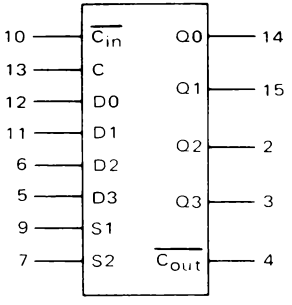
Universal Hexadecimal Counter

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This binary counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

A prescaler can be constructed using the MC10136 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 1000 MHz prescaler is possible using an MC1699 1GHz divide by 4, an MC12013 500 MHz divide by 10-11, and the MC10136.



SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	Φ	H	L	L	H	H	L
L	H	Φ	Φ	Φ	Φ	L	H	H	L	H	H	H
L	H	Φ	Φ	Φ	Φ	L	H	L	H	H	H	H
L	H	Φ	Φ	Φ	Φ	L	H	H	H	H	H	L
L	H	Φ	Φ	Φ	Φ	H	L	H	H	H	H	H
L	H	Φ	Φ	Φ	Φ	H	H	H	H	H	H	H
H	H	Φ	Φ	Φ	Φ	Φ	H	H	H	H	H	H
L	L	H	H	L	L	Φ	H	H	H	L	L	L
H	L	Φ	Φ	Φ	Φ	L	H	L	H	L	L	H
H	L	Φ	Φ	Φ	Φ	L	H	H	L	L	L	H
H	L	Φ	Φ	Φ	Φ	L	H	L	L	L	L	L
H	L	Φ	Φ	Φ	Φ	L	H	H	H	H	H	H

Φ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

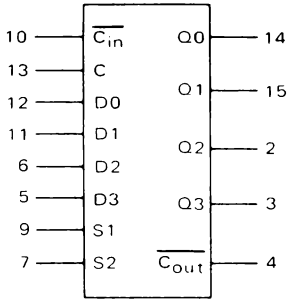
Universal Decade Counter

The MC10137 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. This decade counter is useful in high speed central processors and peripheral controllers, minicomputers, high speed digital communications equipment and instrumentation. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the present mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excersion will depend on the condition of Q1 and/or Q2.

When an output is not needed, it can be left open to conserve system power. (The open emitter output will require no power if left open.) The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is a shown in the State Diagrams.

A prescaler can be constructed using the MC10137 in conjunction with the MC10231 which will operate at over 200 MHz input frequency. A 1000 MHz prescaler is possible using an MC1699 1GHz divide by 4, an MC12013 500 MHz divide by 10-11, and the MC10137



SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	◌	H	H	H	H	L	H
L	H	◌	◌	◌	◌	L	H	L	L	L	H	H
L	H	◌	◌	◌	◌	L	H	H	L	L	H	L
L	H	◌	◌	◌	◌	L	H	L	L	L	L	H
L	H	◌	◌	◌	◌	L	H	H	L	L	L	H
L	H	◌	◌	◌	◌	H	L	H	L	L	L	H
L	H	◌	◌	◌	◌	H	H	H	L	L	L	H
H	H	◌	◌	◌	◌	◌	H	H	L	L	L	H
L	L	H	H	L	L	◌	H	H	H	L	L	H
H	L	◌	◌	◌	◌	L	H	L	H	L	L	H
H	L	◌	◌	◌	◌	L	H	H	L	L	L	H
H	L	◌	◌	◌	◌	L	H	L	L	L	L	L

◌ Don't care

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom

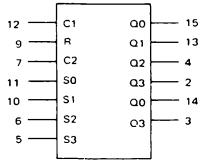
** A clock H is defined as a clock input transition from a low to a high logic level

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 Mhz typ

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)



COUNTER TRUTH TABLES

BI-QUINARY
(Clock connected to C2 and Q3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

BCD
(Clock connected to C1 and Q0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

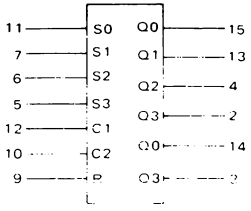
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

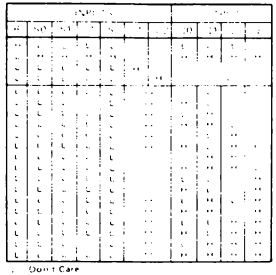
Bi-Quinary Counter

The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.



TRUTH TABLE



Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 370 mW typ/pkg (No Load
f_{tog} = 150 MHz (typ)

Binary Counter

The MC10178 is a four-bit counter capable of divide-be-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.
Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronouse "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

Binary Counter

The MC1654 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or a divide-by-16 functions. When used independently, the divide-by-16 section will toggle at 325 MHz typically. Clock inputs rigger on the positive going edge of the Clock pulse.

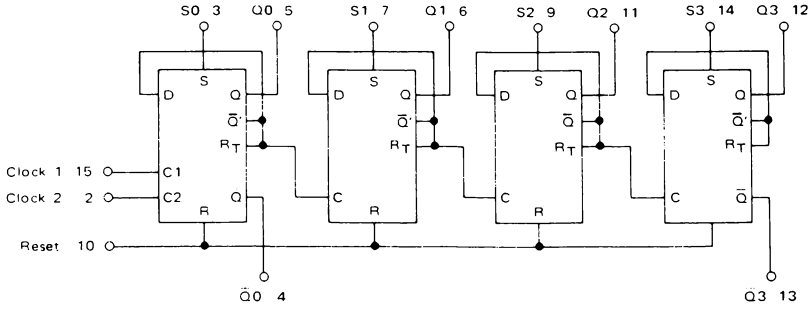
Set and Reset inputs override the Clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
1	0	0	0	0	φ	φ	0	0	0	0
0	1	1	1	1	φ	φ	1	1	1	1
0	0	0	0	0	1	φ	No Count			
0	0	0	0	0	φ	1	No Count			
0	0	0	0	0	••		0	0	0	0
0	0	0	0	0	••		1	0	0	0
0	0	0	0	0	••		0	1	0	0
0	0	0	0	0	••		1	1	0	0
0	0	0	0	0	••		0	0	1	0
0	0	0	0	0	••		1	0	1	0
0	0	0	0	0	••		0	1	1	0
0	0	0	0	0	••		1	1	1	0
0	0	0	0	0	••		0	0	0	1
0	0	0	0	0	••		1	0	0	1
0	0	0	0	0	••		0	1	0	1
0	0	0	0	0	••		1	1	0	1
0	0	0	0	0	••		0	0	1	1
0	0	0	0	0	••		1	0	1	1
0	0	0	0	0	••		0	1	1	1
0	0	0	0	0	••		1	1	1	1

φ = Don't Care

•• V_{IL} → V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.



Power Dissipation = 750 mW typ
f_{Tog} = 325 MHz typ

V_{CC} = 1, 16
V_{EE} = 8

Bi-Quinary Counter

The MC1678 is a four-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 functions. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.*

COUNTER TRUTH TABLES

BCD

(Clock connected to C1 and $\bar{Q}0$ connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY

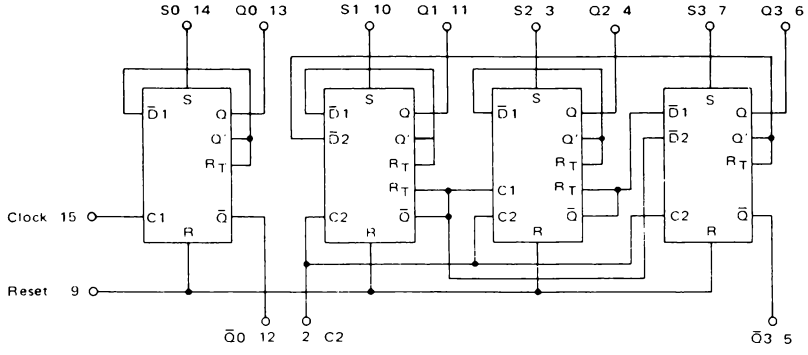
(Clock connected to C2 and Q3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

R-S

C	R	S	Q_{n+1}
ϕ	L	L	Q_n
ϕ	H	L	H
ϕ	L	H	H
ϕ	H	H	ND

ϕ = Don't Care
ND = Not Defined



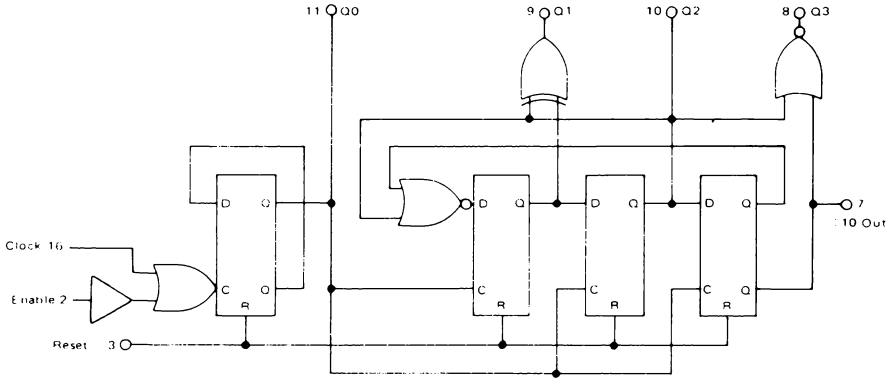
f_{Tog} = 350 MHz typ

P_D = 750 mW typ

1-GHz Divide-by-ten Counter

The MC1696 is a gigahertz bi-quinary decade counter. Its features include clock enable, BCD decoded outputs, and reset. The clock input is internally referenced to −4.2 volts, and requires an a c coupled sinewave input of 800 millivolts peak to peak (typical). The enable input can be driven with a MECL III gate and is ORed with clock input. The reset operates only when either the clock or the enable is high.

A divide-by-ten output (60%/40% high/-low duty cycle) connects to following MECL III or MECL 10,000 circuits for longer counter chains. Additional outputs decoded to standard BCD are available for decoding or display driving. These BCD outputs will not follow the MC1696 operating at top speed, but would normally be read after the counter is stopped.



f_{tog} = 1.2 GHz typ
P_D = 650 mW typ/pkg (No Load)
Output Rise and Fall Times = 1.0 ns (20%/o to 80%/o)

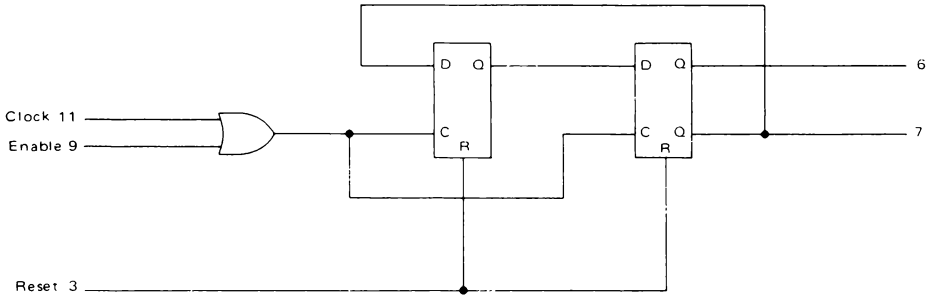
V_{CC1} = Pin 4
V_{CC2} = Pin 5
V_{EE1} = Pin 13
V_{EE2} = Pin 12
Bias Point = Pin 1

Divide-by-four Gigahertz Counter

The MC1699 is a divide-by-four gigahertz counter. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

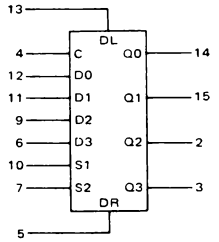
The MC1699 includes clock enable and reset, which are both compatible with MECL III voltage levels. Reset operates only when either the clock or the enable is high.

Pin 13 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.



f_{Tog} = 1.6 MHz typ
P_D = 320 mW Typ/Pkz
(No load −7.0 V supply)

V_{CC1} = Pin 4
V_{CC2} = Pin 5
V_{EE} = Pin 12
Bias Point = Pin 13



TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).

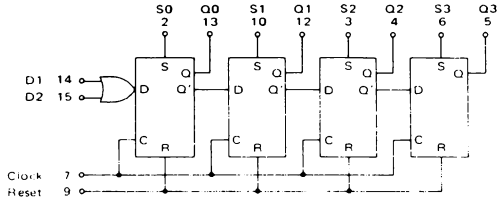
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 425 mW typ/pkg (No Load)
f_{Shift} = 200 MHz typ

Four-Bit Universal Shift Register

The MC10141 is a four-bit universal shift register which performs shift left, or shit right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). All four outputs are capable of driving 50 ohm lines.

When the register is used for serial output only, the unused emitter follower outputs can be left open.



FLIP-FLOP TRUTH TABLE

Inputs				Output
D	C	R	S	Q_n
0	0	0	0	Q_{n-1}
0	0	0	1	1
0	0	1	0	0
0	0	1	1	*
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	*
1	0	0	0	Q_{n-1}
1	0	0	1	1
1	0	1	0	0
1	0	1	1	*
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	*

*Output State Undefined

V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

Total Power Dissipation = 750 mW typ/pkg
Shift Frequency = 325 MHz typ

4-Bit Shift Register

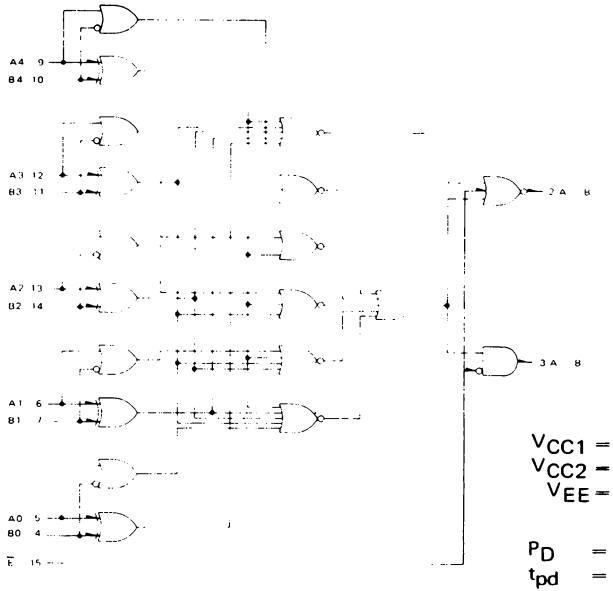
The MC1694 is a 4-Bit register capable of shift rates up to 325 MHz (typical). This shift register operates in the shift-right mode, accepting serial data at either data input D1 or D2. A master reset and individual set inputs override the clock allowing asynchronous entry of information.

5-Bit Magnitude Comparator

The MC10166 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided A < B and A > B. A – B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.

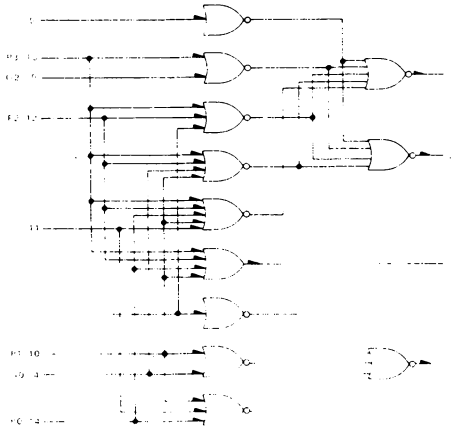
TRUTH TABLE

Inputs			Outputs	
$\bar{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A < Word B		L	H
L	Word A > Word B		H	L



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 440 mW typ/pkg (No Load)
t_{pd} = Data to output 6.0 ns typ
$\overline{E}$ to output 2.5 ns typ

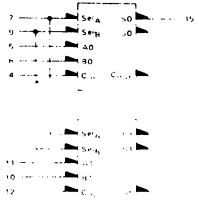


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 300 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Carry, Propagate)
4.0 ns typ (Generate)

Look-Ahead Carry Block

The MC10179 device has 12 low power gates internally connected to perform the lock-ahead carry function. This device has high Σ input pulldown resistors and open emitter outputs. This device has applications in fast look-ahead adders such as with the MC10181. It can be used also as a boolean function generator.



TRUTH TABLE

FUNCTION	INPUTS					OUTPUTS	
	Sel_A	Sel_B	A0	B0	C_{in}	S0	$\overline{S0}$	C_{out}
ADD	L	L	L	L	L	L	H	L
	L	L	H	L	L	H	L	L
	L	L	L	H	L	H	L	L
	L	L	H	H	L	L	H	H
	L	L	L	L	H	H	L	L
	L	L	H	L	H	L	H	H
	L	L	L	H	H	L	H	H
	L	L	H	H	H	H	L	H
SUBTRACT	H	H	L	L	L	L	H	L
	H	H	H	L	L	H	L	L
	H	H	L	H	L	H	L	L
	H	H	H	H	L	L	H	H
	H	H	L	L	H	H	L	L
	H	H	H	L	H	L	H	H
	H	H	L	H	H	L	H	H
	H	H	H	H	H	H	L	H
REVERSE SUBTRACT	H	L	L	L	L	H	L	H
	H	L	H	L	L	L	H	L
	H	L	L	H	L	L	H	L
	H	L	H	H	L	H	L	H
	H	L	L	L	H	L	H	H
	H	L	H	L	H	H	L	H
	H	L	L	H	H	H	L	H
	H	L	H	H	H	L	H	H
	L	H	L	L	L	H	L	L
	L	H	H	L	L	L	H	L
	L	H	L	H	L	L	H	L
	L	H	H	H	L	H	L	H
	L	H	L	L	H	H	L	H
	L	H	H	L	H	L	H	H
	L	H	L	H	H	L	H	H
	L	H	H	H	H	H	L	H

FUNCTION SELECT TABLE

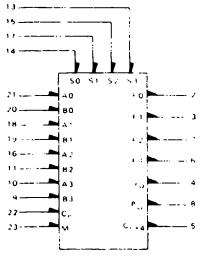
Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

P_D = 360 mW typ/pkg (No Load)
t_{pd} (typ)
C_{in} to C_{out} = 2.2 ns
A0 to S0 = 4.5 ns
A0 to C_{out} = 4.5 ns

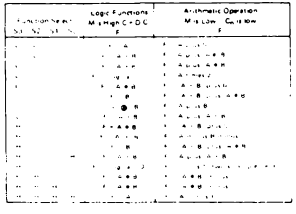
Dual 2-Bit Adder/Subtractor

The MC10180 is a high speed, low power general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays. The MC10180 can be used in any piece multiplier arrays. The MC10180 can be used in any piece of equipment where these operations are necessary.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B. The speed is very fast, with Carry-in to Carry-out propagation delay of 2.2 ns and Operand in to Sum or Carry-out propagation delay of 4.5 ns.



POSITIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 24
V_{EE} = Pin 12

P_D = 600 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 6.5 ns
C_n to C_{n-4} = 3.1 ns
A1 to P_G = 5.0 ns
A1 to G_G = 4.5 ns
A1 C_{n-4} = 5.0

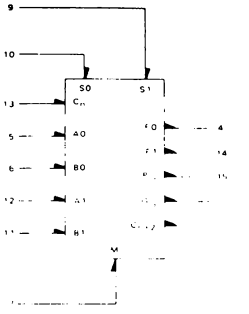
4-Bit Arithmetic Logic Unit/Function Generator

The MC10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions.

Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.

2-Bit Arithmetic Logic Unit/Function Generator



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

Function Select		POSITIVE LOGIC	
		Logic Function	Arithmetic Operation
		M = High	M = Low
S1	S0	F	F
L	L	F = A ⊕ B	F = A plus B plus Carry
L	H	F = A ⊙ B	F = A plus B plus Carry
H	L	F = A • B	F = A plus B plus Carry
H	H	F = A + B	F = A times 2

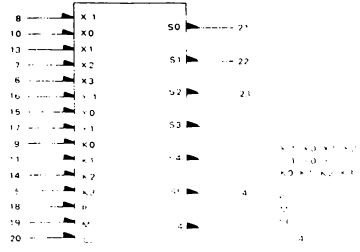
P_D = 575 mW typ/pkg (No Load)
t_{pd} (typ): A1 to F = 7.5 ns
C_n to C_{n-2} = 2.7 ns
A1 to P_G = 6.5 ns
A1 to G_G = 5.5 ns
A1 to C_{n-2} = 7.0 ns

The MC10182 is a high-speed arithmetic logic unit capable of performing 4 logic operations and 4 arithmetic operations on two 2-bit words. Full internal carry is incorporated for arithmetic operation.
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided for a second order look ahead carry using the MC10179. The internal carry is enabled by applying a low level voltage to the mode control input (M).
The MC10182 provides an alternate to the MC10181 four-bit ALU for applications not requiring the extended functions of the MC10181 or for applications requiring a 16-pin package. The MC10182 also differs from the MC10181 in that Word A and B are treated equally for addition and subtraction(A plus B, A minus B, B minus A).
(Continued in next page.)

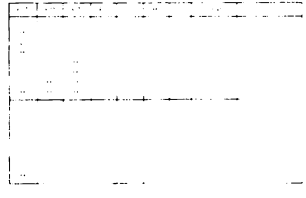
TRUTH TABLE

Input	M	L	L	L	L	H	H	H	H
	S1	L	L	H	H	L	L	H	H
	S0	L	H	L	H	L	H	L	H
A1 B1 A0 B0 C_n		F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}	F1 F0 P_G G_G C_{n+2}
L L L L L		L L H L L	H H L H L	H H L H L	L L H L L	H H L H L	L L H L L	L L L H L	L L L H L
L L L L H		L L H L L	L L L H H	H H L H H	L L H L L	H H L H L	L L L H H	L L L L L	L H H L L
L L L H L		L L H L L	L L H H H	H H L H H	L L H L L	H H L H L	L L H H H	L L L L L	L H H L L
L L L H H		L L H L L	L L H H H	H H L H H	L L H L L	H H L H L	L L H H H	L L L L L	L H H L L
L L H L L		L L H L L	H H L H L	L L H H H	L L H L L	H H L H L	L L H H L	L L L H L	L H H L L
L L H L H		L L H L L	H H L H L	L L H H H	L L H L L	H H L H L	L L H H L	L L L H L	L H H L L
L L H H L		L L H L L	H H L H L	L L H H H	L L H L L	H H L H L	L L H H L	L L L H L	L H H L L
L L H H H		L L H L L	H H L H L	L L H H H	L L H L L	H H L H L	L L H H L	L L L H L	L H H L L
L H L L L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
L H L L H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
L H L H L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
L H L H H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
L H H L L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
L H H H L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
L H H H H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L L L L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L L L H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L L H L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L L H H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L H L L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L H L H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L H H L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H L H H H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H L L L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H L L H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H L H L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H L H H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H H L L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H H L H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H H H L		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L
H H H H H		H L H L L	L L H H H	L H H L L	L H H L L	H L H L L	H L H L L	L L L H L	H L H L L

These outputs are not normally used during logic operation.



TRUTH TABLE



V_{CC} = Pin 24
V_{EE} = Pin 12

P_D = 760 mW typ/pkg (No Load)
t_{pd} = 50 ns typ (8 x 8 bit product)

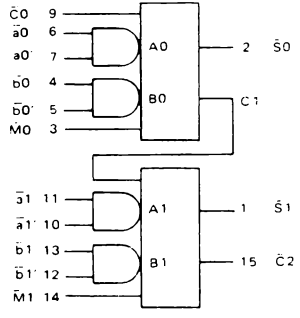
4 x 2 Multiplier

The MC10183 is a 4 x 2 bit multiplier that can multiply 2's complement numbers producing a 2's complement product without correction. The device can be used as a 4 x 2 bit multiplier cell to build larger iterative arrays.

The part performs the function defined as $F = XY + K$, where K is an input fiels used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is a modified Booth's algorithm or multiplier coding technique.

The device consists of a shift network and an adder/subtractor in which 0, 1 times X, or 2 times X is either added or subtracted to input constant K. The Y inputs control multiplication as shown in the Truth Table. The most significant digit in a word carries a negative weight allowing 2's complement numbers of various lenghts to be multiplied. An M-bit by N-bit multiplication produces an M + N bit product.

The $\overline{P}$ polarity input allows multiplication in either positive logic ($\overline{P}$ = high) or negative logic ($\overline{P}$ = low) representation. Also, mode control M inverts $\overline{C}_n$ when high and passes $\overline{C}_n$ directly when left low.



V_{CC} = Pin 16
V_{EE} = Pin 8

P_D = 400 mW typ/pkg (No Load)
t_{pd}: (Outputs loaded 1 kΩ to V_{EE})
C0 to C2 1.7 ns typ
a0 to C2 2.8
a0 to S0 2.7
b0 to S0 3.1
a0 to S1 3.9
b0 to S1 4.4
M0 to S1 8.7

High Speed
2 x 1 Bit Array Multiplier Block

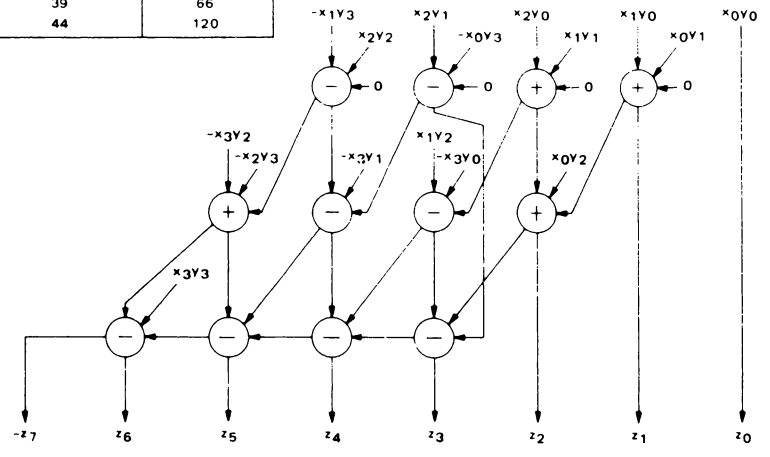
The MC10287 is a dual high speed iterative multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

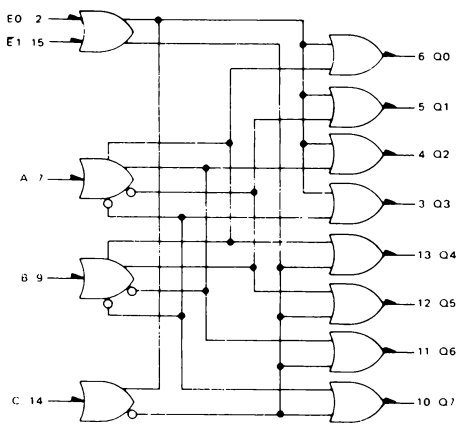
An addition or subtraction is selected by mode controls (M0, M1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M0 and M1 cause addition.

TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT 2's COMPLEMENT ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

4-BIT BY 4-BIT 2's COMPLEMENT ARRAY MULTIPLIER





V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

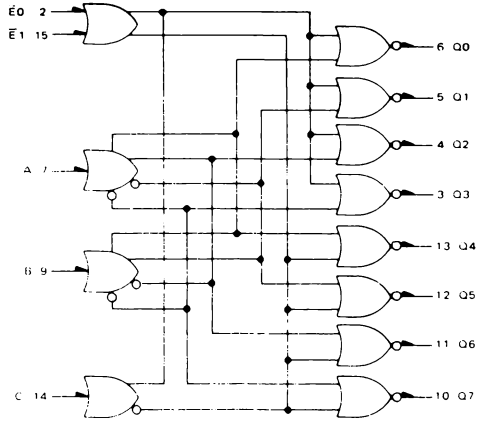
Binary to 1-8 Decoder (Low)

The MC10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high. This device has high Z input pulldown resistors and open emitter outputs.

TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E1}$	$\overline{E0}$	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Φ	Φ	Φ	Φ	H	H	H	H	H	H	H	H
Φ	H	Φ	Φ	Φ	H	H	H	H	H	H	H	H

Φ = Don't Care



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ

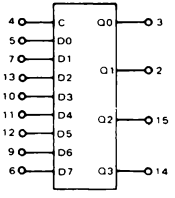
Binary to 1-8 Decoder (High)

The MC10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

TRUTH TABLE

INPUTS					OUTPUTS							
Ē0	Ē1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	○	○	○	○	L	L	L	L	L	L	L	L
○	H	○	○	○	L	L	L	L	L	L	L	L

○ Don't Care



TRUTH TABLE

DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	Φ	Φ	Φ	Φ	Φ	Φ	Φ	H	L	L	L
L	H	Φ	Φ	Φ	Φ	Φ	Φ	H	L	L	H
L	L	H	Φ	Φ	Φ	Φ	Φ	H	L	H	L
L	L	L	H	Φ	Φ	Φ	Φ	H	L	H	H
L	L	L	L	H	Φ	Φ	Φ	H	H	L	L
L	L	L	L	L	H	Φ	Φ	H	H	L	H
L	L	L	L	L	L	H	Φ	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

Φ = Don't Care

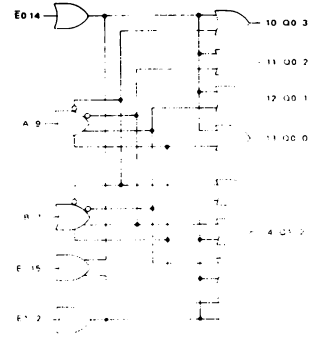
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 545 mW typ/pkg (No Load)
t_{pd} = 7.0 ns typ (Data to Output)

8-input Priority Encoder

The MC10165 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e.g. the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The MC10165 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.



TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
E	E0	E1	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	H	H	H	L	H	H	H	L
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	H	L	H	H	H	L	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	L
L	H	L	H	L	H	H	L	H	H	H	L	H
L	H	L	L	H	H	L	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	L	H	H	H
H	D	D	D	D	H	H	H	H	H	H	H	H

D Don't Care

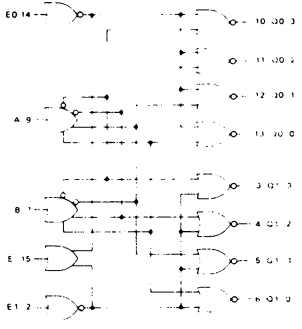
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Dual Binary to 1-4 Decoder (Low)

The MC10171 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}0$ or $\overline{E}1$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

All propagation delay times are equal due to the internal emitter dotting techniques used. High impedance 50 k ohm resistors on all inputs eliminate the need to tie unused inputs to V_{EE}.



TRUTH TABLE

Ē	Ē1	Ē0	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
H	X	X	X	X	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	L
L	H	H	L	H	H	H	L	H	H	H	L	H
L	H	H	H	L	H	L	H	H	H	L	H	H
L	H	H	H	H	L	H	H	H	L	H	H	H
L	H	L	L	L	H	H	H	L	H	H	H	L
L	H	L	L	H	H	H	L	H	H	H	L	H
L	H	L	H	L	H	L	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	L	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H	L
L	L	H	L	H	H	H	L	H	H	H	L	H
L	L	H	H	L	H	L	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H
L	L	L	L	L	H	H	H	L	H	H	H	L
L	L	L	L	H	H	H	L	H	H	H	L	H
L	L	L	H	L	H	L	H	H	H	L	H	H
L	L	L	H	H	L	H	H	H	L	H	H	H

X = Don't Care

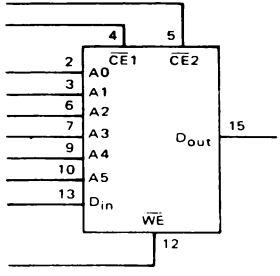
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 325 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

Dual Binary to 1-4 Decoder (High)

The MC10172 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either $\bar{E}0$ or $\bar{E}1$ low, the corresponding selected 4 outputs are low. The common enable $\bar{E}$, when high, forces all outputs low.

All propagation delay times are equal. High impedance 50 k ohm resistors on all inputs eliminate the need to tie unused inputs to V_{EE}.



TRUTH TABLE

MODE	INPUT			OUTPUT
	CE	WE	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

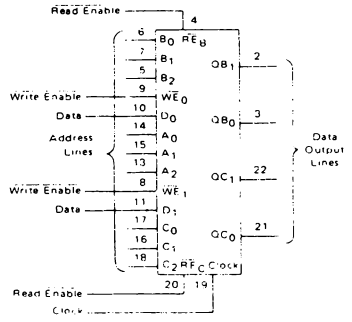
P_D = 420 mW typ/pkg
Access Time = 10 ns max (MCM10142)
= 15 ns max (MCM10140–10148)

64-Bit Random Access Memory

The MC10140, MCM10142 ans MCM10148 are 64-Bit Random Access Memories (RAMs). They offer very high speed, full binary decoding, two chip enable inputs for easy memory expansion, and separate data input and data output pins.

Organization of these memories is 64 one-bit words and they are package in standard 16-pin hermetic dual in-line packages.

MCM10142 and MCM10148 logic levels are fully compatible with the MECL 10,000 logic family and are specified for driving a 50 ohm load. The MCM10140 logic levels are compatible with the MECL 10,000 logic family except they are specified for driving a 90 ohm load.



t_{pd}: Clock to Data out = 5 ns (typ)
(Read Selected)
Address to Data out = 10 ns (typ)
(Clock High)
$\overline{\text{Read Enable}}$ to Data out = 3.5 ns
(Clock high, Addresses present)

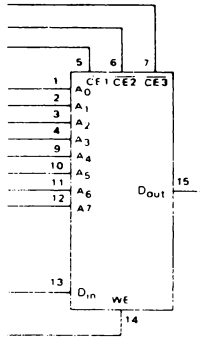
P_D = 610 mW typ/pkg

8 x 2 Multiport Register File (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE – The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0–A_2.

READ – When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).



TRUTH TABLE

MODE	INPUT			OUTPUT
	CE	WE	Din	Dout
Write 0	L	L	L	L
Write 1	*	L	H	L
Read	L	H	*	D
Disabled	H	*	*	L

Don't Care

t_{Access} = 18 ns (typ) (Address Inputs)

256-Bit Random Access Memory

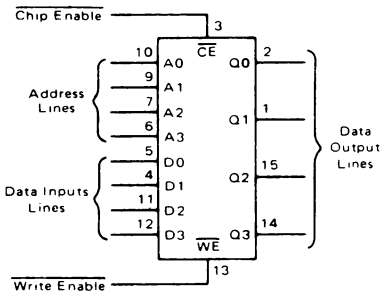
The MCM10144 is a fully decoded 256-bit Random Access Read/Write Memory organized as 256 one bit words. Stored data is selected by means of an eight bit address, consisting of inputs A0 through A7.

The MCM10144 has three active-low chip enable inputs for increased logic flexibility permitting memory expansion up to 2048 words without additional decoding. For larger memories, the upper address words are selected by using one of the $\overline{CE}$ inputs for enabling 1024 word segments.

The MCM10144 operating mode (all $\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the WRITE mode, the output, D_{out}, is low and the data state present at the data input (pin 13) is stored at the selected address. With the $\overline{WE}$ high the chip is in the READ mode and the data state at the selected memory location will be presented, noninverted at the data output (pin 15).

Open emitter outputs permit full *wire-ORing* to data buses, with D_{out} low when the chip is disabled.

The device is fully compatible with the MECL 10,000 logic family. It is designed for use in high speed scratch pad, control, cache, and buffer storage applications.



TRUTH TABLE

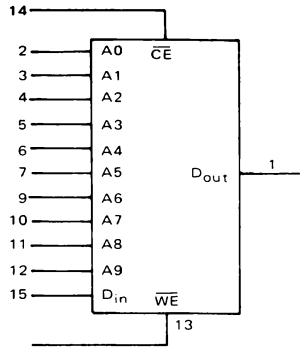
MODE	INPUT			OUTPUT
	CE	WE	D	Q
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

P_D = 625 mW typ/pkg
Access Time = 10 ns typ

64-Bit Register File (RAM)

The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MC10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The Write Enable input, when low, allows data to be entered; when high, disables the data inputs. The Chip Enable input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The Chip Enable, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ø	Q
Disabled	H	ø	ø	L

ø = Don't Care

Access Time: 22 ns typ
P_D = 510 mW/pkg. typ

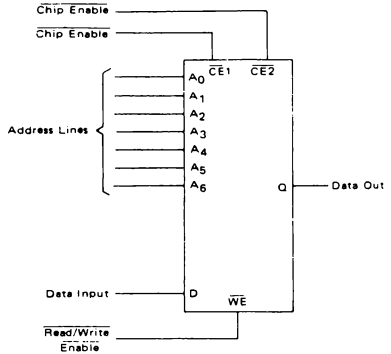
1024-Bit Random Access Memory

The MCM10146 is a fully decoded 1024-bit Random Access Read/Write Memory organized as 1024 one bit words. Stored data is selected by means of a ten bit address, consisting of inputs A0 through A9.

The MCM10146 has an active-low chip enable input ($\overline{CE}$). The operating mode ($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the WRITE mode, the output, D_{out}, is low and the data state present at the data input (pin 15) is stored at the selected address. With the $\overline{WE}$ high the chip is in the READ mode and the data state at the selected memory location will be presented, noninverted at the data output (pin 1).

Open emitter output permits full *wire-ORing* to data buses, with D_{out} low when the chip is disabled.

The device is fully compatible with the MECL 10,000 logic family. It is designed for use in high speed scratch pad, control, cache, and buffer storage applications.



TRUTH TABLE

MODE	INPUT				OUTPUT
	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L	L
Write "1"	L	L	L	H	L
Read	L	L	H	ϕ	Q
Disabled	H	L	ϕ	ϕ	L
	L	H	ϕ	ϕ	L

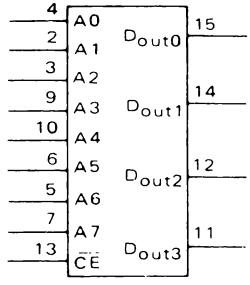
ϕ = don't care

P_D = 415 mW typ/pkg
t_{Access} = 10 ns typ

128-1-Bit Random Access Memory

The MCM10147 is a 128-bit RAM organized as a 128-word by 1-bit array. This organization and the high speed of this MECL 10,000 device make the MCM10147 particularly useful in fast scratch pad, register file, and buffer memory applications. Full address decoding, and two Chip Enables ($\overline{CE}$) are included in this device to permit simple memory expansion.

For writing Data (D) into this memory, both Chip Enables $\overline{CE1}$ and $\overline{CE2}$ are brought low, the address is presented at A0-A6, and the Read/Write Enable ($\overline{WE}$) is taken low while Data is valid. To read a particular address, both Chip Enable inputs must again be low, but the Read/Write input is high (Data input disabled) while the location is addressed.
The two Chip Enables are provided for row or column selection of device packages in an expanded memory system. Either input can be used to select a particular row or column of stored data bits.
Open emitter outputs permit full wire-ORing to data buses, with the output being held low when either Chip Enable is high. Internal input pulldown resistors are not used on this device. Unused inputs should be tied to V_{EE}.

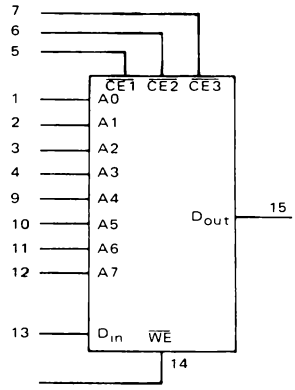


T_{pd}: 25 ns max
P_D : 540 mW

1024-Bit Programmable Read only Memory

The MCM10149 is a 1024 bit programmable read only memory (PROM). The circuit is organized as 256 words of four bits. Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The MCM10149 has a single negative logic chip enable. When the chip is disabled ($\overline{CE}$ = high), all outputs are forced to a logic 0 (low).

The MCM10149 is fully compatible with the MECL 10,000 logic family. It is designed for use in mircro-programming, code conversion, logic simulation, and look-up table storage.



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CE}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

P_D = 520 mW/pkg. typ
Access Times: 12 ns typ

High Speed 256-Bit Random Access Memory

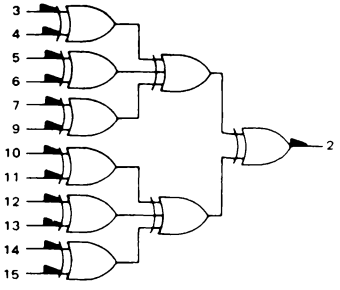
The MCM10152 is a fully decoded 256-bit Random Access Read/Write Memory organized as 256 one bit words. Stored data is selected by means of an eight bit address, consisting of inputs A0 through A7.

The MCM10152 has three active-low chip enable inputs for increased logic flexibility permitting memory expansion up to 2048 words without additional decoding. For larger memories, the upper address words are selected by using one of the $\overline{CE}$ inputs for enabling 1024 word segments.

The MCM10152 operating mode (all $\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the WRITE mode, the output, D_{out}, is low and the data state present at the data input (pin 13) is stored at the selected address. With the $\overline{WE}$ high the chip is in the READ mode and the data state at the selected memory location will be presented, noninverted at the data output (pin 15).

Open emitter outputs permit full *wire-ORing* to data buses, with D_{out} low when the chip is disabled.

The device is fully compatible with the MECL 10,000 logic family. It is designed for use in high speed scratch pad, control, cache, and buffer storage applications.



INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

V_{CC1} – Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

12-Bit Parity Generator-Checker

The MC10160 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

Error Detection-Correction Circuit

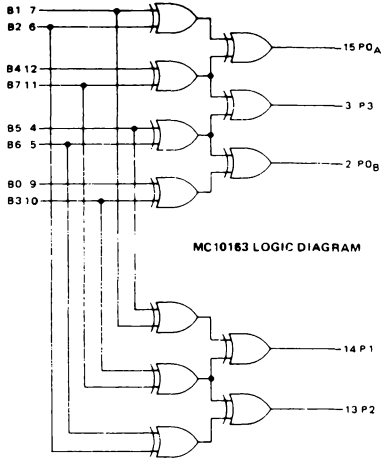
The MC10163 and the MC10193 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for mainframe and add-on memory systems. For example, using eight MC10163's together with eight 12-bit parity checkers (MC10160), single-bit error detection/correction and double-bit error detection can be done on a word of 64-bit lenght. Only eight check bits (B0-B7) need be added to the word. A useful feature of this building block is that the MC10193 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

IBM CODE

$P0_A$ = B1, B2, B4, B7
$P0_B$ = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7

MOTOROLA CODE

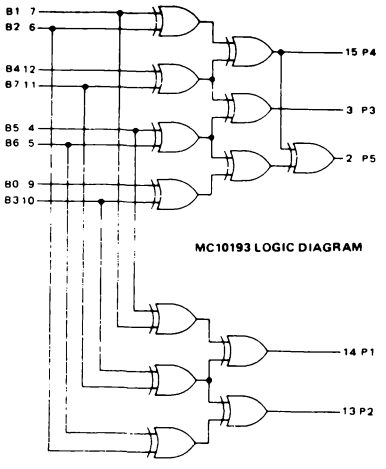
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P4 = B1, B2, B4, B7
P5 = Byte (B0, 1, 2, 3, 4, 5, 6, 7)



MC10163 LOGIC DIAGRAM

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

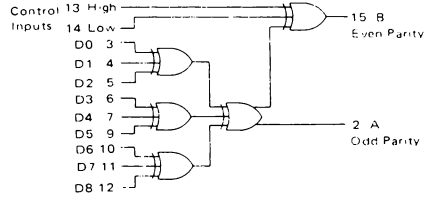
P_D = 250 mW typ/pkg (No Load)
t_{pd} = 7.5 ns typ (pin 7 to pin 2)



MC10193 LOGIC DIAGRAM

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 520 mW typ/gate (No Load)
t_{pd} = 5.0 ns typ



INPUTS	OUTPUTS	
Sum of D Inputs at High Level	Odd Parity Output A	Even Parity Output B
Even	Low	High
Odd	High	Low

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

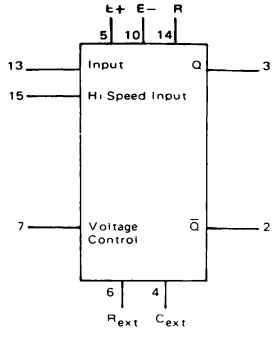
P_D = 300 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Control Inputs to B Output)
4.0 ns typ (Data Inputs to A Output)
6.0 ns typ (Data Inputs to B Output)

9 + 2-Bit Parity Generator-Checker

The MC10170 is a 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits. The function is particularly useful for byte organized systems such as disc and tape systems.

Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's. The MC10170 can generate both even and odd parity.



+ Enable	− Enable	Output
0	0	Triggers on both pos. and neg. input slopes
0	1	Triggers on pos. input slope.
1	0	Triggers on neg. input slope
1	1	Trigger is disabled.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 415 mW typ/pkg (no Load)
Total PW range = $<$6 ns to $>$ 10 ms

Retriggerable One-Shot Multivibrator

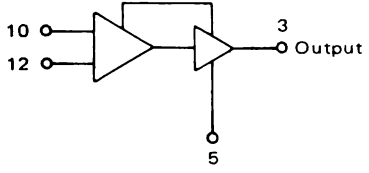
The MC10198 is a retriggerable on-shot MECL 10,000 multivibrator. Two input enables are provided, to permit triggering on positive slope, negative slope, both, or neither. Triggering of this device produce an output pulse with a duration fixed by a choice of an external R-C section and/or voltage.

The timing decade is set by a choice of capacitance ($\sim$ 10pF – 10 μF). R is adjusted ($\sim$ 300 – 3KΩ) to set an exact time.

To use the voltage control of output pulse width, the procedure is: choose the timing decade with a value of C; set sensitivity (decades time change/volt) with R($\sim$400Ω = 2 decades; $\sim$1.8 K –1 decade, 0 to –5 V swing at voltage control input trough a 1KΩ resistor.

Input Schmidt triggers ($\sim$2 ns tpd) are included at the input to sharpen input pulse. When minimum propagation delay is required, the high speed input may be used, by passing the Schmidt triggers.

The reset overrides the inputs, an can immediately terminate an output pulse.



SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

Input Capacitance = 6 pF typ
Maximum Series Resistance
for L (External Inductance) = 50Ω typ
Power Dissipation = 150 mW typ/pkg
(+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

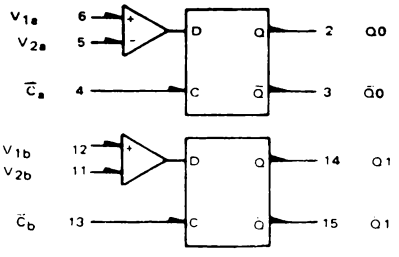
Voltage-Controlled Oscillator

The MC1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with MECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop.

This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity

The MC1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.



TRUTH TABLE

$\overline{C}$	V_1 V_2	$Q0_{n+1}$	$\overline{Q}0_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q}0_n$

ϕ = Don't Care

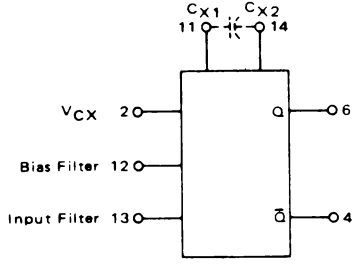
V_{CC} = +5.0 V = Pin 7, 10
V_{EE} = −5.2 V = Pin 8
Gnd = Pin 1, 16

P_D = 330 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (MC1650)
= 3.0 ns typ (MC1651)

Dual A/D Comparator

The MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability. Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$ operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.



V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 8

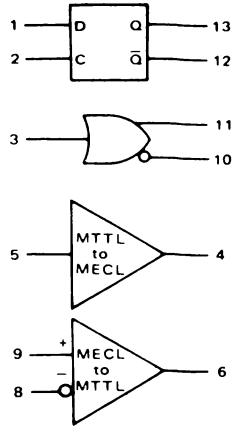
Max Frequency = 155 MHz typ
P_D = 150 mW

Voltage Controlled Multivibrator

The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The MC1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.



D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

V_{CC} = Pin 14
V_{EE} = Pin 7

Max Frequency = 250 MHz typ
P_D = 425 mW

Digital Mixer/Translator

The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. MTTL to MECL and MECL to MTTL translators are provided to familitate interfacing with MECL or MTTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 V dc or −5.2 V dc.

Two-Modulus Prescaler

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide by 5/divide by 6 prescaler; 2) a divide by 2 prescaler; and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide by N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.

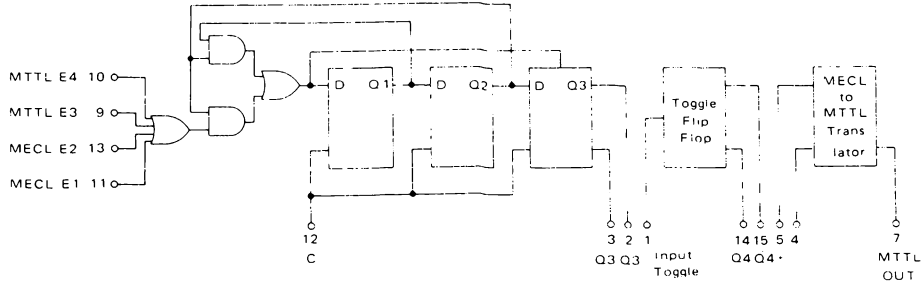
- ÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
- MECL to MTTL Translator on Chip
- +5.0 or -5.2 V Operation*
- 200 MHz (typ) Toggle Frequency

*When using +5.0 V supply, apply +5.0 V to pin 16 (V_{CC}) and ground pin 8 (V_{EE}). When using −5.2 V supply, ground pin 16 (V_{CC}) and apply −5.2 V to pin 8 (V_{EE}).

TOGGLE FLIP-FLOP

Q_n	Q_{n+1}
0	1
1	0

To obtain an MTTL output connect 5 and 4 to 2 and 3 or 14 and 15 respectively. The MECL outputs (2, 3, 14, 15) require terminating resistors. When used, the translator (4 and 5) will provide the proper termination for connection to the Toggle FF.

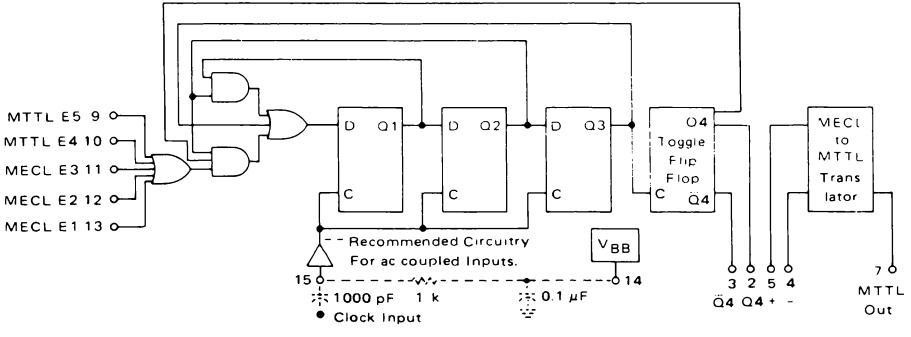


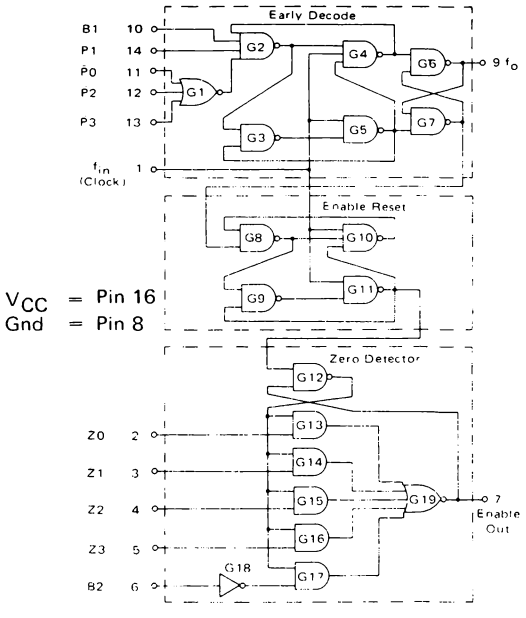
Two-Modulus Prescaler

The MC12013/12513 is a two-modulus prescaler which will divide by 10 and 11. A MECL-to-MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, the MC12013/MC12513 provides a buffered clock input and MECL bias voltage source. Details of operation are on the MC12012 data sheet.

- 600 MHz (typ) Toggle Frequency
- ÷10/11
- +5.0 or −5.2 V Operation*
- P_D = 310 mW/typ

*When using +5.0 V supply, apply +5.0 V to pin 1 (V_{CCO}), pin 6 (MTTL V_{CC}), pin 16 (V_{CC}), and ground pin 8 (V_{EE}). When using -5.2 V supply, ground pin 1 (V_{CCO}), pin 6 (MTTL V_{CC}), and pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}). If the translator is not required, pin 6 may be left open to conserve dc power drain.

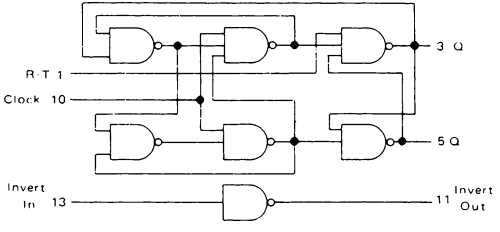




Counter Control Logic

The MC12014 monolithic counter control logic unit is designed for use with the MC12012 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014 consists of a zero detector which controls the modulus of the MC12012, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

P_D = 175 mW/typ



MC12020 • MC12520

Functional Truth Table

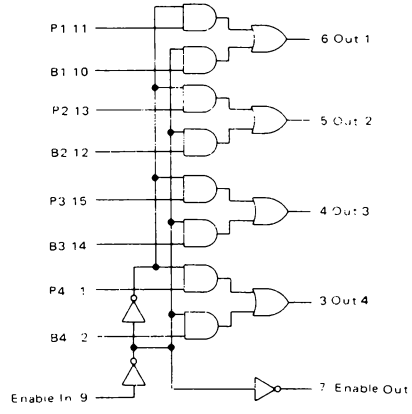
Input		Output	
R T	Clock	Q	$\bar{Q}$
0	0	0	1
0	1	1	1
1	1	1	0
1	0	1	0
1	1	0	1

V_{CC} = Pin 14 = +5.0 Vdc
Gnd = Pin 7
0 @ Clock, R-T = +0.5 Vdc
1 @ Clock, R-T = +4.0 Vdc

P_D = 50 mW/typ

Offset Control

The MC12020/MC12520 is an IF offset control block that provides a digital means of producing automatic IF offset generation for synthesizer tuned transceivers when used in conjunction with the MC12021 or MC12521. It is a modified D-type flip-flop that is capable of two modes of operation. The mode of operation is controlled by the receive/transmit input. When the R/T input is at a logical one level, the part becomes simply a toggle flip-flop and divides by two at both Q and $\bar{Q}$ outputs. With the R/T input at a logical zero level, the Q output becomes a buffer gate that follows the clock input and the $\bar{Q}$ output produces a constant one level. An inverter gate is provided which can be used to invert the clock polarity. This option is to ensure the device can always be clocked on the same edge that clears the counter presets. This device was designed for low frequency operation which allows low power operation. Its maximum current drain is 9.6 mA over temperature.



P_D = 50 mW/typ

Offset Programmer

The MC12021/MC12521 is an IF offset programmer that provides a means of producing automatic IF offset generation for synthesizer tuned transceivers when used in conjunction with the MC12020 or the MC12520 control block. The part is an eight-input, four-output data selector. It is the logic implementation of a four-pole, two position switch with the switch position controlled by the enable input. One set of input codes determine the frequency of transmission and is programmable with either switches or circuitry; the other code determines the IF offset frequency. The enable input is controlled by the Q output of the MC12020/MC12520. This device was designed for low frequency operation which allows for low power operation. Maximum current drain is 9.4 mA over temperature.

Phase-Frequency Detector

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

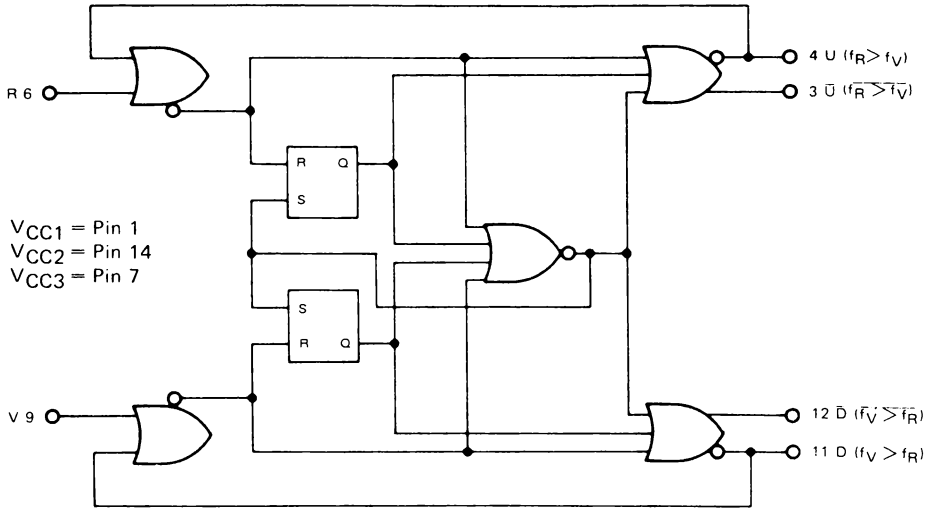
Operating Frequency = 80 MHz typical

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

X = Don't Care

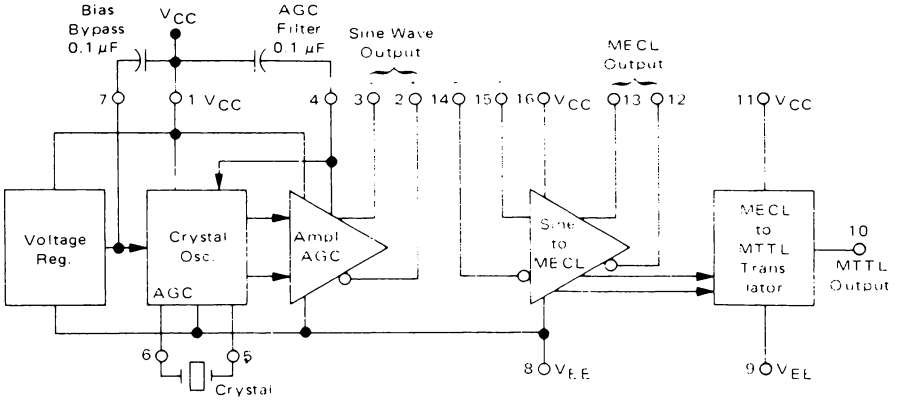
INPUT		OUTPUT			
R	V	U	D	$\overline{U}$	$\overline{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1


R 6
V 9
R
Q
S
S
R
Q
V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{CC3} = Pin 7
4 U ($f_R > f_V$)
3 $\bar{U}$ ($\overline{f_R > f_V}$)
12 $\bar{D}$ ($\overline{f_V > f_R}$)
11 D ($f_V > f_R$)

Crystal Oscillator

The MC12060/12560 and MC12061/12561 are designed for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and MTTL outputs.

- Frequency Range
  - = 100 KHz to 2.0 MHz for MC12060/12560
  - = 2.0 MHz to 20 MHz for MC12061/12561
- Temperature Range
  - = −55 °C to +125 °C for MC12560/12561
  - = 0 °C to +70 °C for MC12060/12061
- Single Supply Operation:
  +5.0 Vdc or 5.2 Vdc
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVp-p typ)
  2. Complementary MECL
  3. Single Ended MTTL

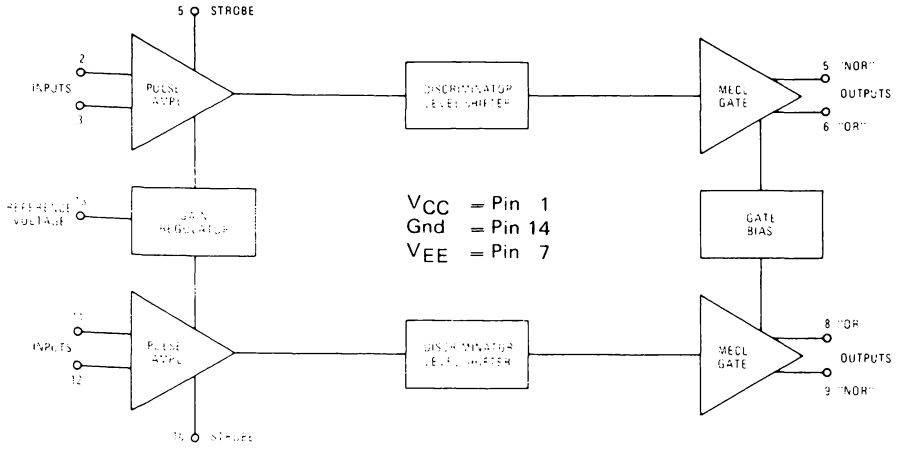


Note: 0.1 μF power supply pin bypass capacitors not shown.

Dual Sense Amplifier

... a dual dc coupled sense amplifier providing output levels compatible with emitter-coupled logic levels. The Mc1543L offers adjustable threshold and excellent threshold stability over a wide range of power-supply voltage variation.

- Input Threshold — Adjustable from 10 to 40 mV (Positive or Negative Signals)
- Both OR and NOR Outputs Available
- Low Power Dissipation
- Threshold Insensitive to V_{CC} or V_{EE} Voltage Variation
- Each Amplifier is Separately Strobed



Power Supply Currents
($V_2 = V_3 = V_{11} = V_{12} = V_{14} = 0$)
I_{CC} = 9.5 mAdc/typ
I_{EE} = 26.5 mAdc/typ

Propagation Delay (Input to Output)
t_{IO} = 28 ns/typ

Propagation Delay (Strobe to Output)
t_{SO} = 16 ns/typ

STANDARD APPLICATION

K SUFFIX
CASE 11 61

P SUFFIX
CASE 199 04

Output Voltage +25°C
5.2 V typ (MC7905.2)
2 V typ (MC7902)

Load Regulation
T_J +25°C, 5.0 mA ≤ I_O ≤ 1.5 A
12 mV typ
250 mA ≤ I_O ≤ 750 mA
4.5 mV typ

Output Noise Voltage (T_A +25°C, 10Hz ≤ f ≤ 100 KHz)
42 μV typ

Negative Voltage Regulators

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.
Available in fixed output voltage options from −2.0 to −24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation − making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 199-04 (Pin Compatible with the VERSAWATT or TO-220) Or Hermetic TO-3 Type Metal Power Package.

MECL 10,000 LITERATURE

DATA SHEETS – With complete performance parameters, plus logic truth tables, test circuits and circuit application tips.

MECL DATA BOOK – Periodically updated. Includes data sheets for all MECL 10,000 devices as well as MECL III and other compatible devices.

THE MECL SYSTEM DESIGN HANDBOOK – Written by Motorola application engineers to provide designers with information on how to use MECL most effectively in a high performance logic system. Gives reasons for using MECL, answers questions, lists design rules, elaborates on types of equipment which benefit from MECL's high level of performance.

MECL 10,000 APPLICATION NOTES

AN-504 – The MC1600 Series MECL III Gates.
AN-532A – MTTL & MECL Avionics Digital Frequency Synthesizer.
AN-534 – Commutating Filter Techniques.
AN-553 – A New Generation of Integrated Avionic Synthesizers.
AN-556 – Interconnection Techniques for MECL 10K.
AN-564 – An ADF Frequency Synthesizer Utilizing Phase Locked Loop IC's.
AN-565 – Using Shift Registers as Pulse Delay Networks.
AN-566 – High-Speed Binary Multiplication Using the MC10181.
AN-567 – MECL Positive & Negative Logic.
AN-572A – Initial Reliability Report for MECL 10K.
AN-573 – Engineering Report: A Comparison Between MECL 10K and Schottky TTL Minicomputer Designs.
AN-579 – Testing MECL 10K.
AN-581 – An 8-Digit 500 MHz Frequency Counter.
AN-583 – A Mainframe Memory System with MECL 10K Control Logic.
AN-584 – Programmable Counters Using the MC10136 & MC10137 (100 MHz).
AN-586 – Measure Frequency & Propagation Delay with MECL.

AN-592 – AC Noise Immunity of MECL 10K (Ref. AN-298).
AN-700 – Simulate MECL System Interconnections with a Computer Program.
AN-701 – Understanding MECL 10,000 DC and AC Data Sheet Specifications.
AN-709 – MECL 10,000 Arithmetic Elements – MC10179, MC10180, MC10181.
AN-720 – Interfacing with MECL 10,000 Integrated Circuits.
AN-726 – Bussing with MECL 10,000 Integrated Circuits.
AN-730 – A High-Speed FIFO Memory Using the MECL MCM10143 Register File.
AN-742 – A 200 MHz autoranging MECL – Mc Mos Frequency counter.