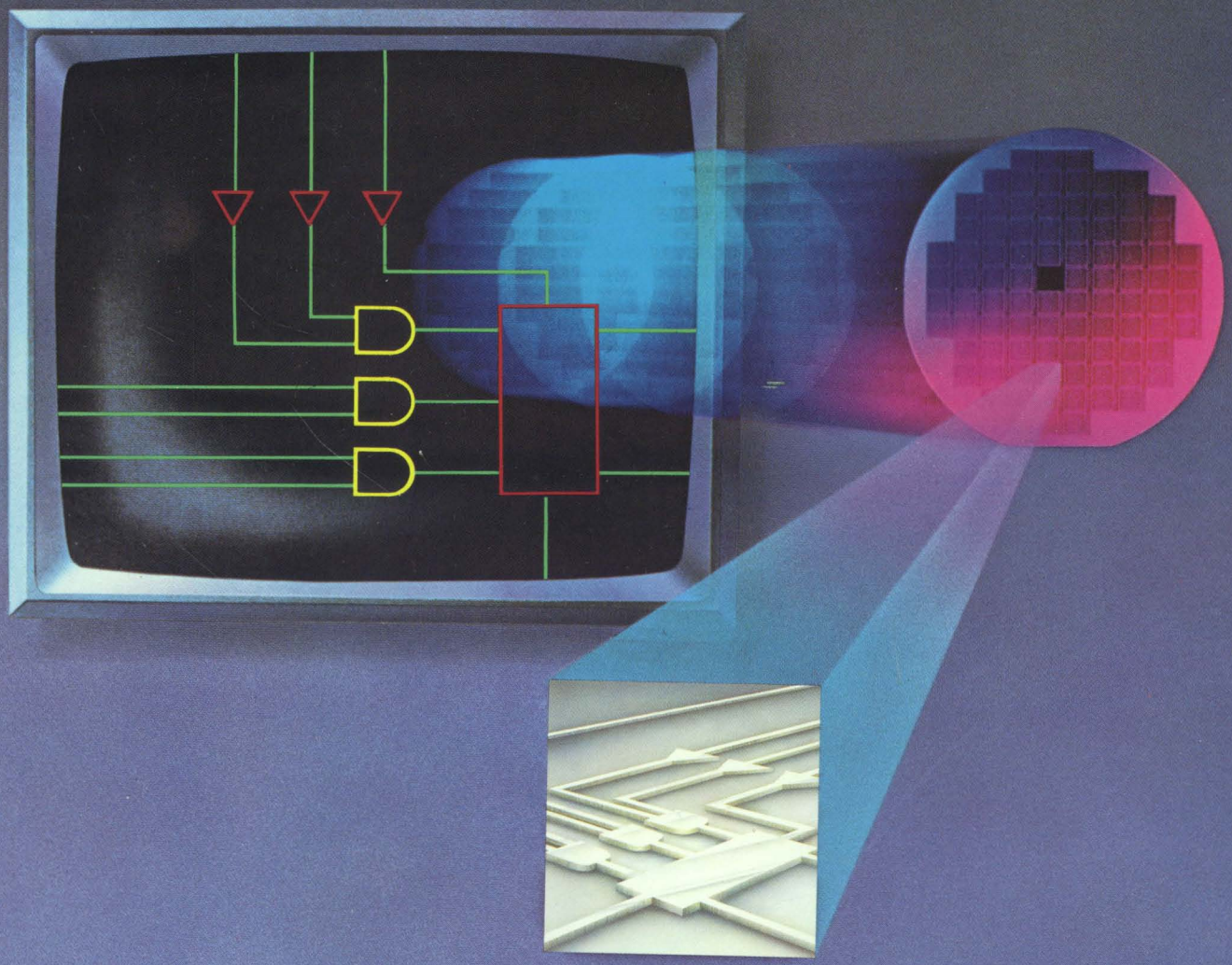
HCA6000DM/AD

HCA6000 Series Macrocell Array Design Manual



MOTOROLA

HCA6000 Series Macrocell Array Design Manual

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MACROCELL DEVICES BY FUNCTION

Macro #	Description	Cell Count
BUFFERS/INVERTERS		
C007	Triple Inverting Buffer	1
C008	Quad Inverter	1
C009	Dual 3-State Inverting Buffer	1
C010	3-State Non-Inverting Buffer	1
C085	Dual Non-Inverting 3-State Driver with 3X Outputs	3
C086	Dual Inverting 3-State Driver with 3X Outputs	3
GATES		
C001	Triple 2-Input NAND Gate	1
C002	Dual 3-Input NAND Gate	1
C003	Dual 2-Input NAND/AND Gate	1
C004	Triple 2-Input NOR Gate	1
C005	Dual 3-Input NOR Gate	1
C006	Dual 2-Input NOR/OR Gate	1
C017	Triple 4-Input NAND Gate	2
C019	Triple 3-Input NAND/AND Gate	2
C020	Triple 4-Input NOR Gate	2
C022	Triple 3-Input NOR/OR Gate	2
C053	2-Input Exclusive OR Gate	1
C054	2-Input 2-Wide OR-AND-Invert	1
C055	2-Input 2-Wide AND-OR-Invert	1
C057	5-Input NAND/AND Gate	2
C058	5-Input NOR/OR Gate	2
C088	4-3-3-3 Input 4-Wide OR-AND-Invert and 2-Input NOR Gate	4
C093	3-Input 3-Wide OR-AND-Invert	3
C094	3-Input 3-Wide AND-OR-Invert	4
C095	4-Input 2-Wide AND-OR-Invert	3
SCHMITT TRIGGER		
C025	Schmitt Trigger	1
LATCHES		
C012	NAND Latch and 2-Input NAND Gate	1
C013	NOR Latch and 2-Input NOR Gate	1
C026	D Latch with Reset (L) and Enable (L)	2
C027	Triple NAND Latch	2
C031	Triple NOR Latch	2
FLIP-FLOPS		
C034	Parallel Load D Flip-Flop with Reset	4
C035	Multiplexed D Flip-Flop with Reset (L)	4
C036	Toggle Enable Flip-Flop with Reset (L)	4
C037	J-K Flip-Flop with Reset and Set	5
C059	Buffered D Flip-Flop	2
C060	Buffered D Flip-Flop with Reset (L) and Set (L)	3
C082	Gated R-S Flip-Flop and 2 Inverters	2
C087	Toggle Enable Flip-Flop with Reset (L) and Synchronous Parallel Load (L)	4
C090	D Flip-Flop with Reset (L) and 3-State Q	4
C097	J-K Flip-Flop with 3-State Outputs and Reset	4

MACROCELL DEVICES BY FUNCTION
(Continued)

Introduction to Motorola CMOS Macrocell Arrays

1

INTRODUCTION TO MOTOROLA CMOS MACROCELL ARRAYS

The Motorola HCA6000 Series Macrocell Arrays (MCA) consists of both 2-micron and 3-micron gate length devices fabricated using a CMOS silicon-gate 2-layer metal technology. This technology provides high speed performance while maintaining the high noise immunity and low power consumption advantages of CMOS. Table 1-1 summarizes the major features of the arrays in the HCA6000 Series.

There are three basic elements that make up each array in the HCA6000 Series: the primary cell, the internal array, and the periphery (see Figure 1-1).

Table 1-1. HCA6000 Series CMOS Macrocell Array Features

Features	2-Micron HCA6200 Series					3-Micron HCA6300 Series			
	HCA6248	HCA6238	HCA6225	HCA6212	HCA6206	HCA6348	HCA6324	HCA6312	HCA6306
Primary Cells	1620	1254	810	400	216	1620	765	400	216
Equivalent Gates	4860	3762	2430	1200	648	4860	2295	1200	648
Input Only Pins	53	2	11	17	4	53	55	17	4
Bidirectional Pins	54	93	76	42	33	54	56	42	33
V_{DD} Pins	8	4	4	4	1	8	6	4	1
V_{SS} Pins	8	4	4	4	1	8	6	4	1
Test Pins	1	1	1	1	1	1	1	1	1
Typical Freq. (MHz)	85	85	85	85	85	70	70	70	70
Total Pins	124	104	96	68	40	124	124	68	40

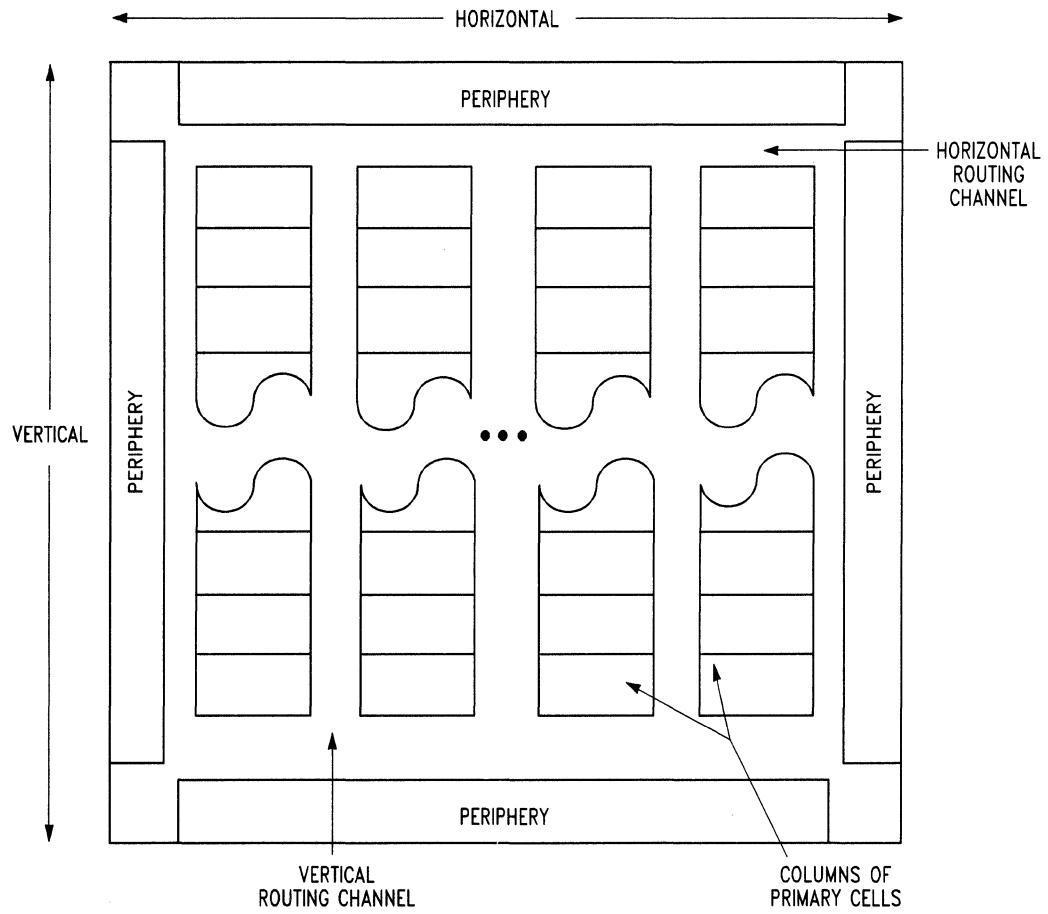

Figure 1-1. Typical Layout of HCA6000 Series Macrocell Array

The primary cell is made of eight N-channel and eight P-channel nondedicated transistors which share common sources and drains. Running through the primary cell are the appropriate V_{DD} and V_{SS} power buses. This allows for easy access to the transistors (see Figures 1-2 and 1-3). One or more primary cells are used to build logic functions referred to as macrocells or macros. These macrocells have been predefined and are stored in the computer aided design (CAD) system. A description of the macrocells is provided in Section 11. In this manual an equivalent "gate" is defined as a 2-input NAND or NOR function, and three gates can be implemented in one primary cell (macro C001).

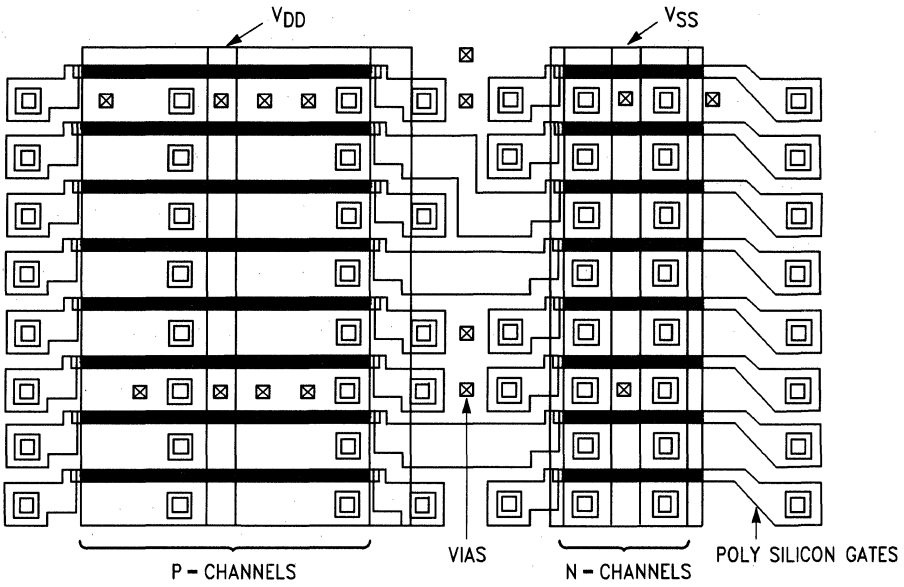

Figure 1-2. Actual Layout of Primary Cell

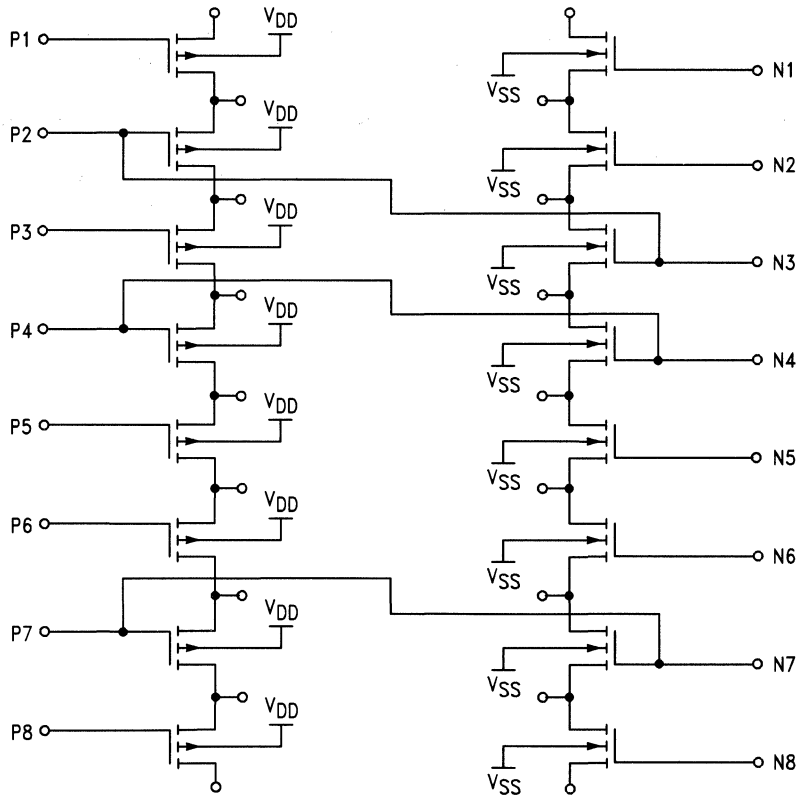

Figure 1-3. Schematic Diagram of a Primary Cell

As stated above, the macrocell functions are predefined. This allows the designer to design with basic logic functions and releases him from the burden of designing VLSI circuits at the transistor level. Another major feature of macrocells is the ability to construct softmacros. Softmacros are combinations of macrocells that perform a desired function. To illustrate, macro C038 is a 1-bit counter which can be used to build a 4-bit counter by stacking four C038's together. This helps prevent the waste that a predefined N-bit counter could create.

The second basic element of each HCA6000 Series Macrocell Array is the internal array. The internal array is an X-Y matrix of primary cells arranged in columns (see Figure 1-1). Two layers of metal are used for implementing and interconnecting macros. The first or bottom layer of metal is used to construct the macrocell functions (these metal patterns are stored in the CAD system and are requested by the designer) and for vertical routing. The second or top layer of metal runs horizontally and interconnects each of the macrocells. The two layers of metal are connected through the dielectric at predefined locations called vias. The placement and routing of the two layers of metal and the via layer is accomplished by the CAD autoplace and autoroute routines.

To optimize a macrocell array design, the CAD system allows the user to predefine macrocell placements as well as prioritize placement and routing for defined critical paths. Changes may also be made after place and route by using interactive graphics on a graphics terminal.

Due to the array structure, it is extremely difficult to utilize 100% of the gates on an array and it is recommended that functions be designed to utilize 90–95% of the gates. At this utilization rate, the CAD should be able to achieve 100% automatic routing.

The third basic element of the HCA6000 Series is the periphery which provides the interface between the internal array and the outside environment. The periphery is made up of V_{DD} pads, V_{SS} pads, input buffer locations, and uncommitted buffer locations. Input buffers (I01X–I10X) may only be used as inputs to the internal array and may be placed at either input buffer or uncommitted buffer locations on the periphery. Output buffers (Y01N, Y02N) may only be used as outputs from the internal array and must be placed at uncommitted buffer locations on the periphery. Bidirectional buffers (B02X–B05X) can be configured as input, output or input/output buffers. Bidirectional buffers must be placed at uncommitted buffer locations on the periphery regardless of the configuration used. The periphery was designed to give maximum flexibility to the user by providing both CMOS and LSTTL compatible input, output and bidirectional options.

All Motorola CMOS macrocell arrays require that one pin be dedicated as a Test-mode pin. The Test-mode pin greatly simplifies the task of checking parametric data on all of the output and bidirectional buffers and enhances the overall testability of the array. For more information on the Test-mode pin see Section 3.

On some HCA6000 Series package sizes, two different options are available. Option 1 type devices always contain fewer V_{DD} and V_{SS} pins than Option 0 type devices. This allows more input or bidirectional buffer locations on Option 1 type devices. If a design has a large number of outputs switching simultaneously the extra power and ground pins available on the Option 0 type devices may reduce the possibility of switching noise interfering with circuit operation.

Not all input, output, and bidirectional options are available for each HCA6000 Series device. Motorola is at present working to add many of these missing options so that each array will have a complete set. The electrical characteristics for the buffer options are provided in Section 8.

Option Flow 2

OPTION FLOW

The first step a customer needs to take in order to place a design on a Motorola HCA6000 Series Macrocell Array is to contact the local Motorola sales office (see the listing in the back of this manual). The sales office can describe the basic macrocell array pricing structure and place the customer in contact with one of Motorola's nationwide network of Field Application Engineers (FAE). Then the customer, the FAE, or both can decide on how to best partition the design to fit into the most economical HCA6000 Series array and package size.

Once the array and package size have been determined, the sales office can write up an option development contract between the customer and Motorola. This contract specifies the cost to the customer for ten prototype devices along with the current rates for computer time on the Motorola CAD system. The completion of this contract is normally accomplished when the customer receives ten prototype devices.

After an option development contract has been signed, work may begin on the Motorola CAD system to translate the design into working silicon (see Figure 2-1). To aid in this process, each customer is assigned a Motorola Option Development Engineer to provide assistance throughout the option development cycle. Complete documentation is also provided in the form of a design manual and a CAD manual. The design manual contains individual data sheets for each macrocell along with rules and guidelines for successfully changing the design into a netlist. The CAD manual explains the Motorola CAD system in detail. Each step of the CAD process is described using examples and sample computer outputs. In addition to the CAD manual, Motorola offers a hands-on training course covering the Motorola CAD system and design methodology.

Designing an HCA6000 Series array using the Motorola CAD system requires very little hardware. For a minimum system all that is needed is an ASCII terminal and a modem. With this setup, all necessary work can be completed at the customers location via direct phone link to the Western Area Computer Center (WACC) in Phoenix, Arizona. Optional hardware might include a graphics terminal (for physical layout editing) and a printer.

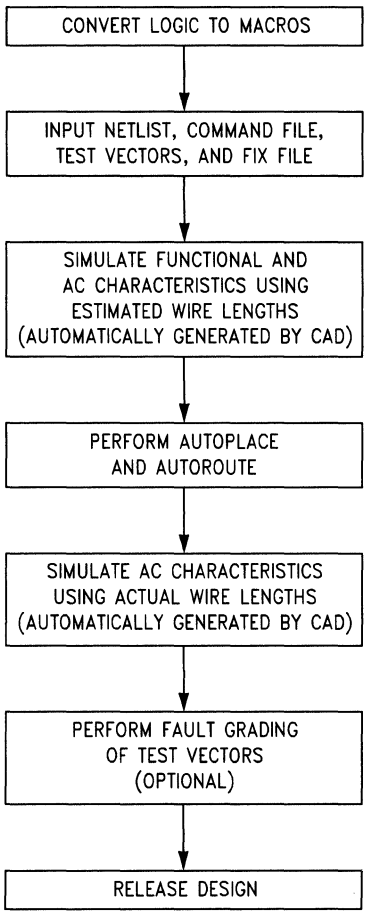

Figure 2-1. Design Flow Using Motorola CAD System Exclusively

As an alternative to using the Motorola CAD system, a customer may choose to use an engineering workstation (EWS) to perform many of the same functions (see Figure 2-2). Motorola supports selected engineering workstation vendors by supplying both electrical and physical design kits which contain the following:

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Electrical Design Kit

1) Component symbols for schematic capture
2) Netlisting program
3) Functional simulation models
4) AC simulation models
5) Communications software
6) Documentation

Physical Design Kit

1) Base die floorplans
2) Physical descriptions for each macrocell
3) Automatic and interactive place-and-route
4) Back annotation of actual metal lengths
5) Documentation

Using an engineering workstation, however, does not completely free the customer from the Motorola CAD system. At several points along the EWS design flow the customer may elect to transfer his design data base to WACC and finish any remaining work. In any case, as the last step before design release, the customer must upload his design data base to WACC and run through a verification process. This is a very important step because results from the Motorola CAD system are the ones which Motorola guarantees.

Still, using an EWS to perform time intensive tasks such as generating a netlist, generating test vectors and initial simulation can dramatically reduce the charges for mainframe time, especially if a customer plans to do more than one option. Also, a design completed on an EWS with the use of Motorola's design kit should pass through the mainframe verification process quickly and with few complications.

After a customer is satisfied that his design is working properly based on the results he has obtained on WACC, he must notify Motorola in writing of the design release. Motorola then takes the appropriate files from the customers WACC account and produces ten prototype devices. These prototype devices are packaged, tested using the customer test vectors, and then shipped to the customer for evaluation. After an evaluation period of four weeks the customer can decide whether or not he wishes to place a production order through his local Motorola sales office.

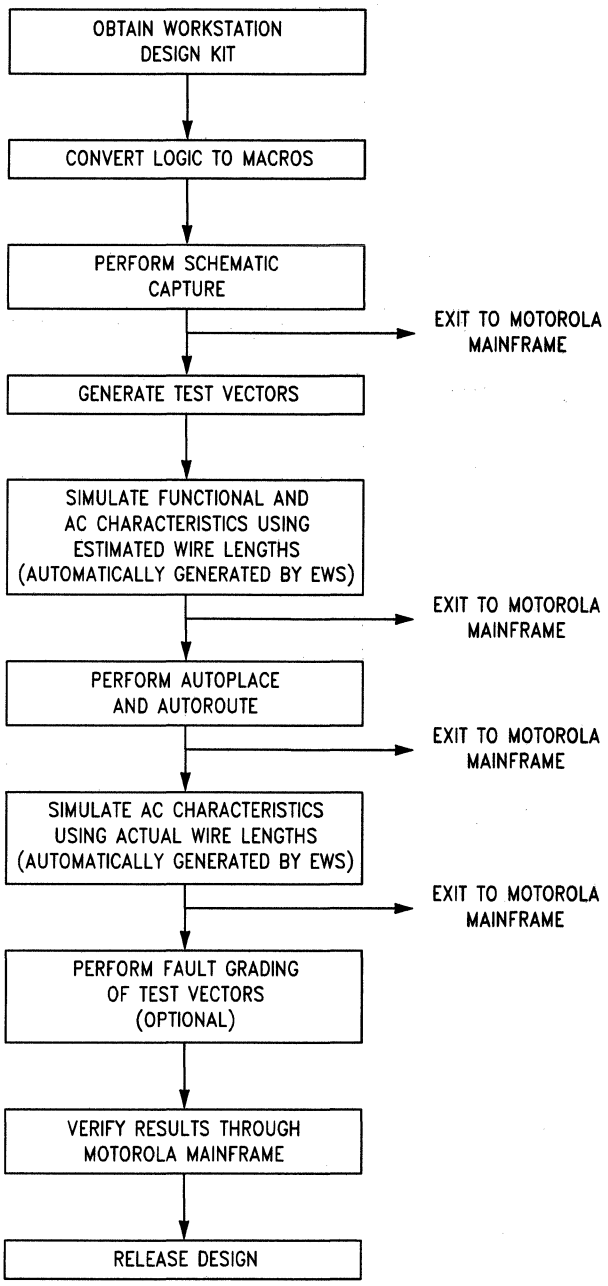


Figure 2-2. Design Flow Using Engineering Workstation and Motorola CAD System

Design Considerations 3

HANDLING PRECAUTIONS

The HCA6000 Series CMOS Macrocell Array (MCA), like all MOS devices, has insulated gates that are subject to voltage breakdown. The gate oxide on MCA devices breaks down at a gate-source potential of about 100 V. To guard against such a breakdown from static discharge or other voltage transients, the protection network shown in Figure 3-1 is used on each input to the MCA. The input protection network (IP) uses a polysilicon resistor in series with the input and before the protection diodes. The purpose of the series resistor is to slow down the rise time of static discharge spikes and allow the protection diodes time to turn on. The diodes, in turn, clamp the input voltage transient to either V_{DD} or V_{SS}. The electrostatic discharge test circuit is shown in Figure 3-2.

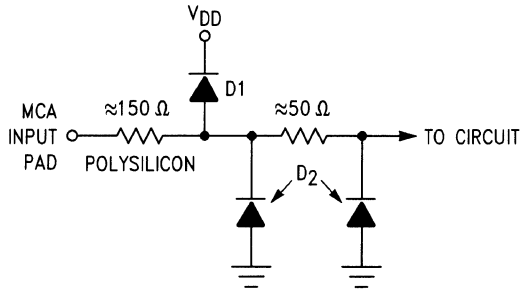


Figure 3-1. Input Protection Network

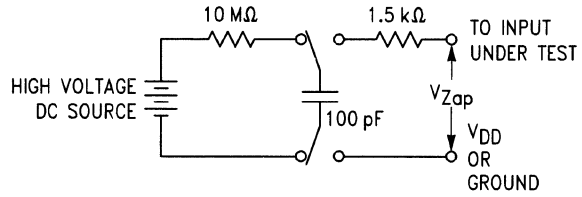


Figure 3-2. Electrostatic Discharge Test Circuit

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to V_{DD}, shorted to ground, or open-circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

Although the input protection network does provide a great deal of protection, CMOS MCA devices are not immune to large static voltage discharges that can be generated by handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–5 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the Maximum Ratings specified in the Electrical Characteristics (Section 8).
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS MCA inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS MCA devices is merely an extension of the device, and the same handling precautions apply. Contacting edge connectors wired directly to CMOS MCA device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of an CMOS MCA device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. For convenience, a graph of the typical added propagation delay is given in Figure 3-3 for a switch point of 0.5 V_{DD} and an input capacitance of 10 pF. Note that the maximum input rise and fall times should not be exceeded. For an input capacitance of 10 pF, a maximum series resistance of 30 kΩ can be used without violating the maximum input rise and fall times. In Figure 3-4, two possible networks are shown using a series resistor to help eliminate off board ESD (Electrostatic Discharge).

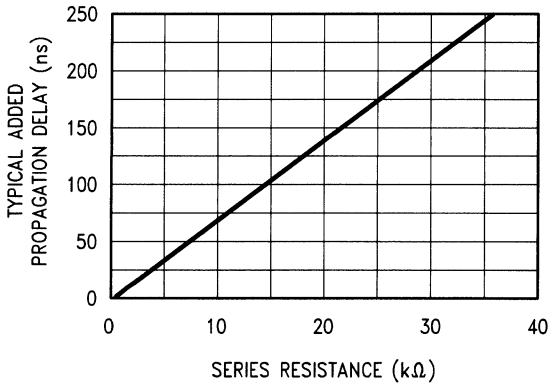
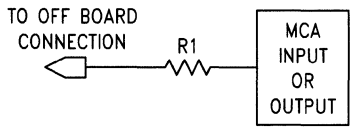
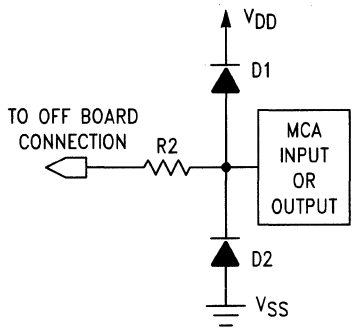


Figure 3-3. Series Resistance Effects



Advantage: Requires minimal board area
Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propogation delays, and output drivers are severely affected.



Advantage: R2 < R1 for the same level protection. Impact on ac and dc characteristics is minimized.
Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:
A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

Figure 3-4. Networks for Minimizing ESD and Reducing CMOS Latch-up Susceptibility

5. All CMOS MCA devices should be stored or transported in materials that are antistatic. CMOS MCA devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
6. All CMOS MCA devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3-5 for an example of a typical work station.

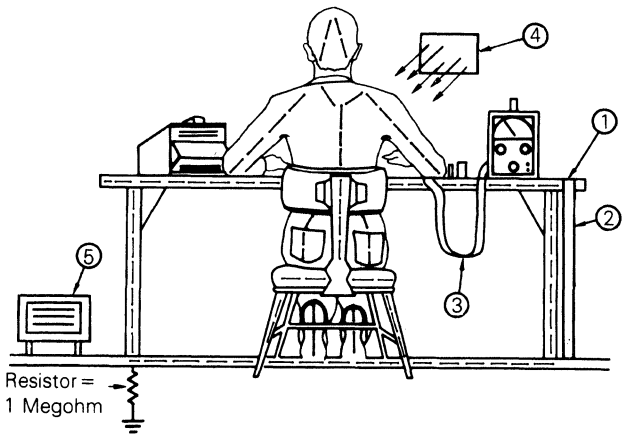


Figure 3-5. Typical Manufacturing Work Station

NOTES:
1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground Strap.
3. Wrist Strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

7. Nylon or other static generating materials should not come in contact with CMOS MCA devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of CMOS MCA packages must be grounded to metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS MCA devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the appartus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations:
    a. The solder pot and conductive conveyer system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board-cleaning operations:
    a. Vapor degreasers and baskets must be grounded to an earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.

d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards containing CMOS MCAs are grounded and a static eliminator is directed at the board.

13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS MCA devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of V_{DD} and V_{SS} before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Continuous use causes deterioration of antistatic coating.

RECOMMENDED FOR READING:

"Total Control of the Static in Your Business"
Available by writing to:
3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769-2963
Or by Calling:
1-800-328-1368

POWER SUPPLIES

HCA6000 Series CMOS Macrocell Arrays, like other CMOS devices, have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS MCA designs to be implemented using inexpensive conventional power supplies, instead of switching power supplies and power supplies with cooling fans. In addition, batteries may be used as either a primary power source or for emergency backup.

The absolute maximum recommended power supply voltage for HCA6000 Series MCAs is 7.0 V. Figure 3-6 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current of the latch-up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided. The low-current junction avalanche region is between 10 and 14 V at T_A = 25°C.

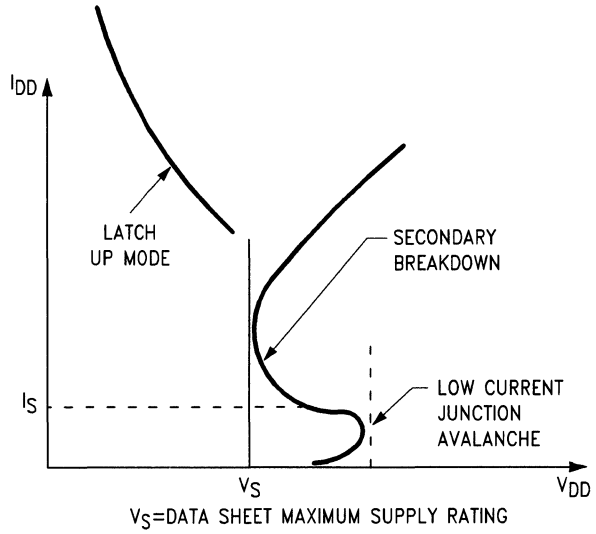


Figure 3-6. Secondary Breakdown Characteristics

In an ideal system design, a power supply should be designed to deliver only enough current to insure proper operation of all devices. The obvious benefit of this type design is cost savings; an added benefit is protection against the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

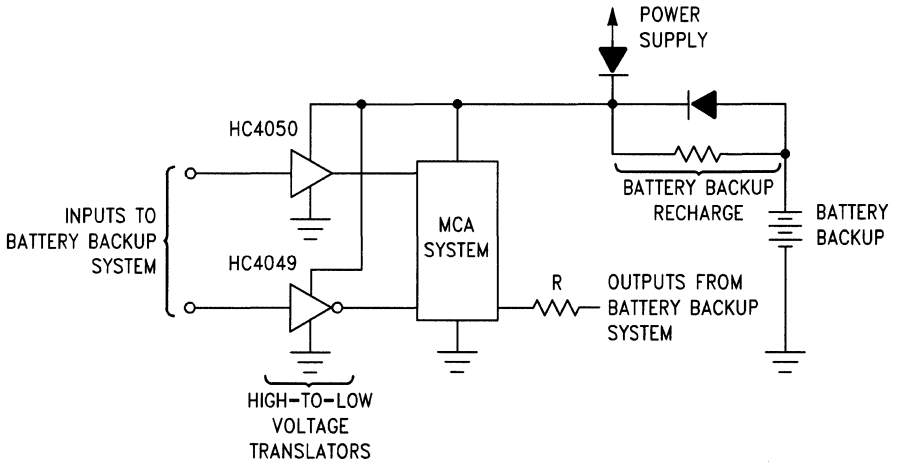


Figure 3-7. Battery Backup System

CMOS MCA devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery operated system:

1. The recommended power supply voltage should be observed. For battery backup systems such as the one in Figure 3-7, the battery voltage must be at least 3.7 V (3 V for the minimum power supply voltage and 0.7 V to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should either use a series resistor to limit the input current to less than 25 mA or use the MC54/74HC4050 or MC54/74HC4049 high-to-low voltage translators.
3. Outputs that are subject to voltage levels above V_{DD} or below V_{SS} should be protected with a series resistor to limit the current to less than 25 mA or with clamping diodes.

INPUTS

Inputs to the internal array can be made by using either input buffers or bidirectional buffers. Input buffers can only be used as inputs while bidirectional buffers can be used as an input, output, or I/O buffer. All input buffers have input protection circuitry (Figure 3-1) and can be configured for either TTL or CMOS switching levels with or without pull-up or pull-down resistors. The following design information pertains to all CMOS MCA inputs regardless of whether an input buffer or bidirectional buffer is used.

All inputs, while in the recommended operating range ($V_{SS} \leq V_{in} \leq V_{DD}$) can be modeled as shown in Figure 3-8. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case, 1 μA, when the inputs are at V_{DD} or V_{SS}, and $V_{DD}=6$ V. This model does not apply to inputs with pull-up or pull-down resistors.

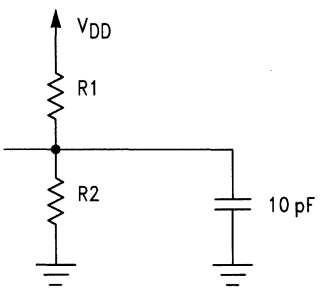


Figure 3-8. Input Model For $V_{SS} \leq V_{in} \leq V_{DD}$

It is possible, when inputs are left open-circuited, for the inputs to be biased at or near the typical switchpoint, where both the P-channel and N-channel transistors are conducting, causing excess current drain. Due to the high gain of the input buffers (see Figure 3-9), the device may also go into oscillation

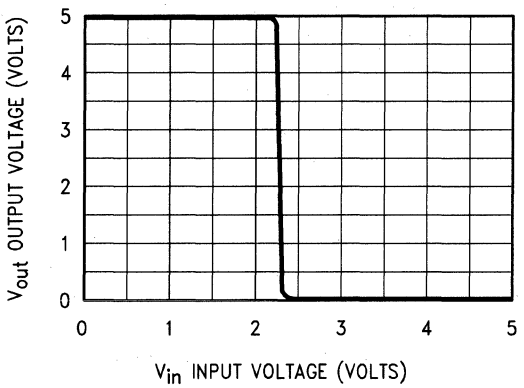


Figure 3-9. Typical Transfer Characteristics For Input Buffers

from any noise in the system. Since CMOS devices disipate the most power during switching, this oscillation can cause very large current drain and undesired switching.

For these reasons, all unused input buffers should be connected either to V_{DD} or V_{SS}. For applications with inputs going to edge connectors, a 100 kΩ resistor to V_{SS} should be used, as well as a series resistor for static protection and current limiting (Figure 3-10). The 100 kΩ resistor will help eliminate any static charges that might develop on the printed circuit board. See Figure 3-4 for other possible protection arrangements and Figure 3-3 for a plot of series resistance versus added propagation delay.

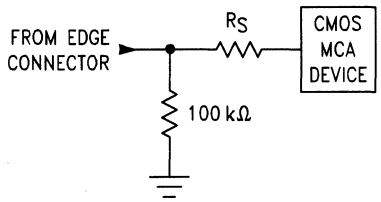


Figure 3-10. External Protection

For input voltages outside of the recommended operating range, the CMOS MCA input is modeled as in Figure 3-11. The resistor-diode protection network allows the user greater freedom when designing a

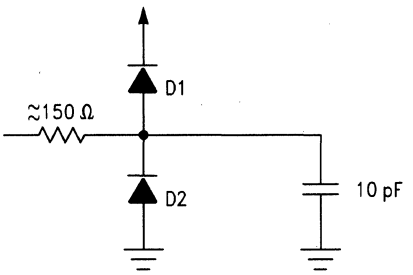


Figure 3-11. Input Model For $V_{in} > V_{DD}$ Or $V_{in} < V_{SS}$

worst case system. The device inputs are guaranteed to withstand voltages from V_{SS} − 0.5 V to V_{DD} + 0.5 V and a maximum current of 25 mA. At low capacitive loads, the output rise and fall times of output buffers can be as low as 3 ns, producing some amount of overshoot and undershoot. With the above input ratings, however, most designs will require no special terminations or design considerations.

Other specifications that should be noted are the maximum input rise and fall times. Figure 3-12 shows the oscillations that may result from exceeding the 500 ns maximum rise and fall times. The output may oscillate because as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input is amplified, and passed through the output. The oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed 500 ns, Schmitt-trigger devices such as the IO5X, IO6X, BO5N, or CO25 are recommended.

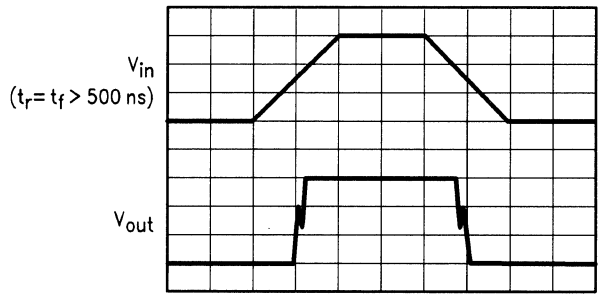


Figure 3-12. Maximum Rise Time Violations

OUTPUTS

Outputs from the internal array can be made through either output buffers or bidirectional buffers. Output buffers can only be used as outputs while bidirectional buffers can be used as an input, output or I/O buffer. All CMOS MCA outputs are buffered to insure consistent output voltage and current performance. All outputs have guaranteed output voltages of V_{OL} = 0.1 V and $V_{OH} = V_{DD} - 0.1$ V for I_{out} = 20 μA (20 CMOS loads). The output drives for all CMOS MCA output and bidirectional options are such that 10 LSTTL loads can be driven with $V_{OL} \leq 0.4$ V across the full temperature range.

CMOS MCA outputs are limited to externally forced output voltages of $V_{SS} - 0.5\ V \leq V_{out} \leq V_{DD} + 0.5$ V. When voltages are forced outside of this range, a Silicon Controlled Rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch-up. For more information on this, see the explanation of CMOS Latch-up in this section.

The maximum rated output current for any output buffer is 25 mA. The output short-circuit currents of these devices will typically exceed these limits. The outputs can, however, be shorted for brief periods of time for logic testing, if the maximum package power dissipation is not violated.

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), two or more outputs may be externally paralleled. Paralleled outputs must be of the same output buffer type and their inputs must originate at the same location.

TEST PIN

All Motorola CMOS Macrocell Arrays come with a dedicated Test-mode pin. This pin cannot be used as an input, output, or power supply connection. The Test-mode pin (TST) is used in conjunction with the Test Data (TD) and Test 3-state (T3) pins to test the output buffers. When the Test-mode pin is activated, all output and bidirectional buffers go into the test mode and accept signals from TD and T3. By varying the data on TD and T3, each possible state of the output buffers can be checked according to the function table for the array size (see individual Base-Array data sheets). The pin numbers for TD and T3 when the Test-mode pin is activated are shown in the pad to pin cross reference guides in the data sheets for each array (Section 10).

Unlike the Test-pin, TD and T3 can be used as regular inputs when the device is not in the test mode. There are certain restrictions, however, as to which input buffer options can be placed at TD and T3 locations. These restrictions, along with a function table for the test mode, are listed in the Base-Array data sheets for each individual array size (Section 10).

The purpose of the test pin is to allow parametric data to be checked without requiring a set of test vectors. There are many advantages to having the test pin built into each array including:

1. Reducing the number of required test vectors.
2. Reducing test-vector development and test time.
3. Allowing board continuity tests to be done on finished boards.
4. Increasing reliability and reducing cost.
5. Providing a de-bug tool.

These advantages more than offset the disadvantage of having one less input or output on each array.

CMOS LATCH-UP

Latch-up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3-13 shows the cross-section of a typical CMOS Inverter and Figure 3-14 shows the parasitic bipolar devices that are activated during latch-up. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned ON, each providing the base current necessary for the other to remain in satura-

tion, thereby latching the devices in the ON state. Unlike a conventional SCR, where the device is turned ON by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned ON by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch-up the CMOS device, the output voltage must be greater than $V_{DD}+0.5$ V or less than $V_{SS}-0.5$ V and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched-up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below:

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:

   $-0.5 \leq V_{in} \leq V_{DD}+0.5$ V (referenced to V_{SS})
   $-0.5 \leq V_{out} \leq V_{DD}+0.5$ V (referenced to V_{SS})
   $|I_{in}| \leq 25$ mA
   $|I_{out}| \leq 25$ mA

2. If voltage transients of sufficient energy to latch-up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum rating of 25 mA. (See Figure 3-4.)
3. Sequence power supplies so that the inputs or outputs of MCA devices are not activated before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
4. Voltage regulating or filtering should be used in board design and layout to insure that power-supply lines are free of excessive noise.
5. Limit the available power supply current to the devices tha are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

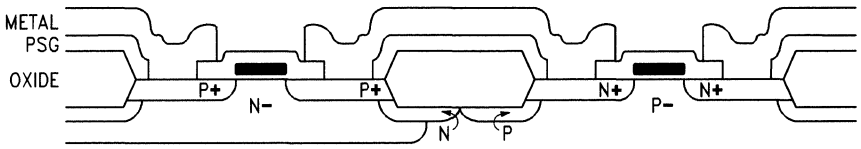


Figure 3-13. CMOS Inverter Cross Section

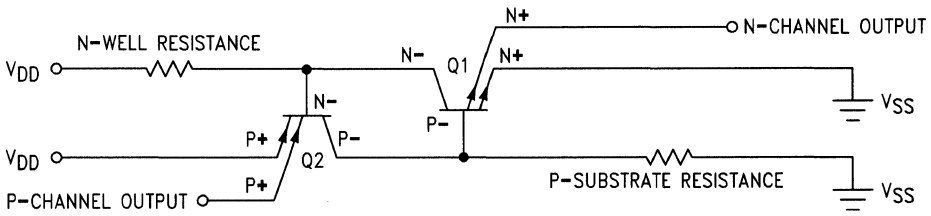


Figure 3-14. Latch-up Circuit Schematic

Timing Considerations

4

GENERAL CMOS CHARACTERISTICS

The basic building clock for CMOS circuits is the complementary-pair MOS inverter shown in Figure 4-1. When the input voltage is high the N-channel transistor (Q2) is ON and the P-channel transistor (Q1) is OFF. The output is thus connected to V_{SS} through the ON resistance of the N-channel transistor. When the input is low, the opposite is true. The P-channel transistor (Q1) is ON and the N-channel transistor (Q2) is OFF. This connects the output to V_{DD} through the ON resistance of the P-channel transistor.

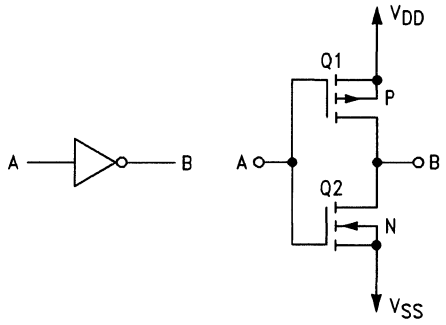


Figure 4-1. Basic CMOS Inverter

Figure 4-2 shows how the inverter is connected to form the NAND and NOR logic functions. Considering the NOR function, the gates of Q1 and Q3 are tied together to form input A of the basic inverter. The gates of Q2 and Q4 form input B. Transistor Q2 acts as a series resistance which is either extremely high or low, depending upon the gate voltage on the inverter formed by Q1 and Q3. Likewise Q1 acts as a series resistance in the second inverter. The output of the circuit is at V_{DD} only when both Q1 and Q2 are ON. This occurs only if both inputs A and B are at V_{SS}. Thus, the output is a logic "1" only when both inputs are logic "0", and a logic "0" otherwise, which is the NOR function.

The CMOS NOR gate can be converted to a NAND gate by interchanging the P- and N-channel devices, and turning the circuit upside down (Figure 4-2). Transistors Q3 and Q4 must be ON for the output to be in the logic "0" condition. More inputs can be added to make 3- and 4-input gates by adding complementary pairs (Figure 4-3).

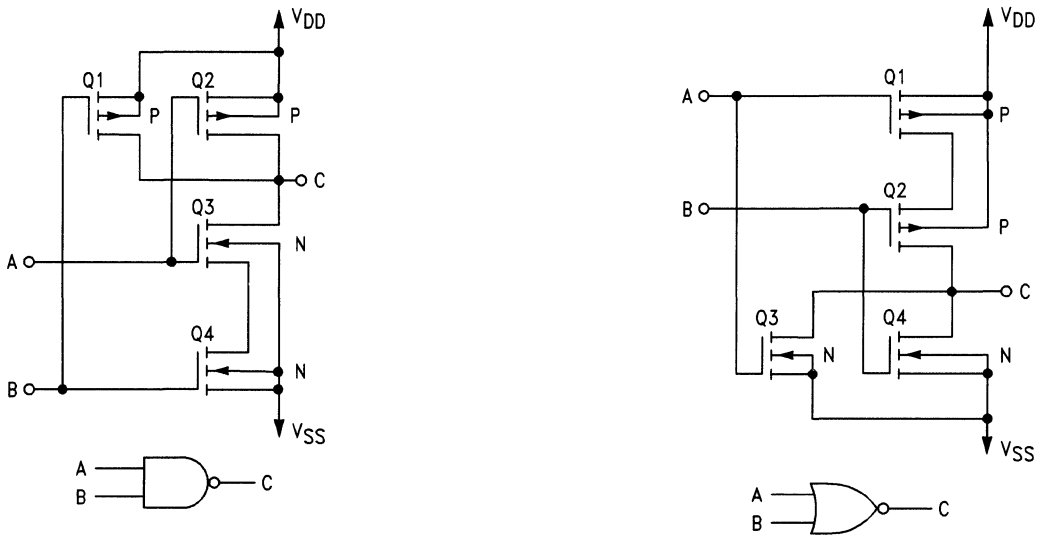


Figure 4-2. Implementation of 2-input NAND and 2-input NOR Gates using CMOS Technology.

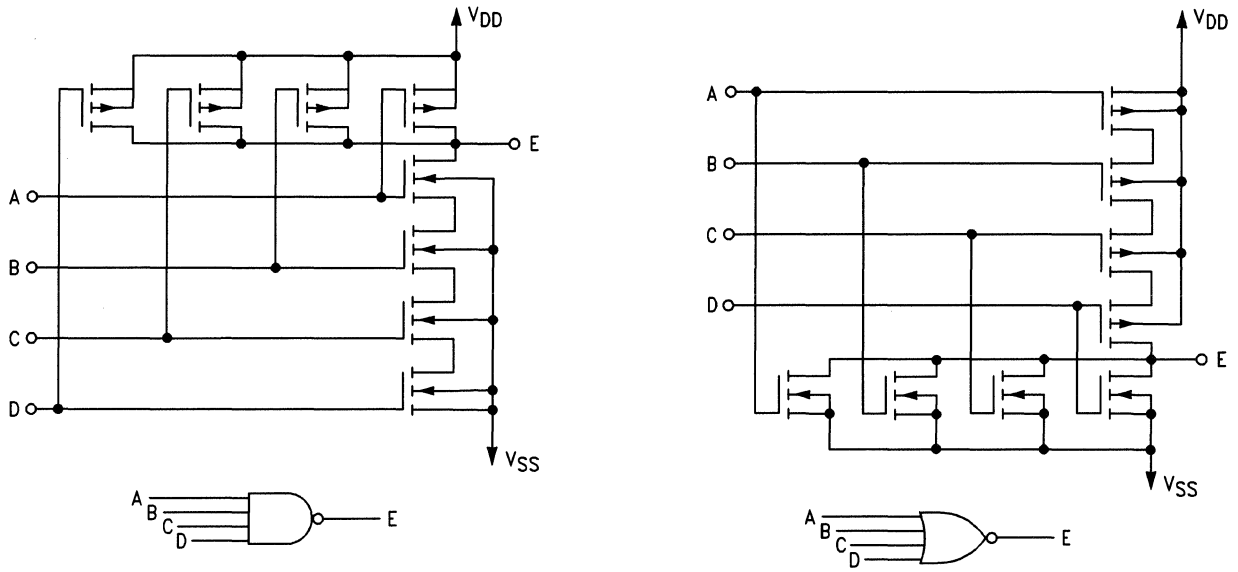


Figure 4-3. Implementation of 4-input NAND and 4-input NOR Gates using CMOS Technology.

PROPAGATION DELAY

The switching speed of a CMOS gate is determined by the time required for the load capacitance to be charged or discharged through the resistance of the ON transistor(s). Each input buffer, macrocell, and output buffer has a data sheet which contains the propagation delay for a specified reference load. This reference load (C_{ref}) is equal to 1 pF for input buffers and macros and 50 pF for output buffers. The propagation delay at the specified reference load is stated for both maximum and minimum conditions as defined in Table 4-1.

Table 4-1. Definition of Minimum and Maximum Simulation Conditions

Factor	Minimum Specification Conditions			Maximum Specifications Conditions		
	Input Buffers	Macrocells	Output Buffers	Input Buffers	Macrocells	Output Buffers
HCA6200 Series 2-Micron HCMOS						
C_L	1 pF	1 pF	50 pF	1 pF	1 pF	50 pF
Input Rise Time	CMOS = 1 ns TTL = 5 ns	0.6 ns	0.6 ns	CMOS = 6 ns TTL = 15 ns	3 ns	3 ns
Input Fall Time	CMOS = 1 ns TTL = 1 ns	0.6 ns	0.6 ns	CMOS = 6 ns TTL = 6 ns	3 ns	3 ns
V_{DD}	5.5 V			4.5 V		
T_A	−40°C			+85°C		
Processing	BEST			WORST		
HCA6300 Series 3-Micron HCMOS						
C_L	1 pF	1 pF	50 pF	1 pF	1 pF	50 pF
Input Rise Time	CMOS = 5 ns TTL = 5 ns	1 ns	1 ns	CMOS = 5 ns TTL = 15 ns	5 ns	5 ns
Input Fall Time	CMOS = 5 ns TTL = 1 ns	1 ns	1 ns	CMOS = 5 ns TTL = 6 ns	5 ns	5 ns
V_{DD}	5.5 V			4.5 V		
T_A	−40°C			+85°C		
Processing	BEST			WORST		

DRIVE COEFFICIENTS (K Values)

Each propagation delay listed on every macrocell data sheet has an associated K value. The K value is calculated as shown below:

$$K = \frac{\Delta \text{ Delay}}{\Delta C_L} = \frac{t_P (C_L = A) - t_P (C_L = B)}{A - B} \quad \text{(Eq. 4-1)}$$

where:

C_L = Load capacitance (pF)

$t_{P(C_L=A)}$ = Propagation delay with capacitive load A (ns)

$t_{P(C_L=B)}$ = Propagation delay with capacitive load B (ns)

A = Capacitance (pF)

B = Capacitance (pF)

K, therefore, is simply the change in propagation delay that occurs due to a change in the load capacitance. The K values listed on each individual data sheet have been calculated with A = 2 pF, B = 1 pF for input buffers and macrocells, A = 100 pF, B = 50 pF for output buffers, and A = 50 pF, B = 15 pF for input clock buffers. These K values are specified at V_{DD} = 5.5 V (minimum conditions) and V_{DD} = 4.5 V (maximum conditions).

When macrocells are paralleled, the output drive is increased and the load capacitance charge/discharge time is reduced. This occurs because the ON resistance of the transistors in each of the macrocells (see CMOS characteristics section) is also paralleled. To account for the resulting reduction in propagation delay, the K value for paralleled macrocells is calculated as shown below:

$$K_P = \left(\frac{1}{n}\right) K \quad \text{(Eq. 4-2)}$$

where:

K_P = New K value for paralleled macrocells (ns/pF)

n = Number of macrocells in parallel

K = K value of a single macrocell (ns/pF)

CAPACITIVE LOAD (C_L)

The propagation delay for any input buffer, macrocell, or output buffer is dependent upon the load capacitance (C_L) that the buffer or macrocell must drive. Load capacitance can come from the capacitance of the inputs that the output is driving, the metal that connects the output to the input(s) being driven, and, in some cases, output capacitance of other macrocells. Load capacitance is calculated from the formula shown below:

$$C_L = C_I + C_{INT} + C_Z \quad \text{(Eq. 4-3)}$$

where:

C_L = Total load capacitance (pF)

C_I = Input capacitance (pF)

C_{INT} = Metal interconnect capacitance (pF)

C_Z = 3-State output capacitance (pF)

Input capacitance (C_I) for HCA6000 Series MCAs is measured with the Input Unit Load (IUL) factor. An IUL of 1.0 is equal to 0.21 pF for 3-micron devices and 0.17 pF for 2-micron devices and represents the capacitance associated with one P-channel and N-channel transistor pair such as is found in a basic CMOS inverter (C008). The input capacitance of inputs with higher IUL factors can be found by multiplying the IUL factor by 0.21 pF for 3-micron devices or 0.17 pF for 2-micron devices (e.g. an IUL of 8 on a 3-micron device is equal to 1.68 pF). To illustrate, suppose that the circuit shown in Figure 4-4 were to be placed on an HCA6300 macrocell array. The input capacitance that output A must drive would be calculated as follows:

IUL of C004 = 1 (Eq. 4-4)
IUL of C007 = 2
IUL of C059 = 1
Total IUL = 4

C_I = (4) (0.21 pF) = 0.84 pF

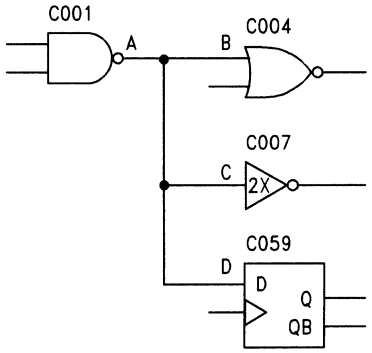


Figure 4-4. Schematic Diagram Showing Several Macrocells and Associated Interconnect Metal

The amount of capacitance per mil of interconnect metal is shown below:

	HCA6200	HCA6300
C_{M1} =	0.00442 pF/mil	0.00675 pF/mil
C_{M2} =	0.00445 pF/mil	0.00450 pF/mil
C_{AVG} =	0.00443 pF/mil	0.00580 pF/mil

where:

C_{M1} = Capacitance of layer one metal.

C_{M2} = Capacitance of layer two metal.

C_{AVG} = Average capacitance of both layers of metal.

Actual metal interconnect lengths on an MCA are not known until after place and route has been completed. For design purposes, the length of interconnect metal can be estimated before place and route by counting the number of inputs and outputs that are to be connected together and multiplying this number by the typical metal length for the array be-

ing used. Each input and output is referred to as a connection (conn) and the interconnect metal is referred to as a net. Typical metal lengths per connection (L_T) for each array are shown below:

HCA6348	40 mils/conn	HCA6248	30 mils/conn
HCA6324	27 mils/conn	HCA6225	18 mils/conn
HCA6312	22 mils/conn	HCA6212	16.5 mils/conn
HCA6306	16 mils/conn	HCA6206	12 mils/conn

The capacitance of the metal interconnect (C_{INT}) can be calculated by multiplying C_{AVG} by the estimated metal interconnect length. For example, if the circuit shown in Figure 4-4 were to be placed on an HCA6348 array, the capacitance due to the metal connecting output A to inputs B, C, and D would be estimated as follows:

$$C_{INT} = (C_{AVG})(L_T)(N) \qquad \text{(Eq. 4-5)}$$

where:

N = Number of inputs and outputs (conn) connected by net.

L_T = Typical metal length (mils) per connection for the array being used.

C_{INT} = (0.00580 pF/mil) (40 mils/conn) (4 conn)
= 0.928 (pF)

The output capacitance of other macrocells needs to be taken into consideration only when 3-state bus structures are being used. An example of a 3-state bus is shown in Figure 4-5. In a 3-state bus, only one macrocell is active at any given time and all others are in the high-impedance state. The outputs of the macrocells in the high-impedance state have an output capacitance (0.26 pF for 3-micron devices and 0.166 pF for 2-micron devices) which the active macrocell must drive in addition to C_I and C_{INT}. The formula for calculating the output capacitance (C_Z) of a 3-state bus configuration is shown below:

$$C_Z = (n-1)(x) \qquad \text{(Eq. 4-6)}$$

where:

C_Z = Total capacitance of 3-state outputs (pF)

n = Number of 3-state outputs connected together

x = Output capacitance of single 3-state output (pF)

If the 3-state bus structure shown in Figure 4-5 were to be placed on an HCA6300 macrocell array, C_Z would be calculated as follows:

$C_Z = (n - 1)(x)$
$= (4 - 1)(0.26\ pF)$
$= 0.78\ pF$

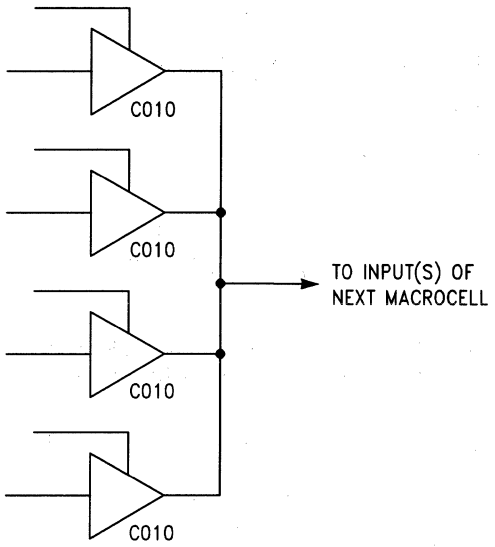


Figure 4-5. Example of 3-state Bus Configuration

PROPAGATION DELAY CALCULATIONS

As previously stated, the propagation delays for input buffers, macrocells, and output buffers are given for a specified reference load on each data sheet. To calculate the propagation delay for other loads, the following formula is used:

$$t_p\ (X\ to\ Y) = t_{p(C_L = C_{ref})} + K\ (C_L - C_{ref}) \qquad \text{(Eq. 4-7)}$$

where:

$t_{p(X\ to\ Y)}$ = Total propagation delay from input X to output Y (ns)

$t_{p(C = C_{ref})}$ = Propagation delay with C_{ref} as load (given on individual data sheets) (ns)

K = K value for propagation delay in question (given on individual data sheets) (ns/pF)

C_L = Load capacitance (pF)
$= C_I + C_{INT} + C_Z$

C_{ref} = Reference load (pF)
= 50 pF for output buffers
= 15 pF for input clock buffers
= 1 pF for input buffers and macrocells

Simple Macrocell Output

Find the total worst case t_{PHL} from A to Y for the C030 connected as shown in Figure 4-6. The circuit is to be placed on an HCA6312 macrocell array.

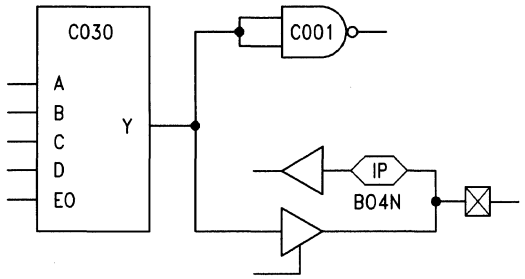


Figure 4-6. Example Circuit for Calculating the Propagation Delay of a Macrocell.

$t_{PHL(A\ to\ Y)} = t_{PHL}\ (@\ C_L = 1\ pF) + K\ (C_L - 1\ pF)$

C_I = [(2) (IUL of C001) + IUL of B04N] (0.21 pF)
= [(2) (1) + (8)] (0.21 pF)
= [10] (0.21 pF)
= 2.1 pF

$C_{INT} = C_{AVG}\ (L_T)\ (N)$
= (0.0058 pF/mil) (22 mils/conn) (4 conn)
= 0.510 pF

$C_L = C_I + C_{INT} + C_Z$
= 2.1 pF + 0.510 pF + 0 pF
= 2.61 pF

$t_{PHL\ (A\ to\ Y)}$ = 24.8 ns + 3.6 ns/pF (2.61 pF − 1 pF)
= 24.8 ns + 5.79 ns
= 30.59 ns

Paralleled Macrocells

Find the total worst case t_{PLH} for the four C008 macrocells connected as shown in Figure 4-7. This circuit is to be placed on an HCA6324 macrocell array.

Note: When calculating the propagation delays for macrocells in parallel, 0 pF must be used as C_{ref} instead of 1 pF. This is because the propagation delay through paralleled macrocells with a $C_L = 1$ pF depends on how many macrocells are paralleled. The propagation delay through paralleled macrocells with a $C_L = 0$ pF, never changes and is unaffected by the number of macrocells placed in parallel. Therefore, the formula for finding the t_{PLH} from A to B would become:

$t_{PLH\ (A\ to\ B)} = t_{PLH}\ (@\ C_L = 0\ pF) + K_P\ (C_L - 0\ pF)$

$t_{PLH}\ (@\ C_L = 0\ pF) = t_{PLH}\ (C_L = 1\ pF) + K\ (0 - 1\ pF)$
= 4 ns + 2.2 ns/pF (−1 pF)
= 1.8 ns

C_I = [(5) (IUL of C060)] (0.21 pF)
= [(5) (1)] (0.21 pF)
= 1.05 pF

$C_{INT} = (C_{AVG})\ (L_T)\ (N)$
= (0.0058 pF) (27 mils/conn) (9 conn)
= 1.41 pF

$C_L = C_I + C_{INT} + C_Z$
= 1.05 pF + 1.41 pF + 0 pF
= 2.46 pF

$K_P = \left(\frac{1}{X}\right) K$
$= \left(\frac{1}{4}\right)\left(2.2\ ns/pF\right)$
= 0.55 ns/pF

$t_{PLH\ (A\ to\ B)}$ = 1.8 ns + 0.55 ns/pF (2.46 pF − 0 pF)
= 3.15 ns

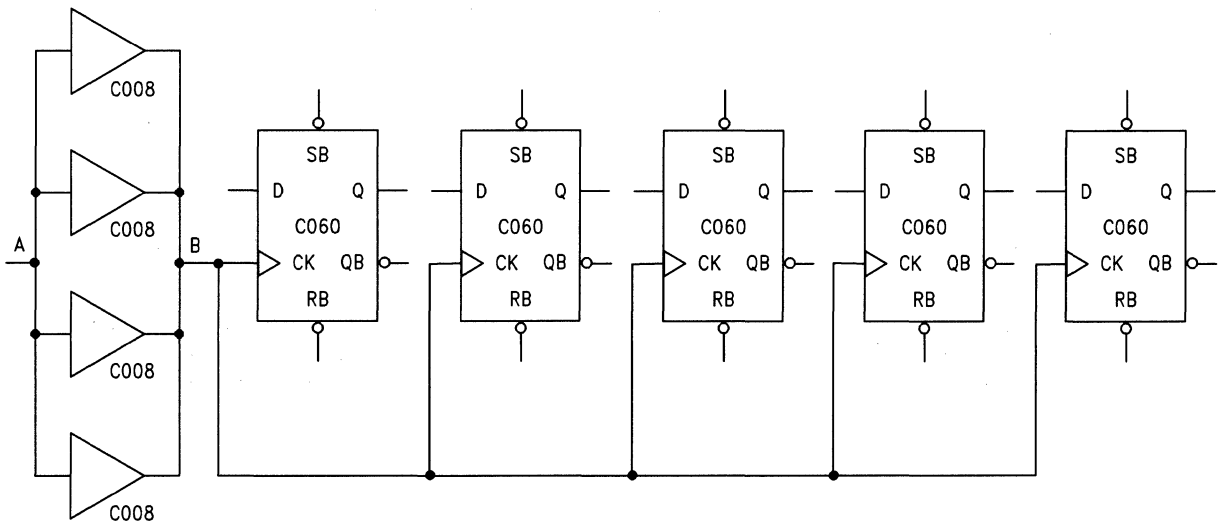


Figure 4-7. Example Circuit for Calculating Propagation Delay of Paralleled Macrocells.

A simplified formula for calculating the propagation delay of parallel macrocells is shown below:

$$t_{P\,(parallel)} = (t_{P\,(@\ C_L\ =\ 1\ pF)} - K) + K_P\,(C_L)$$

3-State Bus

Find the total worst case t_{PHL} from A to B for the 3-state bus configuration shown in Figure 4-8. Only one C009 is driving the C004 at any given time. The 3-state bus is to be placed on an HCA6306 array.

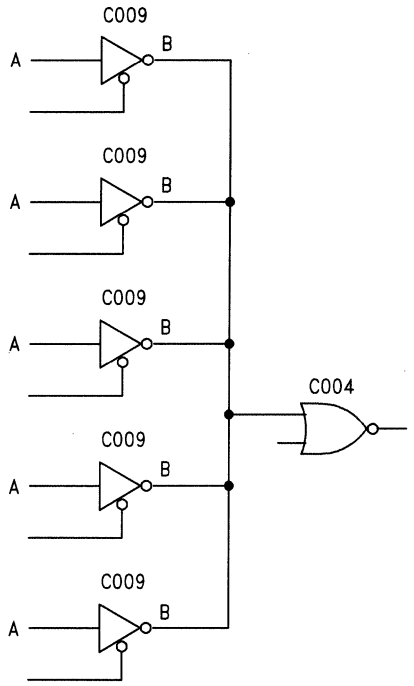


Figure 4-8. Example Circuit for Calculating the Propagation Delay of a 3-state Bus.

$$t_{PHL\,(A\ to\ B)} = t_{PHL\,(@\ C_L\ =\ 1\ pF)} + K\,(C_L - 1\ pF)$$

$$C_I = (IUL\ of\ C004)\ (0.21\ pF)$$
$$= 1\ (0.21\ pF)$$
$$= 0.21\ pF$$

$$C_{INT} = (C_{AVG})\ (L_T)\ (N)$$
$$= (0.0058\ pF/mil)\ (16\ mils/conn)\ (6\ conn)$$
$$= 0.556\ pF$$

$$C_Z = (n - 1)\ (X)$$
$$= (5 - 1)\ (0.26\ pF) = 1.04\ pF$$

$$C_L = C_I + C_{INT} + C_Z$$
$$= 0.21\ pF + 0.556\ pF + 1.04\ pF$$
$$= 1.80\ pF$$

$$t_{PHL\,(A\ to\ B)} = 7.4\ ns + 3.8\ ns/pF\ (1.80\ pF - 1\ pF)$$
$$= 7.4\ ns + 3.04\ ns$$
$$= 10.4\ ns$$

Output Buffer

Find the total worst case t_{PLH} from A to the Bonding Pad (BP) for the bidirectional buffer B02N shown in Figure 4-9. The load capacitance is 125 pF.

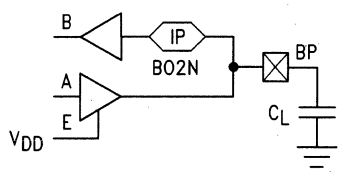


Figure 4-9. Example Circuit for Calculating Propagation Delay of an Output Buffer.

$$t_{PLH\,(A\ to\ BP)} = t_{PLH\,(@\ C_L\ =\ 50\ pF)} + K\,(C_L - 50\ pF)$$
$$= 16.4\ ns + 0.144\ ns/pF\ (125 - 50\ pF)$$
$$= 16.4\ ns + 10.8\ ns$$
$$= 27.2\ ns$$

Dependent Outputs

Calculation of propagation delay for some macrocells is complicated by the fact that one output is dependent upon another output. An example of this is the C003 macrocell shown in Figure 4-10.

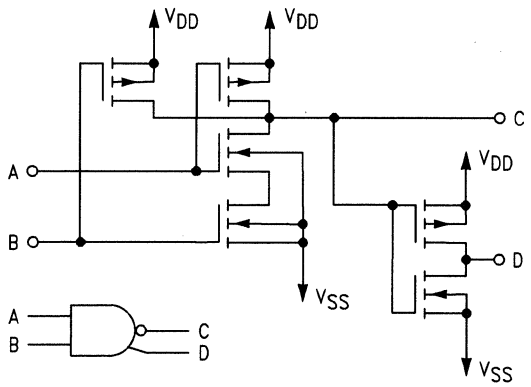


Figure 4-10. Dependent Output Macrocell

The propagation delay from either of the inputs to the D output depends on the loading that is present on the C output. This means that to find the propagation delay from A or B to D, two calculations must be made—one for A or B to C and one for C to D. To make these calculations easier, the data sheets for devices with dependent outputs have a separate specification for the dependent invertor stage (see Table 4-2).

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.4	0.8	1.8	1.8	3.4	0.2	0.6	2.4	2.4	5.2	ns
t_{PHL}		0.8	1.4	2.9	4.6	5.4	0.6	1.2	3.4	3.5	6.6	
t_{PLH}	Propagation Delay, A, B to D (Figure 1)	0.6	2.2	5.6	2.5	10.4	0.6	2.4	6.7	3.0	12.8	ns
t_{PHL}		0.4	1.8	4.0	1.8	7.4	0.4	1.8	5.2	2.2	10.2	
t_{PLH}	Propagation Delay, C to D (Figure 2)	0.6	0.6	2.0	2.5	3.7	0.6	0.8	3.3	3.0	6.2	ns
t_{PHL}		0.4	0.8	1.4	1.8	2.6	0.4	0.8	2.8	2.2	5.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

Table 4-2. Switching Characteristics for C003.

For example, if the circuit shown in Figure 4-11 were to be placed on an HCA6306, the first step in finding the worst case t_{PHL} from B to D would be to find the t_{PLH} from B to C. Output C, in this case, is not connected so it has 0 pF as a load capacitance.

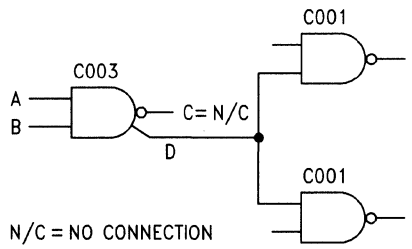


Figure 4-11. Example Circuit for Calculating the Propagation Delay of a Macrocell with a Dependent Output.

$$t_{PLH\ (B\ to\ C)} = t_{PLH\ (@\ C_L\ =\ 1\ pF)} + K\ (C_L - 1\ pF)$$
$$= 5.2\ ns + 2.4\ ns/pF(0\ pF - 1\ pF)$$
$$= 5.2\ ns - 2.4\ ns$$
$$= 2.8\ ns$$

Next, the t_{PHL} delay from C to D is calculated

$$C_I = [(2)\ (IUL\ OF\ C001)]\ (0.21\ pF)$$
$$= [(2)\ (1)]\ (0.21\ pF)$$
$$= 0.42\ pF$$

$$C_{INT} = (C_{AVG})\ (L_T)\ (N)$$
$$= (0.0058\ pF/mil)\ (16\ mils/conn)\ (3\ conn)$$
$$= 0.278\ pF$$

$$C_L = C_I + C_{INT} + C_Z$$
$$= 0.42\ pF + 0.278\ pF + 0\ pF$$
$$= 0.698\ pF$$

$$t_{PHL\ (C\ to\ D)} = t_{PHL\ (@\ C_L\ =\ 1\ pF)} + K\ (C_L - 1\ pF)$$
$$= 5\ ns + 2.2\ ns/pF\ (0.698\ pF - 1\ pF)$$
$$= 5\ ns - 0.302\ ns$$
$$= 4.69\ ns$$

The total delay is then the sum of the B to C and the C to D delays:

$$t_{PHL\ (B\ to\ D)} = 2.8\ ns + 4.69\ ns$$
$$= 7.49\ ns$$

VARIATIONS IN PROPAGATION DELAYS

Temperature

In general, a 10°C increase in junction temperature causes a 3% increase in propagation delay. Junction temperature can be calculated from:

$$T_J = T_A + (\theta_{JA})\ (P_D) \qquad \text{(Eq. 4-8)}$$

where:
T_J = Junction Temperature (°C)
T_A = Ambient Temperature (°C)
θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)
P_D = Power Dissipation of Array (W)

The data provided in Table 4-3 is given not as a guarantee, but as a design aid. The numbers supplied are typical values.

Table 4-3. θ_{JA} Values

Package	Number of Pins	θ_{JA} (°C/W)
Plastic (Alloy 42/copper lead)	16 28 40	146/95 112/74 95/42
Ceramic DIP	28 40	51 50
Side Brazed DIP	28 40	50 40
PCC(copper lead)	28	88
LCC	28 68 84	75 35 35
PGA	28 68 124	36 35 30

Voltage

Variations in propagation delay due to changes in the power supply voltage can be calculated utilizing the graph shown in Figure 4-12.

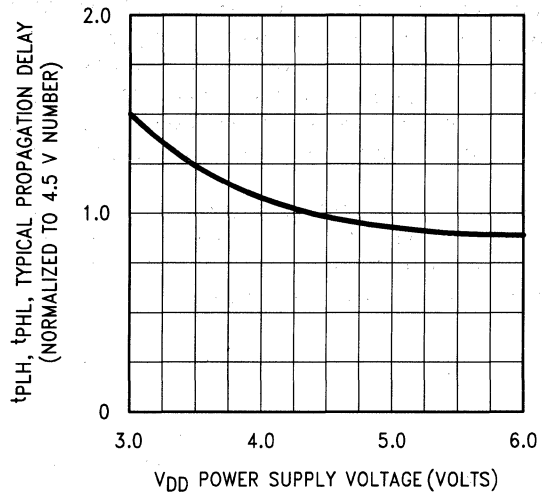


Figure 4-12. Normalized Plot of Propagation Delay Versus V_{DD}

MINIMIZING PROPAGATION DELAYS

To keep propagation delays to a minimum, several design practices should be followed:

A. Keep the fanout for each device as low as possible. As fanout increases, the load capacitance the driving device must charge or discharge increases. Table 4-4 shows how propagation delay changes as fanout increases for a 2-input NAND (C001) and a 2-input NOR (C004).

Table 4-4. Propagation Delays for C001 and C004 with Various Fanouts. Each Fanout Input has an IUL = 1.

Fanout	C001		C004	
	t_{PLH}*	t_{PHL}*	t_{PLH}*	t_{PHL}*
1	3.8 ns	4.8 ns	6.5 ns	3.7 ns
2	4.8 ns	6.4 ns	8.5 ns	4.6 ns
3	5.9 ns	8.0 ns	10.5 ns	5.5 ns
4	7.0 ns	9.6 ns	12.6 ns	6.4 ns
5	8.0 ns	11.1 ns	14.6 ns	7.2 ns
6	9.1 ns	12.7 ns	16.6 ns	8.1 ns
7	10.1 ns	14.3 ns	18.6 ns	9.0 ns
8	11.2 ns	15.9 ns	20.7 ns	9.9 ns

*Worst Case 3-micron numbers

B. Use gates with as few inputs as possible. As the number of inputs increases, the number of transistors in series also increases (see Figure 4-3). This makes the ON resistance between the output and V_{DD} (for NOR gates) or V_{SS} (for NAND gates) higher and increases the time needed to charge or discharge the load capacitance. Table 4-5 shows how the propagation delay changes as the number of inputs increases for NAND gates.

Table 4-5. Propagation Delays for NAND Gates with 2, 3, 4 and 5 Inputs.

Macrocell	t_{PHL}*	t_{PLH}*
2-Input NAND (C001)	6.0 ns	4.6 ns
3-Input NAND (C002)	10.4 ns	5.2 ns
4-Input NAND (C017)	13.2 ns	5.4 ns
5-Input NAND (C057)	16.6 ns	11.4 ns

*Worst Case 3-micron numbers

C. Duplicate logic to increase drive. Parallel macrocells to increase the drive of an output with a high load capacitance as shown in Figure 4-13. This technique can also be applied to decrease the propagation delay of a speed-critical path as shown in Figure 4-14.

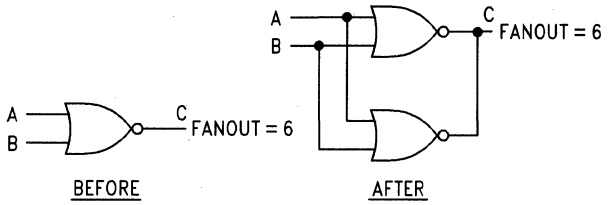


Figure 4-13. Duplicating Logic to Increase the Output Drive

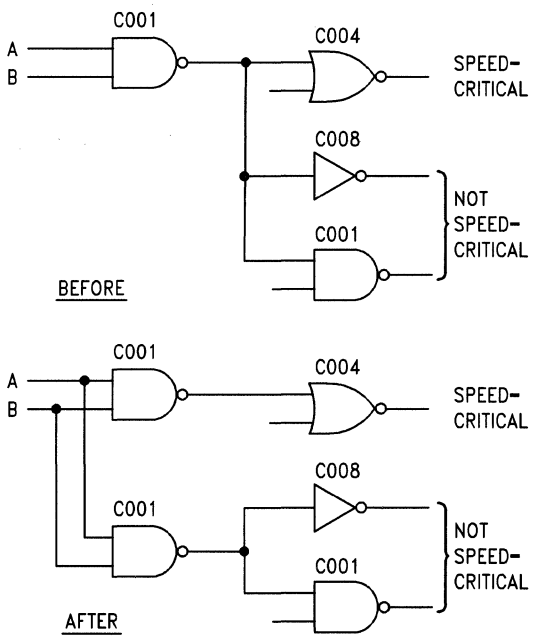


Figure 4-14. Duplicating Logic to Decrease Propagation Delay of Speed Critical Path

The macrocells which may be paralleled are listed below:

C001	C002	C003
C004	C005	C006
C007	C008	C009
C010	C017	C019
C020	C022	C025

To insure proper operation, paralleled macrocells must be of the same type and their inputs must originate at the same location. Also, the gain in speed from paralleling macrocells should more than offset the loss in speed that occurs due to the increased fanout of the macrocell that is driving the duplicate logic. Figure 4-15 shows an example of how propagation delay changes as additional macrocells are placed in parallel. In Figure 4-15, note that there is an optimum number of parallel macrocells for a minimum propagation delay.

D. Use the C007 inverting buffer instead of the C008 inverter when driving high capacitive loads. The C007 has twice the drive capability of the C008.
E. Use large, pre-defined macrocells to implement functions instead of building the functions from smaller macrocells. Large macrocells keep the amount of metal interconnect needed for a function to a minimum, and therefore reduce propagation delays.
F. Use macrocell pre-placement and critical net definition capabilities of the CAD software before automatic placement and routing of the array in areas where timing delays are critical.

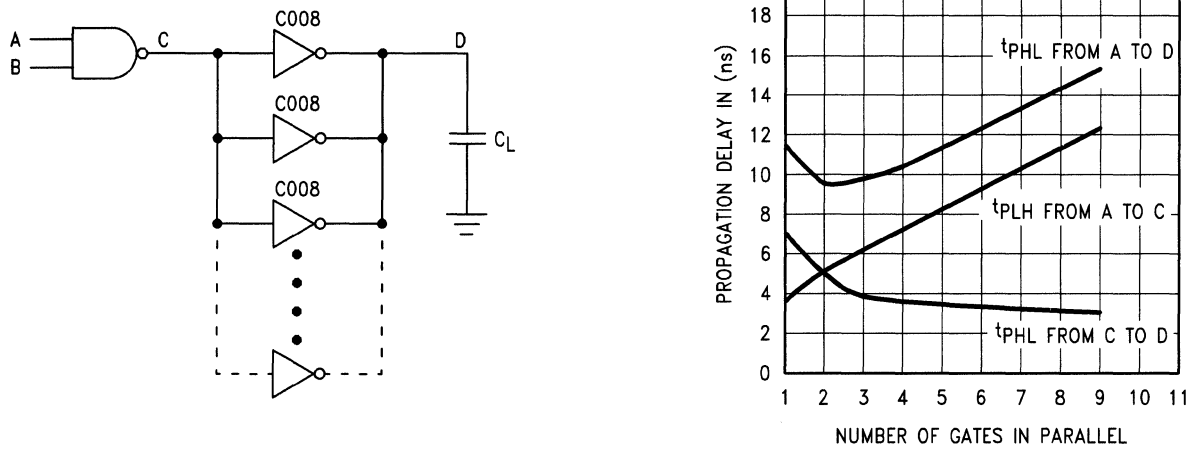


Figure 4-15. Changes in Propagation Delay Due to Paralleling Macrocells

Power Consumption 5

POWER-CONSUMPTION

The amount of power consumed by a CMOS macrocell array is dependent upon the frequencies and load capacitances of the design. Because these factors vary greatly, it is impossible to derive a simple rule of thumb for estimating power consumption in macrocell arrays.

An approximation to the power consumption for any design may be calculated by using the following equation.

P = Dynamic Power Consumption
+ Static (Quiescent) Power Consumption (Eq. 5-1)

$$P = V_{DD}^2 \sum_{i=1}^{n} (C_{Li})\, f_i + I_Q V_{DD}$$

where:

P is the total power consumption.

V_{DD} is the power-supply voltage.

n is the number of input buffers, internal macrocells, and output buffers in the design.

C_L is the load capacitance on the output of an individual input buffer, macrocell, or output buffer. C_L is calculated as described in Section 4.

f is the switching frequency at the output of the individual input buffer, macrocell, or output buffer.

I_Q is the total quiescent current flowing through the array, including the current from CMOS input buffers with pullup or pulldown resistors and TTL input buffers (see Section 8).

The summation indicates that accurate power-consumption approximations are made by considering each element (input buffer, macrocell, and output buffer) of the design individually. Less accurate approximations can be derived by considering only the elements that have high switching frequencies or high load capacitance.

Keep in mind that equation 5-1 only gives an approximation to the actual power that an array will dissipate. No consideration is given to the capacitance and switching frequency of internal nodes which may be present within a macrocell. The power consumed by internal nodes may increase the dynamic power consumption by 15 to 25 percent.

In equation 5-1, ideal square-wave input signals are assumed, but the equation is adequate for input rise and fall times up to approximately 200 ns.

EXAMPLE

This example shows the method for using equation 5-1 to calculate the power consumption of the simple circuit of Figure 5-1. Table 5-1 contains the dynamic power-consumption calculation. An example of the calculation of the numbers found in the C_L column of Table 5-1 is shown below (for an explanation of C_L and other examples, see Section 4). It is assumed that this circuit is to be placed on an HCA6348 array and that all output buffers are driving a 50 pF external load.

$$C_L = C_I + C_{INT} + C_Z$$

where: C_I = Input Capacitance (pF)
C_{INT} = Interconnect Capacitance (pF)
C_Z = 3-State Capacitance (pF)

For the Q output of C060:

C_I = (IUL of YOIN) (0.21 pF)
= (8)(0.21 pF)
= 1.68 pF

$C_{INT} = (C_{AVG})\,(L_T)\,(N)$
= (0.0058 pF/mil) (40 mils/conn) (2 conn)
= 0.46 pF

C_Z = 0 pF

C_L = 1.68 pF + 0.46 pF + 0 pF = 2.14 pF

For the QB output of C060:

C_I = [IUL of C060 (D Input) +
IUL of C034 (CK input)] (0.21 pF)
= (1 + 1) (0.21 pF)
= 0.42 pF

$C_{INT} = (C_{AVG})\,(L_T)\,(N)$
= (0.0058 pF/mil) (40 mils/conn) (3 conn)
= 0.69 pF

C_Z = 0 pF

C_L = 0.42 pF + 0.69 pF + 0 pF = 1.11 pF

5

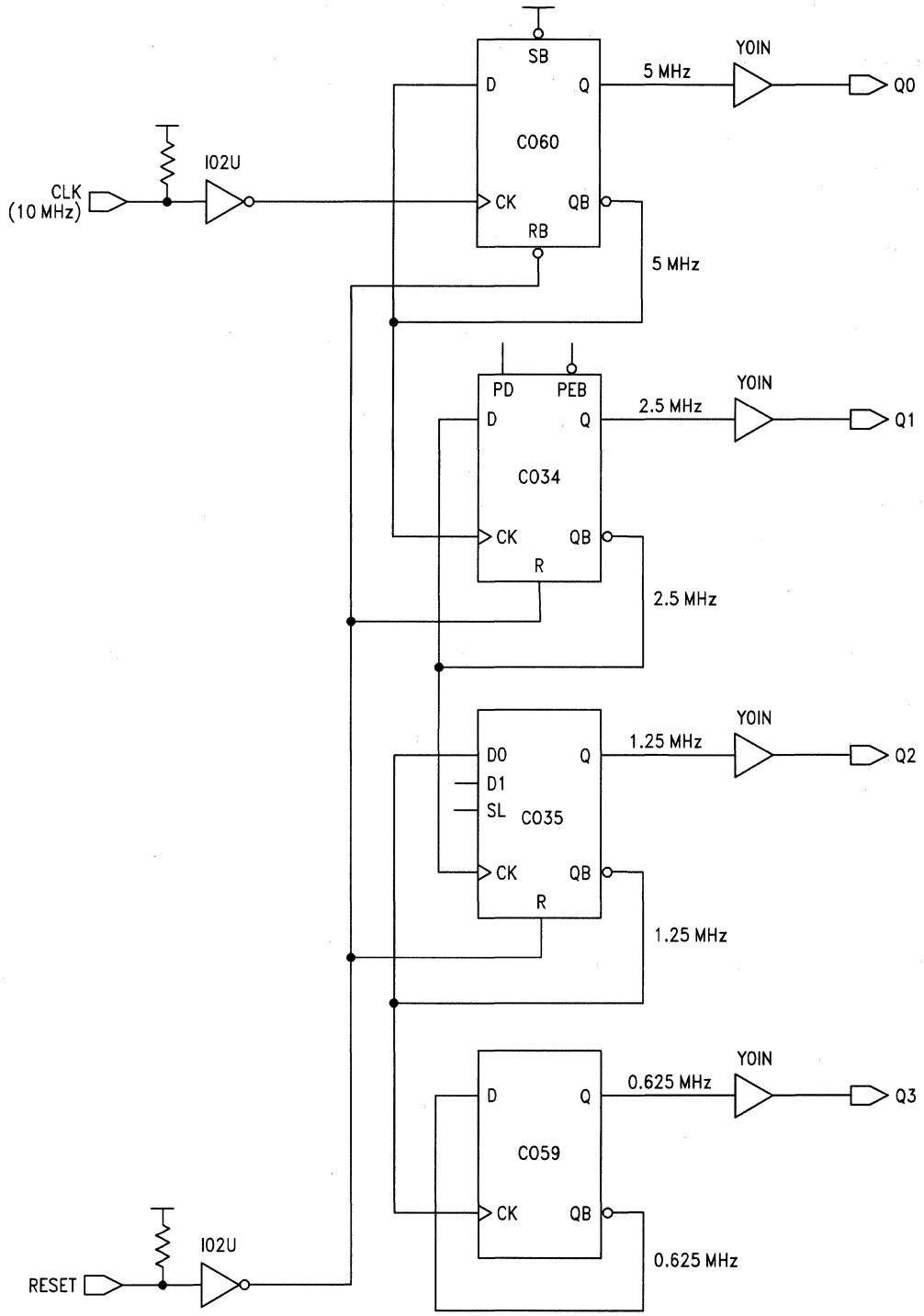


Figure 5-1. 4-Bit Counter Driving Four Outputs

Table 5-1. Dynamic Power Consumption

Macrocell Number	Macrocell Type	C_L (pF) $C_L = C_I + C_{INT}$	f (MHz)	V_{DD}^2 (V^2)	P_{DYN} (mW)
I02U	Input Buffer	$C_L = 0.21 + 0.46 = 0.67$	10	25	0.168
C060	Internal Array	Q: $C_L = 1.68 + 0.46 = 2.14$ QB: $C_L = 0.42 + 0.69 = 1.11$ Total = 3.25	5	25	0.406
C034		Q: $C_L = 1.68 + 0.46 = 2.14$ QB: $C_L = 0.42 + 0.69 = 1.11$ Total = 3.25	2.5	25	0.203
C035		Q: $C_L = 1.68 + 0.46 = 2.14$ QB: $C_L = 0.42 + 0.69 = 1.11$ Total = 3.25	1.25	25	0.102
C059		Q: $C_L = 1.68 + 0.46 = 2.14$ QB: $C_L = 0.21 + 0.46 = 0.67$ Total = 2.81	0.625	25	0.044
Y01N	Output Buffer	External Load = 50.0	5	25	6.250
Y01N		External Load = 50.0	2.5	25	3.125
Y01N		External Load = 50.0	1.25	25	1.562
Y01N		External Load = 50.0	0.625	25	0.781

Approximate Dynamic Power Consumption = 12.64 mW

The quiescent power consumption of the same circuit is calculated by using the I_{DD} data from the Electrical Characteristics table in Section 8. I_{DD} for a package is typically 0.075 mA, with a maximum of 1.00 mA. Current from pull-up, pull-down, and TTL input buffers must also be considered. For the circuit in Figure 5-1, an extra 0.030 mA (maximum) must be added for each of the input buffers having a pull-up device (I02U). Using the maximum numbers:

Static Power Consumption = [1.00 mA + 2 (0.03 mA)] × 5 V
= 5.30 mW

The total power consumption of the circuit is:

P = P (Dynamic) + P (Quiescent)
= 12.64 mW + 5.30 mW
= 17.94 mW

The circuit requires 13 cells, which is equivalent to 39 gates. If this circuit were duplicated enough times to fill an HCA6348 array (123 times, assuming the availability of enough pins), the total power consumption would be:

P_{4800} = (123 × 12.64 mW) + (5V) [1.00 mA + (123 × 2) (0.03 mA)]
= (1554.7 mW) + (41.90 mW)
= 1596.6 mW

The typcial amount of power that can be dissipated by the macrocell array packages varies from about 1.5 W for the 16-pin plastic DIP to about 4.0 W for the 124-PGA (at an ambient temperature of 25°C). Thus, as demonstrated above, CMOS macrocell arrays will rarely generate enough power to require external cooling.

Cell Counts 6

CELL COUNTS

Before any design can be placed on an HCA6000 Series Macrocell Array (MCA), a cell count must be performed. A cell count is the process of converting a design into macrocells from the Motorola CMOS macrocell library and, by doing so, determining the number of primary cells that the design will need. With this information a designer can select the HCA6000 Series array and package that will best suit the requirements of the design.

Before starting the process of changing a design's logic elements into CMOS macrocells, there are several points that should be taken into consideration because they may necessitate partial redesigns:

PACKAGE PREFERENCE

For any given design, there may be certain packages that are preferred over others. Because of this, each HCA6000 Series MCA is offered in a wide variety of package and pinout options. If packaging is of critical concern, however, a check should be made to be sure there is a match between package preference and package offering. This can be done by referring to Section 12 which contains package and pinout information for each array in the HCA6000 Series.

TEST PIN

All HCA6000 Series MCAs contain one Test-mode pin. The purpose of the Test-mode pin is to allow parameteric data to be checked without requiring a set of test vectors. The Test-mode pin must be included in the total pin count of all designs. For more information on the Test-mode pin see Section 3.

MEMORY

At the present time Motorola does not offer any type of RAM or ROM memory on HCA6000 Series MCAs. Any design that includes such memory will have to be altered so that the memory is not placed on the MCA.

OPERATING TEMPERATURE

The HCA6000 Series MCAs are intended to be used in the commercial temperature range (−40°C to +85°C). This will be expanded in the future to include military temperatures (−55°C to +125°C).

POWER SUPPLY

In order for HCA6000 Series MCAs to operate correctly, the power supply must be between 3 V and 6 V dc. Designs calling for supply voltages higher or lower than this may have to be modified.

ANALOG

At present, analog elements cannot be placed on HCA6000 Series MCAs.

After a design has been checked to see that it does not violate any of the above restrictions, a list of all logic functions and the number of times each logic function occurs in the design should be made. When making this list there is no need to count any input or output buffers that the design may have. All inputs and outputs on HCA6000 Series MCAs are made through buffers (input, output or bidirectional) chosen by the user. Therefore, there is no need to duplicate these buffers with additional macrocells in the internal array. For example, if the design shown in Figure 6-1 was to be placed on an HCA6000 Series MCA, the logic function list would look like this:

3 Inverters
2 R-S Latches
4 2-Input NAND Gates
4 2-Input NOR Gates

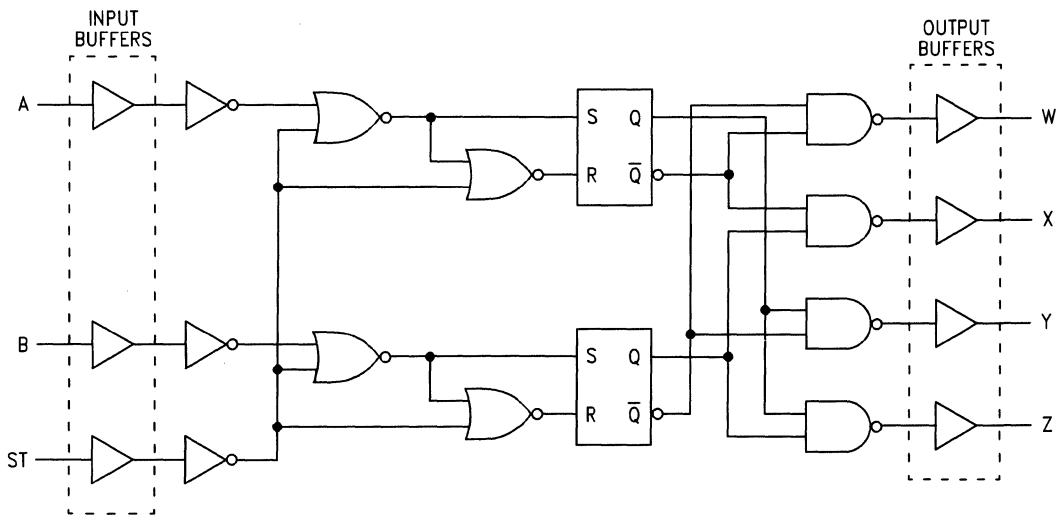


Figure 6-1. Circuit to be Built Using HCA6000 Series Macrocells

Once each of the logic functions has been identified and counted, a macrocell to implement each function is found by referring to Section 11. This process is very similar to designing with TTL components. The difference is that instead of using the parts in a TTL data book to perform the needed logic functions, macrocells from the macrocell library are used. Each of these macrocells is fully characterized and described in Section 11. For Figure 6-1, the macrocells shown in Table 6-1 could be used.

Table 6-1. Information Obtained from Data Sheets of Macrocells That Could Be Used to Build the Circuit Shown in Figure 6-1

Macrocell	Logic Function	Primary Cells Per Macrocell	Number of Functions Per Macrocell
C008	Inverter	1	4
C013	R-S Latch	1	1
	2-Input NOR		1
C001	2-Input NAND	1	3
C004	2-Input NOR	1	3

In this example each macrocell takes up one primary cell (some require two or more). Notice, however, that the number of functions per macrocell varies between one and four (e.g. each C008 contains four inverters, each C001 contains three 2-Input NAND gates, each C013 contains one R-S Latch and one 2-Input NOR, etc.). With this information the number of primary cells that will be needed for the design can be calculated as shown in Table 6-2.

An important point is illustrated by this example. Just as it is not possible to place only part of a TTL package on a circuit board, it is not possible to place a fraction of a macrocell on an array. The design shown in Figure 6-1 requires four 2-Input NAND gates. Each C001 macrocell contains three 2-Input NAND gates and takes up one primary cell. Since four 2-Input NAND gates are needed, two C001s must be used for a total of six gates contained in two primary cells. The extra two gates in the second C001 can either be used in additional circuitry or left uncommitted. This also applies to the unused inverter in the C008.

A question may also arise as to why only one C004 (which contains three 2-Input NOR gates) is used when four NOR gates are needed. The answer is due to the use of the two C013s. Each C013 contains one R-S Latch and one 2-Input NOR gate. Since two C013s are needed for the R-S Latches, and because it is not possible to place just the R-S Latch portion of the C013 on the array, the NOR gate that comes with each latch is used as part of the four that are needed for the design. By using the NOR gate in each of the C013s, the number of NOR gates needed for the design is reduced to two. Thus, only one C004 is needed.

In some instances, there will be a macrocell that completely performs a function that is needed in a design. For example, in Figure 6-1 the following functions were required:

Inverter
R-S Latch
2-Input NAND
2-Input NOR

In each of these cases a macrocell was found that performed the exact function needed. At other times a logic function required in a design may not exactly match one of the macrocells being offered. In such situations it is possible to build the needed function from the available macrocells by breaking the function down into its basic components. For example, a design might call for a 1-of-16 decoder with active low outputs. By referencing Section 11 it can be seen that there is no macrocell that performs this specific function. Such a function can, however, be constructed using various macrocells. A 1-of-16 decoder could be made as shown in Figure 6-2.

Another example is shown in Figure 6-3. In this case, a 4-bit D-type register with 3-state outputs (LS173) is built from elements found in the macrocell library.

Table 6-2. Cell Count for Circuit Shown in Figure 6-1

Function Required By Design	Number Of Functions Required By Design	Macrocell To Implement Function	Primary Cells Per Macrocell	Functions Per Macrocell	Primary Cells Required
Inverter	3	C008	1	4 Inverters	1
R-S Latch	2	C013	1	1 R-S Latch 1 2-Input NOR	2
2-Input NAND	4	C001	1	3 2-Input NAND	2
2-Input NOR	4	C004	1	3 2-Input NOR	1*

*Only one Primary cell is needed because a NOR gate from C013 can be used. TOTAL PRIMARY CELLS = 6

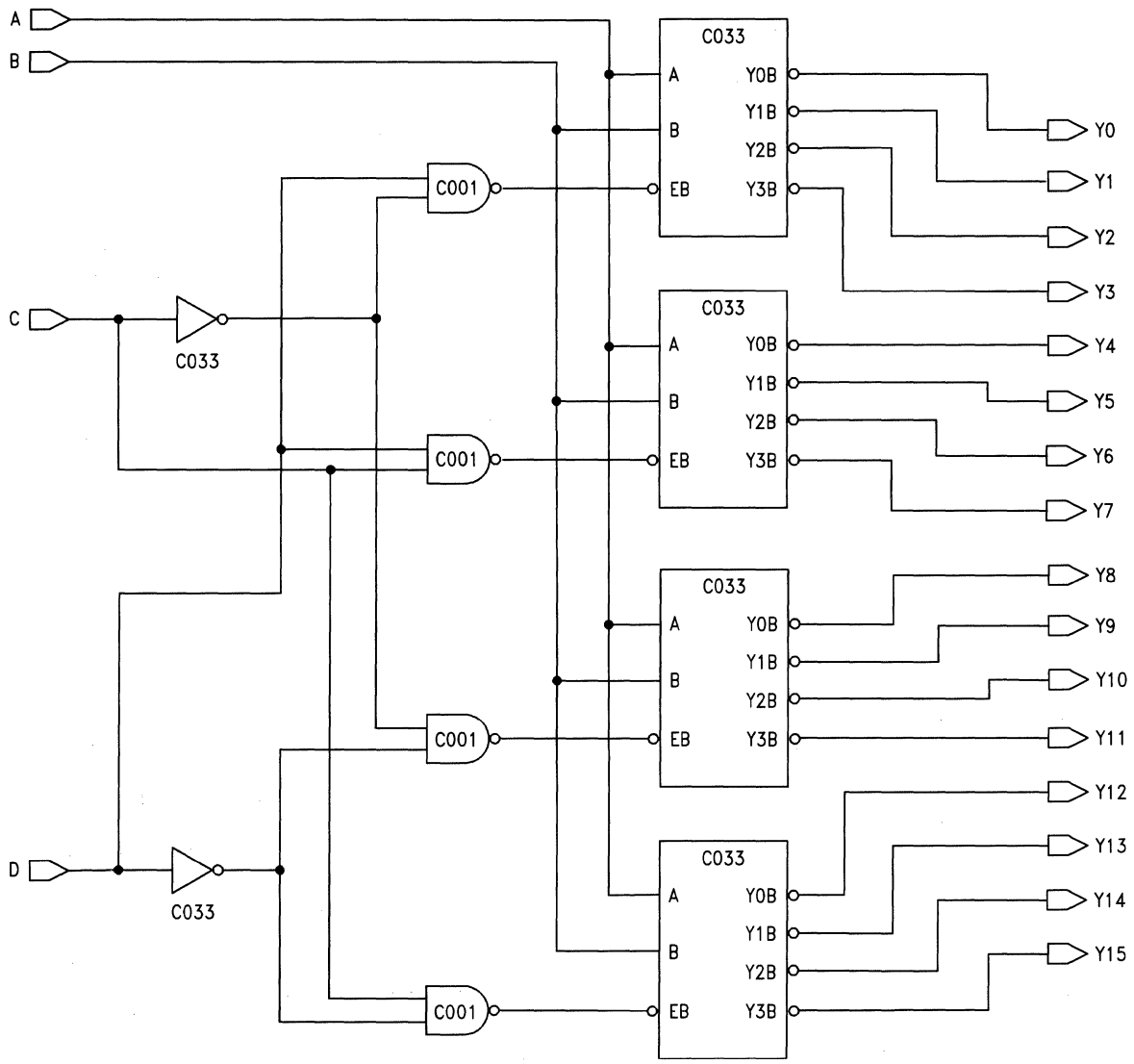


Figure 6-2. 1-of-16 Decoder with Active Low Outputs Built Using 2 Macrocells (C033, C001) and 18 Primary Cells

After each logic function on a design has been converted into its equivalent macrocell or built using a combination of macrocells, the total number of macrocells needed for the design will be known. Then, with the primary cell information provided on each macrocell data sheet, the total number of primary cells can be calculated as shown in Table 6-2.

The last step is to total all of the inputs and outputs on the design (plus one for the Test-mode pin) and match both the total primary cells and the total I/O count to an array size and package. This can be done by referring to Section 10, which contains package, pinout, and primary cell information for each array in the HCA6000 series. At this point the number of equivalent gates in a design may also be found by multiplying the number of primary cells by three. This is due to the fact that a "gate" for HCA6000 Series MCAs is considered to be a 2-Input NAND, and three 2-Input NAND gates can be placed in one primary cell.

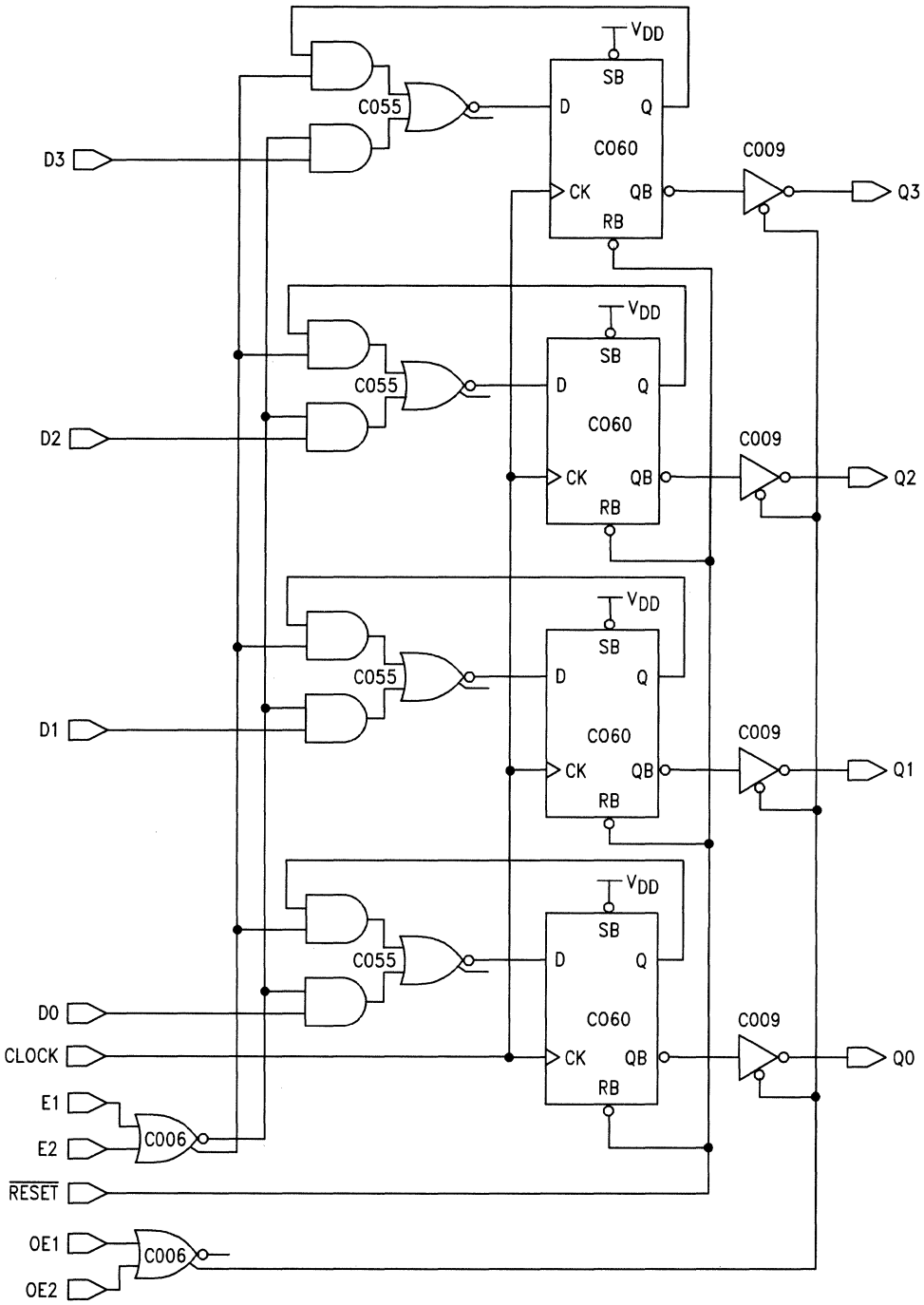


Figure 6-3. Implementation of an LS173 Using 4 Macrocells (C055, C009, C006, C060) and 19 Primary Cells

Design for Testability 7

DESIGNING FOR TESTABILITY

As the circuits being designed and implemented in silicon become larger, the problem of testing the circuits becomes greater. For VLSI semicustom circuits, testability must be a consideration from the beginning of the design. Better testability increases circuit performance and reliability, while it decreases cost and development time.

This section suggests to the macrocell array designer some techniques that should be used to insure testability. The techniques involve the basic concepts of observability and controllability:

Observability connotes the ability of the designer to monitor critical internal nodes of the circuit by bringing them out to pins.

Controllability connotes the ability of the designer to place the internal nodes of the circuit into known states, from which all future states may be predicted.

Whatever test strategy is to be used, implement it early in the design cycle and stick to it. The Motorola macrocell library includes macrocells that support particular test strategies (for example, the C084 macrocell supports the LSSD technique).

MACROCELL ARRAY CIRCUIT-DESIGN TECHNIQUES

OBSERVABILITY

1. Design using dedicated test pins to monitor critical nodes of the circuit. If no dedicated test pins can be made available, it may be possible to replace some output buffers with bidirectional buffers and use the newly created inputs as test inputs. The same method may be used with input buffers to create test outputs. Also, output pins may be multiplexed between normal circuit functioning and test-circuit functioning.
2. As a last resort, when the above methods can not be used, it may be possible, to use the normal circuit inputs for testing. This is done by using input logic combinations that will not occur under normal circuit operation and internally decoding them as test modes.
3. Use test pins to exercise the I/O buffers independently of the internal logic. Note that the testing of I/O buffers is already provided for on Motorola's Macrocell Arrays, with the Test-mode, Test Data, and Test 3-state pins.

CONTROLLABILITY

1. Design using dedicated test logic to provide and control such functions as reset, three-state output enable, preset, data-bus enable, or other means of initializing and controlling the states of the logic.
2. Do not design flip flops, registers, latches, and counters to which there is no access for presetting or initialization.
3. Partition large circuits into smaller, more manageable circuits that will allow the use of control and test logic.
4. Design using synchronous logic. Asynchronous designs can exhibit race conditions that vary as IC processing varies and that may not appear on CAD simulations. Do not allow any unclocked feedback paths, such as those found in ring oscillators.
5. Design so that the circuit does not depend upon internal propagation delays for timing. Such delays will be unreliable, and race-condition problems may arise:
   A. Avoid race conditions to macrocells (such as between data and clock, set and clock, reset and clock, preset and clock, or preset data and preset enable).
   B. Avoid using internal gate delays to create pulses. Specified minimum pulse widths are in the 20- to 30-nanosecond range, but typical minimum pulse widths vary widely as a function of processing.
   C. When using more than one clock, design for worst-case skewing between clocks (approximately 30 nanoseconds).
6. Avoid having large fanouts on edge-sensitive macrocell inputs. A large fanout causes slow rise and fall times, which may result in oscillations, circuit timing problems, or excessive current draw. The maximum rise and fall times that should be seen by the inputs of any macrocell is 500 nanoseconds.
7. Design so that three-state macrocells do not remain in the high-impedance state for an indefinite period of time. This will prevent the macrocell, and subsequent macrocells that are driven by the three-state macrocell, from drawing current unnecessarily.
8. Use several pairs of power-supply (V_{DD} and V_{SS}) pins, especially in designs with high I/O counts. Typically one pair of power-supply pins is needed for every sixteen outputs that could change state at the same time.

SIMULATION AND TEST-PROGRAM TECHNIQUES

OBSERVABILITY

1. During functional and ac simulation, observe several internal nodes, to insure that the circuit is functioning as desired.
2. Keep in mind that Motorola's functional and ac simulators use, at the designer's option, either worst-case conditions (V_{DD} = 4.5 V, temperature = 85°C, $t_r = t_f$ = 5 ns, worst-case processing) or best-case conditions (V_{DD} = 5.5 V, temperature = −40°C, $t_r = t_f$ = 1 ns, best-case processing).

CONTROLLABILITY

1. To avoid long counting sequences during simulation and testing, design counters so that they are broken up, with each section separately presettable. This allows simulation and test steps (vectors) to be used for simulation and testing; not for counting.
2. Because the Motorola CAD simulator used in the macrocell array design process is a functional simulator, rise and fall times are not simulated and violations will not be discovered. However, the impact on propagation delays caused by metal-interconnect lengths and fanout is simulated. This simulation may be done both before and after the macrocells are placed and routed on the array.
3. One important simulation function is to insure that the device can be tested by Motorola's wafer-probe and final-test equipment.
   Race conditions may exist not only because of design flaws, but also because of IC tester limitations. Ideally, a test system would simultaneously apply all input test vectors and later compare circuit outputs with simulation results. Actually, IC testers for macrocell arrays can have more than 20 nanoseconds of skew between needle points (bonding pads) at wafer probe. For this reason, a circuit that simulates properly and is designed for proper flip-flop setup and hold times can fail at wafer probe or final test.
   Designers should be aware of the possibility of tester race conditions and should define test vectors accordingly:
   A. When specifying timing relations, try to allow enough margin to take into account the possible skew of the tester.
   B. When using more than one clock, design for worst-case skewing between clocks.
   C. To avoid skewing problems, do not change any input signal to a clocked macrocell on the active clock edge.
   D. The IRACE and TEST (AC simulation options available on the Motorola CAD system can help identify potential race conditions in the test vector (SPATTERN) file.
4. The Motorola CAD simulator does not check for minimum pulse-width violations. Make sure that the timing specifications for all macrocells are met.
5. Guidelines for creating test vectors:
   A. Simulation (and test) vectors may be different from the input sequence of the actual system application.
   B. Initialize all storage elements at the beginning of the simulation (and test) sequences.
   C. Do not clock a macrocell and change the data on the same vector.
   D. Do not clock macrocells or change data on the vector after a reset or enable signal is removed. There may not have been sufficient recovery time, and the new data may not get clocked in. Unpredictable simulation results may occur.
6. Use the Motorola simulator to help indentify and correct potential problems with test vectors. After the test vector file (SPATTERN or ACPATT) is complete, and the circuit has been successfully simulated:
   A. run the simulation again using the IRACE and the TEST (AC options.
   B. add delays to selected input signals by using the $DELAY or $ACDELAY statements in the FIX file, and run the simulation again.
   If the results of the simulations are different, the above suggestions have been violated and the resulting problems must be corrected.
7. Within the Motorola simulator it is possible to initialize any or all storage elements in the design by using the $SET or $RESET commands in the SPATTERN file. IC testers do not have this automatic initialization capability. In actual operation, when powered up, the storage elements can be in either a set or a reset state, and this power-up state can change from circuit to circuit. A simulation test pattern that depends upon initialized storage elements will almost certainly fail actual test at wafer probe or final test.
   Initialization should be accomplished by signals on the Set or Reset inputs, or by clocking in known data. Do not use simulation initialization commands in the final SPATTERN or ACPATT files.

8. Do not design using flip-flops that self-initialize; or otherwise have the circuit provide the logic necessary to put the output into a desired state. Problems arise because the simulator is not able to do the same initialization procedure. The simulator will show an output of "X" (for undetermined), which will continue to propagate indefinitely.
   Although the Motorola simulator $SET and $RESET commands appear to solve the problem, it is difficult to insure that circuit self-initialization and simulator self-initialization will occur at the same time. Thus, simulation outputs may not agree with later final-test results.

SCAN-PATH DESIGN

This test method, which includes Level-Sensitive Scan Design (LSSD), consists of converting a sequential circuit to an entirely combinational one. This is accomplished by combining all the flip-flops to form a shift register, so that test data can be shifted into each flip-flop and then clocked data shifted out of the shift register.

The advantages of this method are that test-pattern generation is much simpler for combinational logic than it is for sequential logic. Also, fault coverage can easily approach 100% of the detectable faults. The disadvantages include an increase in silicon area, an increase in the test time because of the repeated shifting of data in and out of the circuit, and some decrease in performance due to the additional circuitry. The result, however, is a testable and reliable circuit.

The Motorola Macrocell library includes macrocells that have been designed especially for Scan-Path Design circuits:

Macrocells Used For Increased Testability

C035	Multiplexed D Flip-Flop with Reset
C084	LSSD Shift Register Latch
C700	Dual LSSD L2 Latch
C701	LSSD L1 Latch with ANDed D Inputs
C702	LSSD Dual-Port L1 Latch
C703	LSSD R-S L1 Latch

For implementation examples, refer to the individual data sheets. A general testing methodology is given below, excerpted from Reference 1:

STEP 1: Place the device in the Scan-Path mode, with the flip-flops or other storage elements reconfigured into a shift register. Test the status and operation of each storage element using a Scan-Data In input, a Scan-Data Out output, and a System Clock. Suitable tests for a scan-path register are as follows:

a) Flush Test: In this test, all storage elements are initialized to 0 and a single 1 is clocked through from the Scan-Data In input to the Scan-Data Out output using the System Clock. The procedure can be repeated with a single 0 flushed through a background of 1's. This sequence checks the ability of each storage element to assume both a 0 state and a 1 state.
b) Shift Test: In this test, the sequence 00110011... is shifted through the register. This sequence exercises each storage element through all combinations of present state and future state.

STEP 2: Determine a set of tests for the combinational logic, assuming:

a) total control of all inputs (primary and from the storage elements);
b) direct observability of all outputs (primary and to the storage elements).

STEP 3: Apply each test using the following sequence:

a) Select the Scan-Path mode. Preload the storage elements with test input values and establish additional test input values on the primary inputs.
b) Select the Normal-Operation mode. The steady state output response of the combinational logic can now be clocked into the storage elements.
c) Return to the Scan-Path mode and clock out the contents of the storage elements. Compare these values, plus the values directly observable on the primary outputs, with the expected fault-free response.

REFERENCES

The following books and articles provide more information on designing for testability.

1) Bennetts, R. G., Design of Testable Logic Structures, Addison-Wesley, 1984.

2) Eichelberger, E. B., and Williams, T. W., "A Logic Design Structure for LSI Testability," Journal of Design Automation and Fault-Tolerant Computing, vol. 2, no. 2, May 1978, pp. 165–178.

3) Williams, T. W., et al, "Design for Testability - A Survey," IEEE Transactions on Computers, January 1983, Vol. C31, No. 1.

Electrical Characteristics

8

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD}	25°C Typical	−40 to +85°C Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage, CMOS Input	V_{out} = 0.1 V or V_{DD} − 0.1 V $\|I_{out}\|$ = 20 μA	4.5	2.4	3.15	V
			5.5	2.9	3.85	
	Minimum High-Level Input Voltage, TTL Input	V_{out} = 0.1 V or V_{DD} − 0.1 V $\|I_{out}\|$ = 20 μA	4.5	1.6	2.0	
			5.5	1.6	2.0	
V_{IL}	Maximum Low-Level Input Voltage, CMOS Input	V_{out} = 0.1 V or V_{DD} − 0.1 V $\|I_{out}\|$ = 20 μA	4.5	1.8	1.35	V
			5.5	2.2	1.65	
	Maximum Low-Level Input Voltage, TTL Input	V_{out} = 0.1 V or V_{DD} − 0.1 V $\|I_{out}\|$ = 20 μA	4.5	1.2	0.8	
			5.5	1.2	0.8	
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = −20 μA	4.5	4.499	4.4	V
			5.5	5.499	5.4	
		V_{in} = V_{IH} or V_{IL} I_{out} = −4.0 mA	4.5	4.0	3.70	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{out} = 20 μA	4.5	0.001	0.1	V
			5.5	0.001	0.1	
		V_{in} = V_{IH} or V_{IL} I_{out} = 4.0 mA	4.5	0.20	0.40	
I_{in}	Maximum Input Leakage Current, No Pull Resistor	V_{in} = V_{DD} or V_{SS}	5.5	±0.00001	±1.0	μA
	Maximum Input Current, Pull-Up Resistor	V_{in} = V_{SS}	4.5	—	−25	
			5.5	—	−30	
	Maximum Input Current, Pull-Down Resistor	V_{In} = V_{DD}	4.5	—	70	
			5.5	—	80	
I_{OZ}	Maximum Output Leakage Current, Three-State Output	Output = High Impedance V_{out} = V_{DD} or V_{SS}	5.5	±0.05	±5	μA
	Maximum Output Leakage Current, Open Drain Output	Output = High Impedance V_{out} = V_{DD}	5.5	±0.05	±5	
I_{DD}	Maximum Quiescent Supply Current, No Pull-Up or Pull-Down Resistor	V_{in} = V_{DD} or V_{SS} I_{out} = 0 μA CMOS Inputs	5.5	75	1000	μA
	Maximum Additional Quiescent Supply Current:					μA
I_{DD}	Add Per Pull-Up Resistor Input	V_{in} = V_{SS}	5.5	—	30	
I_{SS}	Add Per Pull-Down Resistor Input	V_{in} = V_{DD}	5.5	—	80	
I_{DD}	Add Per TTL Input	V_{in} = 0.8 V or 2.0 V	5.5	—	400	
C_{in}	Maximum Input Capacitance		—	—	10	pF
C_{out}	Maximum Output Capacitance	Output = High Impedance	—	—	15	pF
$C_{I/O}$	Maximum I/O Capacitance	Configured as Input	—	—	20	pF

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to 7.0	V
V_{in}, V_{out}	DC Input, Output Voltage	−0.5 to V_{DD} +0.5	V
I	DC Current Drain Per Pin, Any Input or Output	25	mA
I	DC Current Drain V_{CC} and GND Pins	50	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage	3.0	6.0	V
V_{in}, V_{out}	Input Voltage, Output Voltage	0.0	V_{DD}	V
T_A	Operating Temperature	−40.0	+85.0	°C
t_r, t_f	Rise and Fall Times	—	500	ns

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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Definitions of Specifications 9

DEFINITIONS OF SPECIFICATIONS

CURRENT

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{DD} **Quiescent Positive Supply Current**
The amount of current flowing into the V_{DD} pin(s) of a macrocell array with no internal nodes switching state. This includes current from inputs with pull-up resistors and/or TTL inputs.

I_{in} **Input Leakage Current**
The leakage current flowing into or out of an input under specified conditions.

I_{OZ} **3-State Output Leakage Current**
The leakage current flowing into or out of a 3-state output in the high impedance state under specified conditions.

I_{SS} **Quiescent Negative Supply Current**
The amount of current flowing out of the V_{SS} pin(s) of a macrocell array with no internal nodes switching state. This includes any current from inputs with pull-down resistors.

VOLTAGE

All voltages are referenced to ground (V_{SS}).

V_{DD} **Positive Power Supply Voltage.**

V_{IH} **Input HIGH Voltage**
The minimum voltage that represents a logic HIGH at an input.

V_{IL} **Input LOW Voltage**
The maximum voltage that represents a logic LOW at an input.

V_{OH} **Output HIGH Voltage**
The minimum voltage at an output terminal for the specified output current.

V_{OL} **Output LOW Voltage**
The maximum voltage at an output terminal for the specified output current.

V_{SS} **Negative Power Supply Voltage.**

CAPACITANCE

C_{in} **Input Capacitance of Input Buffers**
The amount of capacitance associated with the input of an input buffer.

C_I **Input Capacitance of Internal Macrocells**
The amount of capacitance associated with the input of an internal array macrocell.

$C_{I/O}$ **Input Capacitance of Bidirectional Buffers**
The amount of capacitance associated with the input of a bidirectional buffer when using it as an input.

C_L **Load Capacitance**
The amount of capacitance an output must charge and discharge.

C_{INT} **Interconnect Capacitance**
The amount of capacitance associated with metal used to connect internal macrocells.

C_{out} **Output Capacitance of Output Buffers**
The amount of capacitance associated with the output of an output buffer or a bidirectional buffer being used as an output, while in high-impedance state.

C_Z **Output Capacitance of Internal 3-State Macrocells**
The amount of capacitance associated with the output of an internal macrocell in high impedance state.

AC SWITCHING PARAMETERS AND WAVEFORMS

t_{PLH} **Propagation Delay LOW-TO-HIGH**
The time delay from an input signal to the LOW-TO-HIGH transition of an output signal (see Figures 9–1 through 9–4).

t_{PHL} **Propagation Delay HIGH-TO-LOW**
The time delay from an input signal to the HIGH-TO-LOW transition of an output signal (see Figures 9-1 through 9-4).

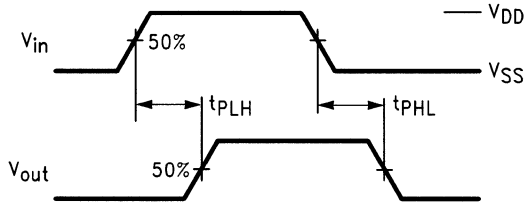

Figure 9-1. Non-Inverting CMOS Input Buffers, Output Buffers and Internal Macrocells

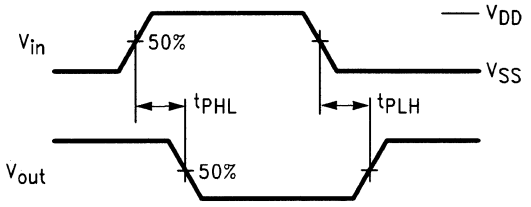

Figure 9-2. Inverting CMOS Input Buffers, Output Buffers and Internal Macrocells

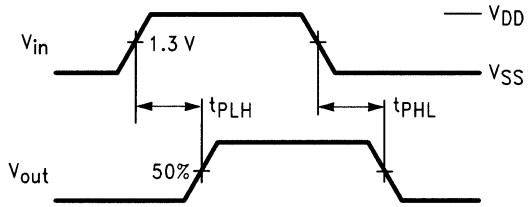

Figure 9-3. Non-Inverting TTL Input Buffers

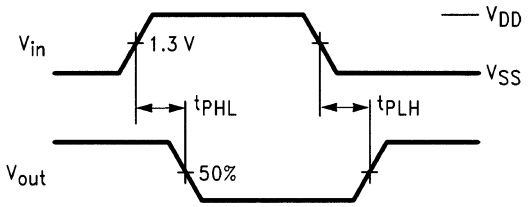

Figure 9-4. Inverting TTL Input Buffers

t_r **Input Signal Rise Time**
LOW-TO-HIGH logic transition time on an input, measured from the 10% to the 90% points of the waveform (see Figure 9-5).

t_f **Input Signal Fall Time**
HIGH-TO-LOW logic transition time on an input, measured from the 90% to the 10% points of the waveform (see Figure 9-5).

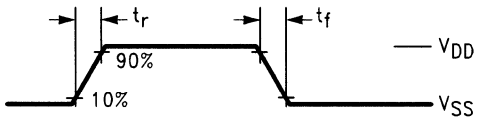

Figure 9-5. t_r and t_f Measurements

t_{PHZ} **Output Disable Time HIGH-TO-Z**
The time delay from an enable signal to where the output is going from an active HIGH level into a 3-state level. For internal macrocells this measurement is independent of load capacitance (see Figures 9-6 and 9-7).

t_{PLZ} **Output Disable Time LOW-TO-Z**
The time delay from an enable signal to where the output is going from an active LOW level into a 3-state level. For internal macrocells this measurement is independent of load capacitance (see Figures 9-6 and 9-7).

t_{PZH} **Output Enable Time Z-TO-HIGH**
The time delay from an enable signal to where the output is going from a 3-state level to an active HIGH level (see Figures 9-6 and 9-7).

t_{PZL} **Output Enable Time Z-TO-LOW**
The time delay from an enable signal to where the output is going from a 3-state level to an active LOW level (see Figures 9-6 and 9-7).

9

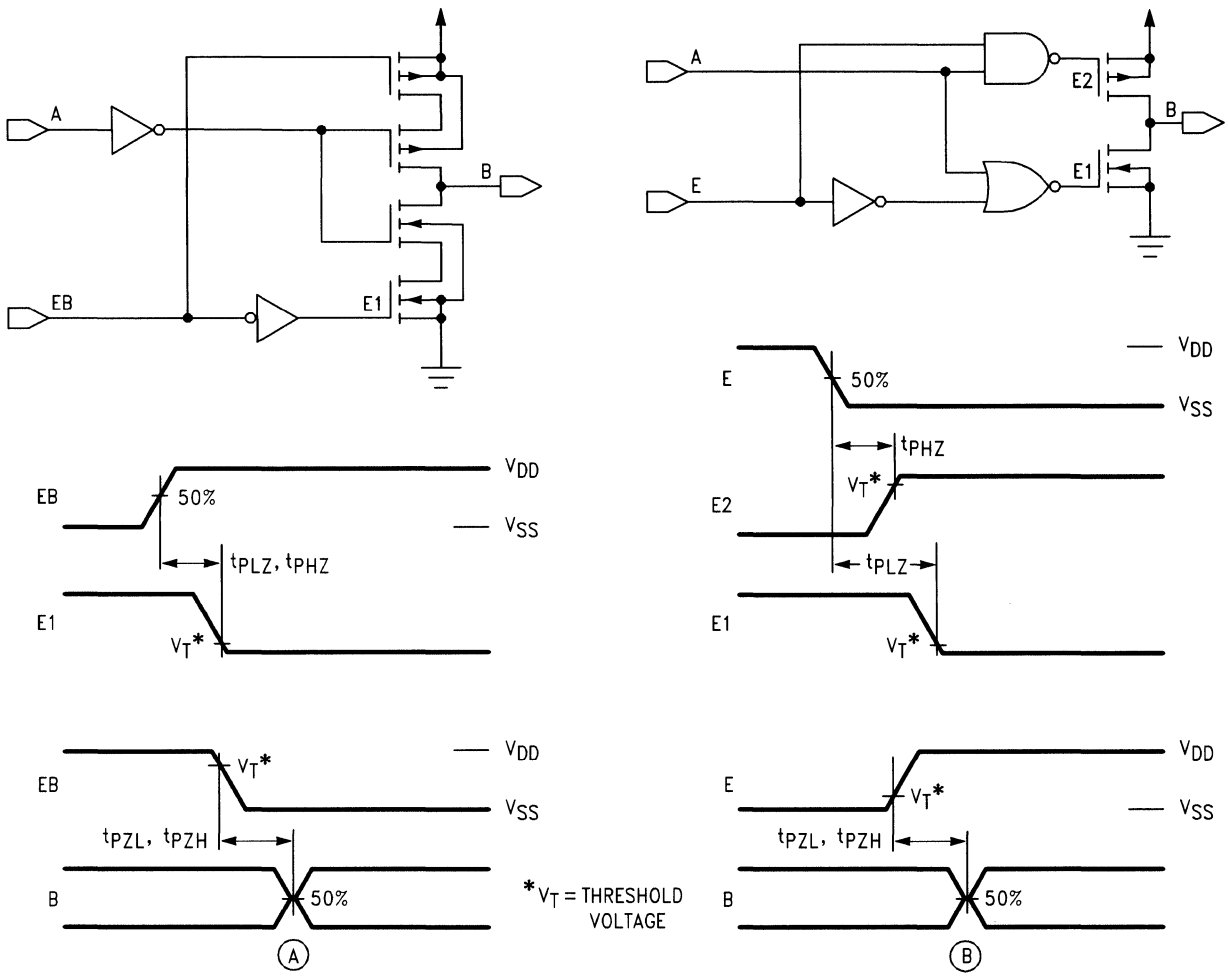

Figure 9-6. Internal Macrocell 3-State Measurements and Example Circuits for A) Active LOW Enabled, and B) Active HIGH Enabled Macrocells

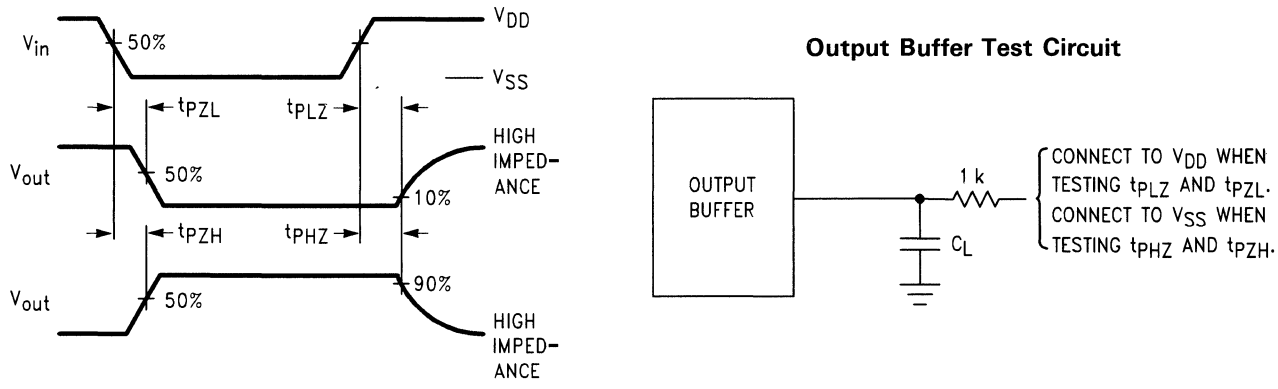

Figure 9-7. Output Buffer 3-State Measurements and Test Circuit

9

t_{rec} **Recovery Time**
The amount of time between the disabling edge of an asynchronous signal (set, reset, load) and the enabling edge of a synchronous signal (clock) (see Figure 9-8).

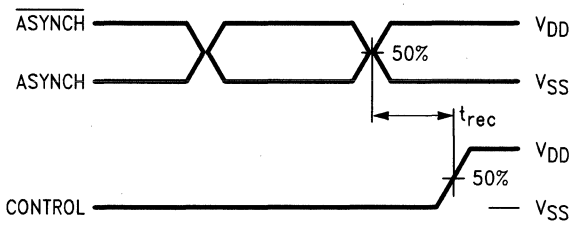

Figure 9-8. Recovery Time, t_{rec}

t_h **Hold Time**
The minimum time during which data to be recognized must remain constant after the specified edge of the control signal (usually the clock) to ensure proper data recognition. (see Figures 9-9 and 9-10).

t_{su} **Setup Time**
The amount of time during which data to be recognized must remain constant prior to the specified edge of the control signal to ensure proper data recognition (see Figures 9-9 and 9-10).

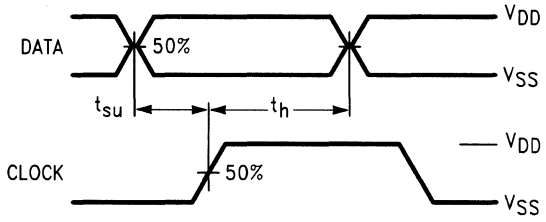

Figure 9-9. t_{su} and t_h Measurements Between Data and Clock Signals of a Flip-Flop

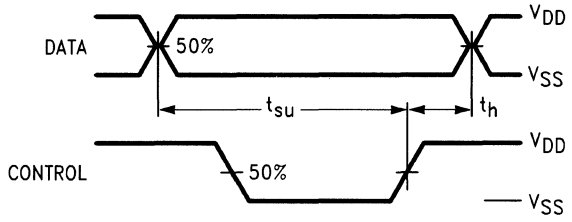

Figure 9-10. t_{su} and t_h Measurements Between Data and a Control Signal (usually EB) for Enabled or Preset/Enabled Macrocells.

$t_{w(H)}$ **Pulse Width (HIGH)**
The time between the 50% point of the rising edge and the 50% point of the falling edge of a pulse (see Figure 9-11).

$t_{w(L)}$ **Pulse Width (LOW)**
The time between the 50% point of the falling edge and the 50% point of the rising edge of a pulse (see Figure 9-11).

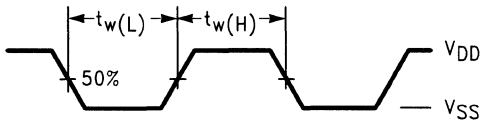

Figure 9-11. Switching Waveform Showing $t_{w(L)}$ and $t_{w(H)}$ Measurements

f_{max} **Maximum Operating Frequency**
The maximum rate at which clock pulses meeting the clock requirements (i.e., t_w, t_r, t_f, 50% duty cycle) may be applied to a sequential circuit. Above this frequency the device is not guaranteed to function.

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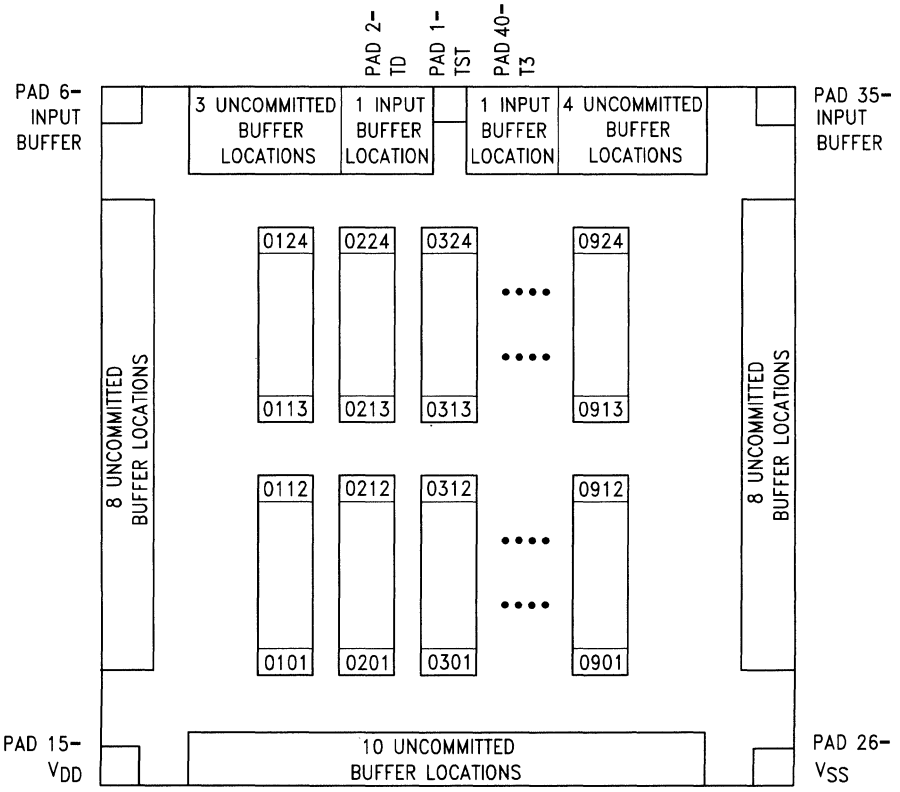
Base-Array Data Sheets 10

HCA6206
HCA6306

2- and 3-Micron 600 Gate Macrocell Array

The HCA6206/6306 provides a total of 216 primary cells contained within 8 columns. There are a maximum of 4 input buffer locations and 33 uncommitted buffer locations. Also available are a maximum of 4 power and ground locations (2 V_{DD}, 2 V_{SS}). The electrical characteristics of the HCA6206/6306 are described in Section 8.

FLOORPLAN



VERTICAL ROUTING (First layer metal)

Routing Channel	1	2	3	4	5	6	7	8	9	10
Number of Tracks	14	14	14	14	14	14	14	14	14	14

Total Vertical Tracks = 140

HORIZONTAL ROUTING (Second layer metal)

10 Tracks per primary cell (24 cells) = 240 Tracks
9 Tracks top and bottom of columns = 18 Tracks
Total Horizontal Tracks = 258

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PERIPHERY OPTIONS AND PLACEMENT

Available Periphery Options	Input Location	Uncommitted Location	TD Location	T3 Location
Bidirectional Buffers				
B02N		X		
B02U		X		
B02D		X		
B03N		X		
B03U		X		
B03D		X		
B04N		X		
B04U		X		
B04D		X		
B05N		X		
B05U		X		
B05D		X		
Output Buffers				
Y01N		X		
Y02N		X		
Input Buffers				
I01N	X	X	X	X
I01U	X	X	X	X
I01D	X	X	X	X
I02N	X	X	X	X
I02U	X	X	X	X
I02D	X	X	X	X
I03N	X	X	X	X
I03U	X	X	X	X
I03D	X	X	X	X
I05N	X	X	X	X
I05U	X	X	X	X
I05D	X	X	X	X
I06N	X	X	X	X
I06U	X	X	X	X
I06D	X	X	X	X
I07N	X	X	X	X
I07U	X	X	X	X
I07D	X	X	X	X
I08N	X	X	X	X
I08U	X	X	X	X
I08D	X	X	X	X
I09N		X		
I10N		X		
I10U		X		
I10D		X		

TD = Test Data Pin
T3 = Test 3-State Pin

10

PAD TO PIN CROSS REFERENCE GUIDE

IC Pad	Package			Pin Type
	28 Pin DIP Option 1	40 Pin DIP Option 1	44 Pin LCC or PCC Option 1	
1	1	1	1	TST
2	2	2	3	TD/Input
3	—	3	4	I/O
4	—	4	5	I/O
5	3	5	6	I/O
6	4	6	7	Input
7	5	7	8	I/O
8	—	8	9	I/O
9	6	9	10	I/O
10	7	10	11	I/O
11	8	11	13	I/O
12	9	12	14	I/O
13	—	13	15	I/O
14	10	14	16	I/O
15	11	15	17	V_{DD}
16	12	16	18	I/O
17	—	17	19	I/O
18	13	18	20	I/O
19	—	19	21	I/O
20	14	20	22	I/O
21	15	21	24	I/O
22	—	22	25	I/O
23	16	23	26	I/O
24	—	14	27	I/O
25	17	25	28	I/O
26	18	26	29	V_{SS}
27	19	27	30	I/O
28	—	28	31	I/O
29	20	29	32	I/O
30	21	30	33	I/O
31	22	31	35	I/O
32	—	32	36	I/O
33	23	33	37	I/O
34	24	34	38	I/O
35	25	35	39	Input
36	26	36	40	I/O
37	—	37	41	I/O
38	27	38	42	I/O
39	—	39	43	I/O
40	28	40	44	T3/Input

PACKAGING

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6206	016PDIP1	2	11	1	1	1	0
	028PDIP1 028HDIP1 028-LCC1 028-PCC1	4	21	1	1	1	0
	040PDIP1 040HDIP1	4	33	1	1	1	0
	044-LCC1 044-PCC1	4	33	1	1	1	4
HCA6306	028PDIP1 028HDIP1	4	21	1	1	1	0
	040PDIP1 040HDIP1	4	33	1	1	1	0
	044-LCC1 044-PCC1	4	33	1	1	1	4

Package Abbreviations for this Publication:
PDIP: Plastic Dual In-Line Package
HDIP: Side-Brazed Ceramic Dual In-Line Carrier
LCC: Ceramic Leadless Chip Carrier
PCC: Plastic Leaded Chip Carrier (Quad Pack)

TEST MODE FUNCTION TABLE

Input			Output Buffer Type	Output
Test Mode	Test Data	Test 3-State		
L	X	X	X	From Array
H	X	H	Any	Z
H	H	L	Bidirectional	L
H	L	L	Option	H
H	H	X	Y02N	L
H	L	X	Y02N	Z
H	H	X	Y01N	L
H	L	X	Y01N	H

X = Don't Care
Z = High Impedance

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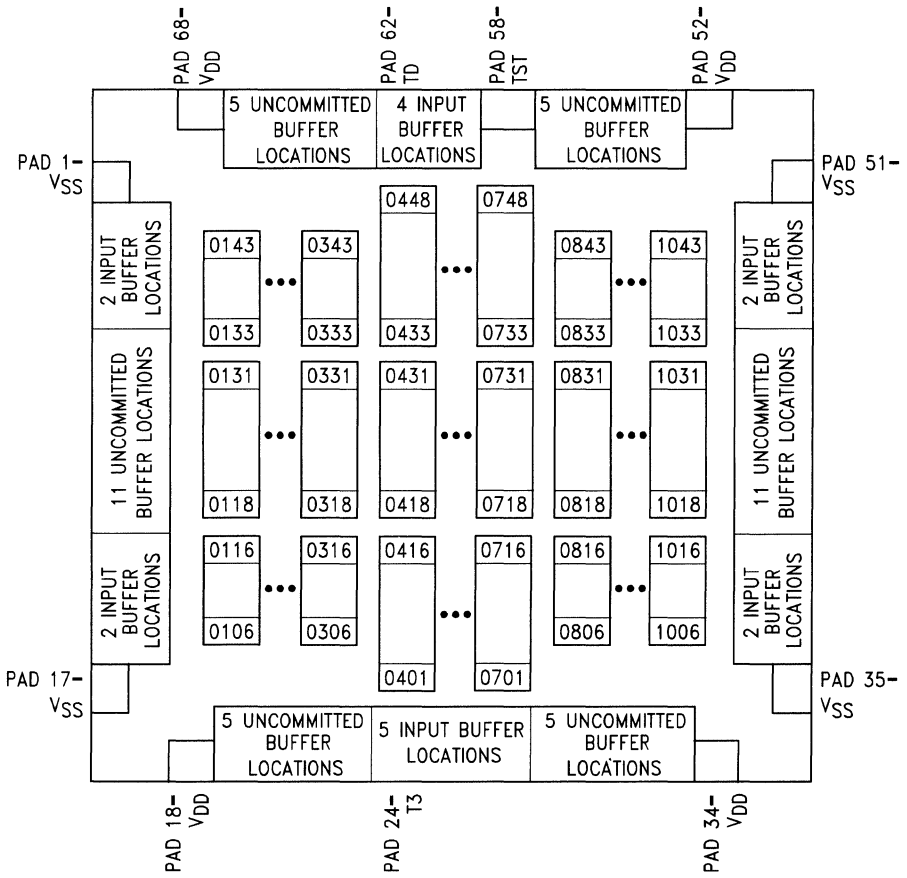
HCA6212
HCA6312

2- and 3-Micron 1200 Gate Macrocell Array

The HCA6212/6312 provides a total of 400 primary cells contained within 10 columns. There are a maximum of 17 input buffer locations and 42 uncommitted buffer locations. Also available are a maximum of 8 power and ground locations (4 V_{DD}, 4 V_{SS}). The electrical characteristics of the HCA6212/6312 are described in Section 8.

FLOORPLAN



VERTICAL ROUTING (First layer metal)

Routing Channel	1	2	3	4	5	6	7	8	9	10	11
Number of Tracks	12	13	14	15	16	17	16	15	14	13	12

Total Vertical Tracks = 157

HORIZONTAL ROUTING (Second layer metal)

10 Tracks per primary cell (48 cells) = 480 Tracks
4 Tracks top and bottom of columns = 8 Tracks
Total Horizontal Tracks = 488

10

PERIPHERY OPTIONS AND PLACEMENTS

Available Periphery Options	Input Location	Uncommitted Location	TD Location	T3 Location	TST Location
Bidirectional Buffers					
B02N		X			
B02U		X			
B02D		X			
B03N		X			
B03U		X			
B03D		X			
B04N		X			
B04U		X			
B04D		X			
B05N		X			
B05U		X			
B05D		X			
Output Buffers					
Y01N		X			
Y02N		X			
Input Buffers					
I01N	X	X	X	X	
I01U	X	X	X	X	
I01D	X	X	X	X	
I02N	X	X	X	X	X
I02U	X	X	X	X	X
I02D	X	X	X	X	X
I03N	X	X			
I03U	X	X			
I03D	X	X			
I05N	X	X			
I05U	X	X			
I05D	X	X			
I07N		X			
I07D		X			
I09N		X			

TD = Test Data Pin
T3 = Test 3-State Pin
TST = Test-Mode Pin

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PAD TO PIN CROSS REFERENCE GUIDE

IC Pad	Package							Pin Type
	28 Pin	40 Pin	44 Pin	48 Pin	52 Pin	68 Pin		
	DIP	DIP	LCC or PCC	DIP	LCC or PCC	LCC or PCC	PGA	
	Option 1	Option 1	Option 1	Option 1	Option 1	Option 0	Option 0	
1	—	—	—	—	—	10	H3	V_{SS}
2	—	—	7	—	8	11	K1	Input
3	—	—	—	—	—	12	J3	Input
4	5	7	8	9	9	13	K2	I/O
5	6	8	9	10	10	14	K3	I/O
6	—	9	10	11	11	15	J4	I/O
7	7	10	11	12	12	16	K4	I/O
8	—	—	—	—	13	17	J5	I/O
9	—	—	—	—	14	18	K5	I/O
10	—	—	12	—	15	19	K6	I/O
11	8	11	13	13	16	20	J6	I/O
12	—	12	14	14	17	21	K7	I/O
13	9	13	15	15	18	22	K8	I/O
14	10	14	16	16	19	23	J7	I/O
15	—	—	—	—	—	24	K9	Input
16	—	—	—	—	—	25	J8	Input
17	11	15	17	17	20	26	J9	V_{SS}
18	—	—	—	—	—	27	H8	V_{DD}
19	12	16	18	18	21	28	K10	I/O
20	—	17	19	19	22	29	H9	I/O
21	13	18	20	20	23	30	J10	I/O
22	—	19	21	21	24	31	H10	I/O
23	—	—	22	22	25	32	G9	I/O
24	14	20	23	23	26	33	G10	T3/Input
25	—	—	—	24	27	34	F9	Input
26	—	—	—	—	—	35	F10	Input
27	—	—	—	25	—	36	E10	Input
28	—	—	—	26	—	37	E9	Input
29	15	21	24	27	28	38	D10	I/O
30	—	22	—	28	29	39	C10	I/O
31	16	23	25	29	30	40	D9	I/O
32	—	24	26	30	31	41	B10	I/O
33	17	25	27	31	32	42	C9	I/O
34	18	26	28	32	33	43	B9	V_{DD}
35	—	—	—	—	—	44	C8	V_{SS}
36	—	—	29	—	34	45	A10	Input
37	—	—	—	—	—	46	B8	Input
38	19	27	30	33	35	47	A9	I/O
39	20	28	31	34	36	48	A8	I/O
40	—	29	32	35	37	49	B7	I/O
41	21	30	33	36	38	50	A7	I/O
42	—	—	34	—	39	51	B6	I/O
43	—	—	—	—	40	52	A6	I/O
44	—	—	—	—	41	53	A5	I/O
45	22	31	35	37	42	54	B5	I/O
46	—	32	36	38	43	55	A4	I/O
47	23	33	37	39	44	56	A3	I/O
48	24	34	38	40	45	57	B4	I/O
49	—	—	—	—	—	58	A2	Input
50	—	—	—	—	—	59	B3	Input
51	25	35	39	41	46	60	B2	V_{SS}
52	—	—	—	—	—	61	C3	V_{DD}
53	26	36	40	42	47	62	A1	I/O
54	—	37	41	43	48	63	C2	I/O
55	27	38	42	44	49	64	B1	I/O

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Package							Pin Type
	28 Pin	40 Pin	44 Pin	48 Pin	52 Pin	68 Pin		
	DIP	DIP	LCC or PCC	DIP	LCC or PCC	LCC or PCC	PGA	
	Option 1	Option 1	Option 1	Option 1	Option 1	Option 0	Option 0	
56	—	39	43	45	50	65	C1	I/O
57	—	—	44	46	51	66	D2	I/O
58	28	40	1	47	52	67	D1	TST
59	—	—	—	48	—	68	E2	Input
60	—	—	—	—	—	1	E1	Input
61	—	—	—	1	—	2	F1	Input
62	1	1	2	2	1	3	F2	TD/Input
63	—	—	—	3	2	4	G1	I/O
64	—	2	3	4	3	5	H1	I/O
65	2	3	4	5	4	6	G2	I/O
66	—	4	5	6	5	7	J1	I/O
67	3	5	—	7	6	8	H2	I/O
68	4	6	6	8	7	9	J2	V_{DD}

PACKAGING

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6212	028PDIP1 028HDIP1 028-LCC1 028-PCC1	2	21	2	2	1	0
	040PDIP1 040HDIP1	2	33	2	2	1	0
	044-LCC1 044-PCC1	4	35	2	2	1	0
	048HDIP1	7	36	2	2	1	0
	052-LCC1 052-PCC1	NOT YET DETERMINED					
	068-LCC0 068-PCC0 068-PGA0 068LPGA0	17	42	4	4	1	0

PACKAGING (Continued)

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6312	028PDIP1 028HDIP1	2	21	2	2	1	0
	040PDIP1 040HDIP1	2	33	2	2	1	0
	044-LCC1 044-PCC1	4	35	2	2	1	0
	048PDIP1 048HDIP1	7	36	2	2	1	0
	052-LCC0 052-PCC0	NOT YET DETERMINED					
	068-LCC0 068-PCC0 068-PGA0 068LPGA0	17	42	4	4	1	0

Package Abbreviations For This Publication:
PDIP: Plastic Dual In-Line Package
HDIP: Side-Brazed Ceramic Dual In-Line Carrier
LCC: Ceramic Leadless Chip-Carrier
PCC: Plastic Leaded Chip-Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid Array

TEST MODE FUNCTION TABLE

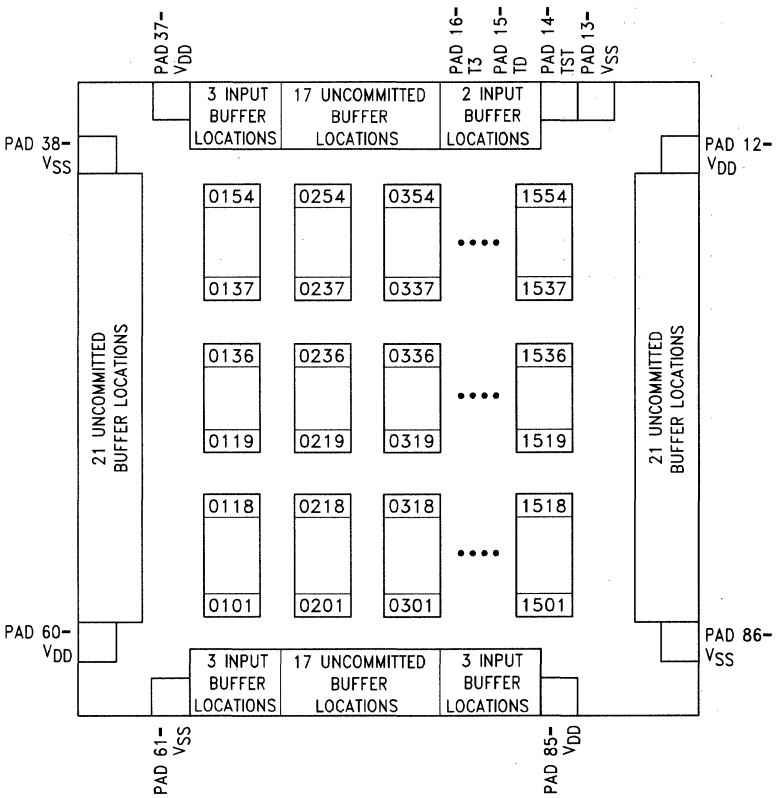
Input			Output Buffer Type	Output
Test Mode	Test Data	Test 3-State		
L	X	X	X	From Array
H H H	X H L	H L L	Any Bidirectional Option	Z L H
H H	H L	X X	Y01N Y01N	L H
H H	L H	X X	Y02N Y02N	Z L

X = Don't Care
Z = High Impedance

2-Micron 2500 Gate Macrocell Array

The HCA6225 provides a total of 810 primary cells contained within 15 columns. There are a maximum of 11 input buffer locations and 76 uncommitted buffer locations. Also available are a maximum of 8 power and ground locations (4 V_{DD}, 4 V_{SS}). The electrical characteristics of the HCA6225 are described in Section 8.

FLOORPLAN



VERTICAL ROUTING (First layer metal)

Routing Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Number of Tracks	16	16	16	17	19	20	21	22	22	21	20	19	17	16	16	16

Total Vertical Tracks = 294

HORIZONTAL ROUTING (Second layer metal)

10 Tracks per primary cell (54 cells) = 540 Tracks
14 Tracks bottom of columns = 14 Tracks
14 Tracks top of columns = 14 Tracks
Total Horizontal Tracks = 568

PERIPHERY OPTIONS AND PLACEMENT

Available Periphery Options	Input Location	Uncommitted Location	TD Location	T3 Location	TST Location
Bidirectional Buffers					
B02N		X			
B02U		X			
B02D		X			
B03N		X			
B03U		X			
B03D		X			
B04N		X			
B04U		X			
B04D		X			
B05N		X			
B05U		X			
B05D		X			
Output Buffers					
Y01N		X			
Y02N		X			
Input Buffers					
I01N	X	X	X	X	X
I01U	X	X	X	X	X
I01D	X	X	X	X	X
I02N	X	X	X	X	X
I02U	X	X	X	X	X
I02D	X	X	X	X	X
I03N	X	X			X
I03U	X	X			X
I03D	X	X			X
I05N	X	X			
I05U	X	X			
I05D	X	X			
I07N		X			
I07D		X			
I09N		X			

TD = Test Data Pin
T3 = Test 3-State Pin
TST = Test-Mode Pin

PAD TO PIN CROSS REFERENCE GUIDE

IC Pad	Packages									Pin Type
	40 Pin	44 Pin	52 Pin	68 Pin		84 Pin		124 Pin		
	DIP	LCC or PCC	LCC or PCC	LCC or PCC	PGA	LCC	PGA	LCC or PCC	PGA	
	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	
1	1	1	1	1	E1	1	F1	1	G3	I/O
2	—	—	—	2	F1	2	F2	2	G1	I/O
3	—	—	2	3	F2	3	F3	3	H1	I/O
4	—	2	—	—	—	4	G1	4	H2	I/O
5	2	—	3	4	G1	5	H1	5	H3	I/O
6	—	3	—	—	—	6	G2	6	J1	I/O
7	3	—	—	5	H1	7	J1	7	K1	I/O
8	—	4	4	6	G2	8	G3	8	J2	I/O
9	4	—	5	7	J1	9	K1	9	J3	I/O
10	—	5	6	8	H2	10	H2	10	L1	I/O
11	5	6	7	9	J2	11	J2	12	K2	I/O
12	—	—	—	—	—	—	—	13	K3	V_{DD}
13	6	7	8	10	H3	12	H3	19	M3	V_{SS}
14	7	8	9	11	K1	13	J3	20	L4	TST
15	8	9	10	12	J3	14	K2	21	M4	TD/Input
16	9	10	11	13	K2	15	K3	23	N3	T3/Input
17	—	—	—	—	—	16	H4	24	L5	I/O
18	—	—	—	—	—	17	J4	25	M5	I/O
19	—	—	—	—	—	—	—	26	N4	I/O
20	—	—	—	14	K3	18	K4	27	N5	I/O
21	—	—	12	15	J4	19	J5	28	L6	I/O
22	—	—	—	16	K4	—	—	29	M6	I/O
23	10	11	13	—	—	20	H5	30	N6	I/O
24	—	—	—	17	J5	21	K5	31	M7	I/O
25	—	12	14	18	K5	22	K6	32	L7	I/O
26	—	—	—	19	K6	23	J6	33	N7	I/O
27	11	13	15	—	—	24	H6	34	N8	I/O
28	—	—	—	20	J6	25	K7	35	M8	I/O
29	12	14	16	21	K7	26	K8	36	L8	I/O
30	—	—	—	22	K8	27	J7	37	N9	I/O
31	13	15	17	23	J7	28	K9	38	N10	I/O
32	—	—	18	24	K9	29	H7	39	M9	I/O
33	14	16	19	25	J8	30	K10	40	L9	I/O
34	—	—	—	—	—	—	—	41	N11	Input
35	—	—	—	—	—	—	—	43	M10	Input
36	—	—	—	—	—	31	J8	44	L10	Input
37	15	17	20	26	J9	32	J9	45	M11	V_{DD}
38	—	—	—	—	—	—	—	51	K11	V_{SS}
39	16	18	21	27	H8	33	H8	52	K12	I/O
40	—	19	22	28	K10	34	H9	54	L13	I/O
41	17	—	23	29	H9	35	J10	55	J11	I/O
42	—	20	24	30	J10	36	H10	56	J12	I/O
43	18	—	—	31	H10	37	G8	57	K13	I/O
44	—	21	25	—	—	38	G9	58	J13	I/O
45	19	—	—	32	G9	39	G10	59	H11	I/O
46	—	22	26	—	—	40	F9	60	H12	I/O
47	20	—	—	33	G10	41	F8	61	H13	I/O
48	—	—	—	34	F9	42	F10	62	G12	I/O
49	—	23	27	35	F10	43	E10	63	G11	I/O
50	—	—	—	36	E10	44	E9	64	G13	I/O
51	21	—	28	37	E9	45	E8	65	F13	I/O
52	—	24	—	—	—	46	D10	66	F12	I/O
53	22	—	29	38	D10	47	C10	67	F11	I/O
54	—	25	—	—	—	48	D9	68	E13	I/O
55	23	—	—	39	C10	49	B10	69	D13	I/O

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Packages									Pin Type
	40 Pin	44 Pin	52 Pin	68 Pin		84 Pin		124 Pin		
	DIP	LCC or PCC	LCC or PCC	LCC or PCC	PGA	LCC	PGA	LCC or PCC	PGA	
	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	
56	—	26	30	40	D9	50	D8	70	E12	I/O
57	24	—	31	41	B10	51	A10	71	E11	I/O
58	—	27	32	42	C9	52	C9	72	C13	I/O
59	25	28	33	43	B9	53	B9	74	D12	I/O
60	—	—	—	—	—	—	—	75	D11	V_{DD}
61	26	29	34	44	C8	54	C8	81	B11	V_{SS}
62	—	—	—	—	—	55	B8	82	C10	Input
63	—	—	—	—	—	—	—	83	B10	Input
64	—	—	—	—	—	—	—	85	A11	Input
65	27	30	35	45	A10	54	A9	86	C9	I/O
66	—	—	36	46	B8	55	A8	87	B9	I/O
67	28	31	37	47	A9	58	C7	88	A10	I/O
68	—	—	—	48	A8	59	B7	89	A9	I/O
69	29	32	38	49	B7	60	A7	90	C8	I/O
70	—	—	—	50	A7	61	B6	91	B8	I/O
71	30	33	39	—	—	62	C6	92	A8	I/O
72	—	—	—	51	B6	63	A6	93	B7	I/O
73	—	34	40	52	A6	64	A4	94	C7	I/O
74	—	—	—	53	A5	65	B5	95	A7	I/O
75	31	35	41	—	—	66	C5	96	A6	I/O
76	—	—	—	54	B5	67	A4	97	B6	I/O
77	32	36	42	55	A4	68	A3	98	C6	I/O
78	—	—	—	56	A3	69	B4	99	A5	I/O
79	33	37	43	57	B4	70	A2	100	A4	I/O
80	—	—	44	58	A2	71	C4	101	B5	I/O
81	34	38	45	59	B3	72	A1	102	C5	I/O
82	—	—	—	—	—	—	—	103	A3	Input
83	—	—	—	—	—	—	—	105	B4	Input
84	—	—	—	—	—	73	B3	106	C4	Input
85	35	39	46	60	B2	74	B2	107	B3	V_{DD}
86	—	—	—	—	—	—	—	113	D3	V_{SS}
87	36	40	47	61	C3	75	C3	114	D2	I/O
88	—	41	48	62	A1	76	C2	116	C1	I/O
89	37	—	49	63	C2	77	B1	117	E3	I/O
90	—	42	50	64	B1	78	C1	118	E2	I/O
91	38	—	—	65	C1	79	D3	119	D1	I/O
92	—	43	—	—	—	80	D2	120	E1	I/O
93	39	—	51	66	D2	81	D1	121	F3	I/O
94	—	44	—	—	—	82	E2	122	F2	I/O
95	40	—	52	67	D1	83	E3	123	F1	I/O
96	—	—	—	68	E2	84	E1	124	G2	I/O

PACKAGING

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6225	040PDIP1 040HDIP1	2	33	2	2	1	0
	044-LCC1 044-PCC1	2	37	2	2	1	0
	052-LCC1 052-PCC1	2	45	2	2	1	0
	068-LCC1 068-PCC1 068-PGA1	2	61	2	2	1	0
	084-LCC1 084-PCC1 084-PGA1	5	74	2	2	1	0
	124-LCC1 124-PCC1 124-PGA1 124LPGA1	11	76	4	4	1	28

Package Abbreviations for this Publication:
PDIP: Plastic Dual In-Line Package
HDIP: Side-Brazed Ceramic Dual In-Line Carrier
LCC: Ceramic Leadless Chip Carrier
PCC: Plastic Leaded Chip Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid Array

TEST MODE FUNCTION TABLE

Input			Output Buffer Type	Output
Test Mode	Test Data	Test 3-State		
L	X	X	X	From Array
H H H	X H L	H L L	Any Bidirectional Option	Z L H
H H	H L	X X	Y01N Y01N	L H
H H	L H	X X	Y02N Y02N	Z L

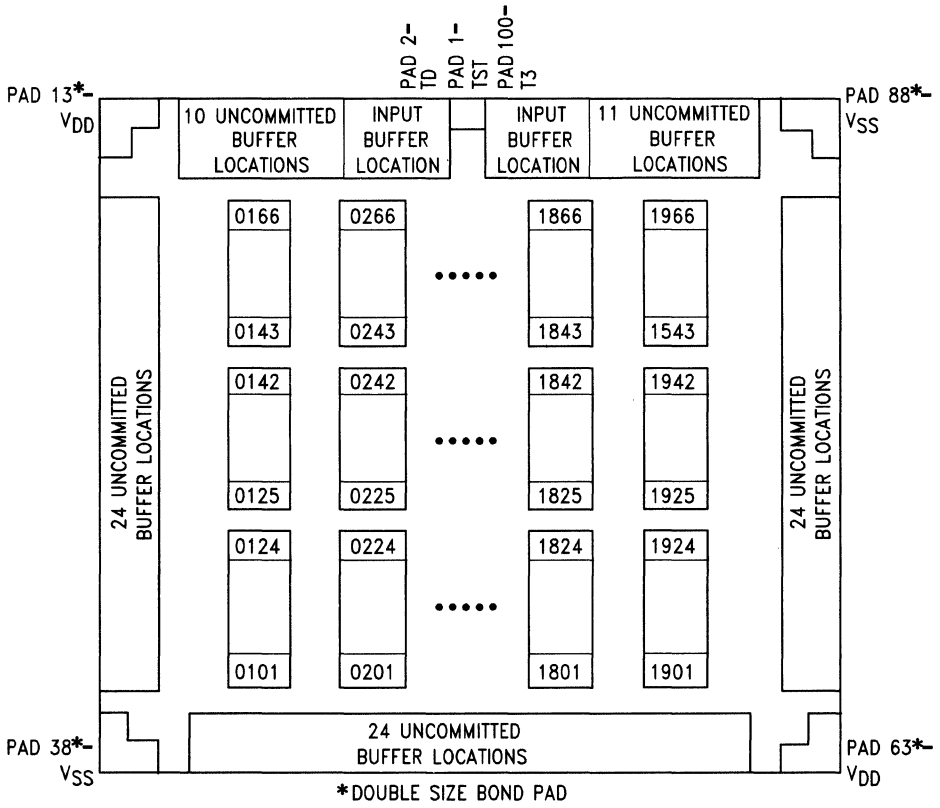
X = Don't Care
Z = High Impedance

HCA6238

2-Micron 3800 Gate Macrocell Array

The HCA6238 provides a total of 1254 primary cells contained within 19 columns. There are a maximum of 2 input buffer locations and 93 uncommitted buffer locations. Also available are a maximum of 8 power and ground locations (4 V_{DD}, 4 V_{SS}). The electrical characteristics of the HCA6238 are described in Section 8.

FLOORPLAN



*DOUBLE SIZE BOND PAD

VERTICAL ROUTING (First layer metal)

Routing Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Number of Tracks	15	16	18	19	20	20	20	20	20	20	20	20	20	20	20	20	19	18	16	15

Total Vertical Tracks = 376

HORIZONTAL ROUTING (Second layer metal)

10 Tracks per primary cell (66 cells)	= 660 Tracks
13 Tracks bottom of columns	= 13 Tracks
13 Tracks top of columns	= 13 Tracks
Total Horizontal Tracks	= 686

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PERIPHERY OPTIONS AND PLACEMENT

Available Periphery Options	Input Location	Uncommitted Location	TD Location	T3 Location
Bidirectional Buffers				
B02N		X		
B02U		X		
B02D		X		
B03N		X		
B03U		X		
B03D		X		
B04N		X		
B04U		X		
B04D		X		
B05N		X		
B05U		X		
B05D		X		
Output Buffers				
Y01N		X		
Y02N		X		
Input Buffers				
I01N	X	X	X	X
I01U	X	X	X	X
I01D	X	X	X	X
I02N	X	X	X	X
I02U	X	X	X	X
I02D	X	X	X	X
I03N	X	X	X	X
I03U	X	X	X	X
I03D	X	X	X	X
I05N	X	X	X	X
I05U	X	X	X	X
I05D	X	X	X	X
I06N	X	X	X	X
I06U	X	X	X	X
I06D	X	X	X	X
I07N	X	X	X	X
I07U	X	X	X	X
I07D	X	X	X	X
I08N	X	X	X	X
I08U	X	X	X	X
I08D	X	X	X	X
I09N		X		

TD = Test Data Pin
T3 = Test 3-State Pin

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PAD TO PIN CROSS REFERENCE GUIDE

IC Pad	Package						Pin Type
	68 Pin		84 Pin		124 Pin		
	LCC or PCC	PGA	LCC or PCC	PGA	LCC	PGA	
	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	
1	1	E1	1	F1	1	G3	TST
2	2	F1	2	F2	2	G1	TD/INP
3	—	—	3	F3	3	H1	I/O
4	3	F2	4	G1	4	H2	I/O
5	—	—	—	—	5	H3	I/O
6	4	G1	5	H1	6	J1	I/O
7	—	—	6	G2	7	K1	I/O
8	5	H1	7	J1	8	J2	I/O
9	6	G2	8	G3	9	J3	I/O
10	7	J1	9	K1	10	L1	I/O
11	8	H2	10	H2	12	K2	I/O
12	9	J2	11	J2	13	K3	I/O
13	10	H3	12	H3	17, 18	L3, M2	V_{DD}
14	11	K1	13	J3	19	M3	I/O
15	12	J3	14	K2	20	L4	I/O
16	13	K2	15	K3	21	M4	I/O
17	—	—	16	H4	24	L5	I/O
18	14	K3	17	J4	25	M5	I/O
19	—	—	18	K4	26	N4	I/O
20	15	J4	19	J5	27	N5	I/O
21	—	—	—	—	28	L6	I/O
22	16	K4	—	—	29	M6	I/O
23	17	J5	20	H5	30	N6	I/O
24	—	—	21	K5	31	M71	I/O
25	—	—	22	K6	32	L7	I/O
26	18	K5	—	—	33	N7	I/O
27	19	K6	23	J6	34	N8	I/O
28	—	—	—	—	35	M8	I/O
29	20	J6	24	H6	36	L8	I/O
30	—	—	25	K7	37	N9	I/O
31	21	K7	26	K8	38	N10	I/O
32	—	—	—	—	39	M9	I/O
33	22	K8	27	J7	40	L9	I/O
34	23	J7	28	K9	41	N11	I/O
35	—	—	29	H7	43	M10	I/O
36	24	K9	30	K10	44	L10	I/O
37	25	J8	31	J8	45	M11	I/O
38	26	J9	32	J9	48, 49	K10, N13	V_{SS}
39	27	H8	33	H8	51	K11	I/O
40	28	K10	34	H9	52	K12	I/O
41	29	H9	35	J10	54	L13	I/O
42	30	J10	36	H10	55	J11	I/O
43	31	H10	37	G8	56	J12	I/O
44	—	—	38	G9	57	K13	I/O
45	32	G9	39	G10	58	J13	I/O
46	—	—	40	F9	59	H11	I/O
47	33	G10	41	F8	60	H12	I/O
48	—	—	—	—	61	H13	I/O
49	34	F9	42	F10	62	G12	I/O
50	35	F10	43	E10	63	G11	I/O
51	—	—	—	—	64	G13	I/O
52	36	E10	44	E9	65	F13	I/O
53	—	—	45	E8	66	F12	I/O
54	37	E9	—	—	67	F11	I/O
55	—	—	46	D10	68	E13	I/O

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Package						Pin Type
	68 Pin		84 Pin		124 Pin		
	LCC or PCC	PGA	LCC or PCC	PGA	LCC	PGA	
	Option 1	Option 1	Option 1	Option 1	Option 1	Option 1	
56	38	D10	47	C10	69	D13	I/O
57	—	—	48	D9	70	E12	I/O
58	39	C10	49	B10	71	E11	I/O
59	40	D9	50	D8	72	C13	I/O
60	41	B10	51	A10	74	D12	I/O
61	42	C9	52	C9	75	D11	I/O
62	43	B9	53	B9	76	C12	I/O
63	44	C8	54	C8	79, 80	C11, B12	V_{DD}
64	45	A10	55	B8	82	C10	I/O
65	46	B8	56	A9	83	B10	I/O
66	47	A9	57	A8	85	A11	I/O
67	48	A8	58	C7	86	C9	I/O
68	49	B7	59	B7	87	B9	I/O
69	—	—	60	A7	88	A10	I/O
70	—	—	61	B6	89	A9	I/O
71	50	A7	—	—	90	C8	I/O
72	—	—	62	C6	91	B8	I/O
73	51	B6	63	A6	92	A8	I/O
74	—	—	—	—	93	B7	I/O
75	52	A6	64	A5	94	C7	I/O
76	—	—	—	—	95	A7	I/O
77	53	A5	65	B5	96	A6	I/O
78	—	—	66	C5	97	B6	I/O
79	54	B5	67	A4	98	C6	I/O
80	—	—	—	—	99	A5	I/O
81	55	A4	—	—	100	A4	I/O
82	—	—	68	A3	101	B5	I/O
83	56	A3	69	B4	102	C5	I/O
84	57	B4	70	A2	103	A3	I/O
85	—	—	71	C4	105	B4	I/O
86	58	A2	72	A1	106	C4	I/O
87	59	B3	73	B3	107	B3	I/O
88	60	B2	74	B2	110, 111	D4, A1	V_{SS}
89	61	C3	75	C3	112	C2	I/O
90	62	A1	76	C2	113	D3	I/O
91	63	C2	77	B1	114	D2	I/O
92	64	B1	78	C1	116	C1	I/O
93	65	C1	79	D3	117	E3	I/O
94	—	—	80	D2	118	E2	I/O
95	66	D2	81	D1	119	D1	I/O
96	—	—	82	E2	120	E1	I/O
97	67	D1	83	E3	121	F3	I/O
98	—	—	—	—	122	F2	I/O
99	—	—	—	—	123	F1	I/O
100	68	E2	84	E1	124	G2	T3/INP

PACKAGING

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6238	068-LCC1 068-PCC1 068-PGA1 068LPGA1	2	61	2	2	1	0
	084-LCC1 084-PCC1 084-PGA1 084LPGA1	2	77	2	2	1	0
	124-LCC1 124-PGA1 124LPGA1	2	93	4	4	1	20

Package Abbreviations for this Publication:
LCC: Ceramic Leadless Chip Carrier
PCC: Plastic Leaded Chip Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid Array

TEST MODE FUNCTION TABLE

Input			Output Buffer Type	Output
Test Mode	Test Data	Test 3-State		
L	X	X	X	From Array
H	X	H	Any	Z
H	L	L	Bidirectional	H
H	H	L	Buffer	L
H	L	X	Y01N	H
H	H	X	Y01N	L
H	L	X	Y02N	Z
H	H	X	Y02N	L

X = Don't Care
Z = High Impedance

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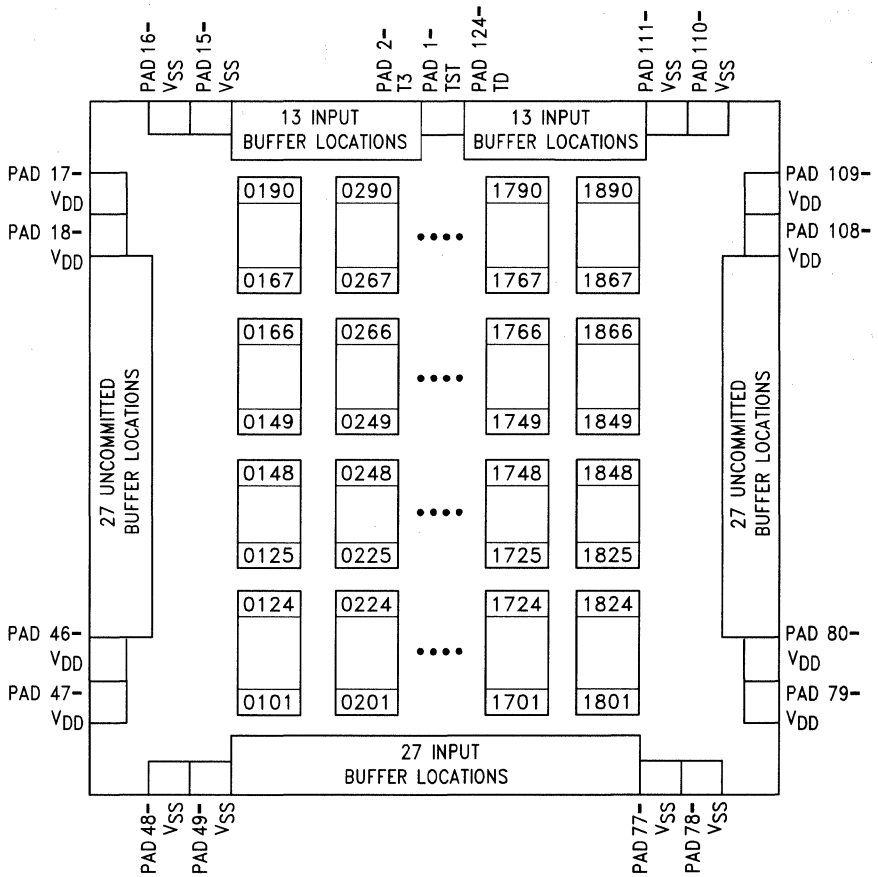
HCA6248
HCA6348

2- and 3-Micron 4800 Gate Macrocell Array

The HCA6248/6348 provides a total of 1620 primary cells contained within 18 columns. There are a maximum of 53 input buffer locations and 54 uncommitted buffer locations. Also available are a maximum of 16 power and ground locations (8 V_{DD}, 8 V_{SS}). The electrical characteristics of the HCA6248/6348 are described in Section 8.

FLOORPLAN



VERTICAL ROUTING (First layer metal)

Routing Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Number of Tracks	20	29	29	31	32	32	32	32	32	32	32	32	32	32	32	31	29	29	20

Total Vertical Tracks = 570

HORIZONTAL ROUTING (Second layer metal)

10 Tracks per primary cell (90 cells) = 900 Tracks
7 Tracks top and bottom of columns = 14 Tracks
Total Horizontal Tracks = 914

PERIPHERY OPTIONS AND PLACEMENT

Available Periphery Options	Input Location	Uncommitted Location	TD Location	T3 Location
Bidirectional Buffers				
B02N		X		
B03N		X		
B04N		X		
Output Buffers				
Y01N		X		
Y02N		X		
Input Buffers				
I01N	X	X	X	X
I01U	X	X	X	X
I01D	X	X	X	X
I02N	X	X	X	X
I02U	X	X	X	X
I02D	X	X	X	X
I03N	X	X	X	X
I03U	X	X	X	X
I03D	X	X	X	X
I08N		X		
I08U		X		
I08D		X		
I09N		X		

TD = Test Data Pin
T3 = Test 3-State Pin

PAD TO PIN CROSS REFERENCE GUIDE

IC Pad	Package							Pin Type
	68 Pin		84 Pin		124 Pin			
	LCC or PCC	PGA	LCC or PCC	PGA	LCC or PCC	PGA		
	Option 0	Option 0	Option 0	Option 0	Option 0	Option 0	Option 1	
1	1	E1	1	F1	1	G2	G3	TST
2	2	F1	2	F2	2	G3	G1	T3/Input
3	—	—	3	F3	3	H1	H1	Input
4	—	—	—	—	4	H2	H2	Input
5	3	F2	—	—	5	H3	H3	Input
6	—	—	—	—	6	J1	J1	Input
7	4	G1	—	—	7	J2	K1	Input
8	—	—	—	—	8	K1	J2	Input
9	5	H1	4	G1	9	K2	J3	Input
10	—	—	5	H1	10	L1	L1	Input
11	6	G2	6	G2	11	M1	M1	Input
12	—	—	7	J1	12	L2	K2	Input
13	7	J1	8	G3	13	N1	K3	Input
14	8	H2	9	K1	14	M2	L2	Input
15	9	J2	10	H2	15	J3	N1	V_{SS}
16	9	J2	11	J2	16	K3	K4	V_{SS}
17	10	H3	12	H3	17	K4	L3	V_{DD}
18	10	H3	13	J3	18	L4	M2	V_{DD}
19	11	K1	—	—	19	L3	M3	I/O
20	12	J3	14	K2	20	M3	L4	I/O
21	—	—	15	K3	21	N2	M4	I/O
22	13	K2	16	H4	22	N3	N2	I/O
23	—	—	17	J4	23	M4	N3	I/O
24	14	K3	18	K4	24	N4	L5	I/O
25	—	—	—	—	25	M5	M5	I/O
26	15	J4	—	—	26	N5	N4	I/O
27	—	—	—	—	27	L5	N5	I/O
28	16	K4	—	—	28	M6	L6	I/O
29	—	—	19	J5	29	N6	M6	I/O
30	17	J5	20	H5	30	L6	N6	I/O
31	—	—	21	K5	31	N7	M7	I/O
32	18	K5	22	K6	32	M7	L7	I/O
33	—	—	23	J6	33	L7	N7	I/O
34	19	K6	24	H6	34	N8	N8	I/O
35	—	—	—	—	35	M8	M8	I/O
36	20	J6	—	—	36	L8	L8	I/O
37	—	—	—	—	37	N9	N9	I/O
38	21	K7	25	K7	38	M9	N10	I/O
39	—	—	26	K8	39	N10	M9	I/O
40	22	K8	27	J7	40	M10	L9	I/O
41	—	—	28	K9	41	N11	N11	I/O
42	23	J7	29	H7	42	N12	N12	I/O
43	—	—	30	K10	43	M11	M10	I/O
44	24	K9	31	J8	44	M12	L10	I/O
45	25	J8	32	J9	45	L10	M11	I/O
46	26	J9	—	—	46	L9	M12	V_{DD}
47	26	J9	—	—	47	K10	L11	V_{DD}
48	27	H8	33	H8	48	L11	K10	V_{SS}
49	27	H8	—	—	49	K11	N13	V_{SS}
50	28	K10	34	H9	50	N13	L12	Input
51	29	H9	35	J10	51	L12	K11	Input
52	—	—	36	H10	52	M13	K12	Input
53	30	J10	37	G8	53	L13	M13	Input
54	—	—	38	G9	54	K12	L13	Input
55	31	H10	39	G10	55	K13	J11	Input

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Package							Pin Type
	68 Pin		84 Pin		124 Pin			
	LCC or PCC	PGA	LCC or PCC	PGA	LCC or PCC	PGA		
	Option 0	Option 0	Option 0	Option 0	Option 0	Option 0	Option 1	
56	—	—	40	F9	56	J12	J12	Input
57	32	G9	—	—	57	J13	K13	Input
58	—	—	—	—	58	J11	J13	Input
59	33	G10	—	—	59	H12	H11	Input
60	—	—	—	—	60	H13	H12	Input
61	—	—	—	—	61	H11	H13	Input
62	34	F9	41	F8	62	G13	G12	Input
63	35	F10	42	F10	63	G12	G11	Input
64	36	E10	43	E10	64	G11	G13	Input
65	—	—	44	E9	65	F13	F13	Input
66	—	—	45	E8	66	F12	F12	Input
67	37	E9	46	D10	67	F11	F11	Input
68	—	—	—	—	68	E13	E13	Input
69	38	D10	—	—	69	E12	D13	Input
70	—	—	—	—	70	D13	E12	Input
71	39	C10	—	—	71	D12	E11	Input
72	—	—	47	C10	72	C13	C13	Input
73	40	D9	48	D9	73	B13	B13	Input
74	—	—	49	B10	74	C12	D12	Input
75	41	B10	50	D8	75	A13	D11	Input
76	42	C9	51	A10	76	B12	C12	Input
77	43	B9	52	C9	77	E11	A13	V_{SS}
78	43	B9	53	B9	78	D11	D10	V_{SS}
79	44	C8	54	C8	79	D10	C11	V_{DD}
80	44	C8	—	—	80	C10	B12	V_{DD}
81	45	A10	55	B8	81	C11	B11	I/O
82	46	B8	56	A9	82	B11	C10	I/O
83	—	—	57	A8	83	A12	B10	I/O
84	47	A9	58	C7	84	A11	A12	I/O
85	—	—	59	B7	85	B10	A11	I/O
86	48	A8	60	A7	86	A10	C9	I/O
87	—	—	61	B6	87	B9	B9	I/O
88	49	B7	—	—	88	A9	A10	I/O
89	—	—	—	—	89	C9	A9	I/O
90	50	A7	—	—	90	B8	C8	I/O
91	—	—	62	C6	91	A8	B8	I/O
92	51	B6	63	A6	92	C8	A8	I/O
93	—	—	64	A5	93	A7	B7	I/O
94	52	A6	65	B5	94	B7	C7	I/O
95	—	—	66	C5	95	C7	A7	I/O
96	53	A5	67	A4	96	A6	A6	I/O
97	—	—	—	—	97	B6	B6	I/O
98	54	B5	—	—	98	C6	C6	I/O
99	—	—	—	—	99	A5	A5	I/O
100	55	A4	—	—	100	B5	A4	I/O
101	—	—	—	—	101	A4	B5	I/O
102	56	A3	68	A3	102	B4	C5	I/O
103	—	—	69	B4	103	A3	A3	I/O
104	57	B4	70	A2	104	A2	A2	I/O
105	—	—	71	C4	105	B3	B4	I/O
106	58	A2	72	A1	106	B2	C4	I/O
107	59	B3	73	B3	107	C4	B3	I/O
108	60	B2	74	B2	108	C5	B2	V_{DD}
109	60	B2	—	—	109	D4	C3	V_{DD}
110	61	C3	75	C3	110	C3	D4	V_{SS}

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Package							Pin Type
	68 Pin		84 Pin		124 Pin			
	LCC or PCC	PGA	LCC or PCC	PGA	LCC or PCC	PGA		
	Option 0	Option 0	Option 0	Option 0	Option 0	Option 0	Option 1	
111	61	C3	—	—	111	D3	A1	V_{SS}
112	62	A1	76	C2	112	A1	C2	Input
113	63	C2	77	B1	113	C2	D3	Input
114	—	—	78	C1	114	B1	D2	Input
115	64	B1	79	D3	115	C1	B1	Input
116	—	—	80	D2	116	D2	C1	Input
117	65	C1	81	D1	117	D1	E3	Input
118	—	—	—	—	118	E2	E2	Input
119	66	D2	—	—	119	E1	D1	Input
120	—	—	—	—	120	E3	E1	Input
121	67	D1	—	—	121	F2	F3	Input
122	—	—	82	E2	122	F1	F2	Input
123	—	—	83	E3	123	F3	F1	Input
124	68	E2	84	E1	124	G1	G2	TD / Input

PACKAGING

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6248	068-LCC0 068-PCC0 068-PGA0 068LPGA0	29	30	4	4	1	0
	084-LCC0 084-PCC0 084-PGA0 084LPGA0	35	38	4	6	1	0
	124-LCC0 124-PCC0 124-PGA0 124-PGA1 124LPGA1	53	54	8	8	1	0
HCA6348	084-LCC0 084-PCC0 084-PGA0 084LPGA0	35	38	4	6	1	0
	124-LCC0 124-PCC0 124-PGA0	53	54	8	8	1	0

Package Abbreviations for this Publication:
LCC: Ceramic Leadless Chip Carrier
PCC: Plastic Leaded Chip Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid Array

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TEST MODE FUNCTION TABLE

Input Buffer Type		Input			Output Buffer Type	Output
Test Data	Test 3-State	Test Mode	Test Data	Test 3-State		
X	X	L	X	X	X	From Array
IO1X or IO3X	IO1X or IO3X	H H H	X L H	H L L	Any Bidirectional Option	Z H L
		H H	L H	X X	Y01N	H L
		H H	L H	X X	Y02N	Z L
IO1X or IO3X	IO2X	H H H	X L H	L H H	Any Bidirectional Option	Z H L
		H H	L H	X X	Y01N	H L
		H H	L H	X X	Y02N	Z L
IO2X	IO1X or IO3X	H H H	X L H	H L L	Any Bidirectional Option	Z L H
		H H	L H	X X	Y01N	L H
		H H	L H	X X	Y02N	L Z
IO2X	IO2X	H H H	X L H	L H H	Any Bidirectional Option	Z L H
		H H	L H	X X	Y01N	L H
		H H	L H	X X	Y02N	L Z

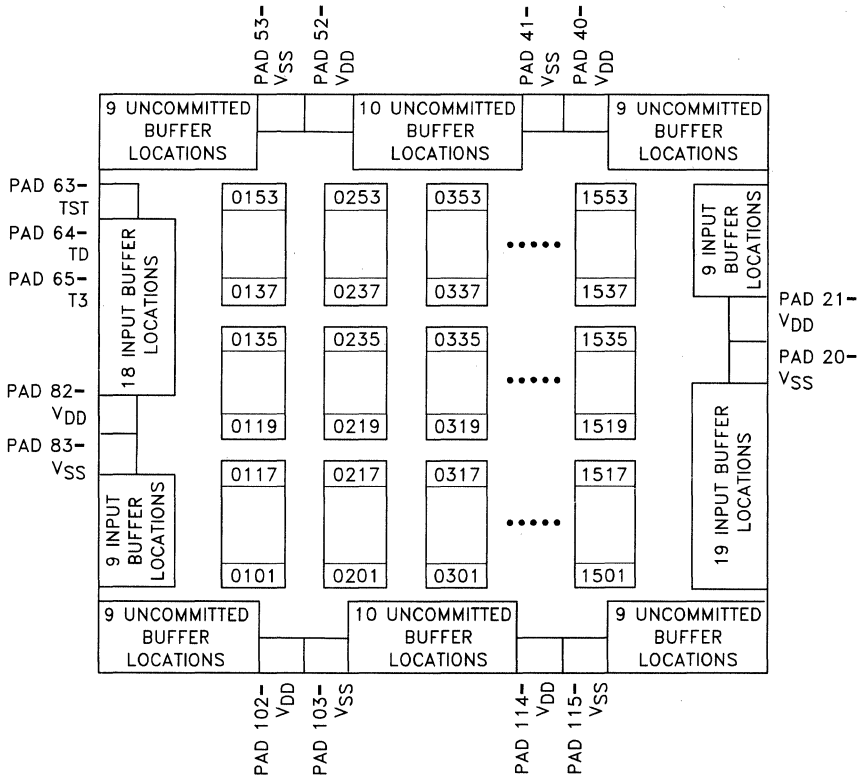
X = Don't Care
Z = High Impedance

HCA6324

3-Micron 2400 Gate Macrocell Array

The HCA6324 provides a total of 765 primary cells contained within 15 columns. There are a maximum of 55 input buffer locations and 56 uncommitted buffer locations. Also available are a maximum of 12 power and ground locations (6 V_{DD}, 6 V_{SS}). The electrical characteristics of the HCA6324 are described in Section 8.

FLOORPLAN



VERTICAL ROUTING (First layer metal)

Routing Channel	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Number of Tracks	15	16	16	17	18	19	20	21	21	20	19	18	17	16	16	15

Total Vertical Tracks = 284

HORIZONTAL ROUTING (Second layer metal)

10 Tracks per primary cell (53 cells)	= 530 Tracks
14 Tracks bottom of columns	= 14 Tracks
9 Tracks top of columns	= 9 Tracks
Total Horizontal Tracks	= 553

PERIPHERY OPTIONS AND PLACEMENT

Available Periphery Options	Input Location	Uncommitted Location	TD Location	T3 Location
Bidirectional Buffers				
B02N		X		
B02U		X		
B03N		X		
B03U		X		
Output Buffer				
Y01N		X		
Input Buffers				
I01N	X	X	X	X
I01U	X	X	X	X
I02N	X	X	X	X
I02U	X	X	X	X

TD = Test Data Pin
T3 = Test 3-State Pin

PAD TO PIN CROSS REFERENCE GUIDE

IC Pad	Packages									Pin Type
	40 Pin	44 Pin	48 Pin	68 Pin		84 Pin		124 Pin		
	DIP	LCC or PCC	DIP	LCC or PCC	PGA	LCC or PCC	PGA	LCC	PGA	
	Option 1	Option 0	Option 1	Option 1	Option 1	Option 0	Option 0	Option 0	Option 1	
1	27	30	32	45	A10	55	B8	17	L3	Input
2	—	—	—	46	B8	56	A9	18	M2	Input
3	—	—	—	—	—	57	A8	19	M3	Input
4	28	—	33	—	—	—	—	20	L4	Input
5	—	—	—	—	—	—	—	21	M4	Input
6	—	—	—	—	—	58	C7	22	N2	Input
7	—	—	34	—	—	59	B7	23	N3	Input
8	29	31	—	47	A9	—	—	24	L5	Input
9	—	—	—	48	A8	60	A7	25	M5	Input
10	—	—	—	—	—	—	—	26	N4	Input
11	30	32	35	49	B7	61	B6	27	N5	Input
12	—	—	—	—	—	—	—	28	L6	Input
13	—	33	—	50	A7	62	C6	29	M6	Input
14	—	—	36	51	B6	63	A6	30	N6	Input
15	—	—	—	—	—	64	A5	31	M7	Input
16	—	34	—	—	—	—	—	32	L7	Input
17	—	—	—	52	A6	65	B5	33	N7	Input
18	—	—	—	53	A5	66	C5	34	N8	Input

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Packages									Pin Type
	40 Pin	44 Pin	48 Pin	68 Pin		84 Pin		124 Pin		
	DIP	LCC or PCC	DIP	LCC or PCC	PGA	LCC or PCC	PGA	LCC	PGA	
	Option 1	Option 0	Option 1	Option 1	Option 1	Option 0	Option 0	Option 0	Option 1	
19	—	—	—	—	—	—	—	35	M8	Input
20	31	35	37	54	B5	67	A4	36	L8	V_{SS}
21	32	36	38	55	A4	68	A3	37	N9	V_{DD}
22	—	—	—	—	—	—	—	38	N10	Input
23	—	—	—	56	A3	69	B4	39	M9	Input
24	—	—	—	—	—	—	—	40	L9	Input
25	33	37	39	57	B4	70	A2	41	N11	Input
26	—	—	—	—	—	—	—	42	N12	Input
27	—	—	—	—	—	—	—	43	M10	Input
28	—	—	—	58	A2	71	C4	44	L10	Input
29	—	—	40	—	—	72	A1	45	M11	Input
30	34	38	41	59	B3	73	B3	46	M12	Input
31	35	39	42	60	B2	74	B2	47	L11	I/O
32	—	—	43	—	—	—	—	48	K10	I/O
33	36	40	44	61	C3	75	C3	49	N13	I/O
34	—	—	45	62	A1	76	C2	50	L12	I/O
35	—	41	—	—	—	77	B1	51	K11	I/O
36	37	—	—	63	C2	78	C1	52	K12	I/O
37	—	42	46	64	B1	79	D3	53	M13	I/O
38	38	—	—	65	C1	80	D2	54	L13	I/O
39	—	43	47	66	D2	81	D1	55	J11	I/O
40	—	—	—	—	—	82	E2	56	J12	V_{DD}
41	—	—	—	—	—	83	E3	57	K13	V_{SS}
42	39	44	48	67	D1	—	—	58	J13	I/O
43	—	—	—	—	—	—	—	59	H11	I/O
44	40	—	—	—	—	—	—	60	H12	I/O
45	—	—	—	68	E2	84	E1	61	H13	I/O
46	—	1	—	1	E1	1	F1	62	G12	I/O
47	—	—	—	—	—	—	—	63	G11	I/O
48	—	—	—	—	—	—	—	64	G13	I/O
49	1	2	1	2	F1	2	F2	65	F13	I/O
50	2	—	—	—	—	—	—	66	F12	I/O
51	3	—	—	—	—	—	—	67	F11	I/O
52	—	3	2	3	F2	3	F3	68	E13	V_{DD}
53	—	4	3	4	G1	4	G1	69	D13	V_{SS}
54	4	—	—	5	H1	5	H1	70	E12	I/O
55	—	5	—	—	—	6	G2	71	E11	I/O
56	5	—	—	6	G2	7	J1	72	C13	I/O
57	—	—	—	—	—	8	G3	73	B13	I/O
58	—	—	—	7	J1	9	K1	74	D12	I/O
59	—	—	4	8	H2	10	H2	75	D11	I/O
60	—	6	5	9	J2	11	J2	76	C12	I/O
61	—	—	6	—	—	—	—	77	A13	I/O
62	6	7	7	10	H3	12	H3	78	D10	I/O
63	7	8	8	11	K1	13	J3	79	C11	TST
64	8	9	9	12	J3	14	K2	80	B12	TD/Input
65	9	10	10	13	K2	15	K3	81	B11	T3/Input
66	—	—	—	—	—	—	—	82	C10	Input
67	—	—	—	—	—	—	—	83	B10	Input
68	—	—	—	—	—	16	H4	84	A12	Input
69	—	—	—	—	—	17	J4	85	A11	Input
70	—	—	—	14	K3	—	—	86	C9	Input
71	—	—	11	—	—	—	—	87	B9	Input
72	—	—	—	15	J4	18	K4	88	A10	Input

PAD TO PIN CROSS REFERENCE GUIDE (Continued)

IC Pad	Packages									Pin Type
	40 Pin	44 Pin	48 Pin	68 Pin		84 Pin		124 Pin		
	DIP	LCC or PCC	DIP	LCC or PCC	PGA	LCC or PCC	PGA	LCC	PGA	
	Option 1	Option 0	Option 1	Option 1	Option 1	Option 0	Option 0	Option 0	Option 1	
73	10	—	—	16	K4	19	J5	89	A9	Input
74	—	11	—	—	—	—	—	90	C8	Input
75	—	—	—	17	J5	20	H5	91	B8	Input
76	—	—	12	18	K5	21	K5	92	A8	Input
77	—	—	—	—	—	—	—	93	B7	Input
78	—	12	—	—	—	22	K6	94	C7	Input
79	—	—	—	—	—	—	—	95	A7	Input
80	—	—	—	19	K6	23	J6	96	A6	Input
81	—	—	—	—	—	24	H6	97	B6	Input
82	11	13	13	20	J6	25	K7	98	C6	V_{DD}
83	12	14	14	21	K7	26	K8	99	A5	V_{SS}
84	—	—	—	—	—	—	—	100	A4	Input
85	—	—	—	22	K8	27	J7	101	B5	Input
86	—	—	—	—	—	—	—	102	C5	Input
87	13	15	15	23	J7	28	K9	103	A3	Input
88	—	—	—	—	—	—	—	104	A2	Input
89	—	—	16	—	—	—	—	105	B4	Input
90	—	—	—	—	—	29	H7	106	C4	Input
91	—	—	—	24	K9	30	K10	107	B3	Input
92	14	16	17	25	J8	31	J8	108	B2	Input
93	15	17	18	26	J9	32	J9	109	C3	I/O
94	—	—	19	—	—	—	—	110	D4	I/O
95	16	18	20	27	H8	33	H8	111	A1	I/O
96	—	—	21	28	K10	34	H9	112	C2	I/O
97	17	19	—	29	H9	35	J10	113	D3	I/O
98	—	—	—	—	—	36	H10	114	D2	I/O
99	—	—	—	30	J10	37	G8	115	B1	I/O
100	18	20	—	31	H10	38	G9	116	C1	I/O
101	—	21	22	32	G9	39	G10	117	E3	I/O
102	—	—	—	—	—	40	F9	118	E2	V_{DD}
103	—	—	—	—	—	41	F8	119	D1	V_{SS}
104	19	22	23	33	G10	—	—	120	E1	I/O
105	—	—	—	—	—	—	—	121	F3	I/O
106	20	—	24	34	F9	42	F10	122	F2	I/O
107	—	—	—	—	—	—	—	123	F1	I/O
108	—	23	—	—	—	43	E10	124	G2	I/O
109	—	—	—	—	—	—	—	1	G3	I/O
110	—	—	—	—	—	—	—	2	G1	I/O
111	21	—	—	35	F10	44	E9	3	H1	I/O
112	—	—	—	—	—	—	—	4	H2	I/O
113	—	—	25	—	—	—	—	5	H3	I/O
114	—	24	26	36	E10	45	E8	6	J1	V_{DD}
115	—	25	27	37	E9	46	D10	7	K1	V_{SS}
116	22	—	—	38	D10	47	C10	8	J2	I/O
117	23	26	—	39	C10	48	D9	9	J3	I/O
118	—	—	—	—	—	49	B10	10	L1	I/O
119	24	27	—	40	D9	50	D8	11	M1	I/O
120	—	—	—	41	B10	51	A10	12	K2	I/O
121	—	—	28	42	C9	52	C9	13	K3	I/O
122	25	28	29	43	B9	53	B9	14	L2	I/O
123	—	—	30	—	—	—	—	15	N1	I/O
124	26	29	31	44	C8	54	C8	16	K4	I/O

PACKAGING

Array Type	Package	Input Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6324	040PDIP1 040HDIP1	11	24	2	2	1	0
	044-LCC1 044-PCC1	13	22	4	4	1	0
	048PDIP1 048HDIP1	15	24	4	4	1	0
	068-LCC1 068-PCC1 068-PGA1	25	34	4	4	1	0
	084-LCC0 084-PCC0 084-PGA0 084LPGA0	33	38	6	6	1	0
	124-PGA1 124LPGA1	55	56	6	6	1	0

Package Abbreviations for this Publication:
PDIP: Plastic Dual In-Line Package
HDIP: Side-Brazed Ceramic Dual In-Line Package
LCC: Ceramic Leadless Chip Carrier
PCC: Plastic Leaded Chip Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid Array

TEST MODE FUNCTION TABLE

Input			Output Buffer Type	Output
Test Mode	Test Data	Test 3-State		
H	X	X	X	From Array
L L L	X H L	H L L	Any Bidirectional Option	Z L H
L L	H L	X X	Y01N Y01N	L H

X = Don't Care
Z = High Impedance

Macrocell Data Sheets 11

B02N
B02U
B02D

Non-Inverting Bidirectional Buffer with TTL Input Switching Levels

Netlist Format:
$SUBU B02X
BPO B / E A BPI
Note: X=N, U, or D

Pin Names:

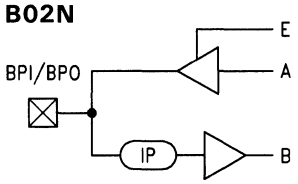
BPO/BPI—Bonding Pad Out/Bonding Pad In. This is a bidirectional input that is treated as separate input and output signals for simulation purposes. An I and O must be appended to the desired signal name in the netlist to give unique input and output signal names.

B—Input data to the internal array.

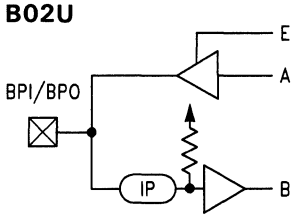
A—Output data from the internal array.

E—3-state enable signal from the internal array.

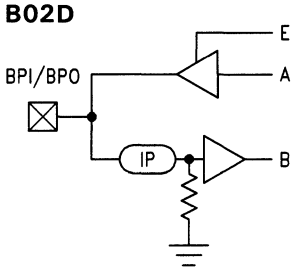
B02N



B02U



B02D



FUNCTION TABLE

E	BPI	A	B	BPO	Function
L	L/H	X	L/H	Z	The pin functions as an input. Data from the internal array is enabled and data from the BPI pin is enabled.
H	L/H	L/H	L/H	L/H	The pin functions as an output, with data originating from the internal array at point A. The data at point A appears at the BPO output and at point B.

SWITCHING CHARACTERISTICS* (C_L = as shown)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to BPO (Figures 1 and 3) C_L=50 pF	0.026	2.2	5.8	0.108	10.7	0.028	3.0	8.9	0.144	16.4	ns
t_{PHL}		0.034	2.6	6.2	0.124	11.5	0.018	3.0	8.4	0.136	15.6	
t_{PLZ}	Propagation Delay, E to BPO (Figures 2 and 4) C_L=50 pF R_L=1 kΩ	—	5.7	3.5	—	6.5	—	7.8	7.6	—	14.0	ns
t_{PHZ}		—	5.9	2.8	—	5.1	—	8.4	7.8	—	14.4	
t_{PZL}		0.034	3.1	7.8	0.124	14.5	0.018	3.8	10.8	0.136	20.0	
t_{PZH}		0.026	2.2	5.8	0.108	10.7	0.028	3.2	9.1	0.144	16.8	
t_{PLH}	Propagation Delay, BPI to B (Figure 1) C_L=1 pF	0.4	1.4	2.9	2.0	5.3	0.4	2.6	4.4	2.6	8.0	ns
t_{PHL}		0.4	1.5	4.4	2.0	8.2	0.6	3.2	7.6	3.2	14.0	

*See Section 4 for minimum, typical, and maximum conditions.

**$t_{P(total)}=t_P(C_L=1\ pF)+K(C_L-1\ pF)$, for the A output,
$t_{P(total)}=t_P(C_L=50\ pF)+K(C_L-50\ pF)$, for the BPO output, for K in units of ns/pF. See Section 4.

11

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A	8.0
		E	7.0

SWITCHING WAVEFORMS

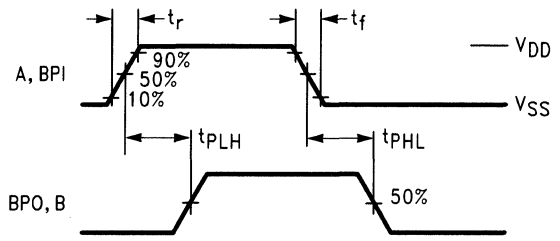


Figure 1

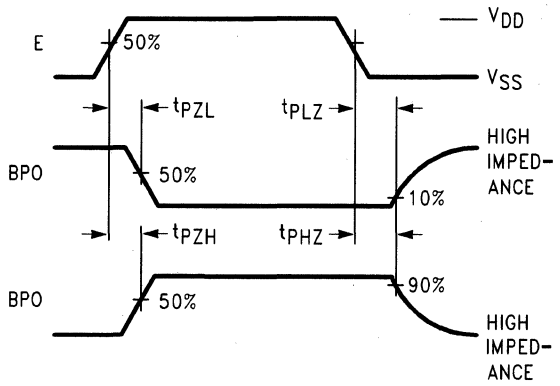
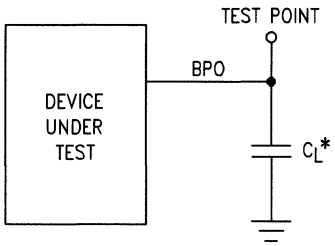
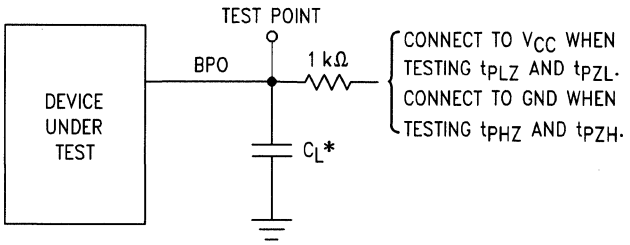


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit



* Includes all probe and jig capacitance.

Figure 4. Test Circuit

11

B03N
B03U
B03D

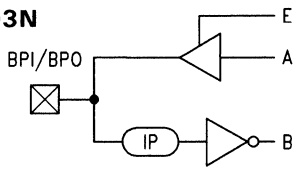
Inverting Bidirectional Buffer with CMOS Input Switching Levels

Netlist Format:
$SUBU B03X
BPO B / E A BPI
Note: X = N, U, or D

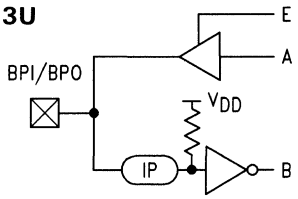
Pin Names:

BPO/BPI—Bonding Pad Out/Bonding Pad In. This is a bidirectional input that is treated as separate input and output signals for simulation purposes. An I and O must be appended to the desired signal name in the netlist to give unique input and output signal names.
B—Input data to the internal array.
A—Output data from the internal array.
E—3-state enable signal from the internal array.

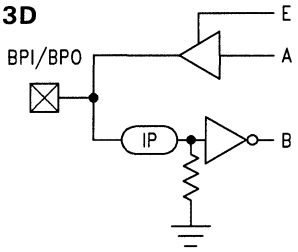
B03N



B03U



B03D



FUNCTION TABLE

E	BPI	A	B	BPO	Function
L	L/H	X	H/L	Z	The pin functions as an input. Data from the internal array is enabled and data from the BPI pin is enabled.
H	L/H	L/H	H/L	L/H	The pin functions as an output, with data originating from the internal array at point A. The data at point A appears at the BPO output and at point B.

SWITCHING CHARACTERISTICS* (C_L = as shown)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to BPO (Figures 1 and 4) C_L = 50 pF	0.026	2.2	5.8	0.108	10.7	0.028	3.0	8.9	0.144	16.4	ns
t_{PHL}		0.034	2.6	6.2	0.124	11.5	0.018	3.0	8.4	0.136	15.6	
t_{PLZ}	Propagation Delay, E to BPO (Figures 2 and 5) C_L = 50 pF, R_L = 1 KΩ	—	5.7	3.5	—	6.5	—	7.8	7.6	—	14.0	ns
t_{PHZ}		—	5.9	2.8	—	5.1	—	8.4	7.8	—	14.4	
t_{PZL}		0.034	3.1	7.8	0.124	14.5	0.018	3.8	10.8	0.136	20.0	
t_{PZH}		0.026	2.2	5.8	0.108	10.7	0.028	3.2	9.1	0.144	16.8	
t_{PLH}	Propagation Delay, BPI to B (Figure 3) C_L = 1 pF	0.3	0.6	1.7	1.4	3.2	0.8	2.8	3.9	2.8	7.2	ns
t_{PHL}		0.3	0.7	1.7	1.2	3.2	0.6	2.4	3.5	2.8	6.4	

*See Section 4 for minimum, typical, and maximum conditions.
**t_P(total) = t_P(C_L = 1 pF) + K(C_L − 1 pF), for the A output, t_P(total) = t_P(C_L = 50 pF) + K(C_L − 50 pF), for the BPO output, for K in units of ns/pF. See Section 4.

11

INPUT LOAD FACTORS

IUL	Input Unit Load Factor	A	8.0
		E	7.0

SWITCHING WAVEFORMS

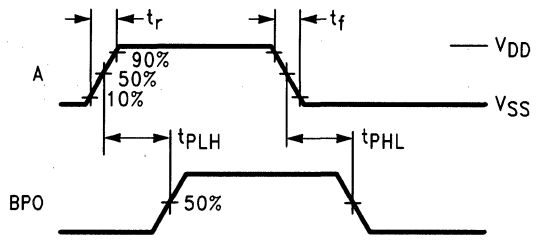


Figure 1

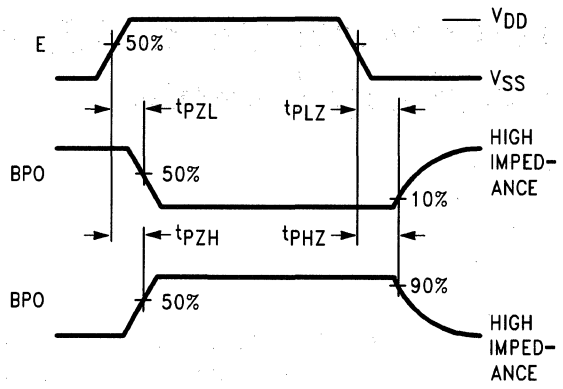


Figure 2

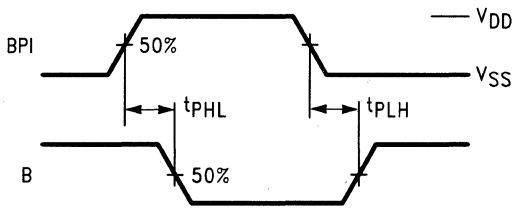
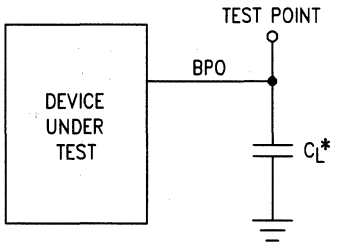
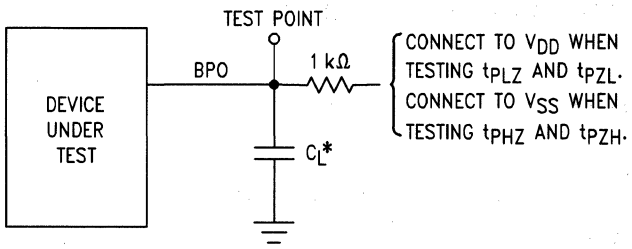


Figure 3



*Includes all probe and jig capacitance.

Figure 4. Test Circuit



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

11

B04N
B04U
B04D

Non-Inverting Bidirectional Buffer with CMOS Input Switching Levels

Netlist Format:
$SUBU B04X
BPO B / E A BPI

Note: X = N, U, or D

Pin Names:

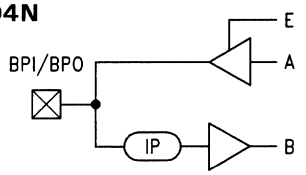
BPO/BPI—Bonding Pad Out/Bonding Pad In. This is a bidirectional input that is treated as separate input and output signals for simulation purposes. An I and O must be appended to the desired signal name in the netlist to give unique input and output signal names.

B—Input data to the internal array.

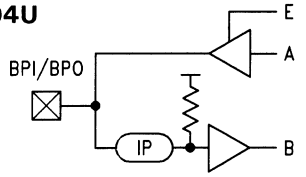
A—Output data from the internal array.

E—3-state enable signal from the internal array.

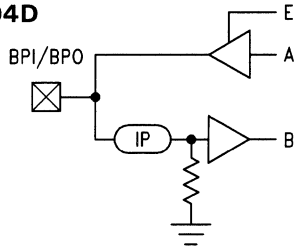
B04N



B04U



B04D



FUNCTION TABLE

E	BPI	A	B	BPO	Function
L	L/H	X	L/H	Z	The pin functions as an input. Data from the internal array is enabled and data from the BPI pin is enabled.
H	L/H	L/H	L/H	L/H	The pin functions as an output, with data originating from the internal array at point A. The data at point A appears at the BPO output and at point B.

SWITCHING CHARACTERISTICS* (C_L = as shown)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to BPO (Figures 1 and 3) C_L = 50 pF	0.026	2.2	5.8	0.108	10.7	0.028	3.0	8.9	0.144	16.4	ns
t_{PHL}		0.034	2.6	6.2	0.124	11.5	0.018	3.0	8.4	0.136	15.6	
t_{PLZ}	Propagation Delay, E to BPO (Figures 2 and 4) C_L = 50 pF R_L = 1 kΩ	—	5.7	3.5	—	6.5	—	7.8	7.6	—	14.0	ns
t_{PHZ}		—	5.9	2.8	—	5.1	—	8.4	7.8	—	14.4	
t_{PZL}		0.034	3.1	7.8	0.124	14.5	0.018	3.8	10.8	0.136	20.0	
t_{PZH}		0.026	2.2	5.8	0.108	10.7	0.028	3.2	9.1	0.144	16.8	
t_{PLH}	Propagation Delay, BPI to B (Figures 1 and 3) C_L = 1 pF	0.4	0.8	2.3	1.4	4.2	0.4	2.6	4.5	2.4	8.4	ns
t_{PHL}		0.4	0.9	2.4	1.2	4.4	0.4	3.0	5.0	1.6	9.2	

*See Section 4 for minimum, typical, and maximum conditions.

**$t_{p(total)} = t_p(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for the A output, $t_{p(total)} = t_p(C_L = 50\text{ pF}) + K(C_L - 50\text{ pF})$, for the BPO output, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A	8.0
		E	7.0

11

SWITCHING WAVEFORMS

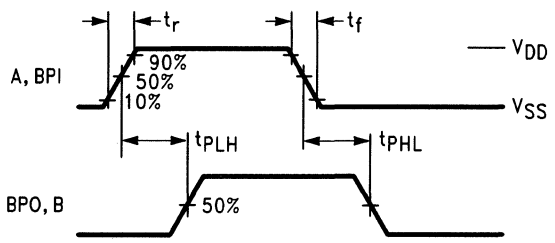


Figure 1

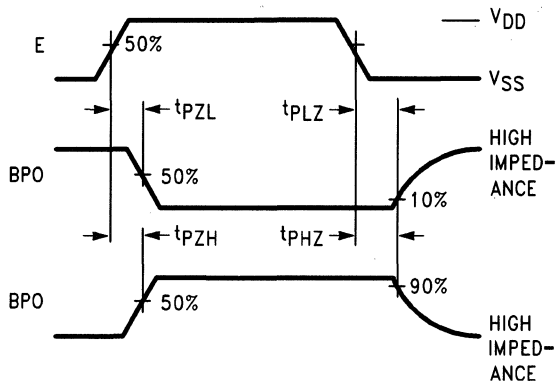
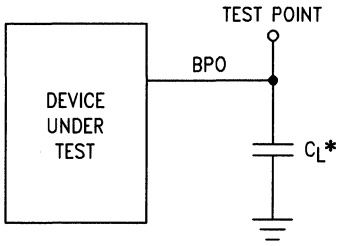
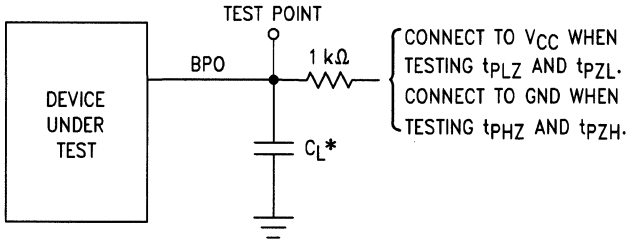


Figure 2



* Includes all probe and jig capacitance.

Figure 3. Test Circuit



* Includes all probe and jig capacitance.

Figure 4. Test Circuit

11

B05N
B05U
B05D

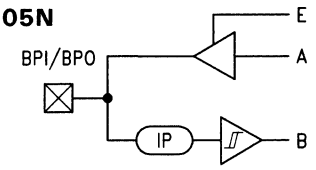
Non-Inverting Bidirectional Buffer with Schmitt Trigger Switching Levels

Netlist Format:
$SUBU B05X
BPO B / E A BPI
Note: X = N, U, or D

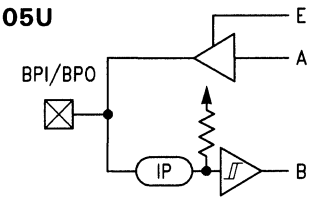
Pin Names:

BPO/BPI—Bonding Pad Out/Bonding Pad In. This is a bidirectional input that is treated as separate input and output signals for simulation purposes. An I and O must be appended to the desired signal name in the netlist to give unique input and output signal names.
B—Input data to the internal array.
A—Output data from the internal array.
E—3-state enable signal from the internal array.

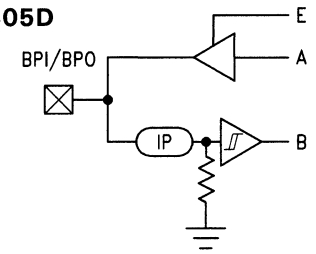
B05N



B05U



B05D



FUNCTION TABLE

E	BPI	A	B	BPO	Function
L	L/H	X	L/H	Z	The pin functions as an input. Data from the internal array is enabled and data from the BPI pin is enabled.
H	L/H	L/H	L/H	L/H	The pin functions as an output, with data originating from the internal array at point A. The data at point A appears at the BPO output and at point B.

ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V DC, T_A = −40°C to +85°C)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS		HCA6300 Series 3-Micron HCMOS		Unit
		Min	Max	Min	Max	
V_{T+}	Positive-Going Threshold Voltage	3.2	3.4	3.1	3.4	V
V_{T-}	Negative-Going Threshold Voltage	0.8	1.1	0.7	1.1	V
V_H	Hysteresis Voltage	2.1	2.6	2.0	2.7	V

SWITCHING CHARACTERISTICS* (C_L = as shown)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to BPO (Figures 1 and 3) C_L = 50 pF	0.026	2.2	5.8	0.108	10.7	0.028	3.0	8.9	0.144	16.4	ns
t_{PHL}		0.034	2.6	6.2	0.124	11.5	0.018	3.0	8.4	0.136	15.6	
t_{PLZ}	Propagation Delay, E to BPO (Figures 2 and 4) C_L = 50 pF, R_L = 1 KΩ	—	5.7	3.5	—	6.5	—	7.8	7.6	—	14.0	ns
t_{PHZ}		—	5.9	2.8	—	5.1	—	8.4	7.8	—	14.4	
t_{PZL}		0.034	3.1	7.8	0.124	14.5	0.018	3.8	10.8	0.136	20.0	
t_{PZH}		0.026	2.2	5.8	0.108	10.7	0.028	3.2	9.1	0.144	16.8	
t_{PLH}	Propagation Delay, BPI to B (Figure 1) C_L = 50 pF	0.4	1.3	3.4	1.6	6.2	0.6	4.2	6.7	2.4	12.4	ns
t_{PHL}		0.4	2.9	8.5	1.8	15.8	0.6	7.4	16.5	2.8	30.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for the A output,
$t_{p(total)} = t_p(C_L = 50\ pF) + K(C_L - 50\ pF)$, for the BPO output, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A	8.0
		E	7.0

SWITCHING WAVEFORMS

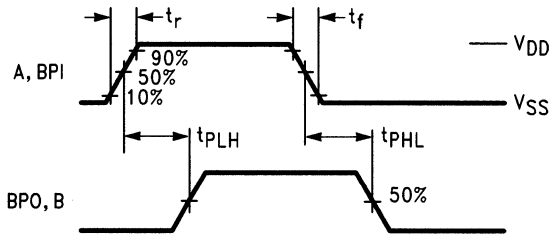


Figure 1

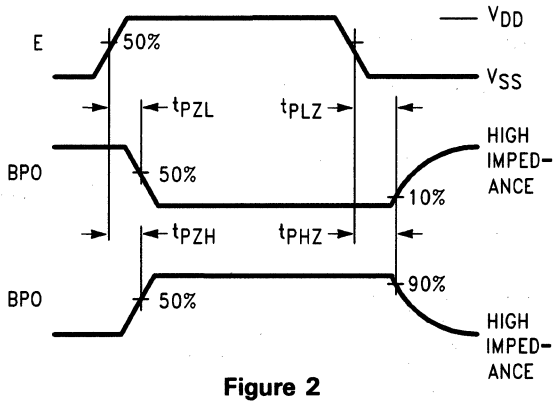
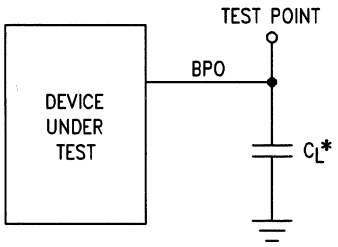
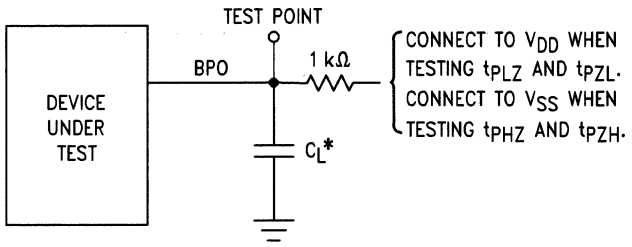


Figure 2



*Includes all probe and jig capacitance.

Figure 3. Test Circuit

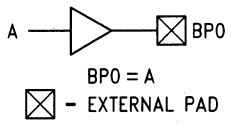


*Includes all probe and jig capacitance.

Figure 4. Test Circuit

Y01N

Non-Inverting Output Buffer



Netlist Format:
$SUBU Y01N
BPO / A

Pin Names:
BPO—Bonding Pad Output
A—Output Data from the Internal Array

SWITCHING CHARACTERISTICS* (C_L = 50 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to BPO (Figures 1 and 2)	0.024	2.2	5.6	0.108	10.3	0.032	2.8	8.2	0.152	15.6	ns
t_{PHL}		0.032	2.5	5.9	0.124	10.9	0.028	2.8	6.7	0.120	13.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 50\ pF) + K(C_L - 50\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A	8.0

SWITCHING WAVEFORMS

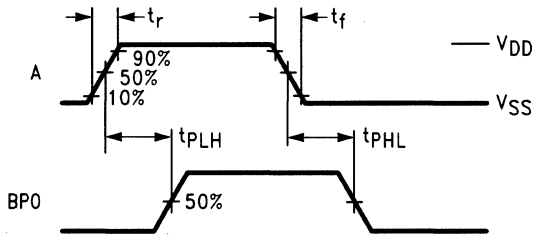
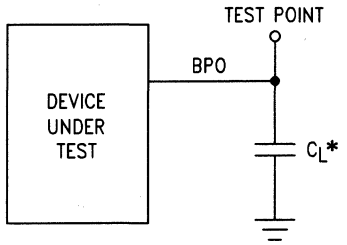


Figure 1



* Includes all probe and jig capacitance.

Figure 2

11

Y02N

Open Drain Output Buffer

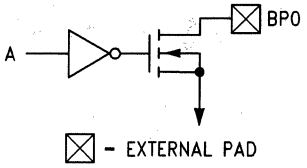
Netlist Format:
$SUBU Y02N
BPO / A

Pin Names:
BPO—Bonding Pad Output
A—Input data from the internal array

FUNCTION TABLE

Input A	Output BPO
L	L
H	Z

Z = High Impedance



SWITCHING CHARACTERISTICS* (C_L = 50 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLZ}	Propagation Delay, (Figures 1, 2, and 3)	—	5.3	2.4	—	4.4	—	6.4	5.7	—	11.2	ns
t_{PZL}		0.034	2.3	5.5	0.132	10.1	0.028	2.6	9.7	0.128	12.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_{p(@50\ pF)} + K(C_L - 50\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A	8.0

SWITCHING WAVEFORMS

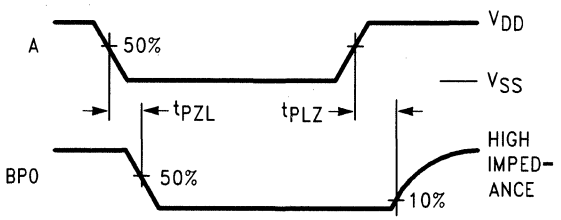
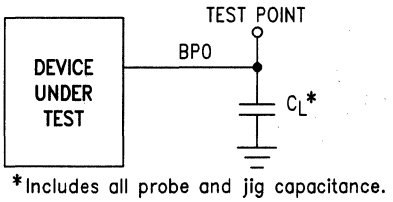
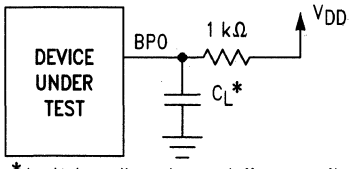


Figure 1



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



*Includes all probe and jig capacitance.

Figure 3

11

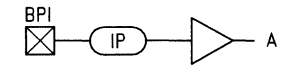
I01N
I01U
I01D

Non-Inverting Input Buffer with TTL Input Switching Levels

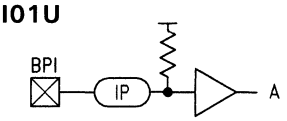
Netlist Format:
$SUBU I01X
A / BPI
Note: X=N, U or D

Pin Names:
BPI—Bonding Pad Input.
A—Input data to the internal array.

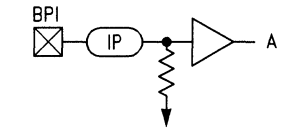
I01N

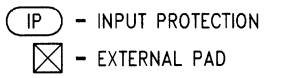


I01U



I01D





SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1)	0.5	1.5	3.0	2.0	5.5	0.5	2.7	5.1	2.6	8.2	ns
t_{PHL}		0.5	1.6	4.5	2.0	8.4	0.6	3.2	7.7	3.2	14.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

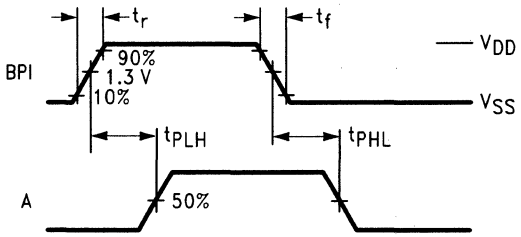


Figure 1

11

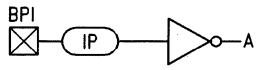
I02N
I02U
I02D

Inverting Input Buffer with CMOS Input Switching Levels

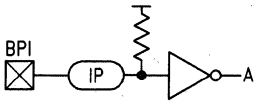
Netlist Format:
$SUBU I02X
A / BPI
Note: X = N, U, or D

Pin Names:
BPI—Bonding Pad Input.
A—Input data to the internal array.

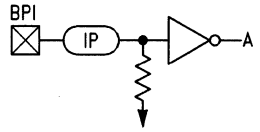
I02N



I02U



I02D



IP - INPUT PROTECTION
- EXTERNAL PAD

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1)	0.4	0.8	1.8	1.4	3.4	0.8	2.8	4.8	2.8	7.2	ns
t_{PHL}		0.4	0.8	1.8	1.3	3.4	0.6	2.4	3.4	2.8	6.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

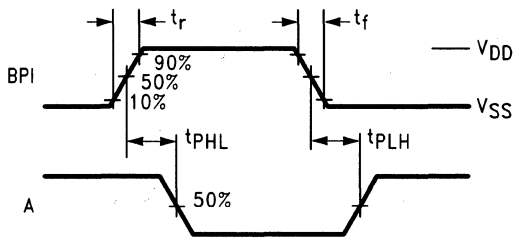


Figure 1

11

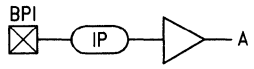
I03N
I03U
I03D

Non-Inverting Input Buffer with CMOS Input Switching Levels

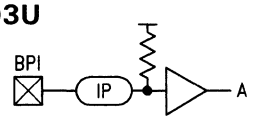
Netlist Format:
$SUBU I03X
A / BPI
Note: X=N, U, or D

Pin Names:
BPI—Bonding Pad Input.
A—Input data to the internal array.

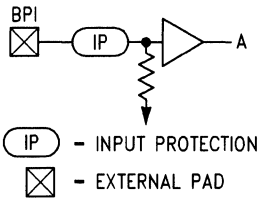
I03N



I03U



I03D



SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1)	0.3	1.0	2.4	1.4	4.4	0.4	2.6	4.6	2.4	8.4	ns
t_{PHL}		0.4	1.0	2.4	1.3	4.5	0.4	3.0	5.5	1.6	9.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

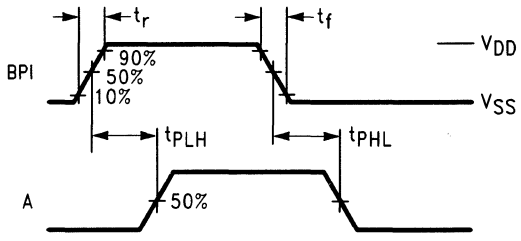


Figure 1

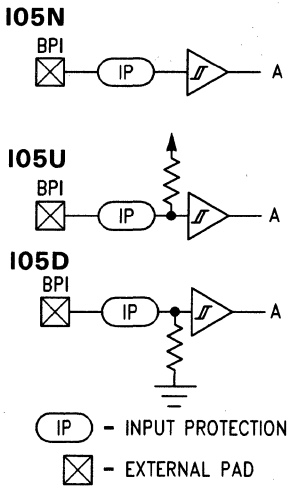
11

I05N
I05U
I05D

Non-Inverting Input Buffer with Schmitt Trigger Switching Levels

Netlist Format:
$SUBU I05X
A / BPI
Note: X=N, U, or D

Pin Names:
BPI—Bonding Pad Input.
A—Input data to the internal array.



ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to +85°C)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS		HCA6300 Series 3-Micron HCMOS		Unit
		Min	Max	Min	Max	
V_{T+}	Positive-Going Threshold Voltage	3.2	3.4	3.1	3.4	V
V_{T-}	Negative-Going Threshold Voltage	0.8	1.1	0.7	1.1	V
V_H	Hysteresis Voltage	2.1	2.6	2.0	2.7	V

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1)	0.4	1.4	3.5	1.6	6.5	0.6	4.2	6.7	2.4	12.4	ns
t_{PHL}		0.4	3.2	8.6	1.8	16.0	0.6	7.4	16.4	2.8	30.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

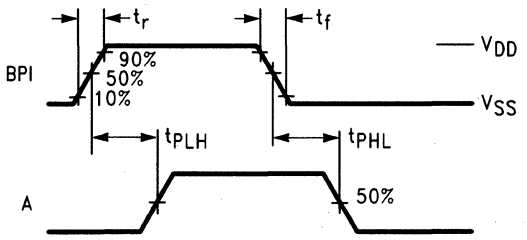


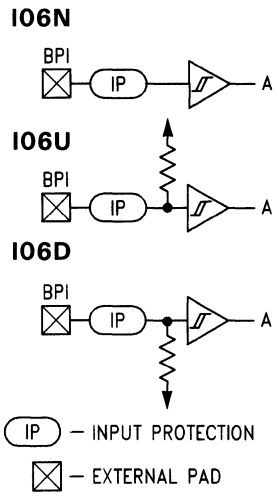
Figure 1

I06N
I06U
I06D

Non-Inverting Input Clock Buffer with Schmitt Trigger Switching Levels

Netlist Format:
$SUBU I06X
A / BPI
Note: X = N, U or D

Pin Names:
BPI —Bonding Pad Input.
A—Input data to the internal array.



ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 Vdc, T_A = −40° to +85°C)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS		HCA6300 Series 3-Micron HCMOS		Unit
		Min	Max	Min	Max	
V_{T+}	Positive-Going Threshold Voltage	3.2	3.4	3.1	3.4	V
V_{T-}	Negative-Going Threshold Voltage	0.8	1.1	0.7	1.1	V
V_H	Hysteresis Voltage	2.1	2.6	2.0	2.7	V

SWITCHING CHARACTERISTICS* (C_L = as shown)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1) C_L = 15 pF	0.026	2.1	5.8	0.109	10.8	0.028	4.4	11.0	0.136	19.3	ns
t_{PHL}		0.034	3.7	10.8	0.120	20.0	0.028	7.2	19.5	0.140	36.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 15\ pF) + K(C_L - 15\ pF)$, for K in units of ns/pF. See Section 4.

11

SWITCHING WAVEFORMS

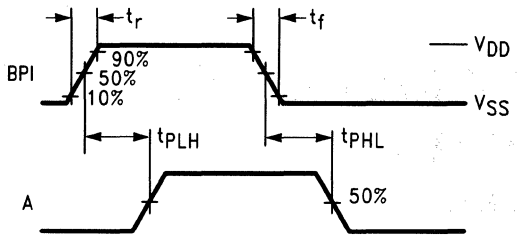


Figure 1

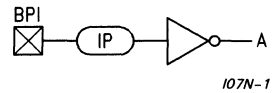
I07N
I07U
I07D

Inverting Input Clock Buffer with CMOS Input Switching Levels

Netlist Format:
$SUBU I07X
A / BPI
Note: X=N, U, or D

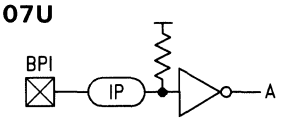
Pin Names:
BPI —Bonding Pad Input.
A—Input data to the internal array.

I07N



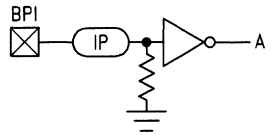
I07N-1

I07U



I07N-2

I07D



IP – INPUT PROTECTION

– EXTERNAL PAD

SWITCHING CHARACTERISTICS* (C_L = 15 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1) C_L = 15 pF	0.029	1.1	2.0	0.111	3.7	0.032	2.6	4.2	0.144	7.0	ns
t_{PHL}		0.031	1.4	2.2	0.123	4.1	0.024	2.6	6.3	0.120	6.8	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

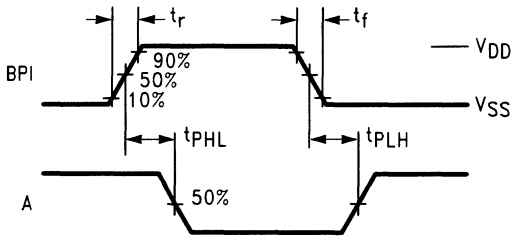


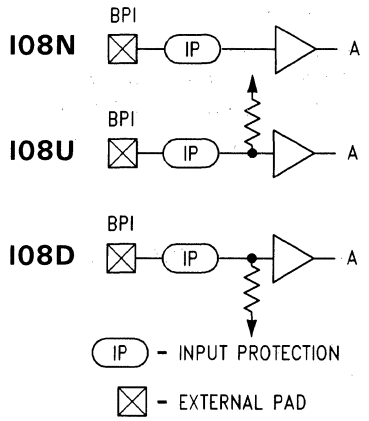
Figure 1

I08N
I08U
I08D

Non-Inverting Input Clock Buffer with CMOS Switching Levels

Netlist Format:
$SUBU I08N
A / BPI
Note: X=N, U or D

Pin Names:
BPI—Bonding Pad Input.
A—Input data to the internal array.



SWITCHING CHARACTERISTICS* (C_L = 15 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1) C_L = 15 pF	0.026	1.2	2.9	0.111	5.3	0.024	2.8	6.1	0.136	9.8	ns
t_{PHL}		0.034	1.2	2.8	0.126	5.1	0.028	2.4	5.2	0.136	9.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 15\ pF) + K(C_L - 15\ pF)$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

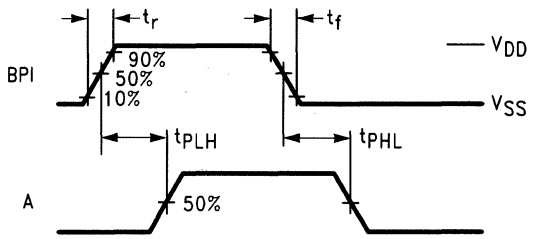


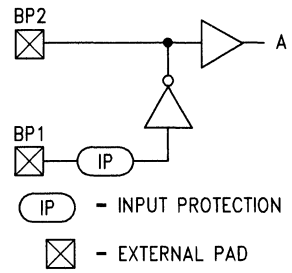
Figure 1

11

I09N

Oscillator with Clock Buffer

I09N*



*Requires two uncommitted buffer locations.

Netlist Format:
$SUBU I09N
BP2 A / BP1

Pin Names:
BP1—Bonding pad input.
BP2—Bonding pad output.
A—Input data to the internal array.

SWITCHING CHARACTERISTICS* (C_L = as noted)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BP1 to BP2 (Figure 1) C_L=50 pF	0.024	2.2	4.4	0.096	8.2	0.028	2.8	6.4	0.112	11.8	ns
t_{PHL}		0.032	2.8	5.0	0.128	9.2	0.028	2.8	5.7	0.128	10.6	
t_{PLH}	Propagation Delay, BP1 to A (Figure 1) C_L=15 pF	0.028	3.8	8.2	0.114	15.2	0.028	4.8	12.0	0.149	22.2	ns
t_{PHL}		0.028	4.2	8.4	0.126	15.5	0.028	4.6	10.8	0.132	20.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L=15\ pF) + K(C_L-15\ pF)$, for output A, $t_{P(total)} = t_P(C_L=50\ pF) + K(C_L-50\ pF)$, for output BP2. See Section 4.

SWITCHING WAVEFORMS

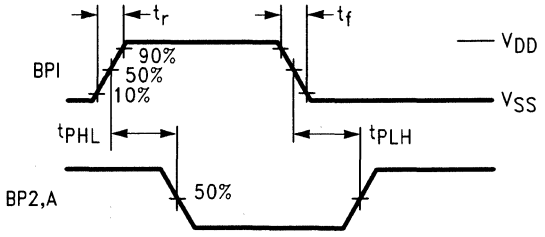


Figure 1

11

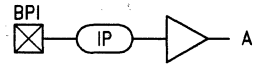
I10N
I10U
I10D

Non-Inverting Clock Driver with TTL Input Switching Levels

Netlist Format:
$SUBU I10X
A / BPI
Note: X=N, U or D

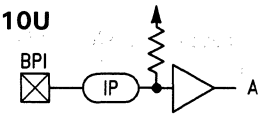
Pin Names:
BPI—Bonding Pad Input.
A—Input data to the internal array.

I10N



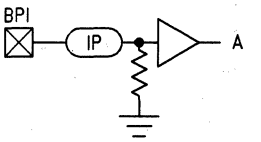
I10N-1

I10U



I10N-2

I10D



IP - INPUT PROTECTION
⊠ - EXTERNAL PAD

SWITCHING CHARACTERISTICS* (C_L = as shown)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, BPI to A (Figure 1) C_L = 15 pF	0.017	2.1	5.1	0.074	9.4	0.029	2.6	8.6	0.154	16.0	ns
t_{PHL}		0.020	2.1	6.2	0.086	11.4	0.017	3.0	10.8	0.131	20.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 15\ pF) + K\ (C_L - 15\ pF)$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

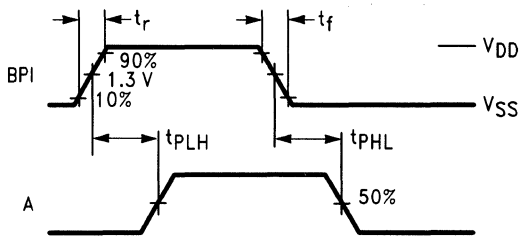


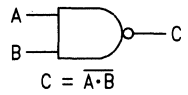
Figure 1

11

C001

Triple 2-Input NAND Gate

(1/3 OF MACROCELL)



Primary Cells: 1
Netlist Format:
$SUBU C001
C1 C2 C3 / A1 B1 A2 B2 A3 B3

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.4	0.6	1.6	1.8	3.0	0.5	1.0	2.5	2.5	4.6	ns
t_{PHL}		0.8	1.0	2.7	3.4	5.0	0.7	1.2	3.2	3.6	6.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B	1.0

SWITCHING WAVEFORMS

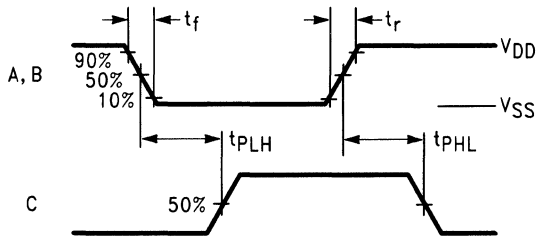


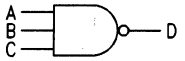
Figure 1

11

C002

Dual 3-Input NAND Gate

(1/2 OF MACROCELL)



$D = \overline{A \cdot B \cdot C}$

Primary Cells: 1
Netlist Format:
$SUBU C002
D1 D2 / A1 B1 C1 A2 B2 C2

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, (Figure 1)	0.4	0.6	1.7	1.2	3.2	0.6	1.2	2.8	2.4	5.2	ns
t_{PHL}		1.0	1.6	3.8	4.8	7.4	1.0	2.0	5.6	5.2	10.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C	1.0

SWITCHING WAVEFORMS

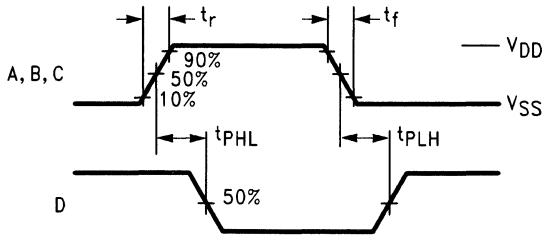


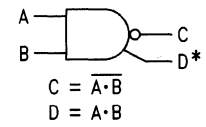
Figure 1

11

C003

Dual 2-Input NAND/AND Gate

(1/2 OF MACROCELL)



Primary Cells: 1
Netlist Format:
$SUBU C003
C1 D1 C2 D2 / A1 B1 A2 B2

*This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

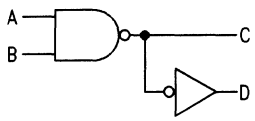
Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.4	0.8	1.8	1.8	3.4	0.2	0.6	2.4	2.4	5.2	ns
t_{PHL}		0.8	1.4	2.9	4.6	5.4	0.6	1.2	3.4	3.5	6.6	
t_{PLH}	Propagation Delay, A, B to D (Figure 1)	0.6	2.2	5.6	2.5	10.4	0.6	2.4	6.7	3.0	12.8	ns
t_{PHL}		0.4	1.8	4.0	1.8	7.4	0.4	1.8	5.2	2.2	10.2	
t_{PLH}	Propagation Delay, C to D (Figure 2)	0.6	0.6	2.0	2.5	3.7	0.6	0.8	3.3	3.0	6.2	ns
t_{PHL}		0.4	0.8	1.4	1.8	2.6	0.4	0.8	2.8	2.2	5.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B	1.0

FUNCTION DIAGRAM



SWITCHING WAVEFORMS

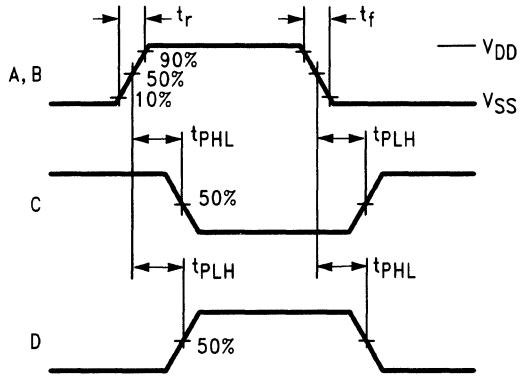


Figure 1

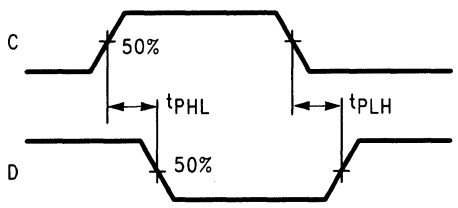


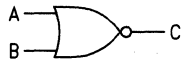
Figure 2

11

C004

Triple 2-Input NOR Gate

(1/3 OF MACROCELL)



$C = \overline{A+B}$

Primary Cells: 1
Netlist Format:
$SUBU C004
C1 C2 C3 / A1 B1 A2 B2 A3 B3

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.8	1.0	2.8	3.6	5.2	0.9	1.6	4.2	4.6	8.0	ns
t_{PHL}		0.4	0.8	1.8	1.8	3.4	0.4	0.8	2.3	2.0	4.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B	1.0

SWITCHING WAVEFORMS

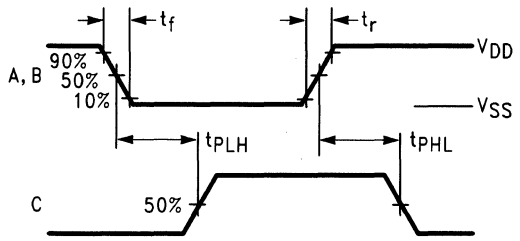


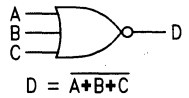
Figure 1

11

C005

Dual 3-Input NOR Gate

(1/2 OF MACROCELL)



$D = \overline{A+B+C}$

Primary Cells: 1
Netlist Format:
$SUBU C005
D1 D2 / A1 B1 C1 A2 B2 C2

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C to D (Figure 1)	1.0	1.4	5.3	3.6	9.8	1.2	2.2	6.2	6.6	12.0	ns
t_{PHL}		0.4	0.8	1.6	1.8	3.0	0.4	1.0	2.7	2.4	5.0	

*See Section 4 for minimum, typical, and maximum conditions.
**t_P (total) = $t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors — A, B, C	1.0

SWITCHING WAVEFORMS

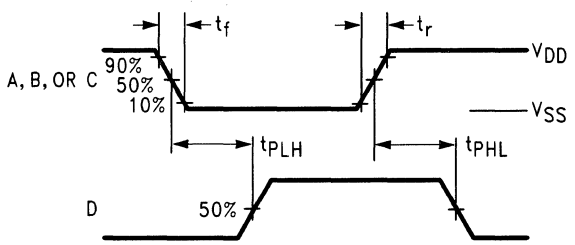


Figure 1

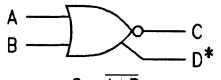
11

C006

Dual 2-Input NOR/OR Gate

Primary Cells: 1
Netlist Format:
$SUBU C006
C1 D1 C2 D2 / A1 B1 A2 B2

(1/2 OF MACROCELL)



$C = \overline{A+B}$
$D = A+B$

* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.8	1.2	3.2	3.2	6.0	1.0	1.6	4.4	4.8	8.4	ns
t_{PHL}		0.4	1.0	2.2	1.8	4.0	0.4	1.0	2.4	2.0	4.4	
t_{PLH}	Propagation Delay, A, B to D (Figure 1)	0.4	1.8	4.2	1.8	7.8	0.4	1.8	5.1	2.2	9.8	ns
t_{PHL}		0.6	2.4	6.1	2.5	11.2	0.4	2.6	7.5	3.0	14.6	
t_{PLH}	Propagation Delay, C to D (Figure 2)	0.4	0.4	2.1	1.8	2.4	0.4	0.8	2.9	2.2	5.4	ns
t_{PHL}		0.6	1.0	2.8	2.5	3.3	0.4	1.0	3.4	3.0	6.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_P(total) = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$ for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B	1.0

SWITCHING WAVEFORMS

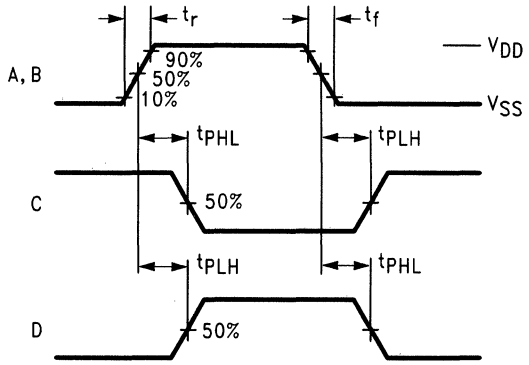


Figure 1

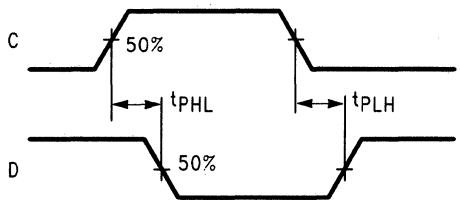
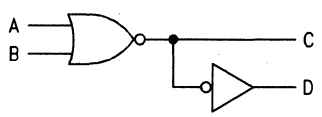


Figure 2

LOGIC DIAGRAM

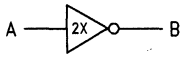


11

C007

Triple Inverting Buffer

(1/3 OF MACROCELL)



$B = \overline{A}$

Primary Cells: 1
Netlist Format:
$SUBU C007
B1 B2 B3 / A1 A2 A3

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.2	0.4	1.0	1.0	1.8	0.4	0.6	1.5	1.4	2.6	ns
t_{PHL}		0.2	0.4	1.0	1.0	2.0	0.4	0.6	1.5	1.4	2.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Load Factors—A	2.0

SWITCHING WAVEFORMS

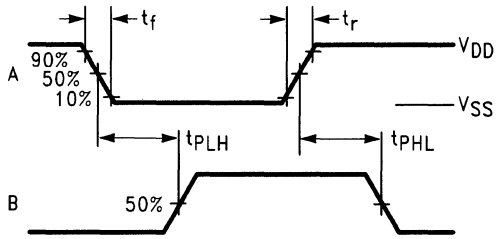


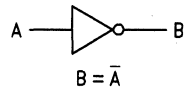
Figure 1

11

C008

Quad Inverter

(1/4 OF MACROCELL)



Primary Cells: 1
Netlist Format:
$SUBU C008
B1 B2 B3 B4 / A1 A2 A3 A4

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.4	0.8	1.7	1.8	3.2	0.4	0.8	2.1	2.2	4.0	ns
t_{PHL}		0.4	1.0	1.8	1.8	3.4	0.4	0.8	2.1	2.2	4.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A	1.0

SWITCHING WAVEFORMS

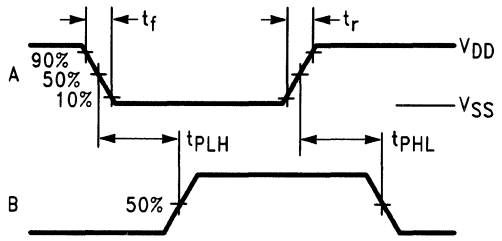


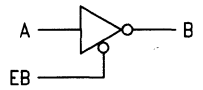
Figure 1

11

C009

Dual 3-State Inverting Buffer

(1/2 OF MACROCELL)



Primary Cells: 1
Netlist Format:
$SUBU C009
B1 B2 / A1 EB1 A2 EB2

Pin Names
A—Data Input
B—Data Output
EB—Enable Bar

FUNCTION TABLE

EB	A	B
L	L	H
L	H	L
H	X	Z

Z = High Impedance
X = Don't Care

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

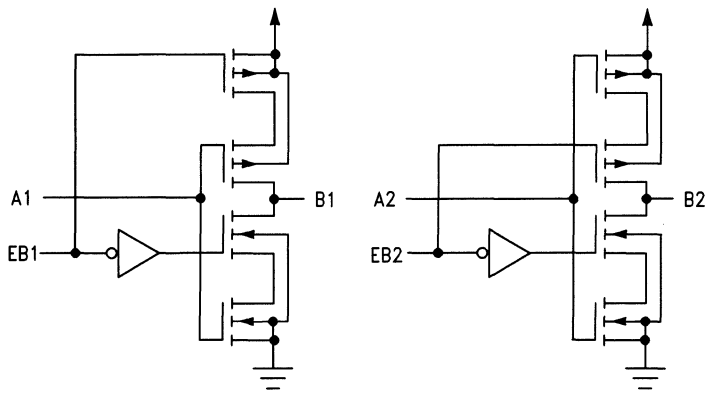
Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.8	1.2	2.9	3.6	5.3	0.8	1.6	4.9	4.8	9.0	ns
t_{PHL}		1.0	1.2	2.9	3.6	5.3	0.6	1.4	4.0	3.8	7.4	
t_{PLZ}	Propagation Delay, EB to B (Figure 2)	—	0.4	1.2	—	2.2	—	1.0	1.2	—	2.4	ns
t_{PHZ}		—	0.4	1.2	—	2.2	—	1.0	1.2	—	2.4	
t_{PZL}		0.8	1.4	3.5	3.6	6.4	0.8	1.2	4.3	4.8	8.0	
t_{PZH}		1.0	1.4	3.2	3.6	6.0	0.6	1.2	4.5	3.8	8.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A	1.0
		EB	1.7

FUNCTION DIAGRAM



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SWITCHING WAVEFORMS

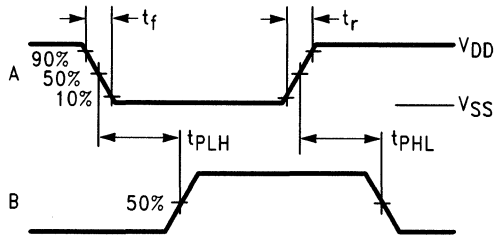


Figure 1

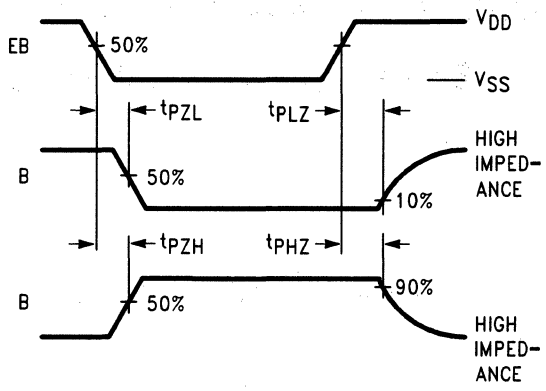
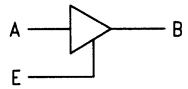


Figure 2

C010

3-State Non-Inverting Buffer



Primary Cells: 1
Netlist Format:
$SUBU C010
B / A E

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

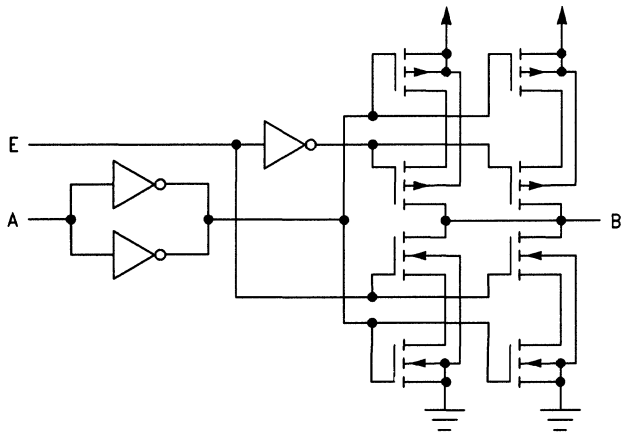
Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.4	1.0	2.6	1.8	4.8	0.4	1.4	4.9	2.4	7.6	ns
t_{PHL}		0.4	1.0	2.2	1.8	4.0	0.4	1.4	4.0	2.0	6.6	
t_{PLZ}	Propagation Delay, E to B (Figure 2)	—	0.4	0.9	—	1.6	—	1.0	2.6	—	3.4	ns
t_{PHZ}		—	0.6	2.2	—	4.0	—	1.0	2.6	—	3.4	
t_{PZL}		0.4	0.8	1.9	1.8	3.6	0.4	1.2	3.5	2.0	4.4	
t_{PZH}		0.4	1.0	2.6	1.8	4.8	0.4	1.2	3.5	2.4	6.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF), + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A	2.0
		E	1.7

FUNCTION DIAGRAM



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SWITCHING WAVEFORMS

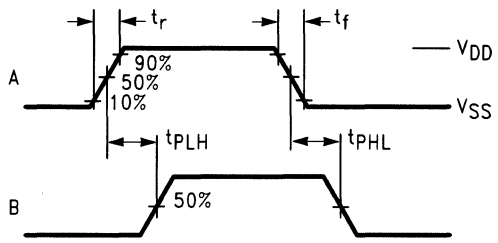


Figure 1

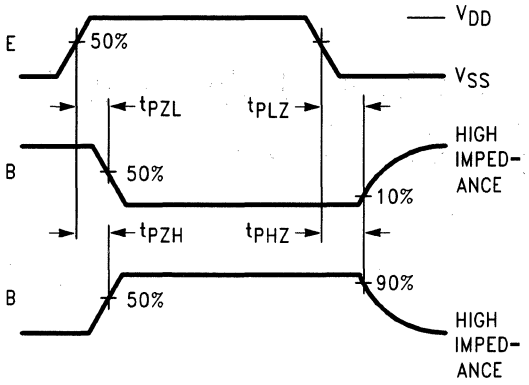


Figure 2

11

C012

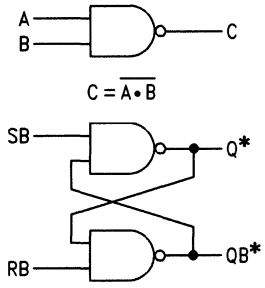
NAND Latch and 2-Input NAND Gate

Primary Cells: 1
Netlist Format:
$SUBU C012
C Q QB / A B SB RB

FUNCTION TABLE

Inputs		Outputs	
SB	RB	Q	QB
L	L	H*	H*
L	H	H	L
H	L	L	H
H	H	No Change	

* Both outputs will remain high as long as SB and RB are low, but the output states are unpredictable if SB and RB go high simultaneously.



* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.4	0.8	1.7	1.8	3.2	0.4	0.8	2.4	2.6	4.6	ns
t_{PHL}		0.6	1.2	2.7	3.4	5.0	0.8	1.2	3.2	3.8	6.2	
t_{PLH}	Propagation Delay, SB to Q (Figure 2)	0.4	0.8	1.8	2.0	3.4	0.6	1.0	2.7	2.4	5.0	ns
t_{PHL}	Propagation Delay, SB to QB (Figure 2)	1.4	2.2	5.4	6.4	10.0	0.8	2.6	7.1	3.8	13.4	ns
t_{PHL}	Propagation Delay, RB to Q (Figure 2)	1.4	2.2	5.4	6.4	10.0	0.8	2.6	7.1	3.8	13.4	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 2)	0.4	0.8	1.8	2.0	3.4	0.6	1.0	2.7	2.4	5.0	ns
t_{PHL}	Propagation Delay, Q to QB (Figure 3)	1.4	1.8	4.6	6.4	8.6	0.8	1.6	4.5	3.8	8.4	ns
t_{PHL}	Propagation Delay, QB to Q (Figure 3)	1.4	1.8	4.6	6.4	8.6	0.8	1.6	4.5	3.8	8.4	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, SB and RB	1.0

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SWITCHING WAVEFORMS

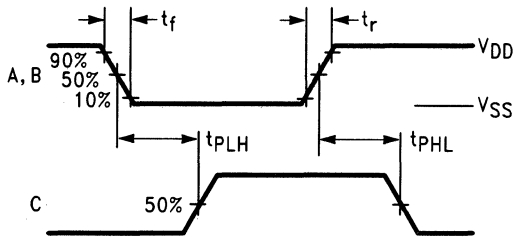


Figure 1

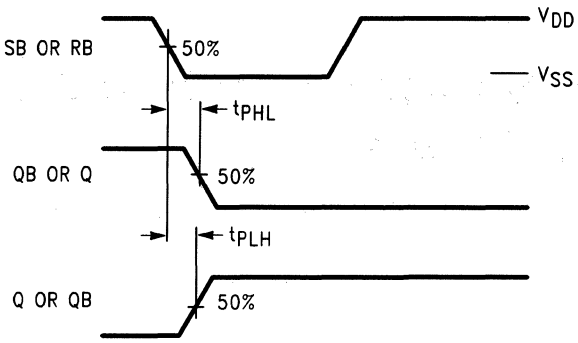


Figure 2

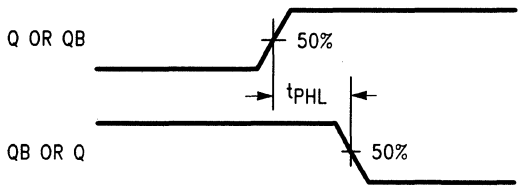
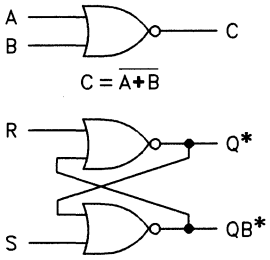


Figure 3

C013

NOR Latch and 2-Input NOR Gate



Primary Cells: 1
Netlist Format:
$SUBU C013
C Q QB / A B R S

FUNCTION TABLE

Inputs		Outputs	
S	R	Q	QB
L	L	No Change	
L	H	L	H
H	L	H	L
H	H	L*	L*

* Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously.

* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.6	1.2	3.0	3.6	5.6	1.0	1.6	4.2	4.6	7.8	ns
t_{PHL}		0.2	0.6	1.8	1.8	3.4	0.4	0.8	2.3	2.0	4.2	
t_{PLH}	Propagation Delay, S to Q (Figure 2)	1.4	2.2	5.6	6.0	10.4	1.1	2.8	7.7	5.6	14.2	ns
t_{PHL}	Propagation Delay, S to QB (Figure 2)	0.6	1.0	2.1	2.0	3.8	0.4	0.8	2.5	2.0	4.6	ns
t_{PHL}	Propagation Delay, R to Q (Figure 2)	0.6	1.0	1.9	2.0	3.6	0.4	0.8	2.5	2.0	4.6	ns
t_{PLH}	Propagation Delay, R to QB (Figure 2)	1.4	2.2	5.3	6.0	9.8	1.1	2.8	7.7	5.6	14.2	ns
t_{PLH}	Propagation Delay, Q to QB (Figure 3)	1.4	1.8	4.0	6.0	7.4	0.4	1.4	5.2	5.6	9.6	ns
t_{PLH}	Propagation Delay, QB to Q (Figure 3)	1.4	1.8	4.6	6.0	8.6	0.4	1.4	5.2	5.6	9.6	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pf. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A,B,S,R	1.0

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SWITCHING WAVEFORMS

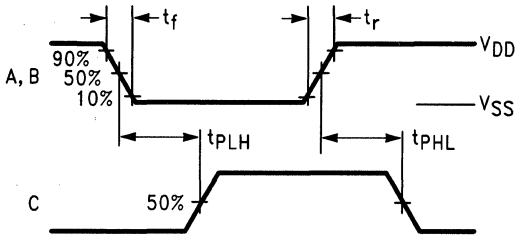


Figure 1

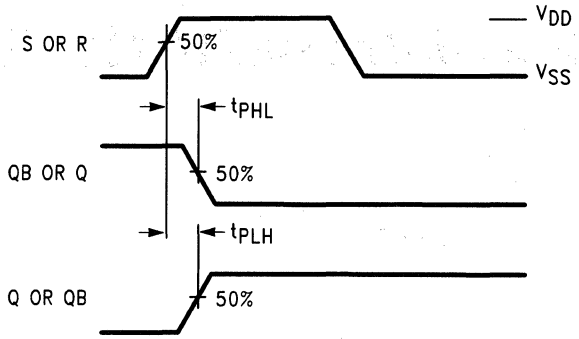


Figure 2

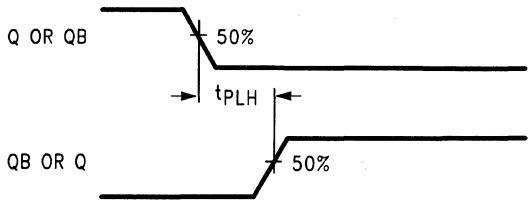
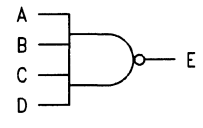


Figure 3

C017

Triple 4-Input NAND Gate

(1/3 OF MACROCELL)



$E = \overline{A \cdot B \cdot C \cdot D}$

Primary Cells: 2
Netlist Format:

```
$SUBU C017
E1 E2 E3 / A1 B1 C1 D1 A2 B2 &
C2 D2 A3 B3 C3 D3
```

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C, D to E (Figure 1)	0.2	0.4	1.9	1.8	3.6	0.6	1.2	3.0	2.4	5.4	ns
t_{PHL}		1.2	2.2	5.9	6.8	11.0	1.4	2.6	7.0	6.8	13.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C, D	1.0

SWITCHING WAVEFORMS

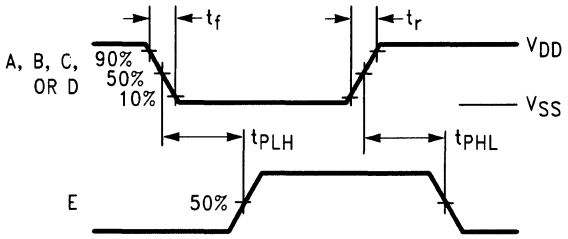


Figure 1

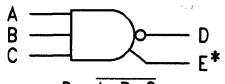
11

C019

Triple 3-Input NAND/AND Gate

Primary Cells: 2
Netlist Format:
$SUBU C019
D1 E1 D2 E2 D3 E3 / A1 B1 &
C1 A2 B2 C2 A3 B3 C3

(1/3 OF MACROCELL)



$D = \overline{A \cdot B \cdot C}$
$E = A \cdot B \cdot C$

* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B or C to D (Figure 1)	0.4	0.8	1.9	1.8	3.6	0.4	1.2	3.1	2.0	5.8	ns
t_{PHL}		1.2	1.6	4.5	4.8	8.4	0.9	2.0	5.6	5.2	10.4	
t_{PLH}	Propagation Delay, A, B or C to E (Figure 1)	0.4	2.6	7.5	2.7	13.8	0.6	3.4	9.7	3.2	18.0	ns
t_{PHL}		0.4	1.6	4.2	2.0	7.8	0.5	2.2	5.9	2.5	11.0	
t_{PLH}	Propagation Delay, D to E (Figure 2)	0.4	2.4	2.0	2.7	3.7	0.6	1.0	4.1	3.2	7.6	ns
t_{PHL}		0.4	0.4	1.7	2.0	3.2	0.5	1.0	2.8	2.5	5.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C	1.0

SWITCHING WAVEFORMS

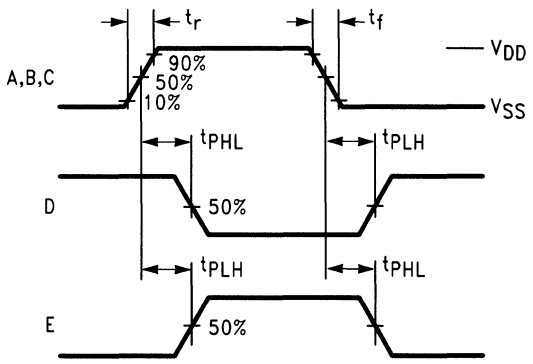


Figure 1

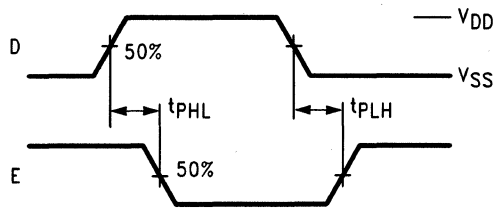


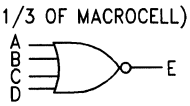
Figure 2

11

C020

Triple 4-Input NOR Gate

(1/3 OF MACROCELL)



$E = \overline{A+B+C+D}$

Primary Cells: 2
Netlist Format:

```
$SUBU C020
E1 E2 E3 / A1 B1 C1 D1 A2 B2 C2 D2 &
A3 B3 C3 D3
```

SWITCHING CHARACTERISTICS* ($C_L = 1$ pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C, D to E (Figure 1)	0.8	2.2	6.3	6.6	11.6	1.6	2.8	8.9	7.4	16.6	ns
t_{PHL}		0.4	1.0	2.2	2.2	4.0	0.4	1.0	2.5	2.4	4.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

SWITCHING WAVEFORMS

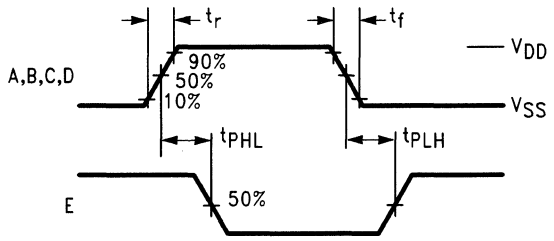


Figure 1

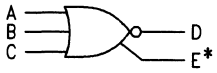
11

C022

Triple 3-Input NOR/OR Gate

Primary Cells: 2
Netlist Format:
$SUBU C022
D1 E1 D2 E2 D3 E3 / A1 B1 C1 &
A2 B2 C2 A3 B3 C3

(1/3 OF MACROCELL)



$D = \overline{A \cdot B \cdot C}$
$E = A \cdot B \cdot C$

* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

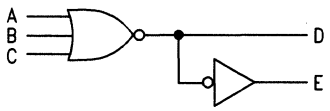
Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C to D (Figure 1)	1.1	1.8	4.9	5.6	9.0	1.2	2.4	7.5	6.8	13.8	ns
t_{PHL}		0.5	1.0	2.2	2.0	4.1	0.6	1.2	3.0	2.3	5.4	
t_{PLH}	Propagation Delay, A, B, C to E (Figure 1)	0.4	2.0	4.4	2.0	8.2	0.4	2.2	6.1	2.4	11.2	ns
t_{PHL}		0.4	2.8	8.2	2.7	15.2	0.4	3.8	11.4	3.2	21.0	
t_{PLH}	Propagation Delay, D to E (Figure 2)	0.4	0.8	2.2	2.0	2.8	0.4	1.0	3.1	2.4	5.8	ns
t_{PHL}		0.4	0.4	3.4	2.7	4.7	0.4	1.4	3.9	3.2	7.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C	1.0

FUNCTION DIAGRAM



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SWITCHING WAVEFORMS

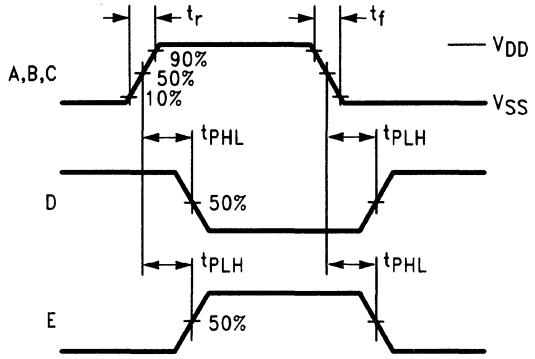


Figure 1

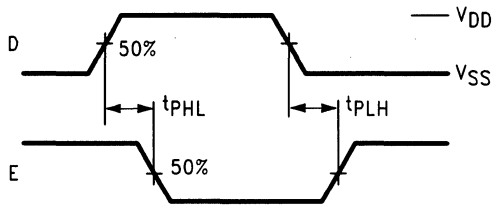
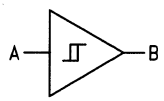


Figure 2

C025

Schmitt Trigger



Primary Cells: 1
Netlist Format:
$SUBU C025
B / A

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, voltages referenced to V_{SS})

Symbol	Parameter	Typical†	Unit
V_{T+} (Max)	Maximum Positive-Going Threshold Voltage (Figure 2)	3.4	V
V_{T-} (Min)	Minimum Negative-Going Threshold Voltage (Figure 2)	1.3	V
V_H (Max)	Maximum Hysteresis Voltage (Figure 2)	1.3	V

† These values are given to aid in calculating additional propagation delay due to RC time constants formed by loading capacitance and MOS transistor-on resistance. Because this Schmitt Trigger is an internal device and these values have been computer-calculated, these values are not guaranteed for test purposes.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.2	1.8	4.3	1.8	8.0	0.6	2.4	6.7	3.2	12.8	ns
t_{PHL}		0.6	1.6	4.3	2.0	8.0	0.6	2.6	7.1	2.8	13.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A	2.0

SWITCHING WAVEFORMS

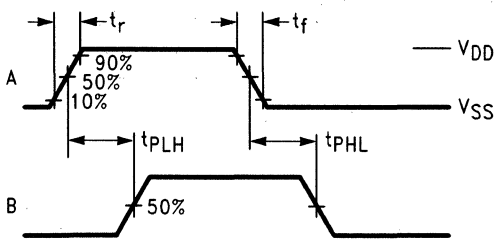


Figure 1

11

(a) A Schmitt Trigger squares up inputs with slow rise and fall times in cases where long metal connections may cause high RC delays.

(b) A Schmitt Trigger offers maximum noise immunity from internal switching noise.

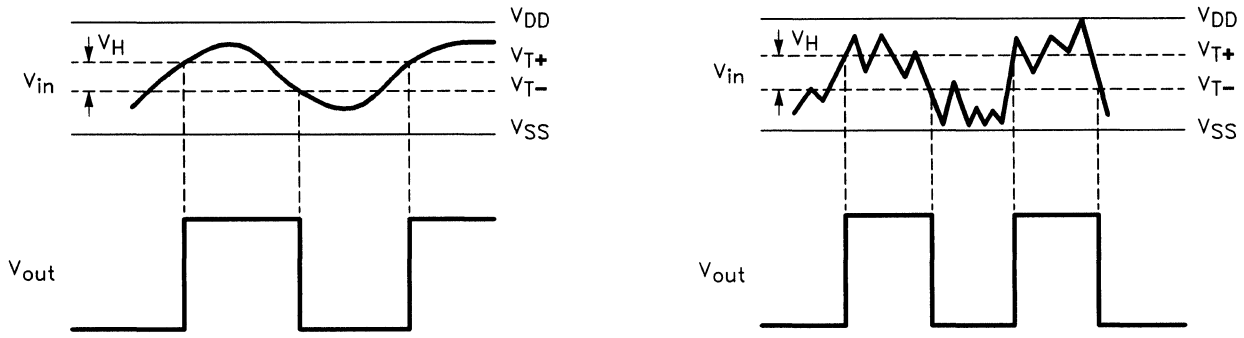
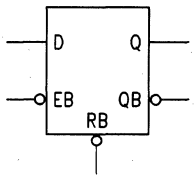


Figure 2. Typical Schmitt Trigger Applications

C026

D Latch with Reset(L) and Enable(L)



Primary Cells: 2
Netlist Format:
$SUBU C026
Q QB / D EB RB

FUNCTION TABLE

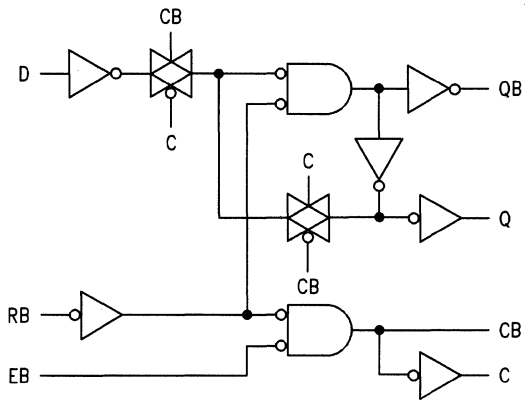
EB	D	RB	Q	QB
L	L	H	L	H
L	H	H	H	L
H	X	H	No Change	
X	X	L	L	H

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, D to Q (Figure 1)	0.4	1.8	5.2	2.2	9.6	0.6	2.8	8.0	2.6	15.4	ns
t_{PHL}		0.4	1.6	4.5	2.2	8.4	0.4	2.2	7.1	2.4	14.2	
t_{PLH}	Propagation Delay, D to QB (Figure 1)	0.4	1.4	3.9	2.0	7.2	0.6	2.6	6.9	2.9	13.0	ns
t_{PHL}		0.6	1.6	4.9	2.2	9.0	0.6	2.4	6.8	2.9	13.2	
t_{PHL}	Propagation Delay, RB to Q (Figure 2)	0.4	1.8	5.1	2.2	9.4	0.4	3.0	8.4	2.4	16.2	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 2)	0.4	1.4	4.8	2.2	7.0	0.6	2.2	6.2	2.9	12.0	ns
t_{PLH}	Propagation Delay, EB to Q (Figure 3)	0.4	2.2	6.5	2.2	12.0	0.6	3.4	9.9	2.6	19.4	ns
t_{PHL}		0.4	2.0	6.1	2.2	11.2	0.4	3.2	9.3	2.4	18.2	
t_{PLH}	Propagation Delay, EB to QB (Figure 3)	0.4	1.8	5.5	2.0	10.2	0.6	2.8	8.5	2.9	17.0	ns
t_{PHL}		0.6	2.0	6.2	2.2	11.4	0.6	3.0	8.8	2.9	17.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in ns/pF. See Section 4.

FUNCTION DIAGRAM



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TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85° C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to EB (Figure 4)	5.2	7.0	ns
t_h	Hold Time	EB to D (Figure 4)	1.2	1.0	ns
t_w	Pulse Width	RB (Figure 2) EB (Figure 4)	4.8 7.8	11.0 12.0	ns

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—D, RB, EB	1.0

SWITCHING WAVEFORMS

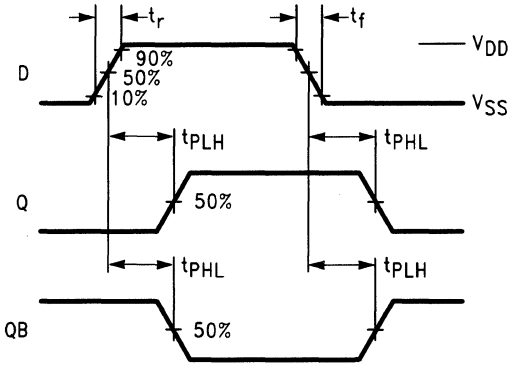


Figure 1

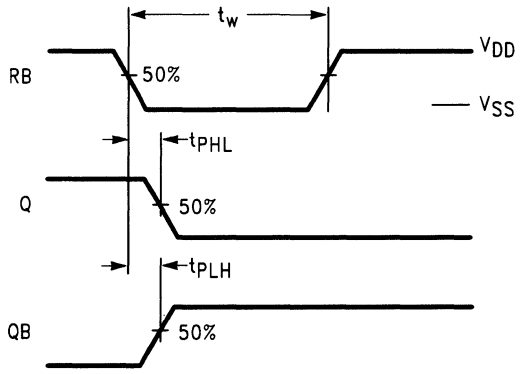


Figure 2

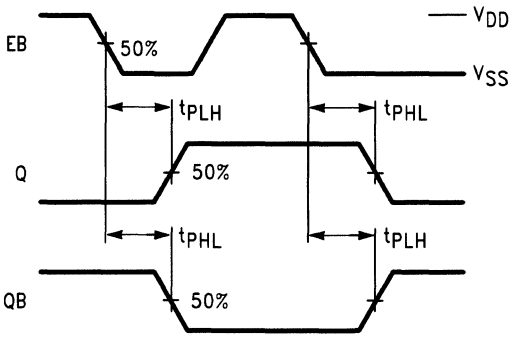


Figure 3

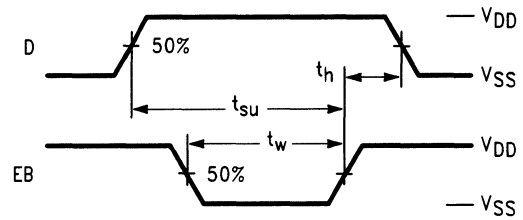


Figure 4

C027

Triple NAND Latch

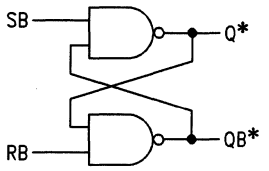
Primary Cells: 2
Netlist Format:
$SUBU C027
Q1 QB1 Q2 QB2 Q3 QB3 / &
SB1 RB1 SB2 RB2 SB3 RB3

FUNCTION TABLE

Inputs		Outputs	
SB	RB	Q	QB
L	L	H*	H*
L	H	H	L
H	L	L	H
H	H	No Change	

* Both outputs will remain high as long as SB and RB are low, but the output states are unpredictable if SB and RB go high simultaneously.

(1/3 OF MACROCELL)



* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, SB to Q (Figure 1)	0.4	0.8	1.8	2.0	3.4	0.6	1.0	2.7	2.4	5.0	ns
t_{PHL}	Propagation Delay, SB to QB (Figure 1)	1.4	2.2	5.4	6.6	10.0	0.8	2.6	7.1	3.8	13.4	ns
t_{PHL}	Propagation Delay, RB to Q (Figure 1)	1.4	2.2	5.4	6.6	10.0	0.8	2.6	7.1	3.8	13.4	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 1)	0.4	0.8	1.8	2.0	3.4	0.6	1.0	2.7	2.4	5.0	ns
t_{PHL}	Propagation Delay, Q to QB (Figure 2)	1.4	1.8	6.6	6.6	8.6	0.8	1.6	4.5	3.8	8.4	ns
t_{PHL}	Propagation Delay, QB to Q (Figure 2)	1.4	1.8	2.0	6.6	8.6	0.8	1.6	4.5	3.8	8.4	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pf. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—SB, RB	1.0

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SWITCHING WAVEFORMS

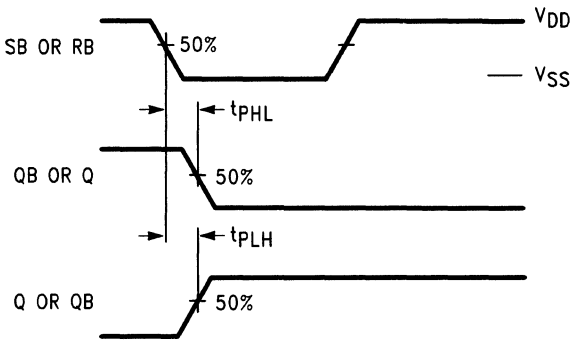


Figure 1

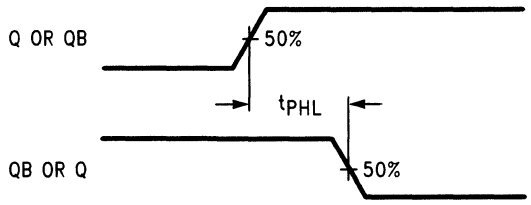
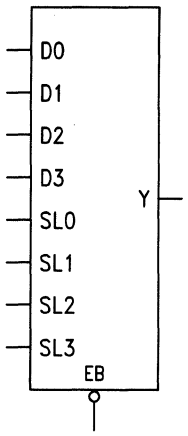


Figure 2

C028

4-to-1 Multiplexer with 3-State Output



Primary Cells: 3
Netlist Format:
$SUBU C028
Y / D0 D1 D2 D3 SL0 SL1 &
SL2 SL3 EB

Pin Names:
D0–D3—Data Inputs
SL0–SL3—Select Inputs
EB—Output Enable Bar

FUNCTION TABLE

EB	SL0	SL1	SL2	SL3	Y
L	H	L	L	L	D0
L	L	H	L	L	D1
L	L	L	H	L	D2
L	L	L	L	H	D3
H	X	X	X	X	Z

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, D0–D3, SL0–SL3 to Y (Figures 1 and 2)	0.4	1.8	4.6	2.0	8.6	0.6	2.8	8.4	3.0	15.6	ns
t_{PHL}		0.4	1.8	5.1	2.0	9.4	0.6	3.0	8.4	2.6	15.6	
t_{PLZ}	Propagation Delay, EB to Y (Figure 3)	—	1.0	2.6	—	4.8	—	3.0	3.7	—	7.8	ns
t_{PHZ}		—	0.8	1.8	—	3.4	—	3.0	5.2	—	5.6	
t_{PZL}		0.4	1.8	4.8	2.0	8.8	0.6	3.0	5.2	2.6	11.4	
t_{PZH}		0.4	1.6	3.9	2.0	7.2	0.6	3.0	5.2	3.0	10.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—D0–D3, SL0–SL3, EB	1.0

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SWITCHING WAVEFORMS

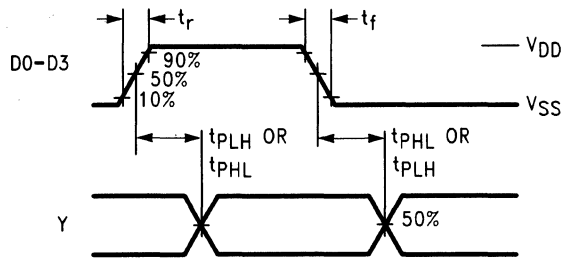


Figure 1

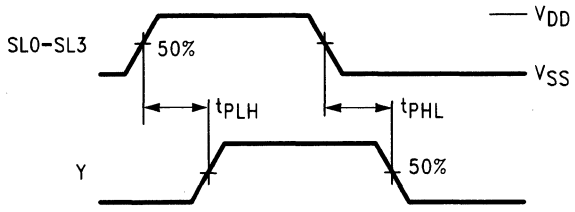


Figure 2

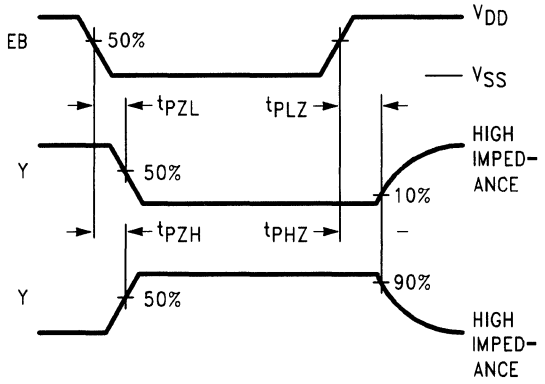
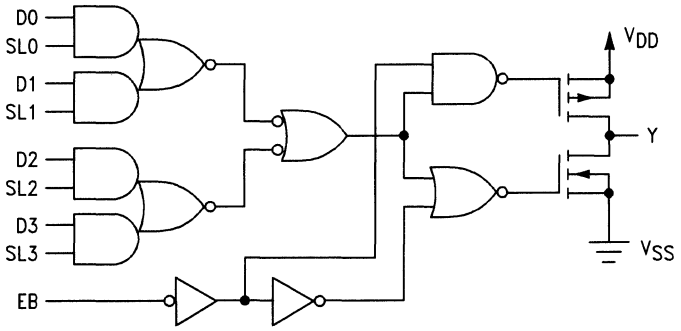


Figure 3
Refer to Figure 7 in Section 9.

FUNCTION DIAGRAM



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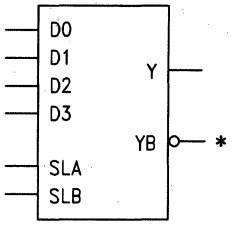
C029

4-to-1 Data Multiplexer

Primary Cells: 3
Netlist Format:
$SUBU C029
Y YB / D0 D1 D2 D3 SLA SLB

Pin Names:
D—Data In
SLA—Select A (LSB)
SLB—Select B (MSB)
Y—Data Out
YB—Data Out Bar



*This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

FUNCTION TABLE

SLB	SLA	Y	YB
L	L	D0	$\overline{D0}$
L	H	D1	$\overline{D1}$
H	L	D2	$\overline{D2}$
H	H	D3	$\overline{D3}$

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, any D to Y (Figure 1)	0.4	1.6	4.3	1.2	8.0	0.4	2.2	6.8	2.0	13.6	ns
t_{PHL}		0.4	1.6	4.4	1.4	8.2	0.4	2.2	6.8	2.0	13.6	
t_{PLH}	Propagation Delay, any D to YB (Figure 1)	0.4	2.0	5.6	1.4	10.4	0.4	2.8	8.4	2.0	16.6	ns
t_{PHL}		0.4	2.0	5.6	1.4	10.4	0.4	2.8	8.4	2.0	16.6	
t_{PLH}	Propagation Delay, SLA to Y (Figure 1)	0.4	1.8	5.5	1.2	10.0	0.4	3.0	8.8	2.0	17.2	ns
t_{PHL}		0.4	1.8	5.5	1.4	10.2	0.4	3.0	8.8	2.0	17.2	
t_{PLH}	Propagation Delay, SLA to YB (Figure 1)	0.4	2.4	6.7	1.4	12.4	0.4	3.6	10.4	2.0	20.2	ns
t_{PHL}		0.4	2.4	6.7	1.4	12.4	0.4	3.6	10.4	2.0	20.2	
t_{PLH}	Propagation Delay, SLB to Y (Figure 1)	0.4	1.6	4.1	1.2	7.6	0.4	2.2	6.7	2.0	13.2	ns
t_{PHL}		0.4	1.6	4.3	1.4	8.0	0.4	2.2	6.7	2.0	13.2	
t_{PLH}	Propagation Delay, SLB to YB (Figure 1)	0.4	2.0	5.5	1.4	10.2	0.4	2.8	8.3	2.0	16.2	ns
t_{PHL}		0.4	2.0	5.4	1.4	10.0	0.4	2.8	8.3	2.0	16.2	
t_{PLH}	Propagation Delay, Y to YB (Figure 2)	0.4	0.8	1.8	1.4	3.4	0.4	0.6	1.6	2.0	3.0	ns
t_{PHL}		0.4	0.8	1.8	1.4	3.4	0.4	0.6	1.6	2.0	3.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in ns/pF. See Section 4.

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INPUT LOAD FACTORS

IUL	Input Unit Load Factors—D0, D1, D2, D3, SLA, SLB	1.0

SWITCHING WAVEFORMS

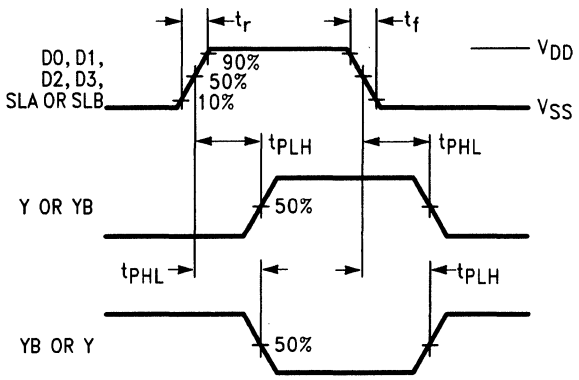


Figure 1

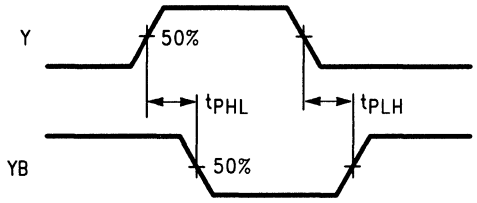
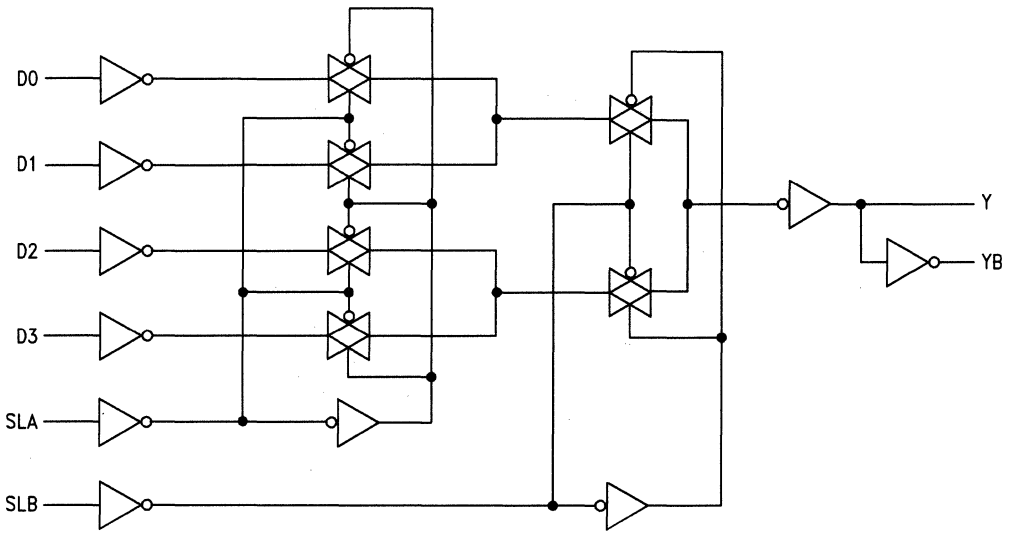


Figure 2

FUNCTION DIAGRAM



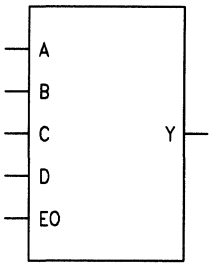
11

C030

4-Bit Parity Checker

Primary Cells: 3
Netlist Format:
$SUBU C030
Y / A B C D EO

Pin Names:
A, B, C, D—Data Inputs
EO—Even/Odd Parity Select
Y—Parity Output



FUNCTION TABLE

Input EO	Number of inputs A through D that are high	Output Y
L	0, 2, 4	H
	1, 3	L
H	0, 2, 4	L
	1, 3	H

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C, D to Y (Figure 1)	0.8	1.8	7.2	4.0	13.4	0.8	5.2	14.1	3.6	24.4	ns
t_{PHL}		1.0	2.6	8.6	5.0	16.0	0.8	5.2	14.1	3.6	24.8	
t_{PLH}	Propagation Delay, EO to Y (Figure 1)	0.8	1.4	3.7	4.0	6.8	0.8	2.2	5.9	3.6	11.4	ns
t_{PHL}		1.0	1.6	3.9	5.0	7.2	0.8	2.2	5.9	3.6	12.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(1\ pF) + K(C_L - 1pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C, D, EO	1.0

SWITCHING WAVEFORMS

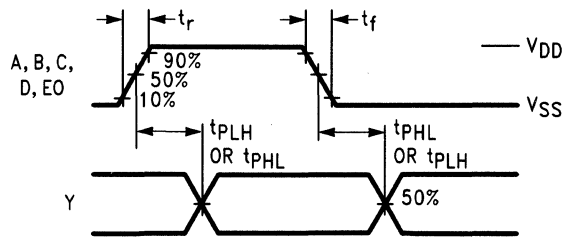
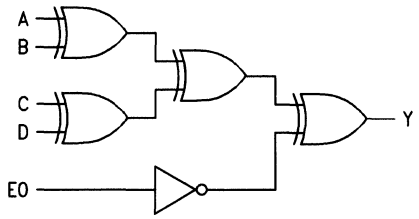
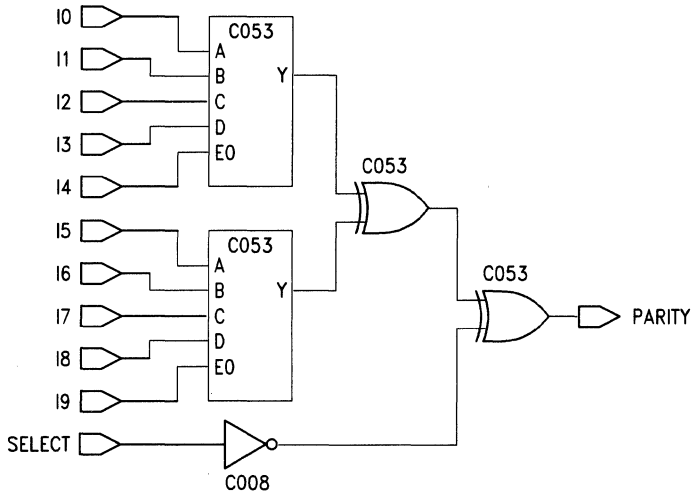


Figure 1

LOGIC DIAGRAM



10-BIT PARITY GENERATOR EXAMPLE



Function Table

Input Select	Sum of Inputs I0 through I9	Output Parity
Low	Even	High
	Odd	Low
High	Even	Low
	Odd	High

C031

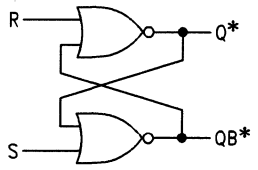
Triple NOR Latch

Primary Cells: 2
Netlist Format:
$SUBU C031
Q1 QB1 Q2 QB2 Q3 QB3 / &
R1 S1 R2 S2 R3 S3

FUNCTION TABLE

S	R	Q	QB
L	L	NO CHG	
L	H	L	H
H	L	H	L
H	H	L*	L*

*Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously.



*This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, S to Q (Figure 1)	1.6	2.4	6.4	6.6	11.8	1.1	2.8	7.7	5.6	14.2	ns
t_{PHL}	Propagation Delay, S to QB (Figure 1)	0.4	1.2	2.8	2.0	5.2	0.4	0.8	2.5	2.0	4.6	ns
t_{PHL}	Propagation Delay, R to Q (Figure 1)	0.4	1.2	2.9	2.0	5.4	0.4	0.8	2.5	2.0	4.6	ns
t_{PLH}	Propagation Delay, R to QB (Figure 1)	1.6	2.4	6.4	6.6	11.8	1.1	2.8	7.7	5.6	14.2	ns
t_{PLH}	Propagation Delay, Q to QB (Figure 2)	1.6	1.6	4.6	6.6	7.8	1.1	2.4	5.2	5.6	9.6	ns
t_{PLH}	Propagation Delay, QB to Q (Figure 2)	1.6	1.6	4.6	6.6	7.8	1.1	2.4	5.2	5.6	9.6	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—R, S	1.0

SWITCHING WAVEFORMS

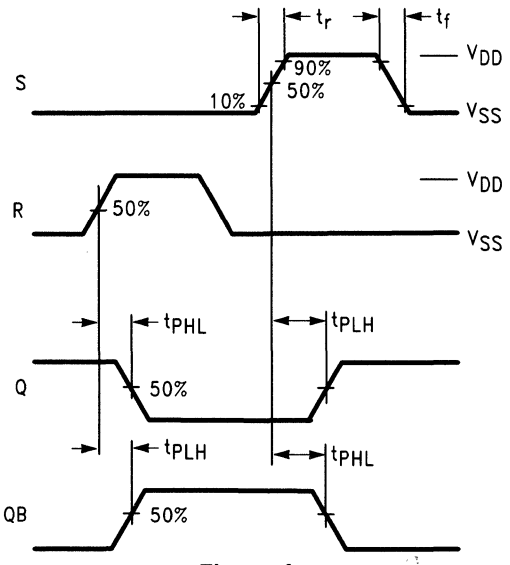


Figure 1

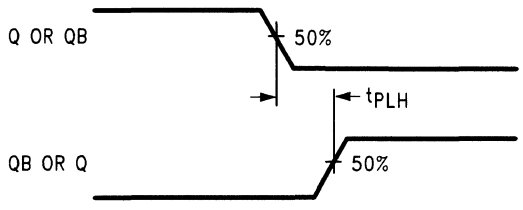
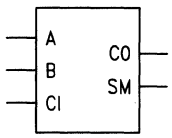


Figure 2

11

C032

Full Adder



Primary Cells: 3
Netlist Format:
$SUBU C032
CO SM / A B CI

Pin Names:
A, B—Binary Data Inputs
CI—Carry In
CO—Carry Out
SM—Sum Output

FUNCTION TABLE

A	B	CI	SM	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to CO (Figure 1)	0.4	2.6	6.8	2.0	12.6	0.8	4.8	13.5	3.2	26.0	ns
t_{PHL}		0.6	2.6	7.9	2.4	14.6	0.8	4.8	13.5	3.2	26.0	
t_{PLH}	Propagation Delay, A, B to SM (Figure 1)	0.4	2.8	7.9	2.0	14.6	0.8	4.0	12.1	4.2	24.0	ns
t_{PHL}		0.4	3.0	7.9	2.0	14.6	0.8	4.0	12.1	4.2	24.0	
t_{PLH}	Propagation Delay, CI to CO (Figure 1)	0.4	1.6	4.3	2.0	8.0	0.8	2.4	6.4	3.2	12.0	ns
t_{PHL}		0.6	1.6	4.3	2.4	8.0	0.8	2.4	6.4	3.2	12.0	
t_{PLH}	Propagation Delay, CI to SM (Figure 1)	0.4	1.8	4.6	2.0	8.6	0.8	2.4	6.7	4.2	13.0	ns
t_{PHL}		0.4	2.0	5.0	2.0	9.2	0.8	2.4	6.7	4.2	13.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, CI	1.0

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SWITCHING WAVEFORMS

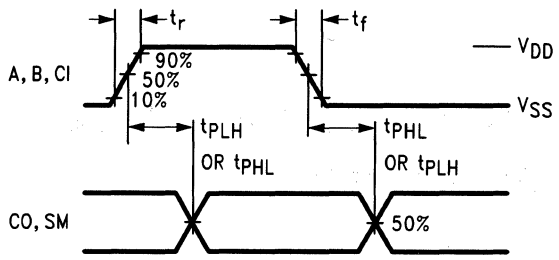
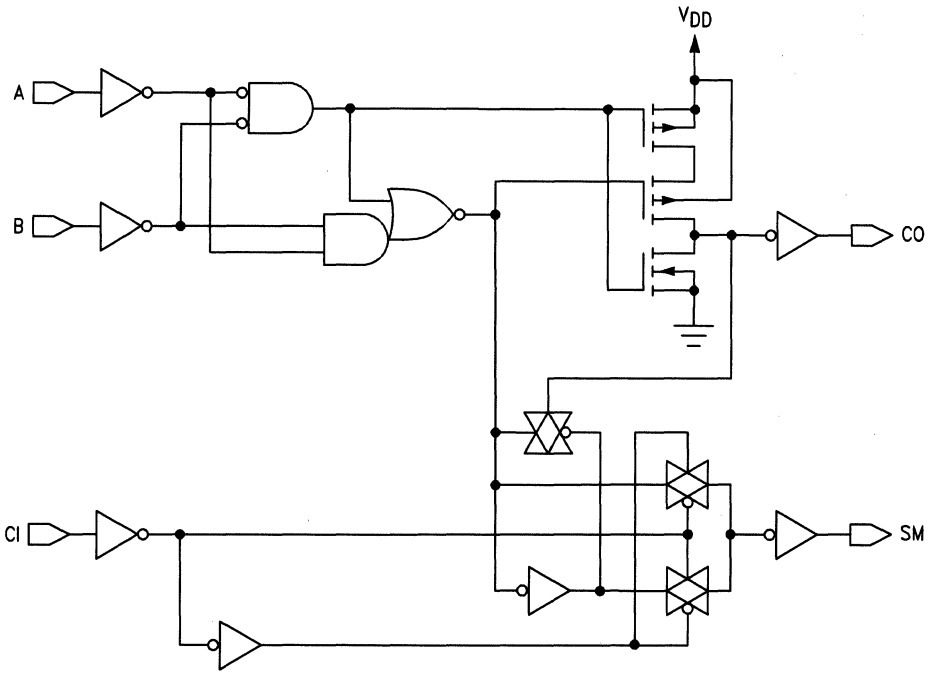


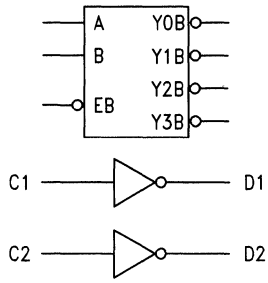
Figure 1

FUNCTION DIAGRAM



C033

1-of-4 Decoder With Active-Low Outputs and 2 Inverters



Primary Cells: 4
Netlist Format:
$SUBU C033
Y0B Y1B Y2B Y3B D1 D2 / A B &
EB C1 C2

Pin Names:
A, B—Inputs A=LSB B=MSB
EB—Active Low Enable
Y0B–Y3B—Active-Low Decoded Outputs
C1, C2—Inverter Inputs
D1, D2—Inverter Outputs

FUNCTION TABLE

A	B	EB	Y0B	Y1B	Y2B	Y3B
X	X	H	H	H	H	H
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A,B to Y3B, (3 levels) (Figure 1) A to Y1B, B to Y2R	0.4	1.2	3.5	1.8	6.4	0.6	2.2	5.9	2.8	11.0	ns
t_{PHL}		0.8	2.0	5.3	3.4	9.8	0.7	2.6	7.5	4.0	14.6	
t_{PLH}	Propagation Delay, A,B to Y0B–Y2B (4 levels) (Figure 1)	0.4	1.6	4.6	1.8	8.6	0.6	2.6	7.4	2.8	14.4	ns
t_{PHL}		0.8	2.2	6.7	3.4	12.4	0.7	3.4	9.5	4.0	18.4	
t_{PLH}	Propagation Delay, EB to Y0B–Y3B (Figure 2)	0.4	1.4	3.2	1.8	6.0	0.6	1.6	4.5	2.8	8.8	ns
t_{PHL}		0.8	1.6	4.1	3.4	7.6	0.7	2.0	5.7	4.0	11.0	
t_{PLH}	Propagation Delay, C to D (Figure 1)	0.4	0.8	1.7	1.8	3.2	0.4	0.8	2.4	2.6	4.6	ns
t_{PHL}		0.4	0.8	1.8	1.8	3.4	0.4	0.8	2.1	2.0	4.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, EB and C	1.0

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SWITCHING WAVEFORMS

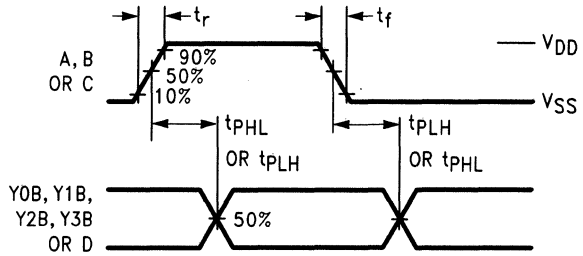


Figure 1

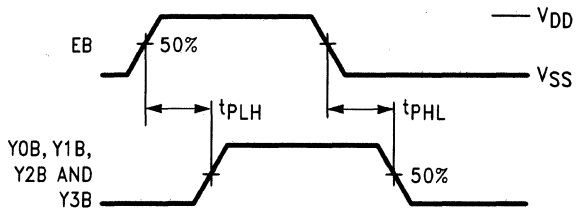
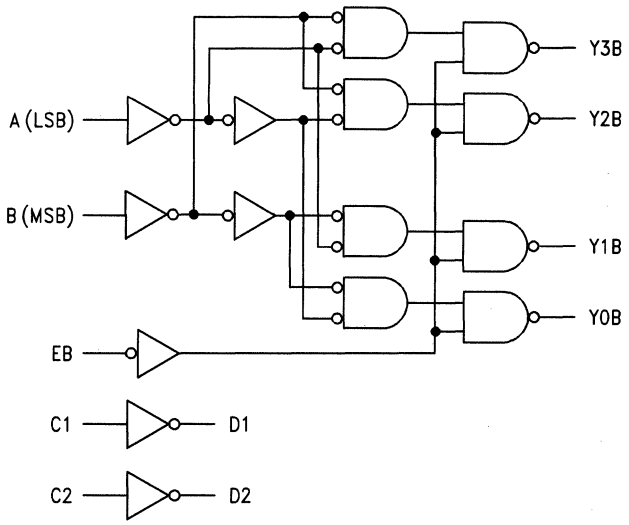


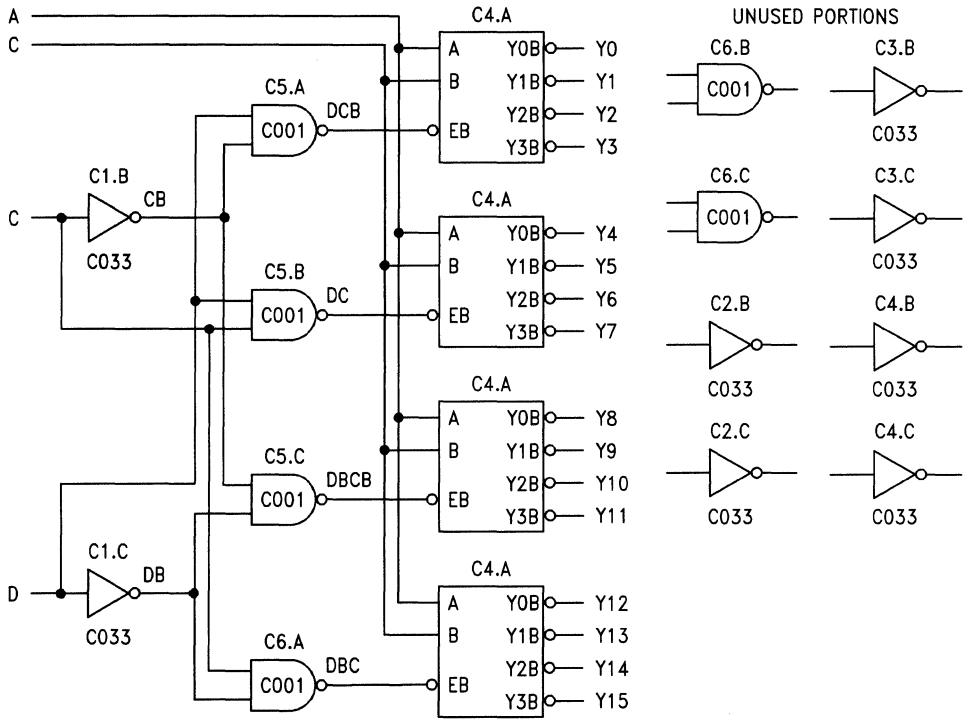
Figure 2

LOGIC DIAGRAM



POSSIBLE APPLICATION

1-of-16 Decoder w/ Outputs (L)
18 Cells

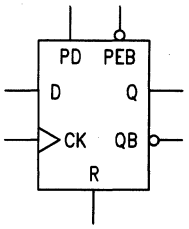


NETLIST FORMAT:

```
$$
$SUBU C033
Y0 Y1 Y2 Y3 CB DB / A B DCB C D
$SUBU C033
Y4 Y5 Y6 Y7 * * / A B DC * *
$SUBU C033
Y8 Y9 Y10 Y11 * * / A B DBCB * *
$SUBU C033
Y12 Y13 Y14 Y15 * * / A B DBC * *
$SUBU C001
DCB DC DBCB / D CB D C CB DB
$SUBU C001
DBC * * / C DB * * * *
$$
```

C034

Parallel Load D Flip-Flop with Reset



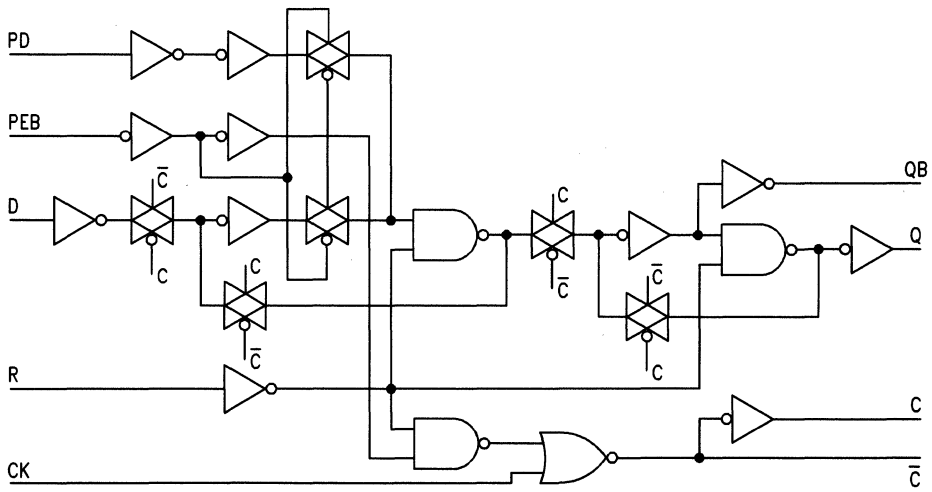
Primary Cells: 4
Netlist Format:
$SUBU C034
Q QB / PEB PD D CK R

Pin Names:
PEB—Preset Enable Bar
PD—Preset Data
D—Data In
CK—Clock
R—Reset
Q—Data Out
QB—Data Out Bar

FUNCTION TABLE

CK	R	PEB	D	Q	QB	Function Description
X	H	X	X	L	H	Reset flip-flop output Q low. R overrides CK and PEB inputs.
X	L	L	X	PD	$\overline{PD}$	Data at the PD input is loaded asynchronously into the flip-flop. The flip-flop is disabled while PEB = L.
⌐	L	H	L	L	H	Data at the D input is loaded into the flip-flop on the rising edge of the clock.
⌐	L	H	H	H	L	
¬	L	H	X	No Change	No Change	Outputs are not affected on the falling edge of the clock.

FUNCTION DIAGRAM



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SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	55	—	—	—	—	35	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	2.4	7.1	2.2	13.2	0.6	4.4	12.6	2.8	24.4	ns
t_{PHL}		0.6	2.0	5.8	2.2	10.8	0.6	3.6	10.3	2.2	20.0	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	1.8	5.0	2.2	9.2	0.6	3.0	8.8	2.8	17.2	ns
t_{PHL}		0.4	2.0	5.8	2.2	10.8	0.6	3.4	9.9	2.6	19.4	
t_{PHL}	Propagation Delay, R to Q (Figure 2)	0.6	1.4	4.3	2.2	8.0	0.6	2.4	6.5	2.2	12.4	ns
t_{PLH}	Propagation Delay, R to QB (Figure 2)	0.4	2.6	5.6	2.2	13.9	0.6	3.2	9.2	2.8	17.8	ns
t_{PLH}	Propagation Delay, PEB to Q (Figure 5)	0.4	3.6	10.6	2.2	19.6	0.6	6.2	17.5	2.8	34.0	ns
t_{PHL}		0.6	3.0	9.8	2.2	16.2	0.6	5.6	15.4	2.2	29.6	
t_{PLH}	Propagation Delay, PEB to QB (Figure 5)	0.4	2.6	7.9	2.2	14.6	0.6	5.0	13.9	2.8	26.8	ns
t_{PHL}		0.4	3.2	9.2	2.2	17.0	0.6	5.4	15.0	2.6	29.0	
t_{PLH}	Propagation Delay, PD to Q (Figure 3)	0.4	3.0	9.6	2.2	17.8	0.6	5.6	15.9	2.8	31.0	ns
t_{PHL}		0.6	2.6	7.9	2.2	14.6	0.6	4.8	13.7	2.2	26.6	
t_{PLH}	Propagation Delay, PD to QB (Figure 3)	0.4	2.4	7.0	2.2	13.0	0.6	4.2	12.2	2.8	23.8	ns
t_{PHL}		0.4	2.8	8.3	2.2	15.4	0.6	4.6	13.3	2.6	26.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85° C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to CK (Figure 4)	4.8	9.0	ns
		PD to PEB (Figure 6)	8.8	12.0	
t_h	Hold Time	CK to D (Figure 4)	2.8	4.0	ns
		PEB to PD (Figure 6)	0.6	4.0	
t_{rec}	Recovery Time	R to CK (Figure 2)	16.2	23.0	ns
		PEB to CK (Figure 5)	17.8	25.0	
t_w	Pulse Width	CK, $t_{w(L)}$ (Figure 1)	9.0	16.0	ns
		CK, $t_{w(H)}$ (Figure 1)	4.4	16.0	
		R (Figure 2)	8.8	13.0	
		PEB (Figure 5)	10.4	15.0	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—PEB, PD, D, CK, R	1.0

SWITCHING WAVEFORMS

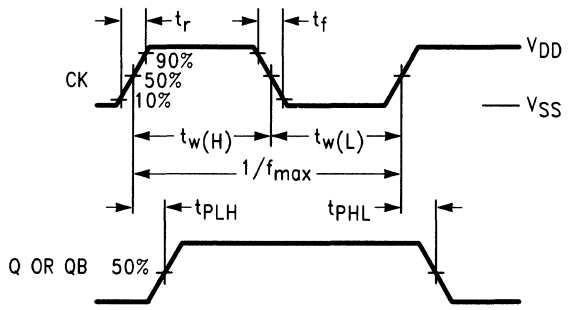


Figure 1

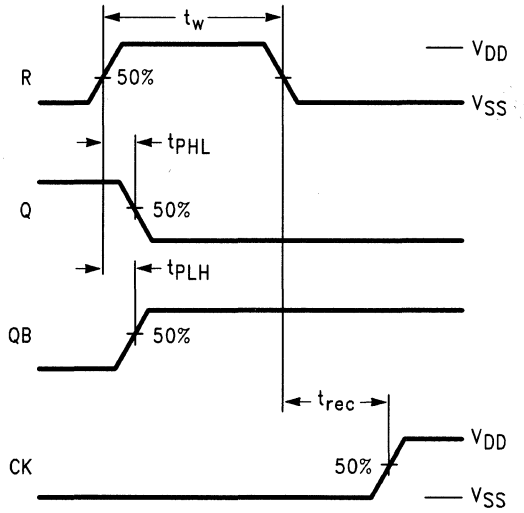


Figure 2

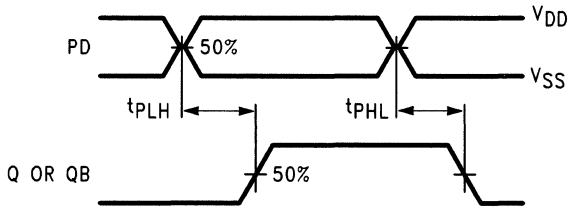


Figure 3

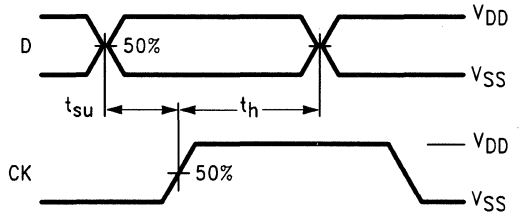


Figure 4

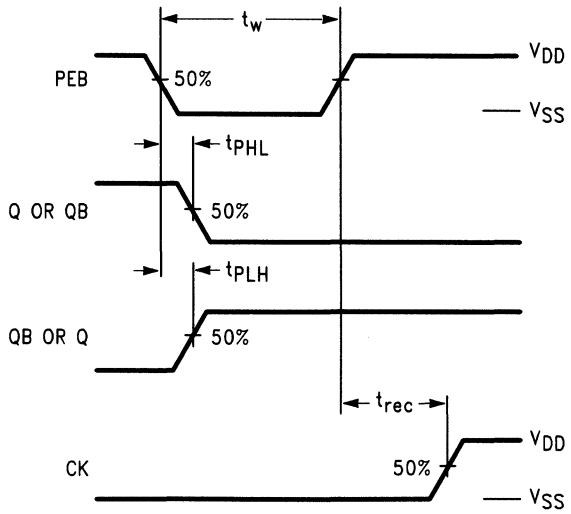


Figure 5

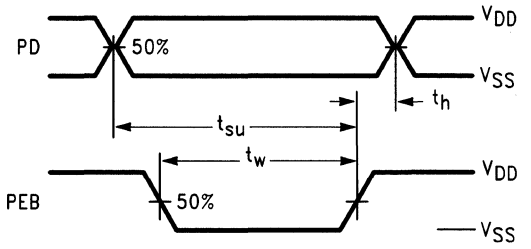
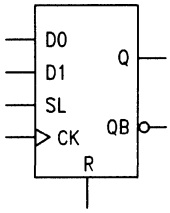


Figure 6

C035

Multiplexed D Flip-Flop with Reset (L)



Primary Cells: 4
Netlist Format:
$SUBU C035
Q QB / D0 D1 SL CK R

Pin Names:
CK—Clock
R—Reset
SL—Select
D0,D1—Data Inputs
Q1, QB—Data Outputs

FUNCTION TABLE

CK	R	SL	D1	D0	Q	QB	Function Performed
X	H	X	X	X	L	H	Reset Outputs
↗	L	L	X	X	D1	$\overline{D1}$	Data from D1 goes to Outputs
↗	L	H	X	X	D0	$\overline{D0}$	Data from D0 goes to Outputs
↘	L	X	X	X	No Change		None

X=Don't Care

SWITCHING CHARACTERISTICS* (C_L=1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	59	—	—	—	—	33	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	2.4	7.0	1.2	13.0	0.4	4.6	13.3	3.0	23.0	ns
t_{PHL}		0.4	2.8	7.2	2.0	13.4	0.4	4.6	11.8	2.0	21.6	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	2.4	6.3	2.0	11.6	0.4	3.6	9.9	2.0	18.8	ns
t_{PHL}		0.4	2.2	5.8	2.2	10.8	0.4	3.6	10.6	2.0	19.4	
t_{PHL}	Propagation Delay, R to Q (Figure 2)	0.4	3.0	7.6	2.0	14.0	0.4	3.6	12.2	2.0	22.8	ns
t_{PLH}	Propagation Delay, R to QB (Figure 2)	0.4	2.6	6.6	2.0	12.2	0.4	3.6	11.0	2.0	20.0	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD}=4.5 to 5.5 V, T_A=−40° to +85°C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D0,D1 to CK (Figure 3)	8.8	11.0	ns
		SL to CK (Figure 3)	8.8	16.0	
t_h	Hold Time	CK to D0,D1 (Figure 3)	2.4	10.0	ns
		CK to SL (Figure 3)	2.4	8.0	
t_{rec}	Recovery Time	R to CK (Figure 2)	7.0	14.0	ns
t_w	Pulse Width	CK, $t_{w(L)}$ (Figure 1)	9.0	17.0	ns
		CK, $t_{w(H)}$ (Figure 1)	9.0	17.0	
		R (Figure 2)	7.0	13.0	

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INPUT LOAD FACTORS

IUL	Input Unit Load Factors—D0,SL,D1,CK and R	1.0

SWITCHING WAVEFORMS

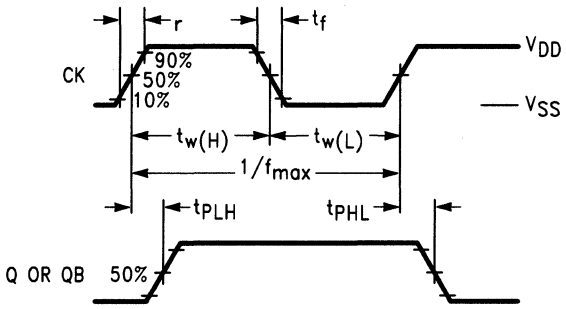


Figure 1

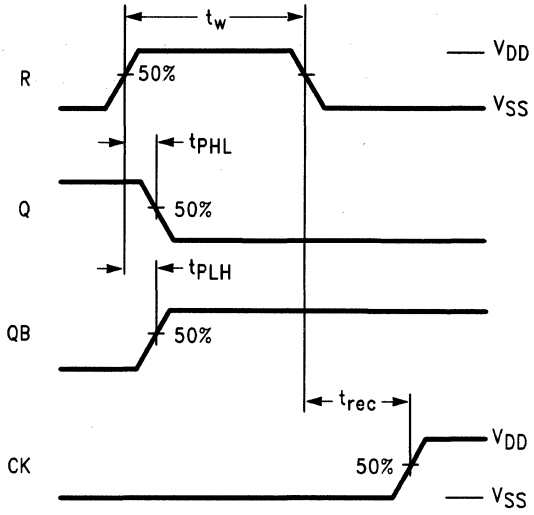


Figure 2

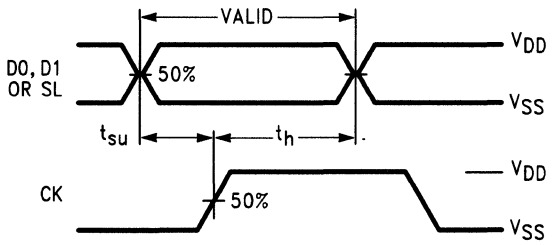
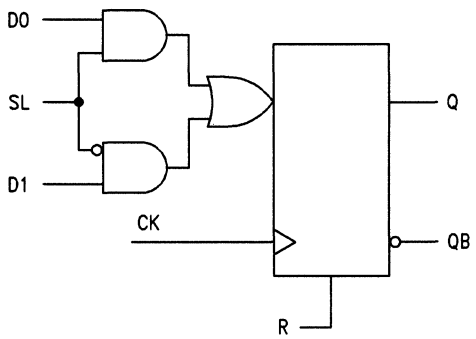


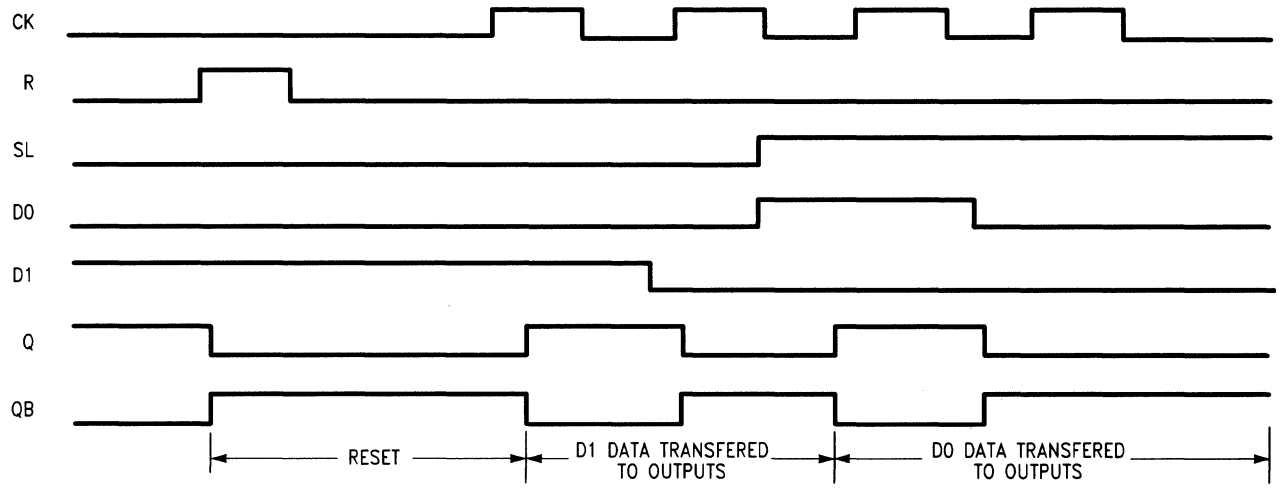
Figure 3

LOGIC DIAGRAM

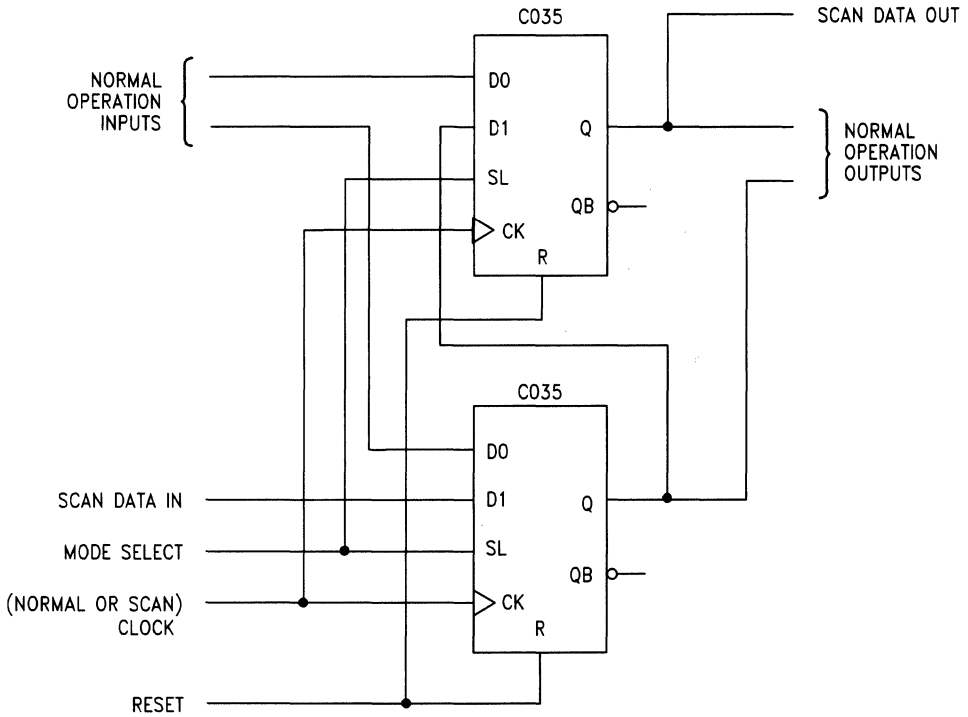


11

TIMING DIAGRAM

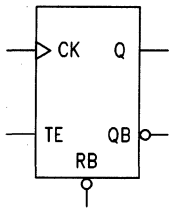


LSSD EXAMPLE USING C035



C036

Toggle Enable Flip-Flop With Reset (L)



Primary Cells: 4
Netlist Format:
$SUBU C036
Q QB / CK TE RB

Pin Names:
CK—Clock Input
TE—Toggle Enable Input
RB—Reset Bar Input
Q, QB—Data Outputs

FUNCTION TABLE

RB	TE	CK	Q	QB
L	X	X	L	H
H	H	↗	Outputs Toggle	
H	X	↘	No Change	
H	L	↗	No Change	

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% duty cycle)	—	—	—	—	—	—	—	—	—	40	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	2.6	7.9	2.0	14.6	0.6	4.6	14.1	1.7	24.8	ns
t_{PHL}		0.4	2.6	7.9	2.0	14.6	0.7	4.4	13.2	2.3	23.2	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	2.4	7.0	2.0	13.0	0.7	3.8	11.8	2.6	19.8	ns
t_{PHL}		0.4	2.4	7.2	2.0	13.4	0.6	4.0	12.1	2.2	21.4	
t_{PHL}	Propagation Delay, RB to Q (Figure 2)	0.4	2.6	7.5	2.0	13.8	0.7	4.2	12.8	2.3	23.0	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 2)	0.4	2.0	5.8	2.0	10.8	0.7	3.8	11.1	2.6	19.8	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$ for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5V, T_A = −40 to +85°C)

Symbol	Parameter		HCA6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	TE to CK (Figure 3)	7.6	11.0	ns
t_h	Hold Time	CK to TE (Figure 3)	0.0	1.0	ns
t_{rec}	Recovery Time	RB to CK (Figure 2)	9.8	17.0	ns
t_w	Pulse Width	CK, $t_{w(L)}$ (Figure 1)	6.8	13.0	ns
		CK, $t_{w(H)}$ (Figure 1)	7.4	13.0	
		RB (Figure 2)	4.8	10.0	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—CK, TE, RB	1.0

SWITCHING WAVEFORMS

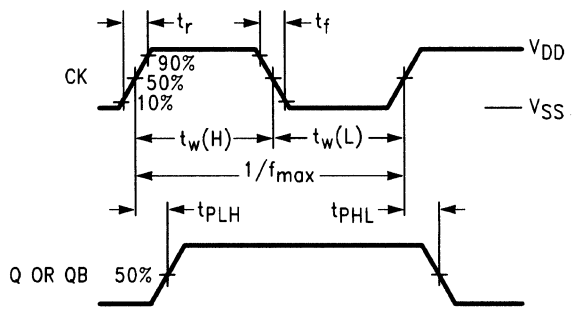


Figure 1

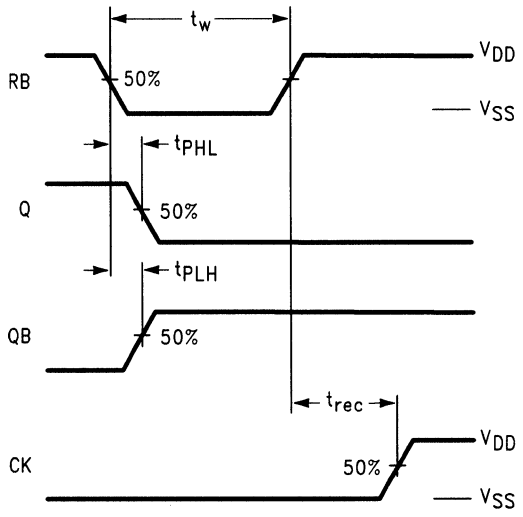


Figure 2

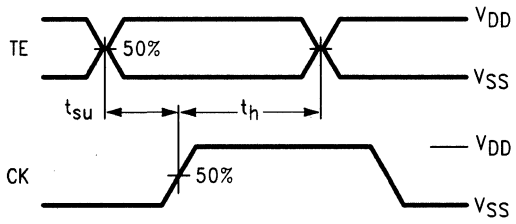
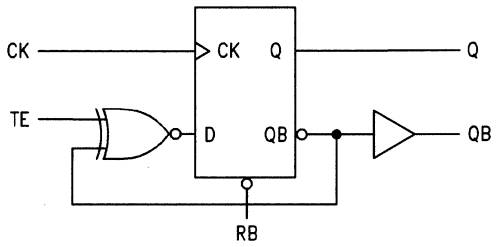


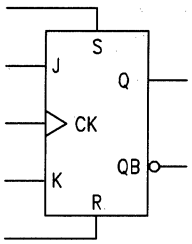
Figure 3

FUNCTION DIAGRAM



C037

J-K Flip-Flop with Reset & Set



Primary Cells: 5
Netlist Format:
$SUBU C037
Q QB / S J CK K R

FUNCTION TABLE

R	S	CK	J	K	Q	QB
H	L	X	X	X	L	H
L	H	X	X	X	H	L
L	L	↗	L	L	No Change	
L	L	↗	L	H	L	H
L	L	↗	H	L	H	L
L	L	↗	H	H	Toggle	
L	L	↘	X	X	No Change	
H	H	X	X	X	L*	L*

* Both outputs will remain low as long as Set and Reset are high, but the output states are unpredictable if Set and Reset go low simultaneously.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	60	—	—	—	—	35	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	2.2	6.5	2.4	12.0	0.6	4.0	11.9	3.8	21.0	ns
t_{PHL}		0.6	2.2	6.3	2.4	11.6	0.4	3.4	10.4	3.0	19.2	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	2.6	7.7	2.4	14.2	0.6	4.4	12.9	3.2	23.6	ns
t_{PHL}		0.4	2.6	7.4	2.2	13.6	0.4	4.2	12.2	2.4	22.2	
t_{PHL}	Propagation Delay, R to Q (Figure 2)	0.6	1.6	4.5	2.4	8.4	0.4	2.4	6.7	3.0	13.6	ns
t_{PLH}	Propagation Delay, R to QB (Figure 2)	0.4	2.0	6.1	2.4	11.2	0.6	3.2	9.5	3.2	19.6	ns
t_{PLH}	Propagation Delay, S to Q (Figure 2)	0.4	2.6	7.8	2.4	14.4	0.6	3.8	11.0	3.8	21.4	ns
t_{PHL}	Propagation Delay, S to QB (Figure 2)	0.4	1.4	4.4	2.2	8.2	0.4	2.4	6.6	2.4	12.2	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—J, K, CK, S and R	1.0

11

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85° C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	J or K to CK (Figure 3)	9.0	17.0	ns
t_h	Hold Time	CK to J or K (Figure 3)	0.0	1.0	ns
t_{rec}	Recovery Time	R to CK (Figure 3) S to CK (Figure 2)	15.2 15.0	21.0 23.0	ns
t_w	Pulse Width	CK (Figure 1) R (Figure 2) S (Figure 2)	8.2 8.0 8.4	15.8 10.0 12.0	ns

SWITCHING WAVEFORMS

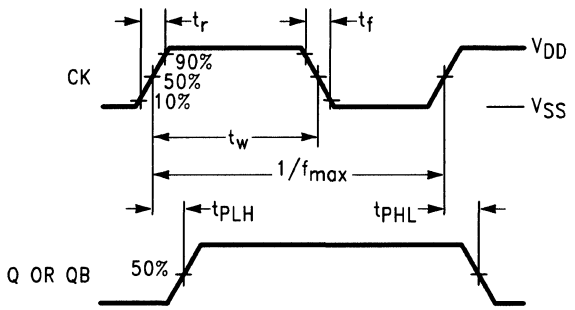


Figure 1

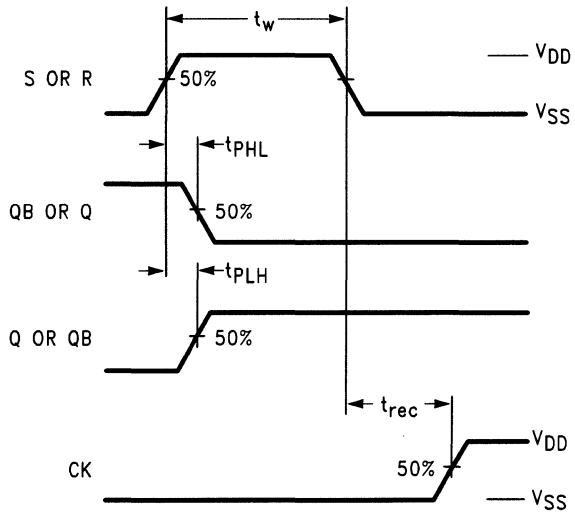


Figure 2

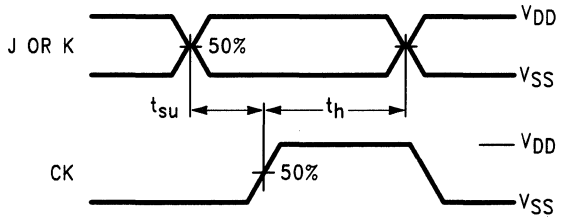
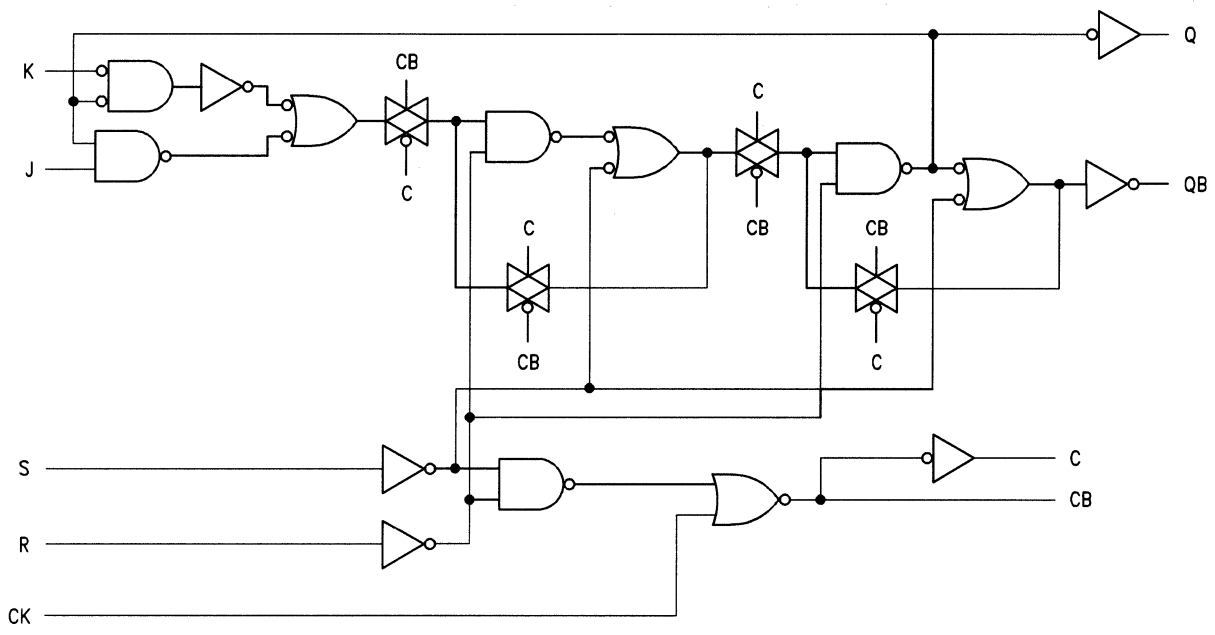


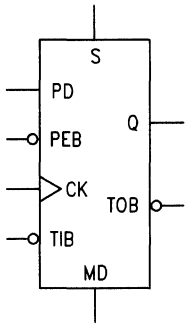
Figure 3

FUNCTION DIAGRAM



C038

1-Bit Presettable Up/Down Counter with Set



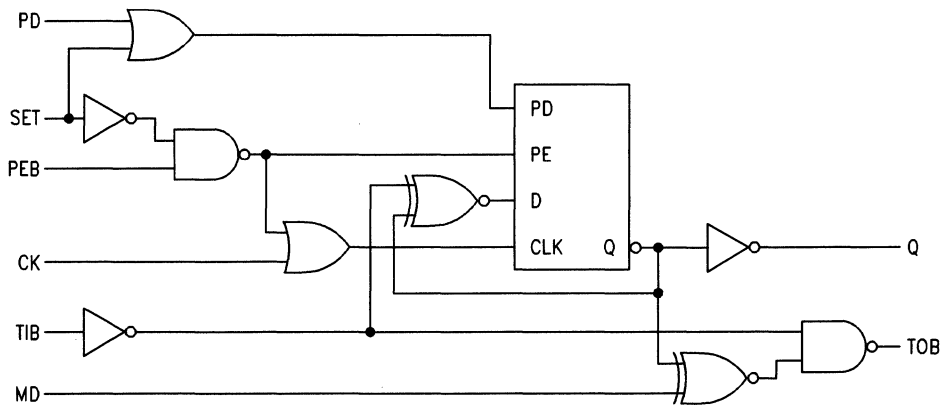
Primary Cells: 5
Netlist Format:
$SUBU C038
Q TOB / S PD PEB CK TIB MD

Pin Names:
S—Set Input
PD—Preset Data Input
PEB—Preset Enable Bar Input
CK—Clock Input
TIB—Toggle Input Bar
MD—Mode
Q—Counter Output
TOB—Toggle Output Bar

FUNCTION TABLE

CK	S	PEB	PD	TIB	MD	TOB	Q	Function Description
X	H	X	X	L	L/H	L/H	H	Set counter output Q high. S overrides CK and PEB inputs. TOB is dependent on TIB and MD.
X	X	X	X	H	X	H	No Change	
X	L	L	L/H	L	L	H/L	L/H	Data at the PD input is loaded asynchronously into the counter. The counter is disabled while PEB = L. For MD = L and TIB = L, Q = TOB. For MD = H and TIB = L, TOB is the complement of Q.
X	L	L	L/H	L	H	L/H	L/H	
⌐	L	H	X	L	L	Toggle	Toggle	Count up mode, advances to next state.
⌐	L	H	X	L	H	Toggle	Toggle	Count down mode, advances to next state.
⌐	L	H	X	H	X	H	No Change	This and all succeeding stages are disabled while TIB = H.
⌙	L	H	X	L	X	No Change	No Change	Outputs are not affected on the falling edge of the clock.

FUNCTION DIAGRAM



SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	55	—	—	—	—	40	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.6	3.6	5.4	2.0	10.0	0.6	3.0	8.3	2.6	15.8	ns
t_{PHL}		0.6	2.2	5.8	2.0	10.8	0.6	3.2	8.7	2.4	16.6	
t_{PLH}	Propagation Delay, CK to TOB (Figure 1)	0.6	2.8	7.6	2.0	14.0	0.6	4.2	11.8	3.8	22.8	ns
t_{PHL}		1.0	3.0	8.1	3.6	15.0	1.0	4.4	12.0	4.4	23.4	
t_{PLH}	Propagation Delay, S to Q (Figure 2)	0.6	3.0	8.2	2.0	15.2	0.6	1.8	9.2	2.6	20.8	ns
t_{PLH}	Propagation Delay, S to TOB (Figure 2)	0.6	3.4	9.1	2.0	16.8	0.6	3.2	13.3	3.8	25.6	ns
t_{PHL}		1.0	3.8	11.0	3.6	20.4	1.0	3.4	13.5	4.4	27.8	
t_{PLH}	Propagation Delay, PEB to Q (Figure 3)	0.6	3.0	7.6	2.0	13.6	0.6	3.4	9.8	2.6	19.2	ns
t_{PHL}		0.6	3.4	8.5	2.0	15.8	0.6	4.0	10.7	2.4	20.4	
t_{PLH}	Propagation Delay, PEB to TOB (Figure 3)	0.6	4.0	10.4	2.0	19.2	0.6	5.8	14.5	3.8	26.8	ns
t_{PHL}		1.0	4.0	10.4	3.6	19.2	1.0	6.2	14.8	4.4	26.8	
t_{PLH}	Propagation Delay, PD to Q (Figure 4)	0.6	2.6	7.1	2.0	13.2	0.6	4.0	10.8	2.6	20.6	ns
t_{PHL}		0.6	3.0	8.3	2.0	15.4	0.6	4.6	13.1	2.4	25.8	
t_{PLH}	Propagation Delay, PD to TOB (Figure 4)	0.6	5.2	10.2	2.0	18.8	0.6	4.8	15.7	3.8	30.8	ns
t_{PHL}		1.0	6.4	9.9	3.6	19.0	1.0	6.0	15.4	4.4	28.0	
t_{PLH}	Propagation Delay, TIB to TOB (Figure 5)	0.6	3.0	3.4	2.0	6.2	0.6	1.6	4.5	3.8	8.8	ns
t_{PHL}		1.0	4.6	4.4	3.6	8.2	1.0	2.4	6.1	4.4	11.2	
t_{PLH}	Propagation Delay, MD to TOB (Figure 6)	0.6	3.0	2.6	2.0	4.8	0.6	1.8	4.1	3.8	7.2	ns
t_{PHL}		1.0	4.4	3.7	3.6	6.8	1.0	2.0	5.0	4.4	9.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85° C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	TIB to CK (Figure 8)	8.6	15.0	ns
		PD to PEB (Figure 7)	7.4	13.0	
t_h	Hold Time	CK to TIB (Figure 8)	0.0	1.0	ns
		PEB to PD (Figure 7)	2.8	1.0	
t_{rec}	Recovery Time	S to CK (Figure 2)	11.2	22.0	ns
		PEB to CK (Figure 9)	10.2	22.0	
t_w	Pulse Width	CK (Figure 1)	7.8	14.0	ns
		S (Figure 2)	9.2	15.0	
		PEB (Figure 3)	7.8	13.0	

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INPUT LOAD FACTORS

IUL	Input Unit Load Factors	CK, PEB, PD, TIB	1.0
		S, MD	2.0

SWITCHING WAVEFORMS

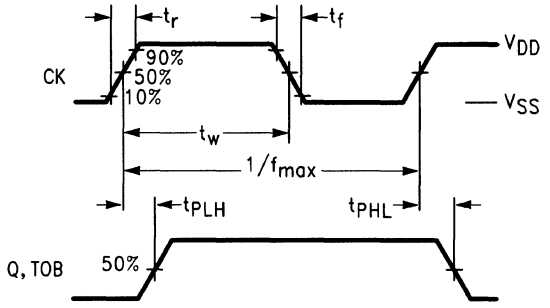


Figure 1

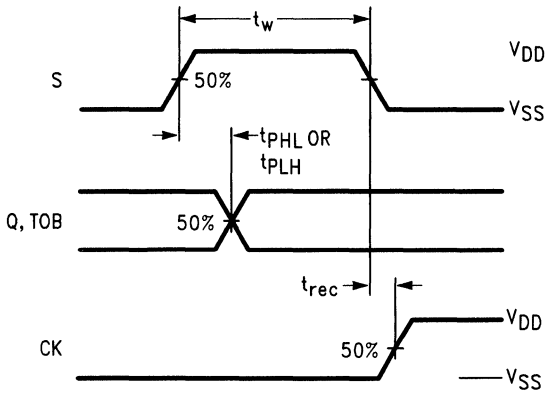


Figure 2

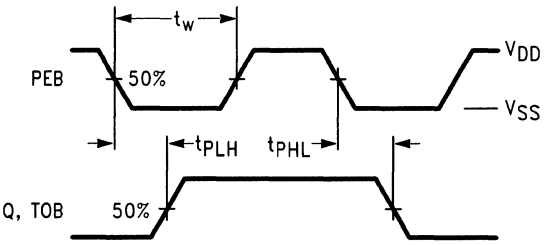


Figure 3

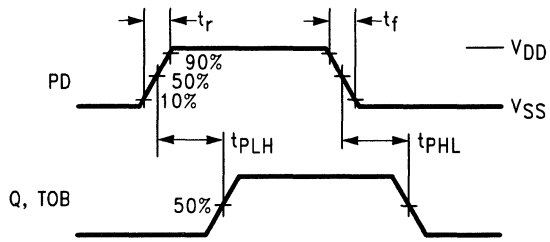


Figure 4

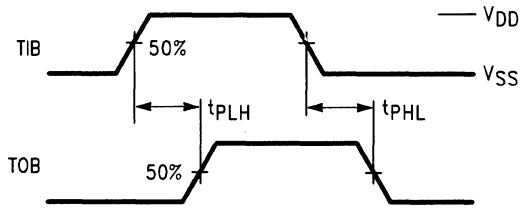


Figure 5

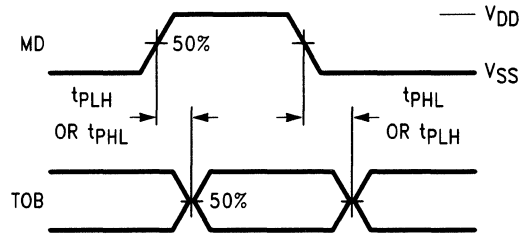


Figure 6

SWITCHING WAVEFORMS (Continued)

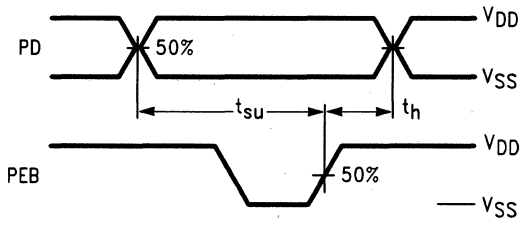


Figure 7

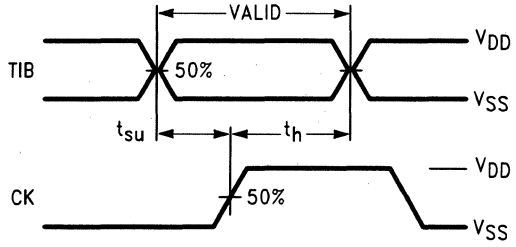


Figure 8

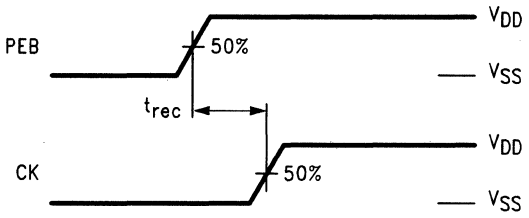
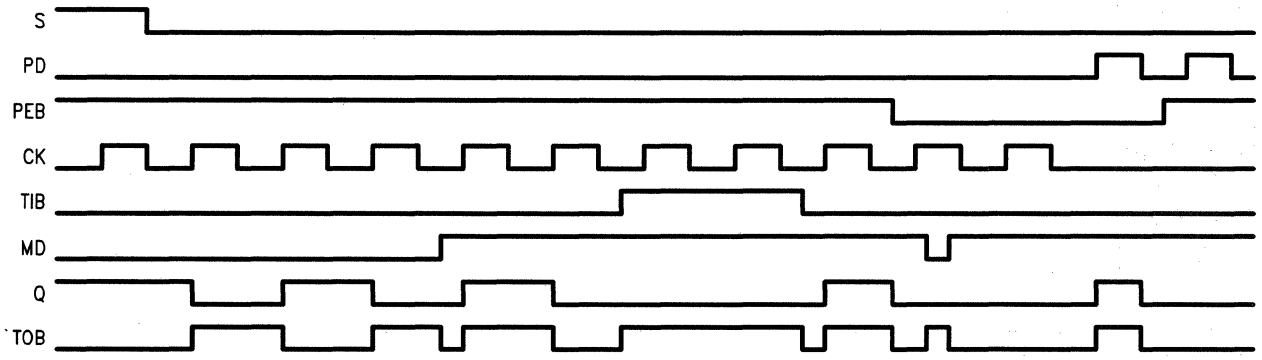
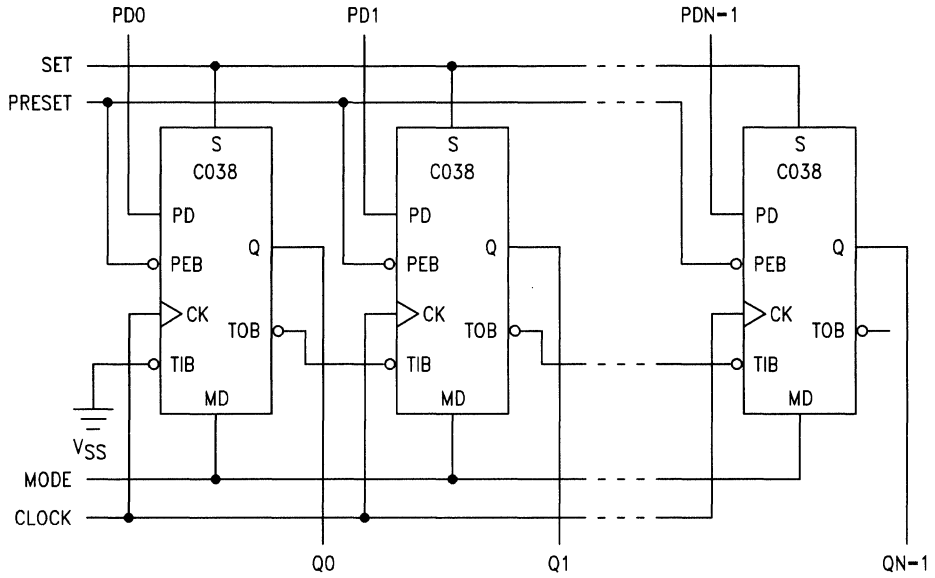


Figure 9

TIMING DIAGRAM



N-BIT COUNTER EXAMPLE



Maximum Frequency Calculation:
$1/f_{max} = t_P$ (CK to TOB) + [(n − 2)•t_P (TIB to TOB)] + t_{su} (TIB to CK)
Where n = number of stages
t_P = Worst case propagation delay

Example f_{max} Calculation:
4-bit Counter
Assume 1 pF loading conditions
n = 4
t_P (CK to TOB) = 23.4 ns
t_P (TIB to TOB) = 11.2 ns
t_{su} (TIB to CK) = 15.0 ns
$1/f_{max}$ = 23.4 ns + [(4 − 2)•11.2 ns] + 15.0 ns
= 60.8 ns
f_{max} = 16.4 MHz

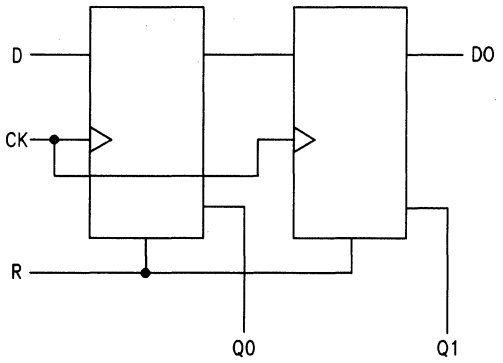
Note: The loading on TOB will probably be less than 1 pF, allowing a higher maximum frequency. The 1 pF load assumes driving two inputs and 100 mils of interconnect metal.

C039

2-Bit Serial-In/Parallel-Out Shift Register

Primary Cells: 5
Netlist Format:
$SUBU C039
Q0 Q1 DO / D CK R

Pin Names:
D—Serial Data Input
CK—Clock Input
R—Asynchronous Reset Input
Q0, Q1—Parallel Data Outputs
DO—Serial Data Output



FUNCTION TABLE

Inputs		Function
R	CK	
H	X	All outputs are asynchronously reset to low.
L	⌐	Data at D is shifted to Q0; Q0 data is shifted to Q1/DO.
L	⌐	No Change.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% duty cycle)	—	—	—	—	55	—	—	—	—	40	MHz
t_{PLH}	Propagation Delay, CK to Q0, Q1, DO (Figure 1)	0.6	2.8	7.6	2.4	14.0	0.6	4.4	12.5	2.4	23.2	ns
t_{PHL}		0.6	2.2	6.4	2.2	11.8	0.4	3.6	10.2	1.6	18.8	
t_{PHL}	Propagation Delay, R to Q0, Q1, DO (Figure 2)	0.6	1.8	4.8	2.2	8.8	0.4	2.6	7.1	1.6	13.2	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40 to +85°C)

Symbol	Parameter		HCA6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to CK (Figure 3)	1.2	10.0	ns
t_h	Hold Time	CK to D (Figure 3)	1.8	9.0	ns
t_{rec}	Recovery Time	R to CK (Figure 2)	8.2	24.0	ns
t_w	Pulse Width	CK(L) (Figure 1)	6.6	11.0	ns
		CK(H) (Figure 1)	1.6	11.0	
		R (Figure 2)	5.6	11.0	

INPUT LOAD FACTORS

IUL	Input Unit Load Factor—D, CK, R	1.0

11

SWITCHING WAVEFORMS

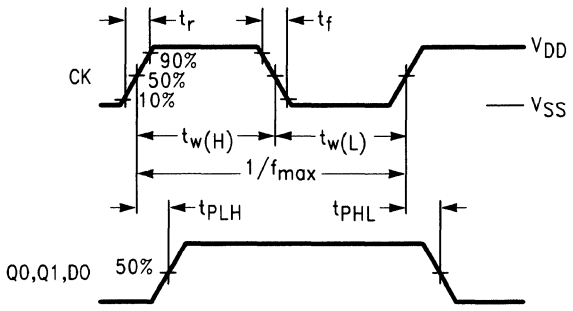


Figure 1

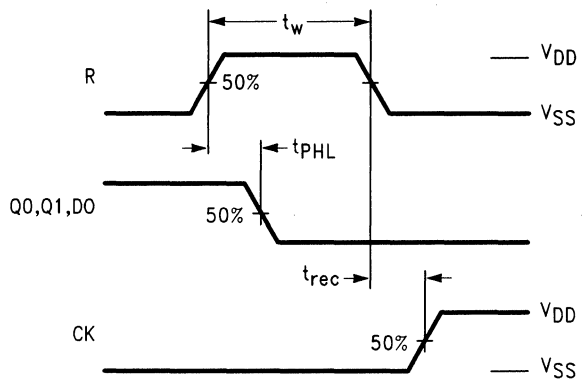


Figure 2

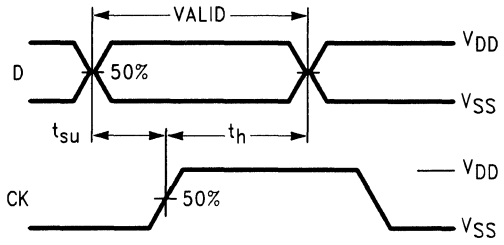
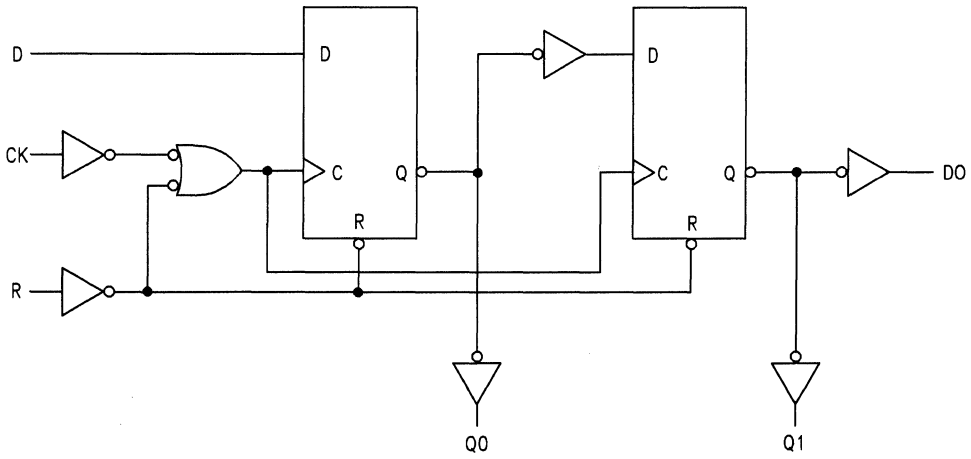
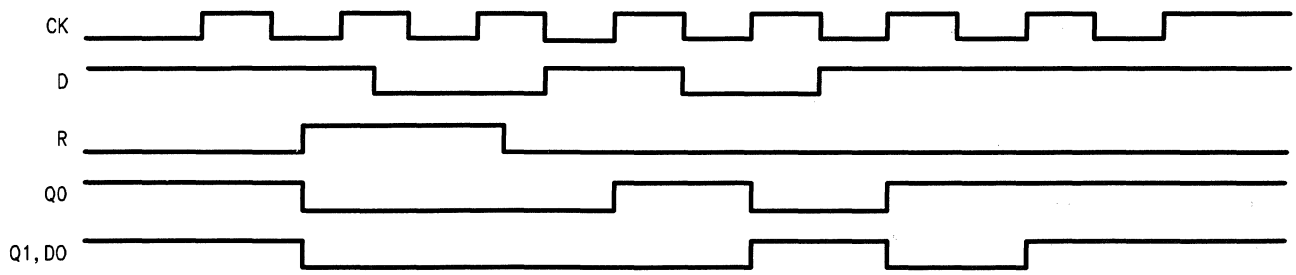


Figure 3

FUNCTION DIAGRAM

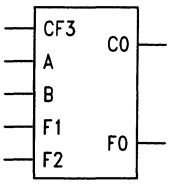


TIMING DIAGRAM



C040

1-Bit ALU with 7 Functions



Primary Cells: 6
Netlist Format:
$SUBU C040
CO FO / CF3 A B F1 F2

Pin Names:
CF3—Carry In/F3
A, B—Data Inputs
F1, F2—Function Inputs
CO—Carry Output
FO—Function Output

FUNCTION TABLE

Inputs			Outputs		Operation Performed
F1	F2	CF3	FO	CO	
L	L	L/H	★	*	Summation of A, B and CF3 (FO) with carry out (CO)
L	H	L	$A \oplus B$	L	XOR of A and B
L	H	H	$\overline{A \oplus B}$	H	XNOR of A and B
H	L	L	$\overline{A \bullet B}$	L	NAND of A and B
H	L	H	$A \bullet B$	H	AND of A and B
H	H	L	$A + B$	L	OR of A and B
H	H	H	$\overline{A + B}$	H	NOR of A and B

★$A \oplus B \oplus CF3$
* $A \bullet CF3 + A \bullet B + B \bullet CF3$

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A or B to FO (Figure 1)	0.2	1.6	9.3	1.4	17.2	0.3	4.0	12.8	1.7	23.6	ns
t_{PHL}		0.4	1.8	10.3	1.4	19.0	0.3	6.2	19.2	1.7	35.6	
t_{PLH}	Propagation Delay, A or B to CO (Figure 1)	0.4	2.0	11.0	1.4	20.4	0.5	6.8	21.0	2.5	38.8	ns
t_{PHL}		0.4	2.6	12.1	2.4	22.4	0.5	6.8	21.0	2.5	38.8	
t_{PLH}	Propagation Delay, CF3 to FO (Figure 1)	0.2	1.0	4.5	1.4	8.4	0.3	2.2	6.6	1.7	12.2	ns
t_{PHL}		0.4	1.2	4.1	1.4	7.6	0.3	2.2	6.6	1.7	12.2	
t_{PLH}	Propagation Delay, CF3 to CO (Figure 1) (full adder mode)	0.4	1.2	3.8	1.4	7.0	0.5	2.2	6.7	2.5	12.4	ns
t_{PHL}		0.4	1.6	4.8	2.4	8.8	0.5	2.6	8.1	2.5	15.0	
t_{PLH}	Propagation Delay, CF3 to CO (Figure 1) (non-full adder mode)	0.4	1.0	2.9	1.4	5.4	0.5	1.6	4.9	2.5	9.0	ns
t_{PHL}		0.4	1.4	4.0	2.4	7.4	0.5	2.2	6.6	2.5	12.2	
t_{PLH}	Propagation Delay, F1 or F2 to FO (Figure 1)	0.2	2.2	9.7	1.4	18.0	0.3	4.4	13.3	1.7	24.6	ns
t_{PHL}		0.4	2.4	10.7	1.4	19.8	0.3	6.4	19.8	1.7	36.6	
t_{PLH}	Propagation Delay, F1 or F2 to CO (Figure 1)	0.4	1.2	10.9	1.4	20.2	0.5	3.0	13.1	2.5	24.2	ns
t_{PHL}		0.4	1.8	13.4	2.4	24.8	0.5	3.0	22.3	2.5	41.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A, B, F1, F2	1.0
		CF3	2.0

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SWITCHING WAVEFORMS

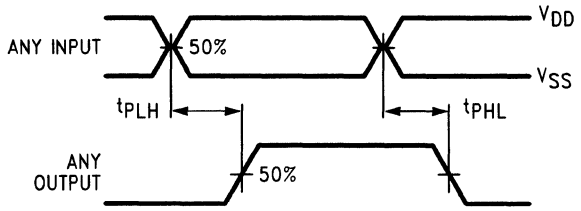
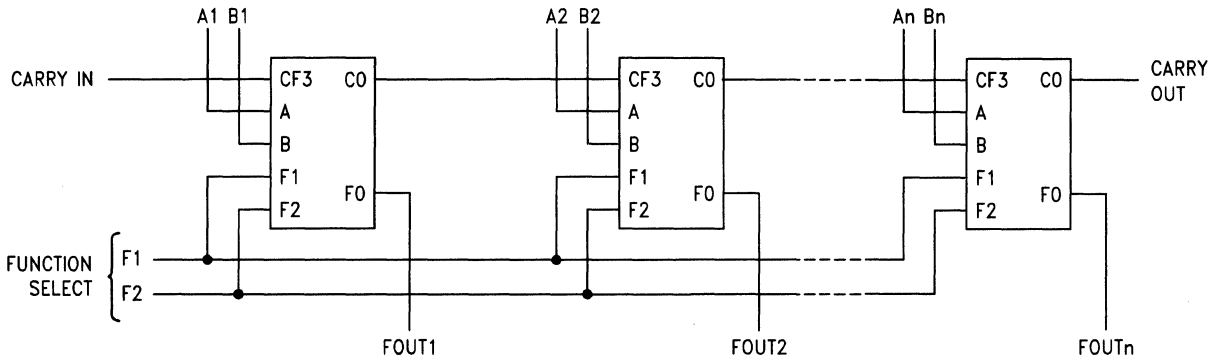


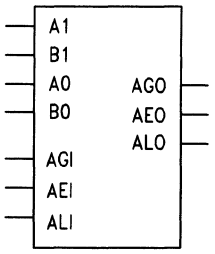
Figure 1

N-BIT ALU EXAMPLE



C041

2-Bit Magnitude Comparator



Primary Cells: 6
Netlist Format:
$SUBU C041
AGO AEO ALO / A1 B1 A0 B0 AGI AEI ALI

Pin Names:
A1, B1, A0, B0—Binary data inputs
AGI, AEI, ALI—A data greater than, equal to, and less than B data cascade inputs respectively
AGO, AEO, ALO—A data greater than, equal to, and less than B data outputs, respectively

FUNCTION TABLE

A1, B1	A0, B0	$A>B_{in}$	$A=B_{in}$	$A<B_{in}$	$A>B_{out}$	$A=B_{out}$	$A<B_{out}$
A1>B1	X	X	X	X	H	L	L
A1<B1	X	X	X	X	L	L	H
A1=B1	A0>B0	X	X	X	H	L	L
A1=B1	A0<B0	X	X	X	L	L	H
A1=B1	A0=B0	H	X	X	H	X	X
A1=B1	A0=B0	X	H	X	X	H	X
A1=B1	A0=B0	X	X	H	X	X	L
A1=B1	A0=B0	L	L	L	L	L	L

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A1, B1, A0, B0 to ALO, AGO (Figure 1)	0.4	2.2	7.1	1.0	13.2	0.4	5.2	14.2	2.0	27.8	ns
t_{PHL}		0.4	2.2	8.3	1.2	15.4	0.4	5.4	14.4	2.0	28.4	
t_{PLH}	Propagation Delay, A1, B1, A0, B0 to AEO (Figure 1)	0.4	2.8	8.3	1.2	15.4	0.4	5.4	14.8	2.0	28.4	ns
t_{PHL}		0.4	2.4	7.1	1.2	13.2	0.4	5.0	12.6	2.0	26.8	
t_{PLH}	Propagation Delay, AGI, AEI, ALI to ALO, AGO (Figure 1)	0.4	1.8	2.6	1.0	4.8	0.4	1.4	3.8	2.0	7.2	ns
t_{PHL}		0.4	1.8	2.7	1.2	5.0	0.4	1.6	4.2	2.0	7.8	
t_{PLH}	Propagation Delay, AGI, AEI, ALI to AEO (Figure 1)	0.4	2.0	2.7	1.2	5.0	0.4	1.6	4.2	2.0	7.8	ns
t_{PHL}		0.4	2.0	2.2	1.2	4.0	0.4	1.2	3.2	2.0	6.2	

*See Section 4 for minimum, typical and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, AGI, AEI, ALI	1.0

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SWITCHING WAVEFORMS

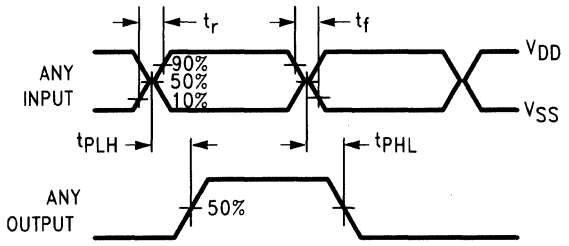
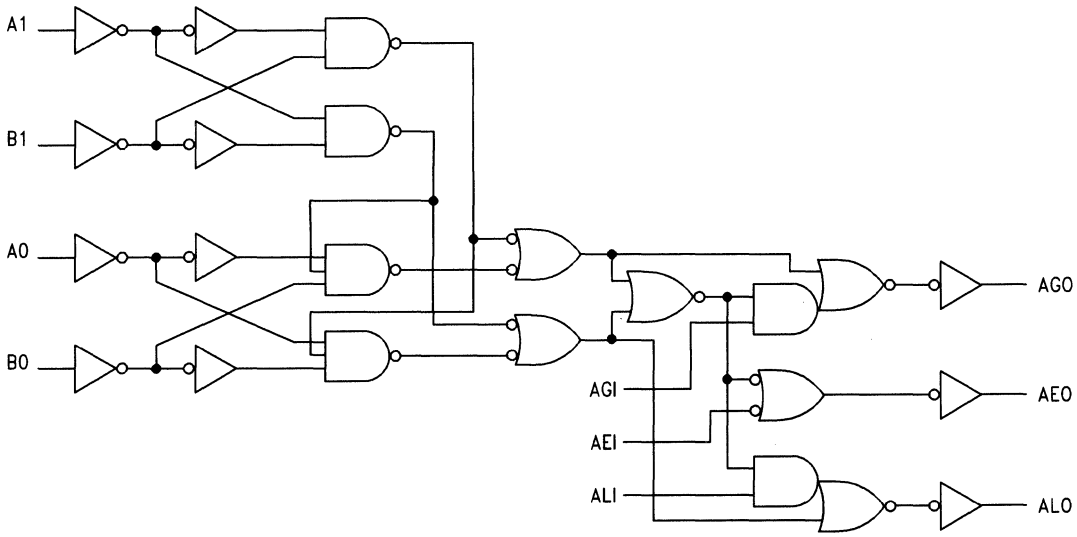
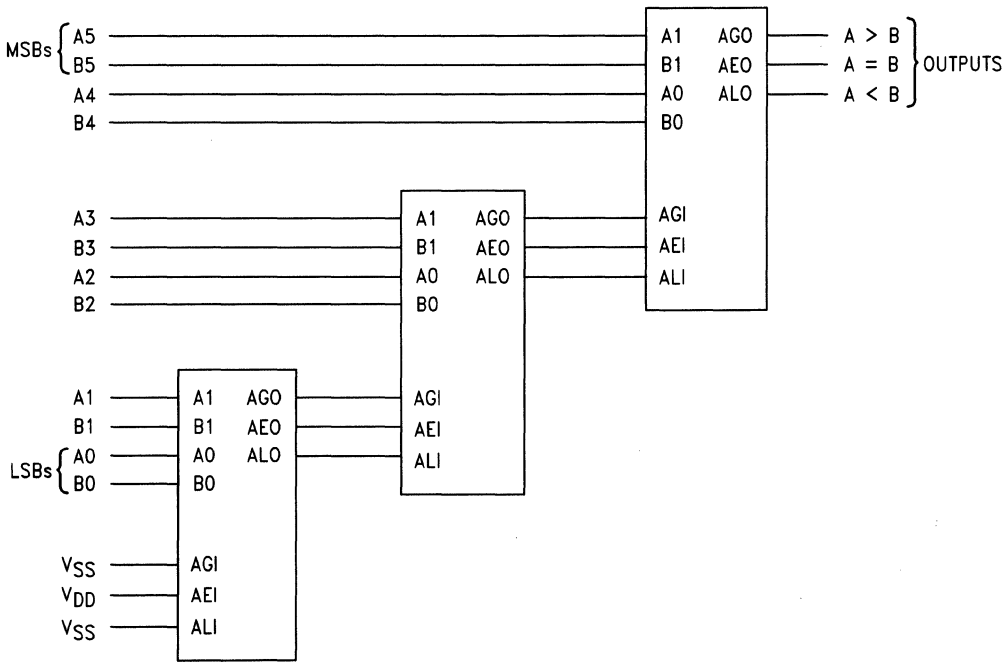


Figure 1

FUNCTION DIAGRAM

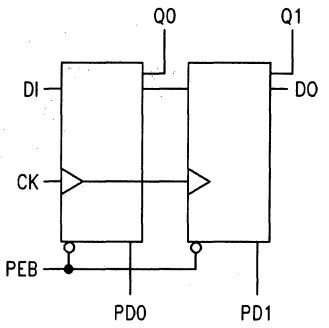


CASCADING COMPARATORS



C042

2-Bit Serial/Parallel Shift Register



Primary Cells: 6
Netlist Format:
$SUBU C042
Q0 Q1 DO / DI CK PEB PD0
PD1

Pin Names:
CK—Clock
PEB—Active Low Preset Enable
DI—Data Input
PD0, PD1—Preset Data Inputs
Q0, Q1—Parallel Shift-Register Output
DO—Data Output

FUNCTION TABLE

CK	PEB	DI	PD0	PD1	Q0	Q1 = DO	Function Performed
X	L	X	X	X	PD0	PD1	Asynchronous parallel data load. Overrides clock input.
⌐	H	X	X	X	DI	$Q0_{n-1}$	Synchronous serial shift.
¬	H	X	X	X	No Change		

X = Don't Care
$Q0_{n-1}$ = Previous State of Q0

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, CK to Q0, Q1, DO (Figure 1)	0.4	2.2	6.6	2.0	12.2	0.6	3.6	10.4	2.2	19.2	ns
t_{PHL}		0.4	2.0	6.1	2.0	11.2	0.6	3.6	10.3	2.2	19.2	
t_{PLH}	Propagation Delay, PEB to Q0, Q1, DO (Figure 2)	0.4	2.4	7.7	2.0	14.2	0.6	4.6	14.6	2.2	27.0	ns
t_{PHL}		0.4	2.8	8.4	2.0	15.6	0.6	4.6	14.3	2.2	26.6	
t_{PLH}	Propagation Delay, PD to Q0, Q1, DO (Figure 3)	0.4	2.2	6.6	2.0	12.2	0.6	3.8	12.2	2.2	22.6	ns
t_{PHL}		0.4	2.2	6.7	2.0	12.4	0.6	3.8	12.2	2.2	22.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85°C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	DI–CK (Figure 4)	3.8	10.0	ns
		PD–PEB (Figure 5)	5.8	12.0	
t_h	Hold Time	CK to DI (Figure 4)	2.8	7.0	ns
		PEB to PD (Figure 5)	2.6	7.0	
t_{rec}	Recovery Time	PEB to CK (Figure 6)	15.6	19.0	ns
t_w	Pulse Width	CK–$t_{w(L)}$ (Figure 1)	8.0	13.6	ns
		CK–$t_{w(H)}$ (Figure 1)	5.2	13.6	
		PEB (Figure 5)	8.6	12.0	

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INPUT LOAD FACTORS

IUL	Input Unit Load Factors—DI, CK, PEB, PD0, PD1	1.0

SWITCHING WAVEFORMS

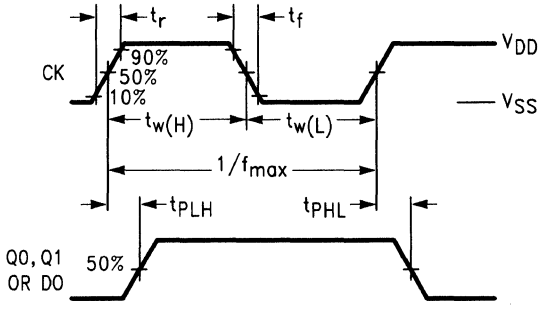


Figure 1

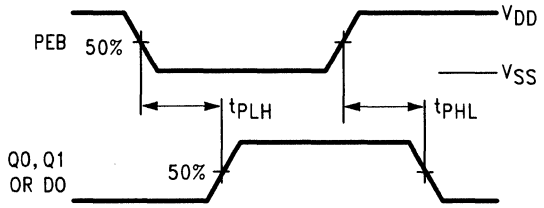


Figure 2

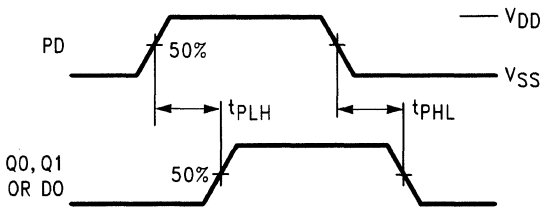


Figure 3

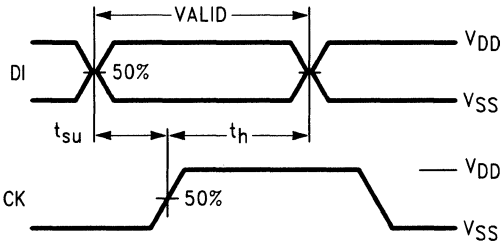


Figure 4

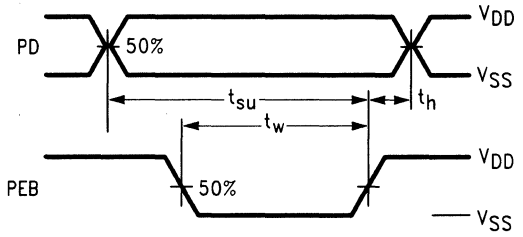


Figure 5

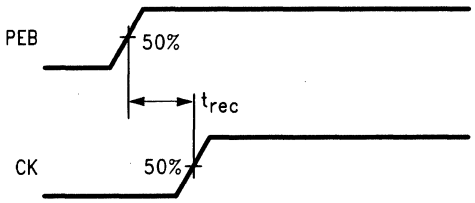
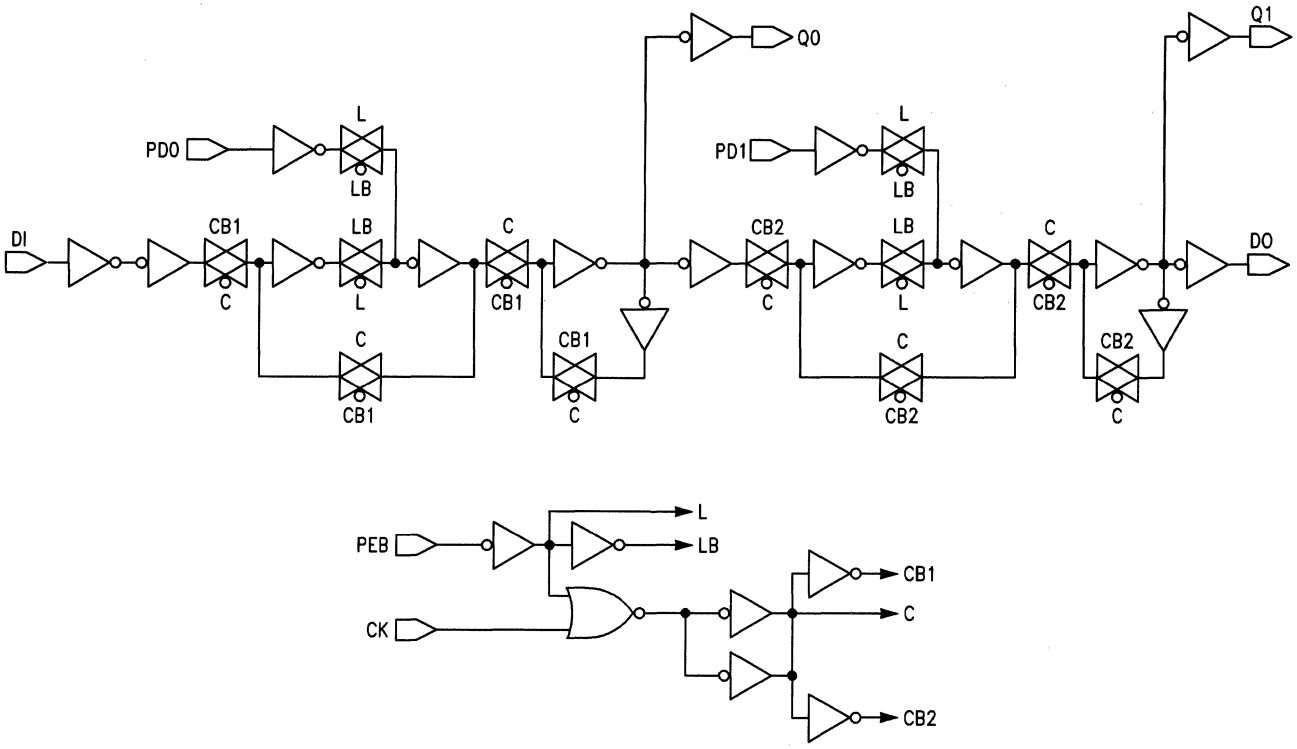
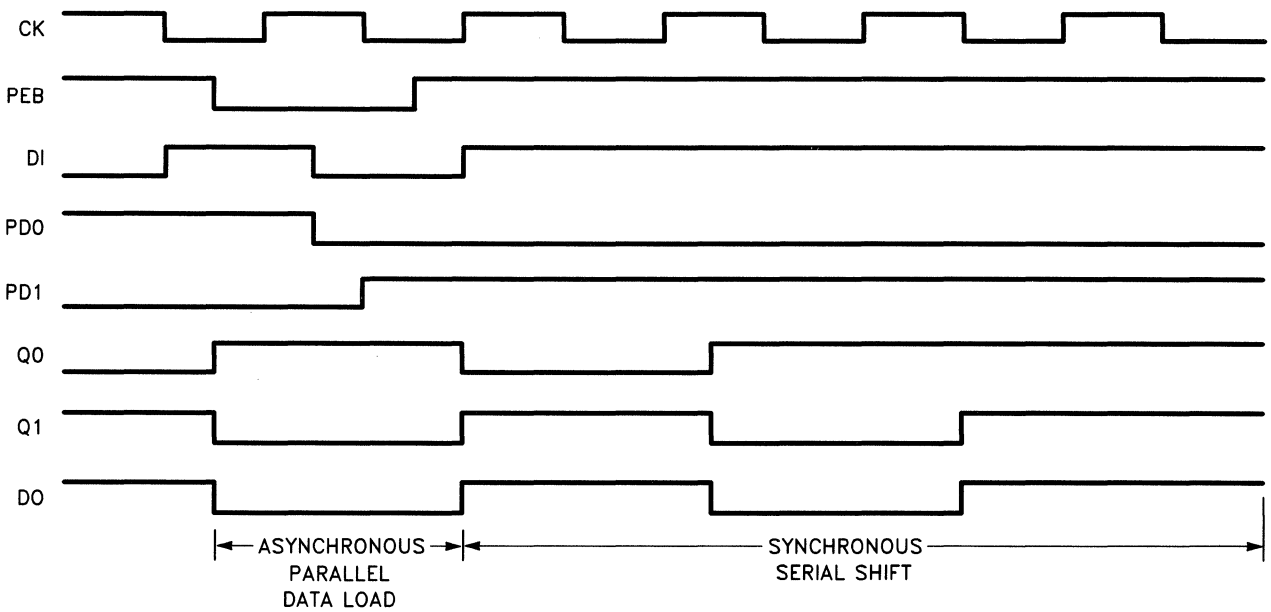


Figure 6

LOGIC DIAGRAM



TIMING DIAGRAM



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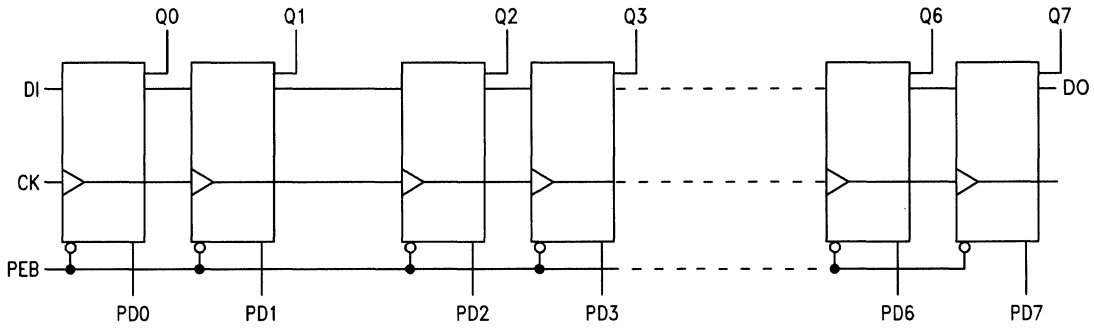
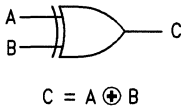
TYPICAL APPLICATION
8-Bit Serial/Parallel Shift Register



C053

2-Input Exclusive OR Gate

Primary Cells: 1
Netlist Format:
$SUBU C053
C / A B



FUNCTION TABLE

A	B	C
L	L	L
L	H	H
H	L	H
H	H	L

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.2	1.2	3.5	1.2	6.4	0.4	2.0	5.4	1.8	10.2	ns
t_{PHL}		0.2	1.2	3.4	1.0	6.2	0.3	1.6	4.6	1.8	9.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B	1.0

SWITCHING WAVEFORMS

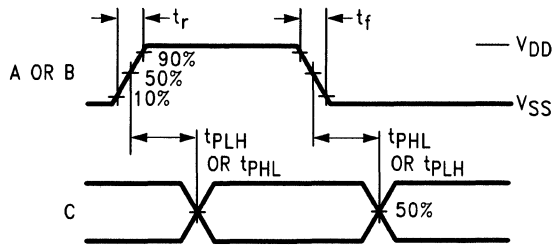


Figure 1

11

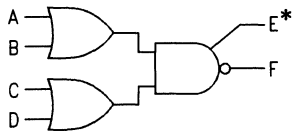
C054

2-Input 2-Wide OR-AND-Invert

Primary Cells: 1
Netlist Format:
$SUBU C054
E F / A B C D

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	E	F
L	L	X	X	L	H
X	X	L	L	L	H
H	X	H	X	H	L
H	X	X	H	H	L
X	H	H	X	H	L
X	H	X	H	H	L



$E = \overline{(A+B)\cdot(C+D)}$

$F = (A+B)\cdot(C+D)$

*This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

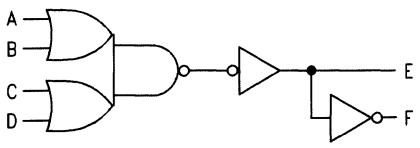
Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A,B,C,D to E (Figure 1)	0.4	1.4	3.5	2.0	6.4	0.6	2.4	7.1	2.4	13.2	ns
t_{PHL}		0.4	1.6	5.6	2.2	6.6	0.6	2.6	7.0	2.0	13.0	
t_{PLH}	Propagation Delay, A,B,C,D to F (Figure 1)	0.4	2.4	3.6	2.2	10.4	0.5	3.6	10.1	2.2	18.6	ns
t_{PHL}		0.4	2.4	5.6	2.2	10.4	0.5	3.4	10.0	2.6	18.4	
t_{PLH}	Propagation Delay, E to F (Figure 2)	0.4	0.6	2.1	2.2	3.0	0.5	1.0	3.0	2.2	5.6	ns
t_{PHL}		0.4	0.8	2.2	2.2	3.0	0.5	1.0	2.8	2.6	5.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A,B,C,D	1.0

FUNCTION DIAGRAM



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SWITCHING WAVEFORMS

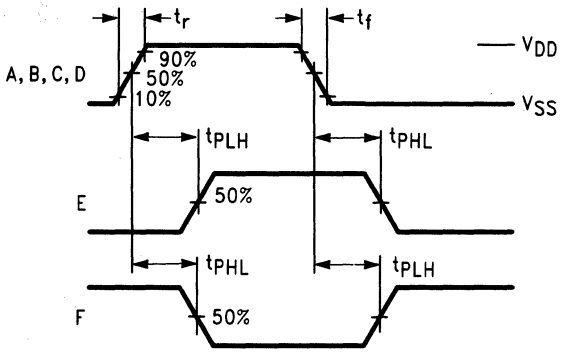


Figure 1

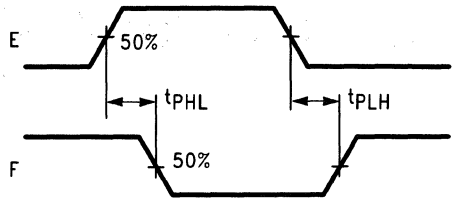


Figure 2

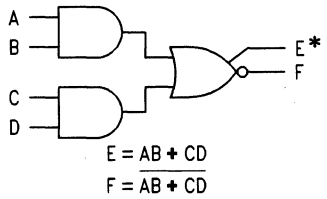
C055

2-Input 2-Wide AND-OR-Invert

Primary Cells: 1
Netlist Format:
$SUBU C055
E F / A B C D

FUNCTION TABLE

A	B	C	D	E	F
X	X	H	H	H	L
H	H	X	X	H	L
X	L	L	X	L	H
L	X	X	L	L	H
L	H	L	H	L	H
H	L	H	L	L	H



* This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C, D to E (Figure 1)	0.4	1.0	3.4	2.0	6.2	0.6	2.2	5.9	2.8	11.2	ns
t_{PHL}		0.4	1.4	3.6	2.0	6.6	0.6	2.2	6.0	2.4	11.4	
t_{PLH}	Propagation Delay A, B, C, D to F (Figure 1)	0.4	2.2	5.6	2.2	10.4	0.5	3.2	8.7	2.8	16.6	ns
t_{PHL}		0.4	1.8	5.6	2.2	10.4	0.5	3.2	8.6	2.8	16.4	
t_{PLH}	Propagation Delay, E to F (Figure 2)	0.4	1.2	2.0	2.2	5.8	0.5	1.0	2.7	2.8	5.2	ns
t_{PHL}		0.4	1.2	2.2	2.2	6.2	0.5	1.0	2.7	2.8	5.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C, D	1.0

SWITCHING WAVEFORMS

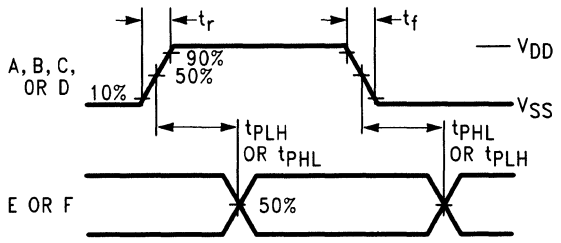


Figure 1

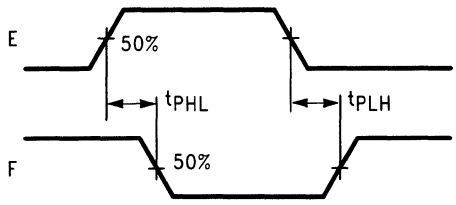
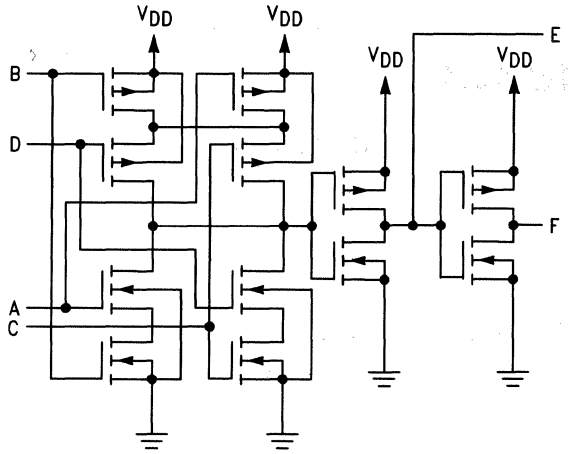


Figure 2

11

CIRCUIT DIAGRAM



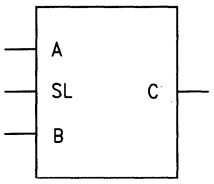
C056

2-to-1 Multiplexer

Primary Cells: 1
Netlist Format:
$SUBU C056
C / A SL B

FUNCTION TABLE

SL	C
L	A
H	B



SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B to C (Figure 1)	0.2	1.0	2.7	1.2	5.0	0.4	1.6	4.4	2.0	8.4	ns
t_{PHL}		0.2	1.0	2.7	1.2	5.0	0.4	1.6	4.4	2.0	8.4	
t_{PLH}	Propagation Delay, SL to C (Figure 1)	0.2	0.8	2.4	1.2	4.4	0.4	1.6	3.9	2.0	7.0	ns
t_{PHL}		0.2	0.8	2.5	1.2	4.6	0.4	1.6	3.9	2.0	7.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A, B	1.0
		SL	2.0

SWITCHING WAVEFORMS

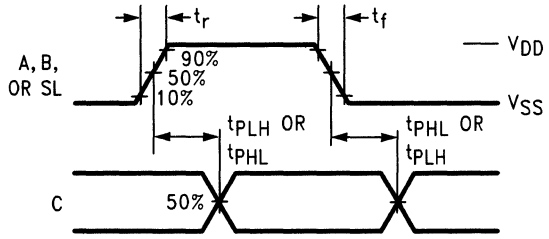
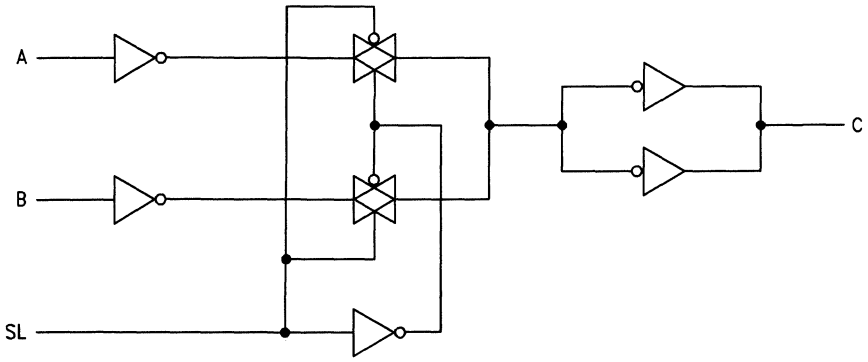


Figure 1

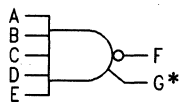
FUNCTION DIAGRAM



C057

5-Input NAND/AND Gate

Primary Cells: 2
Netlist Format:
$SUBU C057
F G / A B C D E



$F = \overline{A \cdot B \cdot C \cdot D \cdot E}$
$G = A \cdot B \cdot C \cdot D \cdot E$

*This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, C, D, E to F (Figure 1)	0.4	1.6	3.8	2.0	7.0	0.9	2.2	6.2	2.3	11.4	ns
t_{PHL}		0.6	2.2	5.5	2.0	10.2	0.6	3.0	9.0	2.5	16.6	
t_{PLH}	Propagation Delay, A, B, C, D, E to G (Figure 1)	0.4	3.0	7.7	2.2	14.2	0.6	4.0	12.0	2.7	22.2	ns
t_{PHL}		0.4	2.6	6.1	2.2	11.2	0.6	3.0	9.0	2.5	16.6	
t_{PLH}	Propagation Delay, F to G (Figure 2)	0.4	0.6	2.2	2.2	3.2	0.6	1.0	3.0	2.7	5.8	ns
t_{PHL}		0.4	0.8	2.3	2.2	3.4	0.6	0.8	2.8	2.5	5.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C, D, E	1.0

SWITCHING WAVEFORMS

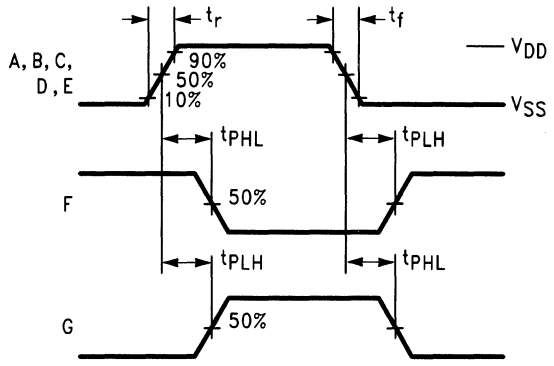


Figure 1

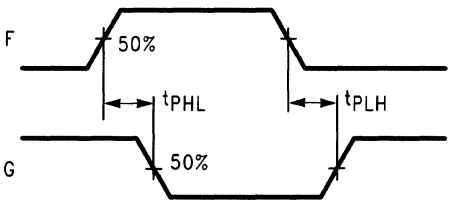
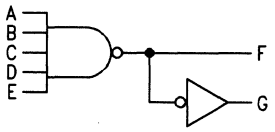


Figure 2

FUNCTION DIAGRAM



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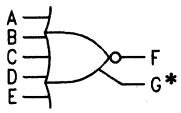
C058

5-Input NOR/OR Gate

Primary Cells: 2
Netlist Format:
$SUBU C058
F G / A B C D E



$F = \overline{A+B+C+D+E}$

$G = A+B+C+D+E$

*This output is dependent on the previous outputs loading and requires special timing considerations. Refer to Section 4.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

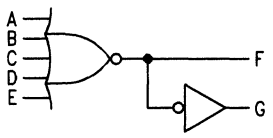
Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A,B,C,D,E to F (Figure 1)	0.2	2.2	5.4	1.8	10.0	0.4	2.6	9.5	1.6	17.6	ns
t_{PHL}		0.2	1.6	3.7	1.6	6.8	0.4	2.0	5.7	1.2	10.6	
t_{PLH}	Propagation Delay, A,B,C,D,E to G (Figure 1)	0.2	2.0	5.4	1.8	10.0	0.4	2.6	7.1	1.4	13.2	ns
t_{PHL}		1.2	2.6	6.7	6.6	12.4	0.4	3.4	11.0	1.8	20.4	
t_{PLH}	Propagation Delay, F to G (Figure 2)	0.2	0.2	1.7	1.8	4.4	0.4	0.6	1.4	1.4	2.6	ns
t_{PHL}		1.2	1.2	1.3	6.6	7.4	0.4	0.8	1.5	1.8	2.8	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A,B,C,D,E	1.0

LOGIC DIAGRAM



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SWITCHING WAVEFORMS

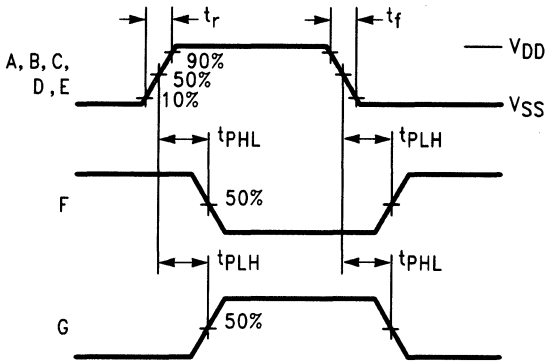


Figure 1

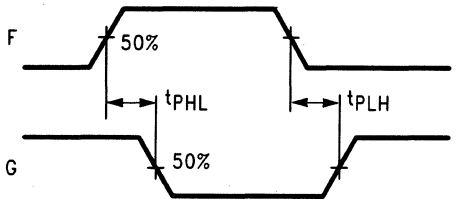
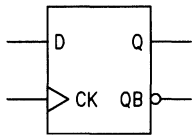


Figure 2

C059

Buffered D Flip-Flop

Primary Cells: 2
Netlist Format:
$SUBU C059
Q QB / D CK



FUNCTION TABLE

CK	D	Q	QB
↗	L	L	H
↗	H	H	L
↘	X	No Change	

X = Don't Care

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	45	—	—	—	—	50	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	1.8	5.0	2.8	9.2	0.3	3.0	7.2	1.9	15.6	ns
t_{PHL}		0.4	1.8	5.3	2.8	9.8	0.3	3.6	9.2	1.2	17.0	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.2	1.4	4.0	1.0	7.4	0.4	3.0	7.5	1.6	13.4	ns
t_{PHL}		0.2	1.4	3.8	1.2	7.0	0.3	2.2	6.2	1.6	11.2	
t_{PLH}	Propagation Delay, QB to Q (Figure 2)	0.2	0.6	1.8	2.8	3.4	0.3	0.6	2.4	1.9	4.6	ns
t_{PHL}		0.2	0.6	1.8	2.8	3.4	0.3	0.8	1.9	1.2	3.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85° C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to CK (Figure 3)	3.0	5.0	ns
t_h	Hold Time	CK to D (Figure 3)	1.6	4.0	ns
t_w	Pulse Width	CK (Figure 1)	11.0	10.0	ns

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—D, CK	1.0

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SWITCHING WAVEFORMS

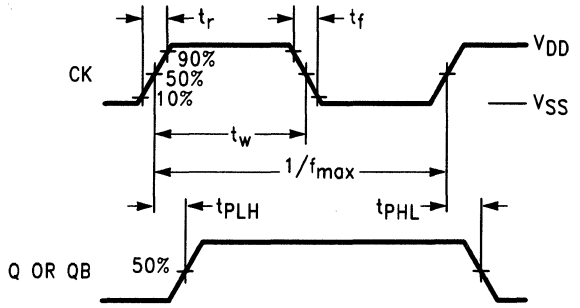


Figure 1

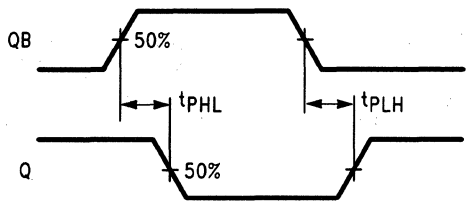


Figure 2

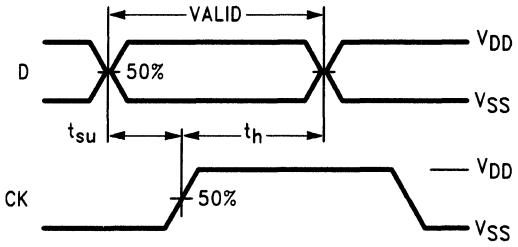
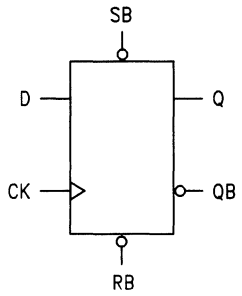


Figure 3

C060

Buffered D Flip-Flop with Reset (L) and Set (L)



Primary Cells: 3
Netlist Format:
$SUBU C060
Q QB / SB D CK RB

Pin Names:
SB—Active Low Set
RB—Active Low Reset
D—Data Input
CK—Clock
Q, QB—Data Outputs

FUNCTION TABLE

SB	RB	D	CK	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
H	H	H	↗	H	L
H	H	L	↗	L	H
L	L	X	X	U	U
H	H	X	↘	No Change	

X = Don't Care
U = Undefined

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	55	—	—	—	—	40	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	2.0	5.0	2.2	9.2	0.6	2.8	7.7	2.8	14.8	ns
t_{PHL}		0.6	2.2	6.0	2.2	11.0	0.6	3.2	8.9	1.6	17.2	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.6	2.4	6.5	2.0	12.0	0.6	3.6	10.1	2.6	19.4	ns
t_{PHL}		0.4	2.2	5.7	2.2	10.6	0.6	3.0	8.3	2.0	16.0	
t_{PHL}	Propagation Delay, RB to Q (Figure 2)	0.6	3.0	8.6	2.2	16.0	0.6	4.8	13.6	1.6	25.6	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 2)	0.6	3.2	9.3	2.0	17.2	0.6	5.0	14.4	2.6	27.6	ns
t_{PLH}	Propagation Delay, SB to Q (Figure 2)	0.4	2.0	5.6	2.2	10.4	0.6	4.2	9.7	2.8	16.8	ns
t_{PHL}	Propagation Delay, SB to QB (Figure 2)	0.4	2.4	6.3	2.2	11.6	0.6	4.6	10.6	2.0	18.2	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85°C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to CK (Figure 3)	4.0	7.0	ns
t_h	Hold Time	CK to D (Figure 3)	2.4	7.0	ns
t_{rec}	Recovery Time	RB to CK (Figure 2) SB to CK (Figure 2)	5.0 5.0	19.0 19.0	ns
t_w	Pulse Width	CK, $t_{w(L)}$ (Figure 1) CK, $t_{w(H)}$ (Figure 1) RB (Figure 2) SB (Figure 2)	8.6 8.6 9.4 6.6	12.0 12.0 15.0 13.0	ns

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—D, CK	1.0

SWITCHING CHARACTERISTICS

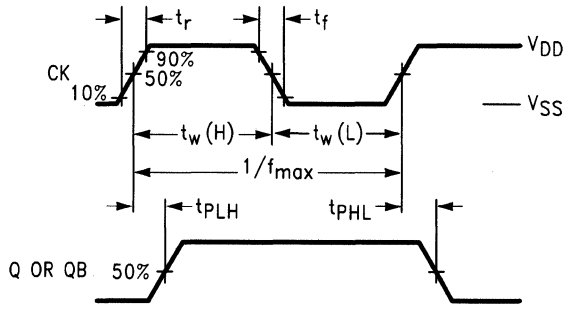


Figure 1

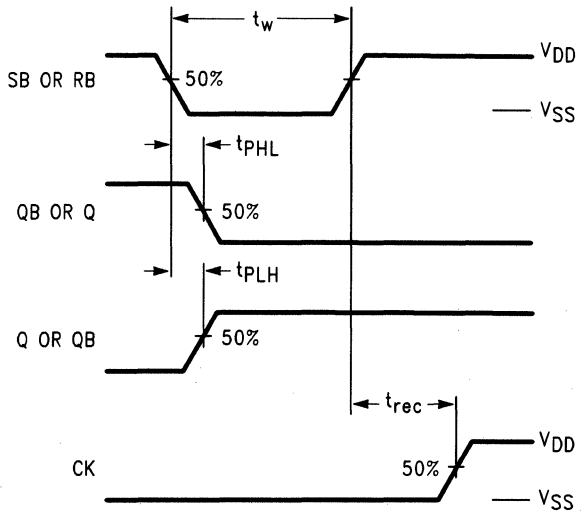


Figure 2

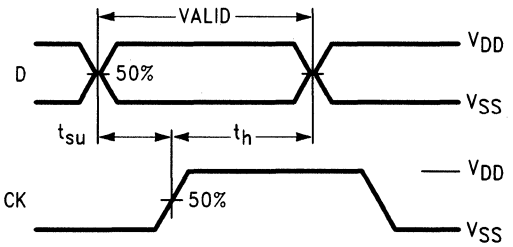
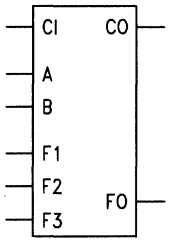


Figure 3

C080

1-Bit ALU with Fast Carry



Primary Cells: 6
Netlist Format:
$SUBU C080
CO FO / CI A B F1 F2 F3

Pin Names:
CI—Carry Input
A,B—Data Inputs
F1, F2, F3—Function Select Inputs
CO—Carry Output
FO—Function Output

FUNCTION TABLE

F1	F2	F3	CI	FO	CO	Function
L	L	X	L/H	A⊕B⊕C	*	Summation of A, B, and CI (FO), with carry out (CO).
L	H	L	X	A⊕B	*	Exclusive-OR of A and B.
L	H	H	X	$\overline{A⊕B}$	*	Exclusive-NOR of A and B.
H	L	L	X	$\overline{A•B}$	*	NAND of A and B.
H	L	H	X	A•B	*	AND of A and B.
H	H	L	X	A+B	*	OR of A and B.
H	H	H	X	$\overline{A+B}$	*	NOR of A and B.

*Carry of A, B, and CI; CO=(A•CI)+(A•B)+(B•CI)

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A, B, to FO (Figure 1)	0.2	4.0	10.3	2.0	19.0	0.2	4.8	18.2	2.8	33.6	ns
t_{PHL}		0.2	4.2	10.6	1.8	19.6	0.4	5.4	17.6	2.0	32.6	
t_{PLH}	Propagation Delay, A, B, to CO (Figure 1)	0.4	2.0	4.3	3.6	8.0	0.6	2.0	7.1	5.6	13.2	ns
t_{PHL}		0.8	1.8	4.1	3.8	7.6	0.8	2.0	9.8	3.6	12.0	
t_{PLH}	Propagation Delay, CI to FO (Figure 1)	0.2	1.6	3.9	2.0	7.2	0.2	2.2	8.9	2.8	16.4	ns
t_{PHL}		0.2	2.2	5.1	1.8	9.4	0.4	2.6	7.9	2.0	14.6	
t_{PLH}	Propagation Delay, CI to CO (Figure 1)	0.4	1.8	3.6	3.6	6.6	0.6	1.8	5.9	5.6	11.0	ns
t_{PHL}		0.8	1.8	3.8	3.8	7.0	0.8	2.4	5.8	3.6	10.8	
t_{PLH}	Propagation Delay, F1, F2, to FO (Figure 1)	0.2	4.4	12.6	2.0	23.4	0.2	4.8	20.0	2.8	37.0	ns
t_{PHL}		0.2	4.4	11.9	1.8	22.0	0.4	5.8	19.1	2.0	35.4	
t_{PLH}	Propagation Delay, F3 to FO (Figure 1)	0.2	2.2	5.1	2.0	9.4	0.2	2.8	8.9	2.8	16.4	ns
t_{PHL}		0.2	2.0	4.6	1.8	8.6	0.4	2.4	8.2	2.0	15.2	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A,B,F1,F2,F3	1.0
		CI	2.0

SWITCHING WAVEFORMS

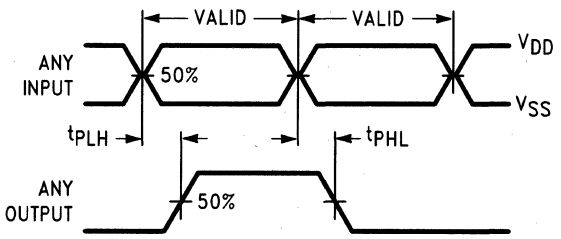
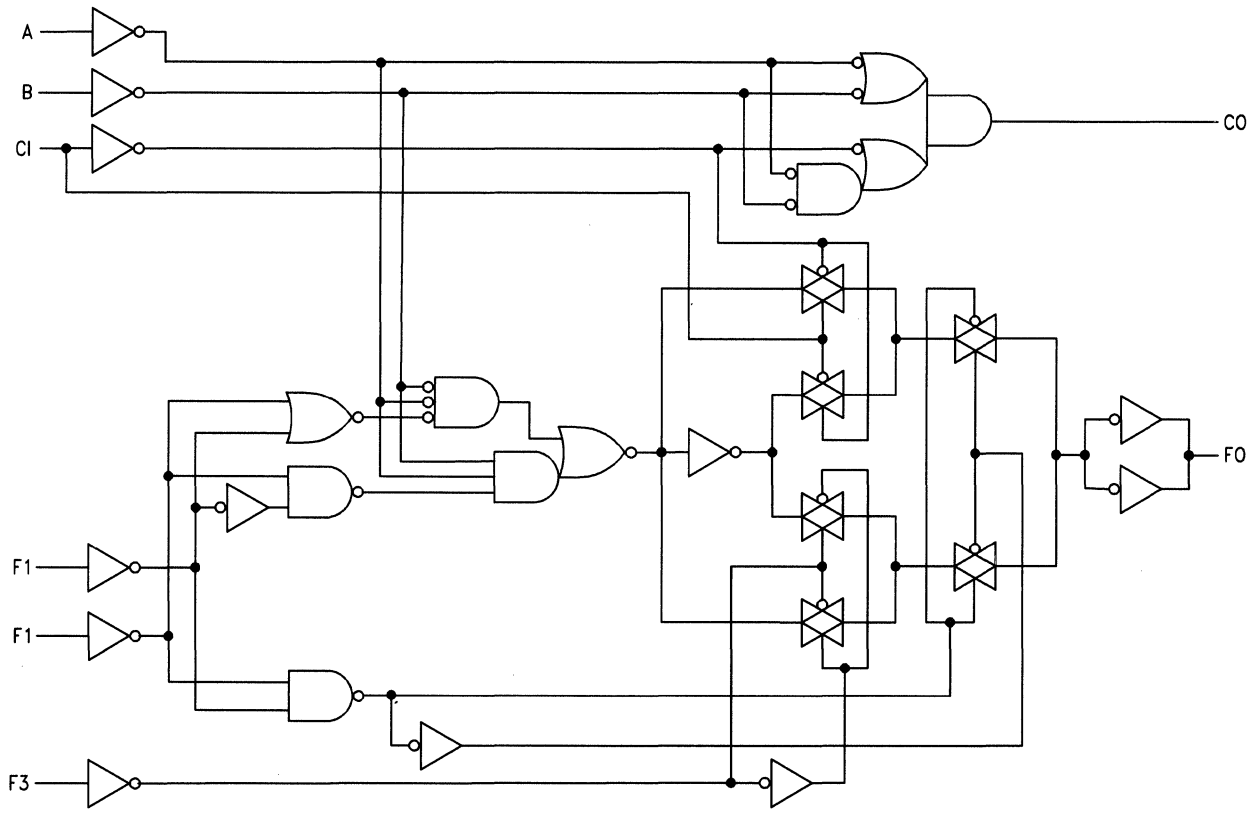
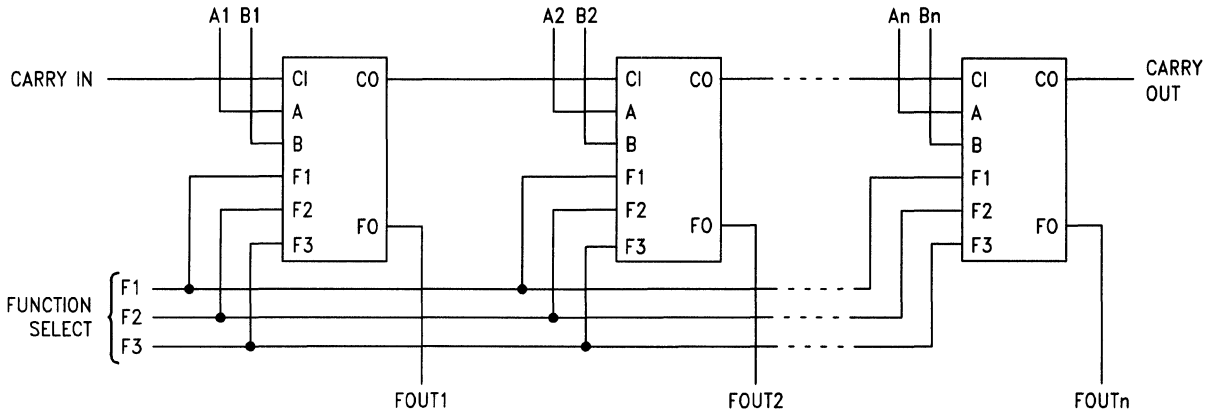


Figure 1

FUNCTION DIAGRAM



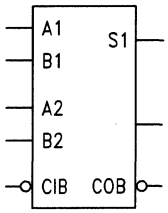
N-Bit ALU EXAMPLE



C081

2-Bit Full Adder with Fast Carry

Primary Cells: 6
Netlist Format:
$SUBU C081
S1 S2 COB / A1 B1 A2 B2 CIB



Pin Names:
A1, A2—Data Word A Inputs
B1, B2—Data Word B Inputs
S1, S2—Sum Outputs
CIB—Carry Input Bar (Active Low)
COB—Carry Output Bar (Active Low)

Function Equations:
$S1 = A1 \oplus B1 \oplus \overline{CIB}$; Summation of A1, B1, and $\overline{CIB}$.
$CO_{int} = A1\ B1 + A1\overline{CIB} + B1\overline{CIB}$; Internal Carry of A1, B1, and $\overline{CIB}$.
$S2 = A2 \oplus B2 \oplus CO_{int}$; Summation of A2, B2, and CO_{int}.
$COB = \overline{A2B2 + A2CO_{int} + B2CO_{int}}$; Carry Out (Active Low) of A2, B2, and CO_{int}.

SWITCHING CHARACTERISTICS* ($C_L = 1$ pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A1, B1 to S1 or A2, B2 to S2 (Figure 1)	0.2	1.9	5.9	1.2	10.9	0.2	2.8	10.6	1.6	19.6	ns
t_{PHL}		0.3	1.7	5.3	1.0	9.8	0.2	2.4	9.3	1.4	17.2	
t_{PLH}	Propagation Delay, A1, B1 to S2 (Figure 1)	0.2	2.9	8.7	1.2	16.1	0.2	4.4	15.8	1.6	29.4	ns
t_{PHL}		0.3	3.0	8.7	1.0	16.1	0.2	4.2	15.5	1.4	28.8	
t_{PLH}	Propagation Delay, A1, B1 to COB (Figure 1)	0.2	2.8	8.4	1.2	15.5	0.3	4.2	15.2	1.7	28.2	ns
t_{PHL}		0.3	2.6	7.4	1.2	13.7	0.2	3.6	12.5	1.5	23.2	
t_{PLH}	Propagation Delay, A2, B2 to COB (Figure 1)	0.2	1.7	5.4	1.2	9.9	0.3	2.6	9.4	1.7	17.4	ns
t_{PHL}		0.3	2.0	5.9	1.2	10.9	0.2	2.6	10.1	1.5	18.6	
t_{PLH}	Propagation Delay, CIB to S1 (Figure 1)	0.2	0.8	2.5	1.2	4.7	0.2	1.2	4.1	1.6	7.6	ns
t_{PHL}		0.3	1.0	3.0	1.0	5.5	0.2	1.2	4.5	1.4	8.4	
t_{PLH}	Propagation Delay, CIB to S2 (Figure 1)	0.2	1.8	4.5	1.2	8.4	0.2	2.6	7.8	1.6	14.4	ns
t_{PHL}		0.3	1.9	4.8	1.0	8.8	0.2	2.6	7.8	1.4	14.6	
t_{PLH}	Propagation Delay, CIB to COB (Figure 1)	0.2	1.7	4.3	1.2	7.9	0.3	2.4	7.3	1.7	13.6	ns
t_{PHL}		0.3	1.9	4.7	1.2	8.7	0.2	2.8	8.1	1.5	15.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

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INPUT LOAD FACTORS

IUL	Input Unit Load Factors	A1, B1, A2, B2	1.0
		CIB	4.0

SWITCHING WAVEFORMS

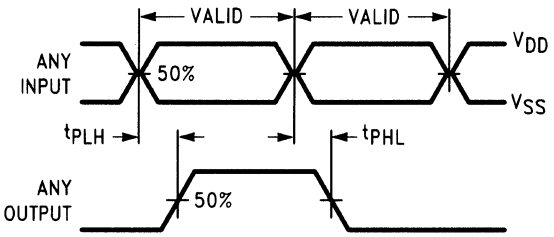
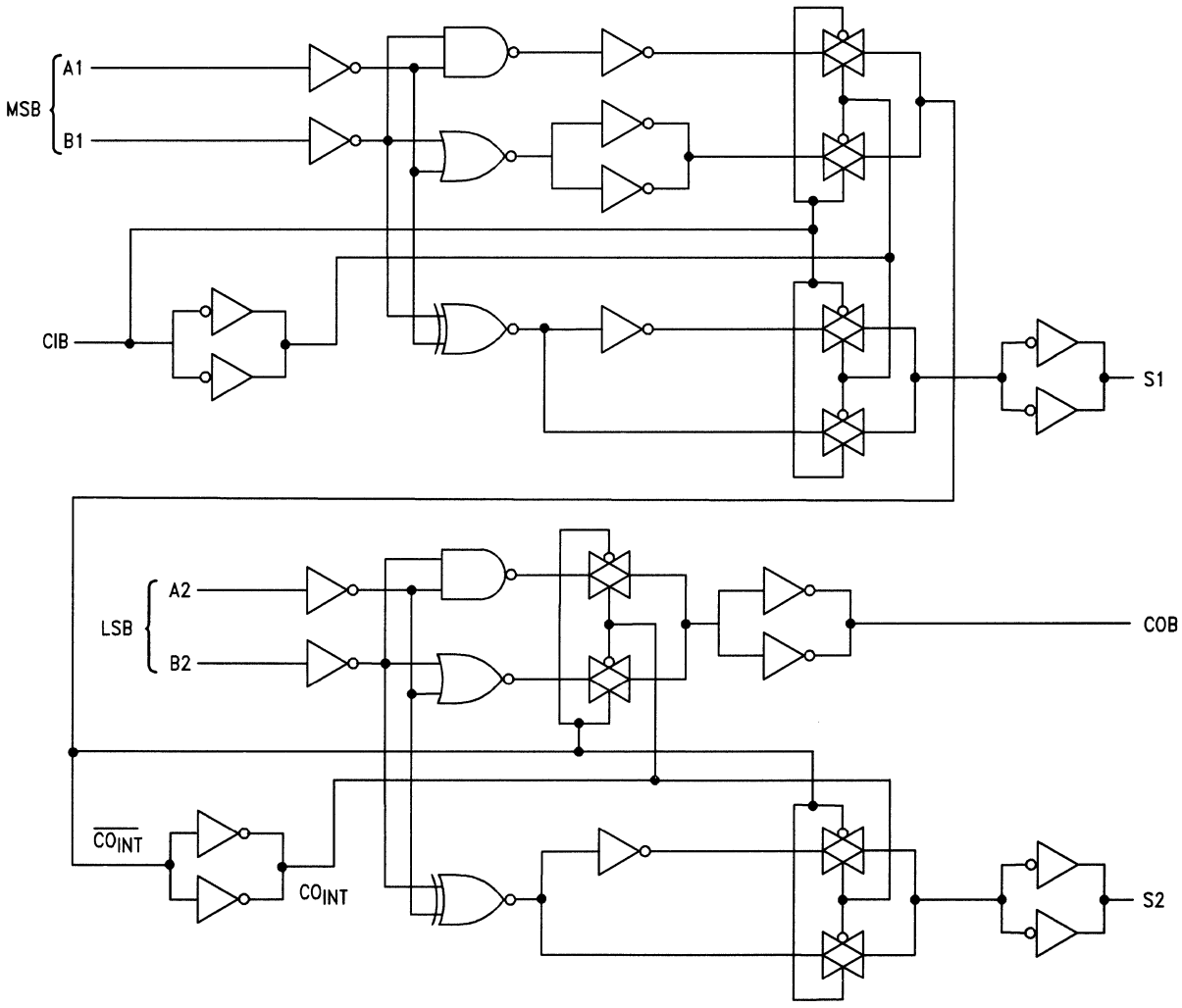


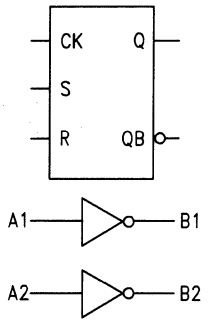
Figure 1

FUNCTION DIAGRAM



C082

Gated R-S Flip-Flop and 2 Inverters



Primary Cells: 2
Netlist Format:
$SUBU C082
Q QB B1 B2 / CK S R A1 A2

FUNCTION TABLE

CK	S	R	Q	QB	Function Performed
L	X	X	No Change		Data Retained
H	L	L	No Change		Data Retained
H	L	H	L	H	Output Q is Reset
H	H	L	H	L	Output Q is Set
H	H	H	H	H	*

U = Undefined
X = Don't Care
*Both outputs will remain high as long as S, R, and CK are high, but output states are unpredictable if S and R go low simultaneously or if CK goes low while S and R are high.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	1.2	2.7	2.1	5.0	0.4	1.6	4.3	2.6	8.0	ns
t_{PHL}		0.4	2.2	5.4	2.1	10.0	0.8	3.0	8.6	3.8	16.0	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	1.2	2.7	2.1	5.0	0.4	1.6	4.3	2.6	8.0	ns
t_{PHL}		0.4	2.2	5.4	2.1	10.0	0.8	3.0	8.6	3.8	16.0	
t_{PLH}	Propagation Delay, S to Q (Figure 2)	0.4	1.2	2.7	2.1	5.0	0.4	1.6	4.3	2.6	8.0	ns
t_{PHL}	Propagation Delay, S to QB (Figure 2)	0.4	2.2	5.4	2.1	10.0	0.8	3.0	8.6	3.8	16.0	ns
t_{PHL}	Propagation Delay, R to Q (Figure 3)	0.4	2.2	5.4	2.1	10.0	0.4	3.0	8.6	3.8	16.0	ns
t_{PLH}	Propagation Delay, R to QB (Figure 3)	0.4	1.2	2.7	2.1	5.0	0.8	1.6	4.3	2.6	8.0	ns
t_{PLH}	Propagation Delay, A to B (Figure 4)	0.4	0.8	1.7	1.8	3.2	0.4	0.8	2.2	2.2	4.0	ns
t_{PHL}		0.4	1.0	1.8	1.8	3.4	0.4	0.8	2.2	2.2	4.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	S, R, A1, A2	1.0
		CK	2.0

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SWITCHING WAVEFORMS

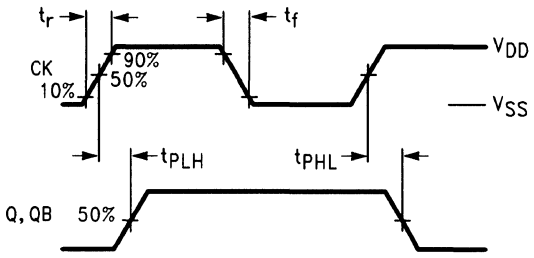


Figure 1

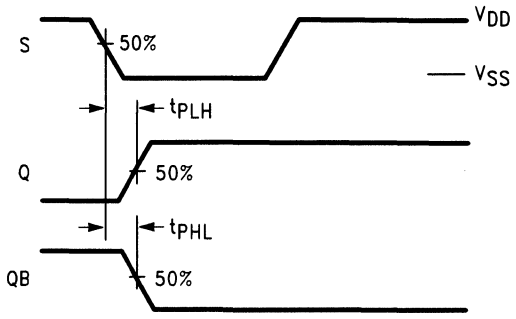


Figure 2

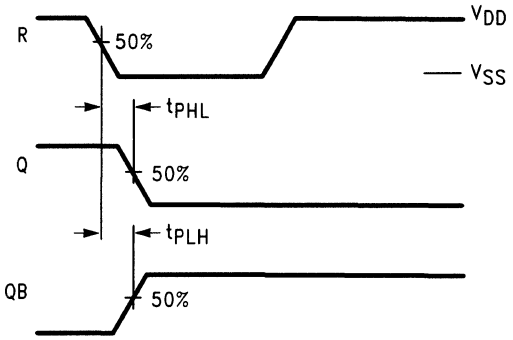


Figure 3

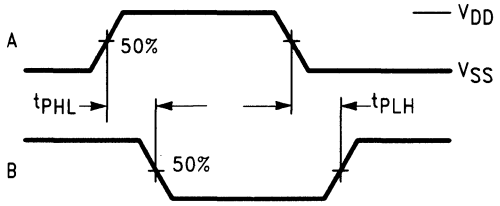
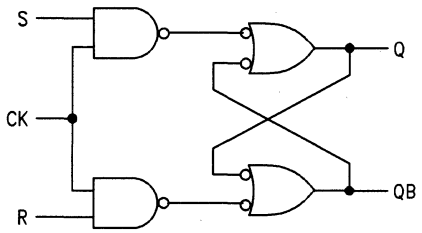
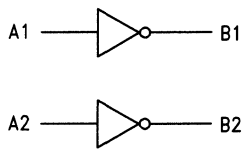


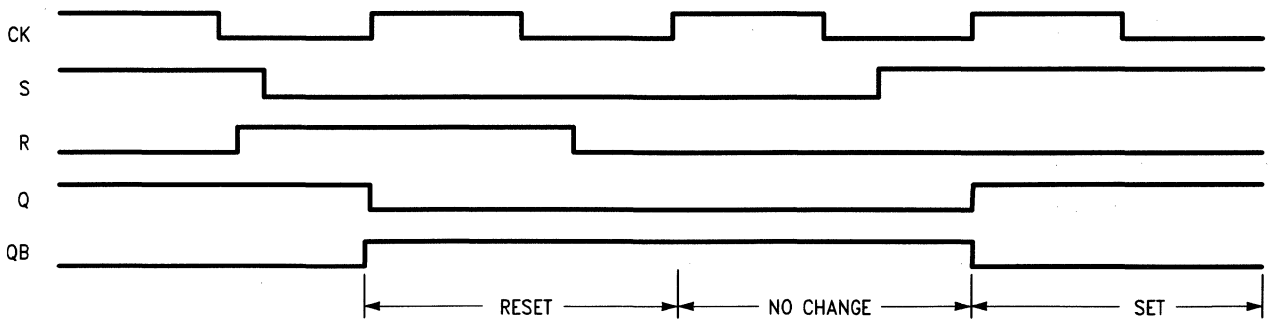
Figure 4

LOGIC DIAGRAMS



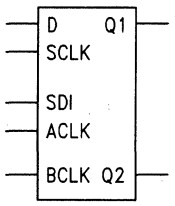


TIMING DIAGRAM



C084

Shift Register Latch LSSD



Primary Cells: 3
Netlist Format:
$SUBU C084
Q1 Q2 / D SCLK SDI ACLK BCLK

Pin Names:
D—Data Input
SCLK—System Latch Enable; Latch Enable for Q1
SDI—Scan Data Input
ACLK—Scan Clock A; Latch Enable for Q1
BCLK—Scan Clock B; Latch Enable for Q2
Q1—Latch 1 Output
Q2—Latch 2 Output

FUNCTION TABLE†

Inputs					Outputs		Mode	Function
SCLK	D	ACLK	SDI	BCLK	Q1	Q2		
H	L/H	L	X	L	L/H	No Change	Normal	Latch 1 is in its transparent mode; Q1 = D.
L	X	H	L/H	L	L/H	No Change	Scan	Latch 1 is in its transparent mode; Q1 = SDI.
X	X	X	X	H	Q1	Q1	Normal/Scan	Latch 2 is in its transparent mode; Q2 = Q1.
L	X	L	X	L	No Change	No Change	Normal/Scan	Latch 1 & 2 data are latched.

†See Section 7 for a description of LSSD.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, D to Q1 (Figure 1)	0.5	1.6	4.8	1.9	8.9	0.5	2.2	8.1	1.9	15.0	ns
t_{PHL}		0.4	1.6	4.8	2.0	8.9	0.4	2.0	8.1	2.0	15.0	
t_{PLH}	Propagation Delay, SCLK to Q1 (Figure 2)	0.5	2.0	5.9	1.9	10.9	0.5	2.6	10.1	1.9	18.6	ns
t_{PHL}		0.4	2.0	5.7	2.0	10.5	0.4	2.4	9.4	2.0	17.4	
t_{PLH}	Propagation Delay, BCLK to Q2 (Figure 2)	0.4	1.4	3.9	1.9	7.2	0.2	1.8	6.4	1.6	11.8	ns
t_{PHL}		0.5	1.3	3.6	2.0	6.7	0.2	1.6	5.7	0.8	10.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

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TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5V, T_A = −40 to +85°C)

Symbol	Parameter		HCA6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to SCLK (Figure 3)	5.8	15.0	ns
		SDI to ACLK (Figure 3)	7.9	17.2	
t_h	Hold Time	SCLK to D (Figure 3)	2.0	4.0	ns
		ACLK to SDI (Figure 3)	1.5	3.0	
t_w	Pulse Width	SCLK (Figure 3)	7.8	14.0	ns
		ACLK (Figure 3)	8.2	17.4	
		BCLK (Figure 3)	4.3	8.6	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	D, SCLK, SDI	1.0
		ACLK,BCLK	2.0

SWITCHING WAVEFORMS

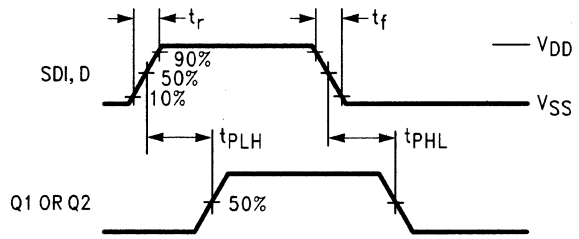


Figure 1

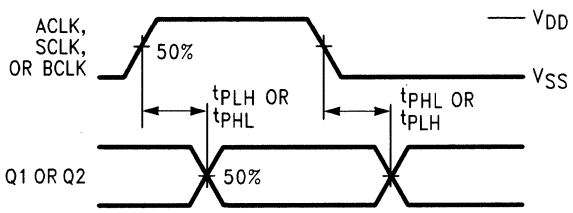


Figure 2

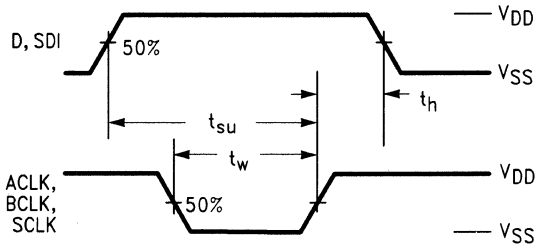
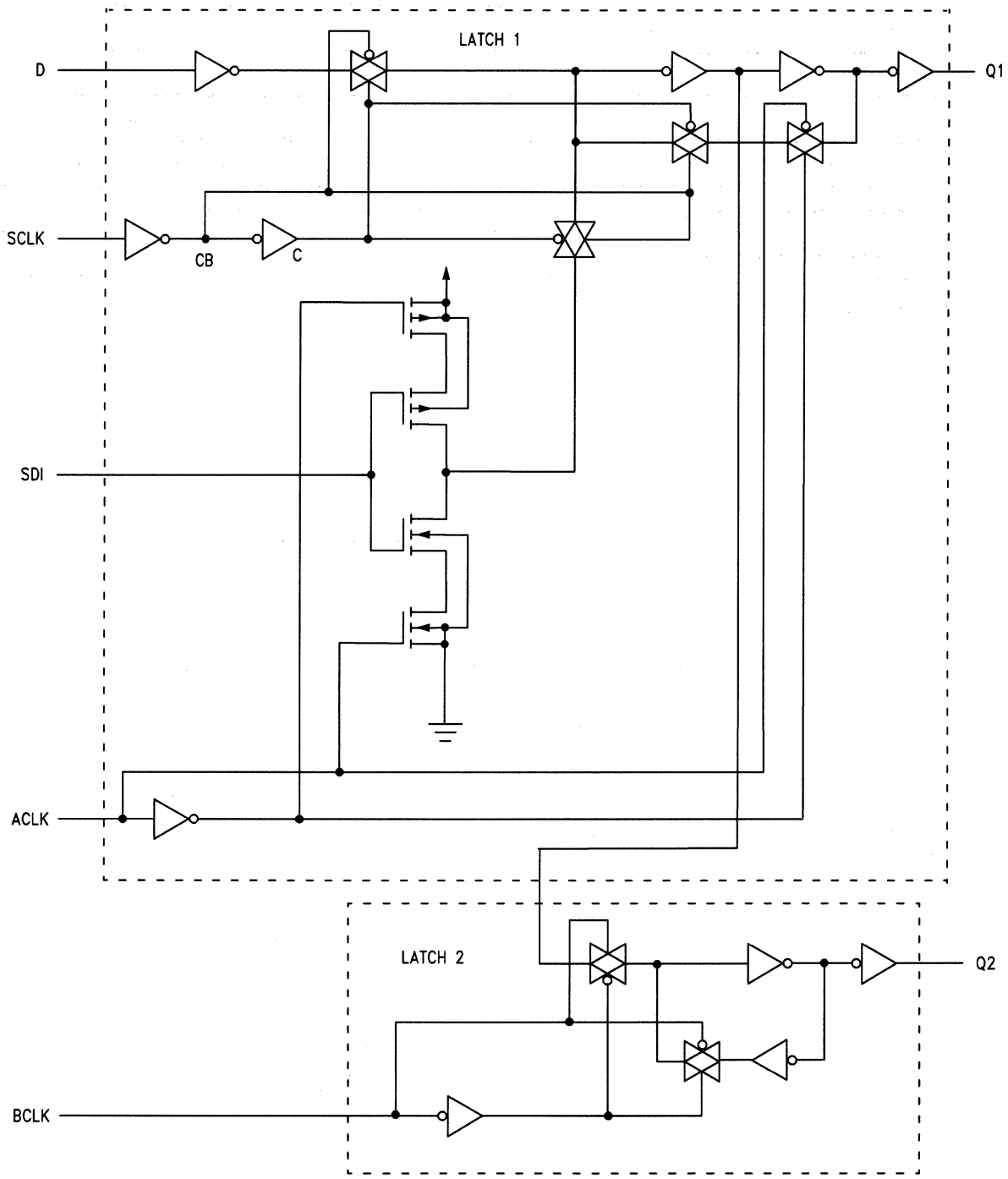
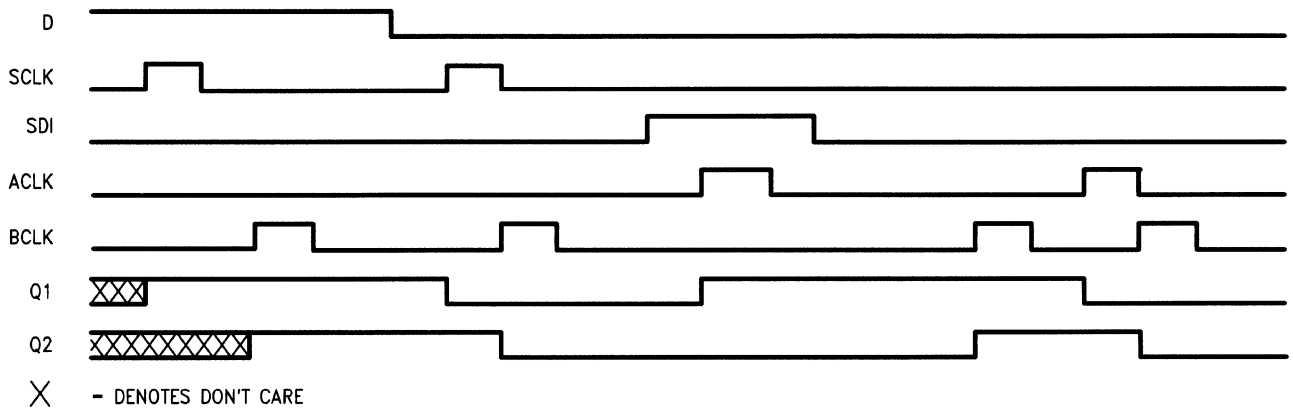


Figure 3

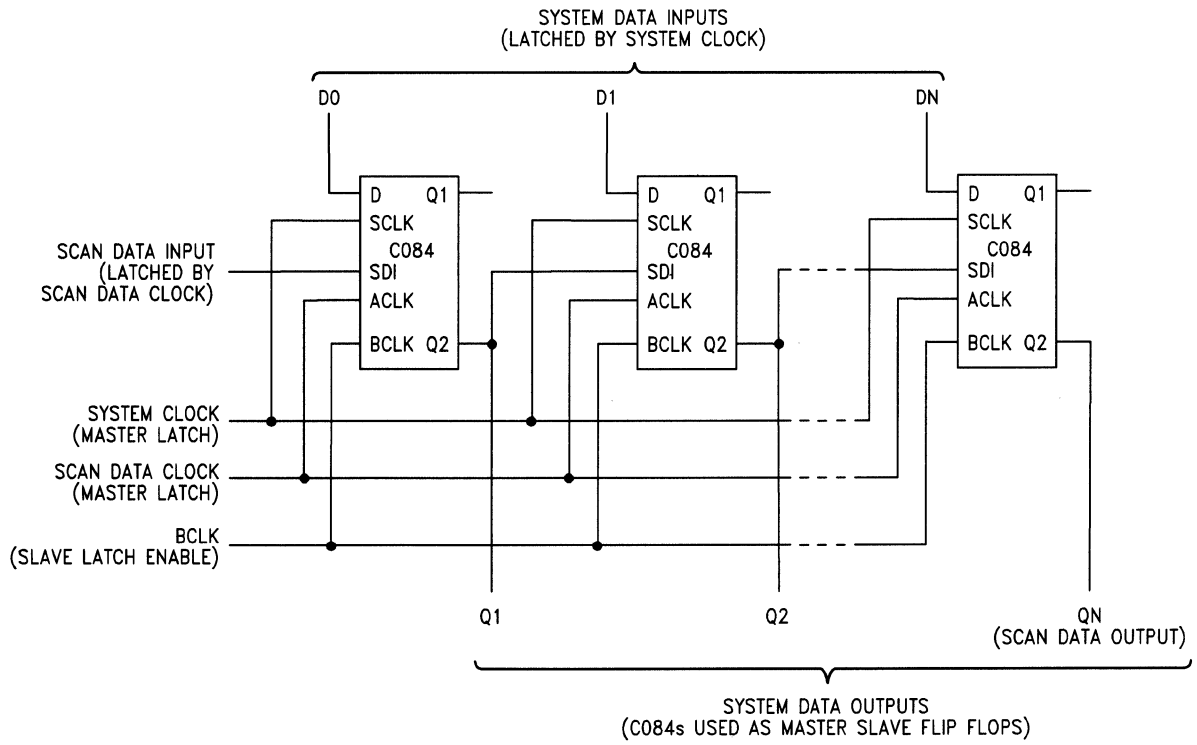
FUNCTION DIAGRAM
C084 Shift Register Latch LSSD



TIMING DIAGRAM

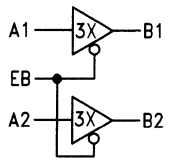


APPLICATION EXAMPLE



C085

Dual Non-Inverting 3-State Driver with 3X Outputs



Primary Cells: 3
Netlist Format:
$SUBU C085
B1 B2 / A1 A2 EB

FUNCTION TABLE

EB	A	B
L	L	L
L	H	H
H	X	Z

Z = High Impedance
X = Don't Care

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.2	0.8	2.3	0.9	4.2	0.2	1.0	3.6	0.8	6.6	ns
t_{PHL}		0.2	0.7	2.1	0.9	3.8	0.3	1.0	3.6	1.0	6.6	
t_{PLZ}	Propagation Delay, EB to B (Figure 2)	—	1.0	2.9	—	5.4	—	1.4	5.0	—	9.4	ns
t_{PHZ}		—	0.9	2.5	—	4.7	—	1.4	4.5	—	8.4	
t_{PZL}		0.2	1.5	4.4	0.9	8.2	0.3	2.2	7.9	1.0	14.6	
t_{PZH}		0.2	1.4	3.8	0.9	7.1	0.2	2.0	6.7	0.8	12.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	EB	1.0
		A1, A2	2.0

SWITCHING WAVEFORMS

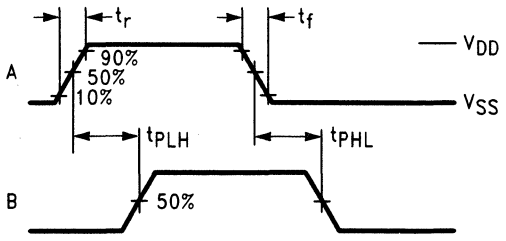
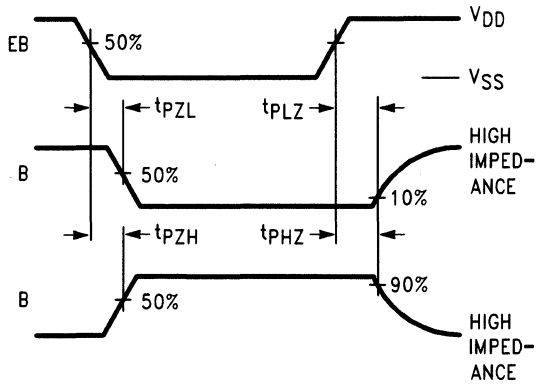


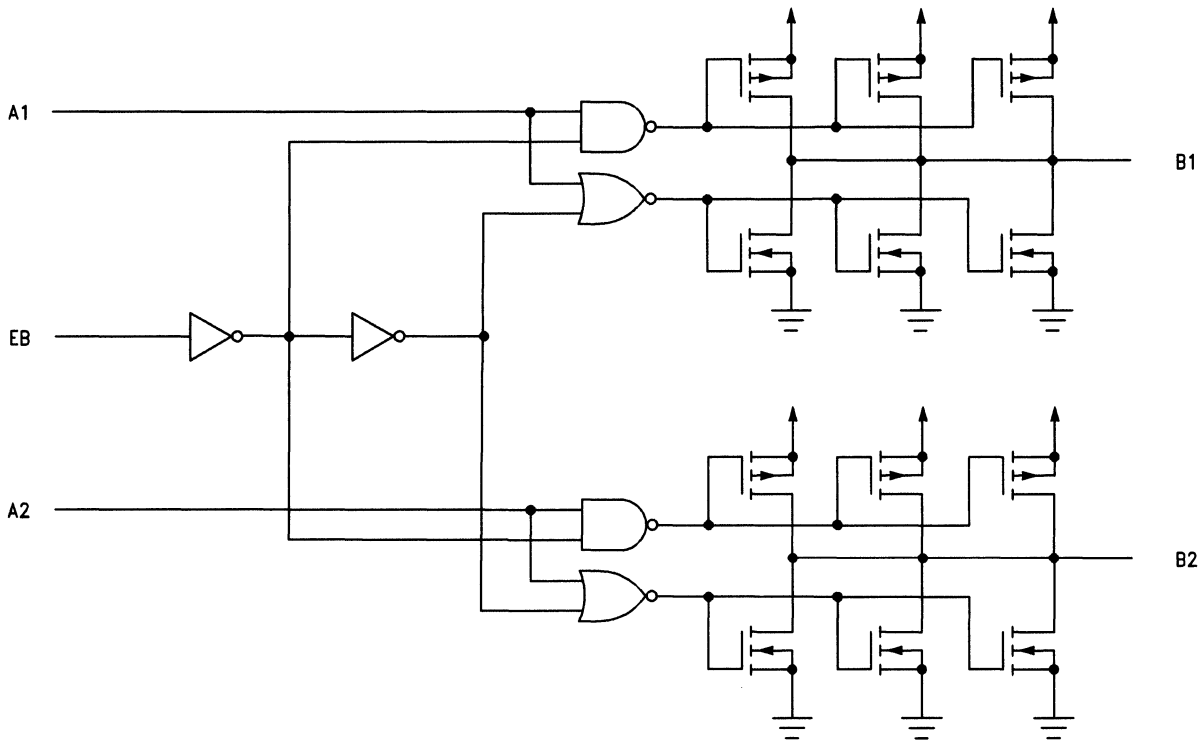
Figure 1



Refer to Figure 7 in Section 9.
Figure 2

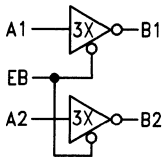
11

FUNCTION DIAGRAM



C086

Dual Inverting 3-State Driver with 3X Outputs



Primary Cells: 3
Netlist Format:
$SUBU C086
B1 B2 / A1 A2 EB

FUNCTION TABLE

EB	A	B
L	L	H
L	H	L
H	X	Z

Z = High Impedance
X = Don't Care

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A to B (Figure 1)	0.2	1.0	3.0	0.8	5.6	0.3	1.4	5.2	1.2	9.8	ns
t_{PHL}		0.2	1.0	2.9	0.9	5.4	0.8	1.2	5.0	0.8	9.2	
t_{PLZ}	Propagation Delay, EB to B (Figure 2)	—	1.0	2.9	—	5.4	—	2.4	5.1	—	9.4	ns
t_{PHZ}		—	0.8	2.4	—	4.5	—	1.2	4.4	—	8.2	
t_{PZL}		0.2	1.7	4.5	0.8	8.3	0.8	2.2	8.0	0.8	14.8	
t_{PZH}		0.2	1.3	3.7	0.9	6.8	0.3	1.8	6.5	1.2	12.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A1, A2, EB	1.0

SWITCHING WAVEFORMS

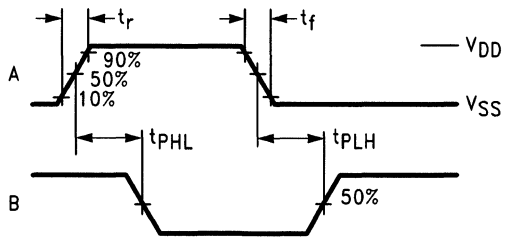
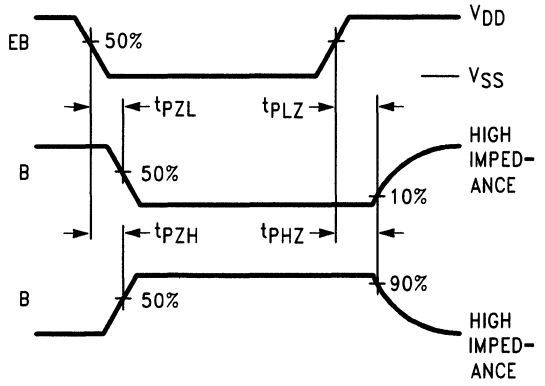


Figure 1



Refer to Figure 7 in Section 9.
Figure 2

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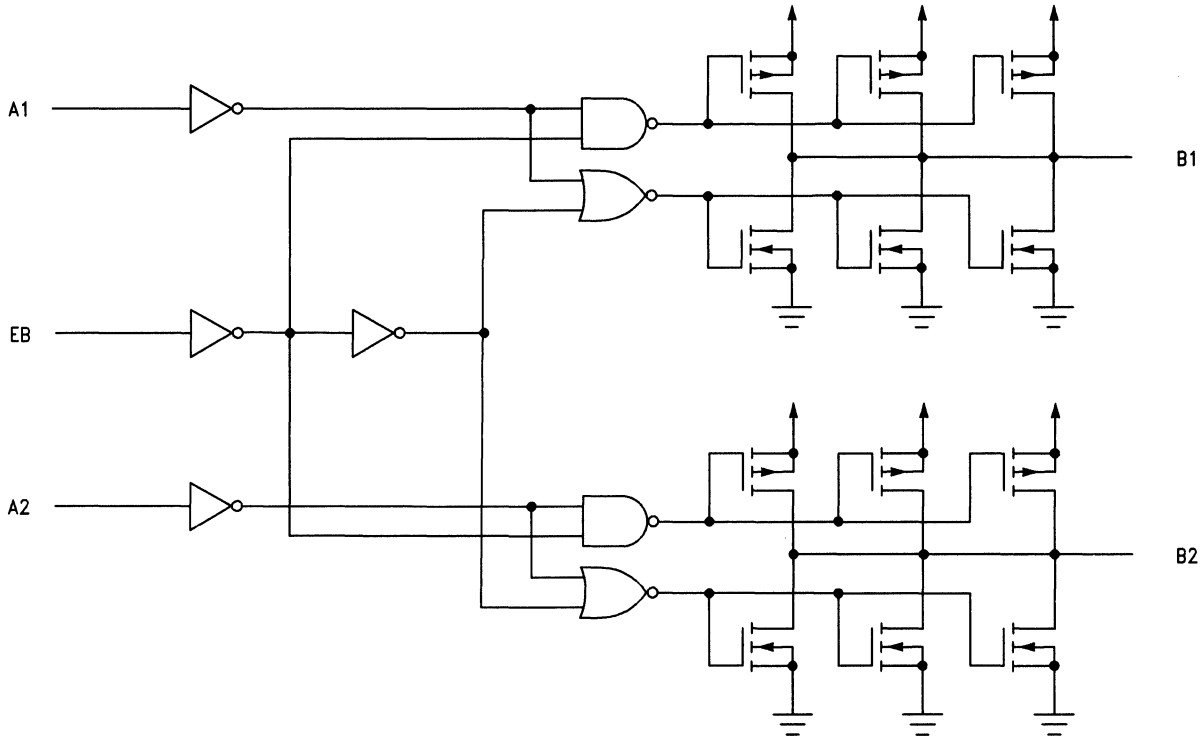
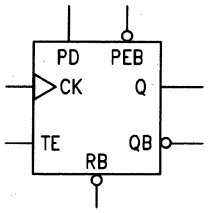
FUNCTION DIAGRAM



C087

Toggle Enable Flip-Flop with Reset (L) and Synchronous Parallel Load (L)



Primary Cells: 4
Netlist Format:
$SUBU C087
Q QB / PEB PD CK TE RB

Pin Names:
PEB—Preset Enable Bar (Active Low)
PD—Preset Data Input
CK—Clock Input
TE—Toggle Enable
RB—Asynchronous Reset (Active Low)
Q, QB—Data Outputs

FUNCTION TABLE

CK	RB	TE	PEB	PD	Q	QB	Function Description
X	L	X	X	X	L	H	Asynchronous reset of flip-flop outputs. RB overrides CK and PEB inputs.
⌐	H	X	L	L/H	L/H	H/L	Preset data at the PD input is loaded synchronously into the flip-flop.
X	H	L	H	X	No Change	No Change	Disabled Mode.
⌐	H	H	H	X	Toggle	Toggle	Outputs toggle on the rising edge of the clock.
¬	H	X	X	X	No Change	No Change	Outputs are not affected on the falling edge of the clock.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	45	—	—	—	—	31	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.2	2.6	6.9	1.2	12.8	0.2	3.2	11.8	1.8	21.8	ns
t_{PHL}		0.2	2.4	6.3	1.4	11.6	0.4	3.2	10.8	1.6	20.0	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	1.8	4.6	2.2	8.6	0.4	2.4	8.2	2.6	15.2	ns
t_{PHL}		0.6	2.0	5.3	2.2	9.8	0.4	2.4	8.1	3.0	15.0	
t_{PHL}	Propagation Delay, RB to Q (Figure 2)	0.2	2.4	6.5	1.4	12.0	0.4	3.2	11.5	1.6	21.2	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 2)	0.4	2.0	5.3	2.2	9.8	0.4	2.6	9.2	2.6	17.0	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

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TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to 85°C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	TE to CK (Figure 3)	10.8	20.0	ns
		PD to CK (Figure 4)	6.2	11.4	
		PEB to CK (Figure 5)	7.6	14.2	
t_h	Hold Time	CK to TE (Figure 3)	0.0	3.4	ns
		CK to PD (Figure 4)	0.0	3.4	
		CK to PEB (Figure 5)	0.0	0.0	
t_{rec}	Recovery Time	RB to CK(Figure 2)	10.0	16.0	ns
t_w	Pulse Width	CK $t_{w(H)}$ (Figure 1)	11.0	16.0	ns
		CK $t_{w(L)}$ (Figure 1)	12.0	16.0	
		RB (Figure 2)	9.0	18.8	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—PEB, PD, CK, TE, and RB	1.0

SWITCHING WAVEFORMS

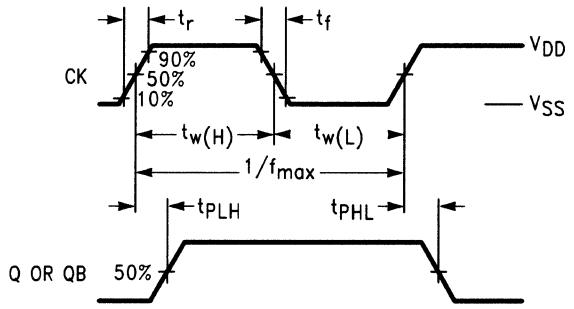


Figure 1

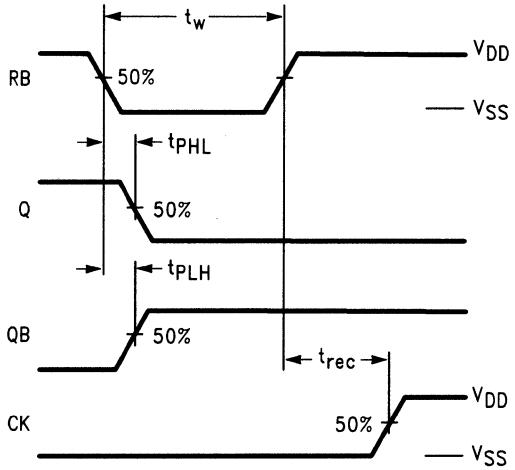


Figure 2

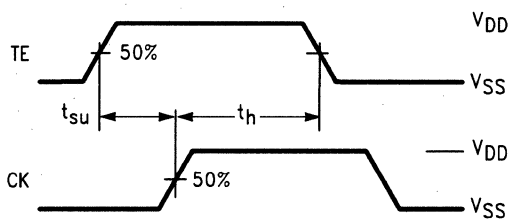


Figure 3

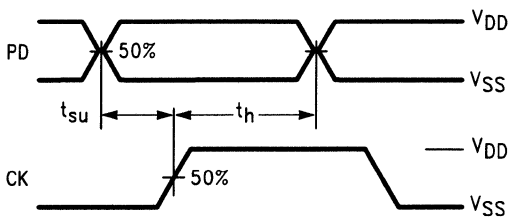


Figure 4

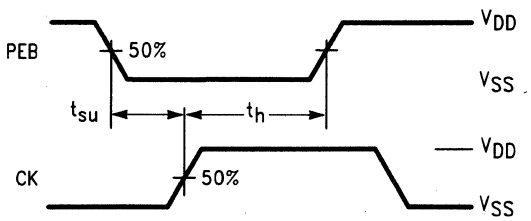
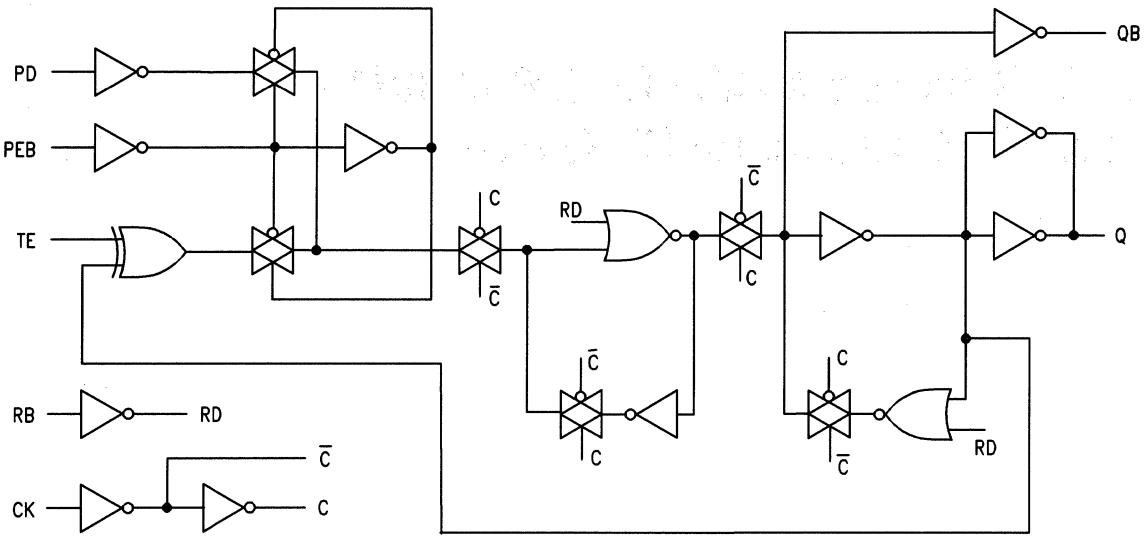


Figure 5

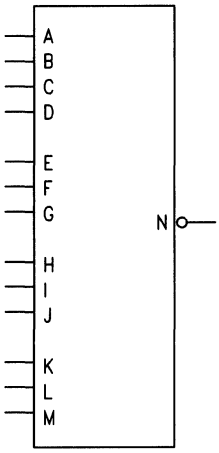
FUNCTION DIAGRAM

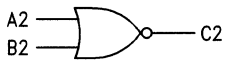


C088

4-3-3-3 Input 4-Wide OR-AND-Invert & 2-Input NOR Gate

Primary Cells: 4
Netlist Format:
$SUBU C088
N C2 / A B C D E F G H I J K L M A2 B2





$N = \overline{(A+B+C+D)\cdot(E+F+G)\cdot(H+I+J)\cdot(K+L+M)}$
$C2 = \overline{A2+B2}$

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A through M to N (Figure 1)	0.4	1.2	4.6	2.0	8.6	0.4	1.6	7.7	2.4	14.2	ns
t_{PHL}		0.8	1.6	5.2	3.6	9.6	0.6	1.8	8.0	3.8	14.8	
t_{PLH}	Propagation Delay, A2, B2 to C2 (Figure 1)	0.8	1.0	2.8	3.6	5.2	0.8	1.2	4.3	5.0	8.0	ns
t_{PHL}		0.4	0.8	1.8	1.8	3.4	0.4	0.8	2.4	1.2	4.4	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A through M, A2, B2	1.0

SWITCHING WAVEFORMS

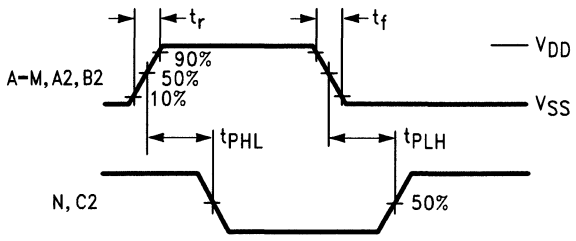
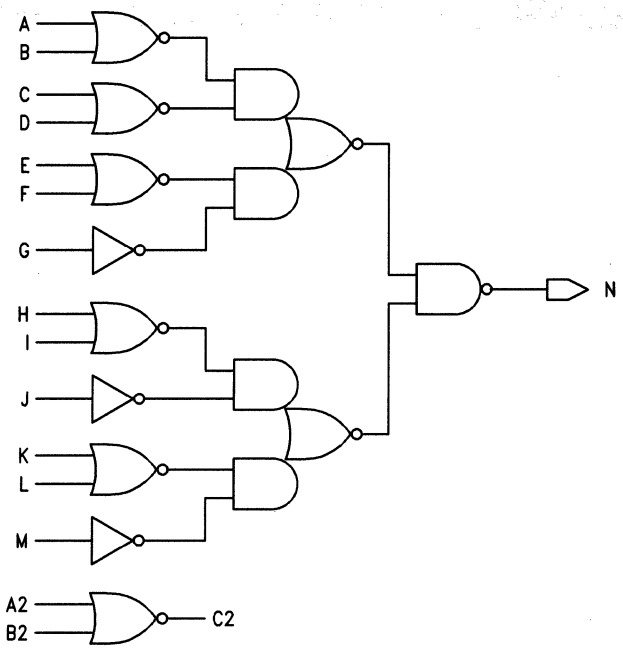


Figure 1

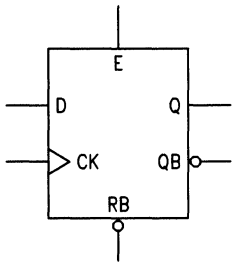
11

LOGIC DIAGRAM



C090

D Flip-Flop with Reset (L) and 3-State Q



Primary Cells: 4
Netlist Format:
$SUBU C090
Q QB / E D CK RB

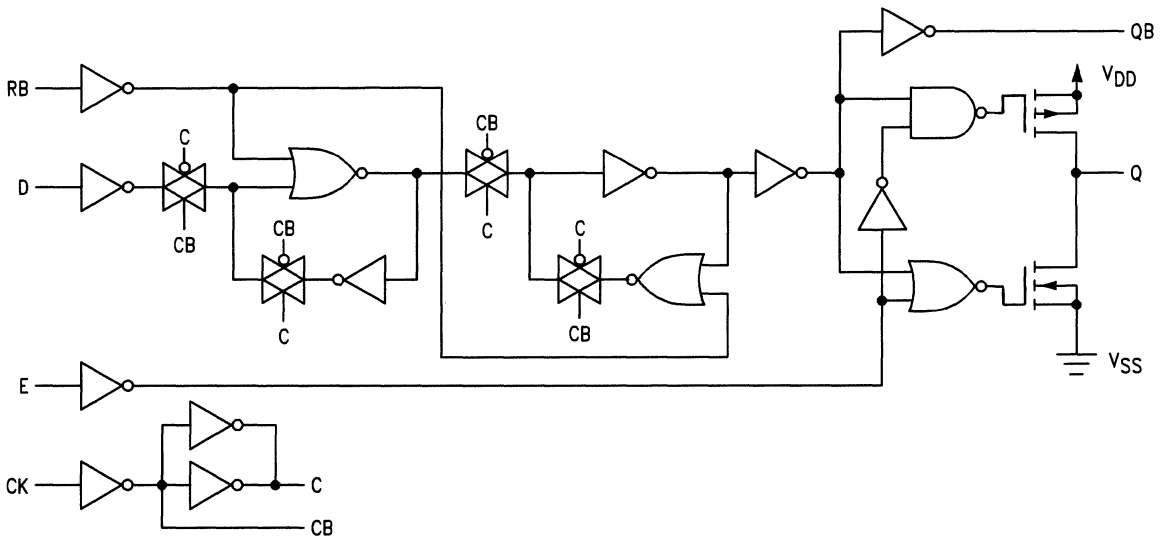
Pin Names:
E—Output Enable (Q output only)
D—Data Input
CK—Clock Input
RB—Asynchronous Reset Bar (Active Low)
Q, QB—Data Outputs

FUNCTION TABLE

CK	D	RB	E	Q	QB
X	X	X	L	Z	X
X	X	L	H	L	H
↗	L	H	H	L	H
↗	H	H	H	H	L
↘	X	H	H	No Change	No Change

Z = High-Impedance State
X = Don't Care

FUNCTION DIAGRAM



SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	60	—	—	—	—	35	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.4	4.0	10.2	1.8	18.8	0.4	4.8	13.8	2.6	25.6	ns
t_{PHL}		0.4	4.0	9.4	2.0	17.4	0.4	4.4	13.6	2.2	25.2	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.4	3.4	8.0	2.0	14.8	0.4	3.8	11.6	2.8	21.4	ns
t_{PHL}		0.4	3.6	9.2	2.0	17.0	0.4	4.2	12.0	2.2	22.2	
t_{PHL}	Propagation Delay, RB to Q (Figure 2)	0.4	4.0	9.4	2.0	17.4	0.4	4.6	14.4	2.2	26.6	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 2)	0.4	3.4	8.0	2.0	14.8	0.4	4.0	12.3	2.8	22.8	ns
t_{PLZ}	Propagation Delay, E to Q (Figure 3)	—	1.2	2.3	—	4.2	—	1.4	3.6	—	6.6	ns
t_{PZL}		0.4	2.0	4.4	2.0	8.2	0.4	2.4	6.4	2.2	11.8	
t_{PHZ}	Propagation Delay, E to Q (Figure 3)	—	1.4	3.0	—	5.6	—	1.8	5.0	—	9.2	ns
t_{PZH}		0.4	2.2	5.2	1.8	9.6	0.4	2.8	8.0	2.6	14.8	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_P(total) = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5V, T_A = −40° to 85°C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	D to CK (Figure 4)	5.6	9.8	ns
t_h	Hold Time	CK to D (Figure 4)	2.8	4.6	ns
t_{rec}	Recovery Time	RB to CK (Figure 2)	4.2	6.8	ns
t_w	Pulse Width	CK, t_w(L)(Figure 1)	8.2	14.2	ns
		CK, t_w(H) (Figure 1)	7.8	12.6	
		RB (Figure 2)	8.8	11.4	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—E, D, CK, RB	1.0

11

SWITCHING WAVEFORMS

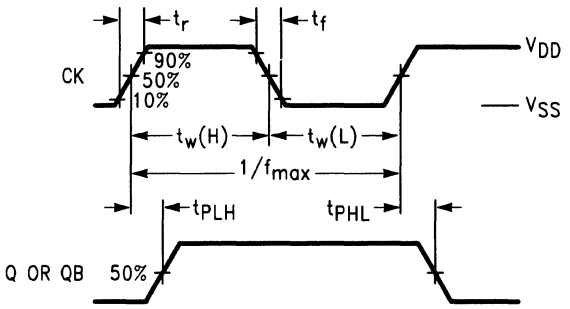


Figure 1

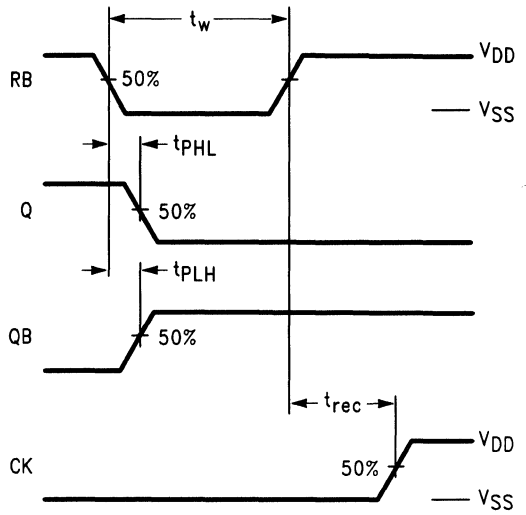


Figure 2

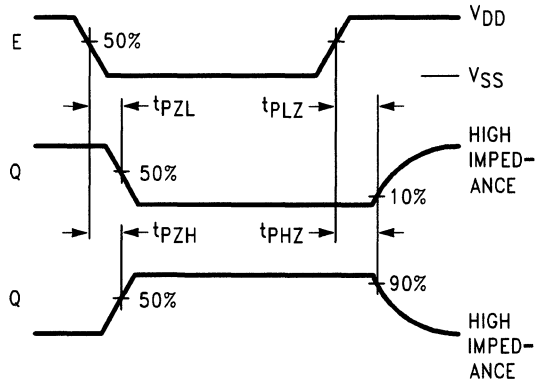


Figure 3

Refer to Figure 7 in Section 9.

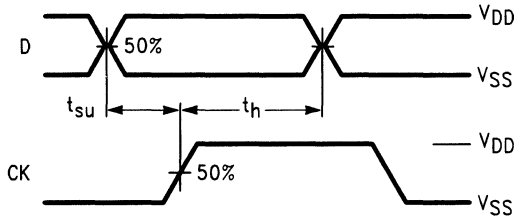
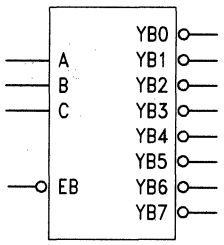


Figure 4

C091

1-of-8 Decoder with Output (L) & Enable (L)



Primary Cells: 6
Netlist Format:
$SUBU C091
YB0 YB1 YB2 YB3 YB4 &
YB5 YB6 YB7 / A B C EB

Pin Names:
A—Address Input (MSB)
B—Address Input
C—Address Input (LSB)
EB—Output Enable—(Active Low)
YB0–YB7—Decoded Outputs (Active Low)

FUNCTION TABLE

EB	A	B	C	YB0	YB1	YB2	YB3	YB4	YB5	YB6	YB7
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	H	H	H	H	H	H	H	H

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, EB to any YB (Figure 1)	0.6	2.4	5.9	4.0	11.0	0.6	2.8	9.2	3.0	17.0	ns
t_{PHL}		0.8	3.4	9.2	4.0	17.0	0.8	4.2	14.1	4.6	26.0	
t_{PLH}	Propagation Delay, A to YB—0, 1, 2, 3 (Figure 2)	0.6	1.8	4.3	4.0	8.0	0.6	2.0	5.9	3.0	11.0	ns
t_{PHL}		0.8	2.0	5.9	4.0	11.0	0.8	2.2	7.0	4.6	13.0	
t_{PLH}	Propagation Delay, A to YB—4, 5, 6, 7 (Figure 2)	0.6	2.2	4.9	4.0	9.0	0.6	2.8	9.5	3.0	17.6	ns
t_{PHL}		0.8	2.8	6.8	4.0	12.6	0.8	3.0	9.5	4.6	17.6	
t_{PLH}	Propagation Delay, B to YB—0, 1, 4, 5 (Figure 2)	0.6	2.4	5.9	4.0	11.0	0.6	2.8	8.6	3.0	16.0	ns
t_{PHL}		0.8	3.4	9.2	4.0	17.0	0.8	4.2	13.5	4.6	25.0	
t_{PLH}	Propagation Delay, B to YB—2, 3, 6, 7 (Figure 2)	0.6	1.8	4.9	4.0	9.0	0.6	2.2	7.4	3.0	13.6	ns
t_{PHL}		0.8	3.0	7.9	4.0	14.6	0.8	3.6	11.7	4.6	21.6	
t_{PLH}	Propagation Delay, C to YB—0, 2, 4, 6 (Figure 2)	0.6	2.4	5.9	4.0	11.0	0.6	2.8	8.6	3.0	16.0	ns
t_{PHL}		0.8	3.4	9.2	4.0	17.0	0.8	4.2	13.5	4.6	25.0	
t_{PLH}	Propagation Delay, C to YB—1, 3, 5, 7 (Figure 2)	0.6	1.8	4.9	4.0	9.0	0.6	2.2	7.4	3.0	13.6	ns
t_{PHL}		0.8	3.0	7.9	4.0	14.6	0.8	3.6	11.7	4.6	21.6	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C, EB	1.0

SWITCHING WAVEFORMS

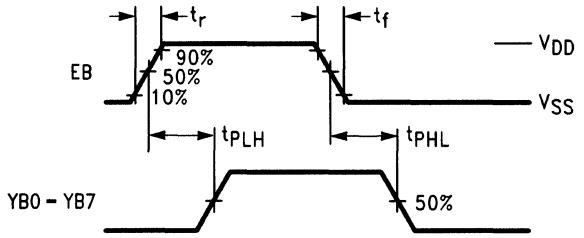


Figure 1

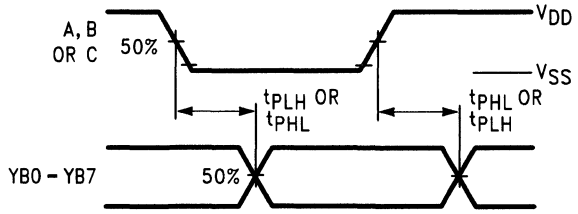
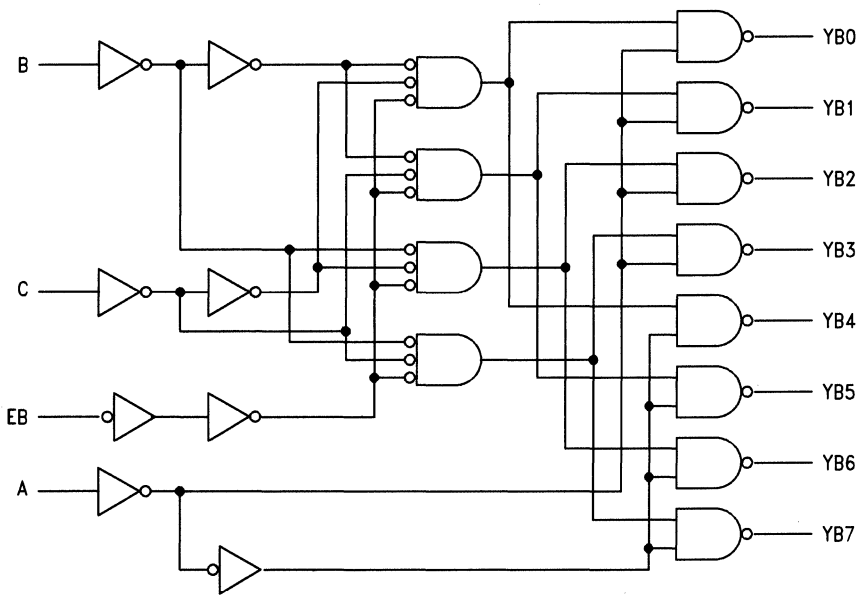


Figure 2

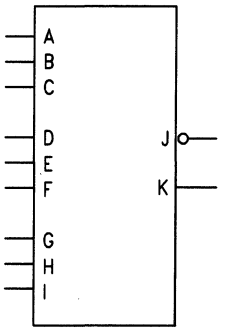
LOGIC DIAGRAM



C093

3 Input 3-Wide OR-AND-Invert

Primary Cells: 3
Netlist Format:
$SUBU C093
J K / A B C D E F G H I



$J = \overline{(A+B+C)\cdot(D+E+F)\cdot(G+H+I)}$
$K = (A+B+C)\cdot(D+E+F)\cdot(G+H+I)$

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A through I, to J (Figure 1)	0.2	1.6	5.9	1.4	11.0	0.2	2.0	9.2	1.8	17.0	ns
t_{PHL}		0.2	1.6	6.6	1.6	12.2	0.2	2.0	10.9	1.8	20.2	
t_{PLH}	Propagation Delay, A through I, to K (Figure 2)	0.2	2.0	7.8	1.0	14.4	0.2	2.6	13.2	1.2	24.4	ns
t_{PHL}		0.2	2.0	7.3	1.0	13.2	0.2	2.4	11.2	1.0	20.8	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A,B,C,D,E,F,G,H,I	1.0

SWITCHING WAVEFORMS

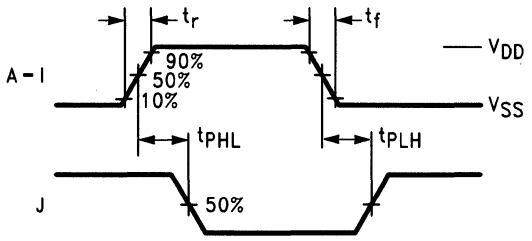


Figure 1

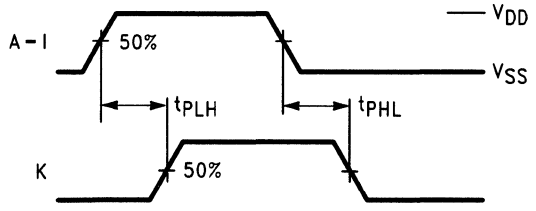
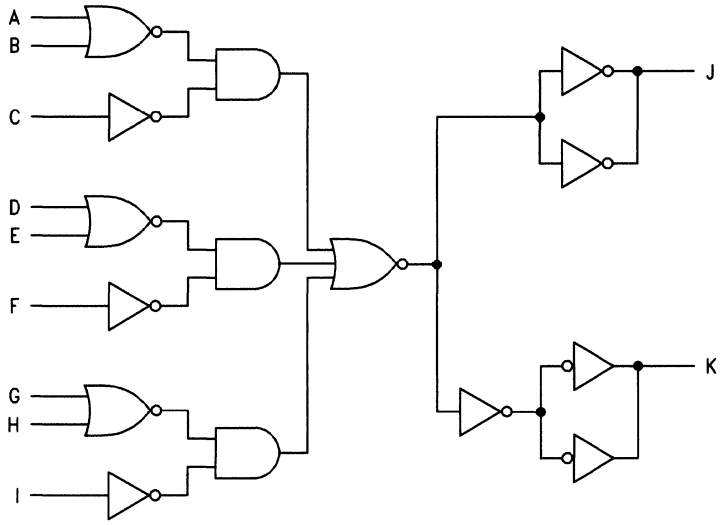


Figure 2

11

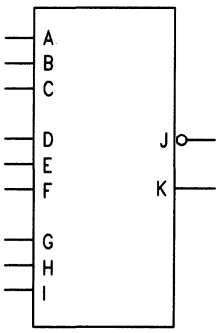
LOGIC DIAGRAM



C094

3 Input 3-Wide AND-OR-Invert

Primary Cells: 4
Netlist Format:
$SUBU C094
J K / A B C D E F G H I



$J = \overline{(A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)}$
$K = (A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)$

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A through I, to J (Figure 1)	0.4	2.2	6.7	1.4	12.4	0.2	2.8	10.6	2.0	19.6	ns
t_{PHL}		0.2	2.2	6.2	0.8	11.4	0.2	2.8	9.6	1.0	17.8	
t_{PLH}	Propagation Delay, A through I, to K (Figure 2)	0.2	2.6	7.6	1.2	14.0	0.2	3.4	12.1	1.4	22.4	ns
t_{PHL}		0.2	2.8	7.6	0.6	14.0	0.2	3.4	11.9	1.0	22.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A,B,C,D,E,F,G,H,I	1.0

SWITCHING WAVEFORMS

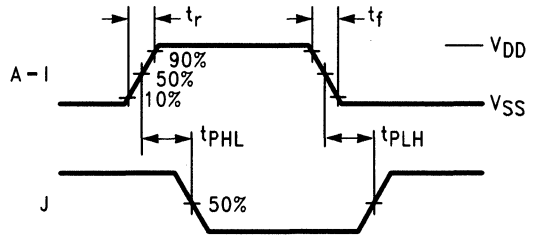


Figure 1

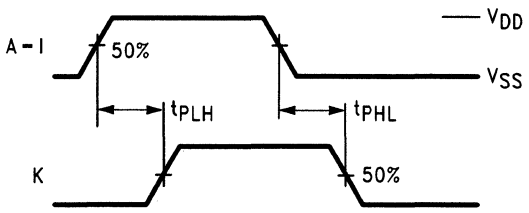
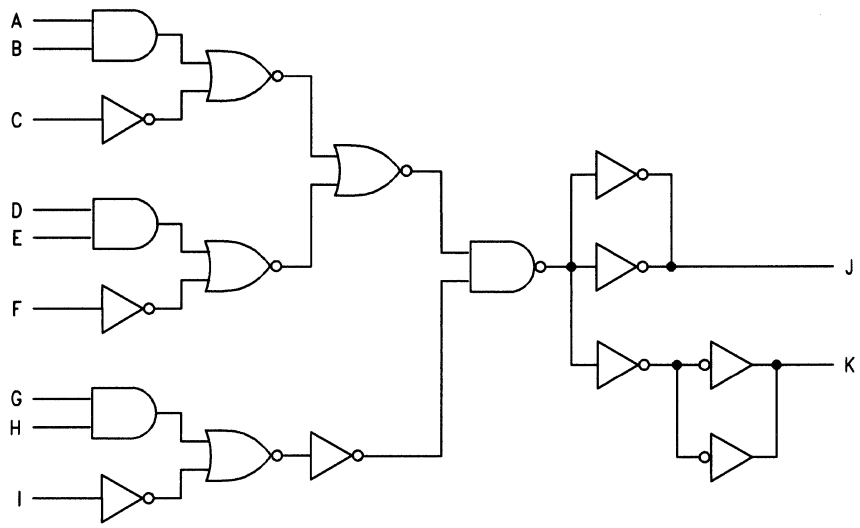


Figure 2

11

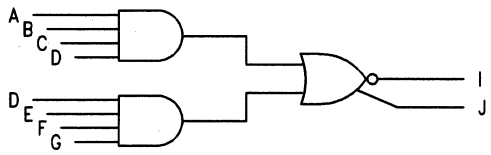
LOGIC DIAGRAM



C095

4-Input 2-Wide AND-OR-Invert

Primary Cells: 3
Netlist Format:
$SUBU C095
I J / A B C D E F G H



$I = \overline{(A \cdot B \cdot C \cdot D)} + \overline{(E \cdot F \cdot G \cdot H)}$
$J = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A through H, to I (Figure 1)	0.8	2.0	5.2	3.6	9.6	0.8	2.6	8.0	4.8	14.8	ns
t_{PHL}		0.6	2.2	5.6	2.4	10.4	0.4	2.6	8.8	2.2	16.2	
t_{PLH}	Propagation Delay, A through H, to J (Figure 2)	0.4	2.2	6.1	1.2	11.2	0.2	2.8	9.7	1.4	18.0	ns
t_{PHL}		0.2	2.2	5.4	1.2	10.0	0.4	2.6	8.5	1.4	15.8	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A, B, C, D, E, F, G, H	1.0

SWITCHING WAVEFORMS

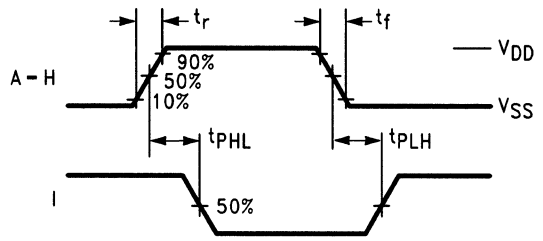


Figure 1

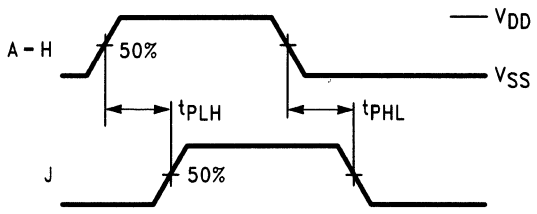
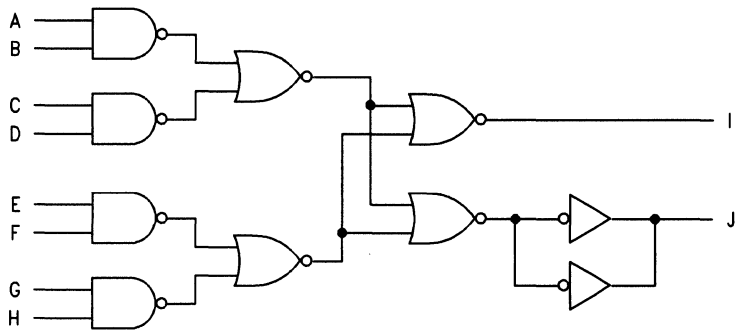


Figure 2

11

LOGIC DIAGRAM

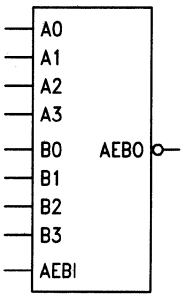


C096

4-Bit Equality Comparator

Primary Cells: 5
Netlist Format:
$SUBU C096
AEBO / A0 A1 A2 A3 &
B0 B1 B2 B3 AEBI

Pin Names:
A0–A3—Data Word A Inputs
B0–B3—Data Word B Inputs
AEBI —A Word Equals B
Word Cascading Input
AEBO —A Word Equals B
Word Output (Active Low)



FUNCTION TABLE

Inputs		Output
Data Words	AEBI	AEBO
A = B	L	L
A ≠ B	L	H
X	H	H

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, A0–A3, B0–B3 to AEBO (Figure 1)	0.4	1.6	5.6	2.0	10.4	0.6	2.2	9.5	2.6	17.6	ns
t_{PHL}		0.8	2.4	7.5	3.4	13.8	0.8	3.0	12.1	3.8	22.4	
t_{PLH}	Propagation Delay, AEBI to AEBO (Figure 2)	0.4	0.8	2.3	2.0	4.2	0.6	1.0	3.6	2.6	6.6	ns
t_{PHL}		0.8	1.2	3.2	3.4	6.0	0.8	1.2	4.4	3.8	8.2	

*See Section 4 for minimum, typical and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—A0–A3, B0–B3, AEBI	1.0

SWITCHING WAVEFORMS

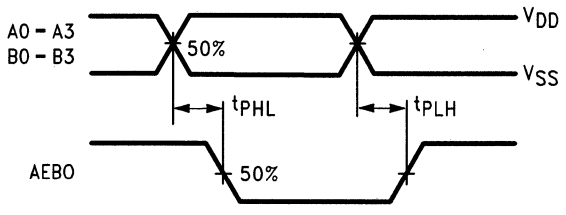


Figure 1

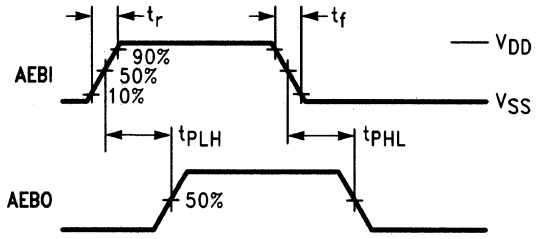
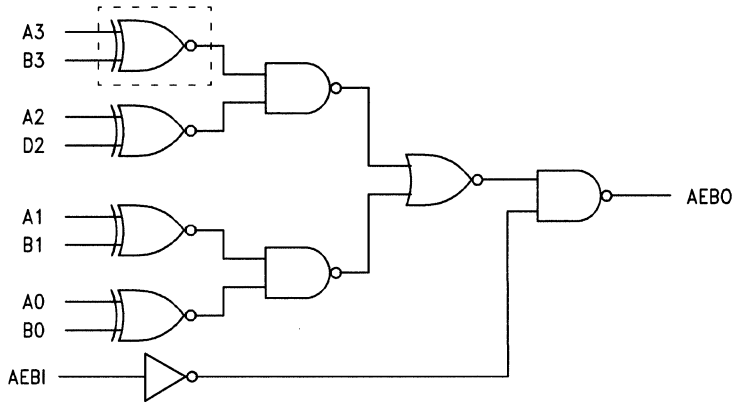
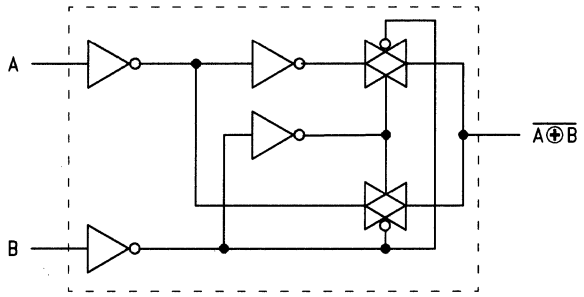


Figure 2

11

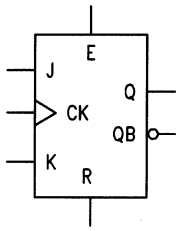
FUNCTION DIAGRAMS





C097

J-K Flip-Flop with 3-State Outputs & Reset



Primary Cells: 4
Netlist Format:
$SUBU C097
Q QB / E J CK K R

Pin Names:
E—Output Enable
J, K—Data Inputs
CK—Clock Input
R—Asynchronous Reset
Q, QB—Data Outputs

FUNCTION TABLE

R	CK	J	K	E	Q	QB
X	X	X	X	L	Z	Z
H	X	X	X	H	L	H
L	⌐	L	L	H	No Change	
L	⌐	L	H	H	L	H
L	⌐	H	L	H	H	L
L	⌐	H	H	H	Toggle	Toggle
L	⌙	X	X	H	No Change	

Z = High-Impedance State
X = Don't Care

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
f	Clock Frequency (50% Duty Cycle) (Figure 1)	—	—	—	—	62	—	—	—	—	35	MHz
t_{PLH}	Propagation Delay, CK to Q (Figure 1)	0.8	2.8	7.7	4.0	14.2	1.0	3.6	12.6	5.2	23.4	ns
t_{PHL}		0.8	2.6	7.1	3.6	13.2	0.8	3.2	11.5	3.6	21.2	
t_{PLH}	Propagation Delay, CK to QB (Figure 1)	0.6	2.8	7.6	3.6	14.0	0.8	3.8	12.9	5.0	23.8	ns
t_{PHL}		0.8	3.0	8.1	3.4	15.0	0.6	3.8	12.9	3.6	23.8	
t_{PHL}	Propagation Delay, R to Q (Figure 2)	0.8	2.0	5.4	3.4	10.0	0.8	2.4	8.2	3.6	15.2	ns
t_{PLH}	Propagation Delay, R to QB (Figure 2)	0.6	2.2	6.6	3.6	12.2	0.8	3.0	11.0	5.0	20.4	ns
t_{PLZ}	Propagation Delay, E to Q (Figure 3)	—	0.8	1.8	—	3.4	—	1.2	3.5	—	6.4	ns
t_{PZL}		0.8	1.8	4.3	3.6	8.0	0.8	2.2	6.2	3.6	11.4	
t_{PHZ}		—	0.8	1.8	—	3.4	—	1.4	3.6	—	6.6	
t_{PZH}		0.8	1.6	4.0	4.0	7.4	1.0	2.0	6.1	5.2	11.2	
t_{PLZ}	Propagation Delay, E to QB (Figure 3)	—	0.8	1.8	—	3.4	—	1.2	3.5	—	6.4	ns
t_{PZL}		0.8	1.8	4.3	3.4	8.0	0.6	2.0	5.9	3.6	11.0	
t_{PHZ}		—	0.8	1.8	—	3.4	—	1.4	3.6	—	6.6	
t_{PZH}		0.6	1.6	3.9	3.6	7.2	0.8	2.0	5.8	5.0	10.8	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\text{ pF}) + K(C_L - 1\text{ pF})$, for K in units of ns/pF. See Section 4.

11

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to +85°C)

Symbol	Parameter		HCA 6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns)	HCA 6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	J or K to CK (Figure 4)	7.6	13.8	ns
t_h	Hold Time	CK to J or K (Figure 4)	0.4	0.6	ns
t_{rec}	Recovery Time	R to CK (Figure 2)	1.6	3.4	ns
t_w	Pulse Width	CK, t_w (L) (Figure 1)	6.0	11.4	ns
		CK, t_w (H) (Figure 1)	8.0	14.0	
		R (Figure 2)	5.4	10.6	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—E,J,CK,K,R	1.0

SWITCHING WAVEFORMS

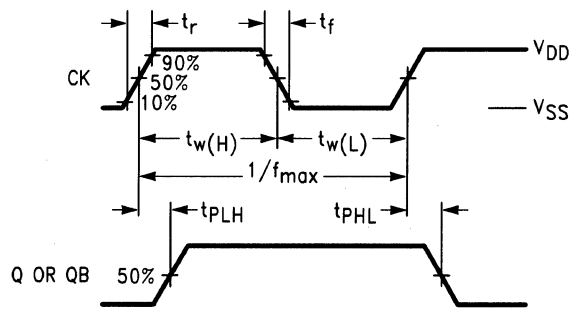
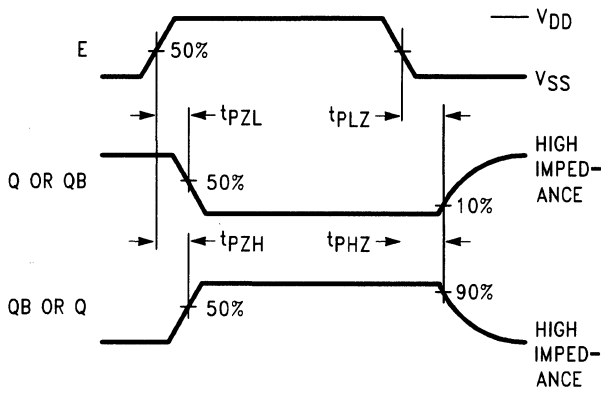


Figure 1



Refer to Figure 7 in Section 9.

Figure 3

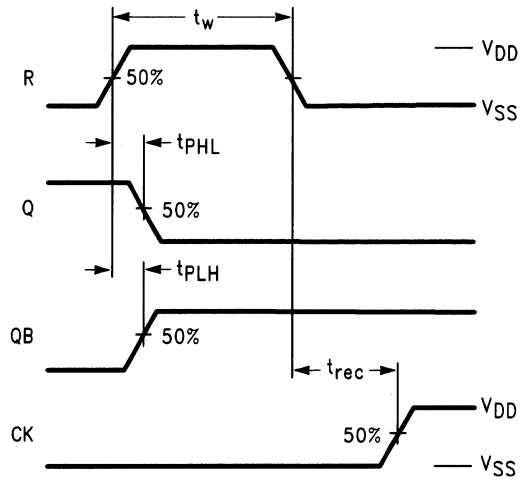


Figure 2

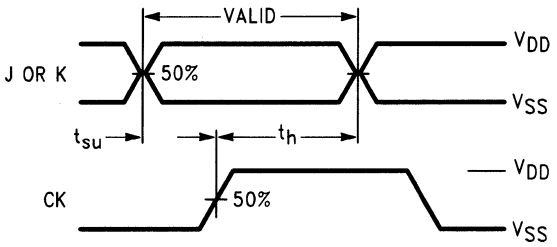
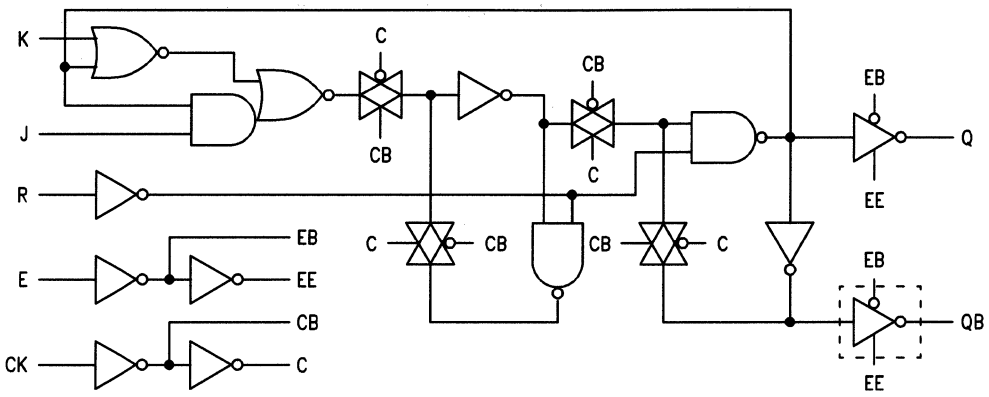
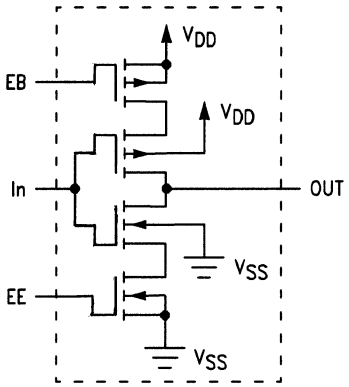


Figure 4

11

FUNCTION DIAGRAMS



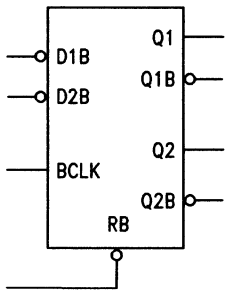


C700

Dual LSSD L2 Latch

Primary Cells: 3
Netlist Format:
$SUBU C700
Q1 Q2 Q1B Q2B / D1B
D2B BCLK RB

Pin Names:
D1B, D2B—Data Inputs (L)
BCLK—Common Latch Enable (Scan Clock B)
RB—Asynchronous Reset Bar (L)
Q, QB—Latch Outputs



FUNCTION TABLE*

Inputs			Outputs		Function
BCLK	DB	RB	Q	QB	
X	X	L	L	H	Both Latches asynchronously reset.
L	L/H	H	H/L	L/H	Latch is in transparent mode; data inputs are active low.
H	X	H	No Change		Data is latched.

*See Section 7 for a description of LSSD.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, DB to Q (Figure 1)	0.5	1.7	4.8	1.9	8.2	0.7	3.0	7.5	2.7	13.8	ns
t_{PHL}		0.6	1.4	4.8	2.1	7.2	0.8	2.4	6.5	2.9	12.0	
t_{PLH}	Propagation Delay, DB to QB (Figure 1)	0.4	1.7	5.9	1.9	8.2	0.7	3.0	7.5	2.5	13.8	ns
t_{PHL}		0.4	2.0	5.7	2.0	9.2	0.7	3.4	8.3	2.9	15.4	
t_{PLH}	Propagation Delay, BCLK to Q (Figure 2)	0.5	1.9	3.9	1.9	10.5	0.7	3.2	9.5	2.7	17.6	ns
t_{PHL}		0.6	1.6	3.6	2.1	8.6	0.8	2.8	7.8	2.9	14.4	
t_{PLH}	Propagation Delay, BCLK to QB (Figure 2)	0.4	1.8	4.8	1.9	9.6	0.7	3.2	8.6	2.5	16.0	ns
t_{PHL}		0.4	2.2	4.8	2.0	11.6	0.7	3.8	10.5	2.9	19.4	
t_{PHL}	Propagation Delay, RB to Q (Figure 3)	0.6	0.9	5.7	2.1	4.9	0.8	1.6	4.4	2.9	8.2	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 3)	0.4	1.4	3.9	1.9	7.0	0.7	2.4	6.4	2.5	11.8	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{P(total)} = t_P(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40° to +85°C)

Symbol	Parameter		HCA6200 Series 2-Micron HCMOS (Input $t_r = t_f = 3$ ns) Minimum	HCA6300 Series 3-Micron HCMOS (Input $t_r = t_f = 5$ ns) Minimum	Unit
t_{su}	Setup Time	DB to BCLK (Figure 4)	6.2	10.4	ns
t_h	Hold Time	BCLK to DB (Figure 4)	2.0	3.4	ns
t_w	Pulse Width	BCLK (Figure 4) RB (Figure 3)	8.4 3.8	14.0 6.4	ns

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	DB, BCLK	1.0
		RB	2.0

SWITCHING WAVEFORMS

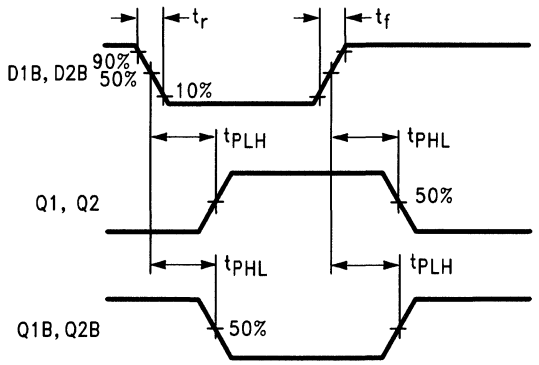


Figure 1

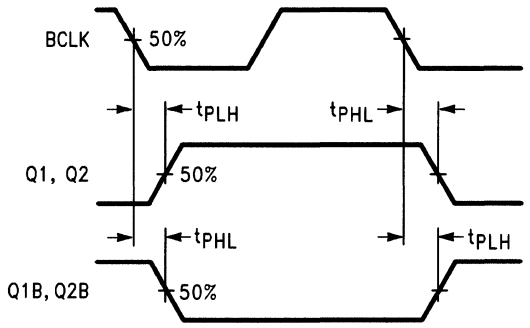


Figure 2

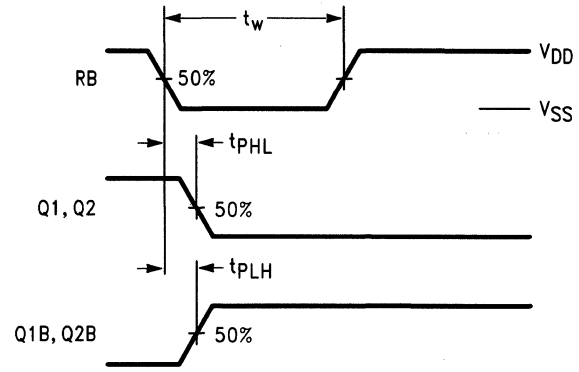


Figure 3

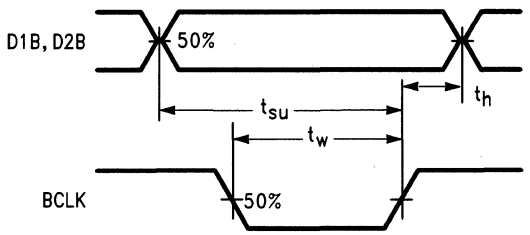


Figure 4

FUNCTION DIAGRAM

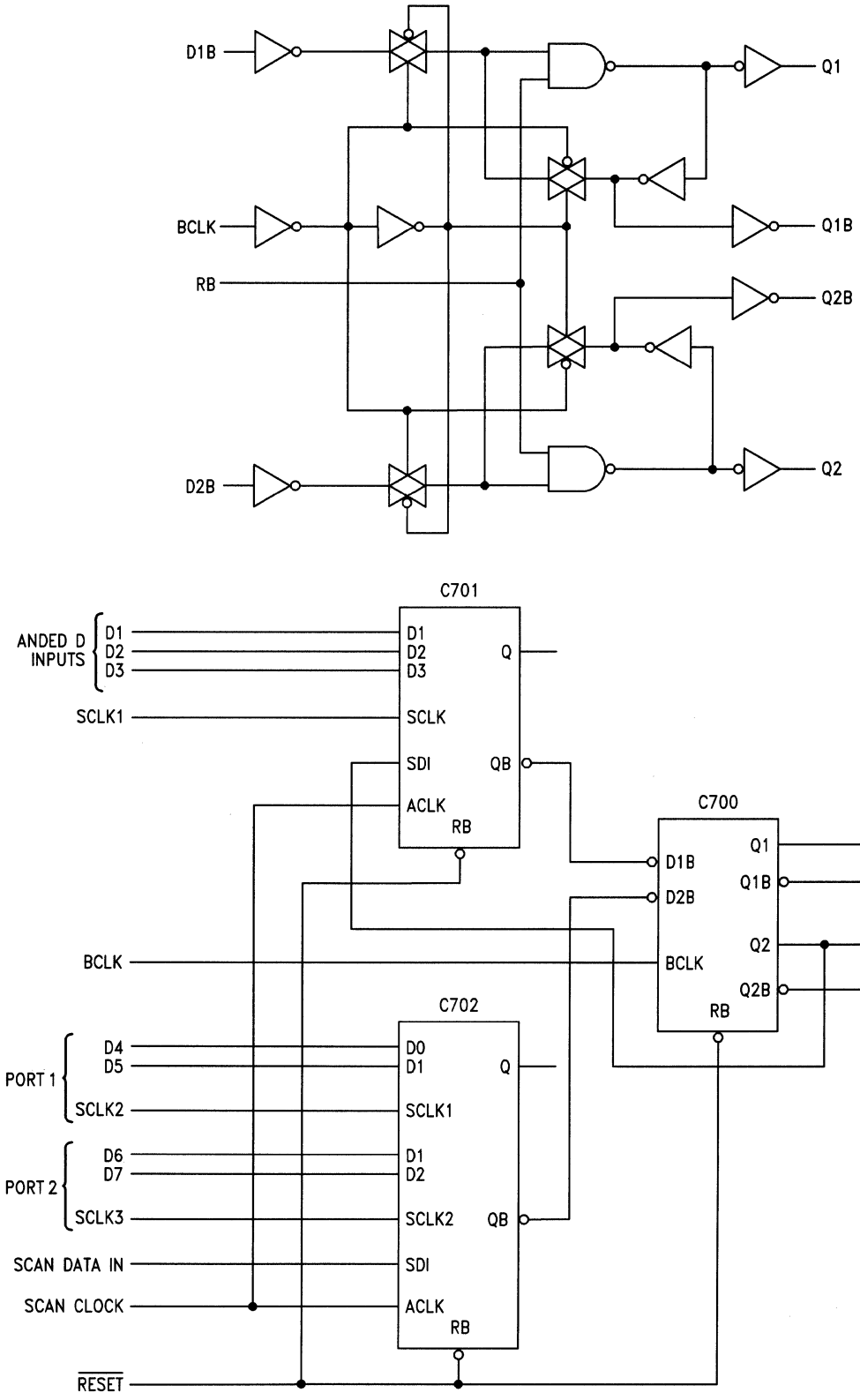
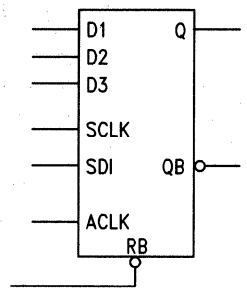


Figure 5. Typical LSSD Application

C701

LSSD L1 Latch with ANDed D Inputs



Primary Cells: 3
Netlist Format:
$SUBU C701
Q QB / D1 D2 D3 SCLK
SDI ACLK RB

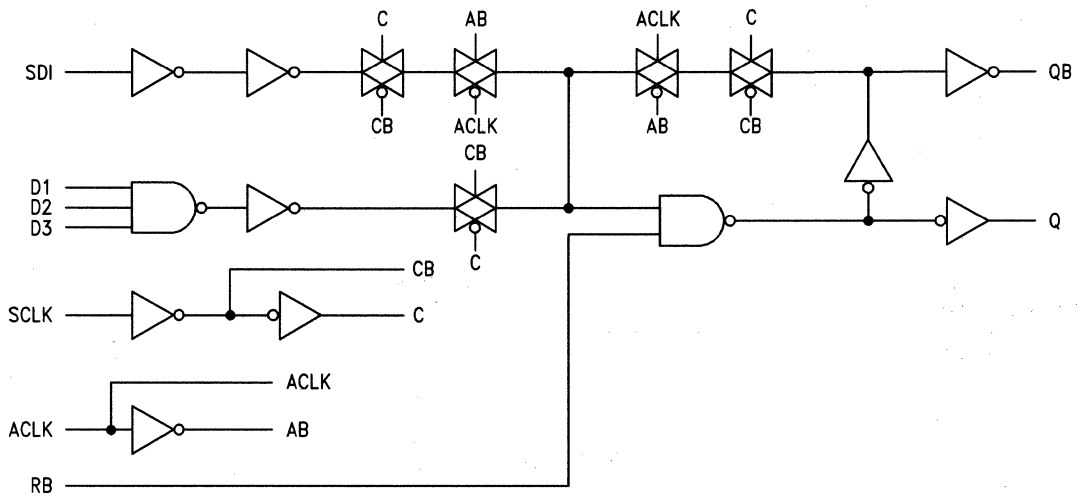
Pin Names:
D1, D2, D3—ANDed Data Inputs
SCLK—Latch Enable for Data Inputs
SDI—Scan Data Input
ACLK—Scan Clock A
Q, QB—Latch Outputs

FUNCTION TABLE*

Inputs							Outputs		Function
SCLK	D1	D2	D3	SDI	ACLK	RB	Q	QB	
L	H	H	H	X	H	H	H	L	Latch is in the transparent mode. Q = D1•D2•D3; QB = Inverse of Q.
L	L	X	X	X	H	H	L	H	
L	X	L	X	X	H	H	L	H	
L	X	X	L	X	H	H	L	H	
H	X	X	X	L/H	L	H	L/H	H/L	Latch is in the transparent mode. Q = SDI; QB = Inverse of Q.
H	X	X	X	X	H	H	No Change	No Change	Data is latched.
X	X	X	X	X	X	L	L	H	Latch is asynchronously reset.

*See Section 7 for a description of LSSD.

FUNCTION DIAGRAM



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SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, D to Q (Figure 1)	0.6	2.5	7.6	2.0	14.0	0.7	4.2	12.6	2.7	23.4	ns
t_{PHL}		0.5	1.9	5.8	2.1	10.7	0.7	3.2	9.7	2.8	18.0	
t_{PLH}	Propagation Delay, D to QB (Figure 1)	0.4	2.0	6.2	2.1	11.5	0.5	3.2	10.4	2.8	19.2	ns
t_{PHL}		0.4	2.2	8.1	2.0	15.0	0.5	3.8	13.6	2.7	25.2	
t_{PLH}	Propagation Delay, SCLK to Q (Figure 2)	0.6	2.0	6.4	2.0	11.8	0.7	3.2	10.7	2.7	19.8	ns
t_{PHL}		0.5	1.9	5.8	2.1	10.7	0.7	3.2	9.7	2.8	18.0	
t_{PLH}	Propagation Delay, SCLK to QB (Figure 2)	0.4	2.1	6.2	2.1	11.5	0.5	3.6	10.4	2.8	19.2	ns
t_{PHL}		0.4	2.4	7.0	2.0	13.0	0.5	4.0	11.8	2.7	21.8	
t_{PLH}	Propagation Delay, SDI to Q (Figure 1)	0.6	2.2	6.2	2.0	11.5	0.7	3.8	10.4	2.7	19.2	ns
t_{PHL}		0.5	2.2	6.2	2.1	11.4	0.7	3.8	10.3	2.8	19.0	
t_{PLH}	Propagation Delay, SDI to QB (Figure 1)	0.4	2.5	7.0	2.0	13.0	0.5	4.2	11.8	2.8	21.8	ns
t_{PHL}		0.4	2.6	7.3	2.0	13.5	0.5	4.4	12.2	2.7	22.6	
t_{PLH}	Propagation Delay, ACLK to Q (Figure 2)	0.6	1.6	4.9	2.0	9.1	0.7	2.8	8.2	2.7	15.2	ns
t_{PHL}		0.5	1.6	4.8	2.1	8.8	0.7	2.8	8.0	2.8	14.8	
t_{PLH}	Propagation Delay, ACLK to QB (Figure 2)	0.4	1.8	5.8	2.1	10.8	0.5	3.0	9.7	2.8	18.0	ns
t_{PHL}		0.4	2.0	6.2	2.0	11.4	0.5	3.2	10.3	2.7	19.0	
t_{PHL}	Propagation Delay, RB to Q (Figure 3)	0.5	1.0	2.6	2.1	4.8	0.7	1.8	4.3	2.8	8.0	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 3)	0.4	1.4	4.2	2.1	7.8	0.5	2.4	7.0	2.8	13.0	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5V to 5.5V, T_A = −40° to +85°C)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS (Input tr = tf = 3 ns)	HCA6300 Series 3-Micron HCMOS (Input tr = tf = 5 ns)	Unit
		Minimum	Minimum	
t_{su}	Setup Time, D to SCLK (Figure 4)	12.4	20.8	ns
	SDI to ACLK (Figure 4)	10.0	16.8	
t_h	Hold Time, SCLK to D (Figure 4)	0.0	0.0	ns
	ACLK to SDI (Figure 4)	0.0	0.0	
t_w	Pulse Width, SCLK (Figure 4)	9.8	16.4	ns
	ACLK (Figure 4)	7.6	12.8	
	RB (Figure 3)	3.8	6.4	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors	D, SCLK, SDI, RB	1.0
		ACLK	2.0

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SWITCHING WAVEFORMS

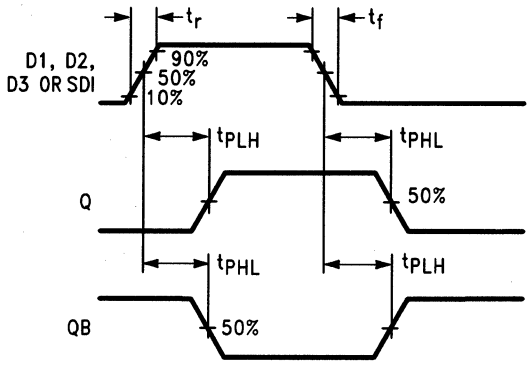


Figure 1

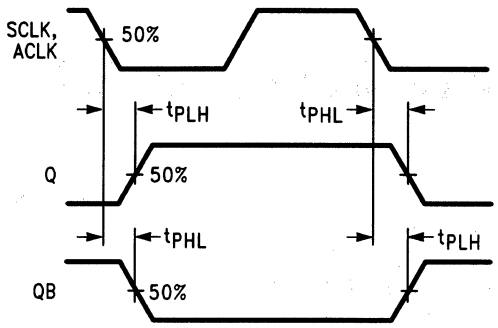


Figure 2

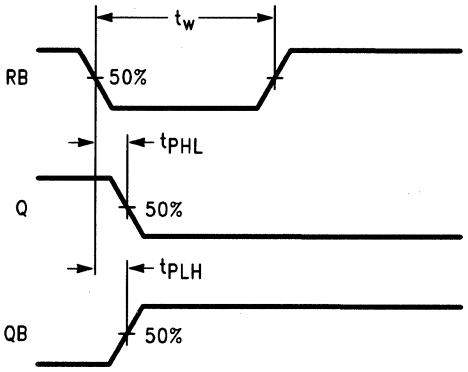


Figure 3

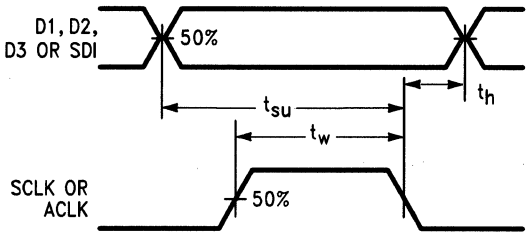
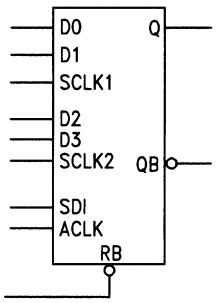


Figure 4

C702

LSSD Dual Port L1 Latch



Primary Cells: 5
Netlist Format:
$SUBU C702
Q QB / D0 D1 SCLK1 D2 D3
SCLK2 SDI ACLK RB

Pin Names:
D0, D1—ANDed D Inputs
Controlled by SCLK1
D2, D3—ANDed D Inputs
Controlled by SCLK2
SCLK1, SCLK2—Latch Enables for
D0–D3
SDI—Scan Data Input,
Controlled by ACLK
ACLK—Scan Clock A
RB—Asynchronous Reset
Q, QB—Latch Outputs

FUNCTION TABLE*

Inputs									Outputs		Function
SCLK1	D0	D1	SCLK2	D2	D3	ACLK	SDI	RB	Q	QB	
X	X	X	X	X	X	X	X	L	L	H	Latch is asynchronously reset.
L	L	X	H	X	X	H	X	H	L	H	Latch is in the transparent mode; Q = D0 • D1, with SCLK1 as the latch enable. QB = Inverse of Q.
L	X	L	H	X	X	H	X	H	L	H	
L	H	H	H	X	X	H	X	H	H	L	
H	X	X	L	L	X	H	X	H	L	H	Latch is in the transparent mode; Q = D2 • D3, with SCLK2 as the latch enable. QB = Inverse of Q.
H	X	X	L	X	L	H	X	H	L	H	
H	X	X	L	H	H	H	X	H	H	L	
H	X	X	H	X	X	L	L/H	H	L/H	H/L	Latch is in the transparent mode; Q = SDI, with ACLK as the latch enable. QB = Inverse of Q.
H	X	X	H	X	X	H	X	H	NO CHANGE	NO CHANGE	Data is latched.

*See Section 7 for a description of LSSD.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
t_{PLH}	Propagation Delay, D0–D3 to Q (Figure 1)	0.6	2.4	7.9	2.3	14.6	0.8	4.0	13.2	3.1	24.4	ns
t_{PHL}		0.5	2.1	6.4	2.0	11.8	0.7	3.6	10.7	2.7	19.8	
t_{PLH}	Propagation Delay, D0–D3 to QB (Figure 1)	0.6	1.8	5.7	2.2	10.6	0.8	3.0	9.6	2.9	17.8	ns
t_{PHL}		0.6	2.4	7.5	2.2	13.9	0.8	4.0	12.5	2.9	23.2	
t_{PLH}	Propagation Delay, SCLK1, SCLK2 to Q (Figure 2)	0.6	2.7	8.4	2.3	15.6	0.8	4.6	14.2	3.1	26.2	ns
t_{PHL}		0.5	2.6	8.1	2.0	15.0	0.7	4.4	13.6	2.7	25.2	
t_{PLH}	Propagation Delay, SCLK1, SCLK2 to QB (Figure 2)	0.6	2.5	7.4	2.2	13.7	0.8	4.2	12.4	2.9	23.0	ns
t_{PHL}		0.6	2.6	8.1	2.2	14.9	0.8	4.4	13.5	2.9	25.0	
t_{PLH}	Propagation Delay, ACLK to Q (Figure 2)	0.6	2.7	8.6	2.3	16.0	0.8	4.6	14.5	3.1	26.8	ns
t_{PHL}		0.5	2.9	9.3	2.0	17.2	0.7	5.0	15.6	2.7	28.8	
t_{PLH}	Propagation Delay, ACLK to QB (Figure 2)	0.6	2.7	8.6	2.2	16.0	0.8	4.6	14.5	2.9	26.8	ns
t_{PHL}		0.6	2.6	8.2	2.2	15.2	0.8	4.4	13.7	2.9	25.4	
t_{PLH}	Propagation Delay, SDI to Q (Figure 1)	0.6	2.7	8.1	2.3	15.0	0.8	4.6	13.6	3.1	25.2	ns
t_{PHL}		0.5	2.6	8.3	2.0	15.4	0.7	4.4	13.9	2.7	25.8	
t_{PLH}	Propagation Delay, SDI to QB (Figure 1)	0.6	2.4	7.6	2.2	14.1	0.8	4.0	12.8	2.9	23.6	ns
t_{PHL}		0.6	2.6	7.7	2.2	14.3	0.8	4.4	13.0	2.9	24.0	
t_{PHL}	Propagation Delay, RB to Q (Figure 3)	0.5	1.7	3.1	2.0	5.8	0.7	3.0	5.3	2.7	9.8	ns
t_{PLH}	Propagation Delay, RB to QB (Figure 3)	0.6	1.1	4.9	2.2	9.1	0.8	2.0	8.2	2.9	15.2	ns

*See Section 4 for minimum, typical, and maximum conditions.
**$t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40°C to +85°C)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
		Minimum	Minimum	
t_{su}	Setup Time D0–D3 to SCLK1, SCLK2 (Figure 4)	11.7	19.8	ns
	SDI to ACLK (Figure 4)	12.8	21.4	
t_h	Hold Time SCLK1, SCLK2 to D0–D3 (Figure 4)	1.3	2.4	ns
	ACLK to SDI (Figure 4)	0.0	0.0	
t_w	Pulse Width SCLK1, SCLK2 (Figure 4)	12.8	21.4	ns
	ACLK (Figure 4)	14.2	23.8	
	RB (Figure 3)	6.4	10.8	

INPUT LOAD FACTORS

IUL	Input Unit Load Factors—SCLK1, SCLK2, D0–D3, I, RB	1.0

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SWITCHING WAVEFORMS

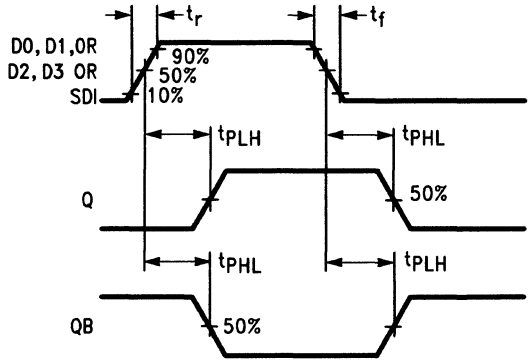


Figure 1

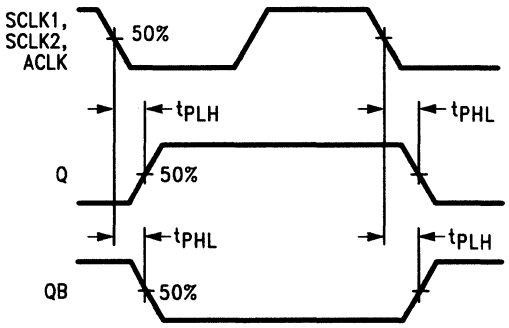


Figure 2

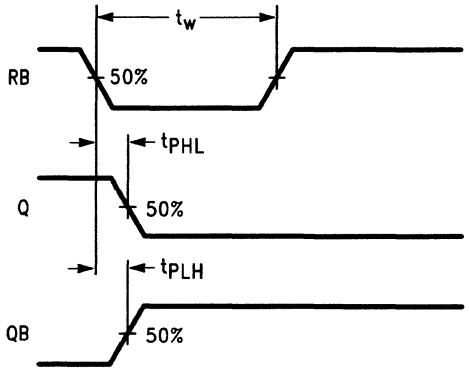


Figure 3

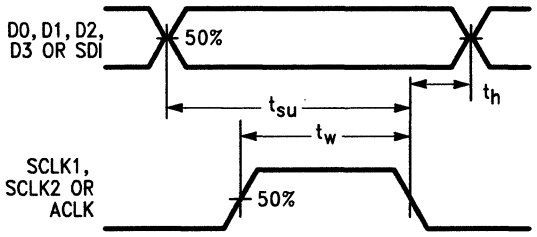
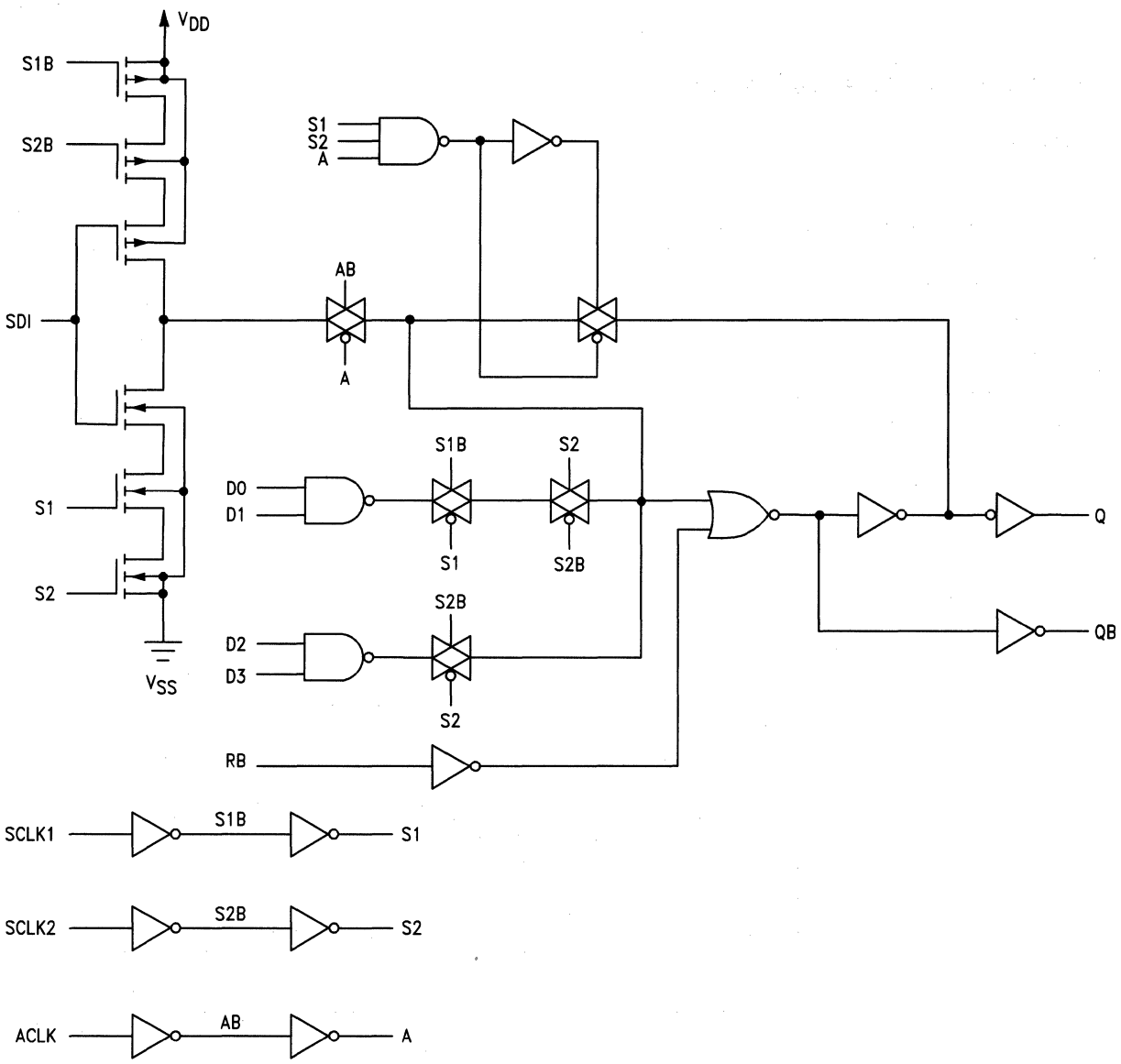


Figure 4

FUNCTION DIAGRAM



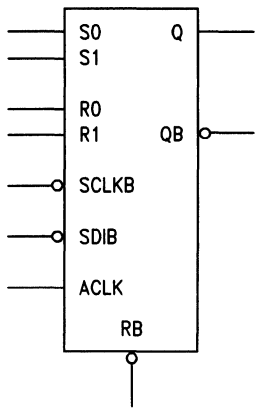
11

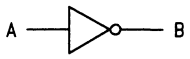
C703

LSSD R-S L1 Latch

Primary Cells: 3
Netlist Format:
$SUBU C703
Q QB B/ S0 S1 R0 R1 SCLKB SDIB ACLK RB A

Pin Names:
S0, S1—ANDed Latch Set Inputs
R0, R1—ANDed Latch Reset Inputs
SCLKB—Latch Enable Inputs for S0, S1, R0, R1 Inputs
SDIB—Scan Data Input Bar
ACLK—Latch Enable for the SDIB Input
RB—Asynchronous Reset (Active Low)
A—Inverter Input
B—Inverter Output





FUNCTION TABLE*

(S0•S1)	(R0•R1)	SCLKB	SDIB	ACLK	RB	Q	QB	Mode	Function
X	X	L	X	H	L	L	H	Normal or Scan	The latch is asynchronously reset. SCLKB, ACLK, and RB are mutually exclusive inputs. A single operation should be done on the latch at a time or unexpected results may occur; SCLKB and ACLK must remain active (SCLKB = L and ACLK = H).
H	L	H	X	H	H	H	L	Normal	The latch operates as an S-R latch with inputs S = (S0•S1) and R = (R0•R1). In the normal mode, the latch is gated by SCLKB. ACLK must remain active (ACLK = H) and RB inactive (RB = H) or unexpected results may occur.
L	H	H	X	H	H	L	H		
L	L	H	X	H	H	No Change	No Change		
H	H	H	X	H	H	L**	L**		
X	X	L	X	H	H	No Change	No Change	Normal or Scan	Data is latched.
X	X	L	L/H	L	H	H/L	L/H	Scan	The latch is operating in the scan mode, with SDIB as the input to the latch. Q and QB follow the SDIB input while the latch is in the transparent mode. SCLKB must remain active (SCLKB = L) and RB inactive (RB = H), or unexpected results may occur.

*See Section 7 for a description of LSSD.
**Both outputs will remain low as long as (S0•S1) and (R0•R1) remain high, but the output states are unpredictable if (S0•S1) and (R0•R1) go low simultaneously or if SCLKB goes low while (S0•S1) and (R0•R1) are high.

SWITCHING CHARACTERISTICS* (C_L = 1 pF on all outputs)

Symbol	Parameter	HCA6200 Series 2-Micron HCMOS					HCA6300 Series 3-Micron HCMOS					Unit
		Min		Typ	Max		Min		Typ	Max		
		K**	Limit		K**	Limit	K**	Limit		K**	Limit	
tPLH	Propagation Delay, S0, S1 to Q (Figure 1)	0.5	3.0	9.5	2.1	17.6	0.7	5.0	15.9	2.8	29.4	ns
tPHL		0.5	2.0	5.5	2.0	10.1	0.7	3.4	9.2	2.7	17.0	
tPLH	Propagation Delay, S0, S1 to QB (Figure 1)	0.5	2.6	8.1	2.1	14.9	0.7	4.4	13.5	2.8	25.0	ns
tPHL		0.5	2.3	7.0	2.1	12.9	0.7	4.0	11.7	2.8	21.6	
tPLH	Propagation Delay, R0, R1 to Q (Figure 1)	0.5	3.0	9.5	2.1	17.6	0.7	5.0	15.9	2.8	29.4	ns
tPHL		0.5	2.0	5.5	2.0	10.1	0.7	3.4	9.2	2.7	17.0	
tPLH	Propagation Delay, R0, R1 to QB (Figure 1)	0.5	2.6	8.1	2.1	14.9	0.7	4.4	13.5	2.8	25.0	ns
tPHL		0.5	2.3	7.0	2.1	12.9	0.7	4.0	11.7	2.8	21.6	
tPLH	Propagation Delay, SCLKB to Q (Figure 2)	0.5	3.0	9.5	2.1	17.6	0.7	5.0	15.9	2.8	29.4	ns
tPHL		0.5	2.0	5.5	2.0	10.1	0.7	3.4	9.2	2.7	17.0	
tPLH	Propagation Delay, SCLKB to QB (Figure 2)	0.5	2.6	8.1	2.1	14.9	0.7	4.4	13.5	2.8	25.0	ns
tPHL		0.5	2.3	7.0	2.1	12.9	0.7	4.0	11.7	2.8	21.6	
tPLH	Propagation Delay, SDIB to Q (Figure 3)	0.5	2.4	7.2	2.1	13.4	0.7	4.0	12.1	2.8	22.4	ns
tPHL		0.5	1.6	4.8	2.0	8.9	0.7	2.8	8.1	2.7	15.0	
tPLH	Propagation Delay, SDIB to QB (Figure 3)	0.5	2.4	7.4	2.1	13.7	0.7	4.0	12.4	2.8	23.0	ns
tPHL		0.5	1.7	4.8	2.1	8.8	0.7	3.0	8.0	2.8	14.8	
tPLH	Propagation Delay, ACLK to Q (Figure 4)	0.5	2.4	7.2	2.1	13.4	0.7	4.0	12.1	2.8	22.4	ns
tPHL		0.5	1.6	4.8	2.0	8.9	0.7	2.8	8.1	2.7	15.0	
tPLH	Propagation Delay, ACLK to QB (Figure 4)	0.5	2.4	7.2	2.1	13.7	0.7	4.0	12.4	2.8	23.0	ns
tPHL		0.5	1.7	4.8	2.1	8.8	0.7	3.0	8.0	2.8	14.8	
tPHL	Propagation Delay, RB to Q (Figure 7)	0.5	2.0	4.8	2.0	8.9	0.7	3.4	8.1	2.7	15.0	ns
tPLH	Propagation Delay, RB to QB (Figure 7)	0.5	2.6	7.4	2.1	13.7	0.7	4.4	12.4	2.8	23.0	ns
tPLH	Propagation Delay, A to B (Figure 8)	0.4	0.8	1.7	1.8	3.2	0.4	0.8	2.2	2.2	4.0	ns
tPHL		0.4	1.0	1.8	1.8	3.4	0.4	0.8	2.2	2.2	4.0	

*See Section 4 for minimum, typical, and maximum conditions.
**$t_{p(total)} = t_p(C_L = 1\ pF) + K(C_L - 1\ pF)$, for K in units of ns/pF. See Section 4.

TIMING REQUIREMENTS (V_{DD} = 4.5 to 5.5 V, T_A = −40 to +85°C)

Symbol	Parameter		HCA6200 Series 2-Micron HCMOS (Input $t_r = t_f$ = 3 ns)	HCA6300 Series 3-Micron HCMOS (Input $t_r = t_f$ = 5 ns)	Unit
			Minimum	Minimum	
t_{su}	Setup Time	S0, S1 to SCLKB (Figure 5)	10.8	18.0	ns
		R0, R1 to SCLKB (Figure 5)	10.8	18.0	
		SDIB to ACLK (Figure 6)	9.5	16.0	
t_h	Hold Time	SCLKB to S0, S1 (Figure 5)	3.0	5.0	ns
		SCLKB to R0, R1 (Figure 5)	3.0	5.0	
		ACLK to SDIB (Figure 6)	1.0	1.8	
t_w	Pulse Width	S0, S1 (Figure 1)	13.6	22.8	ns
		R0, R1 (Figure 1)	13.6	22.8	
		SCLKB (Figure 5)	13.6	22.8	
		ACLK (Figure 6)	9.6	16.0	
		RB (Figure 7)	10.0	17.0	

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INPUT LOAD FACTORS

IUL	Input Unit Load Factors	S0, S1, R0, R1, SCLK, SDIB, ACLKB, RB, A	1.0

SWITCHING WAVEFORMS

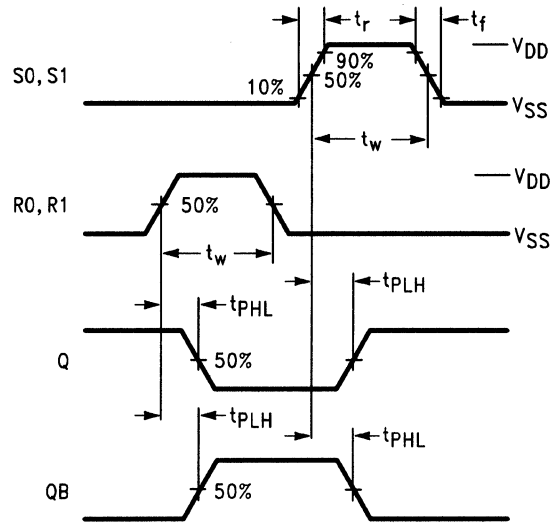


Figure 1

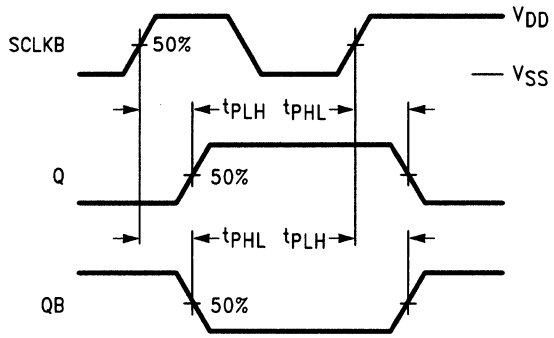


Figure 2

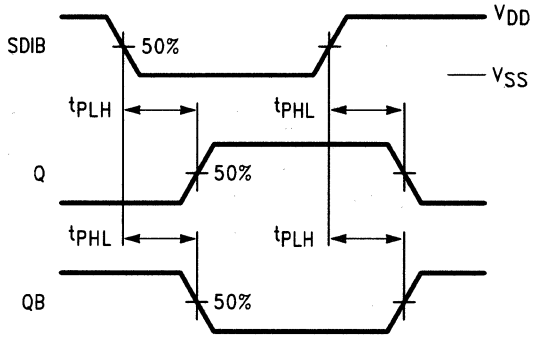


Figure 3

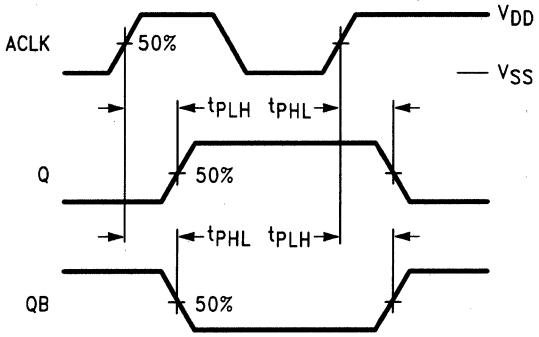


Figure 4

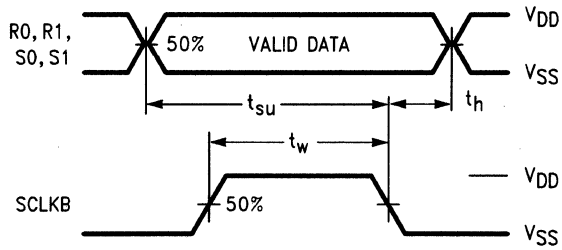


Figure 5

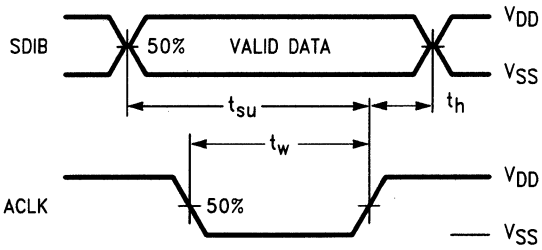


Figure 6

SWITCHING WAVEFORMS (Continued)

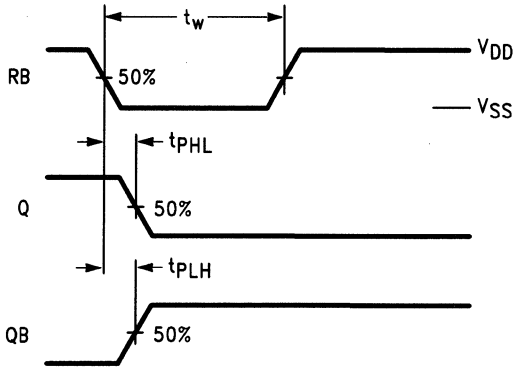


Figure 7

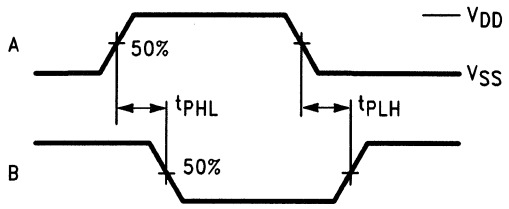
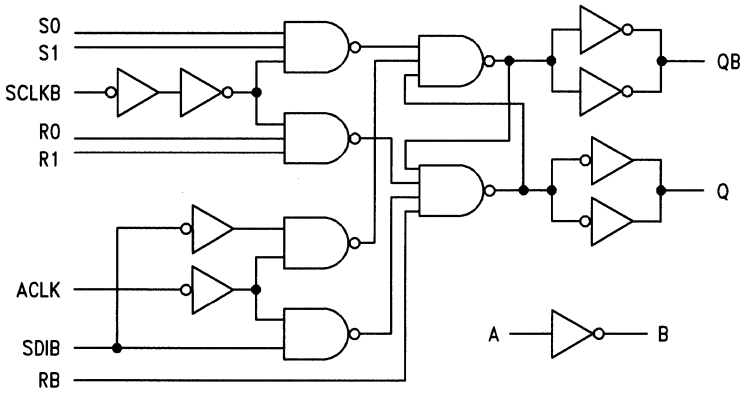


Figure 8

FUNCTION DIAGRAM



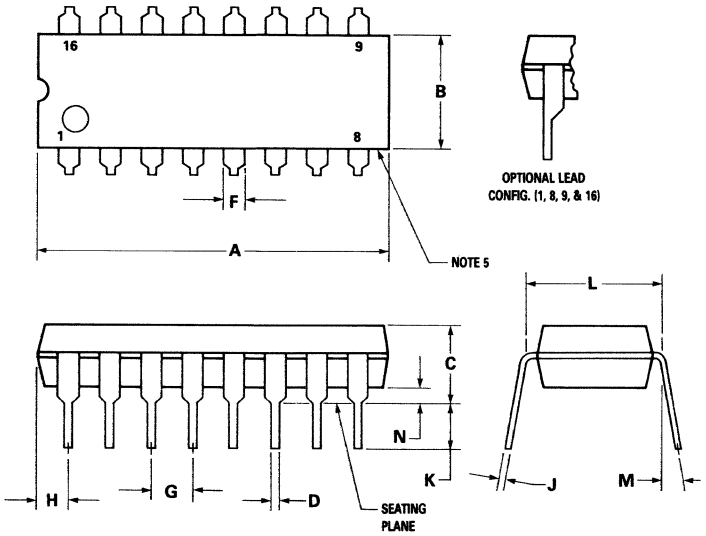
Packaging 12

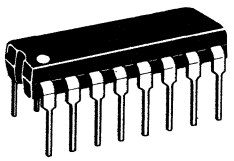
MECHANICAL DATA

Package dimensions, features, and availability are given in this section.

16-PIN PACKAGES

PLASTIC
CASE 648-05

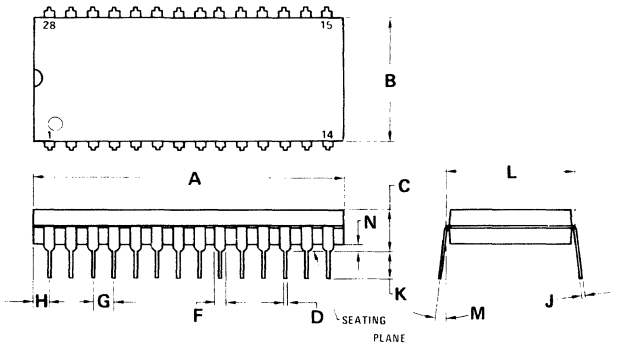


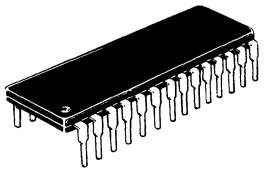


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9 AND 16).
5. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

PLASTIC
CASE 710-02

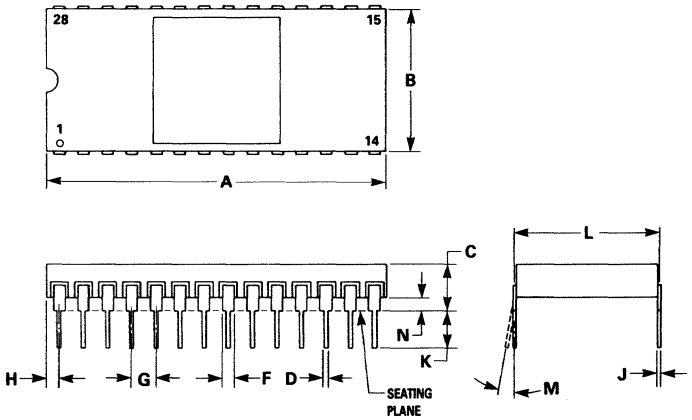


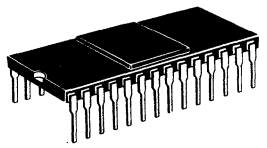


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERAMIC
CASE 719-03

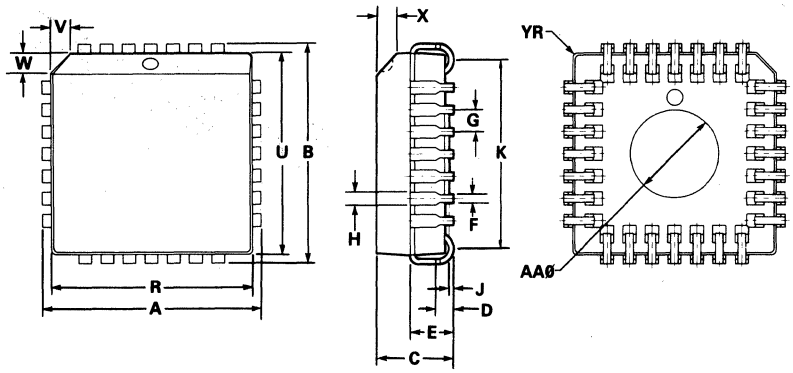


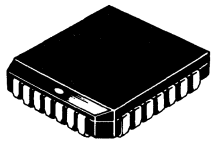


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.73	15.34	0.580	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.52	0.020	0.060

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PLASTIC
CASE 776A-01

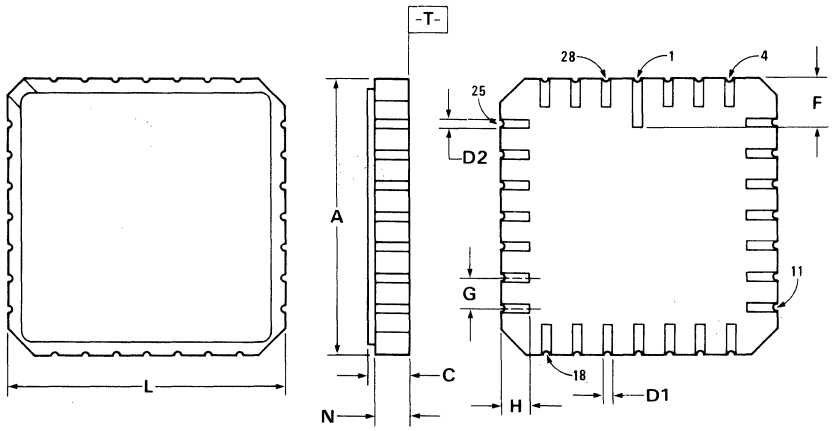


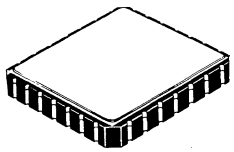


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.13	0.38	0.005	0.015
K	9.91	10.92	0.390	0.430
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020
AA	2.34	2.71	0.088	0.107

NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

CERAMIC
CASE 786-01

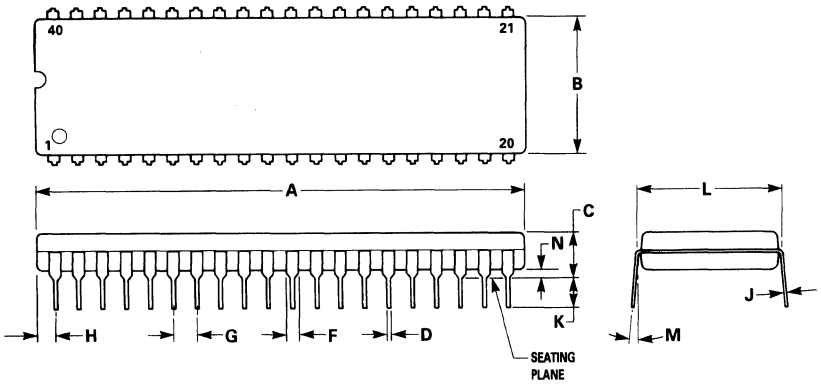


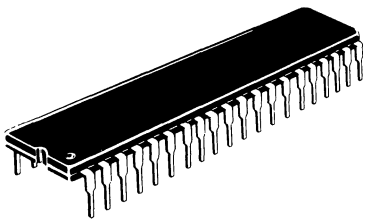


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	11.18	11.68	0.440	0.460
C	1.52	2.03	0.060	0.080
D	0.51	0.76	0.020	0.030
D1	0.51	0.786	0.020	0.030
F	1.91	2.41	0.075	0.095
G	1.27 BSC		0.050 BSC	
H	1.07	1.47	0.042	0.058
L	11.18	11.68	0.440	0.460
N	1.27	1.77	0.050	0.070

NOTES:
1. DIMENSIONS A AND L ARE DATUMS AND -T- IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR TERMINAL D1 (14 PLACES):
   ⌖ | 0.13 (0.005) Ⓜ | T | A Ⓢ | L Ⓢ
   FOR TERMINAL D2 (14 PLACES):
   ⌖ | 0.13 (0.005) Ⓜ | T | L Ⓢ | A Ⓢ
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

PLASTIC
CASE 711-03

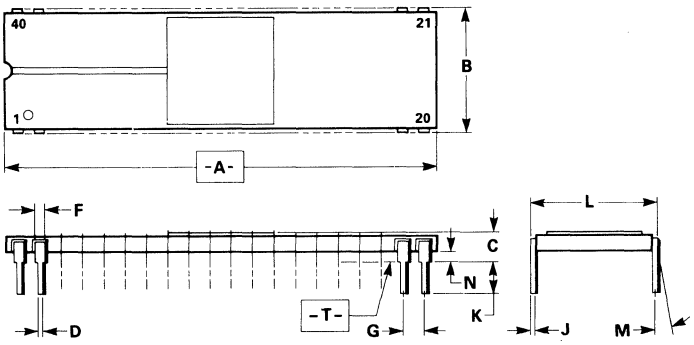


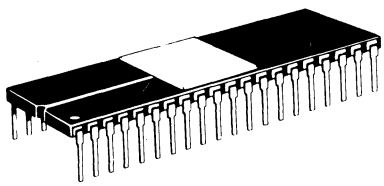


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERAMIC
CASE 715-05

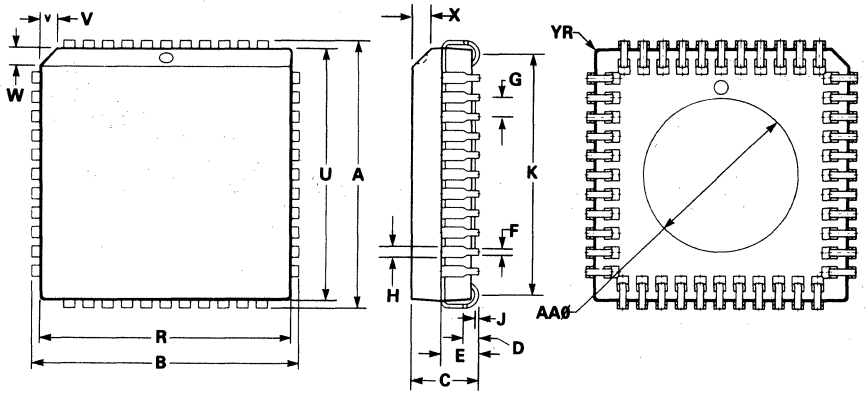


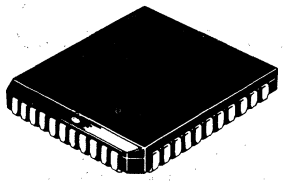


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

PLASTIC
CASE 777A-01

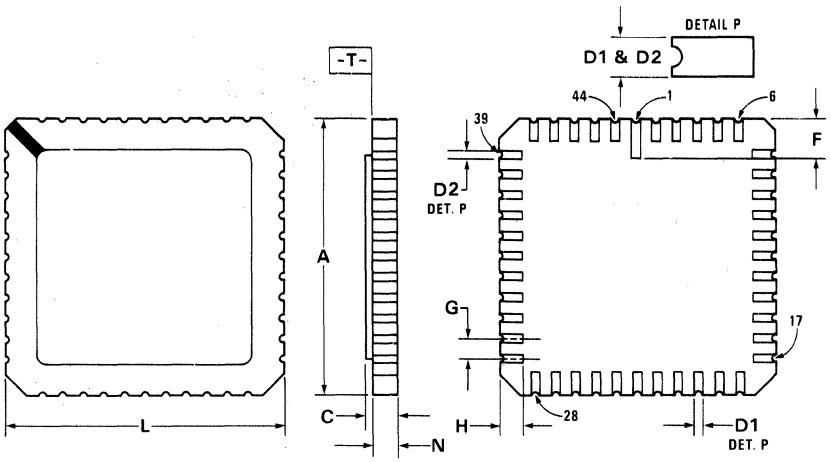


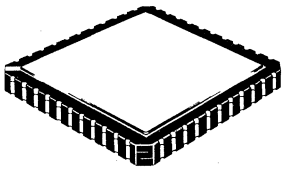


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.13	0.38	0.005	0.015
K	14.99	16.00	0.590	0.630
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.046
Y	0.00	0.50	0.000	0.020
AA	9.86	10.33	0.388	0.407

NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

CERAMIC
CASE 788-01





NOTES:
1. DIMENSIONS A AND L ARE DATUMS AND -T- IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR TERMINAL D1 (22 PLACES):

⌖	0.13 (0.005) Ⓜ	T	A Ⓢ	L Ⓢ

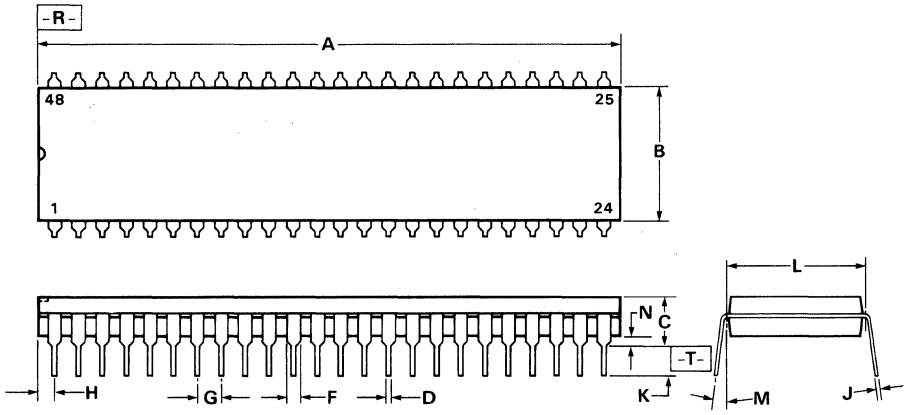
FOR TERMINAL D2 (22 PLACES):

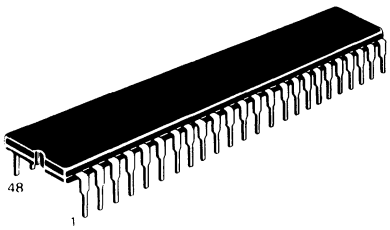
⌖	0.13 (0.005) Ⓜ	T	L Ⓢ	A Ⓢ

3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.26	16.76	0.640	0.660
C	1.65	2.15	0.065	0.085
D	0.51	0.76	0.020	0.030
D1	0.51	0.76	0.020	0.030
F	1.91	2.41	0.075	0.095
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
L	16.26	16.76	0.640	0.660
N	1.40	1.90	0.055	0.075

PLASTIC
CASE 767-02

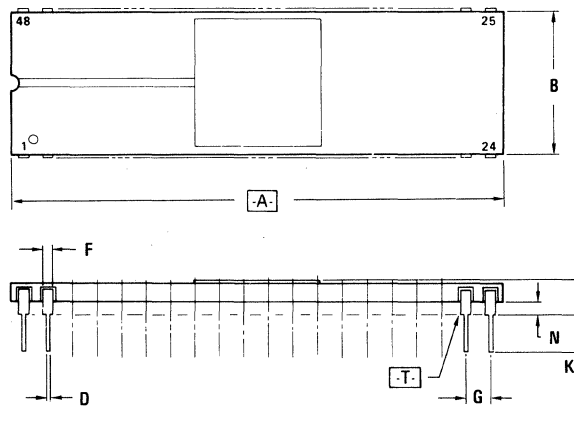


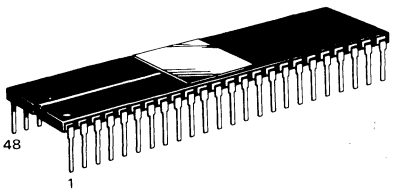


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	61.34	62.10	2.415	2.445
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.55	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.79 BSC		0.070 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.42	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. -R- IS END OF PACKAGE DATUM PLANE. -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS 1 AND 48:
   ⌖ | 0.51 (0.020) | T | B Ⓜ | R
   POSITIONAL TOLERANCE FOR LEAD PATTERN:
   ⌖ | 0.25 (0.010) | T | B Ⓜ
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. DIMENSION L IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
6. CONTROLLING DIMENSION: INCH.

CERAMIC
CASE 740-02

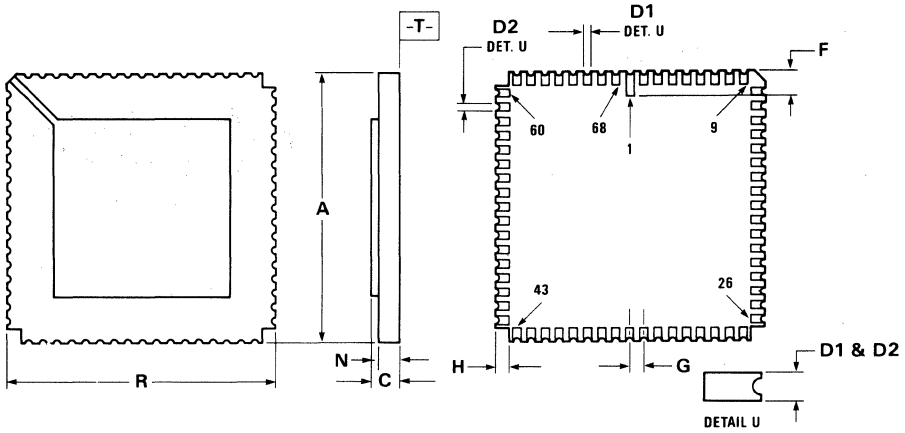


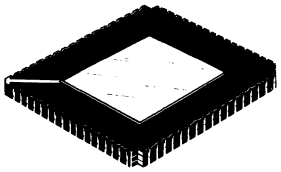


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS:
   ⌖ | Ø 0.25 (0.010)Ⓜ | T | AⓂ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CERAMIC
CASE 760A-02





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	23.88	24.38	0.940	0.960
C	1.75	2.06	0.069	0.081
D1	0.81	0.99	0.032	0.039
D2	0.81	0.99	0.032	0.039
F	2.03	2.28	0.080	0.090
G	1.27 BSC		0.050 BSC	
H	1.14	1.39	0.045	0.055
N	1.52	1.77	0.060	0.070
R	23.88	24.38	0.940	0.960

NOTES:
1. DIMENSIONS A AND R ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR TERMINAL (D1) 34 PLACES:

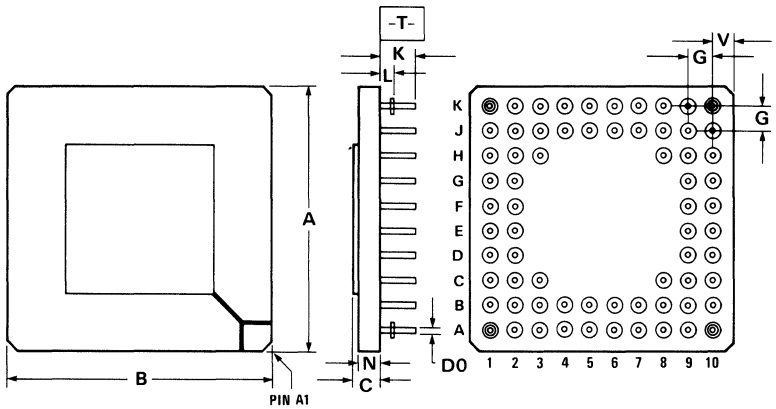
⌖	0.25 (0.010) Ⓜ	T	A Ⓢ	R Ⓢ

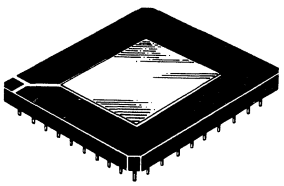
FOR TERMINAL (D2) 34 PLACES:

⌖	0.25 (0.010) Ⓜ	T	A Ⓢ	R Ⓢ

3. DIMENSION H PROVIDES THE SIZE FOR BOTH THE PAD LENGTH AND THE THREE CORNER NOTCHES.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

PIN GRID ARRAY
CASE 765A-02





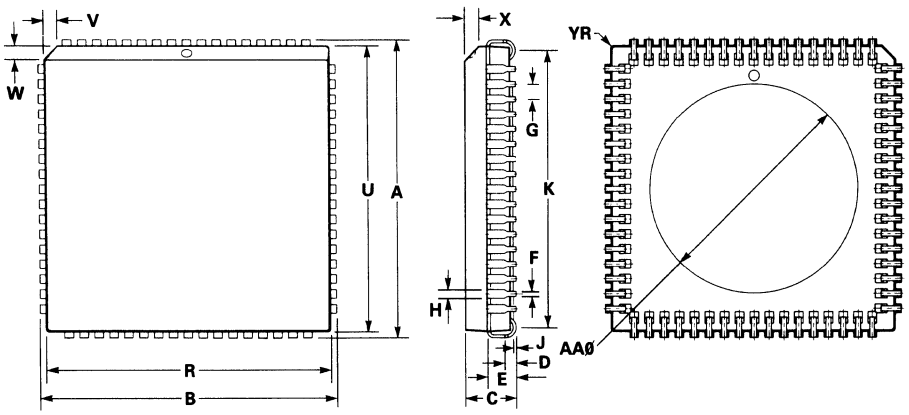
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	26.67	27.17	1.050	1.070
B	26.67	27.17	1.050	1.070
C	1.96	2.59	0.077	0.102
D	0.43	0.60	0.017	0.024
G	2.54 BSC		0.100 BSC	
K	4.32	4.82	0.170	0.190
L	1.02	1.52	0.040	0.060
N	1.78	2.28	0.070	0.090
V	1.68	2.64	0.066	0.104

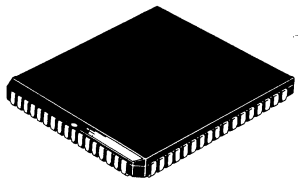
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND -T- IS DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS (68 PLACES):

⌖	ϕ 0.13 (0.005) Ⓜ	T	A Ⓢ	B Ⓢ

3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

PLASTIC
CASE 779A-01

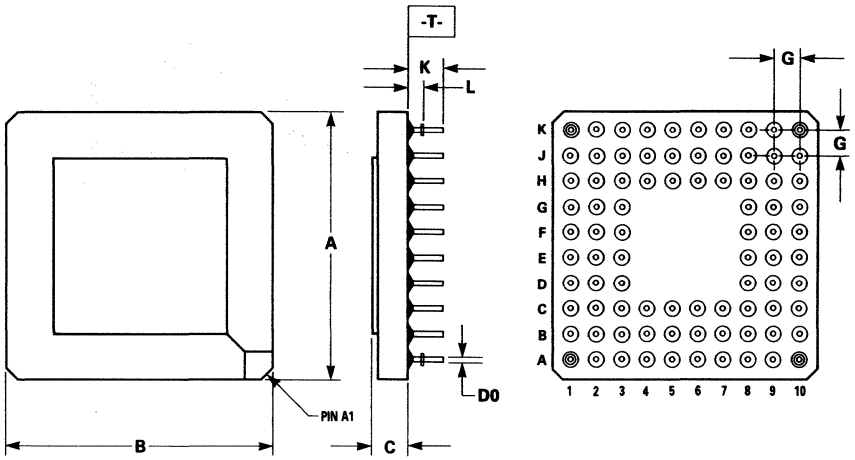


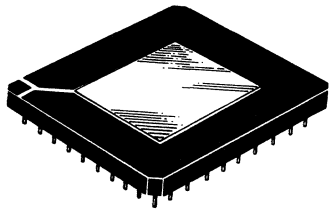


NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.02	25.27	0.985	0.995
B	25.02	25.27	0.985	0.995
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.13	0.38	0.005	0.015
K	22.61	23.62	0.890	0.930
R	24.13	24.28	0.950	0.956
U	24.13	24.28	0.950	0.956
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020
AA	17.48	17.95	0.688	0.707

PIN GRID ARRAY
CASE 793-01





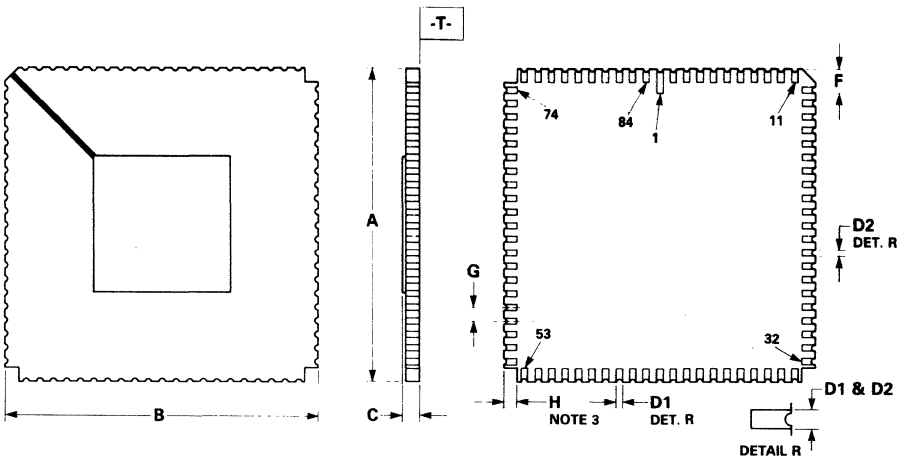
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.62	27.22	1.048	1.072
B	26.72	27.22	1.048	1.072
C	2.03	2.59	0.080	0.102
D	0.43	0.58	0.017	0.023
G	2.54 BSC		0.100 BSC	
K	4.27	4.87	0.168	0.192
L	1.02	1.52	0.040	0.060

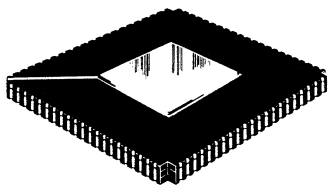
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS: (84 PL)

⌖	ϕ 0.13 (0.005) Ⓛ	T	A Ⓢ	B Ⓢ

3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

CERAMIC
CASE 794-01





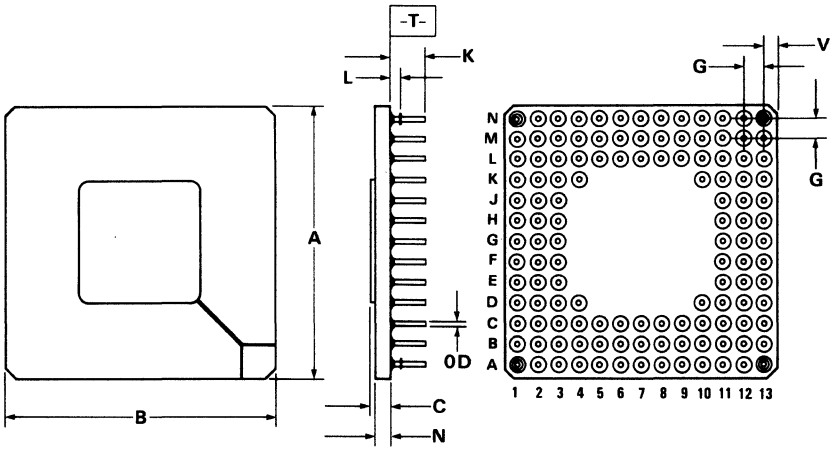
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.83	29.66	1.135	1.168
B	28.83	29.66	1.135	1.168
C	1.52	2.03	0.060	0.080
D	0.53	0.71	0.021	0.028
F	0.64	2.41	0.025	0.095
G	1.27 BSC		0.050 BSC	
H	1.07	1.47	0.042	0.058

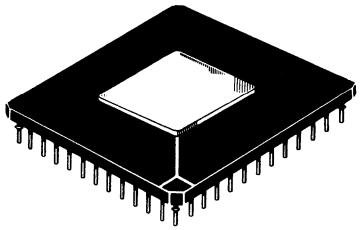
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR TERMINAL D (84 PL)

⌖	0.25 (0.010) Ⓜ	T	A Ⓢ	B Ⓢ

3. H DIMENSION IS TYPICAL AND DEFINES BOTH CONTACT LENGTH AND CORNER NOTCH SIZE.
4. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

PIN GRID ARRAY
CASE 789-01





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	32.89	33.65	1.295	1.325
B	32.89	33.65	1.295	1.325
C	2.06	2.56	0.081	0.101
D	0.43	0.48	0.017	0.019
G	2.54 BSC		0.100 BSC	
K	3.56	4.06	0.140	0.160
L	1.02	1.52	0.040	0.060
N	1.78	2.29	0.070	0.090
V	0.99	2.13	0.039	0.084

NOTES:
1. A AND B ARE DATUMS AND -T- IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR LEADS (124 PL):

⌖	ϕ 0.13 (0.005) Ⓜ	T	A Ⓢ	B Ⓢ

3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

2-MICRON MACROCELL ARRAY PACKAGE AVAILABILITY

Package Type*	Array Type				
	HCA6206	HCA6212	HCA6225	HCA6238	HCA6248
16-pin PDIP	Now				
28-pin PDIP	Now	Now			
28-pin HDIP	Now	Now			
28-pin LCC	□	□			
28-pin PLCC	□	□			
40-pin PDIP	Now	Now	Now		
40-pin HDIP	Now	Now	Now		
44-pin LCC	□	Now	Now		
44-pin PLCC	□	□	□		
48-pin PDIP		□	□		
48-pin HDIP		□	□		
52-pin LCC		□	□		
52-pin PLCC		□	□		
68-pin LCC		□	Now	Now	Now
68-pin PLCC		□	□	□	□
68 PGA		□	Now	Now	Now
Low-cost 68 PGA		□	□	□	□
84-pin LCC			Now	Now	Now
84-pin PLCC			□	□	□
84 PGA			Now	Now	Now
Low-cost 84 PGA				□	□
124-pin LCC			□	□	□
124-pin PLCC			□	□	□
124 PGA			Now	Now	2 options
Low-cost 124 PGA			□	□	□

*Package Abbreviations used for HCA6000-Series Arrays
PDIP: Plastic Dual In-line Package
HDIP: Side-Brazed Ceramic Dual In-line Package
LCC: Ceramic Leadless Chip Carrier
PLCC: Plastic Leaded Chip Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid ARRAY
□Check with your local sales office for availability

2-MICRON MACROCELL ARRAY PACKAGE FEATURE SUMMARY

Array Type	Package	Input-Only Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6206	016PDIP1	2	11	1	1	1	0
	028PDIP1 028HDIP1 028-LCC1 028-PCC1	4	21	1	1	1	0
	040PDIP1 040HDIP1	4	33	1	1	1	0
	044-LCC1 044-PCC1	4	33	1	1	1	4
HCA6212	028PDIP1 028HDIP1 028-LCC1 028-PCC1	2	21	2	2	1	0
	040PDIP1 040HDIP1	2	33	2	2	1	0
	044-LCC1 044-PCC1	4	35	2	2	1	0
	048HDIP1	7	36	2	2	1	0
	052-LCC1 052-PCC1	To Be Determined					
	068-LCC0 068-PCC0 068-PGA0 068LPGA0	17	42	4	4	1	0
HCA6225	040PDIP1 040HDIP1	2	33	2	2	1	0
	044-LCC1 044-PCC1	2	37	2	2	1	0
	052-LCC1 052-PCC1	2	45	2	2	1	0
	068-LCC1 068-PCC1 068-PGA1	2	61	2	2	1	0
	084-LCC1 084-PCC1 084-PGA1	5	74	2	2	1	0
	124-LCC1 124-PCC1 124-PGA1 124LPGA1	11	76	6	6	1	24
HCA6238	068-LCC1 068-PCC1 068-PGA1 068LPGA1	2	61	2	2	1	0
	084-LCC1 084-PCC1 084-PGA1 084LPGA1	2	77	2	2	1	0
	124-LCC1 124-PGA1 124LPGA1	2	93	4	4	1	20

2-MICRON MACROCELL ARRAY PACKAGE FEATURE SUMMARY (Continued)

Array Type	Package	Input-Only Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6248	068-LCC0 068-PCC0 068-PGA0 068LPGA0	29	30	4	4	1	0
	084-LCC0 084-PCC0 084-PGA0 084LPGA0	35	38	4	6	1	0
	124-LCC0 124-PCC0 124-PGA0 124-PGA1 124LPGA1	53	54	8	8	1	0

3-MICRON MACROCELL ARRAY PACKAGE AVAILABILITY

Package Type*	Array Type			
	HCA6306	HCA6312	HCA6324	HCA6348
28-pin PDIP	Now	Now		
28-pin HDIP	Now	Now		
40-pin PDIP	Now	Now	Now	
40-pin HDIP	Now	Now	Now	
44-pin LCC	Now	Now	Now	
44-pin PLCC	Now	Now	Now	
48-pin PDIP		☐	☐	
48-pin HDIP		☐	☐	
52-pin LCC		☐		
52-pin PLCC		☐		
68-pin LCC		Now	Now	
68-pin PLCC		☐	☐	
68 PGA		Now	Now	
Low-cost 68 PGA		☐	☐	
84-pin LCC			Now	Now
84-pin PLCC			☐	☐
84 PGA			Now	Now
Low-cost 84 PGA			☐	☐
124-pin LCC			☐	☐
124-pin PLCC			☐	☐
124 PGA			Now (2 options)	Now
Low-cost 124 PGA			☐	

*Package Abbreviations used for HCA6000-Series Arrays
PDIP: Plastic Dual In-line Package
HDIP: Side-Brazed Ceramic Dual In-line Package
LCC: Ceramic Leadless Chip Carrier
PLCC: Plastic Leaded Chip Carrier (Quad Pack)
PGA: Pin-Grid Array
LPGA: Low-Cost Pin-Grid ARRAY
☐Check with your local sales office for availability

3-MICRON MACROCELL ARRAY PACKAGE FEATURE SUMMARY

Array Type	Package	Input-Only Pins	I/O Pins	V_{DD} Pins	V_{SS} Pins	Dedicated Test Pins	Unconnected Pins
HCA6306	028PDIP1 028HDIP1	4	21	1	1	1	0
	040PDIP1 040HDIP1	4	33	1	1	1	0
	044-LCC1 044-PCC1	4	33	1	1	1	4
HCA6312	028PDIP1 028HDIP1	2	21	2	2	1	0
	040PDIP1 040HDIP1	2	33	2	2	1	0
	044-LCC1 044-PCC1	4	35	2	2	1	0
	048PDIP1 048HDIP1	7	36	2	2	1	0
	052-LCC0 052-PCC0	To Be Determined					
	068-LCC0 068-PCC0 068-PGA0 068LPGA0	17	42	4	4	1	0
HCA6324	040PDIP1 040HDIP1	11	24	2	2	1	0
	044-LCC1 044-PCC1	13	22	4	4	1	0
	048PDIP1 048HDIP1	15	24	4	4	1	0
	068-LCC1 068-PCC1 068-PGA1	25	34	4	4	1	0
	084-LCC0 084-PCC0 084-PGA0 084LPGA0	33	38	6	6	1	0
	124-LCC0 124-PGA0 124-PGA1 124LPGA1	55	56	6	6	1	0
HCA6348	084-LCC0 084-PCC0 084-PGA0 084LPGA0	35	38	4	6	1	0
	124-LCC0 124-PCC0 124-PGA0	53	54	8	8	1	0

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