Guide to Loopback Using the DP8390 Chip Set

National Semiconductor
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OVERVIEW

Loopback capabilities are provided to allow certain tests to be performed to validate operation of the DP8390 NIC, the DP8391 SNI, and the DP8392 CTI prior to transmitting and receiving packets on a live network. Typically these tests may be performed during power up of a node. The diagnostic provides support to verify the following:

1. Verify integrity of data path through each chip. Received data is checked against transmitted data.
2. Verify CRC logic's capability to generate good CRC on transmit.
3. Verify CRC recognition capability of the NIC on receive.
4. Verify that the address recognition logic can
   a. Recognize address match packets
   b. Reject packets that fail to match an address

LOOPBACK MODES

Loopback modes are selected by programming the Transmit Configuration Register. Bits LB0 and LB1 select the type of loopback to be performed. The NIC supports three modes of loopback: internal loopback through the DP8390 controller only *(Figure 1)*, external loopback through the DP8391 encoder/decoder *(Figure 2)*, and external loopback through the DP8392 transceiver *(Figure 3)*.

Loopback Operation in the NIC

To initiate a loopback test, a packet must first be assembled and transferred into the NIC buffer memory. Next, the Transmit Page Start Register, Transmit Byte Count Registers, and Transmit Configuration Register must be programmed. (When loopback mode is selected in the Transmit Configuration Register, the FIFO is split into two halves, one used for transmission and the other for reception.) Finally,

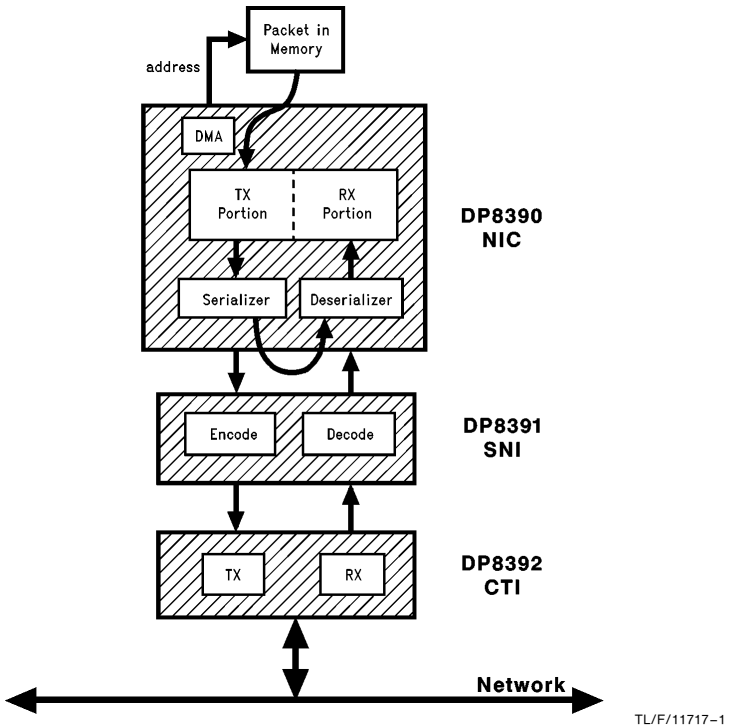

FIGURE 1. Loopback Mode 1: Through the Controller

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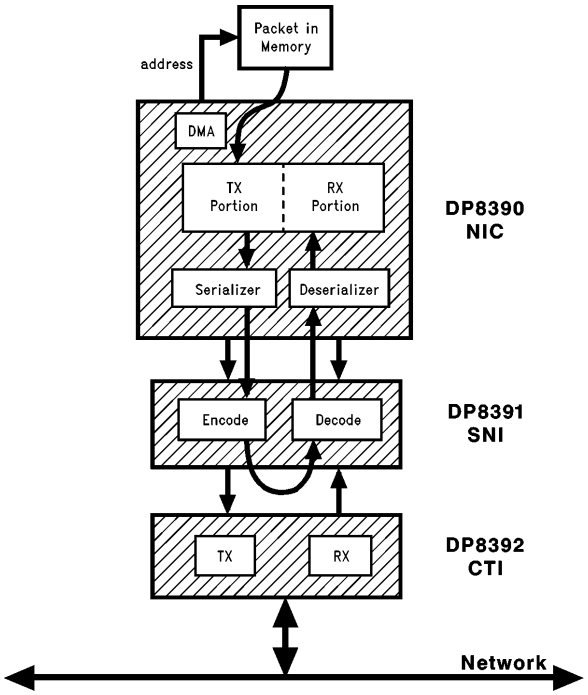

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FIGURE 2. Loopback Mode 2: Through the SNI

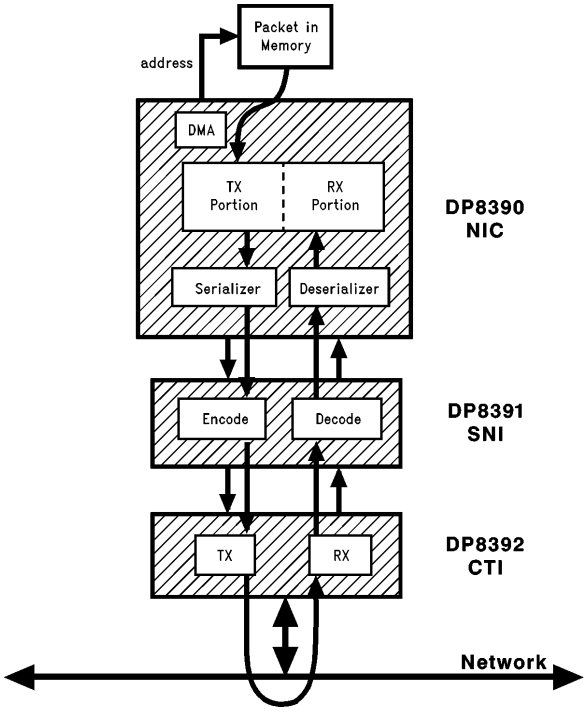

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FIGURE 3. Loopback Mode 3: To the Coax

the transmit command is issued to the Command Register, causing the following operations to occur:

Transmitter Actions

1. Data is transferred from memory by local DMA until the FIFO is filled. For each transfer, the Transmit Byte Count Registers (TBCR0 and TBCR1) are decremented. (Subsequent burst transfers are initiated when the number of bytes in the FIFO drops below the programmed threshold.)
2. The NIC generates 56 bits of preamble followed by an 8-bit synch pattern.
3. Data is transferred from the FIFO to the serializer.
4. If the Inhibit CRC bit is set in the Transmit Configuration Register, no CRC is calculated by the NIC, and the last byte transmitted is the last byte from the FIFO (last byte of the packet). This allows a software CRC to be appended. If the Inhibit CRC bit is not set, the NIC calculates and appends four bytes of CRC to the end of the packet.
5. At the end of transmission, the Packet Transmitted bit is set in the Interrupt Status Register.

Receiver Actions

1. Wait for synch (Start of Frame Delimiter), all preamble bits are ignored.
2. Store packet in the FIFO, increment receive byte count for each incoming byte.
3. If the Inhibit CRC bit is set in the Transmit Configuration Register, the receiver checks the incoming packet for CRC errors. If the Inhibit CRC bit is not set in the Transmit Configuration Register, the receiver does not check for CRC errors; the CRC error bit is set in the Receive Status Register (for address matching packets).
4. At the end of receive, the receive byte count is written into the FIFO and the Receive Status Register is updated. The Packet Received Intact bit is typically set in the Receive Status Register even if the address does not match. If CRC errors are forced, the packet must match the address filters in order for the CRC error bit in the Receive Status Register to be set.

Restrictions Using Loopback

Since the NIC is a half-duplex device, several compromises were required for the implementation of loopback diagnostics. Special attention should be paid to the restrictions placed on the use of loopback diagnostics.

1. The FIFO is split into two halves to allow some buffering of incoming data. The NIC transmits through one half of the FIFO and receives through the second half. Only the last five bytes of a packet can be examined in the FIFO; the DMA does not store the loopback packet in memory. Thus loopback can be considered a modified form of transmission.
2. Splitting of the FIFO has some bus latency implications. The FIFO depth is halved, thus reducing the amount of allowed bus latency. The Loopback Select bit (D3) in the Data Configuration Register should be set to allow all local DMA transfers to continue until the FIFO is filled. In cases where the latency constraints cannot be accommodated, small 7 byte packets can be transmitted. In addition, the FIFO must only be read (by successfully reading port 06h) when in loopback mode; reading the FIFO in other modes will result in the NIC failing to issue the ACK signal properly.
3. The CRC logic is shared by the receiver and the transmitter; thus the NIC cannot generate and check the CRC simultaneously. That is, if the Inhibit CRC bit is not set in the Transmit Configuration Register, the NIC generates and appends the CRC, and software must be used to verify the CRC. On the other hand, if the Inhibit CRC bit is set in the Transmit Configuration Register, the NIC will verify a software generated CRC.
4. Address recognition logic must be checked indirectly through a small series of tests (see Group III Loopback Tests: Address Recognition for further explanation).
5. Between consecutive transmissions in loopback mode, the Transmit Configuration Register must first be set to 00h and the Command Register reset to 21h (followed by a wait state of at least 1.5 ms for the NIC to reset). The desired loopback mode may then be programmed into the Transmit Configuration Register. This step guarantees alignment of the FIFO pointers when data is read from the FIFO.
6. Loopback only operates with byte wide transfers, thus special considerations must be made with word wide transfers. Since the FIFO is split, only half of each word is transferred into the transmit portion of the FIFO. The Byte Order Select bit in the Data Configuration Register can be used to select which half of the word is written into the FIFO (see *Figure 4*).

Note: Although a word is transferred to the NIC, only a byte is transmitted in the loopback packet. To properly transfer all the bytes in the loopback packet, the byte count must be 2 times the actual number of bytes assembled in the loopback packet.

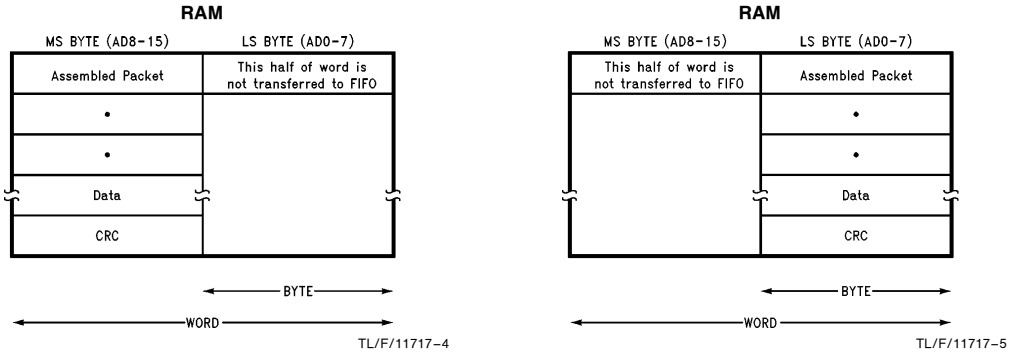

FIGURE 4. Packet Assembly for Loopback Work Wide Transfers

7. During heavily loaded network conditions, external loopback through the SNI and CTI could fail due to interference from the network.

Alignment of Data in the FIFO

During loopback, eight bytes of the FIFO are used for transmission and eight bytes are used for reception. Reception of the packet begins at location zero, and after the pointer reaches the last location in the receive portion of the FIFO, the pointer wraps back to location zero, overwriting the previously received data (see *Figure 5*). The pointer continues to circulate through the FIFO until the last byte is received. The NIC then appends the lower receive byte count and two copies of the upper receive byte count into the next three locations in the FIFO. Thus, only the last five bytes of the received packet may be retrieved.

Note: Although the size limit of a loopback packet is 64 kbytes, the byte counter rolls over at 2048 bytes.

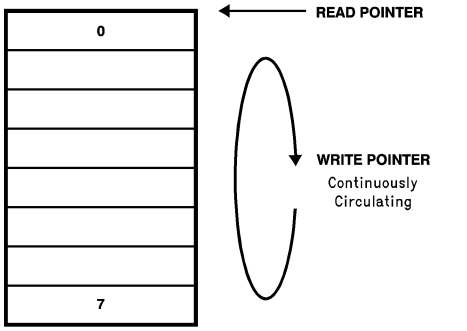

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FIGURE 5. Continuously Circulating FIFO Write Pointer During Loopback

To achieve the packet alignment shown in *Figure 6*, the packet length should be (N*8) + 5 bytes (i.e., 13, 21, etc). If the CRC is appended, the second through fifth byte will be the CRC appended by the NIC. This allows the CRC to be extracted from the NIC and compared to a previously calculated value for verification.

FIFO Location	FIFO Contents	
0	Byte (N*8) + 1	First Byte Read
1	Byte (N*8) + 2 (CRC1)	Second Byte Read
2	Byte (N*8) + 3 (CRC2)	•
3	Byte (N*8) + 4 (CRC3)	•
4	Byte (N*8) + 5 (CRC4)	•
5	Lower Byte Count	•
6	Upper Byte Count	•
7	Upper Byte Count	Last Byte Read

FIGURE 6. Alignment of Packet in FIFO Following Loopback

Loopback Tests

Three types of loopback tests may be performed to verify the data path through the DP8390 chip set. The tests are as follows:

1. Group I tests verify the CRC generation capability of the NIC. In this case, the NIC generates and appends a CRC to the loopback packet, and software is used to verify a matching CRC.
2. Group II tests verify the CRC recognition capability of the NIC. Here, the NIC verifies a software generated CRC.
3. Group III tests verify the address recognition logic of the NIC.

The loopback tests which follow were performed on the DP839EB. During each of the loopback tests, the Data Configuration Register was programmed to 40h.

GROUP I LOOPBACK TESTS: CRC GENERATION

The basic steps necessary to perform the Group I loopback tests (in which the CRC is appended by the NIC) are as follows:

1. Set Command Register to 21h (page 0).
2. Initialize Data Configuration Register to 40h.
3. Initialize Receive Configuration Register to 1Fh (promiscuous mode).
4. Initialize Transmit Byte Count Registers and Transmit Page Start Register.
5. Set Command Register to 22h (start mode).
6. Create loopback packet and transfer into NIC buffer memory.
7. Transmit dummy packet to check for unterminated or unconnected cable:
   a. Set Transmit Configuration Register to 00h (normal operation).
   b. Write FFh to Interrupt Status Register to reset.
   c. Set Command Register to 26h (transmit). Note that the Command Register must first be in start mode (22h) before transmitting (26h).
   d. Loop until the Packet Transmitted bit is set in the Interrupt Status Register. If the timeout loop completes and this bit is not set, the transmit has timed out, and the cable may not be connected.
   e. Check Interrupt Status Register for 08h (transmit Error. If the Transmit Error bit is set, excessive collisions have occurred, and the cable may not be terminated.
8. Start loopback mode 1 test (TCR = 02h):
   a. Reset Transmit Configuration Register to 00h.
   b. Reset Command Register to 21h. If the NIC is currently receiving a packet, it will wait for the reception of the current packet to complete before it will reset. Thus, a wait state of at least 1.5 ms is necessary to insure that the NIC will completely reset.
   c. Program the Transmit Configuration Register to the appropriate loopback mode.
   d. Write FFh to Interrupt Status Register to reset.
   e. Set Command Register to 22h (start mode).

f. Set Command Register to 26h (transmit).

g. Wait for transmit to complete (Command Register = 22h).

h. Check Interrupt Status Register for 06h (good transmission).

i. Read FIFO and compare CRC with previously calculated CRC.

9. Start loopback mode 2 test (TCR = 04h): See Step 8.
10. Transmit a dummy packet to change the contents of the FIFO. If this step is not taken before external loopback through the CTI and the AUI cable is not connected, the NIC does not receive anything into its FIFO. Thus the contents of the FIFO are not changed, and the loopback test reads a good CRC. See Step 7.
11. Start loopback mode 3 test (TCR = 06h): See Step 8.
12. If mode 3 lookback fails, transmission may have been aborted due to excessive collisions (check the Transmit Status Register). In this case, network traffic has interferred and the CTI may still be operational.

GROUP I RESULTS

The following examples show what results can be expected from a properly operating NIC during Group I loopback operations. The restrictions and results of each loopback mode are listed for reference.

Internal Loopback through the NIC

Path	TCR	RCR	TSR	RSR	ISR
NIC Internal (Mode 1)	02H	1FH	51H	02H	06H

Note 1: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

Note 2: CRC errors are always indicated by the receiver if the CRC is appended by the transmitter.

Note 3: Only the Packet Transmitted and Receive Error bits in the Interrupt Status Register are set; the Packet Received bit is set only if status is written to memory. In loopback this action does not occur, and the Packet Received bit remains 0 for all loopback modes.

External Loopback through the SNI

Path	TCR	RCR	TSR	RSR	ISR
NIC External (Mode 2)	04H	1FH	41H	02H	06H

Note 1: CD Heartbeat is set in the Transmit Status Register; Carrier Sense Lost is not set since it is generated by the external encoder/decoder.

External Loopback through the CTI

Path	TCR	RCR	TSR	RSR	ISR
NIC External (Mode 3)	06H	1FH	01H	02H	06H

Note 1: CD Heartbeat and Carrier Sense Lost should not be set. The Transmit Status Register could, however, also contain 01, 03, 07, and a variety of other values depending on whether collisions were encountered or the packet was deferred.

Note 2: The Interrupt Status Register will contain 08 if the packet is not transmittable.

During external loopback the NIC is now exposed to network traffic. It is therefore possible for the contents of both the receive portion of the FIFO and the Receive Status Register to be corrupted by any other packet on the network. Thus, in a live network, the contents of the FIFO and Receive Status Register should not be depended on. The NIC will still abide by the standard CSMA/CD protocol in external loopback mode (the network will not be disturbed by the loopback packet).

GROUP II LOOPBACK TESTS: CRC RECOGNITION

The basic steps necessary to perform the Group II loopback tests (in which a software CRC is appended to the packet) are similar to those outlined previously for the Group I tests, with the following exceptions:

1. The loopback packet created must have a software appended CRC.
2. When programming the Transmit Configuration Register to the desired loopback mode, the Inhibit CRC bit must be set.
3. After the loopback packet has been transmitted, check the Interrupt Status Register and/or the Receive Status Register for CRC errors. If a CRC error has occurred, the loopback test has failed.

GROUP II RESULTS

The following examples show what results can be expected from a properly operating NIC during Group II loopback operations. The restrictions and results of each loopback mode are listed for reference.

Internal Loopback through the NIC

Path	TCR	RCR	TSR	RSR	ISR
NIC Internal (Mode 1)	03H	1FH	51H	01H	02H

Note 1: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

Note 2: Only the Packet Transmitted bit in the Interrupt Status Register is set. The packet received bit is set only if status is written to memory. In loopback this action does not occur, and the Packet Received bit remains 0 for all loopback modes.

External Loopback through the SNI

Path	TCR	RCR	TSR	RSR	ISR
NIC External (Mode 2)	05H	1FH	41H	01H	02H

Note 1: CD Heartbeat is set in the Transmit Status register; Carrier Sense Lost is not set since it is generated by the external encoder/decoder.

External Loopback through the CTI

Path	TCR	RCR	TSR	RSR	ISR
NIC External (Mode 3)	07H	1FH	01H	01H	02H

Note 1: CD Heartbeat and Carrier Sense Lost should not be set. The Transmit Status Register could, however, also contain 01, 03, 07, and a variety of other values depending on whether collisions were encountered or the packet was deferred.

Note 2: The Interrupt Status Register will contain 08 if the packet is not transmittable.

During external loopback the NIC is now exposed to network traffic. It is therefore possible for the contents of both the received portion of the FIFO and the Receive Status Register to be corrupted by any other packet on the network. Thus, in a live network, the contents of the FIFO and Receive Status Register should not be depended on. The NIC will still abide by the standard CSMA/CD protocol in external loopback mode (the network will not be disturbed by the loopback packet).

GROUP III LOOPBACK TESTS: ADDRESS RECOGNITION

The address recognition logic cannot be directly tested. However, the CRC Error and Frame Alignment Error bits in the Receive Status Register are set only if the address of the packet matches the address filters. Thus, if errors are expected to be set and they are not set, the packet has been rejected on the basis of an address mismatch.

GROUP III RESULTS

One method of testing the address recognition logic would be to transmit two loopback packets, one with a matching physical address, and one with a non-matching address. Both packets should have a CRC appended by the NIC. Expected results for each case follow.

Internal Loopback through the NIC: Matching Physical Address

Path	TCR	RCR	TSR	RSR	ISR
NIC Internal (Mode 1)	02H	00H	51H	02H	06H

Note 1: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

Note 2: CRC errors should be seen in both the Receive Status Register and the Interrupt Status Register for an address matching packet.

Note 3: Only the Packet Transmitted and Receive Error bits in the Interrupt Status Register are set; the Packet Received bit is set only if status is written to memory. In loopback this action does not occur, and the Packet Received bit remains 0 for all loopback modes.

Internal Loopback through the NIC: Non-Matching Physical Address

Path	TCR	RCR	TSR	RSR	ISR
NIC Internal (Mode 1)	02H	00H	51H	01H	02H

Note 1: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

Note 2: CRC errors should not be detected for a non-matching physical address.

Note 3: Only the Packet Transmitted bit in the Interrupt Status Register is set. The packet received bit is set only if status is written to memory. In loopback this action does not occur, and the Packet Received bit remains 0 for all loopback modes.

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