Comparison of COP878x to the Enhanced COP8SAx7 Family—Hardware/ Software Considerations

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INTRODUCTION

The COP8780, COP8781 and COP8782 (COP878x family) are members of the COP8 Basic Family that contain EPROM, RAM, a 16-bit multi-function timer with a single 16-bit autoreload/capture register, 3 interrupt sources with polling scheme, and the MICROWIRE/PLUS™ serial interface. These devices are offered in 20-pin SO/DIP, 28-pin SO/DIP, 40-pin DIP, and 44-pin PLCC. The operating voltage range is from 4.5V to 6.0V.

The COP8SAA7, COP8SAB7 and COP8SAC7 (COP8SAx7 family) devices, on the other hand, are members of the COP8 Feature Family that contain EPROM, RAM, a 16-bit multi-function timer with two autoreload/capture registers, eight interrupt sources supporting vectored interrupt scheme, and the enhanced MICROWIRE/PLUS serial interface. In addition, these devices contain features such as Multi-Input Wakeup, WATCHDOG™/Clock Monitor, Idle timer supporting Idle mode, internal Power-On Reset, on-chip RC oscillator, 8 bytes of user storage space in EPROM, and on-chip EMI reduction circuitry. The devices are offered in 16-pin SO/DIP, 20-pin SO/DIP, 28-pin SO/DIP, 40-pin DIP, and 44-pin PLCC. The operating voltage range is from 2.7V to 5.5V. See the datasheet for more details.

The purpose of this Application Note is to provide a detailed comparison and feature analysis of these two family of devices. Where applicable, this report can be used to assist in converting the code written for the COP878x device to operate on an equivalent COP8SAx7 device.

As suggested, the COP8SAx7 family offers a broad range of additional useful and enhanced features as compared to the COP878x family. With the additional features, the COP8SAx7 family may appear much different, but this family is designed to maintain downward compatibility with the COP878x family as much as possible. The intention has been to offer the COP878x user the capability to maintain the same PCB when converting to COP8SAx7 without any PCB changes.

HIGHLIGHTS OF COP8SAx7 ENHANCEMENTS OVER COP878x

1. The operating voltage range is wider (2.7V to 5.5V).
2. The dynamic supply current is lower.
3. Four additional high sink current outputs (L0–L3) are added (min sink current of 15 mA at $V_{OL} = 1.7$, $V_{CC} = 4.5V$).
4. The R/C oscillator option is expanded to include the choice of selecting on-chip R/C components. The use of on-chip R/C eliminates the cost associated with external R/C oscillator components.
5. The crystal oscillator option is expanded to include the choice of selecting on-chip biasing resistor.
6. COP878x's Port I is replaced with a bi-directional Port F.
7. Schmitt trigger inputs are added to Port L.
8. Pins 21–24 (Ports C4–C7), on the 44-pin PLCC package, are general purpose I/O ports. They are No Connection (NC) on the COP878x.
9. Stack Pointer is automatically initialized by hardware.
10. The user selectable Power-On reset feature is added, in addition to the ability to reset the device externally. The on-chip power-on reset eliminates the need for using external components associated with reset circuitry.
11. The HALT feature is made user selectable.
12. The unique power saving Multi-Input Wakeup feature is added.
13. The interrupt handling is enhanced to support a versatile vectored interrupt scheme. It has a total of eight interrupt sources with independent vectors. The COP878x has a polled interrupt scheme.
14. The Software Trap scheme is enhanced to include its own pending flag.
15. The MICROWIRE/PLUS serial interface is enhanced to include shifting on the alternate clock edge and programmable idle polarity for the shift clock. This allows compatibility with SPI peripherals.
16. The 16-bit multi-function timer/counter is improved to include two autoreload/capture registers. The timer block contains two separate interrupt vectors and two I/O pins. The COP878x timer has a single autoreload/capture register, a single interrupt source, and a single I/O pin.
17. The ECON register is expanded to select additional user selectable features such as WATCHDOG, Power-On Reset, on-chip R/C oscillator, on-chip crystal oscillator biasing resistor, and HALT mode.
18. Added a free running IDLE timer.
19. Added the power saving IDLE mode.
20. Added the user selectable WATCHDOG/Clock Monitor logic.
21. Nine instructions are added to the basic instruction set. The instructions are ANDSZ, IFNE, RLCA, VIS, POP A, PUSH A, RPND, LD B and IFEQ Mem,Imm.
22. The device is offered in 16-pin DIP/SO.
23. Eight bytes of user storage space in EPROM are added in addition to regular program memory space.
24. EMI reduction circuitry is added to achieve low radiated emissions.

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SUMMARY OF DIFFERENCES BETWEEN COP878x AND COP8SAx7

The following table provides a detailed summary of differences between the COP878x and COP8SAx7.

TABLE I

Features	COP878x Family	COP8SAx7
Operating Voltage	4.5V to 6.0V	2.7V to 5.5V
Dynamic Supply Current CKI = 10 MHz	21 mA	7 mA
Typical HALT Current	$< 1\ \mu A$	$< 4\ \mu A$
Port L0–L7	Port L does not have Schmitt Trigger inputs.	Port L has Schmitt Trigger inputs.
Port L0–L3 Min Sink Current $V_{OL} = 1.7V$ at $V_{CC} = 4.5V$	2.0 mA	15 mA
R/C Oscillator	External RC Components	On-Chip RC or On-Chip RC with External C.
R/C Oscillator Frequency Tolerance	R/C Oscillator tolerance is different than COP8SAx7. For example: for CKI = 1 MHz, R = ±1%, C = ±5%, frequency tolerance is approximately ±25% (see Datasheet for more points).	R/C Oscillator tolerance is different than COP878x. For example: for CKI = 1 MHz, using on-chip R/C or on-chip RC with external C, frequency tolerance is approximately ±35% (see Datasheet for more data points).
Crystal Oscillator	External crystal circuitry with external bias Resistor.	External crystal circuitry with the option of choosing external or internal bias resistor.
Input Only Port	Port I is an 8-bit input only port.	Port I is replaced with an 8-bit I/O (Port F).
Pin G1	Pin G1 is an I/O pin.	Pin G1 is a dedicated WATCHDOG output pin if WATCHDOG logic enabled. It is a general purpose I/O if WATCHDOG is not enabled.
Pin G2	Pin G2 is a general purpose I/O.	Pin G2 is a general purpose I/O or the timer second input capture.
NC Pins on the 44-Pin Package	Pins 21–24 are No Connection (NC).	Pins 21–24 are C4–C7 (I/O Pins).
Stack Pointer	The Stack Pointer must be initialized with software.	The Stack Pointer is initialized by hardware internally on reset.
RAM Map	1. Location 0FF Hex is a general purpose RAM register. 2. Location 0D7 hex is for Port I input pins.	1. Location 0FF Hex is reserved for future RAM expansion. If compatibility with future devices (with more RAM) is not desired, this location can be used as a general purpose RAM location. 2. Location 0D7 Hex is reserved. Port I is replaced by Port F. Port F is read into RAM location 96 Hex instead of location D7 Hex.
Reset	External reset only.	External reset or using on-chip user selectable power-on reset. The external RC delay must be greater than 5x Power Supply Rise time or 15 μs, whichever is greater.
HALT Mode	HALT mode is always enabled.	HALT can be enabled or disabled through ECON control bit.
Exit from HALT Mode	Exit from HALT through Reset or G7 pin (if not used as the oscillator output).	Exit from HALT through reset or G7 pin (if not used as the oscillator output) or Multi-Input Wakeup.
Interrupt Handling	Polled Interrupts	Vectored Interrupts
Interrupt Sources	Software Trap External Interrupt Timer Interrupt	Software Trap External Interrupt Timer Interrupt (2) Multi-Input Wakeup IDLE MICROWIRE/PLUS Default VIS

SUMMARY OF DIFFERENCES BETWEEN COP878x AND COP8SAx7 (Continued)

The following table provides a detailed summary of differences between the COP878x and COP8SAx7. (Continued)

TABLE I (Continued)

Features	COP878x Family	COP8SAx7
Software Trap	Software Trap does not set a pending flag.	Software Trap sets a pending flag.
MICROWIRE/PLUS	1. Does not allow shifting at alternate clock edge. 2. Does not support programmable idle polarity for the shift clock. 3. In Slave mode, the shift clock does not stop after 8 clock pulses.	1. Allows shifting at alternate clock edge. 2. Supports programmable idle polarity for the shift clock for SPI compatibility. 3. In Slave mode, the shift clock stop after 8 clock pulses.
Multifunction 16-Bit Timer	The timer has: 1. One 16-bit counter with a single 16-bit register. 2. One I/O pin. 3. One interrupt source. 4. No underflow interrupt pending flag in the capture mode.	The timer has: 1. One 16-bit counter with two 16-bit registers. 2. One output and two input pins. 3. Two interrupt sources. 4. Underflow interrupt pending flag in the capture mode.
ECON Register	ECON register selects the security, clock, and RAM size options.	ECON register selects the security, clock, WATCHDOG, power-on reset, and HALT options. Bit functions for the clock option and bit polarity for the security option are different. RAM size is selected by device.
Idle Timer/Idle Mode	Does not contain an Idle Timer. Does not support Idle Mode.	Contains an Idle Time. Supports Idle Mode.
WATCHDOG/Clock Monitor	Does not contain WATCHDOG/Clock Monitor.	Contains WATCHDOG/Clock Monitor.
Instruction Set	COP8 Basic family instruction set.	COP888 Feature family instruction set (9 additional instructions as compared to Basic family). The instructions are ANDSZ, IFNE, RLCA, VIS, POP A, PUSH A, RPND, LD B, and IFEQ Mem,Imm.
Packages	20-pin SO/DIP, 28-pin SO/DIP, 40-pin DIP, 44-pin PLCC.	16-pin SO/DIP, 20-pin SO/DIP, 28-pin SO/DIP, 40-pin DIP, 44-pin PLCC.
Reading EPROM with Security Enabled	Reads E0 Hex	Reads FF Hex
Contents of ECON Register Shipped from the Factory	Windowed: FF Hex OTP: 7F Hex	Windowed: 00 Hex OTP: 80 Hex
Contents of Program Memory in the Erased State	FF Hex	00 Hex **Note:** Erasure time higher (see Datasheet).
EMI	Does not include EMI reduction circuitry.	Contains EMI reduction circuitry.

COMPATIBILITY—CONVERTING FROM COP878x TO COP8SAx7

The review of differences outlined in Table I, leads to the following steps to be followed in converting from the COP878x to COP8SAx7:

Hardware/ECON Register Considerations

1. R/C Oscillator

Bits 3 and 4 of ECON register must be programmed with 1 and 0 respectively. This will select the on-chip R/C components. External R/C components are not needed unless different operating frequency is required. For a different operating frequency, only a small external capacitor needs to be added from the CKI to the GND pin. See the datasheet for the appropriate capacitor value. There are differences in R/C oscillator tolerances between the COP878x and COP8SAx7. For comparison, see the datasheets for these devices.

2. Crystal Oscillator

Bits 3 and 4 of ECON register must be programmed with 0 and 1 respectively. This will select the crystal oscillator with external biasing resistor. No change to the external crystal oscillator circuitry is required.

3. External Oscillator

Bits 3 and 4 of ECON register must be both programmed with 0.

4. Security Feature

Bit 5 of ECON register must be programmed with 1 to enable the security feature, otherwise must contain a 0 for the security feature to be disabled. This polarity is opposite of COP878x.

5. Reset

Bit 6 of ECON register must be programmed with 0 to disable the on-chip Power-On Reset. The RC delay must be greater than 5x Power Supply rise time or 15 μs, whichever is greater.

6. HALT Mode

Bit 0 of ECON register must be programmed with 0 to enable the HALT mode.

7. WATCHDOG

Bit 2 of ECON register must be programmed with 1 to disable the WATCHDOG logic. This will allow the G1 pin to serve as a general purpose I/O.

8. RAM Select

RAM size is selected by device. For example, COP8SAA has 64 bytes of RAM and COP8SAB/COP8SAC has 128 bytes of RAM.

9. Bit 7 of ECON Register

It is a factory test bit. The polarity is ''Don't Care''.

Software Considerations

1. Pins 21–24 (Ports C4–C7) on the 44-Pin Package

These pins are No Connection (NC) on the COP878x, but are general purpose I/O on the COP8SAx7.

2. Stack Pointer

If the Stack Pointer (SP) is initialized to a value different than 2F Hex (64 bytes of RAM selected) or to 6F Hex (128 bytes of RAM selected), in the code written for COP878x, the SP initialization instruction can be kept in the user program as is although the hardware initializes SP to 2F or 6F (depending on RAM size). If the COP878x code is initializing the SP to 2F Hex or 6F (depending on the RAM size), the initializing instruction can be deleted. If no code changed is desired, the initialization instruction can stay as is (although redundant).

3. Port I/Port F Configuration

Since Port I is replaced by Port F on the COP8SAx7, Port F is configured as Hi-Z inputs upon reset. This means Port F data register (RAM location 94 Hex) and Port F configuration register (RAM location 95 Hex) both contain values of 0 upon reset and user code must ensure they stay at 0. In addition, Port F is read into RAM location 96 Hex instead of RAM location D7 Hex. The COP878x code must be modified to reflect this change.

4. RAM Location FF Hex

RAM location FF Hex is a general purpose RAM location on the COP878x, but it is reserved on the COP8SAx7 for future RAM expansion. If compatibility with future devices (with more RAM) is not desired, this location can be used as a general purpose RAM location to maintain compatibility with COP878x.

5. Multi-Input Wakeup

The COP8SAx7 offers the power saving Multi-Input Wakeup feature. This feature is an alternate function of Port L. The COP878x does not offer this feature. Still there is no code change required because during reset initialization, the Wakeup Enable (RAM address location C9 Hex) register is cleared thus disabling the Multi-Input Wakeup feature.

6. Interrupt Handling

COP878x supports the interrupt polling scheme and it has only three interrupt sources. With the polling scheme, all interrupts cause immediate jump to the single fixed program memory location 0FF Hex. The user program must poll all interrupt pending bits to determine the cause of the interrupt. Once the cause is determined, the user program may jump to an appropriate interrupt handling routine.

The COP8SAx7, with up to eight interrupt sources, supports both polled and vectored interrupt schemes. With the vectored interrupt scheme, a vector table is used. The vector table placed in the program memory, contains the start addresses for each of the user's interrupt routines. This table is used by the device to determine where to jump when a particular interrupt occurs. When an interrupt occurs, the device initially jumps to the single fixed program memory location 0FF Hex. Then user program may call a special instruction (VIS) to cause a jump to the vector table followed by a jump to user specified interrupt service routine. The user may elect not to use the VIS instruction, not place the vector table in the program memory, and simply poll each interrupt pending bit as described for the COP878x.

In order to keep the COP878x interrupt handling code compatible with the COP8SAx7, all additional interrupt sources that are available on the COP8SAx7 must be disabled. These additional sources include interrupts associated with the Idle timer, MICROWIRE/PLUS, and Multi-Input Wakeup. Since the COP8SAx7 multi-function timer block contains two interrupt sources, to maintain compatibility with the COP878x, the second interrupt source (Timer T1B Interrupt Enable) must be disabled. All the Enable bits associated with these additional interrupt sources reside in the ICNTRL register (RAM location E8 Hex) and are cleared upon reset. Therefore, there is no code modification required as long as the user keeps the new additional sources disabled, and not use the additional COP8SAx7 interrupt feature (VIS instruction and vector table).

Software Interrupt

The COP8SAx7 software interrupt has a pending flag. This flag is not memory mapped and is cleared by the special RPND instruction. To keep the COP878x code compatible with that of the COP8SAx7 and vectored interrupt scheme is not used, upon entering the interrupt routine (program memory location 0FF Hex), the user program must execute the RPND instruction. This will reset the software interrupt pending flag. The next step is to check the timer and external interrupt pending bits. If none are set, it gives the indication that a software interrupt has occurred.

7. Timer

The timer block contains a second 16-bit register that can be used as an autoreload or capture register depending on the timer operating mode. The following steps need to be considered to run the code written for the COP878x timer on the COP8SAx7.

PWM Mode

a. The second interrupt source must remain disabled (T1ENB bit in the ICNTRL register must be 0). T1ENB bit is cleared upon reset.

b. Pin G3 (T1A) must be used as the timer PWM output pin. Pin G2 is available as a general purpose I/O.

c. The timer's second reload register (T1RB) must be loaded with the same value as the contents of T1RA. This means an instruction must be inserted into the COP8SAx7 code to initialize T1RB.

External Event Mode

a. The second interrupt source must remain disabled (T1ENB bit in the ICNTRL register must be 0). T1ENB bit is cleared upon reset.

b. Pin G3 (T1A) must be used as the timer external event input pin. Pin G2 is available as a general purpose I/O.

c. The timer's second reload register (T1RB) must be loaded with the same value as the contents of T1RA. This means an instruction must be inserted into the COP8SAx7 code to initialize T1RB.

Capture Mode

a. The second interrupt source must remain disabled (T1ENB bit in the ICNTRL register must be 0). T1ENB bit is cleared upon reset.

b. Pin G3 (T1A) must be used as the timer input capture pin. The alternate function of pin G2 (G2 is available as a general purpose I/O) and the capture register T1RB must be ignored. The user can simply read the capture register T1RA.

8. MICROWIRE/PLUS

The MICROWIRE/PLUS feature on the COP8SAx7, supports shifting serial data with the alternate edge of the shift clock and has the ability to select idle polarity for the shift clock. To ensure compatibility with COP878x, bit 6 of Port G configuration register and bit 5 of Port G data register must both contain 0. Upon reset, these bits are cleared and the user code must ensure they stay at 0. In the slave mode, the shift clock on the COP8SAx7 does not stop after 8 clock pulses. The shift clock on the COP8SAx7, on the other hand, stops after 8 clock pulses. No change is required as a result of this difference.

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