Startup Time, Profile Measurement of PLL VCOs and Crystal Oscillators

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Introduction

The startup time of a system clock is an important parameter in communication systems and PLL circuits. Whether it is a cell phone, disk drive, or palm communicator, they all shutdown periodically to save power. It is imperative that the clock "awakes" rapidly to its target frequency with minimium system latency and to conserve power. Especially in the radio communication arena, clock start-up conditions determine the performance, system specifications, and programming requirements.This note intends to alleviate the anxiety and pain that have been associated with startup time measurements, by introducing a test setup that is user friendly and convenient to build.

Conventional Method

There are several ways of ascertaining the settling or lock time of a clock output. One is to utilize a storage or digital sampling oscilloscope. You would typically trigger it off the power-down signal, and monitor the clock output. If the instrument has sufficient memory and/or resolution capability, it may render you a crude estimate of the oscillation frequency or period as a function of time.

Complicated Method

Using more sophisticated equipment such as a Time Interval Analyzer or Domain Modulation Analyzer, you may examine the clock settling profile more accurately. Though they are "trickier" to setup, decent result may be obtained. However, characterizing oscillators and PLLs for wireless communications in particular, the aforementioned machines alone often required exorbitant patience and courage to cultivate meaningful, if repeatable, data. This is because these machines can handle frequency hops quite well, but not startup. Thus, arming and interfacing to test probe issues are among some of the culprits that often frustrate the users and hinder their progress.

Counter Method

The concept behind this method is to simply make a frequency or time interval measurement of the oscillator/clock output via a (user set) time window. The accuracy of which can easily render better than 1 ppm depending on the resolution of the counter employed. Moreover, since the apparatus is made up of two or three instruments, there are more hooks available for monitoring and for optimizing your test needs.

Typical Bench Setup

A sample measurement setup consists of the following instruments: An universal time interval counter such as a Stanford Research SR-620, or HP5370B UTIC; two Pulse/function generators such as SR-DG535 and/or HP3325B; a LeCroy- 9354L digital scope or equivalent; and a FET probe. The basic connection is depicted in *Figure 1*.

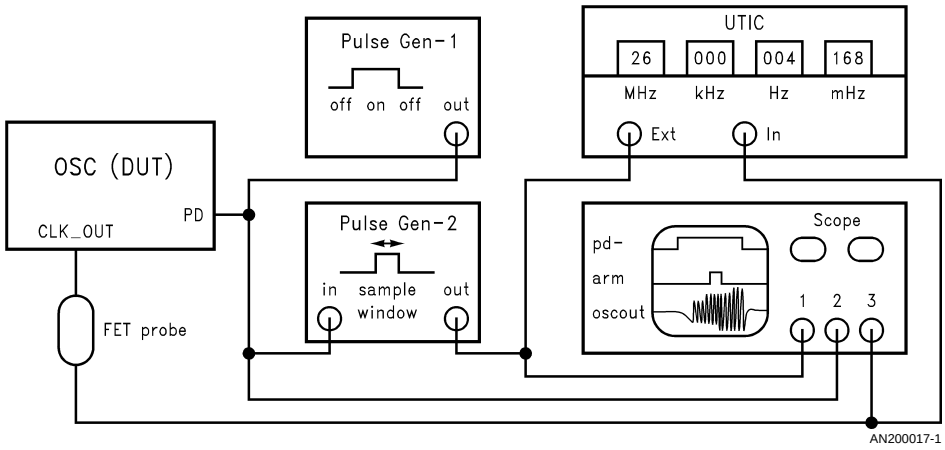

FIGURE 1. Sample Measurement Setup

Example: DUT with 26 MHz output

Pulse Gen-1:	Period=0.1s; CMOS levels
Pulse Gen-2:	Trigger off Pulse-Gen-1; T_W=10 µs; Delay=user
UTIC:	Ext. arm/trig by Pulse Gen-2; Input=FET Probe; Samples=10; Mode=Period or Frequency
Sampling Scope:	Trigger off Pulse Gen-1; Horizontal ≥ 200 Ms/s; Memory depth ≥ 200 Mpt

Frequency vs Time Measurement

By setting the "sample window" pulse delay and width appropriate for your system, you may record the oscillator frequency at any instance within the duration the oscillator is powered-up. *Figure 1* shows a typical test connection where you would externally arm the counter with the "sample window" pulse, and use a FET probe to feed the signal to the scope/counter. When the signal amplitude becomes very low such as during startup, it is recommended to set the counter to "auto trigger", and trim the probe's DC offset as necessary for an optimal triggering level.

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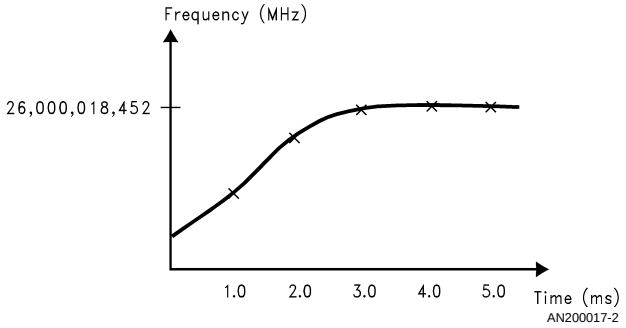

FIGURE 2. Plot of a Xtal Oscillator Startup Time Profile

Measurement Tips

1. Extraneous perturbations: As with any sensitive analog measurements, ensure your test environment is “clean and quiet”. Harmony between Heaven & Earth (radiation and grounding) is imperative to success. That is, not to ground your system to the “Earth” ground to avoid coupling noise from other systems (like an elevator or refrigerator). Allow no power cycling in your neighborhood such as from a cryo_thermo machine or a soldering iron with temperature regulation, microwave oven, etc. And avoid turning on your radio/cell-phone. Confine the test in a Faraday case as necessary and, lastly, do not turn on any fluorescent lamp while you are inside!

2. Choosing Probes: You should use a FET probe to monitor the oscillator output to minimize the loading effects. The HP85024A is a fine choice, but, the TEK P6201/02A has demonstrated exceptional performance in most cases. These probes exhibit CL=1.5 pF (when used with a X10 attenuation tip) and have DC offset adjustment to further facilitate triggering of the counter.

Summary

Oscillator startup or frequency pushing measurement setup described in this note is easy to assemble. It’s made up of some low cost general purpose equipment, which produces a fixture capable of uncompromising precision and accuracy.

The test setup may be further automated with a PC and applicable software such as Visual Basic, which performs shifting the sampling window, capturing the data, and plotting the startup profile automatically.

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