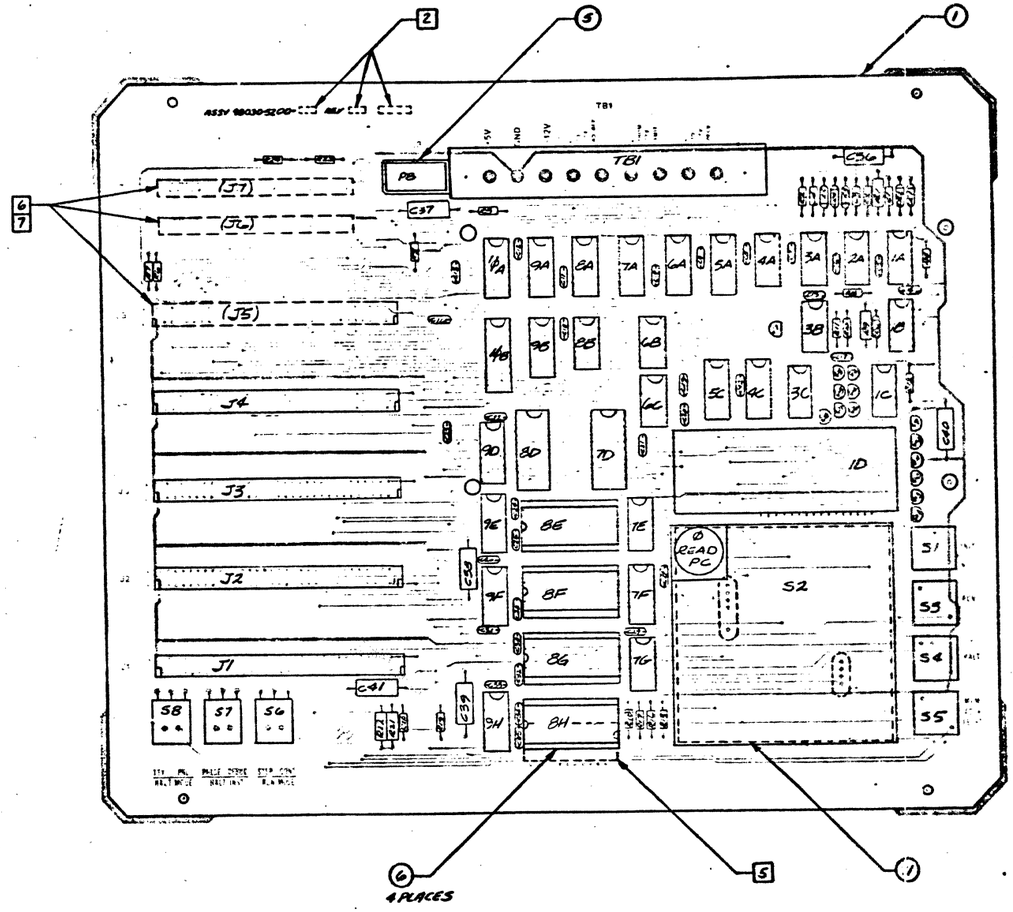
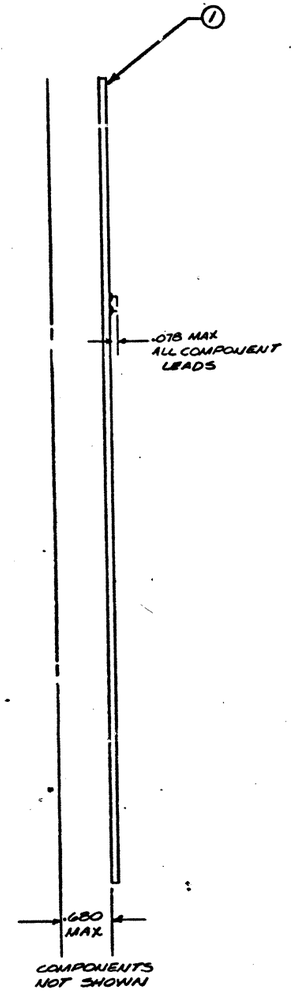
X383-1

REVISIONS			
APPROVED	DATE	DCN NUMBER	REV
[illegible]	4-K-76	PROD. RQ. J137-0748	A
[illegible]	7/1/76	DCN IMP-2678	B
[illegible]	12 DEC 77	DCN# IMP-2787	C
[illegible]	[illegible]	DCN# IMP-2992	D





NOTE - UNLESS OTHERWISE SPECIFIED:
1. FRONT SIDE CIRCUITRY SHOWN SHADED FOR CLARITY
2. MARK APPLICABLE DASH NO., REV LEVEL AND S/N J2 -.18 HIGH CHARACTERS APPROX. AS SHOWN
3. FOR LOGIC DIAGRAM SEE 8703052ØØ
4. LOCATION NO/REF DES SHOWN FOR REF
5. HOLE PATTERN (BJ) FOR FUTURE OPTION
6. J5, J6 & J7, ARE OPTIONAL (CUSTOMER INSTALLS)
7. HOLES FOR J5, J6, J7 (168 HOLES) ARE TO BE FREE OF SOLDER

QTY REQD	ITEM	PART NUMBER	DESCRIPTION
		MATERIALS	
NEXT ASSEMBLY	MATERIAL	SEE B/M	
USED			
		NORM Inspect 10 Aug 76	
		2 Aug 76	
		OTHER SPECIFIED	
		DIMENSIONS IN INCHES AND INCLUDE CHEMICALLY [illegible] FINISH	
		TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± 1/32 DECIMALS ± .010 ANGLES ± 30' BREAK SHARP EDGES BREAK SHARP CORNERS	

National Semiconductor Corporation
2900 Semiconductor Drive Santa Clara, Calif 95051

ASS'Y PRINTED WIRING -
SCIMP LCDS
MOTHERBOARD (EURO CARD)

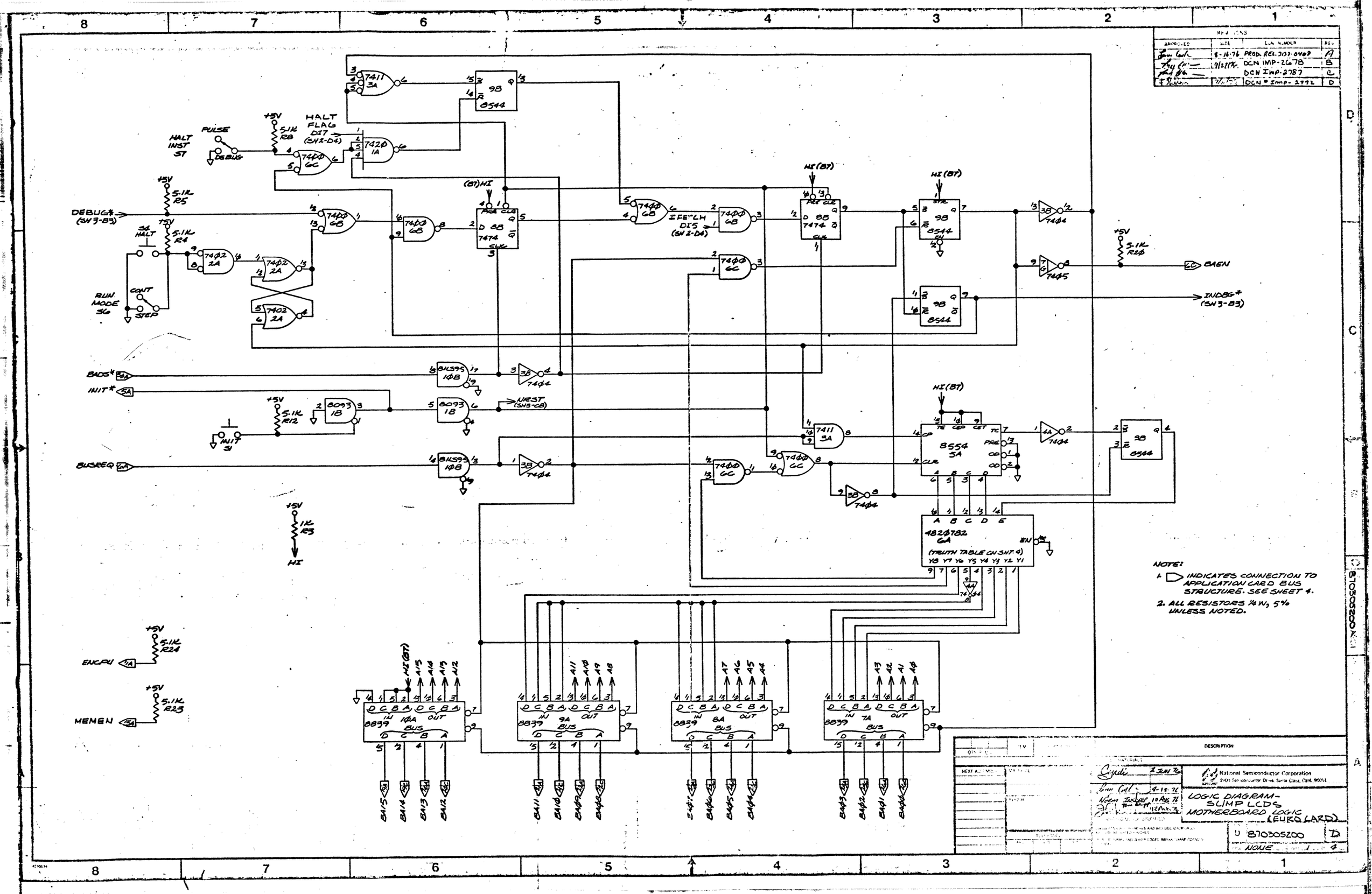
SIZE	DWG NO	REV
D	98Ø3052ØØ	D

SCALE 1 TO 1 WEIGHT 1 1 1

4230034

FORMAT A-4A

D 98Ø3052ØØ D



REVISIONS
APPROVED | DATE | DCN NUMBER | REV
8-16-76 | PROD. REL. 3137-0409 | A
DCN IMP-2678 | B
DCN IMP-2787 | C
DCN # IMP-2992 | D
HALT INST S7
PULSE
DEBUG
HALT FLAG DI7 (SH2-D4)
DEBUG* (SH3-B3)
S4 HALT
RUN MODE S6
CONT
STEP
BADS*
INIT*
INIT S1
BUSREQ
ENCPU
MEMEN
NRST (SH3-C8)
IFETCH DI5 (SH2-D4)
HI (B7)
BAEN
INDBG* (SH3-B3)
8554 5A
4820782 6A
(TRUTH TABLE ON SHT. 4)
8839 10A
8839 9A
8839 8A
8839 7A
NOTE:
1. INDICATES CONNECTION TO APPLICATION CARD BUS STRUCTURE. SEE SHEET 4.
2. ALL RESISTORS 1/4 W, 5% UNLESS NOTED.
DESCRIPTION
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051
LOGIC DIAGRAM-
SLIMP LCDS
MOTHERBOARD LOGIC
(EUROCARD)
D 870305200 D
NONE 1 4
870305200

REVISIONS			
APPROVED	DATE	DCN NUMBER	REV
		SEE SHT 1	

FDSEL* (SH 3-C8)

MEMSEL*

A11 (SH1-A5)

A10 (SH1-A5)

A9 (SH2-A5)

A15 (SH2-A6)

(SH1-A6) A14
(SH1-A6) A13
(SH1-A6) A12

74S155 9D

74S40 1A

74S04 1A

MM5204/14/44 8E ISP-8F/0018

MM5204/14/44 8F ISP-8F/00DA

MM5204/14/44 8G ISP-8F/0018 OR ISP-8F/000NB

MM5204/14/44 8H ISP-8F 000A -OR ISP-8F/000NA

8T39 9F

8T39 9E

A8 (SH1-A5)

MM2101 8D

MM2101 7D

MM5246 (OPTIONAL) SEE NOTE 1 8J

BRDS* B7C

BWDS* B7D

8T595 10B

8T595 10B

NRS (SH3-A8)

NWS (SH3-C8)

FROM TTY XMIT TB1-7 −

510Ω ½W R21

-12V

+5V

1N3604 CR5

1N3604 CR4

1µf C4

270Ω R2

FROM TTY XMIT TB1-6 +

1µf C3

1N3604 CR3

74S04

TTY (SH3-C3)

1N3604 CR2

1N3604 CR1

R1 120Ω ½W

1µf C1

1µf C2

TB1-8 TO TTY RCV

TB1-9 TO TTY RCV

BFLG4 (SH2-B7)

-12V

68Ω ½W R22

TB1-5 TO TTY RD RLY

+5V

470Ω R10

75Ω ½W R9

BFLG1 (SH2-B7)

390Ω R11

2N5143 Q1

1N3604 CR6

.01µf C17

TB1-4 TO TTY RD RLY

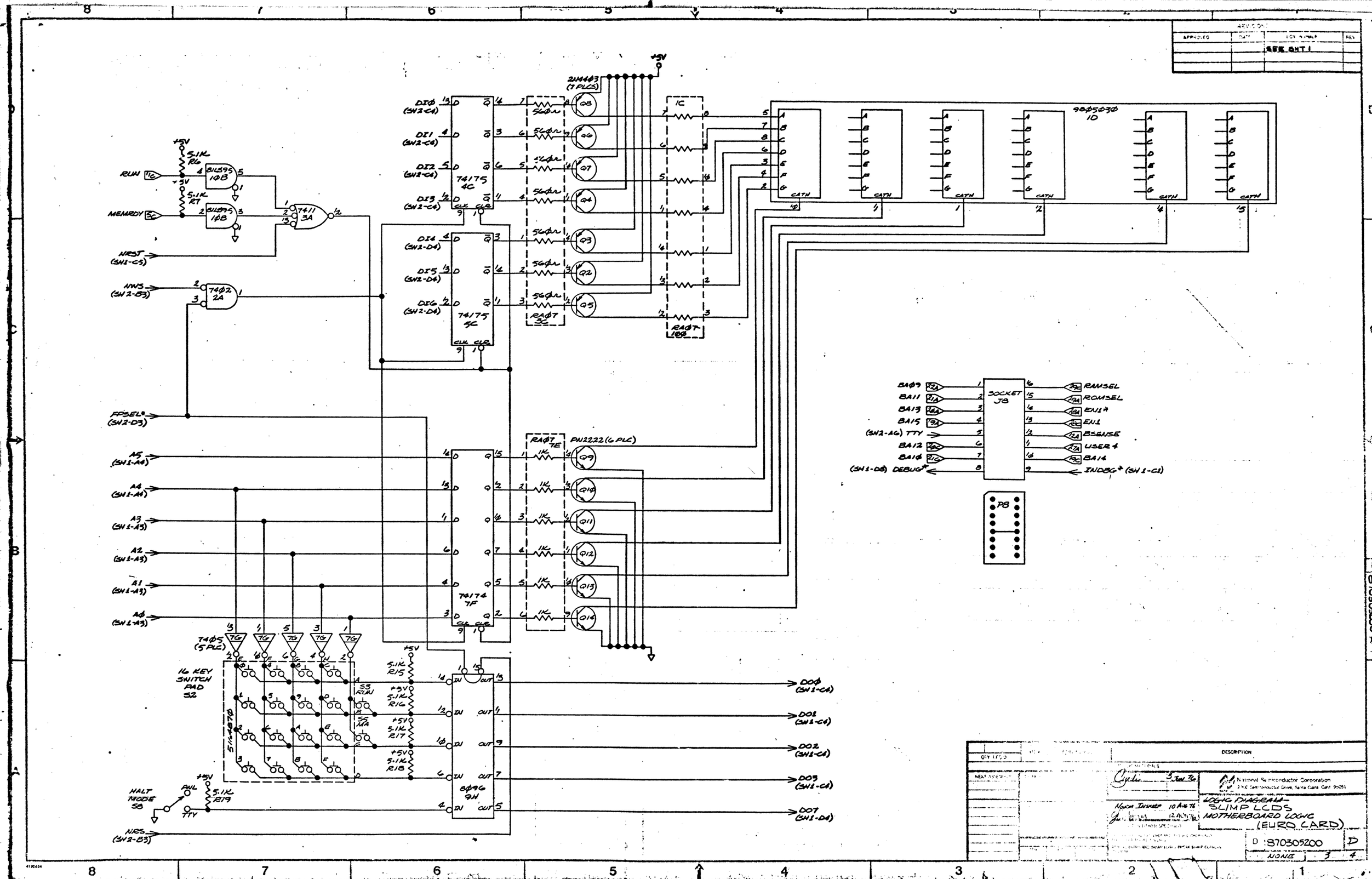
NOTE:
1. WHEN MM5246 2K X 8 ROM IS USED, ROM/PROM 8E - 8H ARE NOT USED ON THE BOARD.
2. A0 - A8 AND D00 - D07 ARE TIED TOGETHER RESPECTIVELY ON 8E, 8F, 8G, AND 8H.

QTY REQ'D	ITEM	PART NUMBER	DESCRIPTION
NEXT ASSEMBLY		MATERIALS	

Drawn	4 Jan 76	National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051
Approved	10 Aug 76	LOGIC DIAGRAM - SCMP LCDS MOTHERBOARD LOGIC (EURO CARD)
Released	12 Aug 76	

SIZE	DRAWING NO.	REV
D	8703052D0	D
NONE	2	4

8703052D0A



SEE SHT 1
RUN
MEMRDY
NRST (SH1-C5)
NWS (SH2-B3)
FPSEL* (SH2-D3)
A5 (SH1-A4)
A4 (SH1-A4)
A3 (SH1-A3)
A2 (SH1-A3)
A1 (SH1-A3)
A0 (SH1-A3)
HALT MODE S8
NRS (SH2-B3)
DI0 (SH2-C4)
DI1 (SH2-C4)
DI2 (SH2-C4)
DI3 (SH2-C4)
DI4 (SH2-D4)
DI5 (SH2-D4)
DI6 (SH2-D4)
74175 4C
74175 5C
74174 7F
2N4403 (7 PLCS)
RA07 3C
RA07 10D
RA07 7E
PN2222 (6 PLC)
9805030 1D
SOCKET J8
P8
BA09
BA11
BA13
BA15
(SH2-A6) TTY
BA12
BA10
(SH1-D8) DEBUG*
RAMSEL
ROMSEL
EN1*
EN1
BSENSE
USER 4
BA14
INDBG* (SH1-C1)
74105 (5 PLC)
16 KEY SWITCH PAD S2
8096 9H
DO0 (SH1-C4)
DO1 (SH1-C4)
DO2 (SH1-C4)
DO3 (SH1-C4)
DO7 (SH1-D4)
DESCRIPTION
National Semiconductor Corporation
LOGIC DIAGRAM-
SLIMP LCDS
MOTHERBOARD LOGIC
(EURO CARD)
D 870305200 D
NONE 3 4

REVISIONS			
APPROVED	DATE	D.N. NUMBER	REV
		SEE SHT 1	

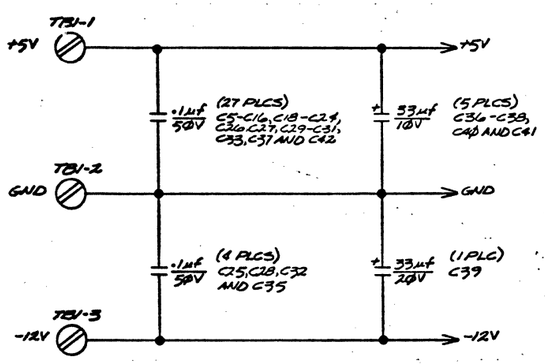
TRUTH TABLE OF ROM LOCATED AT 482Ø782

E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	1	0	0	0	0
0	0	0	1	0	0	0	1	1	0	0	0	0
0	0	0	1	1	0	0	0	0	1	1	0	1
0	0	1	0	0	0	0	1	1	0	0	0	1
0	0	1	0	1	0	0	1	1	0	0	1	0
0	0	1	1	0	0	0	1	1	0	0	1	1
0	0	1	1	1	0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1	1	0	0	0	0
0	1	0	0	1	0	0	0	0	1	1	0	0
0	1	0	1	0	0	0	1	1	0	0	0	1
0	1	0	1	1	0	0	1	1	0	1	0	0
0	1	1	0	0	0	0	1	1	0	1	0	1
0	1	1	0	1	0	0	1	1	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	0	1	1	0
1	0	0	0	1	0	0	1	1	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0	0	0
1	0	0	1	1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	1	1	1	1	0	0	0
1	0	1	0	1	0	0	1	1	1	0	0	0
1	0	1	1	0	0	0	1	1	0	1	1	1
1	0	1	1	1	0	0	1	1	0	0	0	1
1	1	0	0	0	0	0	0	0	1	1	0	0
1	1	0	0	1	0	0	1	1	0	0	1	1
1	1	0	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0	1	1
1	1	1	0	0	0	0	1	1	0	1	0	1
1	1	1	0	1	0	0	1	1	0	0	0	1
1	1	1	1	0	1	1	0	0	1	1	0	1
1	1	1	1	1	0	0	0	0	1	0	1	1

SC/MP EURO LCDS - MOTHERBOARD

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
1A	+5V	1C	+5V
2A	+15V	2C	-15V
3A	-12V	3C	-12V
4A	GND	4C	GND
5A	INIT*	5C	MEMRDY
6A	BUSREQ	6C	BAEN
7A	BD1	7C	BDØ
8A	BD3	8C	BD2
9A	BD5	9C	BD4
1ØA	BD7	1ØC	BD6
11A	ENCPU	11C	RUN
12A	BSENSE	12C	ASENSE
13A	BSOUT	13C	BSIN
14A	BFLG1	14C	BFLGØ
15A	MEMEN	15C	BFLG2
16A	GND	16C	GND
17A	READ	17C	DELAY
18A	HALT	18C	IFETCH
19A	BA15	19C	BA14
2ØA	BA13	2ØC	BA12
21A	BA11	21C	BAIØ
22A	BAØ9	22C	BAØ8
23A	BAØ7	23C	BAØ6
24A	BAØ5	24C	BAØ4
25A	BAØ3	25C	BAØ2
26A	BAØ1	26C	BAØØ
27A	USER 4	27C	USER 3
28A	ENI*	28C	ENI
29A	ROMSEL	29C	RAMSEL
3ØA	BADS*	3ØC	MEMSEL*
31A	BWDS*	31C	BRDS*
32A	GND	32C	GND

PIN CONNECTIONS, 5 PLACES, J1 THROUGH J5



CABLE CONNECTOR J6

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
2	MEMRDY	1	GND
4	BAEN	3	GND
6	BDØ	5	GND
8	BD2	7	GND
1Ø	BD4	9	GND
12	BD6	11	GND
14	RUN	13	GND
16	ASENSE	15	GND
18	BSIN	17	GND
2Ø	BFLGØ	19	GND
22	BFLG2	21	GND
24	READ	23	GND
26	HALT	25	GND
28	BA15	27	GND
3Ø	BA13	29	GND
32	BA11	31	GND
34	BAØ9	33	GND
36	BAØ7	35	GND
38	BAØ5	37	GND
4Ø	BAØ3	39	GND
42	BAØ1	41	GND
44	USER 4	43	GND
46		45	GND
48	BADS*	47	GND
5Ø	BWDS*	49	GND

CABLE CONNECTOR J7

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
2	INIT*	1	GND
4	BUSREQ	3	GND
6	BD1	5	GND
8	BD3	7	GND
1Ø	BD5	9	GND
12	BD7	11	GND
14	ENCPU	13	GND
16	BSENSE	15	GND
18	BSOUT	17	GND
2Ø	BFLG1	19	GND
22	MEMEN	21	GND
24	DELAY	23	GND
26	IFETCH	25	GND
28	BA14	27	GND
3Ø	BA12	29	GND
32	BAIØ	31	GND
34	BAØ8	33	GND
36	BAØ6	35	GND
38	BAØ4	37	GND
4Ø	BAØ2	39	GND
42	BAØØ	41	GND
44	USER 3	43	GND
46		45	GND
48	MEMSEL*	47	GND
5Ø	BRDS*	49	GND

QTY	DESCRIPTION

Sysdia 5 Jan 76

National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, Calif. 95051

Naomi Ishii 10 Aug 76

LOGIC DIAGRAM - SC/MP LCDS MOTHERBOARD LOGIC (EURO CARD)

870305200 D

NONE 4 4

870305200