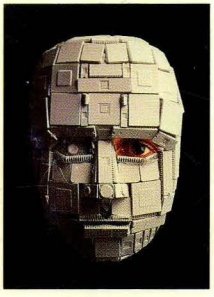
NCR



Digital ASIC Data Book

Creating value

NCR Microelectronic Products Division – Sales Locations

For literature on any NCR product or service, call the NCR hotline toll–free:
1 (800) 334–5454

NCR Microelectronic Products Division
Worldwide Sales Headquarters
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 453–0303

Division Plants

NCR Microelectronic Products Division
2001 Danfield Court
Ft. Collins, CO 80525
(303) 226–9500

PC Chipsets
Commercial ASIC Products
Customer Owned Tooling
Communication Products
Memory Products

NCR Microelectronic Products Division
1635 Aeroplaza Drive
Colorado Springs, CO 80916
(719) 596–5611

High Reliability ASIC
Military Products
Automotive Products
Logic Products
SCSI Products
Internal ASIC
Multichip Modules

North American Sales Offices

Northwest Sales
1731 Technology Drive, Suite 600
San Jose, CA 95110
(408) 441–1080

Southwest Sales
3300 Irvine Avenue, Suite 255
Newport Beach, CA 92660
(714) 474–7095

North Central Sales
8000 Townline Avenue, Suite 209
Bloomington, MN 55438
(612) 941–7075

South Central Sales
17304 Preston Road, Suite 635
Dallas, TX 75252
(214) 733–3594

Northeast Sales
500 West Cummings Park, Suite 4000
Woburn, MA 01801
(617) 933–0778

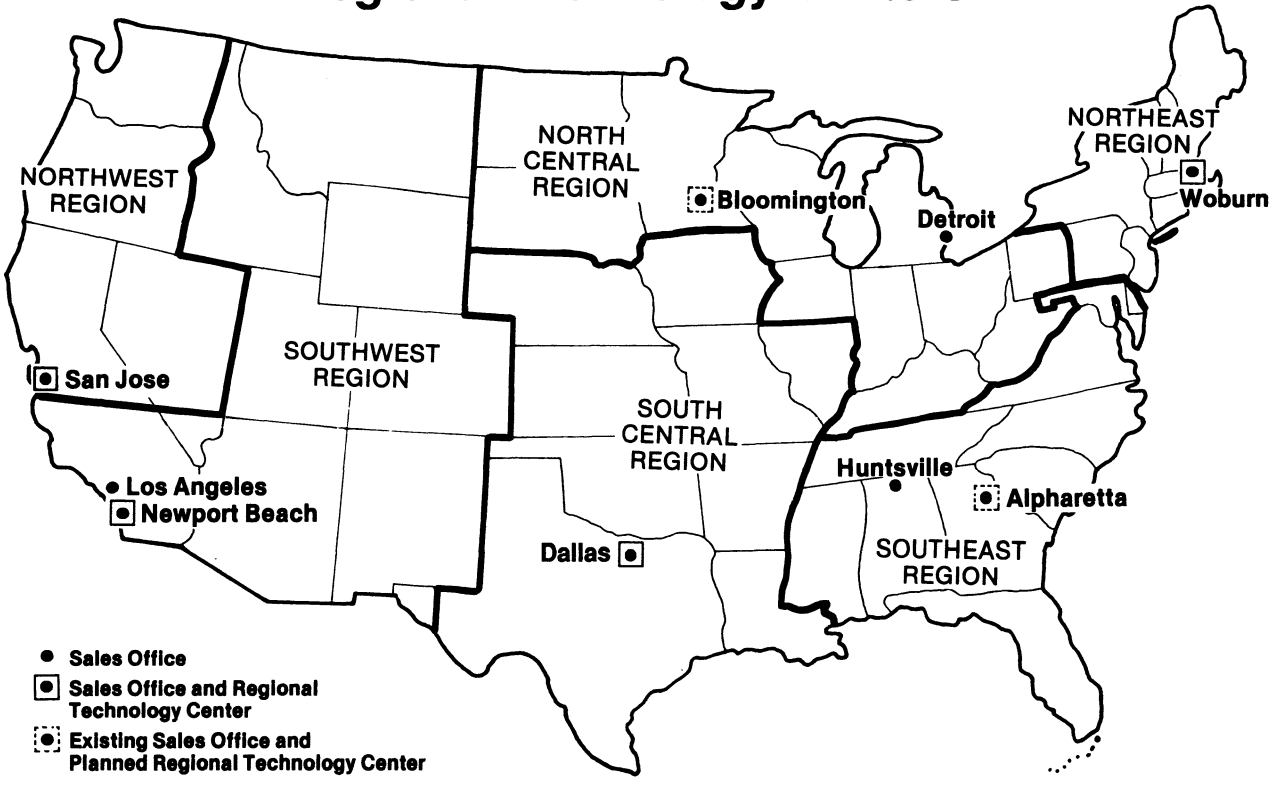
Southeast Sales
1051 Cambridge Square, Suite C
Alpharetta, GA 30201
(404) 740–9151

International Sales Offices

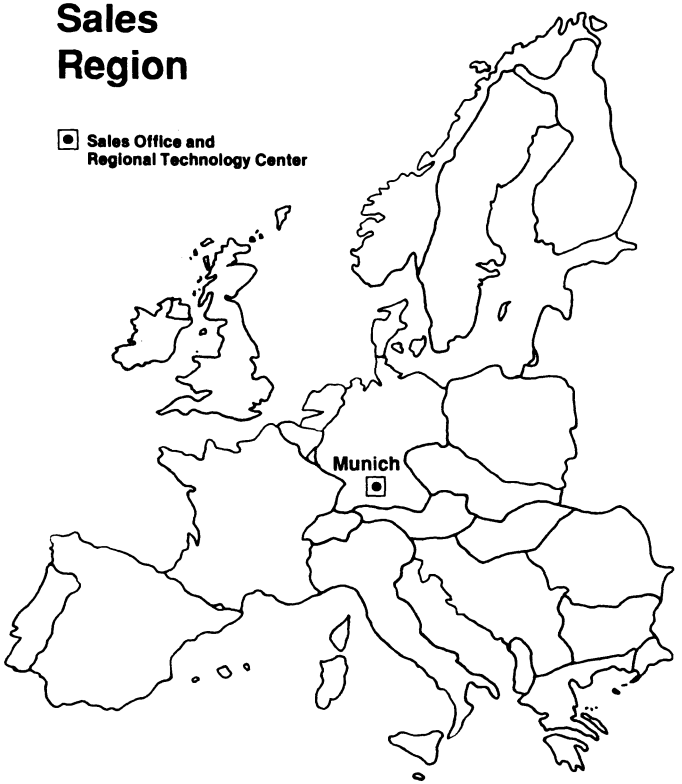
European Sales Headquarters
Westendstr. 193
8000 Munchen 21
Germany
49 89 57931 199

Asia/Pacific Sales Headquarters
35th Floor, Shun Tak Centre
200 Connaught Road
Central Hong Kong
852 859 6044 or 852 859 6046

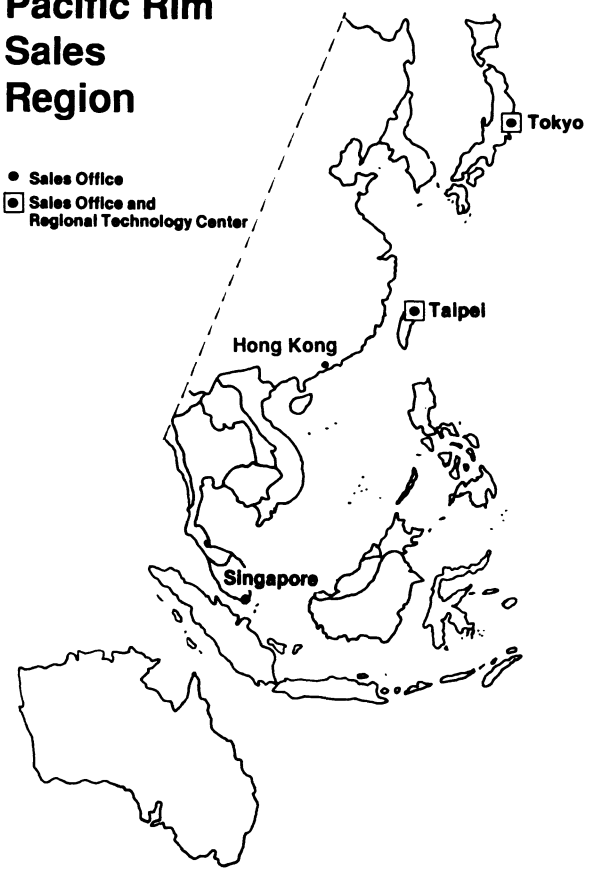
U.S. Sales Regions and Regional Technology Centers



European Sales Region



Pacific Rim Sales Region



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NCR General Information

NCR Microelectronic Products Division Overview

NCR Microelectronic Products is a division of NCR Corporation (Dayton, Ohio), a leader in the development, manufacturing, marketing, and support of business information processing systems for worldwide markets. The NCR Microelectronic Products Division is one of the largest developers and manufacturers of cell-based, mixed-signal Application-Specific Integrated Circuits (ASICs), all of which are designed using NCR's industry-leading, knowledge-based design system. In addition to cell-based libraries, NCR also markets sea-of-gates gate arrays with up to 169,000 total gates. NCR has also built on its expertise in ASIC design and development to offer a wide range of standard integrated circuit products for a variety of applications.

ASIC products are used in commercial, industrial, automotive and military applications and are supported by a broad offering of ASIC design tools that embody and apply hundreds of man-years of knowledge and successful design practices. This on-line expertise can flag potential design problems and alert the designer to opportunities for higher reliability, manufacturability, and testability in ASIC design.

The division is one of the industry's earliest and largest suppliers of Small Computer System Interface (SCSI) chips. NCR also offers a wide range of graphic, communication (including ARCNet™ and Ethernet LAN), memory, microprocessor chips, and a recently announced family of 386SX/DX chipsets and chips for the PC and workstation markets.

Division Business Units

NCR Microelectronic Products Division is organized into seven business units, each with its own management, marketing, and engineering team. The business units also work together to accomplish strategic programs based on division-wide goals and objectives.

Each business unit is supported by an on-site fabrication facility at its headquarters in either Fort Collins or Colorado Springs, and by "second-source" capabilities at the neighboring plant.

Fort Collins Business Units

- Commercial ASICs -
  Cell library development/support for all NCR ASICs; both cell-based and gate array products.
  Design training for all NCR ASIC activities.
  Design/manufacturing support for commercial ASIC applications.
  Technical software support/training for NCR ASIC business units.
- Communications -
  Design/manufacturing/marketing of integrated circuits for LAN and other communications applications.
- Customer-Owned Tooling (COT) -
  Services for those who need or must supplement foundry capabilities.

Colorado Springs Business Units

- Logic Products – Design/manufacturing/marketing of Small Computer System Interface (SCSI) and other peripheral support products, as well as a graphics product line.
- NCR Internal Marketing – Marketing of microelectronic products to other NCR Corporation divisions.
- Multichip Modules – Development, assembly and marketing of multichip modules to the merchant market.

Regional Technology Centers

The NCR Microelectronic Products Division Worldwide Sales Headquarters in San Jose, California, is the home of the first in a networked series of eight company–owned Regional Technology Centers (RTCs). Other RTCs which opened in 1990 include Munich, Orange County, California, and Boston, Massachusetts. Taiwan and Dallas, Texas, opened in the first quarter of 1991. Other planned openings for 1991 include Atlanta, Georgia and Bloomington, Minnesota. These RTCs provide extensive technical support and design resources for NCR customers who are developing ASICs and ASSPs and are equipped with a wide range of hardware and software tools.

NCR also services customers who need turn–key design through an existing network of ten worldwide third–party Value–added Design Centers (VADCs). The division's sales organization includes six Regional Sales Managers in the United States (who manage more than 50 independent sales representatives), plus European and Asia Pacific Sales Directors and sales representatives.

NCR Microelectronic Products Division
A History of Service, Quality, and Support

Division History

NCR's active participation in the microelectronics industry began in 1971 with the design and manufacture of advanced integrated circuits for NCR's internal use. Its first microelectronics plant was opened in Miamisburg, Ohio in the same year. Through these activities, NCR was one of the earliest pioneers in cell-based ASIC research and marketing.

In 1981, NCR Microelectronic Products Division began to sell products to the merchant market. Today, the division is among the most profitable and fastest growing units in the corporation. More than 85 percent of the division's revenue is contributed by external non-captive customers. The division's focus is on CMOS technology, one of the fastest growing semiconductor industry segments. CMOS offers high component density with low power dissipation -- advantages which NCR believes will continue to challenge bipolar technology as feature sizes continue to fall.

Three years after entering the merchant market, NCR Microelectronic Products Division was independently recognized as the leading standard-cell ASIC supplier worldwide. The division has since expanded its ASIC offerings and has developed a broad range of key Application Specific Standard Products (ASSPs) that act as building blocks for today's high-performance personal computers and workstations. NCR believes it offers a competitive edge over other ASIC suppliers because of its unique knowledge-based ASIC design environment and broad expertise in system architecture gained over many years of developing proprietary semiconductor products for NCR general-purpose computer systems and other data processing products and services.

Milestone Events

1963 -- NCR establishes its first microelectronics laboratory.

1966 -- The NCR Microelectronic Products laboratory is expanded to design and manufacture prototype circuits for a number of NCR business machines.

1968 -- NCR produces its first MOS standard cell circuits. NCR is credited with inventing standard cells.

1970 -- NCR incorporates a family of MOS-based circuits into its computers and business machines.

1971 -- NCR completes its first microelectronics plant in Miamisburg, Ohio, and forms a separate unit to design and manufacture advanced ICs for NCR's internal use. Active production ceases here in 1988.

1975 -- NCR expands its microelectronics operation with the addition of a second IC fabrication facility in Colorado Springs, Colorado.

1979 -- NCR adds a third IC fabrication facility in Fort Collins, Colorado.

1981 -- NCR's Microelectronic Products Division enters the merchant market.

1981 -- NCR ships first ASIC products to a major automotive manufacturer.

1982 -- The Colorado Springs IC fabrication facility is replaced with a new, 100,000-square-foot, flagship facility.

1983 -- NCR introduces the industry's first SCSI protocol controller, for which it co-wrote the ANSI standard development document in 1982.

1984 -- NCR receives independent recognition as the leading supplier of standard-cell ICs, the fastest-growing ASIC market segment.

1987 -- NCR introduces the first knowledge-based ASIC design system to aid designers in flagging potential errors or design optimization opportunities. Design Advisor™ becomes part of NCR's design offering, which was expanded through 1987 and 1988.

1988 -- NCR forms a Communications Business Unit to provide ASIC-based standard ICs for LAN, and other communications applications.

1990 -- NCR introduces the VS700 submicron ASIC cell library and VGX700 series gate arrays (.7-micron L-effective, .95-micron drawn).

1990 -- NCR adds industry's first analog submicron cells to the VS700 ASIC cell library.

1990 -- NCR announces support for Verilog™ Simulation tools, Synopsys™ Logic Synthesis tools and IKOS™ ASIC Simulation System.

1990 -- NCR announces a worldwide network of Regional Technology Centers (RTCs), providing extensive technical support and design resources for ASICs and ASSPs.

1991 -- NCR announces the addition of four large application-specific functional cores for PC and workstation peripheral I/O integration; the 85C30-, 82077AA-, 53C90A-, and 53C94-compatible cores.

NCR ASIC Strategy and Goals

NCR's foremost ASIC strategy is to put the design process and control into the hands of our customers and provide them with a wide range of functions to serve their integration needs. NCR has devoted extensive R&D resources to CAD tool development as well as considerable time and thought to workstation vendor agreements, independent design centers, customer training, field support, and an ongoing commitment to customer service and satisfaction.

Standard Cell Leadership

By following this strategy, NCR became the industry standard cell leader in 1984, three years after entering the merchant market. NCR strives to provide the best product and service, and the strongest commitment to customer needs.

NCR's strategic efforts focus on enabling our customers to expedite their product development schedules, and offering products with more features, smaller size, higher reliability, and lower production costs. A rich offering of standard cell and gate array products to provide the optimum integration solution is a key component in this strategy. Comprehensive digital and analog libraries including memory and core processors coupled with high-level market-specific functions such as SCSI cores save ASIC design time, and help assure that the ASIC works the first time in the system.

Mixed-signal Cell-based Design

NCR was one of the first ASIC vendors to offer mixed-signal design and is an industry leader in the production of mixed analog-digital ASIC devices. NCR has tackled the two most pressing and challenging needs of mixed-signal ASIC customers with the introduction of true mixed-signal simulation and thorough, precise, at-speed, mixed-signal test. With DesignSim™ A&D, concurrent analog and digital design and mixed-mode simulation is possible, with the resulting waveforms displayed on the same computer screen in the same time base. ASICs or entire systems, with any combination of feedback, can be simulated concurrently for the most thorough design and functionality analysis possible.

Design System

NCR has made it possible to design with either standard cells or gate arrays using the same design system and tools. You can enter the schematic and then explore which library and geometry best meets system speed and cost requirements. NCR's DesignTest™ tool kit is designed to make it faster and easier to generate a production test program. DesignSim ATL automates the process by providing a high level simulation language to speed simulation vector generation. Expected output information can be added to the simulation vectors automatically by "learning" output states from simulation runs. These vectors can then be used for subsequent pass/fail simulation tests (for example, different voltages, temperatures, process, etc.). The simulation vectors will convert to test vectors automatically.

With the promise of tools, functions, and service for faster product development cycles with complete design process control, NCR's ASIC strategy maintains a constant focus on what designers need to roll out the best products for their market in the shortest possible time.

NCR maintains strategic, long-term alliances to provide our customers with true ASIC alternate sourcing. Identical design automation interfaces and process technology allow second sourcing at every phase of design, development and manufacturing. These alliances cover CMOS gate arrays, cell libraries, CAD tools, and future-generation ASIC products.

NCR is a member of the SEMATECH manufacturing research and development consortium. This membership provides NCR with access to the advanced semiconductor manufacturing processes, materials, equipment, and techniques being developed by SEMATECH. NCR is a firm believer in the benefits of consortium-based research and development work and has been extremely successful in transferring such technology to the commercial market. NCR's Design Advisor (an artificial intelligence-based ASIC design tool), the first commercial product to emerge from the Microelectronics and Computer Technology Corporation (MCC) consortium, is an example of the success NCR has had in productizing consortium-developed technology.

NCR ASIC Products Summary

Overview

NCR offers a full spectrum of ASIC products including extensive cell and gate array libraries in submicron and larger geometries. These libraries offer designers the convenience of a "one-stop ASIC shop." All products are available in commercial, industrial, automotive, and military temperature ranges.

NCR CMOS Standard Cell Libraries

The VS700 (.7 micron L-effective, .95 micron drawn) is a CMOS double-level-metalization (DLM) processed library. This submicron offering provides a 40 percent performance improvement and 40 percent density increase over VS1500F while preserving a design migration path that eliminates the need for schematic entry to achieve smaller geometries.

The VS1500F (1.1 micron L-effective, 1.5 micron drawn) is also a CMOS double-level-metalization (DLM) processed library. This offering is rich in functionality and capabilities, and includes a wide range of analog cells, supercells, user-configured compiled cells, microprocessor cores, memory functions, and other popular and specialized functional blocks.

All NCR libraries are rich in functionality and capabilities. In fact, one of the key areas which sets NCR apart from other standard cell suppliers is the functional richness of our libraries. It's this richness that allows NCR customers to integrate more of their system on ASIC devices. Cells range in complexity from simple buffers to microprocessor cores and EEPROMs.

TYPICAL CELL DELAYS (nsec)		
Cell Drawn Effective	.95µ .7µ	1.5µ 1.1µ
Small inverter	.34	0.6
2-input NAND	.35	0.7
8-input AND	.92	1.7
2-input NOR	.5	0.9
8-input OR	.76	2.5
D Flip-flop with reset (CLK-Q)	.59	1.6

Delay values are in nanoseconds at 25° C and V_{DD} 5.0 volts and for fan-out of two typical loads.

NCR CMOS Supercell Library

Supercells are function blocks which were once available only as discrete ICs. But NCR has taken these complex functions, such as microprocessor cores, peripheral ICs, modular RAM, SCSI, CRTC, ROM, and EEPROM, and added them to our supercell library. This capability provides a total system-on-a-chip level of integration.

NCR's Supercell Library is Growing

NCR features two different types of supercells in its rapidly growing library: "hard" and "soft". Hard supercells are designed from the ground up, and therefore take up less space and improve device performance.

Some areas of standard cell design require greater flexibility than hard supercells can provide. To address this need, NCR's library offers high-level function macros which are soft supercells. These cells are built from several lower complexity function blocks and are stored within the CAD system. These cells can be modified by adding or deleting functions and changing layout configurations.

Supercell Computer Aided Design: ViGen

NCR offers a complete solution for integrating high level functions, such as memory, on the chip. NCR's compilers are designer-configurable via menu entries on industry-standard workstations and popular CAE platforms. You can meet the specific needs of your application without NCR design involvement. You can perform what-if analysis and get immediate feedback. The compilers automatically generate full schematic symbols and models, and the resulting functions can easily be combined with any other NCR library components such as other compiled functions, analog cells, or digital cells.

High-level Function Macros

NCR supplies high-level function macros, including SCSI, floppy disk controllers, ethernet controllers, NCR 8200 series, and other macros for PCs, workstations, and peripheral application ASICs which are 100% compatible with industry standards. Exact reproduction of standard part functions, including the idiosyncrasies which are not documented in standard part data sheets, is a fundamental requirement. These macros save you the considerable time and cost of reverse-engineering these functions.

All macros are checked with NCR's NetChecker™ to assure good operating margins and high manufacturing yields. Operation is compared to the standard part equivalent using hardware modeling simulation techniques. Kit parts are fabricated, plugged into actual systems, and tested to assure they function identically to the standard part.

NCR CMOS Gate Arrays

NCR offers gate array products in the same leading edge technologies used for cell-based ASICs. Arrays implement a design by customizing only the interconnection layers. They are the ideal choice for logic design applications where fast turn time, high gate density, and high performance are important. Gate delays for both cell-based and gate array ASICs are approximately equivalent in the same process technology. The same high-level function macros available for the cell-based ASICs are also available in the gate arrays.

The gate arrays offer high gate and pin densities, with a wide variety of gate/pin counts available. They employ the "sea-of-gates" architecture enhanced to exploit the advantages of the latest router technology. Schematic symbols are identical to the cell-based offerings, so designs can be rapidly converted to cell-based or migrated to the latest technology without re-entering the schematic. All tools that can be used for cell library designs can be used for gate array designs.

The VGX700 (.7 micron L-effective, .95 micron drawn) is a CMOS, double-level-metalization (DLM) processed gate array. Usable gate counts range from 5,000 to over 73,000 with pin counts from 84 to 304.

The VGX1500 (1.1 micron L-effective, 1.5 micron drawn) is also a CMOS, double-level-metalization (DLM) processed gate array. This offering provides usable gate counts from 500 to over 24,000 gates, and pin counts from 28 to 240.

Function Summary

SSI Functions

- Buffers and inverters; output drive and tristate options.
- NAND and NOR; available with 2, 3, and 4 inputs.
- AND and OR; up to 8 inputs.
- EXOR, AOI and OAI "combinational" logic cells; for denser and faster devices.
- Delay cells.
- Two-phase clock drivers.

Flip-Flops/Latches

- Cross-coupled latches; both NOR and NAND type.
- Level-sensitive transparent latches; with or without reset and clock drivers.
- Edge-triggered D flip-flops; with or without reset, set and reset, or clock drivers.
- Edge-triggered JK flip-flops; with or without set, reset and clock driver.
- Non-volatile latch.

MSI Functions

- Generated user-configurable counters, timers, multiplexers, and shift registers.
- 74xx functions.
- Single-bit cascadable shift register with serial or parallel in and serial out; with or without clock driver.
- Single-bit cascadable, loadable, up/down counter with Reset and Enable, carry in, and carry out.
- Full and Half Adders.

Input/Output Pads and Buffers

- Options to give optimal size in pad-limited designs.
- Levels are directly TTL, LSTTL, and CMOS compatible.
- Input cells; choice of standard TTL or variety of Schmitt trigger level.
- Output cells; variety of drive options, open drain, pullup options, up to 48 mA drive.
- Tristate; combination of I/O options.
- Pullups and pulldowns.

Analog Cell Library

- Op Amps
- Comparators
- Analog Switches
- BANDGAP Voltage Reference
- Current Reference
- Crystal Oscillators
- "555" Timer
- Resistors and Capacitors
- A/D Converters
- D/A Converters
- VCO
- Frequency/Clock Synthesizer (3Q91)

Supercell Library

- Compiled ROM
- Compiled Low-power RAM
- Compiled Fast Static RAM
- Compiled Dual-Port RAM
- Compiled FIFO
- Compiled ALU
- Compiled Multiplier-Accumulator (MAC)
- NCR2901
- NCR2910
- Modular EEPROM
- Counter/Timer
- 65C02 Microprocessor
- 68C05 Microprocessor
- SCSI Controllers
- CRT Controller

High Level Function Macros

- NCR146818A - Real Time Clock
- NCR16C450 - UART
- NCR16C550 - UART
- NCR82C284 - Clock Generator and Ready Interface
- NCR82C288 - Bus Controller
- NCR82C37A - DMA Controller
- NCR82C54 - Programmable Interval Timer
- NCR82C59A - Programmable Interrupt Controller
- NCR82C84A - Clock Generator/Driver
- NCR82C88 - Bus Controller
- NCR765 - Floppy Disk Controller
- 82077AA-compatible Floppy Disk Controller
- Digital Data Separator
- 85C30-compatible Serial Communications Controller
- Ethernet-compatible Controller
- SCSI-compatible Cores (53C90A, 53C94)
- JTAG TAP Controller

ASIC Development Cycle

The NCR Semicustom Design flow consists of fourteen steps, as shown in Figure 1–1. The customer or design center performs some steps, and NCR performs others. Here is a summary of the flow.

- Design the circuit, using one of the NCR logic libraries.
- Capture the design schematic on an engineering workstation.
- Simulate the design's functional logic and analyze its timing.
- Lay out the design for manufacturing.
- Simulate the postlayout design.
- Prepare test data for use after manufacturing.

The Semicustom Design flow steps are as follows.

1. Begin by designing the circuit. You will save time in the overall design process if you consider basic testability issues when you design the circuit.
2. Capture the design at the engineering workstation, using the workstation schematic editor. Choose one of the NCR logic cell libraries.
3. Configure compiled cells on-line, while in the workstation schematic editor.
4. Generate the input stimulus waveforms for the logic simulations. It is best to consider tester requirements in the initial simulation input rather than later modifying the simulation input to meet test program requirements. Not all logic simulations have to meet tester requirements; only those to be used as the basis for the test program. You may need to perform additional simulations to test specific portions of your circuit design. The optional tool DesignSim ATL can be used to expedite this step and also automate steps 7 and 8.
5. Perform prelayout timing analysis and simulation.
   a. Perform the functional simulation of the circuit design, using the workstation logic simulator and your input stimulus waveforms. The functional simulation uses unit delays for estimated propagation delays.
   b. Perform optional static timing analysis. This first use of the static timing analysis tool reveals set-up and hold-time violations, race conditions, critical paths, etc. before you perform lengthy pattern driven analysis.
6. Perform the prelayout estimated real-time simulations. Two simulations are required: one using best-case estimated propagations delays and one using worst-case delays.
7. Following successful simulations, generate simulation output files, using the workstation logic simulator. Create two simulation output files: one for the best-case simulation and one for the worst-case simulation.
8. Validate the simulation output files using DesignTest programs. These programs help to validate the usability of the simulation output files for test program generation by the NCR test engineers.
9. Release design to NCR.
   a. Determine the critical paths in the circuit design, calculate design statistics, and list pinout information.
   b. Release the design to NCR for physical layout and interconnect analysis. The design review is conducted now.

10. Place and route.
    a. NCR performs several actions now. We run the automatic cell placement and routing software to generate the physical layout. Then we analyze interconnect resistances and capacitances. Finally, we extract interconnect lengths to calculate real best-case and worst-case propagation delays and send the new delay files to you, so that you can perform postlayout simulations.
    b. NCR can run probabilistic, deterministic, and statistical fault grading on the test patterns. Refer to the fault grading portion of the CAD tool section of the data book for a discussion of fault grading technologies.
11. Postlayout timing analysis and simulation.
    a. Run static timing analysis after layout to verify that all critical path timings are met. This is in addition to verification by pattern-driven simulation.
    b. Perform two postlayout real-time simulations using the actual layout interconnect parameters: one using best-case real propagation delays and one using worst-case delays.
12. Following successful simulations, generate postlayout simulation output files using the workstation logic simulator. Again you must create two simulation output files: one for the best-case simulation and one for the worst-case simulation.
13. Rerun the DesignTest programs to validate the postlayout simulation files. The programs help to validate the usability of the postlayout simulation files for test program generation.
14. Send the postlayout simulation files and the output from the DesignTest programs to NCR. The NCR test engineers now generate the test program from your postlayout simulation files. They extract the test patterns from the simulation files, convert the test patterns to the format required by the automated tester, and then generate the actual test program to be used to test the prototype chips.

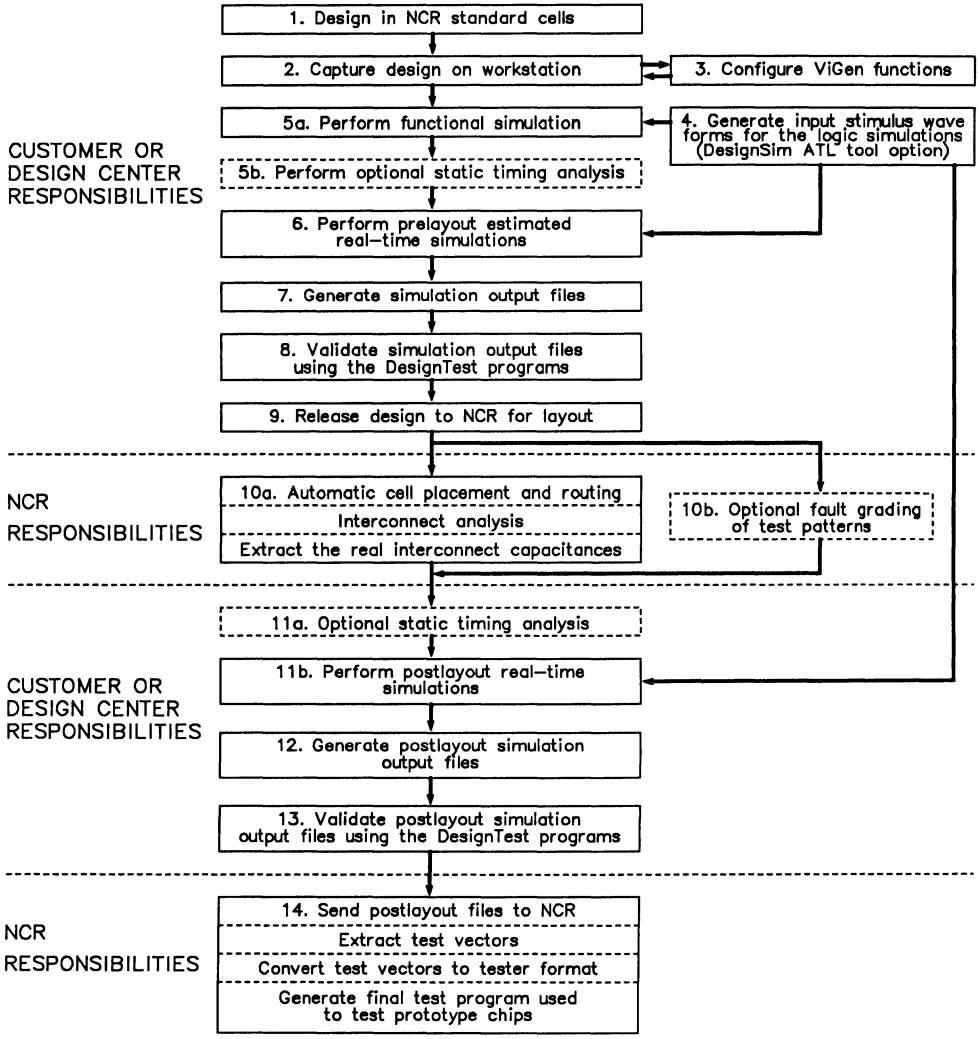


Figure 1–1 NCR semicustom design flow

Requesting a Quote from NCR

For NCR to calculate the amount of silicon that a design will require (die size), you must provide several pieces of information about your design. NCR will use this information to run a die sizing program and prepare a budgetary quote.

Types of Quotes

There are two types of quotes to consider, budgetary and final. A budgetary quote is simply an estimate of the die size and associated costs of producing an Application Specific Integrated Circuit (ASIC) including piece-part cost of production units along with Non-Recurring Engineering (NRE) costs and turnaround times for prototypes and production units. This quote can be used to see if an ASIC design (standard cell or gate array) is feasible. The pricing included in a budgetary quote may change.

The pricing included in a final quote is based upon the actual die size after the physical design is complete (excluding design changes).

Information Needed for a Quote

The data NCR requires to prepare a quote is described below:

- **Estimated digital gate count** – If the quote is budgetary, a gate count will suffice (a 2-input NAND = 1 gate); however, a complete schematic or cell count provides a more accurate die size estimate.
- **Special functions** – This includes analog circuits, memories, and macrocells. Include the specifications for each of these features. Designs which require such functions will be handled on a case by case basis.
- **Package preference** – For any given design, there may be certain packages that are preferred over others. NCR offers a wide variety of package and pinout options. The size of the die and the pinout, however, may restrict the type of package that can be used.
- **Pinout** – The number and type of all input, output, and bidirectional pads needed by a design may influence the size of the die. You should create a list describing all inputs and outputs and pad placement, if fixed. This list should include the type (Schmitt trigger, pullup, inverting, open drain, tristate, etc.) of all input, output, and bidirectional pads. In addition, include the drive capability specifications in milliamps of all output and bidirectional pads. NCR offers output drive capabilities ranging from 2 mA to 48 mA.
- **Supply voltage** – The voltage range over which the design is expected to operate.
- **Maximum frequency** – The maximum frequency at which the design is expected to operate and the proportion of the design operating at that frequency.
- **Temperature range** – The temperature range over which the design is expected to operate. At present, NCR offers standard commercial, industrial, and extended temperature ranges.
- **Expected annual usage** – The volume purchased affects the price.

NCR Semicustom Design Course

Introduction

The Semicustom Design Course is a multi-track, once a month, regularly scheduled course that is taught by Application Engineers. These instructors have an in-depth knowledge of both the hardware and software tools used with NCR's design methodology on supported workstations. We offer a stimulating educational environment where technical professionals can learn about our software tools in a hands-on environment.

What is presented here is a synopsis of what is explained in much more detail in the *NCR Semicustom Design Course Catalog*. This catalog is available by calling the NCR Fort Collins Microelectronic Products Division marketing number (303) 226-9500 and requesting that one be sent to you.

Course Catalog

The Course Catalog contains information on course enrollment (tuition, cancellation and rescheduling policies, enrollment form, etc.), detailed track and module descriptions, and a section on travel information such as lodging (phone numbers and approximate prices) and available transportation. Included in the front pocket is a Fort Collins, Colorado map showing the location of NCR and surrounding lodging accommodations.

Course Overview

This intensive, four-day introductory course familiarizes the design engineer with NCR design methodology. This includes several productivity enhancement tools such as Worksheet, DesignSim ATL, and NetChecker. Both standard cell and gate array technologies are discussed. About 50% of the class time is devoted to "hands-on" workstation experience using the software tools.

Prerequisites

In the Semicustom Design Course you learn how to use software tools that are part of NCR's semicustom IC design methodology. It does NOT provide an introduction to the workstation nor instruction on how to use the simulator. Therefore, you must be familiar with workstation-specific schematic capture and simulation techniques.

Tracks

Within the framework of the Semicustom Design Course, we offer a number of workstation/software dependent tracks. Each track consists of a number of generic and workstation dependent modules. Figure 1-2 shows a pictorial of the various tracks with their associated modules.

The tracks offered are:

- Mentor Graphics on Apollo
- Daisy on Sun (i386)
- DesignSim D (CADAT™) on Sun (3, 4)
- DesignEdit (Cadence) and DesignSim D (CADAT) on Sun (3, 4)

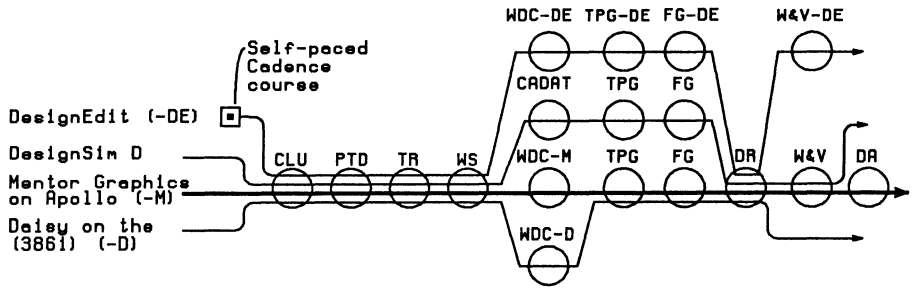


Figure 1-2 Track map

Curriculum

The curriculum consists of a number of modules in which the design process is described. Some modules such as the Cell Library and Usage (CLU) and Tester Restrictions (TR) are generic in nature and contain basic information not specifically related to the design flow. Other modules, such as Workstation Design Capture (WDC) and Test Program verification (TPG VERIF) are workstation specific.

Productivity enhancement is the theme of Worksheet (WS) and the module that discusses the Wisil compiler and Verify (W&V).

Each day comprises a mixture of lecture, workbook exercises, and "hands-on" workstation lab time. You gain workstation experience by using the tools covered in the lecture and by doing specific workbook design examples that permit you to enter a design, simulate it, and create a test program while following the NCR Design Methodology.

The course modules are as follows:

- Cell Library and Usage (CLU)
  This module includes general and specific cell usage information on NCR's libraries: cell naming conventions, data sheet explanations, and methods of doing timing calculations.
- Planning The Design (PTD)
  This short module outlines the design philosophy and requirements that help to ensure a first pass design success.
- Tester Restrictions (TR)
  This module explains terminology and timing limitations on how a device may be tested using Sentry and Trillium™ testers.
- Worksheet (WS)
  This module discusses the database to which you supply test and signal information. It also contains built-in tester knowledge for "compatibility checking".
- WISIL (W&V)
  This module explains the "C-like" test language and unique commands which may be used to generate test vectors and compare them with the expected values.

- Workstation Design Capture (WDC)
  This module discusses the design methodology of schematic capture, functional simulation, timing analysis and estimated real-time simulation as it relates to a specific workstation.
- Test Program verification (TPG verif)
  This module discusses in detail the verification aspect of the design flow. Four tools are covered: Verify, ViPac2, ViComp, and ViStrobe.
- Fault Grading (FG)
  This overview module explains the methods, benefits, and algorithms involved in measuring a device's test qualities.
- Design Review (DR)
  This short module discusses what information and data are required for an NCR design review. It also identifies the personnel who will be in attendance and provide an overview of what to expect in the design review meeting held at the Fort Collins facility.

NCR Site Training

The four day Semicustom Design Course is held at least once a month at the Fort Collins training facility. It begins Tuesday at 8:00 a.m. and runs until about 4:30 p.m.. On the last day the class is officially over by 3:00 p.m. to allow students time to catch a 6:00 p.m. flight out of Denver–Stapleton.

To achieve the optimum 2:1 student to workstation ratio, class size per track is limited to eight students. Because class size is restricted, we recommend enrolling at least four weeks in advance to secure the dates you desire and to ensure adequate lodging.

Customer Site Training

In addition to our regularly scheduled training program, we offer training at your site. If five or more of your technical professionals plan to attend classes at the same time, scheduling training at your site may be more cost effective. We do our best to schedule training that satisfies your needs. To obtain additional information on customer site training, contact your Field Application Engineer, Field Sales representative, or your Product Marketing Engineer.

Quality at NCR Microelectronic Products Division

General Quality Principles

Philosophy

Quality is, and should be, a basic customer expectation. It is the foundation on which we build customer satisfaction, profitability, and growth. Quality is key to our customers' success, which in turn, drives our own.

Our quality goal is zero defects. We believe that to approach this goal, certain principles must be embraced within our plant and sales force. These principles are:

- The quality focus must be on prevention, not appraisal.
- Processes must be continuously improved.
- Quality is everyone's job, not just the Quality Department's.

Organization

NCR is organized to give autonomy to the Quality Organization, while integrating it within the plant to permit direct involvement with other departments. This is accomplished in the plant by having Quality Management report to the General Manager at the same level as the business and manufacturing organizations. In addition, the Quality Organization is supported by an indirect link to the NCR Corporate Vice President of Quality.

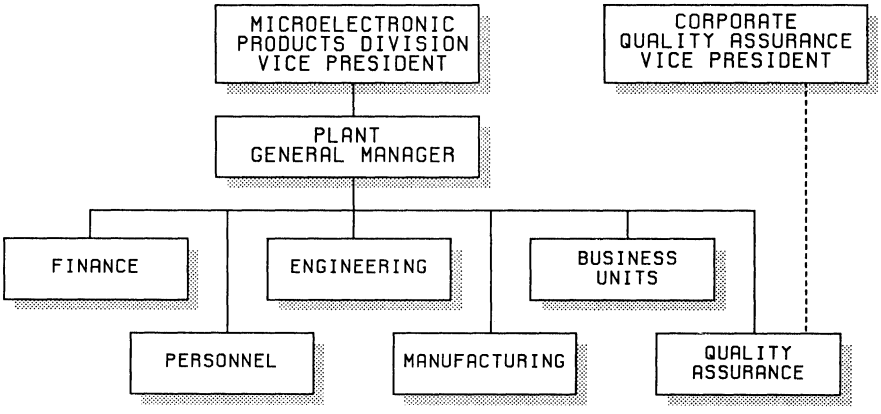


Figure 1–3 NCR Microelectronic Products quality organization

Total Quality Assurance

Quality is integrated throughout the entire process of designing and manufacturing products. These key areas are described below.

Design Quality

Product quality begins up-front, before volume manufacturing begins. Design quality is achieved through the use of NCR's high-quality cell library. Each cell family in the library is computer simulated for functionality and performance and then verified by characterization in silicon. This extensive verification and fine-tuning process provides the designer with maximum confidence that ASIC devices will meet objective specifications the first time.

Thorough measures are used in the design and layout of inputs, outputs, and I/Os to ensure the highest level of protection against electrostatic discharge and latch-up. These extra precautions have paid off for both NCR and its customers, typically producing designs with greater than 5 KV of human body input protection, 1 KV of charge body (machine) input protection, and 200 mA of latch-up protection.

The ASIC design flow at NCR is a fine-tuned process in itself. Through the use of travelers, checklists, customer design reviews, and the most powerful ASIC design tool set in the industry, NCR design centers assure that the design is accomplished accurately, promptly, and to customer requirements. These same tools, processes, and standards are used when designing our family of standard products as well.

Reliability of the cell library elements, manufacturing processes, and manufacturing materials are also verified up-front. The extensive reliability test matrices for initial qualification are shown below.

	Program				
Test	**Process**	**Design**	**Plastic package/ Assembly house**	**Ceramic package/ Assembly house**	**Military Qualification**
HTOL	X	X			X
LTOL	X				
HTSL			X		
85/85	X		X		
Autoclave	X		X		
Temperature Cycle	X	X	X	X	X
Thermal Shock			X	X	X
ESD	X	X			X
Latch-up	X	X			X
SEM	X				
Mechanical Shock					X
Constant Acceleration					X
Solderability			X	X	X
Marking Permanence			X	X	X
Lead Fatigue			X	X	X
Die Shear			X	X	X
Bond Strength			X	X	X
Fine/Gross Leak				X	X
X-ray			X		
Vibration					X
Physical Dimensions			X	X	X
Internal Visual				X	X
External Visual			X	X	X
Internal Water					X
Moisture Resist					X
Salt Atmosphere					X
Adhesion/Leads					X
Lid Torque					X
Vapor Phase	X		X		

Qualification matrix

Manufacturing Quality

Raw Materials

High quality manufacturing begins with high quality materials. Process chemicals, gases, targets, photomasks, and silicon wafers are subject to rigorous programs of Supplier Quality Management.

While we inspect some raw materials, it is more effective to work with our suppliers to assure they deliver only defect-free products. This eliminates the need for redundant incoming inspection at NCR. Our Supplier Quality Program is designed to accomplish this goal. Through detailed supplier site audits, correlation of critical parameters, statistical data studies, and verification of defect-free material, our suppliers may reach a certified status where routine incoming inspection at NCR is no longer necessary. To date, we have certified the primary suppliers of critical materials, accounting for over 75% of fabrication material purchases. When inspections are performed, all materials are physically segregated and secured until the inspection results are complete and found to conform to all purchase specifications and requirements. Non-conforming raw materials are labeled and impounded by the incoming inspection lab. Raw material traceability is maintained through the manufacturing process wherever possible. Procedures are in place to control material with shelf life limitations.

Production Lot Traceability

Complete traceability of production lots is maintained from the formation of the lot through shipment of final product to the customer. The identity of raw materials used throughout the process becomes part of the lot history. Each integrated circuit is marked with lot number and date code data to provide retrieval of a complete processing/raw material history. Records of raw materials, lot processing, inspections, reliability testing, and quality testing are retained for a minimum of three years.

Assembly

Long term relationships have been established with a few key assembly subcontractors as with all raw material and services that NCR purchases. Quality improvement expectations are established and monitored for yields, and other process parameters. NCR retains personnel near the supplier sites to enhance the relationships and quickly resolve any issues.

Operator Certification

The production and quality control operators are a key element in the quality of our manufacturing processes. Their full understanding of the process is essential, and as such, all operators must be certified. Certification begins with classroom instruction on integrated circuit production, Statistical Process Control (SPC), safety, and detailed instruction on the operation they will be running. After classroom instruction, operators are given hands-on instruction where they process material through their operation under the direct supervision of the trainer. When instruction is complete, operators take a certification test, which they must pass without errors. It is only at this point that they may process production material. Recertification is performed at six month intervals.

Statistical Process Control

Statistical Process Control (SPC) is a very effective program at NCR and has been so since 1983. Today, SPC is used widely throughout the manufacturing process. SPC is real time, hand plotted, and operator owned. This means that ownership of the process belongs to the person who is most knowledgeable about the process, the operators. Each data point is taken, plotted, and interpreted by the operator. If an out-of-control situation is encountered, the operator can shut down the process. The process remains down until engineering identifies and corrects the problem. The engineer, shift supervisor, and the operator must approve the correction before production may resume.

Process Capability is an integral part of NCR's statistical approach to process control. The process capability index is calculated for each "operator owned" process. Process capability is continuously driven by engineering. Quality improvement efforts are targeted at reducing process variability to achieve Cpk's of 1.33 or greater.

"Get the process right and the result will be right." NCR's statistical process control is built around this principle. Process monitors and pilots, instead of production materials, are used for inspection and measurement wherever possible. This eliminates the need for additional handling of fragile wafers and components.

NCR's association with Sematech has allowed us to compare our SPC programs with others in our field. It is this comparison, as well as inputs from customer audits, that confirm the effectiveness of NCR's SPC program.

Calibration

Properly maintained and calibrated equipment is necessary to produce components with a high degree of consistency. All NCR manufacturing equipment is on a routine preventive maintenance and calibration schedule. Both preventive maintenance and the calibration systems are based on automated recall, so that scheduled work on any piece of equipment will not go unnoticed.

Document Control

All manufacturing, quality control, incoming inspection, training, and reliability operations are controlled by formal specifications. Each specification is posted at the work station for easy reference. Specifications are under full change control, meaning changes to procedures must be approved by appropriate personnel, stamped by document control, incremented in revision letter, and released to the manufacturing line. Latest revisions of specifications are posted at the work station, and all obsolete copies are removed.

Quality Assurance

While true quality improvement cannot be achieved through inspection, it is important that routine self-evaluations be performed to monitor the effectiveness of our processes. Our quality assurance programs measure the quality and reliability of our products and processes on which they are manufactured.

Quality Conformance Testing

Conformance testing is performed on 100% tested, shipment-ready products. Conformance testing consists of both electrical and visual tests. Samples are randomly selected and tested to customer specifications by the Quality Control group.

Ongoing Reliability Monitors

NCR's ongoing reliability program continuously monitors the reliability of our products. Reliability monitors consist of the following testing:

- High Temperature Operating Life – each process
- SEM/EDAX – each process category
- Autoclave – each package type/assembly site
- 85/85 – each package type/assembly site
- Temperature Cycling – each package type/assembly site
- Marking Permanency – each package type/assembly site
- Solderability – each package type/ assembly site
- Lead Fatigue – each package type/assembly site
- Dimensions – each package type/assembly site

Process Audits

To assure that processes and procedures are performed as intended, Quality Engineering performs a series of process audits. These audits include:

- Training
- Calibration
- Document revision
- Statistical Process Control
- ESD (Electrostatic Discharge)
- Environmental (Temperature/Humidity/Particle)

This series of audits is performed at our overseas assembly sites, our raw material suppliers facilities and subcontract locations, as well as at our own facilities.

Material Review Boards

If during conformance testing, reliability testing, or at any other time in process, material is suspected of being non-conforming or deviated, affected material is segregated and impounded. A Material Review Board (MRB) is then convened to review available data and formulate a disposition plan for affected material. Some examples of dispositions are: define requirements for further testing, no risk/MRB accept, rework material, scrap material. If the decisions of the board indicate an impact to customer commitments or product performance in any way, the customer will be involved in the MRB decision. Records of MRB decisions are on file at NCR.

Failure Analysis

NCR maintains full failure analysis capability in-house. Devices requiring failure analysis (F.A.) may come from a variety of sources, including reliability monitors, conformance testing, or customer returns. The purpose of failure analysis is to determine the root cause of all failures, and to work with the various engineering organizations to establish closed loop corrective action. Root Cause Analysis and Closed Loop Corrective Action assures that recurrence of the failure mode is prevented.

Cycle time of customer returns through failure analysis is determined on a case by case basis. The goal for analysis of casual returns is two weeks. For critical analysis, where the disposition of the production process or material is in question, verification can be performed within 48 hours of receipt, with complete failure analysis and corrective action within one week.

Process Change Notification System

It is our policy to keep our customers informed of our intent to make product enhancements through process changes. Before implementation, all affected customers are sent a notice of intent to change the process. Along with the letter of notification, a description of the change, a reliability qualification plan, and a planned implementation date are included. An NCR contact is provided to answer your questions regarding the change.

Process Flow

Customer procurement specifications are welcomed whenever applicable. Evaluation of customer requirements is typically performed at the time of quotation. Product Engineering will review the specification for non-standard processing, exceptions, cost adders, and alternatives. Open issues will be negotiated with the customer. When the contract is awarded to NCR, all non-standard requirements are transferred to NCR processing travelers by the product engineer. The process traveler defines the flow of the product through each process step or module. Current process/inspection status can be ascertained at any time from the traveler.

Outgoing Testing

All components are 100% electrically tested before shipment to customers. Test programs that exercise the chips are typically derived from the original design simulation vectors in order to assure maximum test coverage.

Shipping

Components are shipped to our customers in an environment that assures components are protected from degradation during transportation and storage, such as electrostatic damage, physical damage, and damage due to environmental exposure.

Quality Improvement

The progression towards zero defects does not happen automatically. Quality improvement must happen at all levels of the organization. The plant Quality Council, comprised of the General Manager and his staff, has defined quality related objectives for each functional organization in the plant. These objectives highlight key parameters, current status, and goals for the future that will position NCR with best-in-class products and processes. These objectives are incorporated into other strategic and operating plans, are the subject of plant operating reviews, and become a yardstick for the measurement of each organization's success.

Process Management

At the heart of quality improvement at NCR is a program called Process Management (PM). PM is a method of defining, documenting, measuring, and improving processes. Processes are defined in terms of inputs, outputs, and tasks. PM promotes the philosophy that each person is an internal customer from a previous operation, is responsible to perform certain tasks, and then is an internal supplier to someone else in the organization.

PM is used to improve processes in all functional organizations, not just manufacturing's.

Closed Loop Corrective Action

When a quality issue is detected, it is important that effective corrective actions are implemented to prevent recurrence. NCR's Closed Loop Corrective Action Program (CLCA) is a formal system in which the problem is identified, root cause is determined, the affected material is contained, the process is corrected, the corrective action is verified, and the results monitored. The process is used in manufacturing, quality assurance, engineering, and service operations.

Customers

NCR produces components for a wide variety of markets and environments. Applications include electronic data processing, communications, industrial process control peripherals, PC/workstations, automotive, and military.

NCR's customers are highly sophisticated and quality conscious users of I.C. components. All of these customers have extremely rigorous requirements for quality and reliability. Through the years, NCR has exceeded these expectations and has attained preferred supplier status with the giants in the field.

Our customers develop their trust in NCR based upon satisfaction with our products, talking with our people, and seeing our operations. We extend an invitation to all of our customers to visit our facilities and see our programs first hand.

NCR CAE Tools

ASIC Design Flow

All semicustom design flows using NCR tools follow the same basic steps. Each step is explained in the upcoming sections. The basic NCR semicustom design flow consists of the following steps:

1. Prepare a design specification.
2. Capture your design in HDL, VHDL or schematic.
3. Enter design information into Worksheet.
4. Create simulation vectors with DesignSim ATL.
5. Perform an architectural simulation for HDL/VHDL portions of design, or functional simulation of schematic.
6. Synthesize and optimize the HDL/VHDL definitions.
7. Optimize schematic descriptions
8. Design rule checks.
9. Perform pre-layout timing simulations.
10. Validate the simulation output.
11. Design rule checks.
12. Design review and handoff.
13. Perform post-layout simulations.
14. Perform fault simulations.
15. Validate post-layout simulations.

Prepare a Design Specification

NCR encourages you to thoroughly plan and specify your design. Proper planning and detailed specifications reduce the number of design errors and difficulties you will encounter. Ideally, a specification describes the functional, timing, electrical, and physical characteristics of the integrated circuit that you intend to build. Further definition can be specified in HDL/VHDL.

Capture of Your Design Idea

After developing your ASIC requirements, capture your design in HDL/VHDL or with a schematic tool. Select an NCR cell library in the synthesis tool or schematic. At the heart of NCR's design system is the Design and Verification Software Package. This software package includes the models for the NCR libraries, cells, macros and ViGen compiler function rich in functionality and capabilities. There are key application specific functions available in the NCR libraries. Also included are DesignTest test generation tools. Check with NCR concerning the support of translation of FPGAs and PLAs to NCR libraries.

Supported Schematic Capture Packages

- Verilog HDL
- VHDL from leading commercial CAE suppliers.
- NETED™/Design Architect™ from Mentor Graphics
- EDGE™/Amadeus™ from Cadence Design Systems
- GED™ from Valid
- ACE™ from DAZIX™
- Viewdraw™ from Viewlogic™

Enter Design Information into Worksheet

Use Worksheet to capture the information needed by the DesignTest tools and by NCR engineers responsible for creating your test program. The DesignTest tools include DesignSim ATL, Verify, ViPac2, and ViStrobe.

Create Simulation Vectors with DesignSim ATL™ (Automated Test Language)

DesignSim ATL is a high-level language that compiles simulation vectors that are guaranteed to be tester compatible. User-defined expected output states can be specified with DesignSim ATL. A sister software package, Verify, provides a meticulous method of checking the results of the simulation with the expected states specified in DesignSim ATL. A "C" pre-processor is required to run DesignSim ATL.

DesignSim ATL currently supports Mentor Graphics QuickSim, Verilog XL and IKOS. Others are in development.

Perform Architectural Simulation

Perform at the RTL or behavioral level. Try design alternatives and simulate.

Synthesize

Synthesize from Verilog HDL, or VHDL, optimize, test synthesis test, pattern synthesis and area/speed tradeoff analysis. Synopsys synthesis is supported. Check with NCR for the support of additional synthesis tools.

Perform Functional Simulations

A functional simulation is a logical simulation of the circuit, with unit delays assigned to each instance in the design. When you perform a functional simulation, you test the logic, not the timing of your design. Functional simulations are intended to help you find and eliminate logic errors in your design before you begin the timing analysis process.

Supported Simulators

- QuickSim™ from Mentor Graphics
- Verilog-XL from Cadence Design Systems
- Viewsim/SD™ from Viewlogic
- IKOS from IKOS Systems
- VHDL Simulators from leading commercial CAE suppliers.

Check with NCR for the support of additional supported simulators.

Perform Pre-layout Timing Simulations

A pre-layout timing simulation, or estimated real-time simulation, is a simulation with timing information added. NCR models provide the capability to generate pre-layout, approximate best-/worst-case delays for the design based on capacitive loading and approximate routing factors. With these calculated delays you must perform two estimated real time simulations: one after calculating and back-annotating worst-case delays and one after calculating and back-annotating best-case delays.

Validate the Simulation Output

Validating the simulation output is made easier if you use Verify to check the simulation outputs with the user-defined expected output states specified in the DesignSim ATL language.

Design Review and Handoff

To aid with the design review and handoff a Design Package Checklist and review questions are provided to help you prepare for the design review.

NCR layout engineers perform the physical layout, extract interconnect loading and calculate the post-layout real-time propagation delays. These delays are provided to you for post-layout simulations.

Perform Post-layout Simulations

A post-layout timing simulation is one in which you check the real-time delays of the circuit. You perform these simulations after the circuit goes through the layout step, using interconnect delays supplied by NCR for your circuit.

With the ability to provide you with accurate post-layout delays, NCR guarantees that silicon will match the simulation results of the simulators supported for full ASIC validation. Therefore, NCR gives you complete control over verifying your design on your workstation. This eliminates the need for NCR to perform resimulations and your NREs will have no CPU charges.

Validated Simulators

- QuickSim from Mentor Graphics
- Verilog from Cadence Design Systems

Check with NCR for the support of additional validated simulators.

Perform Fault Simulations

Fault grading helps to determine the completeness of the test patterns for controlling and observing nodes within the device. Conventional deterministic fault grading is performed by "sticking" a node at 1 or 0, running the test patterns and seeing if the output patterns differed from normal; a difference says that the fault was detected (observed). The process is repeated for all circuit nodes. The resulting report gives the percentage of node faults which will be detected by the patterns, also known as fault coverage. This process requires a great deal of computational power and time to analyze all nodes.

Probabilistic fault grading applies newer algorithms to node toggle counts and other data recorded during a regular simulation with the test patterns. The algorithms determine a list of nodes "not likely" to be adequately controlled or observed and estimates the total coverage. This method is usually accurate to within 3% of results from deterministic fault grading. The advantage of probabilistic fault grading is much less run time and therefore lower cost than deterministic fault grading.

DesignSim ATL and Verify can help decrease the time required to generate manual fault vectors.

Supported Deterministic Fault Simulators

- QuickFault™ from Mentor Graphics
- IKOS from IKOS Systems

Check with NCR for the support of additional deterministic fault simulators.

Supported Probabilistic Fault Simulator

- QuickGrade™ from Mentor Graphics

Validate Post–layout Simulations

You can check the conformity of your simulations by using a set of test programs from NCR, collectively called the DesignTest programs. These programs help you verify that NCR test engineers can use your simulation outputs for generating test programs. If you are using DesignSim ATL and Verify, they will automatically perform the checks necessary and generate correct tester–compatible input patterns and strobe placements.

Checking Design Rules

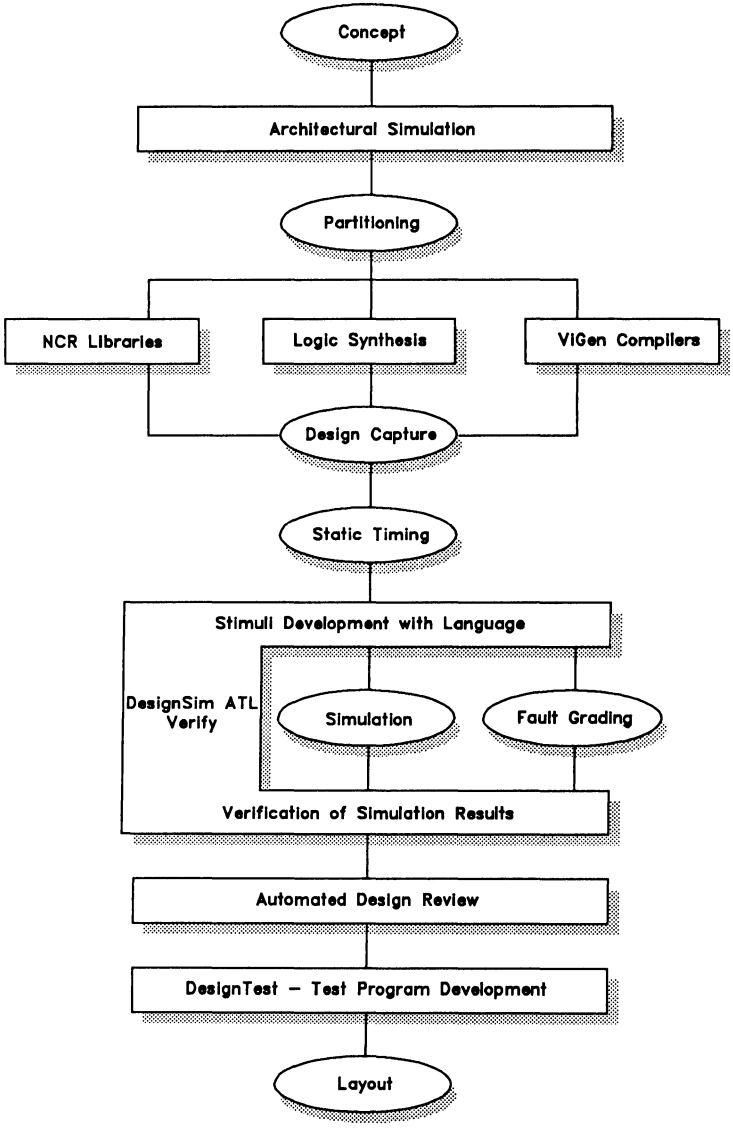
The following is a partial list of NetChecker checks. In the list, the following abbreviations apply:

E = Error message
W = Warning
I = Information

The name of the checks are from the NetChecker report file.

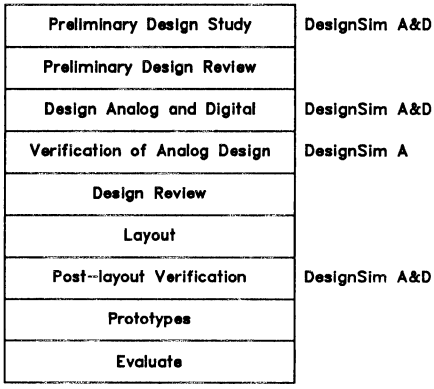
E – Bus contention
E – Flip–flop is not clocked
E – Permanently set or reset flip–flop
E – Floating input pin
E – Misuse of PU30 or PD30
E – Possible meta–stable state
E – Pad pullup or pulldown is missing
E – Disabled PPU or PPD instance
E – Internal use of external pad signal
E – Pad buffer is missing
E – Reversed I/O buffer
W – Driver overload
W – Buffer underload
W – Floating bus
W – Disabled NAND or AND
W – Disabled NOR or OR
W – Disabled AOI or OAI term
W – Disabled AOI or OAI cell
W – Asynchronous feedback path
W – Enable pin tied active or inactive
W – Internal use of PPU or PPD
W – Output pad and buffer incompatibility
I – Input signals
I – I/O signals
I – Output signals
I – Power pad calculations

ASIC Design System Design Flow



The design flow for mixed analog/digital design utilizing DesignSim A&D or SABER/Verilog provides for feasibility analysis with NCR ASIC cells, combined analog/digital simulation and post-layout verification.

Mixed Analog/Digital Design Flow (Utilizing DesignSim A&D)



ASICs within Systems Design

NCR provides premier support of design systems, offering the design engineer full system-level simulation including ASIC chipsets. The design methodology can be top-down with the use of high-level languages such as VHDL or Verilog HDL, or with conventional schematic capture at the printed wire board and ASIC levels, or a combination. Board-level and electromechanical subsystem mixed analog/digital simulation is available by using standard component models provided by specialized CAE modeling companies or directly from CAE software suppliers, models developed by the designer, or both.

NCR customers are experiencing ever improving first-pass success rates with ASICs designed in NCR tools and simulated as components on printed wire boards. ASICs are proven with simulation to work within the system before they are committed to silicon.

As circuit speeds increase with submicron technologies, and systems are designed for higher speeds, NCR's Accurate-Precision Modeling Technology presents the accuracy needed for each unique design implemented with NCR's cell-based and gate array products. The Accurate-Precision Modeling Technology is used for simulation and timing analysis.

Synthesis tools provide for area and speed optimization. Static timing analysis tools help assure that design margins selected by the design engineer are achieved. Timing analysis tools supported from leading CAE suppliers can be applied not only to the ASIC, but also at the printed wire board level.

NCR Supplements Popular CAE Design Tools

NCR supplements support of popular CAE design systems with popular specialty CAE design tools and NCR-developed productivity enhancement tools that provide you with world class design systems. These CAE design systems provide the capability to perform ASICs within systems simulation, top-down design utilizing architectural simulation and synthesis, hardware modeling, and fault grading on industry-standard platforms. Therefore, you have the freedom to design products with NCR ASICs on the workstation of your choice.

Following is the present list of CAE design systems and niche CAE software products that NCR supports. NCR is continually supporting new software; please consult NCR for current information.

CAE Design System Support

- Cadence

  NCR guarantees simulation with Verilog and provides design packages supporting Cadence's Edge and Amadeus schematic capture and Veritime™ timing analysis products. Many NCR design package options are available within the Cadence Design Framework™ environment. Verilog simulation is also supported with Viewlogic and Valid schematic capture.

- Viewlogic

  NCR provides a design kit supporting Viewdraw and Viewsim/SD in its initial release. The following release will support Viewdesign™ logic synthesis.

- Mentor Graphics

  NCR guarantees simulations with Mentor Graphics' Concurrent Engineering Environment. The NCR design package supports all Mentor Graphics design tools including: Design Consultant™ logic synthesis and optimization, Design Architect schematic capture, QuickSim2 simulation and VHDL debugging environment, QuickPath™ static timing analysis, QuickGrade probabilistic fault grading, and QuickFault deterministic fault grading.

Additional CAE Tool Support

- Synthesis:

  Racal-Redac SilcSyn™

  SilcSyn provides logic synthesis from a high-level language (SDDL or VHDL subset), netlist optimization, testability synthesis, automatic test program generation, and area/speed tradeoff synthesis.

  Synopsys Design Compiler™ and HDL Compiler™

  HDL Compiler provides logic synthesis from a high-level language (Verilog HDL or VHDL subset). Design Compiler provides state machine synthesis, accepts netlist or Boolean inputs, performs timing and area optimization and includes schematic generation.

- Schematic Capture:

  Valid Logic Systems' ValidGED

  NCR provides Verilog "golden" simulation of Valid schematics via netlist extraction.

- Logic and Fault Accelerators:

  IKOS Systems' Simulation Accelerators

  NCR models are available for IKOS' logic and fault simulation accelerators. IKOS supports access from the leading schematic capture systems.

- Analog Simulator:

  Analogy's Saber™

  NCR provides analog behavioral models for the Saber analog simulator. Model parameters can be modified by designers.

- Mixed Analog/Digital Simulator:

  Analogy and Racal-Redac/HHB Systems' Saber/CADAT (NCR DesignSim A&D)

  NCR provides analog and digital models for mixed-signal ASIC simulations. Saber/CADAT can be accessed from both the Mentor Graphics and Cadence schematic capture tools.

- Saber/Verilog-XL

  NCR provides analog and digital models for mixed-signal ASIC simulations with SABER/Verilog. Access is from both Mentor Graphics and Cadence schematic capture tools.

NCR VLSI Design and Verification System's Value Added Software

NCR standard cell and gate array libraries

NCR provides a complete set of standard cell and gate array libraries for capturing and verifying your ASIC designs on popular platforms including HP/Apollo, Sun and PCs (IBM-compatible).

These libraries are rich in functionality and capability. Familiar functions, such as the 82CXX and 74CXX soft macros, and easily generated menu-driven compiler functions, such as ROMs, RAMs, FIFOs, and multiplier/accumulators, contribute to ease of design. Additionally, NCR adds to these functions, Application Specific Functions.

Moreover, since all NCR gate array and standard cell libraries share an extensive core of digital functions and are contained within the same suite of NCR Design and Verification tools, designs can be "migrated" between supported libraries at the schematic or netlist level. This capability protects engineering and product investment from obsolescence. In other words, you can easily migrate a VGX1500 gate array design to VS1500 standard cells for cost reduction or to add a ROM. Or, a VS1500 standard cell design can be easily migrated to VS700 libraries. This migration path is an important part of NCR's plans for the future.

The NCR libraries are compatible with many of the industry's leading CAE ASIC design software vendors. Consult NCR for further information.

NCR ViTa™ Timing Calculators

ViTa provides you the capability to generate pre-layout, approximate best-/ worst-case delays for the design based on capacitive loading and approximate routing factors. It also enables you to incorporate interconnect delays calculated after layout for post-layout simulations on your CAE workstation. All NCR tools get delay information from ViTa.

With the ability to provide you with post-layout accurate delays, NCR guarantees that silicon will match the simulation results from the supported simulator. This gives you complete control over your design and eliminates the necessity for NCR to perform resimulations and your NREs will have no CPU charges. Moreover, your workstation will be more fully utilized because you can perform post-layout board-level simulations.

NCR ViGen™ Configurable Compiler Functions

NCR gives you access to silicon compiler function flexibility and densities from library menus within your schematic capture package to incorporate memory and multiplier functions into your standard cell and gate array designs. These are the ViGen Configurable Compiler Functions. The ability to incorporate these functions into your designs is part of the Design and Verification Package.

Thus, ViGen provides a new level of ease-of-use, functional richness, and system integration density. After each ViGen function symbol is configured within the schematic editor, an accurate simulation model is created for simulation and a specification file is created that is used by NCR layout engineers.

For specific options in configuring the ViGen Configurable Compiler Cells, see the appropriate data sheets.

NCR DesignTest™ Design Verification and Test Development Tools

NCR provides the DesignTest suite of tools with the Design and Verification Package to help you ensure that the same simulation vectors that were used for verifying the design on the workstation can also be used to perform "at-speed" testing of your ASIC devices. The DesignTest tools also provide an automatic means to enter and maintain information relating to the ASIC device that is being designed. There are six programs that comprise this suite of tools: DesignSim ATL, Verify, Worksheet, ViPac2, ViComp, ViStrobe and DesignTest Checker.

Worksheet

Worksheet provides the ability to automatically enter, maintain, and view ASIC design and test information for the purposes of simulation and test pattern development. Device and timing information from the worksheets is provided automatically to the other DesignTest tools, such as ViPac2, ViStrobe, and Wisil (DesignSim ATL).

Wisil (DesignSim ATL)

Wisil (Workstation Independent Stimulus Input Language) is a programming language that helps you create simulation input files and files describing your expected output. Because Wisil is a programming language, it has a compiler associated with it.

Verify

Verify, a companion program to DesignSim ATL, automatically compares the expected outputs specified in the high-level language to the actual outputs from the simulation. These "expected outputs" can also be provided from a previous run of a supported simulator. Thus you will be able to verify a design change, compare best-case results with worst-case, compare pre-layout with post-layout, etc.

Wisil and Verify can also be used to transfer patterns between simulators and to simulate patterns from a test program. This method is used by NCR to provide fault grading services which comprehend strobe placements to more accurately grade the patterns used on the production IC tester.

Your ASIC verification and test patterns will also be more thoroughly documented with Wisil. Wisil descriptions document intended device functionality and can include comments which will be passed through to the simulation input stimuli for the particular simulator and to the test program used by NCR test engineers to verify production devices.

Currently supported simulators for the DesignTest tools include QuickSim, Verilog–XL, and IKOS. Supported testers include Sentry and Trillium.

ViPac2

ViPac2 (VLSI Pattern Checker) extracts Sentry and Trillium patterns from the simulation output files. The tool also verifies that the input timings are correct and that the input stimuli can be generated by the tester.

ViComp

ViComp (VLSI Composite) merges best and worst–case simulation output patterns. The result is an ASCII–format output which shows the designer where the data is valid for both best– and worst–case simulations. This information is fed to ViStrobe.

ViStrobe

ViStrobe (VLSI Strobe) assures that you have entered proper strobe placements into Worksheet by analyzing the results of ViComp. This tool identifies strobe placements which miss composite outputs and composite pulses which are too short or cross test periods.

DesignTest Checker

DesignTest Checker (DTC) checks to make sure you have a complete and correct set of Worksheet and test vector files. It detects problems in tool usage that would otherwise go undetected until the NCR design review or design package submission.

NetChecker Design Analysis

The NCR NetChecker provides you with design rule checking. The tool helps ensure first-pass of customer designs. You can run NetChecker at both the sub-block (design module) level and the complete design level. NCR requires that all designs be run through NetChecker before the Design Review.

Engineering Workstation Compatibility

NCR has always been a leader in engineering workstation support. This support is not a recent development but a cornerstone of NCR's design philosophy since we entered the ASIC marketplace in 1981. Recognizing the benefits of open schematic capture and simulation tools, NCR was the first standard cell vendor to port design systems to engineering workstations. Customers have been performing pre- and post-layout simulations with NCR libraries and software on Mentor Graphics workstations since 1983. In 1985 test generation tools were added to speed the design cycle. NCR has now added support of the Cadence and Viewlogic workstations. This capability is enabled by porting the NCR Design and Verification suite of tools to these systems and certifying correct operation of the host workstation tools and logic simulator through sophisticated test procedures.

NCR library models have been correlated with silicon so accurately that the performance seen with the validated simulators is guaranteed in silicon without any mainframe resimulations. This decreases verification and development time. Plus it enables designers to use their workstations to the fullest by performing post-layout board-level simulations.

Additional design capabilities are always being added to each supported workstation. Consult NCR for current information.

NCR DesignSim™ A&D Analog and Digital Simulation

DesignSim A&D brings together two powerful industry-standard simulators for advanced mixed-analog/digital verification of ASIC designs and ASIC-in-system designs. The tool is comprised of DesignSim A, based on the industry-leading Saber from Analogy, Inc., and DesignSim D based on CADAT from Racal-Redac. DesignSim A is known for its accurate and highly graphical simulation of analog systems. Together they provide a powerful and accurate mixed-analog/digital simulation.

NCR also supports SABER/Verilog-XL with analog, digital and hyper models linking NCR analog and digital models. Verilog-XL is from Cadence Design Systems, Inc.

Fault Grading Overview

Fault grading is a measure of how completely your test program checks for potential manufacturing defects in your chip. Fault grading reports the percentage of possible stuck–at–one and stuck–at–zero faults in your chip that will be detected by your test program. Most other types of faults (e.g., stuck–together) will also be picked up by a test program with a high stuck–at–fault coverage. NCR offers two types of fault grading services.

The cost of detecting and fixing a fault increases by about an order of magnitude at each step in the manufacturing process. It costs ten times as much to find and fix a fault at board test as it does to find it with the chip test program. It costs ten times more to find a fault at system test than it does on the board, and ten times more to find the fault in the field than at system test. These are just the direct economic costs; when a fault is found in the field, there are additional costs in customer downtime and lowered perceived quality of your product.

The fault coverage of the test programs used at each of these steps determines how many potential faults pass that step undetected. These economics quickly justify the effort of achieving high fault coverage as early on in the process as possible, and your chip test program is the first (and lowest cost) opportunity to root out faults.

Typically, the patterns used for design verification provide fault coverage of 70–85%. Since a minimum fault coverage of 85% is desirable, and coverage of 90% or more is preferred, most designs require some form of fault grading. This provides you with information on the completeness of your patterns and helps identify any areas requiring additional coverage.

Fault Grading Methodologies

Deterministic

A deterministic fault grade (DFG) runs your test patterns on the chip and stores the result. It will then apply a fault to one net (tie it to 0 or 1) and run the test patterns again until a difference is found between the output of the faulted circuit and the stored "good chip" output. If a difference is found, the fault is detected by the test patterns.

Although techniques can be used to compress the process, a deterministic fault grader must basically run the simulation twice for each net in your circuit. This is CPU intensive and, therefore, an expensive and slow process. Hardware accelerators are frequently used to speed up the job.

Probabilistic

Probabilistic fault grading (PFG) uses mathematical algorithms that estimate the probability that a net will be driven to a 1 or 0 state (controllability) at the same time that a path is sensitized to propagate the result of that change to an output pin (observability). This probability is calculated from the number of state changes on the relevant nets and special transform functions for the logical elements in the path. This net activity information can be collected from a single run of the test program, so the fault grading run time is comparable to that of a single simulation run, with only the overhead of collecting net activity information and calculation of the fault probabilities added.

An estimated fault coverage (accurate to ± 3%) and a list of faults with the poorest observability and controllability statistics are reported. This is not a comprehensive list of uncovered faults, but rather a list of candidate faults to be addressed with additional vectors should you desire higher fault coverage. Because of the faster run times, probabilistic fault grading is substantially less expensive than deterministic.

NCR Fault Grading Options

NCR offers several fault grading alternatives. First, library models are certified for correct operation with fault grading tools supplied by several vendors. Second, NCR offers both probabilistic and deterministic fault grading services.

NCR VS700 Standard Cell Library Data Sheets
Alphabetical Contents

NCR VS700 Standard Cell Library Data Sheets
Functional Contents

Simple Logic Cells

Buffers

Latches

Shift Registers

Decoders and Multiplexers

Flip–Flops

Special Function Cells

Tristate Elements

Input/Output Cells

NCR VS700 Standard Cell Library

Electrical Specifications

DC Characteristics

Sym	Parameter	VDD	Guaranteed Limit			Unit
			0 to 70°C	−40 to 85°C	−55 to 125°C	
V_{IH} (TTL)	Minimum high-level Input voltage	4.5	2.0	2.0	2.0	V
		5.5	2.0	2.0	2.0	
V_{IL} (TTL)	Maximum low-level Input voltage	4.5	0.8	0.8	0.8	V
		5.5	0.8	0.8	0.8	
V_{IH} (CMOS)	Minimum high-level Input voltage	4.5	3.15	3.15	3.15	V
		5.5	3.85	3.85	3.85	
V_{IL} (CMOS)	Maximum low-level Input voltage	4.5	1.35	1.35	1.35	V
		5.5	1.65	1.65	1.65	
V_{OH}	Minimum high-level Output Voltage Any buffer, I_{OH} = −20µa	4.5	4.4	4.4	4.4	V
		5.5	5.4	5.4	5.4	
I_{OH}	Minimum high-level Source Current, V_{OH} = 2.4V					mA
	2mA buffer	4.5	2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	21.8	
	48mA buffer		n/a	n/a	n/a	
V_{OL}	Maximum low-level Output Voltage Any buffer, I_{OL} = 20µa	4.5	0.1	0.1	0.1	V
		5.5	0.1	0.1	0.1	
I_{OL}	Minimum low-level Sink Current, V_{OL} = 0.4V					mA
	2mA buffer		2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	20.6	
	48mA buffer		48.0	48.0	46.6	
I_{IN}	Maximum input leakage current	5.5	±10	±10	±20	µA
I_{OZ}	Maximum output leakage current	5.5	±10	±10	±20	µA

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{DD}	DC power supply voltage	−0.5 to 7.0	V
V_{IN}, V_{OUT}	DC input, output voltage	−0.5 to V_{DD}+0.5	V
I	DC current drain V_{DD} and V_{SS} pins	100	mA
T_{STG}	Storage temperature	−55 to 150	°C
T_L	Lead temperature (less than 10 second soldering)	250	°C
T_{OPER}	Operating temperature Commercial Industrial Military	 0 to 70 −40 to 85 −55 to 125	°C

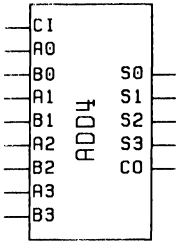
* Stresses beyond those listed in the "Absolute Maximum Ratings" table may cause physical damage to a device and should be avoided. This table does not imply that operation at conditions above those listed in the "Recommended Operating Conditions" is possible. This is a stress rating and operation of a device at or above this rating for an extended period may cause failure or affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	DC power supply voltage	3.0	6.0	V
V_{IN}, V_{OUT}	DC input, output voltage	0	V_{DD}	V

4–Bit Adder

The ADD4 is a four–bit, asynchronous, ripple adder with carry–in/carry–out function. See the ADD4CS data sheet for application notes.



Inputs: CI, A0, B0, A1, B1, A2, B2, A3, B3
Outputs: S0, S1, S2, S3, CO
Input Cap.: CI: 0.251
A0: 0.249
B0: 0.241
A1: 0.210
B1: 0.217
A2: 0.134
B2: 0.136
A3: 0.133
B3: 0.132 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.367 M_{CHL} = 0.323
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 108.0 grids wide, 13.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A0 to CO	2.25	4.22	4.40	4.94
t_{PHL}		2.19	4.11	4.28	4.81
t_{PLH}	A1 to CO	1.94	3.64	3.80	4.26
t_{PHL}		2.03	3.81	3.98	4.46
t_{PLH}	A2 to CO	1.63	3.06	3.20	3.59
t_{PHL}		1.79	3.36	3.51	3.94
t_{PLH}	A3 to CO	1.10	2.08	2.17	2.44
t_{PHL}		1.30	2.45	2.56	2.87
t_{PLH}	B0 to CO	2.26	4.25	4.43	4.98
t_{PHL}		2.18	4.09	4.27	4.79
t_{PLH}	B1 to CO	2.02	3.79	3.95	4.44
t_{PHL}		2.05	3.84	4.01	4.50
t_{PLH}	B2 to CO	1.66	3.13	3.26	3.66
t_{PHL}		1.81	3.40	3.55	3.98
t_{PLH}	B3 to CO	1.14	2.16	2.25	2.53
t_{PHL}		1.32	2.48	2.58	2.90
t_{PLH}	CI to CO	2.28	4.28	4.46	5.01
t_{PHL}		2.19	4.10	4.28	4.80
t_{PLH}	CI to S0	0.979	1.85	1.93	2.17
t_{PHL}		0.759	1.44	1.50	1.69
t_{PLH}	CI to S1	1.32	2.49	2.60	2.92
t_{PHL}		1.23	2.31	2.41	2.71

Timing characteristics (Sheet 1 of 2)

ADD4

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CI to S2	1.85	3.47	3.62	4.06
t_{PHL}		1.75	3.30	3.44	3.86
t_{PLH}	CI to S3	2.38	4.47	4.66	5.24
t_{PHL}		2.28	4.28	4.46	5.01
t_{PLH}	A0,B0 to S0	1.21	2.28	2.37	2.67
t_{PHL}		0.908	1.72	1.79	2.01
t_{PLH}	A0,B0 to S1	1.22	2.31	2.41	2.71
t_{PHL}		1.08	2.05	2.14	2.40
t_{PLH}	A0,B0 to S2	1.74	3.27	3.41	3.83
t_{PHL}		1.61	3.03	3.15	3.54
t_{PLH}	A0,B0 to S3	2.26	4.25	4.43	4.97
t_{PHL}		2.14	4.02	4.20	4.71
t_{PLH}	A1,B1 to S1	1.60	3.01	3.14	3.52
t_{PHL}		1.10	2.07	2.16	2.43
t_{PLH}	A1,B1 to S2	1.59	2.99	3.12	3.50
t_{PHL}		1.35	2.55	2.66	2.99
t_{PLH}	A1,B1 to S3	2.11	3.97	4.14	4.64
t_{PHL}		1.89	3.55	3.70	4.16
t_{PLH}	A2,B2 to S2	1.61	3.03	3.16	3.55
t_{PHL}		1.10	2.07	2.16	2.43
t_{PLH}	A2,B2 to S3	1.88	3.54	3.69	4.14
t_{PHL}		1.54	2.90	3.02	3.40
t_{PLH}	A3,B3 to S3	1.61	3.03	3.16	3.55
t_{PHL}		1.12	2.11	2.20	2.47

Timing characteristics (Sheet 2 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A0 to CO	2.02	0.747
t_{PHL}		1.94	1.14
t_{PLH}	A1 to CO	1.71	0.773
t_{PHL}		1.79	1.05
t_{PLH}	A2 to CO	1.40	0.747
t_{PHL}		1.54	1.13
t_{PLH}	A3 to CO	0.873	0.747
t_{PHL}		1.06	1.05
t_{PLH}	B0 to CO	2.04	0.747
t_{PHL}		1.93	1.11
t_{PLH}	B1 to CO	1.79	0.667
t_{PHL}		1.80	1.07
t_{PLH}	B2 to CO	1.43	0.740
t_{PHL}		1.56	1.11
t_{PLH}	B3 to CO	0.914	0.740
t_{PHL}		1.08	1.03
t_{PLH}	CI to CO	2.05	0.760

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		1.94	1.11
t_{PLH}	CI to S0	0.548	2.77
t_{PHL}		0.481	1.42
t_{PLH}	CI to S1	0.908	2.61
t_{PHL}		0.938	1.54
t_{PLH}	CI to S2	1.43	2.57
t_{PHL}		1.47	1.50
t_{PLH}	CI to S3	1.97	2.63
t_{PHL}		1.99	1.49
t_{PLH}	A0,B0 to S0	0.875	1.76
t_{PHL}		0.618	1.55
t_{PLH}	A0,B0 to S1	0.884	1.87
t_{PHL}		0.829	1.20
t_{PLH}	A0,B0 to S2	1.40	1.85
t_{PHL}		1.36	1.18
t_{PLH}	A0,B0 to S3	1.92	1.85
t_{PHL}		1.89	1.18
t_{PLH}	A1,B1 to S1	1.17	2.73
t_{PHL}		0.821	1.42
t_{PLH}	A1,B1 to S2	1.25	1.87
t_{PHL}		1.10	1.19
t_{PLH}	A1,B1 to S3	1.77	1.88
t_{PHL}		1.63	1.19
t_{PLH}	A2,B2 to S2	1.17	2.90
t_{PHL}		0.828	1.35
t_{PLH}	A2,B2 to S3	1.55	1.79
t_{PHL}		1.29	1.20
t_{PLH}	A3,B3 to S3	1.18	2.79
t_{PHL}		0.860	1.22

Delay coefficients (Sheet 2 of 2)

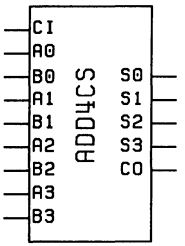
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
S0	0.531	5.14	0.332	2.51
S1	0.595	5.36	0.376	2.31
S2	0.587	5.20	0.343	2.31
S3	0.594	5.11	0.334	2.30
CO	0.227	1.39	0.156	1.87

Rise/Fall time coefficients for the next cell

4–Bit Carry Select Adder

The ADD4CS is a four-bit adder with carry-in/ carry-out function optimized for fast carry-in to carry-out and sum propagation delay.



Inputs: CI, A0, B0, A1, B1, A2, B2, A3, B3
Outputs: S0, S1, S2, S3, CO
Input Cap.: CI: 0.188
A0: 0.246
B0: 0.248
A1: 0.212
B1: 0.216
A2: 0.135
B2: 0.138
A3: 0.133
B3: 0.135 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.550 M_{CHL} = 0.290
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 181.0 grids wide, 14.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A0 to CO	2.70	5.08	5.29	5.94
t_{PHL}		2.44	4.57	4.77	5.35
t_{PLH}	A1 to CO	2.44	4.59	4.79	5.38
t_{PHL}		2.64	4.95	5.16	5.79
t_{PLH}	A2 to CO	2.31	4.36	4.54	5.10
t_{PHL}		2.56	4.81	5.01	5.63
t_{PLH}	A3 to CO	1.78	3.36	3.50	3.93
t_{PHL}		2.05	3.84	4.00	4.49
t_{PLH}	B0 to CO	2.57	4.83	5.04	5.66
t_{PHL}		2.74	5.14	5.36	6.02
t_{PLH}	B1 to CO	2.51	4.71	4.92	5.52
t_{PHL}		2.66	4.98	5.19	5.83
t_{PLH}	B2 to CO	2.35	4.43	4.62	5.19
t_{PHL}		2.59	4.85	5.06	5.68
t_{PLH}	B3 to CO	1.82	3.43	3.58	4.02
t_{PHL}		2.06	3.86	4.02	4.52
t_{PLH}	CI to CO	0.642	1.24	1.29	1.45
t_{PHL}		0.521	0.994	1.04	1.17
t_{PLH}	CI to S0	1.63	3.08	3.21	3.61
t_{PHL}		1.34	2.51	2.62	2.94
t_{PLH}	CI to S1	1.37	2.59	2.70	3.04
t_{PHL}		1.38	2.59	2.70	3.03

Timing characteristics (Sheet 1 of 2)

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CI to S2	1.35	2.55	2.66	2.99
t_{PHL}		1.37	2.57	2.68	3.01
t_{PLH}	CI to S3	1.35	2.55	2.66	2.99
t_{PHL}		1.37	2.57	2.68	3.01
t_{PLH}	A0,B0 to S0	1.26	2.38	2.48	2.79
t_{PHL}		0.903	1.70	1.78	2.00
t_{PLH}	A0,B0 to S1	2.36	4.45	4.64	5.21
t_{PHL}		1.70	3.20	3.33	3.74
t_{PLH}	A0,B0 to S2	2.90	5.45	5.69	6.38
t_{PHL}		2.23	4.18	4.36	4.89
t_{PLH}	A0,B0 to S3	3.42	6.42	6.70	7.52
t_{PHL}		2.76	5.18	5.40	6.06
t_{PLH}	A1,B1 to S1	2.04	3.84	4.00	4.50
t_{PHL}		1.84	3.45	3.59	4.03
t_{PLH}	A1,B1 to S2	2.76	5.19	5.41	6.07
t_{PHL}		2.19	4.11	4.28	4.81
t_{PLH}	A1,B1 to S3	3.29	6.18	6.44	7.23
t_{PHL}		2.73	5.11	5.33	5.98
t_{PLH}	A2,B2 to S2	2.05	3.86	4.02	4.52
t_{PHL}		1.87	3.50	3.65	4.10
t_{PLH}	A2,B2 to S3	3.24	6.08	6.34	7.12
t_{PHL}		2.57	4.82	5.02	5.64
t_{PLH}	A3,B3 to S3	2.03	3.82	3.99	4.48
t_{PHL}		1.86	3.50	3.65	4.09

Timing characteristics (Sheet 2 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A0 to CO	2.39	0.800
t_{PHL}		2.21	1.04
t_{PLH}	A1 to CO	2.16	0.513
t_{PHL}		2.41	1.03
t_{PLH}	A2 to CO	2.03	0.487
t_{PHL}		2.34	1.06
t_{PLH}	A3 to CO	1.50	0.480
t_{PHL}		1.82	1.09
t_{PLH}	B0 to CO	2.27	0.700
t_{PHL}		2.52	1.01
t_{PLH}	B1 to CO	2.23	0.480
t_{PHL}		2.43	1.10
t_{PLH}	B2 to CO	2.08	0.440
t_{PHL}		2.35	1.13
t_{PLH}	B3 to CO	1.54	0.453
t_{PHL}		1.82	1.12
t_{PLH}	CI to CO	0.336	0.747

Delay coefficients (Sheet 1 of 2)

ADD4CS

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		0.291	1.09
t_{PLH}	CI to S0	1.15	2.50
t_{PHL}		1.06	1.51
t_{PLH}	CI to S1	1.05	0.913
t_{PHL}		1.16	0.953
t_{PLH}	CI to S2	1.03	0.880
t_{PHL}		1.15	0.993
t_{PLH}	CI to S3	1.03	0.880
t_{PHL}		1.14	1.01
t_{PLH}	A0,B0 to S0	0.851	1.73
t_{PHL}		0.632	1.49
t_{PLH}	A0,B0 to S1	2.03	0.993
t_{PHL}		1.48	1.00
t_{PLH}	A0,B0 to S2	2.58	0.913
t_{PHL}		2.01	0.947
t_{PLH}	A0,B0 to S3	3.10	0.933
t_{PHL}		2.54	0.967
t_{PLH}	A1,B1 to S1	1.72	0.853
t_{PHL}		1.61	1.01
t_{PLH}	A1,B1 to S2	2.44	0.853
t_{PHL}		1.97	1.03
t_{PLH}	A1,B1 to S3	2.95	1.05
t_{PHL}		2.50	1.03
t_{PLH}	A2,B2 to S2	1.71	1.02
t_{PHL}		1.64	1.01
t_{PLH}	A2,B2 to S3	2.92	0.873
t_{PHL}		2.36	0.913
t_{PLH}	A3,B3 to S3	1.71	0.880
t_{PHL}		1.64	0.967

Delay coefficients (Sheet 2 of 2)

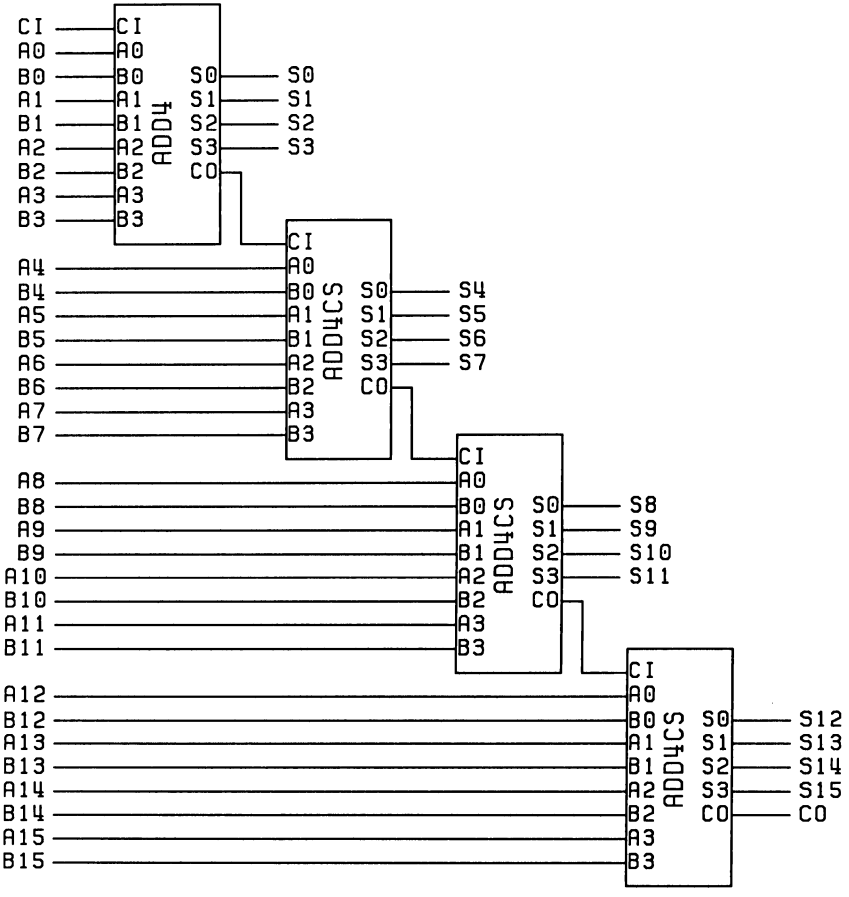
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
S0	0.541	5.14	0.400	2.47
S1	0.223	1.37	0.247	1.16
S2	0.221	1.39	0.243	1.15
S3	0.219	1.38	0.239	1.16
CO	0.146	0.931	0.154	1.85

Rise/Fall time coefficients for the next cell

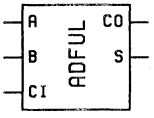
The ADD4 and ADD4CS standard cells offer the designer a performance or cell area choice. The ADD4 is a 4-bit ripple adder with a maximum propagation delay of 2.5ns under nominal conditions. The ADD4CS cell is optimized to provide carry-in to carry-out and sum times less than 1 and 2ns, respectively, for nominal conditions.

Cascading ADD4CS adders with the ADD4 (as shown in the following figure) allows for 16- and 32-bit nominal add times of less than 6 and 11ns, respectively. Speed may be traded off for cell area by using only ADD4 cells.



Full Adder

The ADFUL is a single-bit asynchronous adder with carry-in/carry-out function.



Inputs: A, B, CI
Outputs: CO, S
Input Cap.: A: 0.139
B: 0.138
CI: 0.133 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.346 M_{CHL} = 0.250
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 21.0 grids wide, 11.4 grids high

FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A,B to CO	1.51	2.85	2.97	3.34
t_{PHL}		1.49	2.80	2.92	3.28
t_{PLH}	A,B to S	1.95	3.67	3.83	4.30
t_{PHL}		2.16	4.06	4.23	4.75
t_{PLH}	CI to CO	1.33	2.51	2.62	2.95
t_{PHL}		1.22	2.29	2.39	2.68
t_{PLH}	CI to S	1.79	3.36	3.51	3.94
t_{PHL}		1.89	3.54	3.69	4.14

Timing characteristics

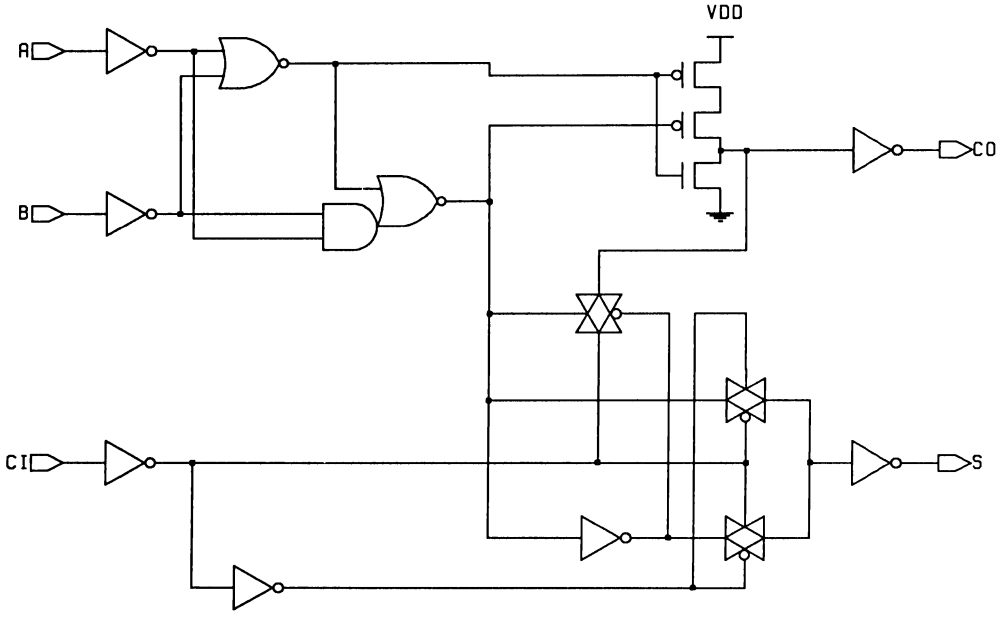
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A,B to CO	1.16	2.10
t_{PHL}		1.17	2.12
t_{PLH}	A,B to S	1.59	2.23
t_{PHL}		1.81	2.52
t_{PLH}	CI to CO	0.978	2.11
t_{PHL}		0.900	2.13
t_{PLH}	CI to S	1.42	2.24
t_{PHL}		1.54	2.35

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
CO	0.174	4.33	0.147	3.33
S	0.299	4.16	0.311	3.20

Rise/Fall time coefficients for the next cell



Functional diagram: ADFUL

AND2

2–Input AND Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.046
B: 0.043 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.117 M_{CHL} = 0.256
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.496	0.934	0.974	1.09
t_{PHL}		0.673	1.27	1.33	1.49
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.236	2.11
t_{PHL}		0.359	2.06

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.122	4.39	0.126	3.19

Rise/Fall time coefficients for the next cell

3–Input AND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.056
B: 0.054
C: 0.051 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.134 M_{CHL} = 0.263
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.555	1.04	1.09	1.22
t_{PHL}		0.862	1.63	1.70	1.91
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.283	2.15
t_{PHL}		0.538	2.13

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.136	4.38	0.196	3.05

Rise/Fall time coefficients for the next cell

4–Input AND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.056
B: 0.054
C: 0.055
D: 0.052 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.155 M_{CHL} = 0.281
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.681	1.28	1.34	1.50
t_{PHL}		0.992	1.87	1.95	2.19
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.395	2.21
t_{PHL}		0.654	2.20

Delay coefficients

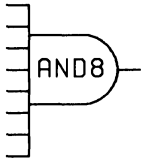
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.173	4.34	0.246	3.01

Rise/Fall time coefficients for the next cell

8–Input AND Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: A, B, C: 0.045
D, E: 0.043
F: 0.044
G: 0.045
H: 0.046 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.210 M_{CHL} = 0.231
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.0 grids wide, 8.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.932	1.75	1.83	2.06
t_{PHL}		0.968	1.82	1.90	2.14
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.572	2.72
t_{PHL}		0.670	2.01

Delay coefficients

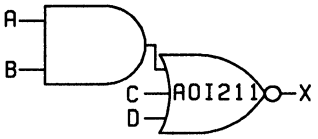
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.323	5.75	0.364	2.95

Rise/Fall time coefficients for the next cell

2–1–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A, B: 0.055
C: 0.047
D: 0.046 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.149 M_{CHL} = 0.085
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 9.9 grids high



$X = \overline{(A \cdot B) + C + D}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.960	1.80	1.88	2.11
t_{PHL}		0.389	0.733	0.764	0.858
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.518	3.79
t_{PHL}		0.187	1.67

Delay coefficients

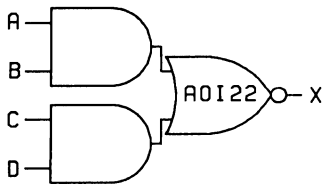
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.787	8.68	0.337	2.81

Rise/Fall time coefficients for the next cell

2–2 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.055
B: 0.056
C: 0.055
D: 0.054 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.275 M_{CHL} = 0.147
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.9 grids high



$$X = \overline{(A \bullet B) + (C \bullet D)}$$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.599	1.14	1.19	1.33
t_{PHL}		0.462	0.873	0.911	1.02
* Slowest input					

Switching characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.289	1.94
t_{PHL}		0.254	1.47

Delay coefficients

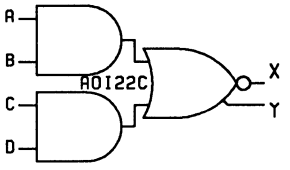
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.524	4.31	0.351	2.73

Rise/Fall time coefficients for the next cell

2–2 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.055
B: 0.056
C: 0.055
D: 0.054 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.284 M_{CHL} = 0.156
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 8.9 grids high



$X = \overline{(A \cdot B) + (C \cdot D)}$

$Y = (A \cdot B) + (C \cdot D)$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.672	1.27	1.33	1.49
t_{PHL}		0.511	0.965	1.01	1.13
t_{PLH}	*IN to Y**	1.05	1.99	2.08	2.34
t_{PHL}		1.22	2.31	2.41	2.71

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.357	1.96
t_{PHL}		0.299	1.47
t_{PLH}	X to Y	0.136	2.17
t_{PHL}		0.163	2.23

Delay coefficients

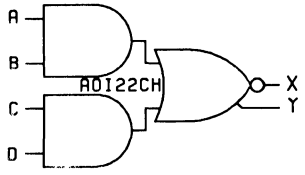
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.680	4.40	0.470	2.72
Y	0.186	4.21	0.196	3.21

Rise/Fall time coefficients for the next cell

2–2 AND–OR–Invert with Complementary Outputs (High Drive)

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A, B: 0.099
C, D: 0.096 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.244 M_{CHL} = 0.184
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.0 grids wide, 9.9 grids high



$X = \overline{(A \cdot B) + (C \cdot D)}$

$Y = (A \cdot B) + (C \cdot D)$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.562	1.07	1.11	1.25
t_{PHL}		0.586	1.11	1.15	1.30
t_{PLH}	*IN to Y**	0.996	1.89	1.97	2.21
t_{PHL}		0.935	1.78	1.85	2.08

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.361	0.987
t_{PHL}		0.415	0.940
t_{PLH}	X to Y	0.134	0.860
t_{PHL}		0.121	0.940

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

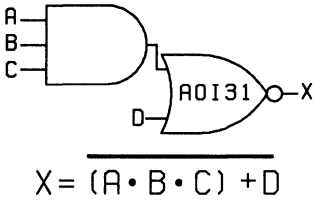
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.725	2.14	0.680	1.76
Y	0.218	1.37	0.172	1.15

Rise/Fall time coefficients for the next cell

AOI31

3–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A, B: 0.056
C: 0.055
D: 0.046 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.240 M_{CHL} = 0.270
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.727	1.37	1.43	1.61
t_{PHL}		0.529	1.01	1.05	1.18
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.364	2.62
t_{PHL}		0.231	1.85

Delay coefficients

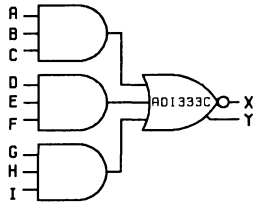
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.714	5.81	0.264	3.85

Rise/Fall time coefficients for the next cell

3–3–3 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: A, B, C, D, E, F: 0.066
G, H, I: 0.064 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.108 M_{CHL} = 0.215
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 13.0 grids wide, 10.4 grids high



$$X = \overline{(A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)}$$

$$Y = (A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)$$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X**	2.14	4.01	4.18	4.69
t_{PHL}		2.20	4.14	4.31	4.84
t_{PLH}	*IN to Y	1.67	3.13	3.26	3.66
t_{PHL}		1.72	3.23	3.37	3.78

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	Y to X	0.107	2.10
t_{PHL}		0.115	2.03
t_{PLH}	*IN to Y	1.37	2.53
t_{PHL}		1.37	2.66

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

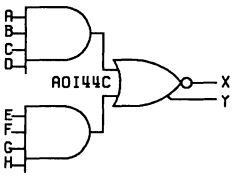
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.194	4.21	0.169	3.11
Y	0.673	4.12	0.652	3.25

Rise/Fall time coefficients for the next cell

AOI44C

4–4 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H
Outputs: X, Y
Input Cap.: A: 0.035
B, C: 0.036
D: 0.037
E: 0.034
F, G: 0.036
H: 0.037 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.233 M_{CHL} = 0.212
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 21.0 grids wide, 9.4 grids high



$$X = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$$

$$Y = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.20	2.26	2.36	2.65
t_{PHL}		1.33	2.50	2.61	2.93
t_{PLH}	*IN to Y	1.54	2.89	3.02	3.39
t_{PHL}		1.33	2.50	2.61	2.93
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.704	4.00
t_{PHL}		1.01	2.36
t_{PLH}	A,B,C,D,E,F,G,H to Y	1.24	2.07
t_{PHL}		1.02	2.21

Delay coefficients

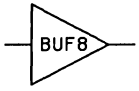
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.340	8.44	0.391	3.10
Y	0.181	4.23	0.204	3.18

Rise/Fall time coefficients for the next cell

Noninverting Buffer (8X Drive)

BUF8 has 8 times the drive of an SBUF.



Inputs: A
Outputs: X
Input Cap.: A: 0.059 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.171 M_{CHL} = 0.166
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 10.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.517	0.977	1.02	1.14
t_{PHL}		0.581	1.10	1.14	1.28

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.409	0.360
t_{PHL}		0.473	0.380

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

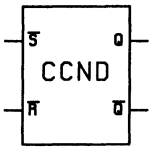
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.203	0.407	0.204	0.400

Rise/Fall time coefficients for the next cell

Cross–Coupled NAND Latch

CCND is very sensitive to negative spikes on SB or RB.

Inputs: SB, RB
Outputs: Q, QB
Input Cap.: All: 0.042 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.280 M_{CHL} = 0.275
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.4 grids high



FUNCTION TABLE

SB	RB	Q	QB
L	L	*	*
L	H	H	L
H	L	L	H
H	H	Q_o	QB_o

*Both outputs will remain high as long as SB and RB remain low, but the output states are unpredictable if SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	RB to Q	0.881	1.66	1.74	1.95
t_{PLH}	RB to QB	0.504	0.960	1.00	1.13
t_{PHL}		0.416	0.796	0.831	0.935
t_{PLH}	SB to Q	0.506	0.965	1.01	1.13
t_{PHL}		0.416	0.796	0.831	0.935
t_{PHL}	SB to QB	0.884	1.67	1.74	1.96

Timing characteristics

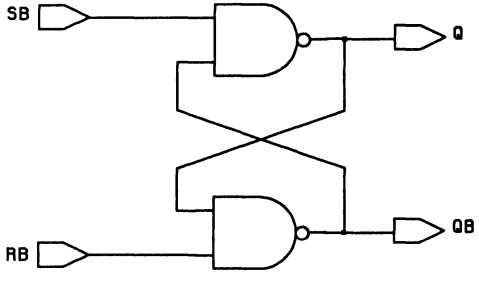
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	RB to Q	0.375	3.91
t_{PLH}	RB to QB	0.179	2.07
t_{PHL}		0.150	1.51
t_{PLH}	SB to Q	0.180	2.09
t_{PHL}		0.150	1.51
t_{PHL}	SB to QB	0.378	3.91

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.338	4.49	0.224	3.05
QB	0.334	4.47	0.224	3.04

Rise/Fall time coefficients for the next cell

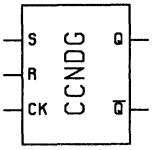


Functional diagram: CCND

Gated R/S Flip–Flop

CCNDG is very sensitive to positive spikes on S and R while CK is high.

Inputs: S, CK, R
Outputs: Q, QB
Input Cap.: S: 0.035
CK: 0.073
R: 0.035 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.094 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.0 grids wide, 8.4 grids high



FUNCTION TABLE

CK	S	R	Q	QB
L	X	X	Q_o	QB_o
H	L	L	Q_o	QB_o
H	L	H	L	H
H	H	L	H	L
H	H	H	*	*

*Both outputs will remain high as long as S, R, and CK are high, but the output states are unpredictable if S and R go low simultaneously or if CK goes low while S and R are still high.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	R to Q	1.30	2.43	2.53	2.84
t_{PLH}	R to QB	0.702	1.32	1.37	1.54
t_{PHL}		0.739	1.38	1.44	1.61
t_{PLH}	S to Q	0.698	1.31	1.37	1.53
t_{PHL}		0.735	1.37	1.43	1.60
t_{PHL}	S to QB	1.29	2.41	2.52	2.82
t_{PLH}	CK to Q	0.709	1.33	1.39	1.56
t_{PHL}		1.31	2.45	2.56	2.87
t_{PLH}	CK to QB	0.720	1.35	1.41	1.58
t_{PHL}		1.30	2.43	2.53	2.84

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	R to Q	0.748	5.51
t_{PLH}	R to QB	0.453	2.10
t_{PHL}		0.443	2.96

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	S to Q	0.449	2.10
t_{PHL}		0.440	2.95
t_{PHL}	S to QB	0.740	5.53
t_{PLH}	CK to Q	0.458	2.11
t_{PHL}		0.759	5.55
t_{PLH}	CK to QB	0.467	2.13
t_{PHL}		0.750	5.53

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

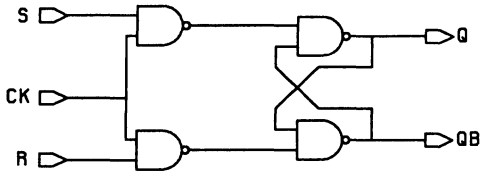
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.369	4.20	0.387	5.82
QB	0.373	4.19	0.387	5.82

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time S to CK	2.35	1.38	0.843
t_{su}	Setup Time R to CK	1.77	1.04	0.635
t_h	Hold Time CK to S	1.35	0.790	0.483
t_h	Hold Time CK to R	2.94	1.72	1.05
t_{pwh}	Pulse Width (high) CK	4.13	2.42	1.48

Timing requirements

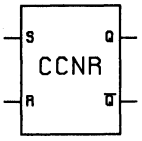


Functional diagram: CCNDG

Cross–Coupled NOR Latch

CCNR is very sensitive to positive spikes on S and R.

Inputs: S, R
Outputs: Q, QB
Input Cap.: All: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.492 M_{CHL} = 0.223
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 7.9 grids high



FUNCTION TABLE

S	R	Q	QB
L	L	Q_o	QB_o
L	H	L	H
H	L	H	L
H	H	*	*

*Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	R to Q	0.867	1.65	1.72	1.94
t_{PHL}		0.434	0.826	0.862	0.969
t_{PLH}	R to QB	1.33	2.51	2.62	2.95
t_{PLH}	S to Q	1.33	2.51	2.62	2.95
t_{PLH}	S to QB	0.867	1.65	1.72	1.94
t_{PHL}		0.434	0.826	0.862	0.969

Timing characteristics

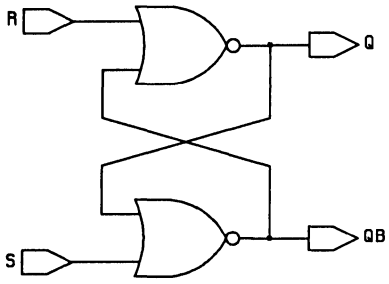
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	R to Q	0.289	3.71
t_{PHL}		0.150	1.91
t_{PLH}	R to QB	0.518	6.03
t_{PLH}	S to Q	0.521	6.01
t_{PLH}	S to QB	0.289	3.71
t_{PHL}		0.150	1.91

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.597	8.62	0.191	3.38
QB	0.596	8.62	0.191	3.38

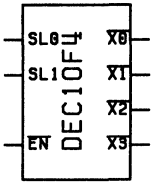
Rise/Fall time coefficients for the next cell



Functional diagram: CCNR

1–of–4 Decoder

Inputs: SL0, SL1, ENB
Outputs: X0B, X1B, X2B, X3B
Input Cap.: SL0: 0.123
SL1: 0.125
ENB: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.331 M_{CHL} = 0.188
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 22.0 grids wide, 11.4 grids high



FUNCTION TABLE

SL0	SL1	ENB	X0B	X1B	X2B	X3B
X	X	H	H	H	H	H
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*SL to XnB	0.960	1.81	1.89	2.13
t_{PHL}		1.19	2.23	2.32	2.61
t_{PLH}	*ENB to XnB	0.890	1.68	1.76	1.97
t_{PHL}		1.11	2.08	2.17	2.44
* SL timing applies to both SL0 and SL1. XnB represents any output.					

Timing characteristics

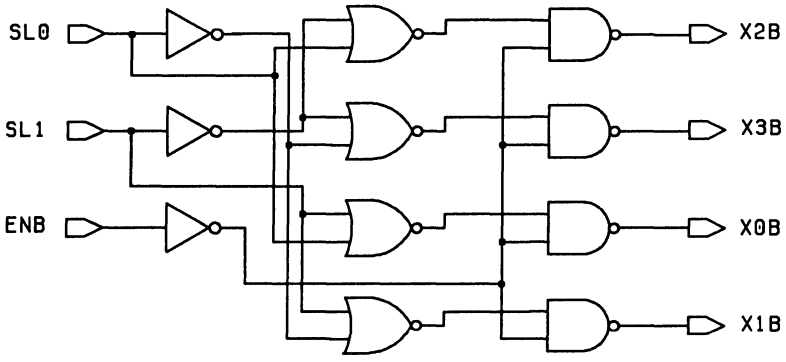
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*SL to XnB	0.666	1.55
t_{PHL}		0.795	3.13
t_{PLH}	*ENB to XnB	0.592	1.59
t_{PHL}		0.730	2.99

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X0B	0.254	2.71	0.282	5.26
X1B	0.254	2.71	0.282	5.26
X2B	0.254	2.71	0.282	5.26
X3B	0.254	2.71	0.282	5.26

Rise/Fall time coefficients for the next cell

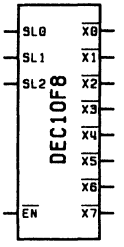


Functional diagram: DEC1OF4

DEC1OF8

1–of–8 Decoder

Inputs: SL0, SL1, SL2, ENB
Outputs: X0B, X1B, X2B, X3B, X4B, X5B, X6B, X7B
Input Cap.: SL0, SL1: 0.034
SL2: 0.033
ENB: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.182 M_{CHL} = 0.192
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 42.0 grids wide, 13.4 grids high



FUNCTION TABLE

SL0	SL1	SL2	ENB	X0B	X1B	X2B	X3B	X4B	X5B	X6B	X7B
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*SL to XnB	1.82	3.41	3.55	3.98
t_{PHL}		1.97	3.69	3.85	4.32
t_{PLH}	SL2 to XnB	0.954	1.79	1.87	2.10
t_{PHL}		1.09	2.05	2.14	2.40
t_{PLH}	SL2 to X4B,X5B,X6B,X7B	1.53	2.87	3.00	3.36
t_{PHL}		1.54	2.89	3.02	3.39
* SL timing applies to SL0, SL1 and ENB. XnB represents any output.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*SL to XnB	1.52	2.18
t_{PHL}		1.56	3.31
t_{PLH}	SL2 to XnB	0.659	2.19
t_{PHL}		0.706	3.05

Delay coefficients (Sheet 1 of 2)

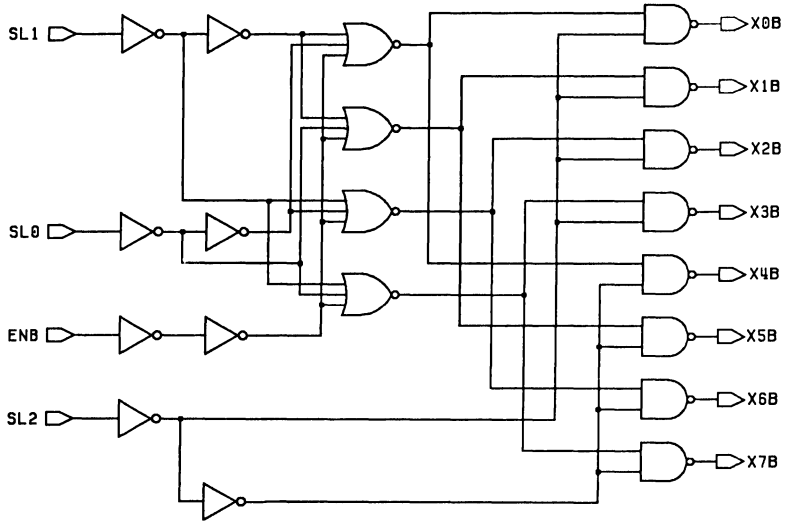
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	SL2 to X4B,X5B,X6B,X7B	1.25	2.09
t_{PHL}		1.16	3.03

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X0B	0.316	4.08	0.337	5.20
X1B	0.316	4.08	0.337	5.20
X2B	0.316	4.08	0.337	5.20
X3B	0.316	4.08	0.337	5.20
X4B	0.308	4.04	0.314	5.20
X5B	0.308	4.04	0.314	5.20
X6B	0.308	4.04	0.314	5.20
X7B	0.308	4.04	0.314	5.20

Rise/Fall time coefficients for the next cell

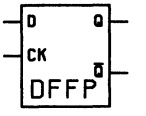


Functional diagram: DEC1OF8

DFFP

D Flip–Flop, Positive Edge Triggered

DFFP is a fully static D-type flip-flop. It is positive edge triggered with respect to the single phase clock input (CK). For a faster version of this cell, see DFFPF.



Inputs: D, CK
Outputs: Q, QB
Input Cap.: D: 0.036
CK: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.200 M_{CHL} = 0.211
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.0 grids wide, 10.4 grids high

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.04	1.96	2.04	2.29
t_{PHL}		1.25	2.35	2.45	2.75
t_{PLH}	*CK to QB	1.91	3.59	3.74	4.20
t_{PHL}		1.84	3.46	3.61	4.06
* The propagation delay from CK to QB depends on the CK to Q delay and rise/fall time. See the Timing Equation application note for more information.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.560	3.97
t_{PHL}		0.853	3.07
t_{PLH}	Q to QB (CK)	0.241	2.09
t_{PHL}		0.252	2.25

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

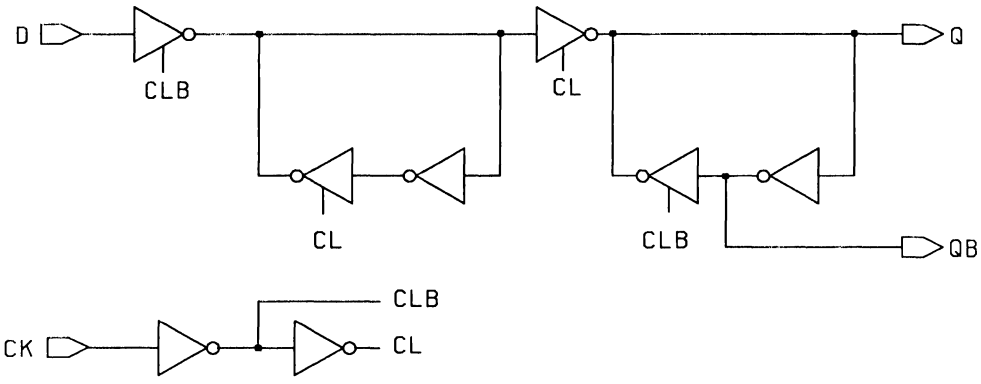
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.737	8.74	0.593	5.19
QB	0.333	4.31	0.319	3.21

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.16	0.680	0.415
t_h	Hold Time CK to D	--0.291	-0.170	-0.104
t_{pwh}	Pulse Width (high) CK	5.10	2.99	1.83
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27

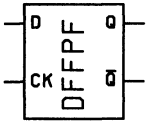
Timing requirements



Functional diagram: DFFP

Fast D Flip–Flop, Positive Edge Triggered

DFFPF is a fully static D-type flip-flop. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q, QB
Input Cap.: D: 0.114
CK: 0.204 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.191 M_{CHL} = 0.212
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 13.0 grids wide, 13.4 grids high

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.389	0.740	0.772	0.868
t_{PHL}		0.598	1.13	1.18	1.33
t_{PLH}	CK to QB	0.402	0.764	0.797	0.896
t_{PHL}		0.627	1.19	1.24	1.39

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.197	1.12
t_{PHL}		0.366	1.43
t_{PLH}	CK to QB	0.219	1.03
t_{PHL}		0.403	1.35

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

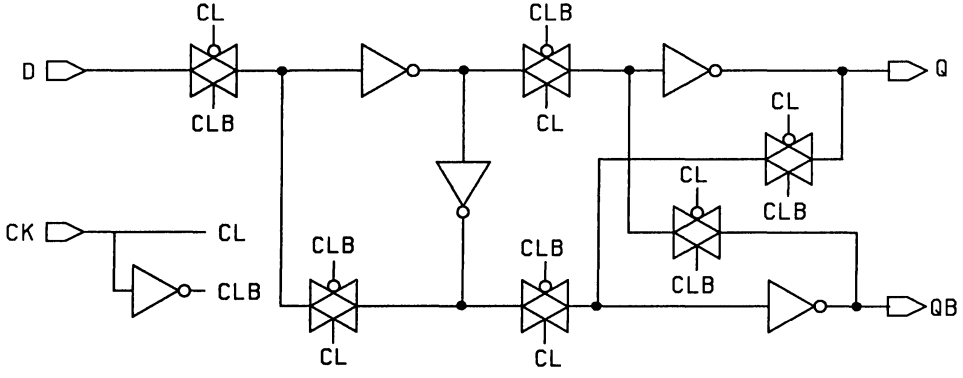
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.165	2.17	0.258	1.60
QB	0.161	2.15	0.259	1.48

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.956	0.560	0.342
t_h	Hold Time CK to D	0.376	0.220	0.135
t_{pwh}	Pulse Width (high) CK	2.95	1.73	1.06
t_{pwl}	Pulse Width (low) CK	2.95	1.73	1.06

Timing requirements

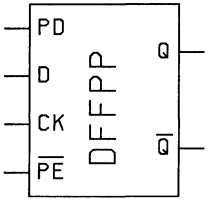


Functional diagram: DFFPF

D Flip–Flop with Parallel Data Input, Positive Edge Triggered

DFFPP is a D–type, positive edge triggered flip–flop with parallel load, and single clock input. Parallel data from PD is transparent when PEB is low.

Inputs: D, PD, PEB, CK
Outputs: Q, QB
Input Cap.: D: 0.066
PD: 0.052
PEB: 0.034
CK: 0.036 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.148 M_{CHL} = 0.235
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 20.0 grids wide, 13.4 grids high



FUNCTION TABLE

D	PD	PEB	CK	Q	QB
X	H	L	X	H	L
X	L	L	X	L	H
H	X	H	↑	H	L
L	X	H	↑	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.07	2.01	2.09	2.35
t_{PHL}		1.29	2.42	2.53	2.84
t_{PLH}	*CK to QB	1.77	3.33	3.47	3.90
t_{PHL}		1.71	3.22	3.36	3.77
t_{PLH}	PD to Q	1.25	2.35	2.45	2.75
t_{PHL}		1.41	2.65	2.77	3.11
t_{PLH}	*PD to QB	1.90	3.57	3.72	4.17
t_{PHL}		1.89	3.55	3.70	4.15
t_{PLH}	PEB to Q	1.69	3.17	3.30	3.70
t_{PHL}		2.26	4.23	4.41	4.95
t_{PLH}	*PEB to QB	2.76	5.18	5.40	6.07
t_{PHL}		2.34	4.39	4.57	5.14

* The propagation delay from PD, PEB, and CK to QB depends on the delay from each pin to the Q output. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.734	2.74
t_{PHL}		1.03	1.65
t_{PLH}	Q to QB (CK)	0.231	1.43
t_{PHL}		0.209	1.23
t_{PLH}	PD to Q	0.929	2.61
t_{PHL}		1.15	1.67
t_{PLH}	Q to QB (PD)	0.268	1.09
t_{PHL}		0.195	1.28
t_{PLH}	PEB to Q	1.36	2.72
t_{PHL}		1.98	1.76
t_{PLH}	Q to QB (PEB)	0.246	1.53
t_{PHL}		0.219	1.16

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.806	5.95	0.539	2.57
QB	0.330	2.93	0.297	1.63

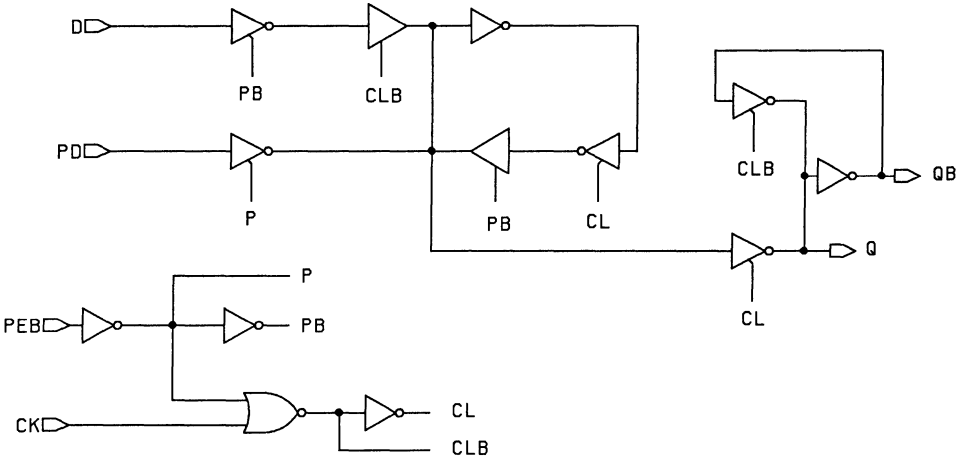
Rise/fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time PD to PEB	1.57	0.920	0.563
t_{su}	Setup Time D to CK	2.35	1.38	0.843
t_h	Hold Time PEB to PD	-0.291	-0.170	-0.104
t_h	Hold Time CK to D	-0.291	-0.170	-0.104
t_{pwh}	Pulse Width (high) CK	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) PEB	4.71	2.76	1.69
t_{pwl}	Pulse Width (low) CK	6.65	3.91	2.38
rt	Recovery Time PEB	5.70	3.34	2.04

Timing requirements

DFFPP

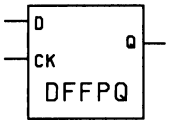


Functional diagram: DFFPP

D Flip–Flop, Positive Edge Triggered

DFFPQ is a fully static D-type flip-flop with only a Q output. It is positive edge triggered with respect to the single phase clock input (CK).

Inputs: D, CK
Outputs: Q
Input Cap.: D: 0.066
CK: 0.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.148 M_{CHL} = 0.165
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.0 grids wide, 9.9 grids high



FUNCTION TABLE

D	CK	Q
L	↑	L
H	↑	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.541	1.02	1.06	1.19
t_{PHL}		0.780	1.47	1.53	1.72

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.324	1.55
t_{PHL}		0.531	1.79

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.222	2.97	0.338	2.19

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.956	0.560	0.342

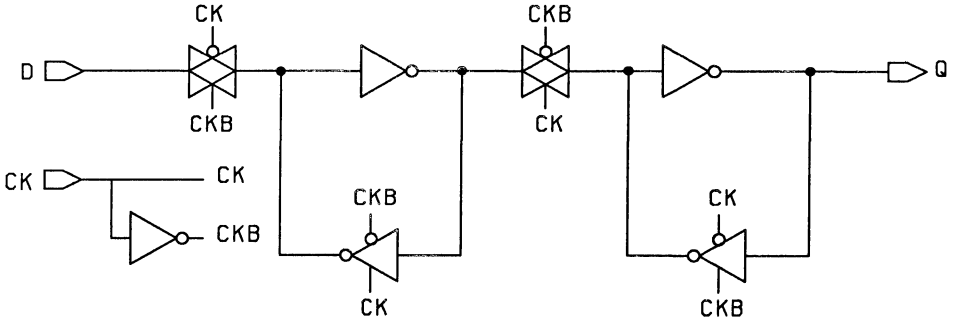
Timing requirements

DFFPQ

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_h	Hold Time CK to D	0.392	0.230	0.141
t_{pwh}	Pulse Width (high) CK	3.14	1.84	1.12
t_{pwl}	Pulse Width (low) CK	4.91	2.88	1.76

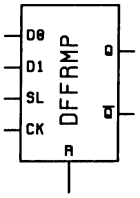
Timing requirements [continued]



Functional diagram: DFFPQ

D Flip–Flop with Reset and Multiplexed Inputs, Positive Edge Triggered

DFFRMP is a fully static D-type edge triggered flip-flop with a multiplexed D input. Selection of D0 or D1 is controlled by SL. It is positive edge triggered with respect to the single clock input CK. R is asynchronous and active high.



Inputs: R, D0, D1, SL, CK
Outputs: Q, QB
Input Cap.: R: 0.034
D0: 0.056
D1: 0.059
SL: 0.034
CK: 0.044 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.256 M_{CHL} = 0.287
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 24.0 grids wide, 12.4 grids high

FUNCTION TABLE

D0	D1	SL	R	CK	Q	QB
X	X	X	H	X	L	H
H	X	H	L	↑	H	L
L	X	H	L	↑	L	H
X	H	L	L	↑	H	L
X	L	L	L	↑	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.957	1.80	1.88	2.11
t_{PHL}		1.28	2.42	2.52	2.83
t_{PLH}	*CK to QB	1.90	3.59	3.74	4.21
t_{PHL}		1.72	3.24	3.38	3.80
t_{PHL}	*R to Q	1.81	3.41	3.56	4.00
t_{PLH}	R to QB	0.994	1.87	1.95	2.19

* The propagation delay from CK to QB depends on the CK to Q delay and rise/fall time. Also, the delay from R to Q depends on the R to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.655	1.95
t_{PHL}		0.989	1.75
t_{PLH}	Q to QB (CK)	0.287	1.39
t_{PHL}		0.282	1.66
t_{PHL}	QB to Q (R)	0.351	1.49
t_{PLH}	R to QB	0.662	2.25

Delay coefficients

DFFRMP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

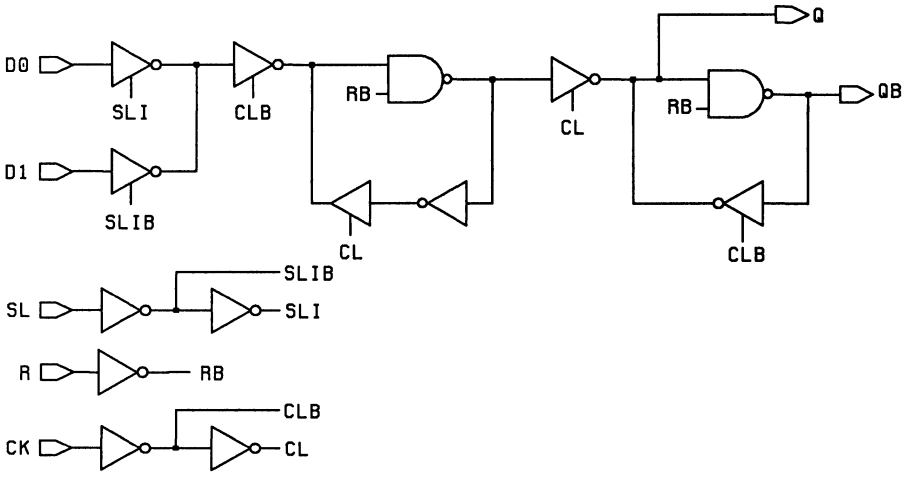
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.744	4.23	0.582	2.49
QB	0.744	4.23	0.582	2.49

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D0 to CK	2.56	1.50	0.917
t_{su}	Setup Time D1 to CK	2.56	1.50	0.917
t_{su}	Setup Time SL to CK	2.95	1.73	1.06
t_h	Hold Time CK to D0	-0.871	-0.510	-0.311
t_h	Hold Time CK to D1	-0.871	-0.510	-0.311
t_h	Hold Time CK to SL	-1.621	-0.950	-0.581
t_{pwh}	Pulse Width (high) R	3.74	2.19	1.34
t_{pwh}	Pulse Width (high) CK	4.52	2.65	1.62
t_{pwl}	Pulse Width (low) CK	4.32	2.53	1.55
rt	Recovery Time R	1.57	0.920	0.563

Timing requirements

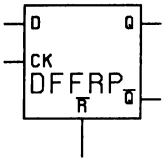


Functional diagram: DFFRMP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRP is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low. For a faster version of this cell, see DFFRPF.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.116
D: 0.043
CK: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.170 M_{CHL} = 0.167
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 15.0 grids wide, 11.4 grids high



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.988	1.86	1.94	2.17
t_{PHL}		1.13	2.12	2.21	2.48
t_{PLH}	*CK to QB	1.74	3.27	3.41	3.83
t_{PHL}		1.61	3.02	3.15	3.54
t_{PHL}	*RB to Q	1.13	2.13	2.22	2.49
t_{PLH}	RB to QB	0.559	1.06	1.10	1.24

* The propagation delay from CK to QB depends on the CK to Q delay and rise/fall time. Also, the delay from RB to Q depends on the RB to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.656	2.61
t_{PHL}		0.892	1.65
t_{PLH}	Q to QB (CK)	0.293	2.13
t_{PHL}		0.236	1.72
t_{PHL}	QB to Q (RB)	0.289	1.45
t_{PLH}	RB to QB	0.270	2.18

Delay coefficients

DFFRP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

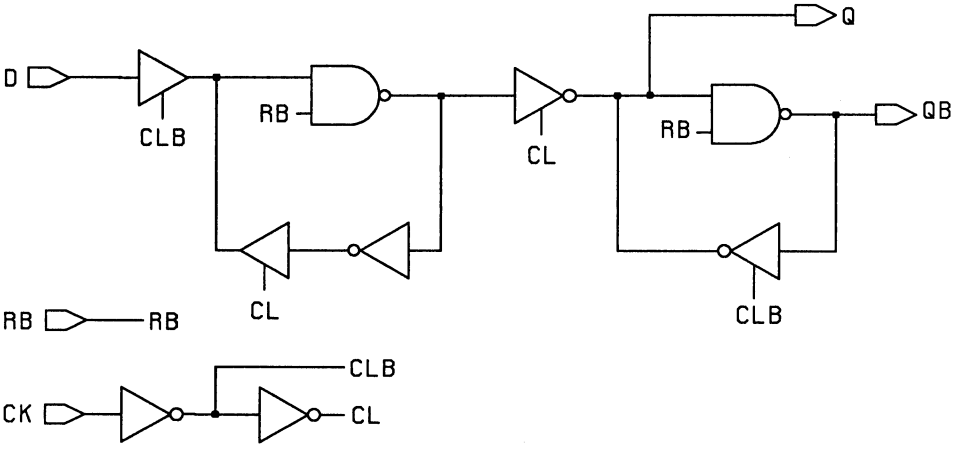
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.742	5.90	0.440	2.69
QB	0.435	4.39	0.368	2.67

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.38	0.810	0.495
t_h	Hold Time CK to D	−0.153	−0.090	−0.055
t_{pwh}	Pulse Width (high) CK	4.71	2.76	1.69
t_{pwl}	Pulse Width (low) RB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CK	4.52	2.65	1.62
rt	Recovery Time RB	0.956	0.560	0.342

Timing requirements

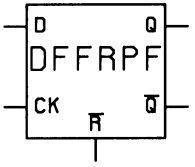


Functional diagram: DFFRP

Fast D Flip–Flop with Reset, Positive Edge Triggered

DFFRPF is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.188
D: 0.121
CK: 0.207 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.263 M_{CHL} = 0.321
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 18.0 grids wide, 13.4 grids high



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.541	1.03	1.07	1.21
t_{PHL}		0.681	1.29	1.35	1.52
t_{PLH}	CK to QB	0.640	1.21	1.26	1.42
t_{PHL}		0.586	1.12	1.16	1.31
t_{PHL}	RB to Q	0.670	1.27	1.33	1.49
t_{PLH}	RB to QB	0.879	1.66	1.73	1.94

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.288	1.43
t_{PHL}		0.416	1.30
t_{PLH}	CK to QB	0.306	2.23
t_{PHL}		0.312	1.39
t_{PHL}	RB to Q	0.428	1.07
t_{PLH}	RB to QB	0.555	2.13

Delay coefficients

DFFRPF

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

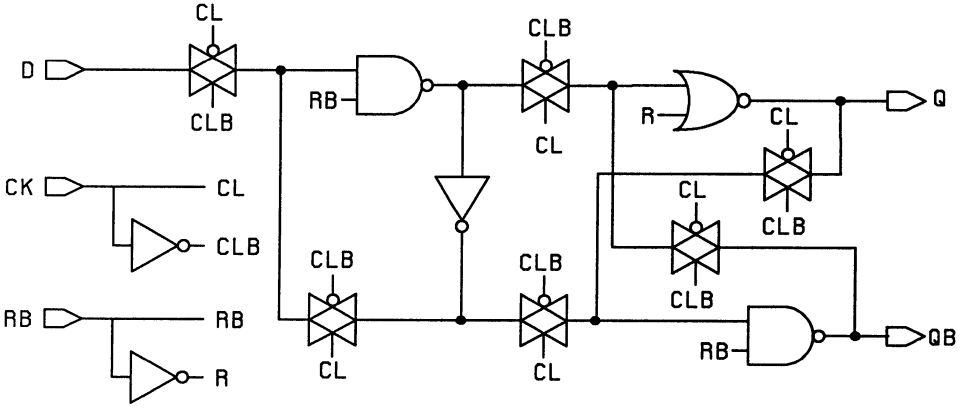
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.313	3.26	0.256	1.79
QB	0.242	4.47	0.197	1.93

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.16	0.680	0.415
t_h	Hold Time CK to D	0.376	0.220	0.135
t_{pwh}	Pulse Width (high) CK	2.95	1.73	1.06
t_{pwl}	Pulse Width (low) RB	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) CK	3.35	1.96	1.20
rt	Recovery Time RB	0.768	0.450	0.275

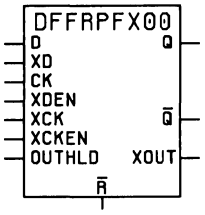
Timing requirements



Functional diagram: DFFRPF

Fast D Flip–Flop, Positive Edge Triggered, with Multiplexed Data and Clock, with Reset Disable

DFFRPFX00 is a fully static D–type, positive edge triggered flip–flop with multiplexed data and clock inputs and an output hold latch. This cell is appropriate for use in internal scan test applications. It is positive edge triggered with respect to CK and XCK. The output hold latch holds data when OUTHLD is high and is transparent when OUTHLD is low. (See functional diagram.) RB is asynchronous and active low unless XDEN is high, in which case RB is disabled.



Inputs: RB, D, CK, XD, XDEN, XCK, XCKEN, OUTHLD
Outputs: Q, QB, XOUT
Input Cap.: RB: 0.043
D: 0.070
CK: 0.071
XD: 0.069
XDEN: 0.164
XCK: 0.069
XCKEN: 0.118
OUTHLD: 0.116 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.281 M_{CHL} = 0.266
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 38.0 grids wide, 13.4 grids high

RB	D	CK	XD	XDEN	XCK	XCKEN	OUTHLD	Q	QB	XOUT
H	D	↑	X	L	X	L	L	D	DB	D
X	X	↑	XD	H	X	L	L	XD	XDB	XD
H	D	↑	X	L	X	L	H	Qo	QBo	D
X	X	↑	XD	H	X	L	H	Qo	QBo	XD
L	X	X	X	L	X	X	X	L	H	L
H	D	X	X	L	↑	H	L	D	DB	D
X	X	X	XD	H	↑	H	L	XD	XDB	XD
H	D	X	X	L	↑	H	H	Qo	QBo	D
X	X	X	XD	H	↑	H	H	Qo	QBo	XD

Function table

DFFRPFX00

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.76	3.30	3.44	3.86
t_{PHL}		1.57	2.95	3.07	3.45
t_{PLH}	CK to QB	1.83	3.44	3.59	4.03
t_{PHL}		1.92	3.60	3.75	4.21
t_{PLH}	CK to XOUT	1.64	3.08	3.21	3.61
t_{PHL}		1.33	2.50	2.60	2.92
t_{PLH}	XCK to Q	2.05	3.86	4.02	4.51
t_{PHL}		1.87	3.51	3.66	4.11
t_{PLH}	XCK to QB	2.13	4.00	4.17	4.68
t_{PHL}		2.22	4.15	4.33	4.86
t_{PLH}	XCK to XOUT	1.94	3.64	3.79	4.26
t_{PHL}		1.63	3.07	3.20	3.59
t_{PLH}	XCKEN to Q	1.96	3.68	3.84	4.31
t_{PHL}		1.77	3.33	3.47	3.90
t_{PLH}	XCKEN to QB	2.04	3.82	3.98	4.47
t_{PHL}		2.12	3.98	4.15	4.66
t_{PLH}	XCKEN to XOUT	1.85	3.47	3.62	4.06
t_{PHL}		1.53	2.88	3.01	3.37
t_{PHL}	XDEN to Q	1.71	3.21	3.35	3.76
t_{PLH}	XDEN to QB	1.23	2.32	2.42	2.72
t_{PHL}	XDEN to XOUT	1.46	2.75	2.87	3.22
t_{PHL}	RB to Q	1.69	3.18	3.31	3.72
t_{PLH}	RB to QB	1.22	2.29	2.39	2.69
t_{PHL}	RB to XOUT	1.51	2.84	2.96	3.32
t_{PLH}	OUTHLD to Q	0.717	1.36	1.42	1.59
t_{PHL}		0.672	1.27	1.33	1.49
t_{PLH}	OUTHLD to QB	0.933	1.76	1.84	2.06
t_{PHL}		0.876	1.65	1.72	1.94

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.39	2.49
t_{PHL}		1.21	2.49
t_{PLH}	CK to QB	1.51	1.99
t_{PHL}		1.65	1.51
t_{PLH}	CK to XOUT	1.35	1.69
t_{PHL}		1.08	1.33
t_{PLH}	XCK to Q	1.68	2.55
t_{PHL}		1.51	2.50
t_{PLH}	XCK to QB	1.81	2.02
t_{PHL}		1.95	1.55
t_{PLH}	XCK to XOUT	1.64	1.75
t_{PHL}		1.39	1.35
t_{PLH}	XCKEN to Q	1.59	2.57

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		1.41	2.49
t_{PLH}	XCKEN to QB	1.72	2.03
t_{PHL}		1.85	1.59
t_{PLH}	XCKEN to XOUT	1.55	1.78
t_{PHL}		1.29	1.33
t_{PHL}	XDEN to Q	1.35	2.53
t_{PLH}	XDEN to QB	0.879	2.35
t_{PHL}	XDEN to XOUT	1.22	1.36
t_{PHL}	RB to Q	1.33	2.53
t_{PLH}	RB to QB	0.865	2.35
t_{PHL}	RB to XOUT	1.26	1.37
t_{PLH}	OUTHLD to Q	0.350	2.49
t_{PHL}		0.315	2.45
t_{PLH}	OUTHLD to QB	0.602	2.13
t_{PHL}		0.614	1.50

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.304	4.31	0.280	3.25
QB	0.249	4.36	0.210	2.60
XOUT	0.312	2.93	0.204	1.69

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.02	0.600	0.367
t_{su}	Setup Time XD to CK	1.77	1.04	0.635
t_{su}	Setup Time XDEN to CK	1.77	1.04	0.635
t_{su}	Setup Time D to XCK	0.512	0.300	0.183
t_{su}	Setup Time XD to XCK	1.19	0.700	0.428
t_{su}	Setup Time XDEN to XCK	1.19	0.700	0.428
t_{su}	Setup Time D to XCKEN	0.683	0.400	0.244
t_{su}	Setup Time CK to XCKEN	2.35	1.38	0.843
t_{su}	Setup Time XD to XCKEN	1.38	0.810	0.495
t_{su}	Setup Time XDEN to XCKEN	1.38	0.810	0.495
t_{su}	Setup Time XCK to XCKEN	2.17	1.27	0.776
t_{su}	Setup Time CK to OUTHLD	2.95	1.73	1.06
t_{su}	Setup Time XCK to OUTHLD	3.74	2.19	1.34
t_{su}	Setup Time XCKEN to OUTHLD	3.93	2.30	1.41
t_h	Hold Time CK to D	0.171	0.100	0.061
t_h	Hold Time CK to XD	−0.444	−0.260	−0.159

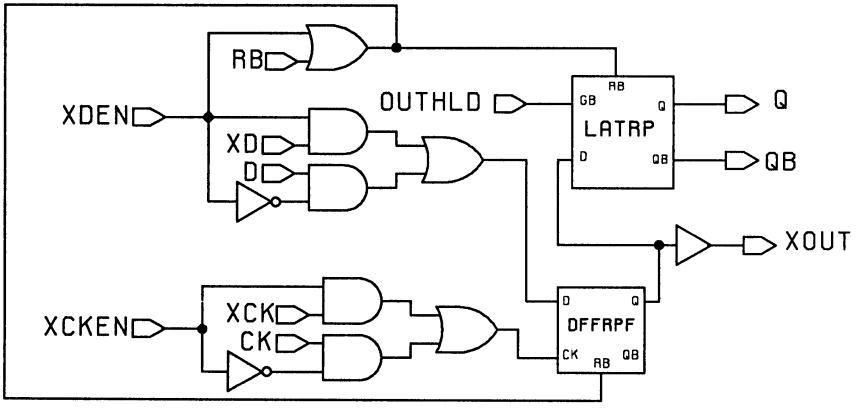
Timing requirements (Sheet 1 of 2)

DFFRPFX00

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_h	Hold Time CK to XDEN	−0.444	−0.260	−0.159
t_h	Hold Time XCK to D	0.683	0.400	0.244
t_h	Hold Time XCK to XD	−0.153	−0.090	−0.055
t_h	Hold Time XCK to XDEN	−0.153	−0.090	−0.055
t_h	Hold Time XCKEN to D	0.512	0.300	0.183
t_h	Hold Time XCKEN to CK	2.35	1.38	0.843
t_h	Hold Time XCKEN to XD	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XDEN	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XCK	2.17	1.27	0.776
t_h	Hold Time OUTHLD to CK	−1.775	−1.040	−0.635
t_h	Hold Time OUTHLD to XCK	−2.372	−1.390	−0.850
t_h	Hold Time OUTHLD to XCKEN	−2.525	−1.480	−0.904
t_{pwh}	Pulse Width (high) CK	3.35	1.96	1.20
t_{pwh}	Pulse Width (high) XCK	3.93	2.30	1.41
t_{pwh}	Pulse Width (high) XCKEN	3.74	2.19	1.34
t_{pwl}	Pulse Width (low) RB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) XDEN	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) XCK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) XCKEN	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) OUTHLD	2.95	1.73	1.06
rt	Recovery Time RB to CK	−1.195	−0.700	−0.428
rt	Recovery Time XDEN to CK	1.57	0.920	0.563
rt	Recovery Time RB to XCK	−1.963	−1.150	−0.702
rt	Recovery Time XDEN to XCK	0.989	0.580	0.354
rt	Recovery Time RB to XCKEN	−1.963	−1.150	−0.702
rt	Recovery Time XDEN to XCKEN	1.18	0.690	0.422

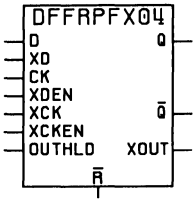
Timing requirements (Sheet 2 of 2)



Functional diagram: DFFRPFX00

Fast High Drive D Flip–Flop, Positive Edge Triggered, with Multiplexed Data and Clock, with Reset Disable

DFFRPFX04 is a fully static D-type, positive edge triggered flip-flop with multiplexed data and clock inputs and an output hold latch. This cell is appropriate for use in internal scan test applications. It is positive edge triggered with respect to CK and XCK. The output hold latch holds data when OUTHLD is high and is transparent when OUTHLD is low. (See functional diagram.) RB is asynchronous and active low unless XDEN is high, in which case RB is disabled.



Inputs: RB, D, CK, XD, XDEN, XCK, XCKEN, OUTHLD
Outputs: Q, QB, XOUT
Input Cap.: RB: 0.043
D: 0.070
CK: 0.071
XD: 0.069
XDEN: 0.164
XCK: 0.069
XCKEN: 0.118
OUTHLD: 0.116 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.200 M_{CHL} = 0.179
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 38.0 grids wide, 13.4 grids high

RB	D	CK	XD	XDEN	XCK	XCKEN	OUTHLD	Q	QB	XOUT
H	D	↑	X	L	X	L	L	D	DB	D
X	X	↑	XD	H	X	L	L	XD	XDB	XD
H	D	↑	X	L	X	L	H	Qo	QBo	D
X	X	↑	XD	H	X	L	H	Qo	QBo	XD
L	X	X	X	L	X	X	X	L	H	L
H	D	X	X	L	↑	H	L	D	DB	D
X	X	X	XD	H	↑	H	L	XD	XDB	XD
H	D	X	X	L	↑	H	H	Qo	QBo	D
X	X	X	XD	H	↑	H	H	Qo	QBo	XD

Function table

DFFRPFX04

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.42	2.66	2.78	3.12
t_{PHL}		1.45	2.72	2.83	3.18
t_{PLH}	CK to QB	1.80	3.37	3.51	3.94
t_{PHL}		1.63	3.06	3.19	3.58
t_{PLH}	CK to XOUT	1.37	2.57	2.68	3.01
t_{PHL}		1.42	2.66	2.77	3.11
t_{PLH}	XCK to Q	1.72	3.23	3.36	3.78
t_{PHL}		1.75	3.29	3.42	3.84
t_{PLH}	XCK to QB	2.10	3.94	4.11	4.61
t_{PHL}		1.93	3.62	3.77	4.23
t_{PLH}	XCK to XOUT	1.67	3.13	3.27	3.67
t_{PHL}		1.72	3.23	3.37	3.78
t_{PLH}	XCKEN to Q	1.62	3.04	3.17	3.56
t_{PHL}		1.66	3.10	3.24	3.63
t_{PLH}	XCKEN to QB	2.01	3.76	3.92	4.40
t_{PHL}		1.83	3.43	3.58	4.02
t_{PLH}	XCKEN to XOUT	1.57	2.94	3.07	3.44
t_{PHL}		1.62	3.04	3.17	3.56
t_{PHL}	XDEN to Q	1.66	3.11	3.24	3.64
t_{PLH}	XDEN to QB	1.22	2.30	2.39	2.69
t_{PHL}	XDEN to XOUT	1.63	3.06	3.19	3.58
t_{PHL}	RB to Q	1.64	3.08	3.21	3.60
t_{PLH}	RB to QB	1.21	2.27	2.36	2.65
t_{PHL}	RB to XOUT	1.71	3.21	3.35	3.76
t_{PLH}	OUTHLD to Q	0.574	1.08	1.13	1.27
t_{PHL}		0.531	1.00	1.05	1.18
t_{PLH}	OUTHLD to QB	0.861	1.62	1.69	1.90
t_{PHL}		0.785	1.48	1.54	1.73

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.21	1.26
t_{PHL}		1.25	1.20
t_{PLH}	CK to QB	1.62	0.920
t_{PHL}		1.48	0.767
t_{PLH}	CK to XOUT	1.12	1.67
t_{PHL}		1.20	1.41
t_{PLH}	XCK to Q	1.51	1.25
t_{PHL}		1.56	1.22
t_{PLH}	XCK to QB	1.92	0.933
t_{PHL}		1.78	0.780
t_{PLH}	XCK to XOUT	1.42	1.65
t_{PHL}		1.50	1.43
t_{PLH}	XCKEN to Q	1.41	1.23

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		1.46	1.19
t_{PLH}	XCKEN to QB	1.83	0.887
t_{PHL}		1.68	0.733
t_{PLH}	XCKEN to XOUT	1.32	1.63
t_{PHL}		1.41	1.39
t_{PHL}	XDEN to Q	1.47	1.19
t_{PLH}	XDEN to QB	0.987	1.51
t_{PHL}	XDEN to XOUT	1.41	1.43
t_{PHL}	RB to Q	1.45	1.21
t_{PLH}	RB to QB	0.972	1.51
t_{PHL}	RB to XOUT	1.49	1.45
t_{PLH}	OUTHLD to Q	0.363	1.27
t_{PHL}		0.347	1.09
t_{PLH}	OUTHLD to QB	0.690	0.867
t_{PHL}		0.630	0.800

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.220	2.26	0.267	1.39
QB	0.220	2.15	0.185	1.28
XOUT	0.252	2.95	0.240	1.73

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.02	0.600	0.367
t_{su}	Setup Time XD to CK	1.77	1.04	0.635
t_{su}	Setup Time XDEN to CK	1.96	1.15	0.702
t_{su}	Setup Time D to XCK	0.512	0.300	0.183
t_{su}	Setup Time XD to XCK	1.19	0.700	0.428
t_{su}	Setup Time XDEN to XCK	1.18	0.690	0.422
t_{su}	Setup Time D to XCKEN	0.683	0.400	0.244
t_{su}	Setup Time CK to XCKEN	2.35	1.38	0.843
t_{su}	Setup Time XD to XCKEN	1.38	0.810	0.495
t_{su}	Setup Time XDEN to XCKEN	1.57	0.920	0.563
t_{su}	Setup Time XCK to XCKEN	2.17	1.27	0.776
t_{su}	Setup Time CK to OUTHLD	2.95	1.73	1.06
t_{su}	Setup Time XCK to OUTHLD	3.53	2.07	1.27
t_{su}	Setup Time XCKEN to OUTHLD	3.74	2.19	1.34
t_h	Hold Time CK to D	0.171	0.100	0.061
t_h	Hold Time CK to XD	−0.444	−0.260	−0.159

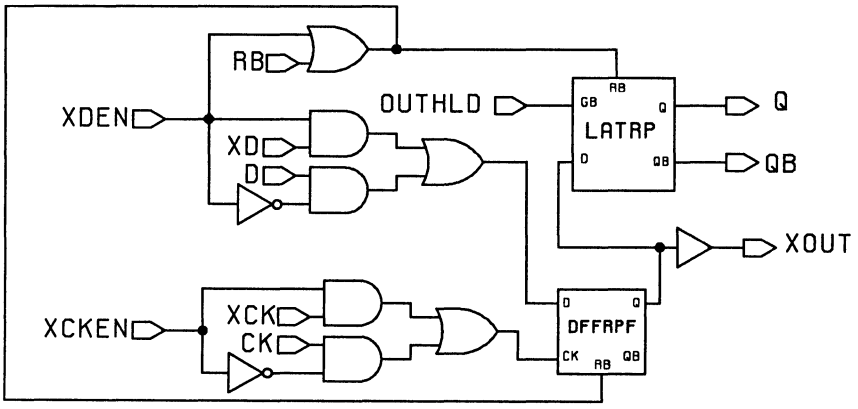
Timing requirements (Sheet 1 of 2)

DFFRPFX04

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_h	Hold Time CK to XDEN	−0.444	−0.260	−0.159
t_h	Hold Time XCK to D	0.512	0.300	0.183
t_h	Hold Time XCK to XD	−0.153	−0.090	−0.055
t_h	Hold Time XCK to XDEN	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to D	0.341	0.200	0.122
t_h	Hold Time XCKEN to CK	2.35	1.38	0.843
t_h	Hold Time XCKEN to XD	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XDEN	−0.153	−0.090	−0.055
t_h	Hold Time XCKEN to XCK	2.17	1.27	0.776
t_h	Hold Time OUTHLD to CK	−1.775	−1.040	−0.635
t_h	Hold Time OUTHLD to XCK	−2.219	−1.300	−0.795
t_h	Hold Time OUTHLD to XCKEN	−2.372	−1.390	−0.850
t_{pwh}	Pulse Width (high) CK	3.14	1.84	1.12
t_{pwh}	Pulse Width (high) XCK	3.74	2.19	1.34
t_{pwh}	Pulse Width (high) XCKEN	3.74	2.19	1.34
t_{pwl}	Pulse Width (low) RB	4.52	2.65	1.62
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) XDEN	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) XCK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) XCKEN	3.35	1.96	1.20
t_{pwl}	Pulse Width (low) OUTHLD	3.14	1.84	1.12
rt	Recovery Time RB to CK	−1.024	−0.600	−0.367
rt	Recovery Time XDEN to CK	1.57	0.920	0.563
rt	Recovery Time RB to XCK	−1.775	−1.040	−0.635
rt	Recovery Time XDEN to XCK	0.989	0.580	0.354
rt	Recovery Time RB to XCKEN	−1.571	−0.920	−0.563
rt	Recovery Time XDEN to XCKEN	1.18	0.690	0.422

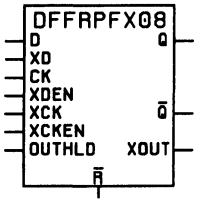
Timing requirements (Sheet 2 of 2)



Functional diagram: DFFRPFX04

Fast D Flip–Flop, Positive Edge Triggered, with Multiplexed Data and Clock, with Reset

DFFRPFX08 is a fully static D-type, positive edge triggered flip-flop with multiplexed data and clock inputs and an output hold latch. This cell is appropriate for use in internal scan test applications. It is positive edge triggered with respect to CK and XCK. The output hold latch holds data when OUTHLD is high and is transparent when OUTHLD is low. (See functional diagram.) RB is asynchronous and active low.



Inputs: RB, D, CK, XD, XDEN, XCK, XCKEN, OUTHLD
Outputs: Q, QB, XOUT
Input Cap.: RB: 0.034
D: 0.070
CK: 0.071
XD: 0.069
XDEN: 0.119
XCK: 0.069
XCKEN: 0.118
OUTHLD: 0.116 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.173 M_{CHL} = 0.165
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 37.0 grids wide, 13.4 grids high

RB	D	CK	XD	XDEN	XCK	XCKEN	OUTHLD	Q	QB	XOUT
H	D	↑	X	L	X	L	L	D	DB	D
H	X	↑	XD	H	X	L	L	XD	XDB	XD
H	D	↑	X	L	X	L	H	Qo	QBo	D
H	X	↑	XD	H	X	L	H	Qo	QBo	XD
L	X	X	X	L	X	X	X	L	H	L
H	D	X	X	L	↑	H	L	D	DB	D
H	X	X	XD	H	↑	H	L	XD	XDB	XD
H	D	X	X	L	↑	H	H	Qo	QBo	D
H	X	X	XD	H	↑	H	H	Qo	QBo	XD

Function table

DFFRPFX08

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.71	3.21	3.35	3.75
t_{PHL}		1.52	2.86	2.98	3.34
t_{PLH}	CK to QB	1.78	3.34	3.48	3.91
t_{PHL}		1.88	3.51	3.66	4.11
t_{PLH}	CK to XOUT	1.60	2.99	3.12	3.50
t_{PHL}		1.29	2.41	2.51	2.82
t_{PLH}	XCK to Q	2.01	3.77	3.93	4.41
t_{PHL}		1.83	3.42	3.57	4.00
t_{PLH}	XCK to QB	2.09	3.91	4.08	4.57
t_{PHL}		2.17	4.07	4.24	4.76
t_{PLH}	XCK to XOUT	1.90	3.55	3.70	4.15
t_{PHL}		1.59	2.98	3.10	3.48
t_{PLH}	XCKEN to Q	1.91	3.58	3.73	4.19
t_{PHL}		1.73	3.24	3.38	3.79
t_{PLH}	XCKEN to QB	1.99	3.73	3.89	4.36
t_{PHL}		2.08	3.89	4.06	4.55
t_{PLH}	XCKEN to XOUT	1.80	3.37	3.51	3.94
t_{PHL}		1.49	2.80	2.91	3.27
t_{PHL}	RB to Q	1.50	2.82	2.94	3.29
t_{PLH}	RB to QB	1.02	1.92	2.00	2.25
t_{PHL}	RB to XOUT	1.32	2.47	2.57	2.89
t_{PLH}	OUTHLD to Q	0.671	1.26	1.32	1.48
t_{PHL}		0.631	1.19	1.24	1.39
t_{PLH}	OUTHLD to QB	0.883	1.66	1.73	1.94
t_{PHL}		0.834	1.57	1.64	1.84

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.37	2.71
t_{PHL}		1.20	2.52
t_{PLH}	CK to QB	1.51	2.03
t_{PHL}		1.64	1.67
t_{PLH}	CK to XOUT	1.33	1.89
t_{PHL}		1.08	1.37
t_{PLH}	XCK to Q	1.68	2.54
t_{PHL}		1.51	2.52
t_{PLH}	XCK to QB	1.81	2.06
t_{PHL}		1.95	1.54
t_{PLH}	XCK to XOUT	1.65	1.76
t_{PHL}		1.38	1.37
t_{PLH}	XCKEN to Q	1.59	2.52
t_{PHL}		1.41	2.47
t_{PLH}	XCKEN to QB	1.72	1.97
t_{PHL}		1.86	1.51

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	XCKEN to XOUT	1.55	1.72
t_{PHL}		1.29	1.31
t_{PHL}	RB to Q	1.18	2.53
t_{PLH}	RB to QB	0.714	2.35
t_{PHL}	RB to XOUT	1.11	1.34
t_{PLH}	OUTHLD to Q	0.348	2.50
t_{PHL}		0.331	2.31
t_{PLH}	OUTHLD to QB	0.606	2.04
t_{PHL}		0.614	1.51

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.304	4.31	0.279	3.24
QB	0.248	4.37	0.207	2.61
XOUT	0.310	2.93	0.200	1.71

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.02	0.600	0.367
t_{su}	Setup Time XD to CK	1.77	1.04	0.635
t_{su}	Setup Time XDEN to CK	1.96	1.15	0.702
t_{su}	Setup Time D to XCK	0.512	0.300	0.183
t_{su}	Setup Time XD to XCK	1.19	0.700	0.428
t_{su}	Setup Time XDEN to XCK	1.18	0.690	0.422
t_{su}	Setup Time D to XCKEN	0.512	0.300	0.183
t_{su}	Setup Time CK to XCKEN	2.35	1.38	0.843
t_{su}	Setup Time XD to XCKEN	1.19	0.700	0.428
t_{su}	Setup Time XDEN to XCKEN	1.38	0.810	0.495
t_{su}	Setup Time XCK to XCKEN	2.17	1.27	0.776
t_{su}	Setup Time CK to OUTHLD	2.95	1.73	1.06
t_{su}	Setup Time XCK to OUTHLD	3.53	2.07	1.27
t_{su}	Setup Time XCKEN to OUTHLD	3.53	2.07	1.27
t_h	Hold Time CK to D	0.171	0.100	0.061
t_h	Hold Time CK to XD	−0.444	−0.260	−0.159
t_h	Hold Time CK to XDEN	−0.444	−0.260	−0.159
t_h	Hold Time XCK to D	0.683	0.400	0.244
t_h	Hold Time XCK to XD	−0.136	−0.080	−0.049
t_h	Hold Time XCK to XDEN	−0.136	−0.080	−0.049
t_h	Hold Time XCKEN to D	0.341	0.200	0.122
t_h	Hold Time XCKEN to CK	2.35	1.38	0.843

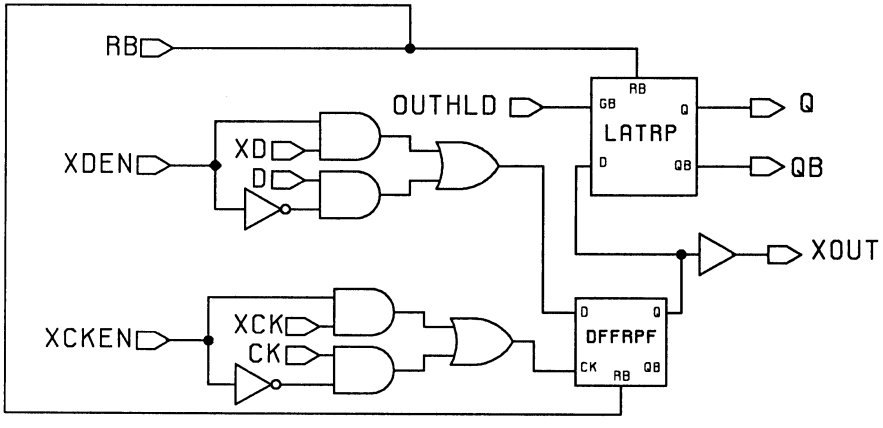
Timing requirements (Sheet 1 of 2)

DFFRPFX08

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_h	Hold Time XCKEN to XD	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XDEN	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XCK	2.17	1.27	0.776
t_h	Hold Time OUTHLD to CK	−1.775	−1.040	−0.635
t_h	Hold Time OUTHLD to XCK	−2.219	−1.300	−0.795
t_h	Hold Time OUTHLD to XCKEN	−2.219	−1.300	−0.795
t_{pwh}	Pulse Width (high) CK	3.35	1.96	1.20
t_{pwh}	Pulse Width (high) XCK	3.93	2.30	1.41
t_{pwh}	Pulse Width (high) XCKEN	3.74	2.19	1.34
t_{pwl}	Pulse Width (low) RB	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) XCK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) XCKEN	3.35	1.96	1.20
t_{pwl}	Pulse Width (low) OUTHLD	2.95	1.73	1.06
rt	Recovery Time RB to CK	−1.383	−0.810	−0.495
rt	Recovery Time RB to XCK	−1.963	−1.150	−0.702
rt	Recovery Time RB to XCKEN	−1.963	−1.150	−0.702

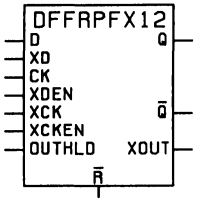
Timing requirements (Sheet 2 of 2)



Functional diagram: DFFRPFX08

Fast High Drive D Flip–Flop, Positive Edge Triggered, with Multiplexed Data and Clock, with Reset

DFFRPFX12 is a fully static D-type, positive edge triggered flip-flop with multiplexed data and clock inputs and an output hold latch. This cell is appropriate for use in internal scan test applications. It is positive edge triggered with respect to CK and XCK. The output hold latch holds data when OUTHLD is high and is transparent when OUTHLD is low. (See functional diagram.) RB is asynchronous and active low.



Inputs: RB, D, CK, XD, XDEN, XCK, XCKEN, OUTHLD
Outputs: Q, QB, XOUT
Input Cap.: RB: 0.034
D: 0.070
CK: 0.071
XD: 0.069
XDEN: 0.118
XCK: 0.069
XCKEN: 0.118
OUTHLD: 0.116 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.278 M_{CHL} = 0.179
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 37.0 grids wide, 13.4 grids high

RB	D	CK	XD	XDEN	XCK	XCKEN	OUTHLD	Q	QB	XOUT
H	D	↑	X	L	X	L	L	D	DB	D
H	X	↑	XD	H	X	L	L	XD	XDB	XD
H	D	↑	X	L	X	L	H	Qo	QBo	D
H	X	↑	XD	H	X	L	H	Qo	QBo	XD
L	X	X	X	L	X	X	X	L	H	L
H	D	X	X	L	↑	H	L	D	DB	D
H	X	X	XD	H	↑	H	L	XD	XDB	XD
H	D	X	X	L	↑	H	H	Qo	QBo	D
H	X	X	XD	H	↑	H	H	Qo	QBo	XD

Function table

DFFRPFX12

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.77	3.33	3.47	3.90
t_{PHL}		1.39	2.60	2.71	3.04
t_{PLH}	CK to QB	1.77	3.32	3.46	3.88
t_{PHL}		1.96	3.67	3.83	4.29
t_{PLH}	CK to XOUT	1.73	3.25	3.39	3.81
t_{PHL}		1.35	2.54	2.65	2.97
t_{PLH}	XCK to Q	2.08	3.90	4.07	4.57
t_{PHL}		1.69	3.18	3.31	3.72
t_{PLH}	XCK to QB	2.08	3.90	4.06	4.56
t_{PHL}		2.26	4.24	4.42	4.96
t_{PLH}	XCK to XOUT	2.04	3.82	3.99	4.48
t_{PHL}		1.66	3.12	3.25	3.65
t_{PLH}	XCKEN to Q	1.98	3.72	3.88	4.35
t_{PHL}		1.60	2.99	3.12	3.50
t_{PLH}	XCKEN to QB	1.98	3.71	3.87	4.34
t_{PHL}		2.17	4.06	4.23	4.75
t_{PLH}	XCKEN to XOUT	1.94	3.64	3.80	4.26
t_{PHL}		1.56	2.93	3.06	3.43
t_{PHL}	RB to Q	1.40	2.63	2.75	3.08
t_{PLH}	RB to QB	1.06	1.99	2.08	2.33
t_{PHL}	RB to XOUT	1.45	2.71	2.83	3.17
t_{PLH}	OUTHLD to Q	0.718	1.36	1.42	1.59
t_{PHL}		0.529	1.00	1.04	1.17
t_{PLH}	OUTHLD to QB	0.889	1.68	1.75	1.97
t_{PHL}		0.902	1.70	1.77	1.99

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.52	1.34
t_{PHL}		1.19	1.19
t_{PLH}	CK to QB	1.56	0.887
t_{PHL}		1.82	0.667
t_{PLH}	CK to XOUT	1.44	1.74
t_{PHL}		1.14	1.39
t_{PLH}	XCK to Q	1.82	1.41
t_{PHL}		1.50	1.19
t_{PLH}	XCK to QB	1.87	0.920
t_{PHL}		2.11	0.733
t_{PLH}	XCK to XOUT	1.74	1.83
t_{PHL}		1.45	1.40
t_{PLH}	XCKEN to Q	1.73	1.38
t_{PHL}		1.40	1.17
t_{PLH}	XCKEN to QB	1.77	0.847
t_{PHL}		2.02	0.700

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	XCKEN to XOUT	1.64	1.78
t_{PHL}		1.35	1.39
t_{PHL}	RB to Q	1.21	1.21
t_{PLH}	RB to QB	0.785	1.55
t_{PHL}	RB to XOUT	1.23	1.43
t_{PLH}	OUTHLD to Q	0.456	1.45
t_{PHL}		0.339	1.15
t_{PLH}	OUTHLD to QB	0.682	0.907
t_{PHL}		0.748	0.787

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.335	2.23	0.265	1.38
QB	0.222	2.14	0.212	1.21
XOUT	0.366	2.95	0.237	1.73

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.02	0.600	0.367
t_{su}	Setup Time XD to CK	1.77	1.04	0.635
t_{su}	Setup Time XDEN to CK	1.77	1.04	0.635
t_{su}	Setup Time D to XCK	0.512	0.300	0.183
t_{su}	Setup Time XD to XCK	1.19	0.700	0.428
t_{su}	Setup Time XDEN to XCK	1.18	0.690	0.422
t_{su}	Setup Time D to XCKEN	0.683	0.400	0.244
t_{su}	Setup Time CK to XCKEN	2.35	1.38	0.843
t_{su}	Setup Time XD to XCKEN	1.38	0.810	0.495
t_{su}	Setup Time XDEN to XCKEN	1.38	0.810	0.495
t_{su}	Setup Time XCK to XCKEN	2.17	1.27	0.776
t_{su}	Setup Time CK to OUTHLD	3.35	1.96	1.20
t_{su}	Setup Time XCK to OUTHLD	3.93	2.30	1.41
t_{su}	Setup Time XCKEN to OUTHLD	3.74	2.19	1.34
t_h	Hold Time CK to D	0.171	0.100	0.061
t_h	Hold Time CK to XD	−0.444	−0.260	−0.159
t_h	Hold Time CK to XDEN	−0.444	−0.260	−0.159
t_h	Hold Time XCK to D	0.683	0.400	0.244
t_h	Hold Time XCK to XD	−0.136	−0.080	−0.049
t_h	Hold Time XCK to XDEN	−0.136	−0.080	−0.049
t_h	Hold Time XCKEN to D	0.341	0.200	0.122
t_h	Hold Time XCKEN to CK	2.35	1.38	0.843

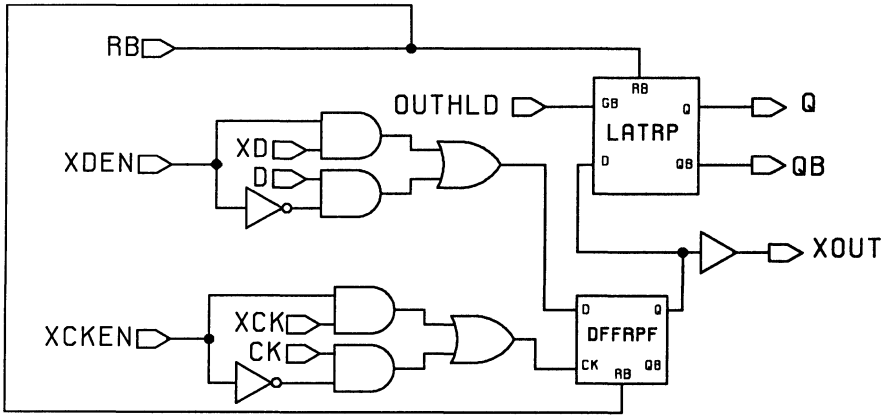
Timing requirements (Sheet 1 of 2)

DFFRPFX12

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_h	Hold Time XCKEN to XD	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XDEN	−0.291	−0.170	−0.104
t_h	Hold Time XCKEN to XCK	2.17	1.27	0.776
t_h	Hold Time OUTHLD to CK	−2.065	−1.210	−0.739
t_h	Hold Time OUTHLD to XCK	−2.509	−1.470	−0.898
t_h	Hold Time OUTHLD to XCKEN	−2.372	−1.390	−0.850
t_{pwh}	Pulse Width (high) CK	3.53	2.07	1.27
t_{pwh}	Pulse Width (high) XCK	3.93	2.30	1.41
t_{pwh}	Pulse Width (high) XCKEN	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) RB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) XCK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) XCKEN	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) OUTHLD	3.14	1.84	1.12
rt	Recovery Time RB to CK	−1.195	−0.700	−0.428
rt	Recovery Time RB to XCK	−1.963	−1.150	−0.702
rt	Recovery Time RB to XCKEN	−1.775	−1.040	−0.635

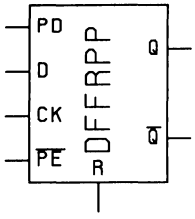
Timing requirements (Sheet 2 of 2)



Functional diagram: DFFRPFX12

D Flip–Flop with Reset and Parallel Data Input, Positive Edge Triggered

DFFRPP is a D-type, positive edge triggered flip-flop with parallel load, and single clock input. Parallel data from PD is transparent when PEB is low. R is asynchronous and active high.



Inputs: R, D, PD, PEB, CK
Outputs: Q, QB
Input Cap.: R: 0.036
D: 0.068
PD: 0.053
PEB: 0.036
CK: 0.035 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.206 M_{CHL} = 0.212
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 24.0 grids wide, 14.4 grids high

FUNCTION TABLE

R	D	PD	PEB	CK	Q	QB
H	X	X	X	X	L	H
L	X	H	L	X	H	L
L	X	L	L	X	L	H
L	H	X	H	↑	H	L
L	L	X	H	↑	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.14	2.13	2.23	2.50
t_{PHL}		1.32	2.48	2.58	2.90
t_{PLH}	*CK to QB	1.90	3.57	3.72	4.18
t_{PHL}		1.79	3.38	3.52	3.96
t_{PLH}	R to QB	1.03	1.94	2.03	2.28
t_{PHL}		2.88	5.39	5.62	6.31
t_{PLH}	R to Q	2.06	3.85	4.02	4.51
t_{PHL}		1.92	3.59	3.75	4.21
t_{PLH}	PD to Q	1.55	2.91	3.03	3.40
t_{PHL}		1.46	2.73	2.85	3.20
t_{PLH}	*PD to QB	2.06	3.88	4.04	4.54
t_{PHL}		2.20	4.14	4.32	4.85
t_{PLH}	PEB to Q	1.76	3.31	3.45	3.87
t_{PHL}		2.30	4.31	4.49	5.04
t_{PLH}	*PEB to QB	2.90	5.45	5.68	6.38
t_{PHL}		2.44	4.58	4.77	5.36

* The propagation delay from PD, PEB, and CK to QB depends on the delay from each pin to the Q output. See the Timing Equation application note for more information.

Timing characteristics

DFFRPP

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.777	2.72
t_{PHL}		1.06	1.68
t_{PLH}	Q to QB (CK)	0.282	1.45
t_{PHL}		0.232	1.25
t_{PLH}	R to QB	0.803	1.44
t_{PHL}		2.62	1.67
t_{PLH}	R to Q	1.71	2.65
t_{PHL}		1.66	1.69
t_{PLH}	PD to Q	1.20	2.65
t_{PHL}		1.19	1.74
t_{PLH}	Q to QB (PD)	0.302	1.53
t_{PHL}		0.224	1.27
t_{PLH}	PEB to Q	1.40	2.75
t_{PHL}		2.04	1.73
t_{PLH}	Q to QB (PEB)	0.308	1.45
t_{PHL}		0.250	1.20

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

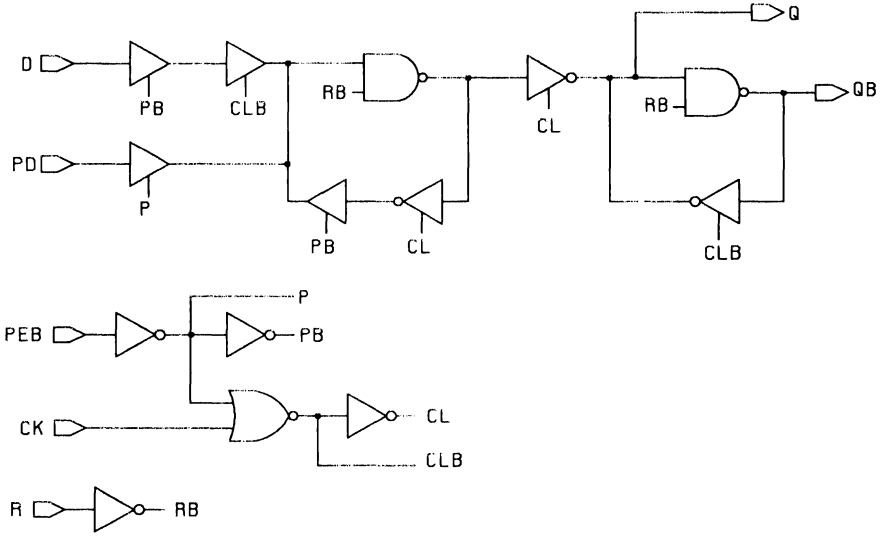
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.915	5.87	0.541	2.76
QB	0.398	2.95	0.362	1.78

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time PD to PEB	1.57	0.920	0.563
t_{su}	Setup Time D to CK	3.14	1.84	1.12
t_h	Hold Time PEB to PD	−0.733	−0.430	−0.263
t_h	Hold Time CK to D	−0.291	−0.170	−0.104
t_{pwh}	Pulse Width (high) R	4.91	2.88	1.76
t_{pwh}	Pulse Width (high) CK	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) PEB	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) CK	6.67	3.91	2.39
rt	Recovery Time R	1.77	1.04	0.635
rt	Recovery Time PEB	5.31	3.11	1.90

Timing requirements



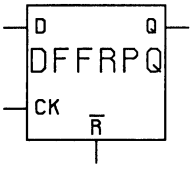
Functional diagram: DFFRPP

DFFRPQ

D Flip–Flop with Reset, Positive Edge Triggered

DFFRPQ is a fully static D-type, positive edge triggered flip–flop with only a Q output. RB is asynchronous and active low.

Inputs: D, CK, RB
Outputs: Q
Input Cap.: D: 0.076
CK: 0.097
RB: 0.086 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.155 M_{CHL} = 0.138
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 13.0 grids wide, 10.9 grids high



FUNCTION TABLE

D	CK	RB	Q
L	↑	H	L
H	↑	H	H
X	X	L	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.656	1.24	1.29	1.45
t_{PHL}		0.830	1.56	1.63	1.83
t_{PHL}	RB to Q	0.740	1.39	1.45	1.63

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.374	2.17
t_{PHL}		0.593	1.79
t_{PHL}	RB to Q	0.489	1.93

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

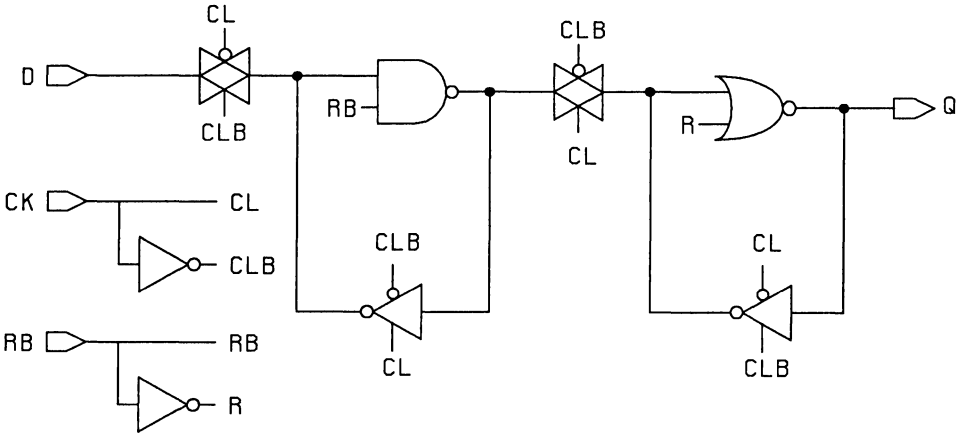
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.395	4.33	0.361	2.29

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.13	0.660	0.404
t_h	Hold Time CK to D	−0.291	−0.170	−0.104
t_{pwh}	Pulse Width (high) CK	3.38	1.990	1.210
t_{pwl}	Pulse Width (low) CK	2.25	1.32	0.800
t_{pwl}	Pulse Width (low) RB	2.35	1.38	0.843
rt	Recovery Time RB	0.392	0.230	0.141

Timing requirements



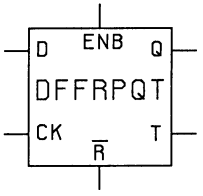
Functional diagram: DFFRPQ

DFFRPQT

D Flip–Flop with Reset and Tristate, Positive Edge Triggered

DFFRPQT is a fully static D-type, positive edge triggered flip–flop. RB is asynchronous for Q and active low. When ENB is high, the T output is in a Hi–Z state and Q functions as on a standard flip–flop. When ENB is low, T equals Q.

Inputs: ENB, D, CK, RB
Outputs: Q, T
Input Cap.: ENB: 0.075
D: 0.076
CK: 0.097
RB: 0.084 pF
Output Cap.:T: 0.033 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.140 M_{CHL} = 0.263
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 17.0 grids wide, 10.9 grids high



FUNCTION TABLE

D	CK	RB	ENB	Q	T
L	↑	H	L	L	L
H	↑	H	L	H	H
X	X	L	L	L	L
L	↑	H	H	L	HiZ
H	↑	H	H	H	HiZ
X	X	L	H	L	HiZ

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to T	0.373	0.706	0.737	0.828
t_{PHL}		0.469	0.894	0.933	1.05
t_{PLH}	CK to Q	0.820	1.54	1.61	1.80
t_{PHL}		1.10	2.06	2.15	2.42
t_{PLH}	CK to T	0.815	1.53	1.60	1.79
t_{PHL}		1.06	2.00	2.08	2.34
t_{PHL}	RB to Q	0.773	1.46	1.52	1.71
t_{PHL}	RB to T	2.67	5.01	5.22	5.86

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to T	0.113	2.01
t_{PHL}		0.216	1.43
t_{PLH}	CK to Q	0.539	2.22
t_{PHL}		0.785	2.01
t_{PLH}	CK to T	0.549	2.07
t_{PHL}		0.767	1.83
t_{PHL}	RB to Q	0.471	1.92
t_{PHL}	RB to T	2.35	2.12

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.468	4.28	0.505	2.40
T	0.275	4.45	0.358	2.22

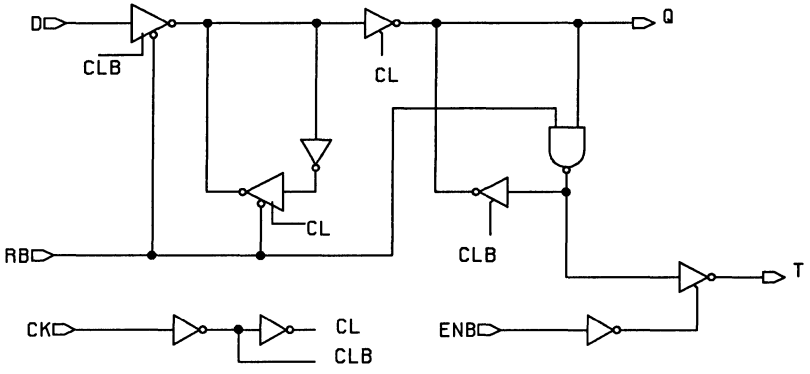
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD} =4.5V T_A =70C	NOMINAL V_{DD} =5.0V T_A =25C	BEST V_{DD} =5.5V T_A =0C
t_{su}	Setup Time D to CK	0.956	0.560	0.342
t_h	Hold Time CK to D	0.205	0.120	0.074
t_{pwh}	Pulse Width (high) CK	3.33	1.96	1.20
t_{pwl}	Pulse Width (low) CK	3.72	2.19	1.34
t_{pwl}	Pulse Width (low) RB	4.71	2.76	1.69
rt	Recovery Time RB	0.392	0.230	0.141

Timing requirements

DFFRPQT

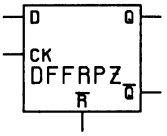


Functional diagram: DFFRPQT

D Flip–Flop with Reset, Positive Edge Triggered, Zero Setup Time

DFFRPZ is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low. It has zero setup time.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.127
D: 0.043
CK: 0.021 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.202 M_{CHL} = 0.215
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 18.0 grids wide, 12.4 grids high



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.76	3.31	3.45	3.87
t_{PHL}		2.80	5.23	5.46	6.12
t_{PLH}	*CK to QB	3.37	6.32	6.59	7.40
t_{PHL}		2.54	4.77	4.97	5.58
t_{PHL}	*RB to Q	1.26	2.38	2.48	2.78
t_{PLH}	RB to QB	0.613	1.16	1.21	1.36

* The propagation delay from CK to QB depends on the CK to Q delay and rise/fall time. Also, the delay from RB to Q depends on the RB to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.47	2.05
t_{PHL}		2.52	1.82
t_{PLH}	Q to QB (CK)	0.247	1.16
t_{PHL}		0.342	1.74
t_{PHL}	QB to Q (RB)	0.381	1.49
t_{PLH}	RB to QB	0.309	2.19

Delay coefficients

DFFRPZ

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

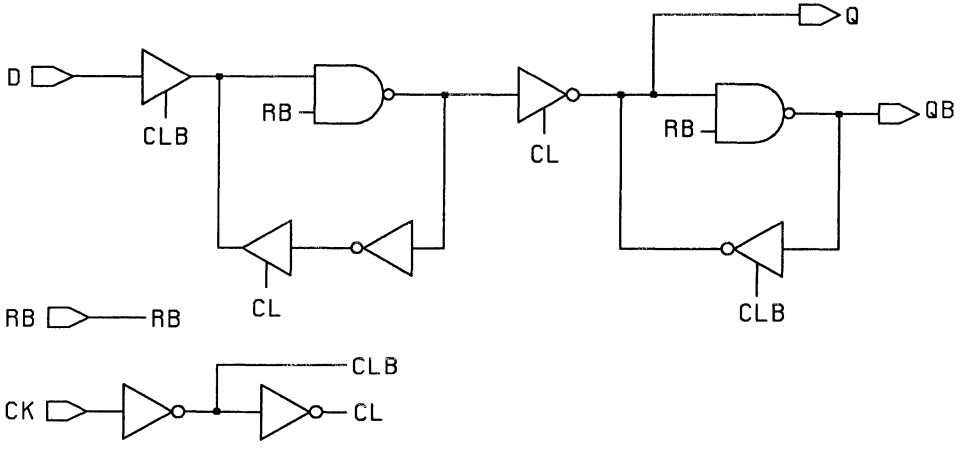
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.878	4.11	0.904	2.31
QB	0.401	2.09	0.448	2.75

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.000	0.000	0.000
t_h	Hold Time CK to D	1.38	0.810	0.495
t_{pwh}	Pulse Width (high) CK	4.71	2.76	1.69
t_{pwl}	Pulse Width (low) RB	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) CK	6.09	3.57	2.18
rt	Recovery Time RB	-1.024	-0.600	-0.367

Timing requirements

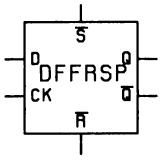


Functional diagram: DFFRP

D Flip–Flop with Reset and Set, Positive Edge Triggered

DFFRSP is a fully static D-type positive edge triggered flip–flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.101
D: 0.052
CK: 0.034
RB: 0.141 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.177 M_{CHL} = 0.202
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 17.0 grids wide, 13.4 grids high



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

*Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to QB	1.04	1.96	2.04	2.29
t_{PHL}		1.27	2.39	2.49	2.79
t_{PLH}	*CK to Q	2.00	3.76	3.92	4.40
t_{PHL}		1.74	3.27	3.41	3.83
t_{PHL}	*RB to Q	1.41	2.66	2.78	3.12
t_{PLH}	RB to QB	0.681	1.28	1.34	1.50
t_{PHL}		0.634	1.20	1.25	1.40
t_{PLH}	SB to Q	0.556	1.05	1.10	1.23
t_{PHL}		0.400	0.760	0.793	0.892
t_{PHL}	*SB to QB	1.49	2.82	2.94	3.30

* The propagation delay from CK and RB to Q depends on the delay from each pin to the QB output. Also, the delay from SB to QB depends on the delay from SB to Q and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to QB	0.702	2.65
t_{PHL}		0.968	2.17
t_{PLH}	QB to Q (CK)	0.336	2.21
t_{PHL}		0.252	1.77

Delay coefficients (Sheet 1 of 2)

DFFRSP

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	QB to Q (RB)	0.283	1.81
t_{PLH}	RB to QB	0.363	2.44
t_{PHL}		0.340	2.09
t_{PLH}	SB to Q	0.264	2.18
t_{PHL}		0.157	1.58
t_{PHL}	Q to QB (SB)	0.562	2.09

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

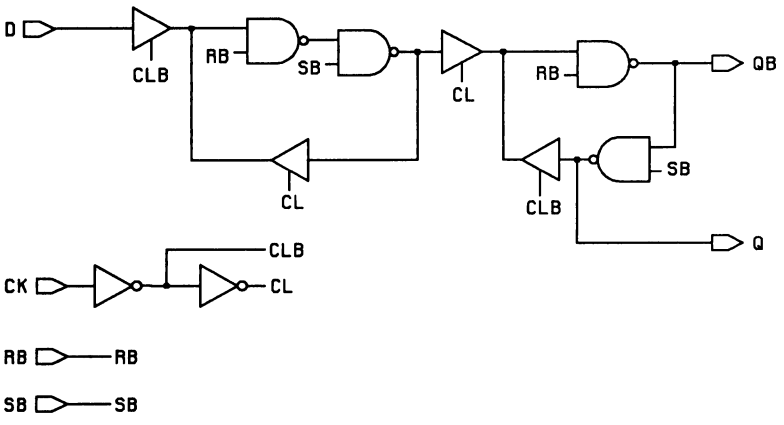
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.471	4.39	0.379	2.67
QB	0.827	5.79	0.666	3.79

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.16	0.680	0.415
t_h	Hold Time CK to D	0.376	0.220	0.135
t_{pwh}	Pulse Width (high) CK	4.52	2.65	1.62
t_{pwl}	Pulse Width (low) SB	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) CK	3.74	2.19	1.34
t_{pwl}	Pulse Width (low) RB	4.32	2.53	1.55
rt	Recovery Time SB	−1.571	−0.920	−0.563
rt	Recovery Time RB	1.16	0.680	0.415

Timing requirements



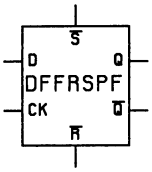
Functional diagram: DFFRSP

DFFRSPF

Fast D Flip–Flop with Reset and Set, Positive Edge Triggered

DFFRSPF is a fully static D–type positive edge triggered flip–flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.166
D: 0.188
CK: 0.081
RB: 0.172 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.196 M_{CHL} = 0.174
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 24.0 grids wide, 15.4 grids high



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

*Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.935	1.76	1.83	2.06
t_{PHL}		0.846	1.59	1.66	1.86
t_{PLH}	CK to QB	0.890	1.68	1.75	1.96
t_{PHL}		0.864	1.63	1.70	1.90
t_{PHL}	*RB to Q	1.17	2.21	2.30	2.59
t_{PLH}	RB to QB	0.331	0.632	0.660	0.742
t_{PHL}		0.285	0.545	0.568	0.639
t_{PLH}	SB to Q	0.294	0.562	0.586	0.660
t_{PHL}		0.274	0.524	0.546	0.615
t_{PHL}	*SB to QB	1.24	2.34	2.44	2.75

* The propagation delay from RB to Q depends on the RB to QB delay and rise/fall time. Also, the delay from SB to QB depends on the delay from SB to Q and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.760	0.927
t_{PHL}		0.681	0.920
t_{PLH}	CK to QB	0.714	0.940
t_{PHL}		0.696	0.953
t_{PHL}	QB to Q (RB)	0.679	1.03
t_{PLH}	RB to QB	0.151	0.980
t_{PHL}		0.133	0.793
t_{PLH}	SB to Q	0.120	0.913
t_{PHL}		0.125	0.760
t_{PHL}	Q to QB (SB)	0.753	1.27

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.295	1.73	0.238	1.29
QB	0.220	1.78	0.258	1.35

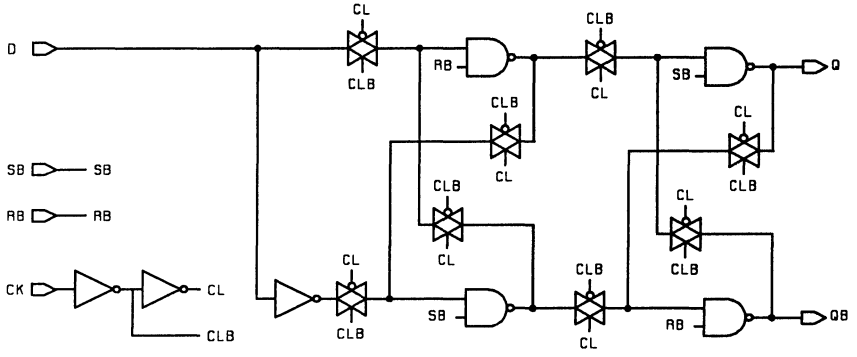
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.563	0.330	0.202
t_h	Hold Time CK to D	0.563	0.330	0.202
t_{pwh}	Pulse Width (high) CK	2.95	1.73	1.06
t_{pwl}	Pulse Width (low) SB	4.52	2.65	1.62
t_{pwl}	Pulse Width (low) CK	3.35	1.96	1.20
t_{pwl}	Pulse Width (low) RB	4.71	2.76	1.69
rt	Recovery Time SB	−1.963	−1.150	−0.702
rt	Recovery Time RB	−2.355	−1.380	−0.843

Timing requirements

DFFRSPF

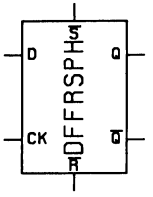


Functional diagram: DFFRSPF

Buffered D Flip–Flop with Reset and Set, Positive Edge Triggered (High Drive)

DFFRSPH is a fully static D-type, edge triggered flip-flop. It is positive edge triggered with respect to the single phase clock (CK). RB and SB are asynchronous and active low. Note: This cell is functionally compatible with a DFFRSP except when both RB and SB are low.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.098
D: 0.051
CK: 0.035
RB: 0.144 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.209 M_{CHL} = 0.217
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 22.0 grids wide, 13.4 grids high



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

*Both Q and QB will be low when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.62	3.05	3.18	3.57
t_{PHL}		1.41	2.65	2.76	3.10
t_{PLH}	CK to QB	1.99	3.73	3.89	4.37
t_{PHL}		2.42	4.54	4.73	5.31
t_{PLH}	RB to Q	0.944	1.78	1.85	2.08
t_{PHL}		1.03	1.93	2.02	2.27
t_{PLH}	RB to QB	1.59	2.99	3.12	3.50
t_{PLH}	SB to Q	1.63	3.06	3.19	3.58
t_{PLH}	SB to QB	0.616	1.16	1.21	1.36
t_{PHL}		0.863	1.63	1.70	1.91

Timing characteristics

DFFRSPH

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.46	0.740
t_{PHL}		1.23	0.907
t_{PLH}	CK to QB	1.85	0.507
t_{PHL}		2.28	0.533
t_{PLH}	RB to Q	0.774	0.820
t_{PHL}		0.843	0.940
t_{PLH}	RB to QB	1.44	0.633
t_{PLH}	SB to Q	1.46	0.853
t_{PLH}	SB to QB	0.461	0.673
t_{PHL}		0.691	0.813

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

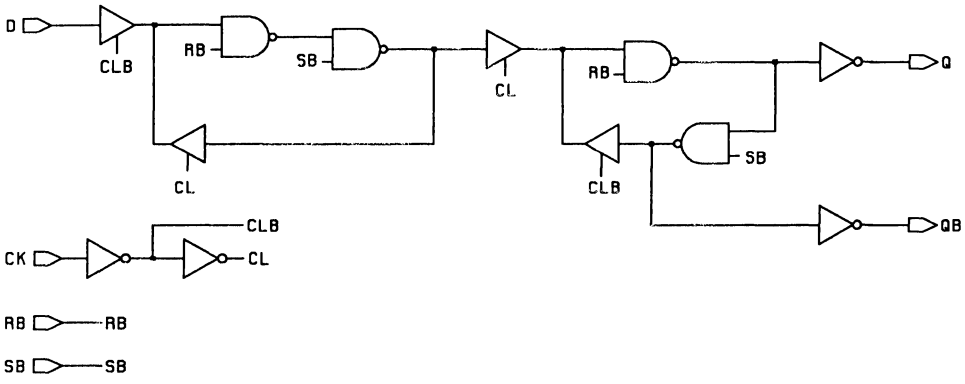
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.333	1.01	0.391	0.927
QB	0.267	1.05	0.295	0.887

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.35	0.790	0.483
t_h	Hold Time CK to D	0.376	0.220	0.135
t_{pwh}	Pulse Width (high) CK	4.52	2.65	1.62
t_{pwl}	Pulse Width (low) SB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CK	3.74	2.19	1.34
t_{pwl}	Pulse Width (low) RB	4.32	2.53	1.55
rt	Recovery Time SB	−1.571	−0.920	−0.563
rt	Recovery Time RB	1.16	0.680	0.415

Timing requirements

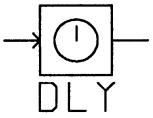


Functional diagram: DFFRSPH

DLYCEL

Delay Cell

Inputs: A
Outputs: X
Input Cap.: A: 0.032 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.72 N = 1.00 W = 1.28
Cell Size: 8.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	6.93	11.8	12.3	13.8
t_{PHL}		6.85	11.7	12.2	13.7

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	6.72	2.12
t_{PHL}		6.64	2.11

Delay coefficients

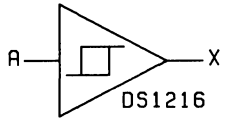
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	3.71	0.480	4.19	0.547

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1216 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.095 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.186 M_{CHL} = 0.062
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 6.0 grids wide, 11.9 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.6V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 400mV Min: 100mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.935	1.63	1.70	1.91
t_{PHL}		1.13	1.98	2.06	2.31

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.874	0.607
t_{PHL}		1.03	0.987

Delay coefficients

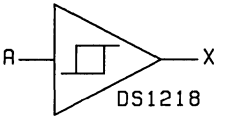
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.244	0.953	0.453	1.05

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1218 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.102 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.192 M_{CHL} = 0.090
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 6.0 grids wide, 11.9 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 600mV Min: 300mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	1.17	2.05	2.14	2.40
t_{PHL}		2.28	3.98	4.15	4.66

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	1.11	0.673
t_{PHL}		2.15	1.31

Delay coefficients

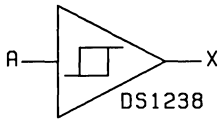
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.336	0.987	1.04	1.32

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1238 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.128 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.058 M_{CHL} = 0.132
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 8.0 grids wide, 11.9 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 3.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 2.6V Min: 2.3V

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	1.40	2.45	2.56	2.87
t_{PHL}		2.98	5.20	5.42	6.08

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	1.32	0.840
t_{PHL}		2.82	1.60

Delay coefficients

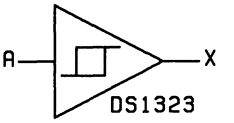
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.726	1.19	1.57	1.47

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1323 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.173 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.121 M_{CHL} = 0.144
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 6.0 grids wide, 11.9 grids high

DC switching parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.3V ± 300mV
High to Low = 1.3V ± 300mV
Hysteresis: Typ: 1.0V Min: 700mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.995	1.74	1.81	2.03
t_{PHL}		1.46	2.55	2.66	2.98

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.928	0.673
t_{PHL}		1.34	1.23

Delay coefficients

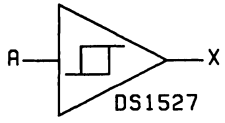
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.294	1.06	0.609	1.26

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1527 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.217 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.093 M_{CHL} = 0.174
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 6.0 grids wide, 11.9 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.7V ± 300mV
High to Low = 1.5V ± 300mV
Hysteresis: Typ: 1.2V Min: 900mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	1.02	1.78	1.86	2.08
t_{PHL}		1.26	2.19	2.29	2.57

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.947	0.720
t_{PHL}		1.15	1.07

Delay coefficients

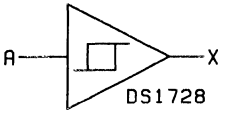
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.331	1.05	0.475	1.14

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1728 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.211 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.065 M_{CHL} = 0.219
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 6.0 grids wide, 11.9 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.8V ± 300mV
High to Low = 1.7V ± 300mV
Hysteresis: Typ: 1.1V Min: 800mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.960	1.68	1.75	1.96
t_{PHL}		1.33	2.31	2.41	2.71

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.890	0.700
t_{PHL}		1.22	1.05

Delay coefficients

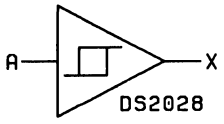
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.326	1.06	0.465	1.11

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS2028 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.448 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.137 M_{CHL} = 0.086
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 9.0 grids wide, 12.4 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.8V ± 300mV
High to Low = 2.0V ± 300mV
Hysteresis: Typ: 800mV Min: 500mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	1.23	2.15	2.24	2.51
t_{PHL}		0.847	1.48	1.54	1.73

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	1.16	0.693
t_{PHL}		0.764	0.833

Delay coefficients

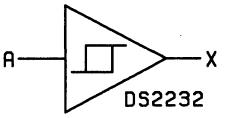
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.340	1.05	0.340	0.927

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS2232 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.196 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.054 M_{CHL} = 0.176
Process Derating: B = 0.69 N = 1.00 W = 1.31
Cell Size: 9.0 grids wide, 11.9 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 3.2V ± 300mV
High to Low = 2.2V ± 300mV
Hysteresis: Typ: 1.0V Min: 700mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.846	1.48	1.54	1.73
t_{PHL}		1.37	2.39	2.49	2.79

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.773	0.727
t_{PHL}		1.30	0.700

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.388	1.13	0.446	0.833

Rise/Fall time coefficients for the next cell

2–Input Exclusive NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.099
B: 0.097 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.196 M_{CHL} = 0.394
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 10.9 grids high

$X = A \cdot B + \overline{A} \cdot \overline{B}$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.735	1.39	1.45	1.62
t_{PHL}		0.759	1.44	1.51	1.69
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.467	1.86
t_{PHL}		0.450	1.43

Delay coefficients

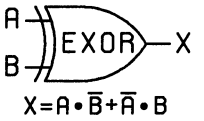
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.438	4.29	0.754	1.38

Rise/Fall time coefficients for the next cell

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.099
B: 0.098 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.176 M_{CHL} = 0.098
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 10.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.507	0.958	0.999	1.12
t_{PHL}		0.347	0.655	0.683	0.767
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.236	1.97
t_{PHL}		0.170	1.36

Delay coefficients

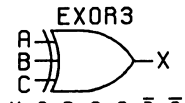
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.412	4.28	0.256	2.95

Rise/Fall time coefficients for the next cell

3–Input Exclusive OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.223
B: 0.325
C: 0.219 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.385 M_{CHL} = 0.305
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 26.0 grids wide, 14.4 grids high



$X=\bar{A}\bullet B\bullet C+A\bullet\bar{B}\bullet\bar{C}$
$+\bar{A}\bullet B\bullet\bar{C}+\bar{A}\bullet\bar{B}\bullet C$

FUNCTION TABLE

A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.953	1.81	1.88	2.12
t_{PHL}		0.796	1.51	1.57	1.77
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.569	2.23
t_{PHL}		0.537	1.31

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

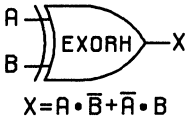
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.35	3.47	0.828	2.48

Rise/Fall time coefficients for the next cell

EXORH

2–Input Exclusive OR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.093
B: 0.092 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.182 M_{CHL} = 0.237
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 14.0 grids wide, 10.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.750	1.41	1.47	1.65
t_{PHL}		0.721	1.36	1.42	1.60
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.593	0.807
t_{PHL}		0.529	0.927

Delay coefficients

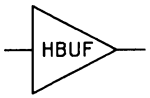
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.156	1.42	0.251	0.947

Rise/Fall time coefficients for the next cell

High Drive Noninverting Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.035 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.175 M_{CHL} = 0.170
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.557	1.05	1.10	1.23
t_{PHL}		0.616	1.16	1.21	1.36

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.423	0.600
t_{PHL}		0.478	0.667

Delay coefficients

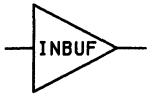
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.189	1.01	0.200	0.807

Rise/Fall time coefficients for the next cell

Noninverting Input Buffer

INBUF is used to buffer the signal from input and I/O pads, and is compatible with 1.4V & 300mV threshold voltage (V_{DD} = 5V). INBUF is tested using V_{IL} = 0.8V and V_{IH} = 2.0V.



Inputs: A
Outputs: X
Input Cap.: A: 0.074 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.107 M_{CHL} = 0.060
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 12.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.604	1.13	1.18	1.32
t_{PHL}		0.833	1.55	1.62	1.82

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.550	0.540
t_{PHL}		0.760	0.727

Delay coefficients

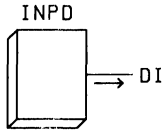
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.178	0.933	0.289	0.827

Rise/Fall time coefficients for the next cell

Input Pad

INPD is used with INBUF, or one of the Schmitt Triggers. Note that the input buffer and the chip package will add additional capacitance to all inputs.



Inputs: PAD
Outputs: DI
Input Cap.: PAD: 3.460 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.031	0.057	0.060	0.067
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.004	0.267

Delay coefficients

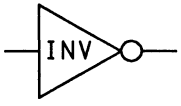
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.032 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.240 M_{CHL} = 0.212
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.0 grids wide, 7.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.381	0.728	0.760	0.855
t_{PHL}		0.363	0.692	0.722	0.812

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.073	2.07
t_{PHL}		0.087	1.87

Delay coefficients

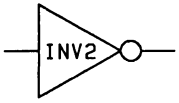
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.111	4.45	0.062	3.36

Rise/Fall time coefficients for the next cell

Inverter (2X Drive)

INV2 has 2 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.059 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.239 M_{CHL} = 0.156
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.269	0.519	0.542	0.610
t_{PHL}		0.243	0.464	0.484	0.545

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.062	1.07
t_{PHL}		0.080	0.973

Delay coefficients

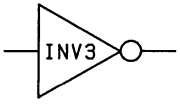
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.086	2.28	0.047	1.74

Rise/Fall time coefficients for the next cell

Inverter (3X Drive)

INV3 has 3 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.092 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.233 M_{CHL} = 0.146
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.220	0.427	0.446	0.503
t_{PHL}		0.197	0.378	0.395	0.445

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.053	0.693
t_{PHL}		0.068	0.680

Delay coefficients

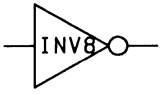
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.066	1.50	0.032	1.17

Rise/Fall time coefficients for the next cell

Inverter (8X Drive)

INV8 has 8 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.237 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.231 M_{CHL} = 0.211
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.177	0.346	0.361	0.408
t_{PHL}		0.173	0.337	0.352	0.397

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.051	0.287
t_{PHL}		0.065	0.193

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.067	0.560	0.028	0.387

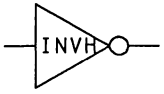
Rise/Fall time coefficients for the next cell

INVH

Inverter (High Drive)

INVH has 3 times the drive of an INV.

Inputs: A
Outputs: X
Input Cap.: A: 0.092 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.233 M_{CHL} = 0.146
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 8.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.220	0.427	0.446	0.503
t_{PHL}		0.197	0.378	0.395	0.445

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.053	0.693
t_{PHL}		0.068	0.680

Delay coefficients

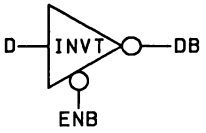
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.067	1.49	0.032	1.17

Rise/Fall time coefficients for the next cell

Tristate Inverter

INVT inverts the input signal when ENB is low. When ENB is high, the output is in a Hi-Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: D: 0.059
ENB: 0.078 pF
Output Cap.: DB: 0.033 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.068 M_{CHL} = 0.250
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 11.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to DB	0.437	0.820	0.855	0.960
t_{PHL}		0.450	0.857	0.895	1.01
t_{PLH}	ENB to DB	0.356	0.669	0.698	0.783
t_{PHL}		0.471	0.897	0.936	1.05

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to DB	0.212	1.96
t_{PHL}		0.201	1.44
t_{PLH}	ENB to DB	0.134	1.93
t_{PHL}		0.219	1.47

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

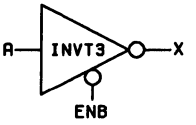
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DB	0.291	4.45	0.361	2.17

Rise/Fall time coefficients for the next cell

INVT3

Tristate Inverter (3X Drive)

INVT3 is a high drive tristate inverter with 3 times the drive of an INVT and a larger intrinsic delay. INVT3 inverts the input signal when ENB is low. When ENB is high, the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: All: 0.034 pF
Output Cap.: X: 0.040 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.182 M_{CHL} = 0.266
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 11.0 grids wide, 10.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.827	1.56	1.62	1.82
t_{PHL}		0.861	1.63	1.69	1.90
t_{PLH}	ENB to X	0.844	1.59	1.66	1.86
t_{PHL}		0.943	1.78	1.86	2.08

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.649	1.02
t_{PHL}		0.655	0.940
t_{PLH}	ENB to X	0.673	0.947
t_{PHL}		0.737	0.947

Delay coefficients

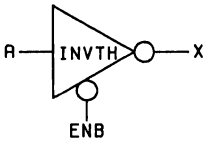
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.163	1.61	0.127	1.32

Rise/Fall time coefficients for the next cell

Tristate Inverter (High Drive)

INVTH is a high drive tristate inverter with 2 times the drive of an INVT and a smaller intrinsic delay. The input signal is inverted when ENB is low. When ENB is high, the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.095
ENB: 0.063 pF
Output Cap.: X: 0.049 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.073 M_{CHL} = 0.267
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 10.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.276	0.521	0.543	0.610
t_{PHL}		0.312	0.602	0.628	0.707
t_{PLH}	ENB to X	0.440	0.826	0.862	0.967
t_{PHL}		0.464	0.885	0.923	1.04

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.125	1.21
t_{PHL}		0.103	0.973
t_{PLH}	ENB to X	0.266	1.43
t_{PHL}		0.228	1.24

Delay coefficients

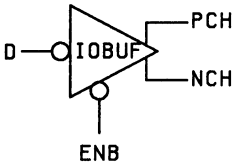
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.237	2.78	0.105	1.76

Rise/Fall time coefficients for the next cell

Input/Output Buffer

IOBUF is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.061
D: 0.394 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.267 M_{CHL} = 0.175
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 13.0 grids wide, 12.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	0.237	0.462	0.482	0.544
t_{PHL}		0.198	0.382	0.399	0.449
t_{PLH}	D to NCH	0.274	0.531	0.554	0.624
t_{PHL}		0.204	0.392	0.409	0.461
t_{PLH}	ENB to PCH	0.664	1.26	1.31	1.48
t_{PHL}		0.587	1.11	1.16	1.30
t_{PLH}	ENB to NCH	1.08	2.04	2.13	2.39
t_{PHL}		1.05	1.97	2.05	2.30

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	0.076	0.493
t_{PHL}		0.090	0.347
t_{PLH}	D to NCH	0.113	0.493
t_{PHL}		0.094	0.360
t_{PLH}	ENB to PCH	0.504	0.480
t_{PHL}		0.465	0.487
t_{PLH}	ENB to NCH	0.919	0.520
t_{PHL}		0.934	0.400

Delay coefficients

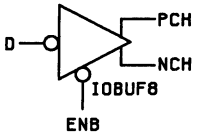
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.263	1.00	0.184	0.563
PCH	0.193	0.937	0.149	0.616

Rise/Fall time coefficients for the next cell

Input/Output Buffer (8X Drive)

IOBUF8 is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.121
D: 0.794 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.255 M_{CHL} = 0.254
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 25.0 grids wide, 12.6 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	0.211	0.412	0.431	0.486
t_{PHL}		0.222	0.431	0.451	0.508
t_{PLH}	D to NCH	0.247	0.478	0.500	0.563
t_{PHL}		0.203	0.397	0.415	0.468
t_{PLH}	ENB to PCH	0.623	1.18	1.23	1.39
t_{PHL}		0.585	1.11	1.16	1.30
t_{PLH}	ENB to NCH	1.03	1.95	2.03	2.28
t_{PHL}		1.05	1.97	2.05	2.31

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	0.083	0.213
t_{PHL}		0.097	0.180
t_{PLH}	D to NCH	0.117	0.227
t_{PHL}		0.066	0.307
t_{PLH}	ENB to PCH	0.491	0.253
t_{PHL}		0.454	0.247
t_{PLH}	ENB to NCH	0.901	0.267
t_{PHL}		0.918	0.213

Delay coefficients

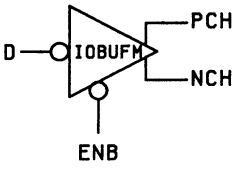
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.262	0.493	0.175	0.276
PCH	0.194	0.440	0.150	0.310

Rise/Fall time coefficients for the next cell

Input/Output Buffer (Medium Drive)

IOBUFM is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.035
D: 0.199 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.235 M_{CHL} = 0.217
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 11.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	0.272	0.523	0.546	0.615
t_{PHL}		0.257	0.496	0.517	0.583
t_{PLH}	D to NCH	0.313	0.601	0.627	0.706
t_{PHL}		0.250	0.483	0.504	0.567
t_{PLH}	ENB to PCH	0.711	1.34	1.40	1.57
t_{PHL}		0.656	1.24	1.29	1.45
t_{PLH}	ENB to NCH	1.14	2.15	2.24	2.52
t_{PHL}		1.13	2.13	2.22	2.50

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	0.089	0.840
t_{PHL}		0.101	0.653
t_{PLH}	D to NCH	0.115	0.993
t_{PHL}		0.106	0.533
t_{PLH}	ENB to PCH	0.521	0.913
t_{PHL}		0.478	0.867
t_{PLH}	ENB to NCH	0.946	0.993
t_{PHL}		0.963	0.793

Delay coefficients

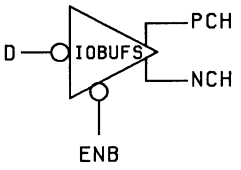
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.264	2.08	0.182	1.08
PCH	0.199	1.84	0.152	1.27

Rise/Fall time coefficients for the next cell

Input/Output Buffer (Small Drive)

IOBUFS is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.036
D: 0.104 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.212 M_{CHL} = 0.239
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 9.6 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	0.353	0.673	0.702	0.790
t_{PHL}		0.348	0.667	0.696	0.783
t_{PLH}	D to NCH	0.412	0.783	0.817	0.919
t_{PHL}		0.317	0.608	0.635	0.715
t_{PLH}	ENB to PCH	0.687	1.30	1.35	1.52
t_{PHL}		0.649	1.23	1.28	1.44
t_{PLH}	ENB to NCH	1.00	1.88	1.96	2.20
t_{PHL}		0.928	1.75	1.82	2.05

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	0.093	1.71
t_{PHL}		0.114	1.34
t_{PLH}	D to NCH	0.128	1.95
t_{PHL}		0.108	1.09
t_{PLH}	ENB to PCH	0.420	1.78
t_{PHL}		0.389	1.59
t_{PLH}	ENB to NCH	0.715	1.96
t_{PHL}		0.700	1.27

Delay coefficients

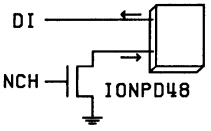
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.274	4.32	0.167	2.04
PCH	0.191	3.67	0.136	2.65

Rise/Fall time coefficients for the next cell

48mA Open Drain Input/Output Pad

IONPD48 is used to form a bidirectional pad that can drive output data, or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 4.570
PAD: 3.730 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 41.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.031	0.057	0.060	0.067
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	213	397	414	465
t_{PHL}		0.517	0.977	1.02	1.15

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.004	0.267
t_{PLH}	NCH to PAD	41.4	3.43
t_{PHL}		0.049	0.008

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	187	27.9	0.034	0.011
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

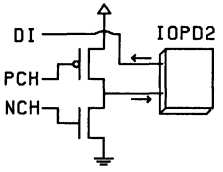
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

2mA Input/Output Pad

IOPD2 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.277
PCH: 0.225
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.631
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	8.06	15.1	15.7	17.7
t_{PHL}		9.23	17.3	18.0	20.2

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.501	0.146
t_{PHL}		0.561	0.168
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.49	0.617	0.657	0.216
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

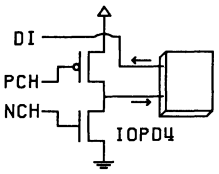
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Input/Output Pad

IOPD4 is used to form a bidirectional pad that can drive output data, or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.501
PCH: 0.446
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	4.18	7.85	8.19	9.19
t_{PHL}		4.76	8.94	9.32	10.5

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.271	0.073
t_{PHL}		0.301	0.084
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.919	0.301	0.332	0.108
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

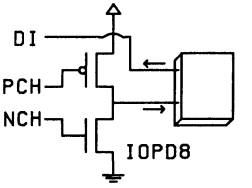
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Input/Output Pad

IOPD8 is used to form a bidirectional pad that can drive data or be put in a Hi-Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.940
PCH: 0.890
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.314
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	2.23	4.20	4.38	4.92
t_{PHL}		2.41	4.52	4.71	5.29

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.163	0.036
t_{PHL}		0.177	0.042
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.491	0.150	0.165	0.054
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

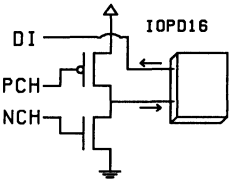
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Input/Output Pad

IOPD16 is used to form a bidirectional pad that can drive output data or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 1.870
PCH: 1.770
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.464 M_{CHL} = 0.114
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.20	2.27	2.36	2.66
t_{PHL}		1.20	2.26	2.35	2.64

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.102	0.018
t_{PHL}		0.106	0.021
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.263	0.075	0.076	0.027
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

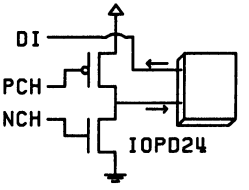
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Input/Output Pad

IOPD24 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 2.540
PCH: 2.400
PAD: 3.590 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.369 M_{CHL} = 0.113
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.949	1.80	1.87	2.11
t_{PHL}		0.940	1.76	1.84	2.06

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.094	0.014
t_{PHL}		0.093	0.016
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.236	0.055	0.068	0.020
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

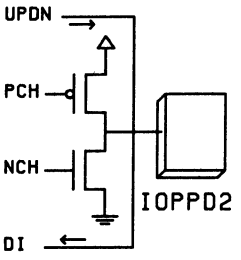
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

IOPPD2

2mA Input/Output Pad with Pullup/Pulldown Port

IOPPD2 is similar to IOPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.279
PCH: 0.223
UPDN: 53.464
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	8.22	15.4	16.1	18.0
t_{PHL}		9.27	17.4	18.1	20.3
t_{PLH}	UPDN to PAD	16.7	31.2	32.5	36.5
t_{PHL}		16.9	31.6	32.9	37.0

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.562	0.148
t_{PHL}		0.612	0.168
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273
t_{PLH}	UPDN to PAD	2.34	0.282
t_{PHL}		1.80	0.297

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.72	0.623	0.748	0.216
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

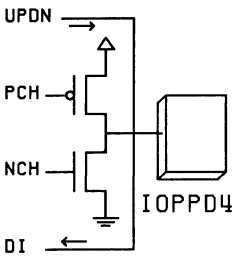
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

IOPPD4

4mA Input/Output Pad with Pullup/Pulldown Port

IOPPD4 is similar to IOPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.500
PCH: 0.443
UPDN: 53.464
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	4.20	7.89	8.22	9.23
t_{PHL}		4.82	9.03	9.42	10.6
t_{PLH}	UPDN to PAD	16.7	31.2	32.5	36.5
t_{PHL}		16.9	31.6	32.9	37.0

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.289	0.073
t_{PHL}		0.304	0.085
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273
t_{PLH}	UPDN to PAD	2.34	0.282
t_{PHL}		1.80	0.297

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.09	0.301	0.342	0.108
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

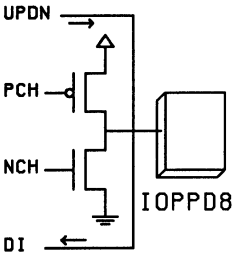
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

IOPPD8

8mA Input/Output Pad with Pullup/Pulldown Port

IOPPD8 is similar to IOPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.938
PCH: 0.878
UPDN: 53.464
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.319
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	2.28	4.29	4.48	5.03
t_{PHL}		2.45	4.60	4.79	5.38
t_{PLH}	UPDN to PAD	16.7	31.2	32.5	36.5
t_{PHL}		16.8	31.3	32.7	36.7

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.164	0.037
t_{PHL}		0.166	0.043
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273
t_{PLH}	UPDN to PAD	2.34	0.282
t_{PHL}		1.80	0.297

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.534	0.150	0.155	0.055
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

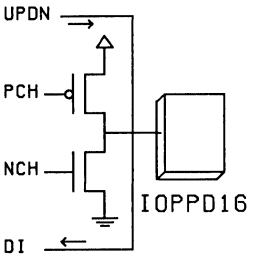
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Input/Output Pad with Pullup/Pulldown Port

IOPPD16 is similar to IOPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 1.820
PCH: 1.750
UPDN: 53.464
PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.475 M_{CHL} = 0.114
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.25	2.36	2.47	2.77
t_{PHL}		1.21	2.27	2.36	2.65
t_{PLH}	UPDN to PAD	16.6	31.1	32.4	36.4
t_{PHL}		16.7	31.2	32.5	36.5

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.099	0.019
t_{PHL}		0.112	0.021
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273
t_{PLH}	UPDN to PAD	2.34	0.282
t_{PHL}		1.80	0.297

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.264	0.076	0.085	0.027
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

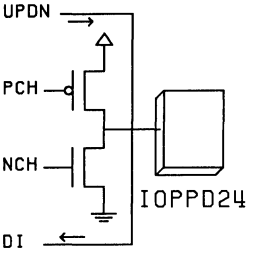
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

IOPPD24

24mA Input/Output Pad with Pullup/Pulldown Port

IOPPD24 is similar to IOPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 2.460
PCH: 2.360
UPDN: 54.094
PAD: 3.590 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.362 M_{CHL} = 0.113
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.029	0.055	0.057	0.064
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.949	1.80	1.87	2.11
t_{PHL}		0.945	1.77	1.85	2.07
t_{PLH}	UPDN to PAD	16.6	31.0	32.3	36.3
t_{PHL}		16.9	31.5	32.8	36.8

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.097	0.014
t_{PHL}		0.098	0.016
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.002	0.273
t_{PLH}	UPDN to PAD	2.10	0.287
t_{PHL}		2.12	0.294

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.237	0.055	0.074	0.020
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

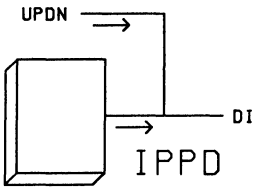
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

Input Pad with Pullup/Pulldown Port

IPPD is similar to INPD but includes an input port, UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See any PPU/PPD data sheet for pullup/pulldown current information.



Inputs: PAD, UPDN
Outputs: DI
Input Cap.: PAD: 3.460
UPDN: 53.464 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.030	0.055	0.058	0.065
t_{PHL}		0.031	0.057	0.060	0.067
t_{PLH}	UPDN to DI	16.1	30.1	31.3	35.2
t_{PHL}		15.9	29.6	30.9	34.6
Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	PAD to DI	0.003	0.267
t_{PHL}		0.004	0.267
t_{PLH}	UPDN to DI	16.1	0.293
t_{PHL}		14.7	11.5

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

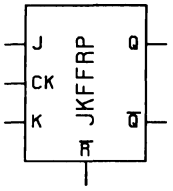
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DI	2.14	0.007	2.14	0.007

Rise/Fall time coefficients for the next cell

J–K Flip–Flop with Reset, Positive Edge Triggered

JKFFRP is a fully static JK-type edge triggered flip–flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.

Inputs: J, CK, K, RB
Outputs: Q, QB
Input Cap.: J: 0.034
CK: 0.124
K: 0.036
RB: 0.106 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.152 M_{CHL} = 0.231
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 19.0 grids wide, 11.9 grids high



FUNCTION TABLE

J	K	CK	RB	Q	QB
H	H	↑	H	QB_o	Q_o
H	L	↑	H	H	L
L	H	↑	H	L	H
L	L	↑	H	Q_o	QB_o
X	X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.08	2.05	2.14	2.40
t_{PHL}		1.35	2.54	2.65	2.98
t_{PLH}	CK to QB	0.464	0.876	0.913	1.03
t_{PHL}		0.400	0.762	0.795	0.895
t_{PLH}	RB to QB	2.72	5.10	5.32	5.97
t_{PHL}	RB to Q	0.831	1.57	1.63	1.84

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.376	1.91
t_{PHL}		0.397	1.59
t_{PLH}	CK to QB	0.233	1.67
t_{PHL}		0.140	1.63
t_{PLH}	RB to QB	1.08	7.15
t_{PHL}	RB to Q	0.519	2.15

Delay coefficients

JKFFRP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

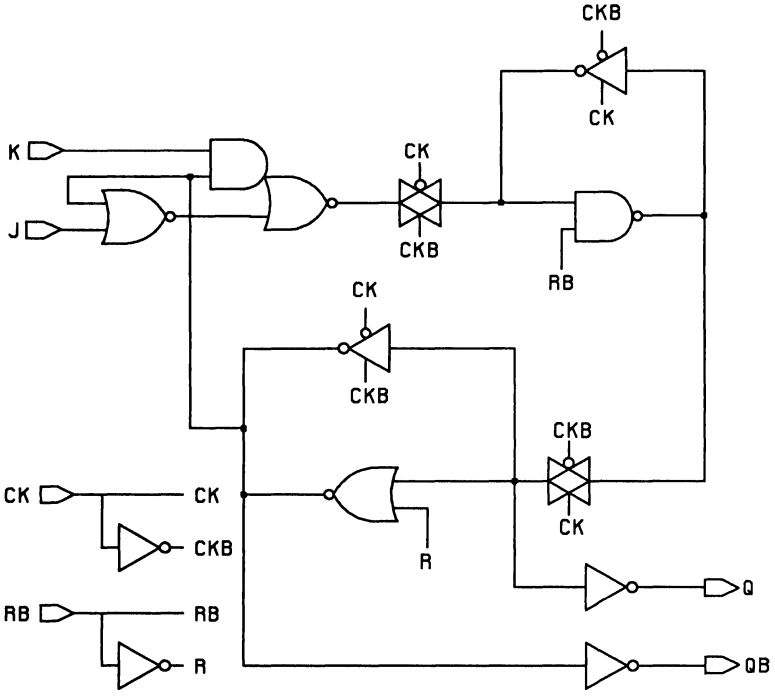
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.767	4.23	0.426	2.44
QB	0.920	5.85	0.417	4.32

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time J to CK	2.55	1.50	0.913
t_{su}	Setup Time K to CK	1.96	1.15	0.702
t_h	Hold Time CK to J	-1.041	-0.610	-0.373
t_h	Hold Time CK to K	0.989	0.580	0.354
t_{pwh}	Pulse Width (high) CK	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) CK	3.35	1.96	1.20
t_{pwl}	Pulse Width (low) RB	5.68	3.33	2.04
rt	Recovery Time RB	0.392	0.230	0.141

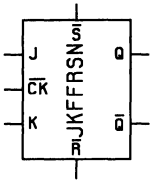
Timing requirements



Functional diagram: JKFFRP

J–K Flip–Flop with Reset and Set, Negative Edge Triggered

JKFFRSN is a fully static JK–type negative edge triggered flip–flop. SB and RB are asynchronous and active low. This cell is functionally compatible with TTL 74LS76. For a faster version of this cell, see JKFFRSNF.



Inputs: J, K, RB, SB, CKB
Outputs: Q, QB
Input Cap.: J: 0.044
K: 0.051
RB: 0.153
SB: 0.108
CKB: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.169 M_{CHL} = 0.171
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 23.0 grids wide, 13.4 grids high

FUNCTION TABLE

J	K	CKB	SB	RB	Q	QB
H	H	↓	H	H	QB_o	Q_o
H	L	↓	H	H	H	L
L	H	↓	H	H	L	H
L	L	↓	H	H	Q_o	QB_o
X	X	X	L	H	H	L
X	X	X	H	L	L	H
X	X	X	L	L	*	*

*Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CKB to QB	1.56	2.92	3.04	3.41
t_{PHL}		1.01	1.90	1.98	2.22
t_{PLH}	*CKB to Q	1.75	3.28	3.42	3.84
t_{PHL}		2.48	4.66	4.86	5.45
t_{PHL}	*RB to Q	1.67	3.14	3.27	3.68
t_{PLH}	RB to QB	0.698	1.32	1.37	1.54
t_{PHL}		0.620	1.17	1.22	1.37
t_{PLH}	SB to Q	0.552	1.04	1.09	1.22
t_{PHL}		0.567	1.07	1.12	1.25
t_{PHL}	*SB to QB	1.44	2.71	2.83	3.17

* The propagation delay from CKB to Q depends on the CKB to QB delay and rise/fall time. The delay from RB to Q depends on the RB to QB delay and rise/fall time. Also, the SB to QB delay depends on the SB to Q delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CKB to QB	1.21	2.74
t_{PHL}		0.740	1.98
t_{PLH}	QB to Q (CKB)	0.432	1.46
t_{PHL}		0.495	1.63
t_{PHL}	QB to Q (RB)	0.531	1.71
t_{PLH}	RB to QB	0.390	2.37
t_{PHL}		0.339	2.09
t_{PLH}	SB to Q	0.331	1.50
t_{PHL}		0.336	1.59
t_{PHL}	Q to QB (SB)	0.514	2.04

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.778	2.92	0.705	2.85
QB	1.07	5.81	0.592	4.21

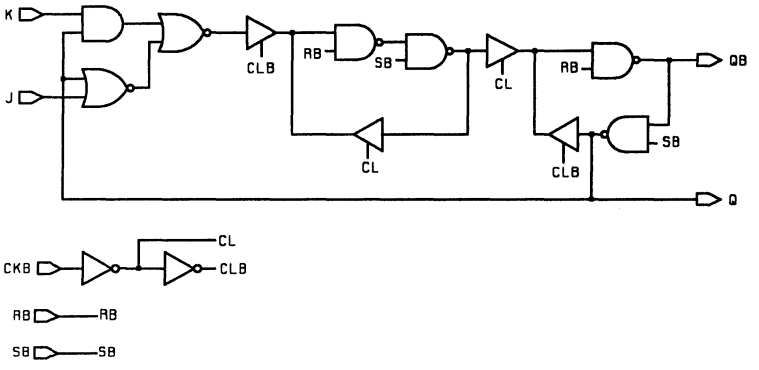
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time J to CKB	2.56	1.50	0.917
t_{su}	Setup Time K to CKB	1.57	0.920	0.563
t_h	Hold Time CKB to J	−0.444	−0.260	−0.159
t_h	Hold Time CKB to K	−0.291	−0.170	−0.104
t_{pwh}	Pulse Width (high) CKB	3.74	2.19	1.34
t_{pwl}	Pulse Width (low) RB	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) SB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CKB	5.31	3.11	1.90
rt	Recovery Time RB	0.171	0.100	0.061
rt	Recovery Time SB	−1.024	−0.600	−0.367

Timing requirements

JKFFRSN

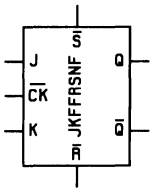


Functional diagram: JKFFRSN

Fast J–K Flip–Flop with Reset and Set, Negative Edge Triggered

JKFFRSNF is a fully static JK–type negative edge triggered flip–flop. SB and RB are asynchronous and active low. This cell is functionally compatible with TTL 74LS76.

Inputs: J, K, RB, SB, CKB
Outputs: Q, QB
Input Cap.: J: 0.061
K: 0.059
RB: 0.156
SB: 0.170
CKB: 0.082 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.166 M_{CHL} = 0.154
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 29.0 grids wide, 15.4 grids high



FUNCTION TABLE

J	K	CKB	SB	RB	Q	QB
H	H	↓	H	H	QB_o	Q_o
H	L	↓	H	H	H	L
L	H	↓	H	H	L	H
L	L	↓	H	H	Q_o	QB_o
X	X	X	L	H	H	L
X	X	X	H	L	L	H
X	X	X	L	L	*	*

*Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CKB to Q	0.836	1.57	1.64	1.84
t_{PHL}		1.00	1.88	1.96	2.20
t_{PLH}	CKB to QB	0.957	1.80	1.88	2.11
t_{PHL}		1.13	2.11	2.20	2.47
t_{PHL}	*RB to Q	1.13	2.14	2.23	2.50
t_{PLH}	RB to QB	0.281	0.536	0.559	0.629
t_{PHL}		0.265	0.506	0.528	0.594
t_{PLH}	SB to Q	0.289	0.552	0.576	0.648
t_{PHL}		0.263	0.502	0.523	0.589
t_{PHL}	*SB to QB	1.56	2.93	3.06	3.43

* The propagation delay from RB to Q depends on the RB to QB delay and rise/fall time. Also, the SB to QB delay depends on the SB to Q delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

JKFFRSNF

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CKB to Q	0.678	0.880
t_{PHL}		0.843	0.947
t_{PLH}	CKB to QB	0.787	1.01
t_{PHL}		0.950	1.11
t_{PHL}	QB to Q (RB)	0.683	1.08
t_{PLH}	RB to QB	0.119	0.920
t_{PHL}		0.124	0.767
t_{PLH}	SB to Q	0.123	0.967
t_{PHL}		0.123	0.753
t_{PHL}	Q to QB (SB)	1.10	1.15

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.286	1.82	0.302	1.25
QB	0.298	1.82	0.386	1.37

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time J to CKB	2.17	1.27	0.776
t_{su}	Setup Time K to CKB	1.57	0.920	0.563
t_h	Hold Time CKB to J	−0.597	−0.350	−0.214
t_h	Hold Time CKB to K	−0.597	−0.350	−0.214
t_{pwh}	Pulse Width (high) CKB	3.35	1.96	1.20
t_{pwl}	Pulse Width (low) RB	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) SB	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) CKB	3.14	1.84	1.12
rt	Recovery Time RB	−2.168	−1.270	−0.776
rt	Recovery Time SB	−2.168	−1.270	−0.776

Timing requirements

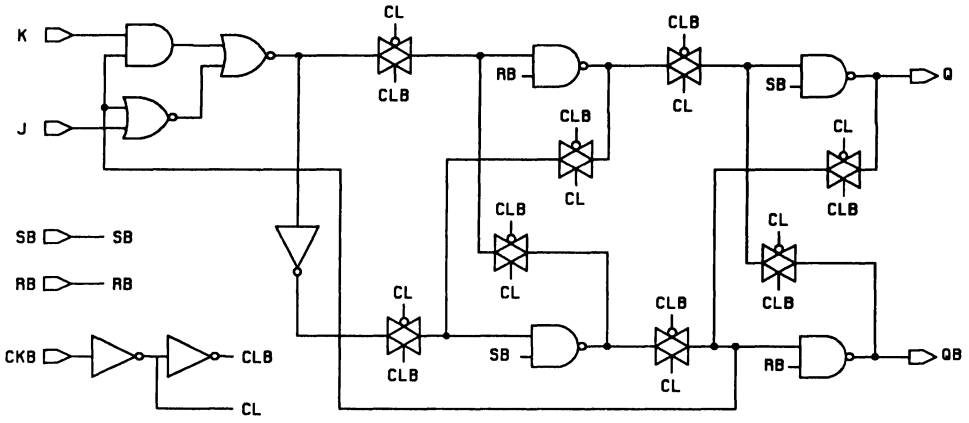
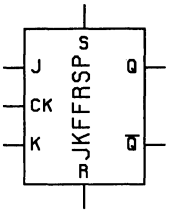


Figure 1 Functional diagram: JKFFRSNF

J–K Flip–Flop with Reset and Set, Positive Edge Triggered

JKFFRSP is a fully static JK–type edge triggered flip–flop. It is positive edge triggered with respect to CK. S and R are asynchronous, and active high. For a faster version of this cell, see JKFFRSPF.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK: 0.051
J: 0.044
K: 0.051
S: 0.131
R: 0.135 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.264 M_{CHL} = 0.269
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 27.0 grids wide, 13.4 grids high

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB_o	Q_o
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q_o	QB_o
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

*Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	2.30	4.32	4.50	5.06
t_{PHL}		1.96	3.68	3.83	4.31
t_{PLH}	CK to QB	1.45	2.72	2.84	3.19
t_{PHL}		1.85	3.47	3.62	4.06
t_{PHL}	R to Q	1.71	3.21	3.35	3.76
t_{PLH}	R to QB	1.22	2.29	2.39	2.68
t_{PHL}		1.84	3.46	3.60	4.04
t_{PLH}	S to Q	0.737	1.39	1.45	1.63
t_{PHL}		0.793	1.50	1.56	1.76
t_{PHL}	S to QB	2.33	4.37	4.55	5.11

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	2.07	1.27
t_{PHL}		1.71	1.39
t_{PLH}	CK to QB	1.17	1.64
t_{PHL}		1.51	2.23
t_{PHL}	R to Q	1.46	1.41
t_{PLH}	R to QB	0.927	1.78
t_{PHL}		1.50	2.24
t_{PLH}	S to Q	0.474	1.52
t_{PHL}		0.541	1.39
t_{PHL}	S to QB	2.01	2.07

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.272	2.63	0.264	1.67
QB	0.255	2.96	0.625	2.45

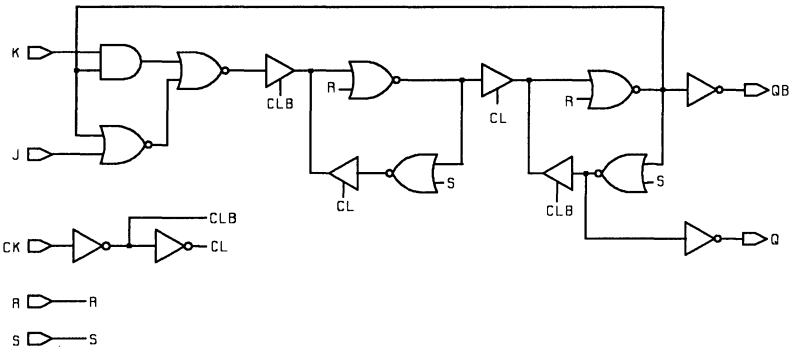
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time J to CK	3.35	1.96	1.20
t_{su}	Setup Time K to CK	2.17	1.27	0.776
t_h	Hold Time CK to J	−1.331	−0.780	−0.476
t_h	Hold Time CK to K	−0.153	−0.090	−0.055
t_{pwh}	Pulse Width (high) CK	4.71	2.76	1.69
t_{pwh}	Pulse Width (high) S	4.32	2.53	1.55
t_{pwh}	Pulse Width (high) R	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CK	4.52	2.65	1.62
rt	Recovery Time S	1.57	0.920	0.563
rt	Recovery Time R	−1.024	−0.600	−0.367

Timing requirements

JKFFRSP

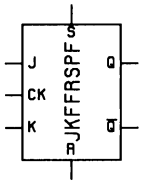


Functional diagram: JKFFRSP

Fast J–K Flip–Flop with Reset and Set, Positive Edge Triggered

JKFFRSPF is a fully static JK-type edge triggered flip-flop. It is positive edge triggered with respect to CK. S and R are asynchronous and active high.

Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK: 0.082
J: 0.061
K: 0.060
S: 0.051
R: 0.052 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.194 M_{CHL} = 0.265
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 32.0 grids wide, 15.4 grids high



FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB*	Q*
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q*	QB*
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

*Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.979	1.84	1.92	2.16
t_{PHL}		0.898	1.70	1.77	1.99
t_{PLH}	CK to QB	1.03	1.93	2.02	2.27
t_{PHL}		1.12	2.11	2.20	2.48
t_{PHL}	*R to Q	1.48	2.80	2.92	3.28
t_{PLH}	R to QB	0.619	1.17	1.22	1.37
t_{PHL}		0.664	1.26	1.31	1.48
t_{PLH}	S to Q	0.602	1.14	1.19	1.33
t_{PHL}		0.726	1.37	1.43	1.61
t_{PHL}	*S to QB	1.99	3.74	3.90	4.38

* The propagation delay from R to Q depends on the R to QB delay and rise/fall time. Also, the S to QB delay depends on the S to Q delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

JKFFRSPF

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.804	0.940
t_{PHL}		0.699	0.880
t_{PLH}	CK to QB	0.847	1.01
t_{PHL}		0.884	1.27
t_{PHL}	QB to Q (R)	0.661	1.10
t_{PLH}	R to QB	0.442	0.953
t_{PHL}		0.465	0.880
t_{PLH}	S to Q	0.417	1.04
t_{PHL}		0.519	0.953
t_{PHL}	Q to QB (S)	1.14	1.30

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

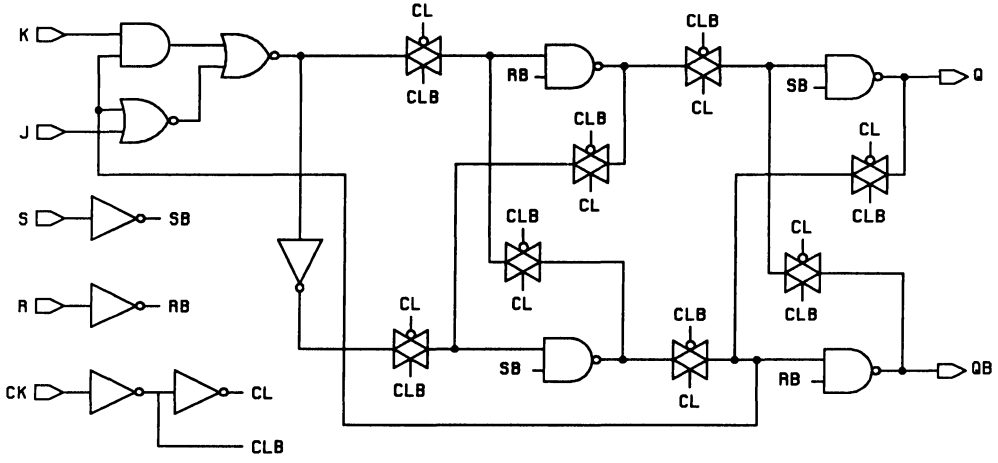
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.322	1.75	0.243	1.31
QB	0.254	1.83	0.366	1.61

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time J to CK	2.35	1.38	0.843
t_{su}	Setup Time K to CK	1.77	1.04	0.635
t_h	Hold Time CK to J	−1.041	−0.610	−0.373
t_h	Hold Time CK to K	−0.153	−0.090	−0.055
t_{pwh}	Pulse Width (high) CK	3.14	1.84	1.12
t_{pwh}	Pulse Width (high) S	5.10	2.99	1.83
t_{pwh}	Pulse Width (high) R	4.71	2.76	1.69
t_{pwl}	Pulse Width (low) CK	3.35	1.96	1.20
rt	Recovery Time S	−1.383	−0.810	−0.495
rt	Recovery Time R	−1.383	−0.810	−0.495

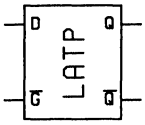
Timing requirements



Functional diagram: JKFFRSPF

Transparent Latch, Positive Edge Triggered

LATP holds data when GB is high and is transparent when GB is low. For a faster version of this cell, see LATPF.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: D: 0.056
GB: 0.033 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.269 M_{CHL} = 0.319
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 10.4 grids high

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q₀	QB₀

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*GB to Q	1.33	2.52	2.63	2.96
t_{PHL}		2.01	3.80	3.96	4.45
t_{PLH}	GB to QB	1.28	2.41	2.51	2.82
t_{PHL}		0.796	1.51	1.57	1.77
t_{PLH}	*D to Q	1.05	2.01	2.09	2.35
t_{PHL}		1.56	2.95	3.07	3.45
t_{PLH}	D to QB	0.799	1.51	1.57	1.77
t_{PHL}		0.521	0.995	1.04	1.17

* The propagation delay from D to Q depends on the D to QB delay and rise/fall time. Also, the GB to Q delay depends on the GB to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	QB to Q (GB)	0.221	1.44
t_{PHL}		0.172	1.23
t_{PLH}	GB to QB	0.922	2.47
t_{PHL}		0.517	1.45
t_{PLH}	QB to Q (D)	0.218	1.44
t_{PHL}		0.200	1.23
t_{PLH}	D to QB	0.421	2.65
t_{PHL}		0.234	1.53

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

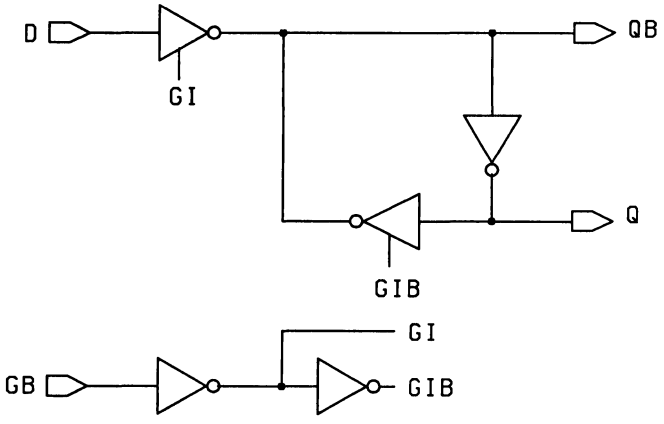
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.315	2.93	0.317	1.61
QB	0.867	5.76	0.432	2.77

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	2.17	1.27	0.776
t_h	Hold Time GB to D	-0.597	-0.350	-0.214
t_{pwl}	Pulse Width (low) GB	4.52	2.65	1.62

Timing requirements

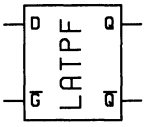


Functional diagram: LATP

Fast Transparent Latch, Positive Edge Triggered

LATPF holds data when GB is high and is transparent when GB is low.

Inputs: D, GB
Outputs: Q, QB
Input Cap.: D: 0.060
GB: 0.108 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.250 M_{CHL} = 0.244
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.0 grids wide, 11.4 grids high



FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q_o	QB_o

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	0.574	1.09	1.14	1.28
t_{PHL}		0.638	1.21	1.26	1.42
t_{PLH}	GB to QB	0.953	1.80	1.87	2.10
t_{PHL}		0.895	1.69	1.76	1.98
t_{PLH}	D to Q	0.643	1.22	1.27	1.43
t_{PHL}		0.703	1.33	1.39	1.56
t_{PLH}	D to QB	1.02	1.92	2.00	2.25
t_{PHL}		0.964	1.82	1.89	2.13

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.346	1.23
t_{PHL}		0.403	1.33
t_{PLH}	GB to QB	0.743	1.05
t_{PHL}		0.683	1.10
t_{PLH}	D to Q	0.415	1.23
t_{PHL}		0.467	1.33
t_{PLH}	D to QB	0.811	1.03
t_{PHL}		0.754	1.07

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

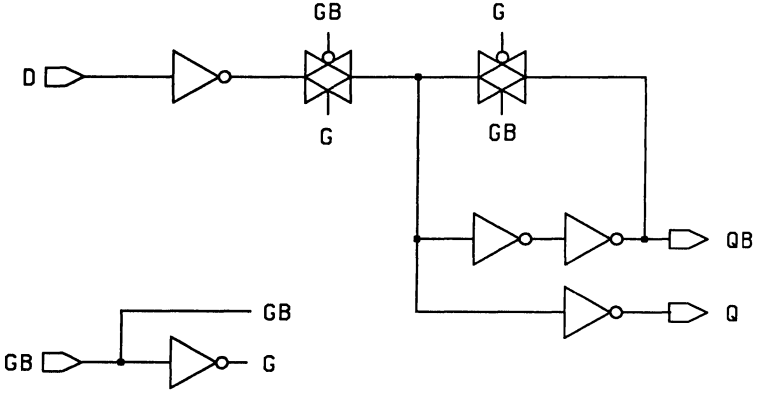
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.190	2.20	0.189	1.75
QB	0.192	2.08	0.171	1.54

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.38	0.810	0.495
t_h	Hold Time GB to D	−0.444	−0.260	−0.159
t_{pwl}	Pulse Width (low) GB	3.14	1.84	1.12

Timing requirements

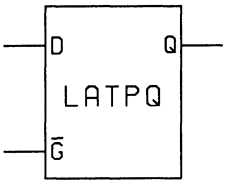


Functional diagram: LATPF

Transparent Latch, Positive Edge Triggered

LATPQ holds data when GB is high and is transparent when GB is low.

Inputs: D, GB
Outputs: Q
Input Cap.: D: 0.056
GB: 0.079 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.286 M_{CHL} = 0.263
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 9.4 grids high



FUNCTION TABLE

D	GB	Q
L	L	L
H	L	H
X	H	Q_o

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	0.853	1.61	1.68	1.89
t_{PHL}		0.681	1.29	1.35	1.51
t_{PLH}	D to Q	0.688	1.30	1.36	1.53
t_{PHL}		0.800	1.51	1.58	1.77

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.592	1.41
t_{PHL}		0.454	1.17
t_{PLH}	D to Q	0.423	1.45
t_{PHL}		0.564	1.26

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

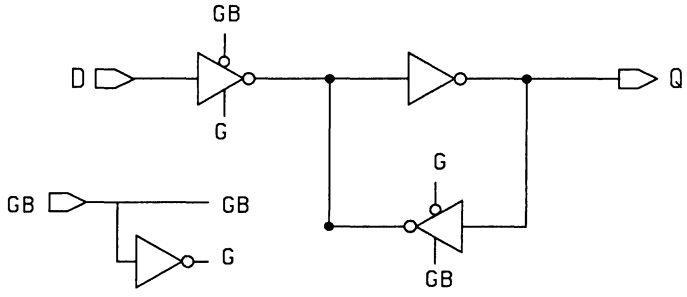
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.269	2.89	0.253	1.61

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD} =4.5V T_A =70C	NOMINAL V_{DD} =5.0V T_A =25C	BEST V_{DD} =5.5V T_A =0C
t_{su}	Setup Time D to GB	1.55	0.910	0.556
t_h	Hold Time GB to D	-0.733	-0.430	-0.263
t_{pwl}	Pulse Width (low) GB	2.93	1.725	1.05

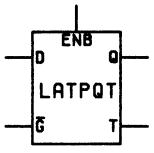
Timing requirements



Functional diagram: LATPQ

Transparent Latch with Tristate, Positive Edge Triggered

LATPQT holds data when GB is high and is transparent when GB is low. When ENB is high, the T output is in a Hi-Z state and Q functions as on a standard latch. When ENB is low, T equals Q.



Inputs: ENB, D, GB
Outputs: Q, T
Input Cap.: ENB: 0.063
D: 0.056
GB: 0.073 pF
Output Cap.: T: 0.028 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.304 M_{CHL} = 0.300
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.0 grids wide, 10.4 grids high

FUNCTION TABLE

D	GB	ENB	Q	T
L	L	L	L	L
H	L	L	H	H
X	H	L	Q_o	T_o
L	L	H	L	Hiz
H	L	H	H	Hiz
X	H	H	Q_o	Hiz

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to T	0.504	0.963	1.00	1.13
t_{PHL}		0.471	0.901	0.940	1.06
t_{PLH}	GB to Q	0.871	1.65	1.72	1.93
t_{PHL}		0.852	1.61	1.68	1.89
t_{PLH}	GB to T	1.07	2.01	2.10	2.36
t_{PHL}		0.908	1.72	1.79	2.01
t_{PLH}	D to Q	0.784	1.48	1.55	1.74
t_{PHL}		0.965	1.82	1.90	2.14
t_{PLH}	D to T	0.987	1.86	1.94	2.18
t_{PHL}		1.03	1.95	2.03	2.28

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to T	0.122	2.55
t_{PHL}		0.196	1.49
t_{PLH}	GB to Q	0.589	1.54
t_{PHL}		0.556	1.70
t_{PLH}	GB to T	0.680	2.60
t_{PHL}		0.593	1.89
t_{PLH}	D to Q	0.502	1.54
t_{PHL}		0.691	1.48
t_{PLH}	D to T	0.593	2.66
t_{PHL}		0.734	1.71

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.263	2.88	0.321	1.67
T	0.271	5.99	0.311	2.12

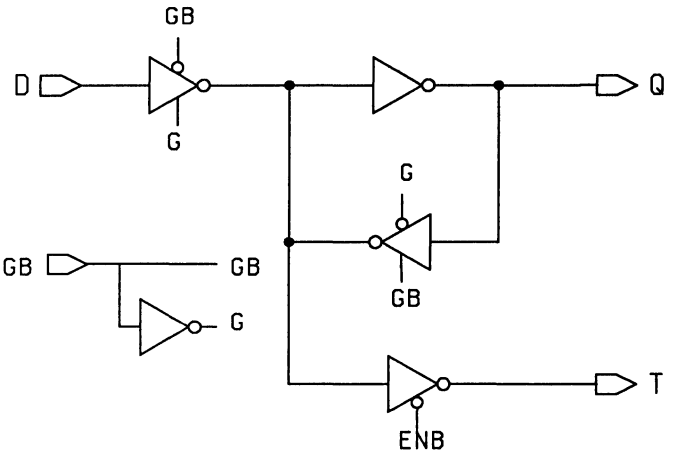
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.77	1.04	0.635
t_h	Hold Time GB to D	−0.291	−0.170	−0.104
t_{pwl}	Pulse Width (low) GB	3.35	1.96	1.20

Timing requirements

LATPQT

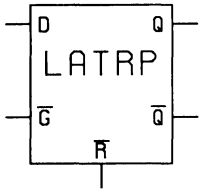


Functional diagram: LATPQT

Transparent Latch with Reset, Positive Edge Triggered

LATRP holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. For a faster version of this cell, see LATRPF.

Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.070
D: 0.046
GB: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.230 M_{CHL} = 0.174
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.0 grids wide, 11.4 grids high



FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q₀	QB₀
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*GB to Q	1.47	2.77	2.89	3.25
t_{PHL}		2.08	3.90	4.07	4.57
t_{PLH}	GB to QB	1.45	2.72	2.84	3.19
t_{PHL}		0.764	1.44	1.50	1.69
t_{PLH}	*D to Q	1.24	2.34	2.44	2.74
t_{PHL}		1.69	3.18	3.32	3.73
t_{PLH}	D to QB	1.06	1.99	2.07	2.33
t_{PHL}		0.563	1.06	1.11	1.25
t_{PLH}	*RB to Q	1.25	2.37	2.47	2.78
t_{PHL}		1.30	2.46	2.56	2.88
t_{PLH}	RB to QB	0.667	1.26	1.32	1.48
t_{PHL}		0.565	1.07	1.11	1.25

* The propagation delay from D to Q depends on the D to QB delay and rise/fall time. The GB to Q delay depends on the GB to QB delay and rise/fall time. Also, the RB to Q delay depends on the RB to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

LATRP

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	QB to Q (GB)	0.273	2.39
t_{PHL}		0.153	1.40
t_{PLH}	GB to QB	0.953	4.01
t_{PHL}		0.500	1.91
t_{PLH}	QB to Q (D)	0.281	2.02
t_{PHL}		0.156	1.47
t_{PLH}	D to QB	0.567	3.92
t_{PHL}		0.300	1.90
t_{PLH}	QB to Q (RB)	0.280	2.16
t_{PHL}		0.175	1.27
t_{PLH}	RB to QB	0.351	2.19
t_{PHL}		0.294	1.98

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

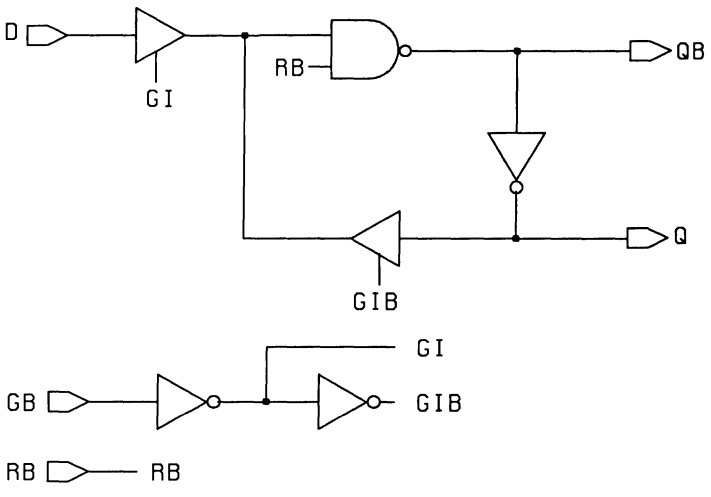
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.398	4.43	0.361	1.65
QB	1.12	8.69	0.537	3.83

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	2.75	1.61	0.984
t_h	Hold Time GB to D	−1.639	−0.960	−0.587
t_{pwl}	Pulse Width (low) RB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) GB	5.31	3.11	1.90
rt	Recovery Time RB	1.96	1.15	0.702

Timing requirements

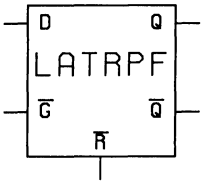


Functional diagram: LATRP

LATRPF

Fast Transparent Latch with Reset, Positive Edge Triggered

LATRPF holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.149
D: 0.080
GB: 0.127 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.258 M_{CHL} = 0.269
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.0 grids wide, 12.4 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q$_o$	QB$_o$
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	0.614	1.16	1.21	1.37
t_{PHL}		0.586	1.11	1.16	1.30
t_{PLH}	GB to QB	0.911	1.72	1.79	2.01
t_{PHL}		0.866	1.64	1.71	1.92
t_{PLH}	D to Q	0.689	1.30	1.36	1.53
t_{PHL}		0.786	1.49	1.55	1.74
t_{PLH}	D to QB	1.12	2.11	2.20	2.47
t_{PHL}		0.943	1.78	1.85	2.08
t_{PLH}	RB to Q	0.679	1.29	1.34	1.51
t_{PHL}		1.55	2.91	3.03	3.40
t_{PLH}	RB to QB	0.561	1.07	1.11	1.25
t_{PHL}		0.936	1.77	1.84	2.07

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.381	1.25
t_{PHL}		0.369	1.04
t_{PLH}	GB to QB	0.713	0.893
t_{PHL}		0.662	0.913
t_{PLH}	D to Q	0.456	1.25
t_{PHL}		0.556	1.17

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to QB	0.917	0.947
t_{PHL}		0.739	0.907
t_{PLH}	RB to Q	0.445	1.26
t_{PHL}		1.27	1.63
t_{PLH}	RB to QB	0.282	1.71
t_{PHL}		0.728	0.953

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

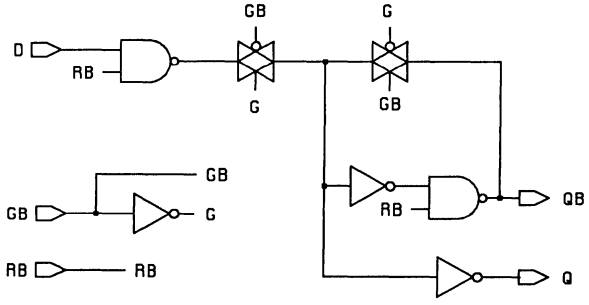
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.180	2.31	0.180	1.37
QB	0.206	2.17	0.189	1.54

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.57	0.920	0.563
t_h	Hold Time GB to D	−0.444	−0.260	−0.159
t_{pwl}	Pulse Width (low) RB	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) GB	3.14	1.84	1.12
rt	Recovery Time RB	1.35	0.790	0.483

Timing requirements



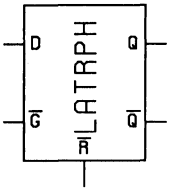
Functional diagram: LATRPF

LATRPH

D Latch with Reset and Enable (High Drive)

LATRPH holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.

Inputs: D, GB, RB
Outputs: Q, QB
Input Cap.: D: 0.048
GB: 0.034
RB: 0.070 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.371 M_{CHL} = 0.415
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 15.0 grids wide, 10.4 grids high



FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.15	2.17	2.27	2.55
t_{PHL}		1.83	3.45	3.59	4.04
t_{PLH}	GB to QB	2.25	4.23	4.41	4.95
t_{PHL}		1.75	3.29	3.43	3.86
t_{PLH}	D to Q	0.939	1.78	1.85	2.08
t_{PHL}		1.41	2.67	2.78	3.12
t_{PLH}	D to QB	1.82	3.43	3.58	4.02
t_{PHL}		1.53	2.88	3.00	3.37
t_{PLH}	RB to Q	0.952	1.80	1.88	2.11
t_{PHL}		0.978	1.85	1.93	2.17
t_{PLH}	RB to QB	1.34	2.53	2.64	2.97
t_{PHL}		1.53	2.89	3.01	3.38

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.903	0.920
t_{PHL}		1.57	0.913
t_{PLH}	GB to QB	2.07	0.273
t_{PHL}		1.51	0.633
t_{PLH}	D to Q	0.692	0.907
t_{PHL}		1.14	0.993
t_{PLH}	D to QB	1.63	0.380

Delay coefficients (Sheet 1 of 2)

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		1.29	0.587
t_{PLH}	RB to Q	0.705	0.907
t_{PHL}		0.712	0.913
t_{PLH}	RB to QB	1.13	0.580
t_{PHL}		1.29	0.680

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

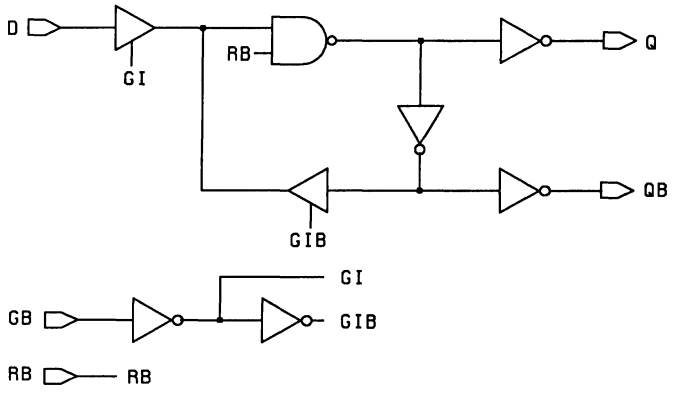
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.295	1.42	0.516	1.03
QB	0.239	1.35	0.266	0.847

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	2.17	1.27	0.776
t_h	Hold Time GB to D	−0.733	−0.430	−0.263
t_{pwl}	Pulse Width (low) GB	4.71	2.76	1.69
t_{pwl}	Pulse Width (low) RB	3.74	2.19	1.34
rt	Recovery Time RB	1.57	0.920	0.563

Timing requirements

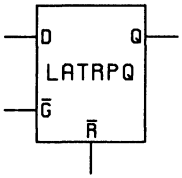


Functional diagram: LATRPH

Transparent Latch with Reset, Positive Edge Triggered

LATRPQ holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.

Inputs: D, GB, RB
Outputs: Q
Input Cap.: D: 0.046
GB: 0.081
RB: 0.070 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.291 M_{CHL} = 0.248
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 9.9 grids high



FUNCTION TABLE

D	GB	RB	Q
L	L	H	L
H	L	H	H
X	H	H	Q_o
X	X	L	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.07	2.01	2.10	2.36
t_{PHL}		0.888	1.68	1.75	1.96
t_{PLH}	D to Q	0.924	1.75	1.82	2.05
t_{PHL}		1.00	1.89	1.97	2.22
t_{PLH}	RB to Q	0.937	1.77	1.85	2.07
t_{PHL}		0.770	1.45	1.52	1.70

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.730	2.15
t_{PHL}		0.644	1.40
t_{PLH}	D to Q	0.586	2.16
t_{PHL}		0.758	1.43
t_{PLH}	RB to Q	0.598	2.17
t_{PHL}		0.537	1.29

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

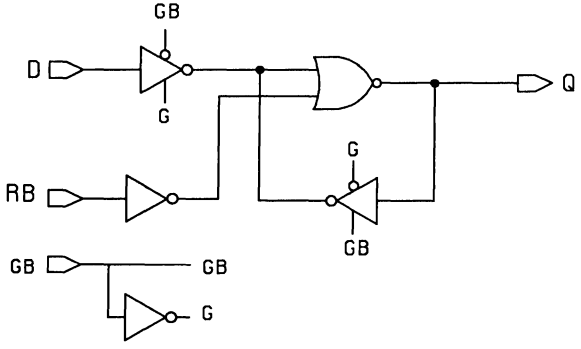
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.406	4.37	0.356	1.65

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	2.17	1.27	0.776
t_h	Hold Time GB to D	-1.177	-0.690	-0.422
t_{pwl}	Pulse Width (low) GB	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) RB	3.35	1.96	1.20
rt	Recovery Time RB	1.38	0.810	0.495

Timing requirements

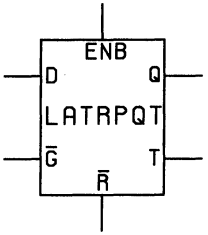


Functional diagram: LATRPQ

Transparent Latch with Reset and Tristate, Positive Edge Triggered

LATRPQT holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. When ENB is high, the T output is in a Hi-Z state and Q functions as a normal latch using any of the given states defined for Q in the FUNCTION TABLE.

Inputs: ENB, D, GB, RB
Outputs: Q, T
Input Cap.: ENB: 0.075
D: 0.046
GB: 0.081
RB: 0.070 pF
Output Cap.: T: 0.032 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.448 M_{CHL} = 0.487
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.0 grids wide, 10.2 grids high



FUNCTION TABLE

D	GB	RB	ENB	Q	T
L	L	H	L	L	L
H	L	H	L	H	H
X	H	H	L	Q_o	T_o
X	X	L	L	L	L
L	L	H	H	L	Hiz
H	L	H	H	H	Hiz
X	H	H	H	Q_o	Hiz
X	X	L	H	L	Hiz

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.34	2.53	2.64	2.96
t_{PHL}		1.26	2.38	2.49	2.79
t_{PLH}	GB to T	1.21	2.30	2.39	2.69
t_{PHL}		1.39	2.64	2.75	3.09
t_{PLH}	D to Q	1.20	2.27	2.37	2.66
t_{PHL}		1.41	2.66	2.77	3.12
t_{PLH}	D to T	1.09	2.07	2.16	2.43
t_{PHL}		1.54	2.91	3.03	3.41
t_{PLH}	RB to Q	1.21	2.29	2.39	2.68
t_{PHL}		1.05	2.00	2.08	2.34
t_{PLH}	RB to T	1.10	2.09	2.18	2.45
t_{PHL}		1.17	2.22	2.31	2.60
t_{PLH}	ENB to T	0.498	0.962	1.00	1.13
t_{PHL}		0.553	1.07	1.11	1.25

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.921	2.29
t_{PHL}		0.876	1.78
t_{PLH}	GB to T	0.820	2.05
t_{PHL}		1.01	1.78
t_{PLH}	D to Q	0.786	2.24
t_{PHL}		1.02	1.78
t_{PLH}	D to T	0.701	2.03
t_{PHL}		1.16	1.79
t_{PLH}	RB to Q	0.794	2.27
t_{PHL}		0.700	1.48
t_{PLH}	RB to T	0.710	2.05
t_{PHL}		0.795	1.69
t_{PLH}	ENB to T	0.119	1.91
t_{PHL}		0.194	1.55

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.476	4.29	0.516	1.77
T	0.245	4.47	0.337	2.23

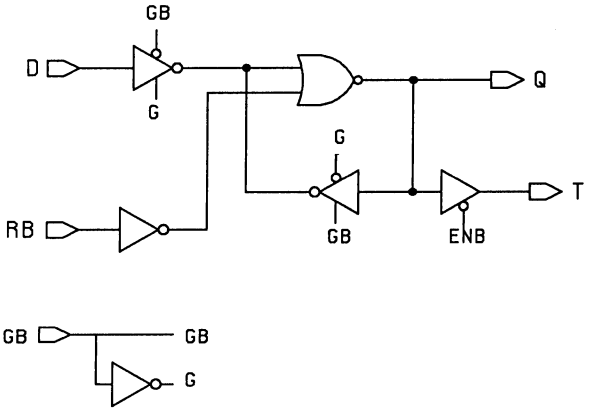
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	2.56	1.50	0.917
t_h	Hold Time GB to D	-1.639	-0.960	-0.587
t_{pwl}	Pulse Width (low) GB	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) RB	3.74	2.19	1.34
rt	Recovery Time RB	1.57	0.920	0.563

Timing requirements

LATRPQT

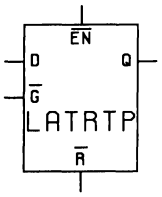


Functional diagram: LATRPQT

Transparent Latch with Reset, Tristate, Positive Edge Triggered

LATRTP holds data when GB is high and is transparent when GB is low. RB is asynchronous with respect to GB and active low. When ENB is high, the output is in a Hi-Z state.

Inputs: ENB, D, GB, RB
Outputs: Q
Input Cap.: ENB: 0.068
D: 0.046
GB: 0.034
RB: 0.071 pF
Output Cap.: Q: 0.044 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.154 M_{CHL} = 0.206
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 13.0 grids wide, 10.4 grids high



FUNCTION TABLE

D	GB	RB	ENB	Q
L	L	H	L	L
H	L	H	L	H
X	H	H	L	Q_0
X	X	L	L	L
X	X	X	H	Z

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to Q	1.05	1.97	2.06	2.31
t_{PHL}		1.18	2.22	2.32	2.60
t_{PLH}	GB to Q	1.24	2.33	2.43	2.72
t_{PHL}		1.58	2.97	3.10	3.48
t_{PLH}	RB to Q	1.06	1.98	2.07	2.32
t_{PHL}		0.856	1.61	1.68	1.89
t_{PLH}	ENB to Q	0.521	0.984	1.03	1.15
t_{PHL}		0.433	0.822	0.857	0.964

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to Q	0.705	2.81
t_{PHL}		0.914	1.81
t_{PLH}	GB to Q	0.897	2.79
t_{PHL}		1.34	1.57
t_{PLH}	RB to Q	0.713	2.79
t_{PHL}		0.614	1.55
t_{PLH}	ENB to Q	0.202	2.55
t_{PHL}		0.244	1.02

Delay coefficients

LATRTP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

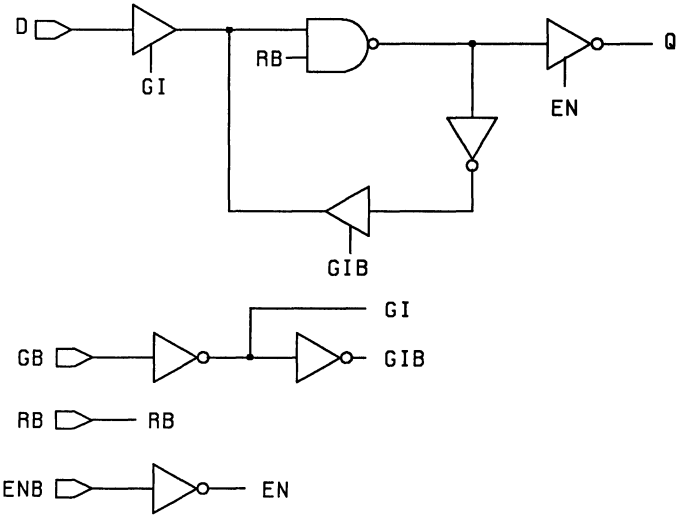
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.302	5.91	0.099	1.87

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.57	0.920	0.563
t_h	Hold Time GB to D	−0.444	−0.260	−0.159
t_{pwl}	Pulse Width (low) GB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) RB	3.35	1.96	1.20
rt	Recovery Time RB	1.35	0.790	0.483

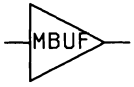
Timing requirements



Functional diagram: LATRTP

Medium Drive Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.035 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.217
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 10.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.462	0.873	0.911	1.02
t_{PHL}		0.522	0.990	1.03	1.16

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.287	1.08
t_{PHL}		0.320	1.11

Delay coefficients

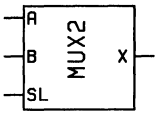
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.144	2.15	0.120	1.65

Rise/Fall time coefficients for the next cell

2–Input Multiplexer

Inputs: SL, A, B
Outputs: X
Input Cap.: SL: 0.086
A: 0.054
B: 0.056 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.275 M_{CHL} = 0.177
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 9.4 grids high



FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.739	1.40	1.46	1.64
t_{PHL}		0.749	1.41	1.47	1.65
t_{PLH}	SL to X	0.812	1.53	1.60	1.80
t_{PHL}		0.979	1.84	1.92	2.15
* Slowest of A or B inputs					

Timing characteristics

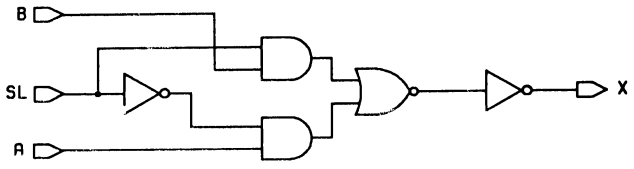
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.408	2.15
t_{PHL}		0.451	2.23
t_{PLH}	SL to X	0.478	2.18
t_{PHL}		0.681	2.24

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.175	4.28	0.190	3.22

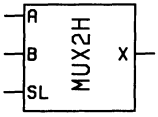
Rise/Fall time coefficients for the next cell



Functional diagram: MUX2

2–Input Multiplexer (High Drive)

Inputs: A, SL, B
Outputs: X
Input Cap.: A: 0.060
SL: 0.095
B: 0.060 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.260 M_{CHL} = 0.226
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 10.4 grids high



FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.631	1.20	1.25	1.40
t_{PHL}		0.690	1.30	1.36	1.53
t_{PLH}	SL to X	0.627	1.19	1.24	1.39
t_{PHL}		0.683	1.29	1.35	1.51
* Slowest of A or B inputs					

Timing characteristics

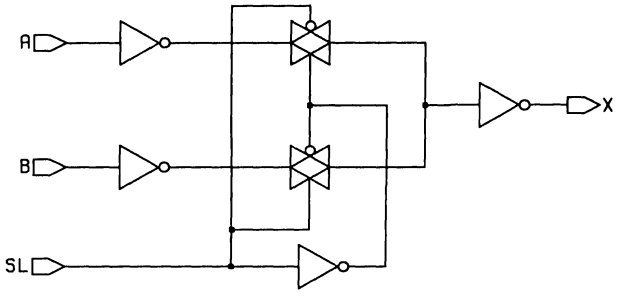
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.435	0.867
t_{PHL}		0.496	0.987
t_{PLH}	SL to X	0.429	0.887
t_{PHL}		0.481	1.07

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.211	1.39	0.231	1.18

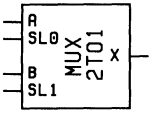
Rise/Fall time coefficients for the next cell



Functional diagram: MUX2H

2–Input Multiplexer with Separate Selects

In normal operation, SL1 and SL0 are complementary signals and X = A when SL0 is high and X = B when SL1 is high.



Inputs: SL1, SL0, A, B
Outputs: X
Input Cap.: SL1: 0.055
SL0, A: 0.056
B: 0.054 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.210 M_{CHL} = 0.194
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 8.9 grids high

FUNCTION TABLE

SL1	SL0	X
L	L	L
L	H	A
H	L	B
H	H	A + B

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A,B to X	0.719	1.36	1.41	1.59
t_{PHL}		0.754	1.42	1.48	1.66
t_{PLH}	SL1,SL0 to X	0.686	1.30	1.35	1.52
t_{PHL}		0.879	1.66	1.73	1.94

Timing characteristics

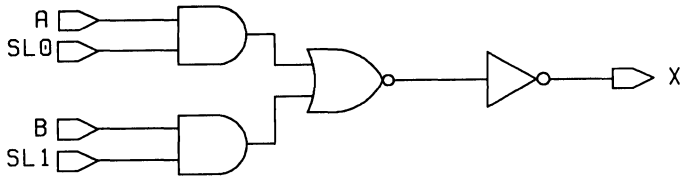
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A,B to X	0.418	2.13
t_{PHL}		0.452	2.21
t_{PLH}	SL1,SL0 to X	0.383	2.15
t_{PHL}		0.576	2.22

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.177	4.24	0.189	3.21

Rise/Fall time coefficients for the next cell

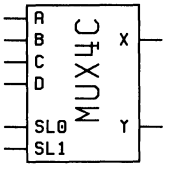


Functional diagram: MUX2TO1

4–Input Multiplexer with Complementary Outputs

SL0 and SL1 cause one of A, B, C, or D to be propagated to the outputs.

Inputs: A, B, C, D, SL0, SL1
Outputs: X, Y
Input Cap.: A, B, C, D: 0.056
SL0, SL1: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.114 M_{CHL} = 0.229
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 20.0 grids wide, 11.4 grids high



FUNCTION TABLE

SL0	SL1	X	Y
L	L	A	$\bar{A}$
H	L	B	$\bar{B}$
L	H	C	$\bar{C}$
H	H	D	$\bar{D}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.902	1.69	1.76	1.98
t_{PHL}		1.27	2.38	2.48	2.79
t_{PLH}	*IN to Y***	1.66	3.12	3.25	3.65
t_{PHL}		1.39	2.62	2.73	3.07
t_{PLH}	**SL to X	1.05	1.96	2.05	2.30
t_{PHL}		1.24	2.33	2.43	2.73
t_{PLH}	**SL to Y	1.63	3.07	3.20	3.59
t_{PHL}		1.53	2.89	3.01	3.38

* Slowest of A,B,C, or D inputs
** SL timing applies to both SL0 and SL1
*** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

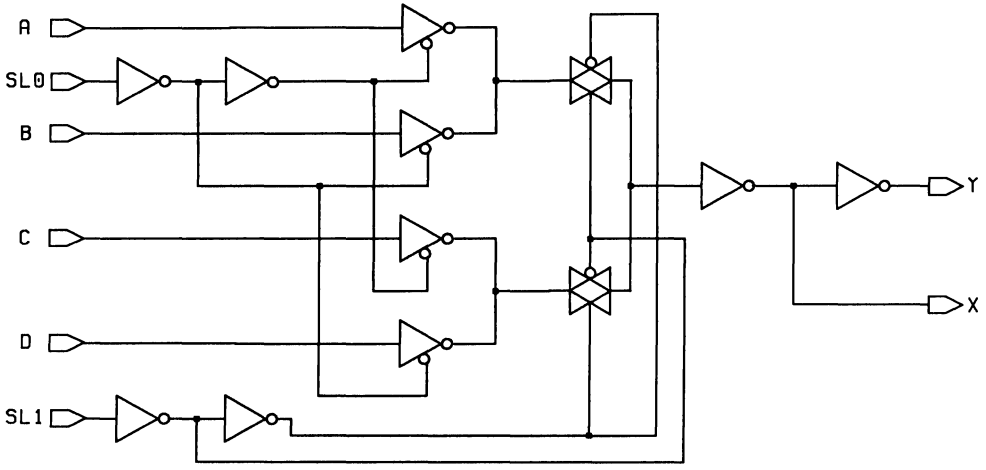
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.633	2.21
t_{PHL}		0.931	2.41
t_{PLH}	X to Y (IN)	0.103	2.06
t_{PHL}		0.124	1.98
t_{PLH}	**SL to X	0.761	2.39
t_{PHL}		0.906	2.40
t_{PLH}	X to Y (SL)	0.099	2.09
t_{PHL}		0.127	1.92

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

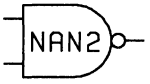
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.383	4.27	0.458	3.30
Y	0.169	4.28	0.120	3.24

Rise/Fall time coefficients for the next cell



Functional diagram: MUX4C

2–Input NAND Gate



Inputs: A, B
Outputs: X
Input Cap.: A: 0.046
B: 0.042 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.244 M_{CHL} = 0.158
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 8.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.458	0.871	0.909	1.02
t_{PHL}		0.305	0.580	0.606	0.681
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.148	2.07
t_{PHL}		0.088	1.51

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.231	4.43	0.080	2.78

Rise/Fall time coefficients for the next cell

2–Input NAND Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.043
B: 0.045 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.278 M_{CHL} = 0.140
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 8.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.496	0.945	0.986	1.11
t_{PHL}		0.338	0.640	0.668	0.751
t_{PLH}	*IN to Y**	0.757	1.44	1.51	1.69
t_{PHL}		0.930	1.76	1.84	2.07

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.171	2.08
t_{PHL}		0.127	1.52
t_{PLH}	X to Y	0.095	2.11
t_{PHL}		0.134	2.03

Delay coefficients

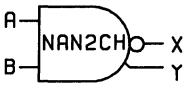
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.324	4.46	0.216	2.73
Y	0.122	4.39	0.105	3.25

Rise/Fall time coefficients for the next cell

2–Input NAND Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.099
B: 0.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.229 M_{CHL} = 0.188
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.331	0.634	0.661	0.744
t_{PHL}		0.401	0.761	0.794	0.892
t_{PLH}	*IN to Y**	0.686	1.31	1.37	1.54
t_{PHL}		0.581	1.11	1.16	1.31

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.162	0.727
t_{PHL}		0.223	0.987
t_{PLH}	X to Y	0.097	0.827
t_{PHL}		0.100	0.767

Delay coefficients

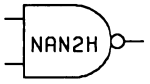
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.320	1.51	0.348	1.91
Y	0.136	1.40	0.084	1.12

Rise/Fall time coefficients for the next cell

2–Input NAND Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.099
B: 0.094 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.227 M_{CHL} = 0.188
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.263	0.507	0.529	0.596
t_{PHL}		0.307	0.586	0.612	0.688
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.097	0.707
t_{PHL}		0.140	0.880

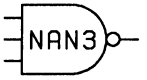
Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.154	1.49	0.114	1.88

Rise/Fall time coefficients for the next cell

3–Input NAND Gate



Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.056
B: 0.055
C: 0.051 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.258 M_{CHL} = 0.131
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.625	1.18	1.24	1.39
t_{PHL}		0.327	0.619	0.646	0.726
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.300	2.17
t_{PHL}		0.135	1.37

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.486	4.47	0.153	2.59

Rise/Fall time coefficients for the next cell

3–Input NAND Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: A: 0.043
B: 0.044
C: 0.045 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.299 M_{CHL} = 0.198
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.520	0.991	1.03	1.16
t_{PHL}		0.459	0.871	0.908	1.02
t_{PLH}	*IN to Y**	1.01	1.92	2.00	2.25
t_{PHL}		1.01	1.91	2.00	2.25

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.187	2.07
t_{PHL}		0.178	1.98
t_{PLH}	X to Y	0.135	2.15
t_{PHL}		0.138	2.04

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.375	4.39	0.360	3.83
Y	0.159	4.31	0.113	3.24

Rise/Fall time coefficients for the next cell

3–Input NAND Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A, B: 0.107
C: 0.110 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.259 M_{CHL} = 0.179
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 10.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.268	0.518	0.541	0.610
t_{PHL}		0.318	0.606	0.632	0.711
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.094	0.653
t_{PHL}		0.150	0.927

Delay coefficients

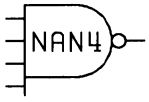
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.142	1.50	0.199	1.96

Rise/Fall time coefficients for the next cell

4–Input NAND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.065
B, C: 0.064
D: 0.061 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.263 M_{CHL} = 0.144
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 10.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.860	1.62	1.69	1.90
t_{PHL}		0.375	0.711	0.742	0.833
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.516	2.34
t_{PHL}		0.187	1.28

Delay coefficients

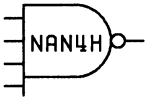
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.831	4.63	0.239	2.49

Rise/Fall time coefficients for the next cell

NAN4H

4–Input NAND Gate (High Drive)



Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.134
B: 0.129
C: 0.130
D: 0.135 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.231 M_{CHL} = 0.155
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.0 grids wide, 10.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.400	0.762	0.795	0.895
t_{PHL}		0.383	0.726	0.758	0.852
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.228	0.747
t_{PHL}		0.249	0.693

Delay coefficients

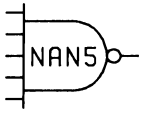
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.387	1.50	0.293	1.67

Rise/Fall time coefficients for the next cell

5–Input NAND Gate

Inputs: A, B, C, D, E
Outputs: X
Input Cap.: A: 0.066
B, C, D: 0.065
E: 0.061 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.250 M_{CHL} = 0.135
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.01	1.90	1.98	2.22
t_{PHL}		0.485	0.914	0.953	1.07
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.649	2.52
t_{PHL}		0.278	1.50

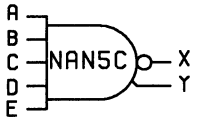
Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.11	4.77	0.387	3.01

Rise/Fall time coefficients for the next cell

5–Input NAND Gate with Complementary Outputs



Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: A: 0.066
B, C, D: 0.065
E: 0.061 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.204 M_{CHL} = 0.144
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 10.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.10	2.08	2.16	2.43
t_{PHL}		0.544	1.03	1.07	1.20
t_{PLH}	*IN to Y**	1.08	2.04	2.13	2.39
t_{PHL}		1.79	3.37	3.51	3.95

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.775	2.44
t_{PHL}		0.335	1.49
t_{PLH}	X to Y	0.151	2.28
t_{PHL}		0.201	2.37

Delay coefficients

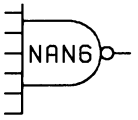
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.33	4.81	0.545	2.97
Y	0.202	4.32	0.375	2.89

Rise/Fall time coefficients for the next cell

6–Input NAND Gate

Inputs: A, B, C, D, E, F
Outputs: X
Input Cap.: A: 0.066
B, C, D, E: 0.065
F: 0.062 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.200 M_{CHL} = 0.144
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.13	2.13	2.22	2.50
t_{PHL}		0.609	1.15	1.20	1.34
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.785	2.65
t_{PHL}		0.373	1.76

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.41	4.93	0.570	3.55

Rise/Fall time coefficients for the next cell

2–Input NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.035
B: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.361 M_{CHL} = 0.179
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 7.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.715	1.36	1.42	1.59
t_{PHL}		0.387	0.736	0.768	0.863
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.188	3.75
t_{PHL}		0.119	1.93

Delay coefficients

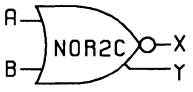
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.301	8.47	0.154	3.26

Rise/Fall time coefficients for the next cell

2–Input NOR Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.037
B: 0.036 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.381 M_{CHL} = 0.144
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 8.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.858	1.63	1.70	1.91
t_{PHL}		0.429	0.810	0.845	0.950
t_{PLH}	*IN to Y**	0.947	1.80	1.88	2.12
t_{PHL}		1.43	2.70	2.82	3.17

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.316	3.82
t_{PHL}		0.179	1.89
t_{PLH}	X to Y	0.106	2.08
t_{PHL}		0.150	2.18

Delay coefficients

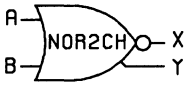
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.619	8.60	0.297	3.19
Y	0.127	4.33	0.178	3.21

Rise/Fall time coefficients for the next cell

2–Input NOR Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.123
B: 0.118 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.211 M_{CHL} = 0.145
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 10.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.435	0.827	0.862	0.969
t_{PHL}		0.324	0.614	0.641	0.720
t_{PLH}	*IN to Y**	0.553	1.06	1.10	1.24
t_{PHL}		0.715	1.36	1.42	1.59

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.243	1.03
t_{PHL}		0.196	0.667
t_{PLH}	X to Y	0.085	0.747
t_{PHL}		0.109	0.820

Delay coefficients

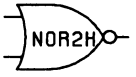
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.468	2.23	0.305	1.07
Y	0.133	1.34	0.119	1.12

Rise/Fall time coefficients for the next cell

2–Input NOR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.103
B: 0.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.227 M_{CHL} = 0.194
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.395	0.753	0.786	0.884
t_{PHL}		0.257	0.493	0.514	0.579
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.169	1.31
t_{PHL}		0.108	0.673

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.275	2.82	0.146	1.09

Rise/Fall time coefficients for the next cell

3–Input NOR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A, B: 0.056
C: 0.053 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.175 M_{CHL} = 0.163
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 9.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.690	1.30	1.36	1.52
t_{PHL}		0.558	1.05	1.10	1.23
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.333	2.83
t_{PHL}		0.279	2.11

Delay coefficients

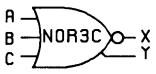
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.550	6.44	0.453	3.30

Rise/Fall time coefficients for the next cell

3–Input NOR Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: A, B: 0.047
C: 0.046 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 9.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.923	1.73	1.81	2.03
t_{PHL}		0.547	1.03	1.08	1.21
t_{PLH}	*IN to Y**	1.01	1.92	2.00	2.25
t_{PHL}		1.60	3.02	3.14	3.53

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.477	3.79
t_{PHL}		0.273	2.05
t_{PLH}	X to Y	0.138	2.14
t_{PHL}		0.170	2.36

Delay coefficients

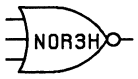
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.892	8.70	0.481	3.29
Y	0.183	4.21	0.242	3.25

Rise/Fall time coefficients for the next cell

3–Input NOR Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.110
B: 0.112
C: 0.105 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.165 M_{CHL} = 0.194
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 11.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.542	1.02	1.07	1.20
t_{PHL}		0.291	0.557	0.581	0.654
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.307	1.66
t_{PHL}		0.135	0.747

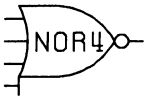
Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.510	3.63	0.224	1.18

Rise/Fall time coefficients for the next cell

4–Input NOR Gate



Inputs: A, B, C, D
Outputs: X
Input Cap.: A, B: 0.056
C: 0.057
D: 0.053 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.176 M_{CHL} = 0.173
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 9.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.997	1.87	1.95	2.19
t_{PHL}		0.613	1.16	1.21	1.36
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.550	3.73
t_{PHL}		0.312	2.29

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

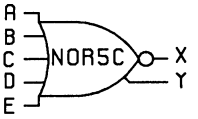
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.955	8.61	0.581	3.50

Rise/Fall time coefficients for the next cell

NOR5C

5–Input NOR Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: A: 0.056
B: 0.055
C, D: 0.057
E: 0.053 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.165 M_{CHL} = 0.142
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.0 grids wide, 9.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X**	2.18	4.09	4.27	4.79
t_{PHL}		1.45	2.73	2.84	3.19
t_{PLH}	*IN to Y	1.01	1.90	1.98	2.23
t_{PHL}		1.71	3.20	3.34	3.75

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	Y to X	0.117	2.09
t_{PHL}		0.121	2.01
t_{PLH}	A,B,C,D,E to Y	0.714	2.29
t_{PHL}		1.38	2.71

Delay coefficients

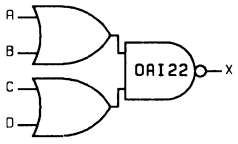
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.189	4.20	0.128	3.21
Y	0.464	4.23	0.616	3.39

Rise/Fall time coefficients for the next cell

2–2 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A, B: 0.046
C, D: 0.045 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.346 M_{CHL} = 0.151
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 8.4 grids high



$X = \overline{(A+B) \cdot (C+D)}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.07	2.03	2.11	2.37
t_{PHL}		0.422	0.798	0.833	0.936
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.541	3.86
t_{PHL}		0.216	1.43

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

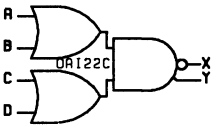
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.06	8.58	0.287	2.67

Rise/Fall time coefficients for the next cell

OAI22C

2–2 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.046
B: 0.045
C, D: 0.044 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.338 M_{CHL} = 0.150
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.0 grids wide, 8.4 grids high



$X = \overline{(A+B) \cdot (C+D)}$

$Y = (A+B) \cdot (C+D)$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.15	2.17	2.26	2.54
t_{PHL}		0.421	0.796	0.830	0.933
t_{PLH}	*IN to Y**	0.926	1.76	1.84	2.07
t_{PHL}		1.85	3.49	3.64	4.09

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.621	3.86
t_{PHL}		0.215	1.43
t_{PLH}	X to Y	0.119	2.11
t_{PHL}		0.190	2.32

Delay coefficients

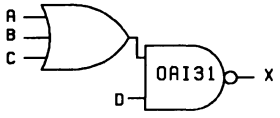
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.09	8.69	0.333	2.66
Y	0.147	4.29	0.306	3.03

Rise/Fall time coefficients for the next cell

3–1 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.090
B, C: 0.095
D: 0.044 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.179 M_{CHL} = 0.106
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 9.4 grids high



$X = \overline{(A+B+C) \cdot D}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.663	1.25	1.30	1.46
t_{PHL}		0.580	1.09	1.14	1.28
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.398	1.90
t_{PHL}		0.374	1.61

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

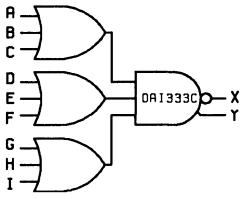
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.649	4.24	0.574	2.76

Rise/Fall time coefficients for the next cell

OAI333C

3–3–3 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: A: 0.066
B, C: 0.065
D, E: 0.067
F: 0.068
G: 0.065
H, I: 0.066 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.158 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 14.0 grids wide, 10.4 grids high



$X = \overline{(A+B+C) * (D+E+F) * (G+H+I)}$

$Y = (A+B+C) * (D+E+F) * (G+H+I)$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X**	2.38	4.45	4.64	5.21
t_{PHL}		1.28	2.40	2.51	2.81
t_{PLH}	*IN to Y	0.975	1.83	1.91	2.14
t_{PHL}		1.92	3.59	3.74	4.20

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	Y to X	0.100	2.06
t_{PHL}		0.106	2.01
t_{PLH}	A,B,C,D,E,F,G,H,I to Y	0.678	2.31
t_{PHL}		1.66	2.60

Delay coefficients

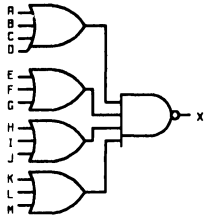
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.186	4.17	0.119	3.21
Y	0.438	4.19	0.732	2.87

Rise/Fall time coefficients for the next cell

4–3–3–3 OR–AND–Invert

Inputs: A, B, C, D, E, F, G, H, I, J, K, L, M
Outputs: X
Input Cap.: A: 0.055
B, C: 0.058
D: 0.057
E, F, G: 0.065
H, I: 0.067
J: 0.068
K: 0.065
L, M: 0.066 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 19.0 grids wide, 10.4 grids high



$X = \overline{(A+B+C+D) \cdot (E+F+G) \cdot (H+I+J) \cdot (K+L+M)}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	2.07	3.86	4.02	4.51
t_{PHL}		1.27	2.37	2.47	2.78
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	1.86	2.06
t_{PHL}		0.976	2.21

Delay coefficients

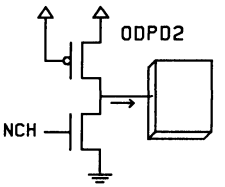
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.215	4.09	0.198	3.19

Rise/Fall time coefficients for the next cell

2mA 5V Open–Drain Output Pad

ODPD2 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.300 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	172	321	334	375
t_{PHL}		9.60	18.0	18.7	21.0

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	9.59	3.24
t_{PHL}		0.585	0.175

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	63.5	22.0	0.635	0.224

Rise/Fall time coefficients for the next cell

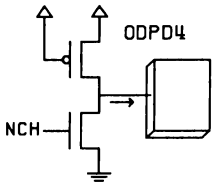
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

4mA 5V Open–Drain Output Pad

ODPD4 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.548 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	173	323	337	378
t_{PHL}		4.98	9.34	9.73	10.9

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	9.81	3.27
t_{PHL}		0.316	0.088

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	63.6	22.0	0.313	0.112

Rise/Fall time coefficients for the next cell

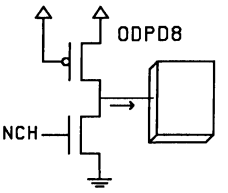
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

8mA 5V Open–Drain Output Pad

ODPD8 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.050 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.519
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	174	325	339	380
t_{PHL}		2.59	4.87	5.08	5.71

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	9.98	3.28
t_{PHL}		0.173	0.044

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	63.6	22.0	0.148	0.056

Rise/Fall time coefficients for the next cell

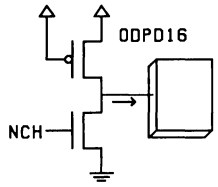
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

16mA 5V Open–Drain Output Pad

ODPD16 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.090 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.101
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	174	326	339	381
t_{PHL}		1.25	2.34	2.44	2.74

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	9.87	3.29
t_{PHL}		0.108	0.022

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	63.6	22.0	0.070	0.028

Rise/Fall time coefficients for the next cell

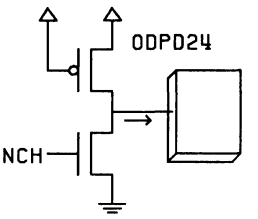
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

24mA 5V Open–Drain Output Pad

ODPD24 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.780 pF
Output Cap.: PAD: 3.540 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.026
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	177	330	344	386
t_{PHL}		0.916	1.71	1.78	2.00

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	11.9	3.29
t_{PHL}		0.105	0.016

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	77.2	22.0	0.071	0.020

Rise/Fall time coefficients for the next cell

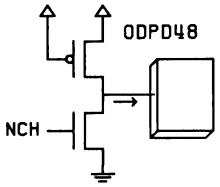
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

48mA 5V Open–Drain Output Pad

ODPD48 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 5.270 pF
Output Cap.: PAD: 4.760 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.125
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 41.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	182	339	354	397
t_{PHL}		0.559	1.05	1.10	1.23

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	17.1	3.29
t_{PHL}		0.057	0.009

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	101	22.0	0.048	0.011

Rise/Fall time coefficients for the next cell

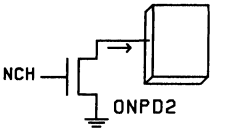
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

2mA 7V Open–Drain Output Pad

ONPD2 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.301 pF
Output Cap.: PAD: 1.830 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.650
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	169	315	329	369
t_{PHL}		9.41	17.6	18.4	20.6

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	6.52	3.24
t_{PHL}		0.383	0.175

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	38.5	22.0	0.399	0.224

Rise/Fall time coefficients for the next cell

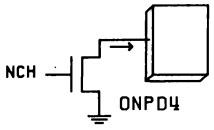
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

4mA 7V Open–Drain Output Pad

ONPD4 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.551 pF
Output Cap.: PAD: 1.830 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	170	318	331	371
t_{PHL}		4.88	9.15	9.54	10.7

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	6.71	3.27
t_{PHL}		0.217	0.088

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	38.5	22.0	0.197	0.112

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

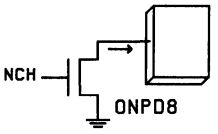
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

ONPD8

8mA 7V Open–Drain Output Pad

ONPD8 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.060 pF
Output Cap.: PAD: 1.830 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.550 M_{CHL} = 0.376
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	171	320	333	374
t_{PHL}		2.49	4.67	4.87	5.46

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	6.88	3.28
t_{PHL}		0.128	0.044

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	38.5	22.0	0.098	0.056

Rise/Fall time coefficients for the next cell

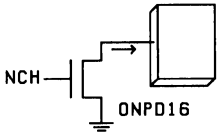
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

16mA 7V Open–Drain Output Pad

ONPD16 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.070 pF
Output Cap.: PAD: 1.830 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.531 M_{CHL} = 0.051
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	172	320	334	375
t_{PHL}		1.20	2.24	2.34	2.63

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	6.75	3.29
t_{PHL}		0.079	0.022

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	38.5	22.0	0.039	0.028

Rise/Fall time coefficients for the next cell

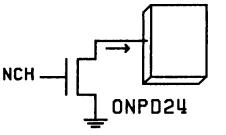
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

24mA 7V Open–Drain Output Pad

ONPD24 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.750 pF
Output Cap.: PAD: 2.170 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.058
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	173	323	336	377
t_{PHL}		0.889	1.66	1.73	1.95

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	8.13	3.29
t_{PHL}		0.065	0.016

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	45.5	22.0	0.034	0.021

Rise/Fall time coefficients for the next cell

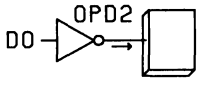
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

2mA Output Pad

OPD2 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 0.527 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	8.73	16.3	17.0	19.1
t_{PHL}		9.82	18.4	19.2	21.5

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.515	0.159
t_{PHL}		0.557	0.180

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.76	0.602	0.635	0.224

Rise/Fall time coefficients for the next cell

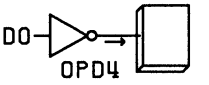
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Output Pad

OPD4 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 1.000 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.631 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	4.54	8.52	8.89	9.98
t_{PHL}		5.06	9.50	9.90	11.1

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.277	0.080
t_{PHL}		0.302	0.090

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.890	0.301	0.317	0.112

Rise/Fall time coefficients for the next cell

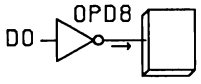
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

8mA Output Pad

OPD8 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 1.950 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.481
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	2.42	4.56	4.76	5.35
t_{PHL}		2.63	4.94	5.15	5.78

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.159	0.040
t_{PHL}		0.175	0.045

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.457	0.150	0.158	0.056

Rise/Fall time coefficients for the next cell

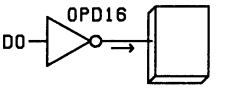
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Output Pad

OPD16 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 3.840 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.500 M_{CHL} = 0.113
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	1.31	2.48	2.59	2.91
t_{PHL}		1.30	2.43	2.53	2.84

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.100	0.020
t_{PHL}		0.098	0.023

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.240	0.075	0.068	0.028

Rise/Fall time coefficients for the next cell

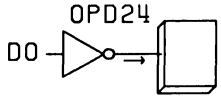
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Output Pad

OPD24 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 5.160 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.375 M_{CHL} = 0.095
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	1.01	1.91	1.99	2.24
t_{PHL}		0.939	1.76	1.83	2.06

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.101	0.015
t_{PHL}		0.099	0.016

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.222	0.055	0.069	0.021

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

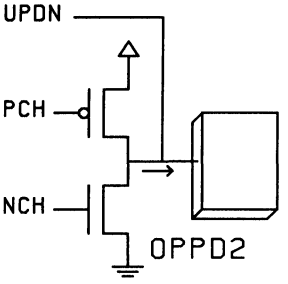
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}-0.5V	-12.00	mA

DC specifications

OPPD2

2mA Tristate Output Pad with Pullup/Pulldown Port

OPPD2 is similar to OTPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 0.276
PCH: 0.213
UPDN: 53.464 pF
Output Cap.: PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	8.09	15.1	15.8	17.7
t_{PHL}		9.22	17.3	18.0	20.2
t_{PLH}	UPDN to PAD	14.3	26.7	27.9	31.3
t_{PHL}		14.3	26.7	27.9	31.3

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.474	0.147
t_{PHL}		0.561	0.168
t_{PLH}	UPDN to PAD	2.04	0.240
t_{PHL}		2.04	0.240

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.42	0.619	0.655	0.216

Rise/Fall time coefficients for the next cell

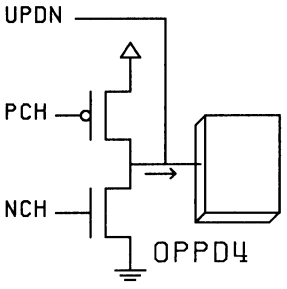
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad with Pullup/Pulldown Port

OPPD4 is similar to OTPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 0.507
PCH: 0.445
UPDN: 53.464 pF
Output Cap.: PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	4.18	7.85	8.18	9.19
t_{PHL}		4.76	8.93	9.31	10.5
t_{PLH}	UPDN to PAD	14.3	26.7	27.9	31.3
t_{PHL}		14.3	26.7	27.9	31.3

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.268	0.073
t_{PHL}		0.300	0.084
t_{PLH}	UPDN to PAD	2.04	0.240
t_{PHL}		2.04	0.240

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.912	0.301	0.332	0.108

Rise/Fall time coefficients for the next cell

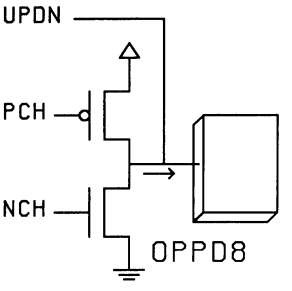
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad with Pullup/Pulldown Port

OPPD8 is similar to OTPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 0.937
PCH: 0.872
UPDN: 53.464 pF
Output Cap.: PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.320
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	2.28	4.29	4.48	5.03
t_{PHL}		2.40	4.51	4.70	5.28
t_{PLH}	UPDN to PAD	14.3	26.7	27.9	31.3
t_{PHL}		14.2	26.5	27.6	31.0

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.163	0.037
t_{PHL}		0.169	0.042
t_{PLH}	UPDN to PAD	2.04	0.240
t_{PHL}		2.04	0.240

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.483	0.150	0.159	0.054

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

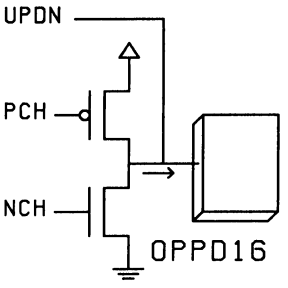
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

OPPD16

16mA Tristate Output Pad with Pullup/Pulldown Port

OPPD16 is similar to OTPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 1.840
PCH: 1.780
UPDN: 53.464 pF
Output Cap.: PAD: 2.970 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.464 M_{CHL} = 0.107
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.20	2.27	2.36	2.66
t_{PHL}		1.20	2.25	2.35	2.64
t_{PLH}	UPDN to PAD	14.2	26.6	27.7	31.1
t_{PHL}		14.1	26.3	27.4	30.8

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.102	0.018
t_{PHL}		0.108	0.021
t_{PLH}	UPDN to PAD	2.04	0.240
t_{PHL}		2.04	0.240

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.265	0.075	0.077	0.027

Rise/Fall time coefficients for the next cell

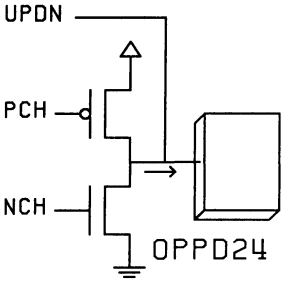
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Tristate Output Pad with Pullup/Pulldown Port

OPPD24 is similar to OTPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 2.470
PCH: 2.400
UPDN: 54.094 pF
Output Cap.: PAD: 3.590 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.369 M_{CHL} = 0.106
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.949	1.80	1.87	2.11
t_{PHL}		0.936	1.75	1.83	2.05
t_{PLH}	UPDN to PAD	14.2	26.6	27.7	31.1
t_{PHL}		14.1	26.4	27.5	30.8

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.094	0.014
t_{PHL}		0.091	0.016
t_{PLH}	UPDN to PAD	2.08	0.240
t_{PHL}		2.08	0.240

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.237	0.055	0.065	0.020

Rise/Fall time coefficients for the next cell

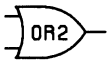
(Worst Case Process, V_{DD} =4.5V, T_A =70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

2–Input OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.037
B: 0.036 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.194 M_{CHL} = 0.217
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.0 grids wide, 8.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.575	1.09	1.13	1.27
t_{PHL}		0.775	1.46	1.53	1.71
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.286	2.07
t_{PHL}		0.467	2.17

Delay coefficients

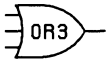
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.127	4.33	0.180	3.19

Rise/Fall time coefficients for the next cell

3–Input OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A, B: 0.047
C: 0.046 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.179 M_{CHL} = 0.175
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.0 grids wide, 9.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.701	1.32	1.38	1.55
t_{PHL}		0.959	1.80	1.88	2.11
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.411	2.15
t_{PHL}		0.649	2.37

Delay coefficients

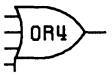
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.185	4.20	0.242	3.25

Rise/Fall time coefficients for the next cell

4–Input OR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.048
B, C: 0.047
D: 0.046 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.209 M_{CHL} = 0.150
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 9.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.754	1.42	1.48	1.67
t_{PHL}		1.27	2.38	2.48	2.78
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.447	2.19
t_{PHL}		0.948	2.57

Delay coefficients

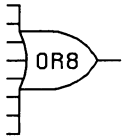
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.218	4.24	0.349	3.34

Rise/Fall time coefficients for the next cell

8–Input OR Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: A: 0.036
B, C, D: 0.037
E: 0.038
F, G: 0.037
H: 0.036 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.206 M_{CHL} = 0.225
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.0 grids wide, 8.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.665	1.26	1.31	1.47
t_{PHL}		0.996	1.88	1.96	2.20
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.371	2.07
t_{PHL}		0.707	1.95

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

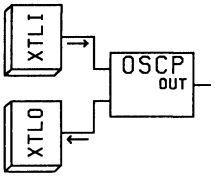
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.273	4.35	0.405	2.55

Rise/Fall time coefficients for the next cell

General Purpose Oscillator

OSCP is a general purpose crystal oscillator cell designed for use with 3 MHz to 20 MHz parallel resonant crystals. Operation above 20 MHz or below 3 MHz is often possible by adding external components. For more details, contact an NCR applications engineer. Tuning capacitors and a startup resistor are supplied internally to the cell so that a parallel resonant crystal is the only external component required. The buffered on-chip output is suitable for driving 5pF loads at 20 MHz.

Inputs: XTLI
Outputs: OUT, XTLO
Input Cap.: XTLI: 34.400 pF
Output Cap.: XTLO: 43.200 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 114.0 grids wide, 80.0 grids high



FEATURES:

- 3 to 20 MHz operation
- On chip tuning capacitor
- On chip startup resistor
- 35% to 65% output duty cycle
- Buffered on-chip output

(Input t_r,t_f= 0.0ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	XTLI to OUT	0.162	0.302	0.315	0.353
t_{PHL}		0.310	0.578	0.603	0.676
For simulation purposes, the XTLI to XTLO propagation delay is zero. The XTLO pin is used for an external crystal connection only. XTLO cannot be connected to any other pad or signal. Input tr,tf are zero since a rise/fall time of 4 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	XTLI to OUT	0.121	0.407
t_{PHL}		0.265	0.447

Delay coefficients

SYMBOL	PARAMETER	NOMINAL PROCESS, V_{DD}=5V, T_A=25C		
		3MHz	10MHz	20MHz
I_{DD}	Typical supply current (mA)	2.00	3.50	5.50
t_0	Typical start-up time (ms)	1.45	1.40	1.40

VS700 OSCP characteristcs

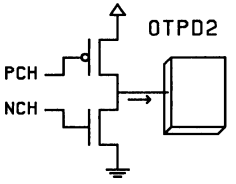
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
OUT	0.533	0.400	0.500	0.453
XTLO	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

2mA Tristate Output Pad

OTPD2 is an output pad capable of output currents up to 2mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 0.295
PCH: 0.231 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	8.73	16.3	17.0	19.1
t_{PHL}		9.82	18.4	19.2	21.5

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.515	0.159
t_{PHL}		0.557	0.180

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.76	0.602	0.634	0.224

Rise/Fall time coefficients for the next cell

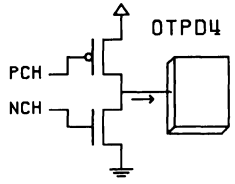
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad

OTPD4 is an output pad capable of output currents up to 4mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 0.535
PCH: 0.467 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.631 M_{CHL} = 0.625
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	4.54	8.52	8.89	9.98
t_{PHL}		5.06	9.50	9.90	11.1

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.277	0.080
t_{PHL}		0.302	0.090

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.890	0.301	0.317	0.112

Rise/Fall time coefficients for the next cell

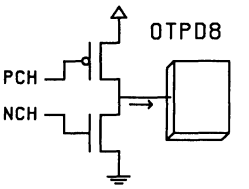
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad

OTPD8 is an output pad capable of output currents up to 8mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 1.020
PCH: 0.935 pF
Output Cap.: PAD: 2.910 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.481
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	2.42	4.56	4.76	5.35
t_{PHL}		2.63	4.94	5.15	5.78

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.159	0.040
t_{PHL}		0.175	0.045

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.457	0.150	0.158	0.056

Rise/Fall time coefficients for the next cell

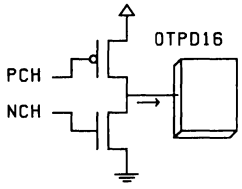
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Tristate Output Pad

OTPD16 is an output pad capable of output currents up to 16mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 1.980
PCH: 1.870 pF
Output Cap.: PAD: 2.910 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.500 M_{CHL} = 0.113
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.31	2.48	2.59	2.91
t_{PHL}		1.30	2.43	2.53	2.84

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.100	0.020
t_{PHL}		0.098	0.023

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.240	0.075	0.068	0.028

Rise/Fall time coefficients for the next cell

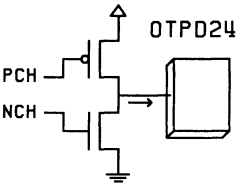
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Tristate Output Pad

OTPD24 is an output pad capable of output currents up to 24mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 2.660
PCH: 2.500 pF
Output Cap.: PAD: 3.540 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.375 M_{CHL} = 0.095
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 31.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.01	1.91	1.99	2.24
t_{PHL}		0.939	1.76	1.83	2.06

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.101	0.015
t_{PHL}		0.099	0.016

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.222	0.055	0.069	0.021

Rise/Fall time coefficients for the next cell

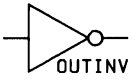
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

Output Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.119 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.212 M_{CHL} = 0.184
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 9.9 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.197	0.383	0.399	0.450
t_{PHL}		0.195	0.376	0.393	0.442

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.054	0.540
t_{PHL}		0.080	0.373

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

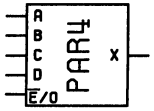
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.068	1.14	0.047	0.720

Rise/Fall time coefficients for the next cell

PAR4

4–Bit Parity Checker

Inputs: A, B, C, D, EBO
Outputs: X
Input Cap.: A, B: 0.034
C: 0.035
D: 0.034
EBO: 0.036 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.250 M_{CHL} = 0.348
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 21.0 grids wide, 12.4 grids high



FUNCTION TABLE

EBO	Number of Inputs Which Are High	X
L	0, 2, 4	H
L	1, 3	L
H	0, 2, 4	L
H	1, 3	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	2.01	3.78	3.94	4.42
t_{PHL}		1.54	2.90	3.03	3.40
t_{PLH}	EBO to X	0.860	1.62	1.69	1.90
t_{PHL}		1.01	1.91	2.00	2.24
* Slowest of A, B, C, or D inputs					

Timing characteristics

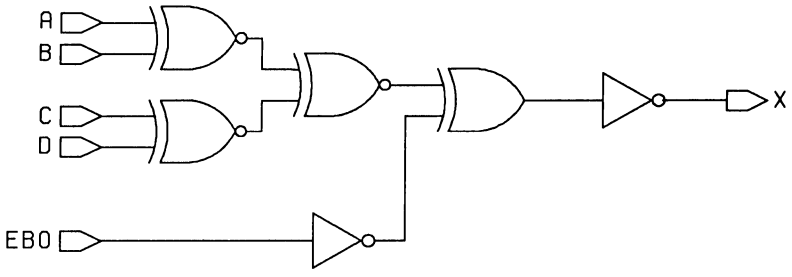
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	1.69	2.22
t_{PHL}		1.15	2.43
t_{PLH}	EBO to X	0.540	2.15
t_{PHL}		0.563	3.03

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.198	4.25	0.221	3.77

Rise/Fall time coefficients for the next cell

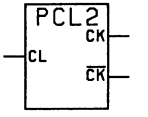


Functional diagram: PAR4

PCL2

Two–Phase Clock

PCL2 is for use with clocked cells and to produce high drive signals of true and complement value. CK is the noninverted or true output and CKB is the inverted or complement output.



Inputs: CL
Outputs: CK, CKB
Input Cap.: CL: 0.070 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.200 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CL to CK	0.561	1.06	1.11	1.24
t_{PHL}		0.608	1.15	1.19	1.34
t_{PLH}	CL to CKB	0.687	1.30	1.35	1.52
t_{PHL}		0.661	1.25	1.30	1.46

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CL to CK	0.414	0.633
t_{PHL}		0.470	0.693
t_{PLH}	CL to CKB	0.543	0.600
t_{PHL}		0.531	0.620

Delay coefficients

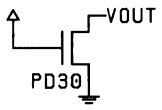
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
CK	0.190	0.987	0.199	0.793
CKB	0.140	1.03	0.116	0.833

Rise/Fall time coefficients for the next cell

30μA N–Channel Pulldown Device

PD30 is a weak n–channel pulldown that sinks 30mA when VOUT equals five volts and can be used as a pulldown on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See the PPD200, PPD400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.



*NOTE: The gate input on the PD30 cannot be used to turn the transistor on or off.

Inputs: VDDIN
Outputs: VOUT
Input Cap.: VDDIN: 0.000 pF
Output Cap.: VOUT: 0.015 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 1.00 N = 1.00 W = 1.00
Cell Size: 10.0 grids wide, 9.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	*VOUT	1525	2034	2120	2378
* Timing is from VOUT = 5V to VOUT = 2.5V					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	*VOUT	1500	254

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

(V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	30μA typical

DC specifications

Power on Reset

Features

- No external components required
- Retriggerable reset under digital control
- Supply glitch immunity

POR is a digital cell that guarantees a logic low level during power up for the purpose of resetting logic elements to known states. Upon application of the positive supply voltage to the device, POR causes SYS to remain low for approximately 6 µs after the positive supply has exceeded 2.9V. This insures that all digital circuits are operational before the SYS output goes high. An additional input is supplied to the cell which allows the output to be retriggered under external control.

FUNCTION TABLE

V_{DD}	RES	SYS
↑	L	⌐
X	H	L
H	↓	⌐

Inputs: RES
Outputs: SYS
Input Cap.: RES: 0.063 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.83 N = 1.00 W = 1.17
Cell Size: 72.0 grids wide, 80.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	RES to SYS	6560	10234	10668	11969
t_{PHL}	RES to SYS	5.97	9.32	9.71	10.9

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	RES to SYS	6560	0.0
t_{PHL}	RES to SYS	5.65	3.25

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
SYS	344	0.000	1.12	4.39

Rise/Fall time coefficients for the next cell

PARAMETER	CONDITIONS	RATING
Supply Current	Nominal Process, V_{DD} = 5V, V_{RES} = 0V, T_A = 25° C	180µA typical
V_{DD} trigger voltage	Nominal Process, T_A = 25° C	2.9V nominal

DC specifications

Application Notes

Reset Timing

The POR cell is not designed for applications requiring precise reset intervals. The duration of the SYS output pulse in a power up condition, or after an external reset input, may vary from the nominal specified timing by 30% or more. Further variations in pulse duration will be observed over varying conditions of supply voltage and temperature. For applications requiring precise timing of a reset signal, an approach utilizing a clocked counter chain is recommended.

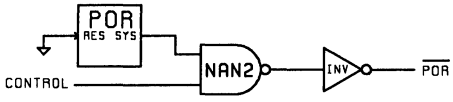
No Relationship exists between the POR SYS output pulse and the start up time of any crystal oscillator in the NCR standard cell library. In general, oscillator cells in the VS700 library require more time to reach stable operation after power is applied than the POR SYS output takes to go high.

POR provides a certain degree of input glitch immunity. The table given below describes the various situations and responses under typical conditions.

CONDITIONS	RESPONSE
* Glitch-free supply RAMP * Supply glitch settles to 2.8V ≥ V_{DD} ≥ 2.7V for at least 35 ns * Supply glitch settles to 2.4V > V_{DD} ≥ 2.0V for at least 20 ns	SYS output high occurs 5.0µs after V_{DD} reaches 2.9V.
*Supply glitch settles to V_{DD} ≥ 2.9V *Supply glitch settles to V_{DD} = 2.0V for less than 10 ns	Will not effect SYS output of POR

Testability

NCR requires the chip be simulated and tested with the reset time out feature of the POR disabled. To achieve this, the RESET input on the POR should be grounded, and the POR output should be ANDed with a control signal (NAN2 and INV – see figure below). The control signal should be accessible by the tester during test time at probe and after the chip is packaged. A static pullup may be connected to the control signal path to enable the reset circuit under normal operation. NCR will review the specific implementation of any circuit using the POR at the time of the design review.



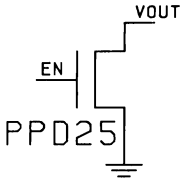
Reset circuit

System Considerations

The NCR POR cell is designed to provide a reset pulse that can be used throughout the chip. If this signal is brought off chip for a system reset, precautions should be taken to insure that all other chips are powered up and functional while the reset pulse is valid.

25μA N–Channel Pulldown Device

PPD25 is a weak n–channel pulldown that sinks 25μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.658 pF
Output Cap.: VOUT: 0.015 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 10.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	11101	19243	20058	22504

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	38.9	221

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

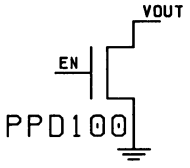
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	25μA typical

DC specifications

100μA N–Channel Pulldown Device

PPD100 is a weak n-channel pulldown that sinks 100μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.198 pF
Output Cap.: VOUT: 0.018 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 7.0 grids wide, 9.6 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	2336	4049	4221	4736

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	2.98	46.7

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

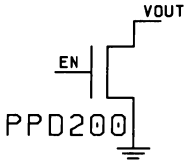
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	100μA typical

DC specifications

200μA N–Channel Pulldown Device

PPD200 is a weak n–channel pulldown that sinks 200μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.107 pF
Output Cap.: VOUT: 0.013 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.631
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 7.0 grids wide, 9.6 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	1165	2020	2105	2362

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.833	23.3

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

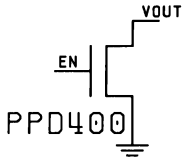
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	200μA typical

DC specifications

400μA N–Channel Pulldown Device

PPD400 is a weak n–channel pulldown that sinks 400μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.097 pF
Output Cap.: VOUT: 0.026 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.625
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 8.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	873	1513	1577	1770

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.705	17.4

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

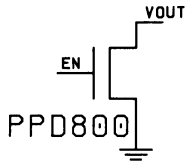
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	400μA typical

DC specifications

800μA N–Channel Pulldown Device

PPD800 is a weak n–channel pulldown that sinks 800μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.172 pF
Output Cap.: VOUT: 0.038 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.625
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 8.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	409	710	740	830

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.562	8.17

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

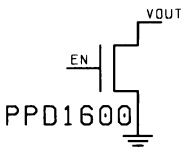
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	800µA typical

DC specifications

1600μA N–Channel Pulldown Device

PPD1600 is a weak n–channel pulldown that sinks 1600μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.096 pF
Output Cap.: VOUT: 0.038 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.625
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 8.0 grids wide, 9.8 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	142	247	257	289

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.184	2.84

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

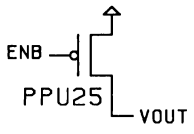
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	1600µA typical

DC specifications

25μA P–Channel Pullup Device

PPU25 is a weak p–channel pullup that sources 25μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.278 pF
Output Cap.: VOUT: 0.025 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 8.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	5332	9242	9634	10809

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	6.17	107

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

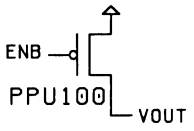
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	25μA typical

DC specifications

100μA P–Channel Pullup Device

PPU100 is a weak p–channel pullup that sources 100μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.109 pF
Output Cap.: VOUT: 0.030 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.631 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 8.0 grids wide, 9.0 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	1473	2554	2663	2987

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	1.16	29.4

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

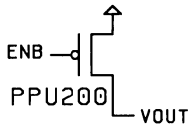
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	100μA typical

DC specifications

200μA P–Channel Pullup Device

PPU200 is a weak p–channel pullup that sources 200μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.184 pF
Output Cap.: VOUT: 0.033 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 9.0 grids wide, 8.8 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	766	1328	1384	1553

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.856	15.3

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

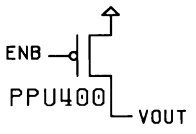
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	200µA typical

DC specifications

400μA P–Channel Pullup Device

PPU400 is a weak p–channel pullup that sources 400μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.190 pF
Output Cap.: VOUT: 0.038 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 9.0 grids wide, 8.8 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	400	693	722	810

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.512	7.97

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

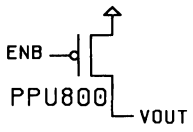
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	400μA typical

DC specifications

800μA P–Channel Pullup Device

PPU800 is a weak p–channel pullup that sources 800μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.146 pF
Output Cap.: VOUT: 0.041 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 8.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	231	400	417	468

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.288	4.60

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

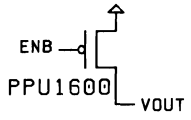
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	800µA typical

DC specifications

1600μA P–Channel Pullup Device

PPU1600 is a weak p-channel pullup that sources 1600μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the application notes.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.215 pF
Output Cap.: VOUT: 0.036 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.625 M_{CHL} = 0.000
Process Derating: B = 0.70 N = 1.00 W = 1.30
Cell Size: 9.0 grids wide, 9.1 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	163	282	294	330

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	39.9	2.45

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

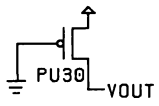
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	1600μA typical

DC specifications

30μA P–Channel Pullup Device

PU30 is a weak p–channel pullup that sources 30μA when VOUT equals zero volts and can be used as a pullup on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See PPU200, PPU400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.



*NOTE: The gate input on the PU30 cannot be used to turn the transistor on or off.

Inputs: GNDIN
Outputs: VOUT
Input Cap.: GNDIN: 0.000 pF
Output Cap.: VOUT: 0.020 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 1.00 N = 1.00 W = 1.00
Cell Size: 8.0 grids wide, 8.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*VOUT	1509	2012	2097	2353
* Timing is from VOUT = 0V to VOUT = 2.5V					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*VOUT	1500	90.5

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

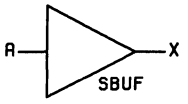
(V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	30μA typical

DC specifications

Small Drive Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.194 M_{CHL} = 0.219
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.0 grids wide, 9.4 grids high



(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.512	0.969	1.01	1.14
t_{PHL}		0.548	1.04	1.08	1.22

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.229	2.01
t_{PHL}		0.257	1.99

Delay coefficients

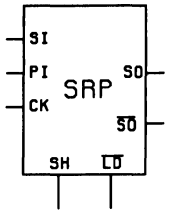
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.122	4.33	0.101	3.25

Rise/Fall time coefficients for the next cell

Shift Register, Positive Edge Triggered

SRP is a 1-bit shift register. It is positive edge triggered with respect to CK. Serial input is clocked in when SH is high. Parallel input is clocked in when LDB is low. SH and LDB should be tied together for normal operation.



Inputs: SI, SH, PI, LDB, CK
Outputs: SO, SOB
Input Cap.: SI, SH: 0.056
PI: 0.052
LDB: 0.070
CK: 0.043 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.196
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 20.0 grids wide, 11.4 grids high

FUNCTION TABLE

SH	SI	LDB	PI	CK	SO	SOB
H	L	H	X	↑	L	H
H	H	H	X	↑	H	L
L	X	L	L	↑	L	H
L	X	L	H	↑	H	L
H	X	L	X	X	*	*
L	X	H	X	X	*	*

* ILLEGAL INPUT COMBINATION

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to SO	1.31	2.44	2.54	2.85
t_{PHL}		1.26	2.37	2.47	2.77
t_{PLH}	*CK to SOB	1.49	2.80	2.92	3.28
t_{PHL}		1.65	3.09	3.22	3.61
* The propagation delay from CK to SOB depends on the CK to SO delay and rise/fall time. See the Timing Equation application note for more information.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to SO	1.16	1.47
t_{PHL}		1.06	1.17
t_{PLH}	SO to SOB	0.121	1.12
t_{PHL}		0.102	1.21

Delay coefficients

SRP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

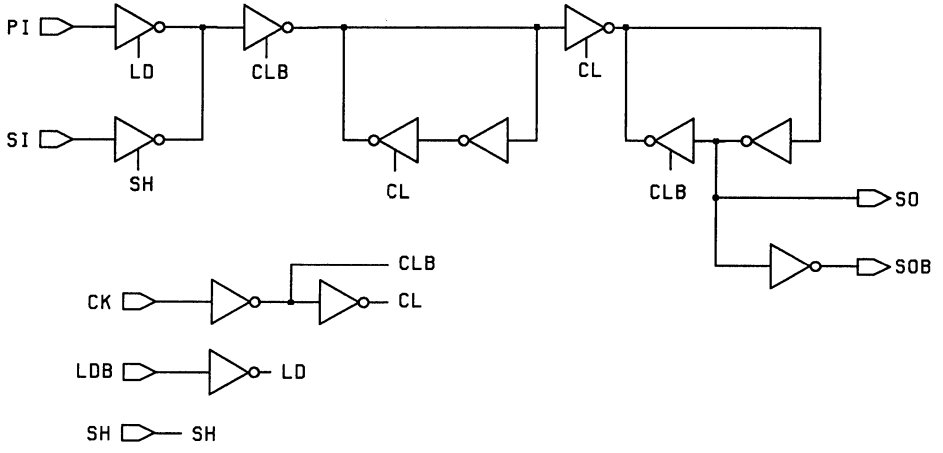
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
SO	0.450	2.27	0.460	1.65
SOB	0.172	2.06	0.121	1.63

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time SI to CK	1.57	0.920	0.563
t_{su}	Setup Time SH to CK	1.57	0.920	0.563
t_{su}	Setup Time PI to CK	1.38	0.810	0.495
t_{su}	Setup Time LDB to CK	1.57	0.920	0.563
t_h	Hold Time CK to SI	−0.444	−0.260	−0.159
t_h	Hold Time CK to SH	−0.291	−0.170	−0.104
t_h	Hold Time CK to PI	−0.444	−0.260	−0.159
t_h	Hold Time CK to LDB	−0.291	−0.170	−0.104
t_{pwh}	Pulse Width (high) CK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) CK	3.74	2.19	1.34

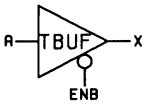
Timing requirements



Functional diagram: SRP

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.035
ENB: 0.078 pF
Output Cap.: X: 0.035 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.263 M_{CHL} = 0.292
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.740	1.40	1.46	1.64
t_{PHL}		0.700	1.33	1.38	1.56
t_{PLH}	ENB to X	0.424	0.811	0.846	0.952
t_{PHL}		0.477	0.911	0.950	1.07

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.433	1.97
t_{PHL}		0.425	1.52
t_{PLH}	ENB to X	0.118	1.96
t_{PHL}		0.197	1.57

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

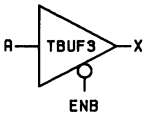
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.289	4.46	0.357	2.18

Rise/Fall time coefficients for the next cell

TBUF3

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.043
ENB: 0.070 pF
Output Cap.: X: 0.052 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.169 M_{CHL} = 0.319
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.0 grids wide, 10.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.550	1.04	1.08	1.22
t_{PHL}		0.861	1.63	1.70	1.91
t_{PLH}	ENB to X	0.611	1.15	1.20	1.35
t_{PHL}		0.589	1.12	1.17	1.32

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.394	0.847
t_{PHL}		0.634	0.933
t_{PLH}	ENB to X	0.452	0.880
t_{PHL}		0.360	0.953

Delay coefficients

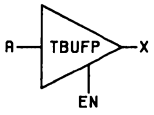
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.180	1.19	0.144	1.19

Rise/Fall time coefficients for the next cell

Noninverting Tristate Buffer

EN is active high. When EN is low, the output is in a Hi–Z state.



Inputs: A, EN
Outputs: X
Input Cap.: A: 0.035
EN: 0.057 pF
Output Cap.: X: 0.035 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.240 M_{CHL} = 0.037
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.0 grids wide, 9.9 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.746	1.41	1.47	1.65
t_{PHL}		0.578	1.08	1.13	1.26
t_{PLH}	EN to X	0.565	1.07	1.12	1.26
t_{PHL}		0.265	0.497	0.518	0.582

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.446	1.99
t_{PHL}		0.410	1.52
t_{PLH}	EN to X	0.236	2.28
t_{PHL}		0.106	1.43

Delay coefficients

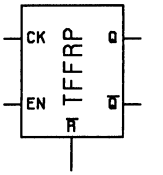
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.518	3.51	0.170	2.80

Rise/Fall time coefficients for the next cell

Toggle Enable Flip–Flop with Reset

TFFRP is a positive edge triggered toggle flip–flop with active high toggle enable and active low reset. For a faster version of this cell, see TFFRPF.



Inputs: RB, EN, CK
Outputs: Q, QB
Input Cap.: RB: 0.118
EN: 0.106
CK: 0.034 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.258 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 21.0 grids wide, 12.4 grids high

FUNCTION TABLE

RB	EN	CK	Q	QB
L	X	X	L	H
H	H	↑	QB_o	Q_o
H	L	↑	Q_o	QB_o

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.02	1.93	2.01	2.26
t_{PHL}		1.18	2.21	2.30	2.58
t_{PLH}	*CK to QB	2.06	3.88	4.04	4.54
t_{PHL}		1.86	3.50	3.65	4.10
t_{PHL}	*RB to Q	1.49	2.81	2.93	3.29
t_{PLH}	RB to QB	0.819	1.55	1.61	1.81

* The propagation delay from CK to QB depends on the CK to Q delay and rise/fall time. Also, the delay from RB to Q depends on the RB to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.653	2.63
t_{PHL}		0.952	1.55
t_{PLH}	Q to QB (CK)	0.513	2.13
t_{PHL}		0.451	1.57
t_{PHL}	QB TO Q (RB)	0.299	1.57
t_{PLH}	RB to QB	0.501	2.10

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

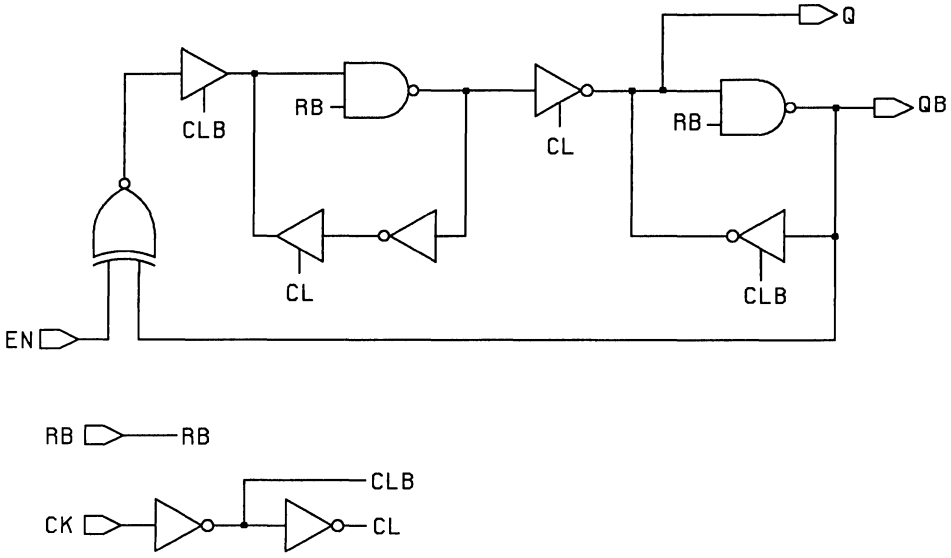
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.806	6.69	0.434	2.66
QB	0.939	4.61	0.674	2.85

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time EN to CK	2.35	1.38	0.843
t_h	Hold Time CK to EN	-0.888	-0.520	-0.318
t_{pwh}	Pulse Width (high) CK	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) RB	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) CK	3.93	2.30	1.41
rt	Recovery Time RB	1.16	0.680	0.415

Timing requirements

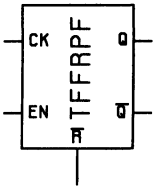


Functional diagram: TFFRP

Fast Toggle Enable Flip–Flop with Reset

TFFRPF is a positive edge triggered toggle flip–flop with active high toggle enable and active low reset.

Inputs: RB, EN, CK
Outputs: Q, QB
Input Cap.: RB: 0.188
EN: 0.118
CK: 0.209 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.177 M_{CHL} = 0.342
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 24.0 grids wide, 14.4 grids high



FUNCTION TABLE

RB	EN	CK	Q	QB
L	X	X	L	H
H	H	↑	QB_o	Q_o
H	L	↑	Q_o	QB_o

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	0.499	0.944	0.984	1.11
t_{PHL}		0.678	1.29	1.35	1.51
t_{PLH}	CK to QB	0.880	1.65	1.73	1.94
t_{PHL}		0.740	1.41	1.47	1.65
t_{PHL}	RB to Q	0.657	1.25	1.30	1.47
t_{PLH}	RB to QB	1.08	2.03	2.11	2.37

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.258	1.67
t_{PHL}		0.397	1.37
t_{PLH}	CK to QB	0.588	2.17
t_{PHL}		0.463	1.33
t_{PHL}	RB to Q	0.403	1.11
t_{PLH}	RB to QB	0.770	2.35

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

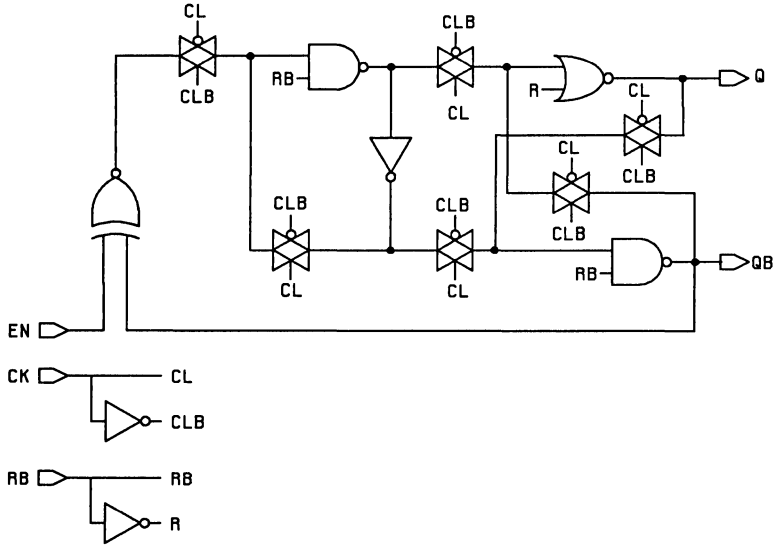
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.282	3.47	0.242	1.85
QB	0.843	4.55	0.438	1.92

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time EN to CK	2.56	1.50	0.917
t_h	Hold Time CK to EN	−0.444	−0.260	−0.159
t_{pwh}	Pulse Width (high) CK	2.95	1.73	1.06
t_{pwl}	Pulse Width (low) RB	4.13	2.42	1.48
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27
rt	Recovery Time RB	0.768	0.450	0.275

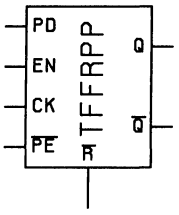
Timing requirements



Functional diagram: TFFRPF

Toggle Enable Flip–Flop with Reset and Synchronous Parallel Load

TFFRPP is a positive edge triggered toggle flip–flop with active low reset and active high toggle enable. Parallel data (PD) is loaded into the flip–flop synchronous to the rising edge of CK when PEB is low.



Inputs: PEB, PD, CK, EN, RB
Outputs: Q, QB
Input Cap.: PEB: 0.057
PD: 0.019
CK: 0.035
EN: 0.105
RB: 0.118 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.196 M_{CHL} = 0.109
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 25.0 grids wide, 12.4 grids high

FUNCTION TABLE

CK	RB	EN	PEB	PD	Q	QB
X	L	X	X	X	L	H
↑	H	X	L	L	L	H
↑	H	X	L	H	H	L
↑	H	H	H	X	QB_o	Q_o
X	H	L	H	X	Q_o	QB_o

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.03	1.94	2.02	2.27
t_{PHL}		1.18	2.20	2.29	2.58
t_{PLH}	*CK to QB	2.04	3.82	3.99	4.48
t_{PHL}		1.76	3.30	3.44	3.86
t_{PHL}	*RB to Q	1.40	2.63	2.74	3.08
t_{PLH}	RB to QB	0.794	1.50	1.56	1.75

* The propagation delay from CK to QB depends on the CK to Q delay and rise/fall time. Also, the delay from RB to Q depends on the RB to QB delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.833	23.3

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

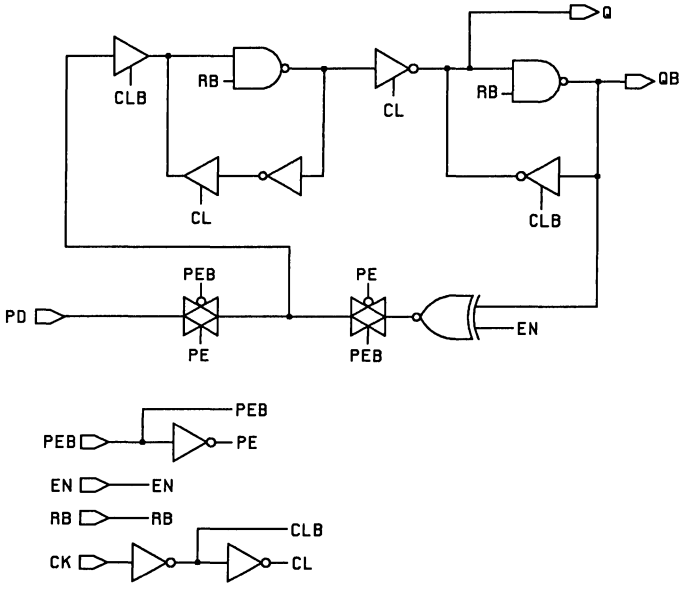
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.813	6.95	0.445	2.59
QB	0.943	4.60	0.680	2.81

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time PEB to CK	1.77	1.04	0.635
t_{su}	Setup Time PD to CK	1.38	0.810	0.495
t_{su}	Setup Time EN to CK	2.95	1.73	1.06
t_h	Hold Time CK to PEB	−0.444	−0.260	−0.159
t_h	Hold Time CK to PD	−0.444	−0.260	−0.159
t_h	Hold Time CK to EN	−1.331	−0.780	−0.476
t_{pwh}	Pulse Width (high) CK	4.91	2.88	1.76
t_{pwl}	Pulse Width (low) CK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) RB	5.10	2.99	1.83
rt	Recovery Time RB	1.16	0.680	0.415

Timing requirements



Functional diagram: TFFRPP

NCR 1.5μ Fast Standard Cell Library Data Sheets
Alphabetical Contents

NCR 1.5μ Fast Standard Cell Library Data Sheets
Functional Contents

Simple Logic Cells

Buffers

Latches

Shift Registers

Decoders and Multiplexers

Flip–flops

Special Function Cells

Tristate Elements

Input/Output Cells

NCR VS1500F Standard Cell Library

Electrical Specifications

DC Characteristics

Sym	Parameter	VDD	Guaranteed Limit			Unit
			0 to 70°C	−40 to 85°C	−55 to 125°C	
V_{IH} (TTL)	Minimum high-level Input voltage	4.5	2.0	2.0	2.0	V
		5.5	2.0	2.0	2.0	
V_{IL} (TTL)	Maximum low-level Input voltage	4.5	0.8	0.8	0.8	V
		5.5	0.8	0.8	0.8	
V_{IH} (CMOS)	Minimum high-level Input voltage	4.5	3.15	3.15	3.15	V
		5.5	3.85	3.85	3.85	
V_{IL} (CMOS)	Maximum low-level Input voltage	4.5	1.35	1.35	1.35	V
		5.5	1.65	1.65	1.65	
V_{OH}	Minimum high-level Output Voltage Any buffer, I_{OH} = −20μa	4.5	4.4	4.4	4.4	V
		5.5	5.4	5.4	5.4	
I_{OH}	Minimum high-level Source Current, V_{OH} = 2.4V	4.5				mA
	2mA buffer		2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	24.0	
	48mA buffer		48.0	48.0	48.0	
V_{OL}	Maximum low-level Output Voltage Any buffer, I_{OL} = 20μa	4.5	0.1	0.1	0.1	V
		5.5	0.1	0.1	0.1	
I_{OL}	Minimum low-level Sink Current, V_{OL} = 0.4V					mA
	2mA buffer		2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	24.0	
	48mA buffer		48.0	48.0	48.0	
I_{IN}	Maximum input leakage current	5.5	±10	±10	±20	μA
I_{OZ}	Maximum output leakage current	5.5	±10	±10	±20	μA

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{DD}	DC power supply voltage	−0.5 to 7.0	V
V_{IN}, V_{OUT}	DC input, output voltage	−0.5 to V_{DD}+0.5	V
I	DC current drain V_{DD} and V_{SS} pins	100	mA
T_{STG}	Storage temperature	−55 to 150	°C
T_L	Lead temperature (less than 10 second soldering)	250	°C
T_{OPER}	Operating temperature Commercial Industrial Military	 0 to 70 −40 to 85 −55 to 125	°C

* Stresses beyond those listed in the "Absolute Maximum Ratings" table may cause physical damage to a device and should be avoided. This table does not imply that operation at conditions above those listed in the "Recommended Operating Conditions" is possible. This is a stress rating and operation of a device at or above this rating for an extended period may cause failure or affect reliability.

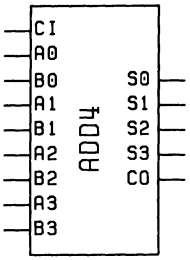
Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	DC power supply voltage	3.0	6.0	V
V_{IN}, V_{OUT}	DC input, output voltage	0	V_{DD}	V

4–Bit Adder

The ADD4 is a four–bit, asynchronous, ripple adder with carry–in/carry–out function. See the ADD4CS data sheet for application notes.

Inputs: CI, A0, B0, A1, B1, A2, B2, A3, B3
Outputs: S0, S1, S2, S3, CO
Input Cap.: CI, A0: 0.406
B0: 0.407
A1: 0.361
B1: 0.360
A2: 0.218
B2: 0.221
A3: 0.218
B3: 0.221 pF
Cell Size: 112 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A0 TO CO	4.60	8.49	8.85	9.93	4.51+0.583*C_L ns
t_{PHL}		4.71	8.70	9.07	10.2	4.57+0.924*C_L ns
t_{PLH}	A1 TO CO	4.04	7.45	7.77	8.72	3.95+0.585*C_L ns
t_{PHL}		4.17	7.69	8.02	9.00	4.02+0.937*C_L ns
t_{PLH}	A2 TO CO	3.23	5.97	6.22	6.98	3.14+0.573*C_L ns
t_{PHL}		3.61	6.66	6.95	7.79	3.47+0.931*C_L ns
t_{PLH}	A3 TO CO	2.10	3.88	4.05	4.54	2.01+0.592*C_L ns
t_{PHL}		2.46	4.54	4.73	5.31	2.32+0.932*C_L ns
t_{PLH}	B0 TO CO	4.63	8.55	8.91	10.0	4.54+0.573*C_L ns
t_{PHL}		4.64	8.56	8.93	10.0	4.49+0.939*C_L ns
t_{PLH}	B1 TO CO	4.15	7.66	7.98	8.96	4.06+0.582*C_L ns
t_{PHL}		4.18	7.72	8.04	9.03	4.04+0.937*C_L ns
t_{PLH}	B2 TO CO	3.34	6.18	6.44	7.22	3.26+0.567*C_L ns
t_{PHL}		3.64	6.73	7.02	7.87	3.50+0.939*C_L ns
t_{PLH}	B3 TO CO	2.20	4.06	4.23	4.75	2.11+0.577*C_L ns
t_{PHL}		2.50	4.62	4.82	5.41	2.36+0.923*C_L ns
t_{PLH}	CI TO CO	4.49	8.30	8.65	9.71	4.41+0.563*C_L ns
t_{PHL}		4.60	8.50	8.86	9.94	4.46+0.929*C_L ns
t_{PLH}	CI TO S0	1.43	2.65	2.76	3.10	1.13+2.05*C_L ns
t_{PHL}		0.939	1.73	1.81	2.03	0.799+0.932*C_L ns
t_{PLH}	CI TO S1	2.27	4.19	4.37	4.90	2.05+1.46*C_L ns
t_{PHL}		1.90	3.51	3.65	4.10	1.75+0.999*C_L ns

Switching characteristics (Sheet 1 of 3)

ADD4

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CI TO S2	3.38	6.24	6.50	7.30	3.16+1.44*C_L ns
t_{PHL}		3.04	5.61	5.85	6.56	2.89+0.995*C_L ns
t_{PLH}	CI TO S3	4.53	8.37	8.73	9.79	4.32+1.42*C_L ns
t_{PHL}		4.19	7.73	8.06	9.04	4.04+0.988*C_L ns
t_{PLH}	A0,B0 TO S0	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_{PLH}	A0,B0 TO S1	2.37	4.38	4.57	5.12	2.15+1.47*C_L ns
t_{PHL}		2.01	3.71	3.86	4.34	1.85+1.01*C_L ns
t_{PLH}	A0,B0 TO S2	3.50	6.46	6.73	7.56	3.28+1.44*C_L ns
t_{PHL}		3.14	5.81	6.05	6.79	2.99+0.999*C_L ns
t_{PLH}	A0,B0 TO S3	4.65	8.59	8.96	10.0	4.43+1.44*C_L ns
t_{PHL}		4.29	7.91	8.25	9.26	4.13+0.998*C_L ns
t_{PLH}	A1,B1 TO S1	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_{PLH}	A1,B1 TO S2	2.56	4.73	4.93	5.53	2.35+1.43*C_L ns
t_{PHL}		1.81	3.34	3.49	3.91	1.66+0.993*C_L ns
t_{PLH}	A1,B1 TO S3	3.27	6.03	6.29	7.05	2.94+2.14*C_L ns
t_{PHL}		3.81	7.04	7.33	8.23	3.60+1.36*C_L ns
t_{PLH}	A2,B2 TO S2	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_{PLH}	A2,B2 TO S3	2.15	3.97	4.14	4.64	1.83+2.14*C_L ns
t_{PHL}		2.66	4.90	5.11	5.74	2.45+1.36*C_L ns
t_{PLH}	A3,B3 TO S3	2.10	3.88	4.05	4.54	1.78+2.14*C_L ns
t_{PHL}		2.01	3.72	3.88	4.35	1.81+1.36*C_L ns
t_r	A0 TO CO	0.735	1.36	1.41	1.59	0.564+1.14*C_L ns
t_f		0.767	1.42	1.48	1.66	0.491+1.84*C_L ns
t_r	A1 TO CO	0.736	1.36	1.42	1.59	0.566+1.14*C_L ns
t_f		0.776	1.43	1.49	1.68	0.498+1.85*C_L ns
t_r	A2 TO CO	0.725	1.34	1.40	1.57	0.554+1.14*C_L ns
t_f		0.780	1.44	1.50	1.68	0.503+1.84*C_L ns
t_r	A3 TO CO	0.739	1.37	1.42	1.60	0.568+1.14*C_L ns
t_f		0.774	1.43	1.49	1.67	0.499+1.83*C_L ns
t_r	B0 TO CO	0.736	1.36	1.42	1.59	0.566+1.13*C_L ns
t_f		0.778	1.44	1.50	1.68	0.501+1.84*C_L ns
t_r	B1 TO CO	0.728	1.34	1.40	1.57	0.556+1.14*C_L ns
t_f		0.778	1.44	1.50	1.68	0.501+1.84*C_L ns
t_r	B2 TO CO	0.735	1.36	1.42	1.59	0.565+1.13*C_L ns
t_f		0.776	1.43	1.49	1.68	0.499+1.85*C_L ns
t_r	B3 TO CO	0.736	1.36	1.42	1.59	0.564+1.14*C_L ns
t_f		0.768	1.42	1.48	1.66	0.493+1.83*C_L ns
t_r	CI TO CO	0.736	1.36	1.42	1.59	0.566+1.13*C_L ns
t_f		0.778	1.44	1.50	1.68	0.500+1.85*C_L ns
t_r	CI TO S0	1.59	2.93	3.06	3.43	0.882+4.70*C_L ns
t_f		1.19	2.20	2.29	2.57	0.835+2.35*C_L ns
t_r	CI TO S1	1.76	3.26	3.40	3.81	1.16+4.06*C_L ns
t_f		1.02	1.89	1.97	2.21	0.659+2.43*C_L ns
t_r	CI TO S2	1.69	3.12	3.26	3.65	1.08+4.09*C_L ns

Switching characteristics (Sheet 2 of 3)

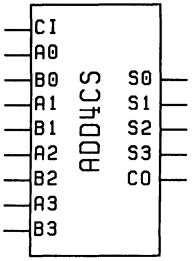
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.02	1.88	1.96	2.20	0.655+2.43*C_L ns
t_r	CI TO S3	1.71	3.16	3.29	3.70	1.10+4.07*C_L ns
t_f		1.02	1.89	1.97	2.21	0.657+2.43*C_L ns
t_r	A0,B0 TO S0	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns
t_r	A0,B0 TO S1	1.73	3.20	3.34	3.75	1.12+4.09*C_L ns
t_f		1.05	1.93	2.01	2.26	0.682+2.42*C_L ns
t_r	A0,B0 TO S2	1.67	3.09	3.22	3.61	1.06+4.10*C_L ns
t_f		1.02	1.89	1.97	2.21	0.660+2.43*C_L ns
t_r	A0,B0 TO S3	1.68	3.11	3.24	3.64	1.07+4.09*C_L ns
t_f		1.03	1.89	1.97	2.22	0.661+2.43*C_L ns
t_r	A1,B1 TO S1	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns
t_r	A1,B1 TO S2	1.71	3.15	3.29	3.69	1.10+4.07*C_L ns
t_f		1.000	1.85	1.93	2.16	0.633+2.45*C_L ns
t_r	A1,B1 TO S3	1.47	2.71	2.82	3.17	0.745+4.80*C_L ns
t_f		0.865	1.60	1.67	1.87	0.445+2.80*C_L ns
t_r	A2,B2 TO S2	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns
t_r	A2,B2 TO S3	1.47	2.72	2.83	3.18	0.751+4.80*C_L ns
t_f		0.879	1.62	1.69	1.90	0.462+2.78*C_L ns
t_r	A3,B3 TO S3	1.46	2.69	2.80	3.15	0.736+4.80*C_L ns
t_f		0.872	1.61	1.68	1.88	0.453+2.79*C_L ns

Switching characteristics (Sheet 3 of 3)

4–Bit Adder with Carry Select

The ADD4CS is a 4–bit adder with carry–in/ carry–out function optimized for fast carry–in to carry–out and sum propagation delay.



Inputs: CI, A0, B0, A1, B1, A2, B2, A3, B3
Outputs: S0, S1, S2, S3, CO
Input Cap.: CI: 0.319
A0: 0.408
B0: 0.405
A1: 0.361
B1: 0.360
A2: 0.218
B2: 0.221
A3: 0.218
B3: 0.221 pF
Cell Size: 186 grids wide, 14 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A0 TO CO	5.05	9.32	9.72	10.9	4.96+0.545*C_L ns
t_{PHL}		4.89	9.04	9.42	10.6	4.75+0.918*C_L ns
t_{PLH}	A1 TO CO	4.69	8.66	9.02	10.1	4.64+0.321*C_L ns
t_{PHL}		5.27	9.74	10.2	11.4	5.13+0.943*C_L ns
t_{PLH}	A2 TO CO	4.18	7.71	8.04	9.02	4.12+0.323*C_L ns
t_{PHL}		4.95	9.15	9.54	10.7	4.81+0.956*C_L ns
t_{PLH}	A3 TO CO	3.11	5.74	5.99	6.72	3.06+0.321*C_L ns
t_{PHL}		3.83	7.08	7.38	8.28	3.69+0.940*C_L ns
t_{PLH}	B0 TO CO	5.05	9.33	9.73	10.9	4.97+0.545*C_L ns
t_{PHL}		4.96	9.16	9.55	10.7	4.82+0.917*C_L ns
t_{PLH}	B1 TO CO	4.84	8.94	9.32	10.5	4.76+0.551*C_L ns
t_{PHL}		5.14	9.49	9.89	11.1	5.00+0.913*C_L ns
t_{PLH}	B2 TO CO	4.33	8.00	8.33	9.35	4.25+0.545*C_L ns
t_{PHL}		4.82	8.90	9.28	10.4	4.68+0.914*C_L ns
t_{PLH}	B3 TO CO	3.24	5.99	6.24	7.00	3.16+0.547*C_L ns
t_{PHL}		3.71	6.85	7.14	8.01	3.57+0.921*C_L ns
t_{PLH}	CI TO CO	0.933	1.72	1.80	2.01	0.844+0.586*C_L ns
t_{PHL}		0.940	1.74	1.81	2.03	0.805+0.901*C_L ns
t_{PLH}	CI TO S0	2.30	4.26	4.44	4.98	2.00+2.05*C_L ns
t_{PHL}		1.84	3.41	3.55	3.98	1.70+0.934*C_L ns
t_{PLH}	CI TO S1	2.07	3.83	3.99	4.47	1.98+0.610*C_L ns

Switching characteristics (Sheet 1 of 3)

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}		2.17	4.01	4.18	4.68	2.07+0.640*C_L ns
t_{PLH}	CI TO S2	2.07	3.83	3.99	4.47	1.98+0.610*C_L ns
t_{PHL}		2.17	4.01	4.18	4.68	2.07+0.640*C_L ns
t_{PLH}	CI TO S3	2.07	3.83	3.99	4.47	1.98+0.610*C_L ns
t_{PHL}		2.17	4.01	4.18	4.68	2.07+0.640*C_L ns
t_{PLH}	A0,B0 TO S0	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_{PLH}	A0,B0 TO S1	4.07	7.53	7.84	8.80	3.98+0.625*C_L ns
t_{PHL}		3.07	5.67	5.91	6.63	2.97+0.648*C_L ns
t_{PLH}	A0,B0 TO S2	5.11	9.44	9.84	11.0	5.02+0.618*C_L ns
t_{PHL}		4.16	7.69	8.02	9.00	4.07+0.643*C_L ns
t_{PLH}	A0,B0 TO S3	6.21	11.5	12.0	13.4	6.11+0.644*C_L ns
t_{PHL}		5.25	9.69	10.1	11.3	5.14+0.661*C_L ns
t_{PLH}	A1,B1 TO S1	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_{PLH}	A1,B1 TO S2	4.70	8.68	9.05	10.2	4.60+0.630*C_L ns
t_{PHL}		3.49	6.45	6.73	7.55	3.39+0.647*C_L ns
t_{PLH}	A1,B1 TO S3	4.67	8.63	9.00	10.1	4.58+0.632*C_L ns
t_{PHL}		5.61	10.4	10.8	12.1	5.51+0.652*C_L ns
t_{PLH}	A2,B2 TO S2	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_{PLH}	A2,B2 TO S3	3.59	6.62	6.90	7.75	3.49+0.631*C_L ns
t_{PHL}		4.47	8.25	8.60	9.65	4.37+0.674*C_L ns
t_{PLH}	A3,B3 TO S3	2.05	3.79	3.95	4.43	1.73+2.13*C_L ns
t_{PHL}		1.94	3.58	3.74	4.19	1.73+1.39*C_L ns
t_r	A0 TO CO	0.618	1.14	1.19	1.33	0.444+1.16*C_L ns
t_f		0.721	1.33	1.39	1.56	0.443+1.85*C_L ns
t_r	A1 TO CO	0.441	0.815	0.850	0.953	0.361+0.534*C_L ns
t_f		0.730	1.35	1.40	1.58	0.452+1.85*C_L ns
t_r	A2 TO CO	0.451	0.832	0.868	0.973	0.371+0.532*C_L ns
t_f		0.725	1.34	1.40	1.57	0.448+1.85*C_L ns
t_r	A3 TO CO	0.446	0.824	0.859	0.964	0.366+0.533*C_L ns
t_f		0.734	1.36	1.41	1.59	0.457+1.84*C_L ns
t_r	B0 TO CO	0.617	1.14	1.19	1.33	0.443+1.16*C_L ns
t_f		0.720	1.33	1.39	1.55	0.442+1.85*C_L ns
t_r	B1 TO CO	0.612	1.13	1.18	1.32	0.437+1.16*C_L ns
t_f		0.719	1.33	1.38	1.55	0.442+1.85*C_L ns
t_r	B2 TO CO	0.619	1.14	1.19	1.34	0.445+1.16*C_L ns
t_f		0.722	1.33	1.39	1.56	0.445+1.84*C_L ns
t_r	B3 TO CO	0.615	1.14	1.18	1.33	0.440+1.16*C_L ns
t_f		0.700	1.29	1.35	1.51	0.420+1.87*C_L ns
t_r	CI TO CO	0.592	1.09	1.14	1.28	0.417+1.16*C_L ns
t_f		0.723	1.34	1.39	1.56	0.446+1.85*C_L ns
t_r	CI TO S0	1.55	2.86	2.99	3.35	0.844+4.71*C_L ns
t_f		1.25	2.31	2.41	2.70	0.904+2.31*C_L ns
t_r	CI TO S1	0.665	1.23	1.28	1.44	0.498+1.11*C_L ns
t_f		0.653	1.21	1.26	1.41	0.506+0.978*C_L ns

Switching characteristics (Sheet 2 of 3)

ADD4CS

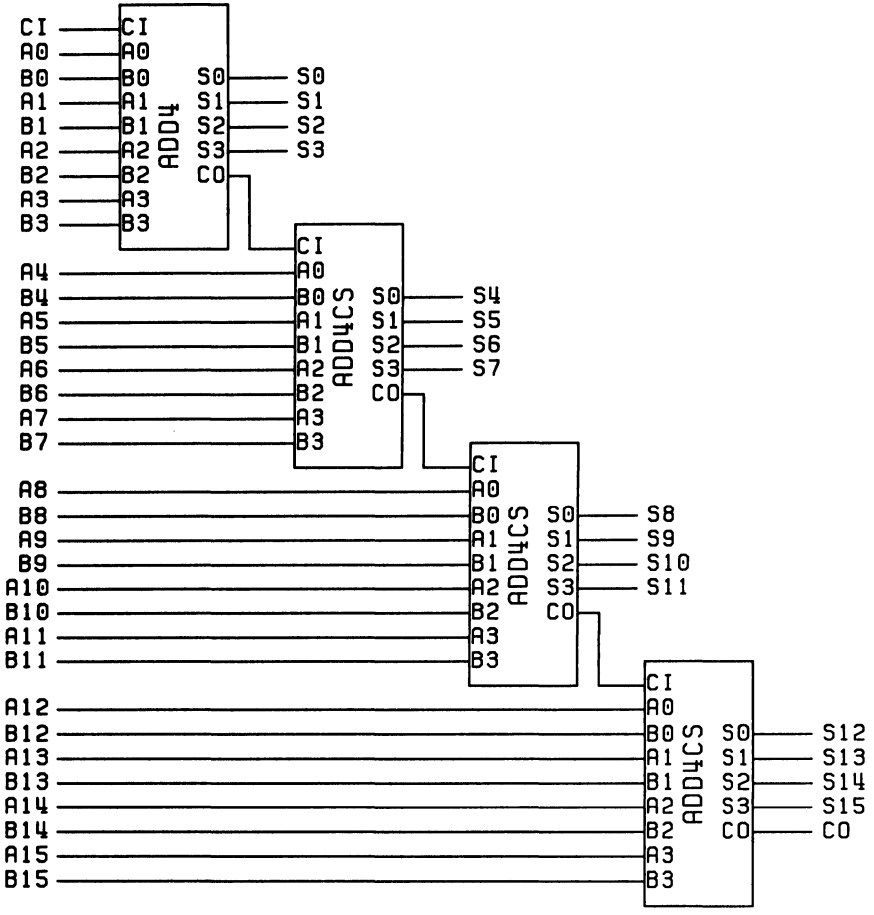
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	CI TO S2	0.665	1.23	1.28	1.44	0.498+1.11*C_L ns
t_f		0.653	1.21	1.26	1.41	0.506+0.978*C_L ns
t_r	CI TO S3	0.665	1.23	1.28	1.44	0.498+1.11*C_L ns
t_f		0.653	1.21	1.26	1.41	0.506+0.978*C_L ns
t_r	A0,B0 TO S0	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns
t_r	A0,B0 TO S1	0.689	1.27	1.33	1.49	0.521+1.12*C_L ns
t_f		0.691	1.28	1.33	1.49	0.547+0.959*C_L ns
t_r	A0,B0 TO S2	0.707	1.31	1.36	1.53	0.543+1.10*C_L ns
t_f		0.690	1.28	1.33	1.49	0.547+0.953*C_L ns
t_r	A0,B0 TO S3	0.666	1.23	1.28	1.44	0.491+1.16*C_L ns
t_f		0.712	1.32	1.37	1.54	0.571+0.938*C_L ns
t_r	A1,B1 TO S1	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns
t_r	A1,B1 TO S2	0.656	1.21	1.26	1.42	0.486+1.13*C_L ns
t_f		0.689	1.27	1.33	1.49	0.545+0.955*C_L ns
t_r	A1,B1 TO S3	0.666	1.23	1.28	1.44	0.494+1.15*C_L ns
t_f		0.656	1.21	1.26	1.42	0.506+1.000*C_L ns
t_r	A2,B2 TO S2	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns
t_r	A2,B2 TO S3	0.702	1.30	1.35	1.52	0.533+1.12*C_L ns
t_f		0.671	1.24	1.29	1.45	0.523+0.986*C_L ns
t_r	A3,B3 TO S3	1.45	2.68	2.80	3.14	0.733+4.79*C_L ns
t_f		0.877	1.62	1.69	1.89	0.459+2.79*C_L ns

Switching characteristics (Sheet 3 of 3)

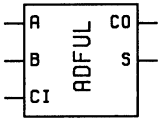
The ADD4 and ADD4CS standard cells offer the designer a performance or cell area choice. The ADD4 is a 4-bit ripple adder with a maximum propagation delay of 6ns under nominal conditions. The ADD4CS cell is optimized to provide carry-in to carry-out and sum times less than 2 and 3ns, respectively, for nominal conditions.

Cascading ADD4CS adders with the ADD4 (as shown in the following figure) allows for 16- and 32-bit nominal add times of less than 13 and 21ns, respectively. Speed may be traded off for cell area by using only ADD4 cells.



Full Adder

The ADFUL is a single-bit asynchronous adder with carry-in/carry-out function.



Inputs: A, B, CI
Outputs: CO, S
Input Cap.: All: 0.210 pF
Cell Size: 22 grids wide, 12 grids high

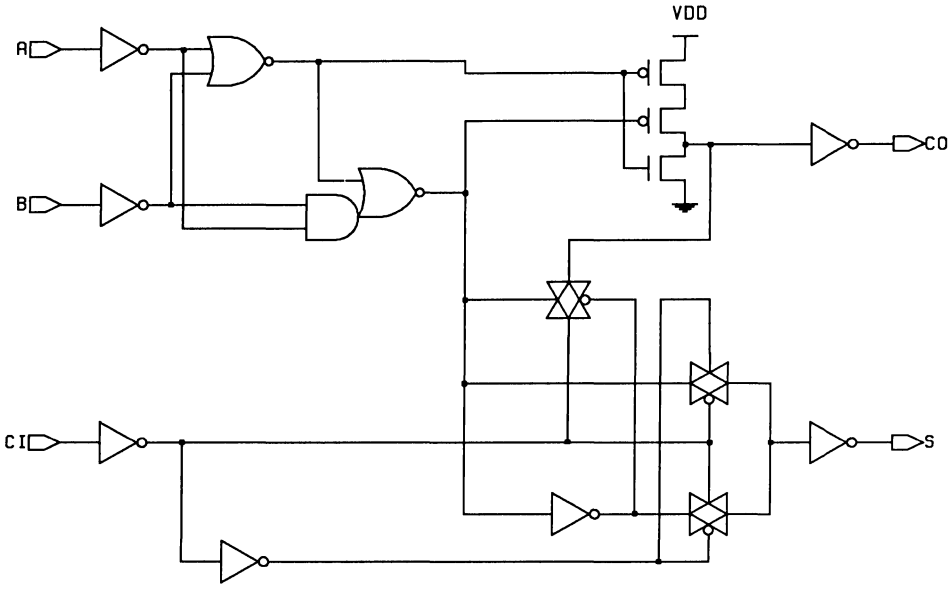
FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO CO	2.72	5.02	5.23	5.87	2.47+1.66*C_L ns
t_{PHL}		2.67	4.93	5.14	5.77	2.43+1.58*C_L ns
t_{PLH}	CI TO CO	2.40	4.43	4.62	5.19	2.15+1.66*C_L ns
t_{PHL}		2.45	4.53	4.72	5.30	2.21+1.59*C_L ns
t_{PLH}	*IN TO S	4.04	7.46	7.77	8.72	3.78+1.70*C_L ns
t_{PHL}		4.03	7.44	7.76	8.70	3.76+1.82*C_L ns
t_{PLH}	CI TO S	3.75	6.93	7.22	8.11	3.49+1.71*C_L ns
t_{PHL}		3.91	7.22	7.52	8.44	3.65+1.68*C_L ns
t_r	*IN TO CO	0.935	1.73	1.80	2.02	0.391+3.62*C_L ns
t_f		0.831	1.54	1.60	1.80	0.375+3.04*C_L ns
t_r	CI TO CO	0.940	1.74	1.81	2.03	0.396+3.62*C_L ns
t_f		0.805	1.49	1.55	1.74	0.345+3.06*C_L ns
t_r	*IN TO S	1.15	2.13	2.22	2.49	0.624+3.52*C_L ns
t_f		1.24	2.30	2.40	2.69	0.798+2.97*C_L ns
t_r	CI TO S	1.25	2.32	2.42	2.71	0.729+3.50*C_L ns
t_f		1.15	2.13	2.22	2.49	0.714+2.93*C_L ns
* Timing applies to either A or B input						

Switching characteristics



Functional diagram: ADFUL

2–Input AND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.071 pF
Cell Size: 4 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.955	1.76	1.84	2.06	0.709+1.64*C_L ns
t_{PHL}		1.21	2.23	2.33	2.61	0.973+1.57*C_L ns
t_r	*IN TO X	0.882	1.63	1.70	1.91	0.336+3.64*C_L ns
t_f		0.790	1.46	1.52	1.71	0.332+3.05*C_L ns
* Slowest input						

Switching characteristics

3–Input AND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.088 pF
Cell Size: 5 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.10	2.04	2.13	2.38	0.855+1.65*C_L ns
t_{PHL}		1.59	2.93	3.05	3.43	1.35+1.60*C_L ns
t_r	*IN TO X	0.919	1.70	1.77	1.98	0.375+3.62*C_L ns
t_f		0.912	1.68	1.76	1.97	0.463+2.99*C_L ns
* Slowest input						

Switching characteristics

AND4

4–Input AND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B, C: 0.088
D: 0.089 pF
Cell Size: 6 grids wide, 10 grids high

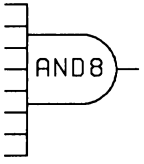
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.37	2.53	2.64	2.96	1.11+1.70*C_L ns
t_{PHL}		1.75	3.23	3.37	3.78	1.51+1.62*C_L ns
t_r	*IN TO X	0.998	1.84	1.92	2.15	0.459+3.59*C_L ns
t_f		0.969	1.79	1.87	2.09	0.521+2.98*C_L ns
* Slowest input						

Switching characteristics

8–Input AND Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: A: 0.072
B, C: 0.071
D, E: 0.072
F, G: 0.071
H: 0.072 pF
Cell Size: 13 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

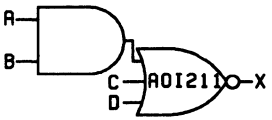
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.74	3.21	3.35	3.75	1.41+2.17*C_L ns
t_{PHL}		1.75	3.23	3.36	3.78	1.51+1.61*C_L ns
t_r	*IN TO X	1.39	2.56	2.67	3.00	0.676+4.74*C_L ns
t_f		1.20	2.22	2.31	2.59	0.753+2.98*C_L ns
* Slowest input						

Switching characteristics

AOI211

2–1–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B: 0.088
C, D: 0.072 pF
Cell Size: 5 grids wide, 10 grids high



$X = \overline{(A \cdot B) + C + D}$

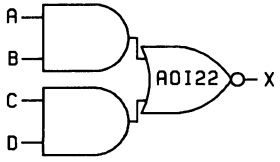
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.62	3.00	3.13	3.51	1.15+3.19*C_L ns
t_{PHL}		0.782	1.45	1.51	1.69	0.569+1.42*C_L ns
t_r	*IN TO X	2.58	4.76	4.97	5.57	1.51+7.14*C_L ns
t_f		1.32	2.43	2.54	2.84	0.899+2.78*C_L ns
* Slowest input						

Switching characteristics

2–2 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B, C: 0.088
D: 0.089 pF
Cell Size: 5 grids wide, 10 grids high



$X = \overline{(A \bullet B) + (C \bullet D)}$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

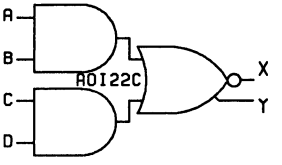
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.919	1.70	1.77	1.99	0.676+1.62*C_L ns
t_{PHL}		0.858	1.58	1.65	1.85	0.650+1.38*C_L ns
t_r	*IN TO X	1.43	2.64	2.75	3.09	0.890+3.60*C_L ns
t_f		1.26	2.33	2.43	2.73	0.847+2.77*C_L ns
* Slowest input						

Switching characteristics

AOI22C

2–2 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.089
B, C: 0.088
D: 0.089 pF
Cell Size: 7 grids wide, 10 grids high



$$X = \overline{(A \cdot B) + (C \cdot D)}$$

$$Y = (A \cdot B) + (C \cdot D)$$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

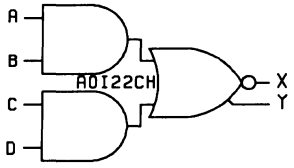
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.02	1.89	1.97	2.21	0.783+1.60*C_L ns
t_{PHL}		0.962	1.78	1.85	2.08	0.757+1.37*C_L ns
t_{PLH}	X TO Y	0.659	1.22	1.27	1.42	0.415+1.62*C_L ns
t_{PHL}		0.681	1.26	1.31	1.47	0.442+1.59*C_L ns
t_{PLH}	*IN TO Y	1.42	2.62	2.73	3.06	1.17+1.62*C_L ns
t_{PHL}		1.46	2.70	2.82	3.16	1.22+1.59*C_L ns
t_r	*IN TO X	1.75	3.24	3.38	3.79	1.22+3.55*C_L ns
t_f		1.56	2.89	3.01	3.38	1.16+2.70*C_L ns
t_r	X TO Y	1.12	2.06	2.15	2.41	0.592+3.49*C_L ns
t_f		1.07	1.97	2.06	2.31	0.635+2.89*C_L ns
t_r	*IN TO Y	1.12	2.06	2.15	2.41	0.592+3.49*C_L ns
t_f		1.07	1.97	2.06	2.31	0.635+2.89*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see Calculating Standard Cell Timings application note.

2–2 AND–OR–Invert with Complementary Outputs (High Drive)

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.158
B: 0.157
C, D: 0.159 pF
Cell Size: 13 grids wide, 10 grids high



$X = \overline{(A \cdot B) + (C \cdot D)}$

$Y = (A \cdot B) + (C \cdot D)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.849	1.57	1.63	1.83	0.728+0.803*C_L ns
t_{PHL}		1.04	1.91	1.99	2.24	0.897+0.918*C_L ns
t_{PLH}	X TO Y	0.408	0.754	0.786	0.881	0.316+0.616*C_L ns
t_{PHL}		0.389	0.719	0.750	0.841	0.296+0.622*C_L ns
t_{PLH}	*IN TO Y	1.31	2.41	2.51	2.82	1.21+0.616*C_L ns
t_{PHL}		1.12	2.06	2.15	2.41	1.02+0.622*C_L ns
t_r	*IN TO X	1.46	2.70	2.81	3.16	1.20+1.75*C_L ns
t_f		1.58	2.92	3.05	3.42	1.30+1.86*C_L ns
t_r	X TO Y	0.639	1.18	1.23	1.38	0.468+1.14*C_L ns
t_f		0.560	1.03	1.08	1.21	0.414+0.971*C_L ns
t_r	*IN TO Y	0.639	1.18	1.23	1.38	0.468+1.14*C_L ns
t_f		0.560	1.03	1.08	1.21	0.414+0.971*C_L ns
* Slowest input						

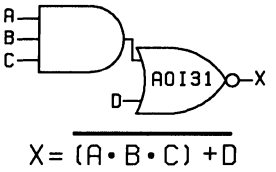
Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see Calculating Standard Cell Timings application note.

AOI31

3–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.089
B, C: 0.088
D: 0.072 pF
Cell Size: 5 grids wide, 10 grids high



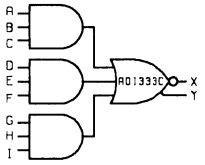
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.13	2.09	2.18	2.44	0.810+2.14*C_L ns
t_{PHL}		0.943	1.74	1.81	2.04	0.649+1.96*C_L ns
t_r	*IN TO X	2.07	3.82	3.98	4.47	1.35+4.77*C_L ns
t_f		1.34	2.48	2.58	2.90	0.726+4.10*C_L ns
* Slowest input						

Switching characteristics

3–3–3 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: A: 0.105
B: 0.106
C, D: 0.105
E: 0.106
F, G: 0.105
H: 0.106
I: 0.105 pF
Cell Size: 18 grids wide, 11 grids high



$X = \overline{(A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)}$

$Y = (A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

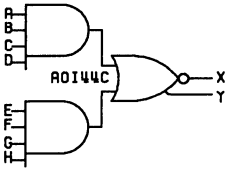
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.406	0.749	0.781	0.876	0.160+1.64*C_L ns
t_{PHL}		0.442	0.817	0.852	0.956	0.208+1.56*C_L ns
t_{PLH}	*IN TO Y	3.60	6.64	6.92	7.77	3.31+1.87*C_L ns
t_{PHL}		3.06	5.66	5.90	6.61	2.78+1.86*C_L ns
t_{PLH}	*IN TO X	3.19	5.89	6.14	6.89	2.94+1.64*C_L ns
t_{PHL}		3.76	6.94	7.24	8.12	3.52+1.56*C_L ns
t_r	Y TO X	0.930	1.72	1.79	2.01	0.388+3.61*C_L ns
t_f		0.849	1.57	1.63	1.83	0.397+3.01*C_L ns
t_r	*IN TO Y	1.99	3.68	3.84	4.31	1.49+3.35*C_L ns
t_f		1.69	3.12	3.25	3.65	1.25+2.92*C_L ns
t_r	*IN TO X	0.930	1.72	1.79	2.01	0.388+3.61*C_L ns
t_f		0.849	1.57	1.63	1.83	0.397+3.01*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays listed for "IN TO X" and delay equation for X assume no load on the Y output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

4–4 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H
Outputs: X, Y
Input Cap.: All: 0.054 pF
Cell Size: 22 grids wide, 10 grids high



$$X = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$$

$$Y = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

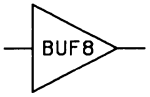
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.05	3.78	3.94	4.42	1.57+3.19*C_L ns
t_{PHL}		2.36	4.35	4.54	5.09	2.11+1.64*C_L ns
t_{PLH}	*IN TO Y	2.70	4.98	5.19	5.82	2.45+1.65*C_L ns
t_{PHL}		2.42	4.47	4.66	5.23	2.18+1.61*C_L ns
t_r	*IN TO X	1.73	3.19	3.33	3.73	0.654+7.15*C_L ns
t_f		1.21	2.23	2.33	2.61	0.766+2.94*C_L ns
t_r	*IN TO Y	0.916	1.69	1.76	1.98	0.372+3.62*C_L ns
t_f		0.909	1.68	1.75	1.96	0.457+3.01*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The Y output delay is not dependent upon the X output delay for this cell.

Noninverting Buffer (8X Drive)

BUF8 has 8 times the drive of an SBUF.



Inputs: A
Outputs: X
Input Cap.: A: 0.106 pF
Cell Size: 6 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

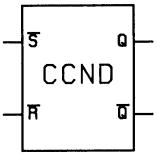
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.955	1.76	1.84	2.06	0.916+0.259*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.03+0.262*C_L ns
t_r	A TO X	0.456	0.842	0.878	0.985	0.394+0.414*C_L ns
t_f		0.501	0.925	0.964	1.08	0.449+0.344*C_L ns

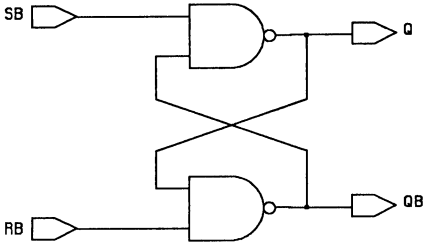
Switching characteristics

Cross–Coupled NAND Latch

CCND is very sensitive to negative spikes on SB or RB.

Inputs: SB, RB
Outputs: Q, QB
Input Cap.: All: 0.072 pF
Cell Size: 5 grids wide, 10 grids high





Functional diagram: CCND

FUNCTION TABLE

SB	RB	Q	QB
L	L	*	*
L	H	H	L
H	L	L	H
H	H	Q_o	QB_o

* Both outputs will remain high as long as SB and RB remain low, but the output states are unpredictable if SB and RB go high simultaneously.

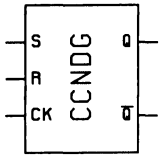
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	SB TO Q	0.805	1.49	1.55	1.74	0.557+1.65*C_L ns
t_{PHL}		0.668	1.23	1.29	1.44	0.464+1.35*C_L ns
t_{PLH}	SB TO QB	0.805	1.49	1.55	1.74	0.557+1.65*C_L ns
t_{PHL}		1.52	2.80	2.92	3.28	1.000+3.43*C_L ns
t_{PLH}	RB TO Q	0.816	1.51	1.57	1.76	0.569+1.65*C_L ns
t_{PHL}		1.53	2.83	2.95	3.31	1.02+3.43*C_L ns
t_{PLH}	RB TO QB	0.816	1.51	1.57	1.76	0.569+1.65*C_L ns
t_{PHL}		0.667	1.23	1.28	1.44	0.463+1.35*C_L ns
t_r	SB TO Q	1.29	2.39	2.49	2.79	0.744+3.64*C_L ns
t_f		1.05	1.95	2.03	2.28	0.639+2.77*C_L ns
t_r	SB TO QB	1.29	2.39	2.49	2.79	0.744+3.64*C_L ns
t_f		1.12	2.08	2.16	2.43	0.639+3.23*C_L ns
t_r	RB TO Q	1.26	2.33	2.43	2.72	0.755+3.37*C_L ns
t_f		1.11	2.05	2.14	2.40	0.626+3.23*C_L ns
t_r	RB TO QB	1.26	2.33	2.43	2.72	0.755+3.37*C_L ns
t_f		1.07	1.97	2.05	2.30	0.651+2.77*C_L ns

Switching characteristics

Gated R/S Flip–Flop

CCNDG is very sensitive to positive spikes on S and R while CK is high.



Inputs: S, CK, R
Outputs: Q, QB
Input Cap.: S: 0.055
CK: 0.108
R: 0.055 pF
Cell Size: 10 grids wide, 10 grids high

FUNCTION TABLE

CK	S	R	Q	QB
L	X	X	Q_o	QB_o
H	L	L	Q_o	QB_o
H	L	H	L	H
H	H	L	H	L
H	H	H	*	*

* Both outputs will remain high as long as S, R, and CK are high, but the output states are unpredictable if S and R go low simultaneously or if CK goes low while S and R are still high.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	S TO Q	1.31	2.42	2.52	2.83	1.06+1.66*C_L ns
t_{PHL}		1.41	2.61	2.72	3.05	0.999+2.76*C_L ns
t_{PHL}	S TO QB	2.39	4.42	4.60	5.16	1.64+4.97*C_L ns
t_{PLH}	CK TO Q	1.30	2.40	2.50	2.81	1.05+1.66*C_L ns
t_{PHL}		2.37	4.38	4.57	5.12	1.63+4.97*C_L ns
t_{PLH}	CK TO QB	1.31	2.43	2.53	2.84	1.07+1.64*C_L ns
t_{PHL}		2.38	4.40	4.58	5.14	1.63+4.97*C_L ns
t_{PHL}	R TO Q	2.39	4.42	4.60	5.16	1.64+4.97*C_L ns
t_{PLH}	R TO QB	1.31	2.42	2.52	2.83	1.06+1.66*C_L ns
t_{PHL}		1.41	2.61	2.72	3.05	0.999+2.76*C_L ns
t_r	S TO Q	1.18	2.19	2.28	2.56	0.640+3.63*C_L ns
t_f		1.67	3.08	3.21	3.61	0.816+5.69*C_L ns
t_f	S TO QB	1.72	3.17	3.31	3.71	0.820+5.98*C_L ns
t_r	CK TO Q	1.21	2.24	2.33	2.62	0.674+3.57*C_L ns
t_f		1.72	3.17	3.30	3.71	0.817+5.99*C_L ns
t_r	CK TO QB	1.22	2.25	2.35	2.64	0.685+3.57*C_L ns
t_f		1.72	3.17	3.30	3.71	0.818+5.98*C_L ns
t_f	R TO Q	1.72	3.17	3.31	3.71	0.820+5.98*C_L ns
t_r	R TO QB	1.18	2.19	2.28	2.56	0.640+3.63*C_L ns
t_f		1.67	3.08	3.21	3.61	0.816+5.69*C_L ns

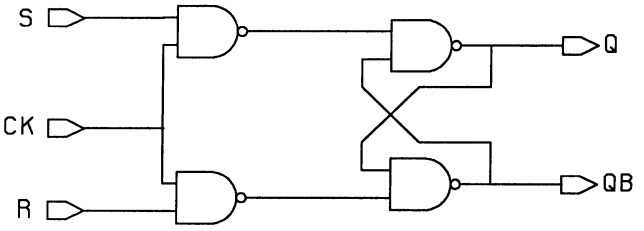
Switching characteristics

CCNDG

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	S to CK	3.00	ns
t_{su}	R to CK	3.00	ns
t_h	CK to S	3.00	ns
t_h	CK to R	3.00	ns
t_{pwh}	High CK Pulse Width	5.00	ns

Timing requirements

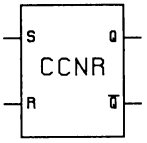


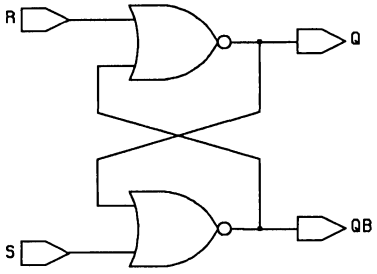
Functional diagram: CCNDG

Cross–Coupled NOR Latch

CCNR is very sensitive to positive spikes on S and R.

Inputs: S, R
Outputs: Q, QB
Input Cap.: All: 0.055 pF
Cell Size: 5 grids wide, 10 grids high





Functional diagram: CCNR

FUNCTION TABLE

S	R	Q	QB
L	L	Q_o	QB_o
L	H	L	H
H	L	H	L
H	H	*	*

* Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

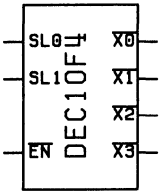
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	S TO Q	1.92	3.54	3.69	4.14	1.14+5.17*C_L ns
t_{PHL}		0.721	1.33	1.39	1.56	0.487+1.56*C_L ns
t_{PLH}	S TO QB	1.19	2.19	2.29	2.57	0.709+3.19*C_L ns
t_{PHL}		0.721	1.33	1.39	1.56	0.487+1.56*C_L ns
t_{PLH}	R TO Q	1.13	2.08	2.17	2.43	0.648+3.19*C_L ns
t_{PHL}		0.704	1.30	1.36	1.52	0.470+1.56*C_L ns
t_{PLH}	R TO QB	1.96	3.62	3.78	4.24	1.19+5.16*C_L ns
t_{PHL}		0.704	1.30	1.36	1.52	0.470+1.56*C_L ns
t_r	S TO Q	2.22	4.10	4.27	4.79	1.11+7.36*C_L ns
t_f		1.01	1.87	1.95	2.19	0.552+3.07*C_L ns
t_r	S TO QB	2.28	4.20	4.38	4.92	1.20+7.19*C_L ns
t_f		1.01	1.87	1.95	2.19	0.552+3.07*C_L ns
t_r	R TO Q	2.18	4.03	4.20	4.72	1.10+7.19*C_L ns
t_f		0.967	1.79	1.86	2.09	0.507+3.07*C_L ns
t_r	R TO QB	2.31	4.26	4.44	4.98	1.20+7.36*C_L ns
t_f		0.967	1.79	1.86	2.09	0.507+3.07*C_L ns

Switching characteristics

DEC1OF4

1–of–4 Decoder

Inputs: SL0, SL1, ENB
Outputs: X0B, X1B, X2B, X3B
Input Cap.: SL0, SL1: 0.200
ENB: 0.055 pF
Cell Size: 25 grids wide, 12 grids high



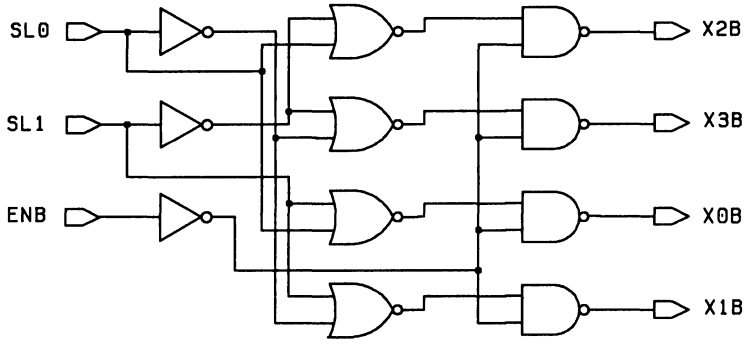
FUNCTION TABLE

SL0	SL1	ENB	X0B	X1B	X2B	X3B
X	X	H	H	H	H	H
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

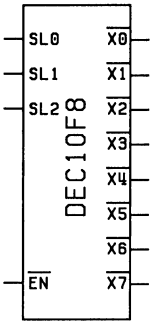
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*SL TO XnB	1.80	3.32	3.46	3.88	1.63+1.12*C_L ns
t_{PHL}		2.33	4.31	4.49	5.04	1.92+2.77*C_L ns
t_{PLH}	*ENB TO XnB	1.43	2.64	2.75	3.09	1.26+1.15*C_L ns
t_{PHL}		1.95	3.60	3.76	4.21	1.53+2.78*C_L ns
t_r	*SL TO XnB	0.776	1.43	1.49	1.68	0.420+2.37*C_L ns
t_f		1.51	2.79	2.91	3.26	0.668+5.61*C_L ns
t_r	*ENB TO XnB	0.963	1.78	1.85	2.08	0.615+2.32*C_L ns
t_f		1.53	2.83	2.95	3.30	0.689+5.60*C_L ns
* SL timing applies to both SL0 and SL1. XnB represents any output.						

Switching characteristics


SL0
SL1
ENB
X2B
X3B
X0B
X1B

1–of–8 Decoder

Inputs: SL0, SL1, SL2, ENB
Outputs: X0B, X1B, X2B, X3B, X4B, X5B, X6B, X7B
Input Cap.: All: 0.055 pF
Cell Size: 48 grids wide, 14 grids high



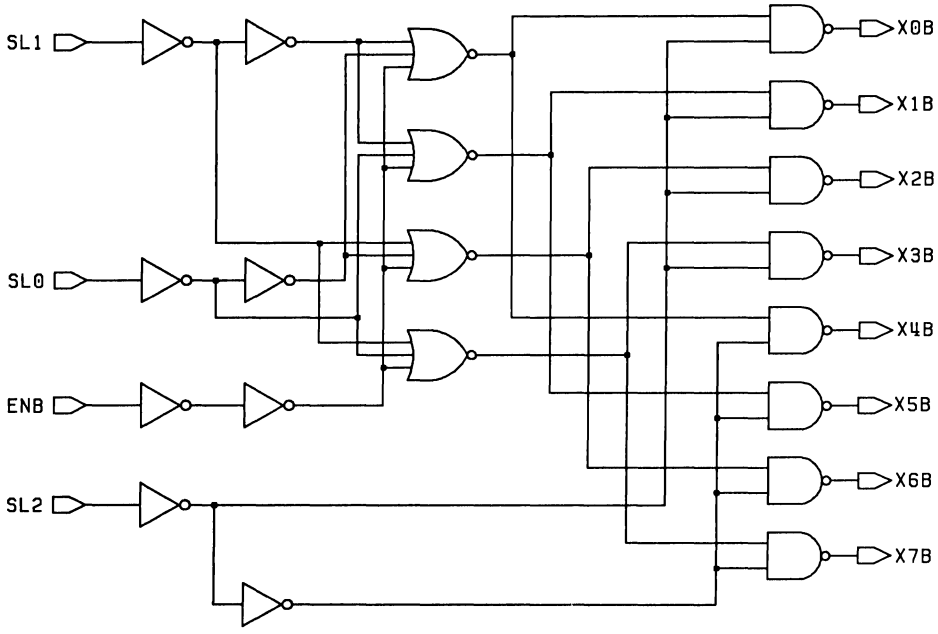
FUNCTION TABLE

SL0	SL1	SL2	ENB	X0B	X1B	X2B	X3B	X4B	X5B	X6B	X7B
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*ENB TO XnB	2.97	5.49	5.72	6.42	2.72+1.67*C_L ns
t_{PHL}		3.44	6.36	6.63	7.44	3.02+2.79*C_L ns
t_{PLH}	*SL2 TO XnB	3.25	6.00	6.25	7.02	2.99+1.69*C_L ns
t_{PHL}		3.39	6.26	6.52	7.32	2.96+2.81*C_L ns
t_r	*ENB TO XnB	1.00	1.85	1.93	2.16	0.462+3.58*C_L ns
t_f		1.55	2.86	2.98	3.34	0.715+5.55*C_L ns
t_r	*SL2 TO XnB	1.09	2.01	2.09	2.35	0.555+3.55*C_L ns
t_f		1.55	2.86	2.98	3.35	0.716+5.55*C_L ns
* ENB timing applies to SL0, SL1 and ENB. XnB represents any output.						

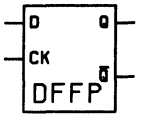
Switching characteristics



Functional diagram: DEC1OF8

D Flip–Flop, Positive Edge Triggered

DFFP is a fully static D-type flip-flop. It is positive edge triggered with respect to the single phase clock input (CK). For a faster version of this cell, see DFFPF.



Inputs: D, CK
Outputs: Q, QB
Input Cap.: D: 0.039
CK: 0.055 pF
Cell Size: 17 grids wide, 11 grids high

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

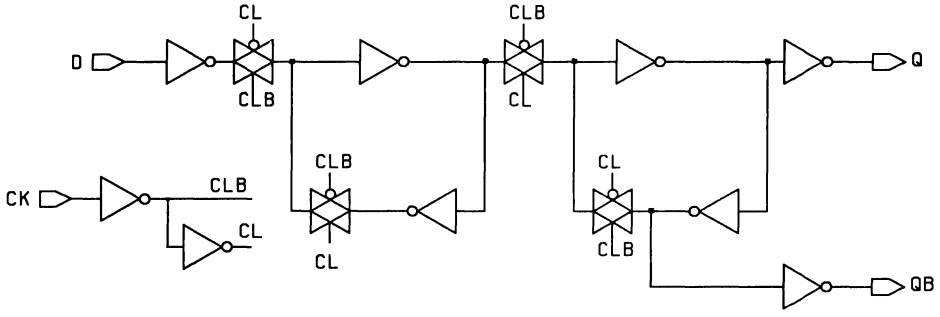
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	2.65	4.90	5.11	5.73	2.52+0.856*C_L ns
t_{PHL}		2.54	4.69	4.89	5.49	2.41+0.839*C_L ns
t_{PLH}	CK TO QB	3.14	5.80	6.04	6.78	3.01+0.812*C_L ns
t_{PHL}		3.30	6.10	6.36	7.14	3.18+0.793*C_L ns
t_r	CK TO Q	0.754	1.39	1.45	1.63	0.493+1.74*C_L ns
t_f		0.678	1.25	1.31	1.46	0.460+1.45*C_L ns
t_r	CK TO QB	0.702	1.30	1.35	1.52	0.441+1.74*C_L ns
t_f		0.638	1.18	1.23	1.38	0.419+1.46*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	2.00	ns
t_h	Hold Time CK to D	−0.75	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	Low CK Pulse Width	4.75	ns

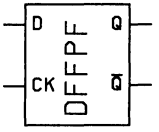
Timing requirements



Functional diagram: DFFP

Fast D Flip–Flop, Positive Edge Triggered

DFFPF is a fully static D-type flip-flop. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q, QB
Input Cap.: D: 0.083
CK: 0.205 pF
Cell Size: 13 grids wide, 13 grids high

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

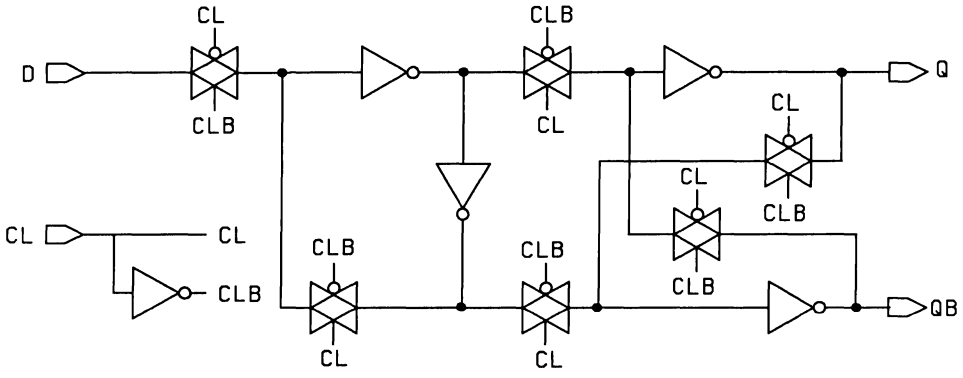
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	0.863	1.59	1.66	1.86	0.650+1.41*C_L ns
t_{PHL}		1.35	2.49	2.60	2.91	1.12+1.53*C_L ns
t_{PLH}	CK TO QB	0.880	1.63	1.69	1.90	0.670+1.40*C_L ns
t_{PHL}		1.35	2.49	2.59	2.91	1.12+1.53*C_L ns
t_r	CK TO Q	0.840	1.55	1.62	1.81	0.376+3.09*C_L ns
t_f		0.924	1.71	1.78	2.00	0.507+2.78*C_L ns
t_r	CK TO QB	0.867	1.60	1.67	1.87	0.407+3.06*C_L ns
t_f		0.951	1.76	1.83	2.05	0.536+2.77*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.25	ns
t_h	Hold Time CK to D	0.00	ns
t_{pwh}	High CK Pulse Width	3.75	ns
t_{pwl}	Low CK Pulse Width	3.75	ns

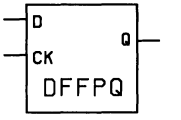
Timing requirements



Functional diagram: DFFPF

D Flip–Flop, Positive Edge Triggered

DFFPQ is a fully static D-type flip-flop with only a Q output. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q
Input Cap.: D: 0.038
CK: 0.145 pF
Cell Size: 10 grids wide, 10 grids high

FUNCTION TABLE

D	CK	Q
L	↑	L
H	↑	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

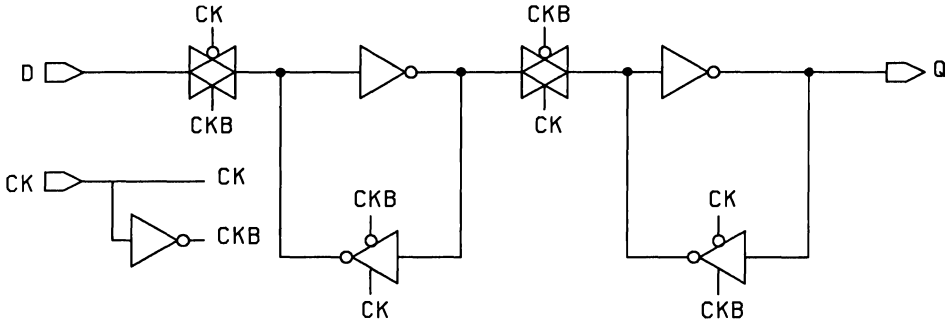
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	0.806	1.49	1.55	1.74	0.663+0.952*C_L ns
t_{PHL}		1.09	2.01	2.10	2.36	0.942+0.987*C_L ns
t_r	CK TO Q	0.679	1.25	1.31	1.47	0.386+1.95*C_L ns
t_f		0.717	1.32	1.38	1.55	0.475+1.61*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−0.50	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	Low CK Pulse Width	4.25	ns

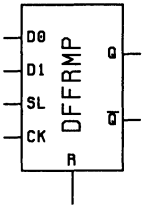
Timing requirements



Functional diagram: DFFPQ

D Flip–Flop with Reset and Multiplexed Inputs, Positive Edge Triggered

DFFRMP is a fully static D-type edge triggered flip-flop with a multiplexed D input. Selection of D0 or D1 is controlled by SL. It is positive edge triggered with respect to the single clock input CK. R is asynchronous and active high.



Inputs: R, D0, D1, SL, CK
Outputs: Q, QB
Input Cap.: R, D0, D1, SL: 0.056
CK: 0.055 pF
Cell Size: 29 grids wide, 12 grids high

FUNCTION TABLE

D0	D1	SL	R	CK	Q	QB
X	X	X	H	X	L	H
H	X	H	L	↑	H	L
L	X	H	L	↑	L	H
X	H	L	L	↑	H	L
X	L	L	L	↑	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

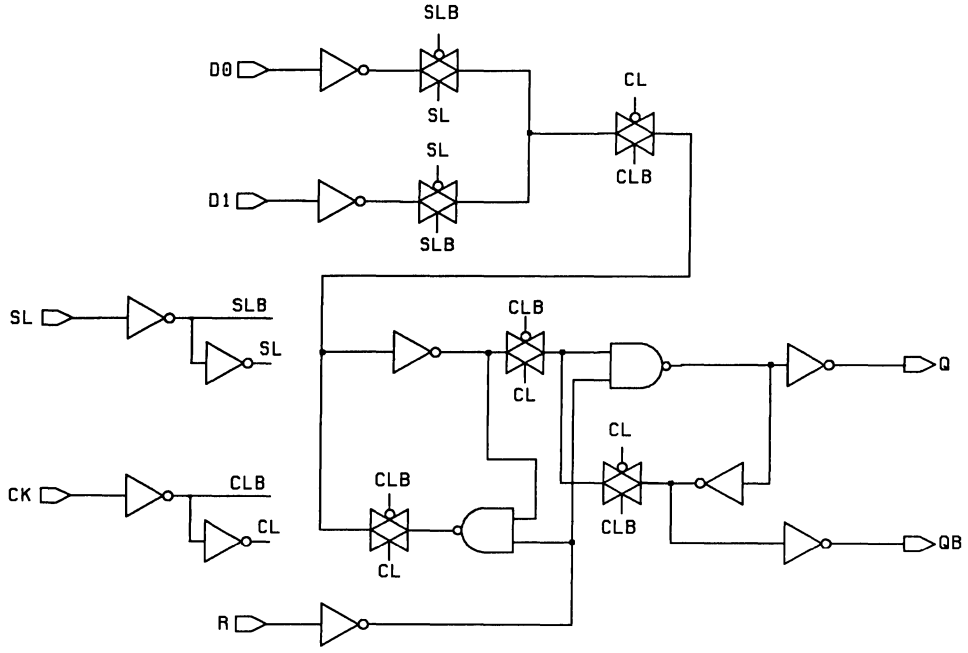
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	R TO Q	1.98	3.66	3.82	4.29	1.74+1.64*C_L ns
t_{PLH}	R TO QB	3.29	6.08	6.34	7.11	3.04+1.66*C_L ns
t_{PLH}	CK TO Q	3.60	6.66	6.94	7.79	3.35+1.69*C_L ns
t_{PHL}		3.31	6.12	6.37	7.15	3.07+1.57*C_L ns
t_{PLH}	CK TO QB	2.58	4.77	4.97	5.58	2.34+1.65*C_L ns
t_{PHL}		2.65	4.89	5.10	5.72	2.41+1.60*C_L ns
t_f	R TO Q	0.952	1.76	1.83	2.06	0.504+2.99*C_L ns
t_r	R TO QB	0.949	1.75	1.83	2.05	0.409+3.60*C_L ns
t_r	CK TO Q	1.06	1.95	2.04	2.28	0.521+3.57*C_L ns
t_f		0.856	1.58	1.65	1.85	0.403+3.01*C_L ns
t_r	CK TO QB	0.967	1.79	1.86	2.09	0.428+3.59*C_L ns
t_f		0.839	1.55	1.62	1.81	0.384+3.03*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D0 to CK	3.00	ns
t_{su}	Setup Time D1 to CK	3.00	ns
t_{su}	Setup Time SL to CK	4.00	ns
t_h	Hold Time CK to D0	−2.00	ns
t_h	Hold Time CK to D1	−2.00	ns
t_h	Hold Time CK to SL	−3.00	ns
t_{pwh}	R Pulse Width (high)	4.75	ns
t_{pwh}	High CK Pulse Width	4.50	ns
t_{pwl}	Low CK Pulse Width	4.75	ns
rt	R Recovery Time	−0.50	ns

Timing requirements

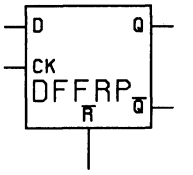


Functional diagram: DFFRMP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRP is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low. For a faster version of this cell, see DFFRPF.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.143
D: 0.038
CK: 0.054 pF
Cell Size: 20 grids wide, 12 grids high



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

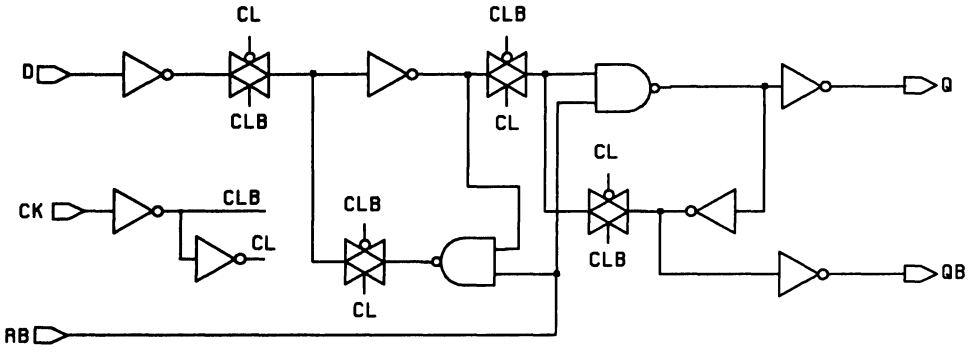
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	2.56	4.73	4.93	5.54	2.43+0.858*C_L ns
t_{PHL}		2.56	4.73	4.93	5.54	2.44+0.830*C_L ns
t_{PLH}	CK TO QB	3.08	5.70	5.94	6.66	2.96+0.815*C_L ns
t_{PHL}		3.71	6.85	7.14	8.01	3.58+0.845*C_L ns
t_{PHL}	RB TO Q	1.27	2.35	2.45	2.75	1.14+0.859*C_L ns
t_{PLH}	RB TO QB	2.17	4.00	4.17	4.68	2.03+0.891*C_L ns
t_r	CK TO Q	0.718	1.33	1.38	1.55	0.455+1.75*C_L ns
t_f		0.656	1.21	1.26	1.42	0.437+1.46*C_L ns
t_r	CK TO QB	0.686	1.27	1.32	1.48	0.424+1.75*C_L ns
t_f		0.817	1.51	1.57	1.77	0.603+1.43*C_L ns
t_f	RB TO Q	0.690	1.27	1.33	1.49	0.472+1.45*C_L ns
t_r	RB TO QB	0.804	1.48	1.55	1.74	0.541+1.75*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	-0.75	ns
t_{pwh}	High CK Pulse Width	4.25	ns
t_{pwl}	RB Pulse Width (low)	4.50	ns
t_{pwl}	Low CK Pulse Width	4.50	ns
rt	RB Recovery Time	-2.00	ns

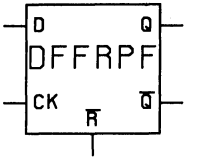
Timing requirements



Functional diagram: DFFRP

Fast D Flip–Flop with Reset, Positive Edge Triggered

DFFRPF is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.



Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.251
D: 0.115
CK: 0.200 pF
Cell Size: 18 grids wide, 14 grids high

FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

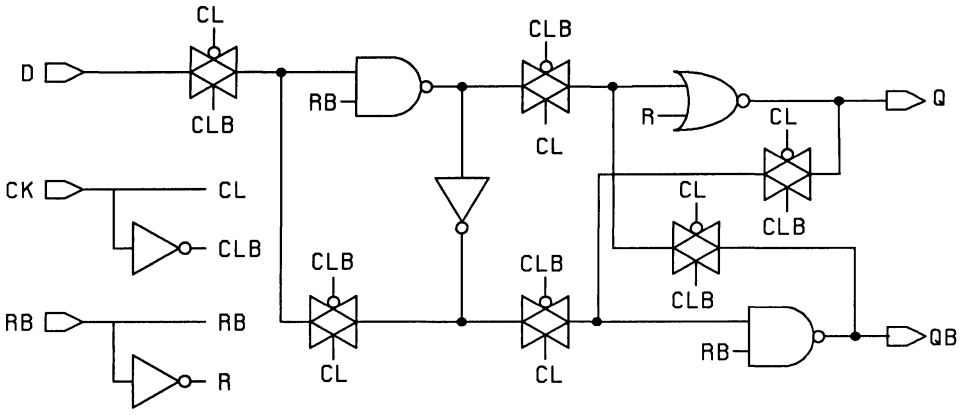
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.04	1.91	1.99	2.24	0.831+1.36*C_L ns
t_{PHL}		1.78	3.29	3.43	3.85	1.55+1.55*C_L ns
t_{PLH}	CK TO QB	1.07	1.98	2.07	2.32	0.859+1.43*C_L ns
t_{PHL}		1.37	2.53	2.64	2.96	1.17+1.36*C_L ns
t_{PHL}	RB TO Q	1.45	2.69	2.80	3.14	1.23+1.52*C_L ns
t_{PLH}	RB TO QB	0.793	1.47	1.53	1.71	0.561+1.55*C_L ns
t_r	CK TO Q	1.16	2.15	2.24	2.51	0.713+3.00*C_L ns
t_f		1.22	2.25	2.35	2.63	0.803+2.77*C_L ns
t_r	CK TO QB	0.996	1.84	1.92	2.15	0.530+3.10*C_L ns
t_f		1.02	1.89	1.97	2.21	0.640+2.55*C_L ns
t_f	RB TO Q	1.45	2.69	2.80	3.14	1.09+2.44*C_L ns
t_r	RB TO QB	1.78	3.28	3.42	3.84	1.40+2.51*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.25	ns
t_h	Hold Time CK to D	−0.25	ns
t_{pwh}	High CK Pulse Width	3.75	ns
t_{pwl}	RB Pulse Width (low)	5.50	ns
t_{pwl}	Low CK Pulse Width	3.75	ns
rt	RB Recovery Time	0.50	ns

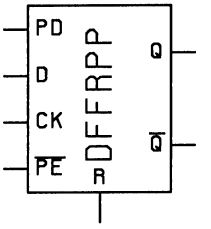
Timing requirements



Functional diagram: DFFRPF

D Flip–Flop with Reset and Parallel Data Input, Positive Edge Triggered

DFFRPP is a D–type, positive edge triggered flip–flop with parallel load, and single clock input. Parallel data from PD is transparent when PEB is low. R is asynchronous and active high.



Inputs: R, D, PD, PEB, CK
Outputs: Q, QB
Input Cap.: R: 0.056
D, PD, PEB, CK: 0.055 pF
Cell Size: 29 grids wide, 12 grids high

FUNCTION TABLE

R	D	PD	PEB	CK	Q	QB
H	X	X	X	X	L	H
L	X	H	L	X	H	L
L	X	L	L	X	L	H
L	H	X	H	↑	H	L
L	L	X	H	↑	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	R TO Q	2.11	3.90	4.07	4.56	1.97+0.944*C_L ns
t_{PHL}		1.74	3.21	3.35	3.76	1.61+0.859*C_L ns
t_{PLH}	R TO QB	2.64	4.88	5.08	5.70	2.51+0.873*C_L ns
t_{PHL}		2.81	5.18	5.40	6.06	2.69+0.797*C_L ns
t_{PLH}	CK TO Q	3.00	5.55	5.78	6.49	2.86+0.952*C_L ns
t_{PHL}		2.53	4.67	4.87	5.46	2.40+0.840*C_L ns
t_{PLH}	CK TO QB	3.14	5.80	6.05	6.79	3.02+0.810*C_L ns
t_{PHL}		3.69	6.82	7.11	7.98	3.57+0.809*C_L ns
t_{PLH}	PD TO Q	3.59	6.64	6.92	7.76	3.45+0.956*C_L ns
t_{PHL}		3.30	6.10	6.36	7.14	3.17+0.853*C_L ns
t_{PLH}	PD TO QB	3.92	7.24	7.55	8.47	3.80+0.822*C_L ns
t_{PHL}		4.29	7.92	8.26	9.26	4.17+0.807*C_L ns
t_{PLH}	PEB TO Q	4.17	7.70	8.02	9.00	4.02+0.956*C_L ns
t_{PHL}		3.34	6.17	6.43	7.21	3.21+0.850*C_L ns
t_{PLH}	PEB TO QB	3.95	7.30	7.61	8.53	3.83+0.824*C_L ns
t_{PHL}		4.86	8.98	9.36	10.5	4.74+0.807*C_L ns
t_r	R TO Q	0.889	1.64	1.71	1.92	0.625+1.75*C_L ns
t_f		0.714	1.32	1.37	1.54	0.497+1.45*C_L ns
t_r	R TO QB	0.800	1.48	1.54	1.73	0.539+1.74*C_L ns

Switching characteristics (Sheet 1 of 2)

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		0.666	1.23	1.28	1.44	0.449+1.44*C_L ns
t_r	CK TO Q	0.883	1.63	1.70	1.91	0.618+1.76*C_L ns
t_f		0.690	1.27	1.33	1.49	0.472+1.45*C_L ns
t_r	CK TO QB	0.701	1.30	1.35	1.52	0.441+1.74*C_L ns
t_f		0.646	1.19	1.24	1.39	0.426+1.46*C_L ns
t_r	PD TO Q	0.897	1.66	1.73	1.94	0.632+1.76*C_L ns
t_f		0.704	1.30	1.35	1.52	0.487+1.44*C_L ns
t_r	PD TO QB	0.686	1.27	1.32	1.48	0.423+1.75*C_L ns
t_f		0.652	1.20	1.26	1.41	0.433+1.46*C_L ns
t_r	PEB TO Q	0.893	1.65	1.72	1.93	0.629+1.76*C_L ns
t_f		0.706	1.30	1.36	1.53	0.490+1.44*C_L ns
t_r	PEB TO QB	0.661	1.22	1.27	1.43	0.398+1.75*C_L ns
t_f		0.650	1.20	1.25	1.40	0.431+1.46*C_L ns

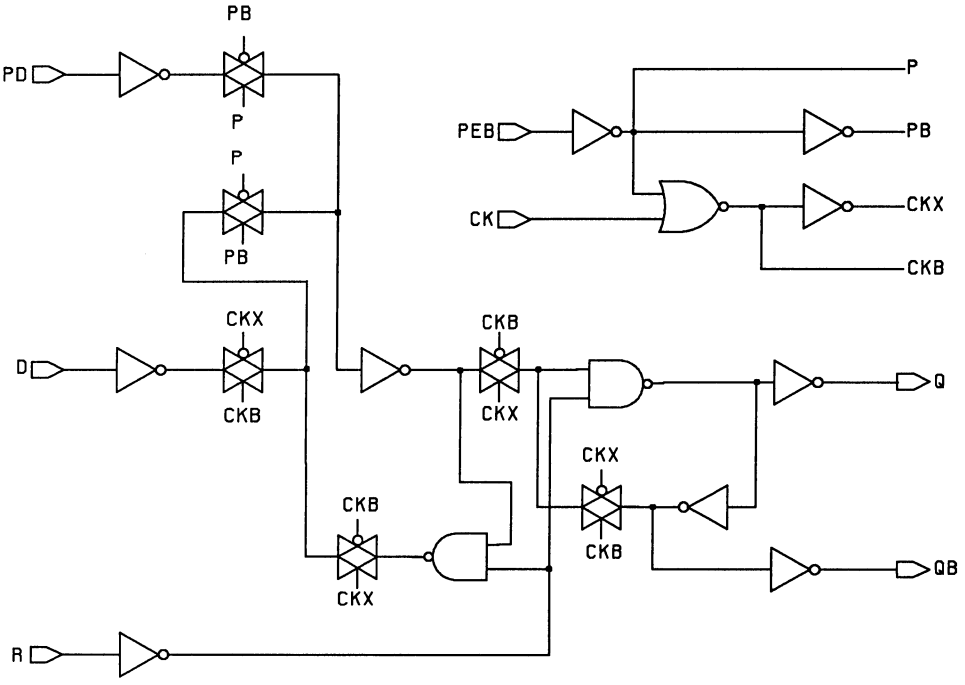
Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	2.50	ns
t_{su}	Setup Time PD to PEB	1.50	ns
t_h	Hold Time CK to D	0.00	ns
t_h	Hold Time PEB to PD	0.00	ns
t_{pwh}	R Pulse Width (high)	5.50	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	PEB Pulse Width (low)	5.00	ns
t_{pwl}	Low CK Pulse Width	6.50	ns
rt	R Recovery Time	-2.75	ns
rt	PEB Recovery Time	5.75	ns

Timing requirements

DFFRPP

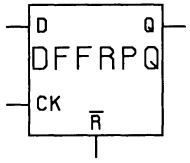


Functional diagram: DFFRPP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRPQ is a fully static D-type, positive edge triggered flip-flop with only a Q output. RB is asynchronous and active low.

Inputs: D, CK, RB
Outputs: Q
Input Cap.: D: 0.038
CK: 0.167
RB: 0.171 pF
Cell Size: 13 grids wide, 11 grids high



FUNCTION TABLE

D	CK	RB	Q
L	↑	H	L
H	↑	H	H
X	X	L	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.05	1.94	2.02	2.27	0.829+1.46*C_L ns
t_{PHL}		1.24	2.29	2.39	2.68	1.06+1.18*C_L ns
t_{PHL}	RB TO Q	0.956	1.76	1.84	2.06	0.856+0.663*C_L ns
t_r	CK TO Q	1.16	2.14	2.23	2.50	0.706+3.02*C_L ns
t_f		0.861	1.59	1.66	1.86	0.563+1.99*C_L ns
t_f	RB TO Q	0.537	0.992	1.03	1.16	0.387+0.998*C_L ns

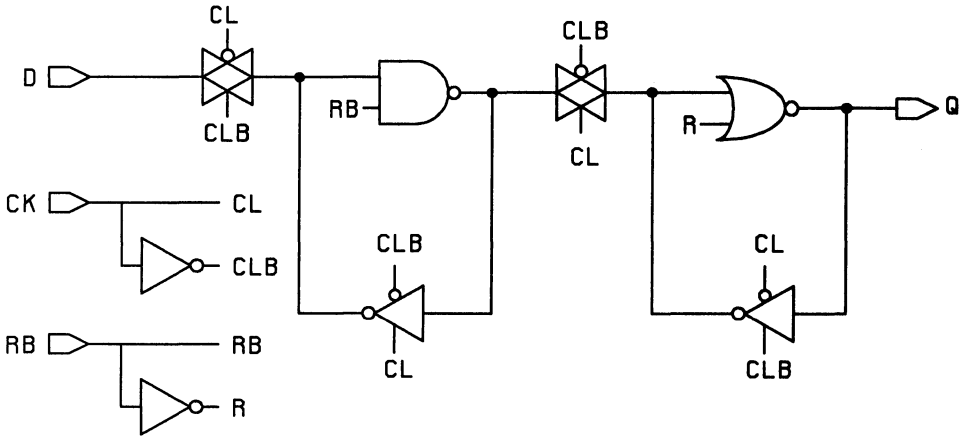
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−0.50	ns
t_{pwh}	High CK Pulse Width	3.75	ns
t_{pwl}	RB Pulse Width (low)	4.25	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	RB Recovery Time	0.00	ns

Timing requirements

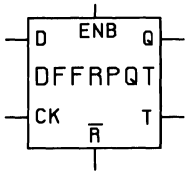
DFFRPQ



Functional diagram: DFFRPQ

D Flip–Flop with Reset and Tristate, Positive Edge Triggered

DFFRPQT is a fully static D-type, positive edge triggered flip-flop with only a Q output. RB is asynchronous and active low. When ENB is high, the T output is in a Hi-Z state and Q functions as a normal flip-flop using any of the given states defined for Q in the Function Table.



Inputs: ENB, D, CK, RB
Outputs: Q, T
Input Cap.: ENB: 0.124
D: 0.038
CK: 0.169
RB: 0.153 pF
Output Cap.: T: 0.152 pF
Cell Size: 17 grids wide, 11 grids high

FUNCTION TABLE

D	CK	RB	ENB	Q	T
L	↑	H	L	L	L
H	↑	H	L	H	H
X	X	L	L	L	L
L	↑	H	H	L	HiZ
H	↑	H	H	H	HiZ
X	X	L	H	L	HiZ

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.25	2.30	2.40	2.69	1.02+1.48*C_L ns
t_{PHL}		1.44	2.66	2.77	3.11	1.28+1.09*C_L ns
t_{PLH}	CK TO T	1.30	2.40	2.50	2.81	1.06+1.57*C_L ns
t_{PHL}		1.50	2.77	2.89	3.24	1.30+1.33*C_L ns
t_{PHL}	RB TO Q	0.993	1.83	1.91	2.15	0.897+0.639*C_L ns
t_{PHL}	RB TO T	1.92	3.54	3.69	4.14	1.72+1.30*C_L ns
t_{PLH}	ENB TO T	0.583	1.08	1.12	1.26	0.316+1.78*C_L ns
t_{PHL}		0.865	1.60	1.67	1.87	0.651+1.42*C_L ns
t_r	CK TO Q	1.23	2.28	2.38	2.67	0.781+3.02*C_L ns
t_f		0.983	1.82	1.89	2.12	0.738+1.63*C_L ns
t_r	CK TO T	1.28	2.37	2.47	2.77	0.778+3.36*C_L ns
t_f		1.24	2.30	2.39	2.68	0.872+2.46*C_L ns
t_f	RB TO Q	0.552	1.02	1.06	1.19	0.420+0.881*C_L ns
t_f	RB TO T	1.23	2.28	2.37	2.66	0.864+2.45*C_L ns
t_r	ENB TO T	1.13	2.09	2.18	2.45	0.610+3.48*C_L ns
t_f		1.02	1.89	1.97	2.21	0.636+2.57*C_L ns

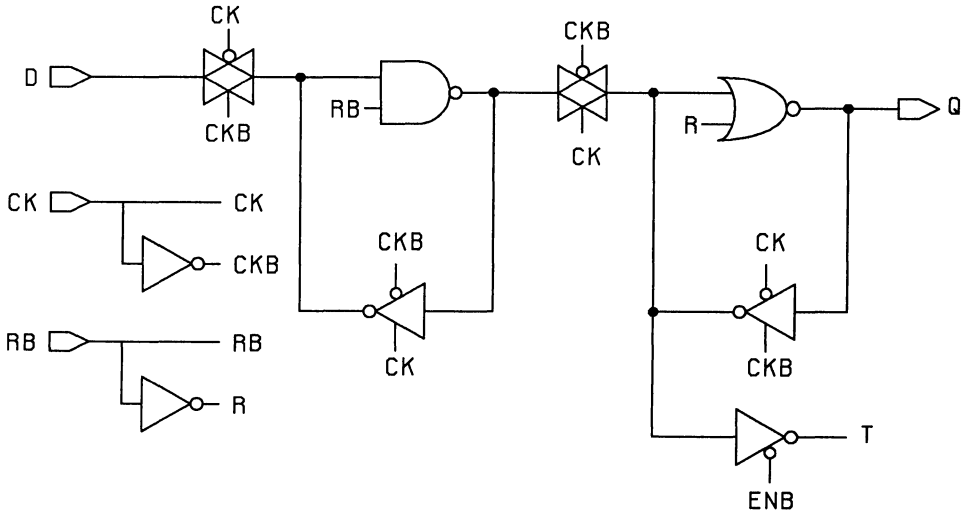
Switching characteristics

DFFRPQT

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−0.50	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	RB Pulse Width (low)	4.25	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	RB Recovery Time	0.00	ns
rt		−0.50	ns

Timing requirements

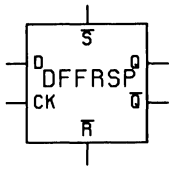


Functional diagram: DFFRPQT

D Flip–Flop with Reset and Set, Positive Edge Triggered

DFFRSP is a fully static D-type positive edge triggered flip-flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.144
D: 0.038
CK: 0.055
RB: 0.144 pF
Cell Size: 26 grids wide, 12 grids high



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	3.83	7.07	7.37	8.27	3.70+0.841*C_L ns
t_{PHL}		3.75	6.92	7.21	8.09	3.62+0.822*C_L ns
t_{PLH}	CK TO QB	3.19	5.90	6.15	6.90	3.07+0.835*C_L ns
t_{PHL}		3.24	5.98	6.23	6.99	3.11+0.806*C_L ns
t_{PHL}	RB TO Q	2.71	5.01	5.23	5.86	2.59+0.822*C_L ns
t_{PLH}	RB TO QB	1.82	3.36	3.51	3.93	1.70+0.831*C_L ns
t_{PHL}		1.60	2.95	3.07	3.45	1.47+0.815*C_L ns
t_{PLH}	SB TO Q	2.10	3.89	4.05	4.54	1.98+0.845*C_L ns
t_{PHL}		1.82	3.37	3.51	3.94	1.70+0.822*C_L ns
t_{PHL}	SB TO QB	3.17	5.86	6.11	6.85	3.05+0.815*C_L ns
t_r	CK TO Q	0.679	1.25	1.31	1.47	0.415+1.76*C_L ns
t_f		0.622	1.15	1.20	1.34	0.402+1.47*C_L ns
t_r	CK TO QB	0.690	1.27	1.33	1.49	0.428+1.74*C_L ns
t_f		0.632	1.17	1.22	1.37	0.413+1.46*C_L ns
t_f	RB TO Q	0.648	1.20	1.25	1.40	0.429+1.46*C_L ns
t_r	RB TO QB	0.708	1.31	1.36	1.53	0.448+1.73*C_L ns
t_f		0.646	1.19	1.24	1.39	0.428+1.45*C_L ns
t_r	SB TO Q	0.691	1.28	1.33	1.49	0.428+1.75*C_L ns
t_f		0.641	1.18	1.23	1.38	0.421+1.46*C_L ns
t_f	SB TO QB	0.653	1.21	1.26	1.41	0.435+1.45*C_L ns

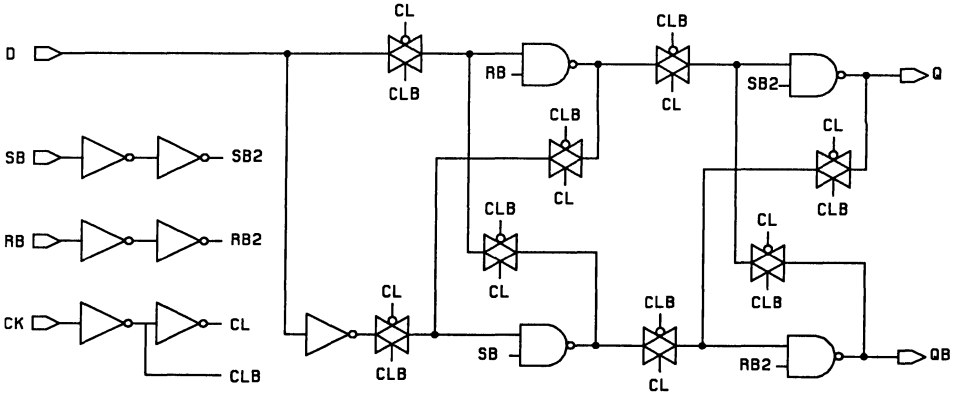
Switching characteristics

DFFRSP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.75	ns
t_h	Hold Time CK to D	−1.00	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
t_{pwl}	SB Pulse Width (low)	4.75	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	RB Recovery Time	−2.25	ns
rt	SB Recovery Time	−0.50	ns

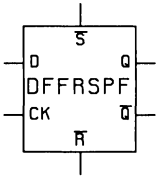
Timing requirements



Functional diagram: DFFRSP

Fast D Flip–Flop with Reset and Set Positive Edge Triggered

DFFRSPF is a fully static D-type positive edge triggered flip-flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.



Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.169
D: 0.105
CK: 0.106
RB: 0.169 pF
Cell Size: 30 grids wide, 12 grids high

FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.84	3.40	3.54	3.97	1.70+0.895*C_L ns
t_{PHL}		1.67	3.09	3.22	3.62	1.56+0.751*C_L ns
t_{PLH}	CK TO QB	1.84	3.40	3.55	3.98	1.71+0.895*C_L ns
t_{PHL}		1.68	3.09	3.23	3.62	1.56+0.739*C_L ns
t_{PHL}	RB TO Q	3.51	6.49	6.77	7.59	3.20+2.07*C_L ns
t_{PLH}	RB TO QB	2.02	3.73	3.89	4.36	1.89+0.882*C_L ns
t_{PHL}		1.71	3.16	3.29	3.69	1.59+0.776*C_L ns
t_{PLH}	SB TO Q	2.04	3.77	3.93	4.41	1.91+0.890*C_L ns
t_{PHL}		1.73	3.20	3.33	3.74	1.61+0.788*C_L ns
t_{PHL}	SB TO QB	3.54	6.53	6.81	7.64	3.22+2.08*C_L ns
t_r	CK TO Q	0.869	1.61	1.67	1.88	0.598+1.81*C_L ns
t_f		0.771	1.42	1.49	1.67	0.563+1.39*C_L ns
t_r	CK TO QB	0.863	1.59	1.66	1.86	0.593+1.80*C_L ns
t_f		0.766	1.41	1.47	1.65	0.556+1.39*C_L ns
t_f	RB TO Q	1.67	3.08	3.21	3.61	1.42+1.65*C_L ns
t_r	RB TO QB	1.48	2.73	2.85	3.20	1.20+1.87*C_L ns

Switching characteristics (Sheet 1 of 2)

DFFRSPF

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

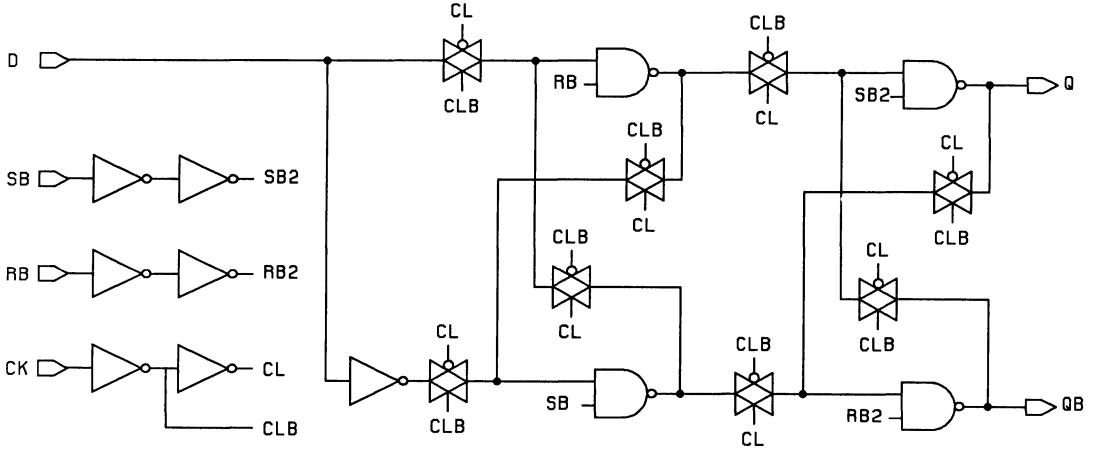
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.25	2.32	2.41	2.71	1.05+1.37*C_L ns
t_r	SB TO Q	1.47	2.72	2.84	3.19	1.19+1.87*C_L ns
t_f		1.26	2.33	2.43	2.72	1.06+1.36*C_L ns
t_f	SB TO QB	1.66	3.06	3.19	3.58	1.41+1.66*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	0.50	ns
t_h	Hold Time CK to D	0.50	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	RB Pulse Width (low)	6.00	ns
t_{pwl}	SB Pulse Width (low)	6.00	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	RB Recovery Time	-3.00	ns
rt	SB Recovery Time	-3.00	ns

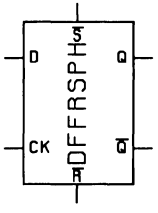
Timing requirements



Functional diagram: DFFRSPF

Buffered D Flip–Flop with Reset and Set, Positive Edge Triggered (High Drive)

DFFRSPH is a fully static D–type, edge triggered flip–flop. It is positive edge triggered with respect to the single phase clock (CK). RB and SB are asynchronous and active low.



Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.163
D: 0.089
CK: 0.105
RB: 0.178 pF
Cell Size: 25 grids wide, 12 grids high

FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be low when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	SB TO Q	2.35	4.34	4.53	5.08	2.26+0.597*C_L ns
t_{PLH}	RB TO Q	1.15	2.12	2.21	2.48	1.05+0.614*C_L ns
t_{PHL}		1.04	1.91	1.99	2.24	0.942+0.623*C_L ns
t_{PLH}	CK TO Q	2.24	4.13	4.31	4.83	2.14+0.632*C_L ns
t_{PHL}		2.67	4.93	5.14	5.77	2.58+0.613*C_L ns
t_{PLH}	SB TO QB	1.31	2.43	2.53	2.84	1.21+0.695*C_L ns
t_{PHL}		1.17	2.16	2.25	2.53	1.07+0.659*C_L ns
t_{PLH}	RB TO QB	2.06	3.80	3.96	4.44	1.95+0.674*C_L ns
t_{PLH}	CK TO QB	3.36	6.21	6.47	7.26	3.27+0.602*C_L ns
t_{PHL}		3.04	5.61	5.85	6.56	2.95+0.564*C_L ns
t_r	SB TO Q	0.694	1.28	1.34	1.50	0.526+1.11*C_L ns
t_r	RB TO Q	0.649	1.20	1.25	1.40	0.479+1.13*C_L ns
t_f		0.523	0.965	1.01	1.13	0.373+0.997*C_L ns
t_r	CK TO Q	0.667	1.23	1.28	1.44	0.493+1.15*C_L ns
t_f		0.647	1.20	1.25	1.40	0.506+0.936*C_L ns
t_r	SB TO QB	0.725	1.34	1.40	1.57	0.547+1.19*C_L ns
t_f		0.626	1.16	1.20	1.35	0.478+0.981*C_L ns

Switching characteristics (Sheet 1 of 2)

DFFRSPH

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

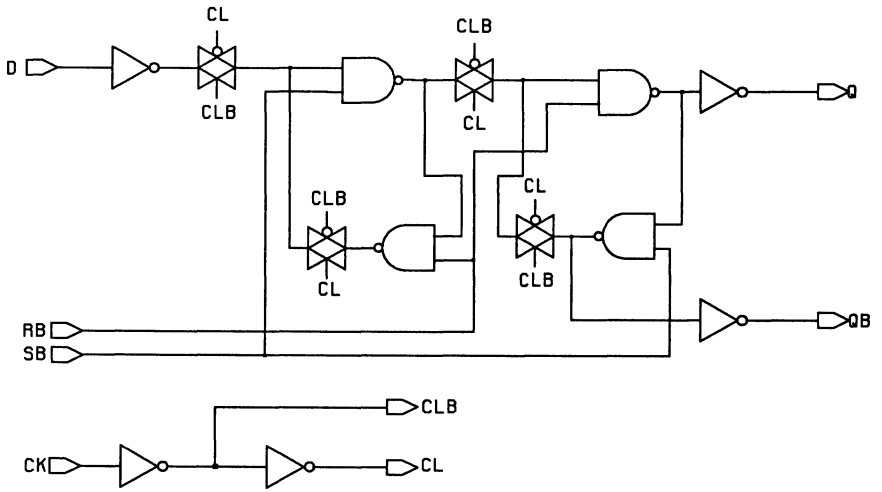
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	RB TO QB	0.750	1.39	1.44	1.62	0.574+1.17*C_L ns
t_r	CK TO QB	0.603	1.11	1.16	1.30	0.429+1.16*C_L ns
t_f		0.563	1.04	1.08	1.22	0.420+0.954*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	2.25	ns
t_h	Hold Time CK to D	−1.00	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	SB Pulse Width (low)	4.50	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	SB Recovery Time	1.00	ns
rt	RB Recovery Time	−2.00	ns

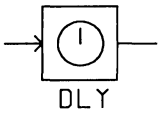
Timing requirements



Functional diagram: DFFRSPH

Delay Cell

Inputs: A
Outputs: X
Input Cap.: A: 0.054 pF
Cell Size: 7 grids wide, 11 grids high



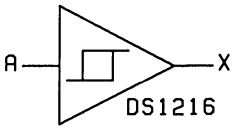
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	4.18	7.72	8.05	9.03	4.05+0.845*C_L ns
t_{PHL}		4.89	9.02	9.41	10.6	4.74+0.971*C_L ns
t_r	A TO X	1.78	3.28	3.42	3.83	1.62+1.04*C_L ns
t_f		2.59	4.78	4.98	5.58	2.43+1.06*C_L ns

Switching characteristics

Schmitt Trigger

DS1216 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.965 pF
Cell Size: 11 grids wide, 11 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.6V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 400mV Min: 100mV

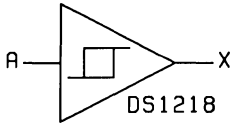
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.902	1.67	1.74	1.95	0.842+0.396*C_L ns
t_{PHL}		3.25	6.00	6.26	7.02	3.12+0.841*C_L ns
t_r	A TO X	0.618	1.14	1.19	1.34	0.489+0.864*C_L ns
t_f		1.37	2.52	2.63	2.95	1.23+0.882*C_L ns

Switching characteristics

Schmitt Trigger

DS1218 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.674 pF
Cell Size: 8 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 600mV Min: 300mV

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

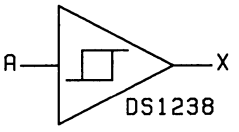
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.982	1.81	1.89	2.12	0.923+0.392*C_L ns
t_{PHL}		3.17	5.86	6.11	6.85	3.04+0.871*C_L ns
t_r	A TO X	0.625	1.16	1.20	1.35	0.493+0.880*C_L ns
t_f		1.38	2.55	2.66	2.99	1.25+0.903*C_L ns

Switching characteristics

DS1238

Schmitt Trigger

DS1238 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.260 pF
Cell Size: 9 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 3.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 2.6V Min: 2.3V

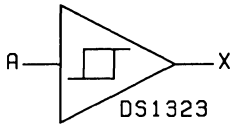
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	4.21	7.78	8.11	9.10	4.09+0.817*C_L ns
t_{PHL}		4.79	8.85	9.22	10.3	4.64+0.970*C_L ns
t_r	A TO X	2.00	3.70	3.86	4.33	1.86+0.978*C_L ns
t_f		2.36	4.36	4.55	5.10	2.21+0.999*C_L ns

Switching characteristics

Schmitt Trigger

DS1323 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.390 pF
Cell Size: 7 grids wide, 12 grids high

DC switching parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.3V ± 300mV
High to Low = 1.3V ± 300mV
Hysteresis: Typ: 1.0V Min: 700mV

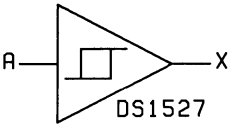
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.39	2.57	2.67	3.00	1.32+0.450*C_L ns
t_{PHL}		2.56	4.72	4.92	5.52	2.44+0.787*C_L ns
t_r	A TO X	0.645	1.19	1.24	1.39	0.509+0.900*C_L ns
t_f		1.22	2.24	2.34	2.62	1.09+0.864*C_L ns

Switching characteristics

Schmitt Trigger

DS1527 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.766 pF
Cell Size: 9 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.7V ± 300mV
High to Low = 1.5V ± 300mV
Hysteresis: Typ: 1.2V Min: 900mV

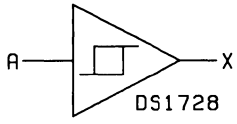
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.85	3.42	3.56	3.99	1.78+0.478*C_L ns
t_{PHL}		2.16	3.99	4.16	4.67	2.06+0.637*C_L ns
t_r	A TO X	1.000	1.85	1.93	2.16	0.859+0.942*C_L ns
t_f		1.10	2.03	2.12	2.38	0.979+0.811*C_L ns

Switching characteristics

Schmitt Trigger

DS1728 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 1.260 pF
Cell Size: 12 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.8V ± 300mV
High to Low = 1.7V ± 300mV
Hysteresis: Typ: 1.1V Min: 800mV

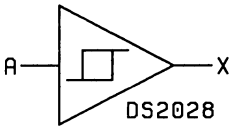
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.90	3.51	3.66	4.10	1.83+0.455*C_L ns
t_{PHL}		1.97	3.63	3.79	4.25	1.88+0.560*C_L ns
t_r	A TO X	1.22	2.25	2.34	2.63	1.08+0.910*C_L ns
t_f		1.08	2.00	2.09	2.34	0.966+0.783*C_L ns

Switching characteristics

Schmitt Trigger

DS2028 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.451 pF
Cell Size: 9 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 2.8V ± 300mV
High to Low = 2.0V ± 300mV
Hysteresis: Typ: 800mV Min: 500mV

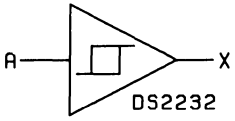
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	2.34	4.32	4.51	5.06	2.26+0.542*C_L ns
t_{PHL}		1.80	3.32	3.46	3.89	1.71+0.576*C_L ns
t_r	A TO X	0.978	1.81	1.88	2.11	0.839+0.930*C_L ns
t_f		0.890	1.64	1.71	1.92	0.775+0.767*C_L ns

Switching characteristics

Schmitt Trigger

DS2232 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.278 pF
Cell Size: 7 grids wide, 12 grids high

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 3.2V ± 300mV
High to Low = 2.2.V ± 300mV
Hysteresis: Typ: 1.0V Min: 700mV

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.89	3.49	3.64	4.08	1.81+0.548*C_L ns
t_{PHL}		1.75	3.22	3.36	3.77	1.66+0.554*C_L ns
t_r	A TO X	0.776	1.43	1.49	1.68	0.641+0.901*C_L ns
t_f		0.869	1.60	1.67	1.88	0.753+0.769*C_L ns

Switching characteristics

EXNOR

2–Input Exclusive NOR

Inputs: A, B
Outputs: X
Input Cap.: A: 0.221
B: 0.220 pF
Cell Size: 11 grids wide, 12 grids high

$X = A \cdot B + \overline{A} \cdot \overline{B}$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.45	2.68	2.79	3.14	1.28+1.14*C_L ns
t_{PHL}		1.47	2.72	2.83	3.18	1.32+0.987*C_L ns
t_r	*IN TO X	1.37	2.53	2.64	2.96	0.994+2.51*C_L ns
t_f		1.28	2.37	2.47	2.77	0.994+1.91*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive NOR

Inputs: A, B
Outputs: X
Input Cap.: A: 0.151
B: 0.149 pF
Cell Size: 6 grids wide, 9 grids high

$X = A \cdot B + \overline{A} \cdot \overline{B}$

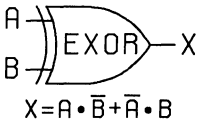
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.11	2.05	2.13	2.39	0.837+1.80*C_L ns
t_{PHL}		1.21	2.24	2.33	2.61	0.995+1.43*C_L ns
t_r	*IN TO X	1.43	2.63	2.75	3.08	0.845+3.87*C_L ns
t_f		1.13	2.09	2.18	2.45	0.713+2.79*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.216
B: 0.217 pF
Cell Size: 11 grids wide, 12 grids high



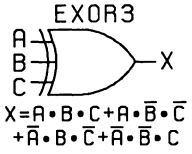
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.44	2.67	2.78	3.12	1.27+1.12*C_L ns
t_{PHL}		1.52	2.80	2.92	3.28	1.37+0.991*C_L ns
t_r	*IN TO X	1.26	2.33	2.42	2.72	0.882+2.51*C_L ns
t_f		1.22	2.26	2.35	2.64	0.934+1.92*C_L ns
* Slowest input						

Switching characteristics

3–Input Exclusive OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.350
B: 0.477
C: 0.347 pF
Cell Size: 16 grids wide, 18 grids high



FUNCTION TABLE

A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.86	3.43	3.57	4.01	1.61+1.65*C_L ns
t_{PHL}		1.61	2.97	3.09	3.47	1.39+1.45*C_L ns
t_r	*IN TO X	2.47	4.56	4.76	5.34	1.93+3.61*C_L ns
t_f		2.32	4.28	4.46	5.00	1.89+2.84*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: All: 0.160 pF
Cell Size: 16 grids wide, 12 grids high

$X = A \cdot \overline{B} + \overline{A} \cdot B$

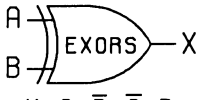
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.53	2.83	2.95	3.31	1.45+0.575*C_L ns
t_{PHL}		1.39	2.57	2.68	3.01	1.30+0.616*C_L ns
t_r	*IN TO X	0.897	1.66	1.73	1.94	0.748+0.991*C_L ns
t_f		0.908	1.68	1.75	1.96	0.783+0.831*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.148
B: 0.140 pF
Cell Size: 6 grids wide, 9 grids high



$X = A \cdot \overline{B} + \overline{A} \cdot B$

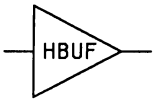
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.14	2.11	2.20	2.47	0.858+1.89*C_L ns
t_{PHL}		1.20	2.21	2.30	2.59	0.993+1.36*C_L ns
t_r	*IN TO X	1.44	2.66	2.77	3.11	0.812+4.17*C_L ns
t_f		1.10	2.03	2.12	2.38	0.717+2.56*C_L ns
* Slowest input						

Switching characteristics

High Drive Noninverting Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 4 grids wide, 11 grids high



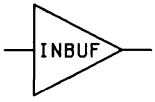
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.06	1.96	2.05	2.30	0.991+0.478*C_L ns
t_{PHL}		1.18	2.17	2.27	2.54	1.10+0.480*C_L ns
t_r	A TO X	0.531	0.980	1.02	1.15	0.401+0.862*C_L ns
t_f		0.554	1.02	1.07	1.20	0.446+0.721*C_L ns

Switching characteristics

Noninverting Input Buffer

INBUF is used to buffer the signal from input and I/O pads, and is compatible with 1.4V ± 300mV threshold voltage (V_{DD} = 5V). INBUF is tested using V_{IL} = 0.8V and V_{IH} = 2.0V.



Inputs: A
Outputs: X
Input Cap.: A: 0.215 pF
Cell Size: 5 grids wide, 12 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

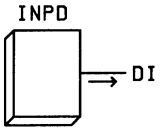
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.558	1.03	1.07	1.20	0.495+0.413*C_L ns
t_{PHL}		1.52	2.81	2.93	3.29	1.44+0.538*C_L ns
t_r	A TO X	0.600	1.11	1.15	1.30	0.488+0.744*C_L ns
t_f		0.985	1.82	1.90	2.13	0.887+0.650*C_L ns

Switching characteristics

INPD

Input Pad

INPD is used with INBUF or one of the Schmitt Triggers. Note that the input buffer and the chip package will add additional capacitance to all inputs.



Inputs: PAD
Outputs: DI
Input Cap.: PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

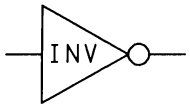
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 2 grids wide, 8 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

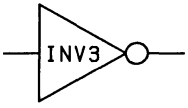
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.584	1.08	1.12	1.26	0.338+1.64*C_L ns
t_{PHL}		0.584	1.08	1.12	1.26	0.351+1.55*C_L ns
t_r	A TO X	0.891	1.65	1.72	1.92	0.348+3.62*C_L ns
t_f		0.758	1.40	1.46	1.64	0.301+3.05*C_L ns

Switching characteristics

INV3

Inverter (3X Drive)

INV3 has 3 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.159 pF
Cell Size: 3 grids wide, 9 grids high

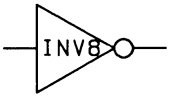
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.362	0.668	0.696	0.781	0.279+0.552*C_L ns
t_{PHL}		0.364	0.672	0.700	0.786	0.284+0.528*C_L ns
t_r	A TO X	0.529	0.977	1.02	1.14	0.363+1.10*C_L ns
t_f		0.467	0.863	0.899	1.01	0.330+0.913*C_L ns

Switching characteristics

Inverting Buffer (8X Drive)

INV8 has 8 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.421 pF
Cell Size: 5 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.263	0.486	0.507	0.569	0.226+0.249*C_L ns
t_{PHL}		0.259	0.478	0.499	0.560	0.222+0.247*C_L ns
t_r	A TO X	0.430	0.794	0.827	0.928	0.374+0.374*C_L ns
t_f		0.398	0.735	0.766	0.859	0.353+0.294*C_L ns

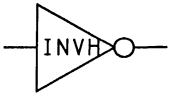
Switching characteristics

INVH

Inverter (High Drive)

INVH has 3 times the drive of an INV.

Inputs: A
Outputs: X
Input Cap.: A: 0.157 pF
Cell Size: 3 grids wide, 10 grids high



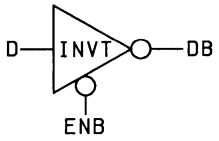
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.371	0.686	0.715	0.802	0.289+0.551*C_L ns
t_{PHL}		0.371	0.685	0.714	0.802	0.292+0.526*C_L ns
t_r	A TO X	0.545	1.01	1.05	1.18	0.379+1.10*C_L ns
t_f		0.473	0.874	0.911	1.02	0.335+0.919*C_L ns

Switching characteristics

Tristate Inverter

INVT inverts the input signal when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: D: 0.106
ENB: 0.126 pF
Output Cap.: DB: 0.138 pF
Cell Size: 5 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

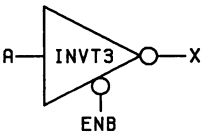
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO DB	0.785	1.45	1.51	1.70	0.546+1.59*C_L ns
t_{PHL}		0.762	1.41	1.47	1.65	0.556+1.37*C_L ns
t_{PLH}	ENB TO DB	0.652	1.20	1.25	1.41	0.415+1.58*C_L ns
t_{PHL}		1.35	2.49	2.59	2.91	1.14+1.38*C_L ns
t_r	D TO DB	1.25	2.31	2.40	2.70	0.714+3.56*C_L ns
t_f		1.09	2.02	2.11	2.36	0.679+2.76*C_L ns
t_r	ENB TO DB	1.19	2.20	2.30	2.58	0.656+3.58*C_L ns
t_f		1.09	2.01	2.09	2.35	0.671+2.77*C_L ns

Switching characteristics

INVT3

Tristate Inverter (3X Drive)

INVT3 is a high drive tristate inverter with 3 times the drive of an INVT and a larger intrinsic delay. INVT3 inverts the input signal when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.055
ENB: 0.053 pF
Output Cap.: X: 0.160 pF
Cell Size: 12 grids wide, 10 grids high

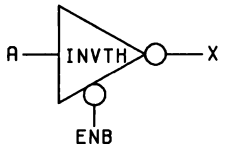
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.61	2.97	3.10	3.47	1.51+0.641*C_L ns
t_{PHL}		1.50	2.76	2.88	3.23	1.40+0.626*C_L ns
t_{PLH}	ENB TO X	1.64	3.02	3.15	3.54	1.54+0.641*C_L ns
t_{PHL}		1.79	3.31	3.45	3.87	1.70+0.625*C_L ns
t_r	A TO X	0.622	1.15	1.20	1.34	0.449+1.15*C_L ns
t_f		0.532	0.982	1.02	1.15	0.383+0.987*C_L ns
t_r	ENB TO X	0.588	1.09	1.13	1.27	0.414+1.16*C_L ns
t_f		0.504	0.931	0.970	1.09	0.354+0.998*C_L ns

Switching characteristics

Tristate Inverter (High Drive)

INVTH is a high drive tristate inverter with 2 times the drive of an INVT and a smaller intrinsic delay. The input signal is inverted when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.158
ENB: 0.057 pF
Output Cap.: X: 0.158 pF
Cell Size: 9 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

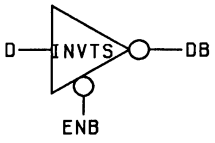
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.550	1.02	1.06	1.19	0.391+1.05*C_L ns
t_{PHL}		0.533	0.985	1.03	1.15	0.397+0.905*C_L ns
t_{PLH}	ENB TO X	0.823	1.52	1.58	1.78	0.661+1.08*C_L ns
t_{PHL}		0.834	1.54	1.60	1.80	0.684+0.995*C_L ns
t_r	A TO X	0.862	1.59	1.66	1.86	0.512+2.33*C_L ns
t_f		0.658	1.22	1.27	1.42	0.387+1.80*C_L ns
t_r	ENB TO X	0.862	1.59	1.66	1.86	0.510+2.34*C_L ns
t_f		0.628	1.16	1.21	1.36	0.355+1.82*C_L ns

Switching characteristics

INVTS

Tristate Inverter

INVTS inverts the input signal when ENB is low. When ENB is high the output is in a Hi-Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: D: 0.096
ENB: 0.122 pF
Output Cap.: DB: 0.129 pF
Cell Size: 4 grids wide, 10 grids high

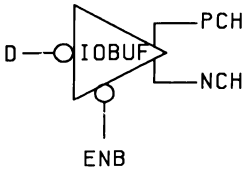
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO DB	0.730	1.35	1.40	1.58	0.476+1.69*C_L ns
t_{PHL}		0.605	1.12	1.16	1.31	0.412+1.28*C_L ns
t_{PLH}	ENB TO DB	0.599	1.11	1.15	1.29	0.320+1.86*C_L ns
t_{PHL}		0.770	1.42	1.48	1.66	0.566+1.36*C_L ns
t_r	D TO DB	1.20	2.22	2.31	2.59	0.651+3.66*C_L ns
t_f		0.902	1.67	1.74	1.95	0.522+2.53*C_L ns
t_r	ENB TO DB	1.15	2.11	2.20	2.47	0.590+3.70*C_L ns
t_f		0.931	1.72	1.79	2.01	0.554+2.51*C_L ns

Switching characteristics

Input/Output Buffer

IOBUF is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 14 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

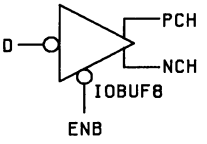
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.55	4.70	4.90	5.50	2.47+0.483*C_L ns
t_{PHL}		1.50	2.78	2.90	3.25	1.43+0.478*C_L ns
t_{PLH}	D TO PCH	1.94	3.59	3.74	4.19	1.87+0.471*C_L ns
t_{PHL}		1.88	3.47	3.62	4.06	1.81+0.484*C_L ns
t_{PLH}	ENB TO NCH	2.32	4.29	4.47	5.02	2.25+0.475*C_L ns
t_{PHL}		1.34	2.47	2.57	2.89	1.26+0.478*C_L ns
t_{PLH}	ENB TO PCH	1.90	3.52	3.67	4.11	1.83+0.470*C_L ns
t_{PHL}		2.02	3.72	3.88	4.35	1.94+0.471*C_L ns
t_r	D TO NCH	0.624	1.15	1.20	1.35	0.499+0.826*C_L ns
t_f		0.594	1.10	1.14	1.28	0.490+0.693*C_L ns
t_r	D TO PCH	0.593	1.10	1.14	1.28	0.468+0.834*C_L ns
t_f		0.579	1.07	1.11	1.25	0.473+0.705*C_L ns
t_r	ENB TO NCH	0.611	1.13	1.18	1.32	0.486+0.832*C_L ns
t_f		0.571	1.05	1.10	1.23	0.466+0.702*C_L ns
t_r	ENB TO PCH	0.532	0.983	1.03	1.15	0.404+0.855*C_L ns
t_f		0.592	1.09	1.14	1.28	0.488+0.694*C_L ns

Switching characteristics

IOBUF8

Input/Output Buffer (8X Drive)

IOBUF8 is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 18 grids wide, 11 grids high

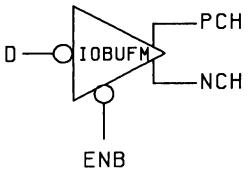
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.94	5.44	5.67	6.36	2.90+0.274*C_L ns
t_{PHL}		1.56	2.88	3.01	3.37	1.52+0.259*C_L ns
t_{PLH}	D TO PCH	2.10	3.88	4.04	4.54	2.06+0.270*C_L ns
t_{PHL}		2.04	3.78	3.94	4.42	2.00+0.298*C_L ns
t_{PLH}	ENB TO NCH	2.55	4.71	4.91	5.51	2.51+0.276*C_L ns
t_{PHL}		1.38	2.55	2.66	2.98	1.34+0.272*C_L ns
t_{PLH}	ENB TO PCH	1.99	3.68	3.83	4.30	1.95+0.278*C_L ns
t_{PHL}		2.11	3.90	4.07	4.56	2.07+0.274*C_L ns
t_r	D TO NCH	0.609	1.12	1.17	1.32	0.549+0.395*C_L ns
t_f		0.568	1.05	1.09	1.23	0.520+0.322*C_L ns
t_r	D TO PCH	0.535	0.989	1.03	1.16	0.474+0.410*C_L ns
t_f		0.530	0.978	1.02	1.14	0.478+0.346*C_L ns
t_r	ENB TO NCH	0.598	1.10	1.15	1.29	0.539+0.392*C_L ns
t_f		0.533	0.984	1.03	1.15	0.482+0.339*C_L ns
t_r	ENB TO PCH	0.499	0.922	0.962	1.08	0.439+0.405*C_L ns
t_f		0.543	1.000	1.05	1.17	0.491+0.345*C_L ns

Switching characteristics

Input/Output Buffer (Medium Drive)

IOBUFM is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 14 grids wide, 11 grids high

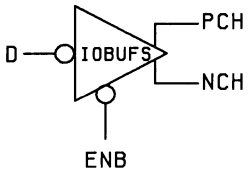
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.57	4.75	4.95	5.55	2.44+0.847*C_L ns
t_{PHL}		1.25	2.30	2.40	2.70	1.17+0.487*C_L ns
t_{PLH}	D TO PCH	1.98	3.66	3.81	4.28	1.85+0.850*C_L ns
t_{PHL}		1.67	3.08	3.21	3.60	1.59+0.480*C_L ns
t_{PLH}	ENB TO NCH	2.32	4.28	4.46	5.01	2.19+0.835*C_L ns
t_{PHL}		1.10	2.03	2.12	2.37	1.03+0.480*C_L ns
t_{PLH}	ENB TO PCH	1.98	3.65	3.81	4.27	1.85+0.845*C_L ns
t_{PHL}		1.81	3.35	3.49	3.92	1.74+0.468*C_L ns
t_r	D TO NCH	0.694	1.28	1.34	1.50	0.432+1.75*C_L ns
t_f		0.503	0.928	0.968	1.09	0.397+0.702*C_L ns
t_r	D TO PCH	0.677	1.25	1.30	1.46	0.413+1.76*C_L ns
t_f		0.498	0.919	0.958	1.08	0.393+0.697*C_L ns
t_r	ENB TO NCH	0.708	1.31	1.36	1.53	0.448+1.74*C_L ns
t_f		0.470	0.868	0.905	1.01	0.363+0.713*C_L ns
t_r	ENB TO PCH	0.654	1.21	1.26	1.41	0.390+1.76*C_L ns
t_f		0.503	0.928	0.968	1.09	0.399+0.690*C_L ns

Switching characteristics

Input/Output Buffer (Small Drive)

IOBUFS is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: ENB: 0.113
D: 0.072 pF
Cell Size: 14 grids wide, 11 grids high

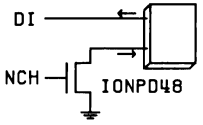
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.71	5.00	5.21	5.85	2.46+1.65*C_L ns
t_{PHL}		1.12	2.07	2.16	2.42	1.05+0.476*C_L ns
t_{PLH}	D TO PCH	2.11	3.89	4.05	4.55	1.85+1.67*C_L ns
t_{PHL}		1.54	2.84	2.97	3.33	1.47+0.467*C_L ns
t_{PLH}	ENB TO NCH	2.47	4.55	4.75	5.33	2.22+1.65*C_L ns
t_{PHL}		0.990	1.83	1.91	2.14	0.920+0.466*C_L ns
t_{PLH}	ENB TO PCH	2.12	3.91	4.08	4.57	1.87+1.65*C_L ns
t_{PHL}		1.67	3.08	3.21	3.60	1.60+0.467*C_L ns
t_r	D TO NCH	0.993	1.83	1.91	2.14	0.452+3.60*C_L ns
t_f		0.464	0.857	0.893	1.000	0.359+0.695*C_L ns
t_r	D TO PCH	0.957	1.77	1.84	2.07	0.413+3.62*C_L ns
t_f		0.463	0.856	0.892	1.000	0.360+0.686*C_L ns
t_r	ENB TO NCH	0.981	1.81	1.89	2.12	0.440+3.61*C_L ns
t_f		0.415	0.767	0.799	0.897	0.307+0.717*C_L ns
t_r	ENB TO PCH	0.947	1.75	1.82	2.05	0.403+3.63*C_L ns
t_f		0.456	0.841	0.877	0.984	0.351+0.694*C_L ns

Switching characteristics

48mA Open Drain Input/Output Pad

IONPD48 is used to form a bidirectional pad that can drive output data, or be put in a Hi-Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD, DI
Input Cap.: NCH: 12.520
PAD: 10.600 pF
Cell Size: 51 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	134	248	258	289	31.3+2.05*C_L ns
t_{PHL}		0.573	1.06	1.10	1.24	0.343+0.005*C_L ns

Switching characteristics

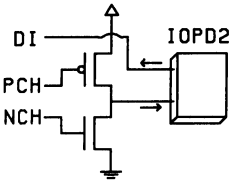
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

2mA Input/Output Pad

IOPD2 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 0.529
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	5.86	10.8	11.3	12.6	0.767+0.102*C_L ns
t_{PHL}		6.55	12.1	12.6	14.1	0.742+0.116*C_L ns
* NCH or PCH						

Switching characteristics

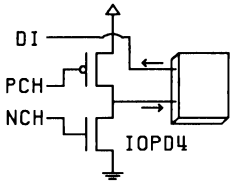
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Input/Output Pad

IOPD4 is used to form a bidirectional pad that can drive output data, or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 1.059
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	3.07	5.66	5.90	6.62	0.536+0.051*C_L ns
t_{PHL}		3.39	6.27	6.54	7.33	0.491+0.058*C_L ns
* NCH or PCH						

Switching characteristics

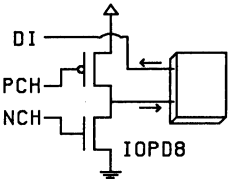
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}–0.5V	–2.00	mA

DC specifications

8mA Input/Output Pad

IOPD8 is used to form a bidirectional pad that can drive data or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 2.120
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.68	3.11	3.24	3.64	0.419+0.025*C_L ns
t_{PHL}		1.84	3.40	3.54	3.98	0.374+0.029*C_L ns
* NCH or PCH						

Switching characteristics

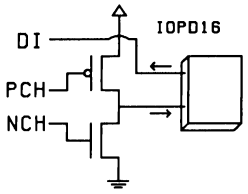
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}–0.5V	–4.00	mA

DC specifications

16mA Input/Output Pad

IOPD16 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH, PCH: 4.240
PAD: 6.900 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.988	1.82	1.90	2.13	0.355+0.013*C_L ns
t_{PHL}		1.06	1.96	2.04	2.29	0.340+0.014*C_L ns
* NCH or PCH						

Switching characteristics

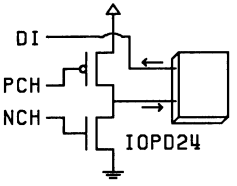
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Input/Output Pad

IOPD24 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes, Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 6.360
PCH: 5.290
PAD: 9.200 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.891	1.65	1.71	1.92	0.373+0.010*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.309+0.010*C_L ns
* NCH or PCH						

Switching characteristics

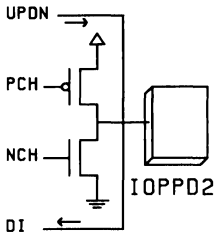
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}-0.5V	-12.00	mA

DC specifications

2mA Input/Output Pad with Pullup/Pulldown Port

IOPPD2 is similar to IOPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 0.529
UPDN: 52.000
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	5.88	10.9	11.3	12.7	0.792+0.102*C_L ns
t_{PHL}		6.58	12.2	12.7	14.2	0.774+0.116*C_L ns
* NCH or PCH						

Switching characteistics

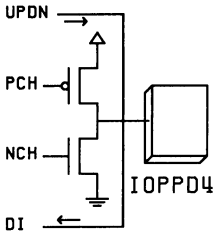
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Input/Output Pad with Pullup/Pulldown Port

IOPPD4 is similar to IOPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 1.059
UPDN: 52.000
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	3.08	5.69	5.93	6.65	0.549+0.051*C_L ns
t_{PHL}		3.41	6.30	6.57	7.37	0.508+0.058*C_L ns
* NCH or PCH						

Switching characteristics

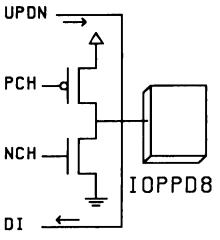
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Input/Output Pad with Pullup/Pulldown Port

IOPPD8 is similar to IOPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 2.120
UPDN: 52.000
PAD: 5.500 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	1.69	3.12	3.25	3.65	0.425+0.025*C_L ns
t_{PHL}		1.85	3.42	3.56	4.00	0.383+0.029*C_L ns
* NCH or PCH						

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

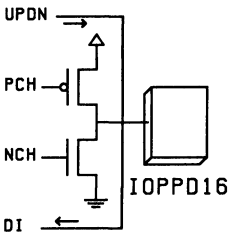
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC specifications

IOPPD16

16mA Input/Output Pad with Pullup/Pulldown Port

IOPPD16 is similar to IOPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH, PCH: 4.240
UPDN: 52.000
PAD: 6.900 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	0.991	1.83	1.91	2.14	0.358+0.013*C_L ns
t_{PHL}		1.06	1.96	2.04	2.29	0.343+0.014*C_L ns
* NCH or PCH						

Switching characteristics

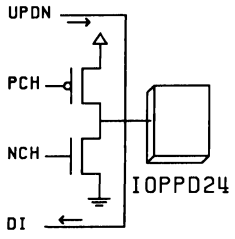
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Input/Output Pad with Pullup/Pulldown Port

IOPPD24 is similar to IOPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 6.360
PCH: 5.300
UPDN: 52.000
PAD: 9.200 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.23	5.96	6.21	6.97	0.523+0.054*C_L ns
t_{PHL}		9.33	17.2	18.0	20.1	0.816+0.170*C_L ns
t_{PLH}	*IN TO PAD	0.893	1.65	1.72	1.93	0.375+0.010*C_L ns
t_{PHL}		0.802	1.48	1.54	1.73	0.313+0.010*C_L ns
* NCH or PCH						

Switching characteristics

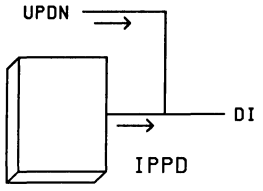
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

Input Pad with Pullup/Pulldown Port

IPPD is similar to INPD but includes an input port, UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See any PPU/PPD data sheet for pullup/pulldown current information.



Inputs: PAD, UPDN
Outputs: DI
Input Cap.: PAD: 5.500
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

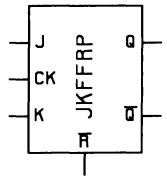
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO DI	3.17	5.86	6.10	6.85	3.14+0.204*C_L ns
t_{PHL}		9.08	16.8	17.5	19.6	9.02+0.323*C_L ns
t_{PLH}	PAD TO DI	0.021	0.039	0.041	0.046	0.003+0.123*C_L ns
t_{PHL}		0.023	0.042	0.044	0.049	0.000+0.152*C_L ns
t_r	PAD TO DI	0.804	1.48	1.55	1.74	0.790+0.093*C_L ns
t_f		0.815	1.50	1.57	1.76	0.801+0.091*C_L ns

Switching characteristics

J–K Flip–Flop with Reset, Positive Edge Triggered

JKFFRP is a fully static JK-type edge triggered flip–flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.



Inputs: J, CK, K, RB
Outputs: Q, QB
Input Cap.: J: 0.055
CK: 0.189
K: 0.055
RB: 0.171 pF
Cell Size: 21 grids wide, 11 grids high

FUNCTION TABLE

J	K	CK	RB	Q	QB
H	H	↑	H	QB_o	Q_o
H	L	↑	H	H	L
L	H	↑	H	L	H
L	L	↑	H	Q_o	QB_o
X	X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.06	1.96	2.05	2.30	0.960+0.682*C_L ns
t_{PHL}		1.26	2.33	2.43	2.73	1.08+1.20*C_L ns
t_{PLH}	CK TO QB	1.96	3.62	3.77	4.23	1.79+1.09*C_L ns
t_{PHL}		2.07	3.82	3.98	4.47	1.98+0.577*C_L ns
t_{PHL}	RB TO Q	3.95	7.29	7.60	8.52	3.74+1.33*C_L ns
t_{PLH}	RB TO QB	1.48	2.73	2.85	3.20	1.31+1.11*C_L ns
t_r	CK TO Q	0.939	1.73	1.81	2.03	0.618+2.13*C_L ns
t_f		0.843	1.56	1.62	1.82	0.571+1.81*C_L ns
t_r	CK TO QB	0.747	1.38	1.44	1.61	0.410+2.25*C_L ns
t_f		0.827	1.53	1.59	1.79	0.593+1.56*C_L ns
t_f	RB TO Q	1.23	2.28	2.38	2.67	0.966+1.79*C_L ns
t_r	RB TO QB	0.708	1.31	1.36	1.53	0.367+2.28*C_L ns

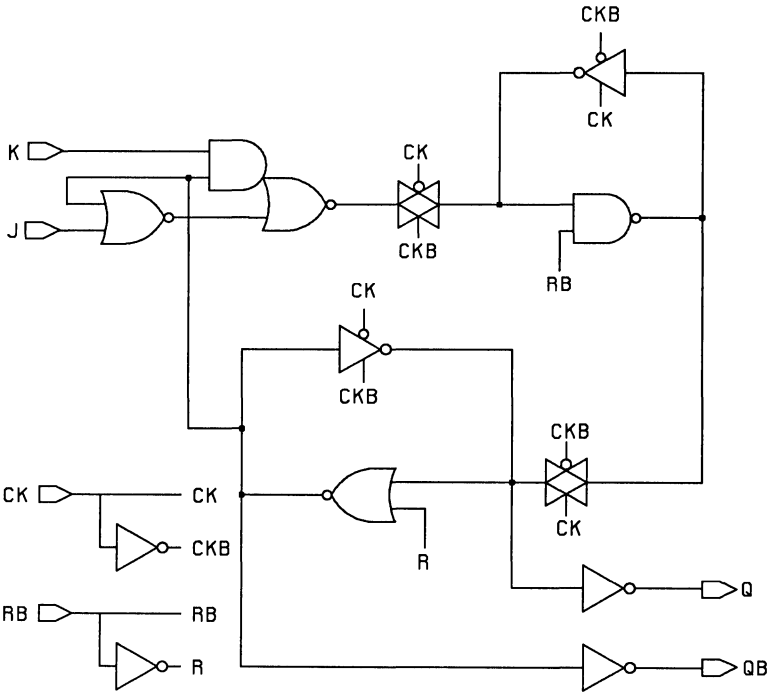
Switching characteristics

JKFFRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	4.00	ns
t_{su}	Setup Time K to CK	3.00	ns
t_h	Hold Time CK to J	−2.75	ns
t_h	Hold Time CK to K	−2.25	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	Low CK Pulse Width	4.00	ns
t_{pwl}	RB Pulse Width (low)	5.00	ns
rt	RB Recovery Time	0.00	ns

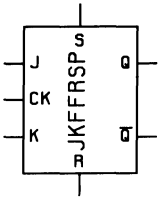
Timing requirements



Functional diagram: JKFFRP

J–K Flip–Flop with Reset and Set, Positive Edge Triggered

JKFFRSP is a fully static JK-type edge triggered flip-flop. It is positive edge triggered with respect to CK. S and R are asynchronous and active high. For a faster version of this cell, see JKFFRSPF.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK, J, K: 0.055
S: 0.118
R: 0.110 pF
Cell Size: 28 grids wide, 12 grids high

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB_o	Q_o
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q_o	QB_o
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

*Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	4.51	8.33	8.68	9.74	4.39+0.812*C_L ns
t_{PHL}		4.60	8.50	8.86	9.95	4.46+0.967*C_L ns
t_{PLH}	CK TO QB	3.22	5.95	6.21	6.96	3.09+0.895*C_L ns
t_{PHL}		3.43	6.33	6.60	7.40	3.27+1.05*C_L ns
t_{PLH}	S TO Q	1.35	2.50	2.60	2.92	1.21+0.944*C_L ns
t_{PHL}		2.32	4.29	4.47	5.01	2.16+1.07*C_L ns
t_{PHL}	S TO QB	3.36	6.20	6.46	7.25	3.20+1.01*C_L ns
t_{PHL}	R TO Q	3.23	5.97	6.22	6.98	3.07+1.06*C_L ns
t_{PLH}	R TO QB	1.28	2.37	2.47	2.77	1.15+0.882*C_L ns
t_{PHL}		2.02	3.73	3.89	4.36	1.87+1.01*C_L ns
t_r	CK TO Q	0.825	1.52	1.59	1.78	0.570+1.70*C_L ns
t_f		0.902	1.67	1.74	1.95	0.678+1.49*C_L ns
t_r	CK TO QB	0.907	1.67	1.75	1.96	0.655+1.68*C_L ns
t_f		1.05	1.93	2.02	2.26	0.826+1.47*C_L ns
t_r	S TO Q	0.844	1.56	1.63	1.82	0.583+1.74*C_L ns

Switching characteristics (Sheet 1 of 2)

JKFFRSP

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

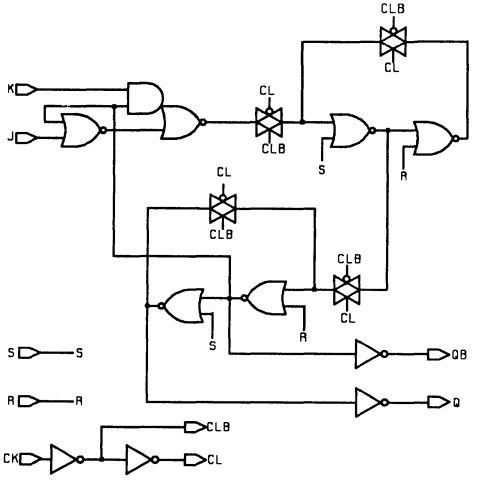
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.13	2.09	2.18	2.45	0.903+1.53*C_L ns
t_f	S TO QB	1.08	1.99	2.07	2.32	0.852+1.49*C_L ns
t_f	R TO Q	1.14	2.10	2.19	2.45	0.906+1.53*C_L ns
t_r	R TO QB	0.752	1.39	1.45	1.62	0.490+1.74*C_L ns
t_f		1.02	1.89	1.97	2.21	0.799+1.48*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	3.75	ns
t_{su}	Setup Time K to CK	3.75	ns
t_h	Hold Time CK to J	-2.00	ns
t_h	Hold Time CK to K	-2.00	ns
t_{pwh}	High CK Pulse Width	6.00	ns
t_{pwh}	Set Pulse Width (high)	5.00	ns
t_{pwh}	Reset Pulse Width (high)	4.75	ns
t_{pwl}	Low CK Pulse Width	4.75	ns
rt	Set Recovery Time	0.25	ns
rt	Reset Recovery Time	-2.25	ns

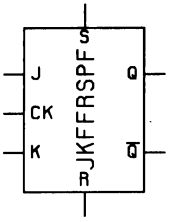
Timing requirements



Functional diagram: JKFFRSP

Fast J–K Flip–Flop with Reset and Set, Positive Edge Triggered

JKFFRSPF is a fully static JK–type edge triggered flip–flop. It is positive edge triggered with respect to CK. S and R are asynchronous and active high.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK: 0.106
J: 0.107
K: 0.140
S: 0.107
R: 0.106 pF
Cell Size: 32 grids wide, 12 grids high

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB*	Q*
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q*	QB*
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

* Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	1.84	3.41	3.55	3.99	1.71+0.880*C_L ns
t_{PHL}		1.67	3.08	3.21	3.60	1.55+0.753*C_L ns
t_{PLH}	CK TO QB	2.04	3.77	3.93	4.41	1.90+0.930*C_L ns
t_{PHL}		1.98	3.67	3.82	4.29	1.86+0.842*C_L ns
t_{PLH}	S TO Q	1.37	2.53	2.64	2.96	1.23+0.892*C_L ns
t_{PHL}		1.14	2.10	2.19	2.46	1.01+0.808*C_L ns
t_{PHL}	S TO QB	3.34	6.17	6.44	7.22	3.02+2.17*C_L ns
t_{PHL}	R TO Q	2.83	5.23	5.45	6.12	2.52+2.07*C_L ns
t_{PLH}	R TO QB	1.32	2.43	2.54	2.84	1.19+0.867*C_L ns
t_{PHL}		1.10	2.03	2.12	2.38	0.984+0.777*C_L ns
t_r	CK TO Q	0.865	1.60	1.67	1.87	0.593+1.81*C_L ns
t_f		0.792	1.46	1.52	1.71	0.586+1.37*C_L ns
t_r	CK TO QB	0.936	1.73	1.80	2.02	0.665+1.80*C_L ns
t_f		0.919	1.70	1.77	1.99	0.711+1.38*C_L ns
t_r	S TO Q	1.73	3.19	3.32	3.73	1.44+1.90*C_L ns

Switching characteristics (Sheet 1 of 2)

JKFFRSPF

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

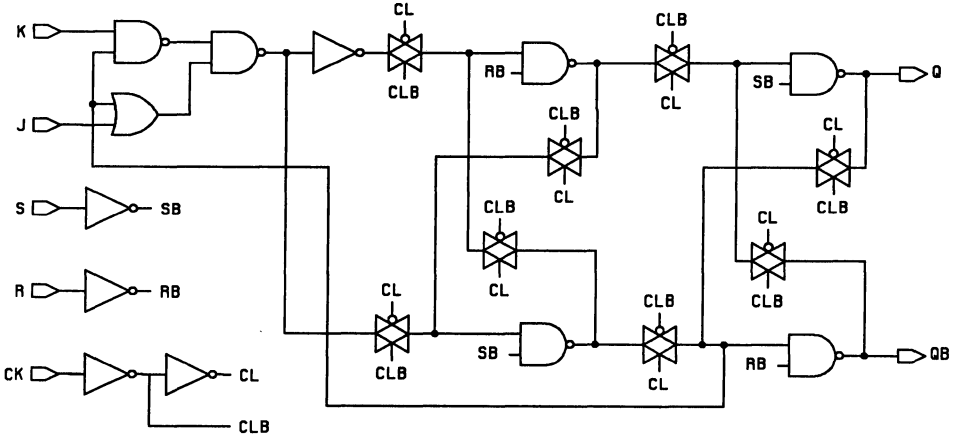
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.59	2.94	3.07	3.44	1.39+1.37*C_L ns
t_f	S TO QB	1.94	3.58	3.73	4.19	1.69+1.67*C_L ns
t_f	R TO Q	2.07	3.82	3.99	4.47	1.83+1.62*C_L ns
t_r	R TO QB	1.44	2.66	2.77	3.11	1.16+1.87*C_L ns
t_f		1.17	2.16	2.25	2.53	0.960+1.40*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	3.25	ns
t_{su}	Setup Time K to CK	3.25	ns
t_h	Hold Time CK to J	−2.25	ns
t_h	Hold Time CK to K	−2.25	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwh}	Set Pulse Width (high)	6.50	ns
t_{pwh}	Reset Pulse Width (high)	6.00	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	Set Recovery Time	−1.75	ns
rt	Reset Recovery Time	−1.75	ns

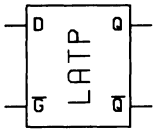
Timing requirements



Functional diagram: JKFFRSPF

Transparent Latch, Positive Edge Triggered

LATP holds data when GB is high and is transparent when GB is low. For a faster version of this cell, see LATPF.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: D: 0.038
GB: 0.055 pF
Cell Size: 12 grids wide, 11 grids high

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	2.50	4.61	4.81	5.39	2.37+0.818*C_L ns
t_{PHL}		3.17	5.85	6.10	6.84	3.04+0.815*C_L ns
t_{PLH}	D TO QB	2.53	4.67	4.87	5.46	2.40+0.875*C_L ns
t_{PHL}		1.91	3.52	3.67	4.12	1.78+0.850*C_L ns
t_{PLH}	GB TO Q	2.90	5.36	5.59	6.27	2.78+0.828*C_L ns
t_{PHL}		3.55	6.55	6.83	7.66	3.42+0.803*C_L ns
t_{PLH}	GB TO QB	2.90	5.35	5.58	6.26	2.76+0.870*C_L ns
t_{PHL}		2.31	4.27	4.45	4.99	2.18+0.856*C_L ns
t_r	D TO Q	0.681	1.26	1.31	1.47	0.418+1.75*C_L ns
t_f		0.629	1.16	1.21	1.36	0.410+1.46*C_L ns
t_r	D TO QB	0.771	1.42	1.48	1.67	0.511+1.73*C_L ns
t_f		0.700	1.29	1.35	1.51	0.483+1.44*C_L ns
t_r	GB TO Q	0.693	1.28	1.33	1.50	0.430+1.75*C_L ns
t_f		0.622	1.15	1.20	1.34	0.402+1.47*C_L ns
t_r	GB TO QB	0.766	1.41	1.47	1.65	0.505+1.73*C_L ns
t_f		0.686	1.27	1.32	1.48	0.468+1.45*C_L ns

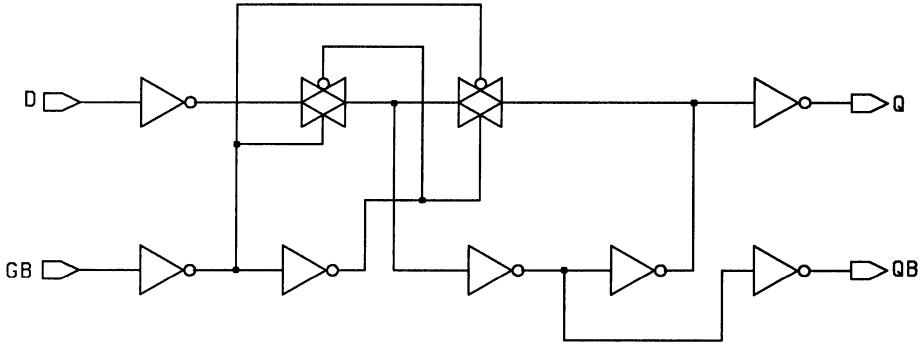
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.25	ns
t_h	Hold Time GB to D	−1.00	ns
t_{pwl}	GB Pulse Width (low)	5.00	ns

Timing requirements

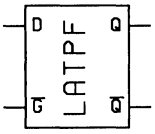
LATP



Functional diagram: LATP

Fast Transparent Latch, Positive Edge Triggered

LATPF holds data when GB is high and is transparent when GB is low.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: D: 0.123
GB: 0.228 pF
Cell Size: 10 grids wide, 12 grids high

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q₀	QB₀

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.01	1.86	1.94	2.18	0.879+0.866*C_L ns
t_{PHL}		1.43	2.65	2.76	3.09	1.30+0.910*C_L ns
t_{PLH}	D TO QB	2.00	3.69	3.84	4.31	1.87+0.807*C_L ns
t_{PHL}		1.58	2.92	3.04	3.41	1.46+0.790*C_L ns
t_{PLH}	GB TO Q	1.39	2.56	2.67	2.99	1.25+0.875*C_L ns
t_{PHL}		1.53	2.82	2.94	3.30	1.39+0.911*C_L ns
t_{PLH}	GB TO QB	2.09	3.86	4.03	4.52	1.97+0.811*C_L ns
t_{PHL}		1.95	3.60	3.75	4.21	1.83+0.801*C_L ns
t_r	D TO Q	0.688	1.27	1.32	1.49	0.422+1.77*C_L ns
t_f		0.787	1.45	1.51	1.70	0.571+1.44*C_L ns
t_r	D TO QB	0.696	1.29	1.34	1.50	0.436+1.73*C_L ns
t_f		0.599	1.11	1.15	1.29	0.381+1.45*C_L ns
t_r	GB TO Q	0.700	1.29	1.35	1.51	0.436+1.76*C_L ns
t_f		0.802	1.48	1.54	1.73	0.587+1.43*C_L ns
t_r	GB TO QB	0.696	1.29	1.34	1.50	0.436+1.73*C_L ns
t_f		0.600	1.11	1.15	1.30	0.382+1.45*C_L ns

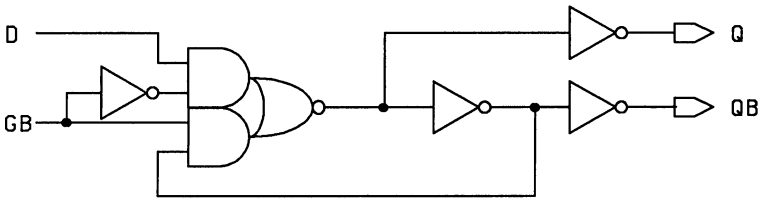
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.50	ns
t_h	Hold Time GB to D	−0.75	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns

Timing requirements

LATPF

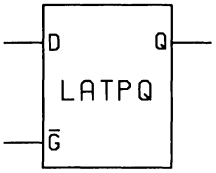


Functional diagram: LATPF

Transparent Latch, Positive Edge Triggered

LATPQ holds data when GB is high and is transparent when GB is low.

Inputs: D, GB
Outputs: Q
Input Cap.: D: 0.062
GB: 0.125 pF
Cell Size: 6 grids wide, 9.5 grids high



FUNCTION TABLE

D	GB	Q
L	L	L
H	L	H
X	H	Q_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.15	2.12	2.21	2.47	1.000+0.959*C_L ns
t_{PHL}		1.37	2.53	2.64	2.96	1.30+0.441*C_L ns
t_{PLH}	GB TO Q	1.38	2.55	2.66	2.98	1.24+0.959*C_L ns
t_{PHL}		1.24	2.30	2.39	2.69	1.09+0.987*C_L ns
t_r	D TO Q	0.752	1.39	1.45	1.63	0.464+1.92*C_L ns
t_f		0.730	1.35	1.41	1.58	0.511+1.46*C_L ns
t_r	GB TO Q	0.762	1.41	1.47	1.64	0.474+1.92*C_L ns
t_f		0.720	1.33	1.39	1.55	0.479+1.60*C_L ns

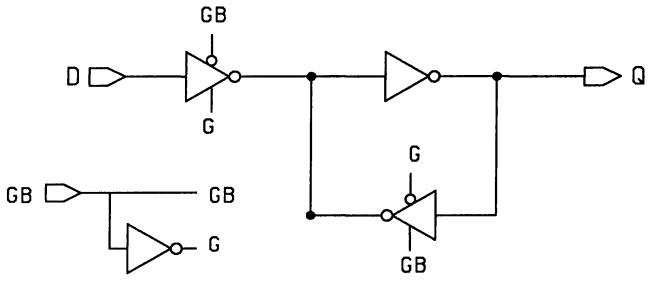
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.00	ns
t_h	Hold Time GB to D	−1.00	ns
t_{pwl}	GB Pulse Width (low)	4.00	ns

Timing requirements

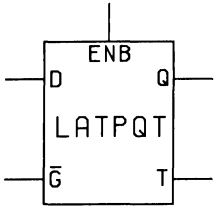
LATPQ



Functional diagram: LATPQ

Transparent Latch with Tristate, Positive Edge Triggered

LATPQT holds data when GB is high and is transparent when GB is low. When ENB is high, the T output is in a Hi−Z state and Q functions as a normal latch using any of the given states defined for Q in the FUNCTION TABLE.



Inputs: ENB, D, GB
Outputs: Q, T
Input Cap.: ENB: 0.121
D: 0.063
GB: 0.126 pF
Output Cap.: Q: 0.000
T: 0.131 pF
Cell Size: 9 grids wide, 10 grids high

FUNCTION TABLE

D	GB	ENB	Q	T
L	L	L	L	L
H	L	L	H	H
X	H	L	Q_o	T_o
L	L	H	L	HiZ
H	L	H	H	HiZ
X	H	H	Q_o	HiZ

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.45	2.68	2.79	3.13	1.29+1.04*C_L ns
t_{PHL}		1.71	3.15	3.28	3.69	1.57+0.897*C_L ns
t_{PLH}	D TO T	1.65	3.04	3.17	3.56	1.40+1.62*C_L ns
t_{PHL}		1.78	3.29	3.43	3.85	1.61+1.17*C_L ns
t_{PLH}	GB TO Q	1.73	3.20	3.34	3.74	1.58+1.04*C_L ns
t_{PHL}		1.74	3.21	3.34	3.75	1.58+1.05*C_L ns
t_{PLH}	GB TO T	1.92	3.54	3.69	4.14	1.67+1.62*C_L ns
t_{PHL}		1.66	3.06	3.19	3.58	1.46+1.33*C_L ns
t_{PLH}	ENB TO T	0.590	1.09	1.14	1.27	0.320+1.80*C_L ns
t_{PHL}		0.853	1.58	1.64	1.84	0.643+1.40*C_L ns
t_r	D TO Q	0.920	1.70	1.77	1.99	0.620+1.99*C_L ns
t_f		0.905	1.67	1.74	1.95	0.665+1.59*C_L ns
t_r	D TO T	1.30	2.41	2.51	2.82	0.784+3.46*C_L ns
t_f		1.16	2.14	2.23	2.50	0.785+2.47*C_L ns
t_r	GB TO Q	0.926	1.71	1.78	2.00	0.625+2.00*C_L ns
t_f		0.911	1.68	1.75	1.97	0.671+1.59*C_L ns
t_r	GB TO T	1.31	2.42	2.52	2.83	0.788+3.46*C_L ns
t_f		1.16	2.14	2.23	2.50	0.786+2.47*C_L ns
t_r	ENB TO T	1.14	2.10	2.19	2.46	0.606+3.55*C_L ns
t_f		0.991	1.83	1.91	2.14	0.613+2.52*C_L ns

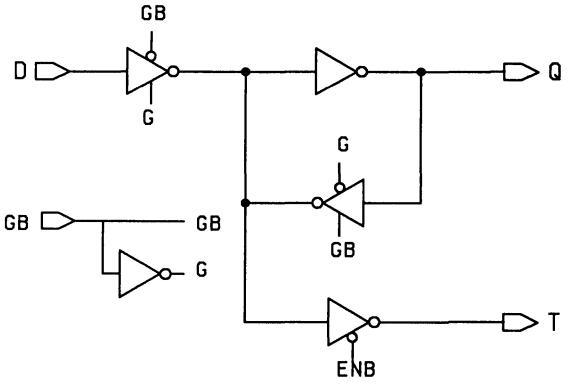
Switching characteristics

LATPQT

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−1.25	ns
t_{pwl}	GB Pulse Width (low)	4.75	ns

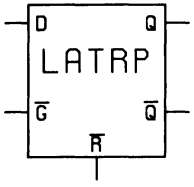
Timing requirements



Functional diagram: LATPQT

Transparent Latch with Reset, Positive Edge Triggered

LATRP holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. For a faster version of this cell, see LATRPF.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.055
D: 0.038
GB: 0.055 pF
Cell Size: 14 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	3.13	5.79	6.03	6.77	3.01+0.811*C_L ns
t_{PHL}		3.29	6.08	6.34	7.12	3.16+0.851*C_L ns
t_{PLH}	D TO QB	2.18	4.03	4.20	4.71	2.06+0.825*C_L ns
t_{PHL}		2.58	4.76	4.96	5.57	2.43+0.980*C_L ns
t_{PLH}	GB TO Q	3.53	6.53	6.80	7.63	3.41+0.794*C_L ns
t_{PHL}		3.62	6.69	6.97	7.82	3.49+0.873*C_L ns
t_{PLH}	GB TO QB	2.51	4.64	4.84	5.42	2.38+0.838*C_L ns
t_{PHL}		2.98	5.50	5.74	6.44	2.83+0.963*C_L ns
t_{PLH}	RB TO Q	2.85	5.27	5.50	6.17	2.73+0.810*C_L ns
t_{PHL}		3.14	5.79	6.04	6.77	2.99+0.972*C_L ns
t_{PLH}	RB TO QB	1.33	2.45	2.55	2.87	1.20+0.829*C_L ns
t_{PHL}		2.30	4.24	4.42	4.96	2.15+0.980*C_L ns
t_r	D TO Q	0.741	1.37	1.43	1.60	0.483+1.72*C_L ns
t_f		0.810	1.50	1.56	1.75	0.594+1.44*C_L ns
t_r	D TO QB	0.698	1.29	1.34	1.51	0.438+1.73*C_L ns
t_f		0.903	1.67	1.74	1.95	0.678+1.49*C_L ns
t_r	GB TO Q	0.756	1.40	1.46	1.63	0.500+1.70*C_L ns
t_f		0.804	1.48	1.55	1.74	0.587+1.44*C_L ns
t_r	GB TO QB	0.679	1.25	1.31	1.47	0.417+1.75*C_L ns
t_f		0.927	1.71	1.79	2.00	0.706+1.47*C_L ns
t_r	RB TO Q	0.737	1.36	1.42	1.59	0.478+1.72*C_L ns
t_f		1.01	1.87	1.95	2.19	0.787+1.51*C_L ns
t_r	RB TO QB	0.622	1.15	1.20	1.34	0.356+1.77*C_L ns
t_f		0.898	1.66	1.73	1.94	0.674+1.49*C_L ns

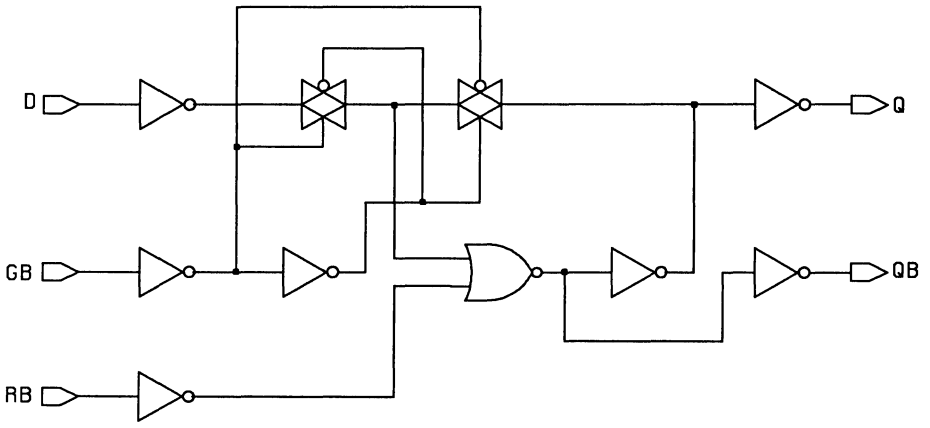
Switching characteristics

LATRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.25	ns
t_h	Hold Time GB to D	−1.50	ns
t_{pwl}	RB Pulse Width (low)	4.00	ns
t_{pwl}	GB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	1.75	ns

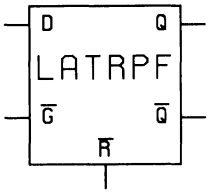
Timing requirements



Functional diagram: LATRP

Fast Transparent Latch with Reset, Positive Edge Triggered

LATRPF holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.176
D: 0.122
GB: 0.229 pF
Cell Size: 12 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.19	2.20	2.29	2.57	1.05+0.921*C_L ns
t_{PHL}		1.49	2.76	2.88	3.23	1.35+0.924*C_L ns
t_{PLH}	D TO QB	2.07	3.82	3.98	4.46	1.95+0.802*C_L ns
t_{PHL}		1.78	3.29	3.43	3.85	1.66+0.817*C_L ns
t_{PLH}	GB TO Q	1.62	2.99	3.11	3.49	1.48+0.919*C_L ns
t_{PHL}		1.57	2.90	3.03	3.40	1.43+0.921*C_L ns
t_{PLH}	GB TO QB	2.13	3.94	4.11	4.61	2.01+0.812*C_L ns
t_{PHL}		2.19	4.05	4.22	4.74	2.07+0.793*C_L ns
t_{PLH}	RB TO Q	1.21	2.24	2.34	2.62	1.08+0.913*C_L ns
t_{PHL}		2.40	4.44	4.63	5.19	2.26+0.941*C_L ns
t_{PLH}	RB TO QB	3.01	5.56	5.80	6.50	2.89+0.804*C_L ns
t_{PHL}		1.80	3.33	3.47	3.90	1.68+0.813*C_L ns
t_r	D TO Q	0.762	1.41	1.47	1.65	0.497+1.77*C_L ns
t_f		0.796	1.47	1.53	1.72	0.578+1.45*C_L ns
t_r	D TO QB	0.703	1.30	1.35	1.52	0.444+1.73*C_L ns
t_f		0.617	1.14	1.19	1.33	0.399+1.45*C_L ns
t_r	GB TO Q	0.779	1.44	1.50	1.68	0.515+1.76*C_L ns
t_f		0.827	1.53	1.59	1.79	0.612+1.43*C_L ns
t_r	GB TO QB	0.710	1.31	1.37	1.53	0.452+1.72*C_L ns
t_f		0.613	1.13	1.18	1.33	0.397+1.44*C_L ns
t_r	RB TO Q	0.781	1.44	1.50	1.69	0.518+1.75*C_L ns
t_f		1.23	2.27	2.37	2.66	1.04+1.23*C_L ns

Switching characteristics (Sheet 1 of 2)

LATRPF

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

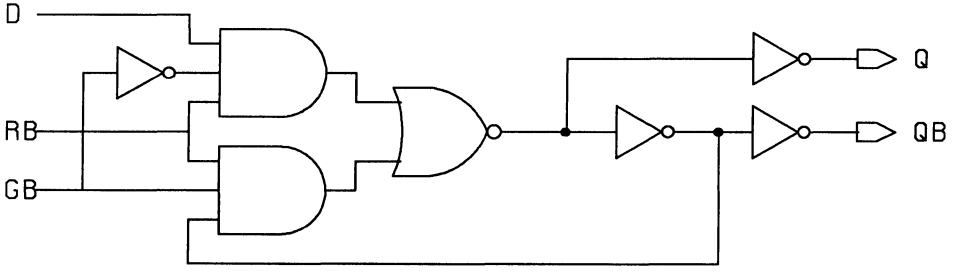
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	RB TO QB	0.727	1.34	1.40	1.57	0.470+1.71*C_L ns
t_f		0.612	1.13	1.18	1.32	0.393+1.46*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.50	ns
t_h	Hold Time GB to D	-1.00	ns
t_{pwl}	RB Pulse Width (low)	6.00	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns
rt	RB Recovery Time	1.25	ns

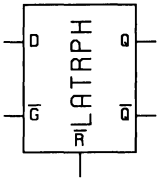
Timing requirements



Functional diagram: LATRPF

D Latch with Reset and Enable (High Drive)

LATRPH holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: D, GB, RB
Outputs: Q, QB
Input Cap.: D: 0.139
GB: 0.054
RB: 0.278 pF
Cell Size: 19 grids wide, 12 grids high

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	2.48	4.57	4.77	5.35	2.39+0.541*C_L ns
t_{PHL}		2.79	5.15	5.37	6.02	2.70+0.551*C_L ns
t_{PLH}	GB TO Q	2.79	5.16	5.38	6.03	2.71+0.551*C_L ns
t_{PHL}		3.19	5.90	6.15	6.90	3.11+0.540*C_L ns
t_{PLH}	RB TO Q	2.47	4.57	4.76	5.35	2.39+0.543*C_L ns
t_{PHL}		1.16	2.15	2.24	2.51	1.07+0.634*C_L ns
t_{PLH}	D TO QB	2.11	3.90	4.07	4.56	2.01+0.641*C_L ns
t_{PHL}		2.00	3.69	3.84	4.31	1.89+0.668*C_L ns
t_{PLH}	GB TO QB	2.52	4.66	4.85	5.45	2.43+0.629*C_L ns
t_{PHL}		2.32	4.28	4.46	5.00	2.21+0.676*C_L ns
t_{PLH}	RB TO QB	2.53	4.67	4.86	5.46	2.44+0.589*C_L ns
t_{PHL}		2.00	3.69	3.84	4.31	1.89+0.670*C_L ns
t_r	D TO Q	0.585	1.08	1.13	1.26	0.418+1.11*C_L ns
t_f		0.517	0.955	0.995	1.12	0.372+0.961*C_L ns
t_r	GB TO Q	0.584	1.08	1.12	1.26	0.416+1.11*C_L ns
t_f		0.522	0.965	1.01	1.13	0.379+0.952*C_L ns
t_r	RB TO Q	0.585	1.08	1.13	1.26	0.418+1.11*C_L ns
t_f		0.583	1.08	1.12	1.26	0.436+0.976*C_L ns
t_r	D TO QB	0.731	1.35	1.41	1.58	0.563+1.12*C_L ns
t_f		0.699	1.29	1.35	1.51	0.551+0.982*C_L ns
t_r	GB TO QB	0.730	1.35	1.41	1.58	0.563+1.11*C_L ns
t_f		0.685	1.26	1.32	1.48	0.536+0.988*C_L ns
t_r	RB TO QB	0.660	1.22	1.27	1.43	0.490+1.13*C_L ns
t_f		0.699	1.29	1.35	1.51	0.552+0.982*C_L ns

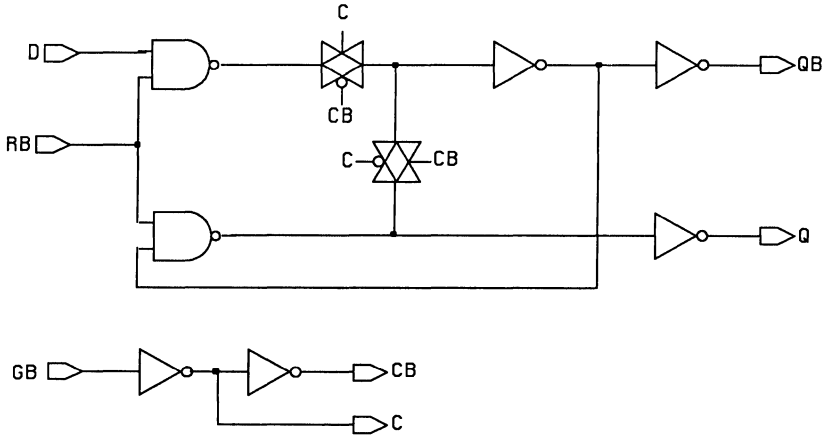
Switching characteristics

LATRPH

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	1.75	ns
t_h	Hold Time GB to D	−1.25	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	1.50	ns

Timing requirements

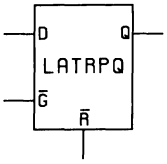


Functional diagram: LATRPH

Transparent Latch with Reset, Positive Edge Triggered

LATRPQ holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.

Inputs: D, GB, RB
Outputs: Q
Input Cap.: D: 0.065
GB: 0.107
RB: 0.055 pF
Cell Size: 8 grids wide, 10 grids high



FUNCTION TABLE

D	GB	RB	Q
L	L	H	L
H	L	H	H
X	H	H	Q_o
X	X	L	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.11	2.06	2.14	2.40	0.899+1.42*C_L ns
t_{PHL}		1.66	3.06	3.19	3.58	1.49+1.07*C_L ns
t_{PLH}	GB TO Q	1.41	2.61	2.72	3.05	1.19+1.43*C_L ns
t_{PHL}		1.48	2.72	2.84	3.19	1.31+1.08*C_L ns
t_{PLH}	RB TO Q	1.11	2.05	2.13	2.39	0.897+1.40*C_L ns
t_{PHL}		1.14	2.11	2.20	2.47	0.982+1.07*C_L ns
t_r	D TO Q	1.11	2.05	2.14	2.40	0.657+3.02*C_L ns
t_f		0.877	1.62	1.69	1.89	0.613+1.76*C_L ns
t_r	GB TO Q	1.12	2.07	2.16	2.42	0.667+3.02*C_L ns
t_f		0.872	1.61	1.68	1.88	0.607+1.77*C_L ns
t_r	RB TO Q	1.10	2.03	2.11	2.37	0.643+3.03*C_L ns
t_f		0.867	1.60	1.67	1.87	0.572+1.96*C_L ns

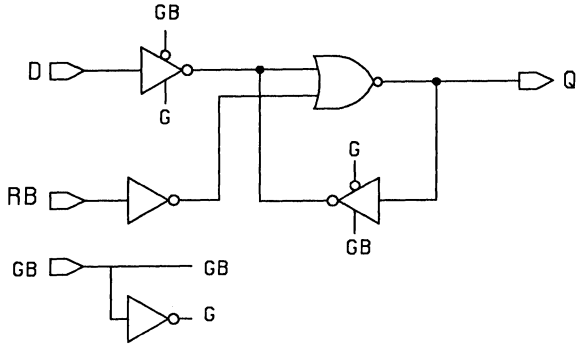
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−0.50	ns
t_{pwl}	GB Pulse Width (low)	4.25	ns
t_{pwl}	RB Pulse Width (low)	5.25	ns
rt	RB Recovery Time	0.25	ns

Timing requirements

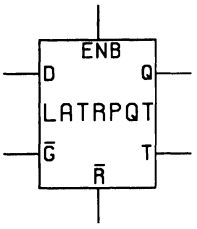
LATRPQ



Functional diagram: LATRPQ

Transparent Latch with Reset and Tristate, Positive Edge Triggered

LATRPQT holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. When ENB is high, the T output is in a Hi-Z state and Q functions as a normal latch using any of the given states defined for Q in the FUNCTION TABLE.



Inputs: ENB, D, GB, RB
Outputs: Q, T
Input Cap.: ENB: 0.121
D: 0.055
GB: 0.123
RB: 0.055 pF
Output Cap.: Q: 0.000
T: 0.135 pF
Cell Size: 13 grids wide, 10 grids high

FUNCTION TABLE

D	GB	RB	ENB	Q	T
L	L	H	L	L	L
H	L	H	L	H	H
X	H	H	L	Q_o	T_o
X	X	L	L	L	L
L	L	H	H	L	HiZ
H	L	H	H	H	HiZ
X	H	H	H	Q_o	HiZ
X	X	L	H	L	HiZ

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.42	2.63	2.74	3.07	1.20+1.49*C_L ns
t_{PHL}		1.58	2.92	3.04	3.42	1.44+0.945*C_L ns
t_{PLH}	D TO T	2.61	4.81	5.02	5.63	2.11+3.31*C_L ns
t_{PHL}		2.78	5.14	5.36	6.01	2.40+2.56*C_L ns
t_{PLH}	GB TO Q	1.67	3.08	3.21	3.60	1.44+1.49*C_L ns
t_{PHL}		1.45	2.68	2.80	3.14	1.29+1.07*C_L ns
t_{PLH}	GB TO T	2.85	5.27	5.49	6.16	2.36+3.31*C_L ns
t_{PHL}		2.65	4.90	5.11	5.73	2.25+2.69*C_L ns
t_{PLH}	RB TO Q	1.14	2.10	2.19	2.46	0.917+1.46*C_L ns
t_{PHL}		1.20	2.21	2.30	2.58	1.02+1.19*C_L ns
t_{PLH}	RB TO T	2.32	4.28	4.47	5.01	1.83+3.27*C_L ns
t_{PHL}		2.44	4.51	4.70	5.28	2.01+2.89*C_L ns
t_{PLH}	ENB TO T	0.548	1.01	1.05	1.18	0.147+2.67*C_L ns
t_{PHL}		0.827	1.53	1.59	1.79	0.527+2.00*C_L ns
t_r	D TO Q	1.33	2.46	2.57	2.88	0.863+3.13*C_L ns
t_f		0.881	1.63	1.70	1.90	0.610+1.80*C_L ns
t_r	D TO T	1.17	2.16	2.25	2.53	0.640+3.53*C_L ns
t_f		0.958	1.77	1.84	2.07	0.576+2.54*C_L ns
t_r	GB TO Q	1.33	2.46	2.57	2.88	0.866+3.12*C_L ns
t_f		0.875	1.62	1.69	1.89	0.604+1.81*C_L ns

Switching characteristics (Sheet 1 of 2)

LATRPQT

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

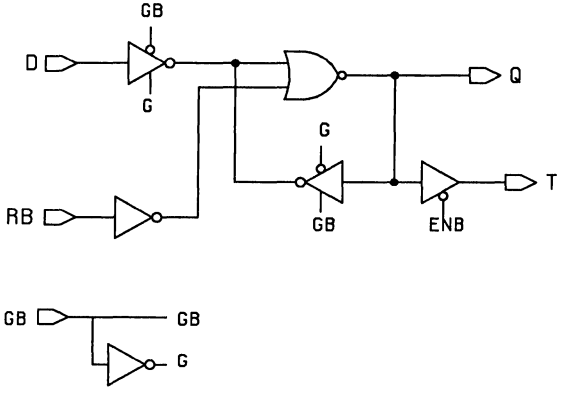
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	GB TO T	1.17	2.16	2.25	2.53	0.640+3.53*C_L ns
t_f		0.958	1.77	1.84	2.07	0.576+2.54*C_L ns
t_r	RB TO Q	1.26	2.34	2.44	2.73	0.789+3.17*C_L ns
t_f		0.989	1.83	1.90	2.14	0.650+2.26*C_L ns
t_r	RB TO T	1.17	2.16	2.25	2.53	0.640+3.53*C_L ns
t_f		0.960	1.77	1.85	2.07	0.578+2.54*C_L ns
t_r	ENB TO T	1.14	2.11	2.19	2.46	0.606+3.55*C_L ns
t_f		0.950	1.75	1.83	2.05	0.568+2.54*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−1.50	ns
t_{pwl}	GB Pulse Width (low)	4.50	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	0.00	ns
rt		1.50	ns

Timing requirements

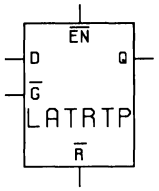


Functional diagram: LATRPQT

Transparent Latch with Reset and Tristate, Positive Edge Triggered

LATRTP holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. When ENB is high, the output is in a Hi-Z state.

Inputs: ENB, D, GB, RB
Outputs: Q
Input Cap.: ENB: 0.126
D: 0.038
GB: 0.056
RB: 0.055 pF
Output Cap.: Q: 0.095 pF
Cell Size: 16 grids wide, 12 grids high



FUNCTION TABLE

D	GB	RB	ENB	Q
L	L	H	L	L
H	L	H	L	H
X	H	H	L	Q_o
X	X	L	L	L
X	X	X	H	Z

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	3.03	5.60	5.84	6.55	2.80+1.55*C_L ns
t_{PHL}		3.25	6.01	6.26	7.03	3.04+1.38*C_L ns
t_{PLH}	RB TO Q	2.76	5.09	5.31	5.96	2.52+1.55*C_L ns
t_{PHL}		2.57	4.75	4.95	5.55	2.36+1.38*C_L ns
t_{PLH}	GB TO Q	3.44	6.36	6.63	7.44	3.21+1.53*C_L ns
t_{PHL}		3.78	6.97	7.27	8.15	3.57+1.37*C_L ns
t_{PLH}	ENB TO Q	0.633	1.17	1.22	1.37	0.393+1.60*C_L ns
t_{PHL}		0.938	1.73	1.81	2.03	0.726+1.41*C_L ns
t_r	D TO Q	1.44	2.67	2.78	3.12	0.930+3.42*C_L ns
t_f		1.39	2.56	2.67	2.99	0.991+2.63*C_L ns
t_r	RB TO Q	1.43	2.64	2.76	3.09	0.917+3.42*C_L ns
t_f		1.39	2.57	2.68	3.01	0.997+2.62*C_L ns
t_r	GB TO Q	1.44	2.65	2.76	3.10	0.922+3.42*C_L ns
t_f		1.39	2.57	2.68	3.00	0.997+2.61*C_L ns
t_r	ENB TO Q	1.22	2.25	2.35	2.64	0.690+3.53*C_L ns
t_f		1.20	2.22	2.31	2.60	0.786+2.77*C_L ns

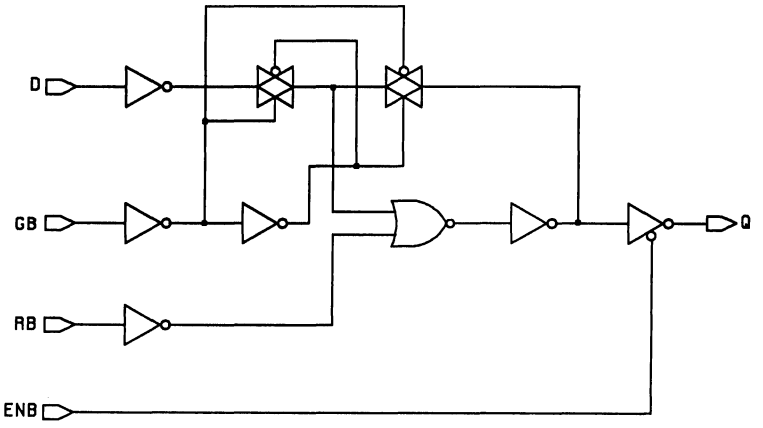
Switching characteristics

LATRTP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	1.50	ns
t_h	Hold Time GB to D	−1.25	ns
t_{pwl}	GB Pulse Width (low)	4.25	ns
t_{pwl}	RB Pulse Width (low)	3.75	ns
rt	RB Recovery Time	0.00	ns
rt		1.00	ns

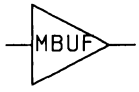
Timing requirements



Functional diagram: LATRTP

Medium Drive Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 3 grids wide, 11 grids high



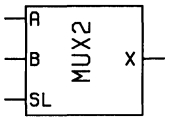
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.975	1.80	1.88	2.11	0.851+0.821*C_L ns
t_{PHL}		1.06	1.95	2.03	2.28	0.936+0.798*C_L ns
t_r	A TO X	0.649	1.20	1.25	1.40	0.384+1.77*C_L ns
t_f		0.630	1.16	1.21	1.36	0.413+1.45*C_L ns

Switching characteristics

2–Input Multiplexer

Inputs: SL, A, B
Outputs: X
Input Cap.: SL: 0.144
A, B: 0.089 pF
Cell Size: 9 grids wide, 12 grids high



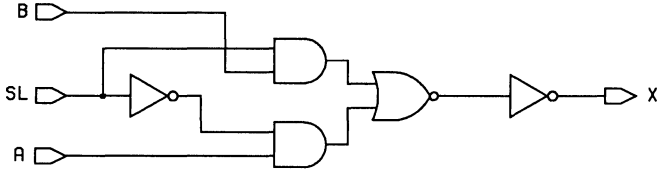
FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.36	2.52	2.63	2.95	1.11+1.67*C_L ns
t_{PHL}		1.34	2.47	2.58	2.89	1.09+1.61*C_L ns
t_{PLH}	SL TO X	1.20	2.22	2.31	2.59	0.949+1.67*C_L ns
t_{PHL}		1.52	2.81	2.93	3.29	1.28+1.64*C_L ns
t_r	*IN TO X	0.969	1.79	1.87	2.09	0.428+3.61*C_L ns
t_f		0.876	1.62	1.69	1.89	0.421+3.03*C_L ns
t_r	SL TO X	0.943	1.74	1.82	2.04	0.399+3.63*C_L ns
t_f		0.911	1.68	1.75	1.97	0.457+3.02*C_L ns
* Slowest of A or B inputs						

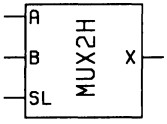
Switching characteristics



Functional diagram: MUX2

2–Input Multiplexer (High Drive)

Inputs: A, SL, B
Outputs: X
Input Cap.: A: 0.106
SL: 0.163
B: 0.105 pF
Cell Size: 8 grids wide, 12 grids high



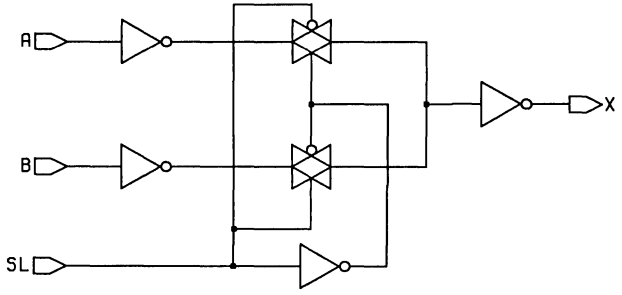
FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.17	2.16	2.25	2.52	1.07+0.626*C_L ns
t_{PHL}		1.26	2.33	2.43	2.73	1.16+0.650*C_L ns
t_{PLH}	SL TO X	1.04	1.91	1.99	2.24	0.941+0.630*C_L ns
t_{PHL}		1.16	2.15	2.24	2.51	1.06+0.658*C_L ns
t_r	*IN TO X	0.635	1.17	1.22	1.37	0.461+1.15*C_L ns
t_f		0.684	1.26	1.32	1.48	0.539+0.967*C_L ns
t_r	SL TO X	0.629	1.16	1.21	1.36	0.455+1.16*C_L ns
t_f		0.657	1.21	1.26	1.42	0.509+0.987*C_L ns
* Slowest of A or B inputs						

Switching characteristics

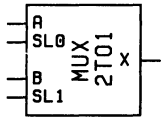


Functional diagram: MUX2H

MUX2TO1

2–Input Multiplexer with Separate Selects

In normal operation, SL1 and SL0 are complementary signals and X = A when SL0 is high, and X = B when SL1 is high.



Inputs: SL1, SL0, A, B
Outputs: X
Input Cap.: All: 0.088 pF
Cell Size: 7 grids wide, 10 grids high

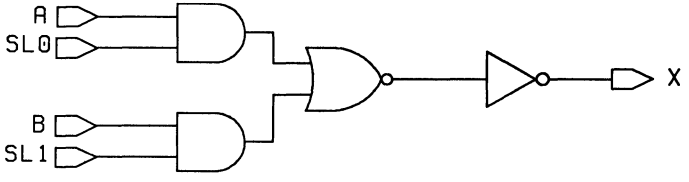
FUNCTION TABLE

SL1	SL0	X
L	L	L
L	H	A
H	L	B
H	H	A + B

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A,B TO X	1.36	2.51	2.62	2.94	1.11+1.67*C_L ns
t_{PHL}		1.34	2.47	2.57	2.89	1.10+1.60*C_L ns
t_{PLH}	*SL TO X	1.35	2.50	2.61	2.93	1.10+1.67*C_L ns
t_{PHL}		1.45	2.67	2.78	3.12	1.20+1.62*C_L ns
t_r	A,B TO X	0.964	1.78	1.86	2.08	0.424+3.60*C_L ns
t_f		0.874	1.61	1.68	1.89	0.421+3.02*C_L ns
t_r	*SL TO X	0.961	1.78	1.85	2.08	0.421+3.60*C_L ns
t_f		0.896	1.66	1.73	1.94	0.444+3.01*C_L ns
* SL timing applies to both SL0 and SL1						

Switching characteristics

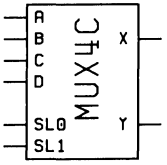


Functional diagram: MUX2TO1

4–Input Multiplexer with Complementary Outputs

SL0 and SL1 cause one of A, B, C, or D to be propagated to the outputs.

Inputs: A, B, C, D, SL0, SL1
Outputs: X, Y
Input Cap.: A, B, C: 0.088
D: 0.089
SL0, SL1: 0.055 pF
Cell Size: 22 grids wide, 12 grids high



FUNCTION TABLE

SL0	SL1	X	Y
L	L	A	$\overline{A}$
H	L	B	$\overline{B}$
L	H	C	$\overline{C}$
H	H	D	$\overline{D}$

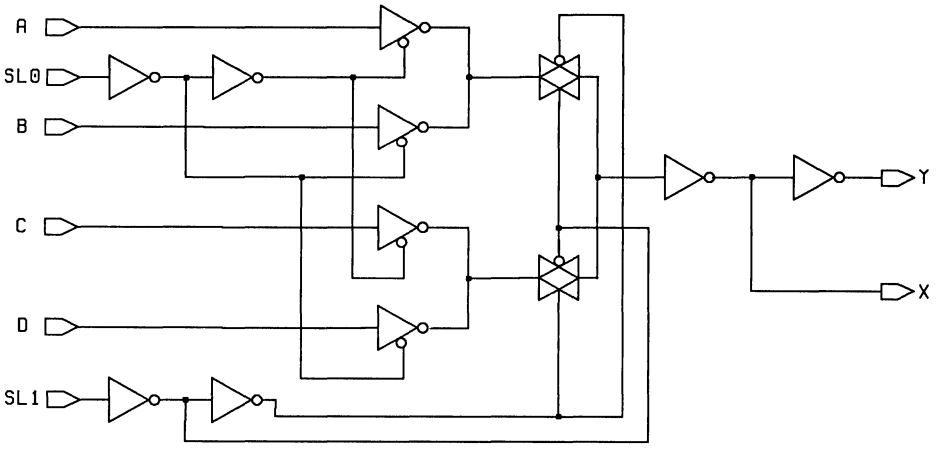
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.82	3.37	3.51	3.94	1.57+1.69*C_L ns
t_{PHL}		2.30	4.26	4.44	4.98	2.05+1.68*C_L ns
t_{PLH}	X TO Y	0.465	0.858	0.894	1.000	0.220+1.63*C_L ns
t_{PHL}		0.539	0.996	1.04	1.16	0.307+1.55*C_L ns
t_{PLH}	**SL TO X	2.07	3.83	3.99	4.48	1.82+1.69*C_L ns
t_{PHL}		2.31	4.26	4.44	4.98	2.05+1.68*C_L ns
t_{PLH}	X TO Y	0.465	0.859	0.895	1.000	0.218+1.65*C_L ns
t_{PHL}		0.547	1.01	1.05	1.18	0.313+1.56*C_L ns
t_{PLH}	*IN TO Y	2.52	4.65	4.85	5.44	2.27+1.63*C_L ns
t_{PHL}		2.11	3.89	4.06	4.55	1.88+1.55*C_L ns
t_{PLH}	**SL TO Y	2.28	4.22	4.40	4.93	2.04+1.65*C_L ns
t_{PHL}		2.60	4.81	5.01	5.62	2.37+1.56*C_L ns
t_r	*IN TO X	1.41	2.60	2.71	3.04	0.874+3.56*C_L ns
t_f		1.47	2.72	2.83	3.18	1.03+2.92*C_L ns
t_r	X TO Y	0.932	1.72	1.79	2.01	0.390+3.61*C_L ns
t_f		0.804	1.48	1.55	1.74	0.348+3.04*C_L ns
t_r	**SL TO X	1.37	2.53	2.63	2.95	0.830+3.58*C_L ns
t_f		1.34	2.48	2.58	2.90	0.893+2.99*C_L ns
t_r	X TO Y	0.912	1.68	1.76	1.97	0.369+3.62*C_L ns
t_f		0.785	1.45	1.51	1.70	0.327+3.05*C_L ns
t_r	*IN TO Y	0.932	1.72	1.79	2.01	0.390+3.61*C_L ns
t_f		0.804	1.48	1.55	1.74	0.348+3.04*C_L ns
t_r	**SL TO Y	0.912	1.68	1.76	1.97	0.369+3.62*C_L ns
t_f		0.785	1.45	1.51	1.70	0.327+3.05*C_L ns

* Slowest of A,B,C, or D inputs
** SL timing applies to both SL0 and SL1

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay and rise time. The delays listed and the delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.



Functional diagram: MUX4C

2–Input NAND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.072 pF
Cell Size: 3 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.755	1.39	1.45	1.63	0.508+1.64*C_L ns
t_{PHL}		0.539	0.995	1.04	1.16	0.336+1.35*C_L ns
t_r	*IN TO X	1.11	2.05	2.14	2.40	0.565+3.63*C_L ns
t_f		0.777	1.44	1.50	1.68	0.361+2.77*C_L ns
* Slowest input						

Switching characteristics

NAN2C

2–Input NAND Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.071 pF
Cell Size: 4 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

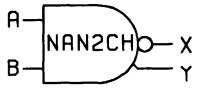
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.786	1.45	1.51	1.70	0.539+1.65*C_L ns
t_{PHL}		0.627	1.16	1.21	1.35	0.422+1.36*C_L ns
t_{PLH}	X TO Y	0.530	0.979	1.02	1.14	0.283+1.64*C_L ns
t_{PHL}		0.556	1.03	1.07	1.20	0.321+1.56*C_L ns
t_{PLH}	*IN TO Y	0.952	1.76	1.83	2.06	0.706+1.64*C_L ns
t_{PHL}		1.09	2.02	2.11	2.36	0.860+1.56*C_L ns
t_r	*IN TO X	1.28	2.36	2.46	2.76	0.733+3.62*C_L ns
t_f		1.02	1.88	1.96	2.20	0.604+2.76*C_L ns
t_r	X TO Y	0.883	1.63	1.70	1.91	0.337+3.64*C_L ns
t_f		0.769	1.42	1.48	1.66	0.309+3.06*C_L ns
t_r	*IN TO Y	0.883	1.63	1.70	1.91	0.337+3.64*C_L ns
t_f		0.769	1.42	1.48	1.66	0.309+3.06*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent on the X output delay. The delays listed for "IN TO Y" and the delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NAND Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.157
B: 0.158 pF
Cell Size: 7 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.535	0.988	1.03	1.16	0.452+0.552*C_L ns
t_{PHL}		0.722	1.33	1.39	1.56	0.589+0.887*C_L ns
t_{PLH}	X TO Y	0.379	0.700	0.730	0.819	0.297+0.545*C_L ns
t_{PHL}		0.346	0.640	0.667	0.748	0.265+0.542*C_L ns
t_{PLH}	*IN TO Y	0.968	1.79	1.86	2.09	0.886+0.545*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.717+0.542*C_L ns
t_r	*IN TO X	1.07	1.98	2.06	2.32	0.914+1.05*C_L ns
t_f		1.26	2.32	2.42	2.72	0.994+1.76*C_L ns
t_r	X TO Y	0.652	1.20	1.26	1.41	0.488+1.09*C_L ns
t_f		0.592	1.09	1.14	1.28	0.459+0.882*C_L ns
t_r	*IN TO Y	0.652	1.20	1.26	1.41	0.488+1.09*C_L ns
t_f		0.592	1.09	1.14	1.28	0.459+0.882*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NAND Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.157
B: 0.158 pF
Cell Size: 5 grids wide, 10 grids high

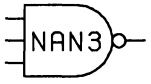
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.454	0.839	0.875	0.981	0.372+0.548*C_L ns
t_{PHL}		0.549	1.01	1.06	1.19	0.413+0.907*C_L ns
t_r	*IN TO X	0.683	1.26	1.31	1.47	0.516+1.11*C_L ns
t_f		0.723	1.34	1.39	1.56	0.447+1.84*C_L ns
* Slowest input						

Switching characteristics

3–Input NAND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.089
B: 0.088
C: 0.089 pF
Cell Size: 4 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.04	1.93	2.01	2.26	0.795+1.66*C_L ns
t_{PHL}		0.648	1.20	1.25	1.40	0.453+1.30*C_L ns
t_r	*IN TO X	1.59	2.94	3.07	3.44	1.05+3.64*C_L ns
t_f		0.934	1.72	1.80	2.02	0.526+2.71*C_L ns
* Slowest input						

Switching characteristics

NAN3C

3–Input NAND Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: A: 0.072
B: 0.071
C: 0.072 pF
Cell Size: 5 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.809	1.49	1.56	1.75	0.560+1.65*C_L ns
t_{PHL}		0.850	1.57	1.64	1.84	0.555+1.96*C_L ns
t_{PLH}	X TO Y	0.623	1.15	1.20	1.35	0.372+1.67*C_L ns
t_{PHL}		0.585	1.08	1.13	1.26	0.349+1.57*C_L ns
t_{PLH}	*IN TO Y	1.18	2.18	2.27	2.55	0.928+1.67*C_L ns
t_{PHL}		1.15	2.12	2.21	2.48	0.909+1.57*C_L ns
t_r	*IN TO X	1.33	2.46	2.57	2.88	0.784+3.65*C_L ns
t_f		1.52	2.80	2.92	3.28	0.906+4.07*C_L ns
t_r	X TO Y	0.951	1.76	1.83	2.06	0.408+3.62*C_L ns
t_f		0.795	1.47	1.53	1.72	0.336+3.06*C_L ns
t_r	*IN TO Y	0.951	1.76	1.83	2.06	0.408+3.62*C_L ns
t_f		0.795	1.47	1.53	1.72	0.336+3.06*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

3–Input NAND Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A, B: 0.174
C: 0.175 pF
Cell Size: 7 grids wide, 11 grids high

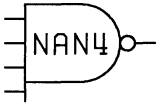
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.539	0.995	1.04	1.16	0.454+0.562*C_L ns
t_{PHL}		0.706	1.30	1.36	1.52	0.556+0.994*C_L ns
t_r	*IN TO X	0.998	1.84	1.92	2.16	0.839+1.06*C_L ns
t_f		1.04	1.93	2.01	2.25	0.748+1.96*C_L ns
* Slowest input						

Switching characteristics

4–Input NAND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.105 pF
Cell Size: 5 grids wide, 12 grids high



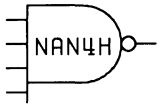
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.38	2.54	2.65	2.97	1.12+1.70*C_L ns
t_{PHL}		0.768	1.42	1.48	1.66	0.578+1.27*C_L ns
t_r	*IN TO X	2.12	3.92	4.09	4.58	1.57+3.65*C_L ns
t_f		1.08	1.99	2.08	2.33	0.677+2.67*C_L ns
* Slowest input						

Switching characteristics

4–Input NAND Gate (High Drive)

Inputs: A, B, C, D
Outputs: X
Input Cap.: A, B, C: 0.211
D: 0.210 pF
Cell Size: 11 grids wide, 12 grids high



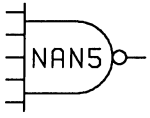
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.724	1.34	1.39	1.56	0.633+0.601*C_L ns
t_{PHL}		0.860	1.59	1.66	1.86	0.732+0.853*C_L ns
t_r	*IN TO X	1.31	2.43	2.53	2.84	1.15+1.10*C_L ns
t_f		1.17	2.16	2.25	2.52	0.906+1.74*C_L ns
* Slowest input						

Switching characteristics

5–Input NAND Gate

Inputs: A, B, C, D, E
Outputs: X
Input Cap.: A: 0.106
B, C, D: 0.105
E: 0.106 pF
Cell Size: 6 grids wide, 12 grids high



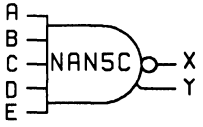
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.57	2.89	3.02	3.39	1.31+1.73*C_L ns
t_{PHL}		1.06	1.96	2.05	2.29	0.826+1.57*C_L ns
t_r	*IN TO X	2.57	4.74	4.94	5.54	2.02+3.66*C_L ns
t_f		1.53	2.82	2.94	3.29	1.03+3.31*C_L ns
* Slowest input						

Switching characteristics

5–Input NAND Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: A: 0.107
B, C: 0.106
D: 0.105
E: 0.106 pF
Cell Size: 7 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

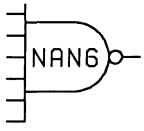
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.70	3.14	3.28	3.68	1.44+1.72*C_L ns
t_{PHL}		1.16	2.15	2.24	2.51	0.926+1.57*C_L ns
t_{PLH}	X TO Y	0.705	1.30	1.36	1.52	0.445+1.73*C_L ns
t_{PHL}		0.830	1.53	1.60	1.79	0.575+1.69*C_L ns
t_{PLH}	*IN TO Y	1.63	3.01	3.14	3.52	1.37+1.73*C_L ns
t_{PHL}		2.27	4.20	4.38	4.91	2.02+1.69*C_L ns
t_r	*IN TO X	2.87	5.29	5.52	6.19	2.32+3.66*C_L ns
t_f		1.80	3.33	3.47	3.89	1.31+3.30*C_L ns
t_r	X TO Y	1.08	1.99	2.07	2.32	0.540+3.57*C_L ns
t_f		1.14	2.10	2.19	2.45	0.693+2.95*C_L ns
t_r	*IN TO Y	1.08	1.99	2.07	2.32	0.540+3.57*C_L ns
t_f		1.14	2.10	2.19	2.45	0.693+2.95*C_L ns
* Slowest Input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see Calculating Standard Cell Timings application note.

6–Input NAND Gate

Inputs: A, B, C, D, E, F
Outputs: X
Input Cap.: A: 0.106
B, C, D, E: 0.105
F: 0.106 pF
Cell Size: 7 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.69	3.12	3.26	3.65	1.43+1.77*C_L ns
t_{PHL}		1.35	2.49	2.60	2.91	1.07+1.87*C_L ns
t_r	*IN TO X	2.90	5.35	5.57	6.25	2.34+3.68*C_L ns
t_f		1.96	3.62	3.77	4.23	1.37+3.94*C_L ns
* Slowest input						

Switching characteristics

2–Input NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.055 pF
Cell Size: 3 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.958	1.77	1.84	2.07	0.480+3.19*C_L ns
t_{PHL}		0.666	1.23	1.28	1.44	0.432+1.56*C_L ns
t_r	*IN TO X	1.68	3.10	3.23	3.62	0.600+7.18*C_L ns
t_f		0.915	1.69	1.76	1.98	0.459+3.04*C_L ns
* Slowest input						

Switching characteristics

2–Input NOR Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.055 pF
Cell Size: 4 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

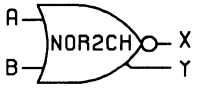
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.19	2.19	2.28	2.56	0.705+3.20*C_L ns
t_{PHL}		0.760	1.40	1.46	1.64	0.524+1.57*C_L ns
t_{PLH}	X TO Y	0.542	1.000	1.04	1.17	0.296+1.64*C_L ns
t_{PHL}		0.690	1.27	1.33	1.49	0.448+1.61*C_L ns
t_{PLH}	*IN TO Y	1.07	1.97	2.05	2.30	0.820+1.64*C_L ns
t_{PHL}		1.40	2.58	2.69	3.01	1.15+1.61*C_L ns
t_r	*IN TO X	2.27	4.19	4.37	4.90	1.19+7.18*C_L ns
t_f		1.14	2.10	2.19	2.46	0.679+3.06*C_L ns
t_r	X TO Y	0.887	1.64	1.71	1.92	0.341+3.64*C_L ns
t_f		0.918	1.70	1.77	1.98	0.467+3.00*C_L ns
t_r	*IN TO Y	0.887	1.64	1.71	1.92	0.341+3.64*C_L ns
t_f		0.918	1.70	1.77	1.98	0.467+3.00*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NOR Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.195
B: 0.193 pF
Cell Size: 7 grids wide, 12 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

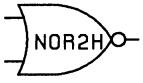
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.662	1.22	1.27	1.43	0.541+0.803*C_L ns
t_{PHL}		0.566	1.05	1.09	1.22	0.486+0.529*C_L ns
t_{PLH}	X TO Y	0.340	0.627	0.654	0.733	0.257+0.546*C_L ns
t_{PHL}		0.390	0.721	0.751	0.843	0.307+0.551*C_L ns
t_{PLH}	*IN TO Y	0.826	1.53	1.59	1.78	0.744+0.546*C_L ns
t_{PHL}		0.931	1.72	1.79	2.01	0.848+0.551*C_L ns
t_r	*IN TO X	1.28	2.36	2.46	2.76	1.03+1.63*C_L ns
t_f		1.01	1.86	1.94	2.18	0.877+0.870*C_L ns
t_r	X TO Y	0.546	1.01	1.05	1.18	0.374+1.14*C_L ns
t_f		0.609	1.12	1.17	1.31	0.469+0.930*C_L ns
t_r	*IN TO Y	0.546	1.01	1.05	1.18	0.374+1.14*C_L ns
t_f		0.609	1.12	1.17	1.31	0.469+0.930*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–Input NOR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.160
B: 0.158 pF
Cell Size: 5 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.580	1.07	1.12	1.25	0.420+1.07*C_L ns
t_{PHL}		0.458	0.847	0.882	0.990	0.379+0.529*C_L ns
t_r	*IN TO X	0.865	1.60	1.67	1.87	0.513+2.35*C_L ns
t_f		0.616	1.14	1.19	1.33	0.476+0.930*C_L ns
* Slowest input						

Switching characteristics

3–Input NOR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.090
B: 0.089
C: 0.090 pF
Cell Size: 4 grids wide, 12 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

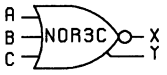
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.06	1.96	2.04	2.29	0.703+2.38*C_L ns
t_{PHL}		0.995	1.84	1.92	2.15	0.753+1.61*C_L ns
t_r	*IN TO X	1.77	3.27	3.41	3.82	0.966+5.35*C_L ns
t_f		1.42	2.62	2.73	3.06	0.955+3.08*C_L ns
* Slowest input						

Switching characteristics

NOR3C

3–Input NOR Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: A: 0.073
B: 0.072
C: 0.073 pF
Cell Size: 5 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

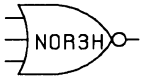
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.45	2.67	2.78	3.12	0.966+3.19*C_L ns
t_{PHL}		0.961	1.77	1.85	2.08	0.721+1.59*C_L ns
t_{PLH}	X TO Y	0.600	1.11	1.15	1.30	0.349+1.67*C_L ns
t_{PHL}		0.745	1.38	1.43	1.61	0.495+1.67*C_L ns
t_{PLH}	*IN TO Y	1.32	2.44	2.54	2.85	1.07+1.67*C_L ns
t_{PHL}		1.71	3.16	3.30	3.70	1.46+1.67*C_L ns
t_r	*IN TO X	2.65	4.90	5.11	5.73	1.58+7.14*C_L ns
t_f		1.48	2.74	2.85	3.20	1.02+3.07*C_L ns
t_r	X TO Y	0.960	1.77	1.85	2.07	0.418+3.61*C_L ns
t_f		1.000	1.85	1.92	2.16	0.549+3.00*C_L ns
t_r	*IN TO Y	0.960	1.77	1.85	2.07	0.418+3.61*C_L ns
t_f		1.000	1.85	1.92	2.16	0.549+3.00*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions see, Calculating Standard Cell Timings application note.

3–Input NOR Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.177
B, C: 0.176 pF
Cell Size: 7 grids wide, 12 grids high



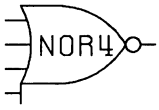
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.907	1.67	1.75	1.96	0.698+1.39*C_L ns
t_{PHL}		0.547	1.01	1.05	1.18	0.463+0.555*C_L ns
t_r	*IN TO X	1.38	2.55	2.66	2.99	0.923+3.06*C_L ns
t_f		0.820	1.51	1.58	1.77	0.676+0.956*C_L ns
* Slowest input						

Switching characteristics

4–Input NOR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.090
B, C: 0.089
D: 0.090 pF
Cell Size: 5 grids wide, 12 grids high



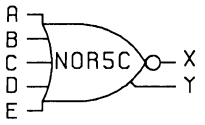
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.53	2.83	2.95	3.31	1.05+3.17*C_L ns
t_{PHL}		1.06	1.96	2.05	2.29	0.812+1.66*C_L ns
t_r	*IN TO X	2.58	4.77	4.98	5.58	1.52+7.09*C_L ns
t_f		1.67	3.08	3.22	3.61	1.20+3.11*C_L ns
* Slowest input						

Switching characteristics

5–Input NOR Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: All: 0.089 pF
Cell Size: 9 grids wide, 11 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

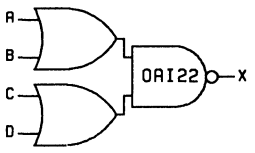
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.469	0.866	0.903	1.01	0.220+1.66*C_L ns
t_{PHL}		0.536	0.991	1.03	1.16	0.302+1.56*C_L ns
t_{PLH}	*IN TO Y	1.85	3.41	3.56	3.99	1.58+1.76*C_L ns
t_{PHL}		2.94	5.42	5.65	6.34	2.66+1.86*C_L ns
t_{PLH}	*IN TO X	3.13	5.77	6.02	6.75	2.88+1.66*C_L ns
t_{PHL}		2.12	3.92	4.08	4.58	1.89+1.56*C_L ns
t_r	Y TO X	0.955	1.76	1.84	2.06	0.413+3.61*C_L ns
t_f		0.808	1.49	1.56	1.75	0.352+3.04*C_L ns
t_r	*IN TO Y	1.49	2.75	2.87	3.22	0.952+3.59*C_L ns
t_f		1.65	3.04	3.17	3.56	1.20+3.01*C_L ns
t_r	*IN TO X	0.955	1.76	1.84	2.06	0.413+3.61*C_L ns
t_f		0.808	1.49	1.56	1.75	0.352+3.04*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays listed for "IN TO X" and delay equation for X assume no load on the Y output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

2–2 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.072
B, C: 0.071
D: 0.072 pF
Cell Size: 5 grids wide, 10 grids high



$X = \overline{(A+B) \bullet (C+D)}$

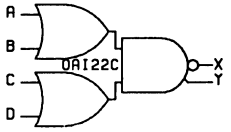
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.79	3.31	3.45	3.87	1.31+3.23*C_L ns
t_{PHL}		0.821	1.52	1.58	1.77	0.614+1.37*C_L ns
t_r	*IN TO X	3.16	5.83	6.08	6.82	2.08+7.16*C_L ns
t_f		1.09	2.01	2.09	2.35	0.671+2.78*C_L ns
* Slowest input						

Switching characteristics

2–2 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: A: 0.072
B: 0.071
C: 0.072
D: 0.071 pF
Cell Size: 7 grids wide, 10 grids high



$X = \overline{(A+B) \cdot (C+D)}$

$Y = (A+B) \cdot (C+D)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.88	3.48	3.63	4.07	1.40+3.23*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.592+1.37*C_L ns
t_{PLH}	X TO Y	0.568	1.05	1.09	1.23	0.319+1.66*C_L ns
t_{PHL}		0.806	1.49	1.55	1.74	0.556+1.66*C_L ns
t_{PLH}	*IN TO Y	1.16	2.14	2.23	2.51	0.911+1.66*C_L ns
t_{PHL}		2.20	4.07	4.24	4.76	1.95+1.66*C_L ns
t_r	*IN TO X	3.19	5.89	6.14	6.89	2.11+7.18*C_L ns
t_f		1.17	2.15	2.24	2.52	0.748+2.78*C_L ns
t_r	X TO Y	0.914	1.69	1.76	1.97	0.368+3.64*C_L ns
t_f		1.12	2.07	2.16	2.42	0.680+2.93*C_L ns
t_r	*IN TO Y	0.914	1.69	1.76	1.97	0.368+3.64*C_L ns
t_f		1.12	2.07	2.16	2.42	0.680+2.93*C_L ns
* Slowest input						

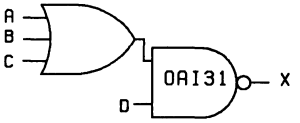
Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays listed for "IN TO Y" and delay equation for Y assume no load on the X output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

OAI31

3–1 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.143
B: 0.142
C: 0.140
D: 0.072 pF
Cell Size: 8 grids wide, 11 grids high



$X = \overline{(A+B+C) \cdot D}$

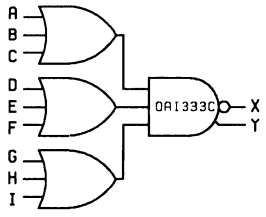
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.15	2.13	2.22	2.49	0.910+1.60*C_L ns
t_{PHL}		1.20	2.21	2.31	2.59	0.984+1.43*C_L ns
t_r	*IN TO X	1.76	3.24	3.38	3.79	1.23+3.53*C_L ns
t_f		1.75	3.23	3.36	3.77	1.33+2.79*C_L ns
* Slowest input						

Switching characteristics

3–3–3 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: A: 0.105
B: 0.107
C, D: 0.105
E: 0.107
F, G: 0.105
H: 0.107
I: 0.105 pF
Cell Size: 17 grids wide, 12 grids high



$X = \overline{(A+B+C) * (D+E+F) * (G+H+I)}$

$Y = (A+B+C) * (D+E+F) * (G+H+I)$

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.412	0.762	0.794	0.891	0.167+1.63*C_L ns
t_{PHL}		0.457	0.843	0.879	0.986	0.222+1.56*C_L ns
t_{PLH}	*IN TO Y	2.04	3.76	3.92	4.40	1.77+1.75*C_L ns
t_{PHL}		3.76	6.94	7.23	8.11	3.48+1.81*C_L ns
t_{PLH}	*IN TO X	3.90	7.20	7.50	8.41	3.65+1.63*C_L ns
t_{PHL}		2.23	4.12	4.30	4.82	2.00+1.56*C_L ns
t_r	Y TO X	0.947	1.75	1.82	2.04	0.406+3.60*C_L ns
t_f		0.784	1.45	1.51	1.69	0.325+3.05*C_L ns
t_r	*IN TO Y	1.47	2.71	2.83	3.17	0.942+3.51*C_L ns
t_f		1.80	3.33	3.47	3.89	1.38+2.82*C_L ns
t_r	*IN TO X	0.947	1.75	1.82	2.04	0.406+3.60*C_L ns
t_f		0.784	1.45	1.51	1.69	0.325+3.05*C_L ns
* Slowest input						

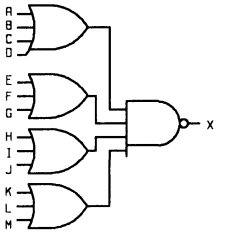
Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays listed for "IN TO X" and delay equation for X assume no load on the Y output. To calculate delays for other loading conditions, see Calculating Standard Cell Timings application note.

OAI4333

4–3–3–3 OR–AND–Invert

Inputs: A, B, C, D, E, F, G, H, I, J, K, L, M
Outputs: X
Input Cap.: A, B, C, D: 0.090
E: 0.105
F: 0.107
G, H: 0.105
I: 0.107
J, K: 0.105
L: 0.107
M: 0.105 pF
Cell Size: 23 grids wide, 12 grids high



$$X = \overline{(A+B+C+D) * (E+F+G) * (H+I+J) * (K+L+M)}$$

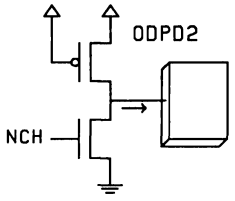
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.78	5.14	5.36	6.01	2.54+1.65*C_L ns
t_{PHL}		3.29	6.08	6.33	7.11	3.04+1.62*C_L ns
t_r	*IN TO X	0.962	1.78	1.85	2.08	0.423+3.59*C_L ns
t_f		0.958	1.77	1.85	2.07	0.510+2.98*C_L ns
* Slowest input						

Switching characteristics

2mA 5V Open–Drain Output Pad

ODPD2 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.529 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	106	195	203	228	9.67+1.92*C_L ns
t_{PHL}		6.53	12.1	12.6	14.1	0.695+0.117*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

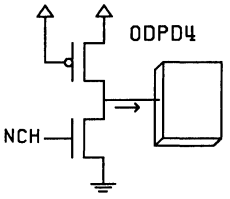
DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

ODPD4

4mA 5V Open–Drain Output Pad

ODPD4 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.059 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	108	200	208	234	11.1+1.94*C_L ns
t_{PHL}		3.35	6.19	6.45	7.24	0.449+0.058*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

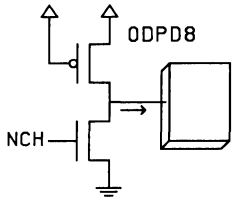
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

8mA 5V Open–Drain Output Pad

ODPD8 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	111	206	215	241	13.5+1.96*C_L ns
t_{PHL}		1.82	3.36	3.50	3.93	0.382+0.029*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

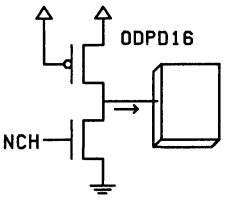
DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

ODPD16

16mA 5V Open–Drain Output Pad

ODPD16 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 4.240 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	117	215	225	252	17.9+1.97*C_L ns
t_{PHL}		1.02	1.88	1.96	2.20	0.298+0.014*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

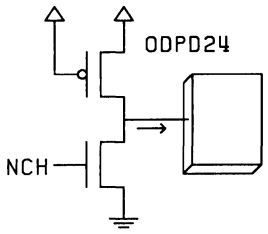
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

24mA 5V Open–Drain Output Pad

ODPD24 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 6.359 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	124	229	238	267	24.1+1.99*C_L ns
t_{PHL}		0.794	1.47	1.53	1.72	0.334+0.009*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

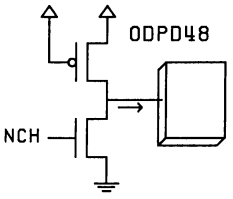
DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

ODPD48

48mA 5V Open–Drain Output Pad

ODPD48 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 12.520 pF
Cell Size: 51 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	142	263	274	307	38.8+2.07*C_L ns
t_{PHL}		0.590	1.09	1.14	1.27	0.360+0.005*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

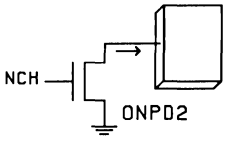
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

2mA 7V Open–Drain Output Pad

ONPD2 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.529 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	102	189	197	221	6.39+1.92*C_L ns
t_{PHL}		6.29	11.6	12.1	13.6	0.487+0.116*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

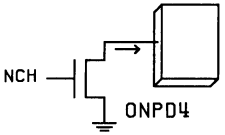
DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

ONPD4

4mA 7V Open–Drain Output Pad

ONPD4 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.059 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	105	194	202	226	7.72+1.94*C_L ns
t_{PHL}		3.23	5.97	6.22	6.98	0.355+0.057*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

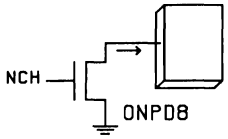
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

8mA 7V Open–Drain Output Pad

ONPD8 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	108	199	208	233	9.84+1.96*C_L ns
t_{PHL}		1.72	3.18	3.32	3.72	0.371+0.027*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

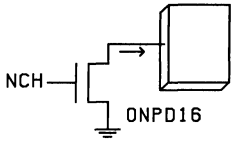
DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

ONPD16

16mA 7V Open–Drain Output Pad

ONPD16 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 4.240 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	113	209	218	244	14.3+1.98*C_L ns
t_{PHL}		0.992	1.83	1.91	2.14	0.274+0.014*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

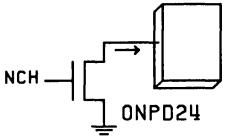
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

24mA 7V Open–Drain Output Pad

ONPD24 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 6.360 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	119	220	229	257	19.5+1.99*C_L ns
t_{PHL}		0.764	1.41	1.47	1.65	0.304+0.009*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

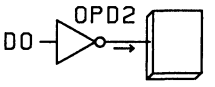
DC specifications

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50 pF load from the output to ground.

OPD2

2mA Output Pad

OPD2 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 1.060 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	5.81	10.7	11.2	12.5	0.745+0.101*C_L ns
t_{PHL}		6.54	12.1	12.6	14.1	0.730+0.116*C_L ns

Switching characteristics

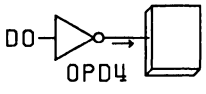
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Output Pad

OPD4 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	3.05	5.64	5.88	6.60	0.524+0.051*C_L ns
t_{PHL}		3.38	6.24	6.50	7.29	0.472+0.058*C_L ns

Switching characteristics

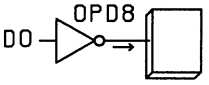
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Output Pad

OPD8 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 4.240 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	1.68	3.10	3.23	3.62	0.413+0.025*C_L ns
t_{PHL}		1.83	3.38	3.53	3.96	0.365+0.029*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

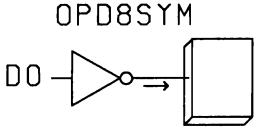
DC specifications

Symmetrical 8mA Output Pad

Features

- Symmetrical hi→low and low→hi drive for off-chip CMOS loads
- Timing specified with input and output at VDD/2
- Drive direct from OSC5402/5502

Symbol



Inputs: DO
Outputs: PAD
Input Cap.: 6.3 pF
Cell Size: 31 grids wide, 60 grids high
Kit Part: OSCARMEYER A

Description

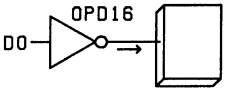
OPD8SYM is functionally similar to the OPD8 cell but with balanced or symmetrical source and sink current drive capability. This results in more closely matched propagation delays between high to low and low to high output swings when driving a CMOS load.

The cell is intended to be driven directly by the OSC5402 or OSC5502 high frequency crystal oscillator cells to provide an off-chip clock signal with the output waveform symmetry from the oscillator preserved as much as possible. In other applications the OPD8SYM can be driven with the same buffers as recommended for an OPD8.

To drive external circuits with an OSC5402 or OSC5502 generated clock, the on-chip oscillator output (OUTB) should drive the OPD8SYM input pin (DO) directly. As with all oscillator cells, the XTLO output should not normally be used to drive external circuits except the crystal and related components.

16mA Output Pad

OPD16 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 8.480 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	0.985	1.82	1.90	2.13	0.352+0.013*C_L ns
t_{PHL}		1.06	1.95	2.03	2.28	0.337+0.014*C_L ns

Switching characteristics

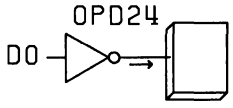
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Output Pad

OPD24 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 11.660 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	0.888	1.64	1.71	1.92	0.371+0.010*C_L ns
t_{PHL}		0.795	1.47	1.53	1.72	0.306+0.010*C_L ns

Switching characteristics

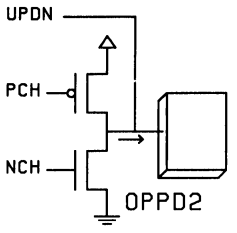
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

2mA Tristate Output Pad with Pullup/Pulldown Port

OPPD2 is similar to OTPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 0.530
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	5.86	10.8	11.3	12.6	0.767+0.102*C_L ns
t_{PHL}		6.55	12.1	12.6	14.1	0.742+0.116*C_L ns
* NCH or PCH						

Switching characteristics

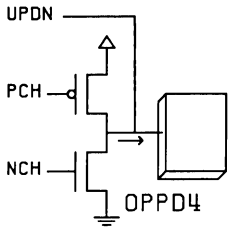
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad with Pullup/Pulldown Port

OPPD4 is similar to OTPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 1.059
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	3.07	5.66	5.90	6.62	0.536+0.051*C_L ns
t_{PHL}		3.39	6.27	6.54	7.33	0.491+0.058*C_L ns
* NCH or PCH						

Switching characteristics

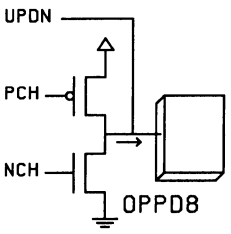
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad with Pullup/Pulldown Port

OPPD8 is similar to OTPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 2.120
UPDN: 52.000 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	1.68	3.11	3.24	3.64	0.419+0.025*C_L ns
t_{PHL}		1.84	3.40	3.54	3.98	0.374+0.029*C_L ns
* NCH or PCH						

Switching characteristics

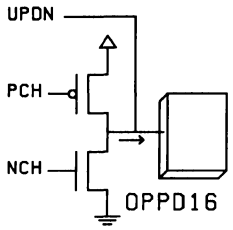
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC specifications

16mA Tristate Output Pad with Pullup/Pulldown Port

OPPD16 is similar to OTPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH, PCH: 4.240
UPDN: 52.000 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.16	5.83	6.08	6.82	0.426+0.055*C_L ns
t_{PHL}		9.06	16.7	17.4	19.6	0.553+0.170*C_L ns
t_{PLH}	*IN TO PAD	0.988	1.82	1.90	2.13	0.355+0.013*C_L ns
t_{PHL}		1.06	1.96	2.04	2.29	0.340+0.014*C_L ns
* NCH or PCH						

Switching characteristics

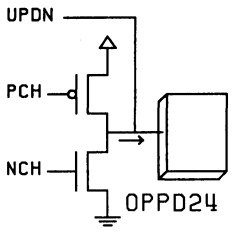
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Tristate Output Pad with Pullup/Pulldown Port

OPPD24 is similar to OTPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 6.360
PCH: 5.300
UPDN: 52.000 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	UPDN TO PAD	3.24	5.98	6.23	6.99	0.504+0.055*C_L ns
t_{PHL}		9.31	17.2	17.9	20.1	0.772+0.171*C_L ns
t_{PLH}	*IN TO PAD	0.891	1.65	1.71	1.92	0.373+0.010*C_L ns
t_{PHL}		0.798	1.47	1.54	1.72	0.309+0.010*C_L ns
* NCH or PCH						

Switching characteristics

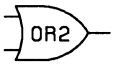
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

2–Input OR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.055 pF
Cell Size: 4 grids wide, 10 grids high



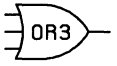
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.08	2.00	2.08	2.34	0.836+1.64*C_L ns
t_{PHL}		1.41	2.61	2.72	3.06	1.17+1.61*C_L ns
t_r	*IN TO X	0.891	1.64	1.71	1.92	0.345+3.64*C_L ns
t_f		0.926	1.71	1.78	2.00	0.475+3.00*C_L ns
* Slowest input						

Switching characteristics

3–Input OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.073
B: 0.072
C: 0.073 pF
Cell Size: 5 grids wide, 10 grids high



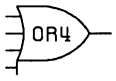
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.32	2.44	2.54	2.85	1.07+1.67*C_L ns
t_{PHL}		1.71	3.16	3.30	3.70	1.46+1.67*C_L ns
t_r	*IN TO X	0.960	1.77	1.85	2.07	0.418+3.61*C_L ns
t_f		1.000	1.85	1.92	2.16	0.549+3.00*C_L ns
* Slowest input						

Switching characteristics

4–Input OR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.073
B, C: 0.072
D: 0.073 pF
Cell Size: 6 grids wide, 10 grids high



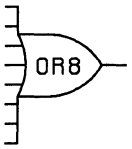
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.39	2.56	2.67	2.99	1.13+1.71*C_L ns
t_{PHL}		2.26	4.17	4.35	4.88	1.99+1.78*C_L ns
t_r	*IN TO X	1.01	1.87	1.95	2.19	0.472+3.61*C_L ns
t_f		1.18	2.17	2.27	2.54	0.726+3.00*C_L ns
* Slowest input						

Switching characteristics

8–Input OR Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: A: 0.055
B, C: 0.054
D, E: 0.055
F, G: 0.054
H: 0.055 pF
Cell Size: 13 grids wide, 10 grids high



(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.45	2.67	2.78	3.12	1.19+1.68*C_L ns
t_{PHL}		2.49	4.61	4.80	5.39	2.26+1.54*C_L ns
t_r	*IN TO X	1.23	2.27	2.37	2.66	0.690+3.61*C_L ns
t_f		1.23	2.27	2.36	2.65	0.816+2.74*C_L ns
* Slowest input						

Switching characteristics

Low Power Crystal Oscillator

Features

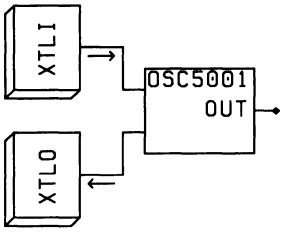
- 10 KHz to 100 KHz operatng range
- Low power (<3 µA at 3.5V)
- 2.7 to 5.5V supply range.
- Amplifier transconductance typically 25–30 µmhos at 3.5V.

Inputs: XTLI
Outputs: OUT, XTLO
Input cap. :XTLI : 5 pF
Output cap. :XTLO : 5 pF
Cell Size: 60 grids high by 63 grids wide
Kit Part: RADAR (X158)

Description

The OSC5001 cell is a low power crystal oscillator core which operates between 10 KHz and 100 KHz. It is well suited for PC real time clock applications. External loading capacitors and an external feedback resistor are required on the XTLI and XTLO pins for proper operation. Cell input and output capacitance values shown are typical values for a packaged part (e.g. RADAR kit part). Figure 2–1 shows a typical application circuit.*

Symbol



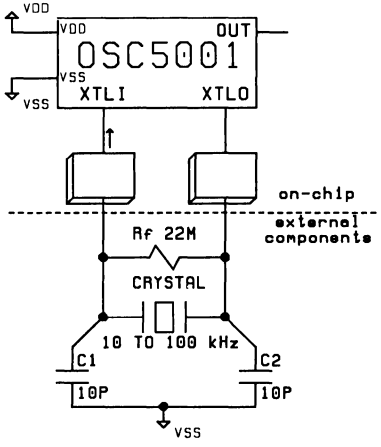


Figure 2–1 Typical application circuit

*See the OSC5001 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	308	568	592	664	307+0.924*C_L ns
t_{PHL}		3.49	6.44	6.71	7.53	3.24+1.64*C_L ns
t_r	XTLI TO OUT	16.2	30.0	31.3	35.1	16.1+0.795*C_L ns
t_f		4.14	7.64	7.97	8.94	3.82+2.12*C_L ns

Switching characteristics

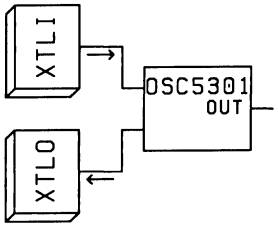
1–10 MHz Crystal Oscillator

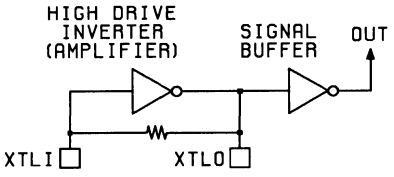
Features

- 1 to 10 MHz operation**
- 40% to 60% output duty cycle
- Buffered on-chip output
- On-chip tuning capacitors
- On-chip bias resistor
- Only requires an external crystal
- Typical gm = 5.2 mA/V

Inputs:	XTLI
Outputs:	OUT, XTLO
Input Cap.:	XTLI: 45 pF
Output Cap.:	XTLO: 50 pF
Cell Size:	109 grids wide, 60 grids high (pad cell)
Kit Part:	VS15_OSC1

Symbol





OSC5301 functional diagram

Description

OSC5301 is a general purpose crystal oscillator cell capable of operation from 1 MHz to 10 MHz.** A fundamental mode quartz crystal is the only external component required since tuning capacitors and a bias (startup) resistor are provided on chip within the cell.

Figure 3–1 shows the internal bias resistor and the load or tuning capacitors required for the crystal pi network. R_B causes the inverter to self bias to approximately $V_{DD}/2$. This is a point where the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B is approximately 1 MΩ and as such it will not affect the AC performance of the circuit.*

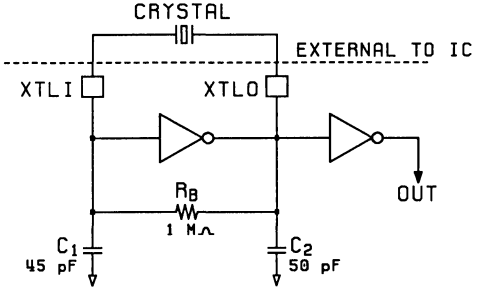


Figure 3–1 Typical fundamental mode circuit

*See the OSC5301 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

**NOTE REGARDING OPERATION AT LESS THAN 3 MHz:

Operation in the range from 1.0–2.9 MHz is discouraged due to limitations of many quartz crystals in that frequency range. The physical size of the quartz blank must be made smaller than the optimum in order to fit into a reasonable standard size package. The result is that non–harmonic modes may be present which vary with temperature and may cause the frequency of oscillation to shift. All modes other than the desired fundamental must be down 6 dB to ensure oscillation at the correct frequency. This means that the equivalent series resistance of undesired modes must be twice that of the fundamental mode.

Most vendors show a 6 dB or better specification in their data sheets. In practice, non–harmonic modes have been observed to become the dominate mode (lowest resistance) as a function of temperature, sometimes over a range of only a few degrees centigrade. For this reason, NCR recommends using a crystal above 2.9 MHz and dividing down to the desired frequency with on–chip flip–flops.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	0.331	0.611	0.637	0.715	0.284+0.311*C_L ns
t_{PHL}		0.344	0.636	0.663	0.743	0.299+0.301*C_L ns
t_r	XTLI TO OUT	0.485	0.895	0.933	1.05	0.399+0.566*C_L ns
t_f		0.410	0.756	0.788	0.885	0.336+0.487*C_L ns

Switching characteristics

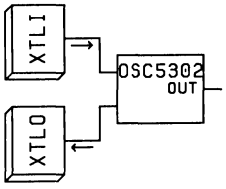
10–25 MHz Crystal Oscillator

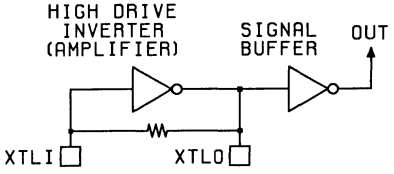
Features

- 10.1 to 25 MHz operation
- 40% to 60% output duty cycle
- Buffered on-chip output
- On-chip tuning capacitors
- On-chip bias resistor
- Only requires an external crystal
- Typical gm = 10.4 mA/V

Inputs:	XTLI
Outputs:	OUT, XTLO
Input Cap.:	XTLI: 45 pF
Output Cap.:	XTLO: 50 pF
Cell Size:	109 grids wide, 60 grids high (pad cell)
Kit Part:	Oscarlater A–G

Symbol





OSC5302 functional diagram

Description

OSC5302 is a general purpose crystal oscillator cell capable of operation from 10.1 MHz to 25 MHz. A fundamental mode quartz crystal is the only external component required since tuning capacitors and a bias (startup) resistor are provided on chip within the cell.

Figure 4–1 shows the internal bias resistor and the load or tuning capacitors required for the crystal pi network. R_B causes the inverter to self bias to approximately $V_{DD}/2$. This is a point where the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B is approximately 1 MΩ and as such it will not affect the AC performance of the circuit.*

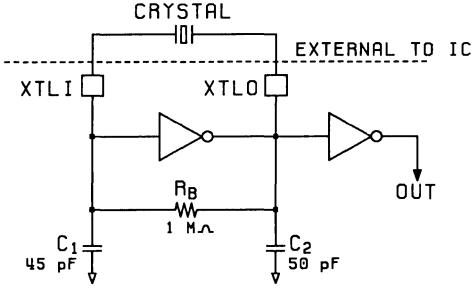


Figure 4–1 Typical fundamental mode circuit

*See the OSC5302 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	0.331	0.611	0.637	0.715	0.284+0.311*C_L ns
t_{PHL}		0.344	0.636	0.663	0.743	0.299+0.301*C_L ns
t_r	XTLI TO OUT	0.485	0.895	0.933	1.05	0.399+0.566*C_L ns
t_f		0.410	0.756	0.788	0.885	0.336+0.487*C_L ns

Switching characteristics

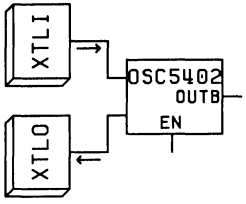
25–50 MHz Crystal Oscillator

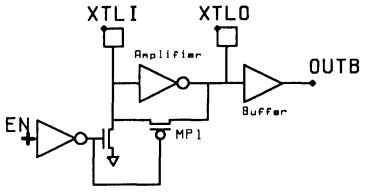
Features

- 25 to 50 MHz operation
- 45% to 55% output duty cycle
- Buffered on-chip output
- Typical gm = 76 mA/V
- Power-down mode

Inputs: XTLI ,EN
Outputs: OUTB, XTLO
Input Cap.: XTLI: 17.143 pF
EN: 0.085 pF
Cell Size: 75 grids by 60 grids high
Kit Part: Oscarmeyer A

Symbol





Functional diagram

Description

OSC5402 is a Pierce type high frequency crystal oscillator cell designed to operate from 25 MHz to 50 MHz. Designs using a fundamental mode crystal require two external tuning capacitors and possibly a resistor to complete the oscillator circuit. Oscillators in this frequency range are often designed to use a third overtone crystal because fundamental mode crystals are not as easy to obtain above 25 or 30 MHz. An additional inductor and coupling capacitor are required for overtone operation.

The power-down mode allows the oscillator to be turned off when it is not needed, to conserve power. This is especially useful in battery powered applications. The EN (ENable) pin must be high for normal operation and low for power-down mode. In power-down mode the self-bias device, MP1, is turned off and the XTLI input is pulled to ground by an open drain n-channel FET. This causes XTLO and OUTB to go to a logic 1.

Preferred locations for OSC5402 are near the center of any side of the packaged part to minimize bond wire and lead frame parasitics.*

*See the OSC5402 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_{PLH}	EN TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_r	XTLI TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns
t_r	EN TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns

Switching characteristics

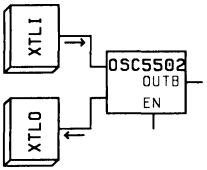
50–70 MHz Crystal Oscillator

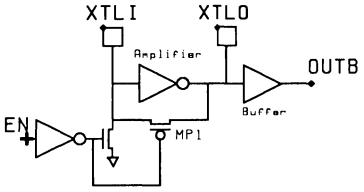
Features

- 50 to 70 MHz operation
- 40% to 60% output duty cycle
- Buffered on-chip output
- Typical gm = 152 mA/V
- Power-down mode

Inputs: XTLI ,EN
Outputs: OUTB, XTLO
Input Cap.: XTLI: 28.780 pF
EN: 0.085 pF
Cell Size: 92 grids by 60 grids high
Kit Part: Oscarmeyer A

Symbol





Functional diagram

Description

OSC5502 is a Pierce type high frequency crystal oscillator cell designed to operate from 50 MHz to 70 MHz. Designs using a fundamental mode crystal require two external tuning capacitors and possibly a resistor to complete the oscillator circuit. Oscillators in this frequency range are often designed to use a third overtone crystal because fundamental mode crystals are not as easy to obtain above 25 or 30 MHz. An additional inductor and coupling capacitor are required for overtone operation.

The power-down mode allows the oscillator to be turned off when it is not needed, to conserve power. This is especially useful in battery powered applications. The EN (ENable) pin must be high for normal operation and low for power-down mode. In power-down mode the self-bias device, MP1, is turned off and the XTLI input is pulled to ground by an open drain n-channel FET. This causes XTLO and OUTB to go to a logic 1.

Preferred locations for OSC5502 are near the center of any side of the packaged part to minimize bond wire and lead frame parasitics. It is also desirable to provide a dedicated V_{DD} and V_{SS} pin next to the oscillator for optimum operation.*

*See the OSC5502 in the *NCR ASIC Analog Data Book* for further information and complete specifications.

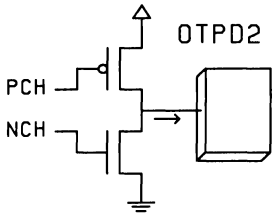
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_{PLH}	EN TO OUTB	1.11	2.05	2.14	2.40	1.09+0.167*C_L ns
t_{PHL}		1.07	1.98	2.06	2.31	1.05+0.160*C_L ns
t_r	XTLI TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns
t_r	EN TO OUTB	0.529	0.976	1.02	1.14	0.488+0.269*C_L ns
t_f		0.541	1.000	1.04	1.17	0.515+0.174*C_L ns

Switching characteristics

2mA Tristate Output Pad

OTPD2 is an output pad capable of output currents up to 2mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 0.530 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	5.81	10.7	11.2	12.5	0.745+0.101*C_L ns
t_{PHL}		6.54	12.1	12.6	14.1	0.730+0.116*C_L ns
* NCH or PCH						

Switching characteristics

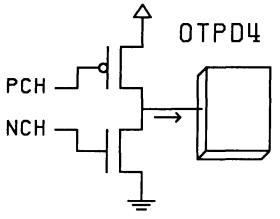
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad

OTPD4 is an output pad capable of output currents up to 4mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 1.059 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	3.05	5.64	5.88	6.60	0.524+0.051*C_L ns
t_{PHL}		3.38	6.24	6.50	7.29	0.472+0.058*C_L ns
* NCH or PCH						

Switching characteristics

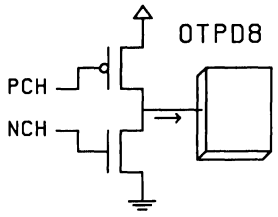
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad

OTPD8 is an output pad capable of output currents up to 8mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 2.120 pF
Cell Size: 22.5 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.68	3.10	3.23	3.62	0.413+0.025*C_L ns
t_{PHL}		1.83	3.38	3.53	3.96	0.365+0.029*C_L ns
* NCH or PCH						

Switching characteristics

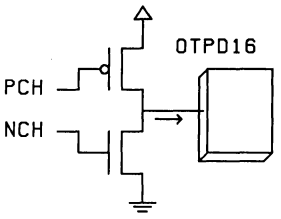
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Tristate Output Pad

OTPD16 is an output pad capable of output currents up to 16mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: All: 4.240 pF
Cell Size: 27 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.985	1.82	1.90	2.13	0.352+0.013*C_L ns
t_{PHL}		1.06	1.95	2.03	2.28	0.337+0.014*C_L ns
* NCH or PCH						

Switching characteristics

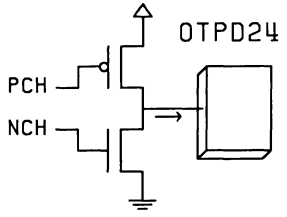
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Tristate Output Pad

OTPD24 is an output pad capable of output currents up to 24mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 6.359
PCH: 5.299 pF
Cell Size: 36 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.888	1.64	1.71	1.92	0.371+0.010*C_L ns
t_{PHL}		0.795	1.47	1.53	1.72	0.306+0.010*C_L ns
* NCH or PCH						

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

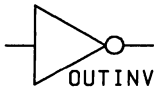
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

OUTINV

Output Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.209 pF
Cell Size: 3 grids wide, 11 grids high



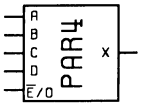
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.321	0.594	0.619	0.694	0.257+0.429*C_L ns
t_{PHL}		0.332	0.613	0.639	0.717	0.271+0.405*C_L ns
t_r	A TO X	0.481	0.888	0.926	1.04	0.359+0.810*C_L ns
t_f		0.443	0.817	0.852	0.956	0.345+0.650*C_L ns

Switching characteristics

4–Bit Parity Checker

Inputs: A, B, C, D, EBO
Outputs: X
Input Cap.: A, B, C: 0.055
D: 0.054
EBO: 0.055 pF
Cell Size: 25 grids wide, 11 grids high



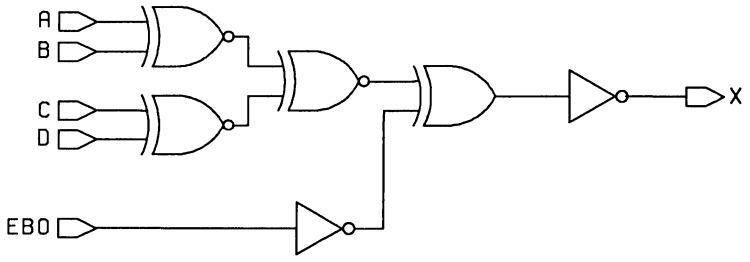
FUNCTION TABLE

EBO	Number of Inputs Which Are High	X
L	0, 2, 4	H
L	1, 3	L
H	0, 2, 4	L
H	1, 3	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	4.60	8.49	8.85	9.93	4.35+1.63*C_L ns
t_{PHL}		5.96	11.0	11.5	12.9	5.62+2.23*C_L ns
t_{PLH}	EBO TO X	1.64	3.02	3.15	3.54	1.38+1.68*C_L ns
t_{PHL}		1.94	3.59	3.74	4.20	1.63+2.10*C_L ns
t_r	*IN TO X	1.21	2.24	2.34	2.62	0.698+3.44*C_L ns
t_f		1.79	3.31	3.45	3.87	1.31+3.24*C_L ns
t_r	EBO TO X	0.950	1.75	1.83	2.05	0.405+3.63*C_L ns
t_f		1.29	2.39	2.49	2.79	0.786+3.38*C_L ns
* Slowest of A, B, C, or D inputs						

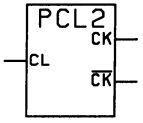
Switching characteristics



PCL2

Two–Phase Clock

PCL2 is for use with clocked cells and to produce high drive signals of true and complement value. CK is the noninverted or true output and CKB is the inverted or complement output.



Inputs: CL
Outputs: CK, CKB
Input Cap.: CL: 0.109 pF
Cell Size: 10 grids wide, 11 grids high

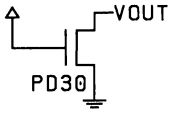
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CL TO CK	1.000	1.85	1.93	2.16	0.929+0.476*C_L ns
t_{PHL}		1.09	2.01	2.10	2.35	1.01+0.485*C_L ns
t_{PLH}	CL TO CKB	1.34	2.47	2.58	2.89	1.27+0.437*C_L ns
t_{PHL}		1.30	2.41	2.51	2.82	1.24+0.451*C_L ns
t_r	CL TO CK	0.563	1.04	1.08	1.22	0.437+0.839*C_L ns
t_f		0.533	0.985	1.03	1.15	0.424+0.725*C_L ns
t_r	CL TO CKB	0.497	0.918	0.957	1.07	0.374+0.821*C_L ns
t_f		0.455	0.840	0.876	0.982	0.351+0.693*C_L ns

Switching characteristics

30μA N–Channel Pulldown Device

PD30 is a weak n–channel pulldown that sinks 30μA when VOUT equals five volts and can be used as a pulldown on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See the PPD200, PPD400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.



*NOTE: The gate input on the PD30 cannot be used to turn the transistor on or off.

Inputs:
Outputs: VOUT
Input Cap.: : 0.000 pF
Output Cap.: VOUT: 0.034 pF
Cell Size: 12 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	*VOUT	1499	2769	2887	3239	1490+58.6*C_L ns
t_f	*VOUT	37.3	68.9	71.9	80.6	19.0+122*C_L ns
* Timing is from VOUT = 4.5V to VOUT = 2.25V						

Switching characteristics

(V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	30μA typical

DC specifications

Power–on Reset

Features

- No external components required
- Retriggerable reset under digital control
- Supply glitch immunity

POR is a digital cell that guarantees a logic low level during power up for the purpose of resetting logic elements to known states. Upon application of the positive supply voltage to the device, POR causes SYS to remain low for approximately 6 µs after the positive supply has exceeded 2.6V. This insures that all digital circuits are operational before the SYS output goes high. An additional input is supplied to the cell which allows the output to be retriggered under external control.

FUNCTION TABLE

V_{DD}	RES	SYS
↑	L	⌐
X	H	L
H	↓	⌐

Inputs: RES
Outputs: SYS
Input Cap.: RES: 0.019 pF
Cell Size: 31 grids wide, 60 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	RES TO SYS	4717	8712	9082	10189	4713+8.55*C_L ns
t_{PHL}		7.98	14.7	15.4	17.2	7.65+2.19*C_L ns
t_r	RES TO SYS	31.8	58.8	61.3	68.8	30.9+6.31*C_L ns
t_f		1.72	3.18	3.32	3.72	1.17+3.67*C_L ns

Switching characteristics

PARAMETERS AND CONDITIONS	RATING
Supply current (V_{DD} = 5V, V_{RES} = 0V)	74 µA typical
Supply current (V_{DD} = 3V, V_{RES} = 0V)	40 µA typical
V_{DD} trigger voltage	2.6V nominal

Electrical specifications

Application Notes

Reset Timing

The POR cell is not designed for applications requiring precise reset intervals. The duration of the SYS output pulse in a power up condition, or after an external reset input, may vary from the nominal specified timing by 30% or more. Further variations in pulse duration will be observed over varying conditions of supply voltage and temperature. For applications requiring precise timing of a reset signal, an approach utilizing a clocked counter chain is recommended.

No relationship exists between the POR SYS output pulse and the start up time of any crystal oscillator in the NCR standard cell library. In general, the multi-megahertz oscillator cells will require anywhere from 1 ms to 20 ms to reach stable operation after power is applied.

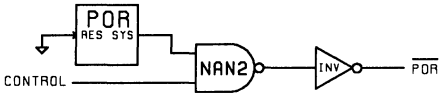
POR provides a certain degree of input glitch immunity. The table given below describes the various situations and responses.

CONDITIONS	RESPONSE
* Glitch-free supply ramp * Supply glitch settles to 2.6V > V_{DD} ≥ 2.0V for at least 100 ns * Supply glitch reaches V_{DD} < 2.0V	SYS output high occurs after V_{DD} = 2.6V + 6.0µs
*Supply glitch settles to V_{DD} ≥ 2.6V *Supply glitch settles to 2.6V > V_{DD} ≥ 2.0V for less than 50 ns	Will not effect SYS output of POR

POR

Testability

NCR requires the chip be simulated and tested with the reset time out feature of the POR disabled. To achieve this, the RESET input on the POR should be grounded, and the POR output should be ANDed with a control signal (NAN2 and INV – see Reset circuit. The control signal should be accessible by the tester during test time at probe and after the chip is packaged. A static pullup may be connected to the control signal path to enable the reset circuit under normal operation. NCR will review the specific implementation of any circuit using the POR at the time of the design review.



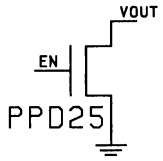
Reset circuit

System Considerations

The NCR POR cell is designed to provide a reset pulse that can be used throughout the chip. If this signal is brought off chip for a system reset, precautions should be taken to insure that all other chips are powered up and functional while the reset pulse is valid.

25μA N–Channel Pulldown Device

PPD25 is a weak n–channel pulldown that sinks 25μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD25 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.891 pF
Output Cap.: VOUT: 0.041 pF
Cell Size: 13 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	5090	9402	9800	10996	18.1+101*C_L ns

Switching characteristics

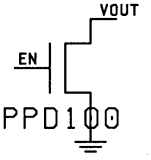
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	25μA typical

DC specifications

100µA N–Channel Pulldown Device

PPD100 is a weak n–channel pulldown that sinks 100µA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD100 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.227 pF
Output Cap.: VOUT: 0.044 pF
Cell Size: 12 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	1262	2331	2430	2726	0.914+25.2*C_L ns

Switching characteristics

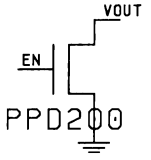
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	100µA typical

DC specifications

200μA N–Channel Pulldown Device

PPD200 is a weak n–channel pulldown that sinks 200μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD200 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.122 pF
Output Cap.: VOUT: 0.038 pF
Cell Size: 8 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	662	1222	1274	1429	0.000+13.2*C_L ns

Switching characteristics

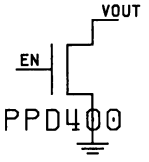
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	200μA typical

DC specifications

400μA N–Channel Pulldown Device

PPD400 is a weak n–channel pulldown that sinks 400μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD400 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.229 pF
Output Cap.: VOUT: 0.045 pF
Cell Size: 9 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	331	611	637	715	0.000+6.62*C_L ns

Switching characteristics

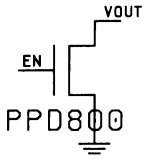
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	400μA typical

DC specifications

800µA N–Channel Pulldown Device

PPD800 is a weak n–channel pulldown that sinks 800µA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD800 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.450 pF
Output Cap.: VOUT: 0.086 pF
Cell Size: 10 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	166	306	319	358	0.000+3.31*C_L ns

Switching characteristics

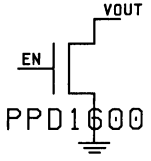
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	800µA typical

DC specifications

1600µA N–Channel Pulldown Device

PPD1600 is a weak n–channel pulldown that sinks 1600µA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD1600 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.227 pF
Output Cap.: VOUT: 0.086 pF
Cell Size: 9 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	84.4	156	163	182	0.000+1.69*C_L ns

Switching characteristics

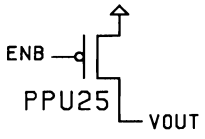
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	1600µA typical

DC specifications

25μA P–Channel Pullup Device

PPU25 is a weak p–channel pullup that sources 25μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU25 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.654 pF
Output Cap.: VOUT: 0.039 pF
Cell Size: 14 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	2164	3997	4166	4674	49.0+42.3*C_L ns

Switching characteristics

(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

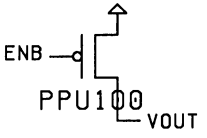
PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	25μA typical

DC specifications

PPU100

100μA P–Channel Pullup Device

PPU100 is a weak p–channel pullup that sources 100μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU100 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.174 pF
Output Cap.: VOUT: 0.048 pF
Cell Size: 8 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	556	1026	1069	1200	11.8+10.9*C_L ns

Switching characteristics

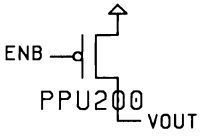
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	100μA typical

DC specifications

200μA P–Channel Pullup Device

PPU200 is a weak p–channel pullup that sources 200μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU200 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.) . The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.094 pF
Output Cap.: VOUT: 0.032 pF
Cell Size: 9 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	284	525	548	614	5.98+5.57*C_L ns

Switching characteristics

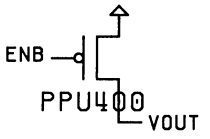
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	200μA typical

DC specifications

400μA P–Channel Pullup Device

PPU400 is a weak p-channel pullup that sources 400μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU400 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.177 pF
Output Cap.: VOUT: 0.061 pF
Cell Size: 9 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	142	262	273	306	3.24+2.77*C_L ns

Switching characteristics

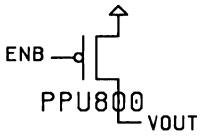
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	400μA typical

DC specifications

800μA P–Channel Pullup Device

PPU800 is a weak p–channel pullup that sources 800μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU800 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.344 pF
Output Cap.: VOUT: 0.117 pF
Cell Size: 11 grids wide, 10 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	71.8	133	138	155	1.88+1.40*C_L ns

Switching characteristics

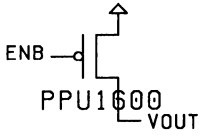
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	800μA typical

DC specifications

1600μA P–Channel Pullup Device

PPU1600 is a weak p–channel pullup that sources 1600μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU1600 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.687 pF
Output Cap.: VOUT: 0.232 pF
Cell Size: 16 grids wide, 9 grids high

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	35.9	66.3	69.1	77.5	1.19+0.694*C_L ns

Switching characteristics

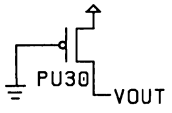
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	1600μA typical

DC specifications

30μA P–Channel Pullup Device

PU30 is a weak p-channel pullup that sources 30μA when VOUT equals zero volts and can be used as a pullup on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See PPU200, PPU400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.



*NOTE: The gate input on the PU30 cannot be used to turn the transistor on or off.

Inputs:
Outputs: VOUT
Input Cap.: : 0.000 pF
Output Cap.: VOUT: 0.021 pF
Cell Size: 3 grids wide, 11 grids high

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*VOUT	1499	2769	2887	3239	1490+58.6*C_L ns
t_r	*VOUT	28.0	51.7	53.9	60.5	9.16+126*C_L ns
* Timing is from VOUT = 0V to VOUT = 2.25V.						

Switching characteristics

(V_{OUT}=0V, V_{DD}=5V)

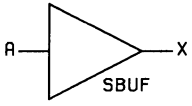
PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	30μA typical

DC specifications

SBUF

Small Drive Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.055 pF
Cell Size: 3 grids wide, 11 grids high



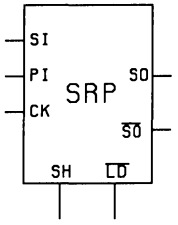
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.981	1.81	1.89	2.12	0.735+1.64*C_L ns
t_{PHL}		1.05	1.93	2.01	2.26	0.811+1.56*C_L ns
t_r	A TO X	0.866	1.60	1.67	1.87	0.318+3.65*C_L ns
t_f		0.770	1.42	1.48	1.66	0.311+3.06*C_L ns

Switching characteristics

Shift Register, Positive Edge Triggered

SRP is a 1-bit shift register. It is positive edge triggered with respect to CK. Serial input is clocked in when SH is high. Parallel input is clocked in when LDB is low. SH and LDB should be tied together for normal operation.



Inputs: SI, SH, PI, LDB, CK
Outputs: SO, SOB
Input Cap.: SI: 0.055
SH: 0.059
PI: 0.056
LDB: 0.059
CK: 0.055 pF
Cell Size: 25 grids wide, 12 grids high

FUNCTION TABLE

SH	SI	LDB	PI	CK	SO	SOB
H	L	H	X	↑	L	H
H	H	H	X	↑	H	L
L	X	L	L	↑	L	H
L	X	L	H	↑	H	L
H	X	L	X	X	*	*
L	X	H	X	X	*	*

* ILLEGAL INPUT COMBINATION

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO SO	2.42	4.47	4.66	5.23	2.30+0.841*C_L ns
t_{PHL}		2.96	5.46	5.69	6.39	2.82+0.912*C_L ns
t_{PLH}	CK TO SOB	3.50	6.46	6.74	7.56	3.38+0.793*C_L ns
t_{PHL}		3.56	6.58	6.86	7.70	3.44+0.834*C_L ns
t_r	CK TO SO	0.734	1.36	1.41	1.59	0.474+1.73*C_L ns
t_f		0.872	1.61	1.68	1.88	0.656+1.44*C_L ns
t_r	CK TO SOB	0.738	1.36	1.42	1.59	0.480+1.72*C_L ns
t_f		0.809	1.49	1.56	1.75	0.591+1.45*C_L ns

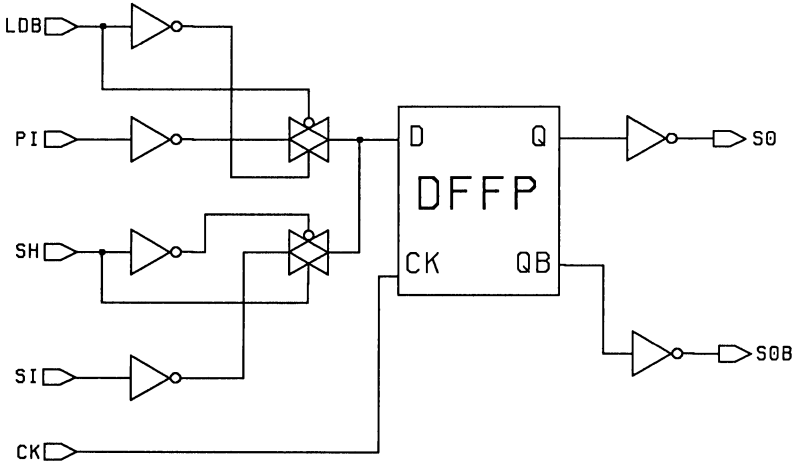
Switching characteristics

SRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time SI to CK	3.00	ns
t_{su}	Setup Time SH to CK	2.75	ns
t_{su}	Setup Time PI to CK	3.25	ns
t_{su}	Setup Time LDB to CK	2.75	ns
t_h	Hold Time CK to SI	−2.25	ns
t_h	Hold Time CK to SH	−2.00	ns
t_h	Hold Time CK to PI	−2.25	ns
t_h	Hold Time CK to LDB	−2.00	ns
t_{pwh}	High CK Pulse Width	4.50	ns
t_{pwl}	Low CK Pulse Width	5.00	ns

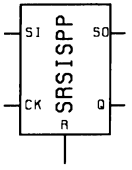
Timing requirements



Functional diagram: SRP

1–Bit Serial–In/Parallel–Out Shift Register

SRSISPP is a single–bit serial input shift register cell. Data on SI is shifted in on the positive edge of CK. Both a serial and parallel output are available to reduce loading on the serial output.



Inputs: SI, CK, R
Outputs: SO, Q
Input Cap.: SI, CK: 0.055
R: 0.054 pF
Cell Size: 26 grids wide, 12 grids high

FUNCTION TABLE

SI	CK	R	SO	Q
X	X	H	L	L
H	↑	L	H	H
L	↑	L	L	L

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*CK TO OUT	3.61	6.67	6.95	7.80	3.35+1.70*C_L ns
t_{PHL}		2.74	5.06	5.28	5.92	2.50+1.58*C_L ns
t_{PHL}	*R TO OUT	2.01	3.70	3.86	4.33	1.76+1.61*C_L ns
t_r	*CK TO OUT	1.20	2.21	2.30	2.59	0.668+3.52*C_L ns
t_f		0.925	1.71	1.78	2.00	0.476+2.99*C_L ns
t_f	*R TO OUT	0.933	1.72	1.80	2.01	0.483+2.99*C_L ns
* OUT refers to both SO and Q						

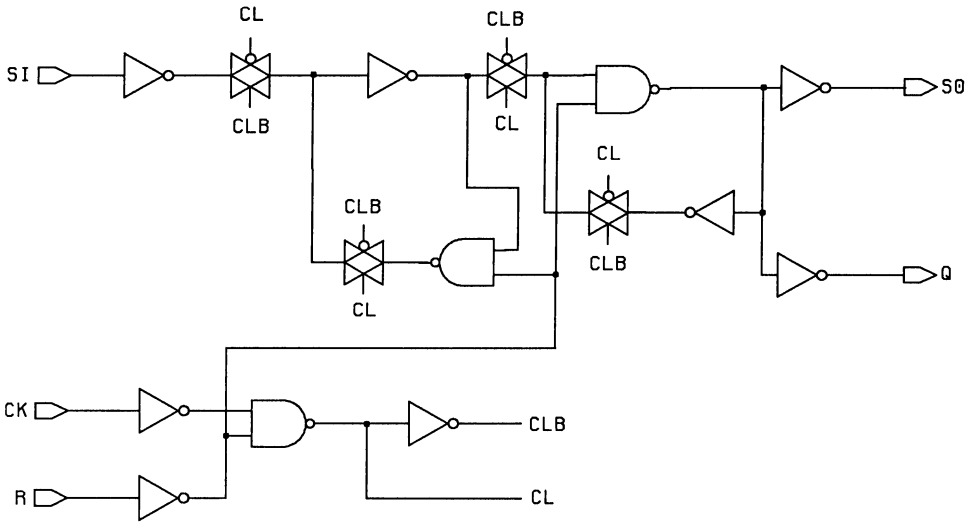
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time SI to CK	0.75	ns
t_h	Hold Time CK to SI	–0.25	ns
t_{pwh}	High CK Pulse Width	4.25	ns
t_{pwh}	R Pulse Width (high)	3.75	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	R Recovery Time	3.50	ns

Timing requirements

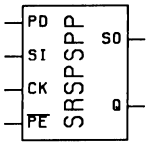
SRSISPP



Functional diagram: SRSISPP

1–Bit Serial/Parallel Shift Register

SRSPSPP is a single–bit serial/parallel input shift register cell. Data on SI is shifted in on the positive edge of CK. Data is loaded asynchronously when PEB goes low. Both serial and parallel outputs are available to reduce loading on the serial output.



Inputs: PEB, PD, SI, CK
Outputs: SO, Q
Input Cap.: PEB, PD: 0.055
SI: 0.056
CK: 0.055 pF
Cell Size: 31 grids wide, 12 grids high

FUNCTION TABLE

CK	PEB	PD	SI	SO	Q
X	L	L	X	L	L
X	L	H	X	H	H
↑	H	X	L	L	L
↑	H	X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*PEB TO OUT	4.20	7.77	8.09	9.08	3.96+1.65*C_L ns
t_{PHL}		3.90	7.20	7.51	8.42	3.66+1.58*C_L ns
t_{PLH}	*PD TO OUT	3.99	7.37	7.69	8.62	3.74+1.65*C_L ns
t_{PHL}		3.99	7.37	7.68	8.62	3.75+1.59*C_L ns
t_{PLH}	*CK TO OUT	2.73	5.04	5.25	5.89	2.48+1.65*C_L ns
t_{PHL}		2.86	5.28	5.50	6.17	2.62+1.57*C_L ns
t_r	*PEB TO OUT	0.916	1.69	1.76	1.98	0.370+3.64*C_L ns
t_f		0.877	1.62	1.69	1.90	0.426+3.01*C_L ns
t_r	*PD TO OUT	0.936	1.73	1.80	2.02	0.391+3.62*C_L ns
t_f		0.859	1.59	1.65	1.86	0.405+3.03*C_L ns
t_r	*CK TO OUT	0.910	1.68	1.75	1.96	0.363+3.64*C_L ns
t_f		0.855	1.58	1.65	1.85	0.401+3.03*C_L ns
* OUT refers to both SO and Q						

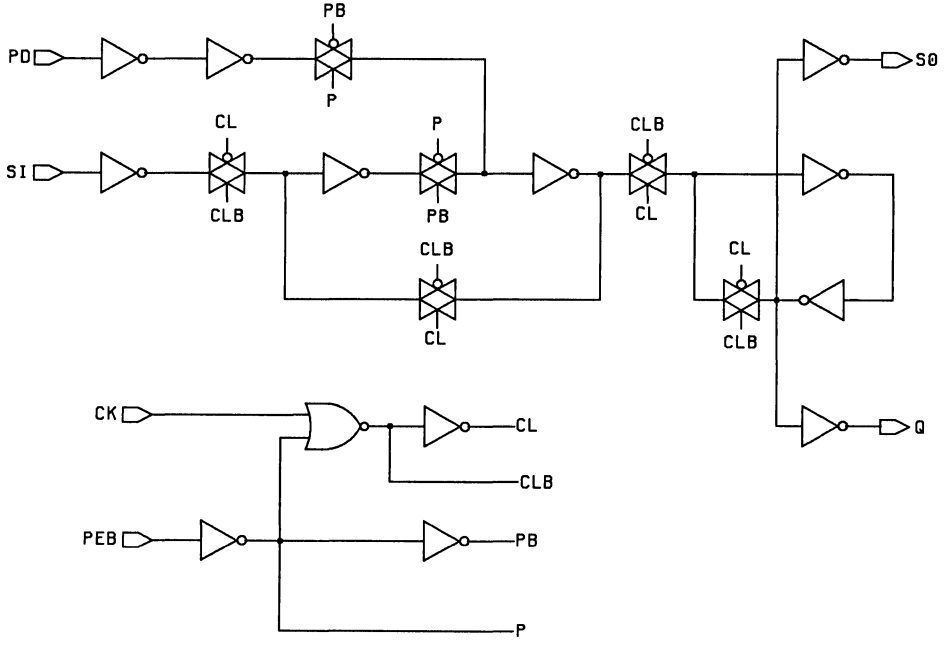
Switching characteristics

SRSPSPP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time SI to CK	2.75	ns
t_{su}	Setup Time PD to PEB	1.50	ns
t_h	Hold Time CK to SI	0.00	ns
t_h	Hold Time PEB to PD	0.00	ns
t_{pwh}	High CK Pulse Width	4.00	ns
t_{pwl}	PEB Pulse Width (low)	3.75	ns
t_{pwl}	Low CK Pulse Width	5.50	ns
rt	PEB Recovery Time	4.50	ns

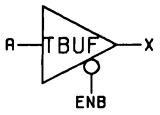
Timing requirements



Functional diagram: SRSPSPP

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.072
ENB: 0.113 pF
Output Cap.: X: 0.168 pF
Cell Size: 9 grids wide, 11 grids high

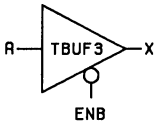
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.19	2.19	2.29	2.57	1.11+0.539*C_L ns
t_{PHL}		1.69	3.13	3.26	3.66	1.59+0.691*C_L ns
t_{PLH}	ENB TO X	1.34	2.48	2.59	2.90	1.27+0.513*C_L ns
t_{PHL}		1.28	2.36	2.46	2.76	1.18+0.677*C_L ns
t_r	A TO X	0.531	0.980	1.02	1.15	0.397+0.891*C_L ns
t_f		0.745	1.38	1.43	1.61	0.617+0.855*C_L ns
t_r	ENB TO X	0.520	0.960	1.000	1.12	0.384+0.903*C_L ns
t_f		0.601	1.11	1.16	1.30	0.470+0.867*C_L ns

Switching characteristics

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.107
ENB: 0.054 pF
Output Cap.: X: 0.158 pF
Cell Size: 10 grids wide, 10 grids high

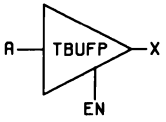
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.05	1.94	2.02	2.27	0.953+0.639*C_L ns
t_{PHL}		1.01	1.87	1.95	2.18	0.920+0.609*C_L ns
t_{PLH}	ENB TO X	1.61	2.98	3.11	3.48	1.52+0.640*C_L ns
t_{PHL}		1.79	3.31	3.45	3.87	1.70+0.621*C_L ns
t_r	A TO X	0.613	1.13	1.18	1.32	0.440+1.15*C_L ns
t_f		0.545	1.01	1.05	1.18	0.398+0.975*C_L ns
t_r	ENB TO X	0.590	1.09	1.14	1.27	0.416+1.16*C_L ns
t_f		0.497	0.917	0.956	1.07	0.346+1.000*C_L ns

Switching characteristics

Noninverting Tristate Buffer

EN is active high. When EN is low, the output is in a Hi-Z state.



Inputs: A, EN
Outputs: X
Input Cap.: A: 0.105
EN: 0.130 pF
Output Cap.: X: 0.168 pF
Cell Size: 8 grids wide, 11 grids high

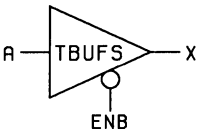
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.13	2.09	2.18	2.44	1.01+0.801*C_L ns
t_{PHL}		1.05	1.95	2.03	2.28	0.946+0.721*C_L ns
t_{PLH}	EN TO X	0.938	1.73	1.81	2.03	0.815+0.817*C_L ns
t_{PHL}		0.388	0.717	0.748	0.839	0.279+0.729*C_L ns
t_r	A TO X	0.907	1.68	1.75	1.96	0.645+1.74*C_L ns
t_f		0.822	1.52	1.58	1.78	0.620+1.34*C_L ns
t_r	EN TO X	1.08	1.99	2.08	2.33	0.835+1.62*C_L ns
t_f		0.669	1.24	1.29	1.44	0.467+1.35*C_L ns

Switching characteristics

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.069
ENB: 0.106 pF
Output Cap.: X: 0.123 pF
Cell Size: 7 grids wide, 9 grids high

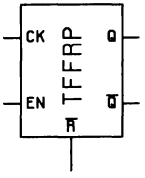
(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.914	1.69	1.76	1.97	0.772+0.939*C_L ns
t_{PHL}		1.39	2.57	2.68	3.00	1.32+0.438*C_L ns
t_{PLH}	ENB TO X	1.03	1.91	1.99	2.23	0.892+0.947*C_L ns
t_{PHL}		0.945	1.74	1.82	2.04	0.811+0.885*C_L ns
t_r	A TO X	0.622	1.15	1.20	1.34	0.330+1.94*C_L ns
t_f		0.700	1.29	1.35	1.51	0.504+1.31*C_L ns
t_r	ENB TO X	0.638	1.18	1.23	1.38	0.348+1.93*C_L ns
t_f		0.589	1.09	1.13	1.27	0.380+1.39*C_L ns

Switching characteristics

Toggle Enable Flip–Flop with Reset

TFFRP is a positive edge triggered toggle flip–flop with active high toggle enable and active low reset. For a faster version of this cell, see TFFRPF.



Inputs: RB, EN, CK
Outputs: Q, QB
Input Cap.: RB: 0.150
EN: 0.095
CK: 0.057 pF
Cell Size: 25 grids wide, 12 grids high

FUNCTION TABLE

RB	EN	CK	Q	QB
L	X	X	L	H
H	H	↑	QB_o	Q_o
H	L	↑	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	RB TO Q	2.10	3.88	4.04	4.54	1.94+1.03*C_L ns
t_{PLH}	CK TO Q	3.61	6.67	6.95	7.80	3.47+0.922*C_L ns
t_{PHL}		4.04	7.46	7.78	8.73	3.90+0.901*C_L ns
t_{PLH}	RB TO QB	3.63	6.71	7.00	7.85	3.50+0.855*C_L ns
t_{PLH}	CK TO QB	2.77	5.13	5.34	5.99	2.64+0.885*C_L ns
t_{PHL}		2.66	4.92	5.12	5.75	2.53+0.894*C_L ns
t_f	RB TO Q	1.03	1.90	1.98	2.22	0.804+1.48*C_L ns
t_r	CK TO Q	0.857	1.58	1.65	1.85	0.595+1.75*C_L ns
t_f		0.804	1.48	1.55	1.74	0.580+1.49*C_L ns
t_r	RB TO QB	0.832	1.54	1.60	1.80	0.575+1.71*C_L ns
t_r	CK TO QB	0.804	1.48	1.55	1.74	0.544+1.73*C_L ns
t_f		0.754	1.39	1.45	1.63	0.532+1.48*C_L ns

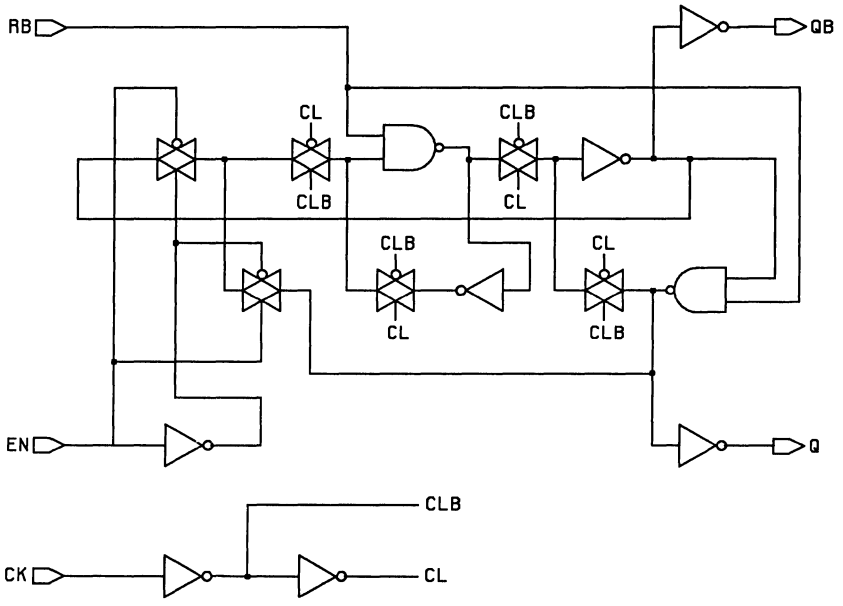
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time EN to CK	2.50	ns
t_h	Hold Time CK to EN	−1.75	ns
t_{pwh}	High CK Pulse Width	5.50	ns
t_{pwl}	RB Pulse Width (low)	6.25	ns
t_{pwl}	Low CK Pulse Width	4.75	ns
rt	RB Recovery Time	−0.50	ns

Timing requirements

TFFRP

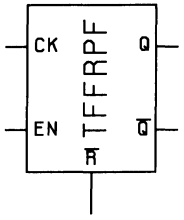


Functional diagram: TFFRP

Fast Toggle Enable Flip–Flop with Reset

TFFRPF is a positive edge triggered toggle flip–flop with active high toggle enable and active low reset.

Inputs: RB, EN, CK
Outputs: Q, QB
Input Cap.: RB: 0.351
EN: 0.126
CK: 0.459 pF
Cell Size: 29 grids wide, 12 grids high



FUNCTION TABLE

RB	EN	CK	Q	QB
L	X	X	L	H
H	H	↑	QB_o	Q_o
H	L	↑	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	RB TO Q	2.18	4.02	4.19	4.70	2.07+0.690*C_L ns
t_{PLH}	CK TO Q	1.66	3.06	3.19	3.58	1.52+0.928*C_L ns
t_{PHL}		1.72	3.17	3.30	3.71	1.62+0.614*C_L ns
t_{PLH}	RB TO QB	3.03	5.60	5.84	6.55	2.91+0.791*C_L ns
t_{PLH}	CK TO QB	2.45	4.52	4.71	5.28	2.33+0.800*C_L ns
t_{PHL}		1.99	3.68	3.83	4.30	1.92+0.456*C_L ns
t_f	RB TO Q	1.15	2.12	2.21	2.48	1.06+0.601*C_L ns
t_r	CK TO Q	0.919	1.70	1.77	1.98	0.657+1.74*C_L ns
t_f		0.716	1.32	1.38	1.55	0.604+0.747*C_L ns
t_r	RB TO QB	0.717	1.32	1.38	1.55	0.453+1.75*C_L ns
t_r	CK TO QB	0.704	1.30	1.35	1.52	0.440+1.76*C_L ns
t_f		0.526	0.971	1.01	1.14	0.424+0.675*C_L ns

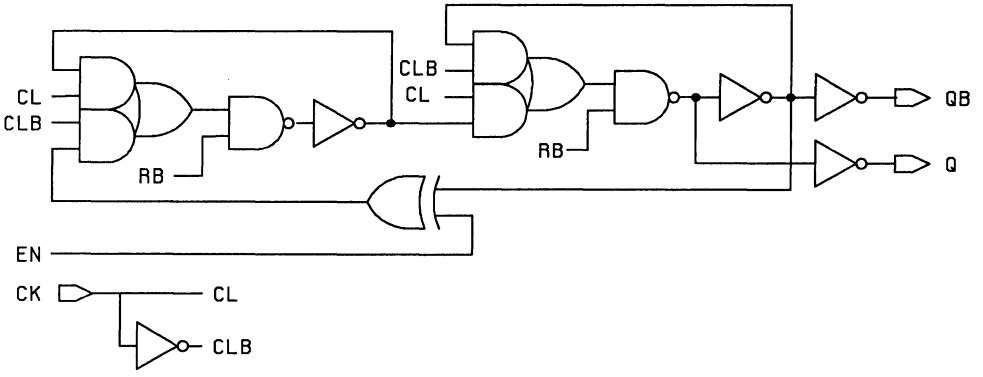
Switching characteristics

TFFRPF

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time EN to CK	4.50	ns
t_h	Hold Time CK to EN	−3.00	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	RB Pulse Width (low)	6.25	ns
t_{pwl}	Low CK Pulse Width	4.25	ns
rt	RB Recovery Time	1.25	ns

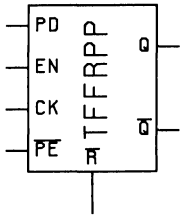
Timing requirements



Functional diagram: TFFRPF

Toggle Enable Flip–Flop with Reset and Synchronous Parallel Load

TFFRPP is a positive edge triggered toggle flip–flop with active low reset and active high toggle enable. Parallel data (PD) is loaded into the flip–flop synchronous to the rising edge of CK when PEB is low.



Inputs: PEB, PD, CK, EN, RB
Outputs: Q, QB
Input Cap.: PEB: 0.057
PD, CK: 0.055
EN: 0.054
RB: 0.055 pF
Cell Size: 41 grids wide, 12 grids high

FUNCTION TABLE

CK	RB	EN	PEB	PD	Q	QB
X	L	X	X	X	L	H
↑	H	X	L	L	L	H
↑	H	X	L	H	H	L
↑	H	H	H	X	QB_o	Q_o
X	H	L	H	X	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.15 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	3.49	6.45	6.73	7.55	3.24+1.67*C_L ns
t_{PHL}		2.96	5.47	5.70	6.40	2.72+1.62*C_L ns
t_{PLH}	CK TO QB	2.12	3.92	4.08	4.58	1.86+1.74*C_L ns
t_{PHL}		2.68	4.95	5.16	5.79	2.39+1.96*C_L ns
t_{PHL}	RB TO Q	3.26	6.03	6.28	7.05	3.02+1.61*C_L ns
t_{PLH}	RB TO QB	2.49	4.60	4.79	5.37	2.23+1.72*C_L ns
t_r	CK TO Q	1.08	1.99	2.07	2.33	0.543+3.56*C_L ns
t_f		0.966	1.78	1.86	2.09	0.520+2.97*C_L ns
t_r	CK TO QB	1.10	2.03	2.12	2.38	0.564+3.57*C_L ns
t_f		1.50	2.77	2.89	3.24	1.05+3.01*C_L ns
t_f	RB TO Q	0.916	1.69	1.76	1.98	0.466+3.00*C_L ns
t_r	RB TO QB	1.13	2.09	2.18	2.44	0.600+3.53*C_L ns

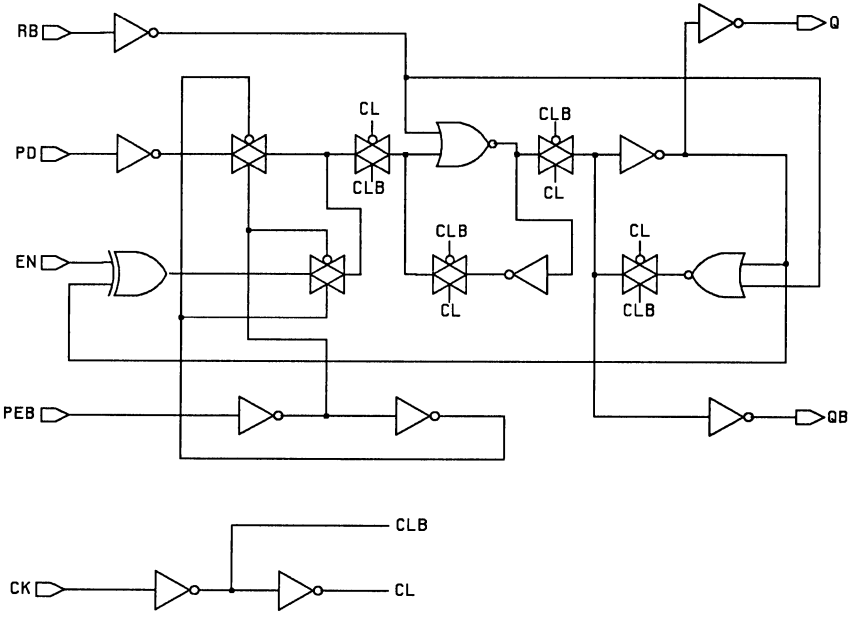
Switching characteristics

TFFRPP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time PEB to CK	4.00	ns
t_{su}	Setup Time PD to CK	3.50	ns
t_{su}	Setup Time EN to CK	6.50	ns
t_h	Hold Time CK to PEB	−3.25	ns
t_h	Hold Time CK to PD	−2.25	ns
t_h	Hold Time CK to EN	−4.25	ns
t_{pwh}	High CK Pulse Width	5.75	ns
t_{pwl}	Low CK Pulse Width	5.50	ns
t_{pwl}	RB Pulse Width (low)	4.75	ns
rt	RB Recovery Time	0.75	ns

Timing requirements



Functional diagram: TFFRPP

NCR VGX700 Gate Array Library Data Sheets
Alphabetical Contents

NCR VGX700 Gate Array Library Data Sheets
Functional Contents

Simple Logic Cells

Buffers

Latches

Decoders and Multiplexers

Flip–Flops

Tristate Elements

Input/Output Cells

Special Function Cells

NCR VGX700 Gate Array Library

Electrical Specifications

DC Characteristics

Sym	Parameter	VDD	Guaranteed Limit			Unit
			0 to 70°C	−40 to 85°C	−55 to 125°C	
V_{IH} (TTL)	Minimum high-level Input voltage	4.5	2.0	2.0	2.0	V
		5.5	2.0	2.0	2.0	
V_{IL} (TTL)	Maximum low-level Input voltage	4.5	0.8	0.8	0.8	V
		5.5	0.8	0.8	0.8	
V_{IH} (CMOS)	Minimum high-level Input voltage	4.5	3.15	3.15	3.15	V
		5.5	3.85	3.85	3.85	
V_{IL} (CMOS)	Maximum low-level Input voltage	4.5	1.35	1.35	1.35	V
		5.5	1.65	1.65	1.65	
V_{OH}	Minimum high-level Output Voltage Any buffer, I_{OH} = −20µa	4.5	4.4	4.4	4.4	V
		5.5	5.4	5.4	5.4	
I_{OH}	Minimum high-level Source Current, V_{OH} = 2.4V	4.5				mA
	2mA buffer		2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	22.8	
	48mA buffer		n/a	n/a	n/a	
V_{OL}	Maximum low-level Output Voltage Any buffer, I_{OL} = 20µa	4.5	0.1	0.1	0.1	V
		5.5	0.1	0.1	0.1	
I_{OL}	Minimum low-level Sink Current, V_{OL} = 0.4V					mA
	2mA buffer		2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	15.1	
	24mA buffer		24.0	24.0	21.6	
	48mA buffer		48.0	48.0	43.2	
I_{IN}	Maximum input leakage current	5.5	±10	±10	±20	µA
I_{OZ}	Maximum output leakage current	5.5	±10	±10	±20	µA

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{DD}	DC power supply voltage	−0.5 to 7.0	V
V_{IN}, V_{OUT}	DC input, output voltage	−0.5 to V_{DD} +0.5	V
I	DC current drain V_{DD} and V_{SS} pins	100	mA
T_{STG}	Storage temperature	−55 to 150	°C
T_L	Lead temperature (less than 10 second soldering)	250	°C
T_{OPER}	Operating temperature Commercial Industrial Military	 0 to 70 −40 to 85 −55 to 125	°C

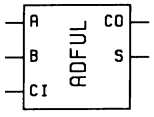
* Stresses beyond those listed in the "Absolute Maximum Ratings" table may cause physical damage to a device and should be avoided. This table does not imply that operation at conditions above those listed in the "Recommended Operating Conditions" is possible. This is a stress rating and operation of a device at or above this rating for an extended period may cause failure or affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	DC power supply voltage	3.0	6.0	V
V_{IN}, V_{OUT}	DC input, output voltage	0	V_{DD}	V

Full Adder

The ADFUL is a single-bit asynchronous adder with carry-in/carry-out function.



Inputs: A, B, CI
Outputs: CO, S
Input Cap.: All: 0.243 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.383 M_{CHL} = 0.440
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.00 gates, 24 array sites

FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A,B to CO	1.53	2.88	3.00	3.37
t_{PHL}		1.30	2.46	2.56	2.88
t_{PLH}	A,B to S	1.73	3.26	3.40	3.82
t_{PHL}		1.95	3.67	3.83	4.30
t_{PLH}	CI to CO	1.34	2.53	2.64	2.97
t_{PHL}		1.18	2.24	2.33	2.62
t_{PLH}	CI to S	1.63	3.07	3.20	3.59
t_{PHL}		1.85	3.48	3.63	4.07

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A,B to CO	1.18	1.15
t_{PHL}		1.01	0.637
t_{PLH}	A,B to S	1.38	1.17
t_{PHL}		1.64	0.780
t_{PLH}	CI to CO	0.997	1.15
t_{PHL}		0.891	0.667
t_{PLH}	CI to S	1.28	1.15
t_{PHL}		1.54	0.750

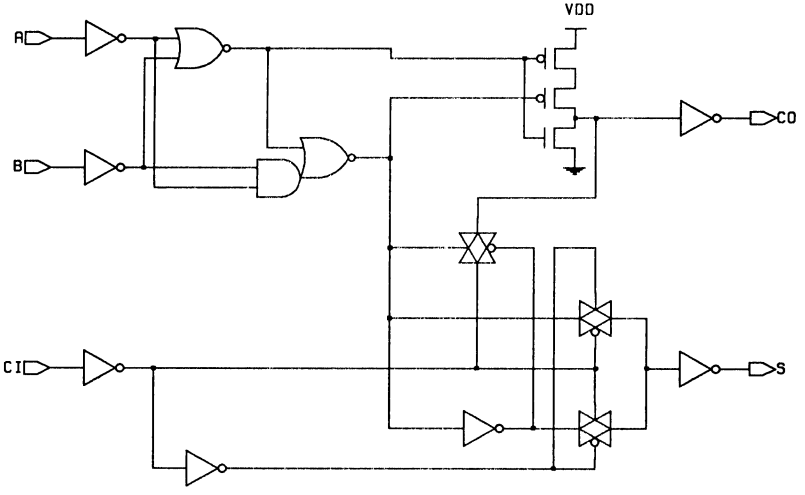
Delay coefficients

ADFUL

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
CO	0.266	2.55	0.294	0.935
S	0.304	2.52	0.392	0.972

Rise/Fall time coefficients for the next cell



Functional diagram: ADFUL

2–Input AND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.061 M_{CHL} = 0.309
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.549	1.03	1.07	1.20
t_{PHL}		0.598	1.14	1.19	1.33
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.334	1.18
t_{PHL}		0.366	0.636

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.183	2.64	0.256	0.949

Rise/Fall time coefficients for the next cell

3–Input AND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.258
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.683	1.27	1.33	1.49
t_{PHL}		0.660	1.25	1.30	1.46
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.495	1.17
t_{PHL}		0.449	0.639

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.253	2.57	0.293	0.921

Rise/Fall time coefficients for the next cell

4–Input AND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.028 M_{CHL} = 0.199
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 6 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.853	1.59	1.66	1.87
t_{PHL}		0.698	1.32	1.37	1.54
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.647	1.22
t_{PHL}		0.506	0.675

Delay coefficients

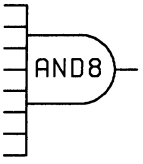
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.331	2.50	0.348	0.879

Rise/Fall time coefficients for the next cell

8–Input AND Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.190
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 12 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.14	2.12	2.21	2.48
t_{PHL}		0.726	1.37	1.43	1.60
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.796	2.13
t_{PHL}		0.537	0.683

Delay coefficients

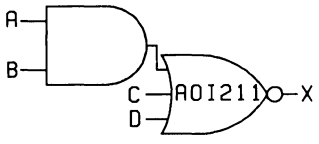
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.500	4.92	0.423	0.877

Rise/Fall time coefficients for the next cell

2–1–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.039 M_{CHL} = 0.100
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



$X = \overline{(A \cdot B) + C + D}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.20	2.25	2.34	2.63
t_{PHL}		0.384	0.723	0.754	0.847
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.684	3.13
t_{PHL}		0.194	0.924

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

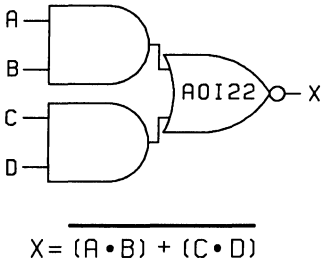
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.999	7.41	0.358	1.72

Rise/Fall time coefficients for the next cell

AOI22

2–2 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.147
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.596	1.12	1.17	1.31
t_{PHL}		0.347	0.659	0.687	0.772
* Slowest input					

Switching characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.266	1.65
t_{PHL}		0.144	0.885

Delay coefficients

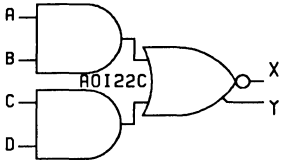
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.467	3.81	0.165	1.72

Rise/Fall time coefficients for the next cell

2–2 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.085 M_{CHL} = 0.137
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 7 array sites



$$X = \overline{(A \cdot B) + (C \cdot D)}$$

$$Y = (A \cdot B) + (C \cdot D)$$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.882	1.65	1.72	1.93
t_{PHL}		0.401	0.758	0.791	0.889
t_{PLH}	*IN to Y**	0.801	1.51	1.58	1.77
t_{PHL}		1.38	2.60	2.71	3.04

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.504	2.14
t_{PHL}		0.204	0.873
t_{PLH}	X to Y	0.167	1.19
t_{PHL}		0.139	0.759

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

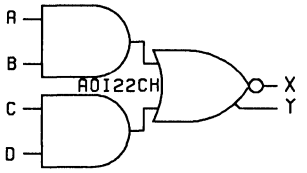
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.04	5.06	0.319	1.69
Y	0.224	2.58	0.410	0.902

Rise/Fall time coefficients for the next cell

AOI22CH

2–2 AND–OR–Invert with Complementary Outputs (High Drive)

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.043 M_{CHL} = 0.167
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.00 gates, 10 array sites



$X = \overline{(A \cdot B) + (C \cdot D)}$

$Y = (A \cdot B) + (C \cdot D)$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to Y	0.651	1.22	1.27	1.43
t_{PHL}		0.936	1.76	1.83	2.06
t_{PLH}	*IN to X**	1.27	2.39	2.49	2.80
t_{PHL}		0.907	1.71	1.78	2.00

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to Y	0.542	0.569
t_{PHL}		0.791	0.466
t_{PLH}	Y to X	0.223	0.562
t_{PHL}		0.098	0.359

Delay coefficients

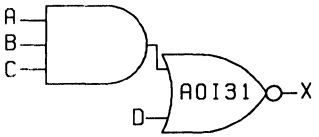
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.290	1.22	0.339	0.361
Y	0.481	1.27	0.529	0.482

Rise/Fall time coefficients for the next cell

3–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.109 M_{CHL} = 0.033
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



$X = \overline{(A \cdot B \cdot C) + D}$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.890	1.67	1.74	1.95
t_{PHL}		0.477	0.892	0.930	1.04
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.498	2.16
t_{PHL}		0.274	1.18

Delay coefficients

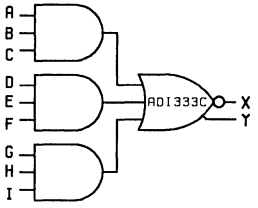
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.703	5.05	0.404	2.33

Rise/Fall time coefficients for the next cell

3–3–3 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.123 M_{CHL} = 0.092
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.50 gates, 13 array sites



$$X = \overline{(A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)}$$

$$Y = (A \cdot B \cdot C) + (D \cdot E \cdot F) + (G \cdot H \cdot I)$$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to Y	1.18	2.21	2.30	2.58
t_{PHL}		1.84	3.43	3.58	4.02
t_{PLH}	*IN to X**	2.34	4.38	4.56	5.12
t_{PHL}		1.49	2.80	2.92	3.28

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to Y	0.926	1.25
t_{PHL}		1.64	0.961
t_{PLH}	Y to X	0.210	1.17
t_{PHL}		0.126	0.617

Delay coefficients

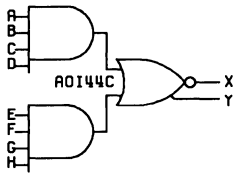
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.287	2.53	0.313	0.844
Y	0.671	2.48	0.750	1.02

Rise/Fall time coefficients for the next cell

4–4 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.244 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.50 gates, 22 array sites



$$X = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$$

$$Y = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.20	2.26	2.35	2.64
t_{PHL}		1.12	2.10	2.19	2.45
t_{PLH}	*IN to Y	1.39	2.62	2.73	3.07
t_{PHL}		1.20	2.25	2.35	2.64
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.754	2.15
t_{PHL}		0.923	0.787
t_{PLH}	*IN to Y	1.11	1.16
t_{PHL}		1.02	0.700

Delay coefficients

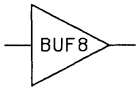
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.458	4.96	0.513	0.949
Y	0.301	2.51	0.373	0.883

Rise/Fall time coefficients for the next cell

Noninverting Buffer (8X Drive)

BUF8 has 8 times the drive of an SBUF.



Inputs: A
Outputs: X
Input Cap.: A: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.260 M_{CHL} = 0.368
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 11 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.498	0.948	0.989	1.11
t_{PHL}		0.657	1.25	1.31	1.47

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.365	0.150
t_{PHL}		0.477	0.162

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

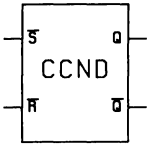
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.293	0.259	0.399	0.073

Rise/Fall time coefficients for the next cell

Cross–Coupled NAND Latch

CCND is very sensitive to negative spikes on SB or RB.

Inputs: SB, RB
Outputs: Q, QB
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.221 M_{CHL} = 0.138
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



FUNCTION TABLE

SB	RB	Q	QB
L	L	*	*
L	H	H	L
H	L	L	H
H	H	Q_o	QB_o

* Both outputs will remain high as long as SB and RB remain low, but the output states are unpredictable if SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	RB to Q	0.654	1.23	1.28	1.44
t_{PLH}	RB to QB	0.489	0.927	0.967	1.09
t_{PHL}		0.639	1.20	1.25	1.41
t_{PLH}	SB to Q	0.491	0.931	0.971	1.09
t_{PHL}		0.643	1.21	1.26	1.42
t_{PHL}	SB to QB	0.867	1.63	1.70	1.91

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	RB to Q	0.457	0.871
t_{PLH}	RB to QB	0.206	1.19
t_{PHL}		0.438	0.891
t_{PLH}	SB to Q	0.209	1.18
t_{PHL}		0.443	0.889
t_{PHL}	SB to QB	0.442	2.29

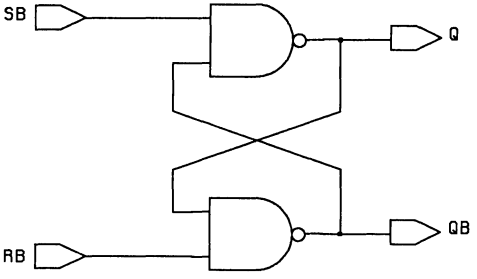
Delay coefficients

CCND

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.440	1.80	0.344	1.64
QB	0.438	1.81	0.339	1.82

Rise/Fall time coefficients for the next cell

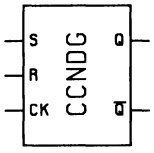


Functional diagram: CCND

Gated R/S Flip–Flop

CCNDG is very sensitive to positive spikes on S and R while CK is high.

Inputs: S, CK, R
Outputs: Q, QB
Input Cap.: S: 0.081
CK: 0.162
R: 0.081 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.139 M_{CHL} = 0.086
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.00 gates, 10 array sites



FUNCTION TABLE

CK	S	R	Q	QB
L	X	X	Q_0	QB_0
H	L	L	Q_0	QB_0
H	L	H	L	H
H	H	L	H	L
H	H	H	*	*

* Both outputs will remain high as long as S, R, and CK are high, but the output states are unpredictable if S and R go low simultaneously or if CK goes low while S and R are still high.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	R to Q	0.858	1.61	1.68	1.88
t_{PLH}	R to QB	0.676	1.27	1.33	1.49
t_{PHL}		0.654	1.23	1.28	1.44
t_{PLH}	S to Q	0.660	1.24	1.30	1.45
t_{PHL}		0.609	1.14	1.19	1.34
t_{PHL}	S to QB	0.839	1.57	1.64	1.84
t_{PLH}	CK to Q	0.676	1.27	1.33	1.49
t_{PHL}		0.846	1.59	1.65	1.86
t_{PLH}	CK to QB	0.658	1.24	1.29	1.45
t_{PHL}		0.860	1.61	1.68	1.89

Timing characteristics

CCNDG

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	R to Q	0.682	0.875
t_{PLH}	R to QB	0.426	1.20
t_{PHL}		0.475	0.891
t_{PLH}	S to Q	0.413	1.18
t_{PHL}		0.432	0.881
t_{PHL}	S to QB	0.664	0.868
t_{PLH}	CK to Q	0.426	1.20
t_{PHL}		0.671	0.869
t_{PLH}	CK to QB	0.408	1.20
t_{PHL}		0.684	0.875

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

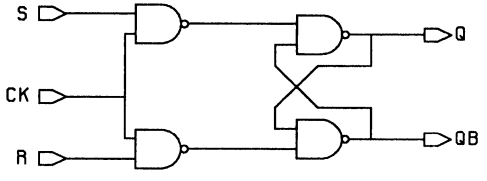
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.467	1.77	0.362	1.62
QB	0.442	1.80	0.364	1.63

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time S to CK	1.77	1.04	0.633
t_{su}	Setup Time R to CK	1.77	1.04	0.633
t_h	Hold Time CK to S	1.77	1.04	0.633
t_h	Hold Time CK to R	1.77	1.04	0.633
t_{pwh}	Pulse Width (high) CK	3.73	2.19	1.34

Timing requirements

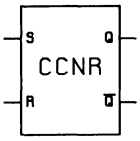


Functional diagram: CCNDG

Cross–Coupled NOR Latch

CCNR is very sensitive to positive spikes on S and R.

Inputs: S, R
Outputs: Q, QB
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.169
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



FUNCTION TABLE

S	R	Q	QB
L	L	Q_o	QB_o
L	H	L	H
H	L	H	L
H	H	*	*

* Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	R to Q	0.894	1.67	1.74	1.95
t_{PHL}		0.275	0.524	0.547	0.615
t_{PLH}	R to QB	0.919	1.72	1.79	2.01
t_{PLH}	S to Q	0.919	1.72	1.79	2.01
t_{PLH}	S to QB	0.894	1.67	1.74	1.95
t_{PHL}		0.275	0.524	0.547	0.615

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	R to Q	0.546	2.18
t_{PHL}		0.109	0.591
t_{PLH}	R to QB	0.575	2.15
t_{PLH}	S to Q	0.575	2.15
t_{PLH}	S to QB	0.546	2.18
t_{PHL}		0.109	0.591

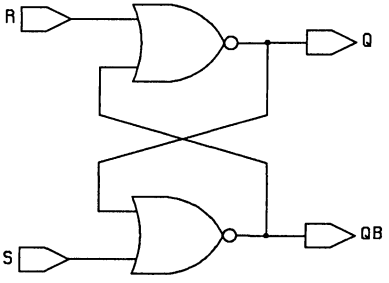
Delay coefficients

CCNR

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.716	5.04	0.222	0.983
QB	0.716	5.03	0.222	0.983

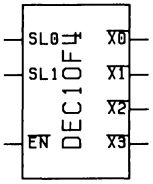
Rise/Fall time coefficients for the next cell



Functional diagram: CCNR

1–of–4 Decoder

Inputs: SL0, SL1, ENB
Outputs: X0B, X1B, X2B, X3B
Input Cap.: SL0, SL1: 0.243
ENB: 0.081 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.451 M_{CHL} = 0.276
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 9.50 gates, 25 array sites



FUNCTION TABLE

SL0	SL1	ENB	X0B	X1B	X2B	X3B
X	X	H	H	H	H	H
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*SL to XnB	0.633	1.21	1.27	1.43
t_{PHL}		0.814	1.54	1.60	1.80
t_{PLH}	*ENB to XnB	0.779	1.49	1.55	1.74
t_{PHL}		0.863	1.63	1.70	1.91
* SL timing applies to both SL0 and SL1. XnB represents any output.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*SL to XnB	0.252	1.20
t_{PHL}		0.545	0.957
t_{PLH}	*ENB to XnB	0.399	1.19
t_{PHL}		0.603	0.899

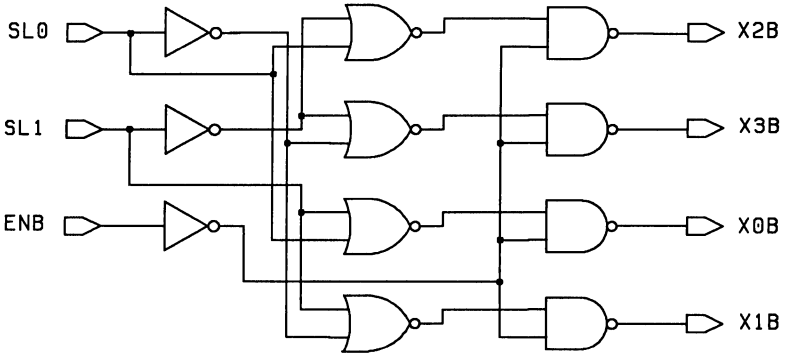
Delay coefficients

DEC1OF4

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X0B	0.266	2.64	0.357	1.56
X1B	0.266	2.64	0.357	1.56
X2B	0.266	2.64	0.357	1.56
X3B	0.266	2.64	0.357	1.56

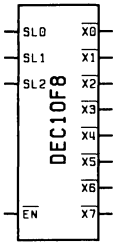
Rise/Fall time coefficients for the next cell



Functional diagram: DEC1OF4

1–of–8 Decoder

Inputs: SL0, SL1, SL2, ENB
Outputs: X0B, X1B, X2B, X3B, X4B, X5B, X6B, X7B
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.257 M_{CHL} = 0.236
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 18.00 gates, 46 array sites



FUNCTION TABLE

SL0	SL1	SL2	ENB	X0B	X1B	X2B	X3B	X4B	X5B	X6B	X7B
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*SL to XnB	1.15	2.16	2.25	2.52
t_{PHL}		1.76	3.29	3.44	3.86
t_{PLH}	SL2 to XnB	0.785	1.48	1.55	1.74
t_{PHL}		0.930	1.75	1.83	2.05
t_{PLH}	SL2 to X4B,X5B,X6B,X7B	1.38	2.60	2.71	3.04
t_{PHL}		1.14	2.15	2.24	2.52
* SL timing applies to SL0, SL1 and ENB. XnB represents any output.					

Timing characteristics

DEC1OF8

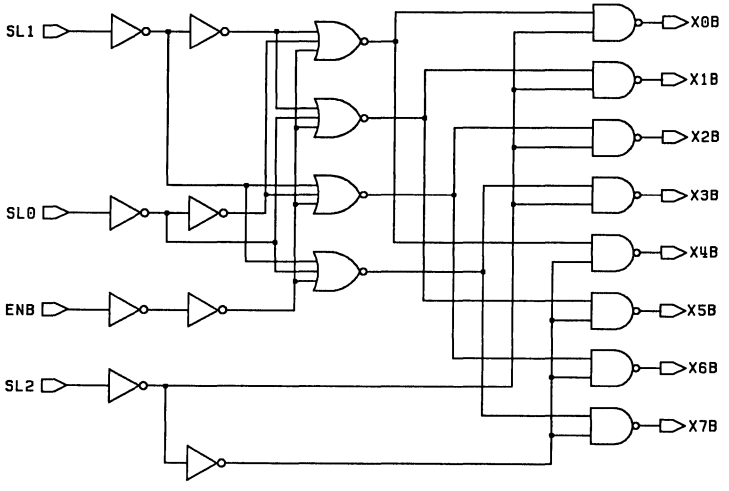
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*SL to XnB	0.854	1.14
t_{PHL}		1.48	1.10
t_{PLH}	SL2 to XnB	0.490	1.17
t_{PHL}		0.680	0.944
t_{PLH}	SL2 to X4B,X5B,X6B,X7B	1.09	1.16
t_{PHL}		0.898	0.907

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X0B	0.333	2.56	0.455	1.56
X1B	0.333	2.56	0.455	1.56
X2B	0.333	2.56	0.455	1.56
X3B	0.333	2.56	0.455	1.56
X4B	0.353	2.54	0.436	1.56
X5B	0.353	2.54	0.436	1.56
X6B	0.353	2.54	0.436	1.56
X7B	0.353	2.54	0.436	1.56

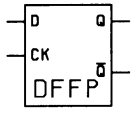
Rise/Fall time coefficients for the next cell



Functional diagram: DEC1OF8

D Flip–Flop, Positive Edge Triggered

DFFP is a fully static D-type flip–flop. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q, QB
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.135 M_{CHL} = 0.145
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.00 gates, 17 array sites

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.20	2.25	2.35	2.63
t_{PHL}		1.05	1.96	2.05	2.30
t_{PLH}	CK to QB	1.39	2.60	2.71	3.04
t_{PHL}		1.40	2.62	2.73	3.07

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.957	1.17
t_{PHL}		0.849	0.850
t_{PLH}	CK to QB	1.15	1.14
t_{PHL}		1.24	0.618

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.286	2.54	0.436	1.00
QB	0.264	2.55	0.307	0.892

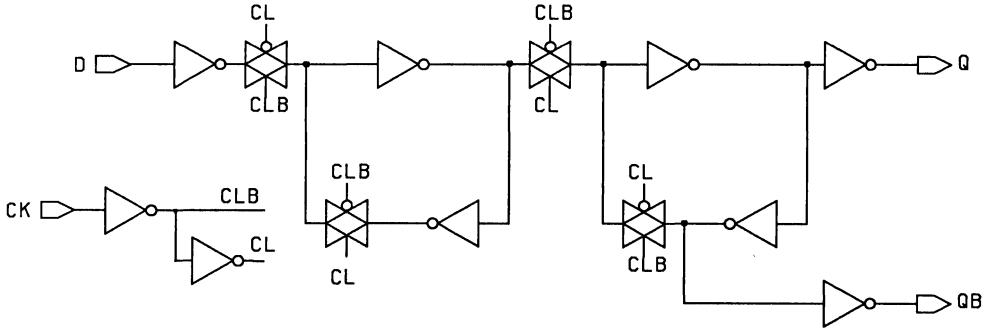
Rise/Fall time coefficients for the next cell

DFFP

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.853	0.500	0.306
t_h	Hold Time CK to D	-0.171	-0.100	-0.061
t_{pwh}	Pulse Width (high) CK	3.34	1.96	1.19
t_{pwl}	Pulse Width (low) CK	3.53	2.07	1.27

Timing requirements

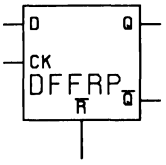


Functional diagram: DFFP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRP is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.162
D, CK: 0.081 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.074 M_{CHL} = 0.066
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.00 gates, 22 array sites



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.17	2.19	2.28	2.56
t_{PHL}		1.06	1.98	2.07	2.32
t_{PLH}	CK to QB	1.40	2.61	2.72	3.05
t_{PHL}		1.35	2.53	2.64	2.96
t_{PHL}	RB to Q	0.710	1.33	1.39	1.56
t_{PLH}	RB to QB	1.04	1.94	2.03	2.27

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.947	1.20
t_{PHL}		0.891	0.885
t_{PLH}	CK to QB	1.18	1.16
t_{PHL}		1.22	0.651
t_{PHL}	RB to Q	0.563	0.745
t_{PLH}	RB to QB	0.821	1.16

Delay coefficients

DFFRP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

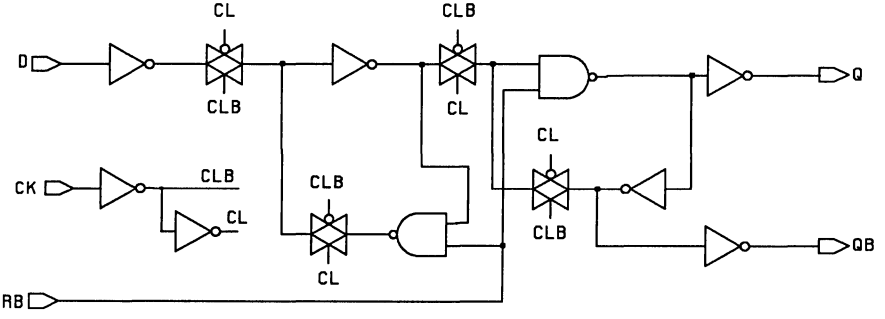
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.339	2.49	0.434	0.935
QB	0.304	2.50	0.363	0.848

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.853	0.500	0.306
t_h	Hold Time CK to D	-0.341	-0.200	-0.122
t_{pwh}	Pulse Width (high) CK	3.34	1.96	1.19
t_{pwl}	Pulse Width (low) RB	3.14	1.84	1.12
t_{pwl}	Pulse Width (low) CK	3.73	2.19	1.34
rt	Recovery Time RB	1.54	0.900	0.550

Timing requirements

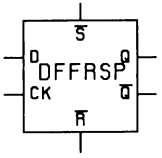


Functional diagram: DFFRP

D Flip–Flop with Reset and Set, Positive Edge Triggered

DFFRSP is a fully static D-type positive edge triggered flip-flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.162
D, CK: 0.081
RB: 0.204 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.154 M_{CHL} = 0.168
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.25 gates, 27 array sites



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to QB	1.35	2.53	2.64	2.96
t_{PHL}		1.42	2.67	2.78	3.12
t_{PLH}	CK to Q	1.83	3.43	3.58	4.02
t_{PHL}		1.70	3.19	3.33	3.74
t_{PHL}	RB to Q	1.36	2.55	2.66	2.98
t_{PLH}	RB to QB	1.01	1.90	1.98	2.22
t_{PHL}		1.05	1.97	2.05	2.31
t_{PLH}	SB to Q	0.846	1.59	1.66	1.86
t_{PHL}		0.735	1.38	1.44	1.62
t_{PHL}	SB to QB	1.44	2.70	2.82	3.16

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to QB	1.10	1.14
t_{PHL}		1.25	0.625
t_{PLH}	CK to Q	1.59	1.13
t_{PHL}		1.53	0.617
t_{PHL}	RB to Q	1.19	0.599
t_{PLH}	RB to QB	0.761	1.16

Delay coefficients (Sheet 1 of 2)

DFFRSP

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		0.879	0.623
t_{PLH}	SB to Q	0.593	1.18
t_{PHL}		0.564	0.625
t_{PHL}	SB to QB	1.27	0.623

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

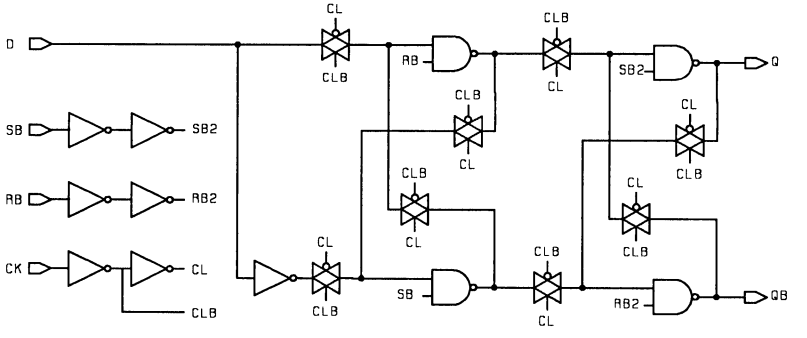
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.260	2.54	0.243	0.948
QB	0.256	2.55	0.284	0.923

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.02	0.600	0.367
t_h	Hold Time CK to D	−0.341	−0.200	−0.122
t_{pwh}	Pulse Width (high) CK	3.34	1.96	1.19
t_{pwl}	Pulse Width (low) SB	3.14	1.84	1.12
t_{pwl}	Pulse Width (low) CK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) RB	3.34	1.96	1.19
rt	Recovery Time SB	−1.195	−0.700	−0.428
rt	Recovery Time RB	1.54	0.900	0.550

Timing requirements

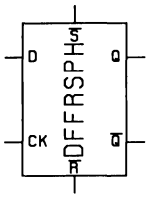


Functional diagram: DFFRSP

Buffered D Flip–Flop with Reset and Set, Positive Edge Triggered (High Drive)

DFFRSPH is a fully static D-type, edge triggered flip-flop. It is positive edge triggered with respect to the single phase clock (CK). RB and SB are asynchronous and active low. Note: This cell is functionally compatible with a DFFRSP except when both RB and SB are low.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.162
D, CK: 0.081
RB: 0.204 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.234 M_{CHL} = 0.264
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.25 gates, 26 array sites



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be low when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.35	2.54	2.65	2.97
t_{PHL}		1.17	2.20	2.29	2.58
t_{PLH}	CK to QB	1.86	3.49	3.64	4.09
t_{PHL}		1.71	3.21	3.34	3.75
t_{PLH}	RB to Q	0.990	1.86	1.94	2.18
t_{PHL}		0.782	1.48	1.54	1.73
t_{PLH}	RB to QB	1.36	2.56	2.67	3.00
t_{PLH}	SB to Q	1.39	2.60	2.71	3.05
t_{PLH}	SB to QB	0.655	1.24	1.29	1.45
t_{PHL}		0.660	1.25	1.30	1.47

Timing characteristics

DFFRSPH

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.15	0.637
t_{PHL}		0.966	0.575
t_{PLH}	CK to QB	1.68	0.508
t_{PHL}		1.53	0.389
t_{PLH}	RB to Q	0.790	0.635
t_{PHL}		0.595	0.474
t_{PLH}	RB to QB	1.18	0.565
t_{PLH}	SB to Q	1.18	0.640
t_{PLH}	SB to QB	0.457	0.622
t_{PHL}		0.483	0.411

Delay coeffiecients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

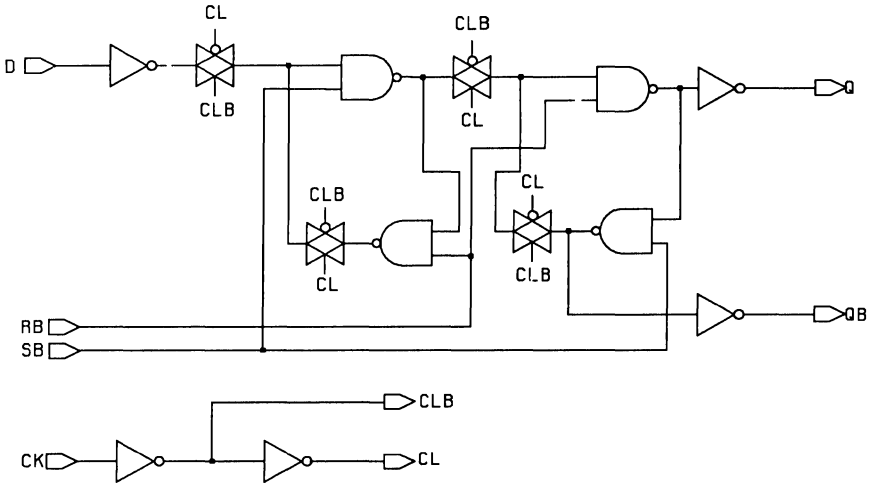
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.416	1.18	0.497	0.466
QB	0.307	1.22	0.348	0.461

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	1.02	0.600	0.367
t_h	Hold Time CK to D	−0.341	−0.200	−0.122
t_{pwh}	Pulse Width (high) CK	3.93	2.30	1.41
t_{pwl}	Pulse Width (low) SB	3.53	2.07	1.27
t_{pwl}	Pulse Width (low) CK	3.73	2.19	1.34
t_{pwl}	Pulse Width (low) RB	3.53	2.07	1.27
rt	Recovery Time SB	−1.195	−0.700	−0.428
rt	Recovery Time RB	1.54	0.900	0.550

Timing requirements

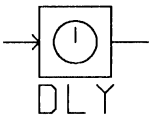


Functional diagram: DFFRSPH

DLYCEL

Delay Cell

Inputs: A
Outputs: X
Input Cap.: A: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.264 M_{CHL} = 0.236
Process Derating: B = 0.72 N = 1.00 W = 1.28
Cell Size: 5.25 gates, 14 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	2.70	4.65	4.85	5.44
t_{PHL}		2.57	4.42	4.61	5.17

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	2.49	0.611
t_{PHL}		2.37	0.635

Delay coefficients

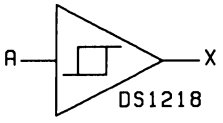
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.409	1.04	0.349	0.891

Rise/Fall time coefficients for the next cell

Schmitt Trigger

DS1218 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.123 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 9 array sites

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 600mV Min: 300mV

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.756	1.41	1.47	1.65
t_{PHL}		0.841	1.57	1.64	1.84

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.569	1.17
t_{PHL}		0.730	0.695

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

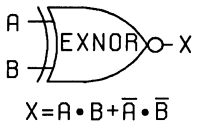
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.380	2.57	0.453	0.652

Rise/Fall time coefficients for the next cell

EXNOR

2–Input Exclusive NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.092 M_{CHL} = 0.296
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.898	1.68	1.75	1.97
t_{PHL}		0.648	1.23	1.28	1.44
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.516	2.15
t_{PHL}		0.380	0.899

Delay coefficients

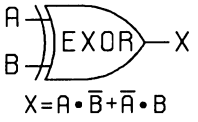
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.630	5.04	0.290	1.67

Rise/Fall time coefficients for the next cell

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.027 M_{CHL} = 0.113
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.764	1.43	1.49	1.67
t_{PHL}		0.365	0.690	0.719	0.808
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.407	2.16
t_{PHL}		0.175	0.892

Delay coefficients

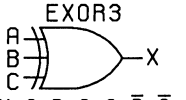
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.646	5.03	0.269	1.70

Rise/Fall time coefficients for the next cell

3–Input Exclusive OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.354 M_{CHL} = 0.476
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 14 array sites



$X=A\bullet B\bullet C+A\bullet\overline{B}\bullet\overline{C}$
$+\overline{A}\bullet B\bullet\overline{C}+\overline{A}\bullet\overline{B}\bullet C$

FUNCTION TABLE

A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.10	2.08	2.16	2.43
t_{PHL}		1.02	1.93	2.02	2.27
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.598	2.20
t_{PHL}		0.664	0.965

Delay coefficients

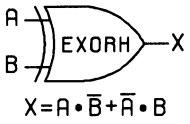
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.369	5.03	0.399	1.57

Rise/Fall time coefficients for the next cell

2–Input Exclusive OR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.061 M_{CHL} = 0.141
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.50 gates, 9 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.824	1.54	1.61	1.81
t_{PHL}		0.858	1.61	1.68	1.89
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.707	0.572
t_{PHL}		0.727	0.450

Delay coefficients

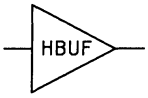
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.265	1.28	0.454	0.385

Rise/Fall time coefficients for the next cell

High Drive Noninverting Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.081 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.215 M_{CHL} = 0.403
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 6 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.505	0.958	0.999	1.12
t_{PHL}		0.702	1.34	1.40	1.57

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.366	0.305
t_{PHL}		0.496	0.232

Delay coefficients

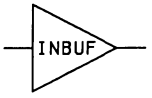
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.342	0.479	0.381	0.241

Rise/Fall time coefficients for the next cell

Noninverting Input Buffer

INBUF is used to buffer the signal from input and I/O pads, and is compatible with 1.4V & 300mV threshold voltage (V_{DD} = 5V). INBUF is tested using V_{IL} = 0.8V and V_{IH} = 2.0V.



Inputs: A
Outputs: X
Input Cap.: A: 0.204 pF
Timing Constants: K = 2.00ns
M_{CLH} = 0.061 M_{CHL} = 0.076
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.25 gates, 6 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.678	1.27	1.32	1.48
t_{PHL}		0.923	1.72	1.80	2.01

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.588	0.561
t_{PHL}		0.850	0.455

Delay coefficients

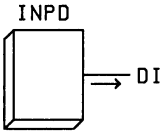
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.270	1.25	0.457	0.440

Rise/Fall time coefficients for the next cell

Input Pad

INPD is used with INBUF, or one of the Schmitt Triggers. Note that the input buffer and the chip package will add additional capacitance to all inputs.



Inputs: PAD
Outputs: DI
Input Cap.: PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.0ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	PAD to DI	0.002	0.003	0.004	0.004
t_{PHL}		0.002	0.003	0.004	0.004
Input tr,tf are zero since a rise/fall time of 5 ns (worst case commercial) is incorporated in the delay coefficients.					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	PAD to DI	0.001	0.005
t_{PHL}		0.001	0.005

Delay coefficients

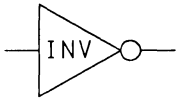
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.081 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.243 M_{CHL} = 0.194
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 0.50 gates, 2 array sites



(Input t_r,t_f= 0.5ns nominal, C_L = 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.390	0.745	0.777	0.874
t_{PHL}		0.239	0.459	0.479	0.539

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.096	1.20
t_{PHL}		0.062	0.595

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

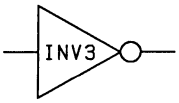
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.144	2.66	0.055	1.09

Rise/Fall time coefficients for the next cell

INV3

Inverter (3X Drive)

INV3 has 3 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.243 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.237 M_{CHL} = 0.171
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.256	0.494	0.516	0.581
t_{PHL}		0.166	0.322	0.336	0.379

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.089	0.422
t_{PHL}		0.062	0.201

Delay coefficients

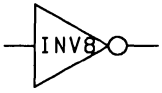
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.124	0.903	0.044	0.434

Rise/Fall time coefficients for the next cell

Inverter (8X Drive)

INV8 has 8 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.648 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.313 M_{CHL} = 0.190
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.00 gates, 9 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.248	0.485	0.506	0.571
t_{PHL}		0.153	0.299	0.312	0.352

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.091	0.160
t_{PHL}		0.061	0.077

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.120	0.353	0.053	0.165

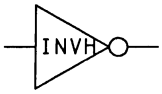
Rise/Fall time coefficients for the next cell

INVH

Inverter (High Drive)

INVH has 3 times the drive of an INV.

Inputs: A
Outputs: X
Input Cap.: A: 0.324 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.283 M_{CHL} = 0.175
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.260	0.505	0.527	0.594
t_{PHL}		0.161	0.312	0.326	0.367

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.090	0.319
t_{PHL}		0.063	0.151

Delay coefficients

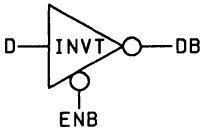
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.107	0.697	0.052	0.335

Rise/Fall time coefficients for the next cell

Tristate Inverter

INVT inverts the input signal when ENB is low. When ENB is high the output is in a Hi–Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: D: 0.162
ENB: 0.159 pF
Output Cap.: DB: 0.115 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.059 M_{CHL} = 0.186
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 6 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to DB	0.511	0.958	0.999	1.12
t_{PHL}		0.315	0.601	0.627	0.705
t_{PLH}	ENB to DB	0.387	0.726	0.757	0.850
t_{PHL}		0.418	0.794	0.828	0.931

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to DB	0.314	1.08
t_{PHL}		0.164	0.456
t_{PLH}	ENB to DB	0.188	1.09
t_{PHL}		0.267	0.458

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

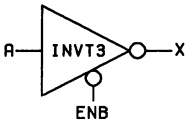
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DB	0.426	2.51	0.289	0.772

Rise/Fall time coefficients for the next cell

INVT3

Tristate Inverter (3X Drive)

INVT3 is a high drive tristate inverter with 3 times the drive of an INVT and a larger intrinsic delay. INVT3 inverts the input signal when ENB is low. When ENB is high the output is in a HI-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: All: 0.081 pF
Output Cap.: X: 0.197 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.340 M_{CHL} = 0.138
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 14 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.861	1.63	1.70	1.91
t_{PHL}		0.762	1.43	1.49	1.68
t_{PLH}	ENB to X	0.838	1.59	1.66	1.86
t_{PHL}		0.978	1.83	1.91	2.15

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.650	0.427
t_{PHL}		0.650	0.338
t_{PLH}	ENB to X	0.625	0.436
t_{PHL}		0.865	0.341

Delay coefficients

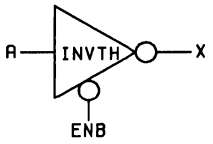
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.409	0.647	0.336	0.338

Rise/Fall time coefficients for the next cell

Tristate Inverter (High Drive)

INVTH is a high drive tristate inverter with 2 times the drive of an INVT and a smaller intrinsic delay. The input signal is inverted when ENB is low. When ENB is high the output is in a HI-Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: All: 0.081 pF
Output Cap.: X: 0.115 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.287 M_{CHL} = 0.228
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.50 gates, 12 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.843	1.59	1.66	1.87
t_{PHL}		0.771	1.46	1.52	1.71
t_{PLH}	ENB to X	0.825	1.56	1.63	1.83
t_{PHL}		0.987	1.86	1.94	2.18

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.624	0.614
t_{PHL}		0.608	0.421
t_{PLH}	ENB to X	0.606	0.614
t_{PHL}		0.825	0.412

Delay coefficients

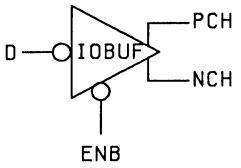
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.349	1.15	0.323	0.470

Rise/Fall time coefficients for the next cell

Input/Output Buffer

IOBUF is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi–Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.379 M_{CHL} = 0.254
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 7.50 gates, 18 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	0.974	1.84	1.92	2.16
t_{PHL}		1.22	2.29	2.39	2.68
t_{PLH}	D to NCH	1.06	2.01	2.09	2.35
t_{PHL}		0.882	1.66	1.74	1.95
t_{PLH}	ENB to PCH	0.970	1.84	1.92	2.15
t_{PHL}		1.43	2.69	2.81	3.15
t_{PLH}	ENB to NCH	1.09	2.05	2.14	2.41
t_{PHL}		0.846	1.60	1.67	1.87

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	0.766	0.306
t_{PHL}		1.06	0.302
t_{PLH}	D to NCH	0.844	0.367
t_{PHL}		0.733	0.266
t_{PLH}	ENB to PCH	0.758	0.327
t_{PHL}		1.27	0.320
t_{PLH}	ENB to NCH	0.868	0.365
t_{PHL}		0.697	0.264

Delay coefficients

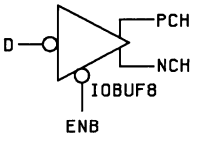
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.473	0.431	0.414	0.216
PCH	0.399	0.474	0.524	0.331

Rise/Fall time coefficients for the next cell

Input/Output Buffer (8X Drive)

IOBUF8 is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi–Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.379 M_{CHL} = 0.241
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 14.00 gates, 32 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	1.36	2.56	2.67	3.00
t_{PHL}		1.39	2.60	2.71	3.05
t_{PLH}	D to NCH	1.63	3.06	3.19	3.59
t_{PHL}		1.31	2.46	2.57	2.88
t_{PLH}	ENB to PCH	1.09	2.06	2.15	2.42
t_{PHL}		1.27	2.39	2.49	2.80
t_{PLH}	ENB to NCH	1.60	3.01	3.14	3.53
t_{PHL}		1.18	2.22	2.31	2.60

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	1.17	0.178
t_{PHL}		1.26	0.122
t_{PLH}	D to NCH	1.44	0.175
t_{PHL}		1.19	0.143
t_{PLH}	ENB to PCH	0.903	0.182
t_{PHL}		1.15	0.129
t_{PLH}	ENB to NCH	1.41	0.203
t_{PHL}		1.05	0.156

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

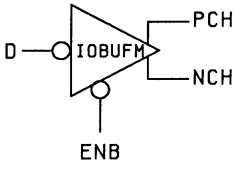
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.439	0.174	0.397	0.118
PCH	0.373	0.273	0.429	0.084

Rise/Fall time coefficients for the next cell

IOBUFM

Input/Output Buffer (Medium Drive)

IOBUFM is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.208
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.50 gates, 14 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	D to PCH	0.865	1.63	1.69	1.90
t_{PHL}		0.974	1.83	1.91	2.15
t_{PLH}	D to NCH	0.911	1.71	1.78	2.00
t_{PHL}		0.749	1.41	1.47	1.66
t_{PLH}	ENB to PCH	0.841	1.58	1.65	1.85
t_{PHL}		1.17	2.19	2.28	2.56
t_{PLH}	ENB to NCH	0.916	1.72	1.79	2.01
t_{PHL}		0.695	1.31	1.37	1.54

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to PCH	0.710	0.559
t_{PHL}		0.813	0.462
t_{PLH}	D to NCH	0.754	0.570
t_{PHL}		0.600	0.387
t_{PLH}	ENB to PCH	0.684	0.572
t_{PHL}		1.00	0.459
t_{PLH}	ENB to NCH	0.759	0.569
t_{PHL}		0.547	0.381

Delay coefficients

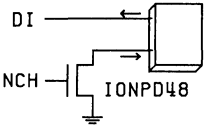
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
NCH	0.318	1.20	0.298	0.451
PCH	0.309	1.18	0.374	0.532

Rise/Fall time coefficients for the next cell

48mA Open Drain Input/Output Pad

IONPD48 is used to form a bidirectional pad that can drive output data, or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 8.094
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.163
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 2 pad sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	201	375	391	439
t_{PHL}		0.480	0.908	0.947	1.06

Timing characteristics

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	34.2	3.34
t_{PHL}		0.062	0.007

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	65.7	22.0	0.075	0.009
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

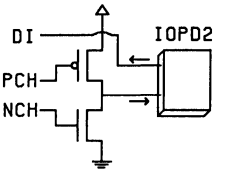
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

2mA Input/Output Pad

IOPD2 is used to form a bidirectional pad that can drive output data or be put in a Hi–Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.475
PCH: 0.354
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.214
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	6.89	12.9	13.4	15.1
t_{PHL}		7.77	14.5	15.1	17.0

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.477	0.127
t_{PHL}		0.483	0.144

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.57	0.521	0.553	0.184
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

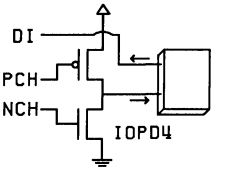
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Input/Output Pad

IOPD4 is used to form a bidirectional pad that can drive output data, or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.876
PCH: 0.701
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.219
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	3.50	6.54	6.82	7.65
t_{PHL}		3.96	7.41	7.73	8.67

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.282	0.063
t_{PHL}		0.271	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.805	0.260	0.289	0.092
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

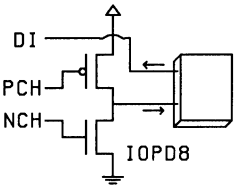
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Input/Output Pad

IOPD8 is used to form a bidirectional pad that can drive data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 1.678
PCH: 1.395
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.213 M_{CHL} = 0.216
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.87	3.51	3.66	4.11
t_{PHL}		2.06	3.86	4.03	4.52

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.183	0.032
t_{PHL}		0.170	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.418	0.130	0.154	0.046
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

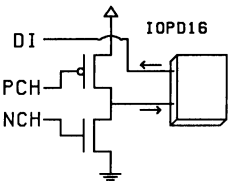
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Input/Output Pad

IOPD16 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 2.881
PCH: 2.436
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.205 M_{CHL} = 0.193
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.13	2.11	2.20	2.48
t_{PHL}		1.22	2.30	2.40	2.69

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.139	0.018
t_{PHL}		0.143	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.250	0.074	0.122	0.026
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

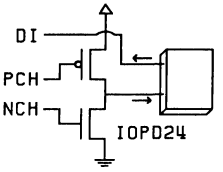
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Input/Output Pad

IOPD24 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selecti on and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH, PAD
Outputs: PAD, DI
Input Cap.: NCH: 4.084
PCH: 3.477
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.152 M_{CHL} = 0.220
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.835	1.57	1.64	1.84
t_{PHL}		0.916	1.73	1.80	2.02

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.121	0.013
t_{PHL}		0.124	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.182	0.052	0.119	0.018
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

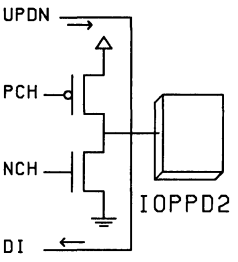
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

IOPPD2

2mA Input/Output Pad with Pullup/Pulldown Port

IOPPD2 is similar to IOPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.475
PCH: 0.354
UPDN: 52.500
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.204
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	6.93	12.9	13.5	15.1
t_{PHL}		7.81	14.6	15.2	17.1

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.515	0.127
t_{PHL}		0.527	0.144

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.73	0.521	0.605	0.184
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

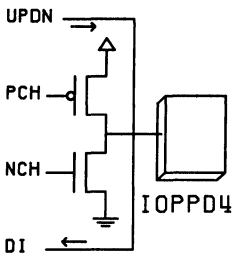
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

IOPPD4

4mA Input/Output Pad with Pullup/Pulldown Port

IOPPD4 is similar to IOPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 0.876
PCH: 0.701
UPDN: 52.500
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.208
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	3.52	6.58	6.86	7.69
t_{PHL}		3.98	7.45	7.76	8.71

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.301	0.063
t_{PHL}		0.294	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.885	0.260	0.316	0.092
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

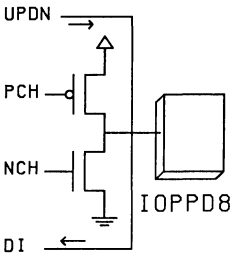
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Input/Output Pad with Pullup/Pulldown Port

IOPPD8 is similar to IOPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 1.678
PCH: 1.395
UPDN: 52.500
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.213 M_{CHL} = 0.213
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.88	3.53	3.68	4.13
t_{PHL}		2.07	3.88	4.05	4.54

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.192	0.032
t_{PHL}		0.183	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.460	0.130	0.165	0.046
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

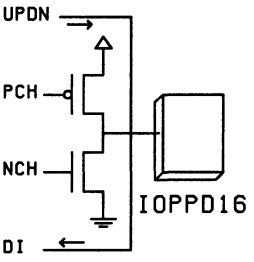
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

IOPPD16

16mA Input/Output Pad with Pullup/Pulldown Port

IOPPD16 is similar to IOPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 2.881
PCH: 2.436
UPDN: 52.500
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.204 M_{CHL} = 0.196
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.13	2.12	2.21	2.49
t_{PHL}		1.22	2.29	2.39	2.68

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.144	0.018
t_{PHL}		0.138	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.274	0.074	0.113	0.026
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

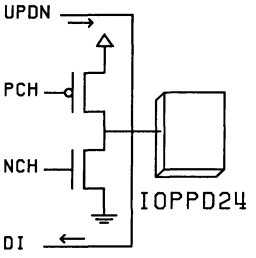
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Input/Output Pad with Pullup/Pulldown Port

IOPPD24 is similar to IOPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN, PAD
Outputs: PAD, DI
Input Cap.: NCH: 4.084
PCH: 3.477
UPDN: 52.500
PAD: 5.497 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.152 M_{CHL} = 0.222
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.839	1.58	1.64	1.85
t_{PHL}		0.921	1.74	1.81	2.03

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.125	0.013
t_{PHL}		0.128	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.197	0.052	0.125	0.018
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

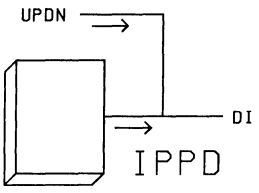
(Worst Case Process, V_{DD} =4.5V, T_A =70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD} −0.5V	−12.00	mA

DC specifications

Input Pad with Pullup/Pulldown Port

IPPD is similar to INPD but includes an input port, UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See any PPU/PPD data sheet for pullup/pulldown current information.



Inputs: PAD, UPDN
Outputs: DI
Input Cap.: PAD: 5.497
UPDN: 52.500 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	PAD to DI	0.001	0.005
t_{PHL}		0.001	0.005

Delay coefficients

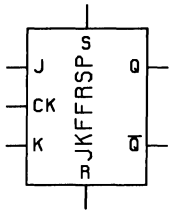
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DI	2.14	0.000	2.14	0.000

Rise/Fall time coefficients for the next cell

J–K Flip–Flop with Reset and Set, Positive Edge Triggered

JKFFRSP is a fully static JK–type edge triggered flip–flop. It is positive edge triggered with respect to CK. S and R are asynchronous and active high.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK, J, K: 0.081
S, R: 0.201 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.231 M_{CHL} = 0.224
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 12.50 gates, 33 array sites

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB_o	Q_o
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q_o	QB_o
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

* Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	2.10	3.93	4.10	4.60
t_{PHL}		1.82	3.42	3.56	4.00
t_{PLH}	CK to QB	1.38	2.59	2.70	3.03
t_{PHL}		1.67	3.12	3.26	3.66
t_{PHL}	R to Q	1.22	2.29	2.39	2.68
t_{PLH}	R to QB	0.766	1.45	1.51	1.69
t_{PHL}		1.77	3.31	3.45	3.88
t_{PLH}	S to Q	0.569	1.08	1.13	1.26
t_{PHL}		0.781	1.47	1.54	1.73
t_{PHL}	S to QB	1.96	3.68	3.83	4.30

Timing characteristics

JKFFRSP

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	1.82	1.13
t_{PHL}		1.61	0.766
t_{PLH}	CK to QB	1.09	1.18
t_{PHL}		1.40	1.10
t_{PHL}	R to Q	1.00	0.754
t_{PLH}	R to QB	0.480	1.18
t_{PHL}		1.50	1.10
t_{PLH}	S to Q	0.281	1.20
t_{PHL}		0.565	0.763
t_{PHL}	S to QB	1.69	1.10

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

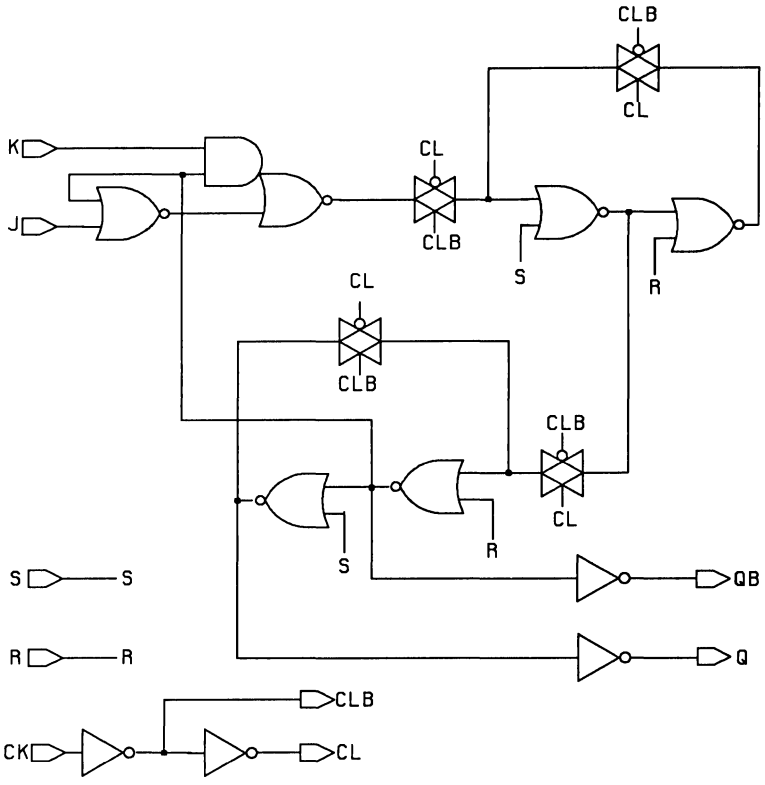
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.277	2.54	0.380	0.956
QB	0.284	2.56	0.722	1.13

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time J to CK	2.16	1.27	0.773
t_{su}	Setup Time K to CK	2.16	1.27	0.773
t_h	Hold Time CK to J	−1.187	−0.696	−0.425
t_h	Hold Time CK to K	−1.187	−0.696	−0.425
t_{pwh}	Pulse Width (high) CK	4.32	2.53	1.55
t_{pwh}	Pulse Width (high) S	3.73	2.19	1.34
t_{pwh}	Pulse Width (high) R	3.14	1.84	1.12
t_{pwl}	Pulse Width (low) CK	4.51	2.65	1.62
rt	Recovery Time S	1.77	1.04	0.633
rt	Recovery Time R	−0.853	−0.500	−0.306

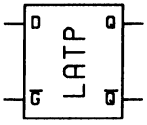
Timing requirements



Functional diagram: JKFFRSP

Transparent Latch, Positive Edge Triggered

LATP holds data when GB is high and is transparent when GB is low.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.314 M_{CHL} = 0.319
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.50 gates, 12 array sites

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q$_o$	QB$_o$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.09	2.06	2.14	2.41
t_{PHL}		1.40	2.63	2.74	3.08
t_{PLH}	GB to QB	1.77	3.32	3.46	3.89
t_{PHL}		1.28	2.41	2.51	2.82
t_{PLH}	D to Q	0.833	1.58	1.64	1.85
t_{PHL}		1.09	2.05	2.14	2.40
t_{PLH}	D to QB	1.41	2.65	2.77	3.11
t_{PHL}		1.02	1.93	2.01	2.26

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.768	1.19
t_{PHL}		1.13	0.854
t_{PLH}	GB to QB	1.46	1.10
t_{PHL}		1.04	0.634
t_{PLH}	D to Q	0.511	1.19
t_{PHL}		0.816	0.861
t_{PLH}	D to QB	1.09	1.15
t_{PHL}		0.787	0.633

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

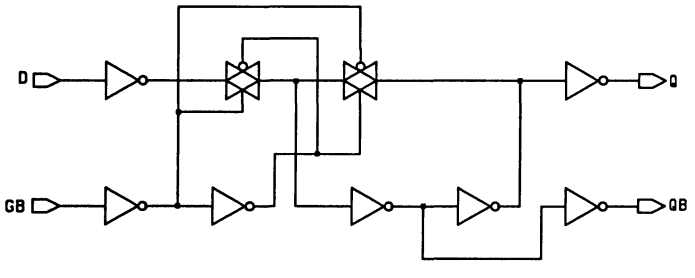
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.291	2.54	0.475	0.980
QB	0.296	2.51	0.355	0.833

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.19	0.700	0.428
t_h	Hold Time GB to D	−0.341	−0.200	−0.122
t_{pwl}	Pulse Width (low) GB	3.93	2.30	1.41

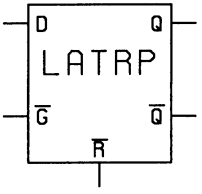
Timing requirements



Functional diagram: LATP

Transparent Latch with Reset, Positive Edge Triggered

LATRP holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. For a faster version of this cell, see LATRPF.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.123
D, GB: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.449 M_{CHL} = 0.352
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.25 gates, 15 array sites

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.28	2.42	2.52	2.83
t_{PHL}		1.51	2.84	2.96	3.33
t_{PLH}	GB to QB	1.90	3.57	3.73	4.19
t_{PHL}		1.43	2.69	2.80	3.15
t_{PLH}	D to Q	1.06	2.01	2.10	2.36
t_{PHL}		1.18	2.22	2.31	2.60
t_{PLH}	D to QB	1.58	2.99	3.11	3.50
t_{PHL}		1.20	2.27	2.37	2.66
t_{PLH}	RB to Q	0.984	1.87	1.95	2.19
t_{PHL}		0.758	1.44	1.50	1.69
t_{PLH}	RB to QB	1.10	2.08	2.17	2.44
t_{PHL}		1.12	2.12	2.21	2.49

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.891	1.24
t_{PHL}		1.22	0.867
t_{PLH}	GB to QB	1.53	1.14
t_{PHL}		1.17	0.665
t_{PLH}	D to Q	0.678	1.21
t_{PHL}		0.888	0.874
t_{PLH}	D to QB	1.22	1.11
t_{PHL}		0.954	0.630
t_{PLH}	RB to Q	0.595	1.25
t_{PHL}		0.494	0.726
t_{PLH}	RB to QB	0.724	1.16
t_{PHL}		0.871	0.653

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.342	2.52	0.410	1.01
QB	0.248	2.56	0.308	0.914

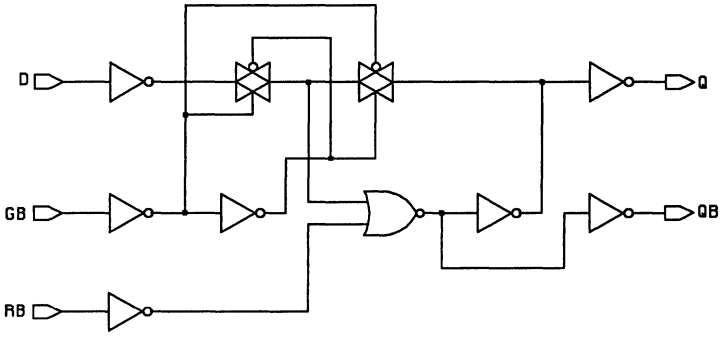
Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.19	0.700	0.428
t_h	Hold Time GB to D	−0.512	−0.300	−0.183
t_{pwl}	Pulse Width (low) RB	3.34	1.96	1.19
t_{pwl}	Pulse Width (low) GB	3.93	2.30	1.41
rt	Recovery Time RB	1.54	0.900	0.550

Timing requirements

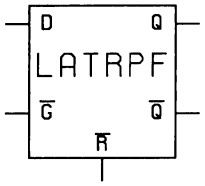
LATRP



Functional diagram: LATRP

Fast Transparent Latch with Reset, Positive Edge Triggered

LATRPF holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.123
D: 0.081
GB: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.296 M_{CHL} = 0.299
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.75 gates, 13 array sites

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.14	2.14	2.23	2.51
t_{PHL}		1.24	2.33	2.43	2.73
t_{PLH}	GB to QB	1.57	2.95	3.08	3.46
t_{PHL}		1.32	2.49	2.60	2.92
t_{PLH}	D to Q	0.972	1.83	1.91	2.15
t_{PHL}		1.28	2.41	2.51	2.82
t_{PLH}	D to QB	1.62	3.04	3.17	3.56
t_{PHL}		1.15	2.17	2.26	2.54
t_{PLH}	RB to Q	0.971	1.83	1.91	2.15
t_{PHL}		0.822	1.56	1.62	1.82
t_{PLH}	RB to QB	1.14	2.14	2.23	2.51
t_{PHL}		1.15	2.17	2.26	2.54

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.812	1.25
t_{PHL}		0.972	0.879
t_{PLH}	GB to QB	1.26	1.13
t_{PHL}		1.10	0.628
t_{PLH}	D to Q	0.644	1.27
t_{PHL}		1.01	0.888

Delay coefficients (Sheet 1 of 2)

LATRPF

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	D to QB	1.31	1.15
t_{PHL}		0.918	0.663
t_{PLH}	RB to Q	0.644	1.27
t_{PHL}		0.578	0.741
t_{PLH}	RB to QB	0.826	1.17
t_{PHL}		0.919	0.659

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

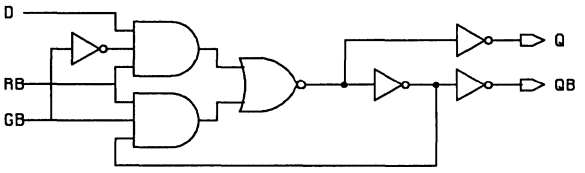
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.360	2.54	0.514	0.886
QB	0.306	2.50	0.361	0.849

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.96	1.15	0.702
t_h	Hold Time GB to D	−0.683	−0.400	−0.244
t_{pwl}	Pulse Width (low) RB	3.14	1.84	1.12
t_{pwl}	Pulse Width (low) GB	3.93	2.30	1.41
rt	Recovery Time RB	1.71	1.00	0.611

Timing requirements

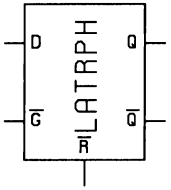


Functional diagram: LATRPF

D Latch with Reset and Enable (High Drive)

LATRPH holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.

Inputs: D, GB, RB
Outputs: Q, QB
Input Cap.: D, GB: 0.081
RB: 0.123 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.376 M_{CHL} = 0.314
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.25 gates, 16 array sites



FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	GB to Q	1.24	2.34	2.44	2.74
t_{PHL}		1.53	2.87	2.99	3.36
t_{PLH}	GB to QB	2.05	3.85	4.01	4.50
t_{PHL}		1.57	2.95	3.08	3.45
t_{PLH}	D to Q	1.02	1.93	2.01	2.26
t_{PHL}		1.19	2.25	2.35	2.63
t_{PLH}	D to QB	1.71	3.23	3.36	3.78
t_{PHL}		1.32	2.49	2.59	2.91
t_{PLH}	RB to Q	0.962	1.82	1.90	2.14
t_{PHL}		0.741	1.41	1.47	1.65
t_{PLH}	RB to QB	1.20	2.26	2.36	2.65
t_{PHL}		1.26	2.38	2.48	2.78

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	GB to Q	0.974	0.682
t_{PHL}		1.30	0.585
t_{PLH}	GB to QB	1.80	0.528
t_{PHL}		1.38	0.371
t_{PLH}	D to Q	0.759	0.632
t_{PHL}		0.972	0.557
t_{PLH}	D to QB	1.48	0.496

Delay coefficients (Sheet 1 of 2)

LATRPH

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}		1.13	0.381
t_{PLH}	RB to Q	0.697	0.669
t_{PHL}		0.535	0.465
t_{PLH}	RB to QB	0.954	0.528
t_{PHL}		1.06	0.415

Delay coefficients (Sheet 2 of 2)

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

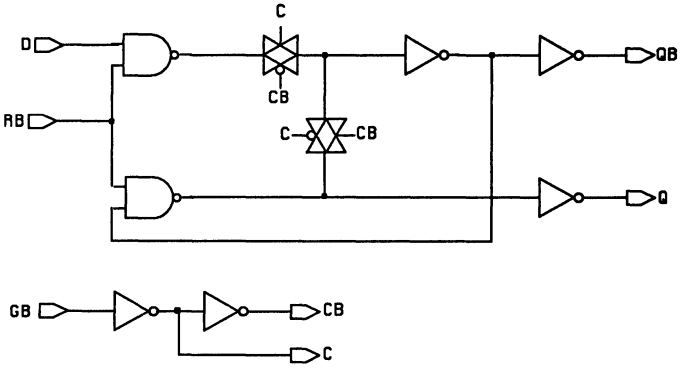
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.409	1.20	0.468	0.553
QB	0.331	1.20	0.397	0.391

Rise/Fall time coefficients for the next cell

Minimum Specifications (ns)

SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to GB	1.57	0.920	0.563
t_h	Hold Time GB to D	-0.853	-0.500	-0.306
t_{pwl}	Pulse Width (low) GB	4.32	2.53	1.55
t_{pwl}	Pulse Width (low) RB	3.53	2.07	1.27
rt	Recovery Time RB	1.71	1.00	0.611

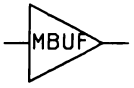
Timing requirements



Functional diagram: LATRPH

Medium Drive Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.125 M_{CHL} = 0.171
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.420	0.793	0.827	0.929
t_{PHL}		0.503	0.951	0.992	1.11

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.274	0.586
t_{PHL}		0.377	0.338

Delay coefficients

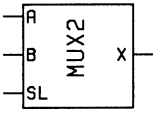
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.220	1.23	0.301	0.424

Rise/Fall time coefficients for the next cell

2–Input Multiplexer

Inputs: SL, A, B
Outputs: X
Input Cap.: SL: 0.162
A, B: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.254 M_{CHL} = 0.187
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.749	1.42	1.48	1.66
t_{PHL}		0.883	1.66	1.73	1.94
t_{PLH}	SL to X	0.894	1.69	1.76	1.98
t_{PHL}		0.861	1.62	1.69	1.90
* Slowest of A or B inputs					

Timing characteristics

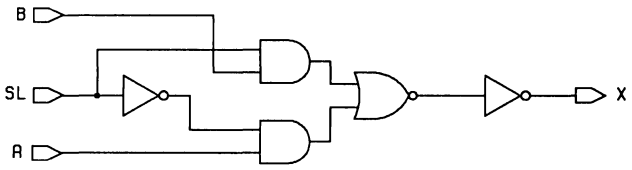
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.458	1.15
t_{PHL}		0.686	0.738
t_{PLH}	SL to X	0.603	1.15
t_{PHL}		0.660	0.767

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.255	2.55	0.382	0.940

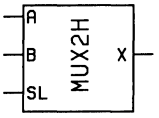
Rise/Fall time coefficients for the next cell



Functional diagram: MUX2

2–Input Multiplexer (High Drive)

Inputs: A, SL, B
Outputs: X
Input Cap.: A: 0.081
SL: 0.162
B: 0.081 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.173 M_{CHL} = 0.101
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.50 gates, 8 array sites



FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.683	1.29	1.34	1.51
t_{PHL}		0.900	1.69	1.76	1.97
t_{PLH}	SL to X	0.829	1.56	1.63	1.83
t_{PHL}		0.880	1.65	1.72	1.93
* Slowest of A or B inputs					

Timing characteristics

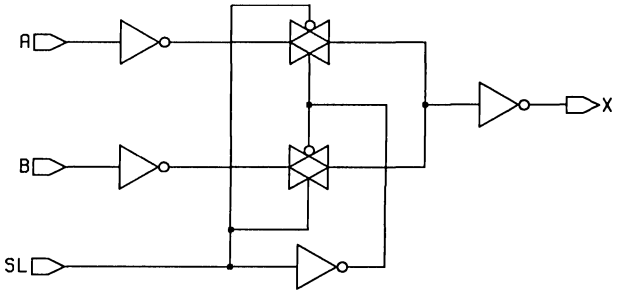
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.518	0.578
t_{PHL}		0.778	0.499
t_{PLH}	SL to X	0.659	0.609
t_{PHL}		0.757	0.505

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.339	1.19	0.471	0.475

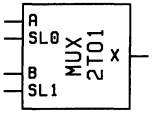
Rise/Fall time coefficients for the next cell



Functional diagram: MUX2H

2–Input Multiplexer with Separate Selects

In normal operation, SL1 and SL0 are complementary signals and X = A when SL0 is high and X = B when SL1 is high.



Inputs: SL1, SL0, A, B
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.086 M_{CHL} = 0.098
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 7 array sites

FUNCTION TABLE

SL1	SL0	X
L	L	L
L	H	A
H	L	B
H	H	A + B

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A,B to X	0.715	1.34	1.40	1.57
t_{PHL}		0.756	1.42	1.48	1.66
t_{PLH}	SL1,SL0 to X	0.672	1.26	1.31	1.47
t_{PHL}		0.857	1.61	1.67	1.88

Timing characteristics

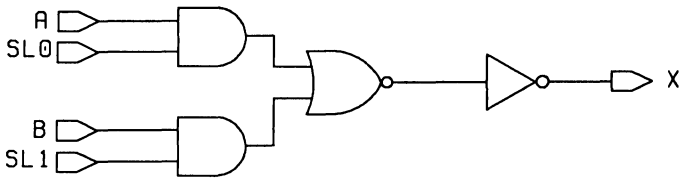
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A,B to X	0.492	1.17
t_{PHL}		0.599	0.721
t_{PLH}	SL1,SL0 to X	0.451	1.15
t_{PHL}		0.698	0.735

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.266	2.55	0.348	0.961

Rise/Fall time coefficients for the next cell

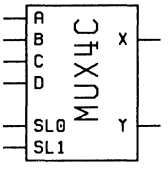


Functional diagram: MUX2TO1

4–Input Multiplexer with Complementary Outputs

SL0 and SL1 cause one of A, B, C, or D to be propagated to the outputs.

Inputs: A, B, C, D, SL0, SL1
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.258 M_{CHL} = 0.221
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.00 gates, 21 array sites



FUNCTION TABLE

SL0	SL1	X	Y
L	L	A	$\overline{A}$
H	L	B	$\overline{B}$
L	H	C	$\overline{C}$
H	H	D	$\overline{D}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.950	1.79	1.87	2.10
t_{PHL}		1.21	2.28	2.38	2.67
t_{PLH}	*IN to Y***	1.75	3.31	3.45	3.87
t_{PHL}		1.35	2.55	2.66	2.99
t_{PLH}	**SL to X	1.34	2.51	2.62	2.94
t_{PHL}		1.16	2.19	2.28	2.56
t_{PLH}	**SL to Y	1.70	3.21	3.35	3.76
t_{PHL}		1.73	3.27	3.41	3.83

* Slowest of A,B,C, or D inputs
** SL timing applies to both SL0 and SL1
*** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

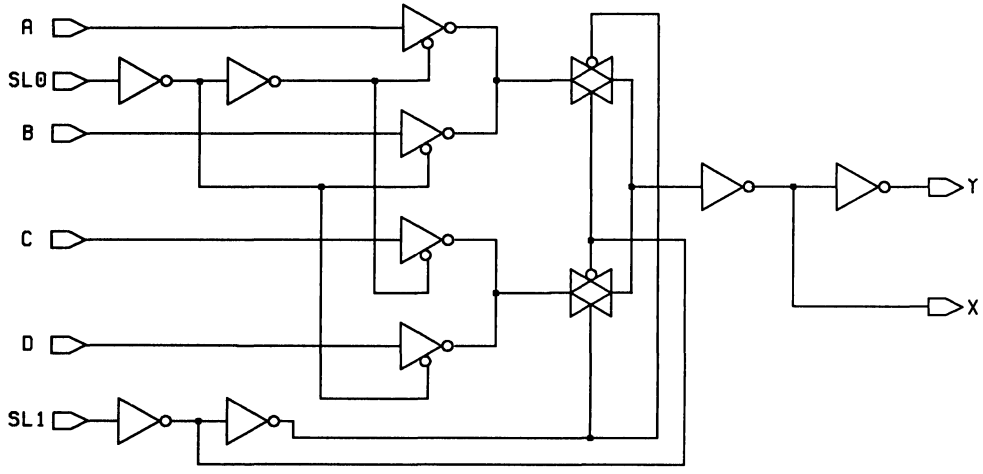
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.653	1.18
t_{PHL}		0.994	0.800
t_{PLH}	X to Y (IN)	0.184	1.19
t_{PHL}		0.117	0.603
t_{PLH}	**SL to X	1.04	1.16
t_{PHL}		0.933	0.859
t_{PLH}	X to Y (SL)	0.184	1.19
t_{PHL}		0.117	0.603

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.510	2.54	0.559	0.980
Y	0.307	2.50	0.340	0.841

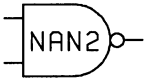
Rise/Fall time coefficients for the next cell



Functional diagram: MUX4C

2–Input NAND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.188 M_{CHL} = 0.112
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.00 gate, 3 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.445	0.844	0.881	0.990
t_{PHL}		0.317	0.600	0.626	0.703
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.177	1.18
t_{PHL}		0.129	0.882

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.256	2.69	0.143	1.71

Rise/Fall time coefficients for the next cell

2–Input NAND Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.186 M_{CHL} = 0.154
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.518	0.980	1.02	1.15
t_{PHL}		0.381	0.723	0.754	0.847
t_{PLH}	*IN to Y**	0.814	1.54	1.61	1.81
t_{PHL}		0.876	1.66	1.73	1.95

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.251	1.18
t_{PHL}		0.176	0.880
t_{PLH}	X to Y	0.158	1.18
t_{PHL}		0.128	0.639

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

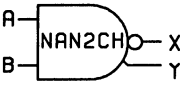
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.478	2.71	0.270	1.69
Y	0.183	2.64	0.256	0.949

Rise/Fall time coefficients for the next cell

NAN2CH

2–Input NAND Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.204 M_{CHL} = 0.148
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.437	0.830	0.866	0.974
t_{PHL}		0.312	0.593	0.618	0.695
t_{PLH}	*IN to Y**	0.638	1.22	1.27	1.43
t_{PHL}		0.709	1.35	1.41	1.58

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.259	0.578
t_{PHL}		0.180	0.437
t_{PLH}	X to Y	0.167	0.578
t_{PHL}		0.122	0.354

Delay coefficients

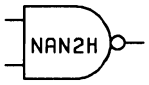
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.497	1.33	0.275	0.825
Y	0.268	1.21	0.280	0.438

Rise/Fall time coefficients for the next cell

2–Input NAND Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.166 M_{CHL} = 0.115
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.334	0.635	0.663	0.745
t_{PHL}		0.252	0.478	0.498	0.560
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.168	0.603
t_{PHL}		0.133	0.439

Delay coefficients

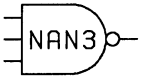
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.238	1.37	0.188	0.809

Rise/Fall time coefficients for the next cell

3–Input NAND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.171 M_{CHL} = 0.035
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.503	0.950	0.991	1.11
t_{PHL}		0.430	0.806	0.840	0.943
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.240	1.19
t_{PHL}		0.232	1.15

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.414	2.66	0.236	2.39

Rise/Fall time coefficients for the next cell

3–Input NAND Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.199 M_{CHL} = 0.046
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.592	1.12	1.17	1.31
t_{PHL}		0.494	0.925	0.965	1.08
t_{PLH}	*IN to Y**	1.04	1.96	2.04	2.30
t_{PHL}		0.886	1.67	1.74	1.96

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.319	1.18
t_{PHL}		0.291	1.15
t_{PLH}	X to Y	0.215	1.17
t_{PHL}		0.145	0.649

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.650	2.64	0.429	2.34
Y	0.253	2.57	0.293	0.921

Rise/Fall time coefficients for the next cell

3–Input NAND Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.179 M_{CHL} = 0.060
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.407	0.772	0.805	0.905
t_{PHL}		0.332	0.624	0.651	0.731
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.235	0.603
t_{PHL}		0.213	0.588

Delay coefficients

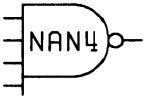
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.424	1.32	0.244	1.19

Rise/Fall time coefficients for the next cell

4–Input NAND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.186 M_{CHL} = 0.058
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.565	1.07	1.11	1.25
t_{PHL}		0.583	1.09	1.14	1.28
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.293	1.21
t_{PHL}		0.327	1.45

Delay coefficients

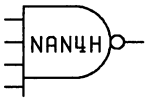
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.540	2.68	0.395	3.02

Rise/Fall time coefficients for the next cell

4–Input NAND Gate (High Drive)

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.202 M_{CHL} = 0.001
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.00 gates, 9 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.477	0.905	0.944	1.06
t_{PHL}		0.455	0.850	0.886	0.994
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.296	0.603
t_{PHL}		0.342	0.705

Delay coefficients

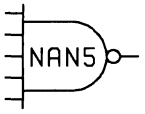
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.569	1.29	0.399	1.49

Rise/Fall time coefficients for the next cell

5–Input NAND Gate

Inputs: A, B, C, D, E
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.176 M_{CHL} = 0.028
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 6 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.611	1.15	1.20	1.35
t_{PHL}		0.749	1.40	1.46	1.64
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.340	1.23
t_{PHL}		0.462	1.72

Delay coefficients

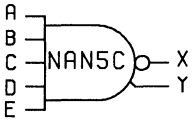
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.696	2.65	0.571	3.67

Rise/Fall time coefficients for the next cell

5–Input NAND Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.169 M_{CHL} = 0.029
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.696	1.31	1.37	1.54
t_{PHL}		0.844	1.58	1.64	1.85
t_{PLH}	*IN to Y**	1.55	2.90	3.02	3.39
t_{PHL}		0.974	1.83	1.91	2.15

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.431	1.21
t_{PHL}		0.557	1.72
t_{PLH}	X to Y	0.270	1.25
t_{PHL}		0.122	0.749

Delay coefficients

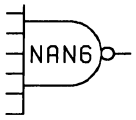
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.906	2.67	0.867	3.63
Y	0.402	2.46	0.400	0.882

Rise/Fall time coefficients for the next cell

6–Input NAND Gate

Inputs: A, B, C, D, E, F
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.020
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.654	1.23	1.28	1.44
t_{PHL}		0.942	1.76	1.83	2.06
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.387	1.25
t_{PHL}		0.613	2.00

Delay coefficients

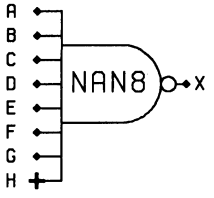
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.824	2.67	0.782	4.33

Rise/Fall time coefficients for the next cell

8–Input NAND Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.178 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.50 gates, 13 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A,B,C,D,E,F,G,H to X	1.01	1.90	1.98	2.22
t_{PHL}		1.17	2.18	2.27	2.55

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A,B,C,D,E,F,G,H to X	0.750	1.15
t_{PHL}		1.05	0.726

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.252	2.55	0.393	0.881

Rise/Fall time coefficients for the next cell

2–Input NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.059 M_{CHL} = 0.154
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.00 gate, 3 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.641	1.20	1.25	1.41
t_{PHL}		0.256	0.489	0.510	0.574
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.270	2.16
t_{PHL}		0.096	0.596

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.356	5.07	0.187	1.03

Rise/Fall time coefficients for the next cell

NOR2C

2–Input NOR Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.057 M_{CHL} = 0.156
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.792	1.48	1.55	1.74
t_{PHL}		0.289	0.549	0.573	0.645
t_{PLH}	*IN to Y**	0.643	1.21	1.27	1.42
t_{PHL}		1.27	2.38	2.48	2.78

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.425	2.15
t_{PHL}		0.128	0.594
t_{PLH}	X to Y	0.146	1.18
t_{PHL}		0.122	0.719

Delay coefficients

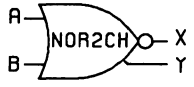
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.795	5.03	0.248	1.03
Y	0.198	2.60	0.368	0.892

Rise/Fall time coefficients for the next cell

2–Input NOR Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.069 M_{CHL} = 0.154
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.624	1.17	1.22	1.37
t_{PHL}		0.239	0.457	0.477	0.536
t_{PLH}	*IN to Y**	0.497	0.942	0.983	1.11
t_{PHL}		0.954	1.80	1.87	2.10

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.426	1.05
t_{PHL}		0.125	0.308
t_{PLH}	X to Y	0.146	0.591
t_{PHL}		0.089	0.433

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

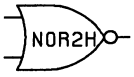
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.801	2.49	0.246	0.504
Y	0.216	1.24	0.339	0.474

Rise/Fall time coefficients for the next cell

NOR2H

2–Input NOR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.031 M_{CHL} = 0.172
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.460	0.861	0.898	1.01
t_{PHL}		0.210	0.405	0.422	0.475
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.275	1.08
t_{PHL}		0.088	0.313

Delay coefficients

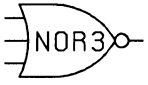
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.363	2.53	0.131	0.587

Rise/Fall time coefficients for the next cell

3–Input NOR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.016 M_{CHL} = 0.153
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gates, 4 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.03	1.92	2.00	2.24
t_{PHL}		0.271	0.517	0.540	0.607
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.516	3.15
t_{PHL}		0.108	0.620

Delay coefficients

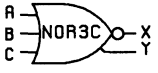
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.752	7.43	0.241	1.04

Rise/Fall time coefficients for the next cell

3–Input NOR Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.112 M_{CHL} = 0.197
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.12	2.10	2.19	2.46
t_{PHL}		0.296	0.567	0.591	0.666
t_{PLH}	*IN to Y**	0.654	1.24	1.30	1.46
t_{PHL}		1.89	3.55	3.70	4.15

* Slowest input
** The propagation delay from IN to Y depends on the IN to X delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.572	3.13
t_{PHL}		0.119	0.591
t_{PLH}	X to Y	0.133	1.19
t_{PHL}		0.155	0.805

Delay coefficients

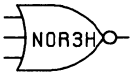
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.36	7.38	0.224	1.03
Y	0.164	2.64	0.419	0.995

Rise/Fall time coefficients for the next cell

3–Input NOR Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.188
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.772	1.44	1.50	1.69
t_{PHL}		0.229	0.440	0.459	0.517
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.520	1.58
t_{PHL}		0.096	0.335

Delay coefficients

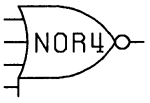
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.754	3.72	0.165	0.611

Rise/Fall time coefficients for the next cell

4–Input NOR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.166
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.52	2.83	2.95	3.31
t_{PHL}		0.285	0.543	0.567	0.638
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.855	4.14
t_{PHL}		0.113	0.639

Delay coefficients

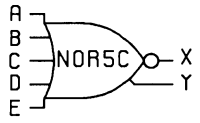
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.31	9.78	0.263	1.08

Rise/Fall time coefficients for the next cell

5–Input NOR Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.127 M_{CHL} = 0.014
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.50 gates, 9 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to Y	0.650	1.22	1.27	1.43
t_{PHL}		1.97	3.67	3.83	4.30
t_{PLH}	*IN to X**	2.52	4.71	4.91	5.51
t_{PHL}		0.875	1.64	1.71	1.92

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to Y	0.404	1.21
t_{PHL}		1.80	1.02
t_{PLH}	Y to X	0.254	1.16
t_{PHL}		0.119	0.594

Delay coefficients

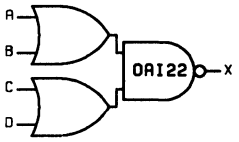
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.279	2.54	0.279	0.860
Y	0.425	2.64	0.786	1.09

Rise/Fall time coefficients for the next cell

2–2 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.109 M_{CHL} = 0.142
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



$X = \overline{(A+B) \cdot (C+D)}$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.711	1.33	1.39	1.56
t_{PHL}		0.357	0.675	0.704	0.792
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.319	2.16
t_{PHL}		0.154	0.893

Delay coefficients

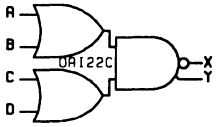
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.448	5.08	0.273	1.69

Rise/Fall time coefficients for the next cell

2–2 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.085 M_{CHL} = 0.080
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 8 array sites



$X = \overline{(A+B) \cdot (C+D)}$

$Y = (A+B) \cdot (C+D)$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to Y	0.718	1.35	1.40	1.58
t_{PHL}		0.821	1.54	1.60	1.80
t_{PLH}	*IN to X**	1.23	2.31	2.41	2.70
t_{PHL}		0.990	1.86	1.94	2.18

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to Y	0.496	1.17
t_{PHL}		0.668	0.745
t_{PLH}	Y to X	0.177	1.17
t_{PHL}		0.108	0.628

Delay coefficients

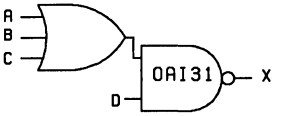
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.253	2.56	0.342	0.821
Y	0.455	2.57	0.459	0.975

Rise/Fall time coefficients for the next cell

3–1 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.089
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



$X = \overline{(A+B+C) \cdot D}$

(Input t_r, t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	1.23	2.29	2.39	2.68
t_{PHL}		0.391	0.735	0.767	0.861
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.724	3.15
t_{PHL}		0.208	0.907

Delay coefficients

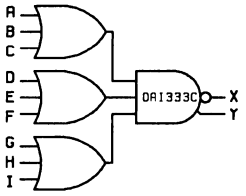
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	1.05	7.40	0.321	1.69

Rise/Fall time coefficients for the next cell

3–3–3 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.142 M_{CHL} = 0.064
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.50 gates, 13 array sites



$$X = \overline{(A+B+C) * (D+E+F) * (G+H+I)}$$

$$Y = (A+B+C) * (D+E+F) * (G+H+I)$$

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to Y	1.38	2.58	2.69	3.02
t_{PHL}		2.10	3.93	4.09	4.59
t_{PLH}	*IN to X**	2.71	5.07	5.29	5.93
t_{PHL}		1.66	3.11	3.25	3.64

* Slowest input
** The propagation delay from IN to X depends on the IN to Y delay and rise/fall time. See the Timing Equation application note for more information.

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to Y	1.13	1.20
t_{PHL}		1.88	1.21
t_{PLH}	Y to X	0.253	1.18
t_{PHL}		0.124	0.616

Delay coefficients

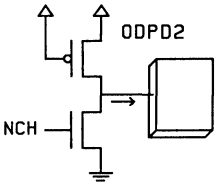
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.316	2.53	0.299	0.898
Y	0.631	2.49	1.05	1.22

Rise/Fall time coefficients for the next cell

2mA 5V Open–Drain Output Pad

ODPD2 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.475 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.192
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	172	322	335	376
t_{PHL}		7.75	14.5	15.1	16.9

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	10.2	3.24
t_{PHL}		0.415	0.145

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	58.3	22.0	0.506	0.187

Rise/Fall time coefficients for the next cell

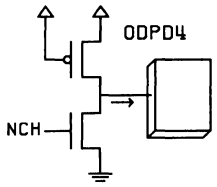
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

4mA 5V Open–Drain Output Pad

ODPD4 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.876 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.196
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	175	327	341	382
t_{PHL}		3.91	7.30	7.61	8.54

Timing characteristics

NOTE:
The TPLH shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	12.1	3.26
t_{PHL}		0.223	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	58.3	22.0	0.261	0.093

Rise/Fall time coefficients for the next cell

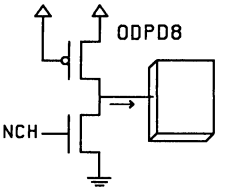
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

8mA 5V Open–Drain Output Pad

ODPD8 is an inverting open-drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.678 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.220
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	179	333	348	390
t_{PHL}		2.02	3.79	3.95	4.43

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	14.8	3.28
t_{PHL}		0.129	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	58.3	22.0	0.145	0.046

Rise/Fall time coefficients for the next cell

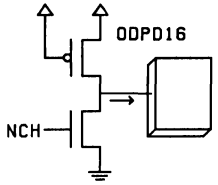
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

16mA 5V Open–Drain Output Pad

ODPD16 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.881 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.159
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	183	341	356	399
t_{PHL}		1.17	2.20	2.29	2.57

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	18.5	3.29
t_{PHL}		0.104	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	58.3	22.0	0.105	0.026

Rise/Fall time coefficients for the next cell

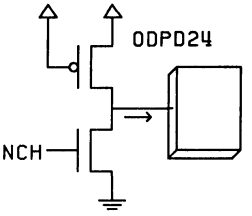
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

24mA 5V Open–Drain Output Pad

ODPD24 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 4.084 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.180
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	187	348	363	407
t_{PHL}		0.871	1.64	1.71	1.92

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	21.7	3.30
t_{PHL}		0.095	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	58.3	22.0	0.103	0.018

Rise/Fall time coefficients for the next cell

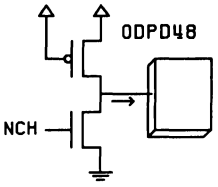
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

48mA 5V Open–Drain Output Pad

ODPD48 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 8.094 pF
Output Cap.: PAD: 8.064 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.153
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.00 gates, 2 pad sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	207	386	402	451
t_{PHL}		0.491	0.928	0.968	1.09

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	40.0	3.33
t_{PHL}		0.077	0.007

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	117	22.0	0.114	0.009

Rise/Fall time coefficients for the next cell

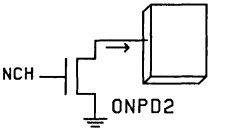
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

2mA 7V Open–Drain Output Pad

ONPD2 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.475 pF
Output Cap.: PAD: 3.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.182
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	169	316	329	369
t_{PHL}		7.55	14.1	14.7	16.5

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	7.03	3.24
t_{PHL}		0.226	0.145

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	29.6	22.0	0.288	0.187

Rise/Fall time coefficients for the next cell

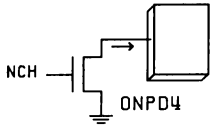
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

4mA 7V Open–Drain Output Pad

ONPD4 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.876 pF
Output Cap.: PAD: 3.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.175
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	172	321	334	375
t_{PHL}		3.80	7.11	7.42	8.32

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	8.84	3.26
t_{PHL}		0.131	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	29.6	22.0	0.151	0.093

Rise/Fall time coefficients for the next cell

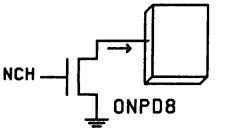
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

DC specifications

8mA 7V Open–Drain Output Pad

ONPD8 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.678 pF
Output Cap.: PAD: 3.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.178
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	175	327	341	383
t_{PHL}		1.96	3.67	3.83	4.30

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	11.5	3.28
t_{PHL}		0.086	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	29.6	22.0	0.090	0.046

Rise/Fall time coefficients for the next cell

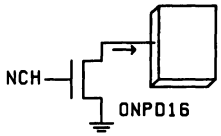
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

16mA 7V Open–Drain Output Pad

ONPD16 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 2.881 pF
Output Cap.: PAD: 3.094 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.183
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	180	335	349	392
t_{PHL}		1.15	2.16	2.25	2.53

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	15.2	3.29
t_{PHL}		0.072	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	29.6	22.0	0.053	0.026

Rise/Fall time coefficients for the next cell

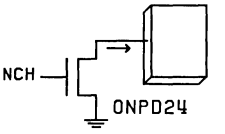
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

24mA 7V Open–Drain Output Pad

ONPD24 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 4.084 pF
Output Cap.: PAD: 3.094 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.171
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH to PAD	183	342	357	400
t_{PHL}		0.850	1.60	1.67	1.87

Timing characteristics

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH to PAD	18.3	3.30
t_{PHL}		0.078	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	29.6	22.0	0.068	0.018

Rise/Fall time coefficients for the next cell

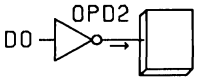
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

2mA Output Pad

OPD2 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 0.836 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.216
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	6.85	12.8	13.3	15.0
t_{PHL}		7.73	14.4	15.1	16.9

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.439	0.127
t_{PHL}		0.439	0.144

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.42	0.521	0.499	0.184

Rise/Fall time coefficients for the next cell

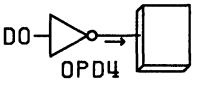
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Output Pad

OPD4 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 1.584 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.158 M_{CHL} = 0.228
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	3.48	6.51	6.78	7.61
t_{PHL}		3.94	7.38	7.69	8.63

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.263	0.063
t_{PHL}		0.248	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.729	0.260	0.260	0.092

Rise/Fall time coefficients for the next cell

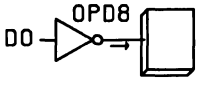
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Output Pad

OPD8 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 3.080 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.212 M_{CHL} = 0.215
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	1.86	3.49	3.64	4.09
t_{PHL}		2.05	3.84	4.00	4.49

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.173	0.032
t_{PHL}		0.158	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.378	0.130	0.142	0.046

Rise/Fall time coefficients for the next cell

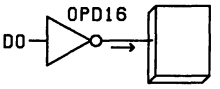
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Output Pad

OPD16 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 5.324 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.205 M_{CHL} = 0.191
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	1.12	2.10	2.19	2.46
t_{PHL}		1.22	2.29	2.38	2.68

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.133	0.018
t_{PHL}		0.137	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.225	0.074	0.113	0.026

Rise/Fall time coefficients for the next cell

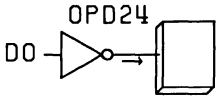
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Output Pad

OPD24 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 7.568 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.152 M_{CHL} = 0.219
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	DO to PAD	0.831	1.56	1.63	1.83
t_{PHL}		0.912	1.72	1.79	2.01

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	DO to PAD	0.117	0.013
t_{PHL}		0.120	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.167	0.052	0.114	0.018

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

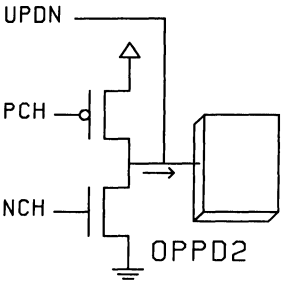
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}−0.5V	−12.00	mA

DC specifications

2mA Tristate Output Pad with Pullup/Pulldown Port

OPPD2 is similar to OTPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.

Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 0.475
PCH: 0.354
UPDN: 52.500 pF
Output Cap.: PAD: 5.504 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.214
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site



(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	6.89	12.9	13.4	15.1
t_{PHL}		7.77	14.5	15.1	17.0

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.477	0.127
t_{PHL}		0.483	0.144

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.57	0.521	0.553	0.184

Rise/Fall time coefficients for the next cell

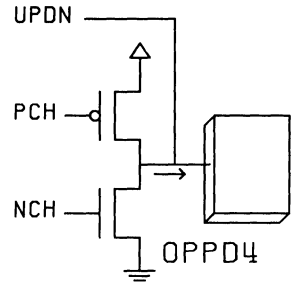
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad with Pullup/Pulldown Port

OPPD4 is similar to OTPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 0.876
PCH: 0.701
UPDN: 52.500 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.219
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	3.50	6.54	6.82	7.65
t_{PHL}		3.96	7.41	7.73	8.67

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.282	0.063
t_{PHL}		0.271	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.805	0.260	0.289	0.092

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

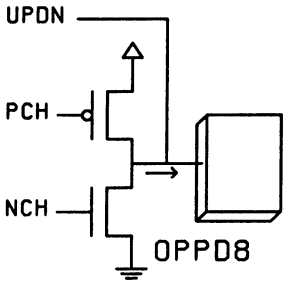
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad with Pullup/Pulldown Port

OPPD8 is similar to OTPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.

Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 1.678
PCH: 1.395
UPDN: 52.500 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.213 M_{CHL} = 0.216
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site



(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.87	3.51	3.66	4.11
t_{PHL}		2.06	3.86	4.03	4.52

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.183	0.032
t_{PHL}		0.170	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.418	0.130	0.154	0.046

Rise/Fall time coefficients for the next cell

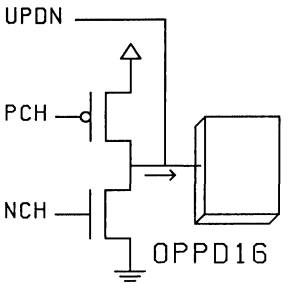
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Tristate Output Pad with Pullup/Pulldown Port

OPPD16 is similar to OTPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 2.881
PCH: 2.436
UPDN: 52.500 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.205 M_{CHL} = 0.193
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.13	2.11	2.20	2.48
t_{PHL}		1.22	2.30	2.40	2.69

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.139	0.018
t_{PHL}		0.143	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.250	0.074	0.122	0.026

Rise/Fall time coefficients for the next cell

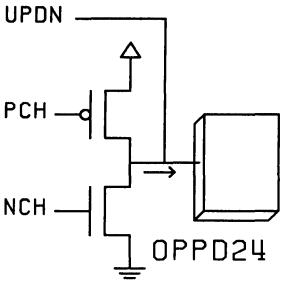
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Tristate Output Pad with Pullup/Pulldown Port

OPPD24 is similar to OTPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 4.084
PCH: 3.477
UPDN: 52.500 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.152 M_{CHL} = 0.220
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.835	1.57	1.64	1.84
t_{PHL}		0.916	1.73	1.80	2.02

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.121	0.013
t_{PHL}		0.124	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.182	0.052	0.119	0.018

Rise/Fall time coefficients for the next cell

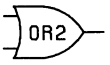
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

2–Input OR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.090 M_{CHL} = 0.119
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.50 gate, 4 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.496	0.933	0.972	1.09
t_{PHL}		0.699	1.31	1.37	1.54
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.269	1.18
t_{PHL}		0.535	0.713

Delay coefficients

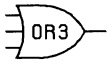
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.198	2.60	0.368	0.892

Rise/Fall time coefficients for the next cell

3–Input OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.114 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.536	1.01	1.05	1.18
t_{PHL}		1.00	1.87	1.95	2.19
* Slowest input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.299	1.18
t_{PHL}		0.872	0.806

Delay coefficients

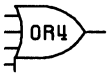
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.204	2.61	0.451	0.963

Rise/Fall time coefficients for the next cell

4–Input OR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.159 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 6 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.573	1.08	1.13	1.27
t_{PHL}		1.43	2.67	2.79	3.13
* Slowest Input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.315	1.20
t_{PHL}		1.29	0.910

Delay coefficients

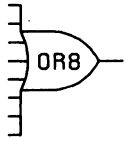
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.220	2.61	0.562	1.05

Rise/Fall time coefficients for the next cell

8–Input OR Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: All: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.146 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 12 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*IN to X	0.628	1.18	1.23	1.38
t_{PHL}		1.51	2.82	2.94	3.30
* Slowest Input					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*IN to X	0.375	1.20
t_{PHL}		1.35	1.02

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.342	2.63	0.571	1.54

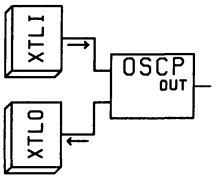
Rise/Fall time coefficients for the next cell

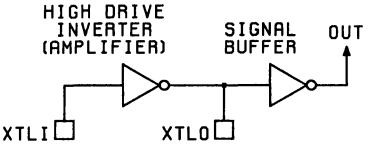
General Purpose Oscillator – Free Placement

- 1* to 50 MHz operation
- 35% to 65% output duty cycle
- Buffered on-chip output
- Typical gm = 80 mA/V

Inputs: XTLI
Outputs: OUT, XTLO
Input Cap.: XTLI: 11.633 pF
Output Cap.: XTLO: 7.307 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.25 gates, 2 pad sites
Kit Part: Culebra 2

*See important note on last page of this data sheet regarding operation below 3 MHz.





OSCFP functional diagram

OSCFP is a general purpose crystal oscillator cell capable of operation from 1 MHz* to over 50 MHz. Fundamental mode applications require one or two external resistors and two external tuning capacitors. Operation above 25 MHz usually requires a third overtone crystal and additional components to form a frequency selective circuit. A parallel resonant type crystal should always be specified.

The OSCFP is built from any two I/O pad cells and therefore may be located at any two adjacent pad locations; however, both pads must be on the same side of the chip. (Contact your NCR applications engineer for more information.) Preferred locations are near the center of any side of the packaged part to minimize bond wire and lead frame parasitics. This is especially important in DIP packages. It is also desirable to place power (V_{DD}) and ground (V_{SS}) pins near the oscillator especially at frequencies above 25 MHz. A short ground trace must be used from the V_{SS} pin(s) to the external tuning capacitors C_1 and C_2.

To drive external circuits with an oscillator generated clock, the on-chip oscillator output (OUT) should drive a buffer and a separate output pad such as an OPD4. The oscillator output, XTLO, should not normally be used to drive external circuits except the oscillator components.

Figures 1 and 2 show the external components required to bias the inverter and for the crystal pi network. R_B causes the inverter to self bias to approximately $V_{DD}/2$. This is a point where the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B is chosen in the range of 1–20 MΩ such that it will not affect the AC performance of the circuit.

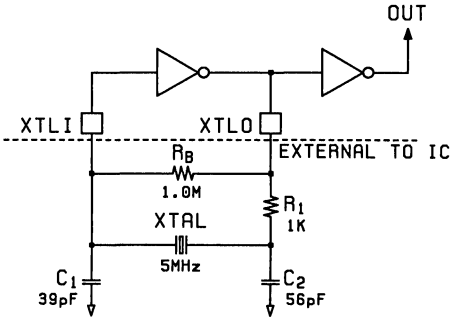


Figure 1 Typical fundamental mode circuit

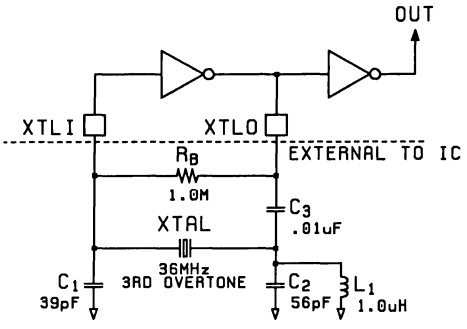


Figure 2 Typical third overtone circuit

C_1 and C_2 along with the crystal forms a pi network which resonates at the specified crystal frequency. The ratio C_2/C_1 should be somewhat greater than unity since it is a term in the loop gain equation. Increasing the ratio too much will cause the voltage swing on XTLI to exceed the supply rails which is undesirable. Typically $1.1 < (C_2/C_1) < 1.5$. The series combination of C_2 and C_1 should be approximately equal to the *load capacitance* specified for the quartz crystal. The strays associated with each node, and the oscillator input and output capacitance should be included in calculations which involve C_2 and C_1. Typical component values are shown in Figures 1 and 2.

Example calculation:

$C_{1\ total}$ = Input C + parasitic C + C_1
= 11.63 + 5.0 + 39 = 55.63 pF

$C_{2\ total}$ = Output C + parasitic C + C_2
= 7.31 + 5.0 + 56 = 68.31 pF

$C_{2\ total} / C_{1\ total} = 1.23$

C_{LOAD} = (55.63 x 68.31) / (55.63 + 68.31)
= 30.7 pF

An exact analysis would need to include the effect of R_1 between the oscillator output and the crystal. The method shown is a reasonable approximation. The crystal load capacitance can be specified as 32 pF which is the closest standard value. Components can also be chosen to match a 20 pF load capacitance crystal.

The output resistance of the oscillator core, along with C_2, forms an RC low pass circuit. This pole contributes additional phase shift to insure a greater than 360 degree phase shift around the loop, which is required for oscillation. At lower oscillator frequencies, it may be necessary to add a resistor, R_1, in series with the output to add phase shift at a lower frequency and insure oscillator startup and stability. This is most important in the 1–20 MHz region. Typical values for R_1 are shown in Table 2. At frequencies above 25 MHz, R_1 can usually be omitted. R_1 also reduces the drive to the crystal and thus crystal power dissipation.

To achieve overtone oscillation, the fundamental frequency must be suppressed by making the loop gain lower at the fundamental frequency compared to the third harmonic frequency. An overtone crystal will resonate at its fundamental frequency unless the loop gain is forced to be higher at the harmonic frequency. Loop gain must be less than one at the fundamental and greater than one at the desired overtone frequency.

The additional components necessary for overtone operation are a coupling capacitor and an inductor. The coupling capacitor is simply a DC block so the inductor does not short the inverter output to ground. In some cases a resistor in the range of 50–100 ohms in series with C_3 will improve waveform symmetry. The inductor, L_1, is selected such that its impedance lowers the loop gain at the fundamental frequency relative to the third harmonic. The resonant frequency of the circuit made up of C_2 and L_1 is set midway between the fundamental and third overtone frequency. This causes the equivalent impedance to look inductive at the fundamental and capacitive at the third overtone frequency. The equivalent capacitance of C_2 and L_1 in parallel at the third overtone is used to calculate C_2 total at the output node. The NCR Oscillator Application Note covers the calculations in greater detail. Some experimentation with component values should be anticipated prior to specifying final production values.

The XTLI input can be driven with an external source with XTLO left unconnected. The maximum operating frequency is no longer 50 MHz but is determined by the load on XTLO, which is several picofarads even when the package pin is not connected. The reason for this is that as an oscillator, C_2 is part of the resonant pi circuit so it does not look like a pure load capacitance as it does when the

inverter is driven without the crystal. For simulation purposes, the XTLI to XTLO propagation delay is zero. In production test, the XTLO pin will be driven with the complement of the XTLI test signal. This is transparent to the designer. Any application of the oscillator cell in which the input is driven should be first reviewed with an NCR applications engineer.

The OSCFP is a Pierce type oscillator circuit in which the crystal is operated in its parallel resonant mode. (Refer to the crystal equivalent circuit - Figure 3.) At parallel resonance, the LRC leg appears slightly inductive and resonates with C_0 and the circuit load capacitances, C_1 and C_2. Typical equivalent circuit component values are shown in Table 1. The values should only be used as a guideline in selecting a crystal for your application. The RMAX column, however, should be adhered to when specifying a crystal. It will insure a quality crystal which will resonate in a circuit using the OSCFP.

The basic equation which governs the minimum g_m required for oscillation is as follows:

$$g_m(min)=(2\pi f)^2 C_{1\,total} {}^*C_{2\,total} {}^*R_m(1+C_o/C_L)^2$$

For reliable startup and operation the actual g_m should be at least twice that predicted by the above equation. The OSCFP will provide a minimum g_m of 50mA/V over worst case temperature and supply voltage. The conditions for oscillation should be met by choosing crystals which meet the maximum series resistance as shown in Table 1. A check can be made by working through the equation for minimum required g_m.

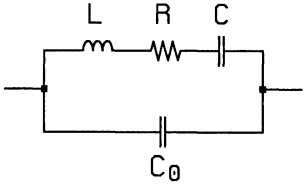


Figure 3 Crystal equivalent circuit

The graphs in Figures 4 and 5 shows maximum supply current as a function of frequency. It represents the maximum of measurements made using crystals from several different vendors. The typical component values shown in Table 2 and Figures 1 and 2 were used in the test circuit. The circuit shown in Figure 1 was used with fundamental mode crystals from 1 - 22 MHz. The circuit shown in Figure 2 was used for overtone measurements from 25 - 50 MHz.

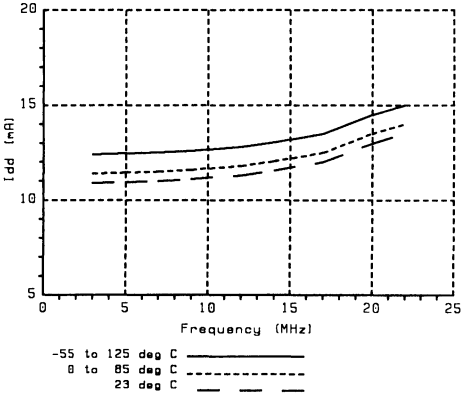


Figure 4 Maximum supply current versus frequency (fundamental)

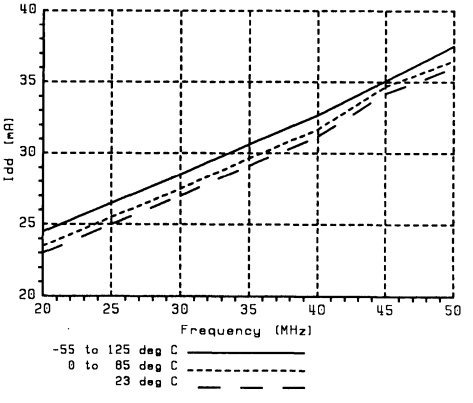


Figure 5 Maximum supply current versus frequency (third overtone)

(Input t_r,t_f= 0.0ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	XTLI to OUT	0.292	0.545	0.568	0.637
t_{PHL}		0.191	0.356	0.372	0.417

Switching characteristics

Crystal Frequency	L	C	C_0	R	R_{MAX}
1 MHz	3082 mH	8.223 fF	4.230 pF	575 Ω	650 Ω
2 MHz	987.4 mH	6.416 fF	3.105 pF	122 Ω	275 Ω
3 MHz	153.3 mH	18.38 fF	4.368 pF	35 Ω	200 Ω
5 MHz	56.36 mH	17.99 fF	4.451 pF	12 Ω	70 Ω
8 MHz	21.41 mH	18.48 fF	4.010 pF	9 Ω	40 Ω
10 MHz	10.64 mH	23.83 fF	5.998 pF	14 Ω	30 Ω
14.3 MHz	5.867 mH	21.06 fF	4.672 pF	6.3 Ω	30 Ω
20 MHz	3.042 mH	20.81 fF	5.310 pF	6.7 Ω	25 Ω
24 MHz	25.005 mH	1.762 fF	4.095 pF	19 Ω	50 Ω
36 MHz	13.321 mH	1.467 fF	6.88 pF	32 Ω	50 Ω
48 MHz	6.997 mH	1.571 fF	6.407 pF	23 Ω	50 Ω

TABLE 1 Typical measured crystal parameters (Represents several manufacturers' AT cut crystals)

Frequency	R1
1 MHz	2 K – 5 KΩ
3 MHz	2 KΩ
5 MHz	1 KΩ
10 MHz	500 Ω
20 MHz	200 Ω

TABLE 2 Typical values for R1 in Figure 1

Suggested References:

Crystal Oscillator Design And Temperature Compensation by Marvin Frerking

Design Of Crystal And Other Harmonic Oscillators by Benjamin Parzen

NCR ASIC Oscillator Application Note

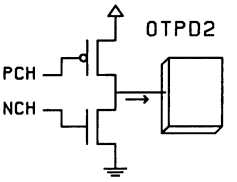
*NOTE REGARDING OPERATION AT LESS THAN 3 MHz:

Operation in the range from 1.0–2.9 MHz is discouraged due to limitations of many quartz crystals in that frequency range. The physical size of the quartz blank must be made smaller than the optimum in order to fit into a reasonable standard size package. The result is that non–harmonic modes may be present which vary with temperature and may cause the frequency of oscillation to shift. All modes other than the desired fundamental must be down at least 6 dB to insure oscillation at the correct frequency. This means that the equivalent series resistance of undesired modes must be twice that of the fundamental mode.

Most vendors show a 6 dB or better specification in their data sheets. In practice, non–harmonic modes have been observed to become the dominate mode (lowest resistance) as a function of temperature, sometimes over a range of only a few degrees centrigrade. For this reason, NCR recommends using a crystal above 2.9 MHz and dividing down to the desired frequency with on–chip flip–flops.

2mA Tristate Output Pad

OTPD2 is an output pad capable of output currents up to 2mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 0.475
PCH: 0.354 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.216
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	6.85	12.8	13.3	15.0
t_{PHL}		7.73	14.4	15.1	16.9

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.439	0.127
t_{PHL}		0.439	0.144

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	1.42	0.521	0.499	0.184

Rise/Fall time coefficients for the next cell

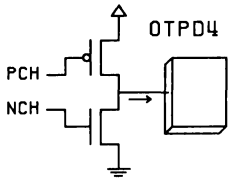
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad

OTPD4 is an output pad capable of output currents up to 4mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 0.876
PCH: 0.701 pF
Output Cap.: PAD: 5.504 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.158 M_{CHL} = 0.228
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	3.48	6.51	6.78	7.61
t_{PHL}		3.94	7.38	7.69	8.63

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.263	0.063
t_{PHL}		0.248	0.072

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.729	0.260	0.260	0.092

Rise/Fall time coefficients for the next cell

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

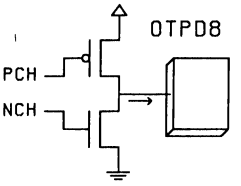
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

OTPD8

8mA Tristate Output Pad

OTPD8 is an output pad capable of output currents up to 8mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 1.678
PCH: 1.395 pF
Output Cap.: PAD: 5.504 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.212 M_{CHL} = 0.215
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.86	3.49	3.64	4.09
t_{PHL}		2.05	3.84	4.00	4.49

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.173	0.032
t_{PHL}		0.158	0.036

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.378	0.130	0.142	0.046

Rise/Fall time coefficients for the next cell

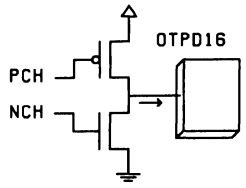
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}−0.5V	−4.00	mA

DC specifications

16mA Tristate Output Pad

OTPD16 is an output pad capable of output currents up to 16mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 2.881
PCH: 2.436 pF
Output Cap.: PAD: 5.504 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.205 M_{CHL} = 0.191
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	1.12	2.10	2.19	2.46
t_{PHL}		1.22	2.29	2.38	2.68

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.133	0.018
t_{PHL}		0.137	0.020

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.225	0.074	0.113	0.026

Rise/Fall time coefficients for the next cell

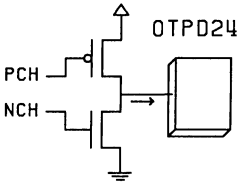
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Tristate Output Pad

OTPD24 is an output pad capable of output currents up to 24mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 4.084
PCH: 3.477 pF
Output Cap.: PAD: 5.504 pF
Timing
Constants: K = 0.08ns
M_{CLH} = 0.152 M_{CHL} = 0.219
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 5.00 gates, 1 pad site

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	NCH,PCH to PAD	0.831	1.56	1.63	1.83
t_{PHL}		0.912	1.72	1.79	2.01

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	NCH,PCH to PAD	0.117	0.013
t_{PHL}		0.120	0.014

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
PAD	0.167	0.052	0.114	0.018

Rise/Fall time coefficients for the next cell

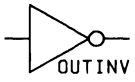
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

Output Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.324 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.283 M_{CHL} = 0.175
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.00 gates, 5 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.260	0.505	0.527	0.594
t_{PHL}		0.161	0.312	0.326	0.367

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.090	0.319
t_{PHL}		0.063	0.151

Delay coefficients

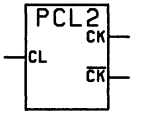
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.107	0.697	0.052	0.335

Rise/Fall time coefficients for the next cell

Two–Phase Clock

PCL2 is for use with clocked cells and to produce high drive signals of true and complement value. CK is the noninverted or true output and CKB is the inverted or complement output.



Inputs: CL
Outputs: CK, CKB
Input Cap.: CL: 0.162 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.244 M_{CHL} = 0.328
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 6.00 gates, 13 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CL to CK	0.507	0.963	1.00	1.13
t_{PHL}		0.671	1.27	1.33	1.50
t_{PLH}	CL to CKB	0.771	1.46	1.52	1.71
t_{PHL}		0.688	1.31	1.36	1.53

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CL to CK	0.358	0.288
t_{PHL}		0.494	0.244
t_{PLH}	CL to CKB	0.614	0.341
t_{PHL}		0.517	0.205

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

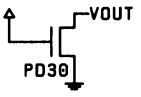
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
CK	0.288	0.539	0.381	0.241
CKB	0.443	0.371	0.281	0.234

Rise/Fall time coefficients for the next cell

30μA N–Channel Pulldown Device

PD30 is a weak n–channel pulldown that sinks 30μμA when VOUT equals five volts and can be used as a pulldown on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See the PPD200, PPD400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see Pullup and Pulldown Current Range Specifications application note.

This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.



* NOTE: The gate input on the PD30 cannot be used to turn the transistor on or off.

Inputs: VDDIN
Outputs: VOUT
Input Cap.: VDDIN: 0.000 pF
Output Cap.: VOUT: 0.136 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 9 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	*VOUT	1511	2821	2940	3299
* Timing is from VOUT = 5V to VOUT = 2.5V					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	*VOUT	1500	70.8

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

PD30

(V_{OUT}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	V_{DD}=5V, Nominal Process, 25°C	30μA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	10μA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	12μA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	18μA maximum
*Maximum supply current conditions for PD30.		

DC specifications

Power on Reset

Features

- No external components required
- Retriggerable reset under digital control
- Supply glitch immunity

POR is a digital cell that guarantees a logic low level during power up for the purpose of resetting logic elements to known states. Upon application of the positive supply voltage to the device, POR causes SYS to remain low for approximately 5µs after the positive supply has exceeded 3.4V. This insures that all digital circuits are operational before the SYS output goes high. An additional input is supplied to the cell which allows the output to be retriggered under external control.

FUNCTION TABLE

V_{DD}	RES	SYS
↑	L	⌐¬
X	H	L
H	↓	⌐¬

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	RES to SYS	4676	8730	9100	10210
t_{PHL}		3.97	7.41	7.72	8.66

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	RES to SYS	4675	10.9
t_{PHL}		3.51	2.86

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
SYS	39.2	0.256	1.37	5.63

Rise/Fall time coefficients for the next cell

PARAMETER	CONDITIONS	RATING
Supply Current	Nominal Process, V_{DD} = 5V, V_{RES} = 0V, T_A = 25° C	250µA typical
V_{DD} trigger voltage	Nominal Process, T_A = 25° C	3.4V nominal

DC specifications

Application Notes

Reset Timing

The POR cell is not designed for applications requiring precise reset intervals. The duration of the SYS output pulse in a power up condition, or after an external reset input, may vary from the nominal specified timing by 30% or more. Further variations in pulse duration will be observed over varying conditions of supply voltage and temperature. For applications requiring precise timing of a reset signal, an approach utilizing a clocked counter chain is recommended.

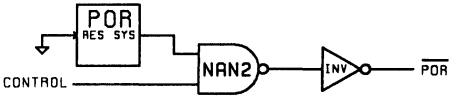
No relationship exists between the POR SYS output pulse and the start up time of any crystal oscillator in the NCR standard cell library. In general, the multi-megahertz oscillator cell, OSCFP, will require anywhere from 1ms to 20ms to reach stable operation after power is applied.

POR provides a certain degree of input glitch immunity. The table given below describes the various situations and responses under typical conditions.

CONDITIONS	RESPONSE
* Glitch-free supply RAMP * Supply glitch settles to V_{DD} = 3.4V for at least 25ns * Supply glitch settles to 3.4V > V_{DD} ≥ 2.7V for at least 10ns	SYS output high occurs 4.7µs after V_{DD} reaches 3.4V. Note: V_{SYS} tracks V_{DD}.
* Supply glitch settles to V_{DD} ≥ 3.4V * Supply glitch settles to V_{DD} = 2.7V for less than 10ns	Will not effect SYS output of POR

Testability

NCR requires the chip be simulated and tested with the reset time out feature of the POR disabled. To achieve this, the RESET input on the POR should be grounded, and the POR output should be ANDed with a control signal (NAN2 and INV - see figure below). The control signal should be accessible by the tester during test time at probe and after the chip is packaged. A static pullup may be connected to the control signal path to enable the reset circuit under normal operation. NCR will review the specific implementation of any circuit using the POR at the time of the design review.



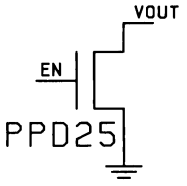
Reset circuit

System Considerations

The NCR POR cell is designed to provide a reset pulse that can be used throughout the chip. If this signal is brought off chip for a system reset, precautions should be taken to insure that all other chips are powered up and functional while the reset pulse is valid.

25μA N–Channel Pulldown Device

PPD25 is a weak n–channel pulldown that sinks 25μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.042 pF
Output Cap.: VOUT: 0.128 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.75 gates, 8 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	7206	13452	14023	15733

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	47.4	143

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

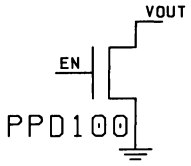
(V_{EN}=5V, V_{OUT}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	V_{DD}=5V, Nominal Process, 25°C*	25µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	10µA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	12µA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	18µA maximum
*Maximum supply current conditions for PPD25.		

DC specifications

100μA N–Channel Pulldown Device

PPD100 is a weak n-channel pulldown that sinks 100μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.042 pF
Output Cap.: VOUT: 0.128 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 8 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	1983	3702	3859	4330

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	122	37.2

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

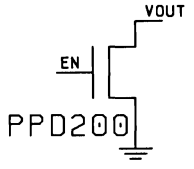
(V_{EN}=5V, V_{OUT}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	V_{DD}=5V, Nominal Process, 25°C	100µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	10µA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	12µA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	18µA maximum
* Maximum supply current conditions for PPD100.		

DC specifications

200μA N–Channel Pulldown Device

PPD200 is a weak n–channel pulldown that sinks 200μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.084 pF
Output Cap.: VOUT: 0.138 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.75 gates, 9 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	1232	2301	2398	2691

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	201	20.6

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

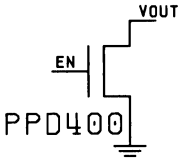
(V_{EN}=5V, V_{OUT}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	V_{DD}=5V, Nominal Process, 25°C	200µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	10µA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	12µA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	18µA maximum
* Maximum supply current conditions for PPD200.		

DC specifications

400μA N–Channel Pulldown Device

PPD400 is a weak n–channel pulldown that sinks 400μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.042 pF
Output Cap.: VOUT: 0.132 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.25 gates, 8 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	457	853	889	998

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.001	9.14

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

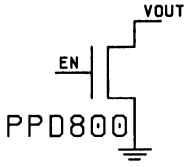
(V_{EN}=5V, V_{OUT}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	V_{DD}=5V, Nominal Process, 25°C	400µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	10µA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	12µA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	18µA maximum
*Maximum supply current conditions for PPD400.		

DC specifications

800μA N–Channel Pulldown Device

PPD800 is a weak n–channel pulldown that sinks 800μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.042 pF
Output Cap.: VOUT: 0.136 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.175
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.25 gates, 10 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	241	451	470	527

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.102	4.83

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

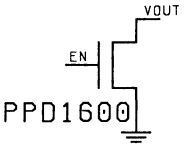
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	800μA typical

DC specifications

1600μA N–Channel Pulldown Device

PPD1600 is a weak n–channel pulldown that sinks 1600μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pulldown on internal tristate bus lines. If used this way, timing effects of the current sink on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.084 pF
Output Cap.: VOUT: 0.136 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.156
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.75 gates, 8 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PHL}	EN to VOUT	128	239	249	280

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PHL}	EN to VOUT	0.172	2.56

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

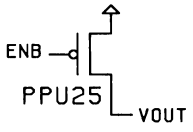
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	1600μA typical

DC specifications

25μA P–Channel Pullup Device

PPU25 is a weak p–channel pullup that sources 25μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.039 pF
Output Cap.: VOUT: 0.139 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.25 gates, 10 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	5157	9627	10035	11259

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.001	103

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

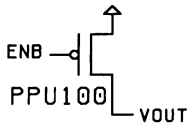
(V_{ENB}=0V, V_{OUT}=0V)

PARAMETER	CONDITIONS	RATING
Pullup Current	V_{DD}=5V, Nominal Process, 25°C	25µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	450nA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	600nA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	800nA maximum
*Maximum supply current conditions for PPU25.		

DC specifications

100μA P–Channel Pullup Device

PPU100 is a weak p–channel pullup that sources 100μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.078 pF
Output Cap.: VOUT: 0.125 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.75 gates, 9 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	1099	2051	2138	2399

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.001	22.0

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

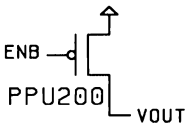
(V_{ENB}=0V, V_{OUT}=0V)

PARAMETER	CONDITIONS	RATING
Pullup Current	V_{DD}=5V, Nominal Process, 25°C	100µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	450nA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	600nA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	800nA maximum
*Maximum supply current conditions for PPU100.		

DC specifications

200μA P–Channel Pullup Device

PPU200 is a weak p–channel pullup that sources 200μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.039 pF
Output Cap.: VOUT: 0.124 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.50 gates, 8 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	763	1424	1484	1665

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.001	15.3

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

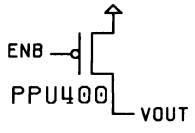
(V_{ENB}=0V, V_{OUT}=0V)

PARAMETER	CONDITIONS	RATING
Pullup Current	V_{DD}=5V, Nominal Process, 25°C	200µA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	450nA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	600nA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	800nA maximum
*Maximum supply current conditions for PPU200.		

DC specifications

400μA P–Channel Pullup Device

PPU400 is a weak p-channel pullup that sources 400μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see Pullup and Pulldown Current Range Specifications the application note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.039 pF
Output Cap.: VOUT: 0.139 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.187 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.25 gates, 6 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	260	486	506	568

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.018	5.20

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

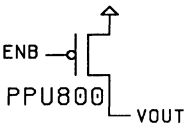
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	400μA typical

DC specifications

800μA P–Channel Pullup Device

PPU800 is a weak p–channel pullup that sources 800μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.039 pF
Output Cap.: VOUT: 0.140 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.100 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.00 gate, 5 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	139	260	271	304

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.100	2.78

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

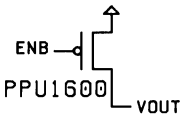
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	800μA typical

DC specifications

1600μA P–Channel Pullup Device

PPU1600 is a weak p-channel pullup that sources 1600μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells, where VOUT is connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD16, etc.). The cell can also be used as a pullup on internal tristate bus lines. If used this way, timing effects of the current source on cells tied to the bus are not modeled. Therefore, timings for cells tied to the bus are not guaranteed. To determine current ranges over various process, voltage, and temperature conditions, see the Pullup and Pulldown Current Range Specifications application note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.039 pF
Output Cap.: VOUT: 0.140 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.156 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 0.25 gates, 3 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 50.0pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	ENB to VOUT	68.9	129	134	150

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	ENB to VOUT	0.064	1.38

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

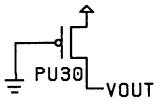
PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	1600μA typical

DC specifications

30μA P–Channel Pullup Device

PU30 is a weak p–channel pullup that sources 30μA when VOUT equals zero volts and can be used as a pullup on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See PPU200, PPU400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see Pullup and Pulldown Current Range Specifications application note.

This cell contains a voltage reference that produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.



*NOTE: The gate input on the PU30 cannot be used to turn the transistor on or off.

Inputs: GNDIN
Outputs: VOUT
Input Cap.: GNDIN: 0.000 pF
Output Cap.: VOUT: 0.124 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 2.25 gates, 8 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	*VOUT	1511	2821	2941	3300
* Timing is from VOUT = 0V to VOUT = 2.5V					

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	*VOUT	1500	72.4

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
VOUT	0.000	0.000	0.000	0.000

Rise/Fall time coefficients for the next cell

(V_{OUT}=0)

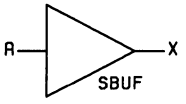
PARAMETER	CONDITIONS	RATING
Pullup Current	V_{DD}=5V, Nominal Process, 25°C	30μA typical
Supply Current	V_{DD}=5.5V, Best Case Process, 70°C*	450nA maximum
	V_{DD}=5.5V, Best Case Process, 85°C*	600nA maximum
	V_{DD}=5.5V, Best Case Process, 125°C*	800nA maximum
*Maximum supply current conditions for PU30.		

DC specifications

SBUF

Small Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.184 M_{CHL} = 0.349
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 1.00 gate, 3 array sites



(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.475	0.900	0.939	1.05
t_{PHL}		0.545	1.04	1.09	1.22

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.207	1.19
t_{PHL}		0.309	0.560

Delay coefficients

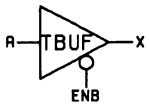
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.149	2.66	0.219	0.920

Rise/Fall time coefficients for the next cell

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.081
ENB: 0.159 pF
Output Cap.: X: 0.115 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.099 M_{CHL} = 0.185
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.665	1.25	1.30	1.46
t_{PHL}		0.597	1.13	1.18	1.32
t_{PLH}	ENB to X	0.400	0.753	0.785	0.882
t_{PHL}		0.421	0.798	0.832	0.936

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.450	1.08
t_{PHL}		0.443	0.476
t_{PLH}	ENB to X	0.186	1.08
t_{PHL}		0.270	0.455

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

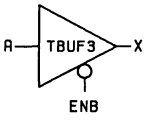
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.438	2.50	0.332	0.752

Rise/Fall time coefficients for the next cell

TBUF3

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.162
ENB: 0.081 pF
Output Cap.: X: 0.197 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.340 M_{CHL} = 0.178
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 4.50 gates, 12 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.574	1.09	1.14	1.28
t_{PHL}		0.629	1.19	1.24	1.39
t_{PLH}	ENB to X	0.838	1.59	1.66	1.86
t_{PHL}		0.989	1.86	1.94	2.18

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.368	0.394
t_{PHL}		0.502	0.329
t_{PLH}	ENB to X	0.625	0.436
t_{PHL}		0.860	0.339

Delay coefficients

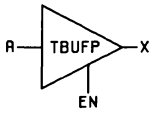
Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.355	0.698	0.343	0.325

Rise/Fall time coefficients for the next cell

Noninverting Tristate Buffer

EN is active high. When EN is low, the output is in a Hi–Z state.



Inputs: A, EN
Outputs: X
Input Cap.: A: 0.081
EN: 0.165 pF
Output Cap.: X: 0.115 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.055 M_{CHL} = 0.140
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 3.00 gates, 7 array sites

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.657	1.23	1.28	1.44
t_{PHL}		0.564	1.06	1.11	1.24
t_{PLH}	EN to X	0.439	0.824	0.859	0.964
t_{PHL}		0.210	0.402	0.419	0.472

Timing characteristics

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.461	1.08
t_{PHL}		0.429	0.476
t_{PLH}	EN to X	0.235	1.13
t_{PHL}		0.079	0.452

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.485	2.46	0.218	0.835

Rise/Fall time coefficients for the next cell

NCR VGX1500 Gate Array Library Data Sheets
Alphabetical Contents

NCR VGX1500 Gate Array Library Data Sheets
Functional Contents

Simple Logic Cells

Buffers

Latches

Decoders and Multiplexers

Flip–Flops

Tristate Elements

Input/Output Cells

Special Function Cells

NCR VGX1500 Gate Array Library

Electrical Specifications

DC Characteristics

Sym	Parameter	VDD	Guaranteed Limit			Unit
			0 to 70°C	−40 to 85°C	−55 to 125°C	
V_{IH} (TTL)	Minimum high-level Input voltage	4.5	2.0	2.0	2.0	V
		5.5	2.0	2.0	2.0	
V_{IL} (TTL)	Maximum low-level Input voltage	4.5	0.8	0.8	0.8	V
		5.5	0.8	0.8	0.8	
V_{IH} (CMOS)	Minimum high-level Input voltage	4.5	3.15	3.15	3.15	V
		5.5	3.85	3.85	3.85	
V_{IL} (CMOS)	Maximum low-level Input voltage	4.5	1.35	1.35	1.35	V
		5.5	1.65	1.65	1.65	
V_{OH}	Minimum high-level Output Voltage Any buffer, I_{OH} = −20µa	4.5	4.4	4.4	4.4	V
		5.5	5.4	5.4	5.4	
I_{OH}	Minimum high-level Source Current, V_{OH} = 2.4V					mA
	2mA buffer	4.5	2.0	2.0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	24.0	
	48mA buffer		48.0	48.0	48.0	
V_{OL}	Maximum low-level Output Voltage Any buffer, I_{OL} = 20µa	4.5	0.1	0.1	0.1	V
		5.5	0.1	0.1	0.1	
I_{OL}	Minimum low-level Sink Current, V_{OL} = 0.4V					mA
	2mA buffer		2.0	2 0	2.0	
	4mA buffer		4.0	4.0	4.0	
	8mA buffer		8.0	8.0	8.0	
	16mA buffer		16.0	16.0	16.0	
	24mA buffer		24.0	24.0	24.0	
	48mA buffer		48.0	48.0	48.0	
I_{IN}	Maximum input leakage current	5.5	±10	±10	±20	µA
I_{OZ}	Maximum output leakage current	5.5	±10	±10	±20	µA

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{DD}	DC power supply voltage	−0.5 to 7.0	V
V_{IN}, V_{OUT}	DC input, output voltage	−0.5 to V_{DD}+0.5	V
I	DC current drain V_{DD} and V_{SS} pins	100	mA
T_{STG}	Storage temperature	−55 to 150	°C
T_L	Lead temperature (less than 10 second soldering)	250	°C
T_{OPER}	Operating temperature Commercial Industrial Military	 0 to 70 −40 to 85 −55 to 125	°C

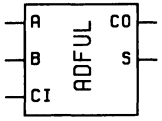
* Stresses beyond those listed in the "Absolute Maximum Ratings" table may cause physical damage to a device and should be avoided. This table does not imply that operation at conditions above those listed in the "Recommended Operating Conditions" is possible. This is a stress rating and operation of a device at or above this rating for an extended period may cause failure or affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	DC power supply voltage	3.0	6.0	V
V_{IN}, V_{OUT}	DC input, output voltage	0	V_{DD}	V

Full Adder

The ADFUL is a single-bit asynchronous adder with carry-in/carry-out function.



Inputs: A, B, CI
Outputs: CO, S
Input Cap.: A: 0.322
B: 0.308
CI: 0.328 pF
Cell Size: 9.0 gates, 24 array sites

FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H

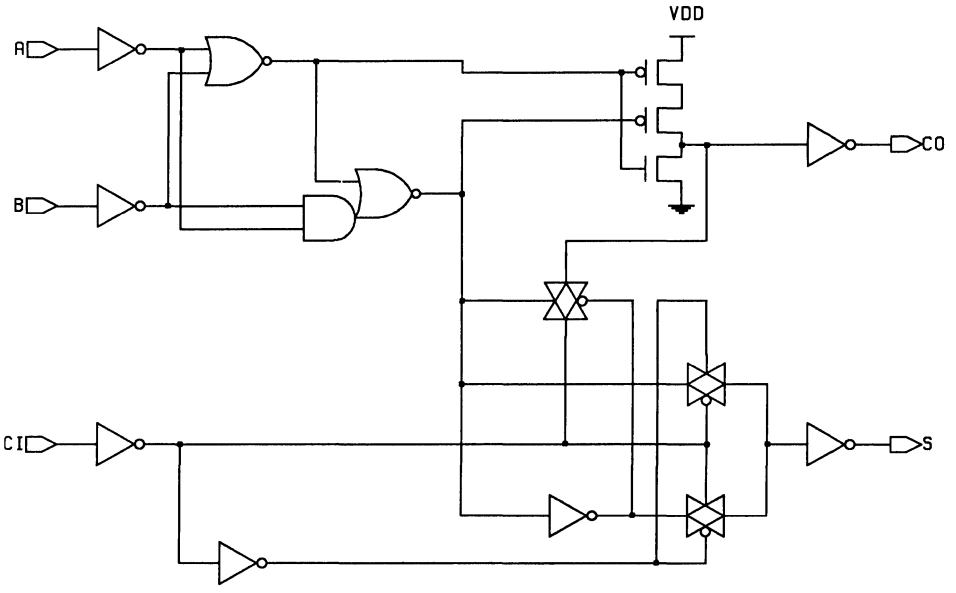
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO S	3.34	6.12	6.38	7.16	3.06+1.35*C_L ns
t_{PHL}		3.60	6.62	6.90	7.74	3.42+0.916*C_L ns
t_{PLH}	CI TO S	3.14	5.77	6.01	6.75	2.87+1.37*C_L ns
t_{PHL}		3.53	6.48	6.76	7.58	3.35+0.888*C_L ns
t_{PLH}	*IN TO CO	2.72	5.00	5.21	5.84	2.45+1.35*C_L ns
t_{PHL}		2.39	4.39	4.58	5.14	2.24+0.752*C_L ns
t_{PLH}	CI TO CO	2.58	4.73	4.93	5.53	2.31+1.34*C_L ns
t_{PHL}		2.26	4.14	4.32	4.84	2.12+0.687*C_L ns
t_r	*IN TO S	2.16	3.96	4.13	4.63	1.71+2.25*C_L ns
t_f		1.55	2.85	2.97	3.34	1.36+0.972*C_L ns
t_r	CI TO S	1.94	3.57	3.72	4.17	1.46+2.39*C_L ns
t_f		1.52	2.79	2.91	3.26	1.30+1.07*C_L ns
t_r	*IN TO CO	1.57	2.88	3.01	3.37	1.05+2.60*C_L ns
t_f		1.34	2.46	2.57	2.88	1.13+1.06*C_L ns
t_r	CI TO CO	1.70	3.12	3.25	3.65	1.18+2.60*C_L ns
t_f		1.33	2.44	2.54	2.85	1.13+0.994*C_L ns

* Timing applies to either A or B input

Switching characteristics

ADFUL



Functional diagram: ADFUL

2–Input AND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 1.50 gates, 4 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.04	1.90	1.98	2.23	0.764+1.36*C_L ns
t_{PHL}		1.000	1.84	1.92	2.16	0.858+0.726*C_L ns
t_r	*IN TO X	1.12	2.05	2.14	2.40	0.542+2.87*C_L ns
t_f		0.809	1.48	1.55	1.74	0.569+1.20*C_L ns
* Slowest input						

Switching characteristics

3–Input AND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites

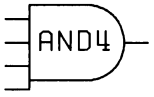
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.40	2.58	2.69	3.02	1.13+1.38*C_L ns
t_{PHL}		1.18	2.17	2.27	2.54	1.03+0.745*C_L ns
t_r	*IN TO X	1.40	2.57	2.68	3.01	0.871+2.65*C_L ns
t_f		0.846	1.55	1.62	1.82	0.599+1.23*C_L ns
* Slowest input						

Switching characteristics

4–Input AND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.50 gates, 6 array sites



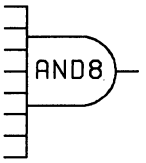
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.82	3.34	3.48	3.91	1.54+1.41*C_L ns
t_{PHL}		1.31	2.40	2.50	2.81	1.15+0.780*C_L ns
t_r	*IN TO X	1.49	2.74	2.85	3.20	0.944+2.73*C_L ns
t_f		0.875	1.61	1.67	1.88	0.623+1.26*C_L ns
* Slowest input						

Switching characteristics

8–Input AND Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 5.0 gates, 12 array sites



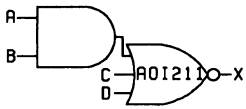
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.40	4.40	4.59	5.15	1.88+2.56*C_L ns
t_{PHL}		1.37	2.51	2.61	2.93	1.21+0.772*C_L ns
t_r	*IN TO X	2.37	4.34	4.53	5.08	1.23+5.68*C_L ns
t_f		1.21	2.22	2.31	2.59	0.997+1.06*C_L ns
* Slowest input						

Switching characteristics

2–1–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



$X = \overline{(A \cdot B) + C + D}$

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

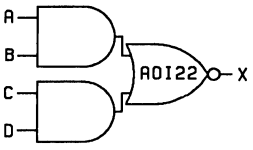
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.29	4.20	4.38	4.91	1.50+3.91*C_L ns
t_{PHL}		0.700	1.28	1.34	1.50	0.469+1.15*C_L ns
t_r	*IN TO X	3.89	7.15	7.45	8.36	2.13+8.79*C_L ns
t_f		1.31	2.41	2.51	2.81	0.850+2.30*C_L ns
* Slowest input						

Switching characteristics

AOI22

2–2 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



$\overline{X = (A \bullet B) + (C \bullet D)}$

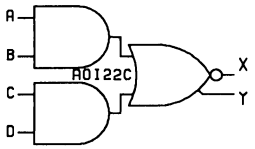
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.09	2.01	2.09	2.35	0.696+1.99*C_L ns
t_{PHL}		0.603	1.11	1.15	1.29	0.371+1.15*C_L ns
t_r	*IN TO X	2.03	3.73	3.89	4.36	1.17+4.29*C_L ns
t_f		0.946	1.74	1.81	2.03	0.481+2.32*C_L ns
* Slowest input						

Switching characteristics

2–2 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 2.50 gates, 7 array sites



$\overline{X = (A \bullet B) + (C \bullet D)}$
$Y = (A \bullet B) + (C \bullet D)$

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.63	2.99	3.12	3.50	1.11+2.62*C_L ns
t_{PHL}		0.710	1.30	1.36	1.52	0.480+1.15*C_L ns
t_{PLH}	X TO Y	0.642	1.18	1.23	1.38	0.366+1.38*C_L ns
t_{PHL}		0.455	0.836	0.871	0.977	0.278+0.884*C_L ns
t_{PLH}	*IN TO Y	1.12	2.06	2.15	2.41	0.846+1.38*C_L ns
t_{PHL}		1.56	2.87	2.99	3.35	1.38+0.884*C_L ns
t_r	*IN TO X	3.29	6.03	6.29	7.05	2.11+5.87*C_L ns
t_f		1.25	2.29	2.39	2.68	0.795+2.27*C_L ns
t_r	X TO Y	0.993	1.82	1.90	2.13	0.400+2.96*C_L ns
t_f		1.32	2.42	2.52	2.83	1.13+0.923*C_L ns
t_r	*IN TO Y	0.993	1.82	1.90	2.13	0.400+2.96*C_L ns
t_f		1.32	2.42	2.52	2.83	1.13+0.923*C_L ns
* Slowest input						

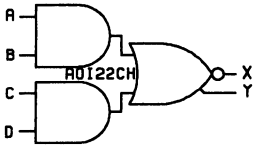
Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

AOI22CH

2–2 AND–OR–Invert with Complementary Outputs (High Drive)

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 4.0 gates, 10 array sites



$X = \overline{(A \cdot B) + (C \cdot D)}$
$Y = (A \cdot B) + (C \cdot D)$

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

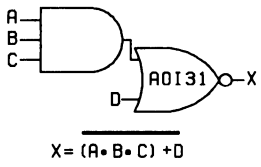
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO Y	1.33	2.44	2.54	2.85	1.19+0.680*C_L ns
t_{PHL}		1.90	3.49	3.64	4.09	1.80+0.488*C_L ns
t_{PLH}	*IN TO X	0.795	1.46	1.52	1.71	0.655+0.694*C_L ns
t_{PHL}		0.316	0.581	0.606	0.679	0.227+0.445*C_L ns
t_{PLH}	Y TO X	2.60	4.77	4.98	5.58	2.46+0.694*C_L ns
t_{PHL}		1.51	2.77	2.89	3.24	1.42+0.445*C_L ns
t_r	*IN TO Y	1.43	2.62	2.74	3.07	1.19+1.21*C_L ns
t_f		1.52	2.80	2.92	3.27	1.42+0.515*C_L ns
t_r	*IN TO X	1.51	2.76	2.88	3.23	1.28+1.12*C_L ns
t_f		0.895	1.64	1.71	1.92	0.802+0.461*C_L ns
t_r	Y TO X	1.51	2.76	2.88	3.23	1.28+1.12*C_L ns
t_f		0.895	1.64	1.71	1.92	0.802+0.461*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

3–1 AND–OR–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

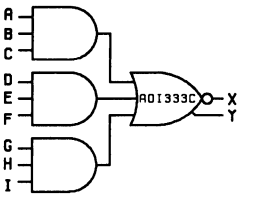
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.64	3.00	3.13	3.51	1.10+2.65*C_L ns
t_{PHL}		0.950	1.74	1.82	2.04	0.619+1.65*C_L ns
t_r	*IN TO X	2.72	4.99	5.21	5.84	1.55+5.86*C_L ns
t_f		1.64	3.01	3.14	3.52	0.976+3.31*C_L ns
* Slowest input						

Switching characteristics

AOI333C

3–3–3 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 5.50 gates, 13 array sites



X= (A•B•C) + (D•E•F) + (G•H•I)
Y= (A•B•C) + (D•E•F) + (G•H•I)

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

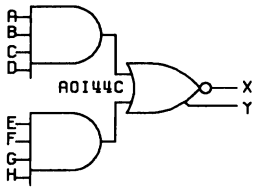
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	Y TO X	0.643	1.18	1.23	1.38	0.354+1.44*C_L ns
t_{PHL}		0.383	0.703	0.733	0.822	0.221+0.806*C_L ns
t_{PLH}	*IN TO Y	2.43	4.47	4.65	5.22	2.13+1.50*C_L ns
t_{PHL}		3.62	6.65	6.93	7.78	3.39+1.13*C_L ns
t_{PLH}	*IN TO X	4.04	7.42	7.73	8.67	3.75+1.44*C_L ns
t_{PHL}		2.51	4.62	4.81	5.40	2.35+0.806*C_L ns
t_r	Y TO X	1.82	3.34	3.48	3.91	1.33+2.44*C_L ns
t_f		1.40	2.57	2.67	3.00	1.19+1.02*C_L ns
t_r	*IN TO Y	2.31	4.24	4.42	4.96	1.78+2.64*C_L ns
t_f		2.16	3.96	4.13	4.63	1.94+1.11*C_L ns
t_r	*IN TO X	1.82	3.34	3.48	3.91	1.33+2.44*C_L ns
t_f		1.40	2.57	2.67	3.00	1.19+1.02*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

4–4 AND–OR–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 8.50 gates, 22 array sites



$X = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$
$Y = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

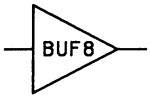
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.23	4.10	4.28	4.80	1.72+2.57*C_L ns
t_{PHL}		2.21	4.06	4.23	4.74	2.04+0.828*C_L ns
t_{PLH}	*IN TO Y	2.74	5.03	5.24	5.88	2.46+1.40*C_L ns
t_{PHL}		2.39	4.39	4.58	5.14	2.23+0.776*C_L ns
t_r	*IN TO X	2.29	4.20	4.38	4.92	1.15+5.71*C_L ns
t_f		1.47	2.70	2.82	3.16	1.25+1.12*C_L ns
t_r	*IN TO Y	1.74	3.20	3.34	3.74	1.24+2.52*C_L ns
t_f		1.37	2.51	2.62	2.94	1.16+1.06*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The Y output delay is not dependent upon the X output delay for this cell.

Noninverting Buffer (8X Drive)

BUF8 has 8 times the drive of an INV but is noninverting.



Inputs: A
Outputs: X
Input Cap.: A: 0.205 pF
Cell Size: 5.0 gates, 11 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

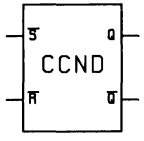
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.04	1.91	1.99	2.24	0.990+0.255*C_L ns
t_{PHL}		1.06	1.95	2.04	2.29	1.02+0.198*C_L ns
t_r	A TO X	1.19	2.18	2.27	2.55	1.13+0.275*C_L ns
t_f		0.798	1.46	1.53	1.71	0.769+0.138*C_L ns

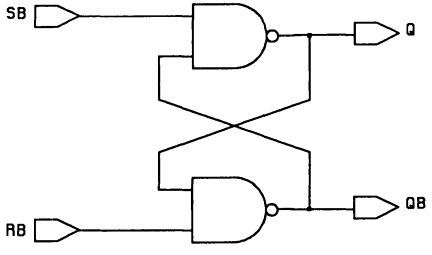
Switching characteristics

Cross–Coupled NAND Latch

CCND is very sensitive to negative spikes on SB or RB.

Inputs: SB, RB
Outputs: Q, QB
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites





Functional diagram: CCND

FUNCTION TABLE

SB	RB	Q	QB
L	L	*	*
L	H	H	L
H	L	L	H
H	H	Q_o	QB_o

* Both outputs will remain high as long as SB and RB remain low, but the output states are unpredictable if SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	SB TO Q	0.755	1.39	1.44	1.62	0.480+1.37*C_L ns
t_{PHL}		1.53	2.81	2.93	3.29	0.969+2.81*C_L ns
t_{PLH}	SB TO QB	0.755	1.39	1.44	1.62	0.480+1.37*C_L ns
t_{PHL}		1.56	2.86	2.98	3.34	0.997+2.80*C_L ns
t_{PLH}	RB TO Q	0.755	1.39	1.44	1.62	0.480+1.37*C_L ns
t_{PHL}		1.56	2.86	2.98	3.34	0.997+2.80*C_L ns
t_{PLH}	RB TO QB	0.755	1.39	1.44	1.62	0.480+1.37*C_L ns
t_{PHL}		1.53	2.81	2.92	3.28	0.965+2.81*C_L ns
t_r	SB TO Q	1.41	2.60	2.71	3.04	0.877+2.68*C_L ns
t_f		1.22	2.24	2.34	2.62	0.698+2.61*C_L ns
t_r	SB TO QB	1.41	2.60	2.71	3.04	0.877+2.68*C_L ns
t_f		1.30	2.38	2.48	2.79	0.787+2.55*C_L ns
t_r	RB TO Q	1.41	2.60	2.71	3.04	0.879+2.68*C_L ns
t_f		1.30	2.38	2.48	2.79	0.787+2.55*C_L ns
t_r	RB TO QB	1.41	2.60	2.71	3.04	0.879+2.68*C_L ns
t_f		1.22	2.24	2.33	2.62	0.696+2.61*C_L ns

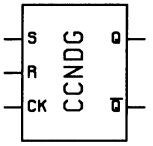
Switching characteristics

CCNDG

Gated R/S Flip–Flop

CCNDG is very sensitive to positive spikes on S and R while CK is high.

Inputs: S, CK, R
Outputs: Q, QB
Input Cap.: S: 0.102
CK: 0.211
R: 0.102 pF
Cell Size: 4.0 gates, 10 array sites



FUNCTION TABLE

CK	S	R	Q	QB
L	X	X	Q_0	QB_0
H	L	L	Q_0	QB_0
H	L	H	L	H
H	H	L	H	L
H	H	H	*	*

* Both outputs will remain high as long as S, R, and CK are high, but the output states are unpredictable if S and R go low simultaneously or if CK goes low while S and R are still high.

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

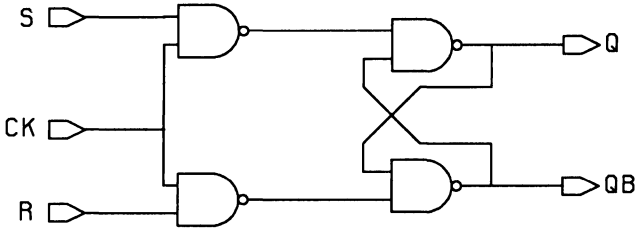
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	S TO Q	1.23	2.26	2.36	2.64	0.959+1.35*C_L ns
t_{PHL}		1.22	2.25	2.34	2.63	0.999+1.11*C_L ns
t_{PHL}	S TO QB	2.12	3.89	4.05	4.54	1.57+2.74*C_L ns
t_{PLH}	CK TO Q	1.23	2.25	2.35	2.64	0.956+1.35*C_L ns
t_{PHL}		2.04	3.75	3.91	4.39	1.46+2.89*C_L ns
t_{PLH}	CK TO QB	1.23	2.26	2.36	2.64	0.951+1.40*C_L ns
t_{PHL}		2.15	3.94	4.11	4.61	1.56+2.91*C_L ns
t_{PHL}	R TO Q	2.11	3.88	4.05	4.54	1.56+2.74*C_L ns
t_{PLH}	R TO QB	1.23	2.25	2.35	2.64	0.955+1.36*C_L ns
t_{PHL}		1.36	2.50	2.61	2.92	1.14+1.12*C_L ns
t_r	S TO Q	1.61	2.95	3.08	3.45	1.09+2.60*C_L ns
t_f		1.30	2.39	2.49	2.79	0.859+2.20*C_L ns
t_f	S TO QB	1.51	2.78	2.89	3.25	0.990+2.60*C_L ns
t_r	CK TO Q	1.65	3.03	3.16	3.54	1.09+2.78*C_L ns
t_f		1.73	3.18	3.31	3.72	1.18+2.74*C_L ns
t_r	CK TO QB	1.48	2.71	2.83	3.17	0.909+2.84*C_L ns
t_f		1.60	2.93	3.06	3.43	0.994+3.01*C_L ns
t_f	R TO Q	1.51	2.78	2.89	3.25	1.000+2.54*C_L ns
t_r	R TO QB	1.60	2.94	3.07	3.44	1.08+2.60*C_L ns
t_f		1.36	2.50	2.60	2.92	0.922+2.19*C_L ns

Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	S to CK	2.25	ns
t_{su}	R to CK	2.25	ns
t_h	CK to S	2.25	ns
t_h	CK to R	2.25	ns
t_{pwh}	High CK Pulse Width	4.25	ns

Timing requirements

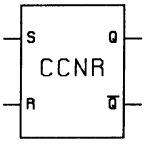


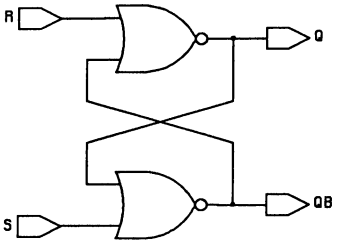
Functional diagram: CCNDG

Cross–Coupled NOR Latch

CCNR is very sensitive to positive spikes on S and R.

Inputs: S, R
Outputs: Q, QB
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites





Functional diagram: CCNR

FUNCTION TABLE

S	R	Q	QB
L	L	Q_o	QB_o
L	H	L	H
H	L	H	L
H	H	*	*

* Both outputs will remain low as long as S and R are high, but the output states are unpredictable if S and R go low simultaneously.

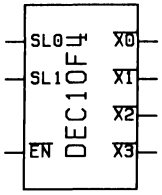
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	S TO Q	1.88	3.45	3.59	4.03	1.18+3.47*C_L ns
t_{PHL}		0.465	0.854	0.890	0.999	0.338+0.636*C_L ns
t_{PLH}	S TO QB	1.85	3.40	3.54	3.97	1.15+3.47*C_L ns
t_{PHL}		0.465	0.854	0.890	0.999	0.336+0.645*C_L ns
t_{PLH}	R TO Q	1.85	3.40	3.54	3.97	1.15+3.48*C_L ns
t_{PHL}		0.465	0.854	0.890	0.999	0.338+0.636*C_L. ns
t_{PLH}	R TO QB	1.88	3.45	3.59	4.03	1.18+3.47*C_L ns
t_{PHL}		0.465	0.854	0.890	0.999	0.338+0.636*C_L ns
t_r	S TO Q	2.60	4.77	4.97	5.58	1.40+5.97*C_L ns
t_f		0.740	1.36	1.42	1.59	0.488+1.25*C_L ns
t_r	S TO QB	2.61	4.80	5.00	5.61	1.42+5.96*C_L ns
t_f		0.740	1.36	1.42	1.59	0.488+1.25*C_L ns
t_r	R TO Q	2.61	4.80	5.00	5.61	1.42+5.96*C_L ns
t_f		0.740	1.36	1.42	1.59	0.487+1.26*C_L ns
t_r	R TO QB	2.60	4.77	4.97	5.58	1.40+5.97*C_L ns
t_f		0.740	1.36	1.42	1.59	0.487+1.26*C_L ns

Switching characteristics

1–of–4 Decoder

Inputs: SL0, SL1, ENB
Outputs: X0B, X1B, X2B, X3B
Input Cap.: All: 0.102 pF
Cell Size: 9.50 gates, 25 array sites



FUNCTION TABLE

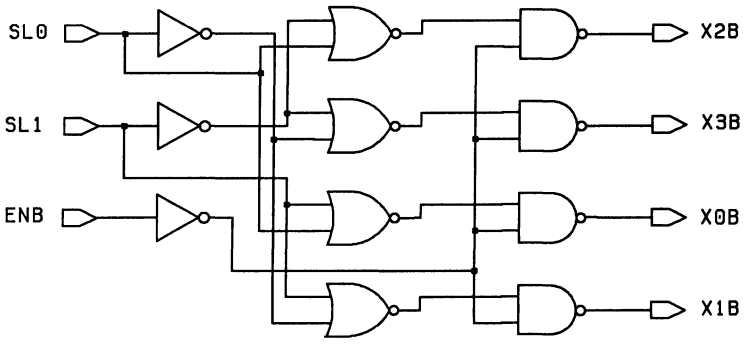
SL0	SL1	ENB	X0B	X1B	X2B	X3B
X	X	H	H	H	H	H
L	L	L	L	H	H	H
H	L	L	H	L	H	H
L	H	L	H	H	L	H
H	H	L	H	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*SL TO XnB	0.888	1.63	1.70	1.91	0.611+1.38*C_L ns
t_{PHL}		1.50	2.75	2.87	3.22	1.25+1.22*C_L ns
t_{PLH}	*ENB TO XnB	0.888	1.63	1.70	1.91	0.611+1.38*C_L ns
t_{PHL}		1.50	2.75	2.87	3.22	1.25+1.22*C_L ns
t_r	*SL TO XnB	1.06	1.95	2.03	2.28	0.452+3.04*C_L ns
t_f		1.43	2.62	2.73	3.06	1.02+2.03*C_L ns
t_r	*ENB TO XnB	1.06	1.95	2.03	2.28	0.452+3.04*C_L ns
t_f		1.43	2.62	2.73	3.06	1.02+2.03*C_L ns
* SL timing applies to both SL0 and SL1. XnB represents any output.						

Switching characteristics

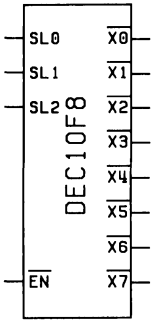
DEC1OF4



Functional diagram: DEC1OF4

1–of–8 Decoder

Inputs: SL0, SL1, SL2, ENB
Outputs: X0B, X1B, X2B, X3B, X4B, X5B, X6B, X7B
Input Cap.: All: 0.102 pF
Cell Size: 18.0 gates, 46 array sites



FUNCTION TABLE

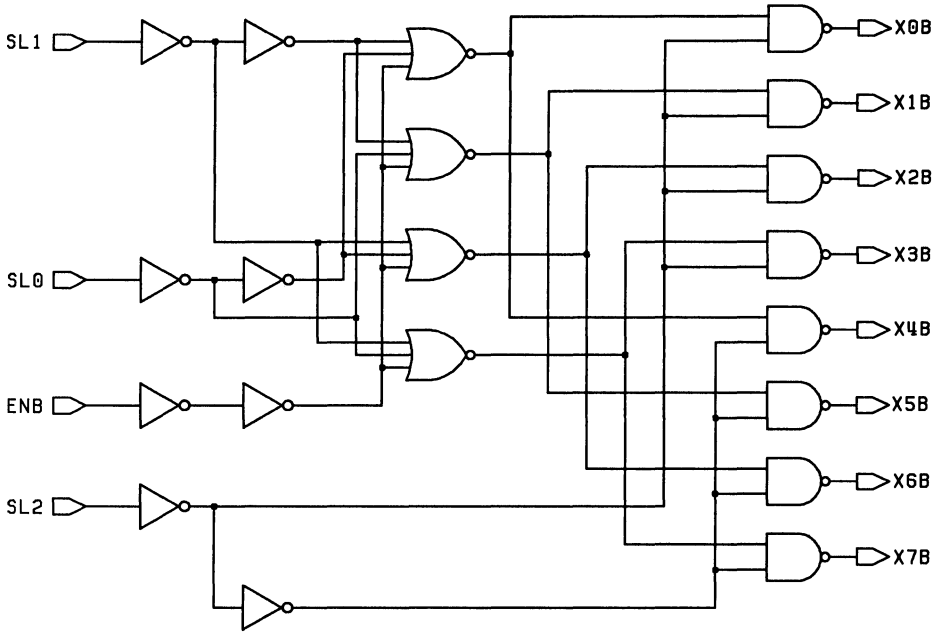
SL0	SL1	SL2	ENB	X0B	X1B	X2B	X3B	X4B	X5B	X6B	X7B
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

(Input t_r, t_f=1.4 ns, C_L=0.2 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*ENB TO XnB	2.06	3.79	3.95	4.43	1.80+1.32*C_L ns
t_{PHL}		3.40	6.25	6.51	7.30	3.12+1.38*C_L ns
t_{PLH}	*SL2 TO XnB	2.45	4.50	4.69	5.26	2.19+1.28*C_L ns
t_{PHL}		3.53	6.48	6.75	7.58	3.25+1.35*C_L ns
t_r	*ENB TO XnB	1.55	2.84	2.96	3.33	1.02+2.65*C_L ns
t_f		2.19	4.03	4.20	4.71	1.85+1.74*C_L ns
t_r	*SL2 TO XnB	1.72	3.16	3.30	3.70	1.20+2.62*C_L ns
t_f		2.16	3.97	4.14	4.64	1.80+1.80*C_L ns
* ENB timing applies to SL0, SL1 and ENB. XnB represents any output.						

Switching characteristics

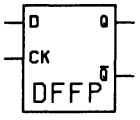
DEC1OF8



Functional diagram: DEC1OF8

D Flip–Flop, Positive Edge Triggered

DFFP is a fully static D-type flip-flop. It is positive edge triggered with respect to the single phase clock input (CK).



Inputs: D, CK
Outputs: Q, QB
Input Cap.: All: 0.102 pF
Cell Size: 7.0 gates, 17 array sites

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	2.27	4.16	4.34	4.87	1.99+1.38*C_L ns
t_{PHL}		2.06	3.79	3.95	4.43	1.87+0.953*C_L ns
t_{PLH}	CK TO QB	2.74	5.03	5.24	5.88	2.47+1.31*C_L ns
t_{PHL}		2.60	4.78	4.98	5.59	2.46+0.722*C_L ns
t_r	CK TO Q	1.28	2.35	2.45	2.75	0.720+2.80*C_L ns
t_f		1.12	2.05	2.14	2.40	0.880+1.18*C_L ns
t_r	CK TO QB	1.28	2.35	2.45	2.75	0.726+2.76*C_L ns
t_f		0.820	1.50	1.57	1.76	0.604+1.07*C_L ns

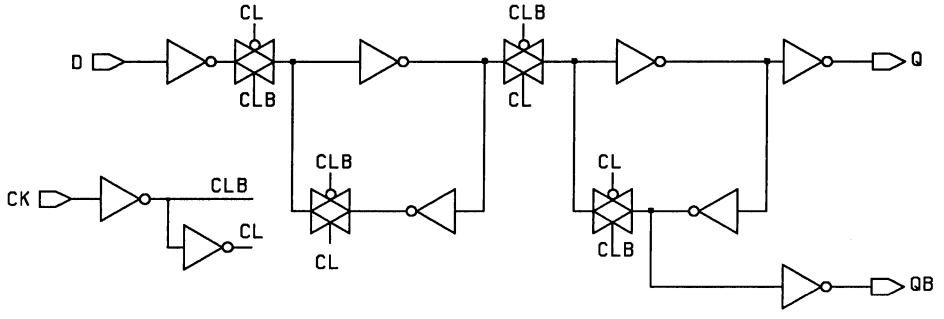
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.25	ns
t_h	Hold Time CK to D	−1.00	ns
t_{pwh}	High CK Pulse Width	4.50	ns
t_{pwl}	Low CK Pulse Width	4.75	ns

Timing requirements

DFFP

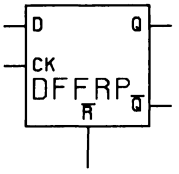


Functional diagram: DFFP

D Flip–Flop with Reset, Positive Edge Triggered

DFFRP is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.218
D, CK: 0.102 pF
Cell Size: 8.0 gates, 22 array sites



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	2.44	4.48	4.67	5.24	2.16+1.37*C_L ns
t_{PHL}		2.08	3.81	3.97	4.46	1.87+1.01*C_L ns
t_{PLH}	CK TO QB	2.82	5.18	5.40	6.06	2.54+1.39*C_L ns
t_{PHL}		2.82	5.19	5.40	6.06	2.66+0.790*C_L ns
t_{PHL}	RB TO Q	1.44	2.65	2.76	3.10	1.27+0.846*C_L ns
t_{PLH}	RB TO QB	2.21	4.06	4.23	4.74	1.95+1.26*C_L ns
t_r	CK TO Q	1.62	2.97	3.10	3.48	1.09+2.62*C_L ns
t_f		1.26	2.32	2.42	2.72	1.000+1.30*C_L ns
t_r	CK TO QB	1.48	2.72	2.83	3.18	0.927+2.76*C_L ns
t_f		1.72	3.15	3.28	3.68	1.60+0.559*C_L ns
t_f	RB TO Q	1.23	2.26	2.36	2.65	1.03+1.01*C_L ns
t_r	RB TO QB	1.50	2.76	2.88	3.23	0.968+2.67*C_L ns

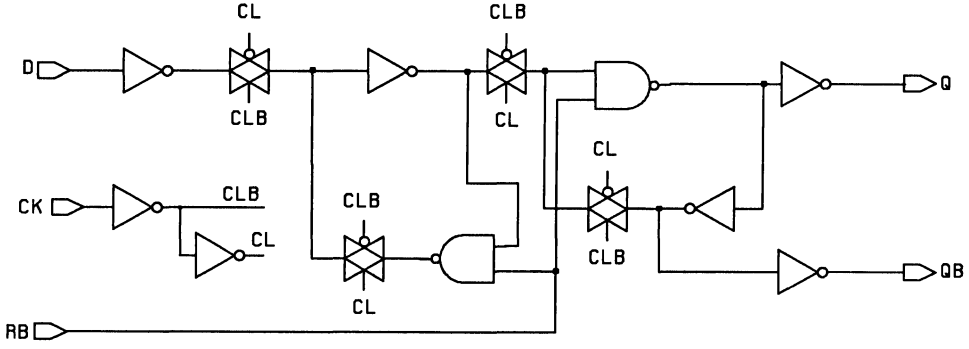
Switching characteristics

DFFRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−1.25	ns
t_{pwh}	High CK Pulse Width	4.75	ns
t_{pwl}	RB Pulse Width (low)	4.25	ns
t_{pwl}	Low CK Pulse Width	5.00	ns
rt	RB Recovery Time	1.75	ns

Timing requirements

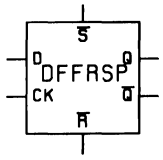


Functional diagram: DFFRP

D Flip–Flop with Reset and Set, Positive Edge Triggered

DFFRSP is a fully static D-type, positive edge triggered flip-flop. SB and RB are asynchronous and active low. This cell is functionally compatible with a TTL 74LS74.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.205
D, CK: 0.102
RB: 0.274 pF
Cell Size: 10.25 gates, 27 array sites



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be high when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	3.74	6.87	7.16	8.04	3.46+1.40*C_L ns
t_{PHL}		3.19	5.85	6.10	6.84	3.00+0.916*C_L ns
t_{PLH}	CK TO QB	2.65	4.86	5.07	5.69	2.39+1.30*C_L ns
t_{PHL}		2.67	4.90	5.11	5.73	2.50+0.845*C_L ns
t_{PHL}	RB TO Q	2.65	4.86	5.07	5.69	2.51+0.675*C_L ns
t_{PLH}	RB TO QB	1.98	3.64	3.79	4.26	1.72+1.30*C_L ns
t_{PHL}		2.24	4.11	4.28	4.81	2.11+0.654*C_L ns
t_{PLH}	SB TO Q	1.72	3.16	3.30	3.70	1.45+1.34*C_L ns
t_{PHL}		1.34	2.46	2.56	2.87	1.20+0.669*C_L ns
t_{PHL}	SB TO QB	2.65	4.87	5.08	5.70	2.47+0.910*C_L ns
t_r	CK TO Q	1.76	3.22	3.36	3.77	1.26+2.49*C_L ns
t_f		1.72	3.16	3.29	3.69	1.59+0.657*C_L ns
t_r	CK TO QB	1.52	2.79	2.91	3.26	0.986+2.67*C_L ns
t_f		1.68	3.09	3.22	3.61	1.58+0.511*C_L ns
t_f	RB TO Q	0.699	1.28	1.34	1.50	0.355+1.72*C_L ns
t_r	RB TO QB	1.41	2.58	2.69	3.02	0.864+2.70*C_L ns

Switching characteristics (Sheet 1 of 2)

DFFRSP

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

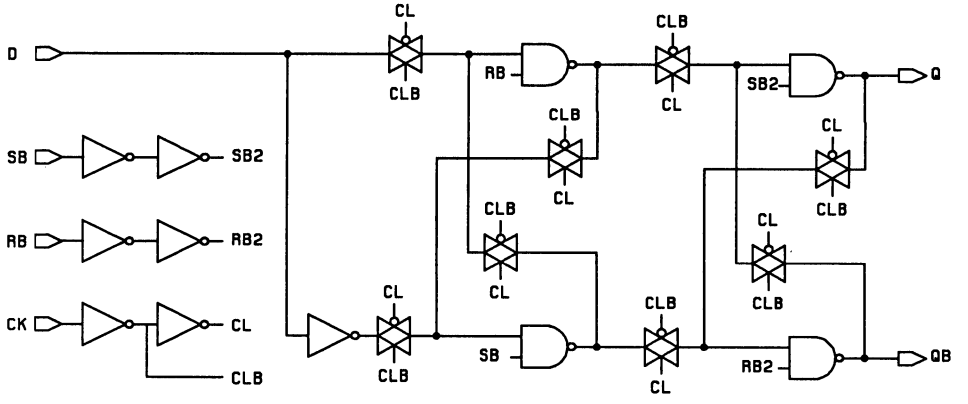
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.40	2.57	2.68	3.01	1.23+0.829*C_L ns
t_r	SB TO Q	1.34	2.46	2.57	2.88	0.794+2.74*C_L ns
t_f		0.558	1.02	1.07	1.20	0.312+1.23*C_L ns
t_f	SB TO QB	1.75	3.21	3.34	3.75	1.62+0.626*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−1.25	ns
t_{pwh}	High CK Pulse Width	4.25	ns
t_{pwl}	SB Pulse Width (low)	4.25	ns
t_{pwl}	Low CK Pulse Width	5.25	ns
t_{pwl}	RB Pulse Width (low)	4.50	ns
rt	SB Recovery Time	−1.25	ns
rt	RB Recovery Time	1.75	ns

Timing requirements

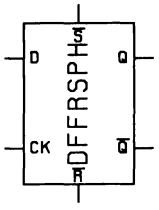


Functional diagram: DFFRSP

Buffered D Flip–Flop with Reset and Set, Positive Edge Triggered (High Drive)

DFFRSPH is a fully static D-type, edge triggered flip-flop. It is positive edge triggered with respect to the single phase clock (CK). RB and SB are asynchronous and active low.

Inputs: SB, D, CK, RB
Outputs: Q, QB
Input Cap.: SB: 0.205
D, CK: 0.102
RB: 0.274 pF
Cell Size: 10.25 gates, 26 array sites



FUNCTION TABLE

D	CK	SB	RB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	X	H	L	L	H
X	X	L	H	H	L
X	X	L	L	*	*

* Both Q and QB will be low when both SB and RB are low, but the output state is indeterminate if both SB and RB go high simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	SB TO Q	2.76	5.07	5.29	5.93	2.58+0.910*C_L ns
t_{PLH}	RB TO Q	1.93	3.55	3.70	4.15	1.77+0.801*C_L ns
t_{PHL}		1.42	2.61	2.72	3.06	1.31+0.565*C_L ns
t_{PLH}	CK TO Q	2.67	4.91	5.12	5.74	2.52+0.781*C_L ns
t_{PHL}		2.13	3.91	4.07	4.57	1.99+0.676*C_L ns
t_{PLH}	SB TO QB	1.16	2.12	2.21	2.48	1.01+0.727*C_L ns
t_{PHL}		1.21	2.23	2.32	2.61	1.12+0.462*C_L ns
t_{PLH}	RB TO QB	2.61	4.79	4.99	5.60	2.47+0.698*C_L ns
t_{PLH}	CK TO QB	3.45	6.34	6.61	7.42	3.31+0.717*C_L ns
t_{PHL}		3.24	5.94	6.20	6.95	3.13+0.543*C_L ns
t_r	SB TO Q	1.80	3.30	3.44	3.86	1.57+1.13*C_L ns
t_r	RB TO Q	1.49	2.74	2.85	3.20	1.25+1.20*C_L ns
t_f		1.08	1.98	2.06	2.32	0.949+0.645*C_L ns
t_r	CK TO Q	1.28	2.35	2.45	2.75	0.980+1.50*C_L ns
t_f		1.46	2.69	2.80	3.14	1.37+0.488*C_L ns

Switching characteristics (Sheet 1 of 2)

DFFRSPH

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

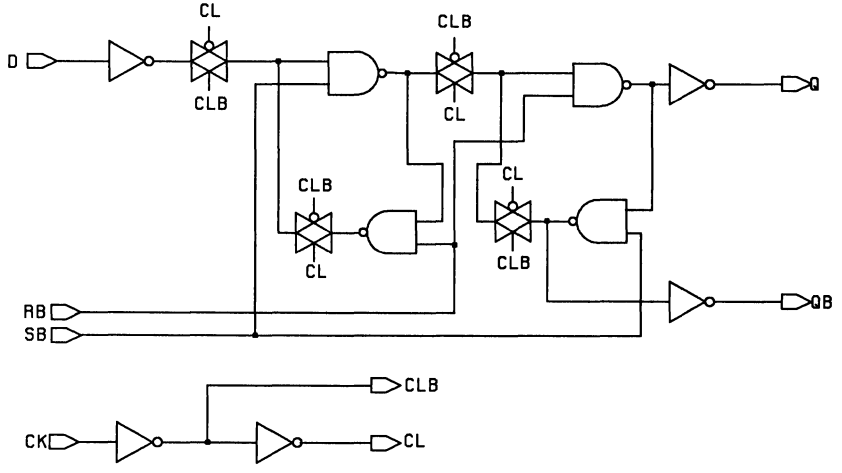
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_r	SB TO QB	0.804	1.48	1.54	1.73	0.505+1.49*C_L ns
t_f		0.827	1.52	1.58	1.78	0.702+0.621*C_L ns
t_r	RB TO QB	0.912	1.67	1.75	1.96	0.628+1.42*C_L ns
t_r	CK TO QB	1.85	3.39	3.53	3.96	1.65+0.982*C_L ns
t_f		1.40	2.57	2.68	3.01	1.34+0.310*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to CK	1.50	ns
t_h	Hold Time CK to D	−1.25	ns
t_{pwh}	High CK Pulse Width	4.25	ns
t_{pwl}	SB Pulse Width (low)	4.75	ns
t_{pwl}	Low CK Pulse Width	5.25	ns
t_{pwl}	RB Pulse Width (low)	5.00	ns
rt	SB Recovery Time	1.25	ns
rt	RB Recovery Time	1.25	ns

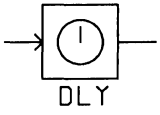
Timing requirements



Functional diagram: DFFRSPH

Delay Cell

Inputs: A
Outputs: X
Input Cap.: A: 0.102 pF
Cell Size: 4.75 gates, 13 array sites



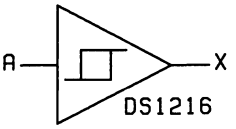
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	4.09	7.52	7.83	8.79	3.91+0.908*C_L ns
t_{PHL}		4.46	8.19	8.54	9.58	4.32+0.690*C_L ns
t_r	A TO X	1.67	3.06	3.19	3.58	1.45+1.07*C_L ns
t_f		1.62	2.98	3.10	3.48	1.45+0.854*C_L ns

Switching characteristics

Schmitt Trigger

DS1216 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.204 pF
Cell Size: 3.75 gates, 12 array sites

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.6V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 400mV Min: 100mV

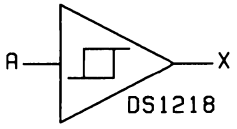
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	2.00	3.68	3.83	4.30	1.21+3.98*C_L ns
t_{PHL}		1.24	2.28	2.38	2.67	1.12+0.629*C_L ns
t_r	A TO X	3.64	6.69	6.97	7.82	1.90+8.71*C_L ns
t_f		1.17	2.14	2.24	2.51	1.01+0.773*C_L ns

Switching characteristics

Schmitt Trigger

DS1218 can be used in place of INBUF to buffer the input and I/O pads.



Inputs: A
Outputs: X
Input Cap.: A: 0.155 pF
Cell Size: 3.0 gates, 8 array sites

DC Switching Parameters (V_{DD}=5V, T_A=25C)

Threshold Voltage: Low to High = 1.8V ± 300mV
High to Low = 1.2V ± 300mV
Hysteresis: Typ: 600mV Min: 300mV

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

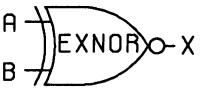
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.48	2.71	2.82	3.17	0.931+2.72*C_L ns
t_{PHL}		1.45	2.66	2.78	3.12	1.29+0.821*C_L ns
t_r	A TO X	2.22	4.08	4.25	4.77	1.02+5.99*C_L ns
t_f		0.801	1.47	1.53	1.72	0.630+0.852*C_L ns

Switching characteristics

EXNOR

2–Input Exclusive NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.214
B: 0.211 pF
Cell Size: 3.0 gates, 7 array sites



$X = A \cdot B + \overline{A} \cdot \overline{B}$

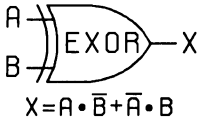
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.63	2.99	3.11	3.49	1.10+2.61*C_L ns
t_{PHL}		1.11	2.03	2.12	2.38	0.877+1.14*C_L ns
t_r	*IN TO X	2.58	4.74	4.95	5.55	1.41+5.85*C_L ns
t_f		1.06	1.95	2.04	2.28	0.600+2.32*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate

Inputs: A, B
Outputs: X
Input Cap.: A: 0.206
B: 0.211 pF
Cell Size: 3.0 gates, 7 array sites



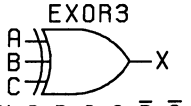
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.46	2.68	2.79	3.14	0.932+2.63*C_L ns
t_{PHL}		0.664	1.22	1.27	1.43	0.433+1.15*C_L ns
t_r	*IN TO X	2.48	4.55	4.75	5.33	1.29+5.92*C_L ns
t_f		1.15	2.11	2.20	2.47	0.690+2.29*C_L ns
* Slowest input						

Switching characteristics

3–Input Exclusive OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 5.0 gates, 14 array sites



$X=\bar{A}\bullet B\bullet\bar{C}+A\bullet\bar{B}\bullet\bar{C}$
$+\bar{A}\bullet B\bullet\bar{C}+\bar{A}\bullet\bar{B}\bullet C$

FUNCTION TABLE

A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

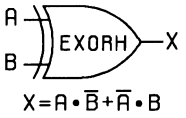
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.54	4.67	4.86	5.46	1.98+2.81*C_L ns
t_{PHL}		1.73	3.18	3.32	3.72	1.47+1.29*C_L ns
t_r	*IN TO X	3.61	6.63	6.91	7.75	2.05+7.79*C_L ns
t_f		1.61	2.95	3.07	3.45	1.000+3.02*C_L ns
* Slowest input						

Switching characteristics

2–Input Exclusive OR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.105
B: 0.102 pF
Cell Size: 3.50 gates, 9 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

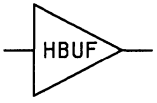
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.48	2.73	2.84	3.19	1.33+0.746*C_L ns
t_{PHL}		1.84	3.38	3.53	3.96	1.73+0.537*C_L ns
t_r	*IN TO X	1.20	2.21	2.30	2.58	0.971+1.15*C_L ns
t_f		1.17	2.15	2.24	2.52	1.05+0.607*C_L ns
* Slowest input						

Switching characteristics

HBUF

High Drive Noninverting Buffer

HBUF has 4 times the drive of an INV but is noninverting.



Inputs: A
Outputs: X
Input Cap.: A: 0.102 pF
Cell Size: 2.50 gates, 6 array sites

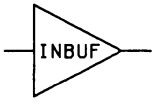
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.923	1.69	1.77	1.98	0.847+0.377*C_L ns
t_{PHL}		1.17	2.15	2.24	2.51	1.12+0.254*C_L ns
t_r	A TO X	0.781	1.43	1.49	1.68	0.641+0.694*C_L ns
t_f		0.820	1.50	1.57	1.76	0.725+0.471*C_L ns

Switching characteristics

Noninverting Input Buffer

INBUF is used to buffer the signal from input and I/O pads, and is compatible with 1.4V & 300mV threshold voltage (V_{DD} = 5V). INBUF is tested using V_{IL} = 0.8V and V_{IH} = 2.0V.



Inputs: A
Outputs: X
Input Cap.: A: 0.259 pF
Cell Size: 2.25 gates, 6 array sites

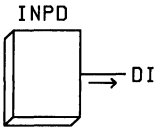
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.581	1.07	1.11	1.25	0.445+0.678*C_L ns
t_{PHL}		1.71	3.15	3.28	3.68	1.59+0.587*C_L ns
t_r	A TO X	0.705	1.29	1.35	1.51	0.413+1.46*C_L ns
t_f		1.41	2.58	2.69	3.02	1.31+0.498*C_L ns

Switching characteristics

Input Pad

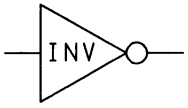
INPD is used with INBUF or a Schmitt Trigger. The propagation delay from the pad to the input of the chip is negligible.



Inputs: PAD
Outputs: DI
Input Cap.: PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.102 pF
Cell Size: 0.50 gates, 2 array sites



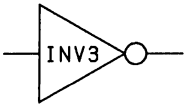
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.631	1.16	1.21	1.36	0.354+1.39*C_L ns
t_{PHL}		0.356	0.654	0.681	0.764	0.221+0.675*C_L ns
t_r	A TO X	1.02	1.88	1.96	2.19	0.434+2.93*C_L ns
t_f		0.683	1.25	1.31	1.47	0.445+1.19*C_L ns

Switching characteristics

Inverter (3X Drive)

INV3 has 3 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.310 pF
Cell Size: 1.50 gates, 4 array sites

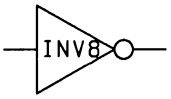
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.420	0.771	0.803	0.901	0.324+0.476*C_L ns
t_{PHL}		0.214	0.393	0.410	0.460	0.159+0.275*C_L ns
t_r	A TO X	0.720	1.32	1.38	1.55	0.523+0.983*C_L ns
t_f		0.580	1.07	1.11	1.25	0.531+0.247*C_L ns

Switching characteristics

Inverting Buffer (8X Drive)

INV8 has 8 times the drive of an INV.



Inputs: A
Outputs: X
Input Cap.: A: 0.830 pF
Cell Size: 4.0 gates, 9 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.345	0.634	0.661	0.741	0.304+0.205*C_L ns
t_{PHL}		0.121	0.222	0.231	0.260	0.086+0.173*C_L ns
t_r	A TO X	0.682	1.25	1.30	1.46	0.640+0.207*C_L ns
t_f		0.548	1.01	1.05	1.18	0.528+0.097*C_L ns

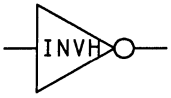
Switching characteristics

INVH

Inverter (High Drive)

INVH has 4 times the drive of an INV.

Inputs: A
Outputs: X
Input Cap.: A: 0.414 pF
Cell Size: 2.0 gates, 5 array sites



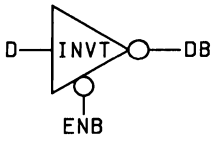
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.391	0.718	0.749	0.840	0.316+0.373*C_L ns
t_{PHL}		0.177	0.324	0.338	0.379	0.129+0.238*C_L ns
t_r	A TO X	0.711	1.30	1.36	1.53	0.601+0.548*C_L ns
t_f		0.571	1.05	1.09	1.22	0.531+0.194*C_L ns

Switching characteristics

Tristate Inverter

INVT inverts the input signal when ENB is low. When ENB is high, the output is in a Hi–Z state.



Inputs: D, ENB
Outputs: DB
Input Cap.: All: 0.102 pF
Output Cap.: DB: 0.127 pF
Cell Size: 1.50 gates, 4 array sites

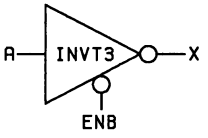
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO DB	1.25	2.29	2.39	2.68	0.717+2.65*C_L ns
t_{PHL}		0.596	1.09	1.14	1.28	0.364+1.16*C_L ns
t_{PLH}	ENB TO DB	0.960	1.76	1.84	2.06	0.425+2.67*C_L ns
t_{PHL}		0.791	1.45	1.51	1.70	0.612+0.890*C_L ns
t_r	D TO DB	2.17	3.98	4.15	4.65	0.998+5.84*C_L ns
t_f		0.956	1.76	1.83	2.05	0.491+2.32*C_L ns
t_r	ENB TO DB	2.08	3.83	3.99	4.47	0.919+5.82*C_L ns
t_f		1.11	2.04	2.13	2.39	0.591+2.60*C_L ns

Switching characteristics

Tristate Inverter (3X Drive)

INVT3 is a high drive tristate inverter with 3 times the drive of an INVT and a larger intrinsic delay. INVT3 inverts the input signal when ENB is low. When ENB is high, the output is in a Hi-Z state.]



Inputs: A, ENB
Outputs: X
Input Cap.: All: 0.102 pF
Output Cap.: X: 0.248 pF
Cell Size: 5.0 gates, 14 array sites

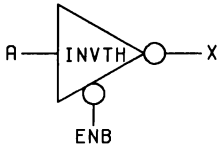
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.56	2.87	2.99	3.35	1.45+0.540*C_L ns
t_{PHL}		1.49	2.74	2.85	3.20	1.40+0.457*C_L ns
t_{PLH}	ENB TO X	1.51	2.77	2.89	3.24	1.39+0.597*C_L ns
t_{PHL}		1.94	3.56	3.71	4.16	1.86+0.363*C_L ns
t_r	A TO X	1.17	2.16	2.25	2.52	1.01+0.801*C_L ns
t_f		1.03	1.89	1.97	2.21	0.955+0.360*C_L ns
t_r	ENB TO X	1.18	2.17	2.27	2.54	1.02+0.805*C_L ns
t_f		1.32	2.42	2.53	2.83	1.27+0.269*C_L ns

Switching characteristics

Tristate Inverter (High Drive)

INVTH is a high drive tristate inverter with 2 times the drive of an INVT and a smaller intrinsic delay. The input signal is inverted when ENB is low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: All: 0.102 pF
Output Cap.: X: 0.127 pF
Cell Size: 4.50 gates, 12 array sites

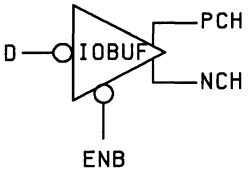
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.57	2.87	3.00	3.36	1.42+0.710*C_L ns
t_{PHL}		1.46	2.68	2.80	3.14	1.35+0.533*C_L ns
t_{PLH}	ENB TO X	1.52	2.80	2.92	3.27	1.37+0.765*C_L ns
t_{PHL}		1.87	3.43	3.58	4.01	1.78+0.434*C_L ns
t_r	A TO X	1.20	2.20	2.29	2.57	0.966+1.15*C_L ns
t_f		0.980	1.80	1.88	2.10	0.853+0.634*C_L ns
t_r	ENB TO X	1.21	2.22	2.32	2.60	0.984+1.13*C_L ns
t_f		1.24	2.27	2.37	2.66	1.14+0.492*C_L ns

Switching characteristics

Input/Output Buffer

IOBUF is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: All: 0.102 pF
Cell Size: 7.50 gates, 18 array sites

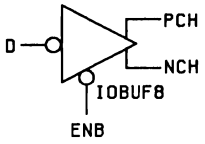
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	1.97	3.62	3.78	4.24	1.88+0.466*C_L ns
t_{PHL}		1.52	2.80	2.91	3.27	1.45+0.363*C_L ns
t_{PLH}	D TO PCH	1.65	3.02	3.15	3.54	1.57+0.385*C_L ns
t_{PHL}		2.25	4.13	4.30	4.83	2.17+0.388*C_L ns
t_{PLH}	ENB TO NCH	1.98	3.63	3.79	4.25	1.87+0.521*C_L ns
t_{PHL}		1.46	2.69	2.80	3.15	1.39+0.354*C_L ns
t_{PLH}	ENB TO PCH	1.62	2.97	3.10	3.48	1.52+0.486*C_L ns
t_{PHL}		2.65	4.87	5.07	5.69	2.58+0.362*C_L ns
t_r	D TO NCH	1.14	2.09	2.18	2.45	1.02+0.576*C_L ns
t_f		1.12	2.05	2.14	2.40	1.08+0.187*C_L ns
t_r	D TO PCH	0.969	1.78	1.85	2.08	0.833+0.677*C_L ns
t_f		1.37	2.51	2.62	2.94	1.29+0.416*C_L ns
t_r	ENB TO NCH	1.13	2.07	2.16	2.42	0.991+0.682*C_L ns
t_f		1.08	1.99	2.07	2.32	1.02+0.314*C_L ns
t_r	ENB TO PCH	1.21	2.23	2.32	2.61	1.10+0.575*C_L ns
t_f		1.35	2.48	2.59	2.90	1.26+0.461*C_L ns

Switching characteristics

Input/Output Buffer (8X Drive)

IOBUF8 is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: All: 0.102 pF
Cell Size: 14.0 gates, 32 array sites

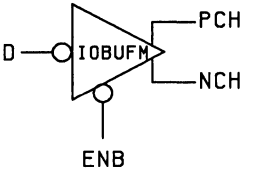
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	2.95	5.42	5.65	6.34	2.89+0.321*C_L ns
t_{PHL}		2.38	4.37	4.56	5.11	2.36+0.106*C_L ns
t_{PLH}	D TO PCH	2.47	4.53	4.72	5.30	2.42+0.250*C_L ns
t_{PHL}		2.43	4.46	4.65	5.22	2.39+0.182*C_L ns
t_{PLH}	ENB TO NCH	3.17	5.82	6.06	6.80	3.14+0.120*C_L ns
t_{PHL}		2.35	4.31	4.49	5.04	2.33+0.079*C_L ns
t_{PLH}	ENB TO PCH	1.94	3.56	3.71	4.16	1.88+0.284*C_L ns
t_{PHL}		2.39	4.38	4.56	5.12	2.36+0.113*C_L ns
t_r	D TO NCH	1.85	3.40	3.55	3.98	1.80+0.239*C_L ns
t_f		1.12	2.05	2.14	2.40	1.04+0.354*C_L ns
t_r	D TO PCH	1.45	2.67	2.78	3.12	1.40+0.248*C_L ns
t_f		1.42	2.61	2.72	3.05	1.37+0.250*C_L ns
t_r	ENB TO NCH	1.29	2.37	2.47	2.77	1.25+0.205*C_L ns
t_f		1.02	1.87	1.95	2.19	0.951+0.340*C_L ns
t_r	ENB TO PCH	1.16	2.12	2.21	2.48	1.10+0.277*C_L ns
t_f		1.15	2.12	2.21	2.48	1.08+0.343*C_L ns

Switching characteristics

Input/Output Buffer (Medium Drive)

IOBUFM is used to drive I/O and tristatable pads. When ENB is high, NCH and PCH drive the pad cell to a Hi-Z state on the pad. When ENB is low, D is output on the pad of the pad cell.



Inputs: ENB, D
Outputs: NCH, PCH
Input Cap.: All: 0.102 pF
Cell Size: 5.50 gates, 14 array sites

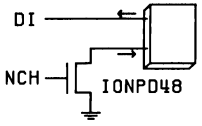
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO NCH	1.70	3.13	3.26	3.66	1.55+0.752*C_L ns
t_{PHL}		1.41	2.58	2.69	3.02	1.31+0.455*C_L ns
t_{PLH}	D TO PCH	1.61	2.96	3.08	3.46	1.47+0.715*C_L ns
t_{PHL}		1.77	3.25	3.39	3.80	1.66+0.539*C_L ns
t_{PLH}	ENB TO NCH	1.83	3.37	3.51	3.94	1.70+0.686*C_L ns
t_{PHL}		1.29	2.36	2.46	2.76	1.20+0.421*C_L ns
t_{PLH}	ENB TO PCH	1.60	2.93	3.06	3.43	1.45+0.710*C_L ns
t_{PHL}		2.23	4.09	4.26	4.78	2.13+0.491*C_L ns
t_r	D TO NCH	1.30	2.39	2.49	2.79	1.07+1.16*C_L ns
t_f		0.868	1.59	1.66	1.86	0.762+0.522*C_L ns
t_r	D TO PCH	1.23	2.26	2.36	2.64	1.000+1.15*C_L ns
t_f		1.29	2.37	2.47	2.77	1.19+0.509*C_L ns
t_r	ENB TO NCH	1.36	2.50	2.60	2.92	1.14+1.12*C_L ns
t_f		0.785	1.44	1.50	1.68	0.662+0.609*C_L ns
t_r	ENB TO PCH	1.21	2.22	2.32	2.60	0.976+1.17*C_L ns
t_f		1.15	2.11	2.20	2.47	1.02+0.643*C_L ns

Switching characteristics

48mA Open–Drain Input/Output Pad

IONPD48 is used to form a bidirectional pad that can drive output data or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD, DI
Input Cap.: NCH: 17.166
PAD: 10.082 pF
Cell Size: 10.0 gates
2 pad sites (high drive pads)
3 pad sites (high count pads)*

*IONPD48 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	145	267	278	312	38.7+2.13*C_L ns
t_{PHL}		0.315	0.578	0.602	0.676	0.083+0.005*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

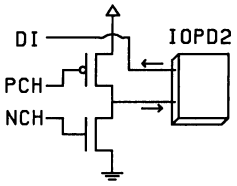
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

2mA Input/Output Pad

IOPD2 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 0.966
PCH: 0.853
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	4.81	8.84	9.21	10.3	0.821+0.080*C_L ns
t_{PHL}		5.72	10.5	10.9	12.3	1.09+0.092*C_L ns
* NCH or PCH						

Switching characteristics

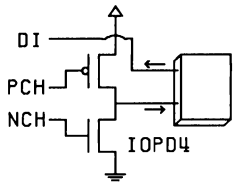
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-1.00	mA

DC specifications

4mA Input/Output Pad

IOPD4 is used to form a bidirectional pad that can drive output data, or be put in a Hi-Z state to allow input to be entered on the pad. The propagation delay from the pad to the input of the chip is negligible. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 1.819
PCH: 1.705
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	2.49	4.58	4.77	5.35	0.468+0.040*C_L ns
t_{PHL}		2.96	5.44	5.67	6.37	0.535+0.049*C_L ns
* NCH or PCH						

Switching characteristics

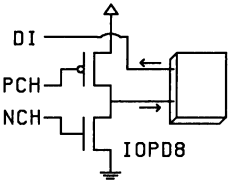
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

8mA Input/Output Pad

IOPD8 is used to form a bidirectional pad that can drive data or be put in a Hi–Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 3.524
PCH: 3.411
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.31	2.41	2.51	2.82	0.299+0.020*C_L ns
t_{PHL}		1.52	2.80	2.92	3.27	0.309+0.024*C_L ns
* NCH or PCH						

Switching characteristics

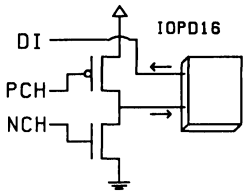
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}–0.5V	–4.00	mA

DC specifications

16mA Input/Output Pad

IOPD16 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 6.082
PCH: 5.968
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.806	1.48	1.54	1.73	0.228+0.012*C_L ns
t_{PHL}		0.872	1.60	1.67	1.87	0.206+0.013*C_L ns
* NCH or PCH						

Switching characteristics

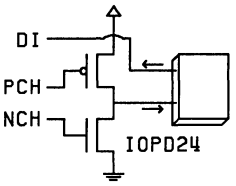
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Input/Output Pad

IOPD24 is used to form a bidirectional pad that can drive output data or be put in a Hi-Z state to allow input data to be entered on the pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD, DI
Input Cap.: NCH: 8.640
PCH: 8.526
PAD: 9.670 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

*IOPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.600	1.10	1.15	1.29	0.195+0.008*C_L ns
t_{PHL}		0.673	1.24	1.29	1.44	0.152+0.010*C_L ns
* NCH or PCH						

Switching characteristics

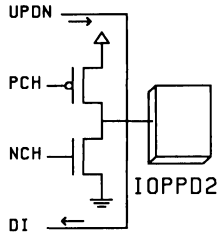
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

2mA Input/Output Pad with Pullup/Pulldown Port

IOPPD2 is similar to IOPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information. The propagation delay from the pad to the input of the chip is negligible.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 0.966
PCH: 0.856
UPDN: 59.670
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	4.83	8.87	9.25	10.4	0.841+0.080*C_L ns
t_{PHL}		5.74	10.5	11.0	12.3	1.11+0.092*C_L ns
* NCH or PCH						

Switching characteristics (CL=50.0pF)

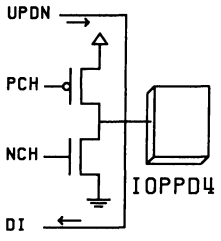
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Input/Output Pad with Pullup/Pulldown Port

IOPPD4 is similar to IOPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information. The propagation delay from the pad to the input of the chip is negligible.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 1.819
PCH: 1.705
UPDN: 59.670
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	2.50	4.59	4.79	5.37	0.477+0.040*C_L ns
t_{PHL}		2.98	5.46	5.69	6.39	0.546+0.049*C_L ns
* NCH or PCH						

Switching characteristics (CL=50pF)

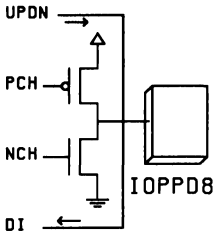
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-2.00	mA

DC specifications

8mA Input/Output Pad with Pullup/Pulldown Port

IOPPD8 is similar to IOPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information. The propagation delay from the pad to the input of the chip is negligible.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 3.524
PCH: 3.411
UPDN: 59.670
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.32	2.42	2.52	2.83	0.304+0.020*C_L ns
t_{PHL}		1.53	2.81	2.93	3.28	0.314+0.024*C_L ns
* NCH or PCH						

Switching characteristics (CL=50.0pF)

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

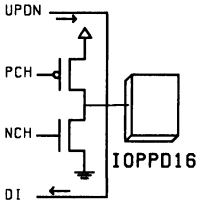
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC characteristics

IOPPD16

16mA Input/Output Pad with Pullup/Pulldown Port

IOPPD16 is similar to IOPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information. The propagation delay from the pad to the input of the chip is negligible.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 6.082
PCH: 5.968
UPDN: 59.670
PAD: 9.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.808	1.48	1.55	1.73	0.229+0.012*C_L ns
t_{PHL}		0.875	1.61	1.67	1.88	0.209+0.013*C_L ns
* NCH or PCH						

Switching characteristics (CL=50.0pF)

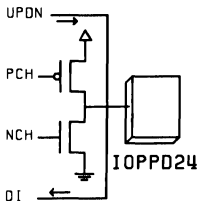
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA
I_{OH} (high level output current)	V_{OH} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Input/Output Pad with Pullup/Pulldown Port

IOPPD24 is similar to IOPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD, DI
Input Cap.: NCH: 8.640
PCH: 8.526
UPDN: 59.670
PAD: 9.670 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

*IOPPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.602	1.10	1.15	1.29	0.197+0.008*C_L ns
t_{PHL}		0.676	1.24	1.29	1.45	0.155+0.010*C_L ns
* NCH or PCH						

Switching characteristics (CL=50.0pF)

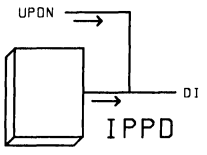
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

Input Pad with Pullup/Pulldown Port

IPPD is similar to INPD but includes an input port, UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See any PPU/PPD data sheet for pullup/pulldown current information.



Inputs: PAD, UPDN
Outputs: DI
Input Cap.: PAD: 9.670
UPDN: 59.670 pF
Cell Size: 5.0 gates, 1 pad site

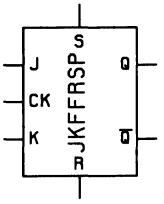
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	PAD TO DI	0.036	0.065	0.068	0.077	0.020+0.080*C_L ns
t_{PHL}		0.041	0.075	0.079	0.088	0.000+0.205*C_L ns
t_r	PAD TO DI	0.146	0.268	0.279	0.313	0.074+0.359*C_L ns
t_f		0.145	0.267	0.278	0.312	0.069+0.379*C_L ns

Switching characteristics

J–K Flip–Flop with Reset and Set, Positive Edge Triggered

JKFFRSP is a fully static JK–type edge triggered flip–flop. It is positive edge triggered with respect to CK. S and R are asynchronous and active high.



Inputs: CK, J, K, S, R
Outputs: Q, QB
Input Cap.: CK, J, K: 0.102
S: 0.256
R: 0.267 pF
Cell Size: 12.50 gates, 33 array sites

FUNCTION TABLE

J	K	CK	S	R	Q	QB
H	H	↑	L	L	QB_o	Q_o
H	L	↑	L	L	H	L
L	H	↑	L	L	L	H
L	L	↑	L	L	Q_o	QB_o
X	X	X	H	L	H	L
X	X	X	L	H	L	H
X	X	X	H	H	*	*

* Both Q and QB will be high as long as S and R are both high, but the output state is indeterminate if both S and R go low simultaneously.

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CK TO Q	4.18	7.67	8.00	8.98	3.92+1.30*C_L ns
t_{PHL}		3.58	6.57	6.84	7.68	3.40+0.853*C_L ns
t_{PLH}	CK TO QB	2.66	4.88	5.09	5.71	2.37+1.41*C_L ns
t_{PHL}		3.21	5.89	6.14	6.89	2.95+1.28*C_L ns
t_{PLH}	S TO Q	0.960	1.76	1.84	2.06	0.688+1.35*C_L ns
t_{PHL}		1.49	2.73	2.84	3.19	1.32+0.818*C_L ns
t_{PHL}	S TO QB	3.69	6.77	7.06	7.92	3.44+1.24*C_L ns
t_{PHL}	R TO Q	2.26	4.14	4.32	4.84	2.09+0.825*C_L ns
t_{PLH}	R TO QB	1.35	2.48	2.58	2.90	1.08+1.36*C_L ns
t_{PHL}		3.42	6.28	6.55	7.35	3.17+1.23*C_L ns
t_r	CK TO Q	1.33	2.43	2.54	2.85	0.773+2.76*C_L ns
t_f		1.19	2.19	2.28	2.56	0.981+1.04*C_L ns
t_r	CK TO QB	1.32	2.42	2.52	2.83	0.753+2.82*C_L ns
t_f		1.75	3.21	3.34	3.75	1.48+1.32*C_L ns
t_r	S TO Q	0.964	1.77	1.84	2.07	0.365+2.99*C_L ns

Switching characteristics (Sheet 1 of 2)

JKFFRSP

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

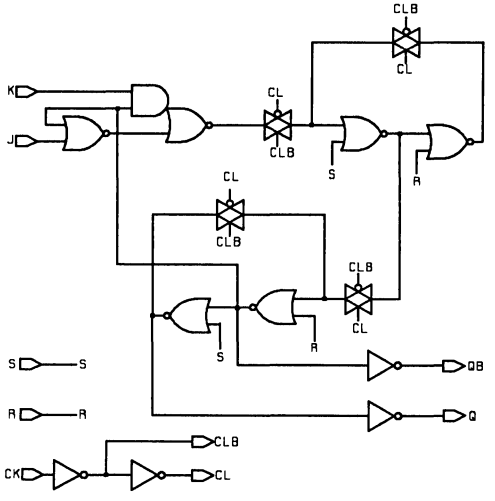
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_f		1.01	1.85	1.93	2.16	0.777+1.14*C_L ns
t_f	S TO QB	1.43	2.62	2.73	3.06	1.14+1.44*C_L ns
t_f	R TO Q	0.819	1.50	1.57	1.76	0.573+1.23*C_L ns
t_r	R TO QB	1.08	1.98	2.07	2.32	0.492+2.93*C_L ns
t_f		1.51	2.78	2.90	3.25	1.24+1.37*C_L ns

Switching characteristics (Sheet 2 of 2)

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time J to CK	4.00	ns
t_{su}	Setup Time K to CK	4.00	ns
t_h	Hold Time CK to J	−3.25	ns
t_h	Hold Time CK to K	−3.25	ns
t_{pwh}	High CK Pulse Width	6.50	ns
t_{pwh}	Set Pulse Width (high)	5.00	ns
t_{pwh}	Reset Pulse Width (high)	4.00	ns
t_{pwl}	Low CK Pulse Width	6.50	ns
rt	Set Recovery Time	3.25	ns
rt	Reset Recovery Time	−1.00	ns

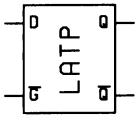
Timing requirements



Functional diagram: JKFFRSP

Transparent Latch, Positive Edge Triggered

LATP holds data when GB is high and is transparent when GB is low.



Inputs: D, GB
Outputs: Q, QB
Input Cap.: All: 0.102 pF
Cell Size: 4.50 gates, 12 array sites

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q_o	QB_o

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.42	2.60	2.71	3.05	1.14+1.39*C_L ns
t_{PHL}		1.87	3.43	3.58	4.01	1.68+0.944*C_L ns
t_{PLH}	D TO QB	2.50	4.59	4.78	5.36	2.23+1.34*C_L ns
t_{PHL}		1.81	3.33	3.47	3.89	1.66+0.725*C_L ns
t_{PLH}	GB TO Q	1.99	3.65	3.80	4.27	1.71+1.36*C_L ns
t_{PHL}		2.35	4.32	4.50	5.05	2.21+0.712*C_L ns
t_{PLH}	GB TO QB	2.02	3.70	3.86	4.33	1.74+1.36*C_L ns
t_{PHL}		2.37	4.36	4.54	5.09	2.23+0.714*C_L ns
t_r	D TO Q	1.41	2.60	2.71	3.04	0.868+2.72*C_L ns
t_f		1.17	2.14	2.24	2.51	0.942+1.12*C_L ns
t_r	D TO QB	1.18	2.17	2.26	2.54	0.610+2.85*C_L ns
t_f		1.34	2.46	2.57	2.88	1.20+0.684*C_L ns
t_r	GB TO Q	1.17	2.15	2.25	2.52	0.598+2.87*C_L ns
t_f		0.905	1.66	1.73	1.94	0.689+1.07*C_L ns
t_r	GB TO QB	1.22	2.24	2.33	2.62	0.649+2.85*C_L ns
t_f		0.910	1.67	1.74	1.95	0.696+1.07*C_L ns

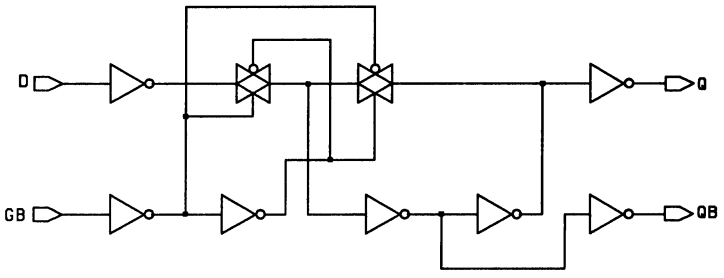
Switching characteristics

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.00	ns
t_h	Hold Time GB to D	-1.00	ns
t_{pwl}	GB Pulse Width (low)	5.25	ns

Timing requirements

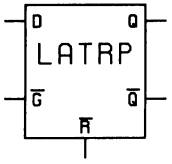
LATP



Functional diagram: LATP

Transparent Latch with Reset, Positive Edge Triggered

LATRP holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low. For a faster version of this cell, see LATRPF.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.161
D, GB: 0.102 pF
Cell Size: 5.25 gates, 15 array sites

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q$_0$	QB$_0$
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.88	3.44	3.59	4.03	1.59+1.40*C_L ns
t_{PHL}		2.00	3.66	3.82	4.29	1.80+0.962*C_L ns
t_{PLH}	D TO QB	2.57	4.73	4.93	5.53	2.30+1.36*C_L ns
t_{PHL}		2.36	4.33	4.51	5.06	2.21+0.725*C_L ns
t_{PLH}	GB TO Q	2.28	4.18	4.36	4.89	1.98+1.46*C_L ns
t_{PHL}		2.72	4.99	5.21	5.84	2.52+0.972*C_L ns
t_{PLH}	GB TO QB	3.32	6.09	6.35	7.13	3.05+1.35*C_L ns
t_{PHL}		2.68	4.92	5.12	5.75	2.53+0.715*C_L ns
t_{PLH}	RB TO Q	1.79	3.29	3.43	3.85	1.51+1.40*C_L ns
t_{PHL}		1.28	2.35	2.45	2.74	1.12+0.775*C_L ns
t_{PLH}	RB TO QB	1.90	3.49	3.64	4.08	1.64+1.32*C_L ns
t_{PHL}		2.14	3.93	4.10	4.60	2.00+0.700*C_L ns
t_r	D TO Q	1.53	2.81	2.93	3.29	0.993+2.68*C_L ns
t_f		1.22	2.25	2.34	2.63	0.997+1.13*C_L ns
t_r	D TO QB	1.29	2.37	2.47	2.77	0.737+2.75*C_L ns
t_f		1.32	2.41	2.52	2.82	1.10+1.06*C_L ns
t_r	GB TO Q	1.41	2.59	2.70	3.03	0.853+2.78*C_L ns
t_f		1.15	2.12	2.21	2.48	0.923+1.15*C_L ns
t_r	GB TO QB	1.17	2.16	2.25	2.52	0.606+2.84*C_L ns
t_f		0.974	1.79	1.86	2.09	0.779+0.971*C_L ns
t_r	RB TO Q	1.30	2.38	2.48	2.78	0.724+2.86*C_L ns
t_f		0.882	1.62	1.69	1.89	0.656+1.12*C_L ns
t_r	RB TO QB	1.21	2.22	2.31	2.59	0.649+2.79*C_L ns
t_f		0.838	1.54	1.60	1.80	0.606+1.16*C_L ns

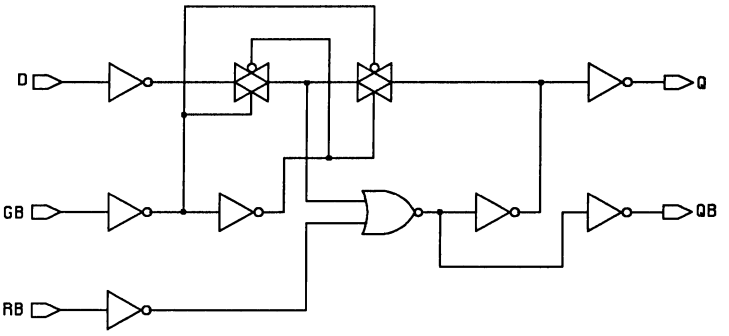
Switching characteristics

LATRP

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.00	ns
t_h	Hold Time GB to D	−1.75	ns
t_{pwl}	RB Pulse Width (low)	4.50	ns
t_{pwl}	GB Pulse Width (low)	5.50	ns
rt	RB Recovery Time	1.75	ns

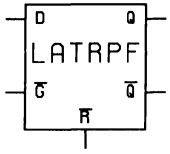
Timing requirements



Functional diagram: LATRP

Fast Transparent Latch with Reset, Positive Edge Triggered

LATRPF holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: RB, D, GB
Outputs: Q, QB
Input Cap.: RB: 0.161
D: 0.102
GB: 0.206 pF
Cell Size: 4.75 gates, 13 array sites

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q$_0$	QB$_0$
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.82	3.35	3.49	3.91	1.52+1.49*C_L ns
t_{PHL}		2.41	4.42	4.61	5.17	2.20+1.03*C_L ns
t_{PLH}	D TO QB	3.03	5.56	5.79	6.50	2.76+1.32*C_L ns
t_{PHL}		2.17	3.98	4.15	4.66	2.02+0.718*C_L ns
t_{PLH}	GB TO Q	2.15	3.94	4.11	4.61	1.84+1.51*C_L ns
t_{PHL}		2.17	3.99	4.15	4.66	1.97+0.991*C_L ns
t_{PLH}	GB TO QB	2.82	5.18	5.40	6.06	2.55+1.33*C_L ns
t_{PHL}		2.48	4.56	4.75	5.33	2.33+0.742*C_L ns
t_{PLH}	RB TO Q	1.86	3.42	3.57	4.00	1.56+1.51*C_L ns
t_{PHL}		1.44	2.64	2.76	3.09	1.27+0.848*C_L ns
t_{PLH}	RB TO QB	2.28	4.19	4.37	4.90	2.03+1.24*C_L ns
t_{PHL}		2.35	4.31	4.50	5.04	2.20+0.735*C_L ns
t_r	D TO Q	1.36	2.50	2.60	2.92	0.779+2.90*C_L ns
t_f		1.22	2.23	2.33	2.61	0.948+1.33*C_L ns
t_r	D TO QB	1.04	1.90	1.98	2.22	0.442+2.97*C_L ns
t_f		0.842	1.54	1.61	1.81	0.609+1.16*C_L ns
t_r	GB TO Q	1.42	2.61	2.72	3.05	0.852+2.85*C_L ns
t_f		1.36	2.49	2.60	2.91	1.15+1.03*C_L ns
t_r	GB TO QB	1.31	2.41	2.51	2.82	0.764+2.74*C_L ns
t_f		0.953	1.75	1.82	2.05	0.746+1.03*C_L ns
t_r	RB TO Q	1.57	2.88	3.00	3.37	1.02+2.75*C_L ns
t_f		1.24	2.28	2.38	2.67	1.06+0.887*C_L ns
t_r	RB TO QB	1.64	3.01	3.13	3.52	1.12+2.60*C_L ns
t_f		1.31	2.41	2.51	2.82	1.10+1.08*C_L ns

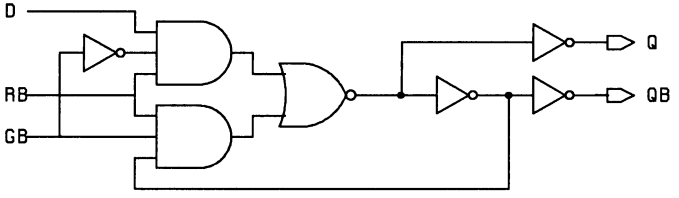
Switching characteristics

LATRPF

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	3.75	ns
t_h	Hold Time GB to D	−2.00	ns
t_{pwl}	RB Pulse Width (low)	4.25	ns
t_{pwl}	GB Pulse Width (low)	5.50	ns
rt	RB Recovery Time	2.00	ns

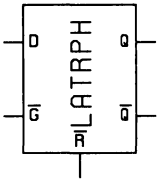
Timing requirements



Functional diagram: LATRPF

Transparent Latch with Reset, Positive Edge Triggered (High Drive)

LATRPH holds data when GB is high and is transparent when GB is low. RB is asynchronous and active low.



Inputs: D, GB, RB
Outputs: Q, QB
Input Cap.: D, GB: 0.102
RB: 0.161 pF
Cell Size: 6.25 gates, 16 array sites

FUNCTION TABLE

D	GB	RB	Q	QB
L	L	H	L	H
H	L	H	H	L
X	H	H	Q_o	QB_o
X	X	L	L	H

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	D TO Q	1.78	3.27	3.41	3.82	1.61+0.867*C_L ns
t_{PHL}		2.06	3.79	3.95	4.43	1.93+0.653*C_L ns
t_{PLH}	GB TO Q	2.37	4.36	4.54	5.10	2.20+0.862*C_L ns
t_{PHL}		2.63	4.83	5.03	5.65	2.47+0.773*C_L ns
t_{PLH}	RB TO Q	1.77	3.24	3.38	3.79	1.61+0.780*C_L ns
t_{PHL}		1.29	2.37	2.47	2.77	1.19+0.497*C_L ns
t_{PLH}	D TO QB	3.00	5.52	5.75	6.45	2.88+0.599*C_L ns
t_{PHL}		2.48	4.56	4.75	5.33	2.37+0.531*C_L ns
t_{PLH}	GB TO QB	3.72	6.84	7.13	8.00	3.57+0.761*C_L ns
t_{PHL}		3.25	5.96	6.21	6.97	3.18+0.323*C_L ns
t_{PLH}	RB TO QB	2.01	3.68	3.84	4.31	1.87+0.677*C_L ns
t_{PHL}		2.39	4.38	4.57	5.12	2.30+0.425*C_L ns
t_r	D TO Q	1.16	2.13	2.22	2.49	0.864+1.48*C_L ns
t_f		1.13	2.07	2.16	2.42	1.01+0.585*C_L ns
t_r	GB TO Q	1.65	3.03	3.16	3.55	1.41+1.19*C_L ns
t_f		1.75	3.22	3.36	3.76	1.64+0.559*C_L ns
t_r	RB TO Q	1.17	2.14	2.23	2.51	0.895+1.36*C_L ns
t_f		0.841	1.54	1.61	1.80	0.725+0.575*C_L ns
t_r	D TO QB	0.832	1.53	1.59	1.79	0.554+1.39*C_L ns
t_f		1.10	2.02	2.10	2.36	0.961+0.684*C_L ns
t_r	GB TO QB	1.63	2.99	3.11	3.49	1.42+1.05*C_L ns
t_f		1.24	2.28	2.37	2.66	1.13+0.547*C_L ns
t_r	RB TO QB	1.19	2.18	2.27	2.54	0.953+1.16*C_L ns
t_f		0.819	1.50	1.57	1.76	0.710+0.539*C_L ns

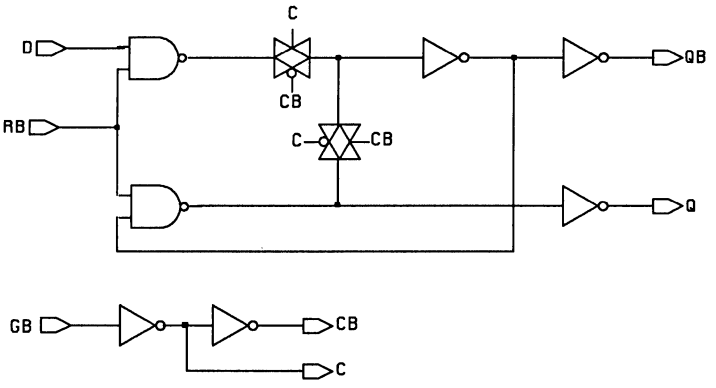
Switching characteristics

LATRPH

(Worst Case, 4.5V, 25C)

SYMBOL	PARAMETER	MINIMUM	UNIT
t_{su}	Setup Time D to GB	2.75	ns
t_h	Hold Time GB to D	−2.50	ns
t_{pwl}	GB Pulse Width (low)	6.00	ns
t_{pwl}	RB Pulse Width (low)	5.00	ns
rt	RB Recovery Time	2.25	ns

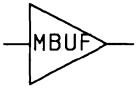
Timing requirements



Functional diagram: LATRPH

Medium Drive Noninverting Buffer

MBUF has 2 times the drive of an INV but is noninverting.



Inputs: A
Outputs: X
Input Cap.: A: 0.102 pF
Cell Size: 1.50 gates, 4 array sites

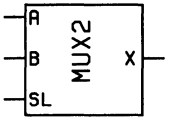
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.741	1.36	1.42	1.59	0.598+0.712*C_L ns
t_{PHL}		0.905	1.66	1.73	1.94	0.824+0.398*C_L ns
t_r	A TO X	0.722	1.33	1.38	1.55	0.418+1.52*C_L ns
t_f		0.711	1.30	1.36	1.53	0.576+0.668*C_L ns

Switching characteristics

2–Input Multiplexer

Inputs: SL, A, B
Outputs: X
Input Cap.: SL: 0.215
A, B: 0.102 pF
Cell Size: 3.0 gates, 7 array sites



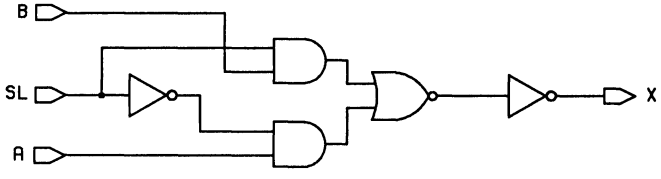
FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.27	2.34	2.44	2.73	1.000+1.35*C_L ns
t_{PHL}		1.57	2.89	3.01	3.38	1.40+0.862*C_L ns
t_{PLH}	SL TO X	1.69	3.10	3.23	3.63	1.42+1.36*C_L ns
t_{PHL}		1.56	2.87	2.99	3.36	1.39+0.871*C_L ns
t_r	*IN TO X	1.21	2.23	2.32	2.60	0.649+2.81*C_L ns
t_f		1.33	2.45	2.55	2.87	1.15+0.896*C_L ns
t_r	SL TO X	1.38	2.54	2.65	2.97	0.840+2.71*C_L ns
t_f		1.33	2.44	2.54	2.85	1.15+0.902*C_L ns
* Slowest of A or B inputs						

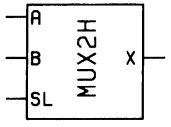
Switching characteristics



Functional diagram: MUX2

2–Input Multiplexer (High Drive)

Inputs: A, SL, B
Outputs: X
Input Cap.: A: 0.102
SL: 0.215
B: 0.102 pF
Cell Size: 3.50 gates, 8 array sites



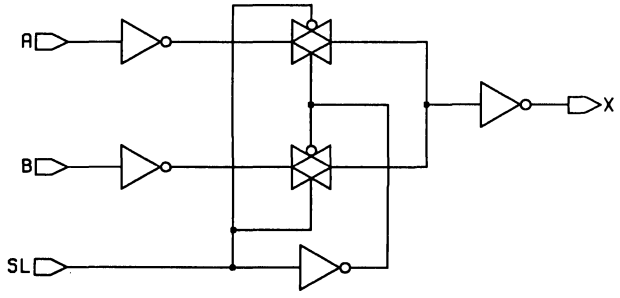
FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.27	2.34	2.44	2.73	1.13+0.716*C_L ns
t_{PHL}		1.66	3.04	3.17	3.55	1.53+0.613*C_L ns
t_{PLH}	SL TO X	1.67	3.07	3.20	3.59	1.52+0.748*C_L ns
t_{PHL}		1.67	3.06	3.19	3.58	1.54+0.620*C_L ns
t_r	*IN TO X	0.891	1.64	1.70	1.91	0.609+1.41*C_L ns
t_f		1.41	2.58	2.69	3.02	1.30+0.549*C_L ns
t_r	SL TO X	1.29	2.37	2.47	2.77	1.05+1.18*C_L ns
t_f		1.43	2.62	2.73	3.06	1.32+0.540*C_L ns
* Slowest of A or B inputs						

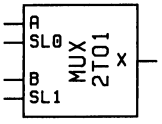
Switching characteristics



Functional diagram: MUX2H

2–Input Multiplexer with Separate Selects

In normal operation, SL1 and SL0 are complementary signals and X = A when SL0 is high and X = B when SL1 is high.



Inputs: SL1, SL0, A, B
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.50 gates, 7 array sites

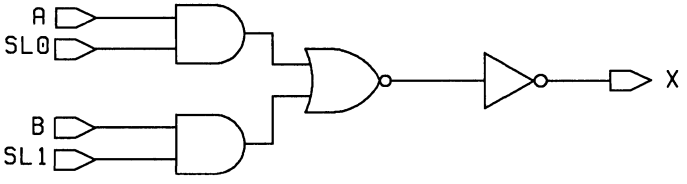
FUNCTION TABLE

SL1	SL0	X
L	L	L
L	H	A
H	L	B
H	H	A + B

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A,B TO X	1.41	2.60	2.71	3.04	1.14+1.38*C_L ns
t_{PHL}		1.44	2.65	2.76	3.09	1.28+0.798*C_L ns
t_{PLH}	*SL TO X	1.23	2.25	2.35	2.63	0.953+1.36*C_L ns
t_{PHL}		1.58	2.91	3.03	3.40	1.41+0.867*C_L ns
t_r	A,B TO X	1.42	2.61	2.72	3.05	0.887+2.67*C_L ns
t_f		1.13	2.08	2.17	2.43	0.922+1.05*C_L ns
t_r	*SL TO X	1.13	2.08	2.17	2.43	0.552+2.90*C_L ns
t_f		1.35	2.47	2.57	2.89	1.17+0.887*C_L ns
* SL timing applies to both SL0 and SL1						

Switching characteristics

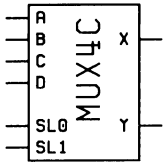


Functional diagram: MUX2TO1

4–Input Multiplexer with Complementary Outputs

SL0 and SL1 cause one of A, B, C, or D to be propagated to the outputs.

Inputs: A, B, C, D, SL0, SL1
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 8.0 gates, 21 array sites



FUNCTION TABLE

SL0	SL1	X	Y
L	L	A	$\overline{A}$
H	L	B	$\overline{B}$
L	H	C	$\overline{C}$
H	H	D	$\overline{D}$

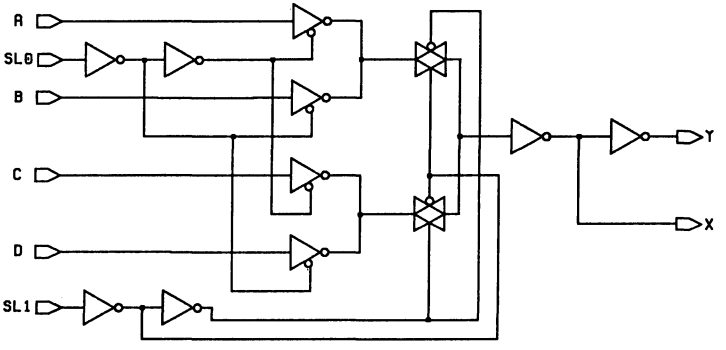
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.79	3.29	3.43	3.85	1.52+1.36*C_L ns
t_{PHL}		2.30	4.23	4.41	4.95	2.12+0.910*C_L ns
t_{PLH}	X TO Y	0.696	1.28	1.33	1.49	0.414+1.40*C_L ns
t_{PHL}		0.378	0.694	0.724	0.812	0.235+0.713*C_L ns
t_{PLH}	**SL TO X	2.65	4.86	5.07	5.68	2.38+1.31*C_L ns
t_{PHL}		2.25	4.14	4.31	4.84	2.06+0.966*C_L ns
t_{PLH}	X TO Y	0.694	1.27	1.33	1.49	0.424+1.35*C_L ns
t_{PHL}		0.182	0.334	0.348	0.391	0.000+0.910*C_L ns
t_{PLH}	*IN TO Y	2.82	5.17	5.39	6.05	2.53+1.40*C_L ns
t_{PHL}		1.90	3.48	3.63	4.07	1.75+0.713*C_L ns
t_{PLH}	**SL TO Y	3.08	5.65	5.89	6.61	2.81+1.35*C_L ns
t_{PHL}		2.24	4.12	4.29	4.81	2.06+0.910*C_L ns
t_r	*IN TO X	1.60	2.94	3.06	3.43	1.02+2.89*C_L ns
t_f		1.80	3.30	3.44	3.86	1.60+0.972*C_L ns
t_r	X TO Y	1.74	3.19	3.33	3.73	1.23+2.52*C_L ns
t_f		1.34	2.46	2.57	2.88	1.21+0.661*C_L ns
t_r	**SL TO X	1.89	3.47	3.61	4.05	1.34+2.75*C_L ns
t_f		1.65	3.03	3.16	3.54	1.43+1.12*C_L ns
t_r	X TO Y	1.59	2.93	3.05	3.42	1.07+2.61*C_L ns
t_f		1.56	2.87	2.99	3.35	1.39+0.842*C_L ns
t_r	*IN TO Y	1.74	3.19	3.33	3.73	1.23+2.52*C_L ns
t_f		1.34	2.46	2.57	2.88	1.21+0.661*C_L ns
t_r	**SL TO Y	1.59	2.93	3.05	3.42	1.07+2.61*C_L ns
t_f		1.56	2.87	2.99	3.35	1.39+0.842*C_L ns

* Slowest of A,B,C, or D inputs
** SL timing applies to both SL0 and SL1

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay and rise time. The delays listed and delay equation for Y assume no load on the X output.



Functional diagram: MUX4C

2–Input NAND Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 1.0 gate, 3 array sites

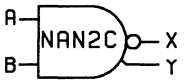
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.771	1.42	1.48	1.66	0.495+1.38*C_L ns
t_{PHL}		0.549	1.01	1.05	1.18	0.316+1.16*C_L ns
t_r	*IN TO X	1.28	2.35	2.45	2.75	0.684+2.97*C_L ns
t_f		0.886	1.63	1.70	1.90	0.428+2.29*C_L ns
* Slowest input						

Switching characteristics

2–Input NAND Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 1.50 gates, 4 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

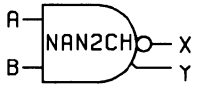
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.897	1.65	1.72	1.93	0.623+1.37*C_L ns
t_{PHL}		0.660	1.21	1.26	1.42	0.429+1.15*C_L ns
t_{PLH}	X TO Y	0.644	1.18	1.23	1.38	0.375+1.34*C_L ns
t_{PHL}		0.386	0.709	0.739	0.829	0.240+0.731*C_L ns
t_r	*IN TO X	1.67	3.07	3.20	3.59	1.09+2.93*C_L ns
t_f		1.18	2.16	2.25	2.53	0.727+2.25*C_L ns
t_r	X TO Y	1.12	2.05	2.14	2.40	0.542+2.87*C_L ns
t_f		0.809	1.48	1.55	1.74	0.569+1.20*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent on the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

2–Input NAND Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.206
B: 0.212 pF
Cell Size: 3.0 gates, 7 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

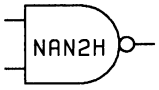
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.751	1.38	1.44	1.61	0.613+0.685*C_L ns
t_{PHL}		0.537	0.986	1.03	1.15	0.419+0.587*C_L ns
t_{PLH}	X TO Y	0.464	0.852	0.888	0.996	0.324+0.699*C_L ns
t_{PHL}		0.300	0.550	0.573	0.643	0.218+0.405*C_L ns
t_{PLH}	*IN TO Y	0.883	1.62	1.69	1.90	0.743+0.699*C_L ns
t_{PHL}		0.913	1.68	1.75	1.96	0.832+0.405*C_L ns
t_r	*IN TO X	1.33	2.44	2.54	2.85	1.03+1.48*C_L ns
t_f		0.924	1.70	1.77	1.98	0.704+1.09*C_L ns
t_r	X TO Y	0.818	1.50	1.57	1.76	0.528+1.45*C_L ns
t_f		0.698	1.28	1.34	1.50	0.565+0.661*C_L ns
t_r	*IN TO Y	0.818	1.50	1.57	1.76	0.528+1.45*C_L ns
t_f		0.698	1.28	1.34	1.50	0.565+0.661*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

2–Input NAND Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.206
B: 0.212 pF
Cell Size: 2.0 gates, 5 array sites



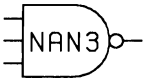
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.632	1.16	1.21	1.36	0.493+0.693*C_L ns
t_{PHL}		0.426	0.782	0.815	0.914	0.308+0.590*C_L ns
t_r	*IN TO X	0.959	1.76	1.83	2.06	0.655+1.52*C_L ns
t_f		0.746	1.37	1.43	1.60	0.524+1.11*C_L ns
* Slowest input						

Switching characteristics

3–Input NAND Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 1.50 gates, 4 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.893	1.64	1.71	1.92	0.616+1.38*C_L ns
t_{PHL}		0.840	1.54	1.61	1.80	0.515+1.62*C_L ns
t_r	*IN TO X	1.46	2.68	2.80	3.14	0.860+3.00*C_L ns
t_f		1.30	2.38	2.48	2.78	0.626+3.35*C_L ns
* Slowest input						

Switching characteristics

NAN3C

3–Input NAND Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

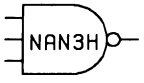
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.02	1.87	1.95	2.19	0.743+1.37*C_L ns
t_{PHL}		0.988	1.81	1.89	2.12	0.663+1.62*C_L ns
t_{PLH}	X TO Y	0.744	1.37	1.42	1.60	0.468+1.38*C_L ns
t_{PHL}		0.461	0.846	0.882	0.990	0.311+0.748*C_L ns
t_{PLH}	*IN TO Y	1.41	2.58	2.69	3.02	1.13+1.38*C_L ns
t_{PHL}		1.20	2.21	2.30	2.59	1.05+0.748*C_L ns
t_r	*IN TO X	2.02	3.71	3.87	4.34	1.45+2.83*C_L ns
t_f		1.83	3.36	3.50	3.93	1.18+3.25*C_L ns
t_r	X TO Y	1.40	2.57	2.68	3.01	0.871+2.65*C_L ns
t_f		0.846	1.55	1.62	1.82	0.599+1.23*C_L ns
t_r	*IN TO Y	1.40	2.57	2.68	3.01	0.871+2.65*C_L ns
t_f		0.846	1.55	1.62	1.82	0.599+1.23*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

3–Input NAND Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.206
B: 0.212
C: 0.215 pF
Cell Size: 3.0 gates, 7 array sites



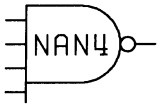
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.737	1.35	1.41	1.58	0.596+0.702*C_L ns
t_{PHL}		0.678	1.24	1.30	1.45	0.516+0.808*C_L ns
t_r	*IN TO X	1.25	2.29	2.38	2.68	0.953+1.46*C_L ns
t_f		1.07	1.96	2.04	2.29	0.738+1.64*C_L ns
* Slowest input						

Switching characteristics

4–Input NAND Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



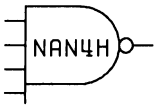
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.986	1.81	1.89	2.12	0.704+1.41*C_L ns
t_{PHL}		1.20	2.20	2.29	2.57	0.776+2.10*C_L ns
t_r	*IN TO X	1.86	3.41	3.56	3.99	1.29+2.85*C_L ns
t_f		1.98	3.64	3.79	4.25	1.12+4.30*C_L ns
* Slowest input						

Switching characteristics

4–Input NAND Gate (High Drive)

Inputs: A, B, C, D
Outputs: X
Input Cap.: A: 0.206
B: 0.209
C: 0.215
D: 0.218 pF
Cell Size: 4.0 gates, 9 array sites



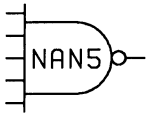
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.833	1.53	1.59	1.79	0.687+0.725*C_L ns
t_{PHL}		0.968	1.78	1.85	2.08	0.751+1.08*C_L ns
t_r	*IN TO X	1.41	2.60	2.71	3.04	1.12+1.49*C_L ns
t_f		1.43	2.63	2.74	3.08	0.994+2.19*C_L ns
* Slowest input						

Switching characteristics

5–Input NAND Gate

Inputs: A, B, C, D, E
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.50 gates, 6 array sites



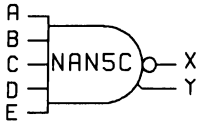
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.07	1.96	2.05	2.30	0.782+1.43*C_L ns
t_{PHL}		1.60	2.94	3.06	3.43	1.08+2.59*C_L ns
t_r	*IN TO X	2.11	3.87	4.04	4.53	1.53+2.88*C_L ns
t_f		2.58	4.73	4.94	5.54	1.49+5.44*C_L ns
* Slowest input						

Switching characteristics

5–Input NAND Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 3.0 gates, 7 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

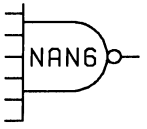
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.23	2.26	2.36	2.64	0.950+1.40*C_L ns
t_{PHL}		1.87	3.43	3.58	4.02	1.36+2.55*C_L ns
t_{PLH}	X TO Y	0.977	1.79	1.87	2.10	0.677+1.49*C_L ns
t_{PHL}		0.486	0.893	0.931	1.04	0.322+0.820*C_L ns
t_{PLH}	*IN TO Y	2.34	4.29	4.47	5.02	2.04+1.49*C_L ns
t_{PHL}		1.44	2.64	2.75	3.09	1.27+0.820*C_L ns
t_r	*IN TO X	2.38	4.36	4.54	5.10	1.78+2.98*C_L ns
t_f		3.23	5.94	6.19	6.94	2.14+5.45*C_L ns
t_r	X TO Y	1.93	3.55	3.70	4.15	1.43+2.52*C_L ns
t_f		1.16	2.13	2.22	2.49	0.947+1.06*C_L ns
t_r	*IN TO Y	1.93	3.55	3.70	4.15	1.43+2.52*C_L ns
t_f		1.16	2.13	2.22	2.49	0.947+1.06*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

6–Input NAND Gate

Inputs: A, B, C, D, E, F
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 3.0 gates, 7 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.15	2.11	2.20	2.47	0.858+1.46*C_L ns
t_{PHL}		2.14	3.93	4.10	4.60	1.53+3.03*C_L ns
t_r	*IN TO X	2.29	4.21	4.38	4.92	1.70+2.97*C_L ns
t_f		3.40	6.24	6.50	7.29	2.10+6.49*C_L ns
* Slowest input						

Switching characteristics

2–Input NOR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 1.0 gate, 3 array sites

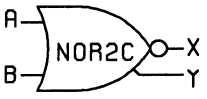
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.15	2.11	2.20	2.46	0.616+2.65*C_L ns
t_{PHL}		0.422	0.775	0.808	0.906	0.288+0.669*C_L ns
t_r	*IN TO X	2.08	3.81	3.98	4.46	0.908+5.84*C_L ns
t_f		0.730	1.34	1.40	1.57	0.486+1.22*C_L ns
* Slowest input						

Switching characteristics

2–Input NOR Gate with Complementary Outputs

Inputs: A, B
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 1.50 gates, 4 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

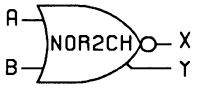
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.40	2.56	2.67	3.00	0.865+2.64*C_L ns
t_{PHL}		0.496	0.911	0.950	1.07	0.365+0.655*C_L ns
t_{PLH}	X TO Y	0.556	1.02	1.06	1.19	0.278+1.39*C_L ns
t_{PHL}		0.481	0.883	0.921	1.03	0.321+0.797*C_L ns
t_{PLH}	*IN TO Y	0.921	1.69	1.76	1.98	0.643+1.39*C_L ns
t_{PHL}		1.35	2.47	2.58	2.89	1.19+0.797*C_L ns
t_r	*IN TO X	2.68	4.93	5.14	5.76	1.49+5.96*C_L ns
t_f		0.862	1.58	1.65	1.85	0.626+1.18*C_L ns
t_r	X TO Y	1.02	1.87	1.95	2.18	0.415+3.00*C_L ns
t_f		0.987	1.81	1.89	2.12	0.751+1.18*C_L ns
t_r	*IN TO Y	1.02	1.87	1.95	2.18	0.415+3.00*C_L ns
t_f		0.987	1.81	1.89	2.12	0.751+1.18*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

2–Input NOR Gate with Complementary Outputs (High Drive)

Inputs: A, B
Outputs: X, Y
Input Cap.: A: 0.206
B: 0.212 pF
Cell Size: 3.0 gates, 7 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

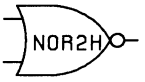
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.13	2.08	2.17	2.43	0.870+1.32*C_L ns
t_{PHL}		0.412	0.757	0.789	0.885	0.343+0.342*C_L ns
t_{PLH}	X TO Y	0.397	0.729	0.760	0.853	0.254+0.716*C_L ns
t_{PHL}		0.371	0.681	0.710	0.796	0.276+0.475*C_L ns
t_{PLH}	*IN TO Y	0.741	1.36	1.42	1.59	0.597+0.716*C_L ns
t_{PHL}		1.24	2.28	2.38	2.67	1.15+0.475*C_L ns
t_r	*IN TO X	2.23	4.09	4.26	4.78	1.64+2.91*C_L ns
t_f		0.736	1.35	1.41	1.58	0.632+0.520*C_L ns
t_r	X TO Y	0.686	1.26	1.31	1.47	0.378+1.54*C_L ns
t_f		0.815	1.50	1.56	1.75	0.688+0.629*C_L ns
t_r	*IN TO Y	0.686	1.26	1.31	1.47	0.378+1.54*C_L ns
t_f		0.815	1.50	1.56	1.75	0.688+0.629*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

2–Input NOR Gate (High Drive)

Inputs: A, B
Outputs: X
Input Cap.: A: 0.206
B: 0.212 pF
Cell Size: 2.0 gates, 5 array sites



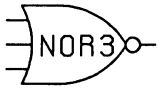
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.890	1.63	1.70	1.91	0.624+1.33*C_L ns
t_{PHL}		0.339	0.623	0.649	0.728	0.268+0.354*C_L ns
t_r	*IN TO X	1.35	2.47	2.57	2.89	0.751+2.96*C_L ns
t_f		0.674	1.24	1.29	1.45	0.571+0.514*C_L ns
* Slowest input						

Switching characteristics

3–Input NOR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 1.50 gates, 4 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.89	3.47	3.61	4.05	1.10+3.94*C_L ns
t_{PHL}		0.464	0.852	0.888	0.996	0.332+0.655*C_L ns
t_r	*IN TO X	3.28	6.02	6.28	7.05	1.50+8.91*C_L ns
t_f		0.848	1.56	1.62	1.82	0.608+1.20*C_L ns
* Slowest input						

Switching characteristics

NOR3C

3–Input NOR Gate with Complementary Outputs

Inputs: A, B, C
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

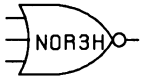
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.13	3.90	4.07	4.56	1.36+3.84*C_L ns
t_{PHL}		0.490	0.899	0.937	1.05	0.364+0.626*C_L ns
t_{PLH}	X TO Y	0.553	1.02	1.06	1.19	0.275+1.39*C_L ns
t_{PHL}		0.482	0.885	0.922	1.03	0.284+0.986*C_L ns
t_{PLH}	*IN TO Y	0.917	1.68	1.76	1.97	0.639+1.39*C_L ns
t_{PHL}		1.84	3.38	3.52	3.95	1.64+0.986*C_L ns
t_r	*IN TO X	4.42	8.11	8.45	9.48	2.65+8.83*C_L ns
t_f		0.820	1.51	1.57	1.76	0.578+1.21*C_L ns
t_r	X TO Y	1.01	1.86	1.94	2.17	0.415+2.99*C_L ns
t_f		1.46	2.68	2.80	3.14	1.25+1.08*C_L ns
t_r	*IN TO Y	1.01	1.86	1.94	2.17	0.415+2.99*C_L ns
t_f		1.46	2.68	2.80	3.14	1.25+1.08*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for Y is dependent upon the X output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

3–Input NOR Gate (High Drive)

Inputs: A, B, C
Outputs: X
Input Cap.: A: 0.206
B: 0.212
C: 0.215 pF
Cell Size: 3.0 gates, 7 array sites



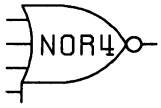
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.47	2.70	2.82	3.16	1.08+1.98*C_L ns
t_{PHL}		0.383	0.703	0.733	0.822	0.312+0.355*C_L ns
t_r	*IN TO X	2.31	4.23	4.41	4.95	1.40+4.54*C_L ns
t_f		0.738	1.35	1.41	1.58	0.633+0.521*C_L ns
* Slowest input						

Switching characteristics

4–Input NOR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



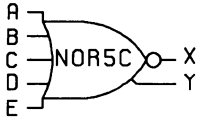
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.86	5.25	5.47	6.14	1.80+5.27*C_L ns
t_{PHL}		0.493	0.904	0.942	1.06	0.375+0.585*C_L ns
t_r	*IN TO X	4.94	9.07	9.46	10.6	2.56+11.9*C_L ns
t_f		0.915	1.68	1.75	1.96	0.662+1.26*C_L ns
* Slowest input						

Switching characteristics

5–Input NOR Gate with Complementary Outputs

Inputs: A, B, C, D, E
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 3.50 gates, 9 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO Y	1.25	2.29	2.39	2.68	0.971+1.38*C_L ns
t_{PHL}		3.85	7.07	7.37	8.27	3.60+1.23*C_L ns
t_{PLH}	Y TO X	0.672	1.23	1.29	1.44	0.385+1.43*C_L ns
t_{PHL}		0.430	0.789	0.823	0.923	0.297+0.665*C_L ns
t_{PLH}	*IN TO X	4.28	7.85	8.18	9.18	3.99+1.43*C_L ns
t_{PHL}		1.40	2.57	2.68	3.01	1.27+0.665*C_L ns
t_r	*IN TO Y	1.60	2.93	3.06	3.43	1.04+2.81*C_L ns
t_f		2.08	3.82	3.98	4.47	1.81+1.32*C_L ns
t_r	Y TO X	1.90	3.49	3.63	4.08	1.41+2.44*C_L ns
t_f		0.788	1.45	1.51	1.69	0.550+1.19*C_L ns
t_r	*IN TO X	1.90	3.49	3.63	4.08	1.41+2.44*C_L ns
t_f		0.788	1.45	1.51	1.69	0.550+1.19*C_L ns
* Slowest input						

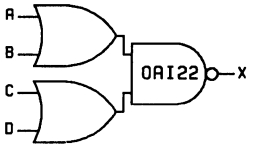
Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

OAI22

2–2 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



$X = \overline{(A+B) \bullet (C+D)}$

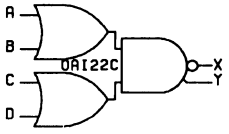
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.26	2.32	2.42	2.71	0.735+2.64*C_L ns
t_{PHL}		0.656	1.20	1.25	1.41	0.423+1.16*C_L ns
t_r	*IN TO X	2.14	3.92	4.09	4.59	0.948+5.94*C_L ns
t_f		1.18	2.16	2.25	2.52	0.719+2.28*C_L ns
* Slowest input						

Switching characteristics

2–2 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 3.0 gates, 8 array sites



$X = \overline{(A+B) \cdot (C+D)}$

$Y = (A+B) \cdot (C+D)$

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

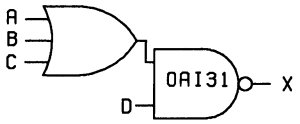
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO Y	1.38	2.54	2.65	2.97	1.11+1.35*C_L ns
t_{PHL}		1.53	2.81	2.93	3.29	1.36+0.862*C_L ns
t_{PLH}	Y TO X	0.714	1.31	1.37	1.53	0.455+1.29*C_L ns
t_{PHL}		0.428	0.785	0.819	0.919	0.288+0.698*C_L ns
t_{PLH}	*IN TO X	2.07	3.81	3.97	4.45	1.81+1.29*C_L ns
t_{PHL}		1.54	2.83	2.95	3.31	1.40+0.698*C_L ns
t_r	*IN TO Y	1.60	2.93	3.05	3.43	1.03+2.83*C_L ns
t_f		1.42	2.60	2.71	3.04	1.22+0.974*C_L ns
t_r	Y TO X	1.45	2.65	2.77	3.10	0.906+2.69*C_L ns
t_f		1.04	1.90	1.98	2.23	0.828+1.04*C_L ns
t_r	*IN TO X	1.45	2.65	2.77	3.10	0.906+2.69*C_L ns
t_f		1.04	1.90	1.98	2.23	0.828+1.04*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays and delay equation listed for "IN TO X" assume no load on the Y output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

3–1 OR–AND–Invert

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



$X = \overline{(A+B+C) \bullet D}$

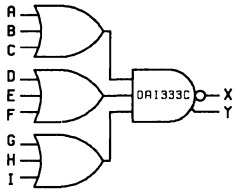
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	2.36	4.34	4.52	5.08	1.58+3.92*C_L ns
t_{PHL}		0.711	1.31	1.36	1.53	0.482+1.14*C_L ns
t_r	*IN TO X	3.91	7.19	7.49	8.40	2.16+8.78*C_L ns
t_f		1.21	2.21	2.31	2.59	0.749+2.28*C_L ns
* Slowest input						

Switching characteristics

3–3–3 OR–AND–Invert with Complementary Outputs

Inputs: A, B, C, D, E, F, G, H, I
Outputs: X, Y
Input Cap.: All: 0.102 pF
Cell Size: 5.50 gates, 13 array sites



$X = \overline{(A+B+C) * (D+E+F) * (G+H+I)}$
$Y = (A+B+C) * (D+E+F) * (G+H+I)$

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

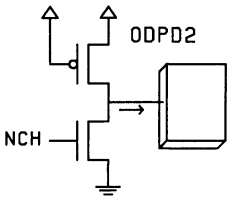
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO Y	2.75	5.05	5.26	5.90	2.46+1.43*C_L ns
t_{PHL}		4.05	7.43	7.75	8.69	3.76+1.42*C_L ns
t_{PLH}	Y TO X	0.755	1.39	1.45	1.62	0.465+1.45*C_L ns
t_{PHL}		0.190	0.348	0.363	0.407	0.000+0.947*C_L ns
t_{PLH}	*IN TO X	4.52	8.30	8.65	9.71	4.23+1.45*C_L ns
t_{PHL}		2.65	4.87	5.07	5.69	2.46+0.947*C_L ns
t_r	*IN TO Y	2.02	3.71	3.86	4.33	1.46+2.78*C_L ns
t_f		2.50	4.58	4.78	5.36	2.21+1.41*C_L ns
t_r	Y TO X	1.94	3.56	3.71	4.17	1.45+2.46*C_L ns
t_f		1.63	2.99	3.12	3.50	1.47+0.775*C_L ns
t_r	*IN TO X	1.94	3.56	3.71	4.17	1.45+2.46*C_L ns
t_f		1.63	2.99	3.12	3.50	1.47+0.775*C_L ns
* Slowest input						

Switching characteristics

NOTE:
The propagation delay for X is dependent upon the Y output delay. The delays and delay equation listed for "IN TO Y" assume no load on the X output. To calculate delays for other loading conditions, see *Calculating Standard Cell and Gate Array Timings* application note.

2mA 5V Open–Drain Output Pad

ODPD2 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.966 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	115	211	219	246	17.9+1.93*C_L ns
t_{PHL}		5.71	10.5	10.9	12.3	0.705+0.100*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

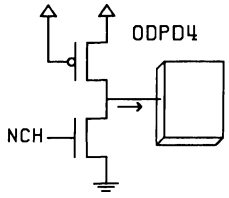
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

4mA 5V Open–Drain Output Pad

ODPD4 is an inverting, open–drain output pad which can have up to 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.819 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	118	217	226	253	20.2+1.96*C_L ns
t_{PHL}		2.88	5.29	5.52	6.19	0.308+0.051*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

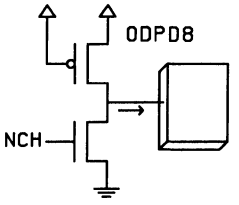
DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

ODPD8

8mA 5V Open–Drain Output Pad

ODPD8 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 3.524 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	123	225	235	263	24.4+1.96*C_L ns
t_{PHL}		1.46	2.68	2.79	3.13	0.157+0.026*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

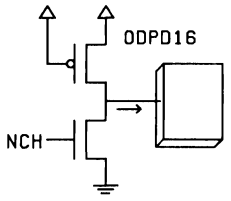
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

16mA 5V Open–Drain Output Pad

ODPD16 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 6.082 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	128	236	246	276	29.1+1.98*C_L ns
t_{PHL}		0.861	1.58	1.65	1.85	0.138+0.014*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

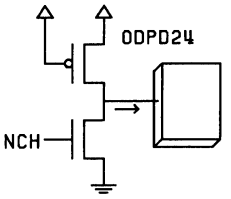
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

24mA 5V Open–Drain Output Pad

ODPD24 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 8.640 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

*ODPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	134	245	256	287	33.3+2.00*C_L ns
t_{PHL}		0.589	1.08	1.13	1.27	0.127+0.009*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

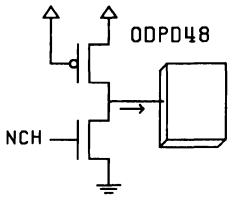
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

48mA 5V Open–Drain Output Pad

ODPD48 is an inverting open–drain output pad which can have up to a 5V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 17.167 pF
Cell Size: 10.0 gates
2 pad sites (high drive pads)
3 pad sites (high count pads)*

*ODPD48 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	159	292	305	342	53.8+2.11*C_L ns
t_{PHL}		0.341	0.627	0.653	0.733	0.110+0.005*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	48.00	mA

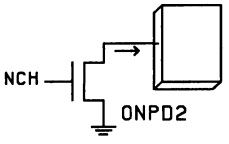
DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

ONPD2

2mA 7V Open–Drain Output Pad

ONPD2 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 0.966 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	109	200	208	234	12.1+1.93*C_L ns
t_{PHL}		5.38	9.87	10.3	11.5	0.230+0.103*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

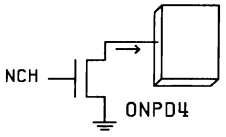
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	2.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

4mA 7V Open–Drain Output Pad

ONPD4 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 1.819 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	112	205	214	240	14.7+1.94*C_L ns
t_{PHL}		2.71	4.97	5.18	5.81	0.132+0.051*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	4.00	mA

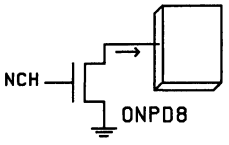
DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

ONPD8

8mA 7V Open–Drain Output Pad

ONPD8 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 3.524 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	117	215	224	251	17.8+1.98*C_L ns
t_{PHL}		1.36	2.50	2.60	2.92	0.087+0.025*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

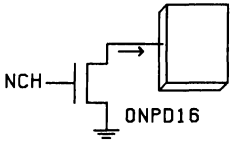
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	8.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

16mA 7V Open–Drain Output Pad

ONPD16 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 6.082 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	123	225	235	264	22.7+2.00*C_L ns
t_{PHL}		0.781	1.43	1.49	1.68	0.058+0.014*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

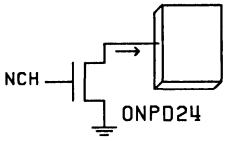
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	16.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

24mA 7V Open–Drain Output Pad

ONPD24 is an inverting open–drain output pad which can have up to a 7V output voltage through an external pullup. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH
Outputs: PAD
Input Cap.: NCH: 8.640 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

* ONPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	NCH TO PAD	127	233	243	273	26.7+2.01*C_L ns
t_{PHL}		0.554	1.02	1.06	1.19	0.091+0.009*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

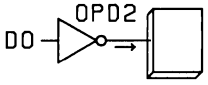
PARAMETER	CONDITION	MINIMUM	UNIT
I_{OL} (low level output current)	V_{OL} = 0.4V	24.00	mA

DC specifications

NOTE:
The T_{PLH} shown for the output was derived using a 10K pullup resistor from the output to V_{DD} and a 50pF load from the output to ground.

2mA Output Pad

OPD2 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 1.850 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	8.44	15.5	16.1	18.1	1.38+0.141*C_L ns
t_{PHL}		3.69	6.77	7.05	7.92	0.562+0.062*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

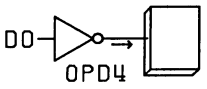
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

OPD4

4mA Output Pad

OPD4 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 3.555 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	4.30	7.89	8.23	9.23	0.740+0.071*C_L ns
t_{PHL}		1.91	3.50	3.65	4.09	0.314+0.032*C_L ns

Switching characteristics

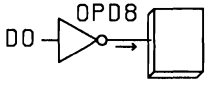
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Output Pad

OPD8 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 6.965 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	2.38	4.36	4.55	5.10	0.582+0.036*C_L ns
t_{PHL}		1.13	2.07	2.16	2.42	0.346+0.016*C_L ns

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

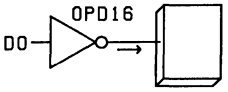
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−4.00	mA

DC specifications

OPD16

16mA Output Pad

OPD16 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 12.081 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	1.35	2.47	2.57	2.89	0.275+0.021*C_L ns
t_{PHL}		0.605	1.11	1.16	1.30	0.142+0.009*C_L ns

Switching characteristics

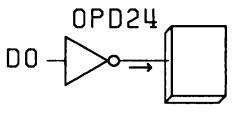
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Output Pad

OPD24 is an inverting output pad. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: DO
Outputs: PAD
Input Cap.: DO: 17.197 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

*OPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	DO TO PAD	0.972	1.79	1.86	2.09	0.249+0.014*C_L ns
t_{PHL}		0.444	0.815	0.849	0.953	0.125+0.006*C_L ns

Switching characteristics

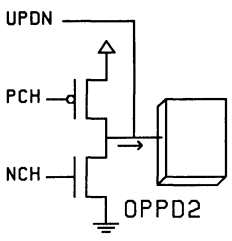
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

2mA Tristate Output Pad with Pullup/Pulldown Port

OPPD2 is similar to OTPD2 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 0.966
PCH: 0.853
UPDN: 59.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	4.81	8.84	9.21	10.3	0.821+0.080*C_L ns
t_{PHL}		5.72	10.5	10.9	12.3	1.09+0.092*C_L ns
* NCH or PCH						

Switching characteristics

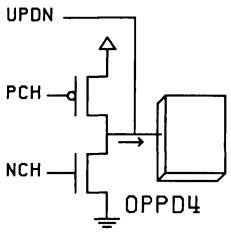
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad with Pullup/Pulldown Port

OPPD4 is similar to OTPD4 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 1.819
PCH: 1.705
UPDN: 59.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	2.49	4.58	4.77	5.35	0.467+0.040*C_L ns
t_{PHL}		2.96	5.44	5.67	6.37	0.535+0.049*C_L ns
* NCH or PCH						

Switching characteristics

(Worst Case Process, V_{DD}=4.5V, T_A=70C)

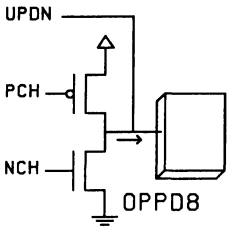
PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

OPPD8

8mA Tristate Output Pad with Pullup/Pulldown Port

OPPD8 is similar to OTPD8 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 3.524
PCH: 3.411
UPDN: 59.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.31	2.41	2.51	2.82	0.299+0.020*C_L ns
t_{PHL}		1.52	2.80	2.92	3.27	0.309+0.024*C_L ns
* NCH or PCH						

Switching characteristics

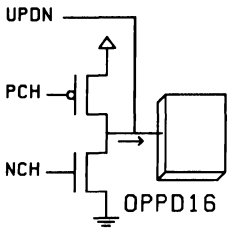
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC specifications

16mA Tristate Output Pad with Pullup/Pulldown Port

OPPD16 is similar to OTPD16 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 6.082
PCH: 5.968
UPDN: 59.670 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.806	1.48	1.54	1.73	0.228+0.012*C_L ns
t_{PHL}		0.872	1.60	1.67	1.87	0.206+0.013*C_L ns
* NCH or PCH						

Switching characteristics

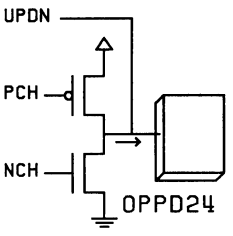
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-8.00	mA

DC specifications

24mA Tristate Output Pad with Pullup/Pulldown Port

OPPD24 is similar to OTPD24 but includes an input port called UPDN. This input must be driven by a PPUxxx or PPDxxx cell. See PPU/PPD data sheet for pullup/pulldown current information.



Inputs: NCH, PCH, UPDN
Outputs: PAD
Input Cap.: NCH: 8.640
PCH: 8.526
UPDN: 59.670 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

* OPPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.600	1.10	1.15	1.29	0.195+0.008*C_L ns
t_{PHL}		0.673	1.24	1.29	1.44	0.152+0.010*C_L ns
* NCH or PCH						

Switching characteristics

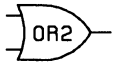
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−12.00	mA

DC specifications

2–Input OR Gate

Inputs: A, B
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 1.50 gates, 4 array sites



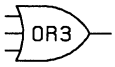
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.886	1.63	1.70	1.90	0.608+1.39*C_L ns
t_{PHL}		1.35	2.47	2.58	2.89	1.19+0.792*C_L ns
t_r	*IN TO X	1.02	1.87	1.95	2.18	0.415+3.00*C_L ns
t_f		0.987	1.81	1.89	2.12	0.751+1.18*C_L ns
* Slowest input						

Switching characteristics

3–Input OR Gate

Inputs: A, B, C
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.0 gates, 5 array sites



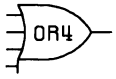
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	0.968	1.78	1.85	2.08	0.691+1.38*C_L ns
t_{PHL}		2.00	3.68	3.83	4.30	1.81+0.938*C_L ns
t_r	*IN TO X	0.993	1.82	1.90	2.13	0.387+3.03*C_L ns
t_f		1.48	2.72	2.84	3.18	1.26+1.10*C_L ns
* Slowest input						

Switching characteristics

4–Input OR Gate

Inputs: A, B, C, D
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 2.50 gates, 6 array sites



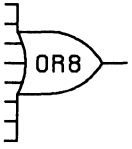
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.000	1.84	1.92	2.16	0.723+1.40*C_L ns
t_{PHL}		2.72	4.99	5.20	5.83	2.47+1.20*C_L ns
t_r	*IN TO X	0.977	1.79	1.87	2.10	0.368+3.04*C_L ns
t_f		1.85	3.40	3.54	3.97	1.62+1.14*C_L ns
* Slowest input						

Switching characteristics

8–Input OR Gate

Inputs: A, B, C, D, E, F, G, H
Outputs: X
Input Cap.: All: 0.102 pF
Cell Size: 5.0 gates, 12 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO X	1.16	2.13	2.22	2.49	0.882+1.40*C_L ns
t_{PHL}		3.03	5.56	5.79	6.50	2.74+1.40*C_L ns
t_r	*IN TO X	1.36	2.50	2.61	2.93	0.781+2.90*C_L ns
t_f		1.96	3.59	3.74	4.20	1.57+1.93*C_L ns
* Slowest input						

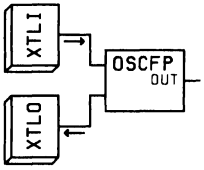
Switching characteristics

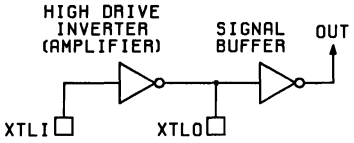
General Purpose Oscillator – Free Placement

- 1 to 50 MHz operation
- 35% to 65% output duty cycle
- Buffered on–chip output

Inputs: XTLI
Outputs: OUT, XTLO
Input Cap.: XTLI: 11.904 pF
Cell Size: 5.50 gates, 2 pad sites
Output Cap.: XTLO: 0.07 pF
Kit Part: Lindsey C

*See important note on last page of this data sheet regarding operation below 3 MHz.





OSCFP functional diagram

OSCFP is a general purpose crystal oscillator cell capable of operation from 1 MHz to over 50 MHz. • Fundamental mode applications require one or two external resistors and two external tuning capacitors. Operation above 25 MHz usually requires a third overtone crystal and additional components to form a frequency selective circuit. A parallel resonant type crystal should always be specified.

The OSCFP is built from any two I/O pad cells and therefore may be located at any two adjacent pad locations; however, both pads must be on the same side of the chip. (Contact your NCR applications engineer for more information.) Preferred locations are near the center of any side of the packaged part to minimize bondwire and leadframe parasitics. This is especially important in DIP packages. It is also desirable to place power (V_{DD}) and ground (V_{SS}) pins near the oscillator especially at frequencies above 25 MHz. A short ground trace must be used from the V_{SS} pin(s) to the external tuning capacitors C_1 and C_2.

To drive external circuits with an oscillator generated clock, the on–chip oscillator output (OUT) should drive a buffer and a separate output pad such as an OPD4. The oscillator output, XTLO, should not normally be used to drive external circuits except the oscillator components.

Figures 1 and 2 show the external components required to bias the inverter and for the crystal pi network. R_B causes the inverter to self bias to approximately $V_{DD}/2$. This is a point where the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B is chosen in the range of 1–20 MΩ such that it will not affect the AC performance of the circuit.

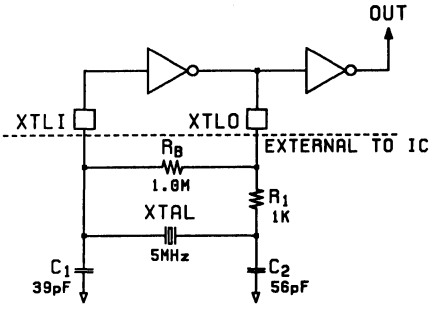


Figure 1 Typical fundamental mode circuit

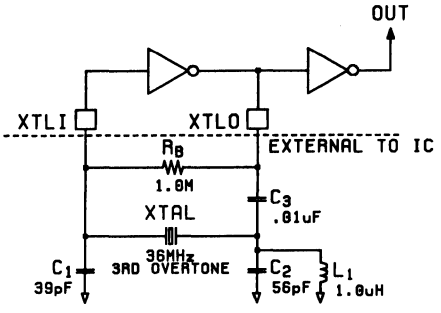


Figure 2 Typical third overtone circuit

C_1 and C_2 along with the crystal forms a pi network which resonates at the specified crystal frequency. The ratio C_2/C_1 should be somewhat greater than unity since it is a term in the loop gain equation. Increasing the ratio too much will cause the voltage swing on XTLI to exceed the supply rails which is undesirable. Typically $1.1 < (C_2/C_1) < 1.5$. The series combination of C_2 and C_1 should be approximately equal to the *load capacitance* specified for the quartz crystal. The strays associated with each node, and the oscillator input and output capacitance should be included in calculations which involve C_2 and C_1. Typical component values are shown in Figures 1 and 2.

Example calculation:

$C_{1\ total}$ = Input C + parasitic C + C_1
= 13.56 + 5.0 + 39 = 57.56 pF

$C_{2\ total}$ = Output C + parasitic C + C_2
= 9.07 + 5.0 + 56 = 70.07 pF

$C_{2\ total} / C_{1\ total} = 1.22$

C_{LOAD} = (57.56 x 70.07) / (57.56 + 70.07)
= 31.6 pF

An exact analysis would need to include the effect of R_1 between the oscillator output and the crystal. The method shown is a reasonable approximation. The crystal load capacitance can be specified as 32 pF which is the closest standard value.

The output resistance of the oscillator core, along with C_2, forms an RC low pass circuit. This pole contributes additional phase shift to insure a greater than 360 degree phase shift around the loop, which is required for oscillation. At lower oscillator frequencies, it may be necessary to add a resistor, R_1, in series with the output to add phase shift at a lower frequency and insure oscillator startup and stability. This is most important in the 1–20MHz region. Typical values for R_1 are shown in Table 2. At frequencies above 25 MHz, R_1 can usually be omitted. R_1 also reduces the drive to the crystal and thus crystal power dissipation.

To achieve overtone oscillation, the fundamental frequency must be suppressed by making the loop gain lower at the fundamental frequency compared to the third harmonic frequency. An overtone crystal will resonate at its fundamental frequency unless the loop gain is forced to be higher at the harmonic frequency. Loop gain must be less than one at the fundamental and greater than one at the desired overtone frequency.

The additional components necessary for overtone operation are a coupling capacitor and an inductor. The coupling capacitor is simply a DC block so the inductor does not short the inverter output to ground. The inductor, L_1, is selected such that its impedance lowers the loop gain at the fundamental frequency relative to the third harmonic. Some experimentation with component values should be anticipated prior to specifying final production values.

The XTLI input can be driven with an external source with XTLO left unconnected. The maximum operating frequency is no longer 50MHz but is determined by the load on XTLO, which is several picofarads even when the package pin is not connected. The reason for this is that as an oscillator, C_2 is part of the resonant pi circuit so it does not look like a pure load capacitance as it does when the inverter is driven without the crystal. For simulation purposes, the XTLI to XTLO propagation delay is zero. In production test, the XTLO pin will be driven with the complement of the XTLI test signal. This is transparent to the designer. Any application of the oscillator cell in which the input is driven should be first reviewed with an NCR applications engineer.

The OSCFP is a Pierce type oscillator circuit in which the crystal is operated in its parallel resonant mode. (Refer to the crystal equivalent circuit – Figure 3.) At parallel resonance, the LRC leg appears slightly inductive and resonates with C_0 and the circuit load capacitances, C_1 and C_2. Typical equivalent circuit component values are shown in Table 1. The values should only be used as a guideline in selecting a crystal for your application.

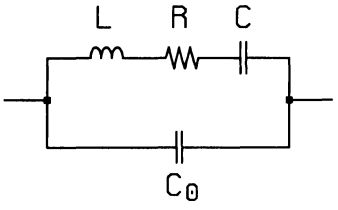


Figure 3 Crystal equivalent circuit

The graph in Figure 4 shows typical supply current as a function of frequency. It represents the average of measurements made at 16 frequencies using crystals from several different vendors. The typical component values shown in Table 2 and Figures 1 and 2 were used in the test circuit. The circuit shown in Figure 1 was used with fundamental mode crystals from 1–22 MHz. The circuit shown in Figure 2 was used for overtone measurements from 25–50 MHz.

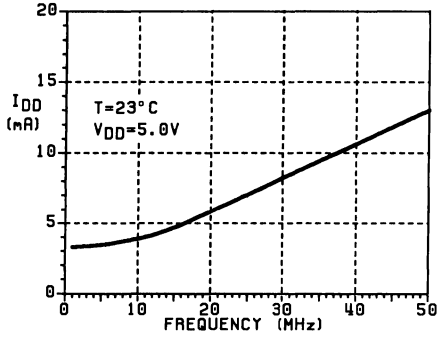


Figure 4 Typical supply current versus frequency

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	XTLI TO OUT	0.246	0.452	0.471	0.529	0.228+0.092*C_L ns
t_{PHL}		0.359	0.660	0.688	0.772	0.343+0.079*C_L ns
t_r	XTLI TO OUT	0.507	0.932	0.971	1.09	0.487+0.099*C_L ns
t_f		0.480	0.881	0.919	1.03	0.473+0.031*C_L ns

Switching characteristics

Crystal Frequency	L	C	C_0	R
1 MHz	3082 mH	8.223 fF	4.230 pF	575 Ω
1 MHz	2960 mH	8.560 fF	4.615 pF	255 Ω
2 MHz	732.5 mH	8.648 fF	3.918 pF	28 Ω
2 MHz	987.4 mH	6.416 fF	3.105 pF	122 Ω
5 MHz	56.36 mH	17.99 fF	4.451 pF	12 Ω
10 MHz	10.64 mH	23.83 fF	5.998 pF	14 Ω
20 MHz	3.042 mH	20.81 fF	5.310 pF	6.7 Ω

TABLE 1 Typical measured crystal parameters (Represents several manufacturers' AT cut crystals)

Frequency	R1
1 MHz	2 k–5 kΩ
2 MHz	2 kΩ
5 MHz	1 kΩ
10 MHz	500 Ω
20 MHz	200 Ω

TABLE 2 Typical values for R1 in Figure 1

Suggested References:

Crystal Oscillator Design And Temperature Compensation by Marvin Frerking

Design Of Crystal And Other Harmonic Oscillators by Benjamin Parzen

*NOTE REGARDING OPERATION AT LESS THAN 3 MHz:

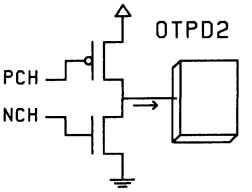
Operation in the range from 1.0–2.9 MHz is discouraged due to limitations of many quartz crystals in that frequency range. The physical size of the quartz blank must be made smaller than the optimum in order to fit into a reasonable standard size package. The result is that non–harmonic modes may be present which vary with temperature and may cause the frequency of oscillation to shift. All modes other than the desired fundamental must be down at least 6 dB to insure oscillation at the correct frequency. This means that the equivalent series resistance of undesired modes must be twice that of the fundamental mode.

Most vendors show a 6 dB or better specification in their data sheets. In practice, non–harmonic modes have been observed to become the dominate mode

(lowest resistance) as a function of temperature, sometimes over a range of only a few degrees centrigrade. For this reason, NCR recommends using a crystal above 2.9 MHz and dividing down to the desired frequency with on-chip flip-flops.

2mA Tristate Output Pad

OTPD2 is an output pad capable of output currents up to 2mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 0.966
PCH: 0.853 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	4.79	8.80	9.17	10.3	0.802+0.080*C_L ns
t_{PHL}		5.69	10.5	10.9	12.2	1.06+0.092*C_L ns
* NCH or PCH						

Switching characteristics

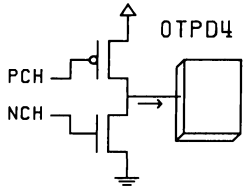
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	2.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−1.00	mA

DC specifications

4mA Tristate Output Pad

OTPD4 is an output pad capable of output currents up to 4mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 1.819
PCH: 1.705 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	2.48	4.56	4.75	5.33	0.458+0.040*C_L ns
t_{PHL}		2.95	5.42	5.65	6.34	0.524+0.049*C_L ns
* NCH or PCH						

Switching characteristics

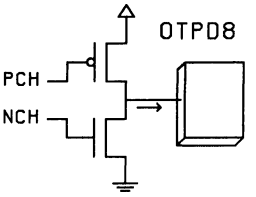
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	4.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−2.00	mA

DC specifications

8mA Tristate Output Pad

OTPD8 is an output pad capable of output currents up to 8mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 3.524
PCH: 3.411 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	1.31	2.40	2.50	2.81	0.294+0.020*C_L ns
t_{PHL}		1.52	2.79	2.91	3.26	0.303+0.024*C_L ns
* NCH or PCH						

Switching characteristics

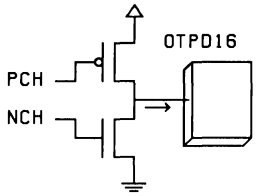
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	8.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-4.00	mA

DC specifications

16mA Tristate Output Pad

OTPD16 is an output pad capable of output currents up to 16mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 6.082
PCH: 5.968 pF
Cell Size: 5.0 gates, 1 pad site

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.804	1.48	1.54	1.73	0.225+0.012*C_L ns
t_{PHL}		0.869	1.60	1.66	1.87	0.203+0.013*C_L ns
* NCH or PCH						

Switching characteristics

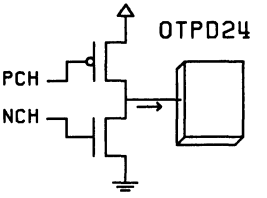
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	16.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}−0.5V	−8.00	mA

DC specifications

24mA Tristate Output Pad

OTPD24 is an output pad capable of output currents up to 24mA. For buffer selection and usage, see application notes Cell Selection and Usage, and Buffer Selection for Pad Cells.



Inputs: NCH, PCH
Outputs: PAD
Input Cap.: NCH: 8.640
PCH: 8.526 pF
Cell Size: 5.0 gates
1 pad site (high drive pads)
2 pad sites (high count pads)*

* OTPD24 pads have unique packaging and ground pad requirements. Please contact your NCR Field Applications Engineer for help in defining acceptable pin placements.

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*IN TO PAD	0.598	1.10	1.14	1.28	0.192+0.008*C_L ns
t_{PHL}		0.669	1.23	1.28	1.44	0.149+0.010*C_L ns
* NCH or PCH						

Switching characteristics

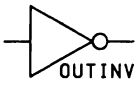
(Worst Case Process, V_{DD}=4.5V, T_A=70C)

PARAMETER	CONDITION	MINIMUM	UNIT
I_{ol} (low level output current)	V_{ol} = 0.4V	24.00	mA
I_{oh} (high level output current)	V_{oh} = V_{DD}-0.5V	-12.00	mA

DC specifications

Output Inverter

Inputs: A
Outputs: X
Input Cap.: A: 0.414 pF
Cell Size: 2.0 gates, 5 array sites



(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

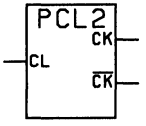
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.391	0.718	0.749	0.840	0.316+0.373*C_L ns
t_{PHL}		0.177	0.324	0.338	0.379	0.129+0.238*C_L ns
t_r	A TO X	0.711	1.30	1.36	1.53	0.601+0.548*C_L ns
t_f		0.571	1.05	1.09	1.22	0.531+0.194*C_L ns

Switching characteristics

PCL2

Two–Phase Clock Driver

PCL2 is for use with clocked cells and to produce high drive signals of true and complement value. CK is the noninverted or true output and CKB is the inverted or complement output.



Inputs: CL
Outputs: CK, CKB
Input Cap.: CL: 0.221 pF
Cell Size: 6.0 gates, 13 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

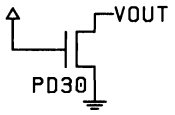
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	CL TO CK	0.902	1.66	1.73	1.94	0.827+0.373*C_L ns
t_{PHL}		1.17	2.15	2.24	2.51	1.12+0.259*C_L ns
t_{PLH}	CL TO CKB	1.46	2.69	2.80	3.14	1.38+0.383*C_L ns
t_{PHL}		1.10	2.02	2.11	2.37	1.05+0.253*C_L ns
t_r	CL TO CK	0.740	1.36	1.42	1.59	0.593+0.730*C_L ns
t_f		0.821	1.51	1.57	1.76	0.725+0.472*C_L ns
t_r	CL TO CKB	0.932	1.71	1.78	2.00	0.832+0.494*C_L ns
t_f		0.747	1.37	1.43	1.60	0.673+0.367*C_L ns

Switching characteristics

30μA N–Channel Pulldown Device

PD30 is a weak n–channel pulldown that sinks 30mA when VOUT equals five volts and can be used as a pulldown on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See the PPD200, PPD400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.

This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.



*NOTE: The gate input on the PD30 cannot be used to turn the transistor on or off.

Inputs:
Outputs: VOUT
Input Cap.:
Output Cap.: VOUT: 0.190 pF
Cell Size: 3.25 gates, 9 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	*VOUT	23.1	42.3	44.1	49.5	9.63+67.0*C_L ns
t_f	*VOUT	50.0	91.8	95.7	107	28.3+108*C_L ns
* Timing is from VOUT = 4.5V to VOUT = 2.25V						

Switching characteristics

(V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	30μA typical

Electrical characteristics

Power on Reset

Features:

- No external components required
- Retriggerable reset under digital control
- Supply glitch immunity

POR is a digital cell that guarantees a logic low level during power up for the purpose of resetting logic elements to known states. Upon application of the positive supply voltage to the device, POR causes SYS to remain low for approximately 2μs after the positive supply has exceeded 2.5V. This ensures that all digital circuits are operational before the SYS output goes high. An additional input is supplied to the cell which allows the output to be retriggered under external control.

FUNCTION TABLE

V_{DD}	RES	SYS
↑	L	⌐
X	H	L
H	↓	⌐

Inputs: RES
Outputs: SYS
Input Cap.: RES: 0.098 pF
Cell Size: 3.25 gates, 150 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	RES TO SYS	2378	4367	4552	5107	2304+363*C_L ns
t_{PHL}		9.13	16.8	17.5	19.6	8.45+3.37*C_L ns
t_r	RES TO SYS	96.9	178	185	208	96.0+4.30*C_L ns
t_f		7.16	13.1	13.7	15.4	6.34+4.05*C_L ns

Switching characteristics

Application Notes

Reset Timing

The POR cell is not designed for applications requiring precise reset intervals. The duration of the SYS output pulse in a power up condition, or after an external reset input, may vary from the nominal specified timing by 30% or more. Further variations in pulse duration will be observed over varying conditions of supply voltage and temperature. For applications requiring precise timing of a reset signal, an approach utilizing a clocked counter chain is recommended.

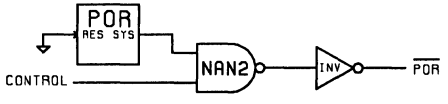
No relationship exists between the POR SYS output pulse and the start up time of any crystal oscillator in the NCR standard cell library. In general, the multi-megahertz oscillator cell, OSCP, will require anywhere from 1ms to 20ms to reach stable operation after power is applied.

POR provides a certain degree of input glitch immunity. The table given below describes the various situations and responses.

CONDITIONS	RESPONSE
* Glitch-free supply ramp * Supply glitch settles to $V_{DD} \leq 2.4V$ for at least 100µs	Sys output high occurs after VDD = 2.5V + 7.4µs
*Supply glitch settles to V_{DD} 2.9V *Supply glitch settles to V_{DD} 2.4V for less than 100µs	Will not effect SYS output of POR

Testability

NCR requires a chip be simulated and tested with the reset time out feature of the POR disabled. To achieve this, the RESET input on the POR should be grounded, and the POR output should be NANDed with a control signal. The control signal should be accessible by the tester during test time at probe and after the chip is packaged. A static pullup may be connected to the control signal path to enable the reset circuit under normal operation. NCR will review the specific implementation of any circuit using the POR at the time of the design review.



Reset circuit

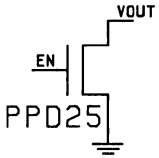
System Considerations

The NCR POR cell is designed to provide a reset pulse that can be used throughout the chip. If this signal is brought off chip for a system reset, precautions should be taken to insure that all other chips are powered up and functional while the reset pulse is valid.

Only one POR can be used per design. Contact your NCR applications engineer for more information.

25μA N–Channel Pulldown Device

PPD25 is a weak n–channel pulldown that sinks 25μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD25 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.051 pF
Output Cap.: VOUT: 0.190 pF
Cell Size: 3.25 gates, 9 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	5633	10342	10780	12095	8.50+112*C_L ns

Switching characteristics

(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

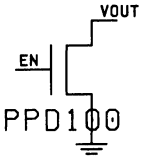
PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	25μA typical

Electrical characteristics

PPD100

100μA N–Channel Pulldown Device

PPD100 is a weak n–channel pulldown that sinks 100μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD100 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.102 pF
Output Cap.: VOUT: 0.190 pF
Cell Size: 2.25 gates, 8 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	1428	2623	2734	3067	0.000+28.6*C_L ns

Switching characteristics

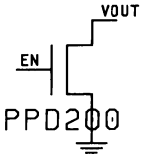
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	100μA typical

Electrical characteristics

200μA N–Channel Pulldown Device

PPD200 is a weak n–channel pulldown that sinks 200μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD200 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.104 pF
Output Cap.: VOUT: 0.190 pF
Cell Size: 3.0 gates, 8 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	746	1369	1428	1602	0.000+14.9*C_L ns

Switching characteristics

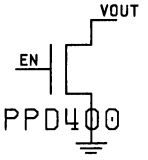
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	200μA typical

Electrical characteristics

400μA N–Channel Pulldown Device

PPD400 is a weak n–channel pulldown that sinks 400μmA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD400 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.051 pF
Output Cap.: VOUT: 0.190 pF
Cell Size: 2.50 gates, 11 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	373	685	714	801	1.67+7.42*C_L ns

Switching characteristics

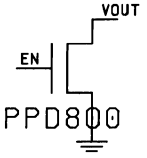
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	400μA typical

Electrical characteristics

800μA N–Channel Pulldown Device

PPD800 is a weak n–channel pulldown that sinks 800μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD800 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.051 pF
Output Cap.: VOUT: 0.190 pF
Cell Size: 1.25 gates, 6 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	198	363	378	424	3.03+3.89*C_L ns

Switching characteristics

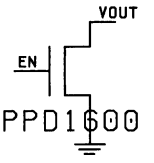
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	800μA typical

Electrical characteristics

1600μA N–Channel Pulldown Device

PPD1600 is a weak n–channel pulldown that sinks 1600μA when VOUT equals five volts. This cell is normally used as a DC pulldown for Input/Output cells. VOUT on the PPD1600 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: EN
Outputs: VOUT
Input Cap.: EN: 0.104 pF
Output Cap.: VOUT: 0.190 pF
Cell Size: 2.50 gates, 11 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PHL}	EN TO VOUT	104	190	198	222	0.876+2.05*C_L ns

Switching characteristics

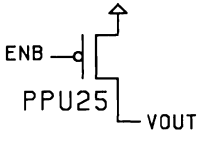
(V_{EN}=5V, V_{OUT}=5V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pulldown Current	Nominal Process, 25° C	1600μA typical

Electrical characteristics

25μA P–Channel Pullup Device

PPU25 is a weak p–channel pullup that sources 25μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU25 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.051 pF
Output Cap.: VOUT: 0.185 pF
Cell Size: 2.25 gates, 7 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	1564	2871	2992	3357	0.000+31.3*C_L ns

Switching characteristics

(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

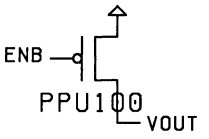
PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	25μA typical

Electrical characteristics

PPU100

100μA P–Channel Pullup Device

PPU100 is a weak p–channel pullup that sources 100μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU100 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.

Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.102 pF
Output Cap.: VOUT: 0.186 pF
Cell Size: 3.0 gates, 9 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	560	1028	1071	1202	0.000+11.2*C_L ns

Switching characteristics

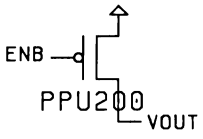
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	100μA typical

Electrical characteristics

200μA P–Channel Pullup Device

PPU200 is a weak p–channel pullup that sources 200μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU200 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.051 pF
Output Cap.: VOUT: 0.191 pF
Cell Size: 1.75 gates, 8 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	282	517	539	605	1.21+5.61*C_L ns

Switching characteristics

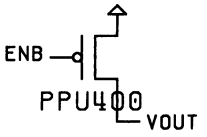
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	200μA typical

Electrical characteristics

400µA P–Channel Pullup Device

PPU400 is a weak p–channel pullup that sources 400µA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU400 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.051 pF
Output Cap.: VOUT: 0.186 pF
Cell Size: 1.0 gate, 5 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	160	294	306	344	0.220+3.19*C_L ns

Switching characteristics

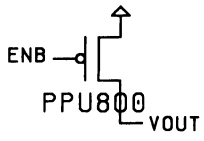
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	400µA typical

Electrical characteristics

800μA P–Channel Pullup Device

PPU800 is a weak p–channel pullup that sources 800μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU800 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.051 pF
Output Cap.: VOUT: 0.186 pF
Cell Size: 0.50 gates, 4 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	81.7	150	156	175	0.980+1.61*C_L ns

Switching characteristics

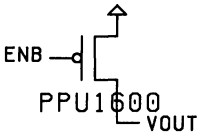
(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	800μA typical

Electrical characteristics

1600μA P–Channel Pullup Device

PPU1600 is a weak p-channel pullup that sources 1600μA when VOUT equals zero volts. This cell is normally used as a DC pullup for Input/Output cells. VOUT on the PPU1600 will be connected to UPDN on I/O cells with the "PPD" designation (IPPD, IOPPD2, OPPD4, etc.). To determine current ranges over various process, voltage, and temperature conditions, see applications note.



Inputs: ENB
Outputs: VOUT
Input Cap.: ENB: 0.104 pF
Output Cap.: VOUT: 0.186 pF
Cell Size: 1.0 gate, 5 array sites

(Input t_r, t_f=1.4 ns, C_L=50.00 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	ENB TO VOUT	42.2	77.4	80.7	90.5	0.882+0.825*C_L ns

Switching characteristics

(V_{ENB}=0V, V_{OUT}=0V, V_{DD}=5V)

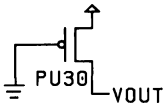
PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	1600μA typical

Electrical characteristics

30μA P–Channel Pullup Device

PU30 is a weak p–channel pullup that sources 30μA when VOUT equals zero volts and can be used as a pullup on internal tristate bus lines. This cell must not be connected directly to Input/Output cells. See PPU200, PPU400, etc. for that application. To determine current ranges over various process, voltage, and temperature conditions, see application note.

This cell produces a small DC current and care should be exercised on its use in designs with low I_{DD} requirements. Please contact your NCR applications engineer for more information.



* NOTE: The gate input on the PU30 cannot be used to turn the transistor on or off.

Inputs:
Outputs: VOUT
Input Cap.:
Output Cap.: VOUT: 0.186 pF
Cell Size: 2.25 gates, 7 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	*VOUT	17.6	32.4	33.8	37.9	4.41+66.1*C_L ns
t_r	*VOUT	34.9	64.1	66.8	75.0	9.54+127*C_L ns
* Timing is from VOUT = 0V to VOUT = 2.25V.						

Switching characteristics

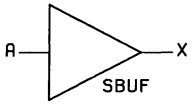
(V_{OUT}=0V, V_{DD}=5V)

PARAMETER	CONDITIONS	RATING
Pullup Current	Nominal Process, 25° C	30μA typical

Electrical characteristics

Small Buffer

Inputs: A
Outputs: X
Input Cap.: A: 0.102 pF
Cell Size: 1.0 gate, 3 array sites



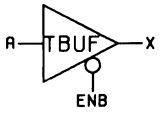
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.785	1.44	1.50	1.69	0.509+1.38*C_L ns
t_{PHL}		0.834	1.53	1.60	1.79	0.701+0.664*C_L ns
t_r	A TO X	1.05	1.93	2.02	2.26	0.461+2.96*C_L ns
t_f		0.680	1.25	1.30	1.46	0.442+1.19*C_L ns

Switching characteristics

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.102
ENB: 0.212 pF
Output Cap.: X: 0.127 pF
Cell Size: 3.0 gates, 7 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

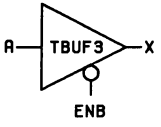
SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.31	2.40	2.50	2.81	1.04+1.33*C_L ns
t_{PHL}		1.06	1.95	2.04	2.28	0.932+0.653*C_L ns
t_{PLH}	ENB TO X	0.712	1.31	1.36	1.53	0.443+1.34*C_L ns
t_{PHL}		0.728	1.34	1.39	1.56	0.607+0.603*C_L ns
t_r	A TO X	1.69	3.10	3.24	3.63	1.13+2.80*C_L ns
t_f		0.892	1.64	1.71	1.92	0.658+1.17*C_L ns
t_r	ENB TO X	1.42	2.61	2.72	3.05	0.835+2.93*C_L ns
t_f		0.820	1.51	1.57	1.76	0.605+1.07*C_L ns

Switching characteristics

TBUF3

Noninverting Tristate Buffer

ENB is active low. When ENB is high, the output is in a Hi–Z state.



Inputs: A, ENB
Outputs: X
Input Cap.: A: 0.205
ENB: 0.102 pF
Output Cap.: X: 0.248 pF
Cell Size: 4.50 gates, 12 array sites

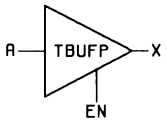
(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	0.870	1.60	1.67	1.87	0.770+0.499*C_L ns
t_{PHL}		1.27	2.34	2.43	2.73	1.20+0.341*C_L ns
t_{PLH}	ENB TO X	1.51	2.77	2.89	3.24	1.39+0.596*C_L ns
t_{PHL}		1.93	3.55	3.70	4.15	1.86+0.362*C_L ns
t_r	A TO X	0.752	1.38	1.44	1.61	0.580+0.858*C_L ns
t_f		0.794	1.46	1.52	1.71	0.681+0.564*C_L ns
t_r	ENB TO X	1.18	2.17	2.27	2.54	1.02+0.805*C_L ns
t_f		1.23	2.25	2.34	2.63	1.18+0.232*C_L ns

Switching characteristics

Noninverting Tristate Buffer

EN is active high. When EN is low, the output is in a Hi–Z state.



Inputs: A, EN
Outputs: X
Input Cap.: A: 0.102
EN: 0.212 pF
Output Cap.: X: 0.127 pF
Cell Size: 3.0 gates, 7 array sites

(Input t_r, t_f=1.4 ns, C_L=0.20 pF)

SYMBOL	PARAM.	NOMINAL V_{DD}=5V	WORST CASE V_{DD}=4.5V			DELAY EQUATION NOM. V_{DD}=5V
		T_A=25C	T_A=70C	T_A=85C	T_A=125C	T_A=25C
t_{PLH}	A TO X	1.34	2.46	2.56	2.87	1.07+1.33*C_L ns
t_{PHL}		1.05	1.92	2.00	2.24	0.916+0.640*C_L ns
t_{PLH}	EN TO X	0.826	1.52	1.58	1.77	0.562+1.32*C_L ns
t_{PHL}		0.386	0.709	0.739	0.829	0.269+0.583*C_L ns
t_r	A TO X	1.65	3.04	3.17	3.55	1.08+2.85*C_L ns
t_f		0.887	1.63	1.70	1.90	0.659+1.14*C_L ns
t_r	EN TO X	1.54	2.83	2.95	3.31	0.962+2.88*C_L ns
t_f		0.713	1.31	1.36	1.53	0.497+1.08*C_L ns

Switching characteristics

NCR ViGen Compiled Cells Data Sheets

VS700 ViGen Compiled Cells

VS1500 ViGen Compiled Cells

VS700 Dual Port RAM

Features

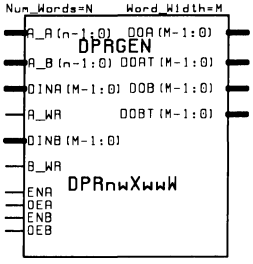
- Variable size RAM array with two independent, bidirectional ports (A,B).
- Read-only option on port A saves area.
- Tristate and always-driving outputs available on both ports.
- Variable number of words and word size up to 16K bits.

Description

The dual port RAM generator produces a RAM array with two fully independent read/write ports. Each port uses clocked operation to reduce complexity and operating power. Each port is precharged when its enable input is low and can read or write data when its enable input is high. To reduce logic circuitry and save cell area, Port A can be programmed to be a read-only port. Ports must be precharged between successive reads and writes.

Symbol

The symbol for DPREN will be unique for each configuration. An example is given here only for reference.



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
Num_Words	4 → 2048 (even only)	Number of data words in RAM array. The number of address lines for each port will be n = $\log_2$ (Num_Words). Number of bits = Num_Words × Word_Width must be ≤16384.
Word_Width	2 → 32	Number of bits in a data word. This affects the number of DINA, DINB, DOA, DOAT, DOB, and DOBT pins. Number of bits = Num_Words × Word_Width must be ≤16384.
PortArw	0 or 1	0: port "A" is read-only. 1: port "A" is read/write. If port "A" is read-only, then the DINA and A_WR pins are removed from the schematic symbol.

DPRGEN

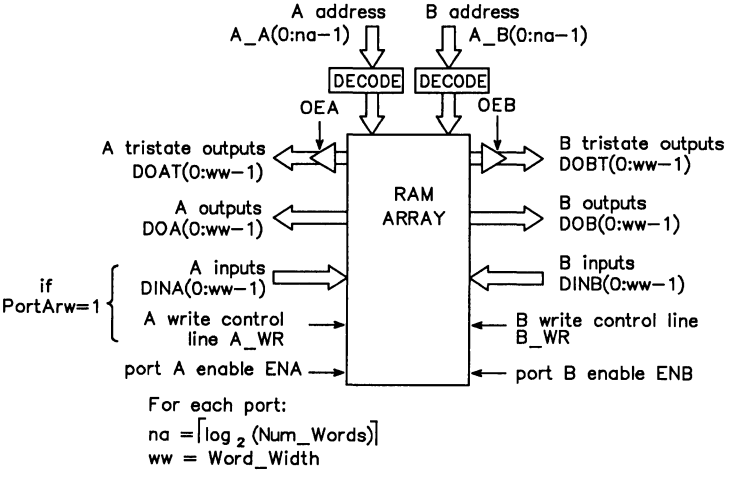
ViGen CONFIGURABLE FUNCTION

Inputs/Outputs

Bus Widths: M = Word_Width, n = $\lceil \log_2 (\text{Num\_Words}) \rceil$

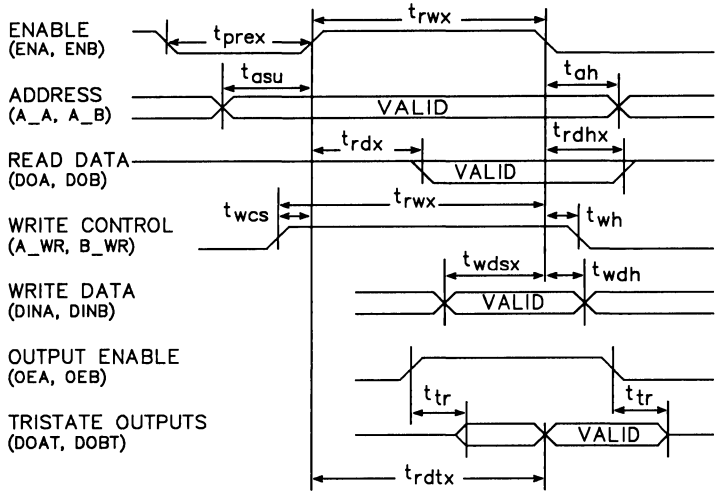
Pin/Bus Name (in TDL order)	Function	Req/Opt	Cap (pF)
INPUTS:			
A_A (n)	A port address bus	Req	0.132
A_B (n)	B port address bus	Req	0.132
DINA (M)	A port data in bus	Opt	0.082
A_WR	A port read/write control (active high write)	Opt	0.058
DINB (M)	B port data in bus	Req	0.082
B_WR	B port read/write control (active high write)	Req	0.058
ENA	A port enable pin	Req	0.109
OEA	DOAT (M) tristate enable pin (tristates when low)	Req	0.058
ENB	B port enable pin	Req	0.109
OEB	DOBT (M) tristate enable pin (tristates when low)	Req	0.058
OUTPUTS:			
DOA (M)	Always-driving A port output bus	Req	
DOAT (M)	Tristate A port output bus	Req	0.037
DOB (M)	Always-driving B port output bus	Req	
DOBT (M)	Tristate B port output bus	Req	0.037

Functional Block Diagram



DPRGEN AC Waveforms

The following waveforms apply equally to port A or port B. If the read–only option is chosen for port A (PortArw = 0), then ignore waveforms referring to write lines. A suffix of "x" in a timing parameter name should be substituted with "a" or "b" for the appropriate port; these parameters may have slightly different values.



Timing Parameters

Name	Description
t_{prex}	Minimum precharge time for port x
t_{asu}	Minimum address setup before rising enable (either port)
t_{ah}	Minimum address hold after falling enable (either port)
t_{rdx}	Maximum read access from rising enable on port x
t_{rdtx}	Maximum read access to tristate outputs from rising enable on port x
t_{rdhx}	Minimum read data hold after falling enable on port x
t_{wcs}	Write control setup before rising enable (either port)
t_{wh}	Write control hold after falling enable (either port)
t_{wdsx}*	Write data setup before falling enable of port x
t_{wdh}	Write data hold after falling enable (either port)
t_{tr}	Output enable to tristate on or off delay (either port)
t_{rwx}	Minimum enable high time of port x for read or write

* See Applications Note titled *Port Contention* which follows.

Timing, Current, and Size Equations

Equations are given in terms of several variables which describe a dual port RAM's characteristics. To solve the timing, current, and size equations given below, first determine values for the variables by following these steps:

1. Num_Words, Word_Width, and PortArw are generator input parameters, and CL is the output capacitance in pF.
2. Col_dec is the internal column decode factor. Possible values for Col_dec are 2, 4, 8, and 16. DPRGEN chooses the smallest valid Col_dec which is $\geq \sqrt{\text{Num\_Words} / \text{Word\_Width}}$.
3. Num_Words is internally rounded up to the nearest multiple of 2 × Col_dec.
4. Rows = internal array rows = Num_Words / Col_dec.
5. Cols = internal array columns = Word_Width × Col_dec.
6. Lr = $\lceil \log_2(\text{Rows}) \rceil$ ($\lceil\ \rceil$ = ceiling function: round up to nearest integer).

All times are NOMINAL (V_{DD} = 5.0 volts, T = 25° C, nominal process). See the *NCR ASIC VS700 Data Book* for voltage and temperature derating values. I_{DD} is specified at V_{DD} = 5.5 volts, T = 25° C, and worst case current process.

PARAM	DESCRIPTION	UNITS	TYPICAL VALUE (ns)
t_{prea}	Port A precharge	ns	= 1.97 + 0.023×Rows + 0.021×Cols + 0.074×Col_dec + 0.021×Lr + 1.160×CL
t_{preb}	Port B precharge	ns	= 1.98 + 0.028×Rows + 0.021×Cols + 0.075×Col_dec + 0.018×Lr + 1.167×CL
t_{asu}	Address setup	ns	= 0.30 + 0.046×Rows + 0.039×Col_dec + 0.035×Word_Width − 0.217×Lr
t_{ah}	Address hold	ns	= 0.00
t_{rda}	DOA read access	ns	= 1.64 + 0.031×Rows + 0.029×Cols + 0.091×Col_dec + 0.079×Lr + 0.953×CL
t_{rdb}	DOB read access	ns	= 1.64 + 0.037×Rows + 0.030×Cols + 0.092×Col_dec + 0.079×Lr + 1.000×CL
t_{rdta}	DOAT read access	ns	= 1.68 + 0.032×Rows + 0.030×Cols + 0.090×Col_dec + 0.064×Lr + 1.233×CL
t_{rdtb}	DOBT read access	ns	= 1.67 + 0.038×Rows + 0.031×Cols + 0.092×Col_dec + 0.071×Lr + 1.173×CL
t_{rdhx}	DOA, DOB read hold	ns	$t_{rdha} = t_{prea}$, $t_{rdhb} = t_{preb}$
t_{wcs}	A_WR, B_WR setup	ns	min = −2.0, max = 2.0
t_{wh}	A_WR, B_WR hold	ns	min = 0.0, max = 2.0
t_{wdsa}	DINA setup	ns	= 1.46 + 0.021×Rows + 0.131×Col_dec + 0.025×Lr
t_{wdsb}	DINB setup	ns	= 1.37 + 0.025×Rows + 0.131×Col_dec + 0.059×Lr
t_{wdh}	DINA, DINB hold	ns	= 0.54 + 0.009×Rows + 0.009×Cols
t_{tr}	Tristate, Untristate	ns	= 0.39 + 0.053×Word_Width
t_{rwx}	Min. ENA, ENB high	ns	$t_{rwa} = t_{rda}$, $t_{rwb} = t_{rdb}$
I_{DD}	Average current per port	µA/MHz	= 8.121×Rows + 3.813×Cols + 7.015×Col_dec + 11.065×Word_Width − 41.712×Lr
Width	Layout width	mils	= 9.41 + 1.264×Rows + 0.303×Col_dec + 1.134×PortArw
Height	Layout height	mils	= 7.68 + 0.834×Cols + 0.142×Col_dec − 0.029×Word_Width + 0.755×Lr

Timing Constants: k = 0.08 ns, M_{CLH} = 0.219, M_{CHL} = 0.163
Process Derating: B = 0.66, N = 1.00, W = 1.40

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See the VS700 Standard Cell Timing Equation application note. These coefficients are independent of the generator input parameters.

OUTPUT BUS	NOMINAL PROCESS, 5V, 25 °C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DOA	0.477	1.87	0.444	1.00
DOB	0.497	1.90	0.476	0.99
DOAT	0.386	1.05	0.246	1.49
DOBT	0.389	1.03	0.263	1.95

Rise/Fall time coefficients for the next cell

Timing Examples

16 x 16 DUAL PORT RAM: Col_dec = 2, Rows = 8, Cols = 32, Lr = 3

Symbol	16 x 16 DUAL PORT RAM (Port A Read/Write)	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		T_A = 25°C		T_A = 70°C		T_A = 85°C		T_A = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{prea}	Precharge time	3.25		6.06		6.31		7.08		ns
t_{preb}	Precharge time	3.29		6.14		6.40		7.18		ns
t_{asu}	Address set-up time	0.66		1.22		1.28		1.43		ns
t_{ah}	Address hold time	0.00		0.00		0.00		0.00		ns
t_{rda}	Read access time		3.40		6.34		6.61		7.42	ns
t_{rdb}	Read access time		3.49		6.51		6.78		7.61	ns
t_{rdta}	Tristate read access time		3.46		6.46		6.73		7.55	ns
t_{rdtb}	Tristate read access time		3.55		6.62		6.90		7.75	ns
t_{rdha}	Read data hold time	3.25		6.06		6.31		7.08		ns
t_{rdhb}	Read data hold time	3.29		6.14		6.40		7.18		ns
t_{wcs}	Write control set-up	−2.00	2.00	−3.73	3.73	−3.89	3.89	−4.37	4.37	ns
t_{wh}	Write control hold	0.00	2.00	0.00	3.73	0.00	3.89	0.00	4.37	ns
t_{wdsa}	Write data set-up	1.97		3.67		3.82		4.29		ns
t_{wdsb}	Write data set-up	2.01		3.74		3.90		4.38		ns
t_{wdh}	Write data hold	0.90		1.68		1.75		1.96		ns
t_{tr}	Tristate, untristate time	1.24		2.31		2.41		2.70		ns
t_{rwa}	Read or write enable high	3.40		6.34		6.61		7.42		ns
t_{rwb}	Read or write enable high	3.49		6.51		6.78		7.61		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 253 µA/MHz per port
AREA = 21.26 x 36.45 = 774.9 mil^2

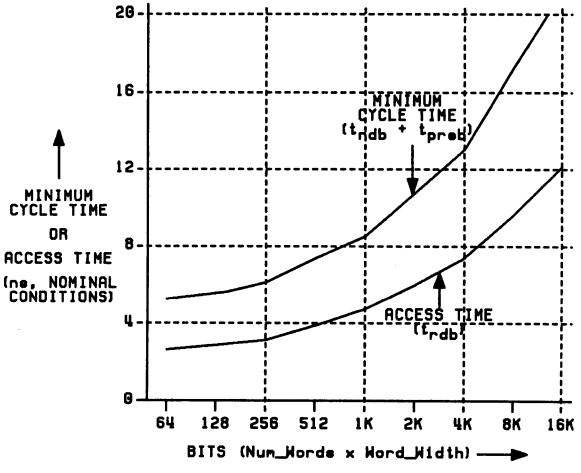
128 x 8 DUAL PORT RAM: Col_dec = 4, Rows = 32, Cols = 32, Lr = 5

Symbol	128 x 8 DUAL PORT RAM (Port A Read-only)	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		T_A = 25°C		T_A = 70°C		T_A = 85°C		T_A = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{prea}	Precharge time	3.99		7.44		7.76		8.70		ns
t_{preb}	Precharge time	4.15		7.74		8.07		9.05		ns
t_{asu}	Address set-up time	1.12		2.10		2.19		2.45		ns
t_{ah}	Address hold time	0.00		0.00		0.00		0.00		ns
t_{rda}	Read access time		4.48		8.37		8.72		9.79	ns
t_{rdb}	Read access time		4.72		8.80		9.17		10.29	ns
t_{rdta}	Tristate read access time		4.54		8.47		8.83		9.90	ns
t_{rdtb}	Tristate read access time		4.79		8.94		9.31		10.45	ns
t_{rdha}	Read data hold time	3.99		7.44		7.76		8.70		ns
t_{rdhb}	Read data hold time	4.15		7.74		8.07		9.05		ns
t_{wcs}	Write control set-up	-2.00	2.00	-3.73	3.73	-3.89	3.89	-4.37	4.37	ns
t_{wh}	Write control hold	0.00	2.00	0.00	3.73	0.00	3.89	0.00	4.37	ns
t_{wdsb}	Write data set-up	2.99		5.57		5.81		6.52		ns
t_{wdh}	Write data hold	1.12		2.08		2.17		2.44		ns
t_{tr}	Tristate, untristate time	0.81		1.52		1.59		1.78		ns
t_{rwa}	Read or write enable high	4.48		8.37		8.72		9.97		ns
t_{rwb}	Read or write enable high	4.72		8.80		9.17		10.29		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 290 µA/MHz per port
AREA = 51.07 x 38.48 = 1965.2 mil^2

Access and Cycle Time
for Word_Width = 8

NCR VS700 ASIC Data Book gives voltage and temperature derating factors. Different configurations of the same size (i.e., 1K×8 and 512×16) will have similar performance. Shown here is a range of configurations, all with Word_Width = 8.



Applications Notes

Using the Tristate Outputs DOAT(i) and DOBT(i)

The tristate outputs of the dual port RAM generator are not implemented in quite the same way as in some other NCR supercells. Figure 7–1 shows the circuits used for both always–driving outputs (DOA(i) and DOB(i)) and the tristate outputs. Instead of a full CMOS transmission gate for the tristate outputs, a single n–channel transistor is used to reduce circuit area. The effect of this is that the tristate outputs, when driven high, will not reach a full V_{DD} level. Instead, they will reach a level of about 3.3 volts when V_{DD} is 5.0 volts. This is enough to be considered a logic high for subsequent gate inputs, but there will be reduced noise margin and increased DC power dissipation caused by this non–rail level.

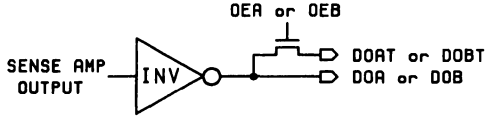


Figure 7–1 Tristate output circuit

For this reason it is important to use pull–up cells on each bit of each tristate output bus (see Figure 7–2). This is good design practice for any tristate line used in semicustom design. The PU30 cell is not meant to provide a valid logic level on a bus line, but only to provide a "default" level for those times when it is not actively driven by anything else.

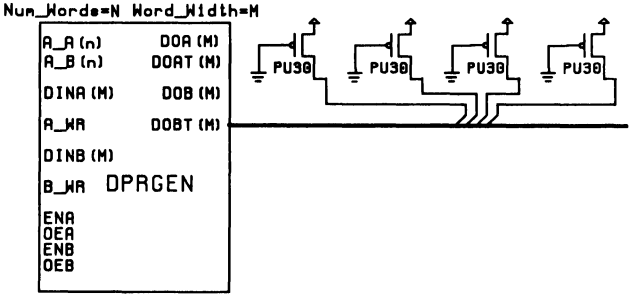


Figure 7–2 Tristate bus pullups

The pullups will cause no problem with "late 1's" on the tristate outputs. During the precharge phase for each port, the internal bit lines and sense amp inputs are pulled high. This causes the always-driving outputs to also go high during precharge. If the output enable line (OEA or OEB) is asserted at the beginning of a read phase, then the tristate outputs will also stay high if they were not immediately previously driven low by another gate. There is no possibility of a glitch on this line (and therefore losing the good high level) since the read access time for a "1" is actually zero. Only 0's in the data word being read have non-zero access time.

Reducing AC Power Dissipation

For most designers, the AC power dissipation of CMOS semicustom chips is not a problem needing consideration since it is very low compared to bipolar or NMOS implementations. Some applications, though, need low AC operating power as well.

If the address lines are allowed to switch several times before becoming stable at the address setup time, then excess AC power dissipation will occur due to the large capacitances on the internal address lines and their complements. This kind of power dissipation is calculated as:

$P=CV^2f$, where P = power
C = total driven capacitance
V = voltage swing (= VDD)
f = switching frequency

Since C is fixed inside the RAM, reducing this power can only be done by reducing the number of times that the address lines switch. This can be done by latching the address lines externally to the dual-port RAM.

Port Contention

The A and B ports of the dual-port RAM are meant to be independent in operation. The possibility of contention between the two ports does exist, however, and can happen in the following combinations:

1. One port's write cycle overlaps the other port's read cycle to the same address (read/write contention).
2. Both ports' write cycles overlap to the same address (write/write contention).

Note that port contention doesn't exist if both ports are reading from the same address. Discrete, dual-port RAM chips contain contention logic that detects when both ports are attempting to access the same address (whether reading or writing). The port which drives this address second is given a busy signal by the contention logic, which inhibits it from actually reading or writing to that address. When the first port has switched to a different address, the busy signal to the second port is deactivated.

This generator does not contain such contention logic, so care must be taken to assure correct operation. The benefit to not including this logic is more flexible operation. For instance, two-port reads can occur from the same address without one port being locked out. This is important for register files; for an example, see Figure 7-4.

Read/write contention can happen in three different ways (see Figure 7-3), and only one of them causes real contention. Of the three read/write overlaps shown, only the first, where the read on one port isn't complete before the other port starts to write, is a case of real port contention and must be avoided. In the second case, where both enables overlap within ± 1.5 ns (nominal), there will be no contention *if the data to be written is stable from the beginning of the write enable.* This overrides the write data setup time parameter in the AC characteristics table. In the third case, the data written to the addressed word will be stable in time for the reading port to access it, so no contention occurs.

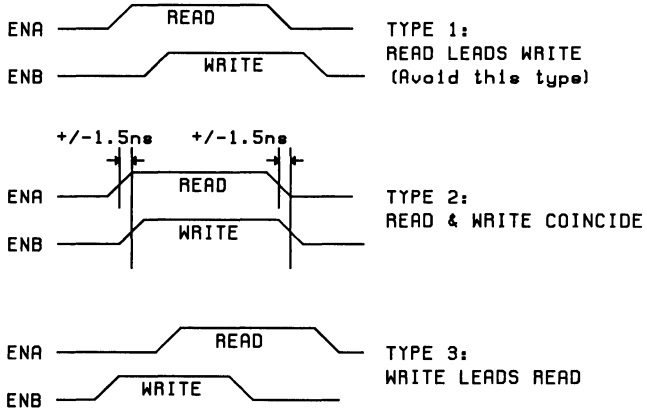


Figure 7-3 Read/Write port contention

Write/write combinations will always cause contention, since the data in the addressed word will contain unknown data except when both ports write identical data. If the enable signals ENA and ENB don't overlap their high times at all, then there is no contention.

Designing for Testability

A test program for a semicustom chip must be able to verify that all circuit functions operate correctly. This implies both functional correctness (correct design) and fault detection (the circuit was manufactured without defects). Several methods exist for a achieving both of these goals, all of which involve some trade–off between degree of checking and the amount of extra logic required. These include:

1. Multiplex part pins to the address and data pins in a test mode.
2. Use scan registers to serially shift in address and input data, and shift out output data.

See the NCR Standard Cell Library Databook, "Designing for Testability" for more information.

Example of Register File used with ALU

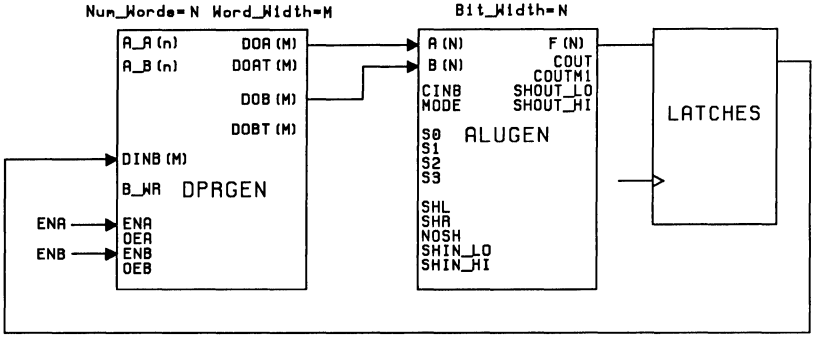


Figure 7–4 DPRGEN as a register file source for ALU operands

In Figure 7–4, the two operands for the ALU are read simultaneously from the A and B ports of the RAM, and then the ALU result is written back to the RAM through port B on the next cycle. The "PortArw" parameter for this RAM is set to "0" because the A port never has data written to it. There will never be any possibility of port contention because of this. The enable signals for each port can be tied together, which causes a dummy read of port A when the result is being written back through port B, or they can be separated as shown. Tying them together requires less logic to generate the ENA signal, but increases the operating power dissipation.

Example of FIFO

Figure 7–5 shows an implementation of a FIFO using the dual–port RAM supercell.

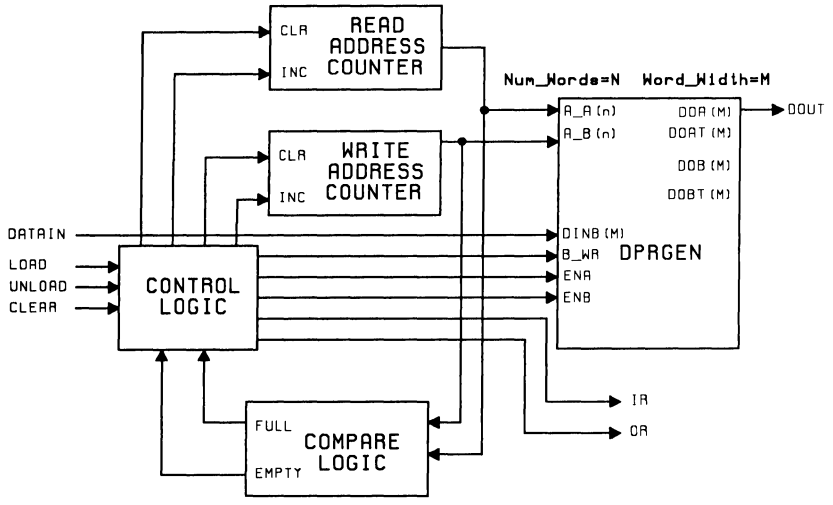


Figure 7–5 DPRGEN used in a FIFO buffer

Data is loaded with the LOAD input from DATAIN, and data is led out to the DOUT bus using UNLOAD. Address comparison determines whether the buffer is full (read address equals write address plus 1) or empty (write address equals read address plus 1). The IR flag (Input Ready) indicates that the FIFO is not full, and the OR flag (Output Ready) indicates the not empty condition.

Naming Conventions

ViGen will automatically create a default cell name for each unique DPRGEN configuration with the configuration information encoded in the following manner:

drwwwwbbpp

where:
wwww = number of words
bb = word width
pp = port (w=write/nw=non-writable)

Therefore, the default names for the two example configurations would be:

dr001616w
dr01208nw

FIFOGEN

ViGen CONFIGURABLE FUNCTION

VS700 FIFO Generator

Features

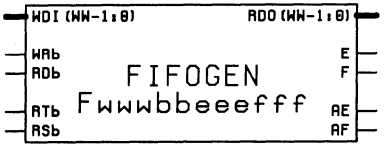
- Compiled FIFO cell allows flexible configurations of up to 6K bits
- Maximum word width of 36 bits
- Maximum number of words is 512
- Fully asynchronous Read/Write operation
- User configurable Almost Full flag
- User configurable Almost Empty flag
- Retransmit ability

Description

FIFOGEN produces a compiled first in first out memory block. FIFOGEN is based on a dual port latch memory cell which allows for completely asynchronous read/write operation. Read and write address values are stored in ring counters which may be cleared with the RSb (Reset) input. The read counter may be independently cleared using the RTb (retransmit) input, thus allowing data to be re-read multiple times. FIFOGEN also has status flags for Empty, Full, Almost Empty, and Almost Full. The user may configure the Almost Full and Almost Empty flags to activate any chosen offset from full and empty respectively.

Symbol

The symbol for FIFOGEN will be unique for each configuration. An example is given here only for reference.



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
Num_Words	4 → 512	Number of words in the FIFO[1], [2]
Word_Width	1 → 36	Number of bits in a word[1]
ae_offset	1 → words-1	Almost Empty offset from Empty for flag activation
af_offset	1 → words-1	Almost Full offset from Full for flag activation

[1] Total number of bits (**Num_Words** x **Word_Width**) must be ≤ 6K.

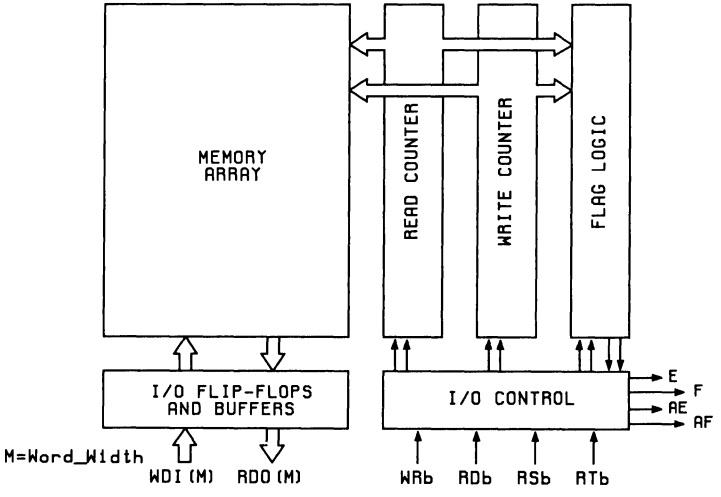
[2] **Num_Words** is internally rounded up to a multiple of the column decode. The column decode is internally selected to be 1 → 8 (by 1) by FIFOGEN to optimize area and performance. Any changes in **Num_Words** will be reported to the user at configuration time.

Inputs/Outputs

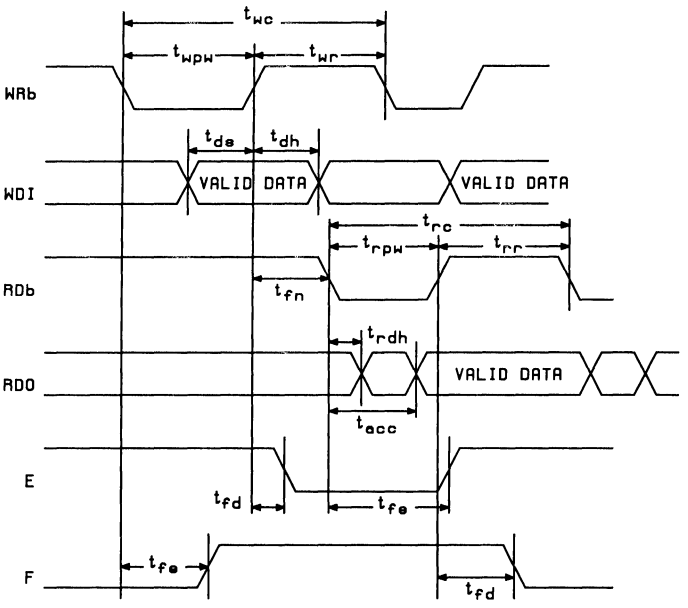
Bus Widths: M = **Word_Width**

Pin/Bus Name (in TDL order)	Function	Req/ Opt	Cap (pF)
INPUTS:			
WRb	Write control pin, active LOW	Req	0.041
RDb	Read control pin, active LOW	Req	0.041
RTb	Retransmit control pin, active LOW. Resets the read counter to first physical memory location	Req	0.041
RSb	Reset control pin, active LOW. Resets the read and write counters to first physical memory location.	Req	0.022
WDI[M]	Write data input bus	Req	0.025
OUTPUTS:			
RDO[M]	Read data output bus	Req	
E	Empty Flag, set HIGH on falling edge of RDb when reading last data word, reset on next rising edge of WRb	Req	
F	Full Flag, set HIGH on falling edge of WRb when writing last data word, reset on next rising edge of RDb	Req	
AE	Almost Empty Flag, set HIGH on falling edge of RDb when reading last data word, reset on rising edge of WRb	Req	
AF	Almost Full Flag, set HIGH on falling edge of WRb when writing last data word, reset on rising edge of RDb	Req	

Functional Block Diagram



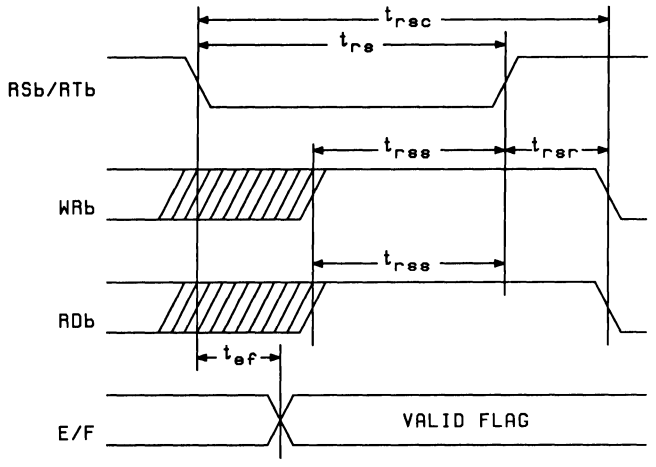
AC Waveforms – Read/Write



Timing Parameters – Read/Write

Name	Description
t_{wc}	Minimum Write cycle time
t_{wpw}	Minimum WRb pulse low
t_{wr}	Minimum Write recovery time (WRb high)
t_{ds}	Minimum data setup time from rising edge of WRb
t_{dh}	Minimum data hold time after rising edge of WRb
t_{rc}	Minimum Read cycle time
t_{rpw}	Minimum RDb pulse low
t_{rr}	Minimum Read recovery time (RDb high)
t_{acc}	Maximum delay RDb falling to valid data
t_{rdh}	Minimum data hold time after falling edge of RDb
t_{fe}	Flag Enable Delay
t_{fd}	Flag Disable Delay
t_{fn}	First Write to first valid Read

AC Waveforms – Reset/Retransmit



Timing Parameters – Reset/Retransmit

Name	Description
t_{rsc}	Minimum Reset/Retransmit cycle time
t_{rs}	Minimum Reset/Retransmit Pulse low
t_{rss}	Minimum WRb/RDb setup before RSb/RTb rising
t_{rsr}	Minimum Reset/Retransmit recovery time
t_{ef}	Minimum Reset/Retransmit to flag output

Timing, Current, and Size Equations

FIFOGEN will select its internal configuration based on the requested parameters. A simple algorithm is used which determines an internal architecture which will optimize area/performance tradeoffs. This architecture defines the number of rows and columns of the memory array. Because the user has no control over the internal column decode, **the resulting configuration may have more words than requested** (but never less). The algorithm is geared to minimize this discrepancy. The user will be notified at configuration time of the actual size of the array. Equations are given in terms of input parameters and internal architecture parameters. These can be found by following these steps:

1. CL is the output capacitance in pF.
2. Generator input parameters which affect delays are **Num_Words**, **Word_Width**. Derived parameters are **col_dec** and **rows**.
3. Calculate first-pass values for derived parameters, for area and performance a square array is best. Use (i).
4. In order to assure reasonable wordline performance, check array width; if it is greater than optimum length (72), decrease column decode (**col_dec**) by one. (ii).
5. Otherwise to optimize number of rows, check if increasing column decode would not cause too long a word line (iii).
6. Finally recalculate **rows** and **cols** if **col_dec** changed (iv, v).

i. if (**Num_Words** ≤ 32) **col_dec** = 1
   else {
   rows = SQRT(**Num_Words**×**Word_Width**), rounded up to an integer.
   col_dec = **Num_Words/rows**, rounded up to an integer.
   if (**col_dec** >8) **col_dec** = 8
ii. if (**col_dec**×**Word_Width** > 72) **col_dec** = **col_dec**−1;
iii. else if (**col_dec**×**Word_Width** < (72 − **Word_Width**) & **col_dec** < 8) **col_dec** = **col_dec**+1;
   }
iv. **rows** = **Num_Words/col_dec**, rounded up to an integer
v. **cols** = **Word_Width**×**col_dec**

All times are NOMINAL (V_{DD} = 5.0 volts, T = 25° C, nominal process). See the *NCR ASIC VS700 Data Book* for voltage and temperature derating values. I_{DD} is specified at V_{DD} = 5.5 volts, T = 25° C, and worst case current process.

PARAM	DESCRIPTION	UNITS	TYPICAL VALUE (ns)
t_{wc}	Write Cycle	ns	= 4.422 + 0.032×**Word_Width** + 0.449×**col_dec** + 0.127×**rows**
t_{wpw}	Write Pulse low	ns	= 2.818 + 0.012×**Word_Width** + 0.135×**col_dec** + 0.065×**rows**
t_{wr}	Write Pulse high	ns	= 1.613 + 0.030×**Word_Width** + 0.329×**col_dec** + 0.061×**rows**
t_{ds}	Write Data Setup	ns	= 0.333 + 0.015×**Word_Width** + 0.022×**col_dec** + 0.002×**cols**
t_{dh}	Write Data Hold	ns	= 1.228 + 0.017×**Word_Width** + 0.025×**col_dec**
t_{rc}	Read Cycle Time	ns	= 4.004 + 0.092×**col_dec** + 0.056×**rows** + 0.015×**cols**
t_{rpw}	Read Pulse low	ns	= 2.818 + 0.012×**Word_Width** + 0.135×**col_dec** + 0.065×**rows**
t_{rr}	Read Pulse high	ns	= 0.926 + 0.029×**cols**
t_{acc}	Read Access	ns	= 2.567 + 0.018×**Word_Width** + 0.005×**cols** + 1.067×**CL**
t_{rdh}	Read Data Hold	ns	= 2.241 + 0.022×**Word_Width** + 0.011×**col_dec** + 0.003×**cols** + 0.520×**CL**
t_{fe}	Flag Enable Delay	ns	= 2.132 + 0.001×**Word_Width** + 0.021×**col_dec** + 1.293×**CL**
t_{fd}	Flag Disable Delay	ns	= 2.172 + 0.001×**Word_Width** + 0.028×**col_dec** + 1.293×**CL**
t_{fn}	1st Write to Read	ns	= 3.977 + 0.009×**Word_Width** + 0.305×**col_dec** + 0.050×**rows**
t_{rsc}	RSb/RTb Cycle Time	ns	= 1.326 + 0.048×**col_dec** + 0.116×**rows** + 0.008×**cols**
t_{rs}	RSb/RTb Pulse low	ns	= 1.255 + 0.027×**col_dec** + 0.066×**rows** + 0.004×**cols**
t_{rss}	WRb/RD/b Setup to RSb/RTb	ns	= 1.987 + 0.028×**rows** + 0.003×**cols**
t_{rsr}	RSb/RTb Recovery Time	ns	= 0.071 + 0.021×**col_dec** + 0.050×**rows** + 0.004×**cols**
t_{ef}	RSb/RTb to Flag delay	ns	= 2.536 + 0.001×**Word_Width** + 0.009×**col_dec** + 1.293×**CL**
I_{DD}	Average current	mA/MHz	= 0.019 + 0.003×**rows** + 0.032×**cols**
Width	Layout width	mils	12.017 + 1.054×**col_dec** + 1.133×**rows**
Height	Layout height	mils	21.891 + 0.002×**col_dec** + 0.003×**rows** +0.874×**cols**

Timing Constants: K = 0.08 ns, M_{CLH} = 0.213, M_{CHL} = 0.213

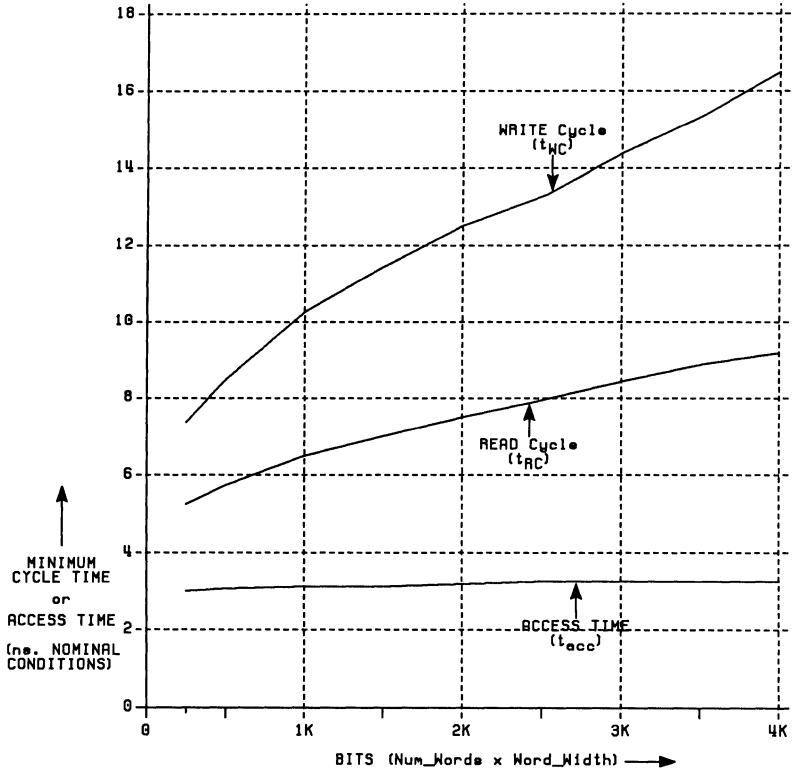
Process Derating: B = 0.66, N = 1.00, W = 1.40

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See the VS700 Standard Cell Timing Equation application note. These coefficients are independent of the generator input parameters.

OUTPUT BUS/PIN	NOMINAL PROCESS, 5V, 25 °C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
RDO	0.454	1.107	0.454	1.107
E,F,AE,AF	0.297	1.680	0.297	1.680

Rise/Fall time coefficients for the next cell

Access and Cycle Times for Word_Width = 8



(See NCR VS1500 ASIC Data Book for process, voltage, and temperature derating factors.)

Timing Examples

Timing for a 64x4 FIFO

Symbol	64x4 FIFO	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	Read access time		2.94		5.49		5.73		6.43	ns
t_{rdh}	Read data hold		2.59		4.84		5.05		5.66	ns
t_{wc}	Write cycle	8.45		15.77		16.43		18.44		ns
t_{rc}	Read cycle	5.49		10.25		10.69		11.99		ns
t_{fn}	First write till first read	6.19		11.55		12.04		13.51		ns
t_{rsc}	Reset cycle time	3.24		6.04		6.29		7.06		ns
t_{ds}	Write data setup time	0.54		1.01		1.06		1.19		ns
t_{dh}	Write data hold	1.42		2.65		2.77		3.10		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 0.698 mA/MHz
AREA = 30.39 × 39.24 = 1192 mil^2

Timing for a 256x9 FIFO

Symbol	256X9 FIFO	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	Read access time		3.24		6.06		6.32		7.09	ns
t_{rdh}	Read data hold		2.85		5.33		5.55		6.23	ns
t_{wc}	Write cycle	12.55		23.43		24.42		27.40		ns
t_{rc}	Read cycle	7.67		14.31		14.92		16.73		ns
t_{fn}	First write till first read	8.04		15.01		15.65		17.56		ns
t_{rsc}	Reset cycle time	6.46		12.05		12.56		14.09		ns
t_{ds}	Write data setup time	0.75		1.40		1.46		1.63		ns
t_{dh}	Write data hold	1.56		2.90		3.03		3.40		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 2.146 mA/MHz
AREA = 59.24 × 76.31 = 4521 mil^2

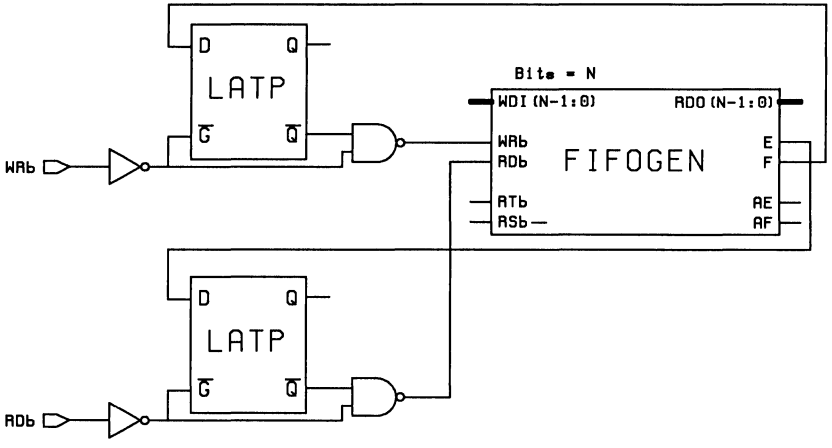
Application Notes

On power up a Reset must be performed before any other operations are performed. This assures that the FIFO is starting from a known state.

Reading the FIFO when it is empty and writing to a full FIFO will cause the status flags to be set unknown during simulation. While the logical state of the flags is predictable, the meaning of the status flags (full, empty, etc.) becomes ambiguous. A reset will clear the FIFO.

Retransmit allows the read pointer to be reset to the first physical memory address. Care must be taken to assure that the intended operation is achieved. Retransmit also causes ambiguous definition of the status flags. During retransmit the empty flag will be set false and the full flag true, so only reads should be performed until the FIFO is empty. The full flag will remain true until the FIFO is empty.

The following circuit may be used to disable reads when the FIFO is empty and writes when it is full.



Naming Conventions

ViGen will automatically create a default name for each FIFOGEN configuration, with the configuration information encoded in the following manner:

fwwwbbeeefff

where:
www = number of words
bb = number of bits
eee = almost empty offset
fff = almost full offset

All of the values have the given number of digits. Values that have less than the given number of digits will be left-padded with zeroes. For instance, a 31×8 FIFO with AE=4 and AF=5 will have a name of:

f03108004005

RAMGEN

ViGen CONFIGURABLE FUNCTION

VS700 RAM Generator

Features

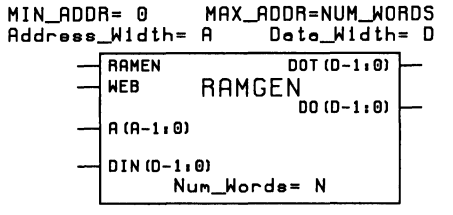
- Modular RAM allows variable configurations up to 64K bits.
- Pseudo static for reduced complexity and operating power (0 DC power)
- Enable input is taken low between each read and write access. This feature is applicable for clocked operation.
- Tristate and always-driving outputs
- Start_Addr parameter allows user to define address space of RAM

Description

The RAM generator produces a low power pseudo static RAM. On reads RAMEN is taken low to precharge internal states and data outputs; then RAMEN is taken high and the sense amp quickly discharges the outputs with a logic low. On writes, RAMEN is initially taken low allowing address inputs to change; data on DIN is written when RAMEN goes high. Many internal states are precharged to V_{DD} - $V_{threshold}$ to reduce power ($=CV^2F$) and decrease read access time. To further reduce AC power dissipation when the RAM is disabled, all inputs are internally gated by RAMEN. By externally tying a tristatable output to a data input, a bidirectional I/O line can be obtained.

Symbol

The symbol for RAMGEN will be unique for each configuration. An example is given here only for reference. Data_Width = Word_Width and Address_Width = $\lceil \log_2 (Num\_Words + Start\_Addr) \rceil$



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
Num_Words	8 → 4096 (even only)	Number of words in RAM array
Word_Width	Any integer ≤64	Number of bits in a word. The total number of bits = Num_Words x Word_Width must be < 65536.
Start_Addr	0 → 4096-Num_Words (even only)	Address of first word in array

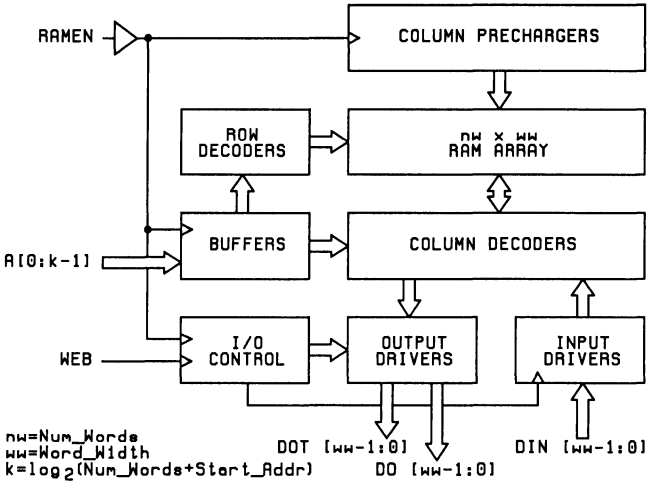
Inputs/Outputs

Pin/Bus Name (in TDL order)	Function	Cap (pF)
INPUTS:		
RAMEN	RAM enable is active high. Internal states are precharged when RAMEN is low. Reads and writes are enabled when RAMEN is high.	0.21
WEB	Read/Write select: active high for read, active low for write.	0.15
A[0:k−1]	Address input bus of width k ($k = \lceil \log_2 (Num\_Words + Start\_Addr) \rceil$). Addresses may only change while RAMEN is low.	0.05
DIN[Word_Width−1:0]	Data input bus.	0.18
OUTPUTS:		
DO[Word_Width−1:0]	Data output bus, driven by RAM (on read) and DIN (on write). Goes high on low RAMEN input.	
DOT[Word_Width−1:0]	Tristate data output bus is driven when WEB and RAMEN inputs are high. Otherwise DOT is at high impedance.	0.06

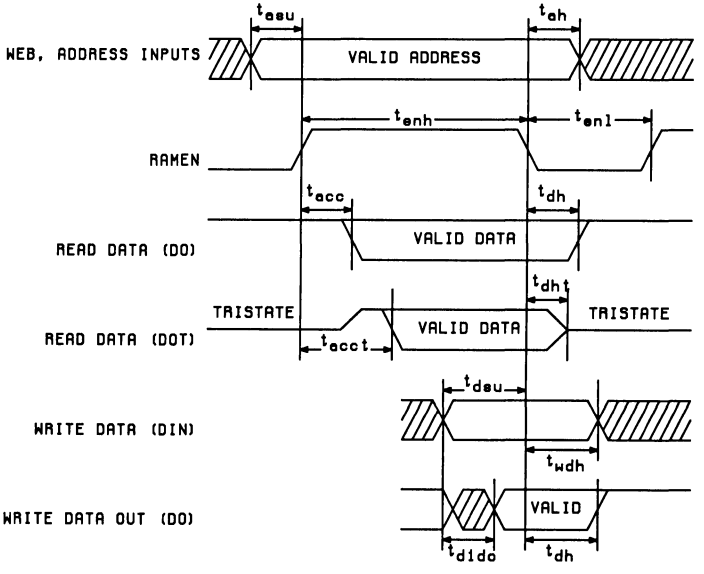
Timing Parameters

Name	Description
t_{acc}	Maximum delay from rising RAMEN to valid output data on DO (Read)
t_{acct}	Maximum delay from rising RAMEN to valid output data on DOT (Read)
t_{dido}	Maximum delay from data in to data out while RAMEN high (Write)
t_{enl}	Minimum RAMEN low pulse width (Read, Write)
t_{enh}	Minimum RAMEN high pulse width (Read, Write)
t_{asu}	Minimum address/WEB setup time before RAMEN rises (Read, Write)
t_{ah}	Minimum address/WEB hold time after RAMEN falls (Read, Write)
t_{dsu}	Minimum input data (DIN) setup time before RAMEN falls (Write)
t_{wdh}	Minimum input data (DIN) hold time after RAMEN falls (Write)
t_{dh}	Minimum delay from falling RAMEN during which DO data remains valid (Read, Write)
t_{dht}	Minimum delay from falling RAMEN until DOT outputs at high impedance (Read)
t_r	Maximum output rise time on DO
t_f	Maximum output fall time on DO
t_{rt}	Maximum output rise time on DOT (Read)
t_{ft}	Maximum output fall time on DOT (Read)

Functional Block Diagram



RAMGEN AC Waveforms



Timing, Power, and Area Equations

Equations are given in terms of several variables which describe a RAM's characteristics. To solve the timing, power, and area equations given below, first determine RAM variables by following these steps:

1. Num_Words, Word_Width, and Start_Addr are generator input parameters.
2. CL is output capacitance in pF.
3. col_dec = internal column decode. Valid values for col_dec are 4, 8, and 16. RAMGEN chooses smallest valid col_dec which is $\geq \sqrt{\text{Num\_Words} / \text{Word\_Width}}$. Use col_dec = 4 if $\sqrt{\text{Num\_Words} / \text{Word\_Width}} \leq 4$.
4. Num_Words is internally rounded up and Start_Addr rounded down to the nearest multiple of 2*col_dec.
5. rows = internal array rows = Num_Words / col_dec.
6. cols = internal array columns = Word_Width*col_dec.
7. Lr = $\lceil \log_2(\text{rows} + \text{Start\_Addr/col\_dec}) \rceil$ (ceiling function: round up to nearest integer).

All times are NOMINAL (V_{DD} = 5.0 volts, T = 25° C, Nom. process). See the NCR VS700 ASIC Data Book for process, voltage, and temperature derating.

PARAM	DESCRIPTION	TYPICAL VALUE (ns)
t_{acc}[1]	DO access Propagation Delay	= 2.95 + 0.014*cols + 0.026*rows + 0.056*Lr + .328*CL
t_{acct}[1]	DOT access Propagation Delay	= 2.96 + 0.014*cols + 0.026*rows + 0.072*Lr + .777*CL
t_{dido}[1]	Data in to data out Propagation Delay	= 3.25 + 0.019*rows + 0.242*Lr + 0.515*CL
t_{enl}[2]	RAMEN low pulse width	= 2.72 + 0.017*cols + 0.032*rows
t_{enh}	RAMEN high pulse width	= t_{acc}
t_{asu}	Address/WEB setup	= 0
t_{ah}	Address/WEB hold	= 0.58 + 0.005*Word_Width + 0.069*Lr
t_{dsu}	Write data setup	= 1.37 + 0.015*rows
t_{wdh}	Write data hold	= 0.50 + 0.041*Word_Width + 0.043*Lr
t_{dh}	DO hold	= 2.41 + 0.036*Word_Width + 0.064*Lr + 0.529*CL
t_{dht}	DOT hold	= 1.21 + 0.071*Word_Width
t_{r}[3]	DO rise	= 0.37 + 1.135*CL
t_{f}[3]	DO fall	= 0.36 + 1.084*CL
t_{rt}[3]	DOT rise	= 0.54 + 3.307*CL
t_{ft}[3]	DOT fall	= 0.34 + 1.033*CL

[1] Propagation Delay Timing Constants: K = 0.08ns $M_{CLH} = M_{CHL} = 0.2$

[2] t_{enl} equals maximum of t_{enl} and ($t_{dh} + t_r$) if outputs driving large capacitances.

[3] Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See the Timing Equation application note for the VS700 Standard Cell Library.

Current Requirements: I = 4.22*rows + 5.88*cols + .0261*rows*cols (μA/MHz)
Worst case current process, V_{DD} = 5.5V, T = 25° C

Cell Height Estimate (mils) = 7.8 + .86*rows

Cell Width Estimate (mils) = 4.6 + offset + .59*cols

if 04 ≤ cols < 40	use offset = 3.3
if 40 ≤ cols < 80	use offset = 4.3
if 80 ≤ cols ≤ 256	use offset = 5.3

Timing Examples

512 x 8 RAM: col_dec = 8, rows = 64, cols = 64, Lr = 6

Symbol	512 x 8 RAM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		T_A = 25°C		T_A = 70°C		T_A = 85°C		T_A = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	DO access		5.96		11.14		11.62		13.04	ns
t_{acct}	DOT access		6.05		11.31		11.79		13.23	ns
t_{dido}	Data in to data out		6.05		11.31		11.79		13.23	ns
t_{enl}	RAMEN low pulse width	5.86		9.99		10.42		11.69		ns
t_{enh}	RAMEN high pulse width	5.96		11.14		11.62		13.04		ns
t_{asu}	Address/WEB set-up	0.00		0.00		0.00		0.00		ns
t_{ah}	Address/WEB hold	1.03		1.76		1.84		2.06		ns
t_{dsu}	Write data set-up	2.33		3.98		4.15		4.65		ns
t_{wdh}	Write data hold	1.09		1.85		1.93		2.17		ns
t_{dh}	DO hold	3.13		5.35		5.58		6.26		ns
t_{dht}	DOT hold	1.78		3.03		3.16		3.55		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 0.75 mA/MHz
AREA = 46.94x62.91 = 2952.60(mils^2)

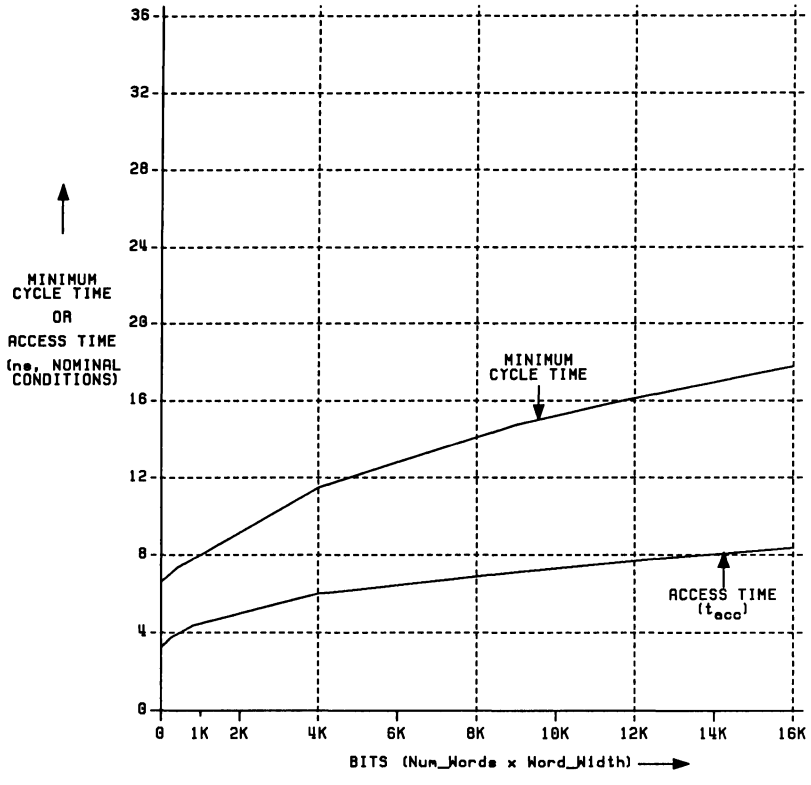
64 x 4 RAM: col_dec = 4, rows = 16, cols = 16, Lr = 4

Symbol	64 x 4 RAM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		T_A = 25°C		T_A = 70°C		T_A = 85°C		T_A = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	DO access		3.93		7.35		7.66		8.60	ns
t_{acct}	DOT access		4.03		7.54		7.86		8.83	ns
t_{dido}	Data in to data out		4.66		8.71		9.08		10.19	ns
t_{enl}	RAMEN low pulse width	3.50		5.98		6.23		6.99		ns
t_{enh}	RAMEN high pulse width	3.93		7.35		7.66		8.60		ns
t_{asu}	Address/WEB set-up	0.00		0.00		0.00		0.00		ns
t_{ah}	Address/WEB hold	0.88		1.50		1.56		1.75		ns
t_{dsu}	Write data set-up	1.61		2.75		2.86		3.21		ns
t_{wdh}	Write data hold	0.84		1.43		1.49		1.67		ns
t_{dh}	DO hold	2.86		4.89		5.09		5.71		ns
t_{dht}	DOT hold	1.49		2.55		2.66		2.98		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 0.17 mA/MHz
AREA = 17.68x21.01 = 371.51(mils^2)

Access and Cycle Time for square arrays (rows = columns)

Graph slightly overestimates for array columns > rows.
Cycle time = $t_{enl} + t_{enh}$



(NCR VS700 ASIC Data Book gives process, voltage, and temperature derating factors.)

Application Notes

Designing for testability

Test programs for ASIC components must be able to verify that all circuit elements in the design are functioning properly. This includes verifying the functional correctness of the design and detecting faults caused by manufacturing defects. There are many methods to improve the testability of a component, all of which involve trade–offs in the amount of extra logic required, the resulting test time, and the degree of test coverage. A highly recommended method for the RAM is to multiplex the address, control, and data lines to the external part pins during a test mode. This allows direct control and observability of the RAM during test. In pin limited situations, the use of scan registers to shift in the address and data and to shift out the output may be desired.

To adequately test the RAM, the following conditions and patterns should be considered:

- Ideally, unique data should be written to every address. Tying address and data input lines together while writing provides such a test of every data value. Verify by comparing each address with address content. Repeat test with address complements written through data inputs. This ensures that logic one and zero are written to every bit and verified. Preferably, all bits should be written first and then read. This pattern will catch faults in the array, address decode, and I/O driver.
- The data output should change frequently between consecutive reads. The above pattern or a "checkerboard" pattern is a good example of this.
- Operate RAM at near maximum frequency to verify that sense amps and other critical timing circuitry are working properly.
- When reading, set data inputs to a value other than the value being read (such as all 0/1). This verifies that outputs are not being driven by inputs during reads.
- Verify tristate control by reading through tristate outputs.

Column address inputs are the least significant bits of the address. If the RAM is operated as specified, then the critical race conditions which can cause write or read disturb problems will not exist in this design.

Output drive

The data outputs (DO) have high output drives approximately equal to the drive of an HBUF. Through the tristate outputs (DOT), the drive is about half the data output drive, or slightly less than the drive of a TBUFP.

RAM BANKS and WORDS not a power of 2

The address space may be redefined by the user with the Start_Addr parameter. When the Start_Addr parameter is given a non-zero value, the RAM block will have an address space from Start_Addr to Num_Words plus Start_Addr. The RAM will automatically be configured with sufficient address lines to access the full address range. This feature allows the designer to use a RAM as part of an address space without the need for external decode logic. Also note that both the DO and DOT outputs will drive indeterminate data when reading from an address out of the RAM's address range (the BLM will read unknowns).

Additional speed can be obtained at the cost of area and power by dividing the RAM into smaller blocks. The RAM can be divided across its address space (i.e., RAMG64×4 → RAMG32×4 + RAMG32×4) or across its word width (i.e., RAMG64×4 → RAMG64×1 + RAMG64×3). When the address space is segmented, a chip select feature is needed to disable all RAMs not being addressed. This feature is obtained by gating each RAMEN input with a chip select input. Avoid glitches on the individual RAMEN inputs of blocks.

When a block of RAM contains a number of words which is not equal to a power of two, be certain that the least significant address bit of the system is wired to address 0 of the RAM.

Naming conventions

ViGen will automatically create a default cell name for each unique RAMGEN configuration. This name is encoded in the following manner:

rawwwwbbssss

where:
wwww = number of words
bb = word width
ssss = starting address

Therefore, the default names for the two example RAMs would be:

ra0512080000
ra0064040000

ROMGEN

ViGen CONFIGURABLE FUNCTION

VS700 ROM Generator

Features

- Compiled ROM cell allows flexible configurations of up to 256K bits
- Maximum word width of 128 bits
- Maximum number of words is 16K
- Clocked operation suitable for microprocessor applications
- Pseudo-static design for low power consumption and 0 DC power

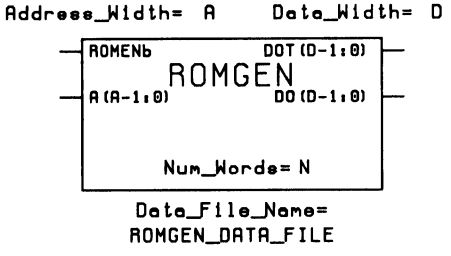
Description

ROMGEN produces a compiled ROM block which is pseudo-static for reduced power consumption, but delivers short access times. The enable input (ROMENb) must be taken high before each access, making the ROM suitable for clocked operation. The ROM is precharged while ROMENb is high, with the internal states pulled up to $V_{DD} - V_{th}$ to reduce power consumption and cycle times. Also, all inputs are gated off while ROMENb is high to reduce AC power dissipation. Data is read from the ROM while ROMENb is low, with both tristatable and constantly-driving outputs available.

Symbol

The symbol for ROMGEN will be unique for each configuration. An example is given here only for reference.

Data_Width = Word_Width
Address_Width = $\lceil \log_2 (\text{Num\_Words}) \rceil$



Input Parameter Ranges

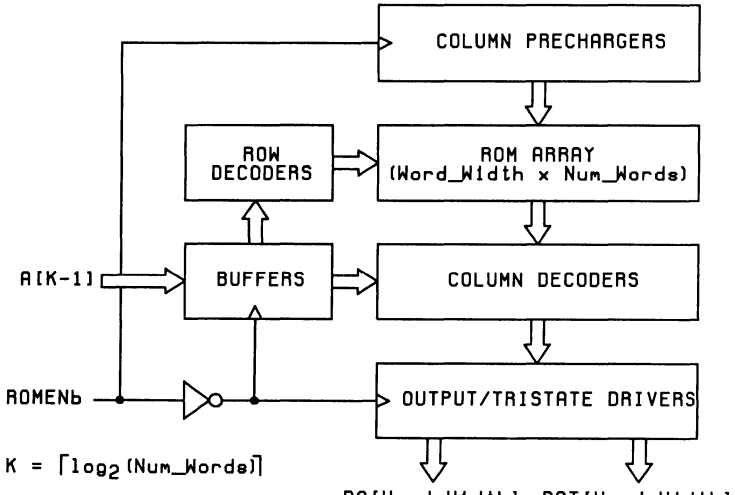
Input Parameter	Allowed Range	Explanation
Word_Width	1 → 128	Word size in bits[1]
Num_Words	128 → 16,384 (multiple of 128)[2]	Number of words in the ROM[1]
fname	ASCII alpha-numeric string	ROM data file name

[1] Total number of ROM bits (Word_Width × Num_Words) must be ≤256K.
[2] Num_Words is internally rounded up to a multiple of 32 times the column decode factor. The column decode is selected to be 4, 8, 16, or 32 by ROMGEN to optimize area and performance.

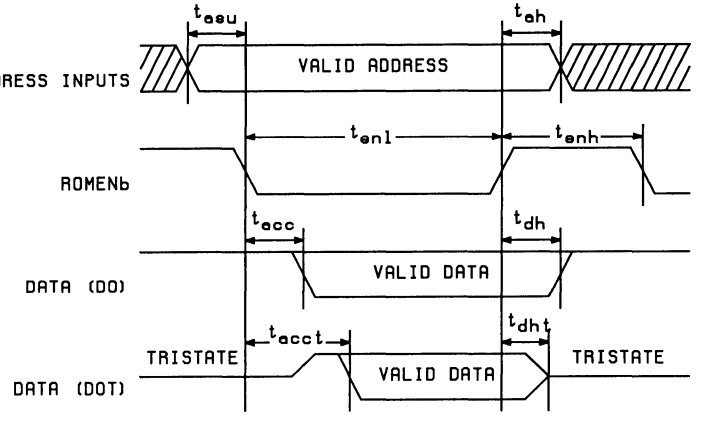
Inputs/Outputs

Pin/Bus Name (in TDL order)	Function	Cap (pF)
INPUTS:		
ROMENb	ROM enable is active low. Internal states are precharged when ROMENb is high.	0.45
A[K]	Address input bus of width K (K = $\lceil \log_2 (\text{Num\_Words}) \rceil$). Addresses may change only while ROMENb is high.	0.19
OUTPUTS:		
DO[Word_Width]	Data output bus. Goes high while ROMENb is high.	
DOT[Word_Width]	Tristate data output bus. DOT is at high impedance while ROMENb is high.	0.10

Functional Block Diagram



ROMGEN AC Waveforms



Timing Parameters

Name	Description
t_{acc}	Maximum delay from ROMENb active low to valid data on DO
t_{acct}	Maximum delay from ROMENb active low to valid output data on DOT
t_{enl}	Minimum ROMENb low pulse width
t_{enh}	Minimum ROMENb high pulse width
t_{asu}	Minimum address setup time before ROMENb goes active low
t_{ah}	Minimum address hold time after ROMENb goes inactive high
t_{dh}	Minimum delay from ROMENb inactive high during which DO data remains valid
t_{dht}	Minimum delay from ROMENb inactive high until DOT goes to high impedance

Timing, Current, and Size Equations

Equations are given in terms of generator parameters and derived variables. These can be found by following these steps:

1. CL is the output capacitance in pF.
2. Generator input parameters are Num_Words, Word_Width.
3. Calculate first-pass values for internal variables:
   TrialRows = SQRT(Num_Words×Word_Width), rounded up to a multiple of 32.
   TrialCols = (Num_Words×Word_Width) / TrialRows.
4. Assume that Col_dec = TrialCols / Word_Width. Then round up to the nearest valid column decode factor of 4, 8, 16, or 32.
5. Num_Words must be rounded up to a multiple of (32×Col_dec).
6. To get the final values:
   Cols = Col_dec×Word_Width
   Rows = Num_Words / Col_dec
   Num_Words = Rows×Col_dec
7. Lr = $\log_2$ (Rows) , Lc = $\log_2$ (Cols).

All times are NOMINAL (V_{DD} = 5.0 volts, T = 25° C, Nominal process). See the *NCR ASIC VS700 Data Book* for process, voltage, and temperature derating factors. I_{DD} is specified at V_{DD} = 5.5V, T = 25° C, and worst case current process.

PARAM	DESCRIPTION	UNITS	TYPICAL VALUE (ns)
t_{acc}	DO access time	ns	= 5.293 − 0.028×Word_Width + 0.040×Rows + 0.012×Cols + 0.030×Col_dec − 0.207×Lr − 0.043×Lc + 0.580×CL
t_{acct}	DOT access time	ns	= 5.306 − 0.042×Word_Width + 0.040×Rows + 0.012×Cols + 0.025×Col_dec − 0.217×Lr − 0.004×Lc + 0.620×CL
t_{enl}	ROMENb low pulse width	ns	= 5.293 − 0.028×Word_Width + 0.040×Rows + 0.012×Cols + 0.030×Col_dec − 0.207×Lr − 0.043×Lc + 0.580×CL
t_{enh}	ROMENb high pulse width	ns	= 8.860 + 0.018×Word_Width + 0.062×Rows + 0.013×Cols + 0.009×Col_dec − 1.721×Lr + 0.238×Lc + 1.060×CL
t_{asu}	Address setup	ns	= 0.000
t_{ah}	Address hold	ns	= 0.734 + 0.016×Lr
t_{dh}	DO hold time	ns	= 2.555 + 0.050×Word_Width+ 0.007×Rows + 0.009×Cols + 0.046×Col_dec − 0.053×Lr − 0.040×Lc + 1.060×CL
t_{dht}	DOT hold time	ns	= 0.710 + 0.053×Word_Width + 0.003×Rows + 0.032×Lr + 0.014×Lc + 1.247×CL
I_{DD}	Average current	µA/ MHz	= 212.9 + 3.41×Word_Width + 1.56×Rows + 0.85×Cols
Width	Layout width	mils	= 12.934 + 0.017×Rows + 0.213×Cols − 0.367×Lr − 0.034×Lc
Height	Layout height	mils	= 8.041 + 0.029×Word_Width + 0.183×Rows + 0.029×Col_dec + 0.346×Lr − 0.043×Lc

Timing Constants: k = 0.08ns, $M_{CLU} = M_{CHL} = 0.26$

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See the VS700 Standard Cell Timing Equation application note. These coefficients are independent of the generator input parameters.

OUTPUT BUS	NOMINAL PROCESS, 5V, 25 °C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
DO	0.484	1.32	0.393	0.62
DOT	0.787	2.30	0.429	0.69

Rise/Fall time coefficients for the next cell

Timing Examples

1024 × 8 ROM: Rows = 64, Cols = 128, Col_dec = 16, Lr = 6, Lc = 7

Symbol	1024 × 8 ROM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	DO access		8.40		15.69		16.36		18.36	ns
t_{acct}	DOT access		8.51		15.90		16.57		18.60	ns
t_{dh}	DO hold	5.23		9.78		10.19		11.44		ns
t_{dht}	DOT hold	2.24		4.21		4.39		4.93		ns
t_{enh}	ROMENb high pulse width	6.66		12.44		12.97		14.55		ns
t_{enl}	ROMENb low pulse width	8.40		15.69		16.36		18.36		ns
t_{asu}	Address setup	0.00		0.00		0.00		0.00		ns
t_{ah}	Address hold	0.83		1.55		1.62		1.81		ns

Switching characteristics (Input t_r, t_f = 0.5ns, CL = 0.1pF)

I_{avg} (ac) = 449 µA/MHz
Cell Width = 38.85 mils
Cell Height = 22.22 mils
Cell Area = 863.2 mils^2

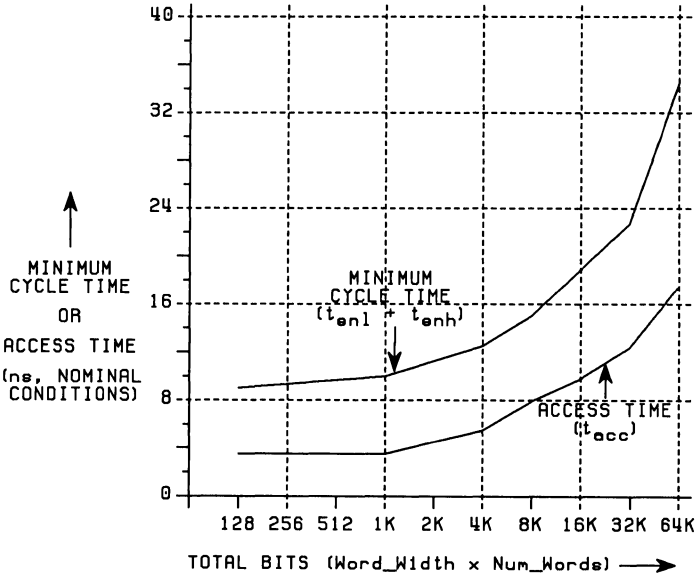
8192 × 8 ROM: Rows = 256, Cols = 256, Col_dec = 32, Lr = 8, Lc = 8

Symbol	8192 × 8 ROM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	DO access		17.64		32.94		34.34		38.53	ns
t_{acct}	DOT access		17.69		33.05		34.45		38.65	ns
t_{dh}	DO hold	8.31		15.54		16.20		18.18		ns
t_{dht}	DOT hold	2.90		5.43		5.66		6.35		ns
t_{enh}	ROMENb high pulse width	17.16		32.06		33.42		37.49		ns
t_{enl}	ROMENb low pulse width	17.64		32.94		34.34		38.53		ns
t_{asu}	Address setup	0.00		0.00		0.00		0.00		ns
t_{ah}	Address hold	0.86		1.61		1.68		1.88		ns

Switching characteristics (Input t_r, t_f = 0.5ns, CL = 0.1pF)

I_{avg} (ac) = 858 µA/MHz
Cell Width = 68.61 mils
Cell Height = 58.47 mils
Cell Area = 4011.6 mils^2

Access and Cycle Time for Word_Width ≤ 8



NCR VS700 ASIC Data Book gives voltage and temperature derating factors.

Application Notes

Data file format

The data file which is used to build ROMGEN is the same data file which is used during simulation of the ROM. For the exact data file format, refer to your *NCR Design Package Manual* documentation referencing use of supercells.

Padding ROM data

In certain cases, the actual size of the data for the ROM may be smaller than the size of the configured ROM. In this case, the data file must be padded to be the same size as the ROM. It is recommended that the data file be padded with all–ones words. This will help to limit power dissipation of the ROM.

Designing for testability

Testability for ASIC parts requires that each of the individual ASIC components be testable, including verification of functional operation, as well as detection of faults introduced in the manufacturing process. The degree to which an individual component in an ASIC design can be effectively tested depends largely on the degree to which that component can be isolated from the rest of the chip. It is highly recommended that the address lines, enable line, and data outputs of the ROM be multiplexed so that the tester (or other external board logic) has direct control and observability of the ROM in the test mode. There is, of course, a trade–off made with respect to speed and area when adding the additional logic required for multiplexing. Other alternatives for testing the ROM include:

- A parity bit can be added to the ROM, and a simple parity checker connected to the outputs of the ROM. The address lines to the ROM could still be multiplexed for the tester to use, while only the result of the parity checker would need to be output to the tester. The parity checker can continue to monitor the ROM during the run mode.
- An alternate scheme which still uses the parity bit and checker would also use a counter connected to the address inputs to count through all of the addresses in test mode. This type of design would be preferable for implementing a BIST (Built–In Self–Test) style architecture.

- Instead of using a parity bit in the ROM, which adds to the size of the ROM required, a signature analyzer could be placed at the output of the ROM. This would require approximately (Word_Width + 4) linear feedback shift registers (LFSR) to be placed at the data outputs (one on each output, plus at least four extras). The address inputs could be generated either by a counter or by a second LFSR string, and the final signature could either be compared on chip, or fed off chip to the tester. This method gives much better coverage of the ROM than does the parity checker method and in a more random fashion, and is an excellent BIST option. The drawback with the signature analysis method is that it cannot be used by the ROM in the run mode.

Some things which should be considered when actually doing the testing on the ROM would include:

- The ROM should be operated at or near the maximum frequency it will set in the application to verify that other critical timing circuitry is operating correctly.
- Verify tristate control by reading through the tristates (if they are used in the design).

In addition to these suggestions, it is recommended that the design guidelines found in the Application Notes section of the NCR ASIC Data Book be strictly followed.

Output drive

The data outputs (DO) have high output drives approximately equal to the drive of an HBUF cell. The output drive for the tristate outputs (DOT) is about half that of the data outputs (about the same as a TBUF cell).

ROMGEN uses a pass gate circuit connected to the data outputs (DO) to generate the DOT outputs. For this reason, heavy loading on the DOT outputs will cause degraded performance of the DO outputs, although this will not be correctly modeled by the simulator. For high drive tristate outputs, it is recommended that a TBUF or equivalent cell be used on the DO outputs.

Naming conventions

ViGen will automatically create a default name for each ROMGEN configuration, with the configuration information encoded in the following manner:

rowwwwwbbbdf

where:
wwwww = number of words
bbb = word width
df = data file designater (from a to zz)

The default names for the two example ROMs would be:

ro01024008a
ro08192008a

VS700 Static RAM Generator

Preliminary Information

Features

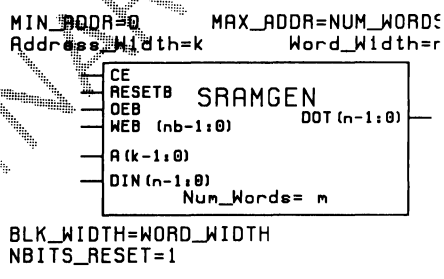
- Configurations up to 72K total bits
- Asynchronous operation – no clock
- Auto power-down after every read
- Independently tristatable outputs
- Multiple write enables allow partial word updates
- Non-zero starting address allowed
- Partial or full array asynchronous reset

Description

SRAMGEN produces a compiled static RAM. High performance is achieved through the use of address transition detection circuits and 2-level sense amps. An automatic power down circuit reduces power to leakage after every read access, eliminating the need to toggle CE for low frequency operation. From one to four write enable inputs allow writes to sub-fields of each memory location. An optional reset input allows a variable number of bits in each memory location to be reset asynchronously.

Symbol

The symbol for SRAMGEN will be unique for each configuration. An example is given here only for reference. Address_Width = $\lceil \log_2 (Num\_Words + Start\_Addr) \rceil$



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
Num_Words	8 → 8192	Number of words in the array[1, 2]
Word_Width	1 → 36	Word size in bits[1]
Start_Addr	0 → 8192–Num_Words	Address of first word in the array[3]
Blk_Width	1 → Word_Width	Number of bits per write enable Up to 4 write enables allowed if Word_Wdith >18 Up to 2 write enables allowed if Word_Width ≤18
Nbits_Reset	0 → Word_Width	Number of bits to reset in each word

[1] Total bits (Word_Width × Num_Words) must be ≤ 73,728.

[2] Num_Words is internally rounded up to 2 times the column decode factor. The column decode is selected to be 2, 4, 8, 16 or 32 by SRAMGEN to optimize area and performance.

[3] Start_Addr is internally rounded down to 2 times the column decode factor.

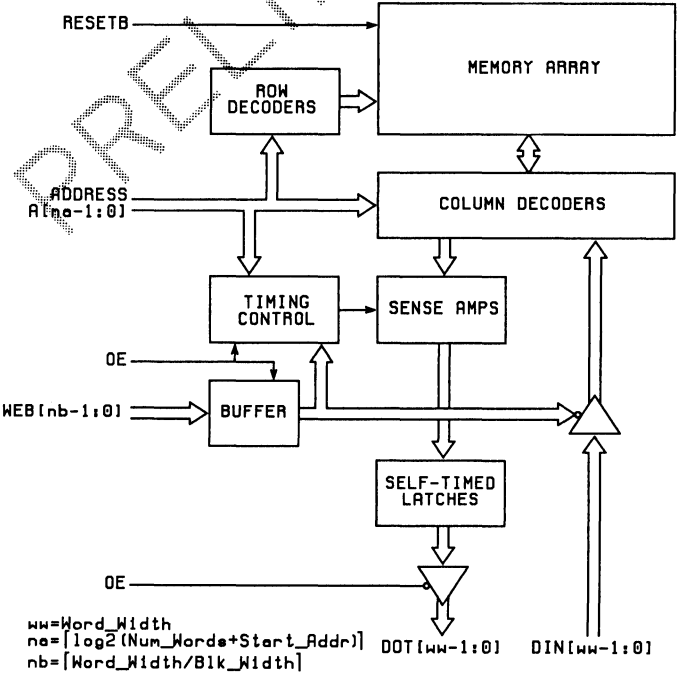
SRAMGEN

ViGen CONFIGURABLE FUNCTION

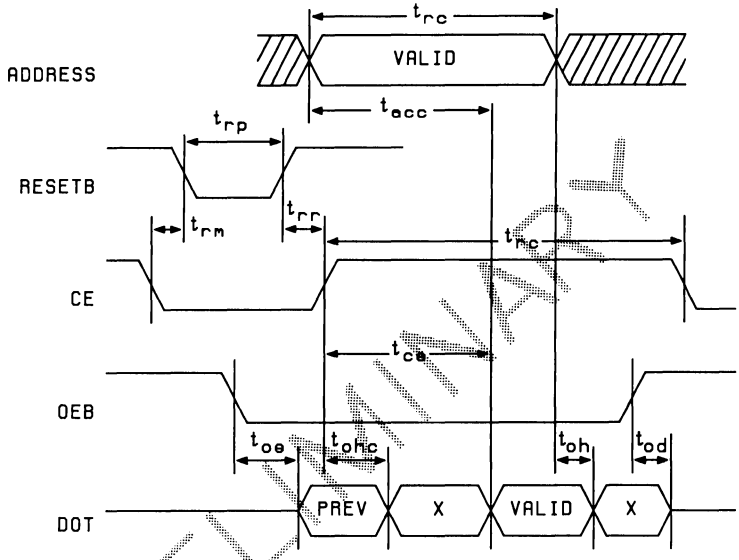
Inputs/Outputs

Pin/Bus Name (in TDL order)	Function	Cap (pF)
INPUTS:		
CE	Cell Enable, active high.	0.130
RESETB	Asynchronous reset, active low	0.020
OEB	Output Enable, active low	0.090
WEB[nb−1:0]	Write enable bus, active low nb=⌈Word_Width/Blk_Width⌉	0.150
A[na−1:0]	Address bus na = ⌈log2(Num_Words + Start_Addr)⌉	0.090
DIN[Word_Width−1:0]	Data input bus	0.065
OUTPUTS:		
DOT[Word_Width−1:0]	Data output bus	0.012

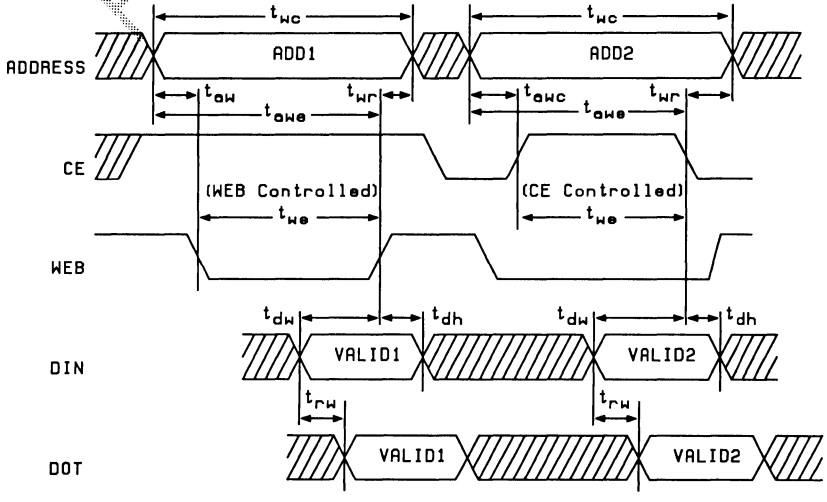
Functional Block Diagram



Read Cycle Timing



Write Cycle Timing



DPRGEN

ViGen CONFIGURABLE FUNCTION

VS1500 Dual Port RAM

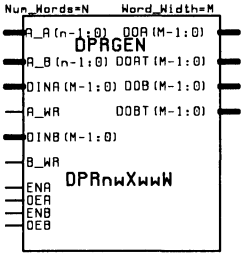
Description

- Variable size RAM array with two independent, bidirectional ports (A, B)
- Read-only option on port A saves area
- Tristate and always-driving outputs available on both ports
- Variable number of words and word size, up to 16K bits

The dual port RAM generator produces a RAM array with two fully independent read/write ports. Each port uses clocked operation to reduce complexity and operating power. Each port is precharged when its enable input is low and can read or write data when its enable input is high. To reduce logic circuitry and save cell area, Port A can be programmed to be a read-only port. Ports must be precharged between successive reads and writes.

Symbol

The symbol for DPRGEN will be unique for each configuration. An example is given here only for reference.



Input Parameter Ranges

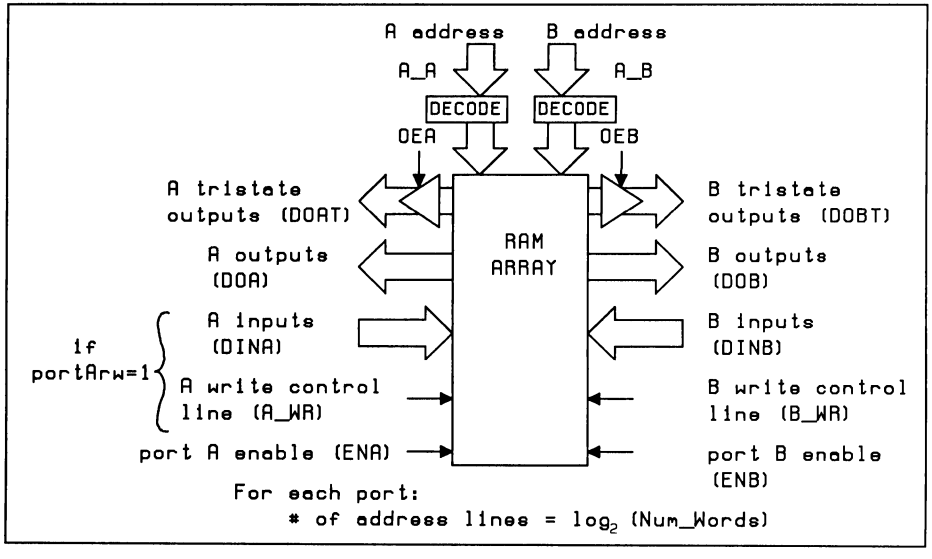
INPUT PARAMETER	ALLOWED RANGE	EXPLANATION
Num_Words	2–2048, even only	Number of data words in the RAM array. The number of address lines for each port will be n = $\log_2$ (Num_Words). Number of bits = Num_Words*Word_Width must be ≤ 16384.
Word_Width	2 – 32	Number of bits in a data word. This affects the number of DINA, DINB, DOA, DOAT, DOB, and DOBT pins. Number of bits = Num_Words*Word_Width must be ≤ 16384.
PortArw	0 or 1	0: port "A" is read-only. 1: port "A" is read/write. If port "A" is read-only, then the DINA and A_WR pins are removed from the schematic symbol.

Inputs/Outputs

Definitions of the DPRGEN inputs and outputs are given in the following table. Input and output pin names are listed in pin-number sequence.

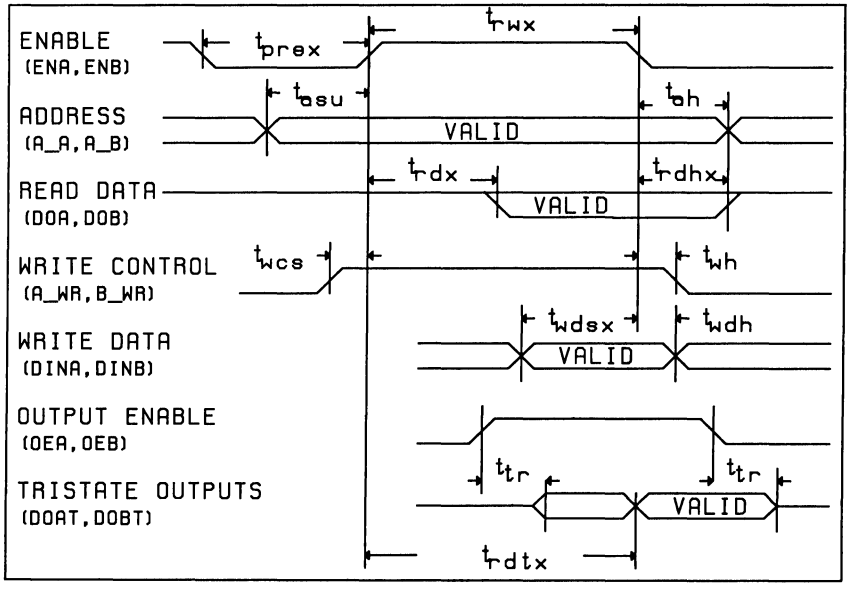
PIN NAME	DEFINITION	REQ/ OPT	CAP
INPUTS:			
A_A (n)	A port address bus (n = $\log_2$ (Num_Words))	REQ	0.159 pF
A_B (n)	B port address bus (n = $\log_2$ (Num_Words))	REQ	0.159 pF
DINA (M)	A port data in bus (M = Word_Width)	OPT	0.113 pF
A_WR	A port read/write control (active high write)	OPT	0.058 pF
DINB (M)	B port data in bus (M = Word_Width)	REQ	0.113 pF
B_WR	B port read/write control (active high write)	REQ	0.058 pF
ENA	A port enable pin	REQ	0.167 pF
OEA	DOAT (M) tristate enable pin	REQ	0.058 pF
ENB	B port enable pin	REQ	0.173 pF
OEB	DOBT (M) tristate enable pin	REQ	0.058 pF
OUTPUTS:			
DOA (M)	Always-driving A port output bus	REQ	
DOAT (M)	Tristate A port output bus	REQ	0.105 pF
DOB (M)	Always-driving B port output bus	REQ	
DOBT (M)	Tristate B port output bus	REQ	0.105 pF

Functional Block Diagram



AC Waveforms

The following waveforms apply equally to port A or port B. If the read only option is chosen for port A (portArw = 0), then ignore waveforms referring to write lines. A suffix of "x" in a timing parameter name should be substituted with "a" or "b" for the appropriate port.



Timing Parameters

t_{prex}	Minimum precharge time for port x
t_{asu}	Minimum address setup before rising enable (either port)
t_{ah}	Minimum address hold after falling enable (either port)
t_{rdx}	Maximum read access from rising enable on port x
t_{rdtx}	Maximum read access to tristate outputs from rising enable on port x
t_{rdhx}	Maximum read data hold after falling enable on port x
t_{wcs}	Write control setup before rising enable (either port)
t_{wh}	Write control hold after falling enable (either port)
t_{wdsx}*	Write data setup before falling enable of port x
t_{wdh}	Write data hold after falling enable (either port)
t_{tr}	Output enable to tristate on or off delay (either port)
t_{rwx}	Minimum enable high time of port x for read or write

* See Applications Note titled *Port Contention* which follows.

Timing Parameters and Cell Size

1. The input parameters are: Num_Words, Word_Width, portArw. CL is output capacitance in pF.
2. Internal column decode ("coldec") must be determined first. Follow these steps (these are the same steps followed by the layout compiler for DPRGEN):
   a. nbits = Num_Words*Word_Width;
   b. `IF (   0 <= nbits <   32) (trial_ncols =   2)` `ncols = number of RAM columns`
      `IF (  32 <= nbits <   64) (trial_ncols =   8)`
      `IF (  64 <= nbits <  192) (trial_ncols =  16)`
      `IF ( 192 <= nbits < 1024) (trial_ncols =  32)`
      `IF (1024 <= nbits < 8192) (trial_ncols =  64)`
      `IF (8192 <= nbits < inf.) (trial_ncols = 128)`
   c. coldec = trial_ncols/Word_Width
   d. Round coldec down to nearest valid value (1,2,4,8, or 16)
   e. Word limits on different values of column decode:
      Num_words must be >= 384 for coldec = 16
      Num_words must be >= 80 for coldec = 8
3. Num_Words is internally rounded up to the nearest multiple of 2*coldec.
4. TIMING EQUATIONS & CELL SIZE: (use nrows = Num_Words/coldec, ncols = Word_Width*coldec)
   – ^{t}prea is for port A, ^{t}preb is for port B, etc. No "a" or "b" suffix means either port.
   – All times in nanoseconds and are NOMINAL (V_{DD}=5.0 volts, T=25°C, Nom. process)
   –See *NCR ASIC Data Book* for process, voltage, and temperature derating.

		Example: Num_Words=16, Word_Width=16, portArw=1, CL=0 (coldec = 2)
^{t}asu = 1.38 + .0656*nrows	MIN	1.9 ns
^{t}ah = 0	MIN	0.0 ns
^{t}prea = 3.81 + .0419*nrows + .0497*ncols + 0.64*CL	MIN	5.7 ns
^{t}preb = 3.77 + .0419*nrows + .0509*ncols + 0.63*CL	MIN	5.7 ns
^{t}rda = 7.18 + .1513*nrows + .1134*ncols + 0.99*CL	MAX	12.0 ns
^{t}rdta = 7.30 + .1513*nrows + .1134*ncols + 1.70*CL	MAX	12.1 ns
^{t}rdb = 7.10 + .1538*nrows + .1197*ncols + 0.97*CL	MAX	12.2 ns
^{t}rdtb = 6.90 + .1538*nrows + .1197*ncols + 1.66*CL	MAX	12.0 ns
^{t}rdha = ^{t}prea	MAX	5.7 ns
^{t}rdhb = ^{t}preb	MAX	5.7 ns
^{t}tr = 2.0 + 1.70*CL	MIN	2.0 ns
^{t}wcs min. = −4.0, max. = 4.0		+4/−4 ns
^{t}wh min. = 0, max. = 4.0		0 to 4.0 ns
^{t}wdsa = 5.78 + .0538*nrows + .0291*ncols (See Note 1)	MIN	7.1 ns
^{t}wdsb = 6.06 + .0500*nrows + .0250*ncols (See Note 1)	MIN	7.3 ns
^{t}wdh = 1.17 + .0075*nrows + .0138*ncols	MIN	1.7ns
^{t}rwx = ^{t}rdx	MIN	a:12.0ns, b:12.2ns

Cell Width (mils) = 12.683 + 1.924*nrows + 1.745*portArw + 0.448*coldec (coldec > 2)
Cell Width (mils) = 16.876 + 1.924*nrows + 3.109*portArw (coldec = 1)
Cell Height (mils) = 11.237 + 1.143*ncols + 0.963*$\log_2$(nrows) + 0.211*coldec − 0.039*Word_Width

Note 1: See Applications Note titled *Port Contention* for a possible exception to this parameter value.

Timing Examples for 16X16 and 128X8 Dual Port Rams

SYMBOL	16X16 DUAL PORT RAM (PORT A READ/WRITE)	NOMINAL VDD=5V		WORST CASE VDD=4.5V						UNITS
		TA=25C		TA=70C		TA=85C		TA=125C		
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{asu}	Address Setup Time Before ENABLE	2		4		4		5		ns
t_{ah}	Address Hold Time after ENABLE	0		0		0		0		ns
t_{prea}	Precharge Time	6		12		13		15		ns
t_{preb}	Precharge Time	6		12		13		15		ns
t_{rwa}	Read or Write Enable High	13		26		27		30		ns
t_{rwb}	Read or Write Enable High	13		26		27		30		ns
t_{rda}	Read Access Time		13	26		27		30		ns
t_{rdb}	Read Access Time		13	26		27		30		ns
t_{rdta}	Tristate Read Access Time		13	27		28		31		ns
t_{rdtb}	Tristate Read Access Time		13	26		27		31		ns
t_{rdha}	Read Data Hold Time		6		12		13		15	ns
t_{rdhb}	Read Data Hold Time		6		12		13		15	ns
t_{tr}	Tristate and Untristate Time		3	6		6		7		ns
t_{wcs}	Write Control Setup	-4	4	-8	8	-9	9	-10	10	ns
t_{wh}	Write Control Hold	0	4		8		9		10	ns
t_{wdsa}	Write Data Setup	7		15		15		17		ns
t_{wdsb}	Write Data Setup	7		15		16		17		ns
t_{wdh}	Write Data Hold	2		3		4		4		ns

Switching Characteristics (Input tr,tf=1.4ns, CL=0.5pF)

SYMBOL	128X8 DUAL PORT RAM (PORT A READ-ONLY) PARAMETER	NOMINAL VDD=5V TA=25C		WORST CASE VDD=4.5V TA=70C		TA=85C		TA=125C		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{asu}	Address Setup Time Before ENABLE	2		5		5		6		ns
t_{ah}	Address Hold Time after ENABLE	0		0		0		0		ns
t_{prea}	Precharge Time	8		16		17		19		ns
t_{preb}	Precharge Time	8		16		17		19		ns
t_{rwa}	Read Enable High	17		36		37		42		ns
t_{rwb}	Read or Write Enable High	18		36		38		43		ns
t_{rda}	Read Access Time		17	36		37		42		ns
t_{rdb}	Read Access Time		18	36		38		43		ns
t_{rdta}	Tristate Read Access Time		18	37		38		43		ns
t_{rdtb}	Tristate Read Access Time		18	37		38		43		ns
t_{rdha}	Read Data Hold Time		8		16		17		19	ns
t_{rdhb}	Read Data Hold Time		8		16		17		19	ns
t_{tr}	Tristate and Untristate Time		3	6		6		7		ns
t_{wcs}	Write Control Setup	-4	4	-8	8	-9	9	-10	10	ns
t_{wh}	Write Control Hold	0	4		8		9		10	ns
t_{wdsb}	Write Data Setup	8		17		18		20		ns
t_{wdh}	Write Data Hold	2		4		5		5		ns

Switching Characteristics (Input tr,tf=1.4ns, CL=0.5pF)

Application Notes

Using the Tristate Outputs DOAT(i) and DOBT(i)

The tristate outputs of the dual port RAM generator are not implemented in quite the same way as in some other NCR supercells. Figure 7–6 shows the circuits used for both always–driving outputs (DOA(i) and DOB(i)) and the tristate outputs. Instead of a full CMOS transmission gate for the tristate outputs, a single n–channel transistor is used to reduce circuit area. The effect of this is that the tristate outputs, when driven high, will not reach a full V_{DD} level. Instead, they will reach a level of about 3.3 volts when V_{DD} is 5.0 volts. This is enough to be considered a logic high for subsequent gate inputs, but there will be reduced noise margin and increased DC power dissipation caused by this non–rail level.

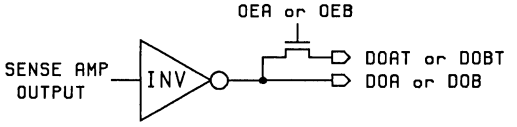


Figure 7–6 Tristate output circuit

For this reason it is important to use pull–up cells on each tristate output line (see Figure 7–7). This is good design practice for any tristate line used in semicustom design. The PU30 cell is not meant to provide a valid logic level on a bus line, but only to provide a "default" level for those times when it is not actively driven by anything else.

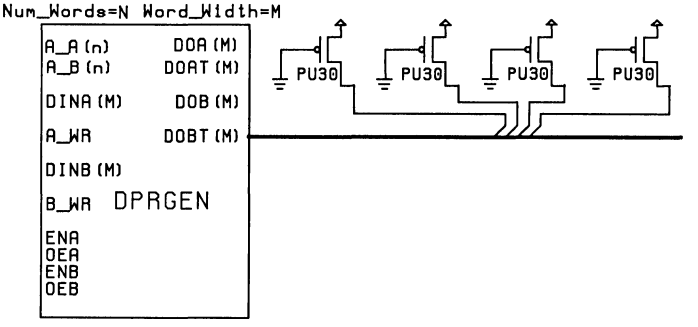


Figure 7–7 Tristate bus pullups

The pullups will cause no problem with "late 1s" on the tristate outputs. During the precharge phase for each port, the internal bit lines and sense amp inputs are pulled high. This causes the always–driving outputs to also go high during precharge. If the output enable line (OEA or OEB) is asserted at the beginning of a read phase, then the tristate outputs will also stay high if they were not immediately previously driven low by another

gate. There is no possibility of a glitch on this line (and therefore losing the good high level) since the read access time for a "1" is actually zero. Only 0's in the data word being read have non-zero access time.

Reducing AC Power Dissipation

For most designers, the AC power dissipation of CMOS semicustom chips is not a problem needing consideration since it is very low compared to bipolar or NMOS implementations. Some applications, though, need low AC operating power as well.

If the address lines are allowed to switch several times before becoming stable at the address setup time, then excess AC power dissipation will occur due to the large capacitances on the internal address lines and their complements. This kind of power dissipation is calculated as:

$P=CV^2f,$

P = power
C = total driven capacitance
V = voltage swing (= VDD)
f = switching frequency

Since C is fixed inside the RAM, reducing this power can only be done by reducing the number of times that the address lines switch. This can be done by latching the address lines externally to the dual-port RAM.

Port Contention

The A and B ports of the dual-port RAM are meant to be independent in operation. The possibility of contention between the two ports does exist, however, and can happen in the following combinations:

1. One port's write cycle overlaps the other port's read cycle to the same address (read/write contention).
2. Both ports' write cycles overlap to the same address (write/write contention).

Note that port contention doesn't exist if both ports are reading from the same address. Discrete, dual-port RAM chips contain contention logic that detects when both ports are attempting to access the same address (whether reading or writing). The port which drives this address second is given a busy signal by the contention logic, which inhibits it from actually reading or writing to that address. When the first port has switched to a different address, the busy signal to the second port is deactivated.

This generator does not contain such contention logic, so care must be taken to assure correct operation. The benefit to not including this logic is more flexible operation. For instance, two-port reads can occur from the same address without one port being locked out. This is important for register files, for an example see Figure 7-9.

Read/write contention can happen in three different ways (see Figure 7–8), and only one of them causes real contention. Of the three read/write overlaps shown, only the first, where the read on one port isn't complete before the other port starts to write, is a case of real port contention and must be avoided. In the second case, where both enables overlap within ± 4ns, there will be no contention *if the data to be written is stable from the beginning of the write enable*. This overrides the write data setup time parameter in the AC characteristics table. In the third case, the data written to the addressed word will be stable in time for the reading port to access it, so no contention occurs.

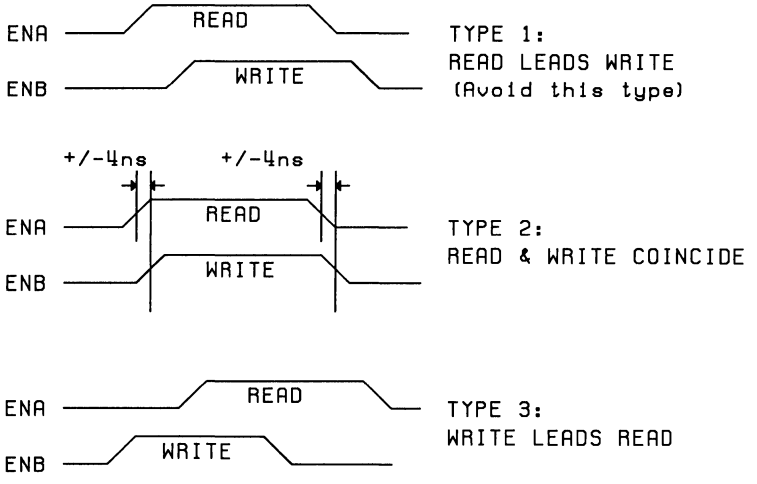


Figure 7–8 Read/Write port contention

Write/write combinations will always cause contention, since the data in the addressed word will contain unknown data except when both ports write identical data. If the enable signals ENA and ENB don't overlap their high times at all, then there is no contention.

Designing for Testability

A test program for a semicustom chip must be able to verify that all circuit functions operate correctly. This implies both functional correctness (correct design) and fault detection (the circuit was manufactured without defects). Several methods exist for a achieving both of these goals, all of which involve some trade-off between degree of checking and the amount of extra logic required. These include:

1. Multiplex part pins to the address and data pins in a test mode.
2. Use scan registers to serially shift in address and input data, and shift out output data.

See the NCR VS2000 Standard Cell Library Databook, Section 6, "Designing for Testability" for more information.

Example of Register File Used with ALU

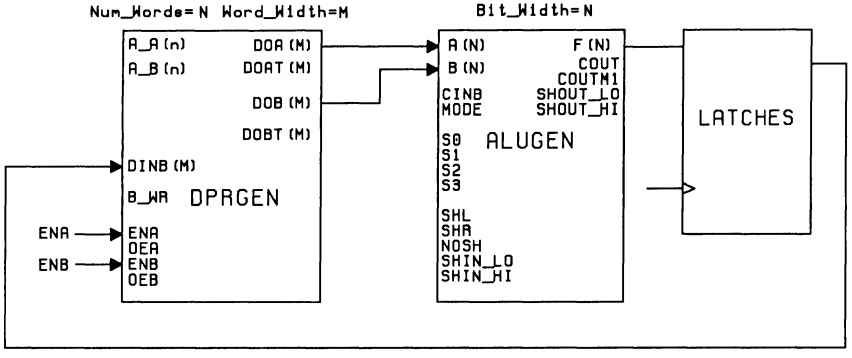


Figure 7-9 DPRGEN as a register file source for ALU operands

In Figure 7-9, the two operands for the ALU are read simultaneously from the A and B ports of the RAM, and then the ALU result is written back to the RAM through port B on the next cycle. The "PortArw" parameter for this RAM is set to "0" because the A port never has data written to it. There will never be any possibility of port contention because of this. The enable signals for each port can be tied together, which causes a dummy read of port A when the result is being written back through port B, or they can be separated as shown. Tying them together requires less logic to generate the ENA signal, but increases the operating power dissipation.

Example of FIFO

Figure 7–10 shows an implementation of a FIFO using the dual-port RAM supercell. Less sophisticated shift register type FIFOs can be built using the "SHFTGEN" supercell.

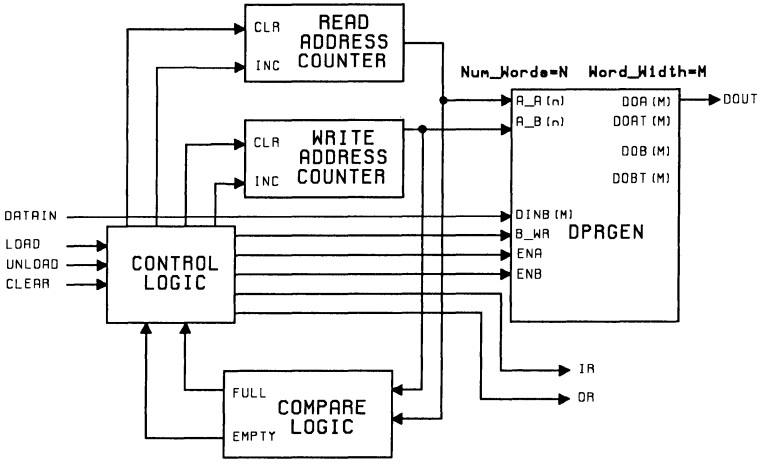


Figure 7–10 DPRGEN used in a FIFO buffer

Data is loaded with the LOAD input from DATAIN, and data is led out to the DOUT bus using UNLOAD. Address comparison determines whether the buffer is full (read address equals write address plus 1) or empty (write address equals read address plus 1). The IR flag (Input Ready) indicates that the FIFO is not full, and the OR flag (Output Ready) indicates the not empty condition.

Naming Conventions

ViGen will automatically create a default cell name for each unique DPRGEN configuration with the configuration information encoded in the following manner:

drwwwwbbpp

where:
wwww = number of words
bb = word width
pp = port (w=write/nw=non-writable)

Therefore, the default names for the two example configurations would be:

dr001616w
dr012816nw

Limitations

QUICKSIM Save and Restore functions will not currently operate with generated cells.

Simulation Error Messages

Simulation using the Mentor Quicksim simulator is done using a behavioral language model (BLM). This model checks for timing and usage errors during simulation. A listing of the possible error message types and their descriptions is included here.

MESSAGES REPORTED BY DPRGEN CONTAIN TWO MAJOR TYPES:

1. OPERATIONAL ERRORS – caused by invalid operation: Unknown data on control lines.
   Invalid states/modes.
   Improper sequence of states.

   OPERATIONAL ERROR SYNTAX

   $inst_name: ERROR *time_of_error error_description*
   $inst_name: *action taken by model because of error*
   $inst_name:

   OPERATIONAL ERRORS INCLUDE

   UNKNOWNS ON ADDRESSES DURING READ.
   UNKNOWNS ON ADDRESSES DURING WRITE.
   WRITE TO SAME ADDRESS FROM A&B PORTS SIMULTANEOUSLY.
   READ/WRITE TO SAME ADDRESS FROM A&B PORTS OUT OF SPEC (see *Port Contention).*
   NO PRECHARGE BETWEEN SUCCESSIVE READ/WRITE OPERATIONS.

   example:

   $i21(dprgen): ERROR Time=2013 UNKNOWN ADDRESS ON A PORT DURING WRITE
   $i21(dprgen): UNKNOWN DATA WILL BE WRITTEN TO EVERY BLOCK OF RAM ARRAY
   $i21(dprgen): WHICH IS ENABLED.

2. TIMING ERRORS/WARNINGS – caused by violation of timing specifications in documentation.
   Warning messages are produced when transitions occur within a margin delta of specification value.

   TIMING ERROR/WARNING SYNTAX

   $inst_name: ERROR *msg_type* OF TYPE *type_check spec_name current_time*
   $inst_name: *control_pin_name direction_of_edge* at *transition_time* ns
   $inst_name: *data_pin_name* changed at *transition_time* ns
   $inst_name: spec is *spec_value* ns (+*margin_value* ns margin)

   examples:

   $i21(dprgen): ERROR TIMING VIOLATION OF TYPE SETUP t_WDS Time=2103 ns
   $i21(dprgen): ENB falling at 1987 ns
   $i21(dprgen): DINB changed at 1980 ns
   $i21(dprgen): spec is 17 ns (+5 ns margin)

   $i21(dprgen): ERROR MARGIN WARNING OF TYPE SETUP t_WDS Time=2103 ns
   $i21(dprgen): ENB falling at 1987 ns
   $i21(dprgen): DINB changed at 1967 ns
   $i21(dprgen): spec is 17 ns (+5 ns margin)

FIFOGEN

ViGen CONFIGURABLE FUNCTION

VS1500 FIFO Generator

Features

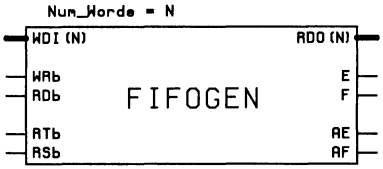
- Compiled FIFO cell allows flexible configurations of up to 6K bits
- Maximum word width of 36 bits
- Maximum number of words is 512
- Fully asynchronous Read/Write operation
- User configurable Almost Full flag
- User configurable Almost Empty flag
- Retransmit ability

Description

FIFOGEN produces a compiled first in first out memory block. FIFOGEN is based on a dual port latch memory cell which allows for completely asynchronous read/write operation. Read and write address values are stored in ring counters which may be cleared with the RSb (Reset) input. The read counter may be independently cleared using the RTb (retransmit) input, thus allowing data to be re-read multiple times. FIFOGEN also has status flags for Empty, Full, Almost Empty, and Almost Full. The user may configure the Almost Full and Almost Empty flags to activate any chosen offset from full and empty respectively.

Symbol

The symbol for FIFOGEN will be unique for each configuration. An example is given here only for reference.



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
Num_Words	4 - 512	Number of words in the FIFO[1], [2]
Word_Width	1 - 36	Number of bits in a word[1]
ae_offset	1 - words-1	Almost Empty offset from Empty for flag activation
af_offset	1 - words-1	Almost Full offset from Full for flag activation

[1] Total number of bits (**Num_Words** x **Word_Width**) must be ≤ 6K.

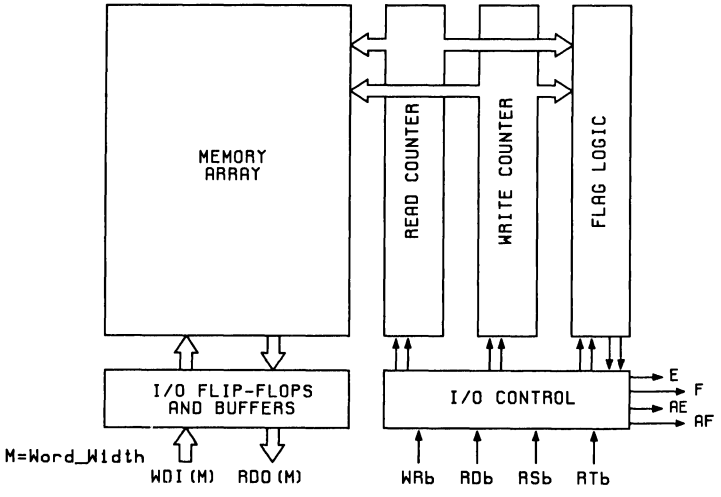
[2] **Num_Words** is internally rounded up to a multiple of the column decode. The column decode is internally selected to be 1-8 (by 1) by FIFOGEN to optimize area and performance. Any changes in **Num_Words** will be reported to the user at configuration time.

Inputs/Outputs

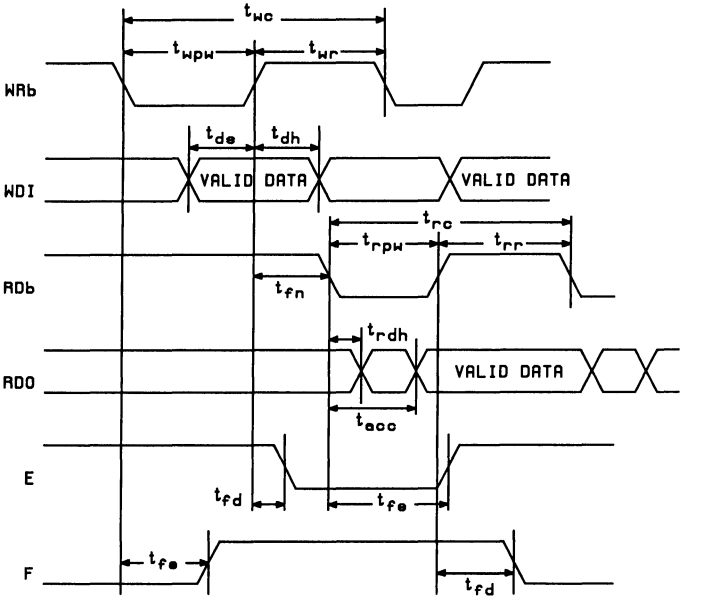
Bus Widths: M = **Word_Width**

Pin/Bus Name (in TDL order)	Function	Req/ Opt	Cap (pF)
INPUTS:			
WRb	Write control pin, active LOW	Req	0.10
RDb	Read control pin, active LOW	Req	0.10
RTb	Retransmit control pin, active LOW. Resets the read counter to first physical memory location	Req	0.10
RSb	Reset control pin, active LOW. Resets the read and write counters to first physical memory location.	Req	0.15
WDI[M]	Write data input bus	Req	0.08
OUTPUTS:			
RDO[M]	Read data output bus	Req	
E	Empty Flag, set HIGH on falling edge of RDb when reading last data word, reset on next rising edge of WRb	Req	
F	Full Flag, set HIGH on falling edge of WRb when writing last data word, reset on next rising edge of RDb	Req	
AE	Almost Empty Flag, set HIGH on falling edge of RDb when reading last data word, reset on rising edge of WRb	Req	
AF	Almost Full Flag, set HIGH on falling edge of WRb when writing last data word, reset on rising edge of RDb	Req	

Functional Block Diagram



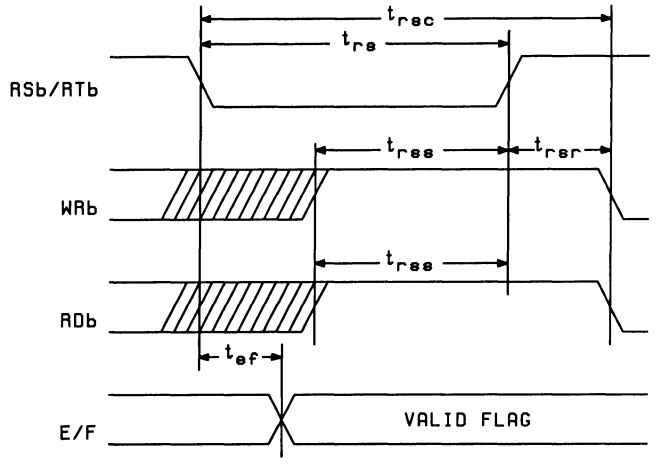
AC Waveforms – Read/Write



Timing Parameters – Read/Write

Name	Description
t_{wc}	Minimum Write cycle time
t_{wpw}	Minimum WRb pulse low
t_{wr}	Minimum Write recovery time (WRb high)
t_{ds}	Minimum data setup time from rising edge of WRb
t_{dh}	Minimum data hold time after rising edge of WRb
t_{rc}	Minimum Read cycle time
t_{rpw}	Minimum RDb pulse low
t_{rr}	Minimum Read recovery time (RDb high)
t_{acc}	Maximum delay RDb falling to valid data
t_{rdh}	Minimum data hold time after falling edge of RDb
t_{fe}	Flag Enable Delay
t_{fd}	Flag Disable Delay
t_{fn}	First Write to first valid Read

AC Waveforms – Reset/Retransmit



Timing Parameters – Reset/Retransmit

Name	Description
t_{rsc}	Minimum Reset/Retransmit cycle time
t_{rs}	Minimum Reset/Retransmit Pulse low
t_{rss}	Minimum WRb/RDb setup before RSb/RTb rising
t_{rsr}	Minimum Reset/Retransmit recovery time
t_{ef}	Minimum Reset/Retransmit to flag output

Timing, Power, and Area Equations

FIFOGEN will select its internal configuration based on the requested parameters. A simple algorithm is used which determines an internal architecture which will optimize area/performance tradeoffs. This architecture defines the number of rows and columns of the memory array. Because the user has no control over the internal column decode, **the resulting configuration may have more words than requested** (but never less). The algorithm is geared to minimize this discrepancy. The user will be notified at configuration time of the actual size of the array. Equations are given in terms of input parameters and internal architecture parameters. These can be found by following these steps:

1. CL is the output capacitance in pF.
2. Generator input parameters which affect delays are **Num_Words**, **Word_Width**. Derived parameters are **col_dec** and **rows**.
3. Calculate first-pass values for derived parameters, for area and performance a square array is best. Use (i).
4. In order to assure reasonable wordline performance, check array width; if it is greater than optimum length (72), decrease column decode (**col_dec**) by one. (ii).
5. Otherwise to optimize number of rows, check if increasing column decode would not cause too long a word line (iii).
6. Finally recalculate **rows** if **col_dec** changed (iv).

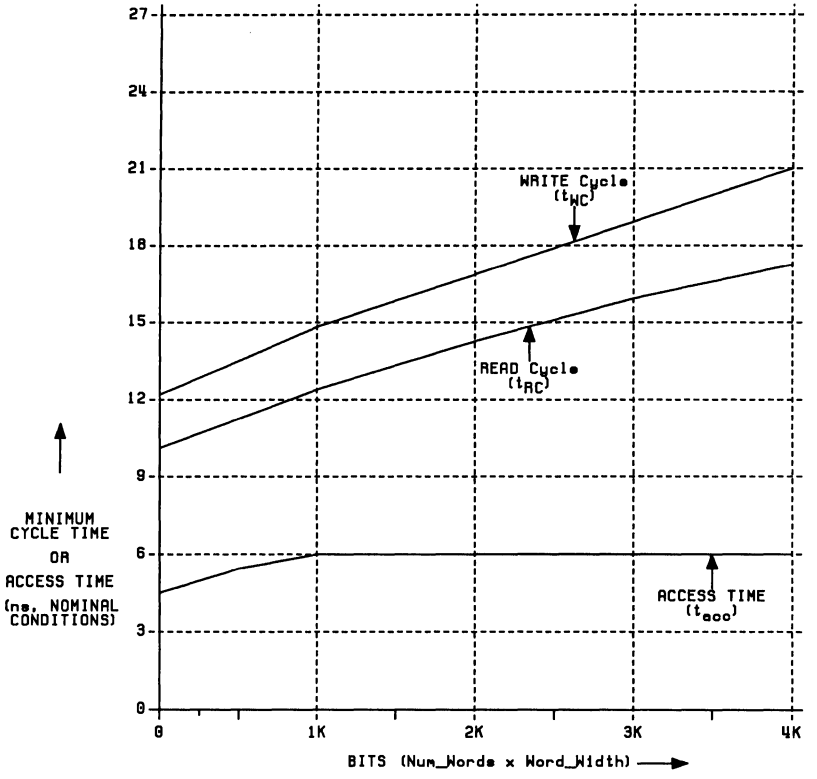
i. if (**Num_Words** ≤ 32) **col_dec** = 1
else {
rows = SQRT(**Num_Words***Word_Width**)**, rounded up to an Integer.
col_dec = **Num_Words/rows**, rounded up to an Integer.
if (**col_dec** >8) **col_dec** = 8
ii. if (**col_dec***Word_Width** > 72) **col_dec** = **col_dec**−1;
iii. else if (**col_dec***Word_Width** < (72 − **Word_Width**) & **col_dec** < 8) **col_dec** = **col_dec** +1;
}
iv. **rows** = **Num_Words/col_dec**, rounded up to an integer

All times are NOMINAL (V_{DD} = 5.0 volts, T = 25° C, nominal process). See the *NCR ASIC VS700 Data Book* for voltage and temperature derating values. I_{DD} is specified at V_{DD} = 5.5 volts, T = 25° C, and worst case current process.

PARAM	DESCRIPTION	UNITS	TYPICAL VALUE (ns)
t_{wc}	Write Cycle	ns	= 9.342 + 0.014×**Word_Width** + 0.122×**rows** + 0.028×**cols**
t_{wpw}	Write Pulse low	ns	= 4.141 + 0.111**rows** + 0.016×**cols**
t_{wr}	Write Pulse high	ns	= 5.201 + 0.014×**Word_Width** + 0.010×**rows** + 0.013×**cols**
t_{ds}	Write Data Setup	ns	= 0.569 + 0.006×**col_dec**
t_{dh}	Write Data Hold	ns	= 2.109 + 0.017×**Word_Width** + 0.003×**cols**
t_{rc}	Read Cycle Time	ns	= 7.541 + 0.086×**col_dec** + 0.084×**rows** + 0.030×**cols**
t_{rpw}	Read Pulse low	ns	= 4.141 + 0.111**rows** + 0.016×**cols**
t_{rr}	Read Pulse high	ns	= 3.400 + 0.086×**col_dec** + 0.025×**cols**
t_{acc}	Read Access	ns	= 3.975 + 0.030×**Word_Width** + 0.018×**col_dec** + 0.003×**cols** + 0.626×**CL**
t_{rdh}	Read Data Hold	ns	= 3.275 + 0.195×**CL**
t_{fe}	Flag Enable Delay	ns	= 4.365 + 0.626×**CL**
t_{fd}	Flag Disable Delay	ns	= 3.938 + 0.626×**CL**
t_{fn}	1st Write to Read	ns	= 8.622 + 0.089×**col_dec** + 0.055×**rows** + 0.032×**cols**
t_{rsc}	RSb/RTb Cycle Time	ns	= 5.425 + 0.007×**Word_Width** + 0.068×**col_dec** + 0.120×**rows** + 0.005×**cols**
t_{rs}	RSb/RTb Pulse low	ns	= 2.614 + 0.082×**rows** + 0.005×**cols**
t_{rss}	WRb/RD/b Setup to RSb/RTb	ns	= 0.750 + 0.059×**rows** + 0.007×**cols**
t_{rsr}	RSb/RTb Recovery Time	ns	= 2.811 + 0.007×**Word_Width** + 0.068×**col_dec** + 0.038×**rows**
t_{ef}	RSb/RTb to Flag delay	ns	= 4.083 + 0.019×**col_dec** + 0.076×**rows** + 0.007×**cols** + 0.626×**CL**
I_{DD}	Average current per port	mA/ MHz	= 0.148 + 0.004 ×**rows** + 0.02×**Word_Width**
Width	Layout width	mils	= 30.33 + 1.180×**cols**
Height	Layout height	mils	= 22.60 + 0.46×**col_dec** + 1.450×**rows**

Timing Constants: K = 0.08 ns, M_{CLH} = 0.261, M_{CHL} = 0.261
Process Derating: B = 0.66, N = 1.00, W = 1.40

Access and Cycle Times



(See NCR VS1500 ASIC Data Book for process, voltage, and temperature derating factors.)

Timing Examples

Timing for a 64x4 FIFO

Symbol	64x4 FIFO	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	Read access time		4.3		8.3		8.7		9.8	ns
t_{rdh}	Read data hold		3.3		6.4		6.7		7.5	ns
t_{wc}	Write cycle	11.5		21.6		22.5		25.2		ns
t_{rc}	Read cycle	9.7		18.0		18.8		21.1		ns
t_{fn}	First write till first read	10.4		19.5		20.3		22.3		ns
t_{rsc}	Reset cycle time	5.4		13.9		14.5		16.3		ns
t_{ds}	Write data setup time	0.6		1.1		1.2		1.3		ns
t_{dh}	Write data hold	2.2		4.2		4.6		4.9		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 0.280 mA/MHz
AREA = 53.93 x 43.75 = 2360 mil^2

Timing for a 256x9 FIFO

Symbol	256X9 FIFO	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	Read access time		4.7		8.9		9.3		10.5	ns
t_{rdh}	Read data hold		3.3		6.4		6.7		7.5	ns
t_{wc}	Write cycle	15.8		29.4		30.6		34.4		ns
t_{rc}	Read cycle	13.1		24.5		25.6		28.7		ns
t_{fn}	First write till first read	13.3		24.8		25.9		29.0		ns
t_{rsc}	Reset cycle time	10.7		20.0		20.9		23.4		ns
t_{ds}	Write data setup time	0.61		1.1		1.2		1.3		ns
t_{dh}	Write data hold	2.5		4.6		4.8		5.4		ns

Switching characteristics (Input t_r, t_f = .5ns nominal, CL = 0.1pF)
Iavg(ac) = 0.476 mA/MHz
AREA = 104.67 x 79.47 = 8318.1 mil^2

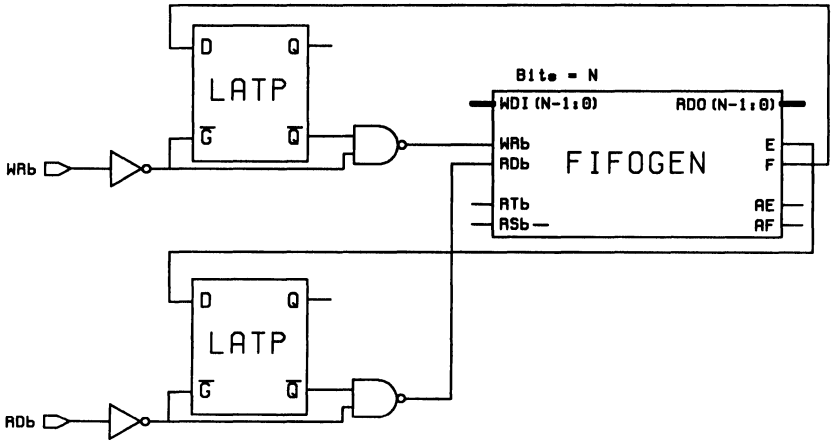
Application Notes

On power up a Reset must be performed before any other operations are performed. This assures that the FIFO is starting from a known state.

Reading the FIFO when it is empty and writing to a full FIFO will cause the status flags to be set unknown during simulation. While the logical state of the flags is predictable, the meaning of the status flags (full, empty, etc.) becomes ambiguous. A reset will clear the FIFO.

Retransmit allows the read pointer to be reset to the first physical memory address. Care must be taken to assure that the intended operation is achieved. Retransmit also causes ambiguous definition of the status flags. During retransmit the empty flag will be set false and the full flag true, so only reads should be performed until the FIFO is empty. The full flag will remain true until the FIFO is empty.

The following circuit may be used to disable reads when the FIFO is empty and writes when it is full.



Naming Conventions

ViGen will automatically create a default name for each FIFOGEN configuration, with the configuration information encoded in the following manner:

fwwwbbeeefff

where:
www = number of words
bb = word width
eee = almost empty offset
fff = almost full offset

All of the values have the given number of digits. Values that have less than the given number of digits will be left-padded with zeroes. For instance, a 31x8 FIFO with AE=4 and AF=5 will have a name of:

f03108004005

MACCGEN

ViGen CONFIGURABLE FUNCTION

VS1500 MAC Generator

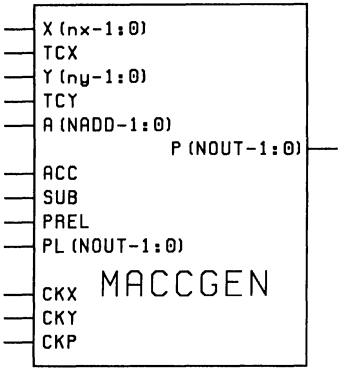
Features

- Variable size compiled multiplier accumulator function
- X and Y inputs independently selectable from 6 to 32 bits wide
- High performance architecture uses Booth encoding and Wallace tree partial product summation
- Two's complement, unsigned magnitude, and mixed mode multiplication
- Input number format can be pin-selectable
- Extra adder input allows implementation of P(i) = X × Y + A ± P(i−1). The A input is usually used for rounding
- X and Y inputs have separate registers and clocks
- Output is registered, with its own clock
- Accumulator functions include ACC, SUB, and preload
- Output may be accumulated up to eight extra bits

Symbol

The symbol for MACCGEN will be unique for each configuration. An example is given here only for reference.

where NOUT = nx + ny + acc_bits
NADD = nx + 4



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
nx	6 – 32 (even only)	Number of bits in the X input word
ny	6 – 32 (even, ny≤nx)	Number of bits in the Y input word
tcx	0, 1, or 2	=0: X in unsigned magnitude format =1: X in two's complement format =2: X input format selectable with an input pin (TCX)
tcy	0, 1, or 2	=0: Y in unsigned magnitude format =1: Y in two's complement format =2: Y input format selectable with an input pin (TCY)
add_in	0 or 1	Selects whether extra word A is to be added (1 = yes)
acc_bits	2, 4, 6, or 8	Number of extra bits to accumulate beyond nx+ny

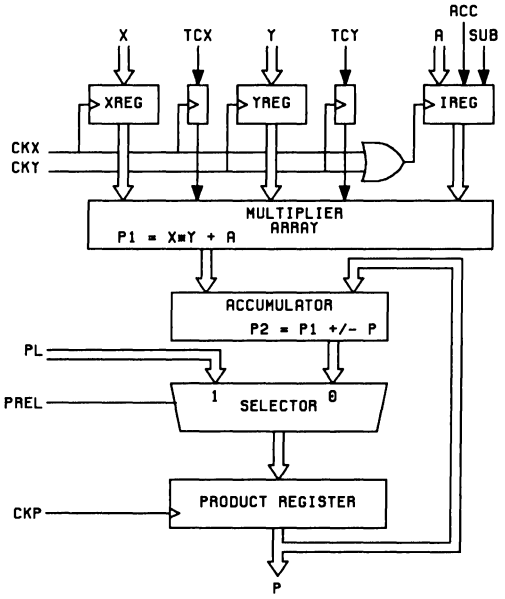
Inputs/Outputs

Pin/Bis Name (in TDL order)	Function	Req/ Opt	Cap (pF)
INPUTS:			
X[0:nx−1]	X input bus. Data on X is loaded into the X input register on the rising edge of CKX.	Req	0.164
Y[0:ny−1]	Y input bus. Data on Y is loaded into the Y input register on the rising edge of CKY.	Req	0.160
A[0:nx+acc_bits+3]	Optional adder input, usually used for rounding. Data on A is loaded into the A register on the rising edge of the logical OR of CKX and CKY. A is treated as a two's complement number, regardless of tcx and tcy selections. Exists if add_in=1.	Opt	0.060
CKX	X input clock, active on rising edge	Req	0.162
CKY	Y input clock, active on rising edge	Req	0.162
CKP	Clock input for the product register. Active on rising edge.	Req	0.110
TCX	X input two's complement control. When HIGH, the X input is treated as a two's complement number. When LOW, X is treated as an unsigned magnitude number. Exists if tcx=2.	Opt	0.091
TCY	Y input two's complement control, similar to TCX. Exists if tcy=2.	Opt	0.100
ACC	Accumulate control. When HIGH, the contents of the product register are added to or subtracted from the current product XxY(+A). Sampled on the rising edge of the logical OR of CKX and CKY.	Req	0.060
SUB	Subtract. When ACC and SUB are both HIGH, the contents of the product register are subtracted from the current product XxY(+A). Sampled on the rising edge of the logical OR of CKX and CKY.	Req	0.060
PREL	Preload control. When HIGH, data on the PL input bus is loaded into the product register on the rising edge of CKP.	Req	0.375
PL[0:nx+ny+acc_bits−1]	Preload bus. Data from PL is loaded into the product register on the rising edge of CKP.	Req	0.153
OUTPUTS:			
P[0:nx+ny+acc_bits−1]	Product register output bus, indicating the current contents of the product register. Updated on the rising edge of CKP.	Req	

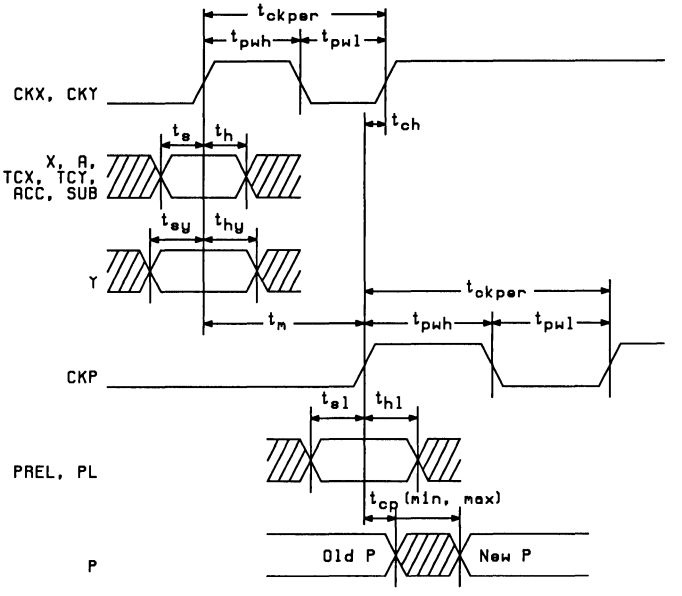
Timing Parameters

Name	Description
t_{ckper}	Minimum clock period for CKX, CKY, or CKP
t_m	Clocked multiply time
t_{cp}	Output delay time for P outputs after a rising CKP edge. The minimum time is the hold time for the previous product, and the time between minimum and maximum is the bus settling time.
t_s	Setup time for X, A, TCX, and TCY inputs before a rising CKX or CKY edge
t_h	Hold time for X, A, TCX, and TCY inputs after a rising CKX or CKY edge
t_{sy}	Setup time for Y inputs before a rising CKY edge
t_{hy}	Hold time for Y inputs after a rising CKY edge
t_{sl}	Setup time for PREL and PL inputs before a rising CKP edge.
t_{hl}	Hold time for PREL and PL inputs after a rising CKP edge.
t_{pwh}	Minimum high clock pulse width
t_{pwl}	Minimum low clock pulse width
t_{ch}	Relative hold time. CKP must rise at or before CKX or CKY to guarantee correct product output.

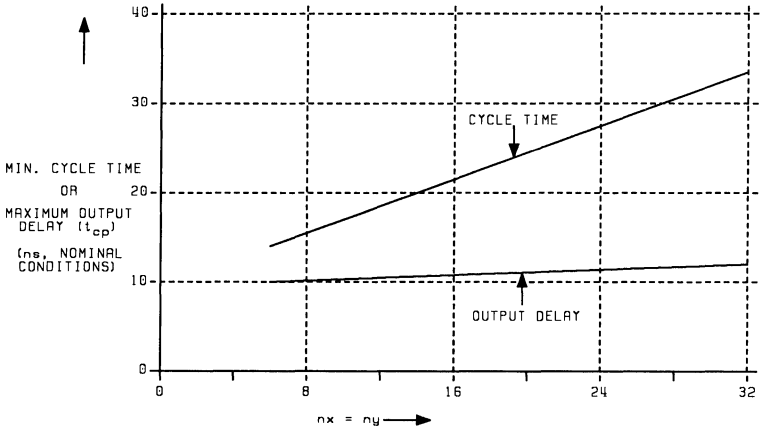
Functional Block Diagram



MACCGEN AC Waveforms



Cycle Time for Square MACS (nx = ny, acc_bits = 4)



(See NCR ASIC Data Book for process, voltage, and temperature derating factors.)

Timing, Power, and Area Equations

1. Input parameters for the following equations are nx, ny and acc_bits. CL is the output capacitance in pF.
2. Timing parameters are specified for nominal process, V_{DD}=5.0 volts, and temperature = 25°C. See the NCR ASIC Data Book for information on derating factors for process, voltage and temperature.
3. All delays for rising and falling outputs are equal, while rise and fall times are individually specified.

PARAM	DESCRIPTION	TYPICAL VALUE (ns)
t_{ckper}	Min. clock period	t_{ckper} = 9.70 + 0.08*nx + 0.67*ny
t_m	Max. clocked multiply/acc or multiply/sub	t_m = 9.70 + 0.08*nx + 0.67*ny
t_{cp}	Output delay NOTE: See App. note #1	$t_{cp(max)}$ = 8.70 + 0.027*nx + 0.060*ny + 0.179*acc_bits + 1.23*CL $t_{cp(min)}$ = 3.57 + 0.020*ny + 1.23*CL
t_s	X,A,TCX, and TCY setup	t_s = 1.56
t_h	X,A,TCX, and TCY hold	t_h = 1.57 + 0.034*nx
t_{sy}	Y setup	t_{sy} = 1.36
t_{hy}	Y hold	t_{hy} = 1.85 + 0.011*ny
t_{sl}	PREL and PL setup	t_{sl} = 1.75 + 0.100*nx + 0.081*ny + 0.097*acc_bits
t_{hl}	PREL and PL hold	t_{hl} = 2.27 + 0.019*nx + 0.028*ny + 0.016*acc_bits
t_{pwh}	Min. high clock pulse	t_{pwh} = 45% of t_{ckper}
t_{pwl}	Min. low clock pulse	t_{pwl} = 45% of t_{ckper}
t_{ch}	Relative hold time	t_{ch} = 0

Rise and Fall Times

t_r = 0.325 + 2.55*CL
t_f = 0.279 + 1.99*CL

Current Requirements: I = 0.0174*ny^2 + 0.115*(nx−ny) mA/MHz
Worst case current process, V_{DD} = 5.5V, T = 25°C
Toggling 0x0 and FF..FFxFF..FF and accumulating

Cell Width (mils) = 9.68 + 2.47*nx + 1.91*ny + 2.33*acc_bits
Cell Height (mils) = 30.72 + 5.86*ny + 2.60*add_in + offset
where: offset = 0 if tcy=1
offset = 11.72 if tcy=0 or 2

Timing Examples

8 x 8 two's complement MAC with rounding, 20–bit product register

(mac0808tta4: nx = 8, ny = 8, tcx = 1, tcy = 1, add_in = 1, acc_bits = 4)

Symbol	8 x 8 MAC	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ckper}	Minimum clock period	15.70		29.4		30.6		34.2		ns
t_m	Maximum multiply time		15.70		29.4		30.6		34.2	ns
t_{cp}	Output delay from CKP	3.91	10.29	7.3	19.3	7.6	20.1	8.5	22.4	ns
t_s	Minimum setup time for X, A inputs	1.56		2.9		3.0		3.4		ns
t_h	Minimum hold time for X, A inputs	1.84		3.4		3.6		4.0		ns
t_{sy}	Minimum setup time for Y inputs	1.36		2.5		2.6		2.9		ns
t_{hy}	Minimum hold time for Y inputs	1.94		3.6		3.7		4.2		ns
t_{sl}	Minimum setup time for PREL, PL	3.59		6.7		7.0		7.8		ns
t_{hl}	Minimum hold time for PREL, PL	2.71		5.1		5.3		5.9		ns
t_{pwh}	Minimum high clock pulse	7.07		13.2		13.8		15.4		ns
t_{pwl}	Minimum low clock pulse	7.07		13.2		13.8		15.4		ns
t_{ch}	Relative hold time	0		0		0		0		ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.15pF)

16 x 16 unsigned MAC with no rounding, 36–bit product register

(mac1616uun4: nx = 16, ny = 16, tcx = 0, tcy = 0, add_in = 0, acc_bits = 4)

Symbol	16 x 16 MAC	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ckper}	Minimum clock period	21.70		40.6		42.3		47.3		ns
t_m	Maximum multiply time		21.70		40.6		42.3		47.3	ns
t_{cp}	Output delay from CKP	4.07	10.99	7.6	20.6	7.9	21.4	8.9	24.0	ns
t_s	Minimum setup time for X inputs	1.56		2.9		3.0		3.4		ns
t_h	Minimum hold time for X inputs	2.11		4.0		4.1		4.6		ns
t_{sy}	Minimum setup time for Y inputs	1.36		2.5		2.6		2.9		ns
t_{hy}	Minimum hold time for Y inputs	2.03		3.7		3.9		4.4		ns
t_{sl}	Minimum setup time for PREL, PL	5.03		9.4		9.8		11.0		ns
t_{hl}	Minimum hold time for Y PREL, PL	3.09		5.8		6.0		6.7		ns
t_{pwh}	Minimum high clock pulse	9.77		18.3		19.0		21.3		ns
t_{pwl}	Minimum low clock pulse	9.77		18.3		19.0		21.3		ns
t_{ch}	Relative hold time	0		0		0		0		ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.15pF)

Application Notes

Output Delay Calculations

Due to the way that the product register is implemented within MACCGEN, the delay from CKP to P is actually dependent on the multiply cycle time. The delay, t_{cp}, is calculated with both a minimum and a maximum value. The minimum value of t_{cp} is the output hold time for the previous product P. Data on the P output bus will not change before t_{cp}(min). The maximum value of t_{cp}, as calculated, only applies when the MAC is being run at maximum frequency (minimum rising CKX/CKY to rising CKP). If the MAC is being run slower, then t_{cp}(max) actually gets less, as shown in Figure 1.

Above a certain multiplication period, referred to in Figure 1 as t_{sync}, t_{cp}(max) will have the same value as t_{cp}(min). In other words, all of the bits in the P bus will switch simultaneously. For multiplication periods between t_{ckper}(min) and t_{sync}, t_{cp}(max) derates linearly as shown.

The period t_{sync} is defined as:

$$t_{sync} = t_{ckper}\ (min) + 1.2^{*}\ (\ t_{cp}(max) - t_{cp}(min)\ )$$

where t_{ckper}, $t_{cp}(max)$, and $t_{cp}(min)$ are all as defined in the parametric equations.

Although the $t_{cp}(min)$ and $t_{cp}(max)$ parameters for each output pin will be slightly different due to differing output capacitive loads, for simplicity the simulation model will assign the shortest $t_{cp}(min)$ and the longest $t_{cp}(max)$ values to the entire P bus. This effect will be minor in most situations.

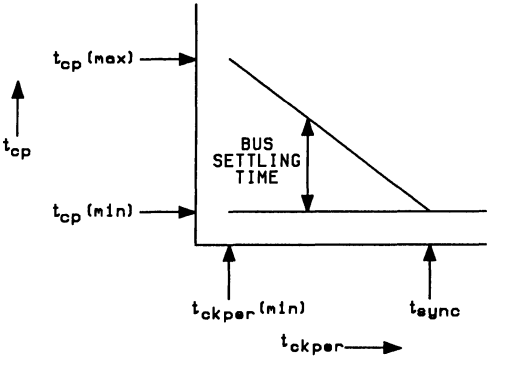


Figure 1 t_{cp} variation with t_{ckper}

Number Formats

It is only a matter of the user's convention to decide where to place the "binary point" for input and output numbers. For instance, MACCGEN treats the products

01.11 * 001.1 = 00010.101 (1.75 * 1.5 = 2.625)

and 0111 * 0011 = 00010101 (7 * 3 = 21)

exactly the same. The most common number formats used are integer and fractional notation.

Integer notation places the binary point after the LSB of both the inputs and the output, whether unsigned or two's complement. Fractional notation, on the other hand, is different for unsigned and two's complement. On inputs, unsigned fractional places the binary point before the MSB, and two's complement fractional places it after the MSB. If acc_bits is 0, unsigned fractional notation will place the binary point before the MSB of the output, and two's complement fractional places it after the output's second most significant bit. If acc_bits is greater than 0, then "acc_bits" extra significant digits are added to the left. These formats are shown in Figure 2.

Integer Unsigned Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
2^{nx-1}	2^{nx-2}		2^1	2^0

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
2^{ny-1}	2^{ny-2}		2^1	2^0

Fractional Unsigned Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
2^{-1}	2^{-2}		2^{-nx+1}	2^{-nx}

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
2^{-1}	2^{-2}		2^{-ny+1}	2^{-ny}

Integer Two's Complement Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
-2^{nx-1}	2^{nx-2}		2^1	2^0

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
-2^{ny-1}	2^{ny-2}		2^1	2^0

Fractional Two's Complement Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
-2^0	2^{-1}		2^{-nx+2}	2^{-nx+1}

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
-2^0	2^{-1}		2^{-ny+2}	2^{-ny+1}

Integer Unsigned Output (nout = nx+ny+acc_bits)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
2^{nout-1}	2^{nout-2}	2^{nout-3}		2^2	2^1	2^0

Fractional Unsigned Output (nout = nx+ny+acc_bits)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
2^{acc_bits-1}	2^{acc_bits-2}	2^{acc_bits-3}		$2^{-nx-ny+2}$	$2^{-nx-ny+1}$	2^{-nx-ny}

Integer Two's Complement Output (nout = nx+ny+acc_bits)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
-2^{nout-1}	2^{nout-2}	2^{nout-3}		2^2	2^1	2^0

Fractional Two's Complement Output (nout = nx+ny+acc_bits)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
-2^{acc_bits+1}	2^{acc_bits}	2^{acc_bits-1}		$2^{-nx-ny+4}$	$2^{-nx-ny+3}$	$2^{-nx-ny+2}$

Figure 2

Product Rounding

The extra adder input, A, provides a flexible way to do whatever product rounding you may need. If you don't need rounding, then setting the input parameter "add_in" to 0 will reduce the circuit area slightly.

Many applications do not need the full precision available from MACCGEN. In a 16x16 MAC, for instance, you may only be able to use the 16 most significant bits of the 32-bit product (assuming acc_bits = 0). To avoid a systematic bias due to truncation error, the result can be rounded by always adding a 1 at the 17th most significant bit. This is accomplished by tying pin A[15] to a logic HIGH, and tying the rest of the A bus to logic LOW. Since the rounding position and value are determined by external logic and not fixed by the MACCGEN compiler, rounding can be conditional and variable, allowing implementation of adaptive algorithms.

Two's Complement Rounding:

Rounding can be done slightly differently for two's complement numbers to get a "free" extra bit of precision. If it is noted that for all products except 10..00 x 10..00, the two most significant bits of the product are identical, then the portion of the product extracted may be right-shifted by one bit. (Assume acc_bits = 0 in the following discussion.)

In a 16x16 MAC, for example, the 16-bit product can be taken as bits 30 (MSB) through 15 (LSB), and rounding would then be done by adding a 1 at bit 14. Of course, to allow this extra bit of precision requires eliminating the value 100..00 as a valid input. In fractional two's complement notation, this corresponds to limiting the input values to the range

$$-0.1111.. \leq X,Y \leq 0.11111 \quad (-1 \text{ not allowed})$$

Multiplying −1 x −1 results in the product −1 using this method. Many standard multiplier parts (IDT IDT7216/17, Cypress CY7C516/17, etc.) include a Format Adjust to allow this mode of output.

Naming Conventions

ViGen will automatically create a default cell name for each unique MACCGEN configuration. This name is encoded in the following manner:

macxxyy u|t|s u|t|s n|a d

where:
xx = number of x bits
yy = number of y bits
u = tcx (tcy) = 0 (first x, then y)
t = tcx (tcy) = 1
s = tcx (tcy) = 2
n = add_in = 0
a = add_in = 1
d = value of acc_bits

The MACs shown in the timing examples charts are therefore named:

mac0808tta4
mac1616uun4

MULTGEN

ViGen CONFIGURABLE FUNCTION

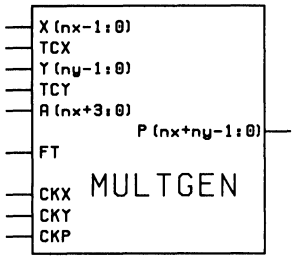
VS1500 Multiplier Generator

Features

- Variable size compiled function, with X and Y inputs independently selectable from 4 to 32 bits wide
- High performance architecture uses Booth encoding and Wallace tree partial product summation
- Two's complement, unsigned magnitude, and mixed mode multiplication
- Input number format can be pin-selectable
- Extra adder input allows implementation of $P = X \times Y + A$. This input is usually used for rounding
- X and Y inputs have separate registers and clocks
- Output is optionally registered with its own clock
- Output register can be pin-selectable

Symbol

The symbol for MULTGEN will be unique for each configuration. An example is given here only for reference.



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
nx	4 – 32 (even only)	Number of bits in the X input word
ny	4 – 32 (even, ny≤nx)	Number of bits in the Y input word
tcx	0, 1, or 2	=0: X in unsigned magnitude format =1: X in two's complement format =2: X input format selectable with an input pin (TCX)
tcy	0, 1, or 2	=0: Y in unsigned magnitude format =1: Y in two's complement format =2: Y input format selectable with an input pin (TCY)
add_in	0 or 1	Selects whether extra word A is to be added (1 = yes)
ft	0, 1 or 2	flow through: =0: output register included =1: no output register included =2: output register selectable with an input pin

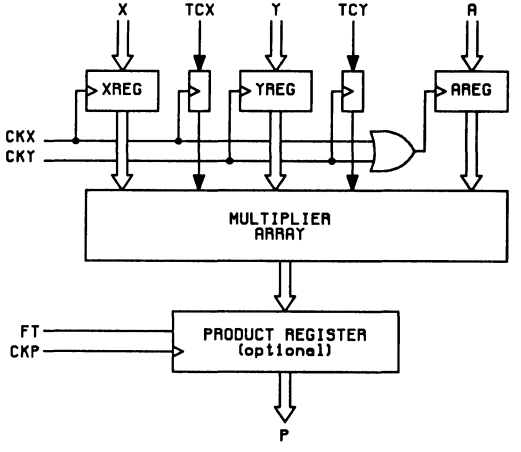
Inputs/Outputs

Pin/Bus Name (in TDL order)	Function	Req/ Opt	Cap (pF)
INPUTS:			
X[0:nx−1]	X input bus. Data on X is loaded into the X input register on the rising edge of CKX.	Req	0.164
Y[0:ny−1]	Y input bus. Data on Y is loaded into the Y input register on the rising edge of CKY.	Req	0.160
A[0:nx+3]	Optional adder input, usually used for rounding. Data on A is loaded into the A register on the rising edge of the logical OR of CKX and CKY. A is treated as a two's complement number, regardless of tcx and tcy selections. Exists if add_in=1.	Opt	0.060
CKX	X input clock, active on rising edge	Req	0.162
CKY	Y input clock, active on rising edge	Req	0.162
CKP	Clock input for the optional product register. Active on rising edge. Exists if ft=0 or ft=2.	Opt	0.110
FT	Flow−through control. When HIGH, the product register is transparent. When LOW, the product register is clocked by CKP. FT may only change when CKP is LOW. Exists if ft=2.	Opt	0.181
TCX	X input two's complement control. When HIGH, the X input is treated as a two's complement number. When LOW, X is treated as an unsigned magnitude number. Exists if tcx=2.	Opt	0.091
TCY	Y input two's complement control, similar to TCX. Exists if tcy=2.	Opt	0.100
OUTPUTS:			
P[0:nx+ny−1]	Output product bus, indicating the current contents of the product register if in clocked operation, or the product of the current x and y register contents if in flow−through mode. If clocked, P is updated after a rising CKP edge. If flow−through, P is updated after a rising CKX or CKY edge.		

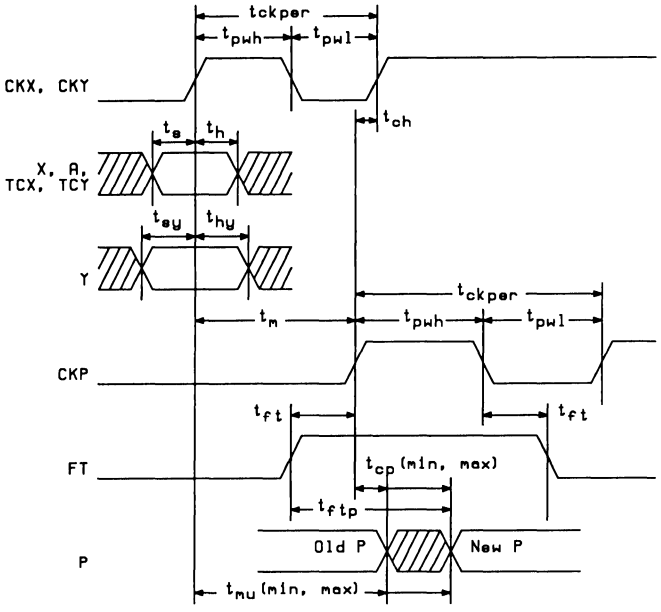
Timing Parameters

Name	Description
t_{ckper}	Minimum clock period for CKX, CKY, or CKP
t_m	Clocked multiply time (if Product Register is used)
t_{mu}	Unclocked multiply time (if Product Register isn't used). The minimum time is the hold time for the previous product, and the time between minimum and maximum is the bus settling time.
t_{cp}	Output delay time for P outputs after a rising CKP edge. The minimum time is the hold time for the previous product, and the time between minimum and maximum is the bus settling time.
t_s	Setup time for X, A, TCX, and TCY inputs before a rising CKX or CKY edge
t_h	Hold time for X, A, TCX, and TCY inputs after a rising CKX or CKY edge
t_{sy}	Setup time for Y inputs before a rising CKY edge
t_{hy}	Hold time for Y inputs after a rising CKY edge
t_{pwh}	Minimum high clock pulse width
t_{pwl}	Minimum low clock pulse width
t_{ch}	Relative hold time. CKP must rise at or before CKX or CKY to guarantee correct product output.
t_{ft}	Minimum transition margin from either CKP edge to changing FT
t_{ftp}	Maximum delay from FT rising edge to valid P output, assuming that t_{mu} is also satisfied

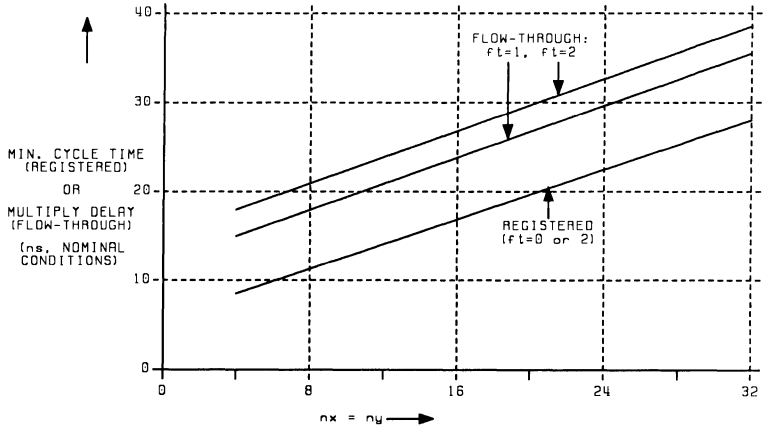
Functional Block Diagram



MULTGEN AC Waveforms



Multiplication Time for Square Multipliers (nx = ny)



(See NCR ASIC Data Book for process, voltage, and temperature derating factors.)

VIGEN COMPILED CELLS

Timing, Power, and Area Equations

1. Input parameters for the following equations are nx and ny. The validity of some equations depends on the input parameter ft. CL is the output capacitance in pF.
2. Timing parameters are specified for nominal process, V_{DD}=5.0 volts, and temperature = 25°C. See the NCR ASIC Data Book for information on derating factors for process, voltage and temperature.
3. All delays for rising and falling outputs are equal, while rise and fall times are individually specified.

PARAM	DESCRIPTION	TYPICAL VALUE (ns)
t_{ckper}	Min. clock period	t_{ckper} = 5.84 + 0.07*nx + 0.63*ny
t_m	Max. clocked multiply	t_m = 5.84 + 0.07*nx + 0.63*ny
$t_{mu(ft=1)}$	Unclocked multiply delay (flow-thru, ft=1)	$t_{mu(max)}$ = 12.08 + 0.10*nx + 0.63*ny + 0.792*CL $t_{mu(min)}$ = 7.08 + 0.792*CL
$t_{mu(ft=2)}$	Unclocked multiply delay (flow-thru, ft=2)	$t_{mu(max)}$ = 15.06 + 0.10*nx + 0.63*ny + 1.23*CL $t_{mu(min)}$ = 7.08 + 1.23*CL
t_{cp}	Output delay (clocked, ft=0 or 2) NOTE: See App. note #1	$t_{cp(max)}$ = 8.05 + 0.014*nx + 0.094*ny + 1.23*CL $t_{cp(min)}$ = 3.77 + 0.041*ny + 1.23*CL
t_s	X,A,TCX, and TCY setup	t_s = 1.30
t_h	X,A,TCX, and TCY hold	t_h = 1.3 + 0.034*nx
t_{sy}	Y setup	t_{sy} = 1.36
t_{hy}	Y hold	t_{hy} = 1.85 + 0.011*ny
t_{pwh}	Min. high clock pulse	t_{pwh} = 45% of t_{ckper}
t_{pwl}	Min. low clock pulse	t_{pwl} = 45% of t_{ckper}
t_{ch}	Relative hold time (clocked)	t_{ch} = 0
t_{ft}	FT transition margin	t_{ft} = 2.5
t_{ftp}	FT to P delay, assuming $t_{mu(max)}$ is also valid	t_{ftp} = $t_{cp(min)}$

Rise and Fall Times

ft=1:	t_r = 0.545 + 1.33*CL	ft=0 or 2:	t_r = 0.325 + 2.55*CL
	t_f = 0.506 + 1.05*CL		t_f = 0.279 + 1.99*CL

Current Requirements: I = 0.0174*ny^2 + 0.115*(nx−ny) mA/MHz
Worst case current process, V_{DD} = 5.5V, T = 25°C
Toggling 0x0 and FF..FFxFF..FF

Cell Width (mils) = 12.50 + 2.48*nx + 1.58*ny

Cell Height (mils) = 10.67 + 5.33*ny + 2.60*add_in + offset1 + offset2

where: offset1 = 0 if tcy=1
offset1 = 10.67 if tcy=0 or 2
offset2 = 0 if ft=1
offset2 = 6.97 if ft=0 or 2

Timing Examples

8 x 8 two's complement multiplier with rounding, product register

(mul0808ttar: nx = 8, ny = 8, tcx = 1, tcy = 1, add_in = 1, ft = 0)

Symbol	8 x 8 Multiplier	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ckper}	Minimum clock period	11.44		21.1		22.0		24.7		ns
t_m	Maximum clocked multiply		11.44		21.1		22.0		24.7	ns
t_{cp}	Output delay from CKP	5.24	9.10	9.7	16.8	10.1	17.5	11.3	19.7	ns
t_s	Minimum setup time for X, A inputs	1.30		2.4		2.5		2.8		ns
t_h	Minimum hold time for X, A inputs	1.57		2.9		3.0		3.4		ns
t_{sy}	Minimum setup time for Y inputs	1.36		2.5		2.6		2.9		ns
t_{hy}	Minimum hold time for Y inputs	1.94		3.6		3.7		4.2		ns
t_{pwh}	Minimum high clock pulse	5.15		9.5		9.9		11.1		ns
t_{pwl}	Minimum low clock pulse	5.15		9.5		9.9		11.1		ns
t_{ch}	Relative hold time	0		0		0		0		ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.15pF)

16 x 16 unsigned multiplier with no rounding, flow–through

(mul1616uunf: nx = 16, ny = 16, tcx = 0, tcy = 0, add_in = 0, ft = 1)

Symbol	16 x 16 Multiplier	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ckper}	Minimum clock period	17.04		31.4		32.8		36.8		ns
t_{mu}	Maximum unclocked multiply	7.20	23.88	13.3	44.1	13.9	46.0	15.5	51.6	ns
t_s	Minimum setup time for X inputs	1.30		2.4		2.5		2.8		ns
t_h	Minimum hold time for X inputs	1.84		3.4		3.6		4.0		ns
t_{sy}	Minimum setup time for Y inputs	1.36		2.5		2.6		2.9		ns
t_{hy}	Minimum hold time for Y inputs	2.03		3.7		3.9		4.4		ns
t_{pwh}	Minimum high clock pulse	7.67		14.1		14.8		16.6		ns
t_{pwl}	Minimum low clock pulse	7.67		14.1		14.8		16.6		ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.15pF)

Application Notes

Output Delay Calculations for Product Registers

This applications note applies only to those multipliers that have product registers, i.e., ft=0 or ft=2. If the flow-through parameter, ft, is equal to 2, then this note only applies when in registered mode (pin FT is LOW).

Due to the way that the product register is implemented within MULTGEN, the delay from CKP to P is actually dependent on the multiply cycle time. The delay, t_{cp}, is calculated with both a minimum and a maximum value. The minimum value of t_{cp} is the output hold time for the previous product P. Data on the P output bus will not change before t_{cp}(min). The maximum value of t_{cp}, as calculated, only applies when the multiplier is being run at maximum frequency (minimum rising CKX/CKY to rising CKP). If the multiplier is being run slower, then t_{cp}(max) actually gets less, as shown in Figure 1.

Above a certain multiplication period, referred to in Figure 1 as t_{sync}, t_{cp}(max) will have the same value as t_{cp}(min). In other words, all of the bits in the P bus will switch simultaneously. For multiplication periods between t_{ckper}(min) and t_{sync}, t_{cp}(max) derates linearly as shown.

The period t_{sync} is defined as:

$$t_{sync} = t_{ckper}\ (min) + 1.2^{*}\ (\ t_{cp}(max) - t_{cp}(min)\ )$$

where t_{ckper}, t_{cp}(max), and t_{cp}(min) are all as defined in the parametric equations.

Although the t_{cp}(min) and t_{cp}(max) parameters for each output pin will be slightly different due to differing output capacitive loads, for simplicity the simulation model will assign the shortest t_{cp}(min) and the longest t_{cp}(max) values to the entire P bus. This effect will be minor in most situations.

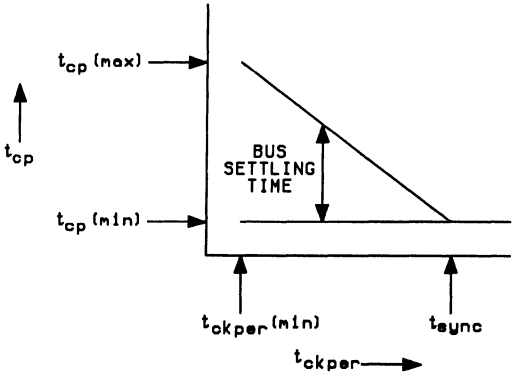


Figure 1 t_{cp} variation with t_{ckper}

Number Formats

It is only a matter of the user's convention to decide where to place the "binary point" for input and output numbers. For instance, MULTGEN treats the products

01.11 * 001.1 = 00010.101 (1.75 * 1.5 = 2.625)

and 0111 * 0011 = 00010101 (7 * 3 = 21)

exactly the same. The most common number formats used are integer and fractional notation.

Integer notation places the binary point after the LSB of both the inputs and the output, whether unsigned or two's complement. Fractional notation, on the other hand, is different for unsigned and two's complement. Unsigned fractional places the binary point before the MSB, and two's complement fractional places it after the MSB for the inputs and after the second most significant bit for the output. These formats are shown in Figure 2.

Integer Unsigned Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
2^{nx-1}	2^{nx-2}		2^1	2^0

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
2^{ny-1}	2^{ny-2}		2^1	2^0

Fractional Unsigned Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
2^{-1}	2^{-2}		2^{-nx+1}	2^{-nx}

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
2^{-1}	2^{-2}		2^{-ny+1}	2^{-ny}

Integer Two's Complement Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
-2^{nx-1}	2^{nx-2}		2^1	2^0

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
-2^{ny-1}	2^{ny-2}		2^1	2^0

Fractional Two's Complement Inputs

X[nx−1]	X[nx−2]	...	X[1]	X[0]
-2^0	2^{-1}		2^{-nx+2}	2^{-nx+1}

Y[ny−1]	Y[ny−2]	...	Y[1]	Y[0]
-2^0	2^{-1}		2^{-ny+2}	2^{-ny+1}

Integer Unsigned Output (nout = nx+ny)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
2^{nout-1}	2^{nout-2}	2^{nout-3}		2^2	2^1	2^0

Fractional Unsigned Output (nout = nx+ny)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
2^{-1}	2^{-2}	2^{-3}		$2^{-nout+2}$	$2^{-nout+1}$	2^{-nout}

Integer Two's Complement Output (nout = nx+ny)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
-2^{nout-1}	2^{nout-2}	2^{nout-3}		2^2	2^1	2^0

Fractional Two's Complement Output (nout = nx+ny)

P[nout−1]	P[nout−2]	P[nout−3]	...	P[2]	P[1]	P[0]
-2^1	2^0	2^{-1}		$2^{-nout+4}$	$2^{-nout+3}$	$2^{-nout+2}$

Figure 2

Product Rounding

The extra adder input, A, provides a flexible way to do whatever product rounding you may need. If you don't need rounding, then setting the input parameter "add_in" to 0 will reduce the circuit area slightly.

Many applications do not need the full precision available from MULTGEN. In a 16x16 multiplier, for instance, you may only be able to use the 16 most significant bits of the 32-bit product. To avoid a systematic bias due to truncation error, the result can be rounded by always adding a 1 at the 17th most significant bit. This is accomplished by tying pin A[15] to a logic HIGH, and tying the rest of the A bus to logic LOW. Since the rounding position and value are determined by external logic and not fixed by the MULTGEN compiler, rounding can be conditional and variable, allowing implementation of adaptive algorithms.

Two's Complement Rounding:

Rounding can be done slightly differently for two's complement numbers to get a "free" extra bit of precision. If it is noted that for all products except 10..00 x 10..00, the two most significant bits of the product are identical, then the portion of the product extracted may be right-shifted by one bit.

In the 16x16 multiplier, for example, the 16-bit product can be taken as bits 30 (MSB) through 15 (LSB), and rounding would then be done by adding a 1 at bit 14. Of course, to allow this extra bit of precision requires eliminating the value 100..00 as a valid input. In fractional two's complement notation, this corresponds to limiting the input values to the range

$$-0.1111.. \leq X,Y \leq 0.11111 \quad (-1 \text{ not allowed})$$

Multiplying −1 x −1 results in the product −1 using this method. Many standard multiplier parts (IDT IDT7216/17, Cypress CY7C516/17, etc.) include a Format Adjust to allow this mode of output.

Naming Conventions

ViGen will automatically create a default cell name for each unique MULTGEN configuration. This name is encoded in the following manner:

mulxxyy u|t|s u|t|s n|a r|f|s

where:
xx = number x bits
yy = number y bits
u = tcx (tcy) = 0 (first x, then y)
t = tcx (tcy) = 1
s = tcx (tcy) = 2
n = add_in = 0
a = add_in = 1
r = ft = 0
f = ft = 1
s = ft = 2 (in the last character position)

The multipliers shown in the timing examples charts are therefore named:

mul0808ttar
mul1616uunf

RAMGEN

ViGen CONFIGURABLE FUNCTION

VS1500 RAM Generator

Features

- Modular RAM allows variable configurations up to 32K bits.
- Pseudo static for reduced complexity and operating power (0 DC power)
- Enable input is taken low between each read and write access. This feature is applicable for clocked operation.
- Tristate and always-driving outputs

Description

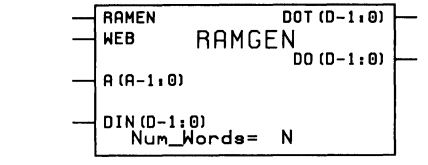
The RAM generator produces a low power pseudo static RAM. On reads, the RAM enable input (RAMEN) is taken low in order to precharge internal states. When RAMEN input is taken high, the sense amp quickly discharges outputs when reading a logic low. On writes, RAMEN is initially taken low in order to allow address inputs to change. Data from the data input bus is written while RAMEN is high. Many internal states are only precharged to $V_{DD} - V_{threshold}$ in order to reduce power ($=CV^2F$) and decrease read discharge time. To further reduce ac power dissipation when the RAM is disabled, all inputs are internally gated by RAMEN. By externally tying a tristatable output to a data input, a bidirectional I/O line can be obtained.

Symbol

The symbol for RAMGEN will be unique for each configuration. An example is given here only for reference.

Data_Width = Word_Width

Address_Width = $\lceil \log_2(\text{Num\_Words}) \rceil$



Input Parameter Ranges

Input Parameter	Allowed Range	Explanation
Num_Words	8 - 2048 (even only)	Number of words in RAM array
Word_Width	Any integer ≤ 32	Number of bits in a word
	8 $\leq$ bits $\leq$ 32768	Number of bits = Num_Words x Word_Width

Inputs/Outputs

Pin/Bus Name (in TDL order)	Function	Cap (pF)
INPUTS:		
RAMEN	RAM enable is active high. Internal states are precharged when RAMEN is low. Reads and writes are enabled when RAMEN is high.	0.377
WEB	Read/Write select: active high for read, active low for write.	0.254
A[0:k−1]	Address input bus of width k ($k = \lceil \log_2 Num\_Words \rceil$). Addresses may only change while RAMEN is low.	0.093
DIN[0:Word_Width−1]	Data input bus.	0.302
OUTPUTS:		
DO[0:Word_Width−1]	Data output bus, driven by RAM (on read) and DIN (on write). Goes high on low RAMEN input.	
DOT[0:Word_Width−1]	Tristate data output bus is driven when WEB and RAMEN inputs are high. Otherwise DOT is at high impedance.	0.190

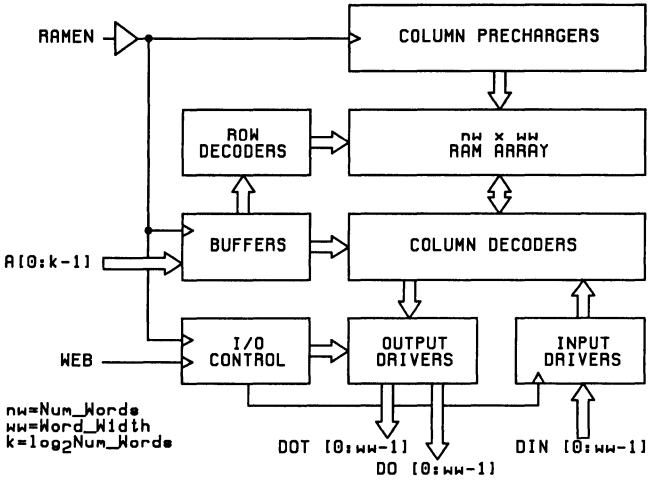
Timing Parameters

Name	Description
t_{asu}	Minimum address/WEB setup time before RAMEN rises (Read, Write)
t_{ah}	Minimum address/WEB hold time after RAMEN falls (Read, Write)
t_{enl}	Minimum RAMEN low pulse width (Read, Write)
t_{enh}	Minimum RAMEN high pulse width (Read, Write)
t_{acc}	Maximum delay from rising RAMEN to valid output data on DO (Read)
t_{dh}	Minimum delay from falling RAMEN during which DO data remains valid (Read, Write)
t_{acct}	Maximum delay from rising RAMEN to valid output data on DOT (Read)
t_{dht}	Minimum delay from falling RAMEN until DOT outputs at high impedance (Read)
t_{dsu}	Minimum input data (DIN) setup time before RAMEN falls (Write)
t_{wdh}	Minimum input data (DIN) hold time after RAMEN falls (Write)
t_{dido}	Maximum delay from data in to data out while RAMEN high (Write)
t_r	Maximum output rise time on DO
t_f	Maximum output fall time on DO
t_{rt}	Maximum output rise time on DOT (Read)
t_{ft}	Maximum output fall time on DOT (Read)

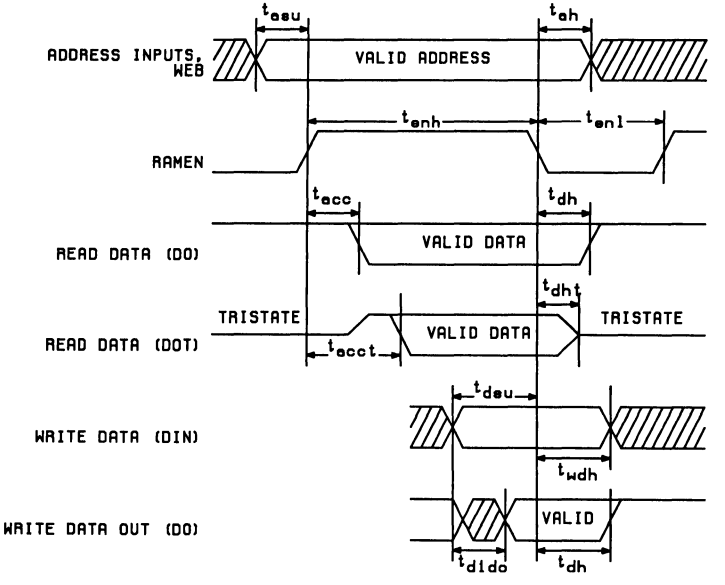
RAMGEN

ViGen CONFIGURABLE FUNCTION

Functional Block Diagram



RAMGEN AC Waveforms



Timing, Power, and Area Equations

Equations are given in terms of several variables which describe a RAM's characteristics. To solve the timing, power, and area equations given below, first determine RAM variables by following these steps:

1. Num_Words and Word_Width are generator input parameters.
2. CL is output capacitance in pF.
3. col_dec = internal column decode. Possible values for col_dec are 4, 8, and 16. RAMGEN chooses smallest col_dec which is $\geq \sqrt{\text{Num\_Words} / \text{Word\_Width}}$. If $\sqrt{\text{Num\_Words} / \text{Word\_Width}} > 8$, use col_dec = 16.
4. Num_Words is internally rounded up to the nearest multiple of 2*col_dec.
5. rows = internal array rows = Num_Words / col_dec.
6. cols = internal array columns = Word_Width*col_dec.
7. Lr = $\lceil \log_2 \text{rows} \rceil$. (ceiling function: round up to nearest integer)

All times are in nanoseconds and are NOMINAL (V_{DD} = 5.0 volts, T = 25°C, Nom. process). See the NCR ASIC Data Book for process, voltage, and temperature derating.

PARAM	DESCRIPTION	TYPICAL VALUE (ns)
t_{asu}	Address/WEB setup	= 0
t_{ah}	Address/WEB hold	= 0.74 + 0.110*Lr + 0.020*Word_Width
t_{enl}**	RAMEN low pulse width	= 4.58 − 0.100*Lr + 0.010*cols + 0.090*rows
t_{enh}*	RAMEN high pulse width	= t_{acc}
t_{acc}*	DO access	= 5.72 − 0.300*Lr + 0.020*cols + 0.076*rows +0.232*CL
t_{dh}	DO hold	= 2.25 + 0.214*Lr + 0.104*Word_Width + 0.390*CL
t_{acct}*	DOT access	= 5.73 − 0.295*Lr + 0.021*cols + 0.076*rows + 0.605*CL
t_{dht}	DOT hold	= 1.25 + 0.119*Word_Width
t_{dsu}*	Write data setup	= 2.68 + 0.026*rows
t_{wdh}	Write data hold	= 0.67 + 0.065*Lr + 0.098*Word_Width
t_{dido}	Data in to data out	= 5.62 + 0.020*cols + 0.067*rows + 0.452*CL
t_r	DO rise	= 0.58 + 0.840*CL
t_f	DO fall	= 0.57 + 0.900*CL
t_{rt}	DOT rise	= 0.77 + 2.230*CL
t_{ft}	DOT fall	= 0.49 + 0.930*CL

* If col_dec equals 4, then 0.5 ns can be subtracted from t_{enh}, t_{acc}, t_{acct}, and t_{dsu}.
** t_{enl} equals maximum of t_{enl} and t_{dh}.

Current Requirements: I = 4.54*rows + 6.32*cols + .0281*rows*cols (μA/MHz)
Worst case current process, V_{DD} = 5.5V, T = 25°C

Cell Height Estimate (mils) = 10.6 + 1.22*rows

Cell Width Estimate (mils) = 6.29 + offset + 0.826*cols

if 04 ≤cols < 40	use offset = 2.50
if 40 ≤cols < 80	use offset = 3.53
if 80 ≤cols ≤256	use offset = 4.87

Timing Examples

512 x 8 RAM: col_dec = 8, rows = 64, cols = 64, Lr = 6

Symbol	512 x 8 RAM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{asu}	Address/WEB set-up	0		0		0		0		ns
t_{ah}	Address/WEB hold	1.56		2.92		3.04		3.40		ns
t_{enl}	RAMEN low pulse width	10.38		19.41		20.24		22.63		ns
t_{enh}	RAMEN high pulse width	10.10		18.88		19.69		22.02		ns
t_{acc}	DO access		10.10		18.88		19.69		22.02	ns
t_{dh}	DO hold	4.42		8.27		8.63		9.65		ns
t_{acct}	DOT access		10.26		19.18		20.00		22.36	ns
t_{dht}	DOT hold	2.20		4.12		4.29		4.80		ns
t_{dsu}	Write data set-up	4.34		8.12		8.47		9.47		ns
t_{wdh}	Write data hold	1.84		3.45		3.60		4.02		ns
t_{dido}	Data in to data out		11.26		21.05		21.95		24.54	ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.15pF)

64 x 4 RAM: col_dec = 4, rows = 16, cols = 16, Lr = 4

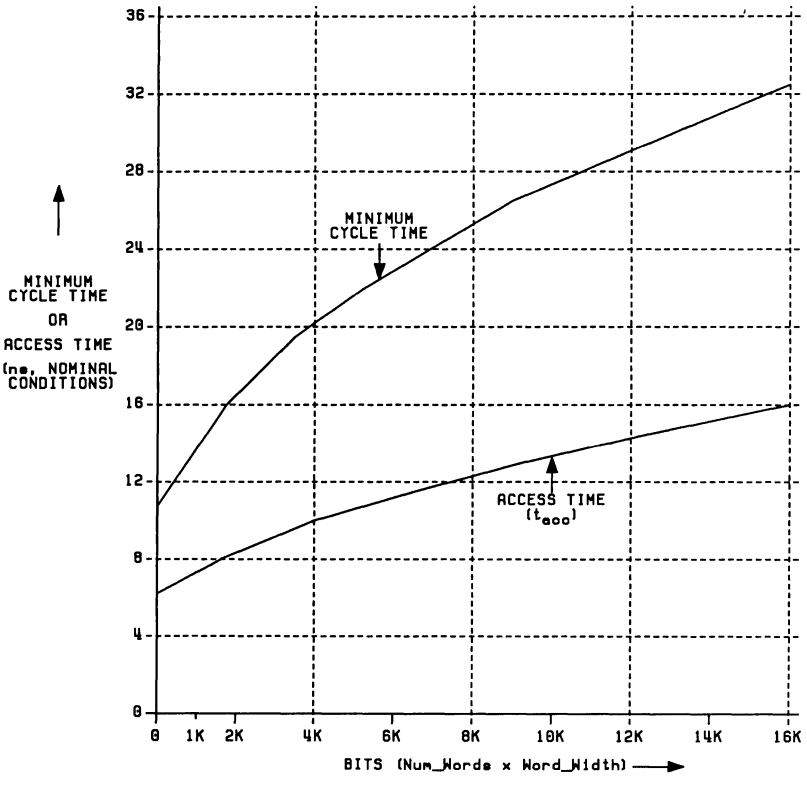
Symbol	64 x 4 RAM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{asu}	Address/WEB set-up	0		0		0		0		ns
t_{ah}	Address/WEB hold	1.26		2.36		2.46		2.75		ns
t_{enl}	RAMEN low pulse width	5.78		10.81		11.27		12.60		ns
t_{enh}*	RAMEN high pulse width	5.59		10.45		10.90		12.19		ns
t_{acc}*	DO access		5.59		10.45		10.90		12.19	ns
t_{dh}	DO hold	3.58		6.70		6.98		7.81		ns
t_{acct}*	DOT access		5.69		10.65		11.10		12.41	ns
t_{dht}	DOT hold	1.73		3.23		3.37		3.76		ns
t_{dsu}*	Write data set-up	2.60		4.85		5.06		5.66		ns
t_{wdh}	Write data hold	1.32		2.47		2.58		2.88		ns
t_{dido}	Data in to data out		7.08		13.24		13.81		15.43	ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.15pF)

*Since col_dec equals 4, 0.5 ns (Nominal) was subtracted from t_{enh}, t_{acc}, t_{acct}, and t_{dsu}.

Access and Cycle Time for square arrays (rows = columns)

Graph slightly overestimates for array columns > rows.
Cycle time = $t_{enl} + t_{enh}$



(See NCR ASIC Data Book for process, voltage, and temperature derating factors.)

Application Notes

Designing for Testability

Test programs for ASIC components must be able to verify that all circuit elements in the design are functioning properly. This includes verifying the functional correctness of the design and detecting faults caused by manufacturing defects. There are many methods to improve the testability of a component, all of which involve trade–offs in the amount of extra logic required, the resulting test time, and the degree of test coverage. A highly recommended method for the RAM is to multiplex the address, control, and data lines to the external part pins during a test mode. This allows direct control and observability of the RAM during test. In pin limited situations, the use of scan registers to shift in the address and data and to shift out the output may be desired.

To adequately test the RAM, the following conditions and patterns should be considered:

- Tying address and data input lines together while writing provides an excellent test of every data value. Verify by comparing each address with address content. This pattern will catch faults in the address decode. Repeat test with address complements written through data inputs. This ensures that logic one and zero are written to every bit and verified. Preferably, all bits should be written first and then read.
- The data output should change frequently between consecutive reads. The above pattern or a "checkerboard" pattern is a good example of this.
- Operate RAM at near maximum frequency to verify that sense amps and other critical timing circuitry are working properly.
- During reads to verify bit contents, set data inputs to a value other than the value being read (such as all 0/1). This verifies that outputs are not being driven by inputs during reads.
- Verify tristate control by reading through tristate outputs.

Column address inputs are the least significant bits of the address. If the RAM is operated as specified, then the critical race conditions which can cause write or read disturb problems will not exist in this design.

Output Drive

The data outputs (DO) have high output drives (approximately equal to the drive of an HBUF). Through the tristate outputs (DOT), the drive is about half the data output drive (slightly less than the drive of a TBUFP).

Naming Conventions

ViGen will automatically create a default cell name for each unique RAMGEN configuration. This name is encoded in the following manner:

rawwwwbb

where:
wwww = number of words
bb = word width

Therefore, the default names for the two example RAMs would be:

ra051208
ra006404

ROMGEN

ViGen CONFIGURABLE FUNCTION

VS1500 ROM Generator

Features

- Compiled ROM cell allows flexible configurations of up to 256K bits
- Maximum word width of 128 bits
- Maximum number of words is 16K
- Clocked operation suitable for microprocessor applications
- Pseudo-static design for low power consumption

Description

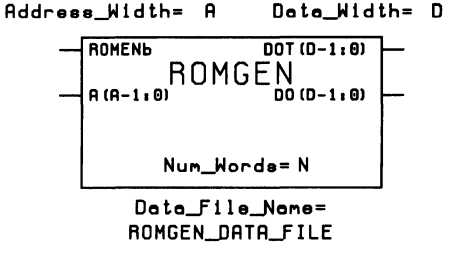
ROMGEN produces a compiled ROM cell which is pseudo-static for reduced power consumption, but delivers short access times. The enable input (ROMENb) must be taken high before each access, making the ROM suitable for clocked operation. The ROM is precharged while ROMENb is high, with the internal states pulled up to $V_{DD} - V_{th}$ to reduce power consumption and cycle times. Also, all inputs are gated off while the ROM is inactive to reduce AC power dissipation. Data is read from the ROM while ROMENb is low, with both tristatable and constantly-driving outputs available.

Symbol

The symbol for ROMGEN will be unique for each configuration. An example is given here only for reference.

Data_Width = Word_Width

Address_Width = $\lceil \log_2(\text{Num\_Words}) \rceil$



Input Paramter Ranges

Input Parameter	Allowed Range	Explanation
Word_Width	1 – 128	Word size in bits[1]
Num_Words	128 – 16,384 (multiple of 128)[2]	Number of words in the ROM[1]
fname	ASCII alpha-numeric string	ROM data file name

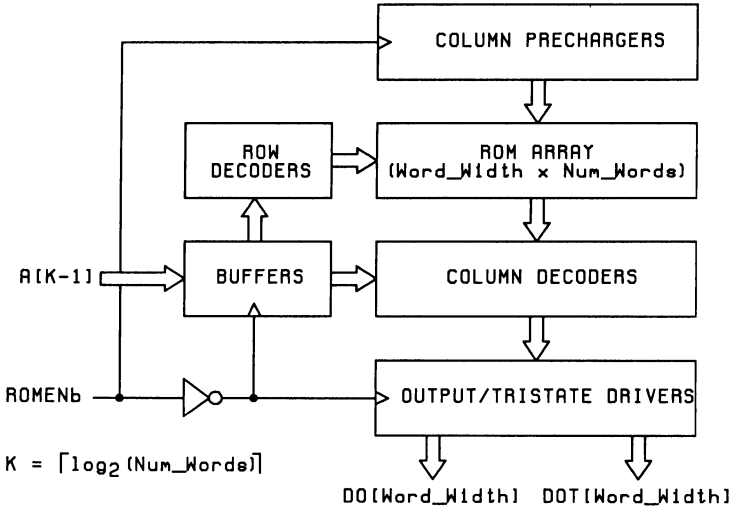
1 Total number of ROM bits (Word_Width × Num_Words) must be ≤256K.

2 Num_Words is internally rounded up to a multiple of 32 times the column decode factor. The column decode is selected to be 4, 8, 16, or 32 by ROMGEN to optimize area and performance.

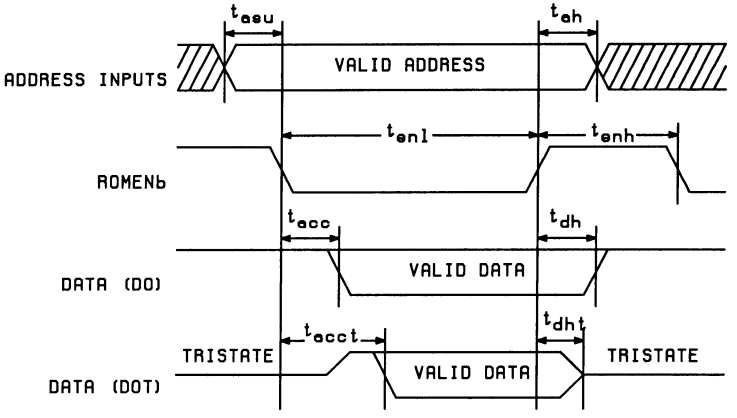
Inputs/Outputs

Pin/Bus Name (in TDL order)	Function	Cap (pF)
INPUTS:		
ROMENb	ROM enable is active low. Internal states are precharged when ROMENb is high.	0.65
A[K]	Address input bus of width K (K = $\lceil \log_2 (\text{Num\_Words}) \rceil$). Addresses may change only while ROMENb is high.	0.28
OUTPUTS:		
DO[Word_Width]	Data output bus. Goes high while ROMENb is high.	
DOT[Word_Width]	Tristate data output bus. DOT is at high impedance while ROMENb is high.	0.19

Functional Block Diagram



ROMGEN AC Waveforms



Timing Parameters

Name	Description
t_{acc}	Maximum delay from ROMENb active low to valid data on DO
t_{acct}	Maximum delay from ROMENb active low to valid output data on DOT
t_{enl}	Minimum ROMENb low pulse width
t_{enh}	Minimum ROMENb high pulse width
t_{asu}	Minimum address setup time before ROMENb goes active low
t_{ah}	Minimum address hold time after ROMENb goes inactive high
t_{dh}	Minimum delay from ROMENb inactive high during which DO data remains valid
t_{dht}	Minimum delay from ROMENb inactive high until DOT goes to high impedance

Timing, Current, and Size Equations

Equations are given in terms of generator parameters and derived variables. These can be found by following these steps:

1. CL is the output capacitance in pF.
2. Generator input parameters are Num_Words, Word_Width. Num_Words must be rounded up to a multiple of 128.
3. Calculate first-pass values for internal variables:
   Rows = SQRT(Num_Words×Word_Width), rounded up to a multiple of 32.
   Cols = (Num_Words×Word_Width) / Rows.
4. Assume that Col_dec = Cols / Word_Width. Then round up to the nearest valid column decode factor of 4, 8, 16, or 32.
5. Num_Words must be rounded up to a multiple of (32×Col_dec).
6. To get the final values:
   Cols = Col_dec×Word_Width
   Rows = Num_Words / Col_dec
   Num_Words = Rows×Col_dec
7. Lr = $\log_2$ (Rows) , Lc = $\log_2$ (Cols).

All times are NOMINAL (V_{DD} = 5.0 volts, T = 25° C, Nominal process). See the *NCR ASIC VS700 Data Book* for process, voltage, and temperature derating factors. I_{DD} is specified at V_{DD} = 5.5V, T = 25+ C, and worst case current process.

PARAM	DESCRIPTION	UNITS	TYPICAL VALUE (ns)
t_{acc}	DO access time	ns	= 12.916 + 0.098×Rows + 0.021×Cols + 0.084×Col_dec − 1.171×Lr − 0.247×Lc + 0.603×CL
t_{acct}	DOT access time	ns	= 12.956 + 0.098×Rows + 0.021×Cols + 0.084×Col_dec − 1.171×Lr − 0.247×Lc + 0.528×CL
t_{enl}	ROMENb low pulse width	ns	= 12.916 + 0.098×Rows + 0.021×Cols + 0.084×Col_dec − 1.171×Lr − 0.247×Lc + 0.603×CL
t_{enh}	ROMENb high pulse width	ns	= 11.711 + 0.063×Word_Width + 0.070×Rows + 0.018×Cols + 0.093×Col_dec − 1.980×Lr − 0.043×Lc + 1.018×CL
t_{asu}	Address setup	ns	= 0.000
t_{ah}	Address hold	ns	= 1.165
t_{dh}	DO hold time	ns	= 3.155 + 0.003×Word_Width+ 0.003×Rows + 0.017×Cols + 0.056×Col_dec + 0.111×Lr + 0.108×Lc + 1.018×CL
t_{dht}	DOT hold time	ns	= 0.943 + 0.066×Word_Width + 0.005×Rows + 0.010×Lr + 0.035×Lc + 1.275×CL
I_{DD}	Average current	µA/ MHz	= 254.939 + 4.321×Word_Width + 1.620×Rows + 1.620×Cols + 12.963×Lc
Width	Layout width	mils	= 19.675 + 0.027×Rows + 0.295×Cols − 0.684×Lr − 0.045×Lc
Height	Layout height	mils	= 11.914 + 0.054×Word_Width + 0.249×Rows + 0.041×Col_dec + 0.654×Lr − 0.162×Lc

Timing Constants: k = 1.40ns, M_{CLU} = M_{CHL} = 0.20

Timing Examples

1024 × 8 ROM: Rows = 64, Cols = 128, Col_dec = 16, Lr = 6, Lc = 7

Symbol	1024 × 8 ROM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	DO access		14.77		27.81		29.00		32.57	ns
t_{acct}	DOT access		14.77		27.81		29.00		32.57	ns
t_{dh}	DO hold	8.37		15.87		16.56		18.61		ns
t_{dht}	DOT hold	2.73		5.35		5.58		6.30		ns
t_{enh}	ROMENb high pulse width	8.82		16.70		17.42		19.58		ns
t_{enl}	ROMENb low pulse width	14.77		27.81		29.00		32.57		ns
t_{asu}	Address setup	0.00		0.00		0.00		0.00		ns
t_{ah}	Address hold	1.16		2.17		2.27		2.54		ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.1pF)

I_{avg} (ac) = 691 µA/MHz
Cell Width = 54.74 mils
Cell Height = 31.73 mils
Cell Area = 1736.9 $mils^2$

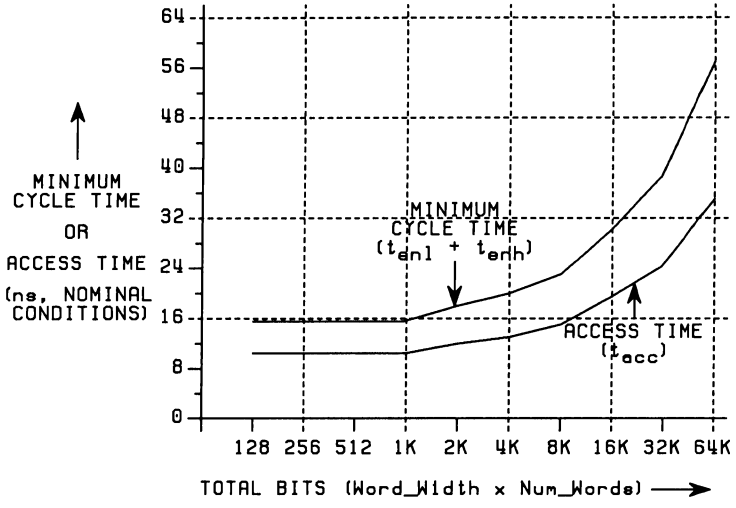
8192 × 8 ROM: Rows = 256, Cols = 256, Col_dec = 32, Lr = 8, Lc = 8

Symbol	8192 × 8 ROM	Nominal V_{DD} = 5V		Worst Case V_{DD} = 4.5V						Units
		TA = 25°C		TA = 70°C		TA = 85°C		TA = 125°C		
	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t_{acc}	DO access		35.03		65.63		68.42		76.80	ns
t_{acct}	DOT access		35.03		65.63		68.42		76.80	ns
t_{dh}	DO hold	12.35		23.30		24.30		27.30		ns
t_{dht}	DOT hold	3.75		7.24		7.56		8.51		ns
t_{enh}	ROMENb high pulse width	22.04		41.39		43.16		48.46		ns
t_{enl}	ROMENb low pulse width	35.03		65.63		68.42		76.80		ns
t_{asu}	Address setup	0.00		0.00		0.00		0.00		ns
t_{ah}	Address hold	1.16		2.17		2.27		2.54		ns

Switching characteristics (Input t_r, t_f = 1.4ns, CL = 0.1pF)

I_{avg} (ac) = 1223 µA/MHz
Cell Width = 96.27 mils
Cell Height = 81.34 mils
Cell Area = 7831 $mils^2$

Access and Cycle Time for Word_Width ≤ 8



NCR VS700 ASIC Data Book gives voltage and temperature derating factors.

Application Notes

Data File Format

The data file which is used to build ROMGEN is the same data file which is used during simulation of the ROM. For the exact data file format, refer to your workstation User's Guide.

Padding ROM Data

In certain cases, the actual size of the data for the ROM may be smaller than the size of the configured ROM. In this case, the data file must be padded to be the same size as the ROM. Normally, the data file is padded with words made up of zeros or ones. In situations where the padding data is unimportant, it is recommended that the data file be padded with all-ones words. This will help to limit power dissipation of the ROM.

Designing for Testability

Testability for ASIC parts requires that each of the individual ASIC components be testable, including verification of functional operation, as well as detection of faults introduced in the manufacturing process. The degree to which an individual component in an ASIC design can be effectively tested depends largely on the degree to which that component can be isolated from the rest of the chip. It is highly recommended that the address lines, enable line, and data outputs of the ROM be multiplexed so that the tester (or other external board logic) has direct control and observability of the ROM in the test mode. There is, of course, a trade-off made with respect to speed and area when adding the additional logic required for multiplexing. Other alternatives for testing the ROM include:

- A parity bit can be added to the ROM, and a simple parity checker connected to the outputs of the ROM. The address lines to the ROM could still be multiplexed for the tester to use, while only the result of the parity checker would need to be output to the tester. The parity checker can continue to monitor the ROM during the run mode.
- An alternate scheme which still uses the parity bit and checker would also use a counter connected to the address inputs to count through all of the addresses in test mode. This type of design would be preferable for implementing a BIST (Built-In Self-Test) style architecture.
- Instead of using a parity bit in the ROM, which adds to the size of the ROM required, a signature analyzer could be placed at the output of the ROM. This would require approximately (Word_Width + 4) linear feedback shift registers (LFSR) to be placed at the data outputs (one on each output, plus at least four extras). The address inputs could be generated either by a counter or by a second LFSR string, and the final signature could either be compared on chip, or fed off chip to the tester. This method gives much better coverage of the ROM than does the parity checker method and in a more random fashion, and is an excellent BIST option. The drawback with the signature analysis method is that it cannot be used by the ROM in the run mode.

Some things which should be considered when actually doing the testing on the ROM would include:

- The ROM should be operated at or near the maximum frequency it will set in the application to verify that other critical timing circuitry is operating correctly.
- Verify tristate control by reading through the tristates (if they are used in the design).

In addition to these suggestions, it is recommended that the design guidelines found in the Application Notes section of the NCR ASIC Data Book be strictly followed.

Output Drive

The data outputs (DO) have high output drives approximately equal to the drive of an HBUF cell. The output drive for the tristate outputs (DOT) is about half that of the data outputs (about the same as a TBUFP cell).

Naming Conventions

ViGen will automatically create a default name for each ROMGEN configuration, with the configuration information encoded in the following manner:

rowwwwwbbbdf	where: wwwww = number of words bbb = word width df = data file designater (from a to zz)

The default names for the two example ROMs would be:

ro01024008aa
ro08192008aa

This default naming convention may not, however, produce unique cell names for two ROMs with the same configuration but with different data files (i.e., the ROMs contain different code). It is left to the user to over-ride the default names, when necessary, to ensure unique names for all ROM cells within a design. When doing this, it is recommended that the configuration parameters be included with the name, as is shown above, along with some unique tag to identify a ROM cell with its data file. When doing this, be sure to follow the cell naming requirements for your workstation, as covered in your User's Guide.

SRAM m x n

ViGen CONFIGURABLE FUNCTION

VS1500 High Speed SRAM

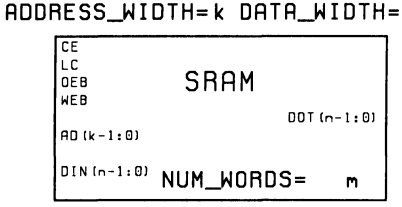
Description

- Modular SRAM allows flexible organization
- Array sizes from 16 to 1024 words of 1 to 16 bits
- Access and Cycle times from 11ns to 22ns, nominal conditions
- Asynchronous operation – requires no clock
- Low power dissipation when unselected

Inputs: CE, LC, OEB, WEB, AD(k), DIN(n)
Outputs: DOT(n)

Symbol

The symbol for SRAM will be unique for each configuration. An example is shown here only for reference.



This SRAM supercell complements the clocked RAM in the standard cell library by offering higher speed at the expense of greater power dissipation. Independent input control lines provide cell enable, output data latching, and output tristate capability.

Input Parameter Ranges

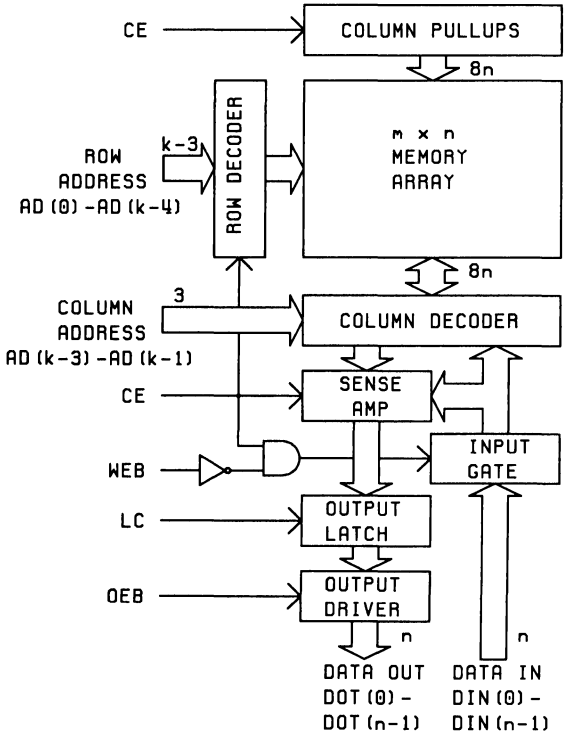
INPUT PARAMETER	ALLOWED RANGE	EXPLANATION
Num_Words	16 – 1024 multiple of 16	The memory array is organized as "m" words of "n" bits each
Word_Width	1 – 16	

Inputs/Outputs

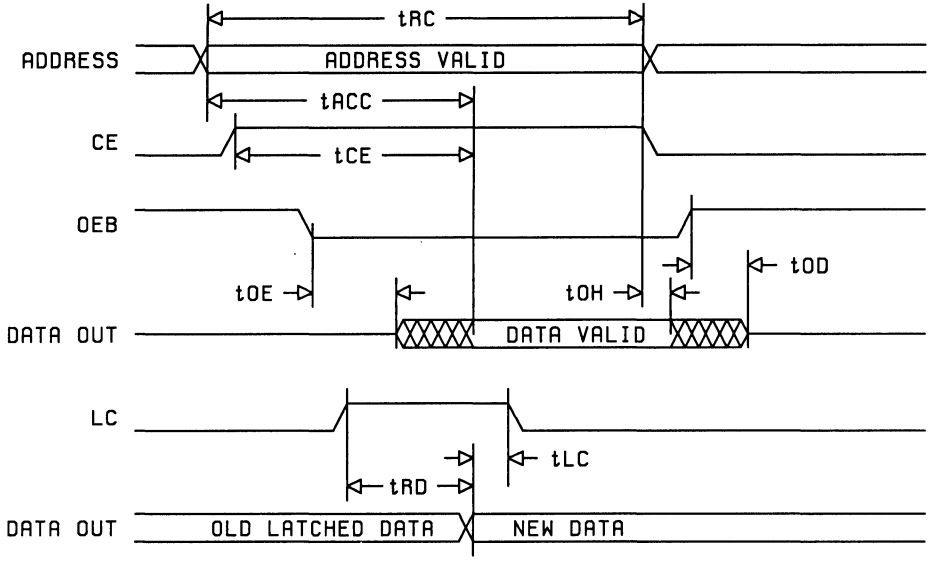
PIN NAME	FUNCTION	CAP (pF)
INPUTS:		
CE	Cell Enable	1.14
LC	Latch Control	1.44*
OEB	Output Enable Bar	0.34
WEB	Write Enable Bar	0.23
AD (k)	Address Bus	0.46
DIN (n)	Data Input Bus	0.24
OUTPUTS:		
DOT (n)	Data Output Bus	0.10

* The capacitance for LC varies with word width.
The value given is for a 16-bit wide word.
C = 0.32 + 0.07*n

Functional Block Diagram



Read Cycle

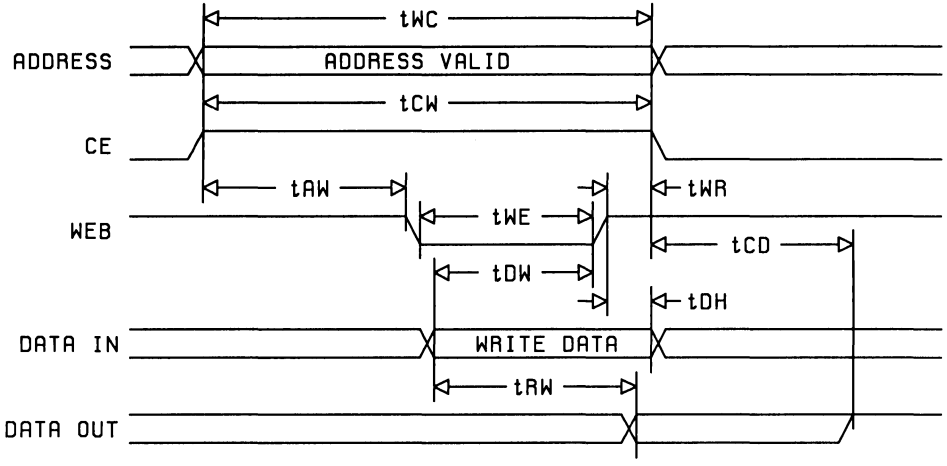


Read Cycle Timing for a 256 x 8 Array

Switching Characteristics (Input tr, tf=1.4ns, CL=0.5pF)

SYMBOL	PARAMETER	NOMINAL VDD=5V		WORST CASE VDD=4.5V						UNITS
		TA=25C		TA=70C		TA=85C		TA=125C		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tRC	Read Cycle Time	14.0		28.7		29.9		33.6		ns
tACC	Address Access Time		14.0		28.7		29.9		33.6	ns
tCE	Cell Enable Time		14.0		28.7		29.9		33.6	ns
tOH	Data Hold Time	0		0		0		0		ns
tOE	Output Enable Time		5.9		12.2		12.7		14.3	ns
tOD	Output Disable Time		5.9		12.2		12.7		14.3	ns
tRD	LC Read Data Time	0	6.5	0	13.4	0	14.0	0	15.7	ns
tLC	Latch Time	0		0		0		0		ns

Write Cycle



Write Cycle Timing for a 256 x 8 Array

Switching Characteristics (Input tr, tf=1.4ns, CL=0.5pF)

SYMBOL	PARAMETER	NOMINAL VDD=5V		WORST CASE VDD=4.5V						UNITS
		TA=25C		TA=70C		TA=85C		TA=125C		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tWC	Write Cycle Time	10.4		21.2		22.1		24.8		ns
tCW	Cell Enable Time	10.4		21.2		22.1		24.8		ns
tAW	Address Write Margin	4.3		8.7		9.1		10.2		ns
tWE	Write Enable Time	4.4		9.0		9.4		10.5		ns
tWR	Write Recovery Time	1.7		3.5		3.7		4.1		ns
tDW	Data Write Time	4.1		8.4		8.8		9.8		ns
tDH	Data Hold Time	3.4		7.0		7.3		8.2		ns
tRW	Read after Write Time		8.0		16.5		17.2		19.3	ns
tCD	Data High from CE Low		17.3		35.6		37.1		41.6	ns

SRAM m x n

ViGen CONFIGURABLE FUNCTION

Timing Parameters and Cell Size as Functions of Input Parameters

1. The input parameters are: NUM_WORDS and DATA_WIDTH. CL is the maximum capacitance in pF of the data output bus. ADDRESS_WIDTH is $\log_2$ (NUM_WORDS) rounded up to the nearest integer.
2. Timing parameters are specified for nominal process, Vdd = 5.0 volts, and temperature = 25°C. See the NCR ASIC Data Book for information on derating factors for process, voltage, and temperature.
3. The coefficient of CL is 0.47 for NDLH, and 0.41 for NDHL.

PARAM	DESCRIPTION	TYPICAL VALUE (ns)
t_{rc}	Read cycle time	10.0 + 0.22*DATA_WIDTH + 0.0078*NUM_WORDS + 0.47*CL
t_{acc}	Address access time	10.0 + 0.22*DATA_WIDTH + 0.0078*NUM_WORDS + 0.47*CL
t_{ce}	Cell enable time	10.0 + 0.22*DATA_WIDTH + 0.0078*NUM_WORDS + 0.47*CL
t_{oh}	Data hold time	0
t_{oe}	Output enable time	5.7 + 0.47*CL
t_{od}	Output disable time	5.7 + 0.47*CL
t_{rd}	LC read data time	6.3 + 0.47*CL
t_{lc}	Latch time	0
t_{wc}	Write cycle time	8.22 + 0.127*DATA_WIDTH + 0.0043*NUM_WORDS
t_{cw}	Cell enable time	8.22 + 0.127*DATA_WIDTH + 0.0043*NUM_WORDS
t_{aw}	Address write margin	2.14 + 0.127*DATA_WIDTH + 0.0043*NUM_WORDS
t_{we}	Write enable time	4.38
t_{wr}	Write recovery time	1.70
t_{dw}	Data write time	4.09
t_{dh}	Data hold time	3.41
t_{rw}	Read after write time	7.8 + 0.47*CL
t_{cd}	Data high from CE low	17.1 + 0.47*CL
t_{r}	Rise time	1.25 + 0.66*CL
t_{f}	Fall time	1.28 + 0.40*CL

Cell Width (mils)

for DATA_WIDTH ≤ 4:

= 1.6 + 7.3*DATA_WIDTH + 1.04*ADDRESS_WIDTH

for DATA_WIDTH > 4:

= 4.7 + 7.3*DATA_WIDTH + 1.04*ADDRESS_WIDTH

Cell Height (mils) = 14.0 + 0.146*NUM_WORDS

Application Notes

General Description

The modular High Speed 1.5m SRAM Supercell provides a means of adding high speed random access memory to a standard cell design. The asynchronous operation and familiar control interface makes this supercell similar to a stand alone static RAM device.

Read Mode

To read the High Speed SRAM, enable the cell (CE high) and assert the desired address. The SRAM is asynchronous and requires no precharge cycle between operations. The read data is gated to the output drivers when the LC signal is high and may be latched by bringing LC low. The output drivers are enabled when OEB is low and are in a high impedance state when OEB goes high. This allows easy interfacing and bidirectional I/O if desired.

The Latch Control signal (LC) operates independently form the Cell Enable signal (CE). If LC makes a transition from high to low while CE is low, all 1s will be latched into the output latches.

Write Mode

To write the SRAM, enable the cell (CE high), assert the desired address, and pulse the write enable bar signal (WEB) low. The data from the data inputs will be written to the memory array.

Power Dissipation

This SRAM supercell uses a truly static design approach commonly seen in stand alone devices. This approach allows the advantage of asynchronous operation with the corresponding faster cycle times at the expense of higher static power dissipation. The IDD current draw will depend on the number of bits per word, but will nominally be in the tens of milliamps range. The SRAM may be placed into a very low power mode (less than 100uA IDD) by bringing the CE signal low. This places the cell in a low power mode that is suitable for battery backed memory storage.

SRAM DC IDD CURRENT (Nominal Conditions)

For DATA_WIDTH ≤ 4
IDD READ = 2.7 + 3.3*DATA_WIDTH mA
IDD WRITE = 2.7 + 4.5*DATA_WIDTH mA

For DATA_WIDTH > 4
IDD READ = 5.4 + 3.3*DATA_WIDTH mA
IDD WRITE = 5.4 + 4.5*DATA_WIDTH mA

IDD WITH CE LOW < 100uA

Designing for Testability

Test programs for ASIC components must be able to verify that all circuit elements in the design are functioning properly. This includes verifying the functional correctness of the design and detecting faults caused by manufacturing defects. There are many methods to improve the testability of a component, all of which involve trade–offs in the amount of extra logic required, the resulting test time, and the degree of test coverage. A highly recommended method for the SRAM is to multiplex the address, control, and data lines to the external part pins during a test mode. This allows direct control and observability of the SRAM during test. In pin limited situations, the use of scan registers to shift in the address and data and shift out the output may be desired.

To adequately test the SRAM, the following conditions should be met as a minimum:

1. Every bit must be written to both a one and a zero at least once and verified.
2. The data output should change frequently between consecutive reads (a "checkerboard" pattern is a good example of this).
3. Use at least one pattern that will catch address decode faults. A good example of this is to write the address value to all locations in memory and then read back the results. Another example is to write the parity of the address to all locations and verify the results. The intent here is to catch faults in the address decode which may otherwise go undetected in a highly repetitive pattern. The "checkerboard" pattern is poor at detecting these types of faults.
4. Write the entire memory first and then read back the results. The intent here is to catch any write or read disturb problems that may otherwise go undetected. This is most effective on a highly unrepetitive pattern such as the one used for address decode fault checking.

Naming Conventions

ViGen will automatically create a default cell name for each unique SRAM configuration. The name of each configurations is encoded in the following manner:

SRAM *num_words X data_width*

Two examples of default names are:

SRAM256X16
SRAM32X8

Limitations

The Mentor BLM will store all bits of a word to unknown values (X's) if any bit of a word is unknown during the write cycle.

NCR Supercells Data Sheets

Core Microprocessor

PC Core Logic Cells

PC and Workstation Peripheral I/O Cells

JTAG Boundary Scan Cells

Page	Cell Name	Cell Description
8–126	BSENBR	Boundary Scan Cell for Tristate Enable
8–127	BSINMUX	Boundary Scan 2–Input Multiplexer
8–129	BSINR	Boundary Scan Cell for Input Pads
8–130	BSINV4	Boundary Scan Inverting 2–Input Multiplexer (4X Drive)
8–132	BSINV8	Boundary Scan Inverting 2–Input Multiplexer (8X Drive)
8–134	BSIOR1	Boundary Scan Cell for Input/Output Pads 1X Drive
8–136	BSIOR4	Boundary Scan Cell for Input/Output Pads 4X Drive
8–138	BSIOR8	Boundary Scan Cell for Input/Output Pads 8X Drive
8–140	BSOTR1	Boundary Scan Cell for Tristate Output Pads 1X Drive
8–141	BSOTR4	Boundary Scan Cell for Tristate Output Pads 4X Drive
8–142	BSOTR8	Boundary Scan Cell for Tristate Output Pads 8X Drive
8–143	BSOUTR1	Boundary Scan Cell for Output Pads 1X Drive
8–144	BSOUTR4	Boundary Scan Cell for Output Pads 4X Drive
8–145	BSOUTR8	Boundary Scan Cell for Output Pads 8X Drive
8–146	IRCELL0	Instruction Register Cell
8–147	IRCELL1	Instruction Register Cell
8–148	TAP_CONTROLLER	TAP Controller

7400 Series Soft Macrocells

Page	Cell Name	Cell Description
8–153	7430	8–Input Positive NAND
8–154	7442	4–Line to 10–Line Decoder
8–156	7443	4–Line to 10–Line Decoder
8–158	7444	4–Line to 10–Line Decoder
8–160	7451	Dual 2–Wide 2–Input AND–OR–INVERT Gates
8–161	4782	2–Bit Binary Full Adder
8–162	7483	4–Bit Binary Full Adders with Fast Carry
8–164	7485	4–Bit Magnitude Comparator
8–166	7486	Quad 2–Input EXCLUSIVE–OR Gates
8–167	7487	4–Bit True/Complement
8–169	7490	Decade Counter
8–171	7492	Divide by Two, Six, or Twelve Counter
8–173	7493	4–Bit Binary Counter
8–175	7494	4–Bit Shift Register with Presets
8–177	7498	4–Bit Data Selector Registers
8–179	74126	Quad–Tristate Buffer
8–181	74138	3– to 8–Line Decoder/Demultiplexer
8–183	74139	Dual 2– to 4–Line Decoders/Demultiplexers
8–185	74147	Decimal to BCD Priority Encoder
8–187	74148	8–Line to 3–Line Priority Encoders
8–189	74150	1 of 16 Data Multiplexer
8–191	74151	1 of 8 Data Multiplexer
8–193	74151NS	1 of 8 Data Multiplexer
8–195	74152	1 of 8 Data Multiplexer
8–197	74153	Dual 4–Line to 1–Line Data Multiplexers
8–199	74156	Dual 2–Line to 4–Line Decoder
8–201	74157	Quad 2– to 1–Line Data Multiplexers
8–203	74157NS	Quad 2– to 1–Line Data Multiplexers
8–205	74158	Quad 2– to 1–Line Multiplexers
8–207	74161	Synchronous 4–Bit Counter
8–209	74161NE	4–Bit Binary Counter No Enable
8–211	74163CP	4–Bit Binary Counter
8–213	74163L	4–Bit Binary Counter
8–215	74163LC	4–Bit Binary Counter
8–217	74163LCP	4–Bit Binary Counter
8–219	74164	8–Bit Serial Shift Register
8–221	74165	8–Bit Shift Register
8–223	74165C	8–Bit Shift Register
8–225	74166	8–Bit Shift Register

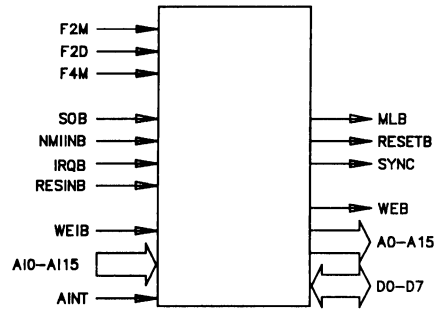
NCR65CX02 Core Microprocessor

Description

- Enhanced software performance including 59 additional OP codes encompassing fourteen new instructions and two additional addressing modes
- 70 microprocessor instructions
- 15 addressing modes
- 210 operational codes
- Up to 5 MHz operation
- Operates at frequencies as low as 200 Hz for even lower power consumption (pseudostatic: stop during F2M low)
- Compatible with NMOS 6500 series microprocessors
- 64 K-byte addressable memory
- Interrupt capability
- Lower power consumption, 4 mA @ 1 MHz
- 8-bit bidirectional data bus
- Bus compatible with M6800
- Non-maskable interrupt
- 8-bit parallel processing
- Decimal and binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack

The 65CX02 supercell is an 8-bit microprocessor which is software compatible with the NMOS 6502. Enhancements include fourteen additional instructions (four more than the NCR65C02 microprocessor), expanded operational codes and two new addressing modes. Bit manipulation instructions have been added to facilitate software control of memory-mapped I/O and control registers. Timings in this datasheet reflect implementation in the VS1500F library. VS700 timings will differ.

Logic Symbol

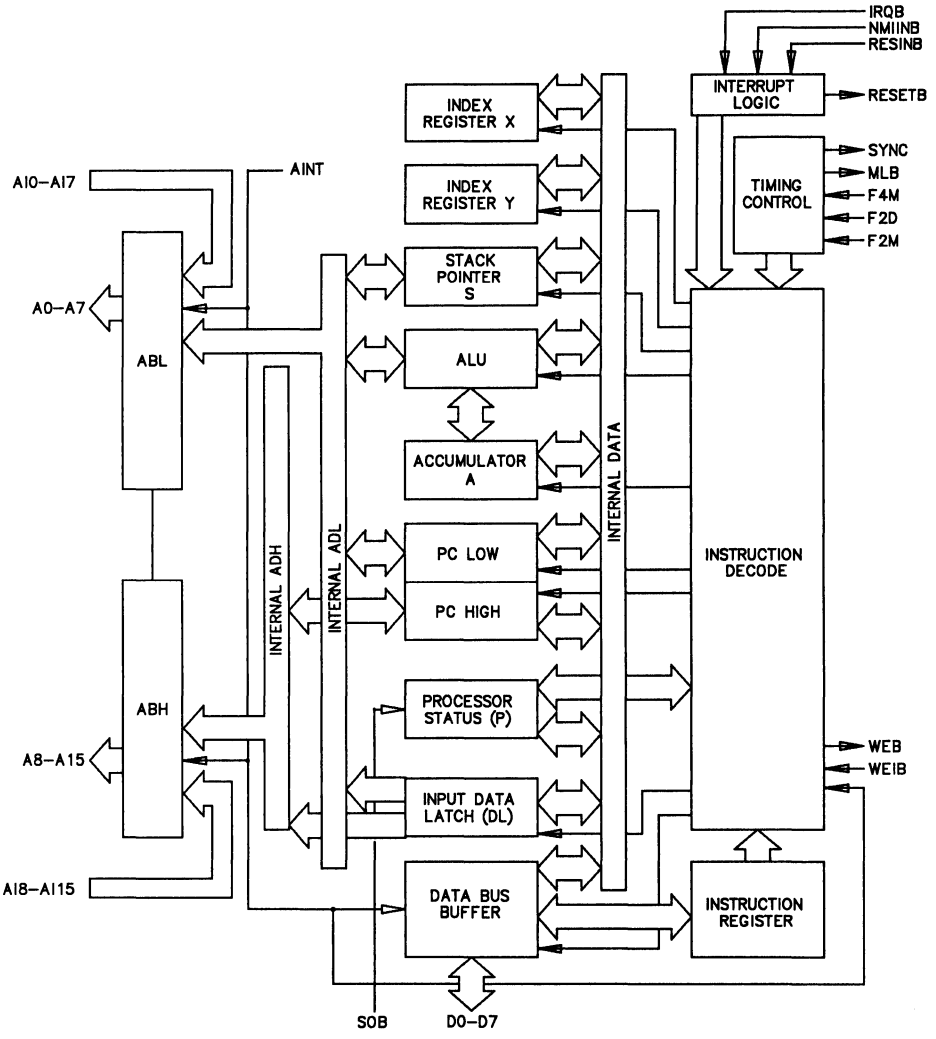


Port Functions

PORT	FUNCTION
A0–A15	Address Bus Outputs
AI0–AI15	Address Bus from External Source (for DMA)
AINT	Internal Address Selector
D0–D7	Bidirectional Data Bus
F2D	Phase 2 Clock for Interrupts
F2M	Phase 2 Clock
F4M	Phase 4 Clock
IRQB	Interrupt Request (Maskable)
MLB	Memory Lock
NMIINB	Non-Maskable Interrupt
RESETB	Reset Output
RESINB	Reset Input
SOB	Set Overflow
SYNC	Synchronize
WEB	Write Enable Output
WEIB	Write Enable from External Source (for DMA)

SUPERCELLS

Functional Block Diagram



Microprocessor Operational Enhancements

Function	NMOS 6502 Microprocessor	NCR65CX02 Supercell
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). OP Code Bytes Cycles X2 2 2 X3, XB 1 1 44 2 3 54,D4,F4 2 4 5C 3 8 DC, FC 3 4
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective addresses.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = 0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flags add one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

New Instruction Mnemonics

HEX	MNEMONIC	DESCRIPTION
0F–7F	BBRn	Branch on bit "n" reset [Zero page]
8F–FF	BBSn	Branch on bit "n" set [Zero page]
80	BRA	Branch relative always [Relative]
3A	DEA	Decrement accumulator [Accum]
1A	INA	Increment accumulator [Accum]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied]
7A	PLY	Pull Y from stack [Implied]
07–77	RMBn	Reset memory bit "n" [Zero page]
87–F7	SMBn	Set memory bit "n" [Zero page]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [Zero page]
74	STZ	Store zero [ZPG, X]
1C	TRB	Test and reset memory bits with accumulator [Absolute]
14	TRB	Test and reset memory bits with accumulator [Zero page]
0C	TSB	Test and set memory bits with accumulator [Absolute]
04	TSB	Test and set memory bits with accumulator [Zero page]

Input Port Capacitances

Port	Input Capacitance (pF)	Port	Input Capacitance (pF)
AI0	.272	AI13	.241
AI1	.270	AI14	.233
AI2	.265	AI15	.225
AI3	.252	AINT	1.849
AI4	.244	D0–D7	.099
AI5	.231	F2D	.278
AI6	.225	F2M	2.139
AI7	.213	F4M	1.177
AI8	.278	IRQB	.174
AI9	.271	NMIINB	.091
AI10	.263	RESINB	.182
AI11	.255	SOB	.176
AI12	.248	WEIB	.115

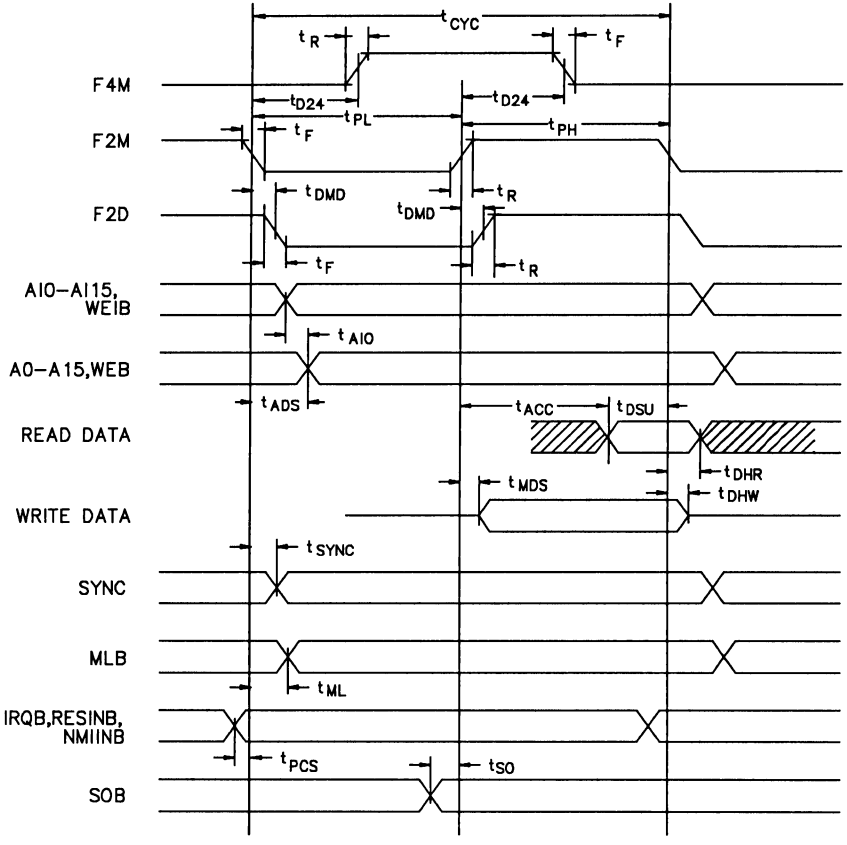
AC Characteristics

V_{DD} = 5V ± 10%, T_A = 0°C to 70°C, Load = .25 pF (VS1500F)

Parameter	Symbol	Min.	Max.	Units
Cycle Time*	t_{CYC}	0.200	5000	µs
Clock Pulse Width Low	t_{PL}	96		ns
Clock Pulse Width High	t_{PH}	96		ns
Fall Time, Rise Time	t_F, t_R		20	ns
Phase 2 to Phase 4 Delay	t_{D24}	$1/2t_{PL}$ – 5	$1/2t_{PL}$ + 5	ns
F2M to F2D Delay	t_{DMD}	– 10	10	ns
Address Input to Output (AINT low)	t_{AIO}	13	25	ns
Address Setup Time (AINT high)	t_{ADS}	23	60	ns
Read Access Time	t_{ACC}	82		ns
Read Data Setup Time	t_{DSU}	9		ns
Read Data Hold Time	t_{DHR}	9		ns
Write Data Delay Time	t_{MDS}		25	ns
Write Data Hold Time	t_{DHW}	9		ns
SYNC Delay Time	t_{SYNC}		25	ns
Memory Lock Delay Time	t_{ML}		25	ns
Processor Control Setup Time**	t_{PCS}	9		ns
SO Setup Time	t_{SO}	9		ns

*The processor can be stopped with F2M and F4M held low.
**This parameter must only be met to guarantee that the signal will be recognized at the current clock cycle.

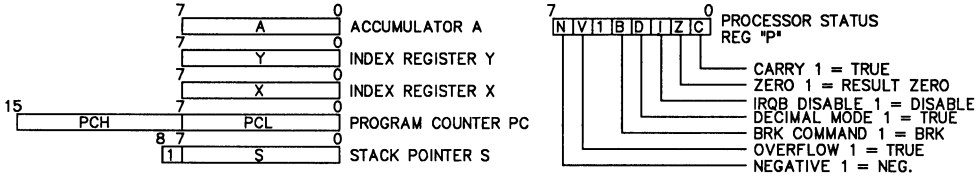
Timing Diagram



Additional Instruction Addressing Modes

HEX	MNEMONIC	DESCRIPTION
72	ADC	Add memory to accumulator with carry [(ZPG)]
32	AND	"AND" memory with accumulator [(ZPG)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZPG, X]
D2	CMP	Compare memory and accumulator [(ZPG)]
52	EOR	"Exclusive Or" memory with accumulator [(ZPG)]
7C	JMP	Jump (New addressing mode) [ABS(IND, X)]
B2	LDA	Load accumulator with memory [(ZPG)]
12	ORA	"OR" memory with accumulator [(ZPG)]
F2	SBC	Subtract memory from accumulator with borrow [(ZPG)]
92	STA	Store accumulator in memory [(ZPG)]

Microprocessor Programming Model



Functional Description

Timing Control

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase two clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program. Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8 bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address. When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts (NMIINB and IRQB). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags (see Microprocessor Programming Model).

Addressing Modes

Fifteen addressing modes are available to the user of the NCR65CX02 microprocessor. The addressing modes are described in the following paragraphs:

Implied Addressing [Implied]
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing [Accum]
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator.

Immediate Addressing [Immediate]
With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing [Absolute]
For absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits. Therefore, this addressing mode allows access to the total 64K bytes of addressable memory.

Zero Page Addressing [Zero Page]
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing [ABS, X or ABS, Y]
Absolute indexed addressing is used in conjunction with the X or Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

Zero Page Indexed Addressing [ZPG, X or ZPG, Y]
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high-order eight bits of memory, and crossing of page boundaries does not occur.

Relative Addressing [Relative]
Relative addressing is used only with branch instructions; it establishes a destination for the conditional branch. The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

Zero Page Indexed Indirect Addressing [(IND, X)]
With zero page indexed indirect addressing (usually referred to as Indirect, X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose content is the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high- and low-order bytes of the effective address must be in page zero.

***Absolute Indexed Indirect Addressing [ABS(IND, X)] (Jump Instruction Only)**
With absolute indexed indirect addressing the contents of the second and third instruction bytes are added to the X register. The result of this addition points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing [(IND), Y]
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

***Zero Page Indirect Addressing [(ZPG)]**
In the zero page indirect addressing mode, the second byte of the instruction points to a memory location on page zero containing the low-order byte of the effective address. The next location on page zero contains the high-order byte of the effective address.

Absolute Indirect Addressing [(ABS)] (Jump Instruction Only)
The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address which is loaded into the 16-bit program counter.

NOTE: * = New Address Modes

Signal Description

Address Bus Outputs (A0–A15)
A0–A15 form a 16-bit address bus for memory and I/O exchanges on the data bus. These outputs will reflect the state of the CPU's internal address if AINT is input high, otherwise the external address (AI0–AI15) is output. The address bus outputs are buffered sufficiently to drive large on-chip busses.

External Address Bus Inputs (AI0–AI15)
An external controller can take over control of the address bus by pulling AINT low asynchronously. Immediately, the address bus outputs (A0–A15) and WEB will reflect the inputs at AI0–AI15 and WEIB.

Address Bus Selector (AINT)
Selects whether the CPU's internal address and write enable, or the external address bus and WEIB will appear at the A0–A15 outputs and WEB. This input is immediate: the outputs will update t_{AIO} after AINT changes.

Data Bus (D0–D7)
The data lines (D0–D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the CPU supercell and other elements of a microcomputer system (on-chip or off-chip). The outputs are buffered sufficiently to drive large on-chip busses.

Interrupt Clock (F2D)
In normal operation, F2D is exactly in phase with the main CPU clock, F2M. F2D is used to latch in the signals RESINB, NMIINB, and IRQB. Separating F2D and F2M allows a low power "sleep mode," where the main CPU can be shut down by stopping F2M and F4M low. A reset or interrupt can then "wake up" the CPU if F2D is still running. The power dissipation necessary to keep F2D running is considerably less than for F2M.

Phase 2 Clock (F2M)
This is the main time base for the CPU. Each cycle begins on a falling edge of F2M. Data bus transfers occur when F2M is high (see Timing Diagram). When the CPU is put in sleep mode or when DMA operations are invoked by pulling AINT low, F2M must stop after a falling edge, so that all data on the data bus will have been latched into its proper destination. If in DMA mode, the data bus will then be available to the external bus master.

Phase 4 Clock (F4M)
F4M is used for additional internal timing in the CPU, and should lead F2M by a quarter cycle (see Timing Diagram). In sleep mode or DMA modes, F4M should be stopped low.

Interrupt Request (IRQB)
This input requests that an interrupt sequence begin within the microprocessor. The IRQB is sampled during F2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during the next cycle. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further IRQBs may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses.

Memory Lock (MLB)
In a multiprocessor system, the MLB output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. MLB goes low during ASL, BBRn, BBSn, DEC, INC, LSR, RMBn, ROL, ROR, SMBn, TRB, and TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt (NMIINB)
A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The NMIINB is sampled during F2; the current instruction is completed and the interrupt sequence begins during the next cycle. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

Note: Since this interrupt is non-maskable, another NMIINB can occur before the first is finished. Care should be taken when using NMIINB to avoid this.

Reset (RESETB)
This output is a buffered version of the CPU's internal reset signal, for use by other circuits on-chip that need to be initialized.

Reset Input (RESINB)
This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on RESINB.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation. A latched version of RESINB will appear at the RESETB output after one falling F2 edge.

Set Overflow (SOB)
A negative transition on this line sets the overflow bit in the status code register. The signal is sampled halfway through each cycle (see Timing Diagram).

Synchronize (SYNC)
This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high at the beginning of an OP CODE fetch and stays high for the remainder of that cycle. If OP CODEs of X3 or XB (X = don't care) are fetched, another OP CODE will be fetched in the next cycle, and SYNC will remain high for the two fetch cycles.

Write Enable (WEB)
This signal is normally in the high state, indicating that the CPU is reading data from memory. If AINT is high, the CPU's internal write signal will appear on the WEB output. When AINT is low, the WEIB input is gated to the WEB output. A low on WEB indicates that whatever device has control of the busses has data to be written to the addressed memory location.

External Write Enable Input (WEIB)
This input is used in conjunction with the AI0–AI15 inputs when AINT is pulled low, to indicate whether the addressed memory location is to be read from or written to.

Instruction Set – Alphabetical Sequence

ADC	Add Memory to Accumulator with Carry	LDX	Load Index X with Memory
AND	"AND" Memory with Accumulator	LDY	Load Index Y with Memory
ASL	Shift One Bit Left	LSR	Shift One Bit Right
*BBRn	Branch on Bit "n" Reset	NOP	No Operation
*BBSn	Branch on Bit "n" Set	ORA	"OR" Memory with Accumulator
BCC	Branch on Carry Clear	PHA	Push Accumulator on Stack
BCS	Branch on Carry Set	PHP	Push Processor Status on Stack
BEQ	Branch on Result Zero	*PHX	Push Index X on Stack
BIT	Test Memory Bits with Accumulator	*PHY	Push Index Y on Stack
BMI	Branch on Result Minus	PLA	Pull Accumulator from Stack
BNE	Branch on Result not Zero	PLP	Pull Processor Status from Stack
BPL	Branch on Result Plus	*PLX	Pull Index X from Stack
*BRA	Branch Always	*PLY	Pull Index Y from Stack
BRK	Force Break	*RMBn	Reset Memory Bit "n"
BVC	Branch on Overflow Clear	ROL	Rotate One Bit Left
BVS	Branch on Overflow Set	ROR	Rotate One Bit Right
CLC	Clear Carry Flag	RTI	Return from Interrupt
CLD	Clear Decimal Mode	RTS	Return from Subroutine
CLI	Clear Interrupt Disable Bit	SBC	Subtract Memory from Accumulator with Borrow
CLV	Clear Overflow Flag	SEC	Set Carry Flag
CMP	Compare Memory and Accumulator	SED	Set Decimal Mode
CPX	Compare Memory and Index X	SEI	Set Interrupt Disable Bit
CPY	Compare Memory and Index Y	*SMBn	Set Memory Bit "n"
*DEA	Decrement Accumulator	STA	Store Accumulator in Memory
DEC	Decrement by One	STX	Store Index X in Memory
DEX	Decrement Index X by One	STY	Store Index Y in Memory
DEY	Decrement Index Y by One	*STZ	Store Zero in Memory
EOR	"Exclusive–Or" Memory with Accumulator	TAX	Transfer Accumulator to Index X
*INA	Increment Accumulator	TAY	Transfer Accumulator to Index Y
INC	Increment by One	*TRB	Test and Reset Memory Bits with Accumulator
INX	Increment Index X by One	*TSB	Test and Set Memory Bits with Accumulator
INY	Increment Index Y by One	TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Pointer
LDA	Load Accumulator with Memory	TYA	Transfer Index Y to Accumulator

Note: * = New Instruction

OPERATIONAL CODES, EXECUTION TIME, AND MEMORY REQUIREMENTS

MNE	OPERATION		IMME-DIATE OP	n	#	ABSO-LUTE OP	n	#	ZERO PAGE OP	n	#	ACCUM OP	n	#	IM-PLIED OP	n	#	(IND), X OP	n	#	(IND), Y OP	n	#	ZPG, X OP	n	#	ZPG, Y OP	n	#	ABS, X OP	n	#	ABS, Y OP	n	#	RELA-TIVE OP	n	#	(ABS) OP	n	#	ABS (IND, X) OP	n	#	(ZPG) OP	n	#	PROCESSOR STATUS CODES 7 N	6 V	5	4 B	3 D	2 I	1 Z	0 C	MNE
ADC	A + M + C → A	(1,3)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2				7D	4	3	79	4	3									72	5	2	N	V					Z	C	ADC
AND	A ∧ M → A	(1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2				3D	4	3	39	4	3									32	5	2	N						Z		AND
ASL	C ← 7 … 0 ← o	(1)				OE	6	3	06	5	2	0A	2	1										16	6	2				1E	6	3													N						Z	C	ASL
BBRn	Branch if M_n = 0	(2)							0F 7F	5	3																																											BBRn
BBSn	Branch if M_n = 1	(2)							8F FF	5	3																																											BBSn
BCC	Branch if C=0	(2)																																			90	2	2													BCC
BCS	Branch if C=1	(2)																																			80	2	2													BCS
BEQ	Branch if Z=1	(2)																																			F0	2	2													BEQ
BIT	A ∧ M	(4,5)	89	2	2	2C	4	3	24	3	2													34	4	2				3C	4	3													M_7* M_6*						Z		BIT
BMI	Branch if N=1	(2)																																			30	2	2													BMI
BNE	Branch if Z=0	(2)																																			D0	2	2													BNE
BPL	Branch if N=0	(2)																																			10	2	2													BPL
BRA	Branch Always	(2)																																			80	2	2													BRA
BRK	Break														00	7	1																																1		1			BRK
BVC	Branch if V=0	(2)																																			50	2	2													BVC
BVS	Branch if V=1	(2)																																			70	2	2													BVS
CLC	0 → C														18	2	1																																					CLC
CLD	0 → D														D8	2	1																																0					CLD
CLI	0 → I														58	2	1																																	0				CLI
CLV	0 → V														B8	2	1																																	0				CLV
CMP	A - M	(1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2				DD	4	3	D9	4	3									D2	5	2	N						Z	C	CMP
CPX	X - M		E0	2	2	EC	4	3	E4	3	2																																											CPX
CPY	Y - M		C0	2	2	CC	4	3	C4	3	2																																											CPY
DEA	A - 1 → A																																																					DEA
DEC	M - 1 → M	(1)				CE	6	3	C6	5	2													D6	6	2				DE	6	3													N						Z		DEC
DEX	X - 1 → X											3A	2	1																																						DEX
DEY	Y - 1 → Y														CA	2	1																																				DEY
EOR	A ∨ M → A		49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2				5D	4	3	59	4	3									52	5	2	N						Z		EOR
INA	A + 1 → A											1A	2	1																																						INA
INC	M + 1 → M	(1)				EE	6	3	E6	5	2													F6	6	2				FE	6	3													N						Z		INC
INX	X + 1 → X														E8	2	1																																				INX
INY	Y + 1 → Y														C8	2	1																																				INY
JMP	Jump to new loc					4C	3	3																																	6C	6	3	7C	6	3								JMP
JSR	Jump Subroutine					20	6	3																																												JSR
LDA	M → A	(1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2				BD	4	3	B9	4	3									B2	5	2	N						Z		LDA
LDX	M → X	(1)	A2	2	2	AE	4	3	A6	3	2																B6	4	2				BE	4	3									N						Z		LDX
LDY	M → Y	(1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2				BC	4	3													N						Z		LDY
LSR	o → 7 … 0 → C	(1)				4E	6	3	46	5	2	4A	2	1										56	6	2				5E	6	3													0						Z	C	LSR
NOP	PC + 1 → PC														EA	2	1																																				NOP
ORA	A V M → A	(1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2				1D	4	3	19	4	3									12	5	2	N						Z		ORA
PHA	A → M_S S - 1 → S														48	3	1																																				PHA
PHP	P → M_S S - 1 → S														08	3	1																																				PHP
PHX	X → M_S S - 1 → S														DA	3	1																																				PHX
PHY	Y → M_S S - 1 → S														5A	3	1																																				PHY
PLA	S + 1 → S M_S → A														68	4	1																																N						Z		PLA
PLP	S + 1 → S M_S → P														28	4	1																																N	V		1	D	I	Z	C	PLP
PLX	S + 1 → S M_S → X														FA	4	1																																N						Z		PLX
PLY	S + 1 → S M_S → Y														7A	4	1																																N						Z		PLY
RMBn	0 → M_n								07 77	5	2																																											RMBn
ROL	7 … 0 ← C	(1)				2E	6	3	26	5	2	2A	2	1										36	6	2				3E	6	3													N						Z	C	ROL
ROR	C → 7 … 0	(1)				6E	6	3	66	5	2	6A	2	1										76	6	2				7E	6	3													N						Z	C	ROR
RTI	Return from Inter.														40	6	1																																N	V		1	D	I	Z	C	RTI
RTS	Return from Subr.														60	6	1																																				RTS
SBC	A - M - $\overline{C}$ → A	(1,3)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2							FD	4	3	F9	4	3							F2	5	2	N	V					Z	C	SBC
SEC	1 → C														38	2	1																																		1	SEC
SED	1 → D														F8	2	1																																				SED
SEI	1 → I														78	2	1																																				SEI
SMBn	1 → M_n								87 F7	5	2																																											SMBn
STA	A → M					8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2							9D	5	3	99	5	3							92	5	2										STA
STX	X → M					8E	4	3	86	3	2																96	4	2																									STX
STY	Y → M					8C	4	3	84	3	2													94	4	2																											STY
STZ	OO → M					9C	4	3	64	3	2													74	4	2				9E	5	3																				STZ
TAX	A → X														AA	2	1																																N						Z		TAX
TAY	A → Y														A8	2	1																																N						Z		TAY
TRB	$\overline{A}$ ∧ M → M	(4)				1C	6	3	14	5	2																																											TRB
TSB	A ∨ M → M	(4)				0C	6	3	04	5	2																																											TSB
TSX	S → X														BA	2	1																																N						Z		TSX
TXA	X → A														8A	2	1																																N						Z		TXA
TXS	X → S														9A	2	1																																					TXS
TYA	Y → A														98	2	1																																N						Z		TYA

NOTES:
1. Add 1 to "n" if page boundary is crossed.
2. Add 1 to "n" if branch occurs to same page.
   Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. V bit equals memory bit 6 prior to execution.
   N bit equals memory bit 7 prior to execution.
*5. The immediate addressing mode of the BIT instruction leaves bits 6 & 7 (V & N) in the Processor Status Code Register unchanged.

X Index X
Y Index Y
A Accumulator
M Memory per effective address
M_S Memory per stack pointer

\+ Add
– Subtract
∧ And
V Or
∀

n No. Cycles
No. Bytes
M_6 Memory bit 6
M_7 Memory bit 7
M_n Memory bit n

SUPERCELLS

SD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			TSB[1] zpg	ORA zpg	ASL zpg	**RMB0[1] zpg**	PHP	ORA imm	ASL A		TSB[1] abs	ORA abs	ASL abs	**BBR0[1] zpg**	0
1	BPL rel	ORA ind, Y	ORA[1, 2] (zpg)		TRB[1] zpg	ORA zpg, X	ASL zpg, X	**RMB1[1] zpg**	CLC	ORA abs, Y	INA[1] A		TRB[1] abs	ORA abs, X	ASL abs, X	**BBR1[1] zpg**	1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg	**RMB2[1] zpg**	PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs	**BBR2[1] zpg**	2
3	BMI rel	AND ind, Y	AND[1, 2] (zpg)		BIT[1] zpg, X	AND zpg, X	ROL zpg, X	**RMB3[1] zpg**	SEC	AND abs, Y	DEA[1] A		BIT[1, 2] abs, X	AND abs, X	ROL abs, X	**BBR3[1] zpg**	3
4	RTI	EOR ind, X				EOR zpg	LSR zpg	**RMB4[1] zpg**	PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs	**BBR4[1] zpg**	4
5	BVC rel	EOR ind, Y	EOR[1, 2] (zpg)			EOR zpg, X	LSR zpg, X	**RMB5[1] zpg**	CLI	EOR abs, Y	PHY[1]			EOR abs, X	LSR abs, X	**BBR5[1] zpg**	5
6	RTS	ADC ind, X			STZ[1] zpg	ADC zpg	ROR zpg	**RMB6[1] zpg**	PLA	ADC imm	ROR A		JMP (abs)	ADC abs	ROR abs	**BBR6[1] zpg**	6
7	BVS rel	ADC ind, Y	ADC[1, 2] (zpg)		STZ[1] zpg, X	ADC zpg, X	ROR zpg, X	**RMB7[1] zpg**	SEI	ADC abs, Y	PLY[1]		JMP[1, 2] abs (ind, X)	ADC abs, X	ROR abs, X	**BBR7[1] zpg**	7
8	BRA[1] rel	STA ind, X			STY zpg	STA zpg	STX zpg	**SMB0[1] zpg**	DEY	BIT[1] imm	TXA		STY abs	STA abs	STX abs	**BBS0[1] zpg**	8
9	BCC rel	STA ind, Y	STA[1, 2] (zpg)		STY zpg, X	STA zpg, X	STX zpg, Y	**SMB1[1] zpg**	TYA	STA abs, Y	TXS		STZ[1] abs	STA abs, X	STZ[1] abs, X	**BBS1[1] zpg**	9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg	**SMB2[1] zpg**	TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs	**BBS2[1] zpg**	A
B	BCS rel	LDA ind, Y	LDA[1, 2] (zpg)		LDY zpg, X	LDA zpg, X	LDX zpg, Y	**SMB3[1] zpg**	CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y	**BBS3[1] zpg**	B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg	**SMB4[1] zpg**	INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs	**BBS4[1] zpg**	C
D	BNE rel	CMP ind, Y	CMP[1, 2] (zpg)			CMP zpg, X	DEC zpg, X	**SMB5[1] zpg**	CLD	CMP abs, Y	PHX[1]			CMP abs, X	DEC abs, X	**BBS5[1] zpg**	D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg	**SMB6[1] zpg**	INX	SBC imm	NOP		CPX abs	SBC abs	INC abs	**BBS6[1] zpg**	E
F	BEQ rel	SBC ind, Y	SBC[1, 2] (zpg)			SBC zpg, X	INC zpg, X	**SMB7[1] zpg**	SED	SBC abs, Y	PLX[1]			SBC abs, X	INC abs, X	**BBS7[1] zpg**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note 1: New OP Codes
Note 2: New Address Modes

Real–Time Clock plus RAM

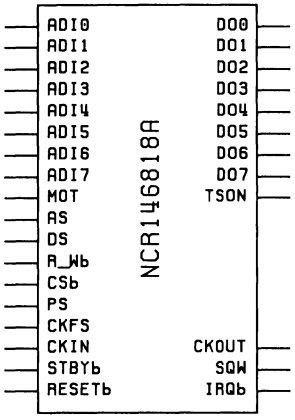
Features

- Binary or BCD counting
- 12– or 24–hour clock with 12–hour a.m. and p.m. mode
- Daylight Savings Time option
- Leap year and end–of–month recognition
- Programmable alarm
- Programmable square–wave output signal
- Bus–compatible interrupt (IRQb)
- Configurable as battery–backup operated from 5.5V to 3V.

Description

The NCR146818A Real–Time Clock plus RAM is a peripheral device which may be used with various microprocessors, microcomputers, and larger computers. This soft macrocell combines three features: a complete time–of–day clock with alarm and one hundred year calendar; a programmable periodic interrupt and square–wave generator; and 50 bytes of low–power static RAM. The Real–Time Clock plus RAM is designed for use as a battery–powered element, including all the common battery backed–up functions such as RAM, time, and calendar. For further functional information, consult the Motorola 146818A datasheet. The use of a lower case "b" at the end of a pin name indicates that the signal is asserted low.

Symbol



VS700 Cell Count: 587
Equivalent Gate Count: 1538
Plus 64 x 8 DPRAM

SUPERCELLS

Inputs/Outputs

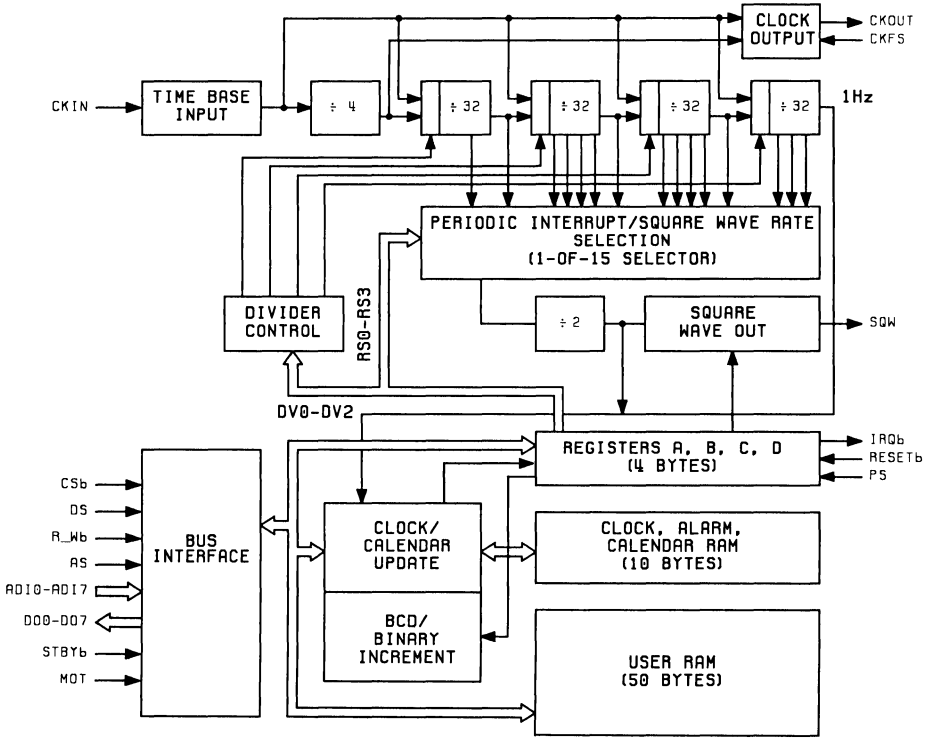
PIN NAME	TYPE	DESCRIPTION
ADI (7–0)	I	ADDRESS & DATA INPUT: Multiplexed Address and Data Bus Input. The Address must be stable during the falling edge of AS. The Data input must be stable during the back edge of DS or R_Wb.
MOT	I	MOTOROLA SELECT; Bus type select. A high on the MOT pin indicates a Motorola type bus interface. A low on the MOT pin indicates an Intel type bus interface.
AS	I	ADDRESS STROBE: The falling edge of AS latches the address from the ADI bus.
DS	I	DATA STROBE: The DS pin is used with the R_Wb pin to latch write data from the ADI and output data to the DO bus.
R_Wb	I	READ/WRITE: The R_Wb pin is used with the DS pin to read and write data.
CSb	I	CELL SELECT: The CSb signal must be low for bus operation. The CSb signal is not latched by AS.
PS	I	POWER SENSE: The PS signal is used to indicate a power fail condition. When PS is low, the VRT bit in register B is cleared.
CKFS	I	CLOCK FREQUENCY SELECT: When CKFS is high, CKOUT is the same frequency as CKIN. When CKFS is low, CKOUT frequency is one fourth the frequency of CKIN.
CKIN	I	CLOCK IN: Time base for the real time clock. Frequencies of 4.19304 MHz, 1.048576 MHz, or 32.768 KHz are supported.
STBYb	I	STANDBY: With STBYb low, access to the NCR146818A is prevented, facilitating battery back–up operation.
RESETb	I	RESET: Asserting RESETb low places the NCR146818A into a known condition. The clock, calendar, and RAM are not affected.
DO(7–0)	O	DATA OUTPUT: The data output bus. The DO bus may be combined with the ADI bus if configured as shown in the application note.
TSON	O	TRISTATE ON: When TSON is high, data is actively driven on the DO bus. When TSON is low the DO bus is in a high impedance state. TSON allows the recombination of the DO and ADI buses.
CKOUT	O	CLOCK OUT: The CKOUT pin outputs a signal of equal or one fourth the time base frequency. If CKFS is low, CKOUT is the same frequency as CKIN. If CKFS is high, CKOUT is one fourth the frequency of CKIN.
SQW	O	SQUARE WAVE: The SQW is a programmable square wave output. Programming register A allows the selection of 15 different frequency values.
IRQb	O	INTERRUPT REQUEST: An active low output on the IRQb pin indicates an interrupt is pending.

Input Signal Capacitance		
PIN	**VS1500F**	**VS700**
ADI(7–0)	0.054 pF	0.032 pF
MOT	0.163 pF	0.095 pF
AS	0.055 pF	0.035 pF
DS	o.159 pF	0.092 pF
R_Wb	0.159 pF	0.092 pF
CSb	0.055 pF	0.032 pF
PS	0.181 pF	0.165 pF
CKFS	0.163 pF	0.095 pF
CKIN	0.106 pF	0.059 pF
STBYb	0.038 pF	0.056 pF
RESETb	0.552 pF	0.478 pF

Output Signal Drive Capability		
PIN	**VS1500F**	**VS700**
DO(7–0)	INTV or DPRGEN	INTV or DPRGEN
TSON	HBUF	HBUF
CKOUT	MUX2H	MUX2H
SQW	MUX2H	MUX2H
IRQb	NOR3H	NOR3H

Note: Input signal capacitance consists of cell input capacitance only. Routing capacitance is not included since the routing will be different for each usage of the soft macrocell.

Functional Block Diagram



SUPERCELLS

Application Notes

This document describes some typical examples of integrating the NCR146818A Soft Macrocell within a designer's ASIC. Figure 8-1 sketches a typical internal bus-oriented interface. This first example incorporates techniques to isolate the battery-supported sections of logic while the rest of the chip is shut off to conserve power. Figure 8-2 shows a standard approach towards controlling and observing all of the macrocell's primary inputs/outputs at some subset of the ASIC's pins. The test access logic is merged with the interconnect of the first example.

The macrocell has been partitioned with battery backup application in mind. For purposes of electrical isolation, the multiplexed address and databus, called DBUS(7:0) in Figure 8-1, is split into an input side, ADI(7:0), and an output side, DO(7:0) which is connected through TBUFPs to DBUS(7:0). The split avoids any possible conduction paths which result when the outputs of tristate buffers in a portion of the chip which could be without power are connected to active or tristate outputs of powered circuits. The output side of the bus is connected only to the input side of receivers, in this case, tristate buffers controlled with TSON. Note that when the macrocell is in standby mode, TSON is low; hence, those buffers controlled with TSON are not driving.

If not using battery backup, it is entirely possible to configure the macrocell to appear to the rest of the ASIC as if the DBUS7:0 bus were bidirectional, simply by tying the input side to the output side. The designer should keep in mind the total loading represented by the input and output sides, however. The input side represents one gate load per each net of the bus; the output side represents five tristate drivers per each net of that bus.

The macrocell does not contain an internal oscillator but can be configured with an oscillator cell to drive the CKIN input. Oscillator cells are available to support all three different input frequencies for the macrocell.

The macrocell does not incorporate decoding logic to place its primary I/O in a suitable configuration for production tests. That particular function should be supplied in order to use the "canned" production test vectors supplied with the macro. If the ASIC has a pin which can serve to indicate a test setup, or an address and/or control combination to indicate same, or some other combination of inputs, a test sequence can be generated to configure the part for the canned vectors.

The Additional hardware required is minimal, since the canned vectors treat the DBUS(7:0) bus as a bidirectional 8-pin bus. Generally speaking, dedicated pins will already exist for DBUS, DS, R_Wb, PS, OSC1, OSC2, STBYb, and IRQb. To use the canned vectors, the designer will need to mux pins to the remaining input signals and mux the output signals to external pins, even if some of the associated functions are not fully utilized. For example, to ensure proper fault coverage of the 22-bit interrupt timer chain, the SQW output signal must be observable.

UIE bit (Register B, bit 4) Reset

The standard data sheet for 146818A states that the UIE bit may be cleared on the rising edge of the Set Bit (Register B, bit 7). The NCR146818A supports this statement completely and will continue to do so until further notice. However, tests conducted on samples of the standard part indicate that the rising edge of the Set Bit has no effect on the contents of the UIE bit.

Initialization of Memory Elements after First Application of Power

As in the standard data sheet for 146818A, NCR makes no claims regarding the state of any memory element (RAM or D Flip–Flop Registers) after power is initially applied to NCR146818A. The user should assume that the state of all memory elements in NCR146818A are unknown after initial power application. The user must properly program the NCR146818A after initial power application, and again after power has been completely removed from NCR146818A and restored to it.

Power Down Design and Usage Considerations

The NCR146818A macrocell is typically used to maintain the time in a battery back–up mode where V_{DD} is $\geq$ 3.0V. It is important to properly isolate the macrocell from the remainder of the ASIC to avoid unnecessary power dissipation in standby mode. NCR will add a separate V_{DD} pad to the design to isolate the macrocell power from the remainder of the ASIC. Contact NCR for further requirements in capturing the macrocell in your design.

The lowest standby power will be obtained when the device is operated with 32.768 KHz input to CKIN. If an external clock is used, an INPD cell should be used at the chip input and its output should be connected directly to the CKIN input. The INPD power must be considered in computing total chip power. If an oscillator cell is used, the INPD power is eliminated but the oscillator cell power must be added to the chip power.

In standby mode, the NCR146818A macrocell should be configured as described in the Motorola 146818A data sheet:

- the divider stage control (bits DV2, DV1, and DV0 of Register A) should be set for 32 KHz operation and CKFS should be tied low to select the low frequency output
- SQW output select bits (RS3–0 of Register A) should be set to turn off the SQW output
- The IRQb output should be disabled by disabling all sources of interrupt (PIE, AIE, and UIE of Register B)
- The CKOUT output should have as small a load as possible.

If the device is configured as stated, the CKIN signal is the only primary signal which will toggle the macrocell. To repeat, if an oscillator cell is used to generate the clock for CKIN, the oscillator power must be considered in the overall standby power during battery operation.

Functional Differences

CMOS Static RAM and Address Map

In the standard 146818A, all 64 bytes of the RAM are directly readable and writeable by the processor program except for the following:

- Registers C and D are read only
- Bit 7 of Register A is read only
- The high order bit of the seconds byte is read only.

However, in the NCR146818A macrocell, the high order bit of the seconds byte is read/write.

The CMOS static RAM can be used as a general purpose RAM. Since the high order bit of the seconds register is readable and writeable, the seconds byte can be used as a general purpose static RAM byte. Thus, with the dividers reset, 60 bytes (including the seconds byte) are available for general use as static RAM.

Update Cycle Times

The following table on Update cycle times has been updated to indicate the guaranteed values for NCR146818A.

UIP Bit	Time Base	Update Cycle Time (Tuc)	Minimum Time before Update Cycle (Tbuc)
1	4.194304 MHz 1.048576 MHz 32.768 KHz	200 µs 200 µs 1590 µs	– – –
0	Any	–	244 µs

Update cycle times

Kit Part Exception

The NCR146818A kit part uses the OSCP cell for the oscillator circuit. See the OSCP cell data sheet for details of its usage. For evaluation, an externally generated clock may be required for proper operation at lower frequencies.

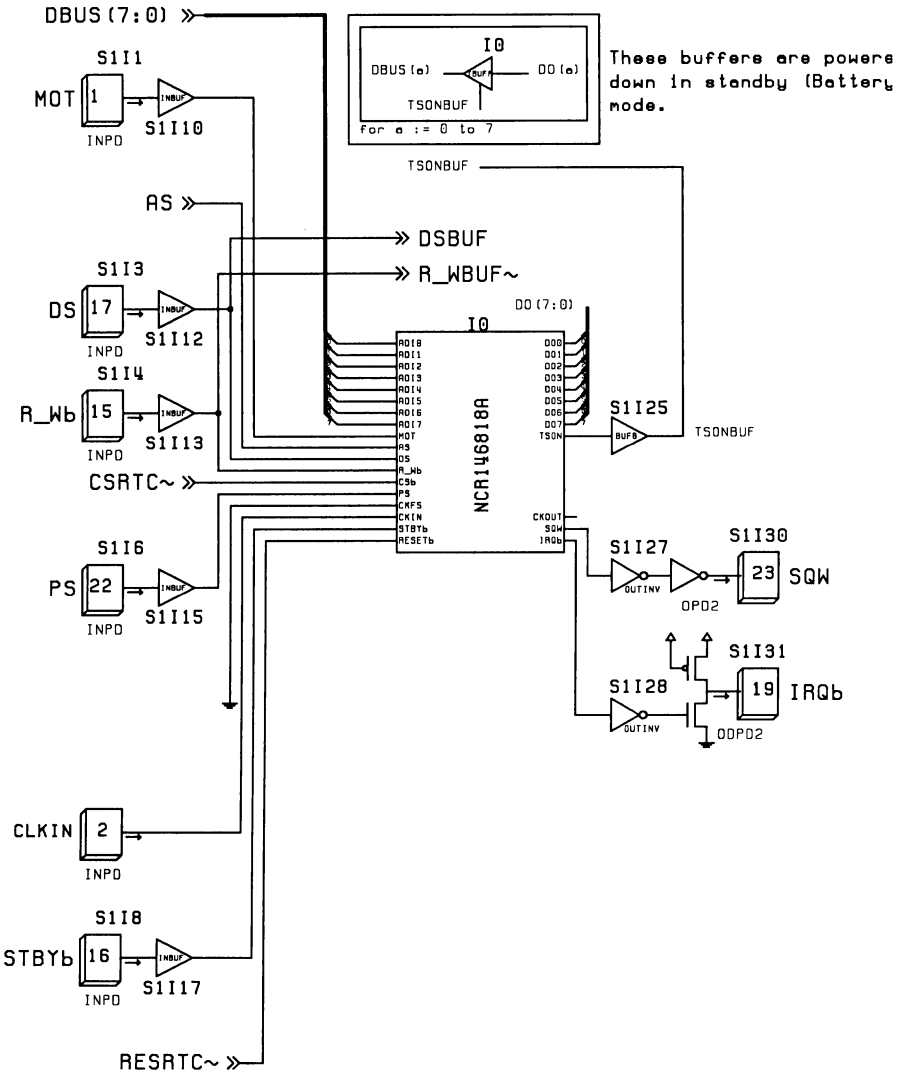


Figure 8–1 Bus connect example

SUPERCELLS

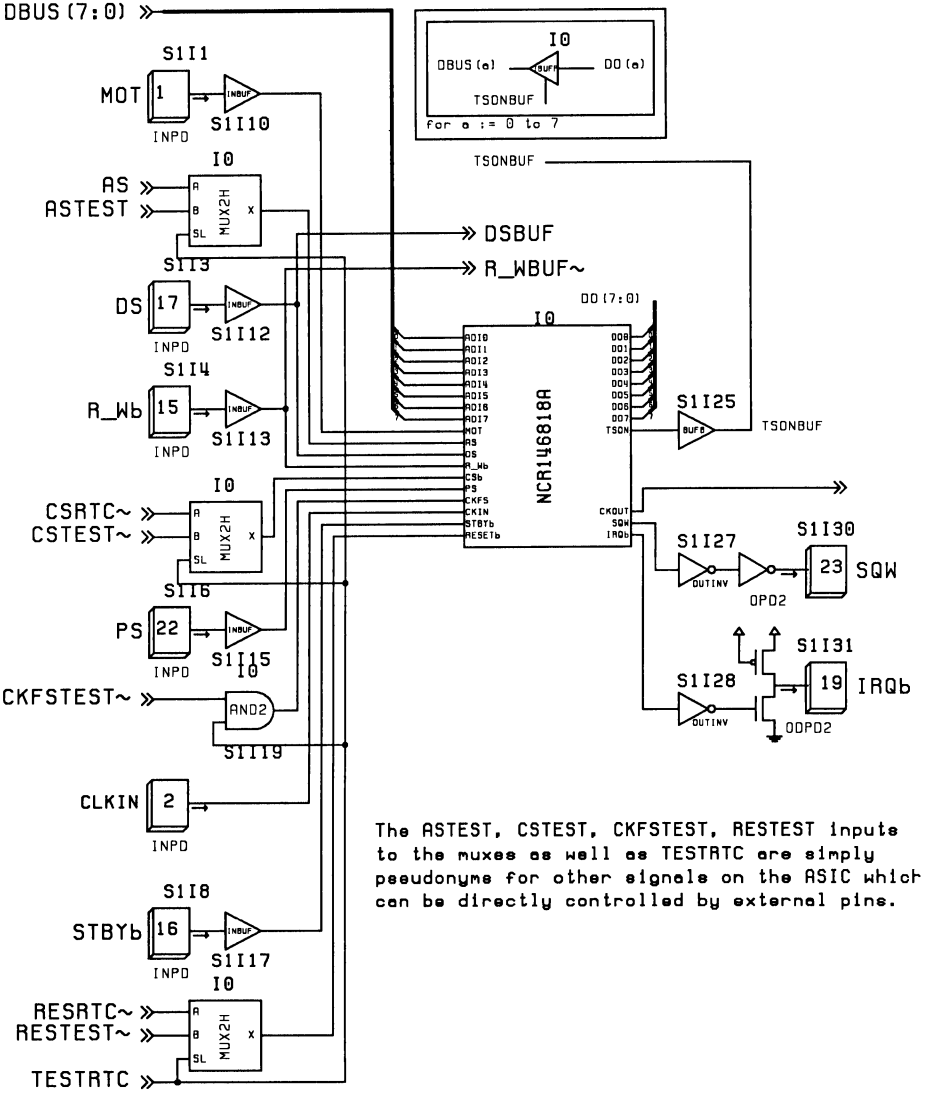


Figure 8–2 Test connect example

AC Characteristics

AC Characteristics Exceptions

- **Chip Select Hold Time after DS, WRb, or RDb**
  The standard data sheet specifies 0 nanoseconds, minimum, for this quantity when V_{DD} = 5.0 volts ± 10%. The NCR146818A supports a Chip Select hold time of 10 nanoseconds, minimum under the same voltage conditions.

- **Peripheral Output Data Delay Time from DS/E or RDb**
  The standard data sheet specifies 20 nanoseconds, minimum, for this quantity when V_{DD} = 5.0 volts ± 10%. The NCR146818A supports a Peripheral Output Data delay time of 0 nanoseconds, minimum under ths same voltage conditions.

Timing Requirements

These timings are derived from the prelayout estimated capacitances. Post layout timing variations may occur.

Temperature and Voltage Range = 0°C to 70°C, VCC = 5 V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
t_{cyc}	Cycle Time	165	DC	ns	
t_{ewl}	Pulse Width, DS/E Low or RDb/WRb High	120	–	ns	
t_{ewh}	Pulse Width, DS/E High or RDb/WRb Low	45	–	ns	
t_r, t_f	Input Rise and Fall Time	–	30	ns	
t_{rwhd}	R/Wb Hold Time	5	–	ns	
t_{rwsu}	R/Wb Setup Time before DS/E	10	–	ns	
t_{cssu}	Chip Select Setup Time before DS, WRb, or RDb	5	–	ns	
t_{cshd}	Chip Select Hold Time	10	–	ns	Note 1
t_{wdhd}	Write Data Hold Time	0	–	ns	
t_{masu}	Muxed Address Valid Time to AS/ALE Fall	30	–	ns	
t_{mahd}	Muxed Address Hold Time	0	–	ns	
t_{ead}	Delay Time DS/E to AS/ALE Rise	50	–	ns	
t_{awh}	Pulse Width, AS/ALE High	65	–	ns	
t_{aed}	Delay Time AS/ALE to DS/E Rise	35	–	ns	
t_{wdsu}	Peripheral Data Setup Time	30	–	ns	
t_{sbsu}	STBYb Setup Time before AS/ALE Rise	5	–	ns	
t_{sbhd}	STBYb Hold Time after AS/ALE Rise	15	–	ns	

Note 1: See the section on AC Characteristics Exceptions for Chip Select Hold Time.

Timing Responses

Temperature and Voltage Range = 0°C to 70°C, VCC = 5 V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
T_{rdhd}	Read Data Hold Time	10	65	ns	Note 1
T_{rdd}	Peripheral Output Data Delay Time from DS/E or RDb	0	25	ns	Notes 1, 2

Note 1: External loading of 1.0 pF used for test case, macrocell only.
Note 2: See the section on AC Characteristics Exceptions for Peripheral Output Data Delay Time.

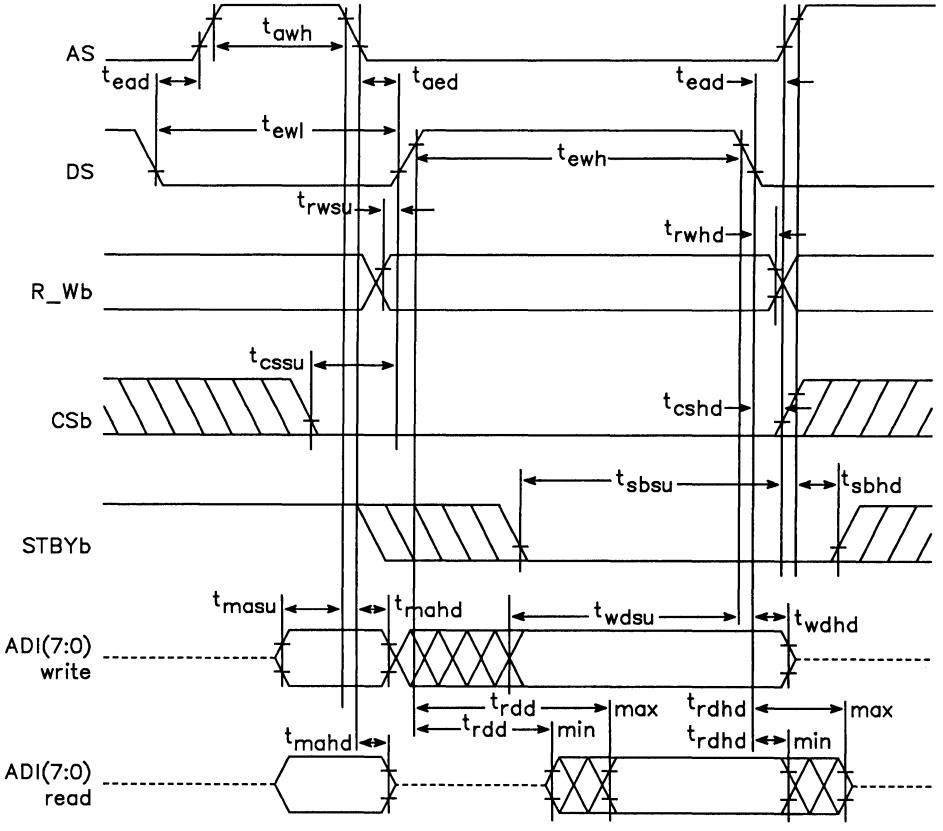


Figure 8–3 Motorola compatible bus timing

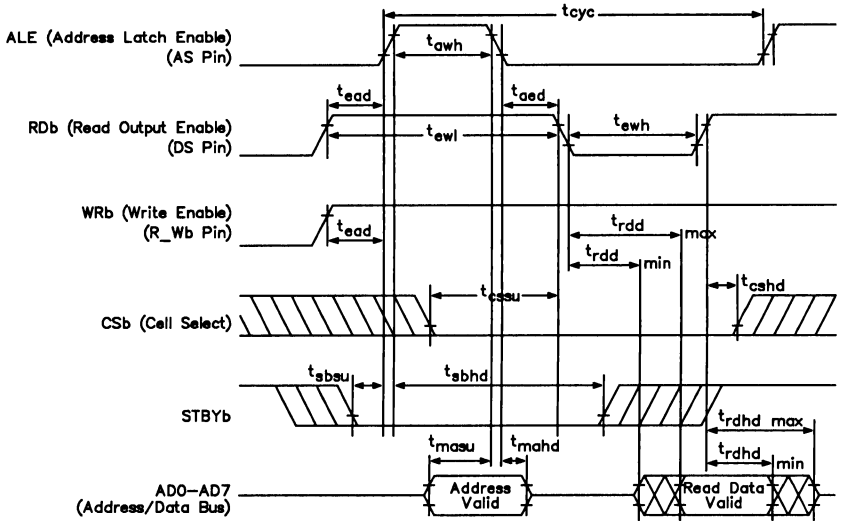


Figure 8–4 INTEL compatible bus timing – Read

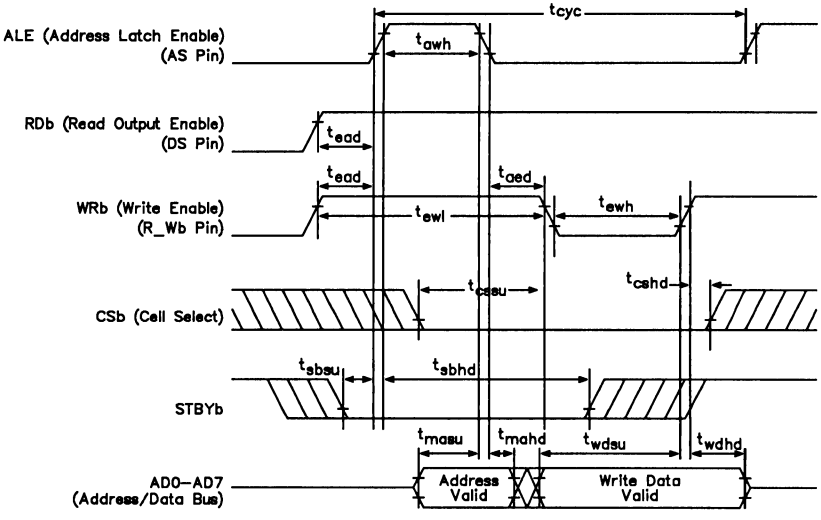


Figure 8–5 INTEL compatible bus timing – Write

NCR16C450

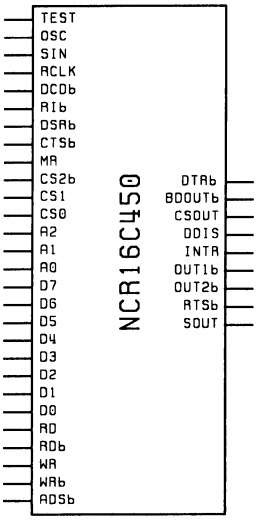
Universal Asynchronous Receiver/Transmitter

Description

- Industry standard 16C450 function
- Programmable character length, parity, stop bits, and baud rate
- Modem controls and prioritized interrupts
- Improved timing in VS700
- Added to design as a single block
- Simulated and routed as individual cells for maximum flexibility

The NCR16C450 is a macrocell designed using the NCR Standard Cell Library to duplicate the function of the industry standard 16C450 UART. The NCR16C450 UART converts parallel data to standard serial format for transmission and converts incoming serial data to parallel format upon reception. The UART can be added to the design using the provided symbol. When the design is expanded, the NCR16C450 will consist only of NCR standard cells. NCR development tools are available for use on the entire design. The use of a lower case "b" at the end of a pin name indicates that the signal is asserted low.

Symbol



VS700 Cell count: 628
Equivalent gate count: 1694
VS1500F Cell count: 628
Equivalent gate count: 1900

Inputs/Outputs

Definitions of the NCR16C450 inputs and outputs are given in the following table.

Pin Name	Type	Description
CS2b, CSI, CS0	I	CELL SELECT: When CS2b is low, CS1 is high, and CS0 is high; the cell is enabled for reading and writing data. The rising edge of ADSb may be used to latch the cell select inputs.
A2, A1, A0	I	REGISTER ADDRESS: These three address inputs are used to select the desired UART registers for reading or writing data. ADSb may be used to latch the address inputs.
RD, RDb	I	READ CONTROL: When the cell is selected and either RD is high or RDb is low, data will be read from the addressed register.
WR, WRb	I	WRITE CONTROL: When the cell is selected and either WR is high or WRb is low, data will be written to the addressed register.

(Sheet 1 of 2)

Pin Name	Type	Description
ADSb	I	ADDRESS STROBE: The rising edge of ADSb latches the cell select and address inputs. When ADSb is low, the cell select and address inputs will propagate through the latches.
SIN	I	SERIAL INPUT: The serial data input to the UART.
RCLK	I	RECEIVER CLOCK: The clock used by the receiver logic. It is 16 times the baud rate.
DCDb	I	DATA CARRIER DETECT: A low indicates that the modem or data set has detected the data carrier.
RIb	I	RING INDICATOR: A low indicates the modem has received a telephone ringing signal.
DSRb	I	DATA SET READY: A low indicates that the modem or data set is ready to establish communications with the UART.
CTSb	I	CLEAR TO SEND: A low indicates that the modem or data set is ready to exchange data.
MR	I	MASTER RESET: When MR is high, the UART is cleared and placed in the standard reset condition.
OSC	I	OSCILLATOR INPUT: Similar to the XIN input of the standard 16C450. However, this signal should come from the output of a OSCP cell or other CMOS compatible cell.
TEST	I	BAUD RATE COUNTER TEST PIN: For test purposes only. When DLAB is set and TEST is high, a read of address 0 will output the complement of the least significant byte of the baud rate counter. A read of address 1 will output the complement of the most significant byte. All other register accesses are inhibited. Tie TEST low for normal operation.
D7–D0	I/O	DATA BUS: An eight–bit bidirectional data bus used to transfer data to and from the UART.
SOUT	O	SERIAL OUTPUT: The serial data output from the transmitter to the communications link.
INTR	O	INTERRUPT: A high INTR indicates that an enabled interrupt is pending.
BDOUTb	O	BAUD OUT: This is the clock used by the transmitter logic and is 16 times the baud rate.
DDIS	O	DRIVER DISABLE: When DDIS is low, data is being read from the UART.
CSOUT	O	CELL SELECT OUT: When CSOUT is high, the UART cell is selected and data bus transfers are enabled.
DTRb	O	DATA TERMINAL READY: When DTRb is low, the UART is ready to establish a communication link.
RTSb	O	REQUEST TO SEND: When RTSb is low, the UART is ready to exchange data.
OUT1b	O	OUTPUT 1: OUT1b will go low when bit 2 of the MCR is programmed high.
OUT2b	O	OUTPUT 2: OUT2b will go low when bit 3 of the MCR is programmed high.

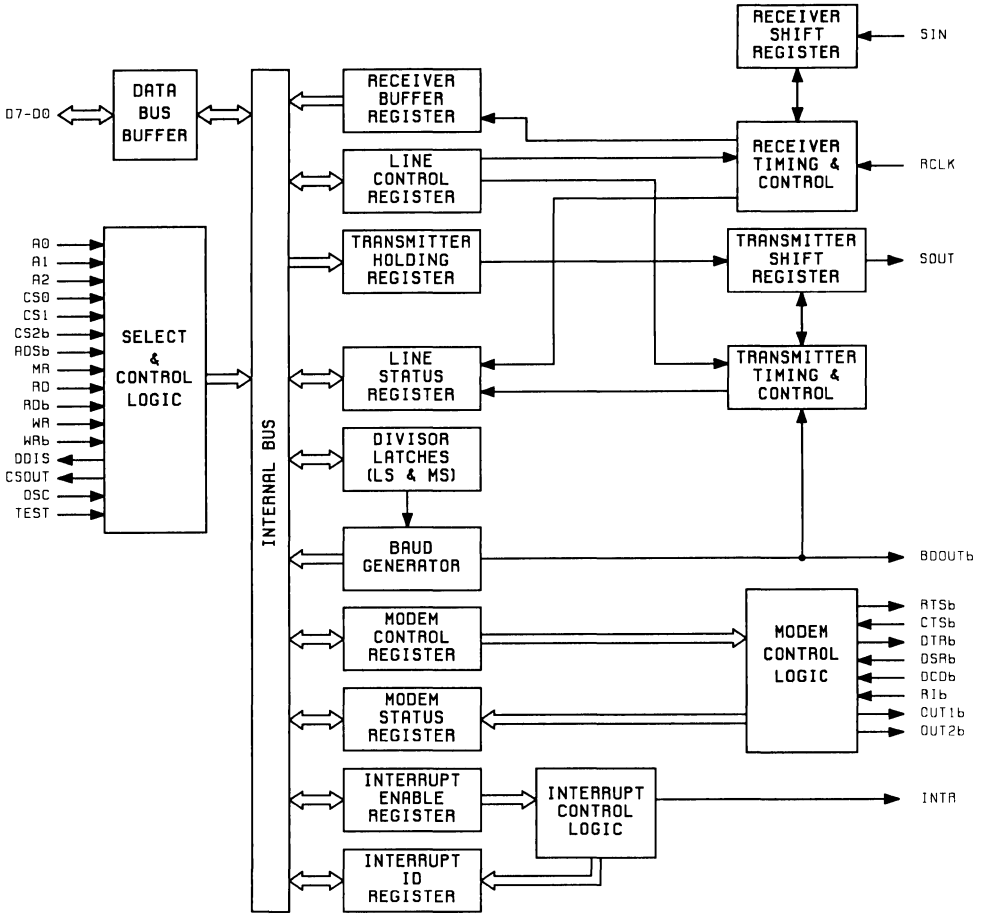
(Sheet 2 of 2)

Input Signal Capacitance		
PIN	**VS1500F**	**VS700**
TEST	0.06 pF	0.03 pF
OSC	0.11 pF	0.06 pF
SIN	0.09 pF	0.05 pF
RCLK	0.16 pF	0.10 pF
DCDb	0.09 pF	0.05 pF
RIb	0.09 pF	0.05 pF
DSRb	0.09 pF	0.05 pF
CTSb	0.09 pF	0.05 pF
MR	0.16 pF	0.10 pF
CS2b	0.06 pF	0.03 pF
CS1	0.09 pF	0.06 pF
CS0	0.09 pF	0.06 pF
A2	0.06 pF	0.03 pF
A1	0.06 pF	0.03 pF
A0	0.06 pF	0.03 pF
RD	0.06 pF	0.03 pF
RDb	0.16 pF	0.10 pF
WR	0.06 pF	0.03 pF
WRb	0.16 pF	0.10 pF
ADSb	0.06 pF	0.04 pF
D7–D0	0.23 pF	0.10 pF

Output Signal Drive Capability		
PIN	**VS1500F**	**VS700**
D7–D0	TBUF	TBUF
DTRb	NAN2H	NAN2H
BDOUTb	INVH	INVH
CSOUT	INV3	INV3
DDIS	INV3	INV3
INTR	MBUF	MBUF
OUT1b	NAN2H	NAN2H
OUT2b	NAN2H	NAN2H
RTSb	NAN2H	NAN2H
SOUT	INVH	INVH

NOTE: Input signal capacitance consists of cell input capacitance only. Routing capacitance is not included since the routing will be different for each usage of the soft macrocell.

Functional Block Diagram



SUPERCELLS

Bit No.	Register Address										
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Bit 0 (Least Significant Bit)	Bit 0	Received Data Available	"0" if Interrupt Pending	Word Length Select Bit 0	Data Terminal Ready	Data Ready	Delta Clear to Send	Bit 0	Bit 0	Bit 8
1	Bit 1	Bit 1	Transmitter Holding Register Empty	Interrupt ID Bit (0)	Word Length Select Bit 1	Request to Send	Overrun Error	Delta Data Set Ready	Bit 1	Bit 1	Bit 9
2	Bit 2	Bit 2	Receiver Line Status	Interrupt ID Bit (1)	Number of Stop Bits	Out 1	Parity Error	Trailing Edge Ring Indicator	Bit 2	Bit 2	Bit 10
3	Bit 3	Bit 3	MODEM Status	0	Parity Enable	Out 2	Framing Error	Delta Data Carrier Detect	Bit 3	Bit 3	Bit 11
4	Bit 4	Bit 4	0	0	Even Parity Select	Loop	Break Interrupt	Clear to Send	Bit 4	Bit 4	Bit 12
5	Bit 5	Bit 5	0	0	Stick Parity	0	Transmitter Holding Register	Data Set Ready	Bit 5	Bit 5	Bit 13
6	Bit 6	Bit 6	0	0	Set Break	0	Transmitter Empty	Ring Indicator	Bit 6	Bit 6	Bit 14
7	Bit 7	Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect	Bit 7	Bit 7	Bit 15

Application Notes

Primary Uses

The NCR16C450 interfaces with the system CPU and a serial port to provide parallel/serial conversion. The NCR16C450 UART receives serial data from a MODEM or peripheral device, checks for error conditions, deletes the standard asynchronous protocol bits, and performs the serial to parallel conversion. The UART also accepts parallel data from the CPU, performs the parallel to serial conversion, inserts the proper asynchronous protocol bits, and transmits the result.

The NCR16C450 is fully programmable and allows complete status reporting. A 16-bit programmable baud rate generator is included as well as MODEM controls and interrupt capability.

Design Information

The NCR16C450 is designed to duplicate the function of the industry standard part. Detailed information can be found in any 16C450 standard device data sheet. A few notes on designing with the NCR16C450 are given below.

OSC input: This signal is similar to the XIN input on the standard part. However, if a crystal oscillator is desired, use a OSCP cell for the crystal connections and feed the output of the OSCP cell to the OSC input of the NCR16C450.

MR input: The NCR16C450 macro cell does not contain a Schmitt trigger. If a slow rise/fall time or an unstable signal is expected on the Master Reset, a Schmitt trigger cell should be used between the external pad and the MR input.

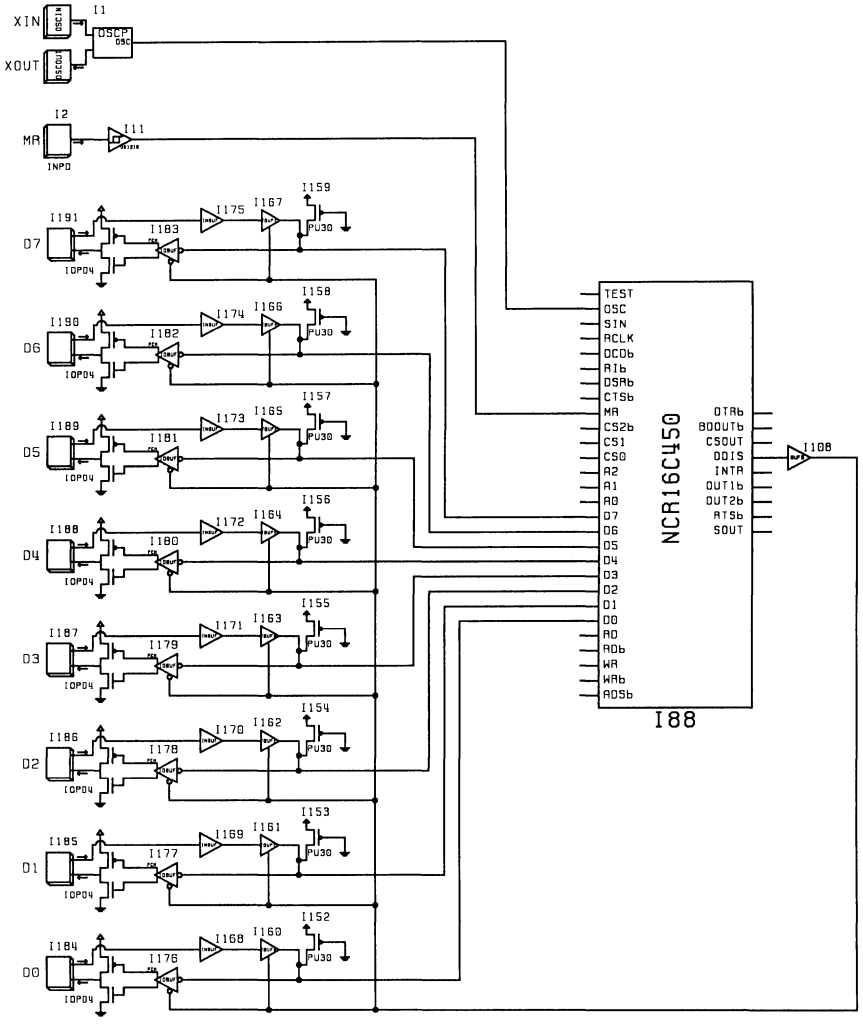
TEST input: A test pin is included on the NCR16C450 UART to allow better testability of the Baud Rate Generator. See INPUTS/OUTPUTS section for details. Tie TEST low for normal operations.

D0-D7 bidirectional bus: The data bus does not have pull-ups (PU30s) or pull-downs (PD30s) internal to the macrocell. They must be added external to the macrocell to prevent excessive current draw. (See Integration Example.)

All inputs and outputs are not buffered for off-chip interfacing. Buffering must be provided by the designer.

Integration Example

The following is an example of how the NCR16C450 macrocell could be interfaced to off-chip circuitry.



Macro OSC, MR, and data bus interface to I/O pads

AC Characteristics

The following timing parameters apply strictly to VS700 macrocell. The VS1500F macrocell will comply with standard part timings only. These timings are derived from prelayout estimated capacitances. Postlayout timing variations may occur.

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
t_{asw}	Address strobe width	25		ns	
t_{aht}	Address hold time	0		ns	
t_{ar}	RD, RDb delay from address	30		ns	See Note 1
t_{ast}	Address setup time	30		ns	
t_{aw}	WR, WRb delay from address	30			See Note 1
t_{cht}	Cell select hold time	0		ns	
t_{cst}	Cell select setup time	30		ns	
t_{csd}	Cell select output delay from select		50	ns	@ 1pF loading (See Note 1)
t_{cr}	RD, RDb delay from cell select	30		ns	See Note 1
t_{cw}	WR, WRb delay from cell select	30		ns	See Note 1
t_{dh}	Data hold time	10		ns	
t_{ds}	Data setup time	20		ns	
t_{df}	RD, RDb to floating data delay	0	20	ns	@ 1pF loading
t_{res}	Master reset pulse width	100		ns	
t_{ra}	Address hold time from RD, RDb	10		ns	See Note 1
t_{rd}	Read cycle delay	30		ns	
t_{rcs}	Cell select hold time from RD, RDb	10		ns	See Note 1
t_{rs}	RD, RDb strobe width	30		ns	
t_{dd}	RD, RDb to driver disable delay		15	ns	@ 1pF loading
t_{rdv}	Delay from RD, RDb to data		30	ns	@ 1pF loading
t_{wah}	Address hold time from WR, WRb	10		ns	See Note 1
t_{wd}	Write cycle delay	30		ns	
t_{wcs}	Cell select hold time from WR, WRb	10		ns	See Note 1
t_{ws}	WR, WRb strobe width	30		ns	
t_{kh}	Duration of clock high pulse	40		ns	
t_{kl}	Duration of clock low pulse	40		ns	
t_{rc}	Read cycle = $t_{ar} + t_{rs} + t_{rd}$	90		ns	
t_{wc}	Write cycle = $t_{aw} + t_{ws} + t_{wd}$	90		ns	

Note 1: Timing parameter applies only when ADSb is held low.

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
Baud Generator					
N	Baud divisor	1	$2^{16}-1$		
t_{ped}	Baud output positive edge delay		20	ns	1 pF load
t_{ned}	Baud output negative edge delay		20	ns	1 pF load
t_{ht}	Baud output high time	300		ns	f_x = 3 MHz÷3, 1 pF load
t_{lt}	Baud output low time	470		ns	f_x = 2 MHz÷2, 1 pF load
Receiver					
t_{dri}	Delay from RD, RDb (RD RBR or RD LSR) to reset interrupt		30	ns	1 pF load
t_{dsc}	Delay from RCLK to sample time		20	ns	
t_{dsi}	Delay from stop to set interrupt		1	RCLK cycles	See Note 1
Transmitter					
t_{dwr}	Delay from WR, WRb (WR THR) to reset interrupt		40	ns	1 pF load
t_{ir}	Delay from RD, RDb (RD IIR) to reset interrupt (THRE)		30	ns	1 pF load
t_{drt}	Delay from initial INTR reset to transmit start	24	40	BAUDOUT cycles	
t_{dwi}	Delay from initial write to interrupt	16	24	BAUDOUT cycles	
t_{sti}	Delay from stop to interrupt (THRE)	8	8	BAUDOUT cycles	
Modem Control					
t_{dwo}	Delay from WR, WRb (WR MCR) to output		20	ns	1 pF load
t_{dir}	Delay to reset interrupt from RD RDb (RD MSR)		30	ns	1 pF load
t_{sim}	Delay to set interrupt from MODEM input		30	ns	1 pF load

Note 1: RCLK is equal to t_{kh} and t_{kl}

Timing Waveforms (All timings are referenced to valid 0 and valid 1)

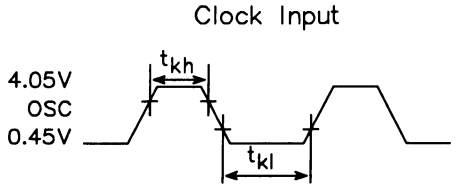


Figure 8-6

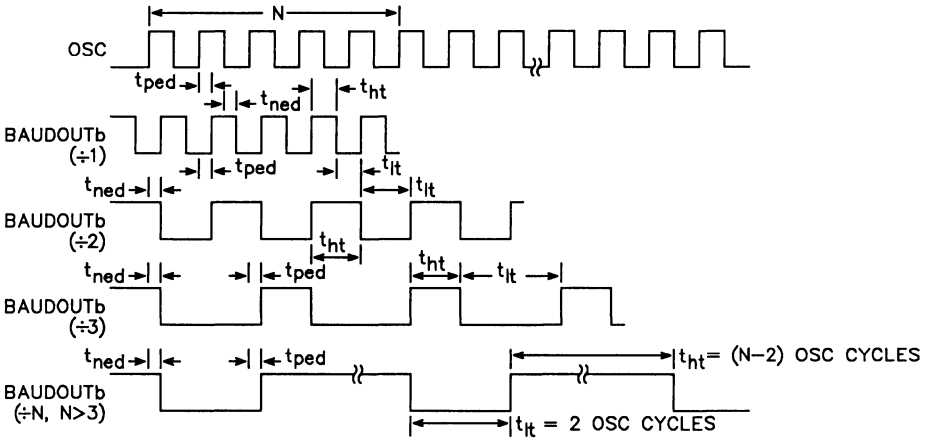
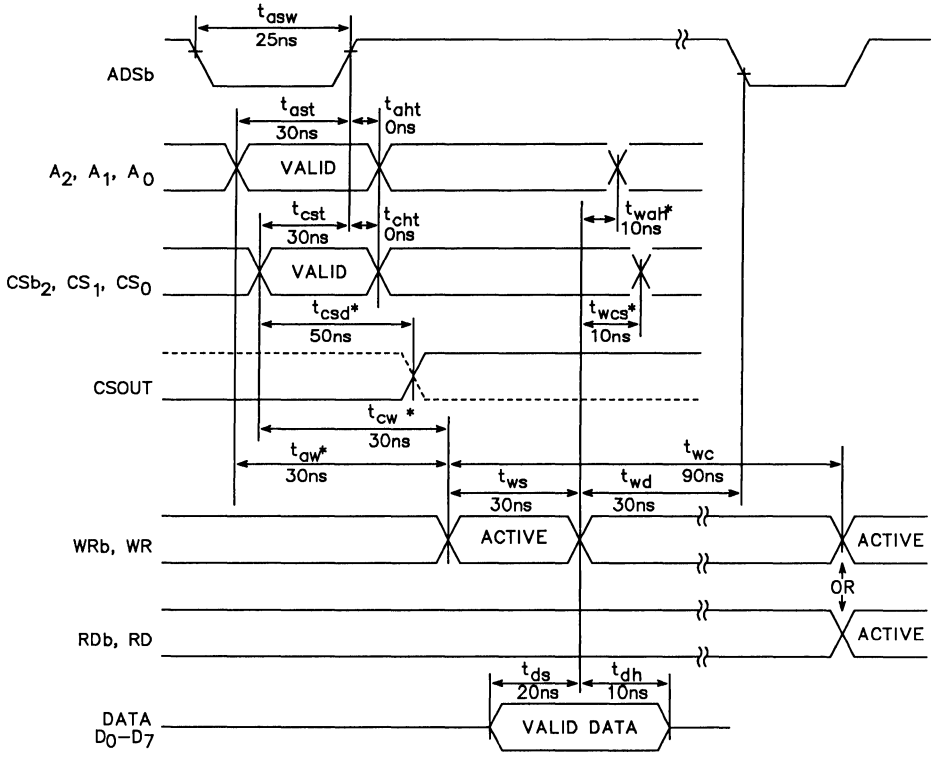


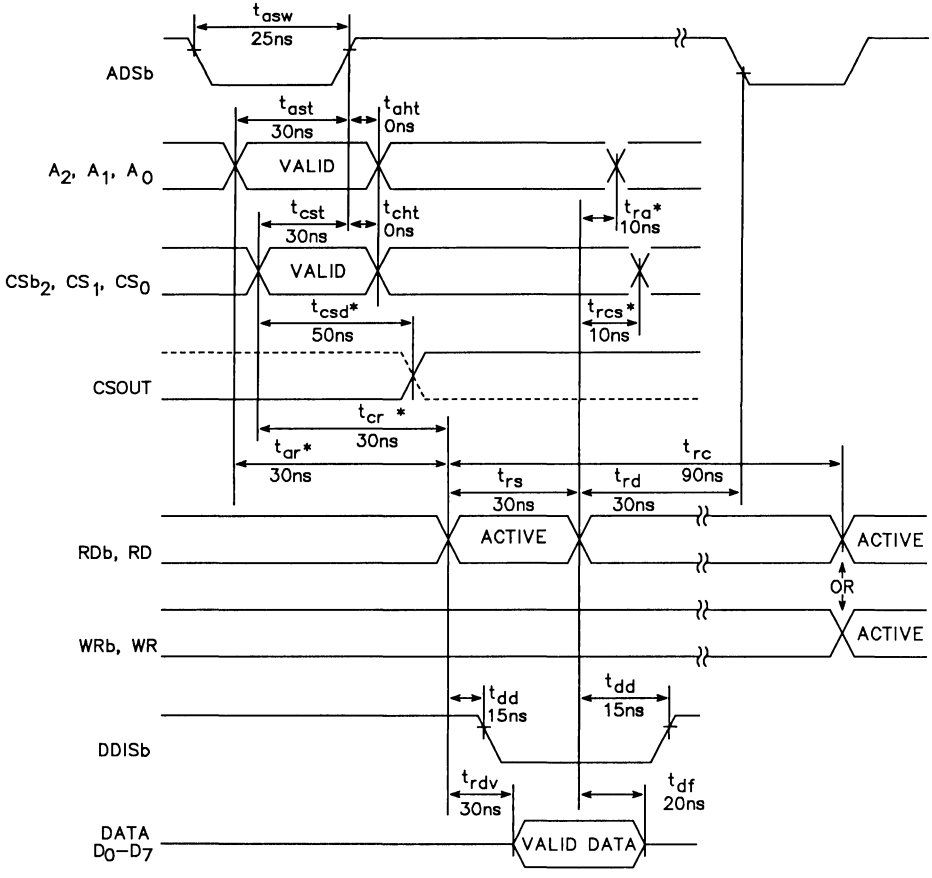
Figure 8-7 BAUDOUT timing

SUPERCELLS



* Timing parameter applies only when ADSb is held low.

Figure 8–8 Write cycle



*Timing parameter applies only when ADSb is held low.

Figure 8-9 Read cycle

SUPERCELLS

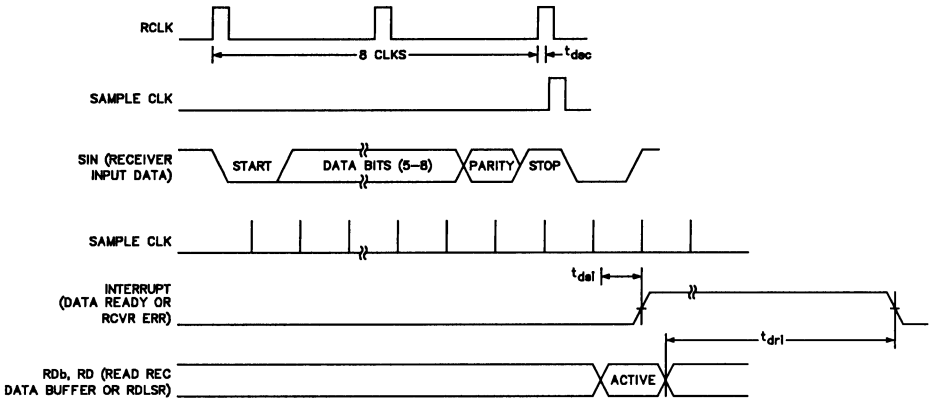


Figure 8–10 Receiver timing

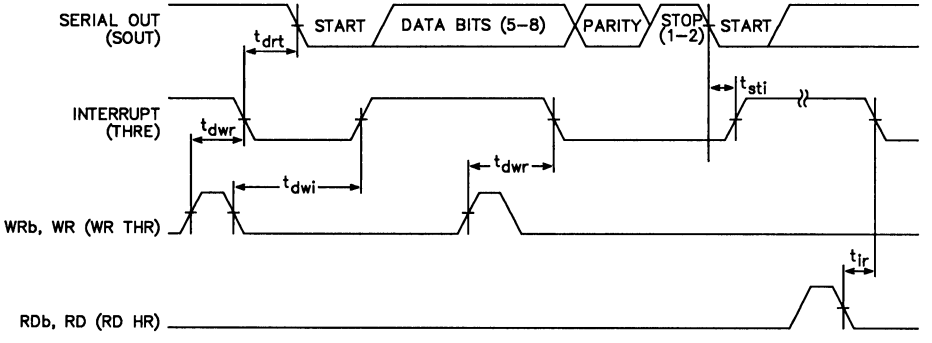


Figure 8–11 Transmitter timing

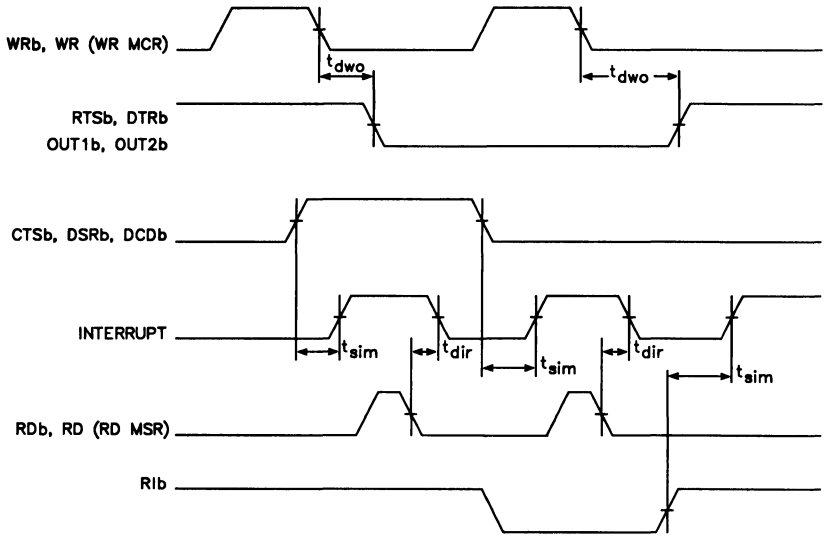


Figure 8–12 MODEM controls timing

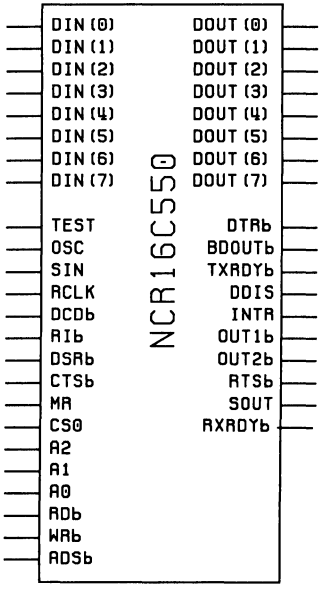
Universal Asynchronous Receiver/Transmitter with FIFOs

Description

- Industry standard 16C550 function
- Programmable character length, parity, stop bits, and baud rate
- Modem controls and prioritized interrupts
- 12 MHz capability
- Added to design as a single block
- Simulated and routed as individual cells for maximum flexibility

The NCR16C550 is a macrocell designed using the NCR Standard Cell Library to duplicate the function of the industry standard 16C550 UART. The NCR16C550 UART converts parallel data to standard serial format for transmission and converts incoming serial data to parallel format upon reception. The NCR16C550 features the FIFO mode in which internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data/byte in the receiver) to be stored in both receive and transmit operations. The UART can be added to the design using the provided symbol. When the design is expanded, the NCR16C550 will consist only of NCR standard cells. NCR development tools are available for use on the entire design. The use of a lower case "b" at the end of a pin name indicates that the signal is asserted low.

Symbol



VS700 Cell count: 1411
Equivalent gate count: 4155

Inputs/Outputs

Definitions of the NCR16C550 inputs and outputs are given in the following table.

Pin Name	Type	Description
CS0	I	CELL SELECT: When CS0 is high; the cell is enabled for reading and writing data. The rising edge of ADSb may be used to latch the cell select inputs.
A2, A1, A0	I	REGISTER ADDRESS: These three address inputs are used to select the desired UART registers for reading or writing data. ADSb may be used to latch the address inputs.
RDb	I	READ CONTROL: When the cell is selected and RDb is low, data will be read from the addressed register.
WRb	I	WRITE CONTROL: When the cell is selected and WRb is low, data will be written to the addressed register.
ADSb	I	ADDRESS STROBE: The rising edge of ADSb latches the cell select and address inputs. When ADSb is low, the cell select and address inputs will propagate through the latches.
SIN	I	SERIAL INPUT: The serial data input to the UART.
RCLK	I	RECEIVER CLOCK: The clock used by the receiver logic. It is 16 times the baud rate.
DCDb	I	DATA CARRIER DETECT: A low indicates that the modem or data set has detected the data carrier.
RIb	I	RING INDICATOR: A low indicates the modem has received a telephone ringing signal.
DSRb	I	DATA SET READY: A low indicates that the modem or data set is ready to establish communications with the UART.
CTSb	I	CLEAR TO SEND: A low indicates that the modem or data set is ready to exchange data.
MR	I	MASTER RESET: When MR is high, the UART is cleared and placed in the standard reset condition.
OSC	I	OSCILLATOR INPUT: Similar to the XIN input of the standard 16C550. However, this signal should come from the output of a OSCP cell or other CMOS compatible cell.
TEST	I	BAUD RATE COUNTER TEST PIN: For test purposes only. When DLAB is set and TEST is high, a read of address 0 will output the complement of the least significant byte of the baud rate counter. A read of address 1 will output the complement of the most significant byte. All other register accesses are inhibited. Tie TEST low for normal operation. When TEST = 1 the device is in a special test mode used only by the supplied test patterns.
DIN(7 – 0)	I	8-BIT DATA BUS: This is used for transferring data into the UART.
SOUT	O	SERIAL OUTPUT: The serial data output from the transmitter to the communications link.
INTR	O	INTERRUPT: A high INTR indicates that an enabled interrupt is pending, and enabled through the IER.
BDOUTb	O	BAUD OUT: This is the clock used by the transmitter logic and is 16 times the baud rate.

(Sheet 1 of 2)

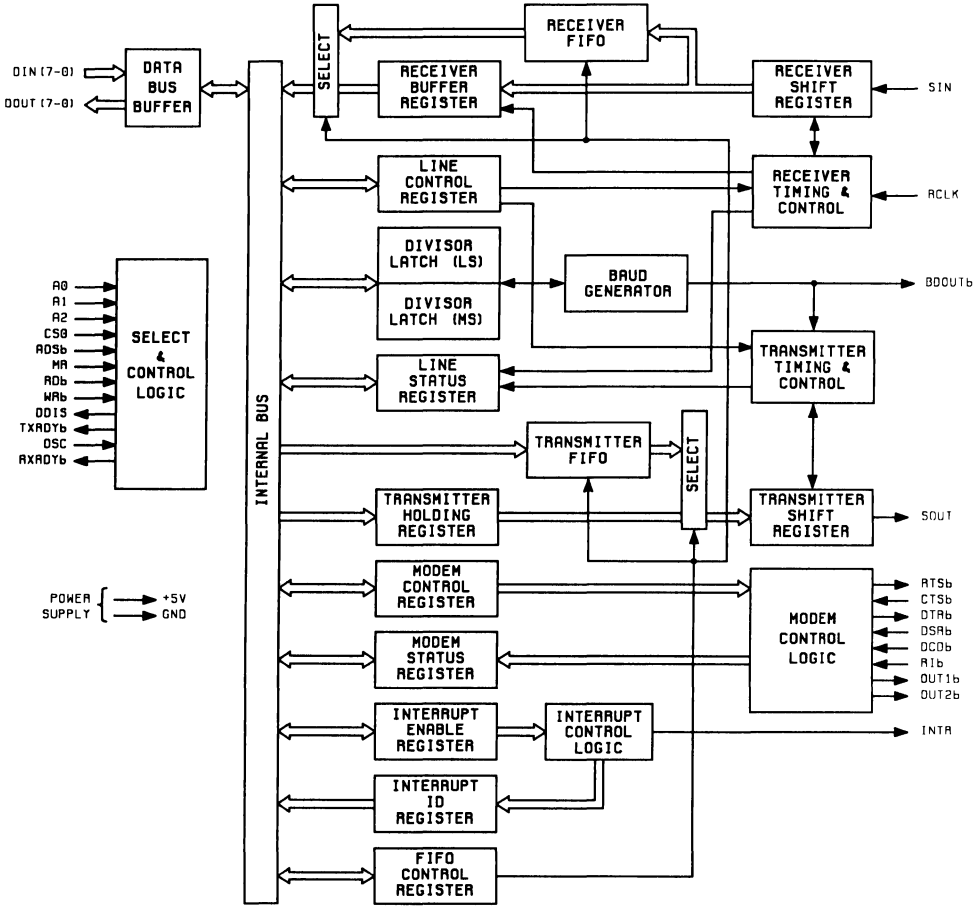
Pin Name	Type	Description
DDIS	O	DRIVER DISABLE: When DDIS is low, data is being read from the UART.
DTRb	O	DATA TERMINAL READY: When DTRb is low, the UART is ready to establish a communication link.
RTSb	O	REQUEST TO SEND: When RTSb is low, the UART is ready to exchange data.
OUT1b	O	OUTPUT 1: OUT1b will go low when bit 2 of the MCR is programmed high.
OUT2b	O	OUTPUT 2: OUT2b will go low when bit 3 of the MCR is programmed high.
DOUT(7 – 0)	O	8–BIT DATA BUS: This is used for transferring data out of the UART.
RXRDYb	O	This pin has 2 modes. When in Mode 0 (16C450 mode), and at least 1 character is in the RCVR FIFO, or RCVR holding register, RXRDY is active low. When in Mode 1 and trigger level or timeout is reached, RXRDY goes active low.
TRXRDYb	O	This pin has 2 modes. When in Mode 0 (16C450) mode), and no characters are in the XMIT FIFO or XMIT holding register, TXRDY goes active low. When in Mode 1, and there is at least one empty location in the XMIT FIFO, TXRDY goes active low.

(Sheet 2 of 2)

Input Signal Capacitance		Output Signal Drive Capability	
TEST	0.035 pF	DOUT7–DOUT0	TBUF
OSC	0.06 pF	DTRb	NAN2H
SIN	0.06 pF	BDOUTb	INVH
RCLK	0.035 pF	DDIS	INV3
DCDb	0.06 pF	INTR	MBUF
RIb	0.06 pF	OUT1b	NAN2H
DSRb	0.06 pF	OUT2b	NAN2H
CTSb	0.06 pF	RTSb	NAN2H
MR	0.035 pF	SOUT	INVH
CSO	0.035 pF	TXRDYb	HBUF
A2	0.035 pF	RXRDYb	HBUF
A1	0.035 pF		
A0	0.035 pF		
RDb	0.035 pF		
WRb	0.035 pF		
ADSb	0.035 pF		
DIN7 – DIN0	0.035 pF		

NOTE: Input signal capacitance consists of cell input capacitance only. Routing capacitance is not included since the routing will be different for each usage of the soft macrocell.

Functional Block Diagram



SUPERCELLS

Bit No.	Register Address											
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Bit 0 (Least Significant Bit)	Bit 0	Enable Received Data Available Interrupt	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Terminal Ready	Data Ready	Delta Clear to Send	Bit 0	Bit 0	Bit 8
1	Bit 1	Bit 1	Enable Transmitter Holding Register Empty Interrupt	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1	Request to Send	Overrun Error	Delta Data Set Ready	Bit 1	Bit 1	Bit 9
2	Bit 2	Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits	Out 1	Parity Error	Trailing Edge Ring Indicator	Bit 2	Bit 2	Bit 10
3	Bit 3	Bit 3	Enable MODEM Status Interrupt	Interrupt ID Bit (2) (Note 1)	DMA Mode Select	Parity Enable	Out 2	Framing Error	Delta Data Carrier Detect	Bit 3	Bit 3	Bit 11
4	Bit 4	Bit 4	0	0	Reserved	Even Parity Select	Loop	Break Interrupt	Clear to Send	Bit 4	Bit 4	Bit 12
5	Bit 5	Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register	Data Set Ready	Bit 5	Bit 5	Bit 13
6	Bit 6	Bit 6	0	FIFOs Enabled (Note 1)	RCVR Trigger	Set Break	0	Transmitter Empty	Ring Indicator	Bit 6	Bit 6	Bit 14
7	Bit 7	Bit 7	0	FIFOS Enabled (Note 1)	RCVR Trigger	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 1)	Data Carrier Detect	Bit 7	Bit 7	Bit 15

Note 1: These bits are always 0 in the NCR16C450 Mode.

Application Notes

Primary Uses

The NCR16C550 interfaces with the system CPU and a serial port to provide parallel/serial conversion. The NCR16C550 UART receives serial data from a MODEM or peripheral device, checks for error conditions, deletes the standard asynchronous protocol bits, and performs the serial to parallel conversion. The UART also accepts parallel data from the CPU, performs the parallel to serial conversion, inserts the proper asynchronous protocol bits, and transmits the result.

The NCR16C550 is fully programmable and allows complete status reporting. A 16-bit programmable baud rate generator is included as well as MODEM controls and interrupt capability.

Design Information

The NCR16C550 is designed to duplicate the function of the industry standard part. Detailed information can be found in any 16C550 standard device data sheet. A few notes on designing with the NCR16C550 are given below.

OSC input: This signal is similar to the XIN input on the standard part. However, if a crystal oscillator is desired, use a OSCP cell for the crystal connections and feed the output of the OSCP cell to the OSC input of the NCR16C550.

MR input: The NCR16C550 macro cell does not contain a Schmitt trigger. If a slow rise/fall time or an unstable signal is expected on the Master Reset, a Schmitt trigger cell should be used between the external pad and the MR input.

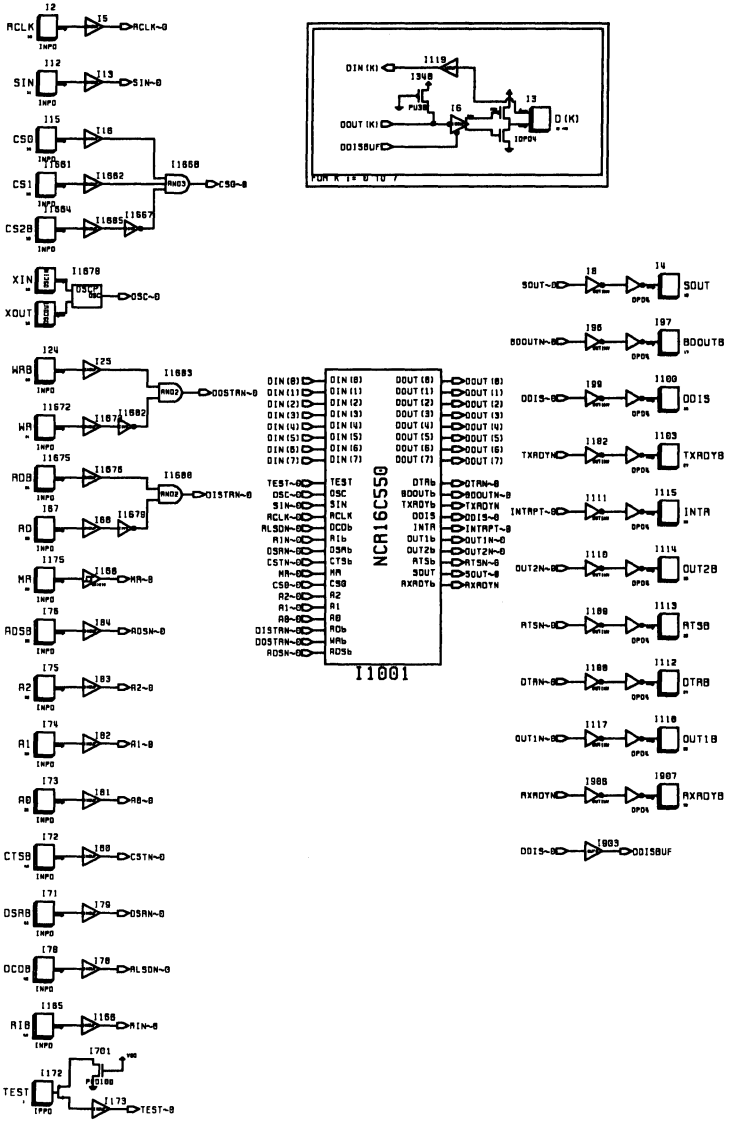
TEST input: A test pin is included on the NCR16C550 UART to allow better testability of the Baud Rate Generator. See INPUTS/OUTPUTS section for details. Tie TEST low for normal operations.

DOUT(0)-DOUT(7) output bus: The data bus does not have pull-ups (PU30s) or pull-downs (PD30s) internal to the macrocell. They must be added external to the macrocell to prevent excessive current draw. (See Integration Example.)

All inputs and outputs are not buffered for off-chip interfacing. Buffering must be provided by the designer.

Integration Example

The following is an example of how the NCR16C550 macrocell could be interfaced to off-chip circuitry.



AC Characteristics

The following timing parameters apply strictly to VS700 macrocell. The VS1500F cell will match standard part timings only. These timings are derived from prelayout estimated capacitances. Postlayout timing variations may occur.

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
t_{asw}	Address strobe width	25		ns	
t_{aht}	Address hold time	0		ns	
t_{ar}	RDb delay from address	30		ns	See Note 1
t_{ast}	Address setup time	30		ns	
t_{aw}	WRb delay from address	30		ns	See Note 1
t_{cht}	Cell select hold time	0		ns	
t_{cst}	Cell select setup time	30		ns	
t_{cr}	RDb delay from cell select	30		ns	See Note 1
t_{cw}	WRb delay from cell select	30		ns	See Note 1
t_{dh}	Data hold time	10		ns	
t_{ds}	Data setup time	20		ns	
t_{df}	RDb to floating data delay	0	20	ns	@ 1pF loading
t_{res}	Master reset pulse width	100		ns	
t_{ra}	Address hold time from RDb	10		ns	See Note 1
t_{rd}	Read cycle delay	30		ns	
t_{rcs}	Cell select hold time from RDb	10		ns	See Note 1
t_{rs}	RDb strobe width	30		ns	
t_{dd}	RDb to driver disable delay		15	ns	@ 1pF loading
t_{rvd}	Delay from RDb to data		30	ns	@ 1pF loading
t_{wah}	Address hold time from WRb	10		ns	See Note 1
t_{wd}	Write cycle delay	30		ns	
t_{wcs}	Cell select hold time from WRb	10		ns	See Note 1
t_{ws}	WRb strobe width	30		ns	
t_{kh}	Duration of clock high pulse	40		ns	
t_{kl}	Duration of clock low pulse	40		ns	
t_{rc}	Read cycle = $t_{ar} + t_{rs} + t_{rd}$	90		ns	
t_{wc}	Write cycle = $t_{aw} + t_{ws} + t_{wd}$	90		ns	

Note 1: Timing parameter applies only when ADSb is held low.

SUPERCELLS

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
Baud Generator					
N	Baud divisor	1	$2^{16}-1$	ns	
t_{ped}	Baud output positive edge delay		20	ns	1 pF load
t_{ned}	Baud output negative edge delay		20	ns	1 pF load
t_{ht}	Baud output high time	100		ns	f_x = 8 MHz÷2, 1 pF load
t_{lt}	Baud output low time	100		ns	f_x = 8 MHz÷2, 1 pF load
Receiver					
t_{dri}	Delay from RDb (RD RBR or RD LSR) to reset interrupt		30	ns	1 pF load
t_{dsc}	Delay from RCLK to sample time		20	ns	
t_{dsi}	Delay from stop to set interrupt		1	RCLK cycles	See Note 1
Transmitter					
t_{dwr}	Delay from WRb (WR THR) to reset interrupt		40	ns	1 pF load
t_{ir}	Delay from RDb (RD IIR) to reset interrupt (THRE)		30	ns	1 pF load
t_{drt}	Delay from initial INTR reset to transmit start	8	24	BAUDOUT cycles	
t_{dwi}	Delay from initial write to interrupt	16	24	BAUDOUT cycles	
t_{sti}	Delay from stop to interrupt (THRE)	8	8	BAUDOUT cycles	
t_{dst}	Delay from start to TXRDY active		8	BAUDOUT cycles	1 pF load
t_{dwt}	Delay from write to TXRDY inactive		25	ns	1 pF load
Modem Control					
dwc_o	Delay from WRb (WR MCR) to output		20	ns	1 pF load
t_{dir}	Delay to reset interrupt from RDb (RD MSR)		30	ns	1 pF load
t_{sim}	Delay to set interrupt from MODEM input		30	ns	1 pF load

Note 1: RCLK is equal to t_{kh} and t_{kl}.

Timing Waveforms (All timings are referenced to valid 0 and valid 1)

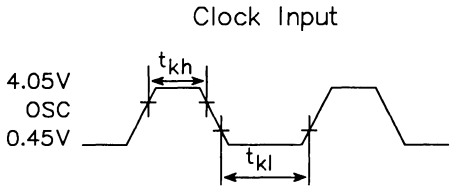


Figure 8-13

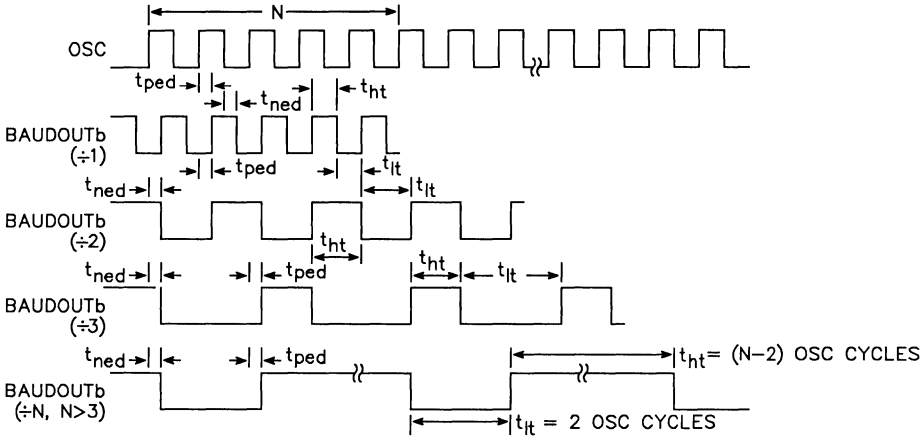
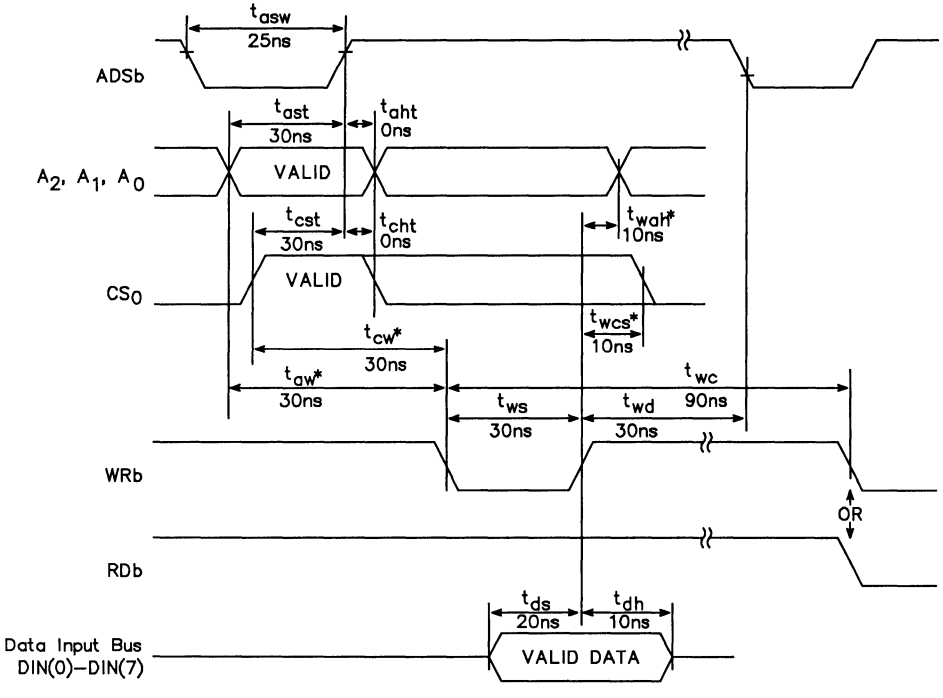
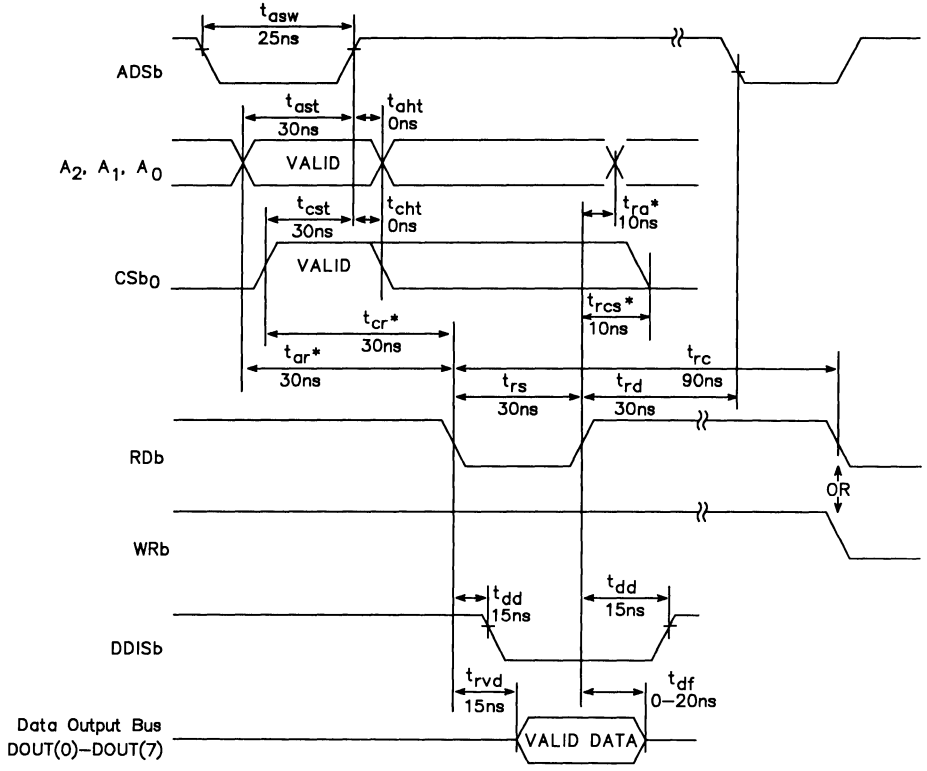


Figure 8-14 BAUDOUT timing



* Timing parameter applies only when ADSb is held low.

Figure 8–15 Write cycle



* Timing parameter applies only when ADSb is held low.

Figure 8–16 Read cycle

SUPERCELLS

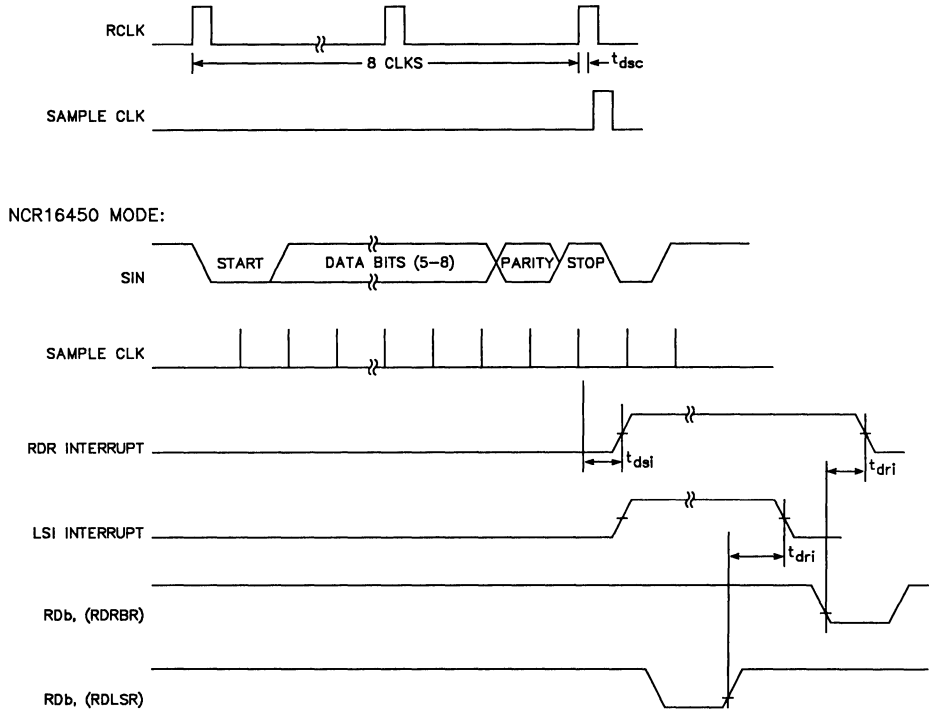


Figure 8–17 Receiver timing

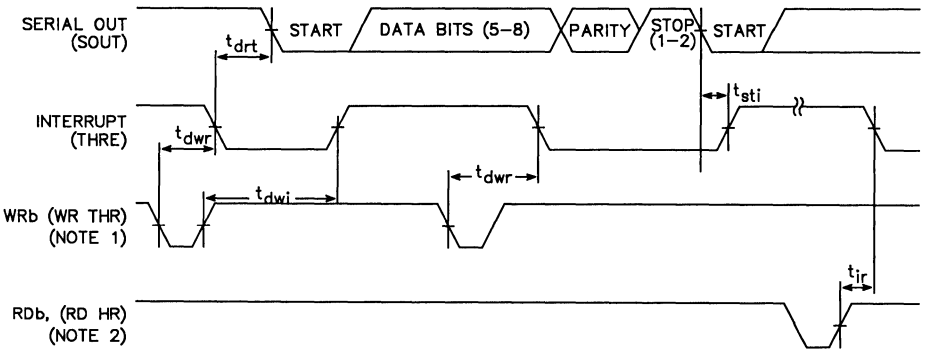


Figure 8–18 Transmitter timing

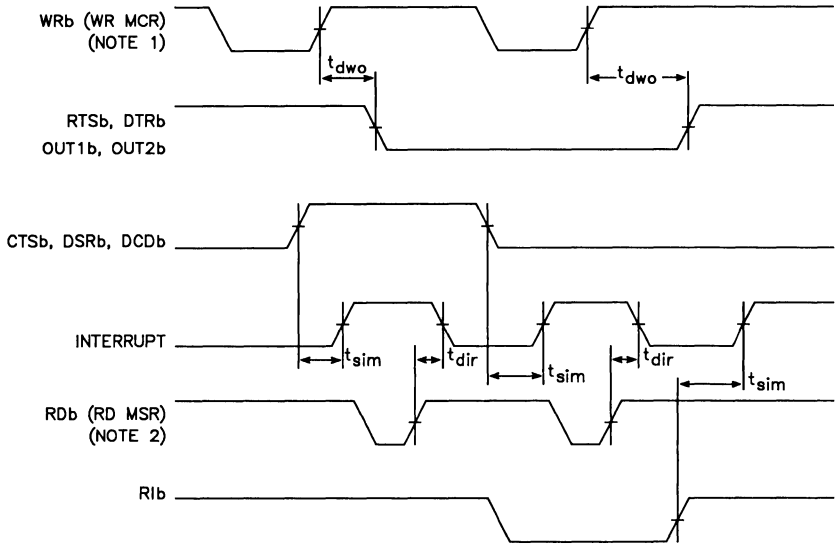


Figure 8–19 MODEM controls timing

Note 1: See Write cycle timing

Note 2: See Read cycle timing

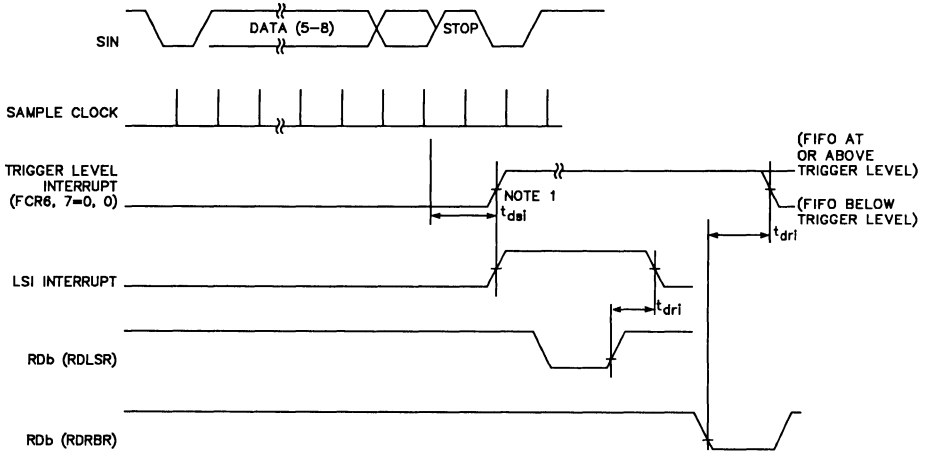


Figure 8–20 RCVR FIFO first byte (This sets RDR)

Note 1: If FCR0 = 1, then t_{dsi} = 3 RCLKs. For a timeout interrupt, t_{dsi} = 8 RCLKs.

SUPERCELLS

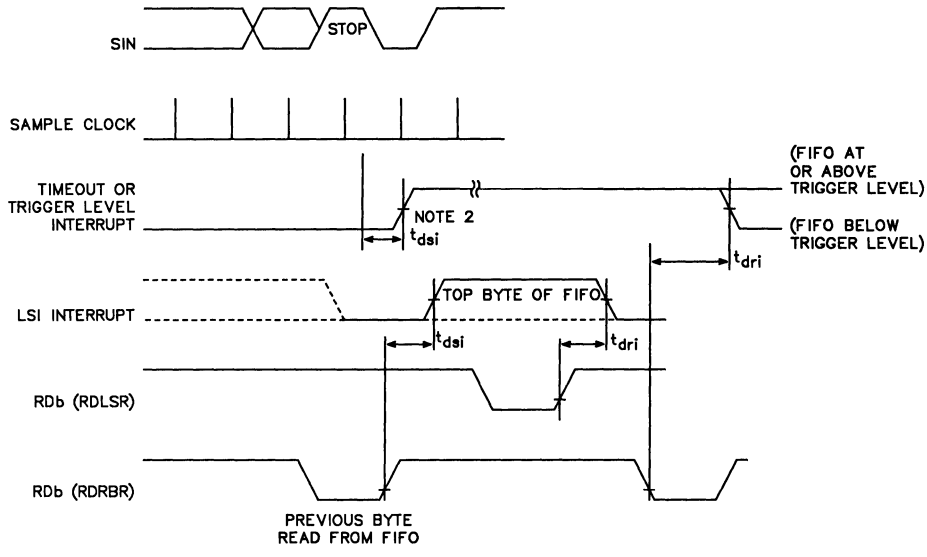


Figure 8-21 RCVR FIFO bytes other than the first byte (RDR is already set)

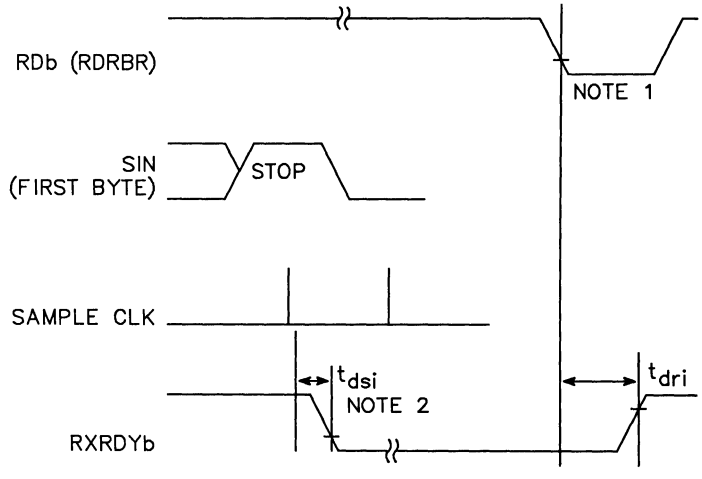


Figure 8-22 Receiver Ready (Pin 29) FCR0=0 or FCR0=1 and FCR3=0 (Mode 0)

Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, then t_{dsi} = 3 RCLKs. For a timeout interrupt, t_{dsi} = 8 RCLKs.

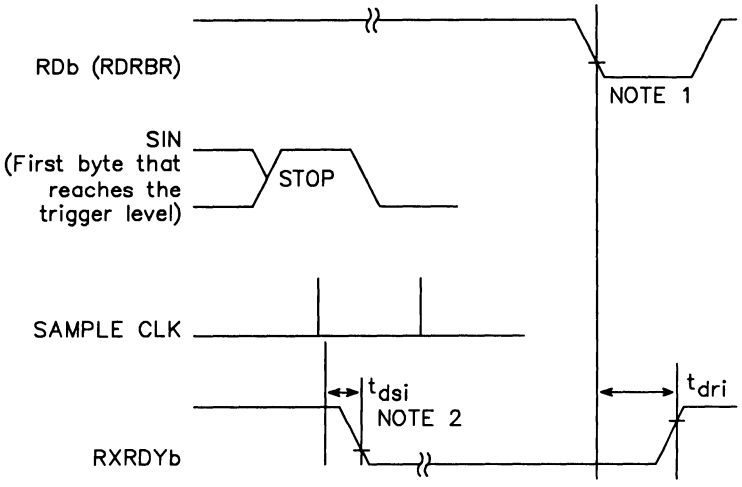


Figure 8-23 Receiver Ready (RXRDYb) FCR0=1 and FCR3=1 (Mode 1)

Note 1: This is the reading of the last byte in the FIFO.
Note 2: If FCR0 = 1, then t_{dsi} = 3 RCLKs.

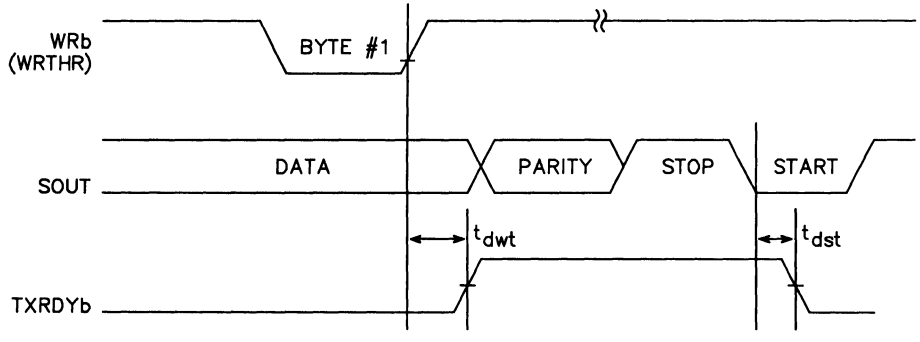


Figure 8-24 Transmitter Ready (TXRDTb) FCR0=0 or FCR0=1 and FCR3=0 (Mode 0)

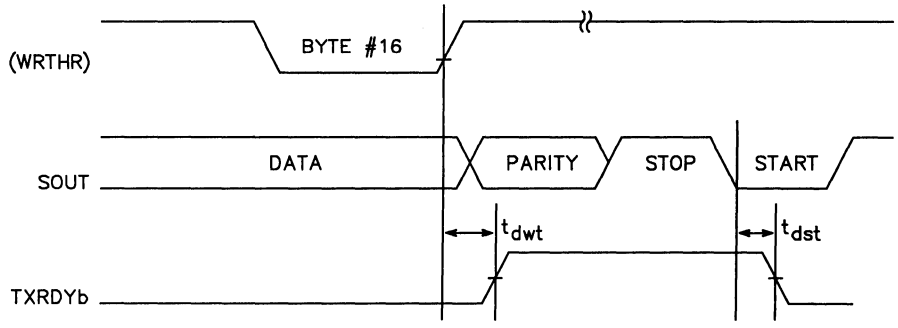


Figure 8-25 Transmitter Ready (TXRDYb) FCR0=1 and FCR3=1 (Mode 1)

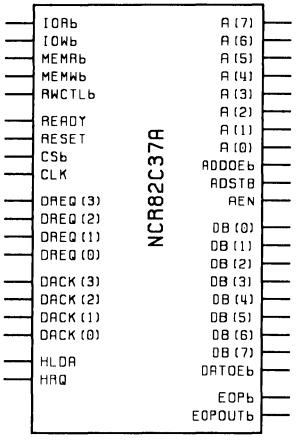
DMA Controller

Description

- Industry standard 8237A function
- Four independent channels
- 5 MHz capability
- Added to ASIC as a single block
- Simulated and routed as individual cells for maximum flexibility

The NCR82C37A is a macrocell designed in the NCR Standard Cell Library to duplicate the function of the industry standard 8237A DMA controller. This NCR Standard Cell Library macrocell may be used the same as any other symbol in the component library to incorporate this function into an ASIC design. When the ASIC design is expanded, the NCR82C37A will consist solely of NCR standard cell library cells. NCR development tools are available for use on the entire design. The use of a lower case "b" at the end of a pin name indicates that the signal is asserted low.

Symbol



VS700 Cell count: 1573
Equivalent gate count: 3691
VS1500F Cell count: 1570
Equivalent gate count: 3321

Inputs/Outputs

Definitions of the NCR82C37A inputs and outputs are given in the following table.

Pin Name	Type	Description
IORb & IOWb	I/O	I/O READ & I/O WRITE: Bidirectional tristate active low. Control lines used during programming operations to read data from or write data to the NCR82C37A. During DMA operations, these lines read data from or write data to the I/O device.
MEMRb & MEMWb	O	MEMORY READ & MEMORY WRITE: Active low outputs. Control lines used in all DMA operations to read data from or write data to memory.
RWCTLb	O	READ/WRITE CONTROL: Active low output. Signal is used to control the direction and state of the drivers which interface to the signals IORb, IOWb, MEMRb, MEMWb. (See "Macro control lines interface to I/O pads" figure for example configuration.)
READY	I	READY: Active high input. Causes NCR82C37A to issue as many wait states as are needed for DMA operations with slower memory and I/O device access times.
RESET	I	RESET: Active high input. Signal activated to reset the NCR82C37A after power-up.

(Sheet 1 of 2)

Pin Name	Type	Description
CSb	I	CHIP SELECT: Active low input. Enables chip for programming operations.
CLK	I	CLOCK: Input. Clocks the NCR82C37A through all internal states.
DREQ(3) – DREQ(0)	I	DMA REQUEST 3,2,1, & 0: Sense of these inputs is programmable. Reset initializes them to active high. Activated by the device requesting direct memory access. Up to four devices can request service with priorities established by the NCR82C37A as programmed.
DACK(3) – DACK(0)	O	DMA ACKNOWLEDGE 3,2,1, & 0: Sense of these inputs is programmable. Reset initializes them to active high. Activated after the NCR82C37A receives HLDA from the CPU to inform the device requesting direct memory access, the request has been granted.
HLDA	I	HOLD ACKNOWLEDGE: Active high input. Received from the CPU indicating the CPU has relinquished control of the bus and control lines to the NCR82C37A. This signal triggers the start of the DMA operation.
HRQ	O	HOLD REQUEST: Active high output. Activated by the NCR82C37A to request the CPU to "hold" so the NCR82C37A can take over as "master" of the bus and control lines.
EOPOUTb	O	END OF PROCESS OUTPUT ENABLE: Active low output. Signal used to control the state of the driver which pulls down the EOPb line. (See "Macro end of process line interface to I/O pad" figure for example configuration).
EOPb	I/O	END OF PROCESS: Bidirectional tristate, active low. As an output, this signal indicates the NCR82C37A has completed a DMA operation. As an input, this signal can be activated to terminate a DMA operation. This signal must be pulled up such that it will stay high unless driven low by the macro or external logic.
DATOEb	O	DATA BUS OUTPUT ENABLE: Active low output. Signal is used to control the direction and state of the drivers which interface to the data bus, DB(7) – DB(0). (See "Macro data lines interface to I/O pads" figure for example configuration.)
DB(7) – DB(0)	I/O	DATA BUS: Bidirectional tristate. Data read or written during programming. High order address during DMA operations. Multiplexed to also temporarily store and output data to be transferred during memory to memory DMA operation.
AEN	O	ADDRESS ENABLE: Active high output. Signal enables the latch containing the high address byte onto the system address bus.
ADSTB	O	ADDRESS STROBE: Active high output. The high order address (A8 – A15) is valid on the data bus, DB(0) – DB(7), at the trailing edge of ADSTB. Used to latch high order address byte.
ADDOEb	O	ADDRESS OUTPUT ENABLE: Active low output. Signal is used to control the direction and state of the drivers which interface to the address bus, A(7) – A(0). (See "Macro address lines interface to I/O pads" figure for example configuration.)
A(0) – A(3)	I/O	ADDRESS (Least Significant Nibble): Bidirectional tristate. Address inputs for reading NCR82C37A during programming. Address outputs during DMA operations.
A(4) – A(7)	O	ADDRESS (Most Significant Nibble): Address outputs during DMA operations.

Input Signal Capacitance

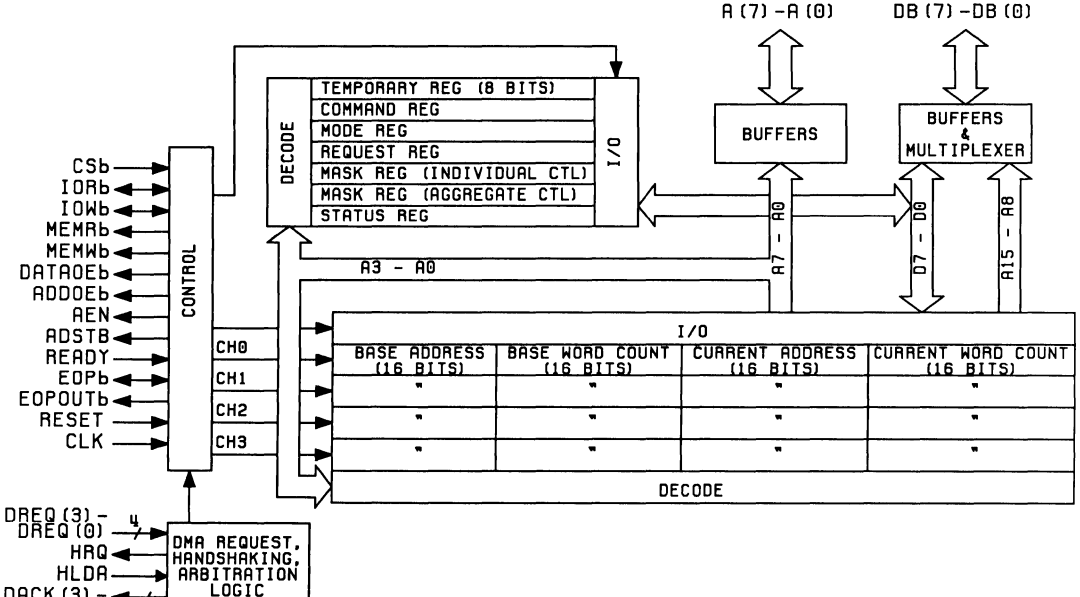
PIN	VS1500F	VS700
IORb	.060 pF	.040 pF
IOWb	.060 pF	,040 pF
READY	.096 pF	.050 pF
RESET	.060 pF	.040 pF
CSb	.060 pF	.060 pF
CLK	.117 pF	.120 pF
DREQ(3) – DREQ(0)	.096 pF	.100 pF
HLDA	.042 pF	.060 pF
EOPb	.202 pF	.050 pF
DB(7) – DB(0)	.183 pF	.210 pF
A(3) – A(0)	.167 pF	.060 pF

Output Signal Drive Capability

PIN	VS1500F	VS700
IORb & IOWb	TBUF	TBUF
MEMRb & MEMWb	TBUF	TBUF
DACK(3) – DACK(0)	EXOR	EXOR
HRQ	CCND	CCND
EOPOUTb	CCND	CCND
EOPb	TBUF	TBUF
DATOEb	NOR2H	NOR2H
DB(7) – DB(0)	TBUF	TBUF
AEN	CCND	CCND
ADSTB	AND2	AND2
ADDOEb	INV3	INV3
A(7) – A(0)	TBUF	TBUF

NOTE: Input signal capacitance consists of cell input capacitance only. Routing capacitance is not included since the routing will be different for each usage of the soft macrocell.

Functional Block Diagram



SUPERCELLS

NCR82C37A

Application Notes

Primary Uses

The NCR82C37A interfaces with the system CPU to execute data transfers, from I/O to memory or from memory to memory, directly without CPU intervention. Transfers can be made from and to any area in the 64K addressing space. The macro contains four independent channels to keep track of up to four I/O to/from memory transfers or two I/O to/from memory transfers and one memory to memory transfer. Several NCR82C37A macros can be cascaded to provide additional channels with the priority handling of multiple DMA requests merged into one network.

The NCR82C37A can be programmed to transfer data by either incrementing or decrementing addresses in three modes:

1. as a block (block mode).
2. as a block in which the transfer can be interrupted and then resumed by the corresponding request input (demand mode).
3. one byte at a time (single mode).

Channels can be programmed to autoinitialize at the completion of a DMA transfer. This allows the transfer to be repeated without reprogramming starting location(s), word count(s), or mode registers. Priority handling of multiple DMA requests is programmable. Cycle timing options are also programmable to increase the data transfer rate (compressed timing) and increase the width of the WRb pulse (extended write).

Design Information

The NCR82C37A is designed to duplicate the function of the industry standard part. Detailed operating information can be found in a standard 8237A device data sheet.

RESET input: This signal must be pulsed high through four clock periods before any other operations can be performed.

PIN 5: Pin 5 of the industry standard 8237A does not affect operation and is recommended tied high by the manufacturers. The NCR82C37A macro does not have this pin.

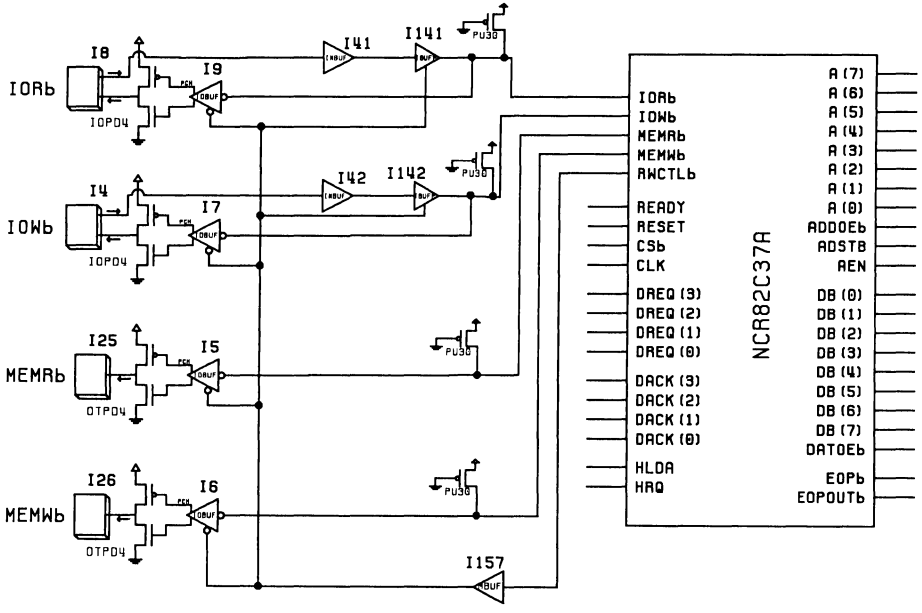
A full logic schematic of the NCR82C37A design can be provided for modification in cases where the designer needs only a portion of the full macrocell. NCR assumes no responsibility for the functionality of a soft macrocell which has been altered in this manner. Please contact your NCR Field Applications Engineer for more information if interested.

Kit Part Exception

The NCR82C37A kit part will not correctly execute memory to memory data transfers. This is due to the fact that the part does not provide the necessary data hold time from the rising edge of MEMWb. See timing specification t_{dvh}. This issue does not apply to the macrocell.

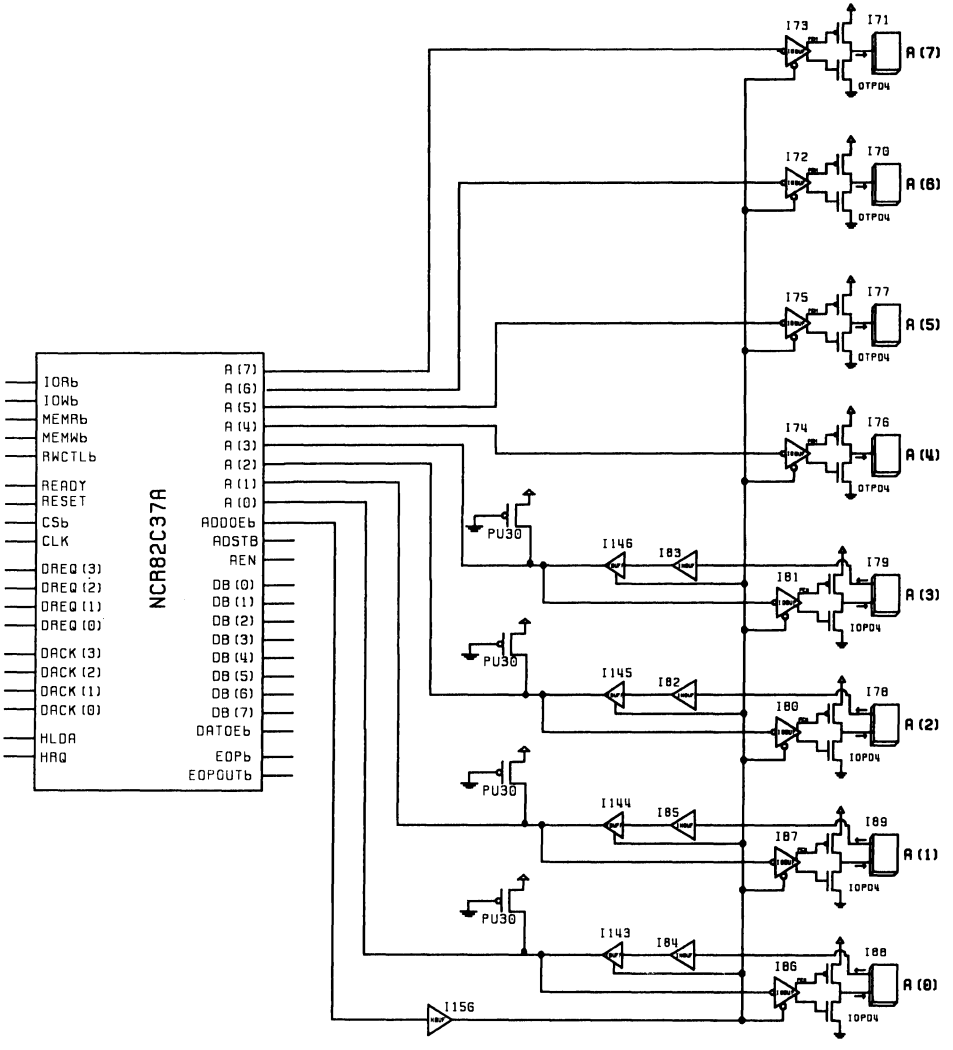
Macro Integration Examples

For maximum integration flexibility, the choice of the type of bidirectional or tristate drivers to interface the macro to on-chip or off-chip circuitry is left to the designer. The drivers are not built-in to the macro. There are also no pullup transistors internal to the macrocell for bidirectional pins. These pullups should be added by the designer in integration. The following four figures are examples of how the macro could be interfaced to off-chip circuitry.

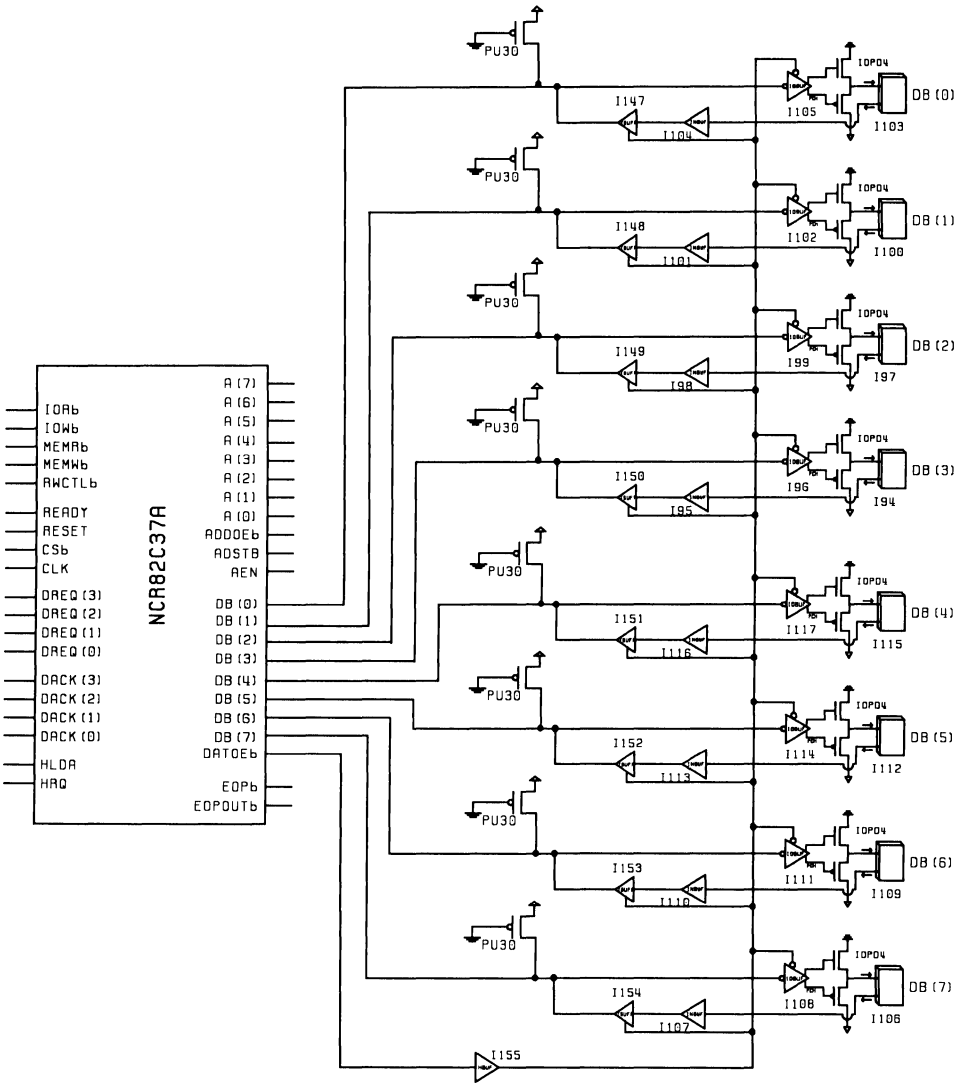


Macro control lines interface to I/O pads

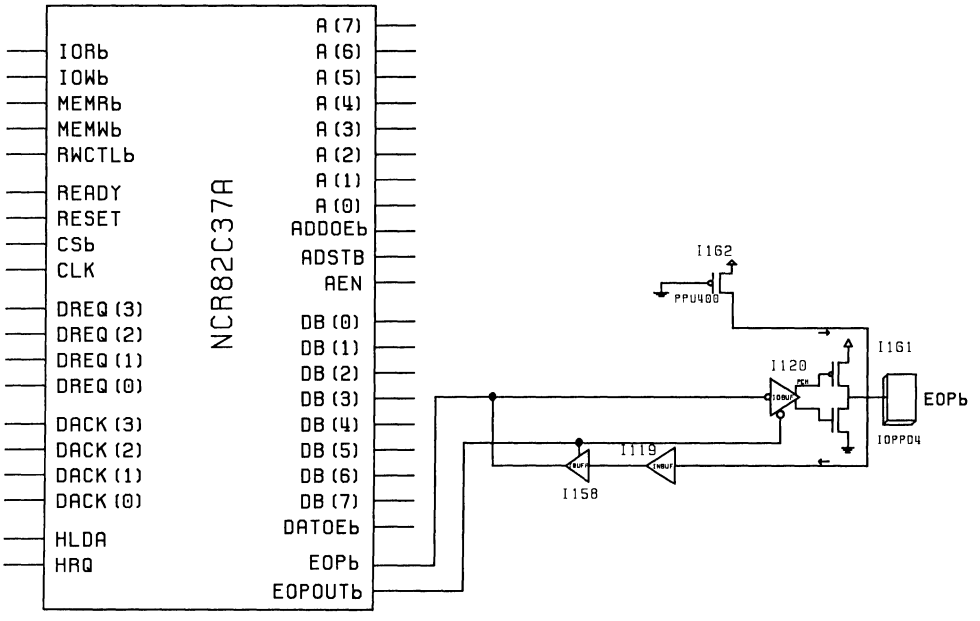
SUPERCELLS



Macro address lines interface to I/O pads



Macro data lines interface to I/O pads



Macro end of process line interface to I/O pad

AC Characteristics – DMA (Master) mode

The following parameters apply strictly to the VS700 macrocell. The VS1500F macrocell will comply with standard part timings only. These timings are derived from prelayout estimated capacitances. Postlayout timing variations may occur.

Temperature and Voltage Range = 0°C to 70°C, VCC = 5 V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit
t_{enl}	AEN HIGH from CLK LOW (S1) Delay time		40	ns
t_{enh}	AEN LOW from CLK HIGH (S1) Delay time		30	ns
t_{afd}	ADR Active to Float Delay from CLK HIGH		30	ns
t_{rwf}	READb or WRITEb Float from CLK HIGH		40	ns
t_{afch}	DB Active to Float Delay from CLK HIGH		40	ns
t_{ahr}	ADR from READb HIGH Hold time	$t_{ck}-50$		ns
t_{ahl}	DB from ADSTB LOW Hold time	40		ns
t_{ahw}	ADR from WRITEb HIGH Hold time	$t_{ck}-25$		ns
t_{ack}	DACK Valid from CLK LOW Delay time (Note 3)		50	ns
	EOPb HIGH from CLK HIGH Delay time (Note 4)		50	ns
	EOPb LOW from CLK HIGH Delay time		50	ns
t_{ach}	ADR Stable from CLK HIGH		50	ns
t_{ast}	DB to ADSTB LOW Setup time	125		ns
t_{ckh}	Clock HIGH Time (Transitions ≤ 10 ns)	60		ns
t_{ckl}	Clock LOW Time (Transitions ≤ 10 ns)	60		ns
t_{ck}	CLK Cycle Time	125		ns
t_{drw}	CLK HIGH to READb or WRITEb LOW Delay (Note 2)		50	ns
t_{rhc}	READb HIGH from CLK HIGH (S4) Delay time (Note 2)		140	ns
t_{whc}	WRITEb HIGH from CLK HIGH (S4) Delay time (Note 2)		120	ns
t_{dq}	HRQ Valid from CLK HIGH Delay time		30	ns
t_{els}	EOPb LOW from CLK LOW Setup time	30		ns
t_{epw}	EOPb Pulse Width	50		ns
t_{fab}	ADR Float to Active Delay from CLK HIGH		30	ns
t_{rwc}	READb or WRITEb Active from CLK HIGH		30	ns
t_{fdc}	DB Float to Active Delay from CLK HIGH		30	ns
t_{hvs}	HLDA Valid to CLK HIGH Setup time		20	ns
t_{dh}	Input Data from MEMRb HIGH Hold time	0		ns
t_{ds}	Input Data to MEMRb HIGH Setup time	120		ns
t_{dvh}	Output Data from MEMWb HIGH Hold time	20		ns
t_{dvs}	Output Data Valid to MEMWb HIGH	175		ns
t_{qst}	DREQ to CLK LOW (SI, S4) Setup time (Note 3)	0		ns
t_{rht}	CLK to READY LOW Hold time	15		ns

(Sheet 1 of 2)

Temperature and Voltage Range = 0°C to 70°C, VCC = 5 V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit
t_{rst}	READY to CLK LOW Setup time	15		ns
t_{sth}	ADSTB HIGH from CLK HIGH Delay time		20	ns
t_{stl}	ADSTB LOW from CLK HIGH Delay time		20	ns

(Sheet 2 of 2)

NOTES:

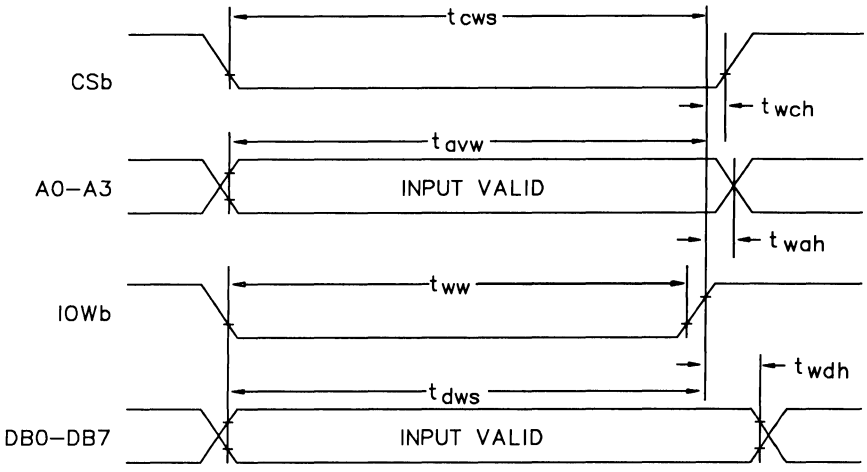
1. Input frequency 5 MHz when RESET.
2. The net IOWb or MEMWb Pulse width for normal write will be t_{ck} – 100 ns and for extended write will be 2 t_{ck} – 100 ns. The net IORb or MEMRb pulse width for normal read will be $2t_{ck}$ – 50 ns and for compressed read will be t_{ck} – 50 ns.
3. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode for DREQ and active low for DACK.
4. EOPb is an open collector output. This parameter assumes the presence of a 2.2K pullup to V_{CC}.

AC Characteristics – Peripheral (Slave) mode

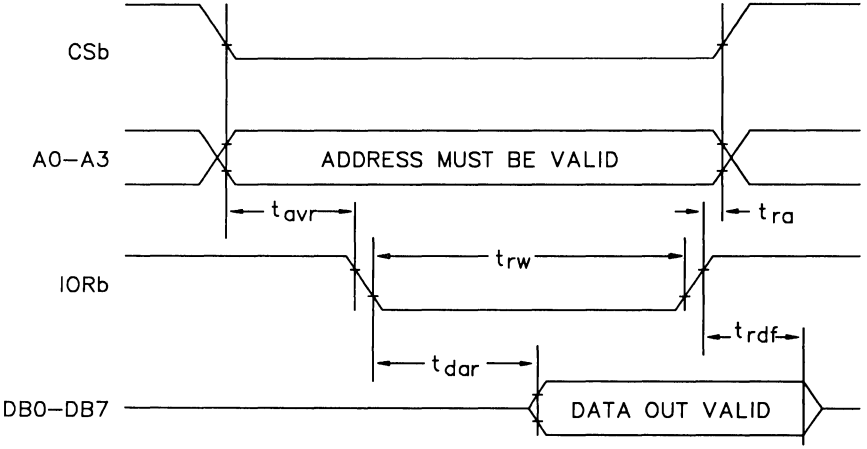
Temperature and Voltage Range = 0°C to 70°C, VCC = 5 V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit
t_{avr}	ADR Valid or CSb LOW to READb LOW	20		ns
t_{avw}	ADR Valid to WRITEb HIGH Setup time	50		ns
t_{cws}	CS LOW to WRITEb HIGH Setup time	50		ns
t_{dws}	Data Valid to WRITEb HIGH Setup time	50		ns
t_{ra}	ADR or CS Hold from READb HIGH	0		ns
t_{dar}	Data Access from READb LOW		90	ns
t_{rdf}	DB Float Delay from READb HIGH	0	50	ns
t_{res}	Power supply HIGH to RESET LOW Setup time	500		ns
t_{rst}	RESET to First IOWRb	1 t_{ck}		ns
t_{rpw}	RESET Pulse width	50		ns
t_{rw}	READb Width	100		ns
t_{wah}	ADR from WRITEb HIGH Hold time	20		ns
t_{wch}	CS HIGH from WRITEb HIGH Hold time	10		ns
t_{wdh}	Data from WRITEb HIGH Hold time	20		ns
t_{ww}	Write Width	50		ns

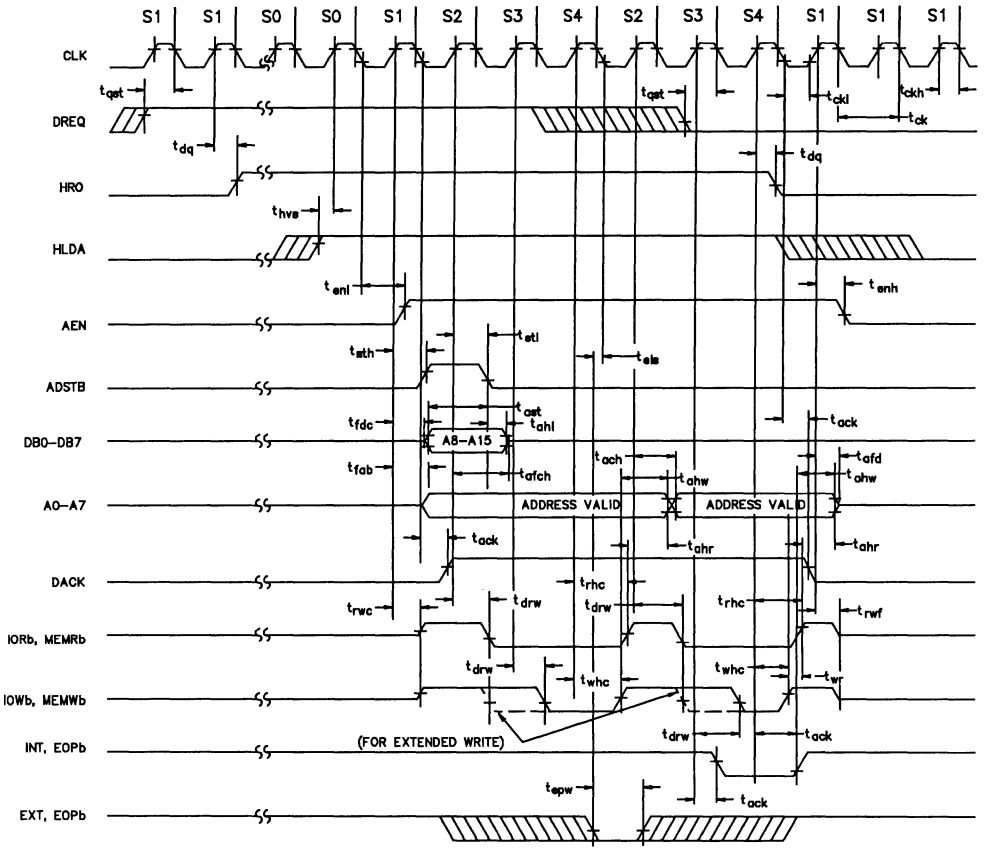
Timing Information



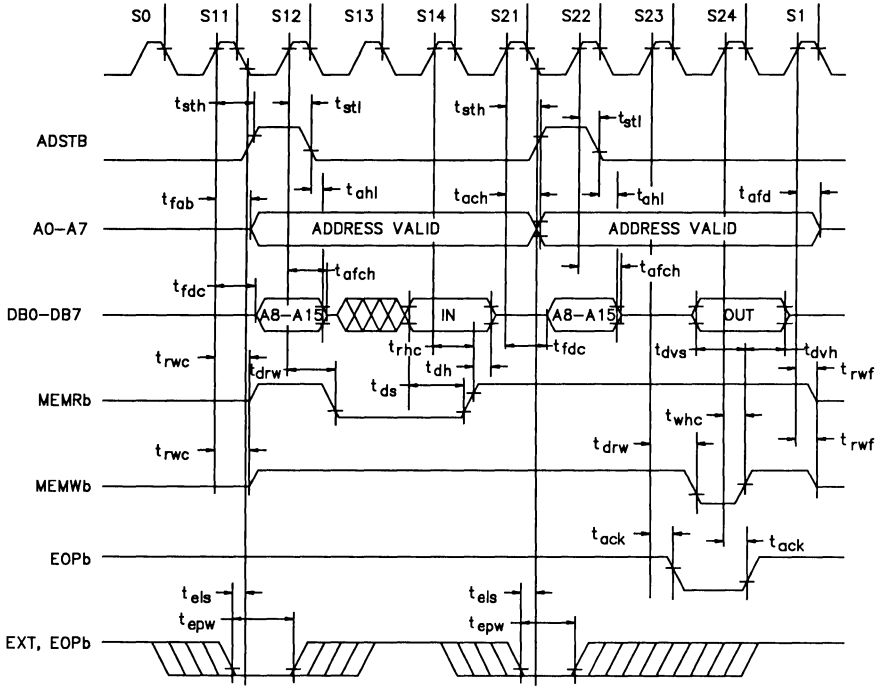
Slave mode write timing



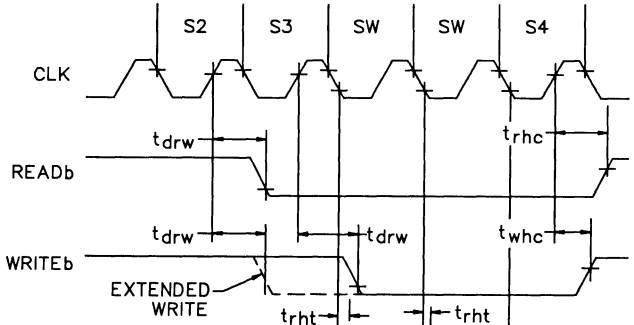
Slave mode read timing



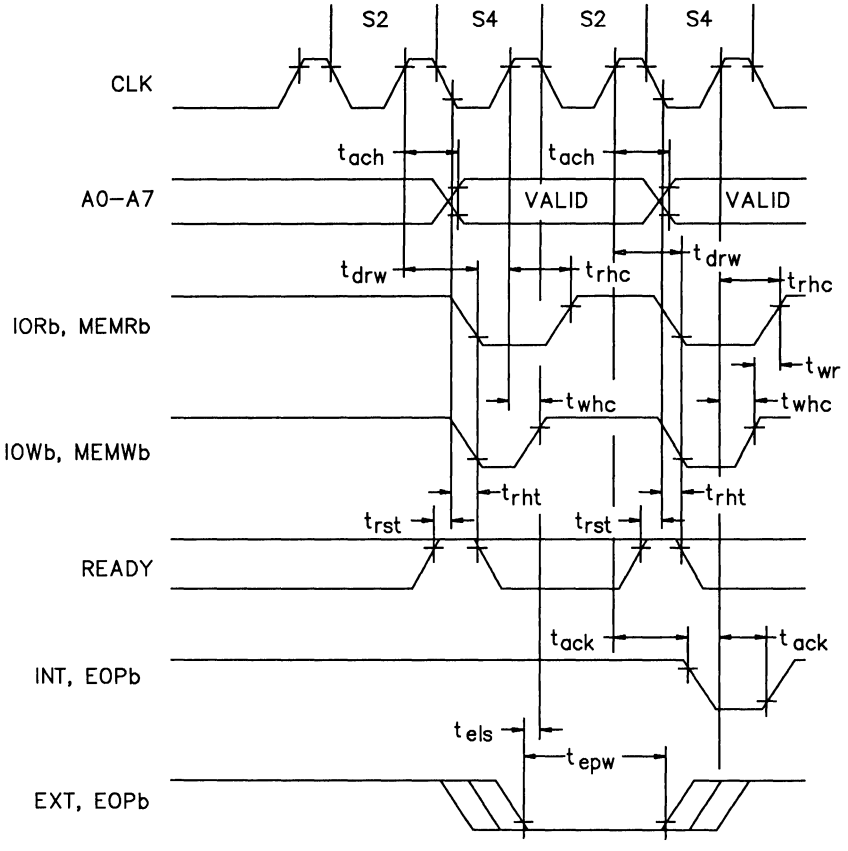
DMA transfer timing



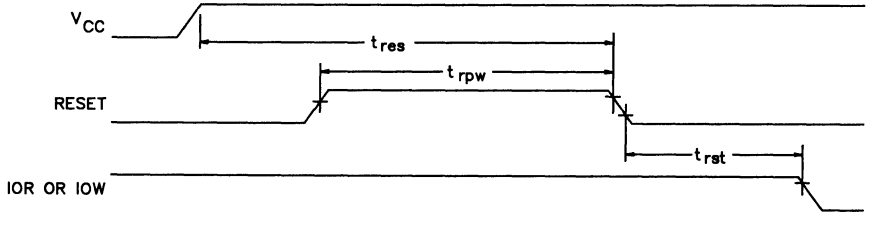
Memory-to-memory transfer timing



Ready timing



Compressed transfer timing



Reset timing

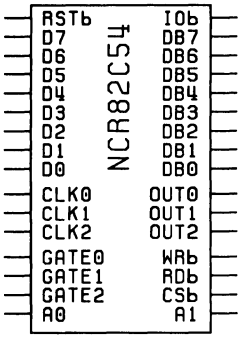
Programmable Interval Timer

Description

- Three independent 16-bit counters
- Binary or BCD counting
- 8 MHz counting rate
- Treated as single cell for design purposes
- Simulated and routed as individual cells for maximum flexibility

The NCR82C54 soft macrocell is functionally equivalent to a standard 8254 device. Each of the three 16-bit counters has six software programmable modes. The NCR82C54 is a superset of the 8253 device. The use of a lower case "b" at the end of a pin name indicates that the signal is asserted low.

Symbol



VS700 Cell count: 1208
Equivalent gate count: 3405
VS1500F Cell count: 1163
Equivalent gate count: 2721

Inputs/Outputs

Definitions of the NCR82C54 inputs and outputs are given in the following table.

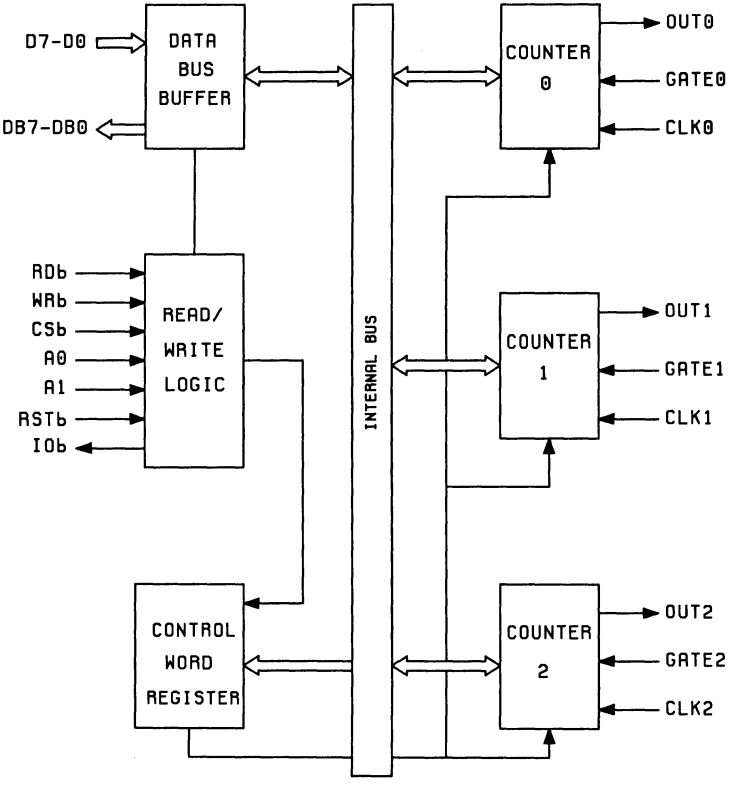
Pin Name	Type	Description
RSTb	I	RESET: Active low input. Signal activated to reset the NCR82C54 for simulation. This pin should be held high during actual use.
D7 -D0	I	DATA BUS IN: Data is written on this bus to the Control Word Register and the Counters during programming. Read-Back and Counter Latch Commands are also issued on this bus.
CLK (0,1,2)	I	CLOCK 0, 1, 2: Clock inputs of Counters 0, 1, and 2 used for loading counts and decrementing the Counters.
GATE(0,1,2)	I	GATE 0, 1, 2: Gate inputs of Counters 0, 1, and 2 used to enable and disable the Counters. Specific use of the Gate signals in operation vary with mode.
A0,A1	I	ADDRESS: Select lines used to address a Counter or the Command Word Register for either a read or write operation.
CSb	I	CHIP SELECT: Active low input. Enables chip for read and write operations.
RDb, WRb	I	READ & WRITE: Active low inputs. Control lines used during programming operations to read data from or write data to the NCR82C54.
OUT(0,1,2)	O	OUTPUT 0, 1, 2: Output signals from Counters 0, 1, and 2.
DB7 - DB0	O	DATA BUS OUT: Data is read on this bus from the Counters or the status register.
IOb	O	I/O ENABLE: I/O direction line used to control tristate drivers on data bus lines DB7 - DB0.

Input Signal Capacitance		
PIN	**VS1500F**	**VS700**
D7–D0	.055 pF	.040 pF
WRb	.421 pF	.250 pF
RDb	.421 pF	.250 pF
CSb	.421 pF	.250 pF
A1–A0	.055 pF	.040 pF
CLK(0,1,2)	.106 pF	.080 pF
GATE(0,1,2)	.055 pF	.040 pF
RSTb	.055 pF	.040 pF

Output Signal Drive Capability		
PIN	**VS1500F**	**VS700**
DB7–DB0	TBUF	TBUF
OUT(0,1,2)	HBUF	HBUF
IOb	NAN3H	NAN3H

NOTE: Input signal capacitance consists of cell input capacitance only. Routing capacitance is not included since the routing will be different for each usage of the soft macrocell.

Functional Block Diagram



Application Notes

Primary Uses

The NCR82C54 interfaces with the system CPU to provide solutions to timing control problems. The macro contains three independently programmable 16-bit counters which can be used to do either binary or binary coded decimal counting. Each of the counters generates an output bit which will have a state determined by the mode of the counter and the value of the current count.

Each of the counters in the NCR82C54 can be programmed to operate in one of six modes:

1. interrupt on terminal count
2. hardware retriggerable one-shot
3. rate generator
4. square wave mode
5. software triggered strobe
6. hardware triggered strobe (retriggerable)

Counters can be enabled or disabled by the gate inputs. The effect of the gate inputs on counting varies depending on the programmed mode of the counter.

Once the counters have been programmed, it is possible at any point to examine the current count or status by writing a Read-Back or Counter Latch Command to the NCR82C54.

Design Information

The NCR82C54 is designed to duplicate the function of the industry standard part. Detailed operating information can be found in any 8254 standard device data sheet.

The NCR82C54 soft macrocell design contains a test input pin called RSTb. This pin is used as an initialization signal when simulating a design. The test pin should be pulsed low at the beginning of each simulation run. This will remove 'indeterminate' logic states inside the three counters. This pin should be held high at all times except to initialize simulations. It is recommended that this pin is used as a reset in a system.

The macrocell design contains no input buffers or output drivers. These must be provided by the user in his or her chip design, along with any input or output pads.

The macrocell design has a split data bus. The input and output signals can be recombined into an internal bidirectional bus using the scheme shown in Figure 8–26. If the signals are to be connected directly to device pads, use the scheme shown in Figure 8–27.

Detailed information on programming the counter modes, and sample timing diagrams can be found in any standard 8254 device data sheet.

A full logic schematic of the NCR82C54 design can be provided for modification in cases where the designer needs only a portion of the full macrocell. NCR assumes no responsibility for the functionality of a soft macrocell which has been altered in this manner. Please contact your NCR Field Applications Engineer for more information if interested.

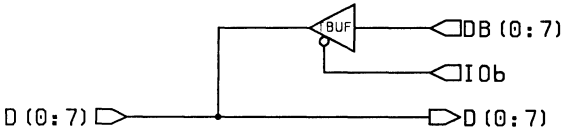


Figure 8–26

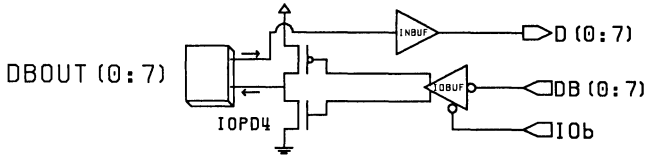


Figure 8–27

AC Characteristics

The following parameters apply strictly to the VS700 macrocell. The VS1500F macrocell will comply with standard part timings only. These timings are derived from prelayout estimated capacitances. Postlayout timing variations may occur.

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit
t_{asw}	Address stable before WRb ↓	0		ns
t_{csw}	CSb stable before WRb ↓	0		ns
t_{htw}	Address hold time after WRb ↑	0		ns
t_{wp}	WRb pulse width	50		ns
t_{dsw}	Data setup time before WRb ↑	50		ns
t_{dh}	Data hold time after WRb ↑	0		ns
t_{cr}	Command recovery time	120		ns

Write cycle

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit
t_{asr}	Address stable before RDb ↓	5		ns
t_{csr}	CSb stable before RDb ↓	0		ns
t_{htr}	Address hold time after RDb ↑	0		ns
t_{rp}	RDb pulse width	50		ns
t_{dd}	Data delay from RDb ↓		50	ns
t_{da}	Data delay from address		50	ns
t_{fl}	RDb ↑ to data floating	5	35	ns
t_{cr}	Command recovery time	120		ns

Read cycle

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit
t_{ck}	Clock period	100	DC	ns
t_{hp}	High pulse width	30		ns
t_{lp}	Low pulse width	50		ns
t_{cr}	Clock rise time		25	ns
t_{cf}	Clock fall time		25	ns
t_{gh}	Gate width high	50		ns
t_{gl}	Gate width low	50		ns
t_{gc}	Gate setup time to CLK ↑	40		ns
t_{gac}	Gate hold time after CLK ↑	50		ns
t_{dco}	Output delay from CLK ↓		100	ns
t_{dgo}	Output delay from gate ↓		100	ns
t_{cd}	CLK delay for loading	0	55	ns
t_{ds}	Gate delay for sampling	−5	40	ns
t_{odw}	OUT delay from mode write		240	ns
t_{csu}	CLK set up for count latch	−40	40	ns

Clock and gate

NOTES:

1. If CLK present at t_{cd} min then Count equals N + 2 CLK pulses, t_{cd} max Count equals N + 1 CLK pulse. t_{cd} min to t_{cd} max, count will be either N + 1 or N + 2 CLK pulses.
2. In Modes 1 and 5, if GATE is present when writing a new Count value, at t_{ds} min Counter will not be triggered, at t_{ds} max Counter will be triggered.
3. If CLK present when writing a Counter Latch or ReadBack Command, at t_{csu} min CLK will be reflected in count value latched, at t_{csu} max CLK will not be reflected in the count value latched. Writing a Counter Latch or ReadBack Command between t_{cl} min and t_{wl} max will result in a latched count value which is ± one least significant bit.
4. External loads of 1 pF used for test case, macrocell only.

Timing Information

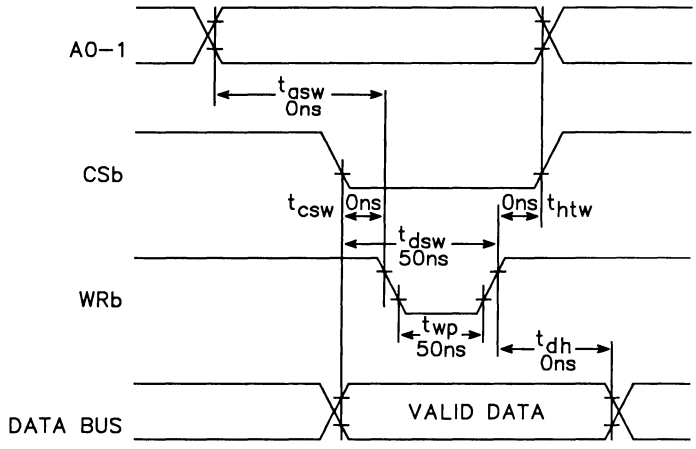


Figure 8–28 Write

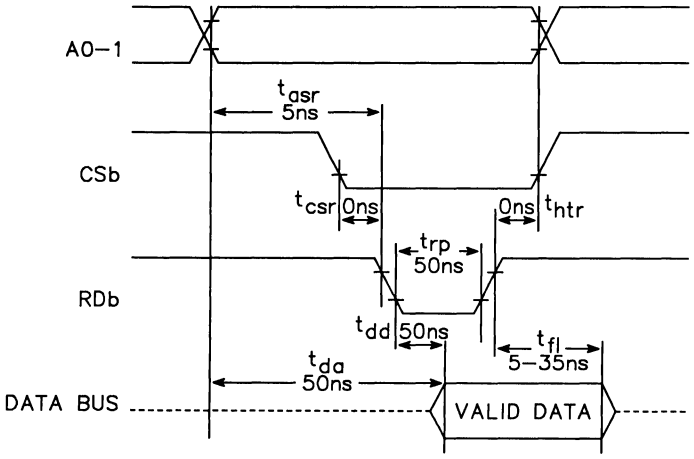


Figure 8–29 Read

SUPERCELLS

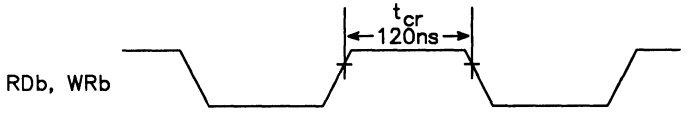


Figure 8–30 Recovery

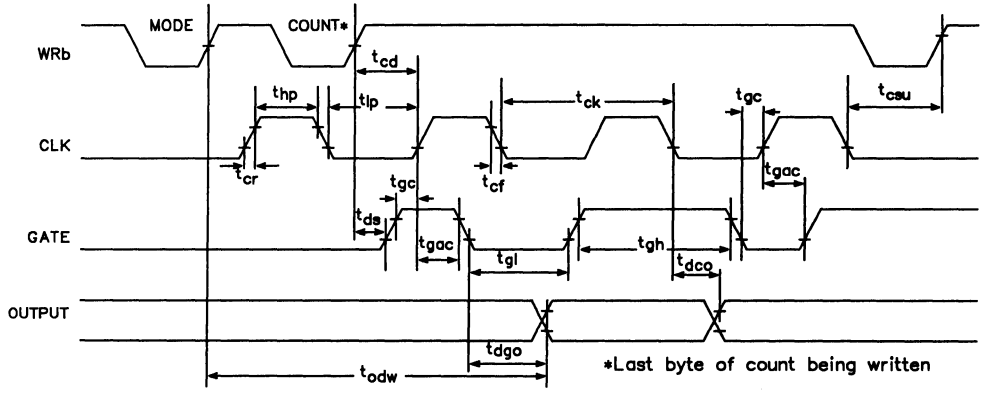


Figure 8–31 Clock and gate

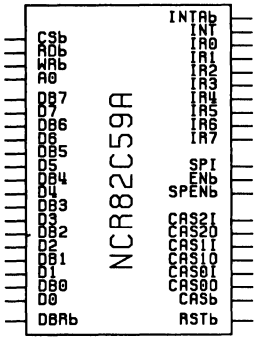
Programmable Interrupt Controller

Description

- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Treated as single cell during design
- Simulated and routed as individual cells for maximum flexibility

The NCR82C59A interrupt controller handles up to 8 vectored interrupts for the CPU. It is cascadable to 64 interrupts. It is compatible with 8080, 8085, 8086, 8088, 80286, and 80386 processors. The use of a lower case "b" at the end of a pin name indicates that the signal is asserted low.

Symbol



VS700 Cell count: 656
Equivalent gate count: 1326
VS1500F Cell count: 717
Equivalent gate count: 1296

Inputs/Outputs

Definitions of the NCR82C59A inputs and outputs are given in the following table.

Pin Name	Type	Description
CSb	I	CHIP SELECT: Active low input. Enables chip for read and write operations.
RDb, WRb	I	READ & WRITE: Active low inputs. Control lines used during programming operations to read data from or write data to the NCR82C59.
A0	I	ADDRESS: Select line used for register selection during reading and writing. Usually connected to the CPU A0 address line.
DB(7-0)	O	DATA BUS OUT: Data is read from the registers or output by an interrupt acknowledge.
D(7-0)	I	DATA BUS IN: Data is written on this bus to set modes of operation and to set registers.
DBRb	O	DATA BUS ENABLE: Data bus direction line used to control tristate drivers on data bus lines DB7-DB0.
RSTb	I	RESET: Active low input. Signal activated to reset the NCR82C59 for simulation. This pin should be held high during actual use.
CASb	O	CASCADE ENABLE: Cascade bus direction line used to control tristate drivers on cascade lines CAS(0,1,2)O

(Sheet 1 of 2)

Pin Name	Type	Description
CAS(0,1,2)I	I	CASCADE ADDRESS: Input when in SLAVE mode. Determines which NCR82C59 is a slave.
CAS(0,1,2)O	O	CASCADE ADDRESS: Output when in MASTER mode. Determines which NCR82C59 is a slave.
SPENb	O	(SLAVE PROGRAM/ENABLE BUFFER) ENABLE: Direction line used to control tristate driver on ENb.
SPI	I	SLAVE PROGRAM INPUT: Used when not in buffered mode to indicate the master or slave status of the particular NCR82C59.
ENb	O	ENABLE BUFFER OUT: Used during buffered mode to control buffer transceivers.
IR(7-0)	I	INTERRUPT REQUESTS: Asynchronous inputs. These lines are raised high to indicate an interrupt pending.
INT	O	INTERRUPT: This pin indicates an interrupt out to the CPU.
INTAb	I	INTERRUPT ACKNOWLEDGE: Active low input. Input from the CPU which acknowledges requested interrupts.

(Sheet 2 of 2)

NOTE: Signals DBRb, SPENb, and CASb are low when data flow is OUT of the macrocell.

Input Signal Capacitance

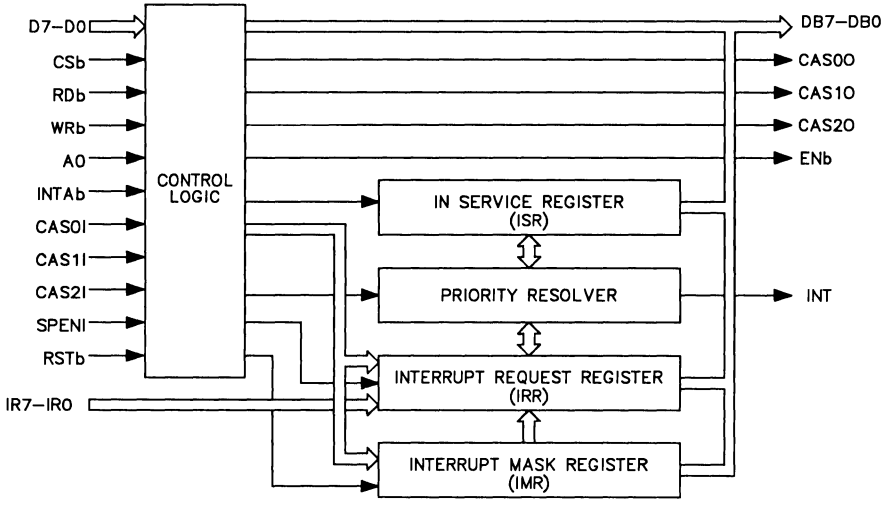
PIN	VS1500F	VS700
CSb	0.421 pF	0.040 pF
RDb	0.421 pF	0.040 pF
WRb	0.421 pF	0.040 pF
A0	0.421 pF	0.040 pF
D7-D0	0.055 pF	0.040 pF
CAS(0,1,2)I	0.160 pF	0.100 pF
SPI	0.110 pF	0.100 pF
IR7-IR0	0.055 pF	0.040 pF
INTAb	0.055 pF	0.040 pF

Output Signal Drive Capability

PIN	VS1500F	VS700
DB7-DB0	TBUF, INVT	TBUF3
DBRb	NOR2H	NOR2H
CASb	INV	INV
CAS(0,1,2)O	NOR2H	NOR2
SPENb	INV	INVH
ENb	NOR2	AND2
INT	BUF8	DFFRSP

NOTE: Input signal capacitance consists of cell input capacitance only. Routing capacitance is not included since the routing will be different for each usage of the soft macrocell.

Functional Block Diagram



Application Notes

Primary Uses

The NCR82C59 interfaces with the system CPU to provide the management in an interrupt environment. The macro accepts interrupt requests from a variety of devices and makes a determination on whether or not to service the current device or the one making a request. This determination is based on a priority scheme that is programmable by the user. This chip has many modes of operation and the user is encouraged to obtain any standard 8259A data sheet for complete information.

The following modes represent a brief synopsis of what this macro cell has available:

Fully nested mode	– general purpose priority mode
Automatic rotation	– equal priority mode
Specific rotation	– specific priority mode
Special mask mode	– control over specific interrupts
Cascade mode	– expansion to more than eight interrupts

All of the above modes are available in both 80/85 and 86/88 modes of operations. They can also be triggered by either level or edge type of interrupting devices. The macro also provides a variety of ways to signify an end of interrupt and the user should consult a complete data sheet for further information.

Design Information

The NCR82C59 was designed to meet the standard part in all aspects of operation. The following deviations from the standard 8259A data sheet were found:

- The 8259A data sheet states that upon receiving an INTAb from the CPU group, that the highest priority ISR bit is set, and the corresponding IRR bit is reset. We found this not to be the case and the standard part does not do the above mentioned until the end of the INTAb sequence.
- The Intel specification states that an Operation Command Word (OCW) can be written to the 8259A any time after the Initialization Command Words have been sent. We found that the standard part will pull its INT line low for the duration of a write pulse if this line has been set prior to the writing of an OCW. We choose not to duplicate this behavior and our part will keep its INT line high during any writes.

The interrupt input lines do not have an internal pullup on them like the standard part. The user must connect the external IR input lines to a IPPD pad with a PPU400 pullup. The output of the pad is connected to an INBUF to the IR input on the supercell. Interrupt input lines connected to an internal node do not require a pullup.

The NCR82C59A supercell has a split data bus. The output data bus is not driven unless the supercell is selected and read or during an interrupt acknowledge sequence. The output bus should be terminated with a PU30 cell to prevent excess power consumption. The user can connect the output bus to the input of a TBUF cell. The output of the TBUF can be connected to the input bus of the cell. The enable of the TBUF can be connected to the signal DBRb. This connection is the preferred method for use with an internal data bus. See Figure 8–32.

Each of the input lines to the supercell represents one inverter load to the source of the signal.

The cascade input lines must be tied low if they are not used. The cascade output lines of the master are connected to the input lines of the slave supercells. The SPI input must be tied high for a master device and tied low for slave devices. If there is only one supercell used, the SPI line must be tied high.

The RSTb input line is a master reset signal to the supercell. It must be controlled to properly initialize the device. RSTb must be pulled low at the start of the system operation or test program.

The following circuit is recommended if an internal data bus is used to interface to the macrocell:

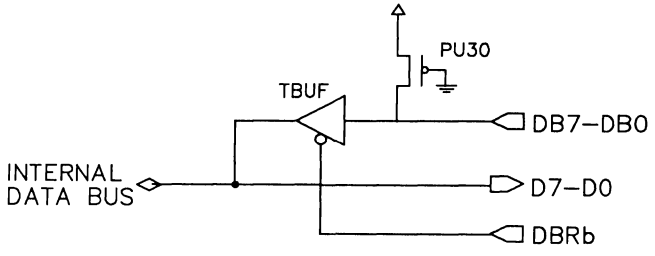


Figure 8–32

AC Characteristics

The following parameters apply strictly to the VS700 macrocell. The VS1500F macrocell will comply with standard part timings only. These timings are derived from prelayout estimated capacitances. Postlayout timing variations may occur.

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
t_{rl}	AO/CSb setup to RD/INTAb ↓	10		ns	
t_{rx}	AO/CSb hold after RD/INTAb ↑	5		ns	
t_{rp}	RDb pulse width	50		ns	
t_{hl}	AO/CSb setup to WRb ↓	25		ns	
t_{wx}	AO/CSb hold after WRb ↑	0		ns	
t_{wp}	WRb pulse width	50		ns	
t_{ds}	Data setup to WRb ↑	40		ns	
t_{dh}	Data hold after WRb ↑	0		ns	
t_{ir}	Interrupt request width (low)	50		ns	See Note 1
t_{cas}	Cascade setup to second or third INTAb ↓ (slave only)	40		ns	
t_{rint}	End of RDb to next RDb End of INTAb to next INTAb within an INTAb sequence only	25		ns	
t_{wen}	End of WRb to next WRb	25		ns	
t_{cen}	End of command to next command (not same command type) End of INTAb sequence to next INTAb sequence	50		ns	

Timing requirements

NOTES:

1. This is the low time required to clear the input latch in the edge triggered mode.
2. External loading of 1 pF used for test case, macrocell only.

Temperature and Voltage Range = 0° C to 70° C, V_{CC} = 5V ± 10%, external load 1 pF

Symbol	Parameter	Min	Max	Unit	Comments/ Conditions
t_{vr}	Data valid from RDb/INTAb ↓		25	ns	See Note 2
t_{df}	Data float after RDb/INTAb ↑	5	15	ns	
t_{od}	Interrupt output delay		40	ns	
t_{vi}	Cascade valid from first INTAb ↓ (Master only)		50	ns	
t_{ea}	Enable active from RDb ↓ or INTAb ↓		40	ns	
t_{ei}	Enable inactive from RDb ↑ or INTAb ↑		10	ns	
t_{dvs}	Data valid from stable address		75	ns	
t_{vd}	Cascade valid to valid data		75	ns	

Timing responses

Timing Information

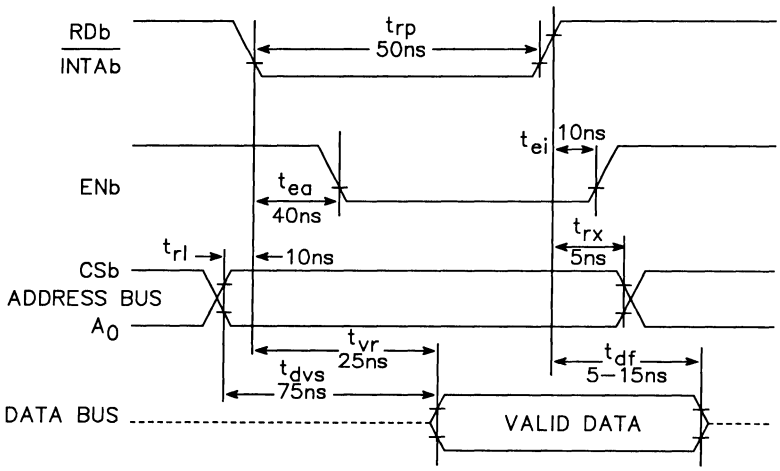


Figure 8–33 Read/INTA

SUPERCELLS

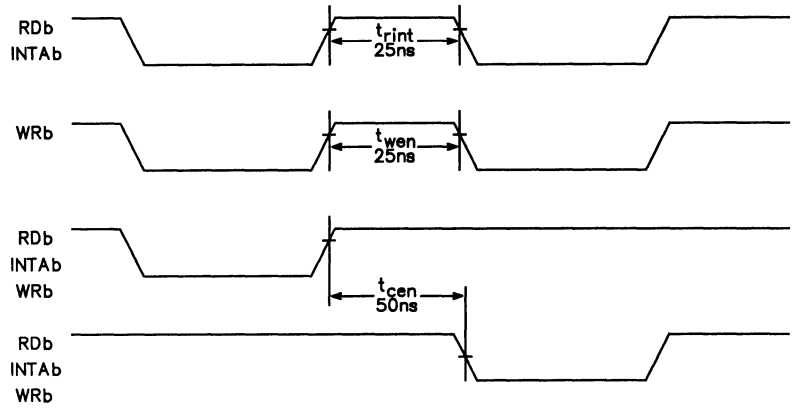


Figure 8–34 Other timing

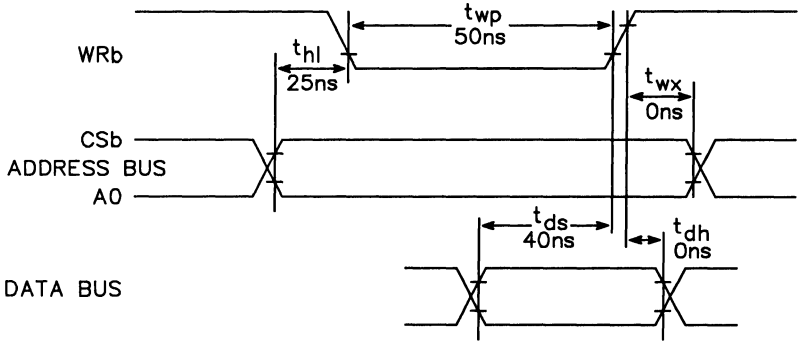


Figure 8–35 Write

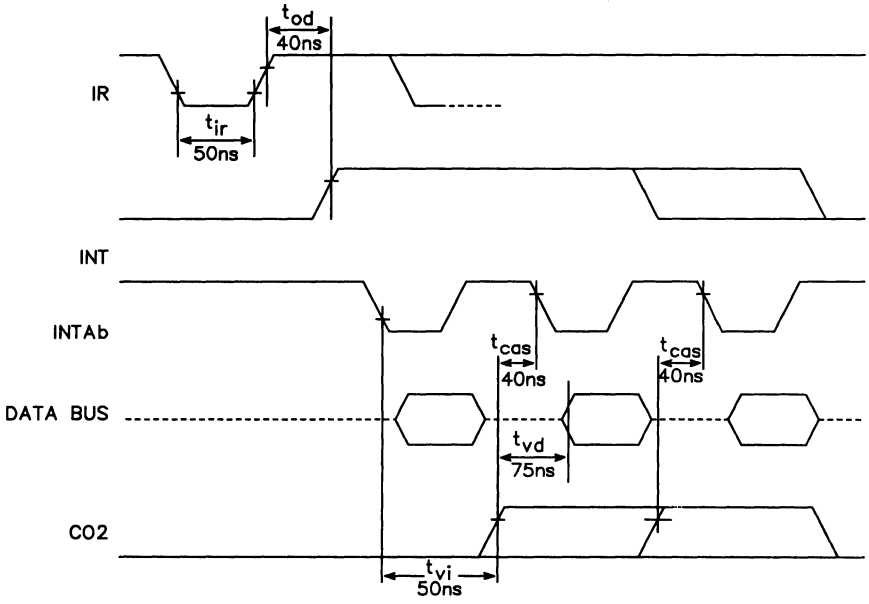


Figure 8–36 INTA sequence

NCR53C90A–Compatible SCSI Controller Core Product Brief

Features

- ASIC core cell compatible with NCR53C90A
- ANSI X3.131–1986 compatible
- On–chip 48 mA drivers
- Control logic for differential transceivers
- Parity generation, optional checking
- Programmable transfer period
- Programmable offset
- 16–byte FIFO
- 12 MB/S DMA interface
- Up to 5 MB/S asynchronous SCSI
- Up to 5 MB/S synchronous SCSI
- 25 MHz clock S/C features
- Submicron CMOS cell–based technology
- Bus model available for Verilog Simulator
- Simulation and test patterns provided
- Combines easily with other high–level digital and analog functions
- Kit parts with pinout identical to standard part
- Kit part package type: 68–pin PLCC

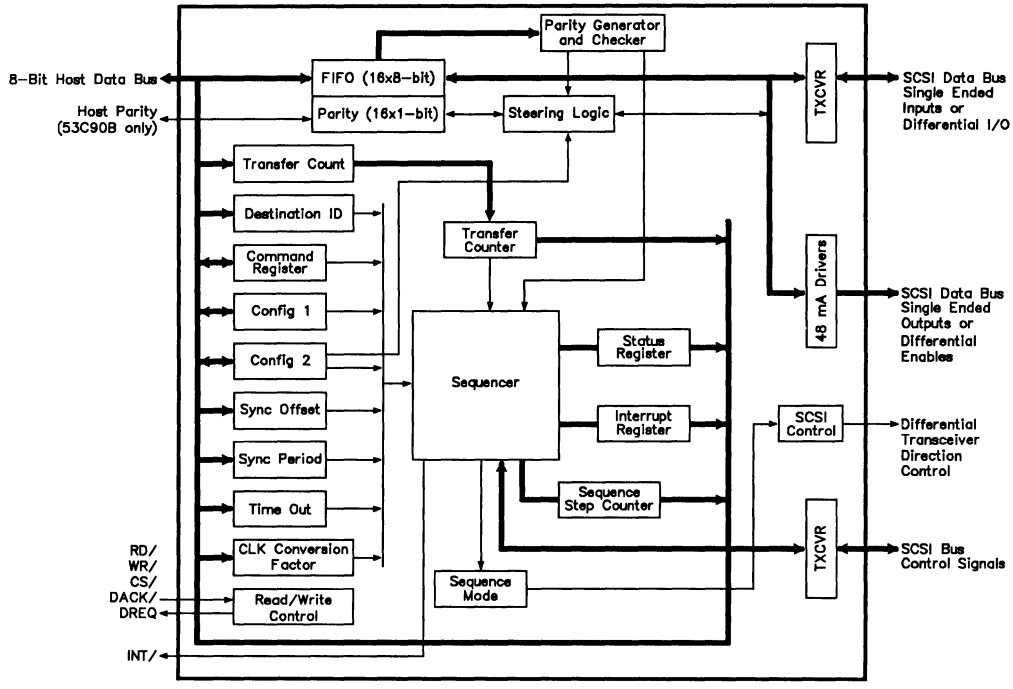
Product Description

The NCR53C90A SCSI Controller ASIC core cell has been developed to be compatible with the NCR53C90A standard part. It matches the functionality of the industry standard device and is fully supported in a semicustom design environment. Bus level and gate level models as well as simulation and test vectors are available under license from NCR. Kit parts matching standard part pinouts and package type are available for early system and firmware verification.

Designed with NCR's cell–based technology, the NCR53C90A–compatible core is a high performance CMOS core conforming to the ANSI standard, X3.131–1986, for Small Computer Systems Interface (SCSI). It is a super–set of the 53C90 with additional commands and a second configuration register. The NCR53C90A–compatible core is intended to directly replace a 53C90 or 53C90A in an existing design. It is 100% compatible with existing 53C90 and 53C90A software.

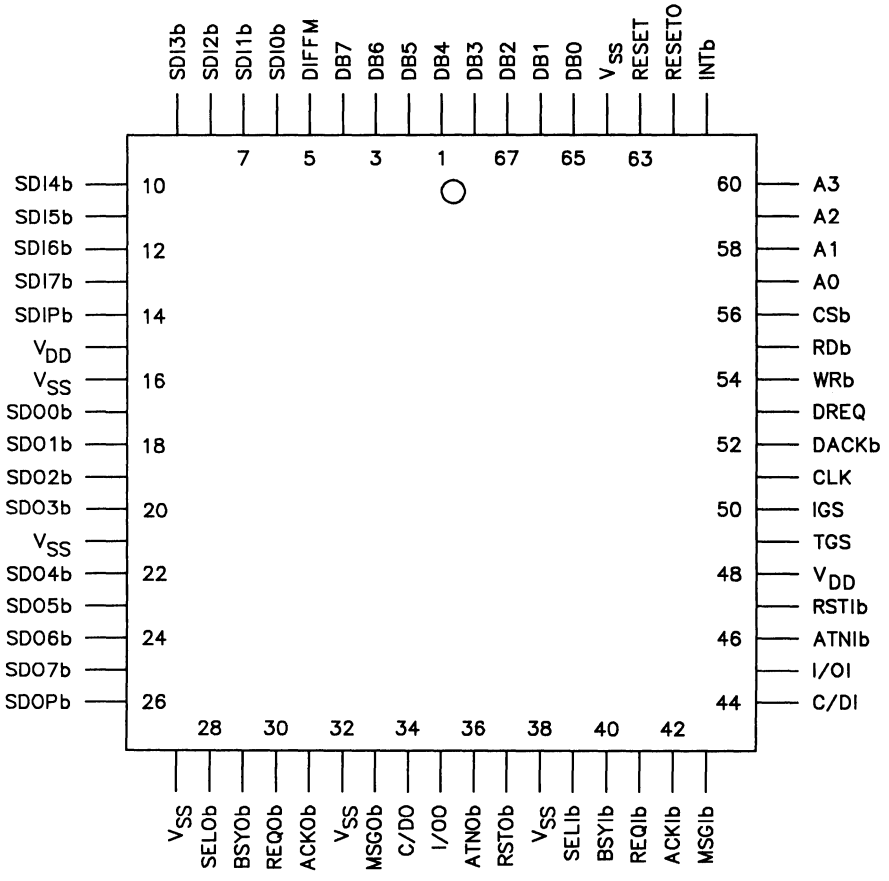
The 53C90 family reduces protocol overhead by performing common SCSI algorithms, or sequences, in response to a single 53C90 command. The NCR53C90A–compatible core will operate at sustained data transfer rates of 5 MB/S in synchronous mode and 5 MB/S in asynchronous mode.

The NCR53C90A–compatible core is fabricated with NCR's VS700 submicron cell–based technology and is available as a kit part in a 68–pin PLCC.



Functional block diagram

SCSI Controller Core



Kit part pinout

Host Processor and SMA Interface Pins – PLCC Package

Pin Name	Type	Description
DB7 – DB0	I/O	ACTIVE– HIGH DATA BUS: This is connected to the DMA controller, CPU and buffer memory. Each pad contains a pull-up to V_{DD} (12.5K minimum).
RESET	I	ACTIVE– HIGH CHIP RESET: Reset must be asserted for two CLK periods, minimum, after the voltage on the power pins has reached V_{DD} min. This input must not be connected to RESETO.
RESETO	O	ACTIVE– HIGH RESET OUTPUT: This output is always asserted when the RESET input is true OR may be asserted when the SCSI reset signal is active if bit 6 of the Config 1 register is cleared and the host has not serviced the interrupt (generated because of SCSI reset) within 1–2 ms (depending on CLK frequency and clock conversion factor).
INT/	O	ACTIVE– LOW, OPEN DRAIN INTERRUPT SIGNAL: This is to the microprocessor. It is latched on the rising edge of CLK and may be cleared by reading the interrupt register or by a host hardware reset, or by a host software reset (but not by a SCSI reset). This output cannot be disabled internally.
A3 – A0	I	ACTIVE– HIGH ADDRESS BUS: This specifies one of the ASPs internal registers for reading or writing. Used with CS/, ignored with DACK/.
CS/	I	ACTIVE– LOW CHIP–SELECT SIGNAL: This enables access to the ASPs internal registers. CS/ accesses any register, including the FIFO, while DACK/ accesses only the FIFO, CS/ and DACK/ must never be active at the same time.
RD/	I	ACTIVE–LOW READ SIGNAL: This enables ASP data onto DB7–DB0. CS/ or DACK/ must also be active.
WR/	I	ACTIVE–LOW WRITE SIGNAL: This strobes DB7–DB0 data into the ASP. CS/ or DACK/ must also be active.
DREQ	O	TRISTATE ACTIVE–HIGH DMA REQUEST: This is to the DMA controller. DREQ will be true as long as the FIFO has at least one byte to send to memory, or has room to receive at least one byte from memory, depending on data direction.
DACK/	I	ACTIVE–LOW DMA ACKNOWLEDGE: This is from the DMA controller. DACK/ accesses the FIFO only, while CS/ accesses any register, including the FIFO, CS/ and DACK/ must never be active at the same time. DACK/ must toggle true then false for every byte transferred.
CLK	I	SQUARE WAVE CLOCK: This generates internal chip timing. A 25 MHz clock with a 35% to 65% duty cycle is required. The minimum frequency required for asynchronous SCSI transmission is 10 MHz. The minimum frequency required for synchronous transmission is 12 MHz. The synchronous transmission rate is equal to the CLK input period divided by the value in the synchronous transfer period register. The asynchronous transfer rate is indirectly affected by CLK frequency.

SCSI Controller Core

SCSI Bus Interface – PLCC Package

Pin Name	Type	Description
SDI0/–SDI7/SDIP	I/O	SCHMITT TRIGGER, ACTIVE–LOW SCSI DATA/PARITY BUS: In single–ended mode (DIFFM = 0) these inputs are SCSI data bus signals. In differential mode (DIFFM = 1) these are bidirectional data and parity signals for external SCSI bus transceivers.
SDO0/–SDO7/ SDOP	O O	48–mA, OPEN DRAIN SCSI DATA PARITY BUS: In single–ended mode (DIFFM = 0) these outputs are active–low SCSI data signals. In differential mode (DIFFM = 1) these outputs are used to control the direction of external differential transceivers, with high meaning output to the SCSI bus, low meaning input from the SCSI bus.
SELO/	O	48–mA, OPEN DRAIN SCSI SELECT SIGNAL: In single–ended mode this output is active–low. In differential mode it is active–high.
BDYO/	O	48–mA, OPEN DRAIN SCSI BUSY SIGNAL: In single–ended mode, this output is active–low. In differential mode it is active–high.
REQO	O	48–mA, OPEN DRAIN, ACTIVE–LOW SCSI REQUEST SIGNAL: This output is only asserted when the ASP is in target mode.
ACKO/	O	48–mA, OPEN DRAIN, ACTIVE–LOW SCSI ACKNOWLEDGE SIGNAL: This output is only asserted when the ASP is in initiator mode.
MSGO/,C/DO, I/OO	O	48–mA, OPEN DRAIN, ACTIVE–LOW SCSI PHASE SIGNALS: These outputs are only asserted when the ASP is in target mode.
ATNO/	O	48–mA, OPEN DRAIN, ACTIVE–LOW SCSI ATTENTION SIGNAL: This output is only asserted when the ASP is in initiator mode. Several ASP commands will set ATN. It is also asserted when the ASP detects an incoming parity error if parity checking is enabled.
RSTO/	O	48–mA, OPEN DRAIN SCSI RESET SIGNAL: In single–ended mode this output is active–low. In differential mode it is active–high. The ASP drives this signal true only when the host writes the SCSI bus reset command to the command register. The pulse length is 25–40 us, depending on CLK frequency and clock conversion factor.
SELI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI SELECT INPUT.
BSYI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI BUSY INPUT.
REQI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI REQUEST INPUT.
ACKI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI ACKNOWLEDGE INPUT.
MSGI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI MESSAGE INPUT.
C/DI	I	SCHMITT TRIGGER SCSI CONTROL/DATA INPUT.
I/OI	I	SCHMITT TRIGGER SCSI INPUT/OUTPUT INPUT.
ATNI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI ATTENTION INPUT.
RSTI/	I	SCHMITT TRIGGER, ACTIVE–LOW SCSI RESET SIGNAL: When this input is true, the ASP will automatically disconnect from the SCSI bus. If bit 6 in the Config 1 register is zero, the ASP will interrupt the host. If the interrupt is not serviced within 1–2 ms, the ASP will reset its host processor.
IGS	O	ACTIVE–HIGH INITIATOR GROUP SELECT SIGNAL: This pin is high whenever the ASP is in initiator mode. It is used in differential mode to enable the initiator signals (ACKO/, ATNO/). When low, the ASP should be receiving these signals.

(Sheet 1 of 2)

Pin Name	Type	Description
TGS	O	ACTIVE–HIGH TARGET GROUP SELECT SIGNAL. This pin is high whenever the ASP is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGO/, C/DO, I/OO). When low, the ASP should be receiving these signals.
DIFFM	I	DIFFERENTIAL MODE ENABLE. When this pin is grounded, the ASP operates in single–ended mode, with separate SCSI data input and output buses. When this pin is high, the ASP operates in differential mode, with bidirectional SCSI data on the SDI pins and active–high differential transceiver enables on the SDO pins.

(Sheet 2 of 2)

Register Description Table

Address (hex)	Read	Write
0	Transfer counter LSB	Transfer count LSB
1	Transfer counter MSB	Transfer count MSB
2	FIFO	FIFO
3	Command	Command
4	Status	Destination bus ID
5	Interrupt	Select/reselect timeout
6	Sequence step	Synchronous period
7	FIFO flags/sequence step	Synchronous offset
8	Configuration 1	Configuration 1
9	NCR reserved	Clock conversion factor
A	NCR reserved	Test mode
B	Configuration 2	Configuration 2

SCSI Controller Core

Register Set

Some Advanced SCSI Controller (ASC) registers have different meanings during reads than writes. When CS/ is true, the register being accessed is determined by either RD/ or WR/ together with the address pins A0–3. The FIFO may be accessed using either CS/ or DACK/ together with RD/ or WR/. Address pins A0–A3 are ignored when DACK/ is active, but must be driven when CS/ is active.

Transfer Count (Write address 0,1)

These two registers together form a 16–bit transfer count for DMA operations. Transfer count specifies the number of bytes that are to be transferred over the SCSI bus.

Transfer Count (Read address 0,1)

A read from these two addresses will return the value currently in the counter.

With one exception, non–DMA commands do not use the counter. The exception is when the ASC has been selected, it decodes the group code field of the CDB (Command Descriptor Block), loads the counter with the number of bytes in the CDB, then decrements once for every byte received.

The transfer counter decrements on the leading edge of :

Target	Decremented by
Data in phase	DACK/
Data out phase	REQO/

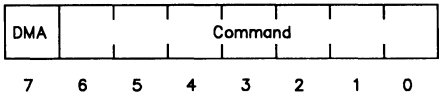
Initiator	Decremented by
Synchronous data in	DACK/
Asynchronous data in	ACKO/
Data out	DACK/

FIFO Register (Read/write address 02)

The FIFO is a 16 by 9–bit first–in–first–out buffer between the SCSI bus and memory. It is accessible by the host processor at this address. It is also accessible by an external DMA controller and by the SCSI bus.

Command Register (Read/write address 03)

The command register is a two deep 8–bit read/write register used to give commands to the ASC. Up to two commands may be stacked in the command register.



Command register (Read/write address 03)

Bit 7 (Enable DMA)
When Bit 7 is set, the command is a DMA instruction.

Command Register								Command Mnemonic	Interrupt
7	6	5	4	3	2	1	0	**Miscellaneous Group**	
X	0	0	0	0	0	0	0	NOP	No
X	0	0	0	0	0	0	1	Flush FIFO	No
X	0	0	0	0	0	1	0	Reset chip	No
X	0	0	0	0	0	1	1	Reset SCSI bus	No*
								Disconnected State Group	
X	1	0	0	0	0	0	0	Reselect sequence	Yes
X	1	0	0	0	0	0	1	Select without ATN sequence	Yes
X	1	0	0	0	0	1	0	Select with ATN sequence	Yes
X	1	0	0	0	0	1	1	Select with ATN and stop sequence	Yes
X	1	0	0	0	1	0	0	Enable selection/reselection	No
X	1	0	0	0	1	0	1	Disable selection/reselection	Yes
X	1	0	0	0	1	1	0	Select with ATN3	Yes
								Target State Group	
X	0	1	0	0	0	0	0	Send message	Yes
X	0	1	0	0	0	0	1	Send status	Yes
X	0	1	0	0	0	1	0	Send data	Yes
X	0	1	0	0	0	1	1	Disconnect sequence	Yes
X	0	1	0	0	1	0	0	Terminate sequence	Yes
X	0	1	0	0	1	0	1	Target command complete sequence	Yes
X	0	1	0	0	1	1	1	Disconnect	No
X	0	1	0	1	0	0	0	Receive message	Yes
X	0	1	0	1	0	0	1	Receive command sequence	Yes
X	0	1	0	1	0	1	0	Receive data	Yes
X	0	1	0	1	0	1	1	Receive command sequence	Yes
X	0	0	0	0	1	0	0	Target abort DMA	No**
								Initiator State Group	
X	0	0	1	0	0	0	0	Transfer information	Yes
X	0	0	1	0	0	0	1	Initiator command complete sequence	Yes
X	0	0	1	0	0	1	0	Message accepted	Yes
X	0	0	1	1	0	0	0	Transfer pad	Yes
X	0	0	1	1	0	1	0	Set ATN	No
X	0	0	1	1	0	1	1	Reset ATN	No

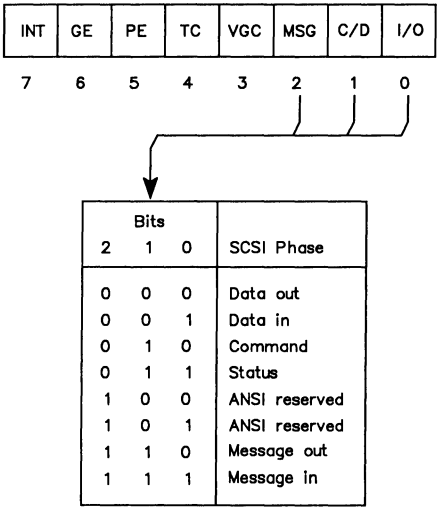
* The command itself does not cause an interrupt; however, external connection of the RSTO/ pin to RSTI/ pin causes an interrupt if the SCSI reset reporting is not disabled in the configuration register.

** The command itself does not cause an interrupt; however, it may allow a stalled command to finish and generate an interrupt.

ASC Command Set

Status Register (Read address 04)

The status register contains important flags that indicate various conditions.



Status Register (Read address 04)

Bit 7 (Interrupt)
This bit is set whenever the INT output is true.

Bit 6 (Gross error)

Bit 5 (Parity error)
This bit will be set if parity checking is enabled.

Bit 4 (Terminal count)
This bit is set when the transfer counter decrements to zero.

Bit 3 (Valid group code)
Command group code.

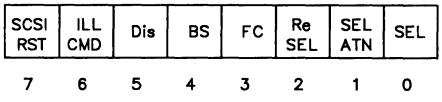
Bit 2–0 (Phase bits)
These bits indicate the phase on the SCSI bus at the time the register was read.

Destination ID (Write address 04)

The least significant 3 bits of this register specify the encoded destination bus ID for a selection or reselection command.

Interrupt Register (Read address 05)

This 8-bit register is used in conjunction with the status register and sequence step register to determine the cause of an interrupt.



Interrupt register (Read address 05)

Bit 7 (SCSI reset detected)
This bit is set if the SCSI reset reporting bit in the Config 1 register is set to zero and the chip detects a reset on the SCSI bus.

Bit 6 (Illegal command)
This bit is set when an unused code is placed in the command register or when the command is from a mode group different than the mode the ASC is currently in. Refer to the *Command Register* definition.

Bit 5 (Disconnect)
In initiator mode, this bit is set when the target disconnects or a selection or reselection time-out occurs. When the ASC is in target mode, this bit is set if a terminate sequence or command complete sequence command causes the ASC to disconnect from the bus.

Bit 4 (Bus service)
This bit indicates that another device is requesting service. In target mode, it is set whenever the initiator asserts ATN (Attention).

In initiator mode, it is set whenever the target is requesting an information transfer phase.

Bit 3 (Function complete)
This bit will be set after any target mode command has completed. In initiator mode, it is set after a target has been selected (before transferring any command phase bytes), after command complete finishes, or after a transfer into command when the target is requesting message in phase.

Bit 2 (Reselected)
This bit is set during reselection phase to indicate that the ASC has been reselected as an initiator.

Bit 1 (Selected with ATN)
This bit is set during selection phase to indicate that the ASC has been selected as a target and that ATN was asserted on the SCSI bus.

Bit 0 (Selected)
This bit is set during selection phase to indicate that the ASC has been selected as a target and that ATN was false during selection.

Time–Out (Write address 05)

This 8–bit write–only register specifies the amount of time to wait for a response during selection or reselection.

Synchronous Transfer Period (Write address 06)

The lower five bits of this register specify the minimum time between leading edges of successive REQ (Request) or ACK (Acknowledge) pulses.

Sequence Step (Read address 06)

The lower 3 bits of this register are used to indicate how far the internal sequencer was able to proceed in executing combination commands.

FIFO Flags (Read address 07)

The least significant five bits of this register indicate how many bytes are currently in the FIFO. The value is binary encoded.

SS2	SS1	SS0	FF4	FF3	FF2	FF1	FF0
7	6	5	4	3	2	1	0

SS = Sequence Step FF = FIFO FLag

FIFO Flags (Read address 07)

The upper three bits are duplicates of the sequence step register bits when operating in normal mode.

Synchronous Offset (Write address 07)

The least significant four bits of this register specify whether the ASC will transfer data phase bytes synchronously or asynchronously. *Zero specifies asynchronous transfer.*

Configuration 1 Register (Config 1) (Read/write address 08)

This 8–bit read/write register specifies various operating conditions for the ASC. Any bit pattern written to this register may be read back and should be identical.

Slow	$\overline{\text{SRR}}$	P Test	En P Chk	Chip Test	My Bus ID		
7	6	5	4	3	2	1	0

Configuration 1 register (Config 1) (Read/write address 08)

Bit 7 (Slow cable mode)

Bit 6 (SCSI Reset Reporting Interrupt Disable)

Bit 5 (Parity test mode)

Bit 4 (Parity enabled)

Bit 3 (Chip test mode enable)

Bit 2–0 (My bus ID)
This bitfield is the bus ID of this device.

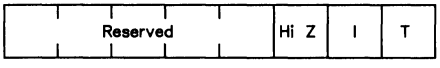
SUPERCELLS

Clock Conversion (Write address 09)

The 53C90A core requires a fixed 25 MHz clock frequency. Writing to this register will have no effect on the clock conversion factors which is fixed at 5.

Test Register (Write address 0A)

This register is enabled by setting the special test mode bit in Config 1 at address 08. After test mode has been entered, a hardware reset or software reset chip must occur before normal operation can begin.



Test register (Write address 0A)

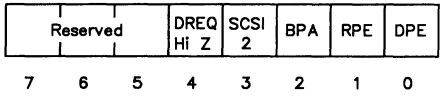
Bit 2 (All outputs to high–impedance)
When this bit is set, all bidirectional and all output pins go to high–impedance.

Bit 1 (Initiator mode)
When this bit is set, the ASC is artificially forced into initiator mode.

Bit 0 (Target mode)
When this bit is set, the ASC is artificially forced into target mode.

Configuration 2 (Config 2) (Read/write address 0B)

The 53C90A and 90B have a second configuration register that did not exist in the original C90.



Configuration 2 (Config 2) (Read/write address 0B)

Bit 4 (DREQ high–impedance)
When this bit is set, the DREQ output (DMA Request) goes to high–impedance.

When this bit is cleared, the DREQ output will be driven to TTL high or low voltages.

Bit 3 (SCSI–2)
Allows the ASC to support two new features adopted in SCSI–2: the three–byte message exchange for tagged–queuing and group 2 commands.

Bit 2 (Target bad parity abort)
When this bit is set, the ASC will abort a receive command or receive data sequence when the ASC detects a parity error.

Compatibility Verification Procedures

The design and verification of a high-level macrocell is directed towards functional compatibility with the existing standard part. The macrocell is designed and verified to match data sheet functionality (where possible), then additional steps are taken to match undocumented functionality.

Creation of a Compatibility Model

A compatibility model of the new macrocell is generated from published sources of information on the standard part including functional specifications, data sheets, applications notes, review sheets and errata sheets. Exceptions to standard part behavior or function will be identified.

A Simplified Bus-level Model for Architectural Evaluation

A simplified and reduced function bus-level model for use in the architectural evaluation of register-level transfers is generated next.

Utilization of Industry Consultants

NCR utilizes the advice of industry consultants who are highly knowledgeable about the operation of the standard part. This additional data includes features and functions which would be apparent to someone who is very familiar with the functionality of the part but would not necessarily be covered in available documentation.

Use of Hardware Modeling Techniques and Extraction of System Patterns for Design Verification

Compatibility test vectors for the part are developed from two sources. First, a hardware modeling system (HML) is generated to create test vectors based on the actual operation of the industry standard part. A second set of vectors is generated by extracting functional and timing information from the compatibility documentation and creating patterns based on this information.

In-system Test and Firmware Verification

To ensure that the macrocell is truly representative of the standard part's functionality, a system test is executed on new sample parts. The test includes the following system parameters to detect any incompatibilities or inconsistencies:

- Selection of controllers and systems
- Special test programs
- System diagnostics
- Selection of operating systems
- Selection of application programs

Final Test Plan

Throughout the compatibility verification process, final test procedures for the macrocell are emphasized. The NCR compatibility procedures provide assurance that the macrocell will function as the standard part does with documented exceptions where warranted.

Kit Parts

Provision of kit parts that are plug-compatible with the existing standard part is a very important aspect of in-system verification. The availability of kit parts allows the customer to verify macrocell operation and compatibility with the existing system design and software. They also provide a convenient way to bread-board "System Solutions in Silicon."

82077AA–Compatible Floppy Disk Controller Core Product Brief

Features

- ASIC core cell compatible with 82077AA
  - PC/AT compatible
  - PS/2 compatible
  - PS/2 Model 30 compatible
- Integrated digital data separator
  - 250 Kbits/sec
  - 300 Kbits/sec
  - 500 Kbits/sec
  - 1 Mbits/sec
- High–speed processor interface
- Perpendicular recording support
- Integrated tape drive support
- Four fully decoded drive select and motor signals
- Programmable write precompensation delays
- Addresses 256 tracks directly, supports unlimited tracks
- 16–byte FIFO
- Submicron CMOS cell–based technology
- Bus model available for Verilog Simulator
- Simulation and test patterns provided
- Combines easily with other high–level digital and analog functions
- Kit part package type: 68–pin PLCC

Product Description

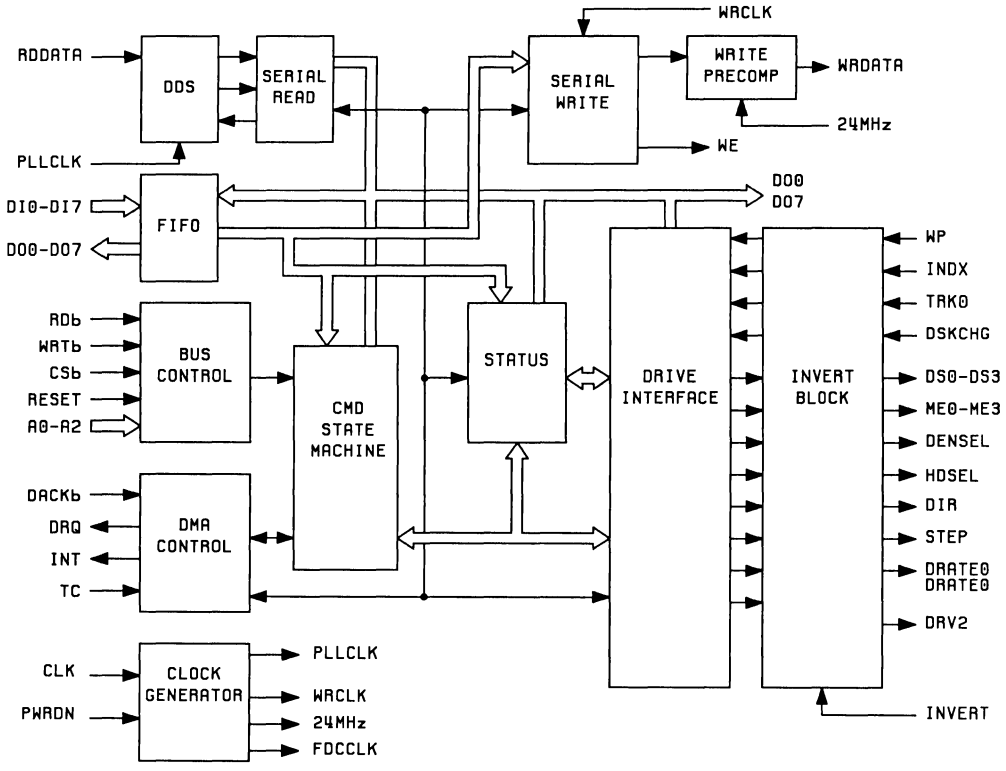
The 82077AA floppy disk controller ASIC core cell has been developed to be compatible with the 82077AA standard part. It matches the functionality of the industry standard device and is fully supported in a semicustom design environment. Bus level and gate level models as well as simulation and test vectors are available under license from NCR. Kit parts matching standard part package type are available for early system and firmware verification.

Designed with NCR's cell–based technology, the 82077AA–compatible core has integrated all of the logic required for floppy disk control and provides floppy disk and tape drive control for the PC/AT and PS/2. All drive control signals are fully decoded with selectable polarity.

The integrated digital data separator needs no external compensation yet allows for a wide motor speed variation with exceptionally low soft error rates. The microprocessor interface has a hardware register compatibility for PC/AT and PS/2 systems. The 16–byte FIFO with programmable thresholds is extremely useful in multi–master systems (PS/2, EISA) or systems with a large amount of bus latency.

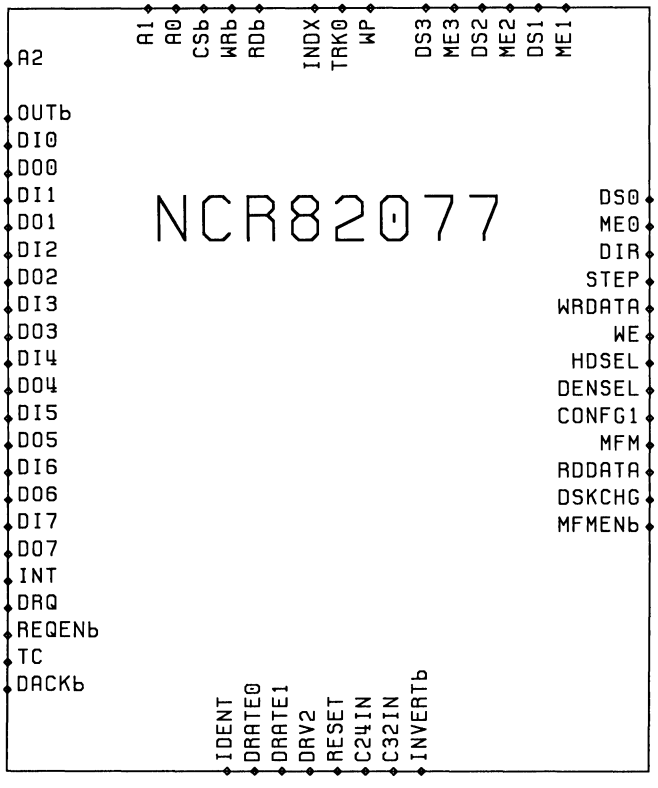
All programmable options default to compatible values. Upon reset, the 82077AA–compatible core defaults to NCR765 functionality. New features are either selected via hardware straps or new commands.

The 82077AA–compatible core is fabricated with NCR's VS700 submicron CMOS cell–based technology and is available as a kit part in a 68–pin PLCC plastic package.



Functional block diagram

Floppy Disk Controller Core



Core symbol

Inputs/Outputs

Pin Name	Type	Description
HOST INTERFACE		
RESET	I	RESET: A high level places the 82077AA in a known idle state. All registers are cleared except those set by the Specify command.
CSb	I	CHIP SELECT: Decodes base address range and qualifies RDb and WRb inputs.
A0 A1 A2	I	ADDRESS: Selects one of the host interface registers:

A2	A1	A0		Register
0	0	0	R	Status Register A
0	0	1	R	Status Register B
0	1	0	R/W	Digital Output Register
0	1	1	R/W	Tape Drive Register
1	0	0	R	Main Status Register
1	0	0	W	Data Rate Select Register
1	0	1	R/W	Data (FIFO)
1	1	0		Reserved
1	1	1	R	Digital Input Register
1	1	1	W	Configuration Control Register

DI0 – DI7	I	DATA BUS: Data bus input
DO0 – DO7	O	DATA BUS: Data bus output
OUTb	O	DATA BUS ENABLE: Control for bidirection of Data Bus
RDb	I	READ: Control signal
WRb	I	WRITE: Control signal
DRQ	O	DMA REQUEST: Requests service from a DMA controller. Normally active high, but goes to high impedance in AT and Model 30
DACKb	I	DMA ACKNOWLEDGE: Control input that qualifies the RDb, WRb inputs in DMA cycles.
TC	I	TERMINAL COUNT: Control line from a DMA controller that terminates the current disk transfer. TC is accepted only while DACKb is active.
INT	O	INTERRUPT: Signals a data transfer in non–DMA mode and when status is valid. Normally active high, but goes to high impedance in AT, and Model 30 modes when the appropriate bit is set in the DOR.
REQENb	O	REQUEST ENABLE: DOR bit to control high impedance in appropriate mode
C24IN	I	24 MHz CLOCK: Connection for a 24 MHz oscillator.
C32IN	I	32 MHz CLOCK: Connection for a 32 MHz oscillator.

(Sheet 1 of 2)

Pin Name	Type	Description
HOST INTERFACE		
IDENT	I	IDENTITY: Upon Hardware RESET, this input (along with MFM pin) selects between the three interface modes. After RESET, this input selects the type of drive being accessed and alters the level on DENSEL. The MFM pin is also sampled at Hardware RESET, and then becomes an output again. Internal pull-ups on MFM permit a no connect.

IDENT	MFM	INTERFACE
1	1 or NC	AT Mode
1	0	ILLEGAL
0	1 or NC	PS/2 Mode
0	0	Model 30 Mode

AT MODE: Major options are: enables DMA Gate logic. TC is active high, Status Registers A & B not available.
PS/2 MODE: Major options are: No DMA Gate logic, TC is active low, Status Registers A & B are available.
MODEL 30 MODE: Major options are: enable DMA Gate logic, TC is active high, Status Registers A & B available.
After Hardware reset this pin determines the polarity of the DENSEL pin. IDENT at a logic level of "1", DENSEL will be active high for high (500 Kbps/1 Mbps) data rates (typically used for 5.25" drives). IDENT at a logic level of "0", DENSEL will be active low for high data rates (typically used for 3.5" drives).

(Sheet 2 of 2)

Pin Name	Type	Description
PLL SECTION		
RDDATA	I	READ DATA: Serial data from the disk. INVERT also affects the polarity of this signal.
MFM	I/O	MFM: At Hardware RESET, aids in configuring the 82077AA. Internal pull-up allows a no connect if a "1" is required. After reset this pin becomes an output and indicates the current data encoding/decoding mode (Note: If the pin is held at logic level "0" during hardware RESET, it must be pulled to "1" after reset to enable the output. The pin can be released on the falling edge of hardware RESET to enable the output). MFM is active high (MFM). MFM may be left tied low after hardware reset, in this case the MFM function will be disabled.
CONFIG	I	CONFIG: The input signal of the core for the MFM I/O description
MFMENb	O	MFM ENABLE: Control for bidirection of MFM
DRATE0 DRATE1	O	DATARATE0-1: Reflects the contents of bits 0, 1 of the Data Rate Register.

Pin Name	Type	Description
DISK CONTROL		
INVERTb	I	INVERT: Strapping option. Determines the polarity of all signals in this section. Should be strapped to ground when using the internal buffers and these signals become active LOW. When strapped to V_{CC}, these signals become active high and external inverting drivers and receivers are required.
ME0 ME1 ME2 ME3	O	ME0–3: Decoded Motor enables for drives 0–3. The motor enable pins are directly controlled via the Digital Output Register.
DS0 DS1 DS2 DS3	O	DRIVE SELECT 0–3: Decoded drive selects for drives 0–3. These outputs are decoded from the select bits in the Digital Output Register and gated by ME0–3.
HDSEL	O	HEAD SELECT: Selects which side of a disk is to be used. An active level selects side 1.
STEP	O	STEP: Supplies step pulses to the drive.
DIR	O	DIRECTIONS: Controls the direction the head moves when a step signal is present. The head moves toward the center if active.
WRDATA	O	WRITE DATA: MFM serial data to the drive. Precompensation value is selectable through software.
WE	O	WRITE ENABLE: Drive control signal that enables the head to write onto the disk.
DENSEL	O	DENSITY SELECT: Indicates whether a low (250/300 Kbps) or high (500 Kbps/1 Mbps) data rate has been selected.
DSKCHG	I	DISK CHANGE: This input is reflected in the Digital Input Register.
DRV2	I	DRIVE2: This indicates whether a second drive is installed and is reflected in Status Register A.
TRK0	I	TRACK0: Control line that indicates that the head is on track 0.
WP	I	WRITE PROTECT; Indicates whether the disk is write protected.
INDX	I	INDES: Indicates the beginning of the track.

Floppy Disk Controller Core

Status, Data and Control Registers

The base address range is supplied via the CSb pin. For PC/AT or PS/2 designs this would be 3F0 Hex to 3F7 Hex.

A2	A1	A0		Register	
0	0	0	R	Status Register A	SRA
0	0	1	R	Status Register B	SRB
0	1	0	R/W	Digital Output Register	DOR
0	1	1	R/W	Tape Drive Register	TSR
1	0	0	R	Main Status Register	MSR
1	0	0	W	Data Rate Select Register	DSR
1	0	1	R/W	Data (FIFO)	FIFO
1	1	0		Reserved	
1	1	1	R	Digital Input Register	DIR
1	1	1	W	Configuration Control Register	CCR

Status Register A (SRA, PS/2 Mode)

7	6	5	4	3	2	1	0
INT PENDING	DRV2b	STEP	TRKOb	HDSEL	INDXb	WPb	DIR

Status Register A (SRA, Model 30 Mode)

7	6	5	4	3	2	1	0
INT PENDING	DRQ	STEP F/F	TRKOb	HDSELb	INDX	WP	DIRb

Status Register B (SRB, PS/2 Mode)

This register is read-only and monitors the state of several disk interface pins. This register is part of the PS/2 register set, and is not accessible in PC/AT mode.

7	6	5	4	3	2	1	0
1	1	DRIVE SEL 0	WRDATA TOGGLE	RDDATA TOGGLE	WE	MOT EN 1	MOT EN 0

Status Register B (SRB, Model 30 Mode)

7	6	5	4	3	2	1	0
DRV2b	DS1b	DS0b	WRDATA F/F	RDDATA F/F	WE F/F	DS3b	DS2b

Digital Output Register (DOR)

The Digital Output Register contains the drive select and motor enable bits, a reset bit and a DMAb GATEb bit.

7	6	5	4	3	2	1	0
MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAb GATEb	RESETb	DRIVE SEL 1	DRIVE SEL 0

Tape Drive Register (TDR)

This register allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. This register is cleared by hardware reset. Software resets have no effect.

7	6	5	4	3	2	1	0
–	–	–	–	–	–	Tape SEL 1	Tape SEL 0

Data Rate Select Register (DSR)

This register is included for compatibility with the 82072 floppy controller and is write–only. Changing the data rate changes the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing.

7	6	5	4	3	2	1	0
S/W RESET	POWER DOWN	0	PRE–COMP 2	PRE–COMP 1	PRE–COMP 0	DRATE SEL 1	DRATE SEL 0

Main Status Register (MSR)

The Main Status Register is read–only register and is used for controlling command input and result output for all commands.

7	6	5	4	3	2	1	0
ROM	DIO	NON DMA	CMD BSY	DRV 3 BUSY	DRV 2 BUSY	DRV 1 BUSY	DRV 0 BUSY

FIFO (Data)

All command parameter information and disk data transfers go through the FIFO. The FIFO is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

Digital Input Register (DIR, PC/AT Mode)

7	6	5	4	3	2	1	0
DSK CHG	–	–	–	–	–	–	–

Digital Input Register (DIR, PS/2 Mode)

7	6	5	4	3	2	1	0
DSK CHG	1	1	1	1	DRATE SEL 1	DRATE SEL 0	HIGHb DENSb

Digital Input Register (DIR, Model 30 Mode)

7	6	5	4	3	2	1	0
DSKb CHGb	0	0	0	DMAb GATEb	NOPREC	DRATE SEL 1	DRATE SEL 0

Configuration Control Register (CCR, PC/AT and PS/2 Modes

This register sets the data rate and is write–only. In the PC/AT it is named the DSR.

7	6	5	4	3	2	1	0
–	–	–	–	–	–	DRATE SEL 1	DRATE SEL 0

Configuration Control Register (CCR, Model 30 Mode)

7	6	5	4	3	2	1	0
–	–	–	–	–	NOPREC	DRATE SEL 1	DRATE SEL 0

Compatibility Verification Procedures

The design and verification of a high-level macrocell is directed towards functional compatibility with the existing standard part. The macrocell is designed and verified to match data sheet functionality (when possible), then additional steps are taken to match undocumented functionality.

Creation of a Compatibility Model

A compatibility model of the new macrocell is generated from published sources of information on the standard part including functional specifications, existing data sheets, applications notes, review sheets and errata sheets. This base-line model is used as the standard against which all test data are later compared.

A Bus-level Model for Architectural Evaluation

A bus-level model for use in the architectural evaluation of register-level transfers is generated next.

Utilization of Industry Consultants

NCR utilizes the advice of industry consultants who are highly knowledgeable about the operation of the standard part. This additional data includes features and functions which would be apparent to someone who is very familiar with the functionality of the part but would not necessarily be covered in available documentation.

Use of Hardware Modeling Techniques and Extraction of System Patterns for Design Verification

Compatibility test vectors for the part are developed from two sources. First, a hardware modeling system (HML) is generated to create test vectors based on the actual operation of the industry standard part. A second set of vectors is generated by extracting functional and timing information from the compatibility documentation and creating patterns based on this information.

In-system Test and Firmware Verification

To ensure that the macrocell is truly representative of the standard part's functionality, a system test is executed on new sample parts. The test includes the following system parameters to detect any incompatibilities or inconsistencies:

- Selection of controllers and systems
- Special test programs
- System diagnostics
- Selection of operating systems
- Selection of application programs

Final Test Plan

Throughout the compatibility verification process, final test procedures for the macrocell are emphasized. The NCR compatibility procedures provide assurance that the macrocell will function as the standard part does.

Kit Parts

Provision of kit parts that are plug-compatible with the existing standard part is a very important aspect of in-system verification. The availability of kit parts allows the customer to verify macrocell operation and compatibility with the existing system design and software. They also provide a convenient way to bread-board "System Solutions in Silicon."

85C30–Compatible Serial Communications Core Product Brief

Features

- ASIC core cell compatible with NMOS 8530
- Dual channel
- Two full–duplex channels
- Independent modem controls in each channel
- Parallel–to–serial or serial–to–parallel
- On–chip baud rate generators
- Digital phase–locked loops
- Asynchronous mode features
  - Programmable stop bits, clock factor, character length and parity
  - Break detection/generation
  - Error detection for framing, overrun and parity
- Synchronous mode features
  - Supports IBM BISYNC, SDLC, SDLC loop, HDLC and ADCCP protocols
  - Programmable CRC generators and checkers
  - SDLC/HDLC support includes frame control, zero insertion and deletion, abort and residue handling
- Generates and checks CRC codes
- Easily interfaced to most CPU's
- Submicron CMOS cell–based technology
- Combines easily with other high–level digital and analog functions
- Bus model for Verilog simulator
- Simulation and test patterns provided
- Kit parts with pinout identical to standard part
- Kit part package type: 40– or 44–pin PLCC

Product Description

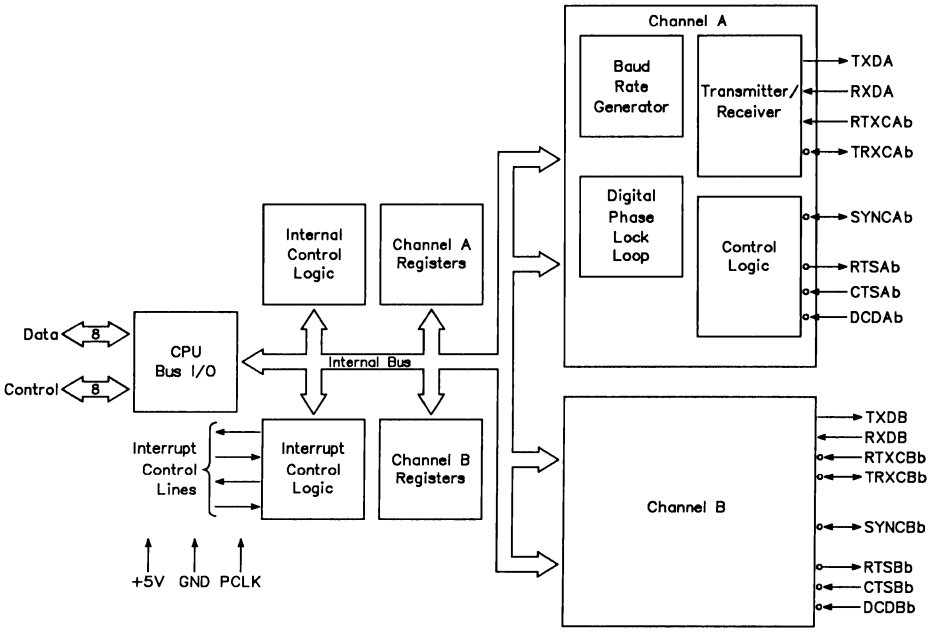
The 85C30–compatible Serial Communications ASIC core cell has been developed to be compatible with the NMOS 8530. It matches the functionality of the industry standard device and is fully supported in a semicustom design environment. Bus level and gate level models as well as simulation and test vectors are available under license from NCR. Kit parts matching standard part pinouts and package type are available for early system and firmware verification.

Designed with NCR's cell–based technology, the 85C30–compatible Serial Communications Core operates as a dual channel, multiprotocol data communications peripheral. It can function in either serial–to–parallel or parallel–to–serial mode. It can be configured to meet a wide variety of serial communications applications, including full and half–duplex architectures, token passing ring (SDLC loop mode), or star configurations.

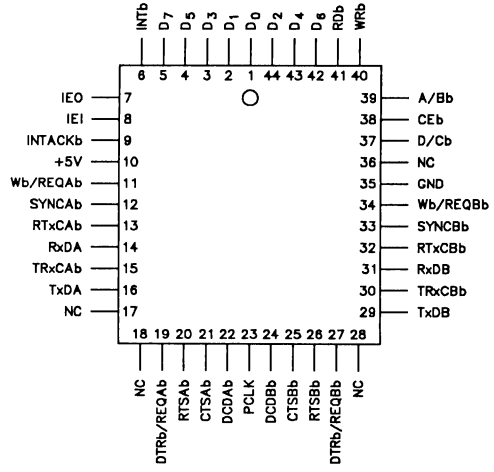
Internal functions which have been integrated into the 85C30–compatible Serial Communications Core include on–chip baud rate generators and digital phase–locked loops. The 85C30–compatible Serial Communications Core can be formatted for asynchronous or synchronous operation with character–oriented protocols such as IBM BISYNC or bit–oriented protocols like HDLC and SDLC, all possible in the synchronous mode.

The 85C30–compatible Serial Communications Core has access to 14 Write registers and 7 Read registers per channel.

The 85C30–compatible Serial Communications Core is fabricated using NCR's VS700 submicron CMOS cell–based technology and will be available as a kit part in a 40– or 44–pin PLCC plastic package in 1991.



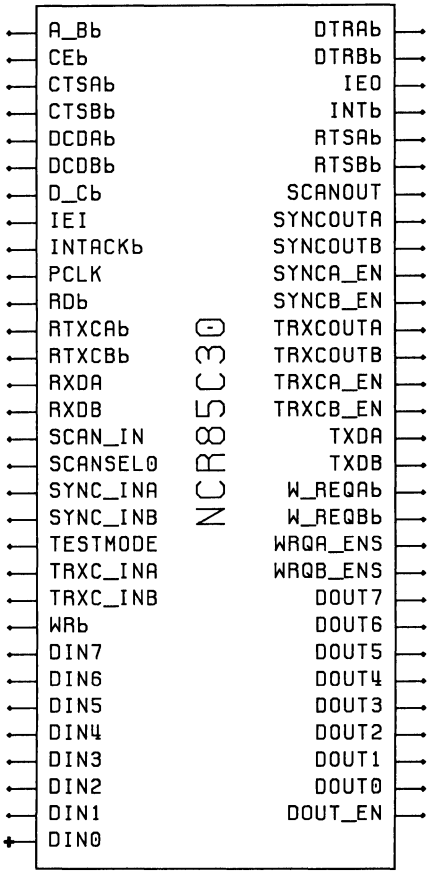
Functional block diagram



Kit part pinout

SUPERCELLS

Serial Communications Core



Core symbol

Inputs/Outputs Table

Pin Name	Type	Description
A_Bb	I	CHANNEL SELECT: A high level on this signal selects Channel A for read or write operations. A low level selects Channel B.
CEb	I	CELL ENABLE: A low level on CEb selects the cell for read or write operation.
CTSAb CTSBb	I I	CLEAR TO SEND: In Auto Enable mode, these signals will enable their respective transmitter when activated low. Otherwise, these signals can be used as general purpose inputs.
DCDAb DCDBb	I I	DATA CARRIER DETECT: In Auto Enable mode, these signals will enable their respective receivers when activated low. Otherwise, these signals can be used as general purpose inputs.
D_Cb	I	DATA/CONTROL SELECT: A high on D_Cb indicates a data transfer operation during a read or write. A low indicates a control operation.
IEI	I	INTERRUPT ENABLE IN: IEI is used with the IEO signal to form an interrupt daisy chain. A high on IEI indicates that no higher priority device has an interrupt request or an interrupt under service.
INTACKb	I	INTERRUPT ACKNOWLEDGE: A low on INTACKb indicates that the succeeding read will be part of an interrupt acknowledge cycle. If IEI is high, the interrupt vector will be placed on the data bus.
PCLK	I	MASTER CLOCK: Master clock signal which allows synchronous operation of the control logic.
RDb	I	READ: A low RDb signal performs a read if the cell is selected. Internal data will be driven onto the data bus. A low on RDb and WRb simultaneously performs a reset.
RTXCAb RTXCBb	I I	RECEIVE/TRANSMIT CLOCKS: These signals can be programmed to be the source clock for the receiver, transmitter, baud rate generator, or the digital phase lock loop in their respective channels.
RXDA RXDB	I I	RECEIVE DATA: These signals receive the serial input stream for their respective channels.
SCANIN	I	SCAN INPUT: When TESTMODE is high, this signal supplies the input to serial partial scan chains to aid in fault testing.
SCANSELO	I	SCAN SELECT: When TESTMODE is high, this signal selects between two internal partial scan chains.
SYNC_INA SYNC_INB	I I	SYNC INPUT: In async mode, these signals control the status of the SYNC/HUNT bit in register 0. In External Sync Mode, these signals are used for character synchronization.
TESTMODE	I	TEST MODE ENABLE: A high on this signal allows the operation of the internal partial scan chains for test purposes. This signal must be forced low for normal operation.
TRXC_INA TRXC_INB	I I	TRANSMIT/RECEIVE CLOCK INPUT: These signals can supply the clock input for the receiver or transmitter if programmed appropriately for their respective channels.
WRb	I	WRITE: A low on this signal indicates a write operation. A low on the WRb and RDb simultaneously performs a reset.
DIN0 – DIN7	I	DATA INPUTS: These signals are the write data inputs for commands or data transfer.

(Sheet 1 of 2)

Serial Communications Core

Pin Name	Type	Description
DOUT0 – DOUT7	O	DATA OUTPUTS: These signals are the data outputs which provide the results of a read operation. These signals can be used with the DIN and DOUT_EN signal to form a bi–directional bus.
DOUT_EN	O	DATA OUTPUT ENABLE: A high on this signal indicates that a valid read operation is active. The DOUT_EN signal can be used to control tristate drivers to form a bi–directional data bus.
DTRAb DTRBb	O O	DATA TERMINAL READY/DMA REQUEST: These signals follow the inverse of the DTR bit in Write Register 5 if programmed for the DTR function in Register 14. This signal can also act as a DMA request if so programmed in Register 14.
IEO	O	INTERRUPT ENABLE OUTPUT: This signal is used with IEI to form an interrupt daisy chain. This signal is high if IEI is high and the controller is servicing an interrupt or has an interrupt pending.
INTb	O	INTERRUPT: A low on INTb indicates an interrupt is pending.
RTSAb RTSBb	O O	REQUEST TO SEND: When in Auto Enable and Async Mode, this signal will go high after the transmitter is empty. Otherwise this signal follows the inverse of the RTS bit in Register 5.
SCANOUT	O	SCAN OUTPUT: This signal scans out the result of the internal partial scan chain.
SYNC_OUTA SYNC_OUTB	O O	SYNC OUTPUT: These signals are active low when the proper sync character or flag has been received in the Synchronous or SDLC modes, respectively.
SYNCA_EN SYNCB_EN	O O	SYNC OUTPUT ENABLE: These signals can be used with the SYNC_IN and SYNC_OUT pins to create a bi–directional SYNC pin. A high on this signal indicates an output.
TRXC_OUTA TRXC_OUTB	O O	TRANSMIT/RECEIVE CLOCK OUTPUT: These signals can be programmed to output the transmitter clock, the baud rate generator output, the digital phase lock loop output, or the oscillator output.
TRXCA_EN TRXCB_EN	O O	TRXC OUTPUT ENABLE: These signals can be used with the TRXC_IN and TRXC_OUT signals to form a bi–directional TRXC pin. A high on this signal indicates an output.
TXDA TXDB	O O	TRANSMIT DATA: These signals are the transmitter serial output data for their respective channels.
W_REQAb W_REQBb	O O	WAIT/REQUEST: These signals can be used as a Wait signal to the CPU or as a DMA request per programming of Write Register 1.
W_REQA_ENS W_REQB_ENS	O O	WAIT/REQUEST ENABLE STRENGTH: These signals can be used with the W_REQb signals to recreate the varied strength of the high level on the W_REQb pin. A high indicates a driving signal, a low indicates a floating signal.

(Sheet 2 of 2)

Register Description

The following sections describe the NCR 85C30 SCC registers. Each register is detailed in terms of bit configuration, the active states (see below) of each bit, their definitions, their functions and their effects upon the internal hardware and external pins.

Note: In the write and read register tables (1–25) that follow, the symbol "•" means that the designated bit corresponds to the particular status/function specified in the "signal" column.

Read Register	Description
RR0	Transmit/Receive Buffer Status and External Status
RR1	Receive Condition Status/Residue Codes
RR2	Interrupt Vector (Modified in B Channel)
RR3	Interrupt Pending (Channel A only)
RR8 *	Receive Buffer
RR10	Loop/Clock Status
RR12	Lower Byte of Time Constant
RR13	Upper Byte of Time Constant
RR15	External Status Interrupt Enable

* Can also be selected by driving D_Cb high during access

Write Register	Description
WR0	Command Register
WR1	TX/RX Interrupt and Data Transfer Mode Definition
WR2	Interrupt Vector
WR3	Receive Parameters and Control
WR4	TX/RX Miscellaneous Parameters and Modes
WR5	Transmit Parameter and Controls
WR6	Sync Character or SDLC Address Field
WR7	Sync Character or SDLC Flag
WR8 *	Transmit Buffer
WR9	Master Interrupt Control
WR10	Miscellaneous Transmitter/Receiver Control Bits
WR11	Clock Mode Control
WR12	Lower Byte of Baud Rate Generator Time Constant
WR13	Upper Byte of Baud Rate Generator Time Constant
WR14	Miscellaneous Control Bits
WR15	External Status/Interrupt Control

* Can also be selected by driving D_Cb high during access

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Register 0						0	0	0
Register 1						0	0	1
Register 2						0	1	0
Register 3						0	1	1
Register 4						1	0	0
Register 5						1	0	1
Register 6						1	1	0
Register 7						1	1	1
Register 8*						0	0	0
Register 9*						0	0	1
Register 10*						0	1	0
Register 11*						0	1	1
Register 12*						1	0	0
Register 13*						1	0	1
Register 14*						1	1	0
Register 15*						1	1	1
Null Code			0	0	0			
Point High			0	0	1			
Reset EXT/Status Interrupts			0	1	0			
Send Abort (SDLC)			0	1	1			
Enable Int on Next R_X Character			1	0	0			
Reset T_X INT Pending			1	0	1			
Error Reset			1	1	0			
Reset Highest IUS			1	1	1			
Null Code	0	0						
Reset R_X CRC Checker	0	1						
Reset T_X CRC Generator	1	0						
Reset T_X Underrun/EOM Latch	1	1						
*with point high command								

TABLE 8–1 Write register 0 – Signal bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Ext Int Enable								•
T_X Int Enable							•	
Parity is special condition						•		
R_X Int Disable				0	0			
R_X Int on first character or special condition				0	1			
Int on all R_X characters or special condition				1	0			
RX Int on special condition only				1	1			
Wait/DMA request on Receive/Transmit			•					
$\overline{\text{Wait}}$/DMA request function		•						
Wait/DMA request enable	•							

TABLE 8–2 Write register 1 – Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

TABLE 8–3 Write register 2 – Interrupt vector

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R_X Enable								•
Sync character Load Inhibit							•	
Address Search Mode (SDLC)						•		
RX CRC Enable					•			
Enter hunt mode				•				
Auto Enables			•					
R_X 5 Bits/Character	0	0						
R_X 7 Bits/Character	0	1						
R_X 6 Bits/Character	1	0						
R_X 8 Bits/Character	1	1						

TABLE 8–4 Write register 3 – Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Parity Enable								•
Parity Even/Odd							•	
Sync Modes Enable					0	0		
1-Stop Bit/Character					0	1		
1.5-Stop Bits/Character					1	0		
2-Stop Bits/Character					1	1		
8-bit Sync Character			0	0				
16-bit Sync Character			0	1				
SDLC Mode (01111110) Flag)			1	0				
External Sync Mode			1	1				
X1 Clock Mode	0	0						
X16 Clock Mode	0	1						
X32 Clock Mode	1	0						
X64 Clock Mode	1	1						

TABLE 8-5 Write register 4 - Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Tx CRC Enable								•
RTS							•	
SDLC/CRC-16						•		
Tx Enable					•			
Send Break				•				
Tx 5 Bits (or less)/Character		0	0					
Tx 7 Bits/Character		0	1					
Tx 6 Bits/Character		1	0					
Tx 8 Bits/Character		1	1					
DTR	•							

TABLE 8-6 Write register 5 - Signal/bit combinations

Protocol	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Monosync, 8 bits	$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$
Monosync, 6 bits	$SYNC_1$	$SYNC_0$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$
Bisync, 16 bits	$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$
Bisync, 12 bits	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	1	1	1	1
SDLC	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
SDLC, (address range)	ADR7	ADR6	ADR5	ADR4	X	X	X	X

TABLE 8–7 Write register 6 – Protocols

Protocol	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Monosync, 8 bits	$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$
Monosync, 6 bits	$SYNC_5$	$SYNC_4$	$SYNC_3$	$SYNC_2$	$SYNC_1$	$SYNC_0$	X	X
Bisync, 16 bits	$SYNC_{15}$	$SYNC_{14}$	$SYNC_{13}$	$SYNC_{12}$	$SYNC_{11}$	$SYNC_{10}$	$SYNC_9$	$SYNC_8$
Bisync, 12 bits	$SYNC_{10}$	$SYNC_{10}$	$SYNC_9$	$SYNC_8$	$SYNC_7$	$SYNC_6$	$SYNC_5$	$SYNC_4$
SDLC	0	1	1	1	1	1	1	0

TABLE 8–8 Write register 7 – Protocols

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
VIS								•
NV							•	
DLC						•		
MIE					•			
Status High/$\overline{\text{Status Low}}$				•				
0			•					
No Reset	0	0						
Channel Reset B	0	1						
Channel Reset A	1	0						
Force Hardware Reset	1	1						

TABLE 8–9 Write register 9 – Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
6-bit/$\overline{8\text{-bit}}$ Sync								•
Loop Mode							•	
Abort/$\overline{\text{Flag}}$ on underrun						•		
Mark/$\overline{\text{Flag}}$ Idle					•			
Go Active on Poll				•				
NRZ		0	0					
NRZI		0	1					
FM1 (Transition = 1)		1	0					
FM0 (Transition = 0)		1	1					
CRC Preset 1/0	•							

TABLE 8-10 Write register 10 - Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{\text{TRxC}}$ Out = XTAL Output							0	0
$\overline{\text{TRxC}}$ Out = Transmit Clock							0	1
$\overline{\text{TRxC}}$ = BR Generator Output							1	0
$\overline{\text{TRxC}}$ Out = DPLL Output							1	1
$\overline{\text{TRxC}}$ O/$\overline{\text{I}}$						•		
Transmit Clock = $\overline{\text{RTxC}}$ Pin				0	0			
Transmit Clock = $\overline{\text{TRxC}}$ Pin				0	1			
Transmit Clock = BR Generator Output				1	0			
Transmit Clock = DPLL Output				1	1			
Receive Clock = $\overline{\text{RTxC}}$ Pin		0	0					
Receive Clock = $\overline{\text{TRxC}}$ Pin		0	1					
Receive Clock = BR Generator Output		1	0					
Receive Clock = DPLL Output		1	1					
$\overline{\text{RTxC}}$ XTAL/$\overline{\text{NO XTAL}}$	•							

TABLE 8-11 Write register 11 - Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Time Constant (Lower Byte)	TC_7	TC_6	TC_5	TC_4	TC_3	TC_2	TC_1	TC_0

TABLE 8–12 Write register 12 – Time constant bits (lower byte)

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Time Constant (Upper Byte)	TC_{15}	TC_{14}	TC_{13}	TC_{12}	TC_{11}	TC_{10}	TC_9	TC_8

TABLE 8–13 Write register 13 – Time constant bits (upper byte)

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
BR Generator Enable								•
BR Generator Source							•	
$\overline{DTR}$/Request Function						•		
Auto Echo					•			
Local Loopback				•				
Null Command	0	0	0					
Enter Search Mode	0	0	1					
Reset Missing Clock	0	1	0					
Disable DPLL	0	1	1					
Set Source = BR Generator	1	0	0					
Set Source = $\overline{RTxC}$	1	0	1					
Set FM Mode	1	1	0					
Set NRZI Mode	1	1	1					

TABLE 8–14 Write register 14 – Signal/bit combinations

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0								•
Zero Count IE							•	
0						•		
DCD IE					•			
Sync/Hunt IE				•				
CTS IE			•					
T_X Underrun/EOM IE		•						
Break/Abort IE	•							

TABLE 8–15 Write register 15 – Signal bits

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
R_X Character Available								•
Zero Count IE							•	
T_X Buffer Empty						•		
DCD					•			
Sync/Hunt				•				
CTS			•					
T_X Underrun/EOM		•						
Break/Abort	•							

TABLE 8–16 Read register 0 – Signal bits

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
All Sent								•
Residue Code 2							•	
Residue Code 1						•		
Residue Code 0					•			
Parity Error				•				
R_X Overrun Error			•					
CRC/Framing Error		•						
End of Frame (SDLC)	•							

TABLE 8–17 Read register 1 – Signal bits

	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector*	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0

* Modified in B channel

TABLE 8–18 Read register 2 – Interrupt vector

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Channel B EXT/STAT IP *								•
Channel B T_X IP *							•	
Channel B R_X IP *						•		
Channel A EXT/STAT IP *					•			
Channel A T_X IP *				•				
Channel A R_X IP *			•					
0		•						
0	•							

* Always 0 in B channel

TABLE 8–19 Read register 3 – Signal bits

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0								•
On Loop							•	
0						•		
0					•			
Loop Sending				•				
0			•					
Two Clocks Missing		•						
One Clock Missing	•							

TABLE 8–20 Read register 10 – Signal bits

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Time Constant (Lower Byte)	TC_7	TC_6	TC_5	TC_4	TC_3	TC_2	TC_1	TC_0

TABLE 8–21 Read register 12 – Time constant bits (lower byte)

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Time Constant (Upper Byte)	TC_{15}	TC_{14}	TC_{13}	TC_{12}	TC_{11}	TC_{10}	TC_9	TC_8

TABLE 8–22 Read register 13 – Time constant bits (upper byte)

Signal	Register MSB ← LSB							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0								•
Zero Count IE							•	
0						•		
DCD IE					•			
Syn/Hunt IE				•				
CTS IE			•					
T_X Underrun/EOM IE		•						
Break/Abort IE	•							

TABLE 8–23 Read register 15 – Signal bits

Compatibility Verification Procedures

The design and verification of a high-level macrocell is directed towards functional compatibility with the existing standard part. The macrocell is designed and verified to match data sheet functionality (when possible), then additional steps are taken to match undocumented functionality.

Creation of a Compatibility Model

A compatibility model of the new macrocell is generated from published sources of information on the standard part including functional specifications, data sheets, application notes, review sheets and errata sheets. Exceptions to standard part behavior or function will be identified.

Simplified Bus-level Model for Architectural Evaluation

A simplified and reduced function bus-level model for use in the architectural evaluation of register-level transfers is generated next.

Utilization of Industry Consultants

NCR utilizes the advice of industry consultants who are highly knowledgeable about the operation of the standard part. This additional data includes features and functions which would be apparent to someone who is very familiar with the functionality of the part but would not necessarily be covered in available documentation.

Use of Hardware Modeling Techniques and Extraction of System Patterns for Design Verification

Compatibility test vectors for the part are developed from two sources. First, a hardware modeling system (HML) is generated to create test vectors based on the actual operation of the industry standard part. A second set of vectors is generated by extracting functional and timing information from the compatibility documentation and creating patterns based on this information.

In-system Test and Firmware Verification

To ensure that the macrocell is truly representative of the standard part's functionality, a system test is executed on new sample parts. The test includes the following system parameters to detect any incompatibilities or inconsistencies:

- Selection of controllers and systems
- Special test programs
- System diagnostics
- Selection of operating systems
- Selection of application programs

Final Test Plan

Throughout the compatibility verification process, final test procedures for the macrocell are emphasized. The NCR compatibility procedures provide assurance that the macrocell will function as the standard part does with documented exceptions where warranted.

Kit Parts

Provision of kit parts that are plug-compatible with the existing standard part is a very important aspect of in-system verification. The availability of kit parts allows the customer to verify macrocell operation and compatibility with the existing system design and software. They also provide a convenient way to bread-board "System Solutions in Silicon."

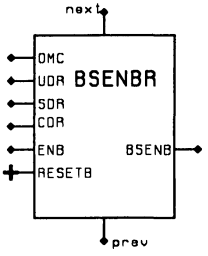
BSENBR

Boundary Scan Cell for Tristate Enable

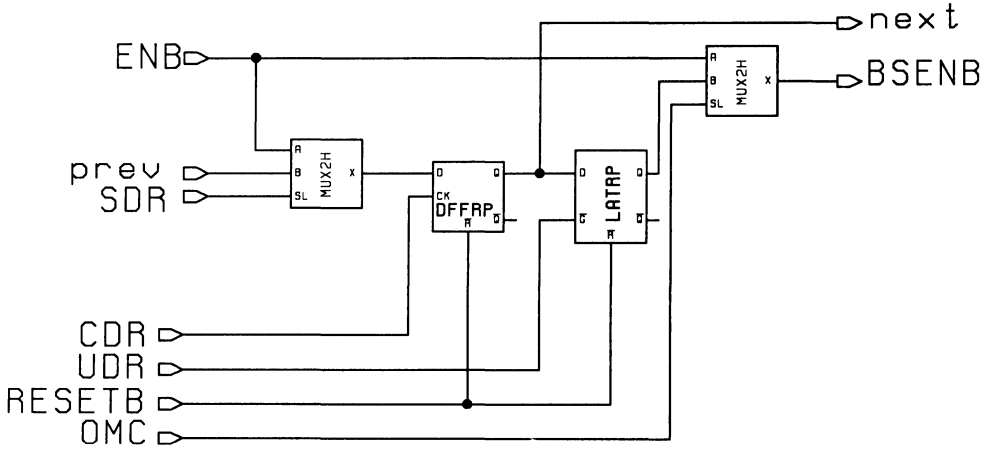
Description

The BSENBR is a boundary scan cell for use with pad tristate enable signals. It contains a scan element and a shadow latch for the element. When the output mode control (OMC) is low, the on-chip system pad enable-bar value is passed from ENB to BSENB. BSENB is connected to the ENB input of the desired tristate or input/output boundary scan cell (BSOTR4, BSIOR8, etc.). When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. Note that only one BSENBR cell is needed if all pads are controlled with a common tristate enable. See application note for an example boundary scan data register using this cell.

Symbol

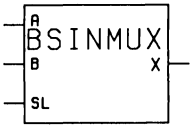


Schematic



Boundary Scan 2–Input Multiplexer

BSINMUX is a two-input multiplexer which, when connected directly to the DI output of a pad cell (INPD, IPPD, IOPDX, IOPPDX), provides minimum delays for input paths used in boundary scan applications. Performance has been optimized (minimum delay) for the A to X delay path. This cell provides no voltage level shifting. The output pin, X, must be connected to the input of an input buffer (INBUF, DS1218, IIBUF, etc.). Refer to boundary scan macrocell data sheets and application notes for additional information regarding use of this cell.



A	B	SL	X
H	X	L	H
L	X	L	L
X	H	H	H
X	L	H	L

Function table

Inputs: A, B, SL
Outputs: X
Input Cap.: A: 1.160
B: 0.320
SL: 0.430 pF
Timing
Constants: K = 2.00ns
M_{CLH} = 0.000 M_{CHL} = 0.000
Process
Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 28.0 grids wide, 15.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.040	0.075	0.078	0.088
t_{PHL}		0.044	0.082	0.085	0.095
t_{PLH}	B to X	0.215	0.402	0.419	0.470
t_{PHL}		0.208	0.388	0.404	0.453
t_{PLH}	SL to X	0.064	0.119	0.125	0.140
t_{PHL}		0.405	0.755	0.787	0.884

Timing characteristics

BSINMUX

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.033	0.073
t_{PHL}		0.033	0.107
t_{PLH}	B to X	0.148	0.673
t_{PHL}		0.139	0.687
t_{PLH}	SL to X	0.054	0.100
t_{PHL}		0.334	0.707

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	2.16	0.073	2.12	0.000

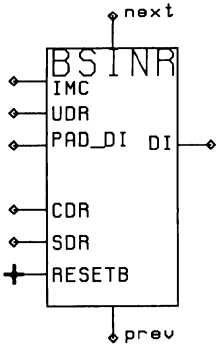
Rise/fall time coefficients for the next cell

Boundary Scan Cell for Input Pads

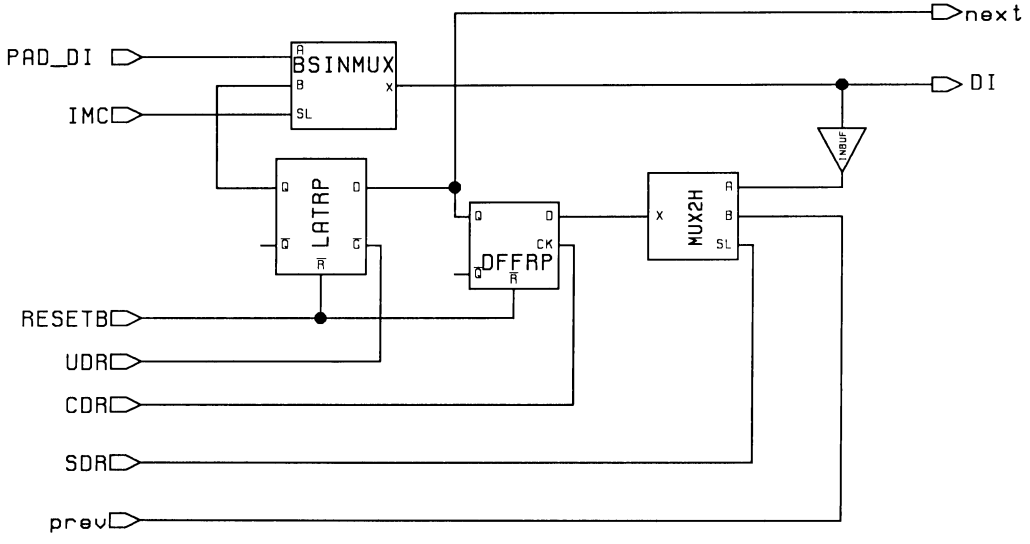
Description

The BSINR is a boundary scan cell for input pads. It contains a scan element and a shadow latch for the element. When the input mode control (IMC) is low, the input pad's value is passed into the on-chip system logic from PAD_DI to DI. When UDR goes low, then high, it latches the scan elements data. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. For best performance, PAD_DI must be connected directly to the DI output of an input pad. The DI output of the BSINR must then be connected to one or more input buffers (INBUF, HBUF, DS1216, etc.).

Symbol



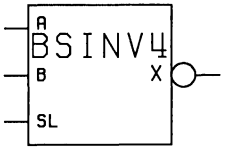
Schematic



SUPERCELLS

Boundary Scan Inverting 2–Input Multiplexer (4X Drive)

BSINV4 is a two–input multiplexer for use in boundary scan applications to drive output pad cells with only one input pin (OPDx, ODPDx, ONPDx, IONPD48). Its drive is equivalent to an OUTINV cell and its performance has been optimized (minimum delay) for the A to X delay path. Refer to boundary scan macrocell data sheets and application notes for additional information regarding use of this cell.



A	B	SL	X
H	X	L	L
L	X	L	H
X	H	H	L
X	L	H	H

Function table

Inputs: A, B, SL
Outputs: X
Input Cap.: A: 0.257
B: 0.072
SL: 0.246 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.144 M_{CHL} = 0.146
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 10.0 grids wide, 12.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.239	0.456	0.476	0.536
t_{PHL}		0.219	0.418	0.436	0.491
t_{PLH}	B to X	0.837	1.57	1.64	1.84
t_{PHL}		0.829	1.56	1.62	1.82
t_{PLH}	SL to X	1.08	2.03	2.11	2.37
t_{PHL}		0.426	0.804	0.839	0.943

Timing characteristics

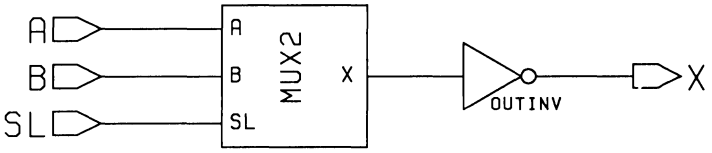
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.131	0.476
t_{PHL}		0.122	0.353
t_{PLH}	B to X	0.583	1.94
t_{PHL}		0.622	1.46
t_{PLH}	SL to X	0.819	2.00
t_{PHL}		0.327	0.372

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.223	1.10	0.093	0.694

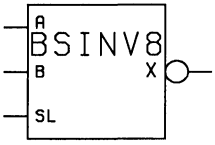
Rise/fall time coefficients for the next cell



Functional diagram: BSINV4

Boundary Scan Inverting 2–Input Multiplexer (8X Drive)

BSINV8 is a two–input multiplexer for use in boundary scan applications to drive output pad cells with only one input pin (OPDx, ODPDx, ONPDx, IONPD48). Its drive is equivalent to an INV8 cell and its performance has been optimized (minimum delay) for the A to X delay path. Refer to boundary scan macrocell data sheets and application notes for additional information regarding use of this cell.



A	B	SL	X
H	X	L	L
L	X	L	H
X	H	H	L
X	L	H	H

Function table

Inputs: A, B, SL
Outputs: X
Input Cap.: A: 0.509
B: 0.128
SL: 0.431 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.095 M_{CHL} = 0.113
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 17.0 grids wide, 12.4 grids high

(Input t_r,t_f= 0.5ns nominal, C_L= 0.1pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	A to X	0.206	0.391	0.408	0.459
t_{PHL}		0.203	0.386	0.403	0.453
t_{PLH}	B to X	0.661	1.24	1.29	1.45
t_{PHL}		0.625	1.17	1.22	1.37
t_{PLH}	SL to X	1.04	1.95	2.03	2.28
t_{PHL}		0.551	1.04	1.08	1.21

Timing characteristics

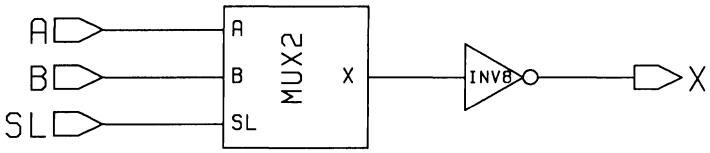
SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	A to X	0.143	0.232
t_{PHL}		0.139	0.163
t_{PLH}	B to X	0.527	0.942
t_{PHL}		0.507	0.701
t_{PLH}	SL to X	0.900	1.00
t_{PHL}		0.485	0.182

Delay coefficients

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
X	0.271	0.544	0.127	0.336

Rise/fall time coefficients for the next cell



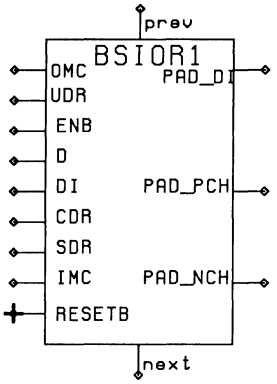
Functional diagram: BSINV8

Boundary Scan Cell for Input/Output Pads 1X Drive

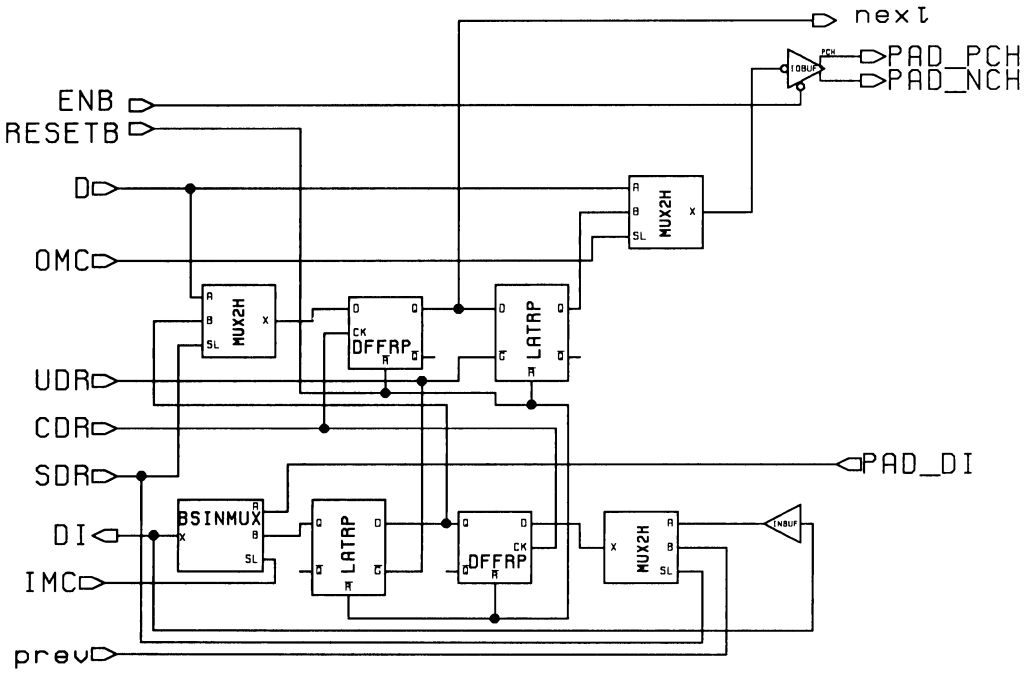
Description

The BSIOR1 is a boundary scan cell for input/output pads. It contains a scan element and a shadow latch for the data coming from the on-chip system logic and for the input from off-chip. When the output mode control (OMC) is low, the on-chip system output is passed from D to PAD_PCH and PAD_NCH when ENB is low. When the input mode control (IMC) is low, the input pads value is passed into the chip from PAD_DI to DI. When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. Note the order, DI's scan element is shifted into D's scan element. RESETB is asynchronous and active low. ENB should be connected to the BSENB output pin of a BSENBR cell (see application note). PAD_PCH and PAD_NCH must be connected respectively to the PCH and NCH input pins of an input/output pad. PAD_DI should be connected directly to the DI output of the pad. The DI output of the BSIOR1 cell must then be connected to one or more input buffers (INBUF, HBUF, DS1216, etc.). See application note for guide to determine input/output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic


next
PAD_PCH
PAD_NCH
ENB
RESETB
D
OMC
UDR
CDR
SDR
DI
IMC
prev
PAD_DI
MUX2H
DFFRP
LATRP
BSINMUX
TOBUF
TNBUF

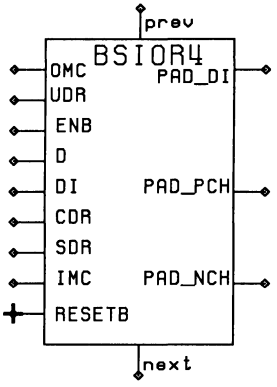
BSIOR4

Boundary Scan Cell for Input/Output Pads 4X Drive

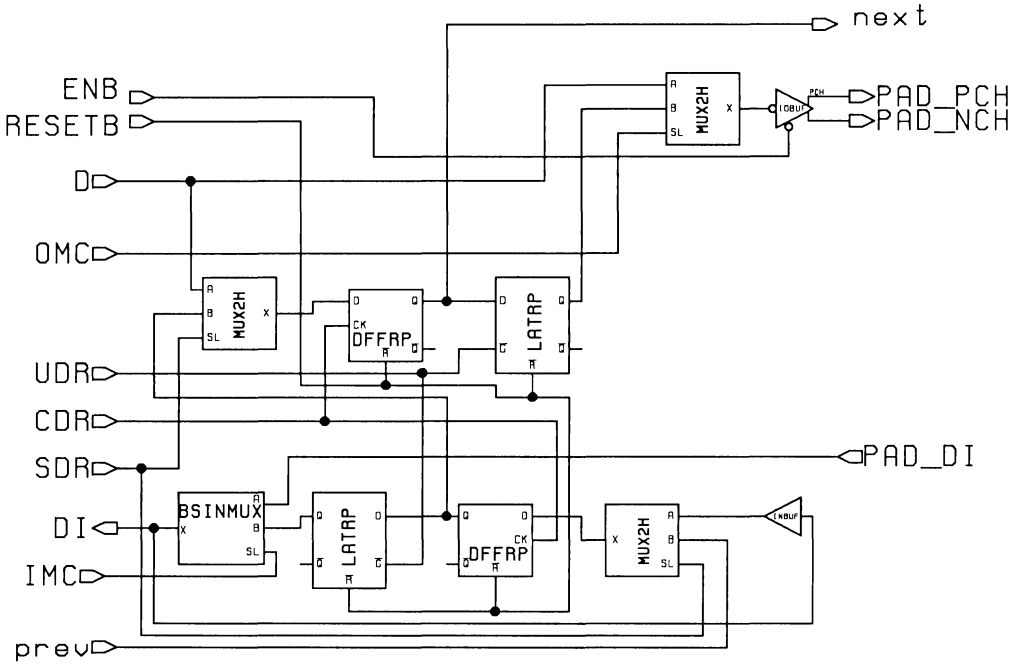
Description

The BSIOR4 is a boundary scan cell for input/output pads. It contains a scan element and a shadow latch for the data coming from the on-chip system logic and for the input from off-chip. When the output mode control (OMC) is low, the on-chip system output is passed from D to PAD_PCH and PAD_NCH when ENB is low. When the input mode control (IMC) is low, the input pads value is passed into the chip from PAD_DI to DI. When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. Note the order, DI's scan element is shifted into D's scan element. RESETB is asynchronous and active low. ENB should be connected to the BSENB output pin of a BSENBR cell (see application note). PAD_PCH and PAD_NCH must be connected respectively to the PCH and NCH input pins of an input/output pad. PAD_DI should be connected directly to the DI output of the pad. The DI output of the BSIOR4 cell must then be connected to one or more input buffers (INBUF, HBUF, DS1216, etc.). See application note for guide to determine input/output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic

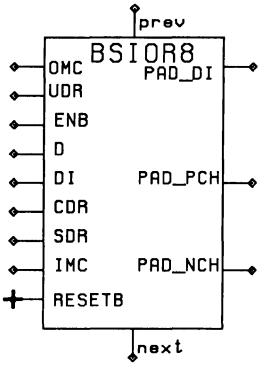

next
ENB
RESETB
D
OMC
UDR
CDR
SDR
DI
IMC
prev
PAD_PCH
PAD_NCH
PAD_DI
MUX2H
DFFRP
LATRP
BSINMUX
IOBUF
INBUF

Boundary Scan Cell for Input/Output Pads 8X Drive

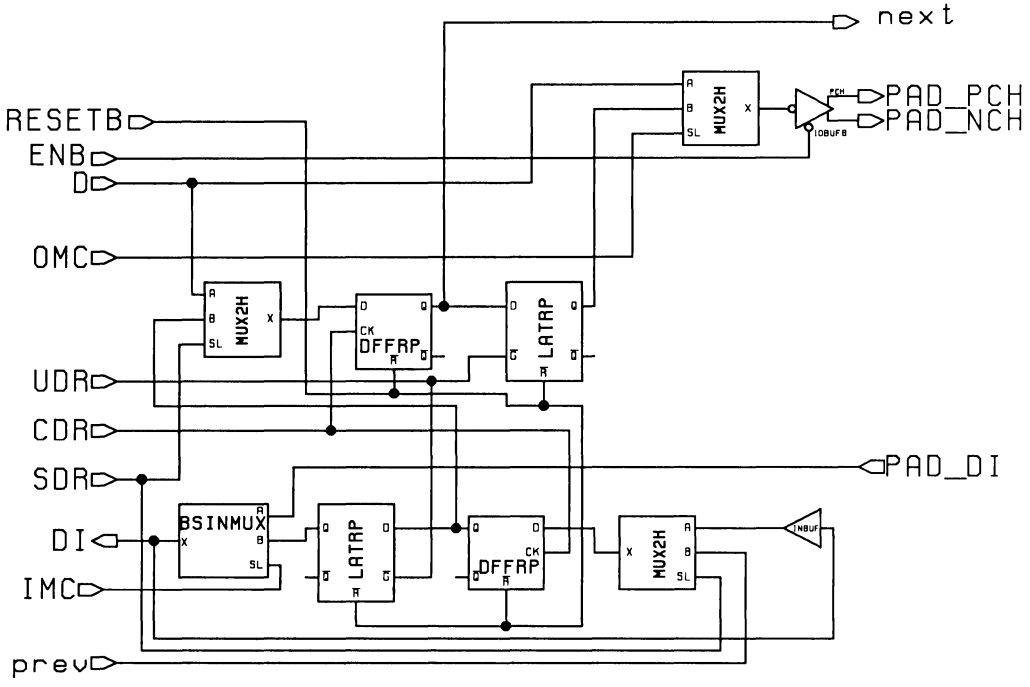
Description

The BSIOR8 is a boundary scan cell for input/output pads. It contains a scan element and a shadow latch for the data coming from the on-chip system logic and for the input from off-chip. When the output mode control (OMC) is low, the on-chip system output is passed from D to PAD_PCH and PAD_NCH when ENB is low. When the input mode control (IMC) is low, the input pads value is passed into the chip from PAD_DI to DI. When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. Note the order, DI's scan element is shifted into D's scan element. RESETB is asynchronous and active low. ENB should be connected to the BSENB output pin of a BSENBR cell (see application note). PAD_PCH and PAD_NCH must be connected respectively to the PCH and NCH input pins of an input/output pad. PAD_DI should be connected directly to the DI output of the pad. The DI output of the BSIOR8 cell must then be connected to one or more input buffers (INBUF, HBUF, DS1216, etc.). See application note for guide to determine input/output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic

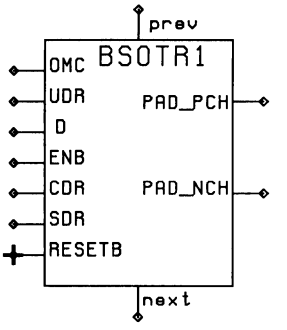

next
RESETB
ENB
D
OMC
UDR
CDR
SDR
DI
IMC
prev
PAD_PCH
PAD_NCH
PAD_DI
MUX2H
DFFRP
LATRP
BSINMUX
IOBUFB
INBUF

Boundary Scan Cell for Tristate Output Pads 1X Drive

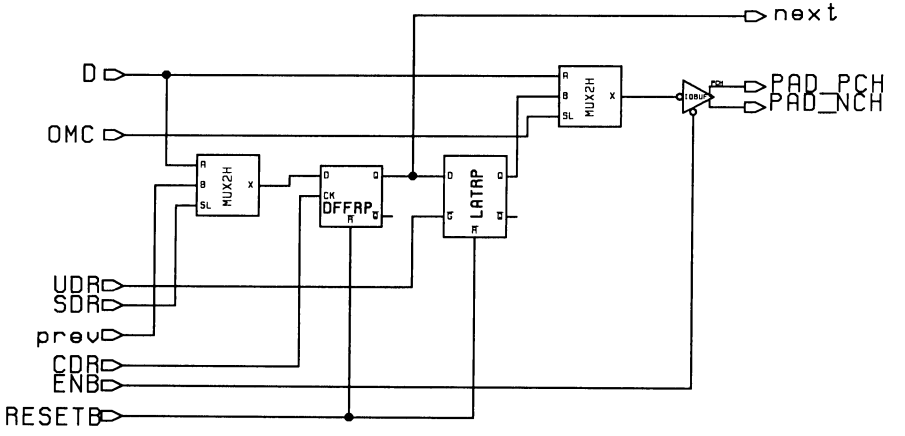
Description

The BSOTR1 is a boundary scan cell for tristate output pads. It contains a scan element and a shadow latch for the data coming from the on-chip system logic. When the output mode control (OMC) is low, the on-chip system output is passed from D to PAD_PCH and PAD_NCH when ENB is low. When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. ENB should be connected to the BSENB output pin of a BSENBR cell (see application note). PAD_PCH and PAD_NCH must be connected respectively to the PCH and NCH input pins of a tristate pad. See application note for guide to determine tristate output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic

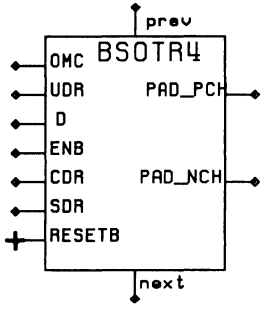


Boundary Scan Cell for Tristate Output Pads 4X Drive

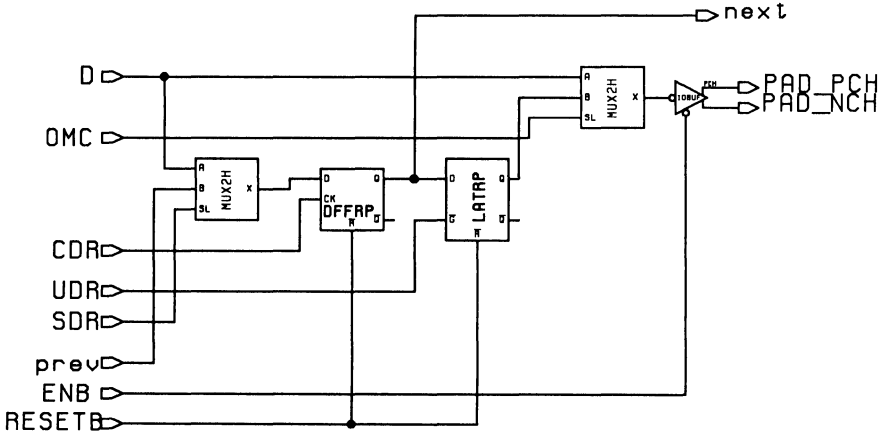
Description

The BSOTR4 is a boundary scan cell for tristate output pads. It contains a scan element and a shadow latch for the data coming from the on-chip system logic. When the output mode control (OMC) is low, the on-chip system output is passed from D to PAD_PCH and PAD_NCH when ENB is low. When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. ENB should be connected to the BSENB output pin of a BSENBR cell (see application note). PAD_PCH and PAD_NCH must be connected respectively to the PCH and NCH input pins of a tristate pad. See application note for guide to determine tristate output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic

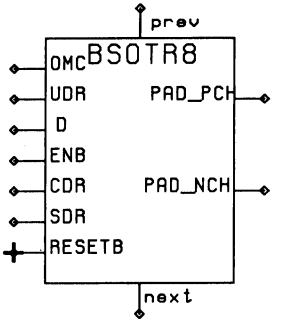


Boundary Scan Cell for Tristate Output Pads 8X Drive

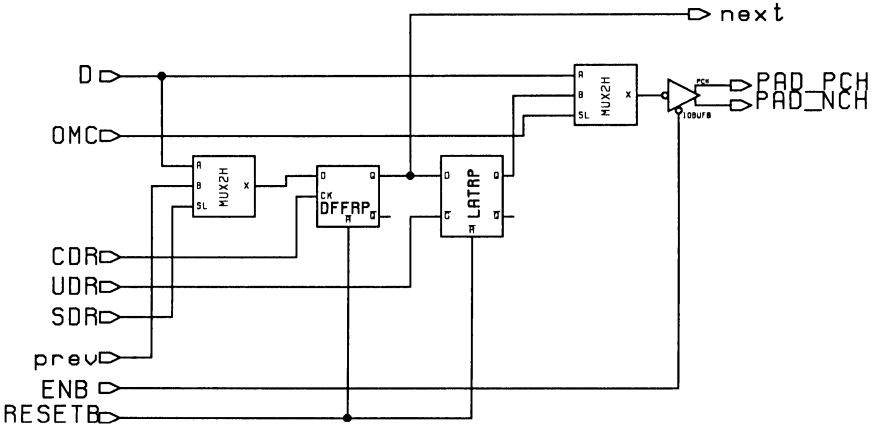
Description

The BSOTR8 is a boundary scan cell for tristate output pads. It contains a scan element and a shadow latch for the data coming from the on-chip system logic. When the output mode control (OMC) is low, the on-chip system output is passed from D to PAD_PCH and PAD_NCH when ENB is low. When UDR goes low, then high, it latches the scan elements value. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. ENB should be connected to the BSENB output pin of a BSENBR cell (see application note). PAD_PCH and PAD_NCH must be connected respectively to the PCH and NCH input pins of a tristate pad. See application note for guide to determine tristate output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic

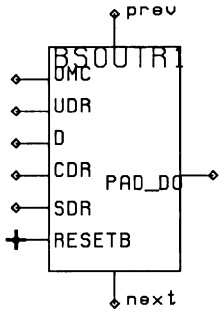


Boundary Scan Cell for Output Pads 1X Drive

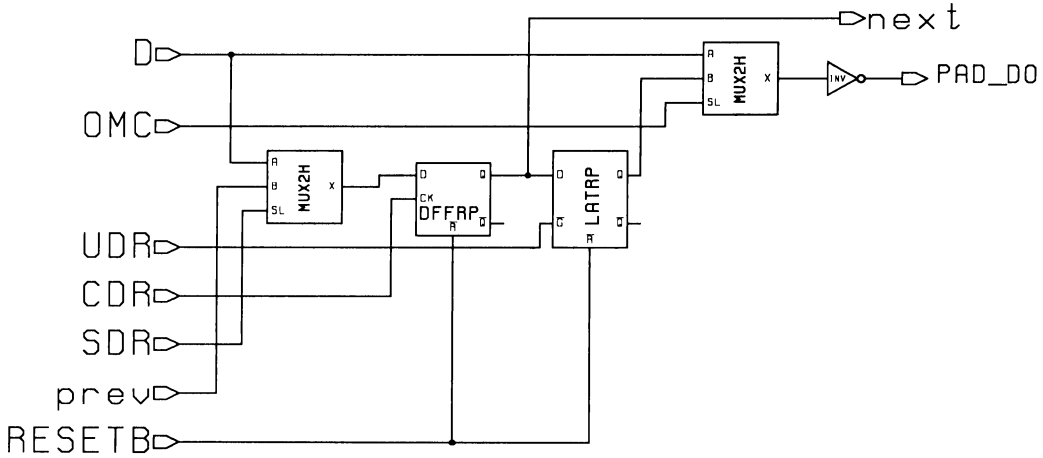
Description

The BSOUTR1 is a boundary scan cell for output pads with just one input pin (OPD2, ODPD8, ONPD24, etc.). It contains a scan element and a shadow latch for the element. When the output mode control (OMC) is low, the on-chip system output is passed to the output pad from D to PAD_DO. When UDR goes low, then high, it latches the scan elements data. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. PAD_DO should be connected directly to the input pin of an output pad. See application note for guide to determine output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic



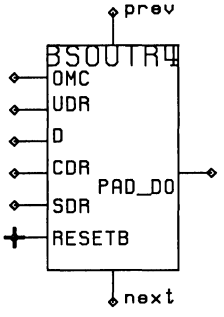
BSOUTR4

Boundary Scan Cell for Output Pads
4X Drive

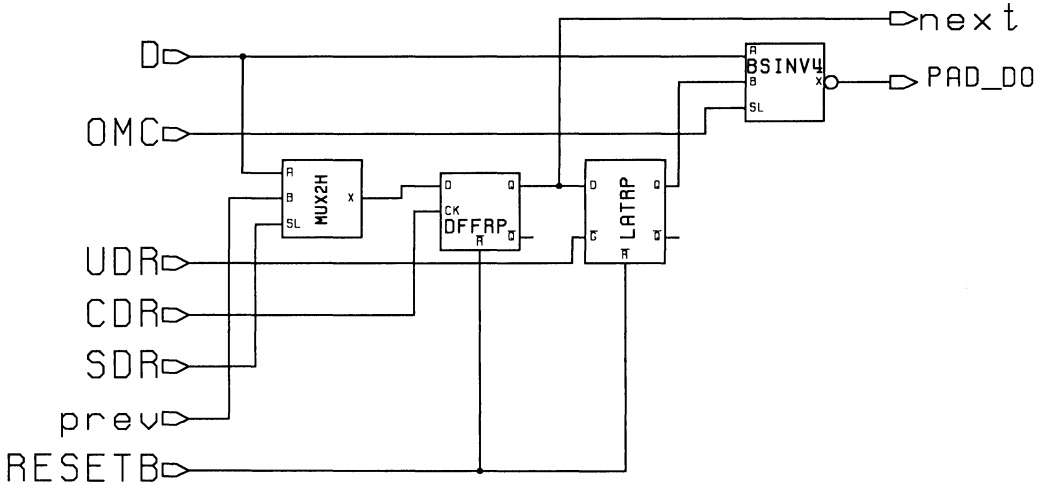
Description

The BSOUTR4 is a boundary scan cell for output pads with just one input pin (OPD2, ODPD8, ONPD24, etc.). It contains a scan element and a shadow latch for the element. When the output mode control (OMC) is low, the on-chip system output is passed to the output pad from D to PAD_DO. When UDR goes low, then high, it latches the scan elements data. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. PAD_DO should be connected directly to the input pin of an output pad. See application note for guide to determine output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic

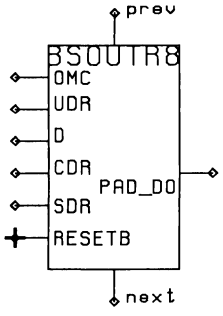


Boundary Scan Cell for Output Pads 8X Drive

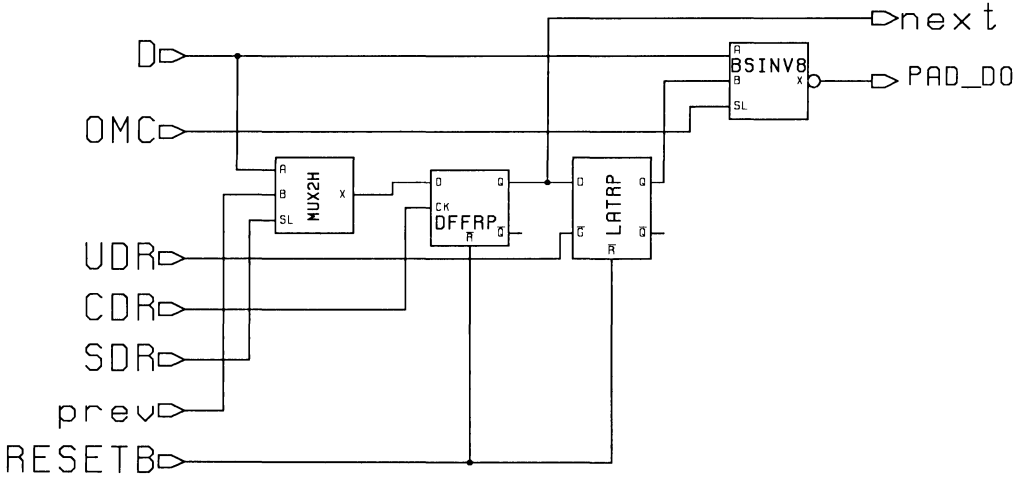
Description

The BSOUTR8 is a boundary scan cell for output pads with just one input pin (OPD2, ODPD8, ONPD24, etc.). It contains a scan element and a shadow latch for the element. When the output mode control (OMC) is low, the on-chip system output is passed to the output pad from D to PAD_DO. When UDR goes low, then high, it latches the scan elements data. CDR is the clock for the scan chain. When SDR is high, it configures the scan chain for shifting from TDI to TDO. RESETB is asynchronous and active low. PAD_DO should be connected directly to the input pin of an output pad. See application note for guide to determine output pad size (2ma, 4ma, etc.) appropriate for use with this cell.

Symbol



Schematic



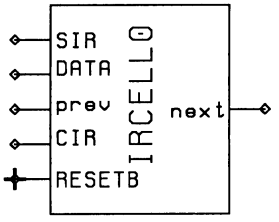
IRCELL0

Instruction Register Cell

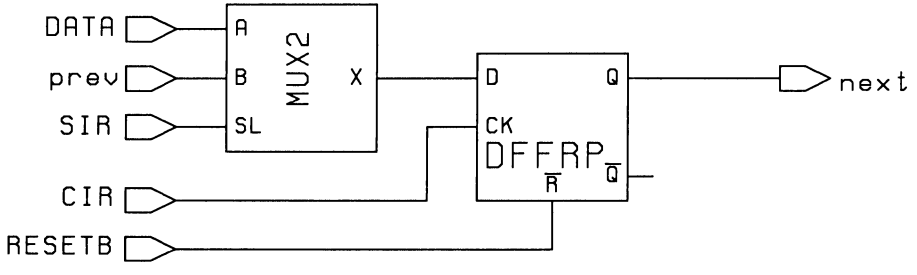
Description

IRCELL0 is an instruction register cell. It contains a storage element. CIR is the clock for the instruction register. When SIR is high, it configures the instruction register for shifting from TDI to TDO. When SIR is low, it parallel loads the instruction register from DATA. When RESETB goes low, the storage element is asynchronously reset to a 0. Instruction decode should occur starting from the 'next' output of this cell. The decoded instruction should be latched with a LATRP cell to avoid decode created glitches (see application note for sample Instruction Register). Note that the two least significant instruction register cells must load a binary '01' pattern (from DATA input) in the CAPTURE_IR state for IEEE standard 1149.1 compatibility. Also note whether IRCELL0 or IRCELL1 will be required to allow asynchronous reset to the correct instruction.

Symbol



Schematic

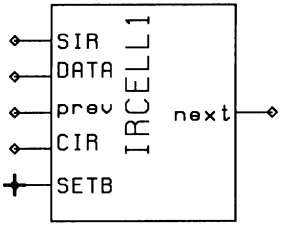


Instruction Register Cell

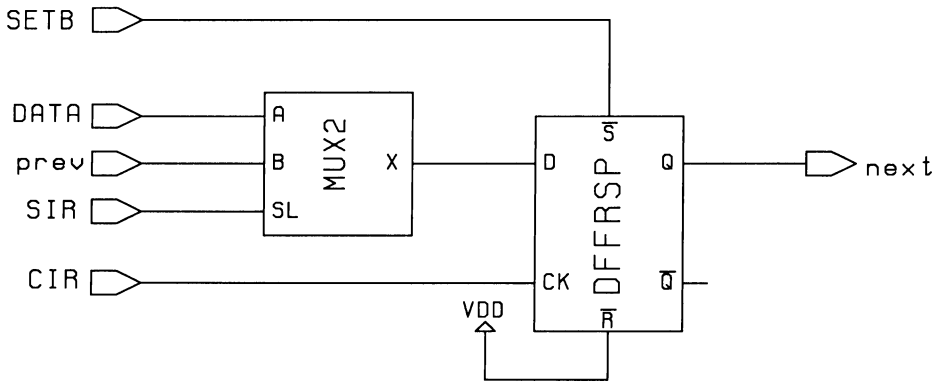
Description

IRCELL1 is an instruction register cell. It contains a storage element. CIR is the clock for the instruction register. When SIR is high, it configures the instruction register for shifting from TDI to TDO. When SIR is low, it parallel loads the instruction register from DATA. When SETB goes low, the storage element is asynchronously set to a 1. Instruction decode should occur starting from the 'next' output of this cell. The decoded instruction should be latched with a LATRP cell to avoid decode created glitches (see application note for sample Instruction Register). Note that the two least significant instruction register cells must load a binary '01' pattern (from DATA input) in the CAPTURE_IR state for IEEE standard 1149.1 compatibility. Also note whether IRCELL0 or IRCELL1 will be required to allow asynchronous reset to the correct instruction.

Symbol



Schematic



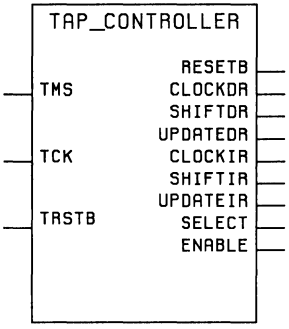
TAP Controller

Description

The TAP_CONTROLLER is a standard cell implementation of the IEEE 1149.1 TAP controller. It is a synchronous 16-state finite state machine that controls 1149.1 circuitry based on the TMS signal. The NCR implementation includes the optional reset pin TRSTB. The state diagram is shown in Figure 8-37. When TRSTB is low, the TAP_CONTROLLER goes to state 15. Otherwise the state changes are based on the value of TMS on the rising edge of TCK. There are nine outputs from the TAP_CONTROLLER whose values are given for each state in Table 8-24. Note that some outputs change with respect to the rising edge of TCK (SELECT) while others change with respect to the falling edge of TCK (RESETB, SHIFTDR, etc.). A small simulation of the TAP_CONTROLLER is shown in Figure 8-38. Since the TAP_CONTROLLER is a soft macrocell, absolute timing parameters cannot be guaranteed until after post-layout simulations have been completed. Some approximate numbers based on a nominal interconnect capacitance and each output driving 10pF follow:

Set up time TMS to TCK : 3 ns
Hold time TCK to TMS : 0 ns

Symbol



Worst Case Commercial Propagation Delays :

TCK \ to RESETB / : 13.7 ns
TCK \ to RESETB \ : 12.9 ns
TCK / to CLOCKDR / : 11.4 ns
TCK \ to CLOCKDR \ : 10.2 ns
TCK \ to SHIFTDR / : 13.7 ns
TCK \ to SHIFTDR \ : 12.9 ns
TCK / to UPDATEDR / : 8.7 ns
TCK \ to UPDATEDR \ : 8.8 ns
TCK / to CLOCKIR / : 11.5 ns
TCK \ to CLOCKIR \ : 10.2 ns
TCK \ to SHIFTIR / : 13.7 ns
TCK \ to SHIFTIR \ : 12.9 ns
TCK / to UPDATEIR / : 8.7 ns
TCK \ to UPDATEIR \ : 8.8 ns
TCK / to SELECT / : 8.8 ns
TCK / to SELECT \ : 7.0 ns
TCK \ to ENABLE / : 14.1 ns
TCK \ to ENABLE \ : 12.7 ns

STATE NAME/#	RESETB	CLOCKDR	SHIFTDR	UPDATEDR	CLOCKIR	SHIFTIR	UPDATEIR	SELECT	ENABLE
EXIT2-DR 0	1	1	0	1	1	0	1	0	0
EXIT1-DR 1	1	1	0	1	1	0	1	0	0
SHIFT-DR 2	1	TCK	1	1	1	0	1	0	1
PAUSE-DR 3	1	1	0	1	1	0	1	0	0
SELECT-IR-SCAN 4	1	1	0	1	1	0	1	0	0
UPDATE-DR 5	1	1	0	0	1	0	1	0	0
CAPTURE-DR 6	1	TCK	0	1	1	0	1	0	0
SELECT-DR-SCAN 7	1	1	0	1	1	0	1	0	0
EXIT2-IR 8	1	1	0	1	1	0	1	1	0
EXIT1-IR 9	1	1	0	1	1	0	1	1	0
SHIFT-IR 10	1	1	0	1	TCK	1	1	1	1
PAUSE-IR 11	1	1	0	1	1	0	1	1	0
RUN TEST/IDLE 12	1	1	0	1	1	0	1	1	0
UPDATE-IR 13	1	1	0	1	1	0	0	1	0
CAPTURE-IR 14	1	1	0	1	TCK	0	1	1	0
TEST LOGIC RESET 15	0	1	0	1	1	0	1	1	0

TABLE 8-24 TAP_CONTROLLER pin table

TAP_CONTROLLER

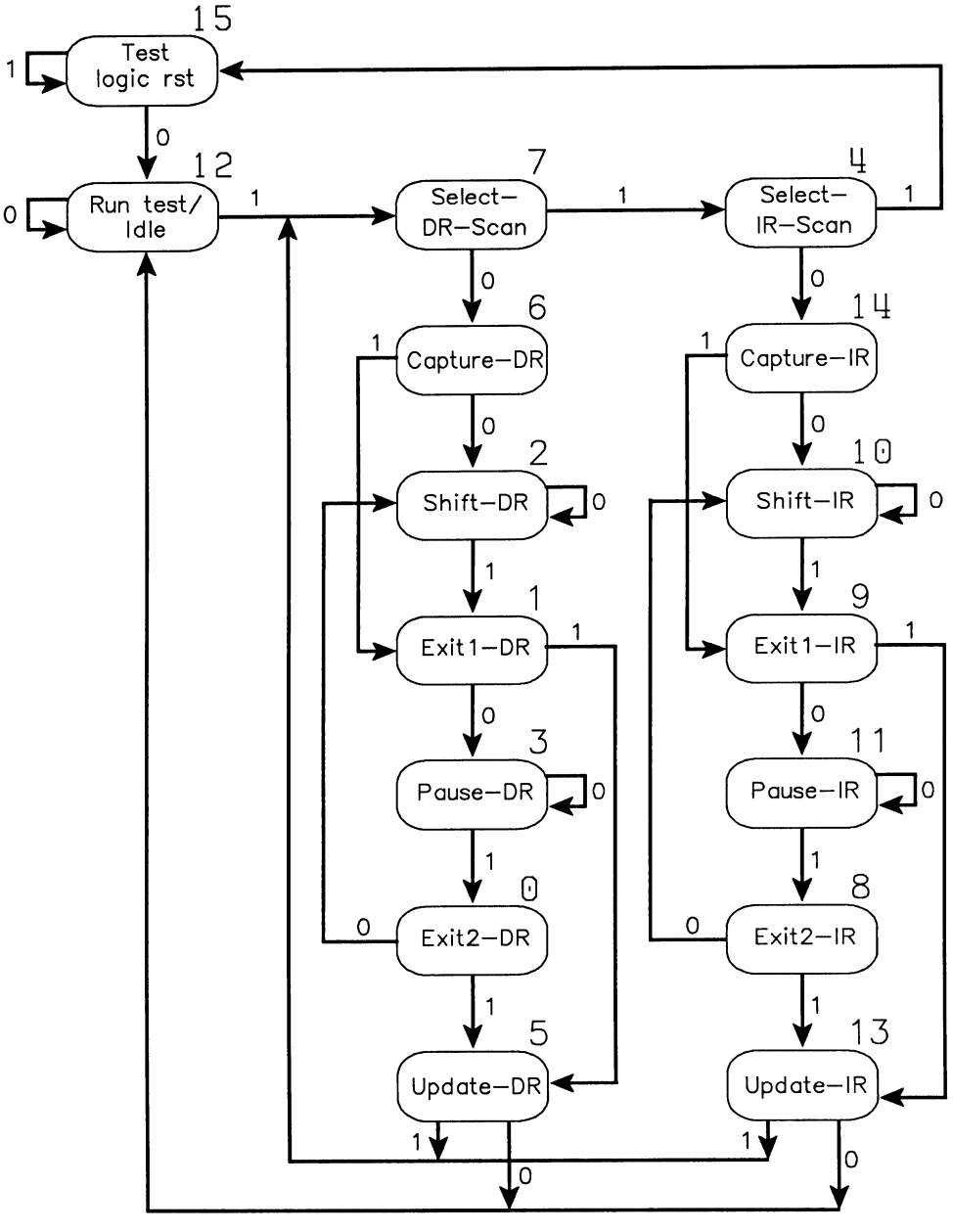


Figure 8–37 TAP_CONTROLLER state diagram

Inputs/Outputs

PIN NAME	TYPE	INPUT CAP./ OUTPUT DRIVE	DESCRIPTION
TMS	I	.199 pF	TEST MODE SELECT
TCK	I	.092 pF	TEST CLOCK
TRSTB	I	.536 pF	TEST RESET
RESETB	O	BUF8	TEST-LOGIC-RESET
CLOCKDR	O	BUF8	DATA-REGISTER-CLOCK
SHIFTDR	O	BUF8	SHIFT-DATA-REGISTER
UPDATEDR	O	BUF8	UPDATE-DATA-REGISTER
CLOCKIR	O	BUF8	INSTRUCTION-REGISTER CLOCK
SHIFTIR	O	BUF8	SHIFT-INSTRUCTION-REGISTER
UPDATEIR	O	BUF8	UPDATE-INSTRUCTION-REGISTER
SELECT	O	BUF8	SELECT-REGISTER
ENABLE	O	BUF8	ENABLE-REGISTER-OUTPUT

TABLE 8-25 TAP_CONTROLLER input capacitance/output drive

Following is a brief description of each state. For a more detailed description, see the IEEE standard 1149.1.

STATE 0 :	Exit2-DR	Temporary state after which scanning the test data register is resumed or terminated.
STATE 1 :	Exit1-DR	Temporary state after which scanning the test data register is suspended or terminated.
STATE 2 :	Shift-DR	The test data register selected is shifted from TDI to TDO.
STATE 3 :	Pause-DR	Shifting of the test data register is suspended.
STATE 4 :	Select-IR	Selection of the instruction register.
STATE 5 :	Update-DR	Latch test data register into parallel output.
STATE 6 :	Capture-DR	Parallel load data into selected test data register.
STATE 7 :	Select-DR	Selection of the test data register based on the instruction register.
STATE 8 :	Exit2-IR	Temporary state after which scanning the instruction register is resumed or terminated.
STATE 9 :	Exit1-IR	Temporary state after which scanning the test data register is suspended or terminated.
STATE 10 :	Shift-IR	The instruction register selected is shifted from TDI to TDO.
STATE 11 :	Pause-IR	Shifting of the instruction register is suspended.
STATE 12 :	Run-Test/Idle	Certain instructions such as RUNBIST cause self test to execute. Others cause the test circuitry to be idle.
STATE 13 :	Update-IR	Latch instruction register into parallel output.
STATE 14 :	Capture-IR	Parallel load data into selected test data register.
STATE 15 :	Test logic-Reset	Test logic is disabled, normal operation takes place.

TAP_CONTROLLER state machine description

TAP_CONTROLLER

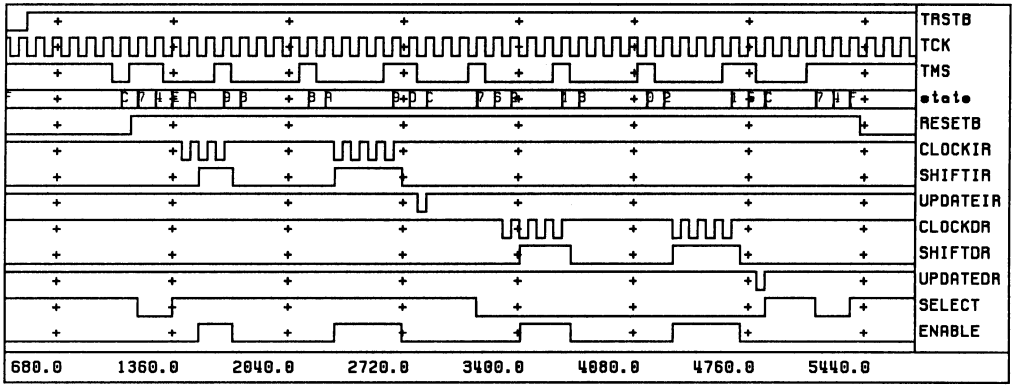


Figure 8-38 TAP_CONTROLLER simulation

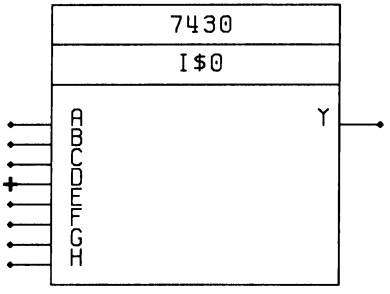
8–Input Positive NAND

Description

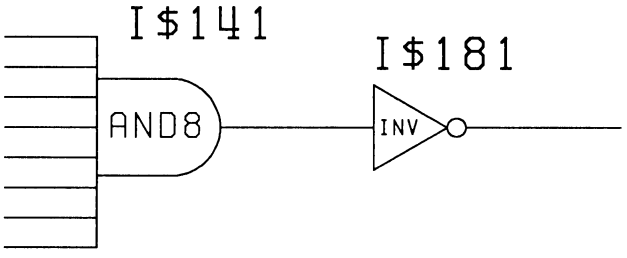
This component contains an 8–input positive NAND gate. When any of the eight inputs are low, the Y output is high. When all of the inputs are high, the Y output is low.

Name: 7430
Gates: 4.8

Symbol



Schematic



SUPERCELLS

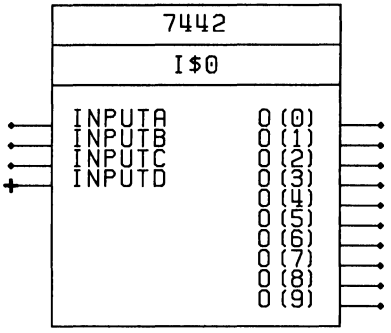
4–Line to 10–Line Decoder

Description

This decoder has four inputs whose binary-coded decimal (BCD) states are converted into a unique, 1 of 10 (DECIMAL) output. When input codes are 0 to 9, the enabled output is active low and all others are high. When input codes are invalid (greater than 9), all outputs have a high value.

Name: 7442
Gates: 28.0

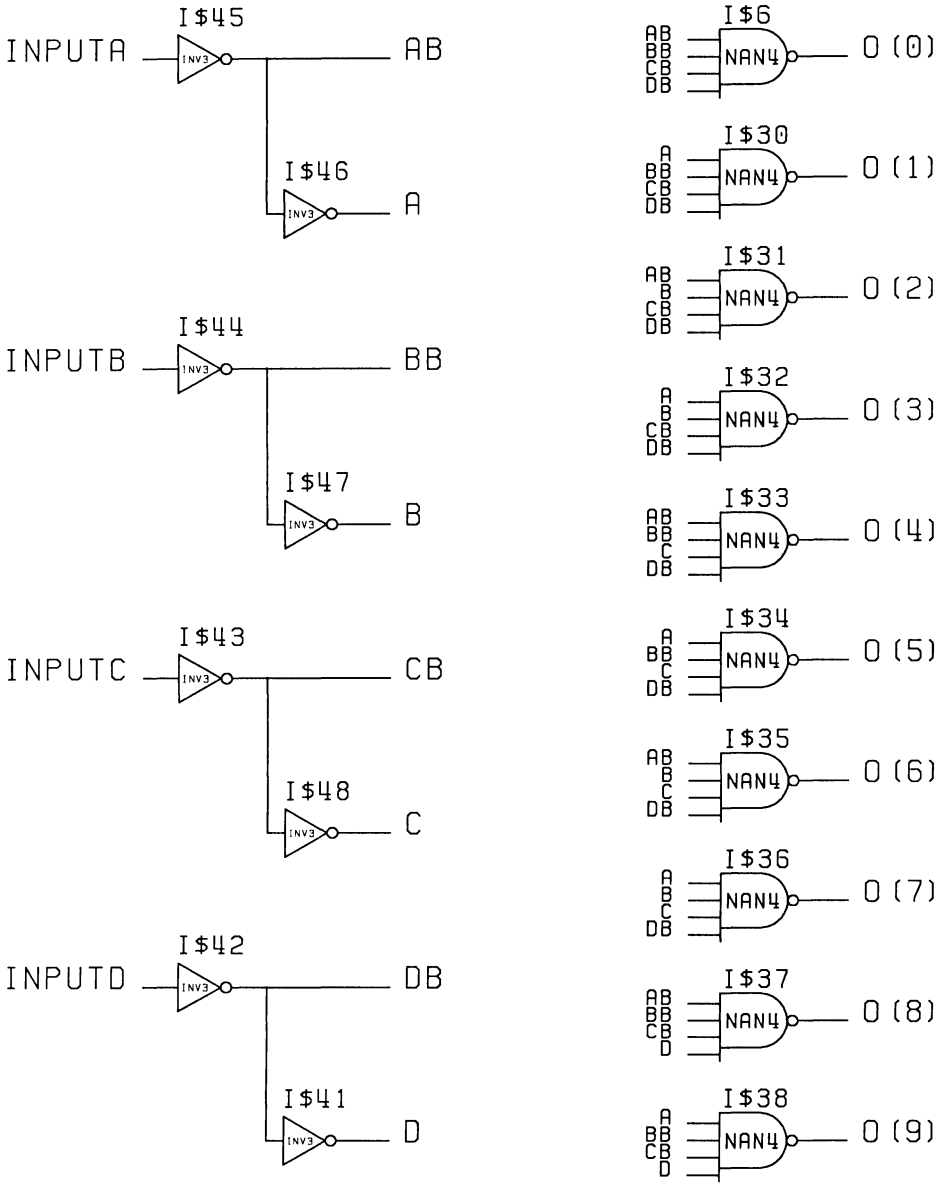
Symbol



Function Table

Input				Output									
D	C	B	A	O(0)	O(1)	O(2)	O(3)	O(4)	O(5)	O(6)	O(7)	O(8)	O(9)
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Schematic


I$45
INPUTA
INV3
AB
I$46
INV3
A
I$44
INPUTB
INV3
BB
I$47
INV3
B
I$43
INPUTC
INV3
CB
I$48
INV3
C
I$42
INPUTD
INV3
DB
I$41
INV3
D
I$6
AB
BB
CB
DB
NAN4
O(0)
I$30
A
BB
CB
DB
NAN4
O(1)
I$31
AB
B
CB
DB
NAN4
O(2)
I$32
A
B
CB
DB
NAN4
O(3)
I$33
AB
BB
C
DB
NAN4
O(4)
I$34
A
BB
C
DB
NAN4
O(5)
I$35
AB
B
C
DB
NAN4
O(6)
I$36
A
B
C
DB
NAN4
O(7)
I$37
AB
BB
CB
D
NAN4
O(8)
I$38
A
BB
CB
D
NAN4
O(9)

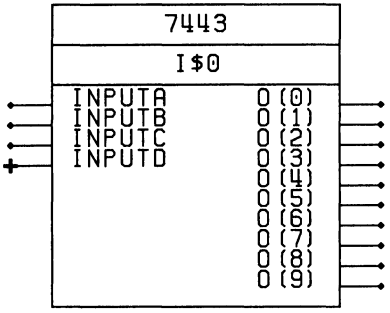
4–Line to 10–Line Decoder

Description

This decoder has four inputs whose excess–3 states are converted into a unique 1 of 10 (DECIMAL) output. When input codes are 3 through 12, the enabled output is active low and all other outputs are high. When input codes are invalid, all outputs remain high.

Name: 7443
Gates: 28.0

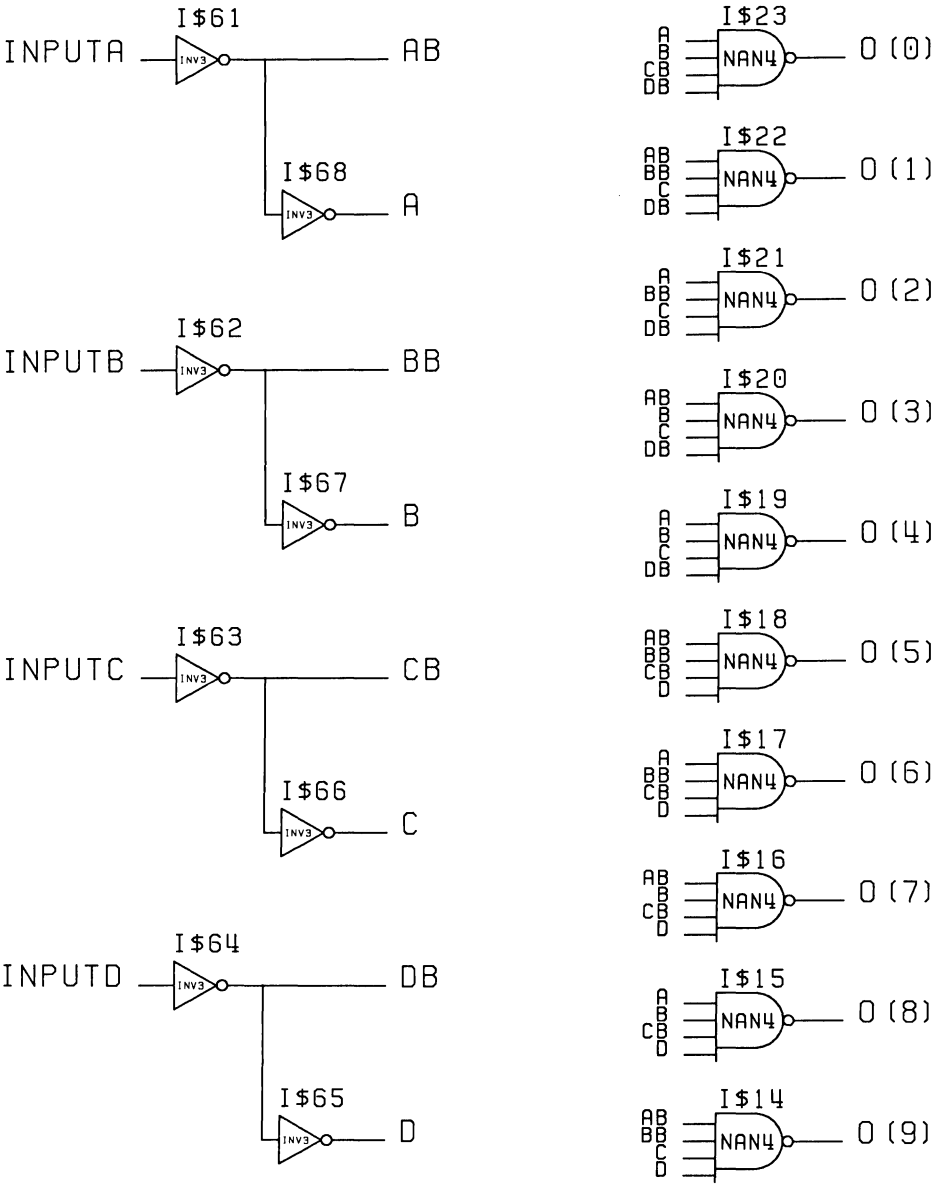
Symbol



Function Table

Input				Output									
D	C	B	A	O(0)	O(1)	O(2)	O(3)	O(4)	O(5)	O(6)	O(7)	O(8)	O(9)
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H
L	H	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	H	H	H	L	H	H	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H	H	H
L	H	H	H	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H	H
H	L	H	H	H	H	H	H	H	H	H	H	L	H
H	H	L	L	H	H	H	H	H	H	H	H	H	L
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Schematic


INPUTA
I$61
INV3
AB
I$68
INV3
A
INPUTB
I$62
INV3
BB
I$67
INV3
B
INPUTC
I$63
INV3
CB
I$66
INV3
C
INPUTD
I$64
INV3
DB
I$65
INV3
D
I$23
NAN4
O(0)
I$22
NAN4
O(1)
I$21
NAN4
O(2)
I$20
NAN4
O(3)
I$19
NAN4
O(4)
I$18
NAN4
O(5)
I$17
NAN4
O(6)
I$16
NAN4
O(7)
I$15
NAN4
O(8)
I$14
NAN4
O(9)

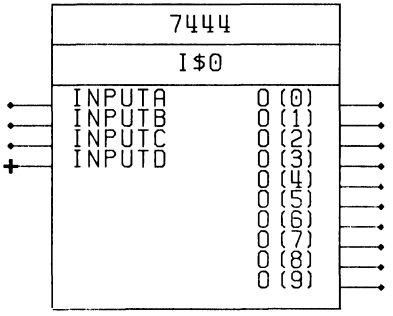
4–Line to 10–Line Decoder

Description

This decoder has four inputs whose excess-3 gray states are converted into a unique 1 of 10 (DECIMAL) output. When input codes are valid, the enabled output is active low and all other outputs are high. When input codes are invalid, all outputs remain high.

Name: 7444
Gates: 28.0

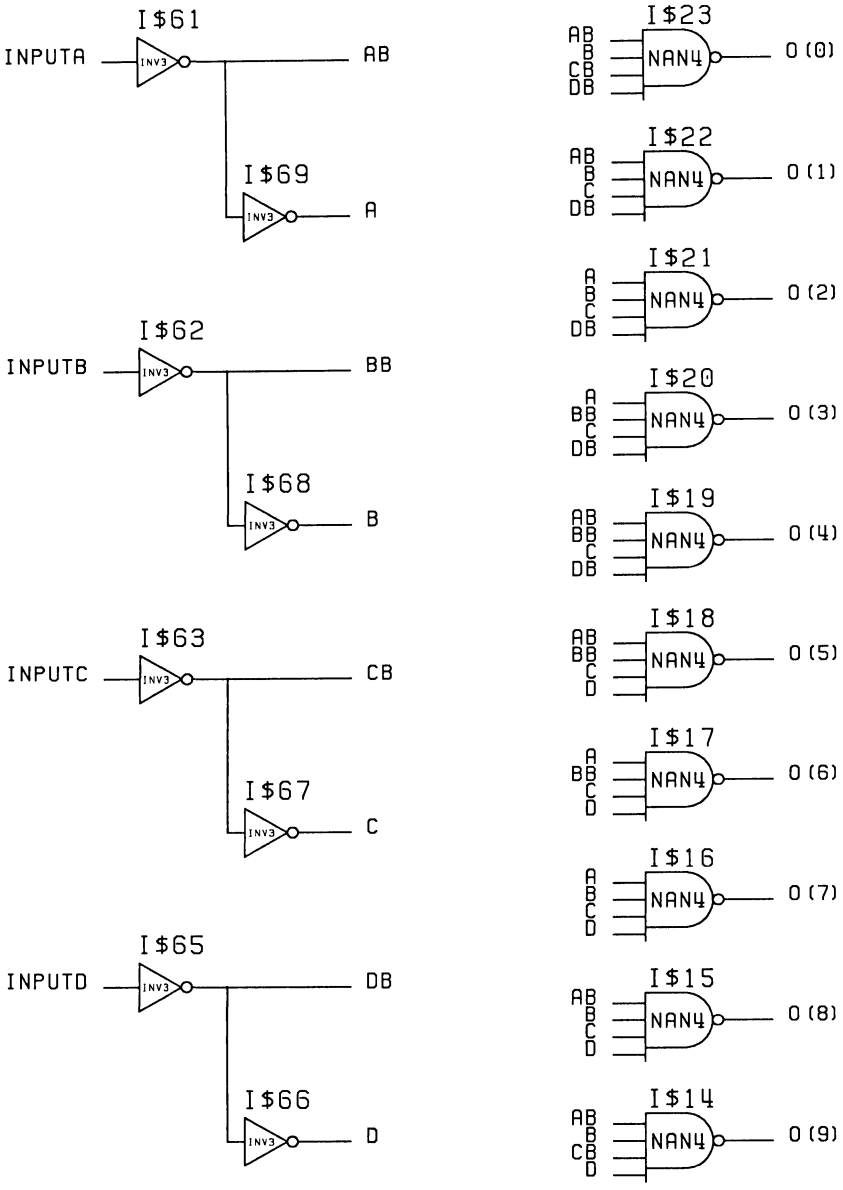
Symbol



Function Table

Input				Output									
D	C	B	A	O(0)	O(1)	O(2)	O(3)	O(4)	O(5)	O(6)	O(7)	O(8)	O(9)
L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	H	L	H	H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H

Schematic


I$61
INPUTA
INV3
AB
I$69
INV3
A
I$62
INPUTB
INV3
BB
I$68
INV3
B
I$63
INPUTC
INV3
CB
I$67
INV3
C
I$65
INPUTD
INV3
DB
I$66
INV3
D
I$23
AB
B
CB
DB
NAN4
O(0)
I$22
AB
B
C
DB
NAN4
O(1)
I$21
A
B
C
DB
NAN4
O(2)
I$20
A
BB
C
DB
NAN4
O(3)
I$19
AB
BB
C
DB
NAN4
O(4)
I$18
AB
BB
C
D
NAN4
O(5)
I$17
A
BB
C
D
NAN4
O(6)
I$16
A
B
C
D
NAN4
O(7)
I$15
AB
B
C
D
NAN4
O(8)
I$14
AB
B
CB
D
NAN4
O(9)

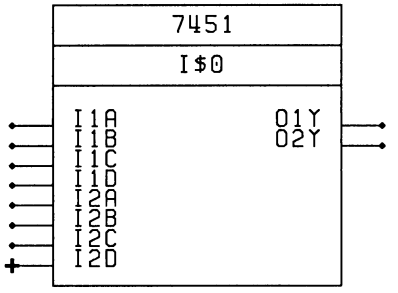
Dual 2–Wide 2–Input AND–OR–INVERT Gates

Description

This component contains two, 2–wide, 2–input AND–OR–INVERT gates. For each AND–OR–INVERT gate, InA and InB are the inputs to the first AND gate and InC and InD are inputs to the second AND gate. These outputs become the inputs to a NOR gate generating the outputs OnY. The equation for O1Y is O1Y = NOT[(1A)(1B) + (1C)(1D)]. The equation for O2Y is O2Y = NOT[(2A)(2B) + (2C)(2D)].

Name: 7451
Gates: 3.5

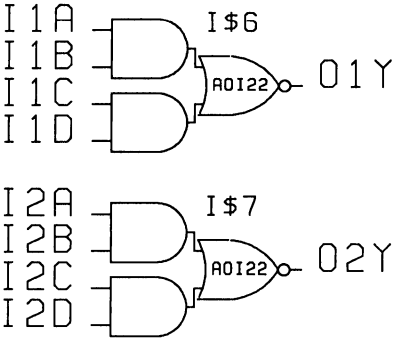
Symbol



Function Table

Input				Output
D	C	B	A	Y
L	L	L	L	H
L	L	L	H	H
L	L	H	L	H
L	L	H	H	L
L	H	L	L	H
L	H	L	H	H
L	H	H	L	H
L	H	H	H	L
H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L

Schematic



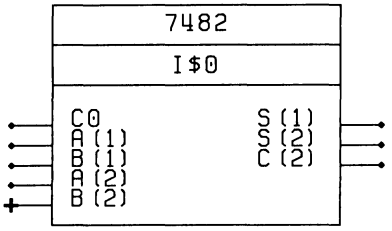
2–Bit Binary Full Adder

Description

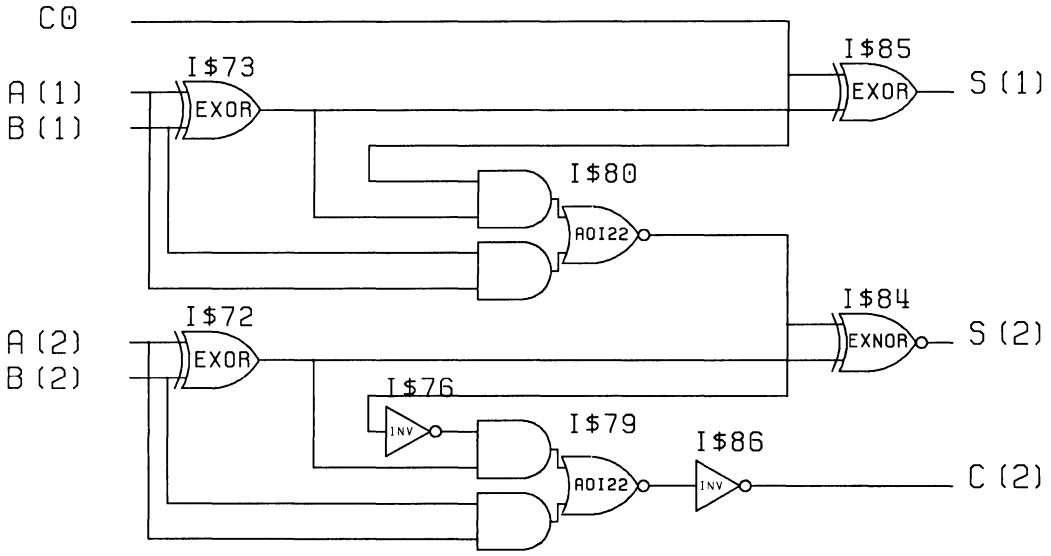
This full adder performs the addition of two incoming, 2–bit, binary numbers with a resultant carry. The inputs A(2), A(1) generate a number A(2)*2 plus A(1)*1 which is added to B(2)*2 plus B(1)*1 and input C0 which is carry in. The sum generated is output as S(2) S(1) and the carry out C(2).

Name: 7482
Gates: 22.5

Symbol



Schematic



SUPERCELLS

7483

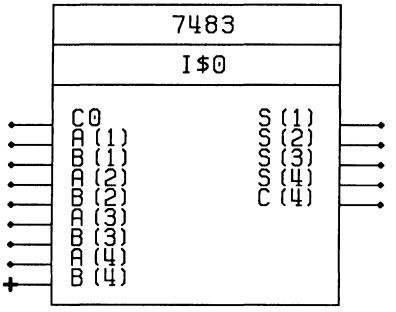
4–Bit Binary Full Adders with Fast Carry

Description

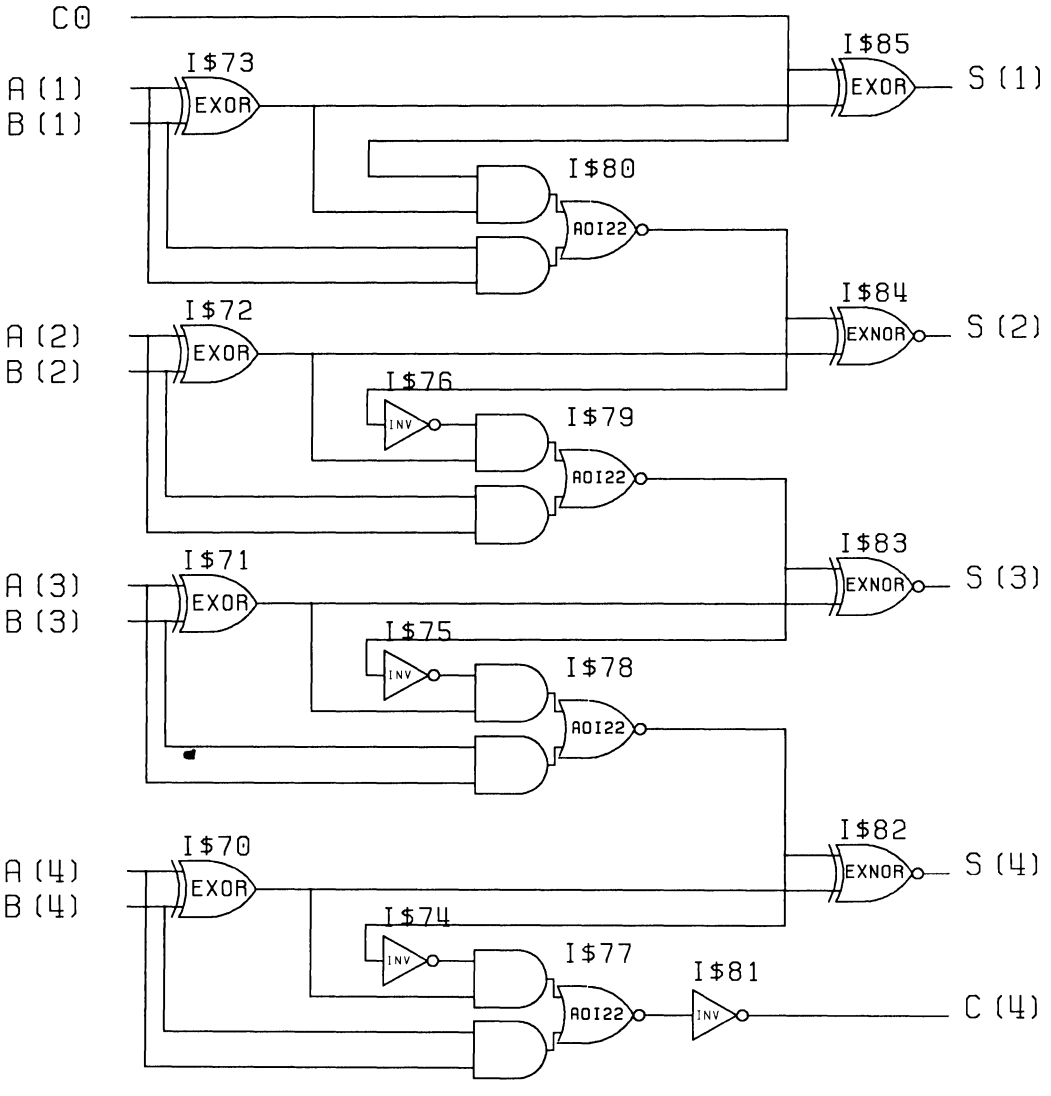
This full adder performs the addition of two incoming, 4–bit, binary numbers with a resultant carry. The inputs A(n) generate a number with the value of A(4)*8 + A(3)*4 + A(2)*2 + A(1)*1 which is added to the number B(4)*8 + B(3)*4 + B(2)*2 + B(1)*1 and CO*1, generating the sum S(4) S(3) S(2) S(1) and the carry out C(4).

Name: 7483
Gates: 45.0

Symbol



Schematic


C0
A (1)
B (1)
I$73
EXOR
I$85
EXOR
S (1)
I$80
AOI22
A (2)
B (2)
I$72
EXOR
I$84
EXNOR
S (2)
I$76
INV
I$79
AOI22
A (3)
B (3)
I$71
EXOR
I$83
EXNOR
S (3)
I$75
INV
I$78
AOI22
A (4)
B (4)
I$70
EXOR
I$82
EXNOR
S (4)
I$74
INV
I$77
AOI22
I$81
INV
C (4)

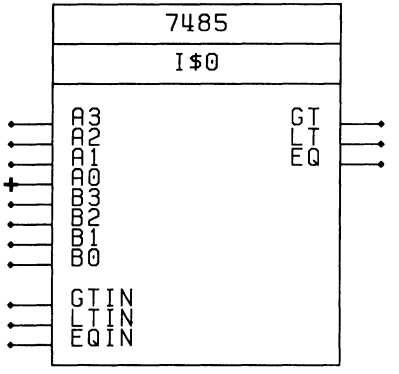
4–Bit Magnitude Comparator

Description

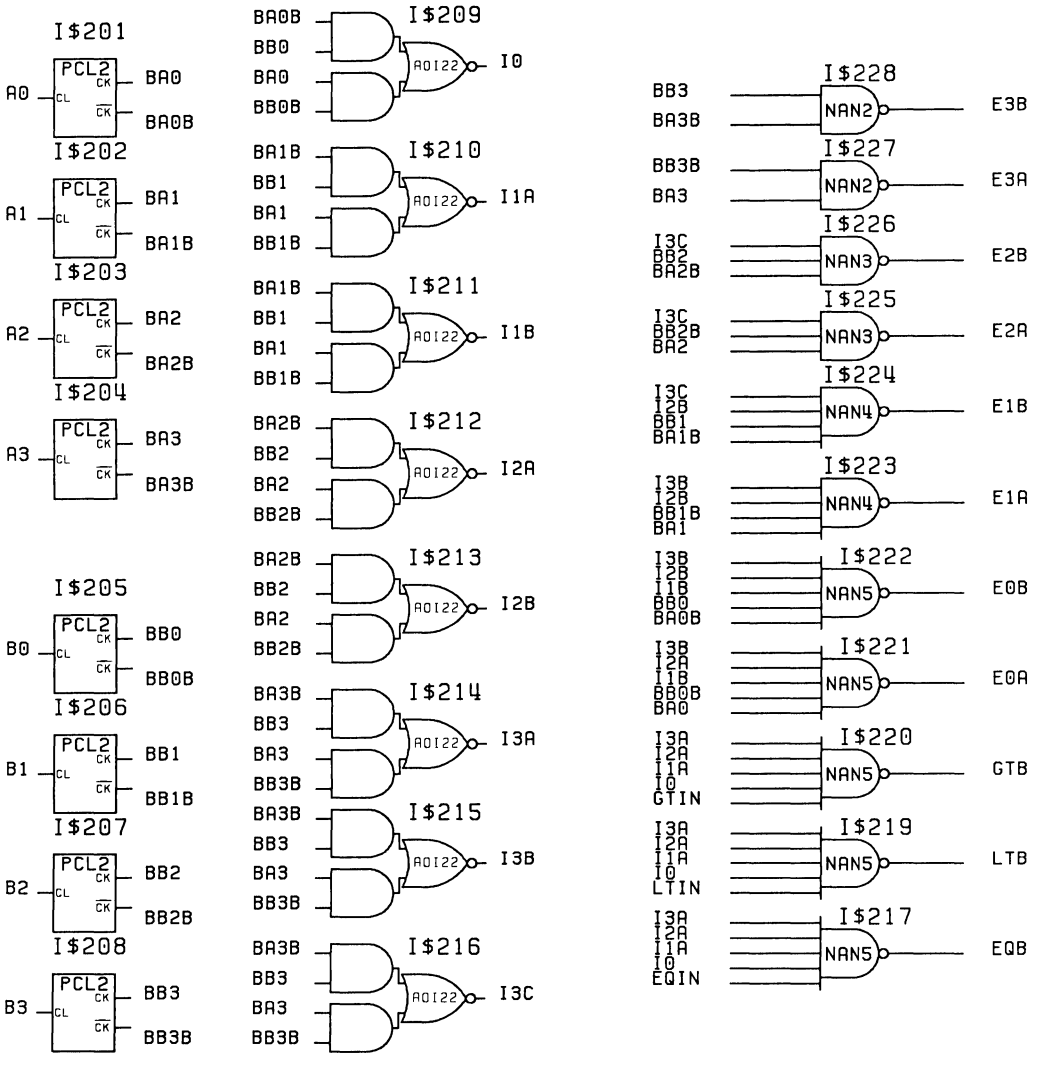
This component performs the comparison of two, 4–bit binary or BCD words and generates three outputs: A < B, A > B, and A = B. By cascading comparators, words of greater length can be compared. Three inputs, A < B, A > B, and A = B, are provided to allow expansion.

Name: 7485
Gates: 70.5

Symbol



Schematic



SUPERCELLS

7486

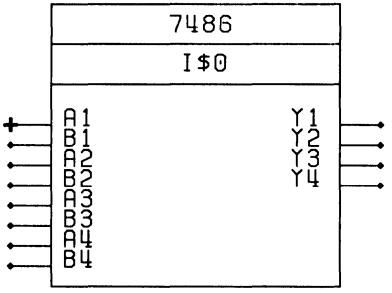
Quad 2–Input EXCLUSIVE–OR Gates

Description

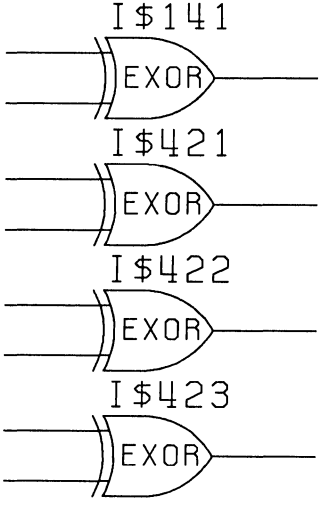
This component contains four, 2–input, EXCLUSIVE–OR gates. When both inputs [A(n) and B(n)] to an EXCLUSIVE–OR gate are at the same logic level, the output Y(n) is low. When the inputs are at different logic levels, the output Y(n) is high.

Name: 7486
Gates: 18.0

Symbol



Schematic



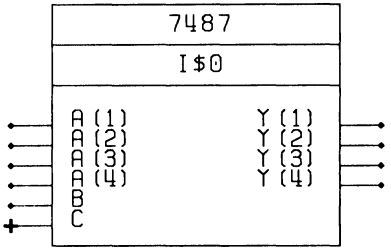
4–Bit True/Complement

Description

This component contains four data inputs, A(4), A(3), A(2) and A(1), two control inputs, B and C, and four outputs, Y(4), Y(3), Y(2), and Y(1). When input B is low, the A inputs are transferred to the Y outputs in either complementary form (when C is low) or true form (when C is high). When input B is high, the Y outputs will be at the complementary level of the C input regardless of the states of the data inputs.

Name: 7487
Gates: 24.0

Symbol

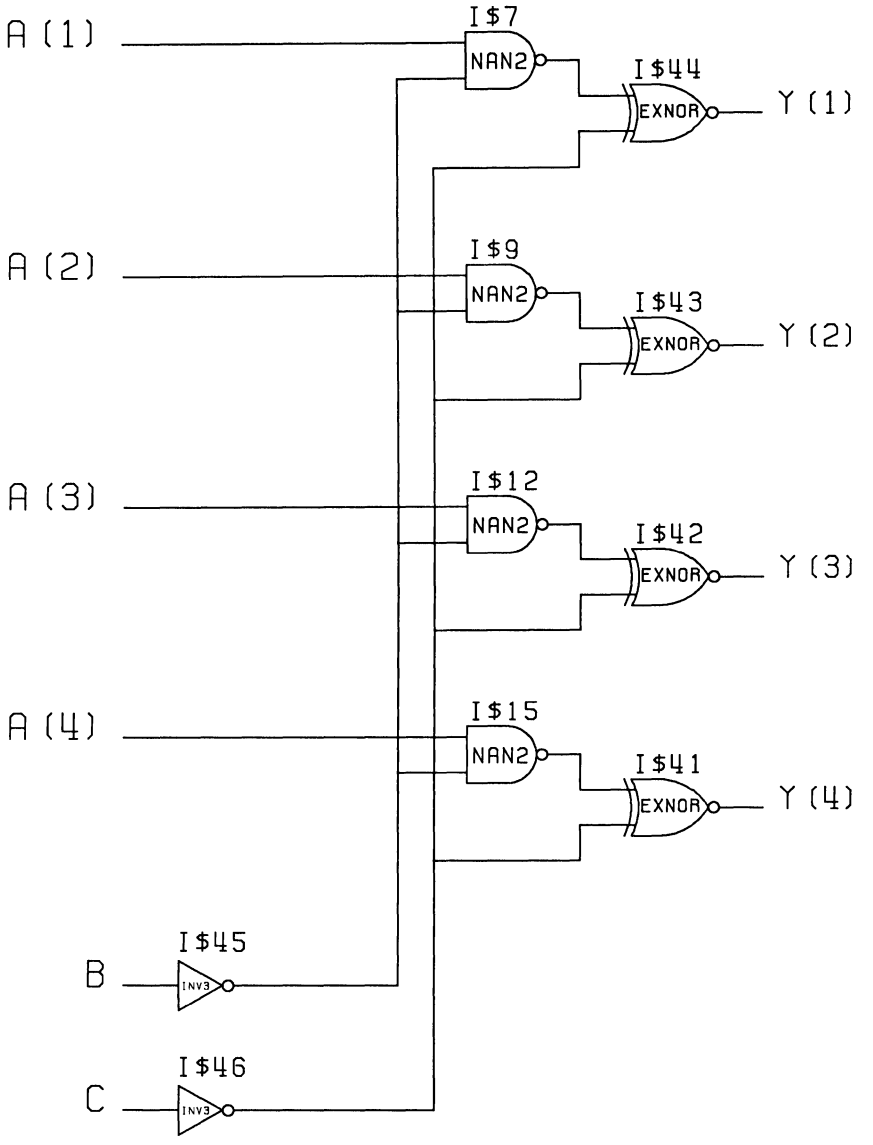


Function Table

Input		Output			
B	C	Y1	Y2	Y3	Y4
L	L	A1b	A2b	A3b	A4b
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

SUPERCELLS

Schematic


A (1)
A (2)
A (3)
A (4)
B
C
I$7
NAN2
I$9
NAN2
I$12
NAN2
I$15
NAN2
I$45
INV3
I$46
INV3
I$44
EXNOR
I$43
EXNOR
I$42
EXNOR
I$41
EXNOR
Y (1)
Y (2)
Y (3)
Y (4)

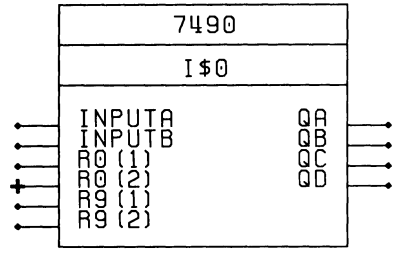
Decade Counter

Description

This component is a 4-bit, ripple counter with a flip-flop that acts as a divide by two counter and three flip-flops that act as a divide by five counter. R0(1) and R0(2) form a gated zero reset that forces all outputs low, independent of the other inputs, when R0(1) and R0(2) are both high. R9(1) and R9(2) form a master set that forces the outputs to nine (HLLH) when both R9(1) and R9(2) are high. To achieve a 4-bit binary decade counter, connect output QA to INPUTB and apply count pulses to INPUTA. To use this component as a bi-quinary divide by ten counter, connect output QD to INPUTA and use INPUTB for the clock. No external connections are needed to use the divide by two or divide by five functions. Divide by two uses INPUTA for the input and QA for the output. Divide by five uses INPUTB for the input and QC for the output.

Name: 7490
Gates: 48.8

Symbol



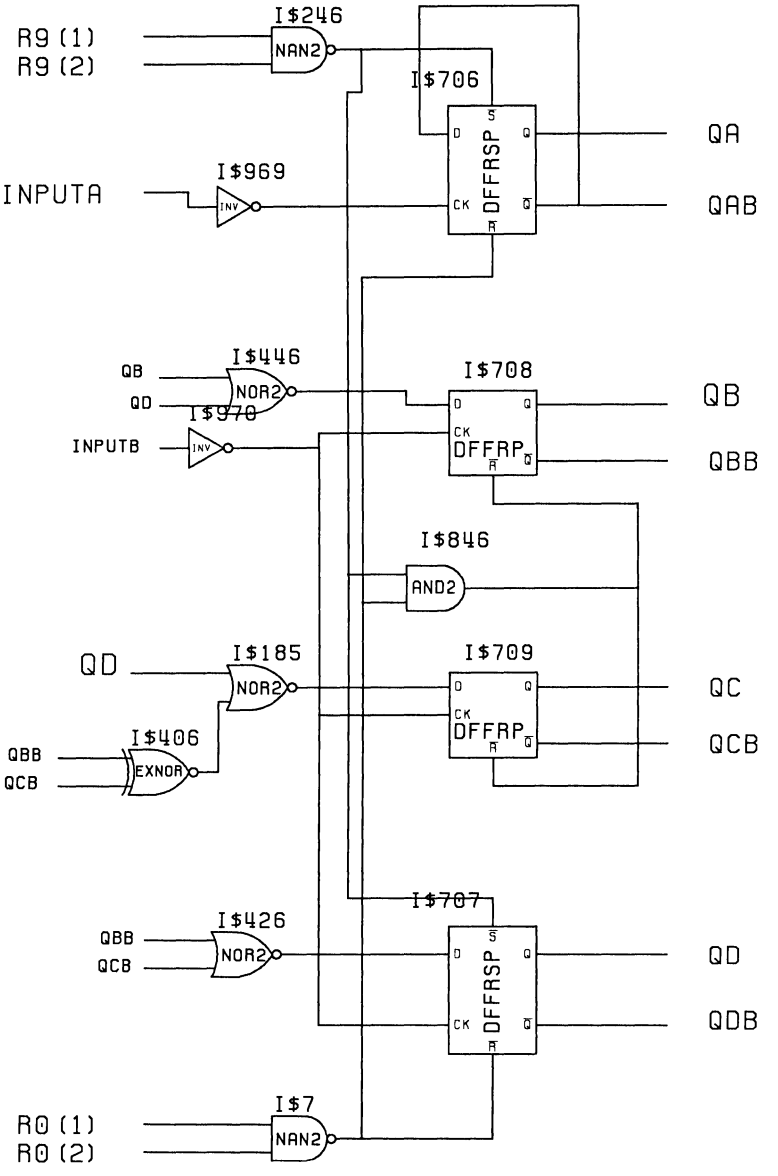
Function Tables

Reset/Count Function Table							
R0(1)	R0(2)	R9(1)	R9(2)	QD	QC	QB	QA
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

BCD Count				
Count	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

SUPERCELLS

Schematic


R9(1)
R9(2)
I$246
NAN2
I$706
QA
INPUTA
I$969
INV
DFFRSP
QAB
QB
I$446
NOR2
QD
I$970
INPUTB
INV
I$708
DFFRP
QB
QBB
I$846
AND2
QD
I$185
NOR2
I$709
QC
QBB
QCB
I$406
EXNOR
DFFRP
QCB
I$707
QBB
QCB
I$426
NOR2
DFFRSP
QD
QDB
R0(1)
R0(2)
I$7
NAN2

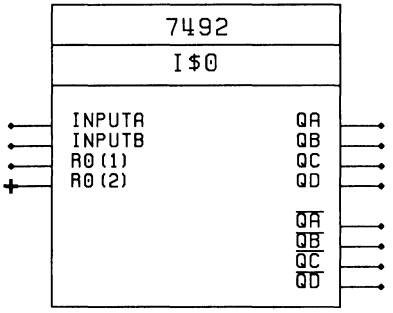
Divide by Two, Six, or Twelve Counter

Description

This counter contains a gated zero reset. When R0(1) and R0(2) are high, all of the counter outputs are low. To achieve a divide by twelve counter, connect output QA to INPUTB and apply count pulses to INPUTA. The output will be at QD. No modifications are necessary for the divide by two or six counters. The divide by two counter is clocked at INPUTA and the output will be at QA. The divide by six counter is clocked at INPUTB and the output will be at QD. The Q outputs and their complements are available.

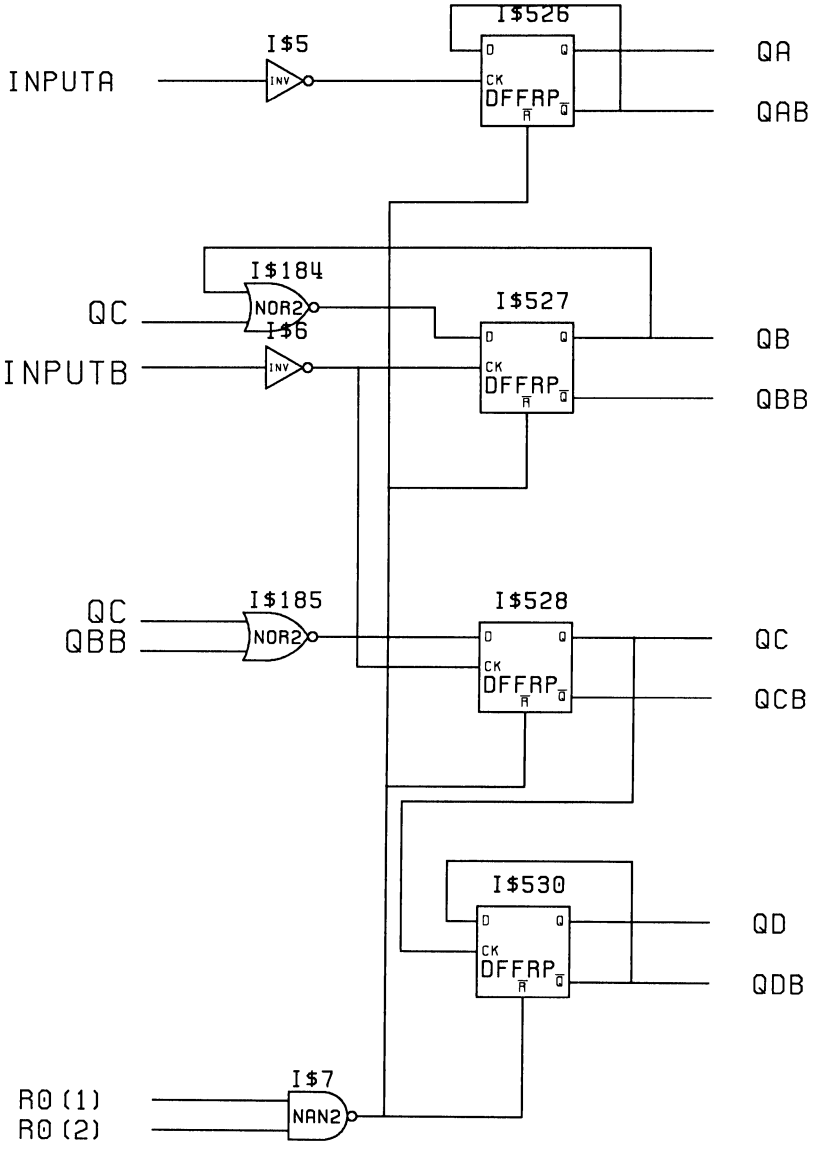
Name: 7492
Gates: 36.0

Symbol



SUPERCELLS

Schematic


I$526
I$5
INPUTA
INV
D
Q
CK
DFFRP
R
Q
QA
QAB
I$184
QC
NOR2
I$6
INPUTB
INV
I$527
QB
QBB
I$185
QC
QBB
NOR2
I$528
QC
QCB
I$530
QD
QDB
I$7
R0(1)
R0(2)
NAN2

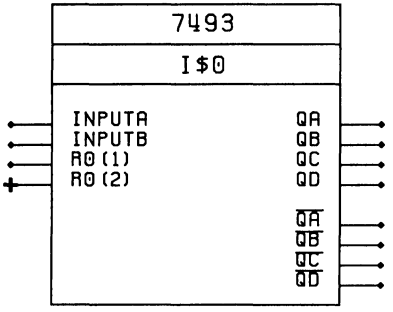
4–Bit Binary Counter

Description

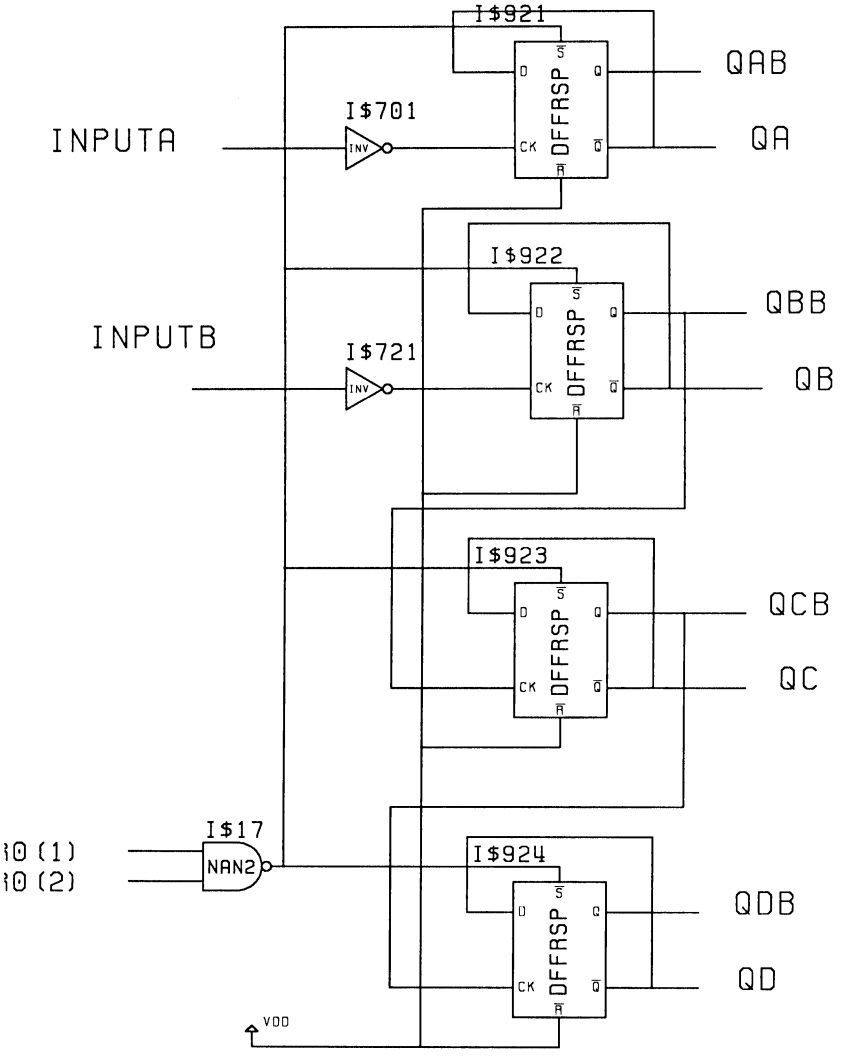
This component is a 4–bit, ripple counter with a flip–flop that acts as a divide by two counter and a 3–stage binary counter for which the count cycle length is divide by eight. R0(1) and R0(2) form a gated zero reset that forces all outputs low, independent of the other inputs. To achieve a 4–bit binary counter, connect output QA to INPUTB and apply count pulses applied to INPUTA. The Q outputs and their complements are available.

Name: 7493
Gates: 44.0

Symbol



Schematic


I$921
QAB
I$701
INPUTA
QA
I$922
QBB
INPUTB
I$721
QB
I$923
QCB
QC
I$17
I$924
QDB
QD
VDD
INV
NAN2
DFFRSP
D
Q
CK
S
R

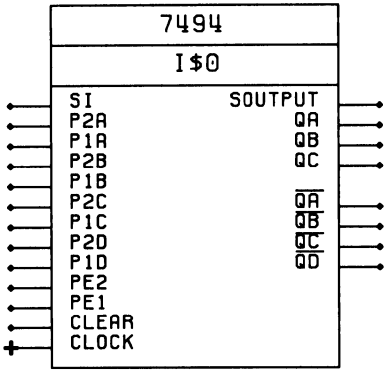
4–Bit Shift Register with Presets

Description

This component is a 4–bit shift register with two asynchronous presets. All four registers can be cleared by applying a high level to the CLEAR input while the internal presets are inactive. Clearing is independent of the level of the clock input. The register may be parallel loaded by first clearing all stages with the CLEAR input, then applying data to either the P1 or P2 inputs of each register stage (A, B, C and D), and finally, bringing the corresponding preset enable input high (PE1 or PE2). Information is transferred to the outputs on the rising edge of the clock. The clear input must be low and the internal presets must be inactive when the register is being clocked. Valid data must be setup at each flip–flop before the rising edge of the clock. The serial input provides data for the first stage while the outputs of each register provide data to the subsequent stages. In addition to the outputs SOUTPUT (QD), QC, QB, and QA, their complements are available.

Name: 7494
Gates: 50.0

Symbol

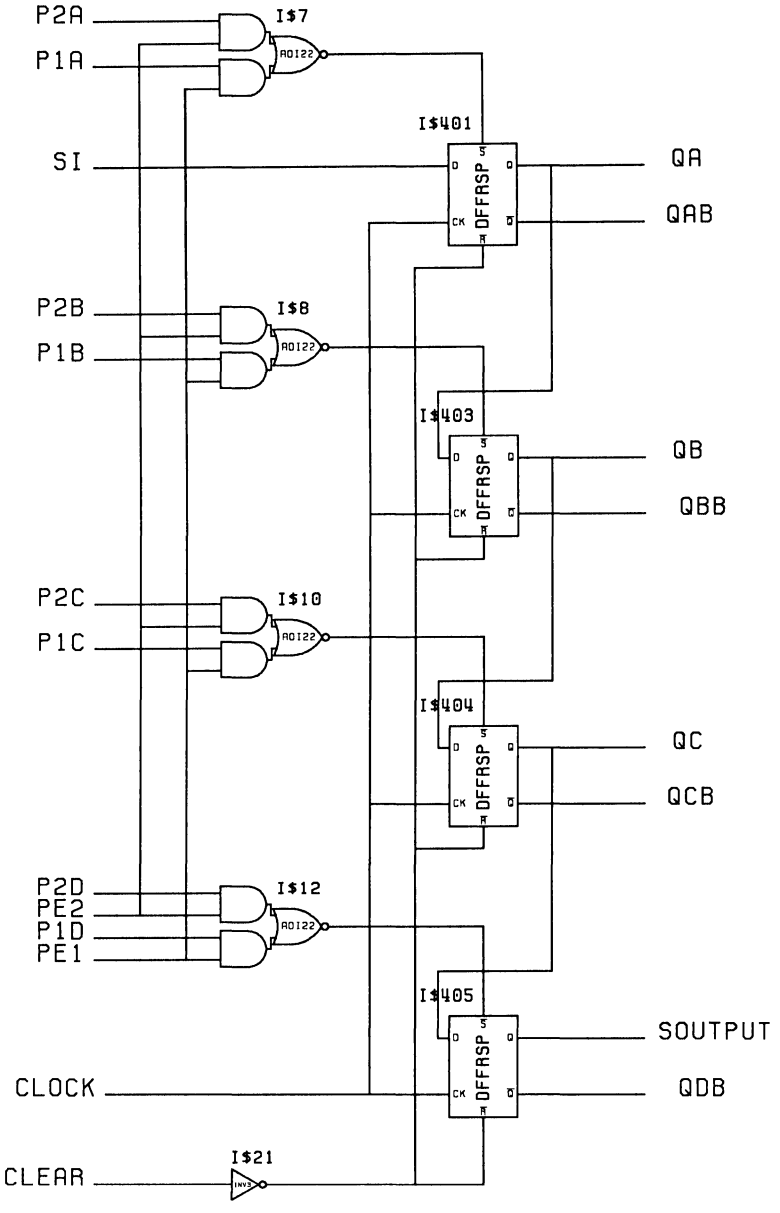


Function Table

Inputs													Outputs			
SI	P1A	P1B	P1C	P1D	P2A	P2B	P2C	P2D	PE1	PE2	Clear	Clock	QA	QB	QC	QD
X	X	X	X	X	X	X	X	X	L	L	H	X	L	L	L	L
X	X	X	X	X	X	X	X	X	L	H	L	X	P2A	P2B	P2C	P2D
X	X	X	X	X	X	X	X	X	H	L	L	X	P1A	P1B	P1C	P1D
X	X	X	X	X	X	X	X	X	L	L	L	L	QA_0	QB_0	QC_0	QD_0
L	X	X	X	X	X	X	X	X	L	L	L	↑	L	QA_N	QB_N	QC_N
H	X	X	X	X	X	X	X	X	L	L	L	↑	H	QA_N	QB_N	QC_N

SUPERCELLS

Schematic


P2A
P1A
I$7
AOI22
I$401
SI
QA
QAB
DFFRSP
P2B
P1B
I$8
I$403
QB
QBB
P2C
P1C
I$10
I$404
QC
QCB
P2D
PE2
P1D
PE1
I$12
I$405
SOUTPUT
QDB
CLOCK
CLEAR
I$21
INV2

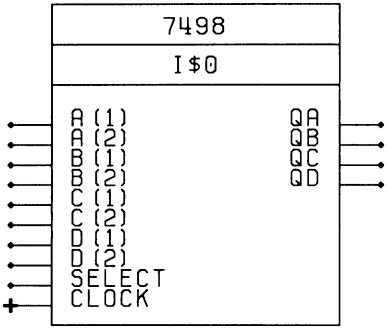
4–Bit Data Selector Registers

Description

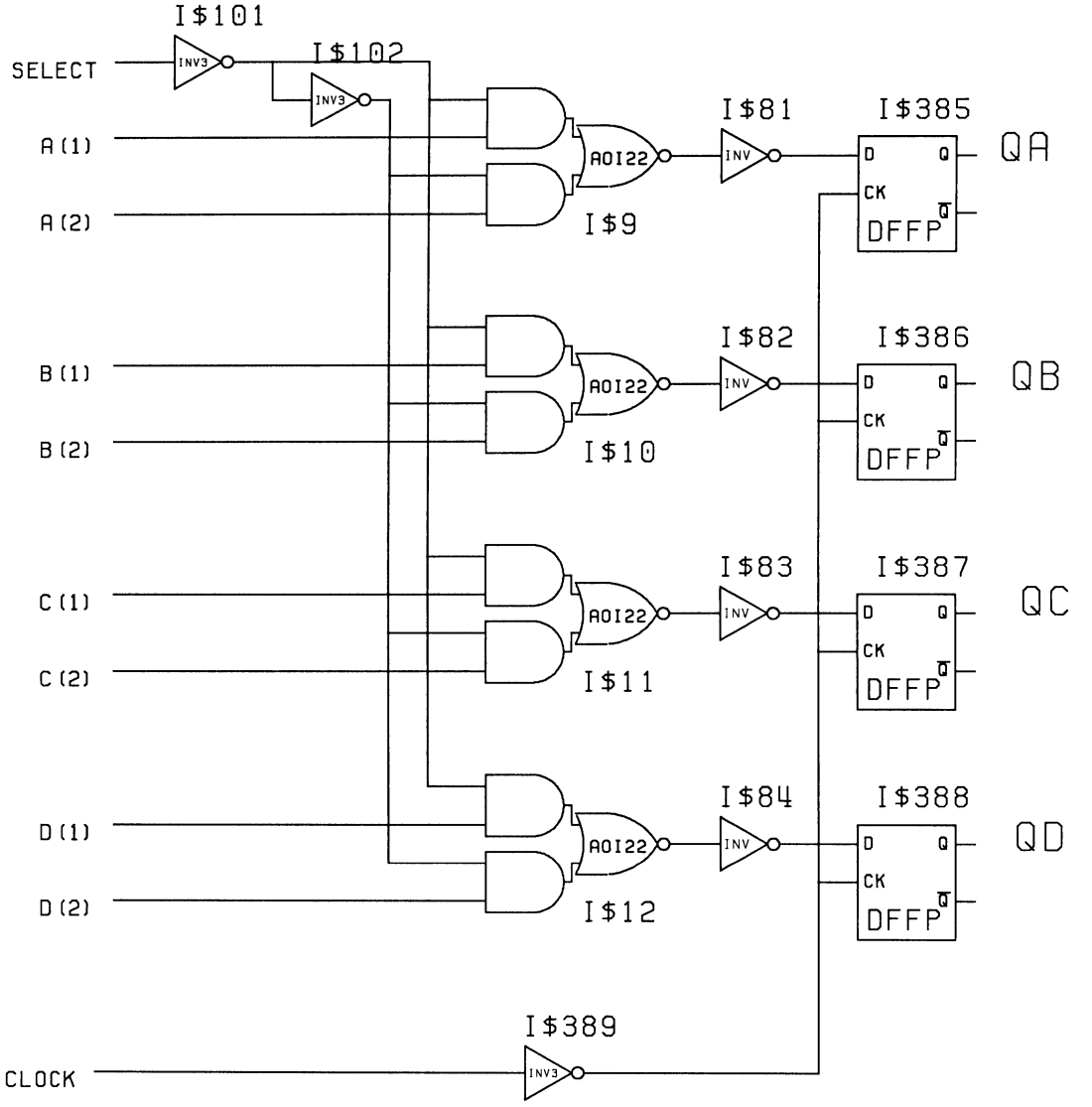
This component contains parallel inputs and outputs and selects 1 of 2, 4–bit words. When the word select input (SELECT) is low, word 1 (A1–D1) is applied to the data input of the flip–flops. When SELECT is high, word 2 (A2–D2) is applied to the data input of the flip–flops. The selected 4–bit word is shifted to the outputs of the flip–flops on the negative going edge of the clock pulse (CLOCK).

Name: 7498
Gates: 37.0

Symbol



Schematic


I$101
I$102
SELECT
INV3
INV3
A(1)
A(2)
B(1)
B(2)
C(1)
C(2)
D(1)
D(2)
AOI22
I$9
AOI22
I$10
AOI22
I$11
AOI22
I$12
I$81
I$82
I$83
I$84
INV
INV
INV
INV
I$385
I$386
I$387
I$388
D
Q
CK
Q
DFFP
QA
QB
QC
QD
I$389
CLOCK
INV3

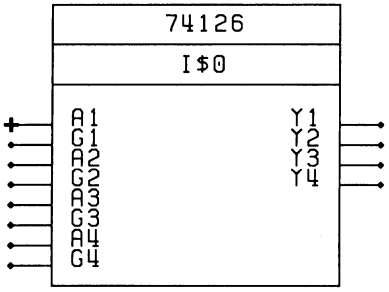
Quad–Tristate Buffer

Description

This component contains four tristate, non–inverting buffers with output enable G(n). When the G(n) input is high, the output is enabled and data is transferred from the A(n) input to the Y(n) output. When the G(n) input is low, the output is disabled and set to the high–impedance state. NOTE: Because the enable inputs are slower than the data inputs, there is a hold time requirement on data inputs.

Name: 74126
Gates: 15.0

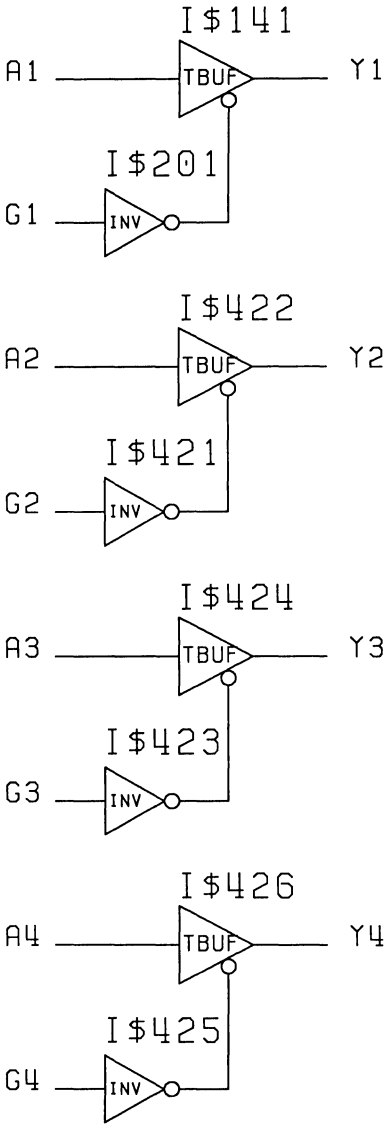
Symbol



A[N]	G[N]	Y[N]
L	H	L
H	H	H
X	L	Z

SUPERCELLS

Schematic


I$141
A1
TBUF
Y1
I$201
G1
INV
I$422
A2
TBUF
Y2
I$421
G2
INV
I$424
A3
TBUF
Y3
I$423
G3
INV
I$426
A4
TBUF
Y4
I$425
G4
INV

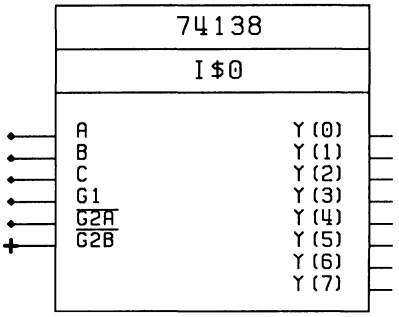
3– to 8–Line Decoder/Demultiplexer

Description

This decoder/demultiplexer contains three select inputs (A, B, C), three enable inputs (G1, $\overline{G2A}$, $\overline{G2B}$), and eight outputs. One of eight mutually exclusive, active low outputs is enabled, depending on the level of the select and enable inputs. All outputs will be high unless $\overline{G2A}$ and $\overline{G2B}$ are low and G1 is high. For expansion or cascading, an enable input can be used as a data input for demultiplexing applications.

Name: 74138
Gates: 25.5

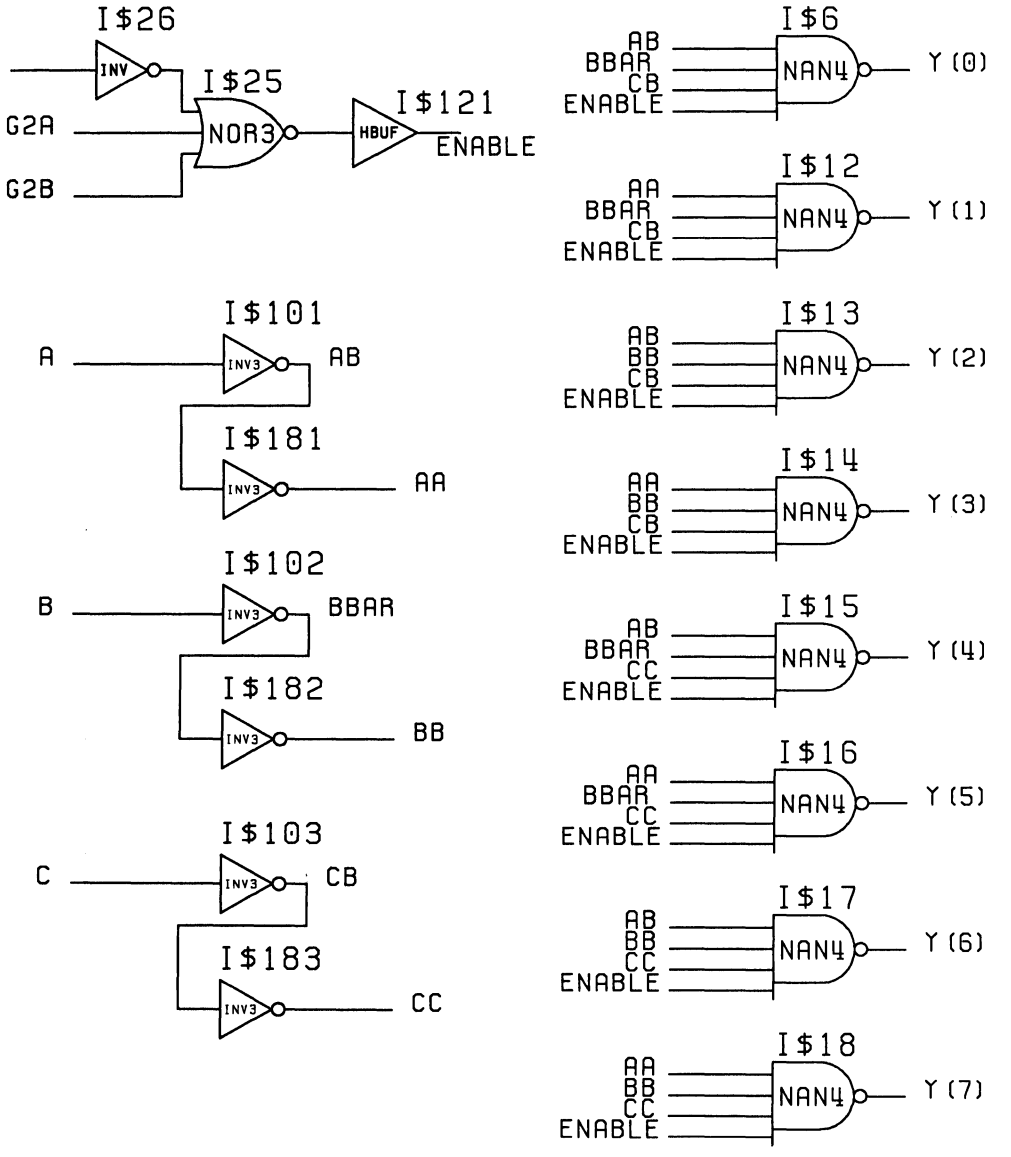
Symbol



C	B	A	G1	$\overline{G2A}$	$\overline{G2B}$	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
X	X	X	X	H	X	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	H	H	H	H	H	H	H
X	X	X	L	X	X	H	H	H	H	H	H	H	H
L	L	L	H	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	H	L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	H	L	L	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	L	L	H	H	H	H	H	L	H	H
H	H	L	H	L	L	H	H	H	H	H	H	L	H
H	H	H	H	L	L	H	H	H	H	H	H	H	L

SUPERCELLS

Schematic


I$26
INV
I$25
NOR3
I$121
HBUF
G2A
G2B
ENABLE
I$101
INV3
A
AB
I$181
AA
I$102
B
BBAR
I$182
BB
I$103
C
CB
I$183
CC
I$6
NAN4
AB
BBAR
CB
ENABLE
Y(0)
I$12
AA
Y(1)
I$13
BB
Y(2)
I$14
Y(3)
I$15
CC
Y(4)
I$16
Y(5)
I$17
Y(6)
I$18
Y(7)

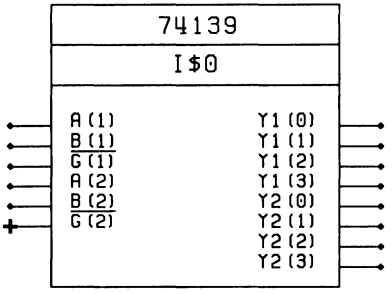
Dual 2– to 4–Line Decoders/Demultiplexers

Description

Each of the two decoders/demultiplexers contains two select inputs [A(n) and B(n)], an enable input [$\overline{G(n)}$], and four outputs. One of four mutually exclusive, active low outputs is enabled, depending on the level of the select and enable inputs. For expansion or cascading, the enable input can be used as a data input for demultiplexing applications. All outputs will be high unless $\overline{G(n)}$ is low.

Name: 74139
Gates: 16.0

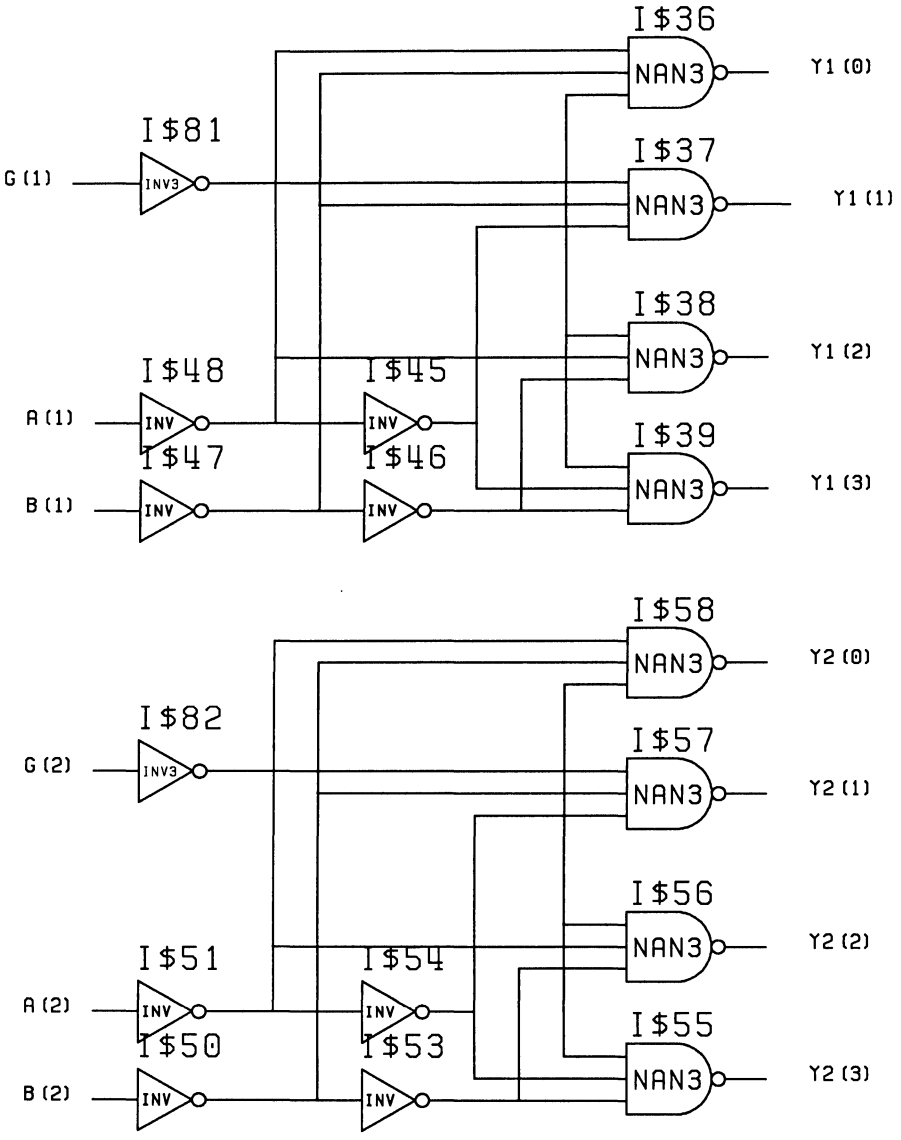
Symbol



Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

SUPERCELLS

Schematic


I$36
NAN3
Y1 (0)
I$81
G (1)
INV3
I$37
NAN3
Y1 (1)
I$38
NAN3
Y1 (2)
I$48
I$45
A (1)
INV
INV
I$47
I$46
I$39
B (1)
INV
INV
NAN3
Y1 (3)
I$58
NAN3
Y2 (0)
I$82
G (2)
INV3
I$57
NAN3
Y2 (1)
I$56
NAN3
Y2 (2)
I$51
I$54
A (2)
INV
INV
I$50
I$53
I$55
B (2)
INV
INV
NAN3
Y2 (3)

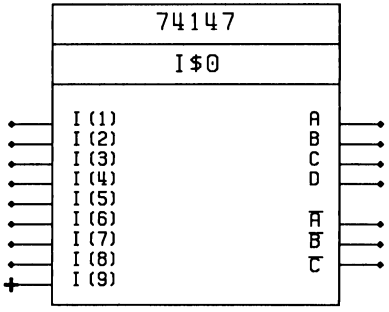
Decimal to BCD Priority Encoder

Description

This component encodes nine data lines to binary coded decimal (BCD). The decimal zero condition occurs when all nine inputs are high. Data inputs and outputs are active low. In addition to the outputs A, B, C, and D, the complements of A, B, and C are available.

Name: 74147
Gates: 37.3

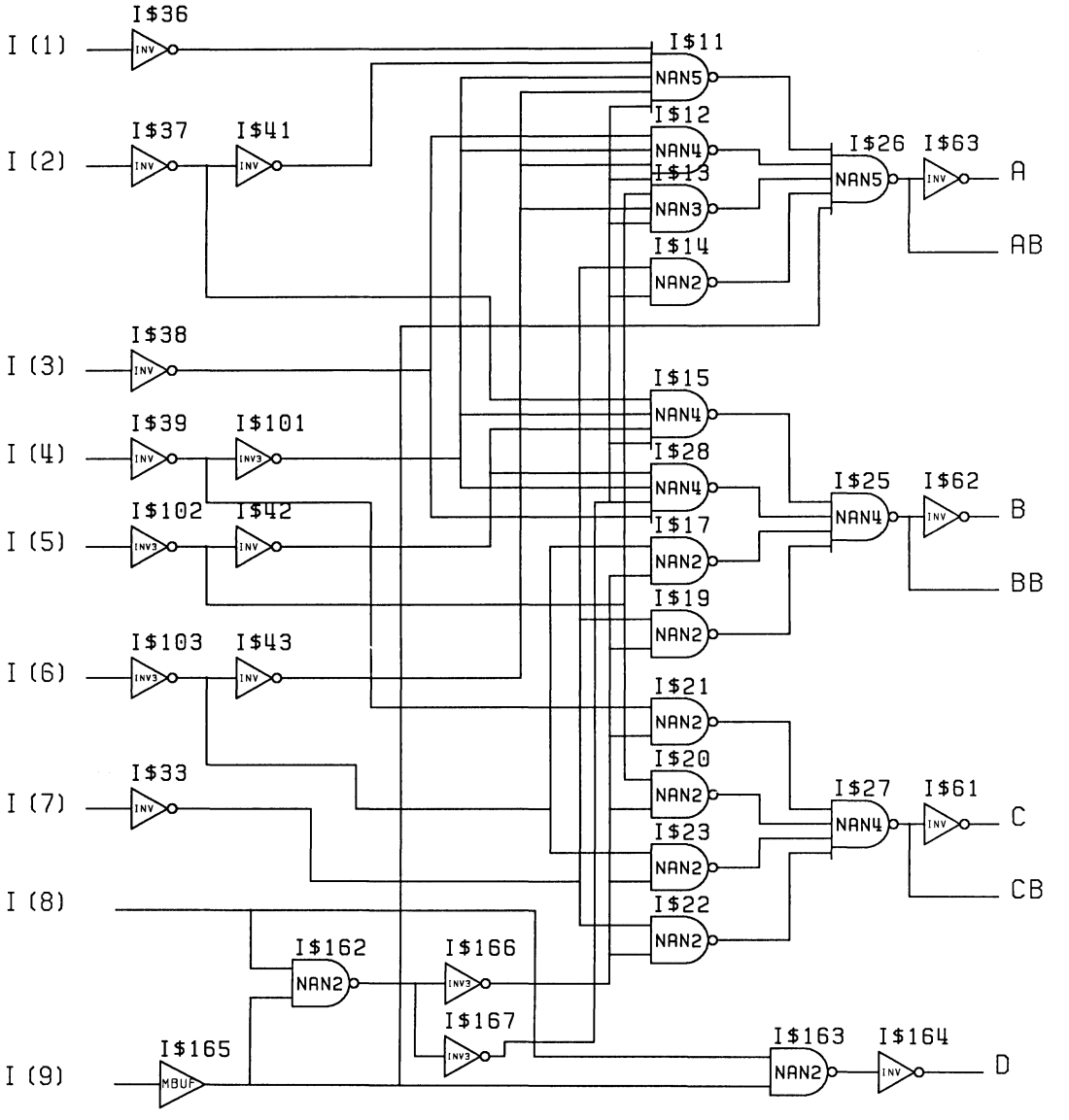
Symbol



Input									Output			
I(1)	I(2)	I(3)	I(4)	I(5)	I(6)	I(7)	I(8)	I(9)	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	L	H
H	H	L	H	H	H	H	H	H	H	H	L	L
H	H	H	L	H	H	H	H	H	H	L	H	H
H	H	H	H	L	H	H	H	H	H	L	H	L
H	H	H	H	H	L	H	H	H	H	L	L	H
H	H	H	H	H	H	L	H	H	H	L	L	L
H	H	H	H	H	H	H	L	H	L	H	H	H
H	H	H	H	H	H	H	H	L	L	H	H	L

SUPERCELLS

Schematic


I (1)
I (2)
I (3)
I (4)
I (5)
I (6)
I (7)
I (8)
I (9)
I$36
I$37
I$41
I$38
I$39
I$101
I$102
I$42
I$103
I$43
I$33
I$162
I$166
I$167
I$165
I$11
I$12
I$13
I$14
I$15
I$28
I$17
I$19
I$21
I$20
I$23
I$22
I$26
I$63
I$25
I$62
I$27
I$61
I$163
I$164
INV
INV3
MBUF
NAN5
NAN4
NAN3
NAN2
A
AB
B
BB
C
CB
D

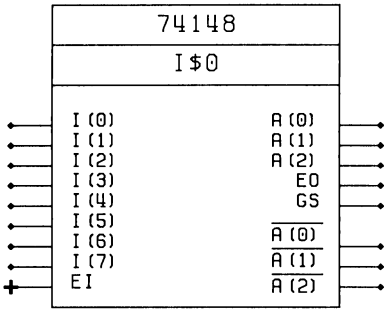
8–Line to 3–Line Priority Encoders

Description

This component encodes eight data lines to three–line binary (octal) when the enable EI is low. When the enable input EI is high, all outputs are high. Data inputs and outputs are active low. Width expansion is provided by cascading signals GS and E0. In addition to the outputs A(2), A(1), and A(0), their complements are available.

Name: 74148
Gates: 39.3

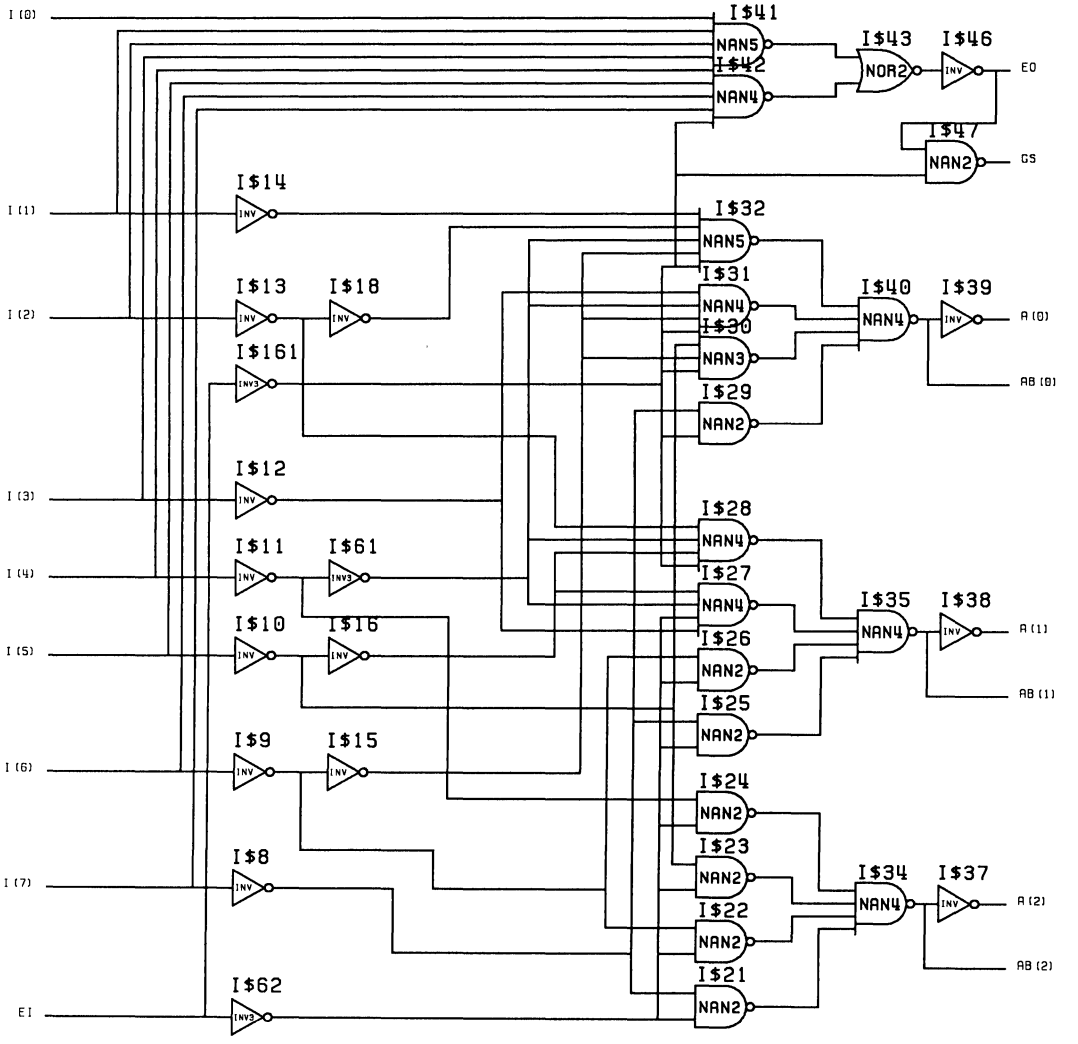
Symbol



Input									Output				
E!	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

SUPERCELLS

Schematic


I (0)
I (1)
I (2)
I (3)
I (4)
I (5)
I (6)
I (7)
EI
I$14
I$13
I$18
I$161
I$12
I$11
I$61
I$10
I$16
I$9
I$15
I$8
I$62
I$41
NAN5
I$42
NAN4
I$43
NOR2
I$46
EO
I$47
NAN2
GS
I$32
NAN5
I$31
NAN4
I$30
NAN3
I$29
NAN2
I$40
NAN4
I$39
A (0)
AB (0)
I$28
NAN4
I$27
NAN4
I$26
NAN2
I$25
NAN2
I$35
NAN4
I$38
A (1)
AB (1)
I$24
NAN2
I$23
NAN2
I$22
NAN2
I$21
NAN2
I$34
NAN4
I$37
A (2)
AB (2)

1 of 16 Data Multiplexer

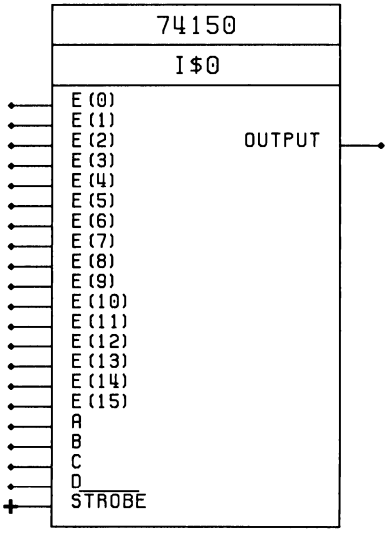
Description

This component selects the data on one of sixteen inputs and transfers it to the output. When the input $\overline{\text{STROBE}}$ is low, the complement of one of the sixteen data inputs (determined by the status of the select inputs A, B, C, D) is transferred to OUTPUT. When $\overline{\text{STROBE}}$ is high, OUTPUT will be high regardless of other input conditions.

Name: 74150
Gates: 66.0

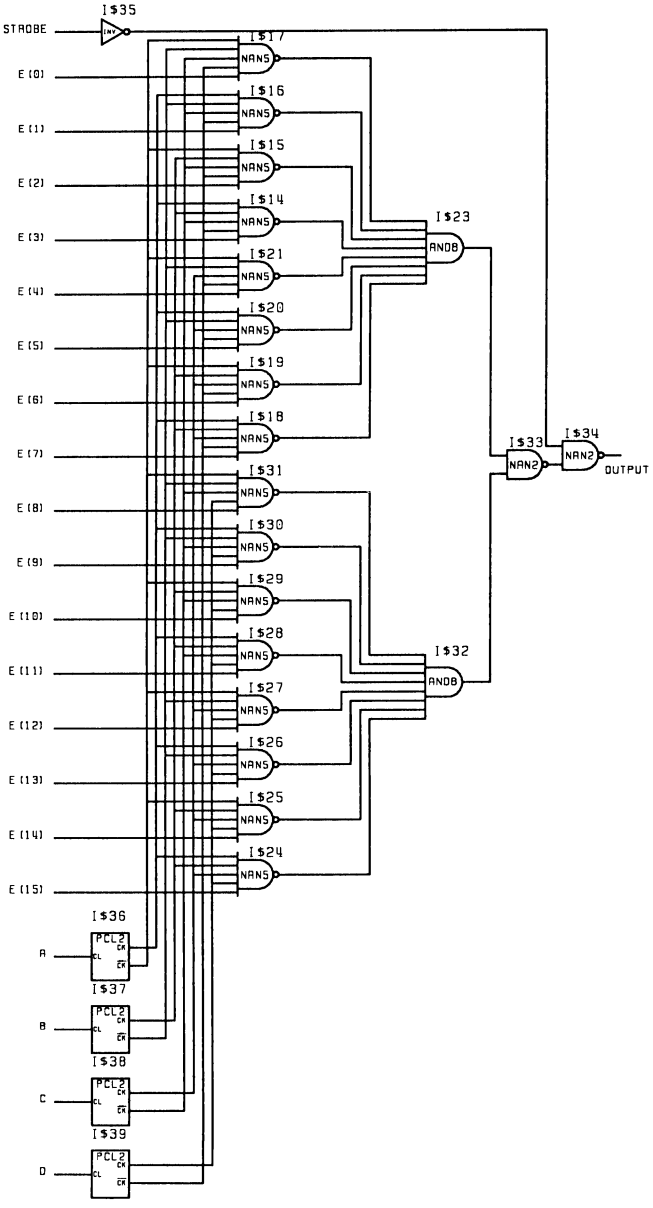
Input				Output	
Select				Strobe	
D	C	B	A	S	W
X	X	X	X	H	1
L	L	L	L	L	E0b
L	L	L	H	L	E1b
L	L	H	L	L	E2b
L	L	H	H	L	E3b
L	H	L	L	L	E4b
L	H	L	H	L	E5b
L	H	H	L	L	E6b
L	H	H	H	L	E7b
H	L	L	L	L	E8b
H	L	L	H	L	E9b
H	L	H	L	L	E10b
H	L	H	H	L	E11b
H	H	L	L	L	E12b
H	H	L	H	L	E13b
H	H	H	L	L	E14b
H	H	H	H	L	E15b

Symbol



SUPERCELLS

Schematic


I$35
STROBE
INV
E(0)
E(1)
E(2)
E(3)
E(4)
E(5)
E(6)
E(7)
E(8)
E(9)
E(10)
E(11)
E(12)
E(13)
E(14)
E(15)
I$17
I$16
I$15
I$14
I$21
I$20
I$19
I$18
I$31
I$30
I$29
I$28
I$27
I$26
I$25
I$24
NAN5
I$23
AND8
I$32
AND8
I$33
NAN2
I$34
NAN2
OUTPUT
I$36
I$37
I$38
I$39
PCL2
A
B
C
D

1 of 8 Data Multiplexer

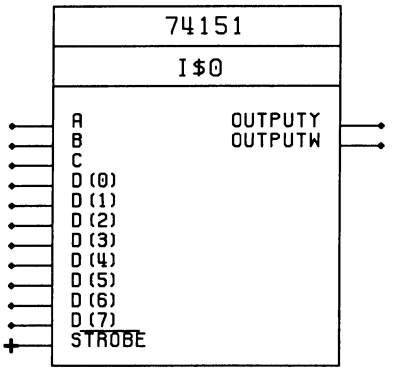
Description

This component selects the data on one of eight inputs and transfers it and its complement to the outputs. When the input $\overline{\text{STROBE}}$ is low, one of eight data inputs (determined by the status of the select inputs A, B, C) is transferred to OUTPUTY and its complement is transferred to OUTPUTW. When the input $\overline{\text{STROBE}}$ is high, OUTPUTY will be low and OUTPUTW will be high regardless of other input conditions.

Name: 74151
Gates: 31.8

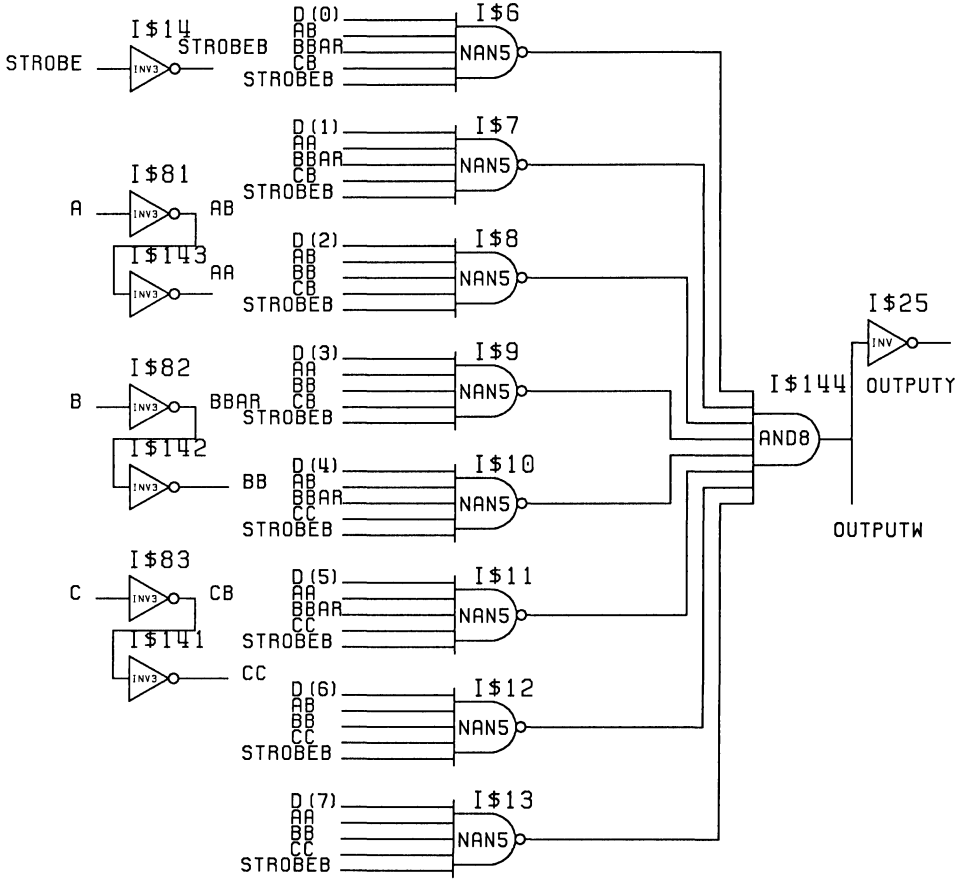
Input				Output	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	D0b
L	L	H	L	D1	D1b
L	H	L	L	D2	D2b
L	H	H	L	D3	D3b
H	L	L	L	D4	D4b
H	L	H	L	D5	D5b
H	H	L	L	D6	D6b
H	H	H	L	D7	D7b

Symbol



SUPERCELLS

Schematic


I$14
STROBE
INV3
STROBEB
I$81
A
INV3
AB
I$143
INV3
AA
I$82
B
INV3
BBAR
I$142
INV3
BB
I$83
C
INV3
CB
I$141
INV3
CC
D(0)
AB
BBAR
CB
STROBEB
I$6
NAN5
D(1)
AA
BBAR
CB
STROBEB
I$7
NAN5
D(2)
AB
BB
CB
STROBEB
I$8
NAN5
D(3)
AA
BB
CB
STROBEB
I$9
NAN5
D(4)
AB
BBAR
CC
STROBEB
I$10
NAN5
D(5)
AA
BBAR
CC
STROBEB
I$11
NAN5
D(6)
AB
BB
CC
STROBEB
I$12
NAN5
D(7)
AA
BB
CC
STROBEB
I$13
NAN5
AND8
I$144
I$25
INV
OUTPUTY
OUTPUTW

1 of 8 Data Multiplexer

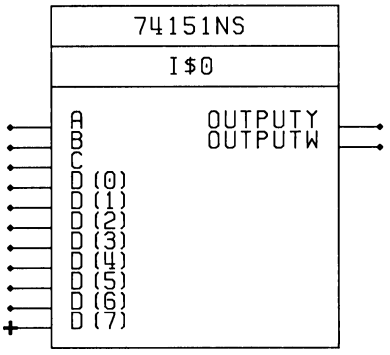
Description

The 74151NS component is the same as the 74151 except that it does not implement the input STROBE. This component selects the data on one of eight inputs and transfers it and its complement to the outputs. Depending on the signals applied to the select inputs (A,B,C), one of eight data inputs is transferred to OUTPUTY, and its complement is transferred to OUTPUTW.

Name: 74151NS
Gates: 26.8

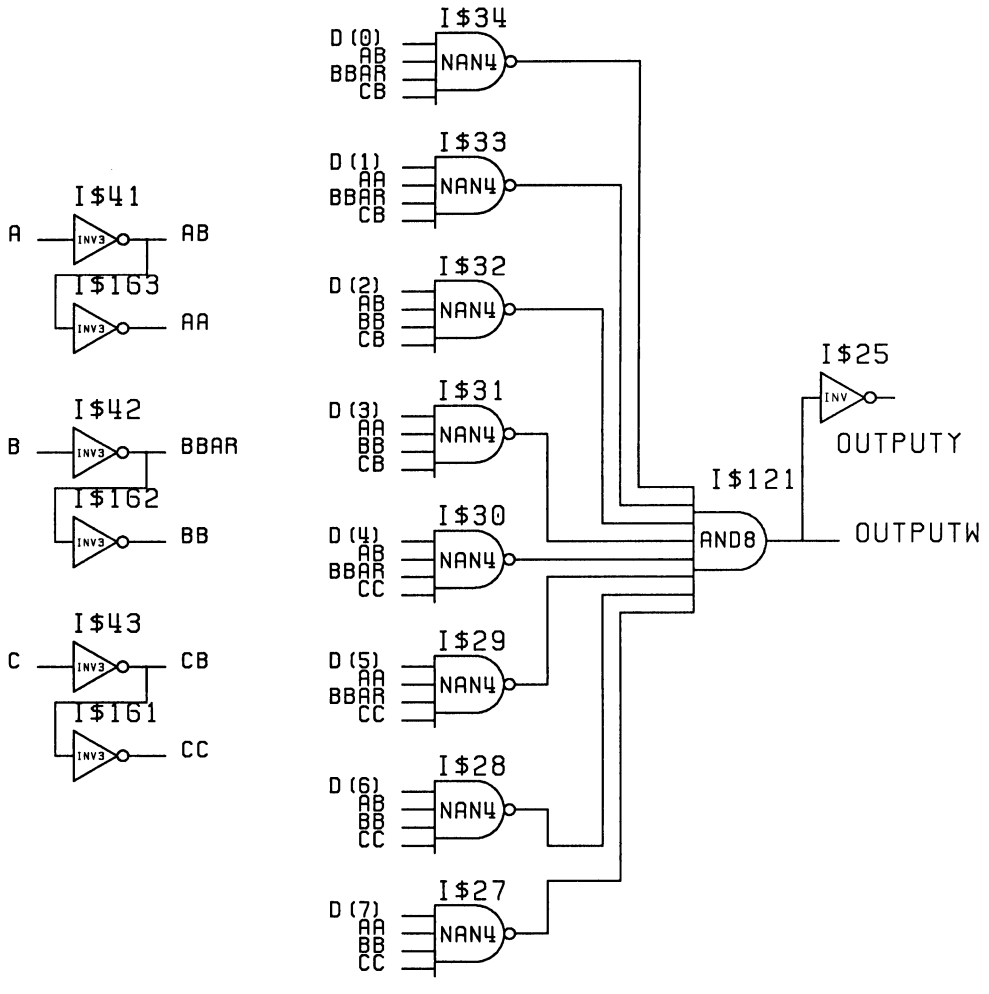
Input			Output	
C	B	A	Y	W
L	L	L	D0	D0b
L	L	H	D1	D1b
L	H	L	D2	D2b
L	H	H	D3	D3b
H	L	L	D4	D4b
H	L	H	D5	D5b
H	H	L	D6	D6b
H	H	H	D7	D7b

Symbol



SUPERCELLS

Schematic


I$41
A
INV3
AB
I$163
INV3
AA
I$42
B
INV3
BBAR
I$162
INV3
BB
I$43
C
INV3
CB
I$161
INV3
CC
I$34
D(0)
AB
BBAR
CB
NAN4
I$33
D(1)
AA
BBAR
CB
NAN4
I$32
D(2)
AB
BB
CB
NAN4
I$31
D(3)
AA
BB
CB
NAN4
I$30
D(4)
AB
BBAR
CC
NAN4
I$29
D(5)
AA
BBAR
CC
NAN4
I$28
D(6)
AB
BB
CC
NAN4
I$27
D(7)
AA
BB
CC
NAN4
I$121
AND8
I$25
INV
OUTPUTY
OUTPUTW

1 of 8 Data Multiplexer

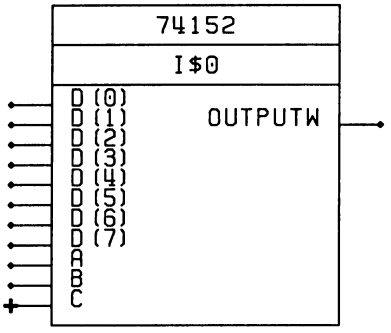
Description

This component selects the data on one of eight inputs and transfers its complement to the output. Depending on the signals applied to the select inputs (A, B, C), the complement of one of eight data inputs is transferred to OUTPUTW.

Name: 74152
Gates: 31.5

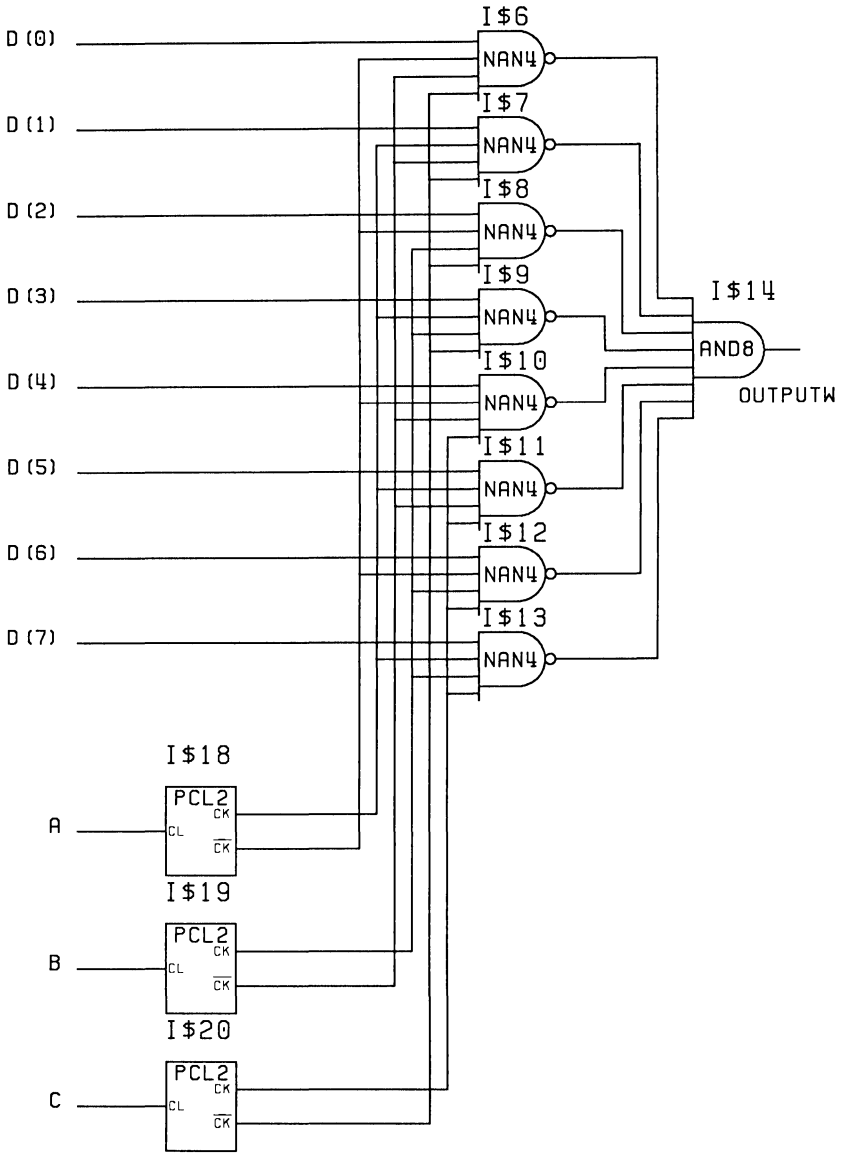
Input			Output
Select			
C	B	A	W
L	L	L	D0b
L	L	H	D1b
L	H	L	D2b
L	H	H	D3b
H	L	L	D4b
H	L	H	D5b
H	H	L	D6b
H	H	H	D7b

Symbol



SUPERCELLS

Schematic


D (0)
D (1)
D (2)
D (3)
D (4)
D (5)
D (6)
D (7)
I$6
NAN4
I$7
NAN4
I$8
NAN4
I$9
NAN4
I$10
NAN4
I$11
NAN4
I$12
NAN4
I$13
NAN4
I$14
AND8
OUTPUTW
I$18
PCL2
CK
CL
CK
A
I$19
PCL2
CK
CL
CK
B
I$20
PCL2
CK
CL
CK
C

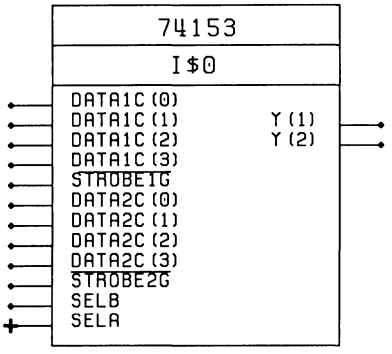
Dual 4–Line to 1–Line Data Multiplexers

Description

This component contains dual, 4–line to 1–line multiplexers with common select inputs (SELA and SELB) and individual enable inputs ($\overline{\text{STROBE1G}}$ and $\overline{\text{STROBE2G}}$). The individual active low enables can be used to strobe the corresponding outputs independently. When the enables are high, the corresponding outputs are forced low. When strobe is low, depending on the signals applied to the select inputs, one of four data inputs is transferred to the respective output of each multiplexer.

Name: 74153
Gates: 29.5

Symbol

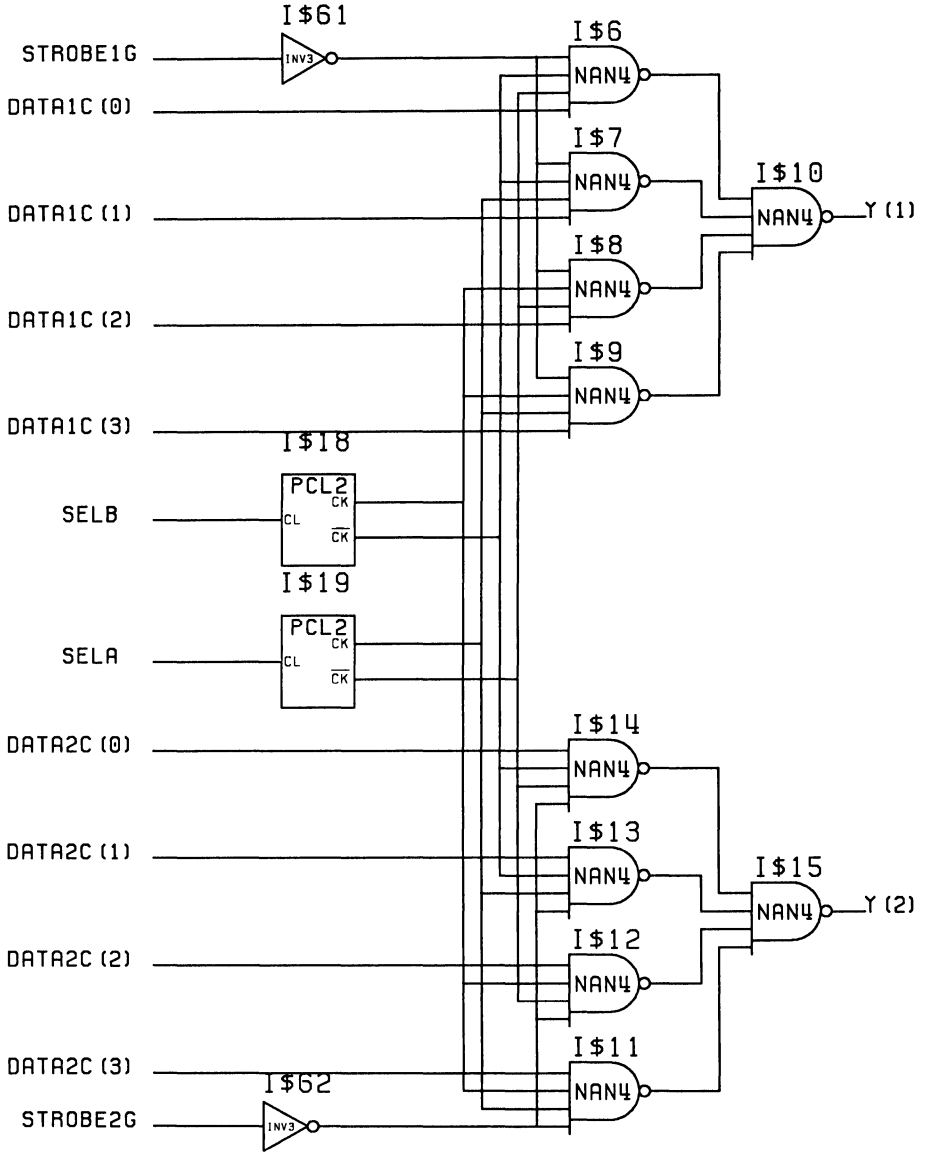


Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

SUPERCELLS

74153

Schematic



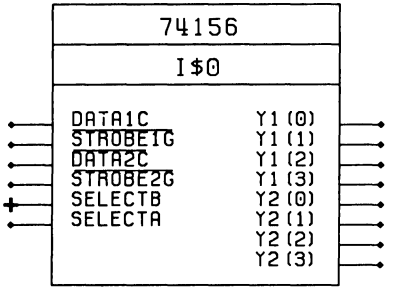
Dual 2–Line to 4–Line Decoder

Description

This component contains common address inputs and separate gated enable inputs which, when enabled, generate address inputs (SELECTA, SELECTB) for each decoder. The address inputs generate four mutually exclusive, active low outputs (Yn(0), Yn(1), Yn(2), Yn(3)). Individual strobes ($\overline{\text{STROBE1G}}$, $\overline{\text{STROBE2G}}$) allow activation/inhibition of each of the two 4-bit sections, as desired. Data applied to DATA1C is inverted at its outputs [Y1(0–3)] and data applied to DATA2C is not inverted at its outputs [Y2(0–3)]. This component can also be used as a 3-line to 8-line decoder or a 1-line to 8-line demultiplexer by tying DATA1C to DATA2C and STROBE1G to STROBE2G.

Name: 74156
Gates: 20.0

Symbol



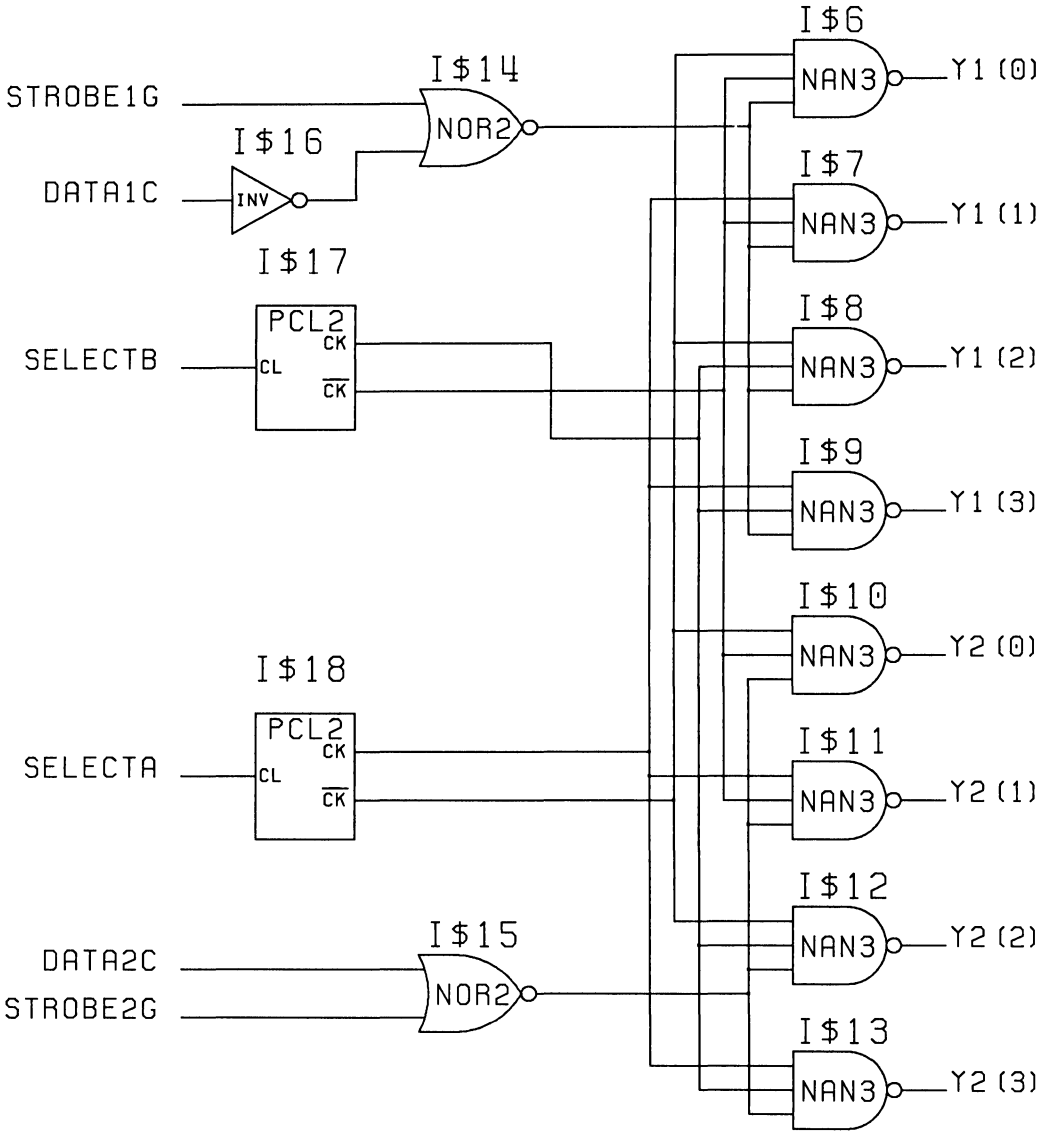
B	A	1G	1C	Y1(0)	Y1(1)	Y1(2)	Y1(3)
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

B	A	2G	2C	Y2(0)	Y2(1)	Y2(2)	Y2(3)
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

				3 line – 8 line configuration							
C	B	A	G	2Y(0)	2Y(1)	2Y(2)	2Y(3)	1Y(0)	1Y(1)	1Y(2)	1Y(3)
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

SUPERCELLS

Schematic

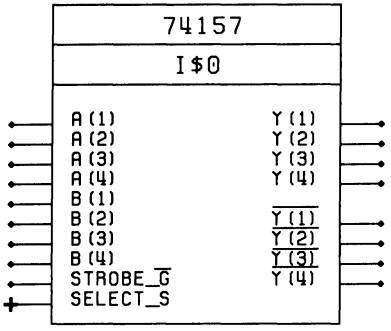

I$6
NAN3
Y1(0)
I$14
NOR2
STROBE1G
I$16
INV
DATA1C
I$7
NAN3
Y1(1)
I$17
PCL2
CK
CL
CK
SELECTB
I$8
NAN3
Y1(2)
I$9
NAN3
Y1(3)
I$10
NAN3
Y2(0)
I$18
PCL2
CK
CL
CK
SELECTA
I$11
NAN3
Y2(1)
I$12
NAN3
Y2(2)
I$15
NOR2
DATA2C
STROBE2G
I$13
NAN3
Y2(3)

Quad 2– to 1–Line Data Multiplexers

Description

Depending on the value of the inputs STROBE_$\overline{G}$ and SELECT_S, four bits of data are selected from one of two sources (A or B) and transferred to the outputs (Y and YB). STROBE_$\overline{G}$ is active low, and when it is low, it enables the selected inputs to be transferred to the outputs. When STROBE_$\overline{G}$ is high, all of the Y outputs are forced low, and all of the YB outputs are forced high, regardless of the other inputs. When SELECT_S is low, the A inputs are selected, and when it is high, the B inputs are selected. The Y outputs and their complements are available.

Symbol



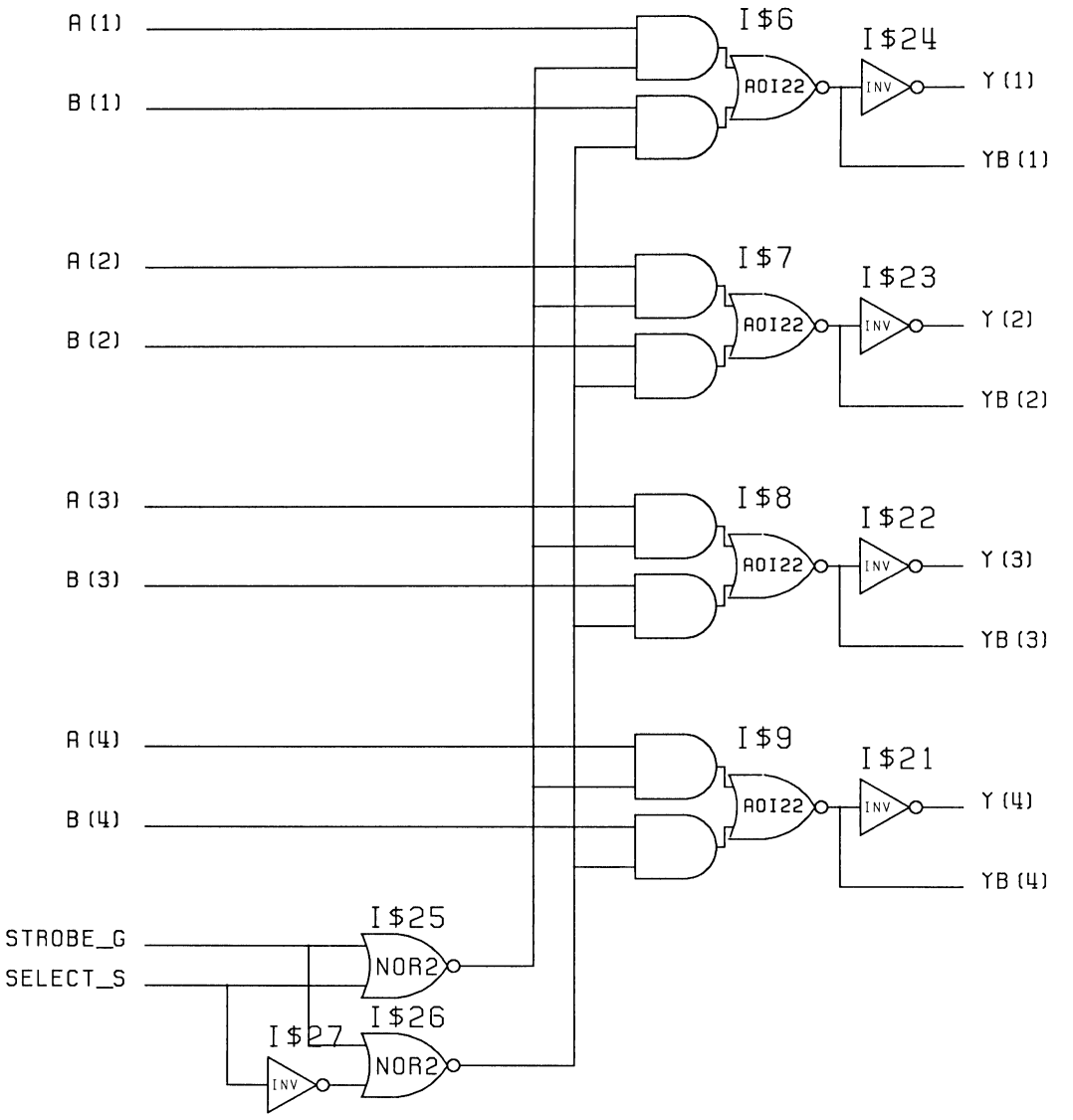
Name: 74157
Gates: 11.5

Strobe	Select	A(1)	A(2)	A(3)	A(4)	B(1)	B(2)	B(3)	B(4)	Y(1)	Y(2)	Y(3)	Y(4)
H	X	X	X	X	X	X	X	X	X	L	L	L	L
L	L					X	X	X	X	A(1)	A(2)	A(3)	A(4)
L	H	X	X	X	X					B(1)	B(2)	B(3)	B(4)

SUPERCELLS

74157

Schematic



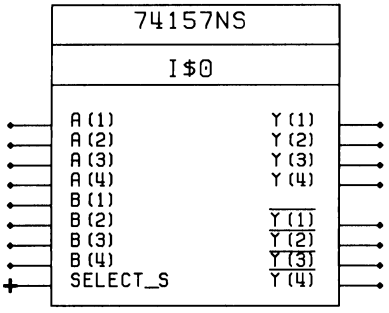
Quad 2– to 1–Line Data Multiplexers

Description

The 74157NS is the same as the component 74157 but without the STROBE_$\overline{G}$ input. Depending on the value of the input SELECT_S, four bits of data are selected from one of two sources (A or B) and transferred to the outputs (Y and YB). When SELECT_S is low, the A inputs are selected; and when it is high, the B inputs are selected. The Y outputs and their complements are available.

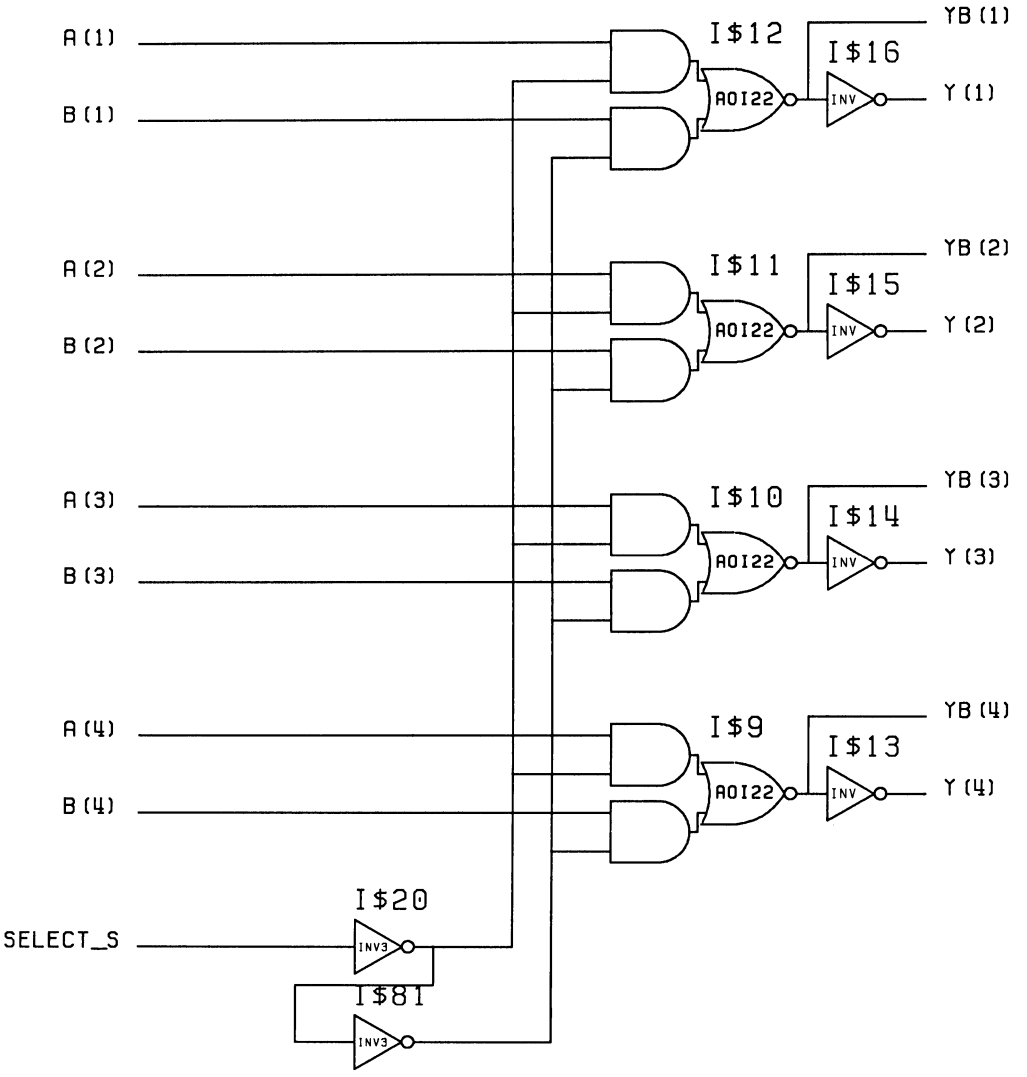
Name: 74157NS
Gates: 11.0

Symbol



SUPERCELLS

Schematic


A(1)
B(1)
A(2)
B(2)
A(3)
B(3)
A(4)
B(4)
SELECT_S
I$12
I$11
I$10
I$9
I$20
I$81
I$16
I$15
I$14
I$13
AOI22
INV
INV3
YB(1)
Y(1)
YB(2)
Y(2)
YB(3)
Y(3)
YB(4)
Y(4)

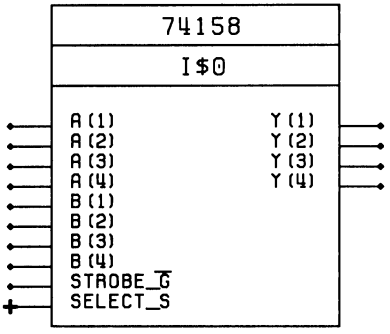
Quad 2– to 1–Line Multiplexers

Description

Depending on the value of the inputs STROBE_$\overline{G}$ and SELECT_S, four bits of data are selected from one of two sources (A or B), and their inverse is transferred to the outputs Y(1–4). STROBE_$\overline{G}$ is active low. When it is low, it enables the complements of the selected inputs to be transferred to the outputs, and when it is high, all of the outputs are forced high regardless of the other inputs. When SELECT_S is low, the A inputs are selected, and when it is high, the B inputs are selected.

Name: 74158
Gates: 9.5

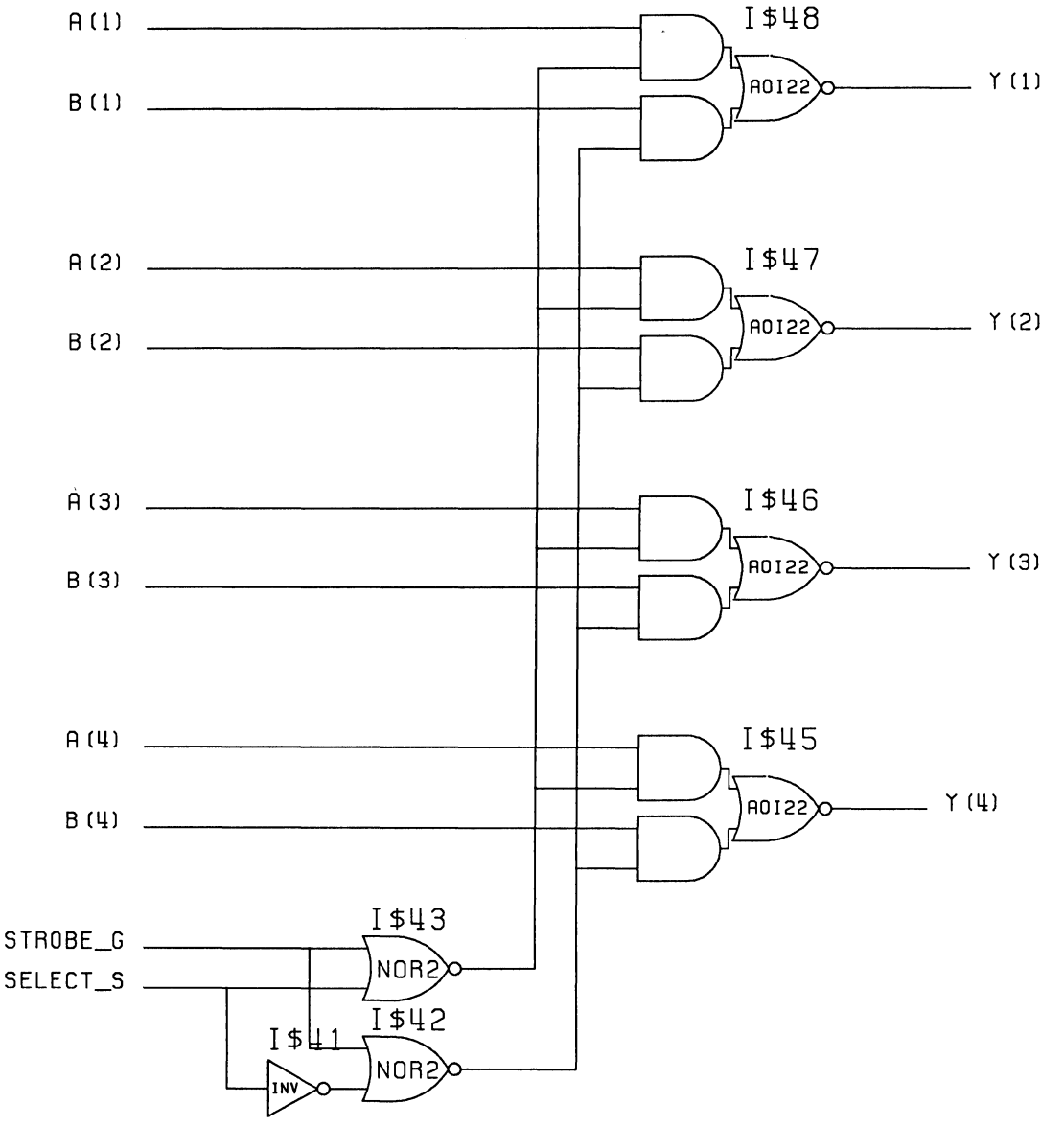
Symbol



Select S	Strobe G	A	B	Y
X	H	X	X	H
L	L	L	X	H
L	L	H	X	L
H	L	X	L	H
H	L	X	H	L

SUPERCELLS

Schematic


A(1)
B(1)
A(2)
B(2)
A(3)
B(3)
A(4)
B(4)
STROBE_G
SELECT_S
I$48
I$47
I$46
I$45
I$43
I$42
I$41
AOI22
NOR2
INV
Y(1)
Y(2)
Y(3)
Y(4)

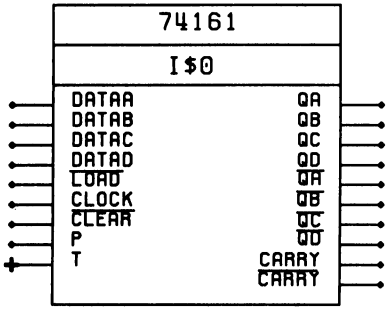
Synchronous 4–Bit Counter

Description

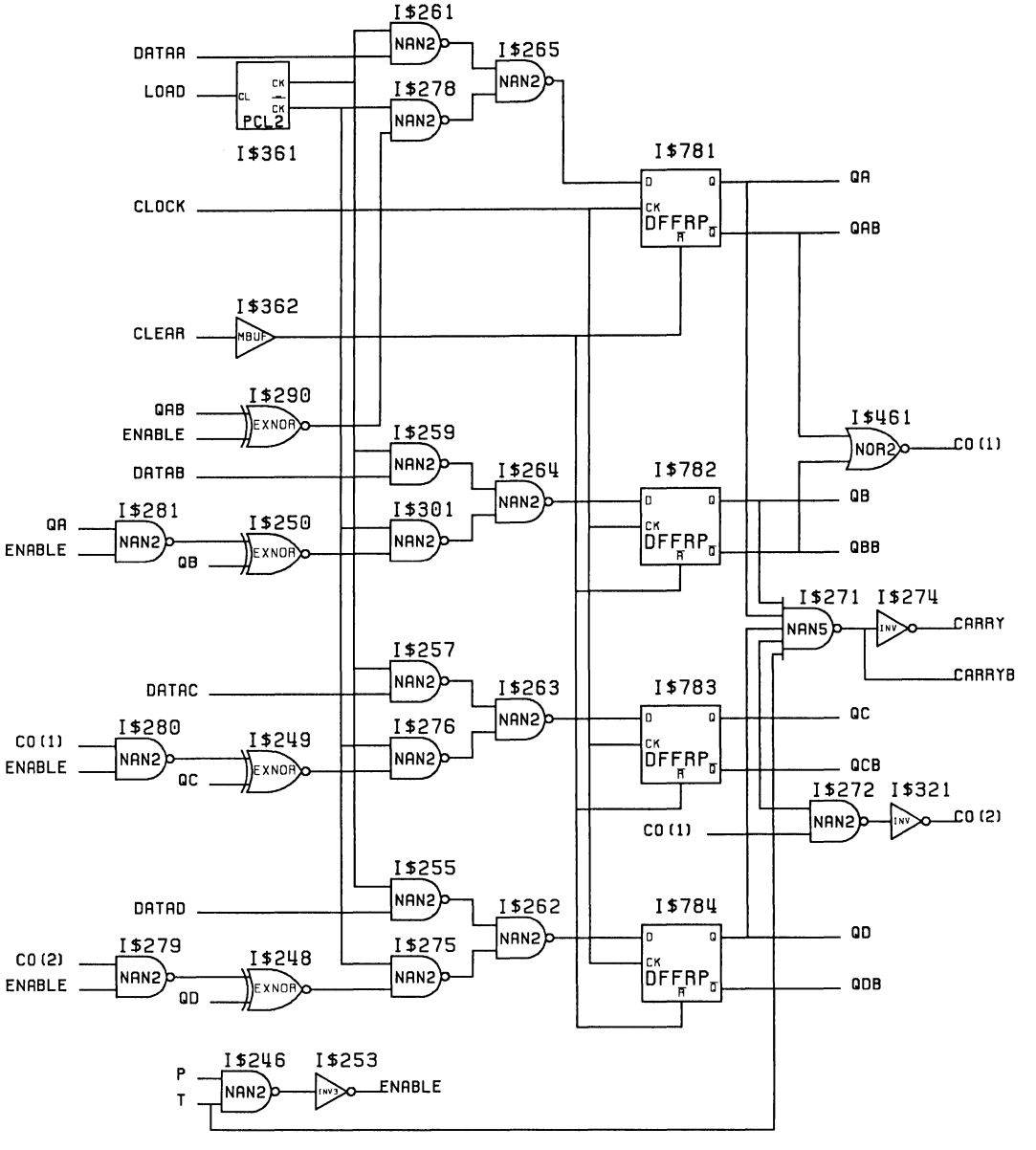
This component is a synchronous, 4–bit binary counter with a synchronous load, an asynchronous clear, and two count enables (P and T). Both P and T must be high to enable counting. The T input is used to enable the high–level overflow ripple carry output (CARRY). During loading and counting, the outputs change on the rising edge of the CLOCK. Both $\overline{\text{CLEAR}}$ and $\overline{\text{LOAD}}$ are active low. The complements of the listed outputs are also available.

Name: 74161
Gates: 77.3

Symbol



Schematic


I$261
NAN2
DATAA
I$265
NAN2
LOAD
CL
CK
CK
PCL2
I$278
NAN2
I$361
I$781
D
Q
QA
CK
DFFRP
R
QAB
CLOCK
I$362
MBUF
CLEAR
I$290
EXNOR
QAB
ENABLE
I$259
NAN2
I$461
NOR2
CO(1)
DATAB
I$264
NAN2
I$782
QB
QA
I$281
NAN2
I$301
NAN2
QBB
ENABLE
I$250
EXNOR
QB
I$271
I$274
NAN5
INV
CARRY
CARRYB
I$257
NAN2
DATAC
I$263
NAN2
I$783
QC
I$280
NAN2
I$276
NAN2
CO(1)
I$249
EXNOR
QCB
ENABLE
QC
I$272
I$321
NAN2
INV
CO(2)
CO(1)
I$255
NAN2
DATAD
I$262
NAN2
I$784
QD
I$279
NAN2
I$275
NAN2
CO(2)
I$248
EXNOR
QDB
ENABLE
QD
I$246
I$253
P
NAN2
INV3
ENABLE
T

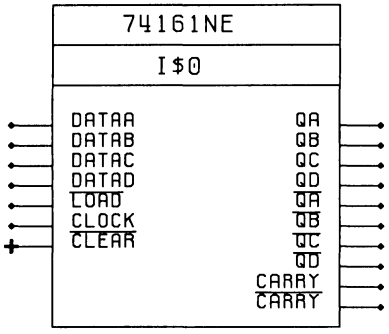
4–Bit Binary Counter No Enable

Description

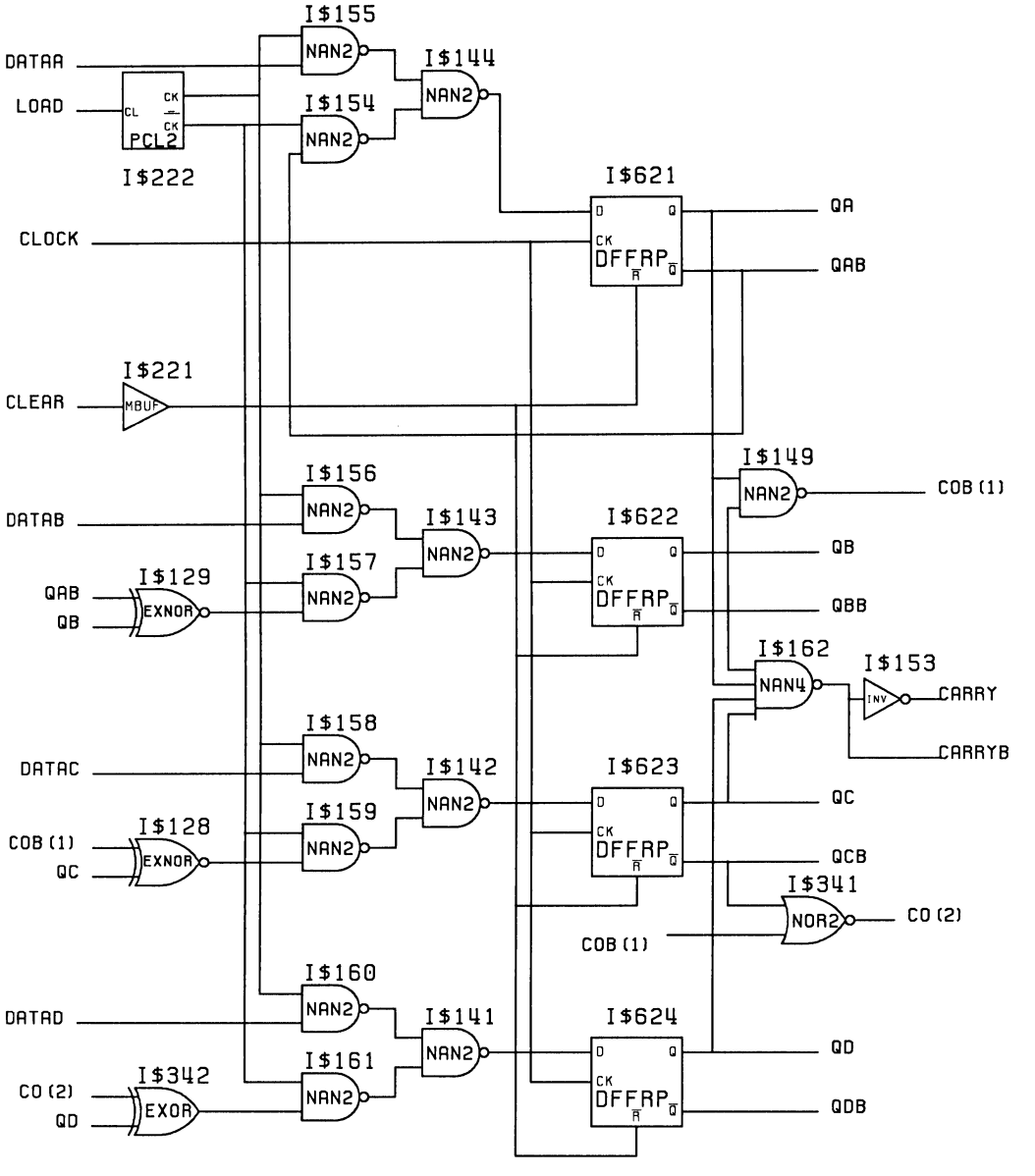
This component is a synchronous, 4–bit, binary counter with a synchronous load and an asynchronous clear. It has a high–level overflow, ripple carry output (CARRY). During loading and counting, the outputs change on the rising edge of the CLOCK input. Both $\overline{\text{CLEAR}}$ and $\overline{\text{LOAD}}$ are active low. The complements of the listed outputs are also available.

Name: 74161NE
Gates: 66.8

Symbol



Schematic


I$155
NAN2
I$144
NAN2
DATAA
LOAD
I$154
NAN2
PCL2
I$222
I$621
D
Q
CK
DFFRP
QA
QAB
CLOCK
I$221
MBUF
CLEAR
I$149
NAN2
COB(1)
I$156
NAN2
I$143
NAN2
I$622
DATAB
I$157
NAN2
QB
QBB
I$129
EXNOR
QAB
QB
I$162
NAN4
I$153
INV
CARRY
CARRYB
I$158
NAN2
I$142
NAN2
I$623
DATAC
I$159
NAN2
QC
QCB
I$128
EXNOR
COB(1)
QC
I$341
NOR2
CO(2)
COB(1)
I$160
NAN2
I$141
NAN2
I$624
DATAD
I$161
NAN2
QD
QDB
I$342
EXOR
CO(2)
QD

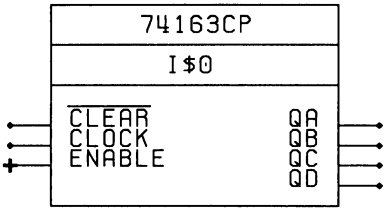
4–Bit Binary Counter

Description

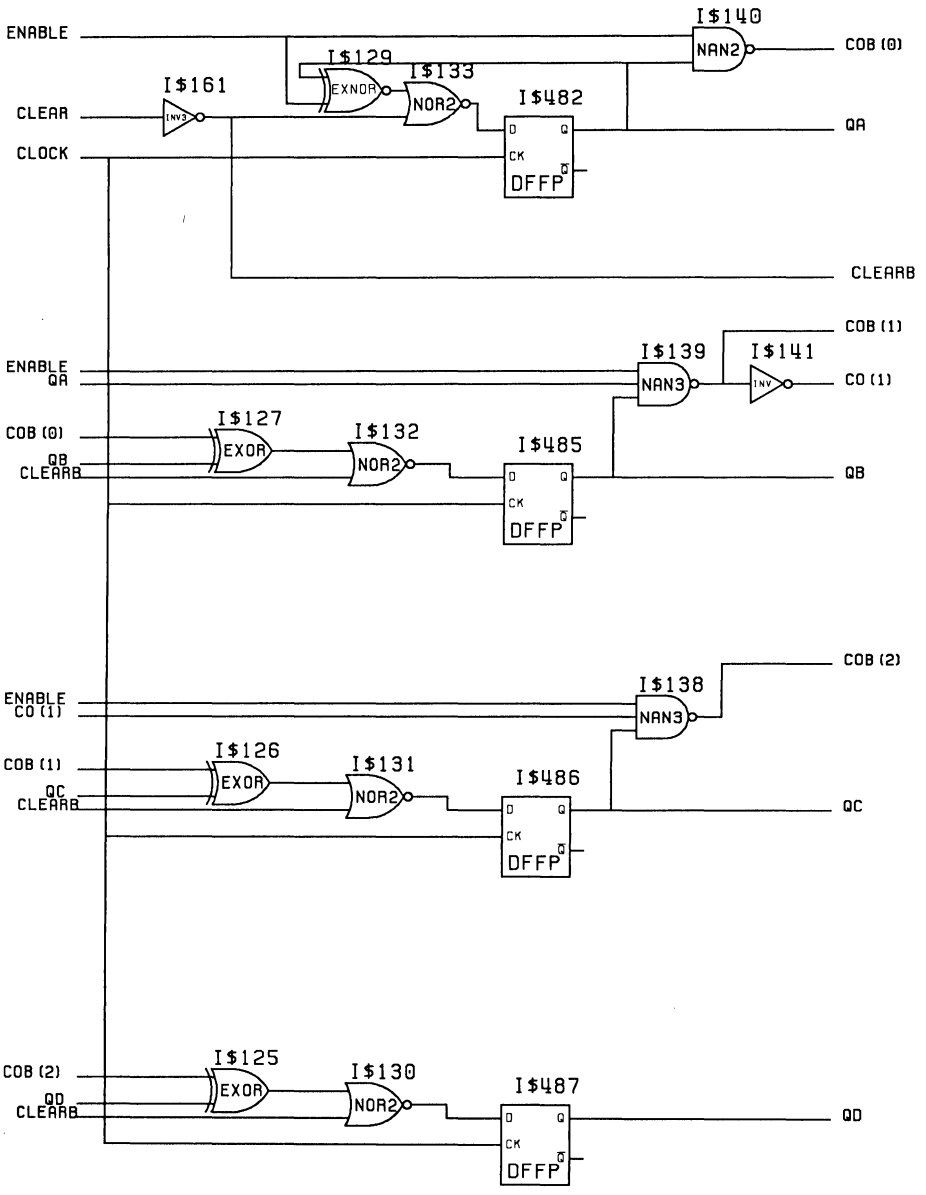
This component is a synchronous, 4–bit, binary counter with a synchronous clear and a count enable (ENABLE). ENABLE is active high to enable counting. During clearing and counting, the outputs change on the rising edge of the CLOCK input. $\overline{\text{CLEAR}}$ is active low.

Name: 74163CP
Gates: 52.0

Symbol



Schematic


ENABLE
CLEAR
CLOCK
I$161
INV3
I$129
EXNOR
I$133
NOR2
I$482
D
Q
CK
DFFP
I$140
NAN2
COB (0)
QA
CLEARB
COB (1)
ENABLE
QA
I$139
NAN3
I$141
INV
CO (1)
COB (0)
QB
CLEARB
I$127
EXOR
I$132
NOR2
I$485
QB
COB (2)
ENABLE
CO (1)
I$138
NAN3
COB (1)
QC
CLEARB
I$126
EXOR
I$131
NOR2
I$486
QC
COB (2)
QD
CLEARB
I$125
EXOR
I$130
NOR2
I$487
QD

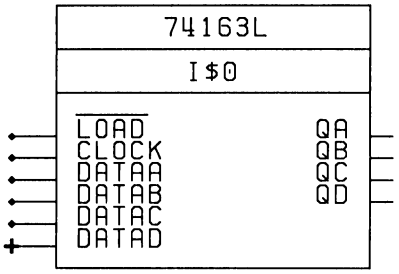
4–Bit Binary Counter

Description

This component is a synchronous, 4–bit, binary counter with a synchronous load. During loading and counting, the outputs change on the rising edge of the CLOCK input. $\overline{\text{LOAD}}$ is active low.

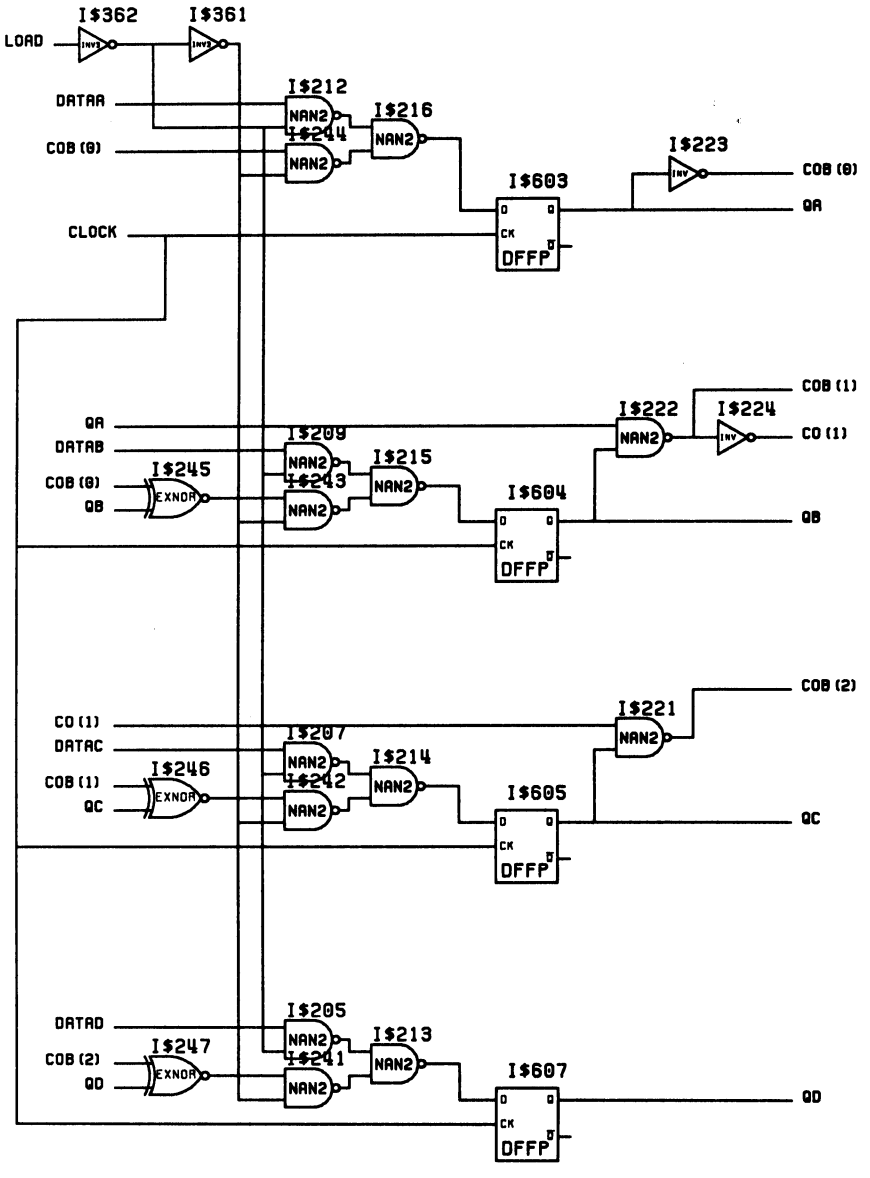
Name: 74163L
Gates: 55.5

Symbol



SUPERCELLS

Schematic


I$362
I$361
LOAD
INV2
DATAA
COB (0)
CLOCK
I$212
I$244
I$216
NAN2
I$603
DFFP
CK
D
Q
I$223
INV
COB (0)
QA
QA
DATAB
COB (0)
QB
I$245
EXNOR
I$209
I$243
I$215
I$604
I$222
I$224
COB (1)
CO (1)
QB
CO (1)
DATAC
COB (1)
QC
I$246
I$207
I$242
I$214
I$605
I$221
COB (2)
QC
DATAD
COB (2)
QD
I$247
I$205
I$241
I$213
I$607
QD

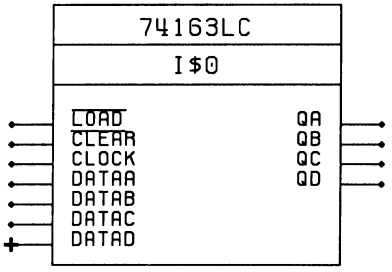
4–Bit Binary Counter

Description

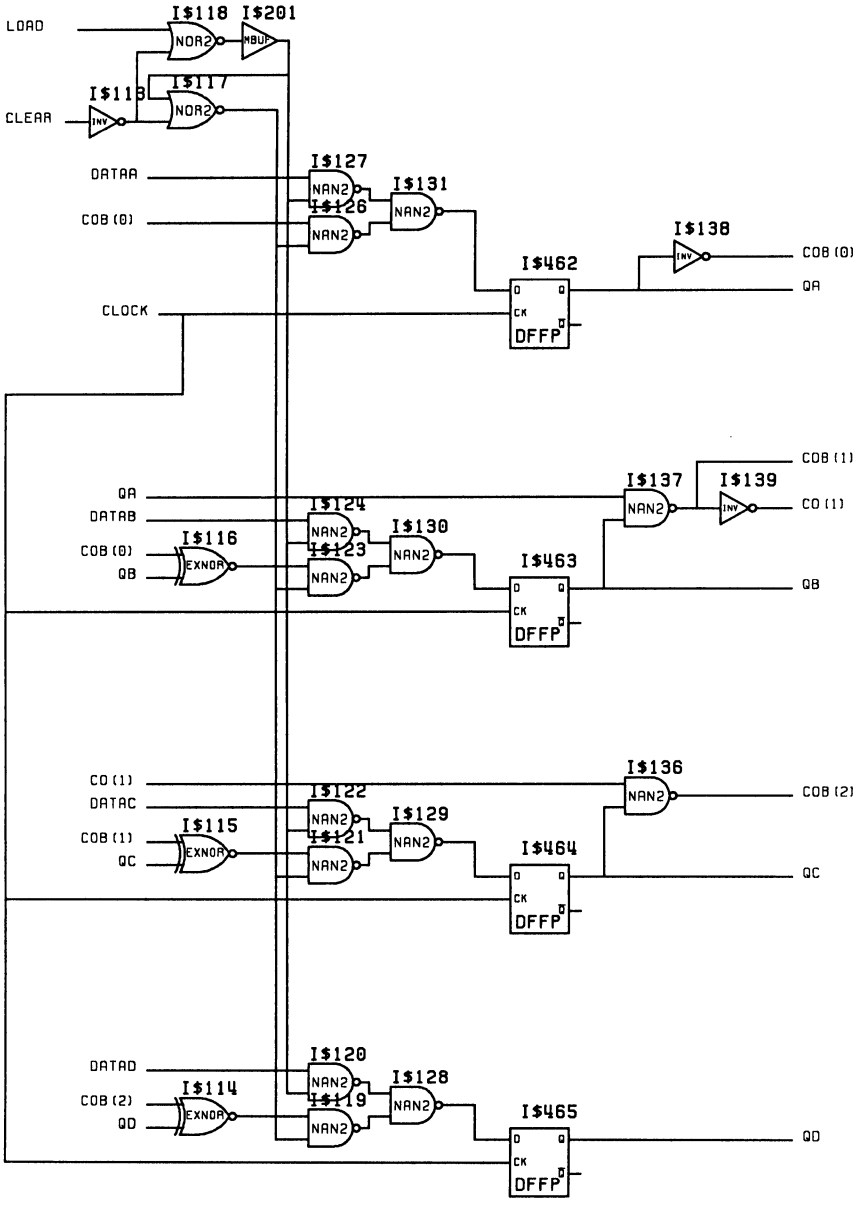
This component is a synchronous, 4–bit, binary counter with a synchronous load and clear. During loading, clearing, and counting, the outputs change on the rising edge of the CLOCK input. $\overline{\text{LOAD}}$ and $\overline{\text{CLEAR}}$ are active low.

Name: 74163LC
Gates: 57.0

Symbol



Schematic


LOAD
I$118
NOR2
I$201
MBUF
CLEAR
I$113
INV
I$117
NOR2
DATAA
COB(0)
I$127
NAN2
I$126
NAN2
I$131
NAN2
I$462
D
Q
CK
Q
DFFP
I$138
INV
COB(0)
QA
CLOCK
COB(1)
QA
DATAB
COB(0)
QB
I$116
EXNOR
I$124
NAN2
I$123
NAN2
I$130
NAN2
I$463
DFFP
I$137
NAN2
I$139
INV
CO(1)
QB
CO(1)
DATAC
COB(1)
QC
I$115
EXNOR
I$122
NAN2
I$121
NAN2
I$129
NAN2
I$464
DFFP
I$136
NAN2
COB(2)
QC
DATAD
COB(2)
QD
I$114
EXNOR
I$120
NAN2
I$119
NAN2
I$128
NAN2
I$465
DFFP
QD

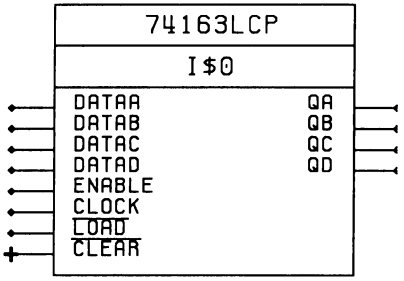
4–Bit Binary Counter

Description

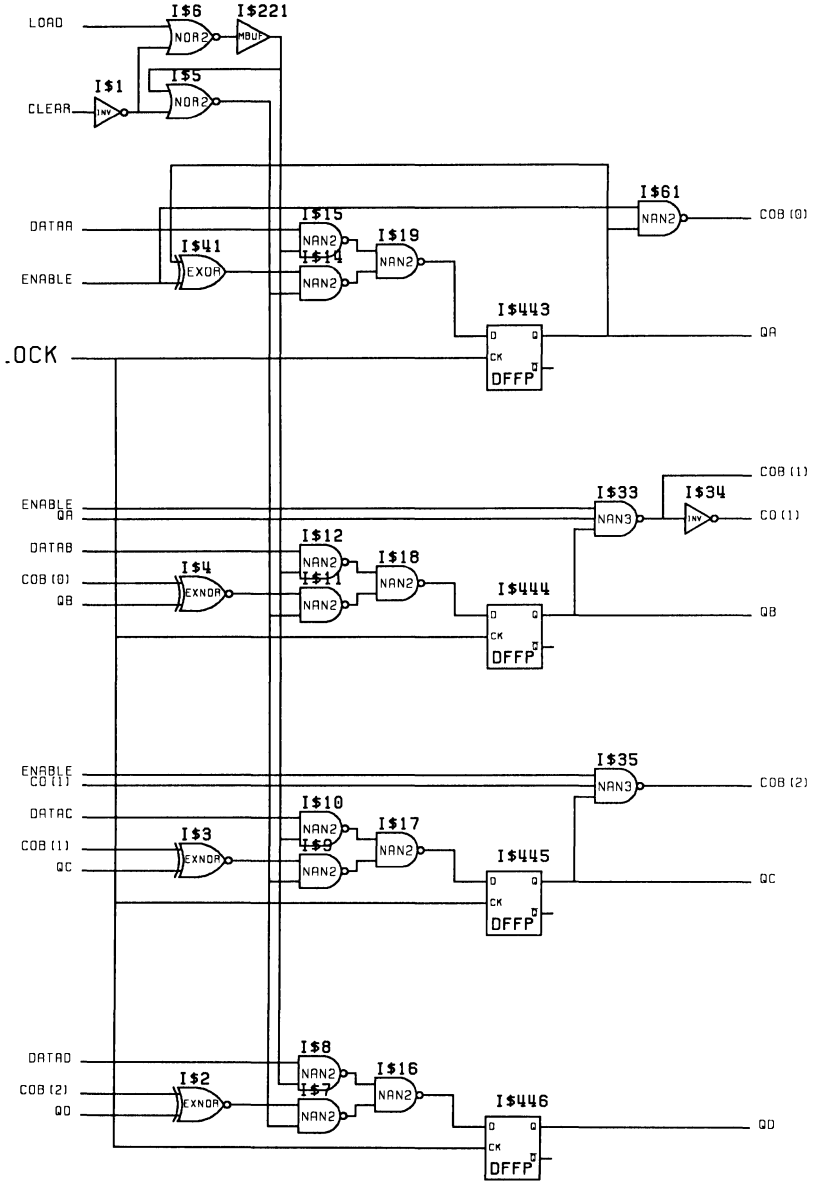
This component is a synchronous, 4-bit, binary counter with a synchronous load and clear and a count enable (ENABLE). ENABLE is active high to enable counting. During loading, clearing, and counting, the outputs change on the rising edge of the CLOCK input. $\overline{\text{LOAD}}$ and $\overline{\text{CLEAR}}$ are active low.

Name: 74163LCP
Gates: 62.5

Symbol



Schematic


LOAD
CLEAR
I$6
NOR2
I$221
MBUF
I$1
INV
I$5
NOR2
DATAA
ENABLE
I$41
EXOR
I$15
NAN2
I$14
NAN2
I$19
NAN2
I$61
NAN2
COB(0)
I$443
D
Q
CK
Q
DFFP
QA
.OCK
ENABLE
QA
DATAB
COB(0)
QB
I$4
EXNOR
I$12
NAN2
I$11
NAN2
I$18
NAN2
I$33
NAN3
I$34
INV
COB(1)
CO(1)
I$444
QB
ENABLE
CO(1)
DATAC
COB(1)
QC
I$3
EXNOR
I$10
NAN2
I$9
NAN2
I$17
NAN2
I$35
NAN3
COB(2)
I$445
QC
DATAD
COB(2)
QD
I$2
EXNOR
I$8
NAN2
I$7
NAN2
I$16
NAN2
I$446
QD

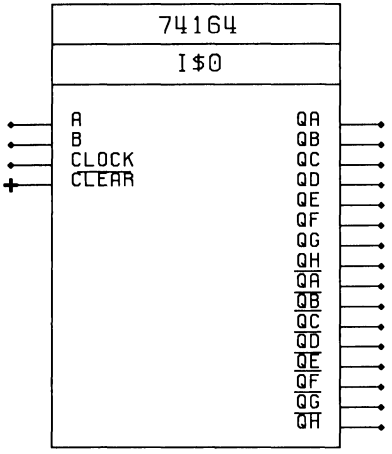
8–Bit Serial Shift Register

Description

This component is a positive edge–triggered, 8–bit shift register with a serial data input and true and inverted outputs (Q and QB) from each of the eight stages. Serial data enters through the AND of the inputs A and B into the D input of the first register. Each rising edge of the CLOCK input shifts data to the subsequent register. An active low $\overline{\text{CLEAR}}$ input forces true outputs low and complementary outputs high.

Name: 74164
Gates: 66.8

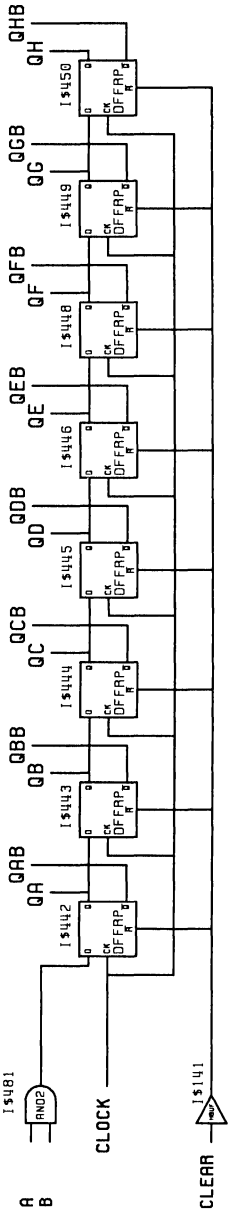
Symbol



Inputs				Outputs		
CLEARb	CLOCK	A	B	QA	QB...	QH
L	X	X	X	L	L	L
H	L	X	X	QA_0	QB_0	QH_0
H	↑	H	H	H	QA_N	QG_N
H	↑	L	X	L	QA_N	QG_N
H	↑	X	L	L	QA_N	QG_N

SUPERCELLS

Schematic


QHB
QH
I$450
QGB
QG
I$449
QFB
QF
I$448
QEB
QE
I$446
QDB
QD
I$445
QCB
QC
I$444
QBB
QB
I$443
QAB
QA
I$442
I$481
AND2
A
B
CLOCK
I$141
CLEAR

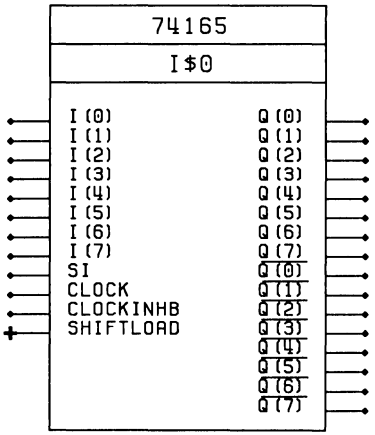
8–Bit Shift Register

Description

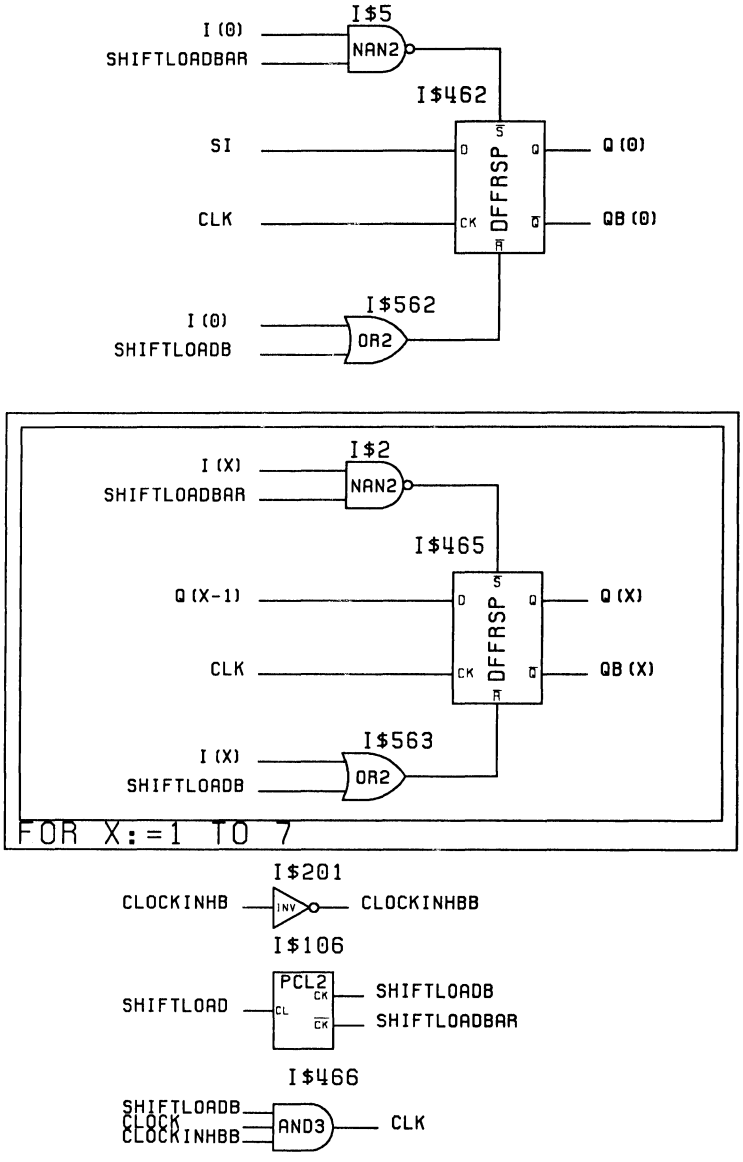
This 8-bit, serial shift register transfers data from Q(0) toward Q(7) on the rising edge of the CLOCK input. During shifting, the serial (SI) input is the data input to the first stage, Q(0). Asynchronous, parallel-in access is available at each stage through individual data inputs that are enabled by a falling transition on the SHIFTLOAD input, regardless of the level of CLOCK, CLOCKINHB or SI. When SHIFTLOAD is high, parallel loading is inhibited. The Q outputs and their complements are available.

Name: 74165
Gates: 108.0

Symbol



Schematic


I$5
I (0)
SHIFTLOADBAR
NAN2
I$462
SI
CLK
D
CK
DFFRSP
Q
QB
S
R
Q (0)
QB (0)
I$562
I (0)
SHIFTLOADB
OR2
I$2
I (X)
SHIFTLOADBAR
NAN2
I$465
Q (X-1)
CLK
Q (X)
QB (X)
I$563
I (X)
SHIFTLOADB
OR2
FOR X:=1 TO 7
I$201
CLOCKINHB
INV
CLOCKINHBB
I$106
SHIFTLOAD
PCL2
CL
CK
SHIFTLOADB
SHIFTLOADBAR
I$466
SHIFTLOADB
CLOCK
CLOCKINHBB
AND3
CLK

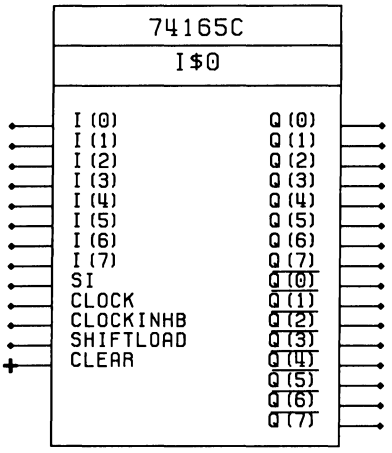
8–Bit Shift Register

Description

This 8-bit, serial shift register transfers data from Q(0) toward Q(7) on the rising edge of the CLOCK input. During shifting, the serial (SI) input is the data input to the first stage, Q(0). Asynchronous, parallel-in access is available at each stage through individual data inputs that are enabled by a falling transition of the SHIFTLOAD input, regardless of the level of CLOCK, CLOCKINHB or SI. When SHIFTLOAD is high, parallel loading is inhibited. This component, in addition to implementing the 74165 function, has an active high asynchronous clear. The Q outputs and their complements are available.

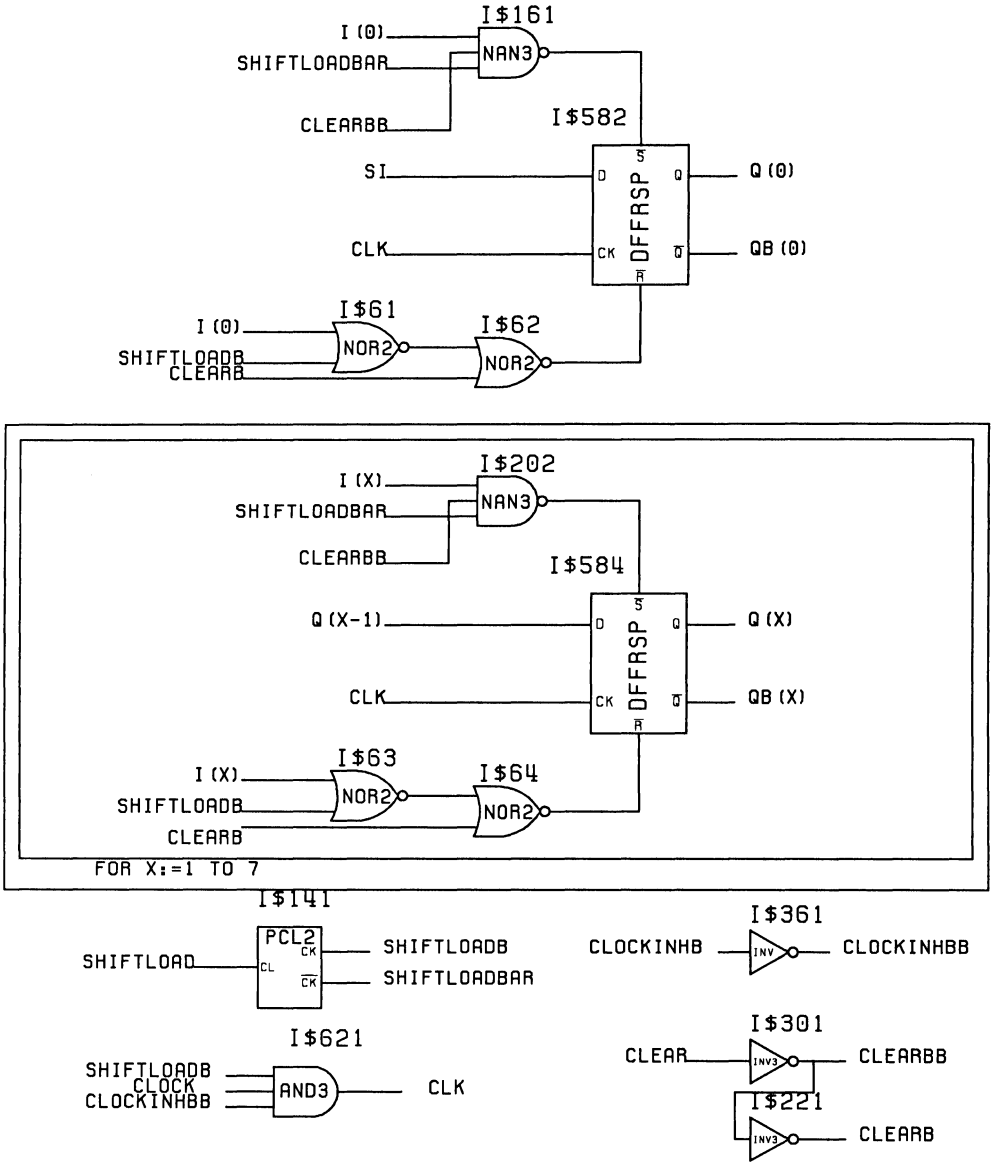
Name: 74165C
Gates: 118.0

Symbol



SUPERCELLS

Schematic


I$161
I(0)
SHIFTLOADBAR
NAN3
CLEARBB
I$582
SI
D
Q
Q(0)
CLK
CK
DFFRSP
QB(0)
I$61
I(0)
NOR2
I$62
SHIFTLOADB
CLEARB
NOR2
I$202
I(X)
SHIFTLOADBAR
NAN3
CLEARBB
I$584
Q(X-1)
D
Q
Q(X)
CLK
CK
DFFRSP
QB(X)
I$63
I(X)
NOR2
I$64
SHIFTLOADB
CLEARB
NOR2
FOR X:=1 TO 7
I$141
PCL2
SHIFTLOAD
CL
CK
SHIFTLOADB
SHIFTLOADBAR
I$361
CLOCKINHB
INV
CLOCKINHBB
I$621
SHIFTLOADB
CLOCK
CLOCKINHBB
AND3
CLK
I$301
CLEAR
INV3
CLEARBB
I$221
INV3
CLEARB

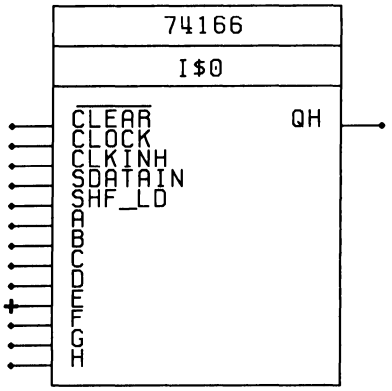
8–Bit Shift Register

Description

This 8-bit, parallel-in or serial-in shift register transfers data toward QH on the rising edge of the CLOCK input. During shifting, the serial input (SDATAIN) is the data input to the first stage, QA. Synchronous, parallel-in access is available at each stage through individual data inputs that are loaded on the rising edge of CLOCK when the inputs SHF_LD and CLKINH are low. $\overline{\text{CLEAR}}$ input is asynchronous and active low.

Name: 74166
Gates: 89.0

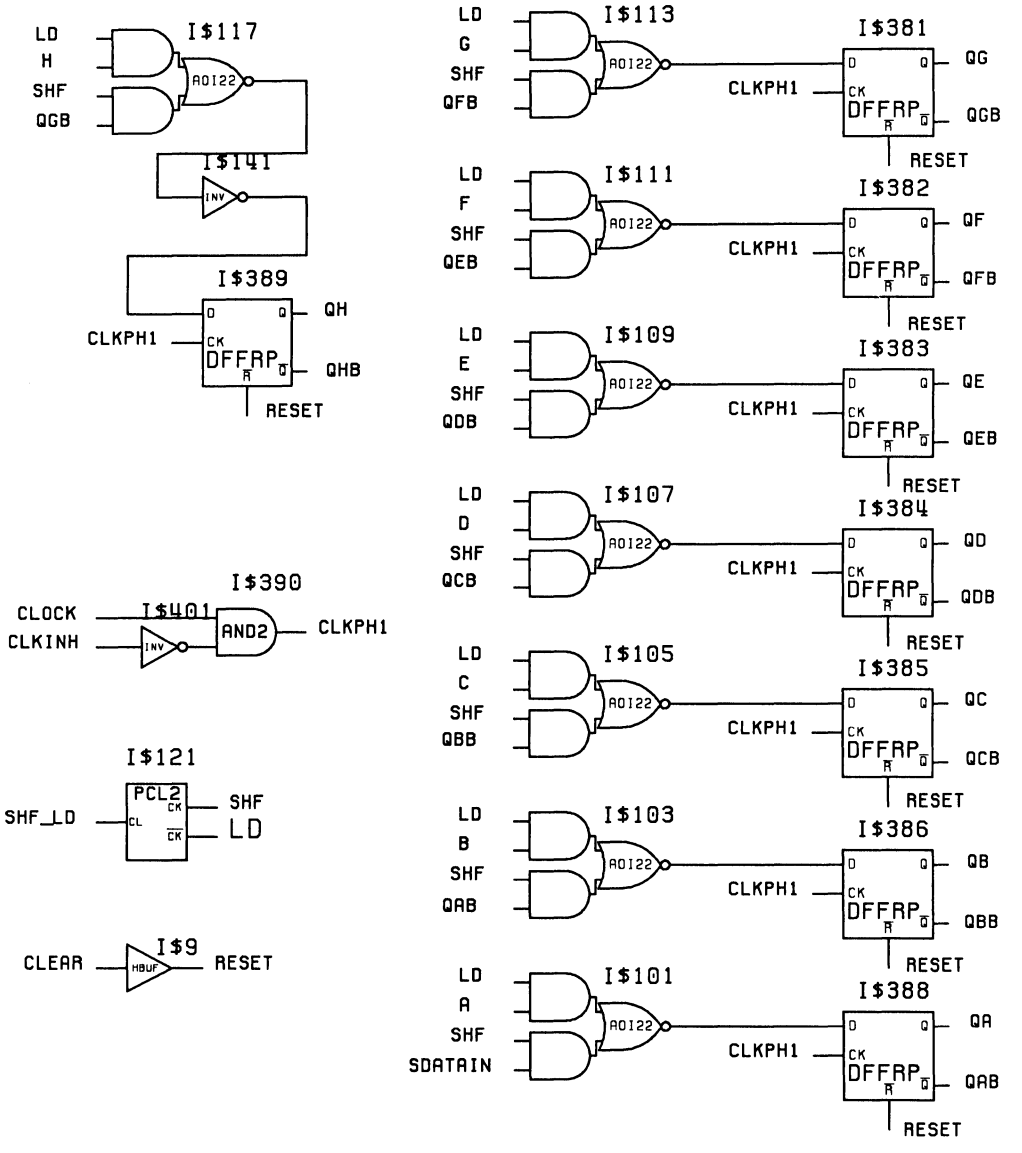
Symbol



Inputs						Internal Outputs		Outputs
CLEARb	SHF_LD	CLKINH	CLOCK	SDATAIN	PARALLEL I(0) ... I(7)	QA	QB	QH
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA_0	QB_0	QH_0
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	QA_N	QG_N
H	H	L	↑	L	X	L	QA_N	QG_N
H	X	H	↑	X	X	QA_0	QB_N	QH_N

SUPERCELLS

Schematic

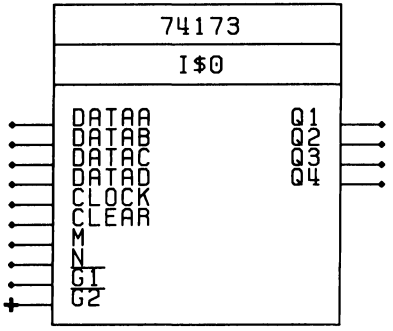

LD
H
SHF
QGB
I$117
AOI22
I$141
INV
I$389
D
Q
CK
DFFRP
QH
QHB
CLKPH1
RESET
CLOCK
CLKINH
I$401
INV
I$390
AND2
CLKPH1
I$121
PCL2
CK
CL
SHF_LD
SHF
LD
CLEAR
I$9
HBUF
RESET
LD
G
SHF
QFB
I$113
CLKPH1
I$381
QG
QGB
RESET
LD
F
SHF
QEB
I$111
I$382
QF
QFB
LD
E
SHF
QDB
I$109
I$383
QE
QEB
LD
D
SHF
QCB
I$107
I$384
QD
QDB
LD
C
SHF
QBB
I$105
I$385
QC
QCB
LD
B
SHF
QAB
I$103
I$386
QB
QBB
LD
A
SHF
SDATAIN
I$101
I$388
QA
QAB

Quad D–Type Flip–Flops

Description

This component contains four, positive edge–triggered flip–flops with individual D–type inputs and tristate true outputs. Each flip–flop will store the state of the corresponding D input on the rising edge of the CLOCK input, when CLEAR, $\overline{G1}$, and $\overline{G2}$ are low. When the gated, output–enable control lines (M and N) are both low, the contents of the flip–flops are available at the Q outputs. A high on either output–enable control line brings the outputs to the high–impedance state. Placing the output in a tristate mode does not inhibit the internal data capture. A high on CLEAR asynchronously resets the flip–flops.

Symbol

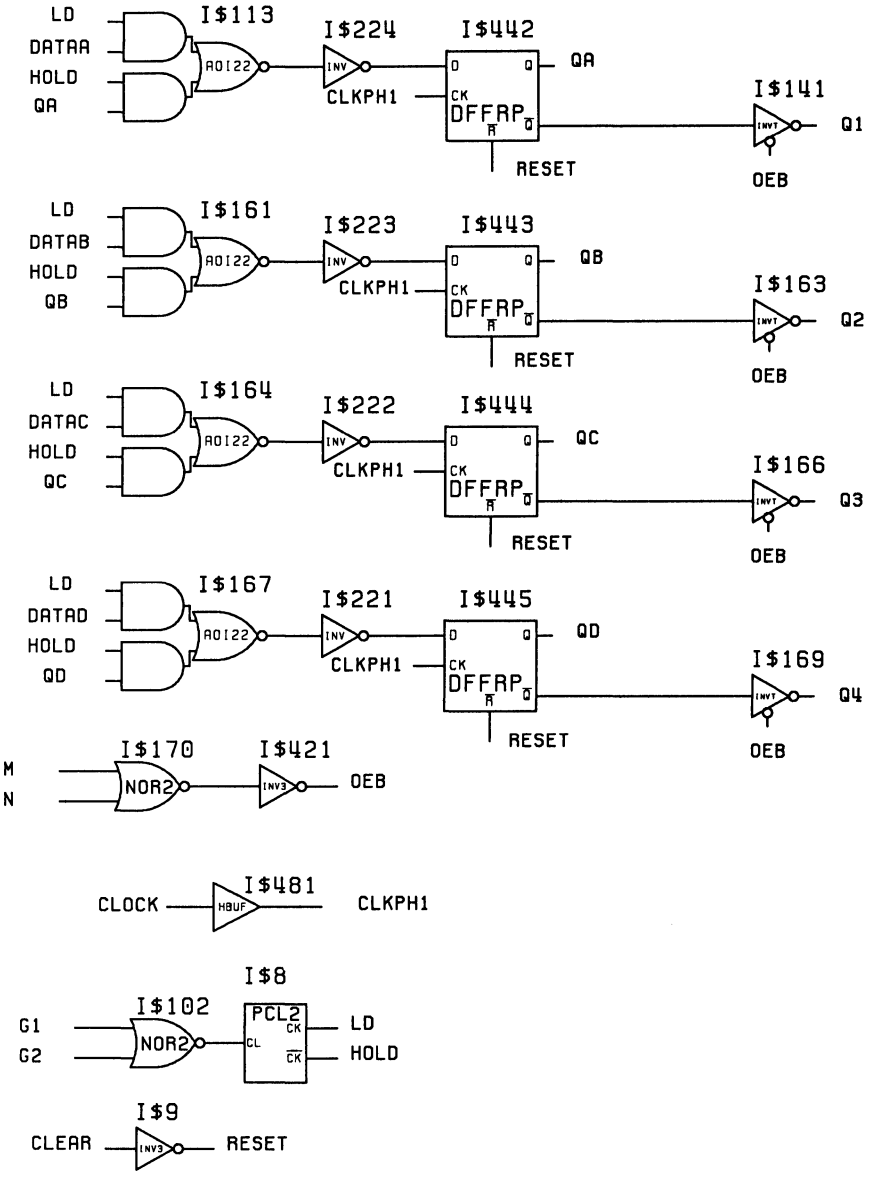


Name: 74173
Gates: 57.3

Inputs							Output
M	N	CLEAR	CLOCK	G1	G2	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	Q_0
L	L	L	↑	H	X	X	Q_0
L	L	L	↑	X	H	X	Q_0
L	L	L	↑	L	L	L	L
L	L	L	↑	L	L	H	H
H	X	X	X	X	X	X	X_Z
X	H	X	X	X	X	X	X_Z

SUPERCELLS

Schematic


LD
DATAA
HOLD
QA
I$113
AOI22
I$224
INV
CLKPH1
I$442
D
Q
CK
DFFRP
RESET
QA
I$141
INVT
OEB
Q1
LD
DATAB
HOLD
QB
I$161
AOI22
I$223
INV
CLKPH1
I$443
D
Q
CK
DFFRP
RESET
QB
I$163
INVT
OEB
Q2
LD
DATAC
HOLD
QC
I$164
AOI22
I$222
INV
CLKPH1
I$444
D
Q
CK
DFFRP
RESET
QC
I$166
INVT
OEB
Q3
LD
DATAD
HOLD
QD
I$167
AOI22
I$221
INV
CLKPH1
I$445
D
Q
CK
DFFRP
RESET
QD
I$169
INVT
OEB
Q4
M
N
I$170
NOR2
I$421
INV3
OEB
CLOCK
I$481
HBUF
CLKPH1
I$8
G1
G2
I$102
NOR2
PCL2
CK
CL
LD
HOLD
I$9
CLEAR
INV3
RESET

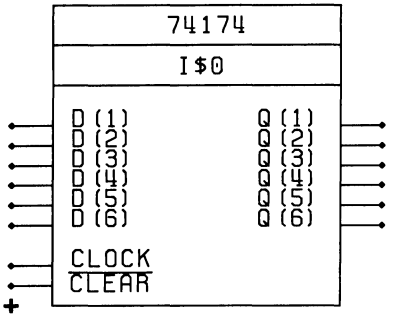
Hex D–Type Flip–Flops

Description

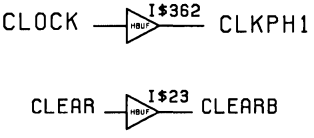
This component contains six, positive edge–triggered, D flip–flops with common $\overline{\text{CLEAR}}$ and CLOCK inputs. For each flip–flop, the D–input state is transferred to its Q output on the rising edge of CLOCK. A low on the $\overline{\text{CLEAR}}$ input forces all outputs low.

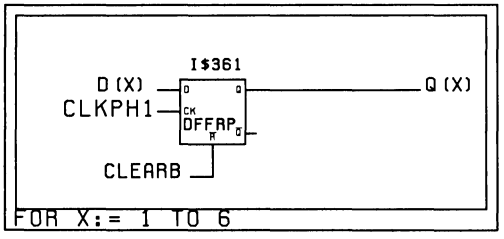
Name: 74174
Gates: 51.0

Symbol



Schematic





SUPERCELLS

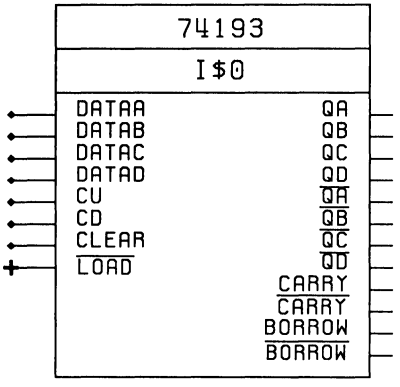
4–Bit Up/Down Binary Counter

Description

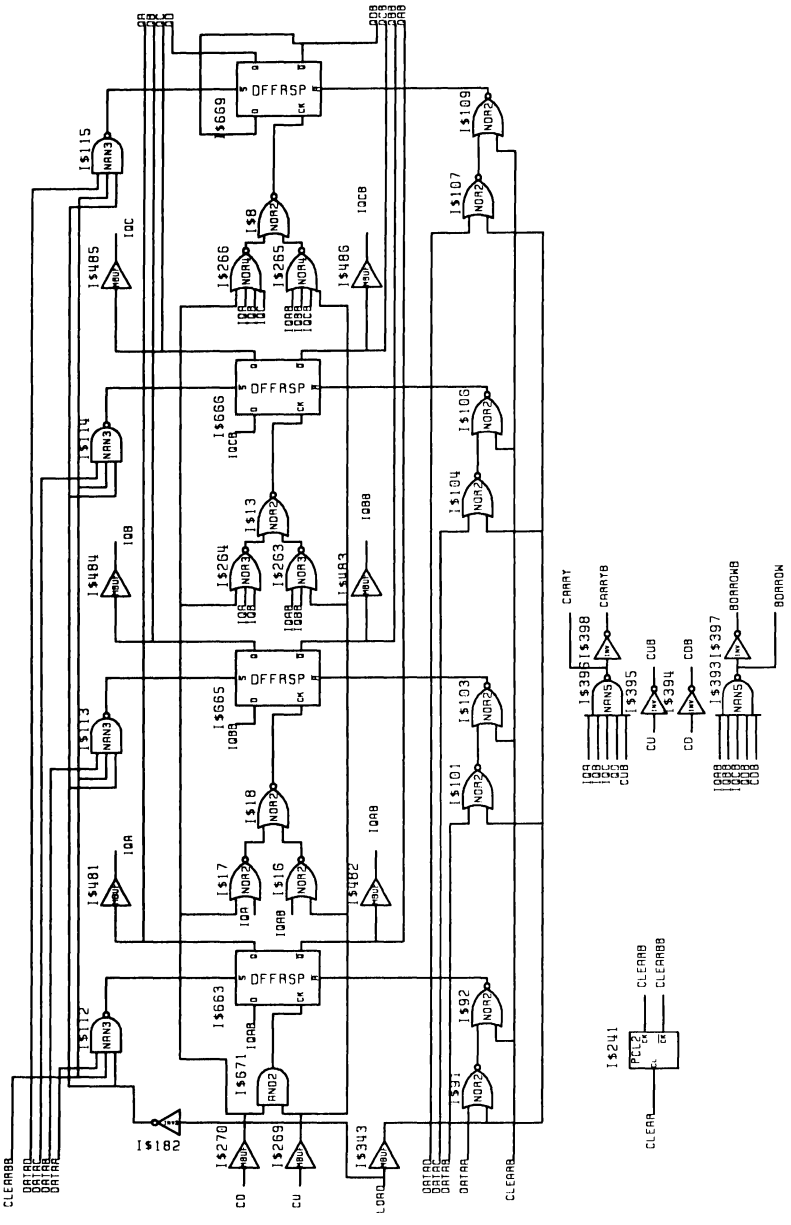
This component is a synchronous, 4–bit, up/down binary counter with dual clocks, and asynchronous clear and load. The active high CLEAR input forces all outputs low. Each output may be preset by entering the desired level on data inputs while $\overline{\text{LOAD}}$ is low. Counting occurs with each rising edge of the count up (CU) or count down (CD) clock. The clock input that is not active must be held high. Both borrow and carry outputs are available to cascade both the up and down counting functions. The complements of the listed outputs are also available.

Name: 74193
Gates: 89.0

Symbol



Schematic


DFFRSP
I$669
I$666
I$665
I$663
I$671
I$270
I$269
I$343
I$182
I$115
I$114
I$113
I$112
I$485
I$484
I$481
I$486
I$483
I$482
I$266
I$265
I$264
I$263
I$8
I$13
I$18
I$17
I$16
I$109
I$107
I$106
I$104
I$103
I$101
I$92
I$31
I$398
I$396
I$395
I$394
I$393
I$397
I$241
CLEARB
CLEARA
CARRY
BORROW
CU
CD
IQA
IQB
IQC
IQD

74193L0

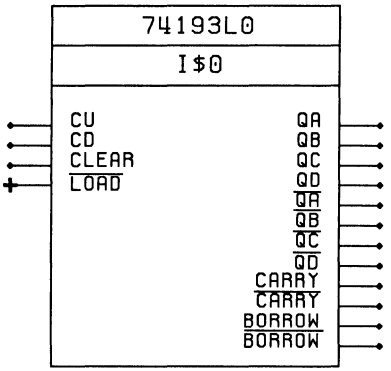
4–Bit Up/Down Binary Counter

Description

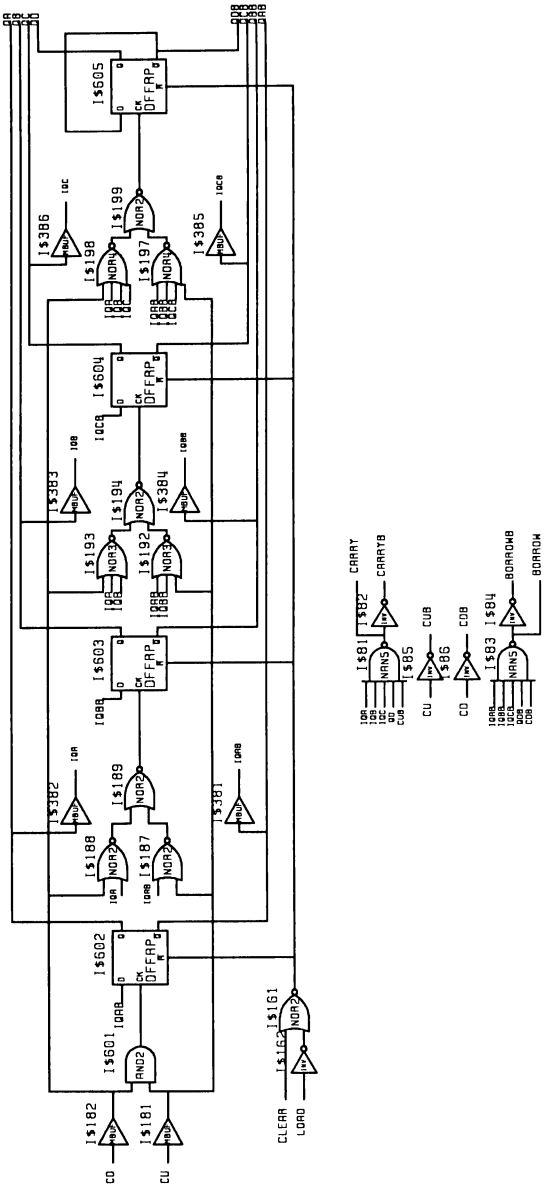
This component is a synchronous, 4–bit, up/down binary counter with dual clocks, and asynchronous clear and load. The active high CLEAR input forces all outputs low. The active low $\overline{\text{LOAD}}$ input presets the outputs low when the $\overline{\text{LOAD}}$ input is driven low. Counting occurs with each rising edge of the count up (CU) or count down (CD) clock. The clock input that is not active must be held high. Both borrow and carry outputs are available to cascade both the up and down counting functions. The complements of the listed outputs are also available.

Name: 74193L0
Gates: 61.8

Symbol



Schematic



SUPERCELLS

74193L0001

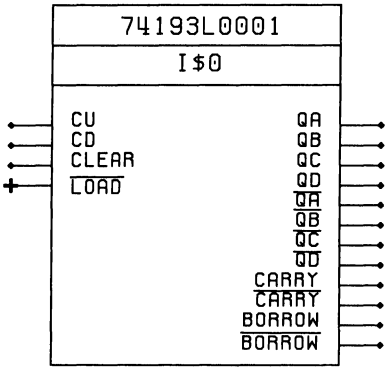
4–Bit Up/Down Binary Counter

Description

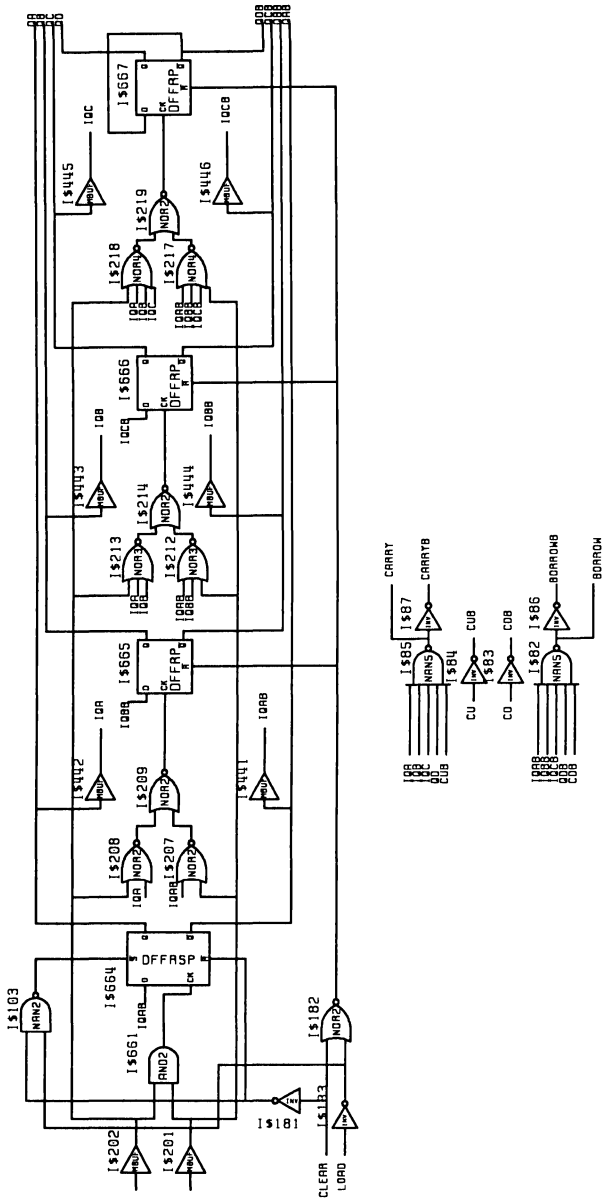
This component is a synchronous, 4–bit, up/down binary counter with dual clocks, and asynchronous clear and load. The active high CLEAR input forces all outputs low. The active low $\overline{\text{LOAD}}$ input presets the outputs to a value of 0001 (e.g. QA = 1) when the $\overline{\text{LOAD}}$ input is driven low. Counting occurs with each rising edge of the count up (CU) or count down (CD) clock. The clock input that is not active must be held high. Both borrow and carry outputs are available to cascade both the up and down counting functions. The complements of the outputs are also available.

Name: 74193L0001
Gates: 65.8

Symbol



Schematic



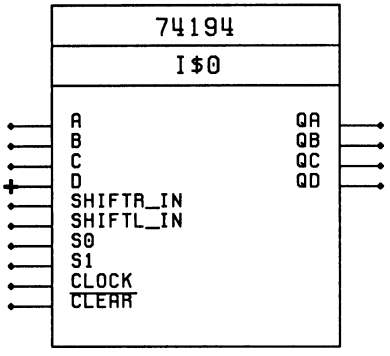
SUPERCELLS

4–Bit Bidirectional Shift Register

Description

This component features parallel inputs and outputs, right–shift and left–shift serial inputs, operating mode control inputs, and a direct clear. Synchronous, parallel loading is performed when both mode control inputs, S0 and S1, are high. The data is loaded into the respective flip–flops on a rising transition of the CLOCK input. Shifting right is accomplished with the rising edge of CLOCK when S0 is high and S1 is low. Serial data is entered on the shift–right (SHIFTR_IN) data input. When S0 is low and S1 is high, data shifts left on the rising edge of CLOCK. When S0 and S1 are both low, clocking is inhibited. The mode controls should only be changed while the clock input is high. The active low CLEAR input forces all outputs low.

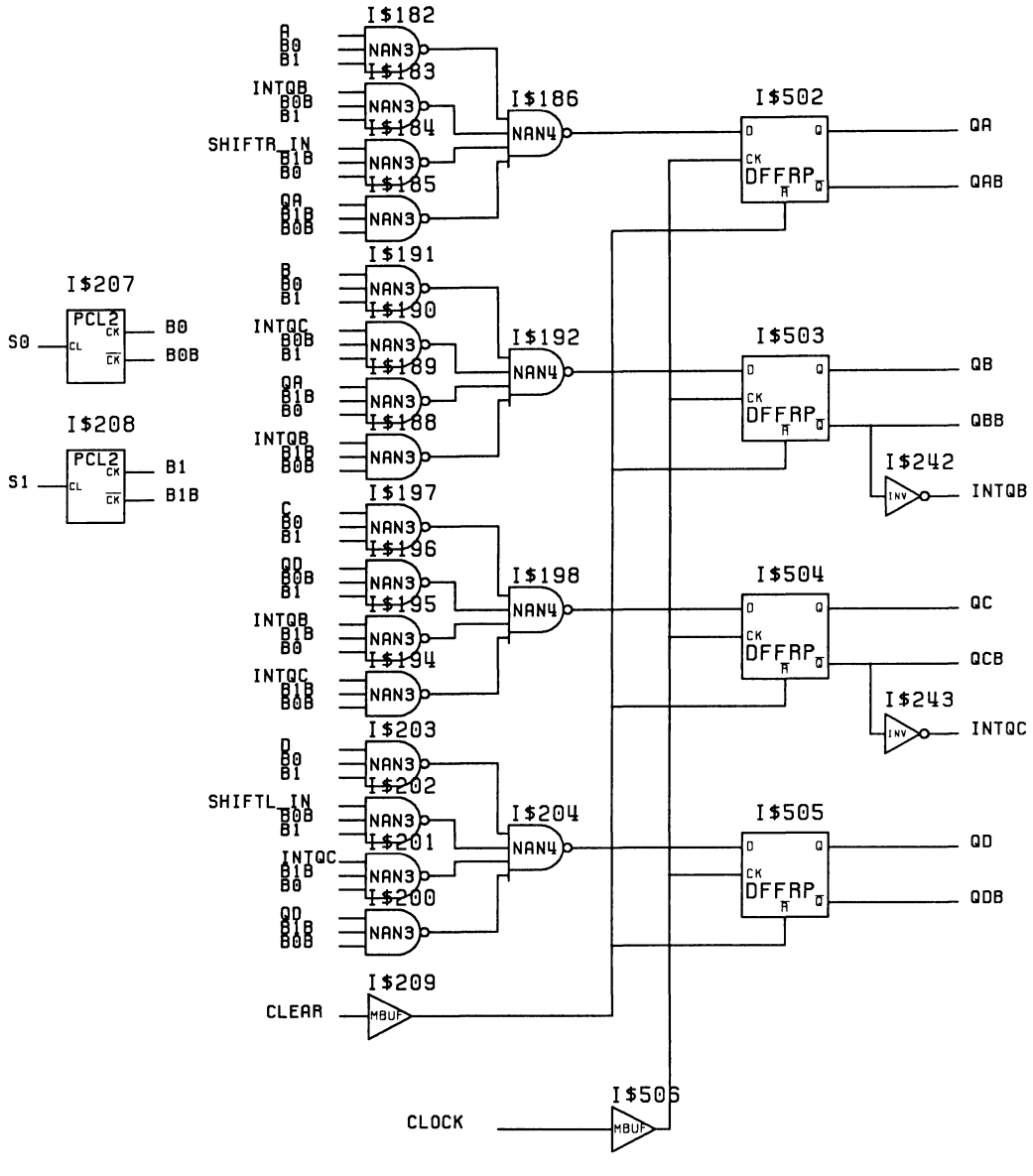
Symbol



Name: 74194
Gates: 70.5

Inputs										Outputs			
CLEARb	Mode		CLOCK	Serial		Parallel				QA	QB	QC	QD
	S1	S0		SHIFTL_IN	SHIFTR_IN	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QA_N	QB_N	QC_N
H	L	H	↑	X	L	X	X	X	X	L	QA_N	QB_N	QC_N
H	H	L	↑	H	X	X	X	X	X	QB_N	QC_N	QD_N	H
H	H	L	↑	L	X	X	X	X	X	QB_N	QC_N	QD_N	L
H	L	L	X	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0

Schematic

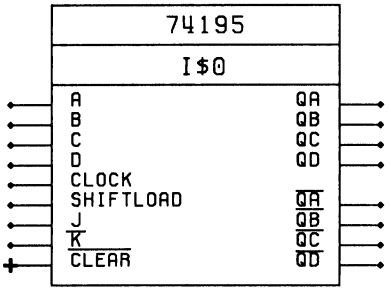

I$182
A
B0
B1
NAN3
I$183
INTQB
B0B
B1
NAN3
I$184
SHIFTR_IN
B1B
B0
NAN3
I$185
QA
B1B
B0B
NAN3
I$186
NAN4
I$502
D
Q
CK
DFFRP
R
Q
QA
QAB
I$207
PCL2
S0
CL
CK
CK
B0
B0B
I$208
PCL2
S1
CL
CK
CK
B1
B1B
I$191
B
B0
B1
NAN3
I$190
INTQC
B0B
B1
NAN3
I$189
QA
B1B
B0
NAN3
I$188
INTQB
B1B
B0B
NAN3
I$192
NAN4
I$503
QB
QBB
I$242
INV
INTQB
I$197
C
B0
B1
NAN3
I$196
QD
B0B
B1
NAN3
I$195
INTQB
B1B
B0
NAN3
I$194
INTQC
B1B
B0B
NAN3
I$198
NAN4
I$504
QC
QCB
I$243
INV
INTQC
I$203
D
B0
B1
NAN3
I$202
SHIFTL_IN
B0B
B1
NAN3
I$201
INTQC
B1B
B0
NAN3
I$200
QD
B1B
B0B
NAN3
I$204
NAN4
I$505
QD
QDB
I$209
CLEAR
MBUF
I$506
CLOCK
MBUF

4–Bit Shift Register

Description

This 4–bit, parallel–access shift register transfers data from QA toward QD on the rising edge of the CLOCK input. During shifting, the serial inputs, J and $\overline{K}$, are the data inputs to the first stage, QA. Synchronous, parallel–in access is available at each stage through individual data inputs that are enabled by taking the SHIFTLOAD input low as the clock input rises. A high on SHIFTLOAD inhibits parallel loading. $\overline{CLEAR}$ is an active low, asynchronous input that sets the parallel outputs low Q(A–D). The Q outputs and their complements are available.

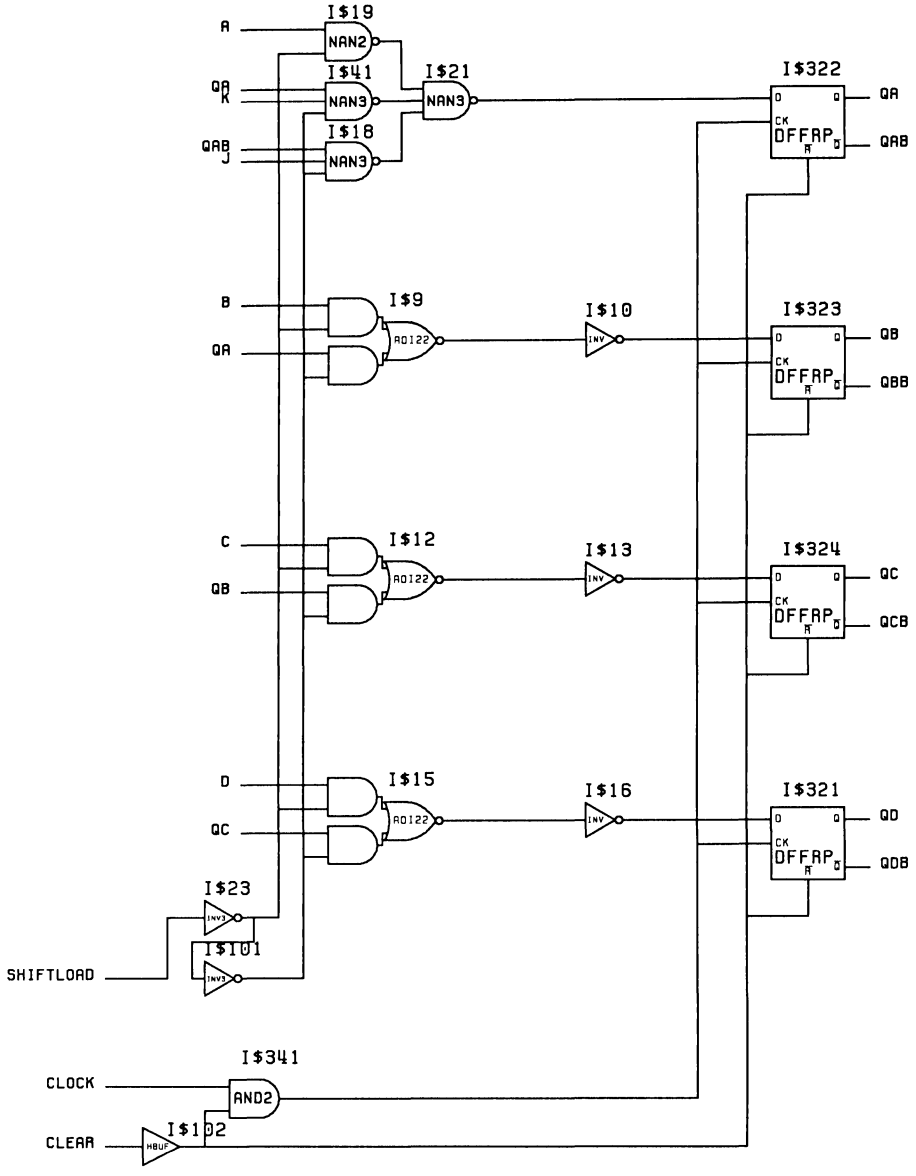
Symbol



Name: 74195
Gates: 48.3

Inputs									Outputs			
CLEAR	SHIFTLOAD	CLOCK	J	$\overline{K}$	A	B	C	D	QA	QB	QC	QD
L	X	X	X	X	X	X	X	X	L	L	L	L
H	L	↑	X	X	a	b	c	d	a	b	c	d
H	H	L	X	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0
H	H	↑	L	H	X	X	X	X	QA_0	QA_0	QB_N	QB_N
H	H	↑	L	L	X	X	X	X	L	QA_N	QB_N	QC_N
H	H	↑	H	H	X	X	X	X	H	QA_N	QB_N	QC_N
H	H	↑	H	L	X	X	X	X	$\overline{QA}_N$	QA_N	QB_N	QC_N

Schematic



SUPERCELLS

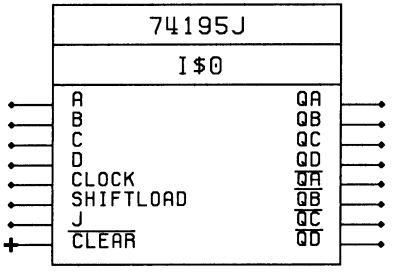
74195J

4–Bit Shift Register

Description

This 4-bit, parallel-access shift register transfers data from QA toward QD on the rising edge of the CLOCK input. During shifting, the serial input, J, is the data input to the first stage, QA. Synchronous, parallel-in access is available at each stage through individual data inputs that are enabled when the SHIFTLOAD input is low, and the CLOCK input rises. A high on SHIFTLOAD inhibits parallel loading. $\overline{\text{CLEAR}}$ is an active low, asynchronous input that sets the parallel outputs low Q(A-D). The Q outputs and their complements are available.

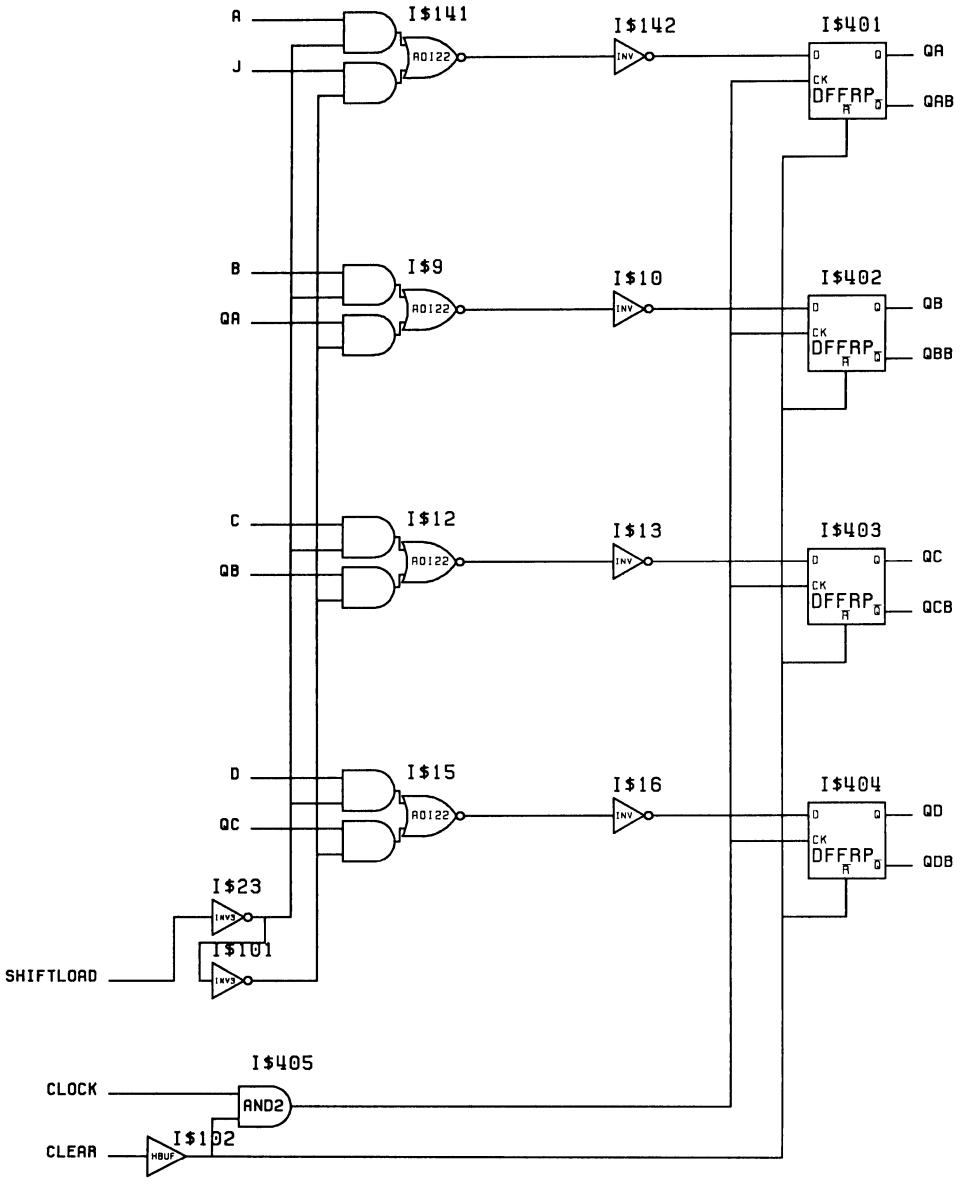
Symbol



Name: 74195J
Gates: 45.8

Inputs								Outputs			
$\overline{\text{CLEAR}}$	SHIFTLOAD	CLOCK	J	A	B	C	D	QA	QB	QC	QD
L	X	X	X	X	X	X	X	L	L	L	L
H	L	↑	X	a	b	c	d	a	b	c	d
H	H	↑	L	X	X	X	X	L	QA_N	QB_N	QC_N
H	H	↑	H	X	X	X	X	H	QA_N	QB_N	QC_N
H	X	L	X	X	X	X	X	QA_0	QB_0	QC_0	QD_0

Schematic



SUPERCELLS

74195S

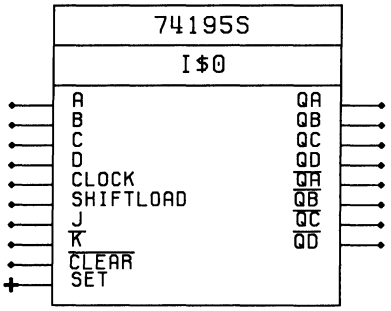
4–Bit Shift Register

Description

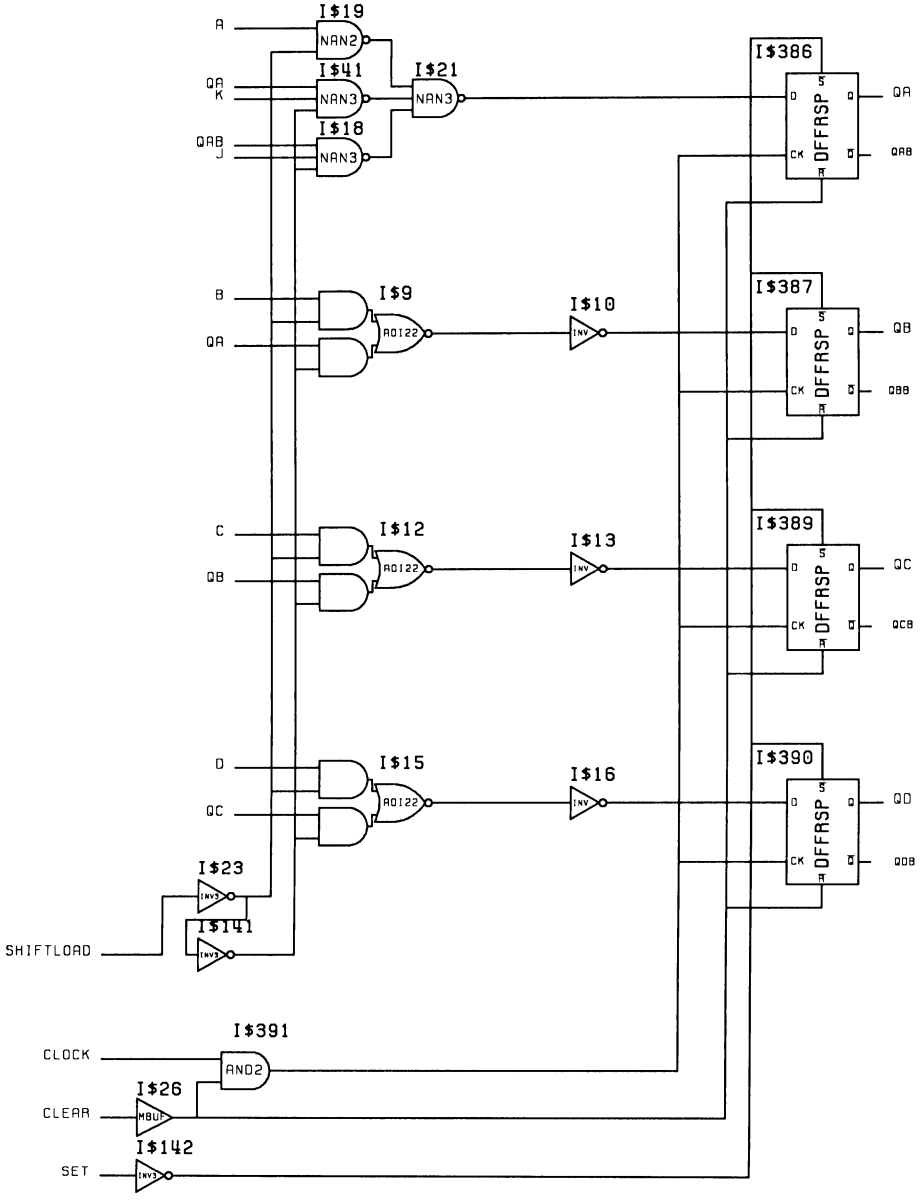
This 4-bit, parallel-access shift register transfers data from QA toward QD on the rising edge of the CLOCK input. During shifting, the serial inputs, J and K, are the data inputs to the first stage, QA. Synchronous, parallel-in access is available at each stage through individual data inputs that are enabled when the SHIFTLOAD input is low, and CLOCK input rises. A high on SHIFTLOAD inhibits parallel loading. When the $\overline{\text{CLEAR}}$ input is taken low, the outputs are asynchronously cleared. This component is the same as the 74195 except that it implements an asynchronous set function determined by the active high SET input. The Q outputs and their complements are available.

Name: 74195S
Gates: 58.8

Symbol



Schematic



SUPERCELLS

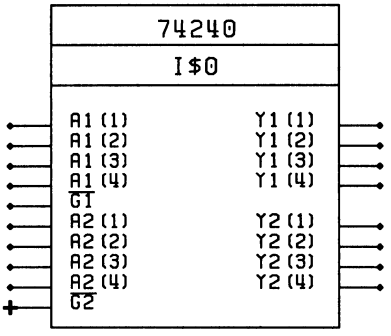
Octal Tristate Buffers

Description

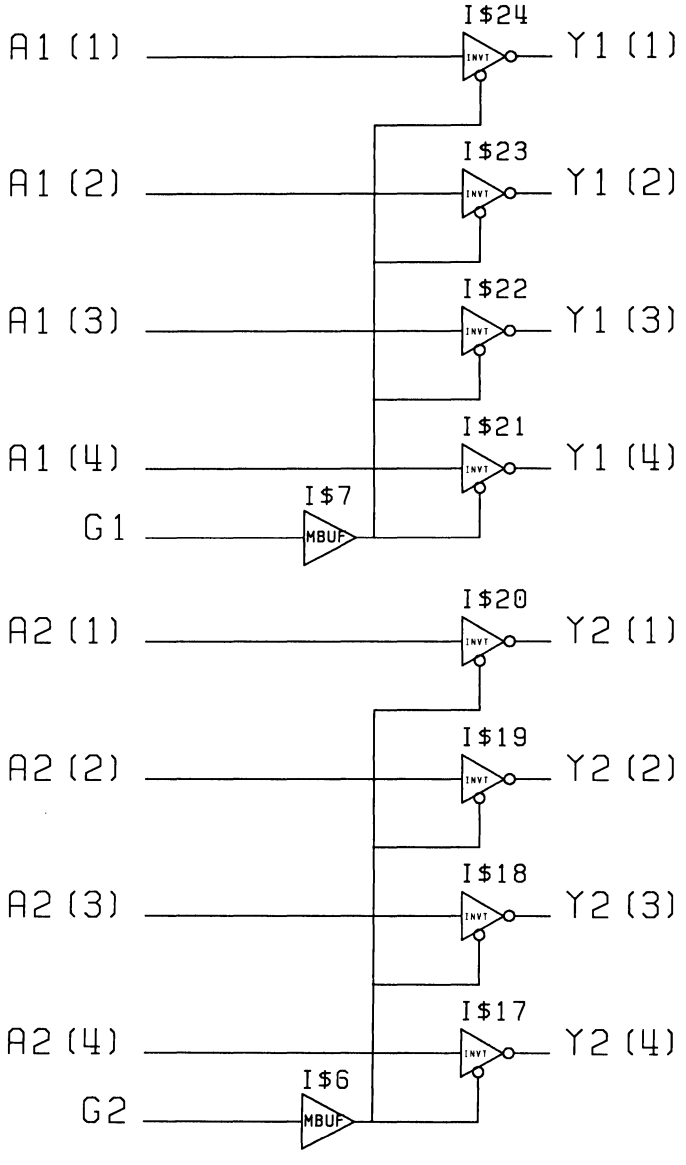
This component contains two 4-bit, inverting, tristate buffers. A separate active low, output-enable control line ($\overline{G1}$ or $\overline{G2}$) exists for each group of four buffers. When the output enables are low, the complement of the input data passes from the A inputs to the Y outputs. When the output enables ($\overline{G1}$ or $\overline{G2}$) are high, the Y outputs are in a high-impedance state. NOTE: Because the output-enable control lines are slower than the data inputs, there is a hold-time requirement on the data inputs.

Name: 74240
Gates: 16.0

Symbol



Schematic


A1 (1)
I$24
INVT
Y1 (1)
A1 (2)
I$23
INVT
Y1 (2)
A1 (3)
I$22
INVT
Y1 (3)
A1 (4)
I$21
INVT
Y1 (4)
I$7
G1
MBUF
A2 (1)
I$20
INVT
Y2 (1)
A2 (2)
I$19
INVT
Y2 (2)
A2 (3)
I$18
INVT
Y2 (3)
A2 (4)
I$17
INVT
Y2 (4)
I$6
G2
MBUF

74244

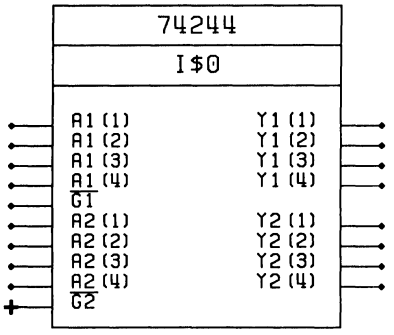
Octal Tristate Buffers

Description

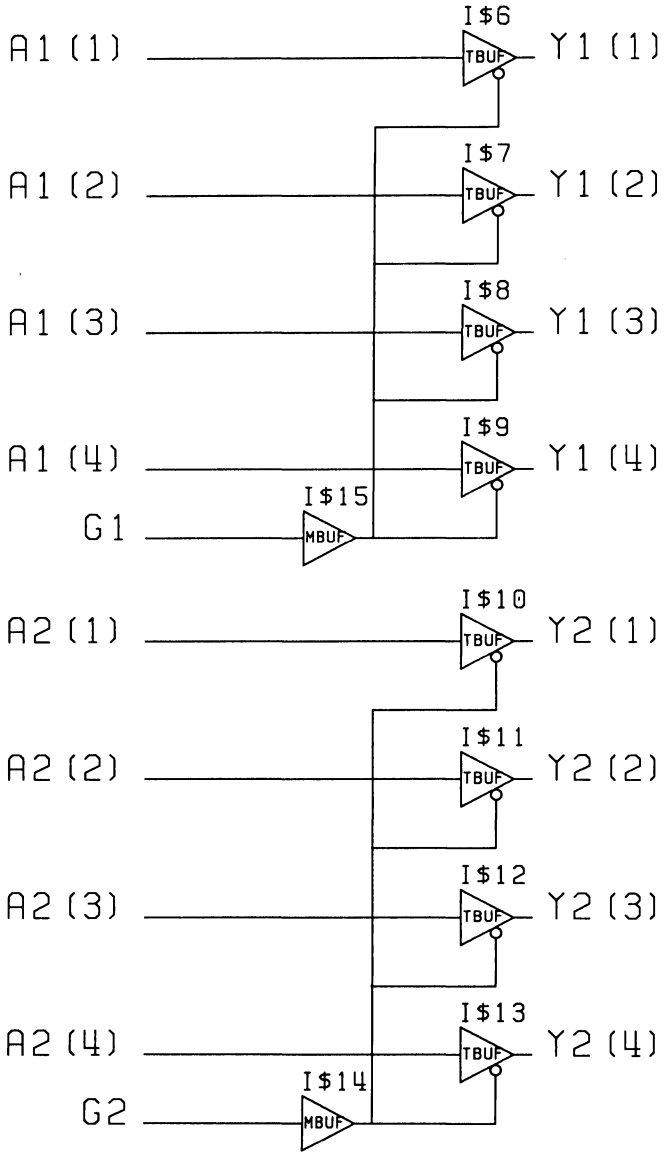
This component contains two 4-bit, non-inverting, tristate buffers. A separate active low output-enable control line ($\overline{G1}$ or $\overline{G2}$) exists for each group of four buffers. When the output enables are low, the input data passes from the A inputs to the Y outputs. When the output enables are high, the Y outputs are in a high-impedance state. NOTE: Because the output-enable control lines are slower than the data inputs, there is a hold-time requirement on data inputs.

Name: 74244
Gates: 28.0

Symbol



Schematic


A1 (1)
A1 (2)
A1 (3)
A1 (4)
G1
A2 (1)
A2 (2)
A2 (3)
A2 (4)
G2
I$6
I$7
I$8
I$9
I$10
I$11
I$12
I$13
I$14
I$15
TBUF
MBUF
Y1 (1)
Y1 (2)
Y1 (3)
Y1 (4)
Y2 (1)
Y2 (2)
Y2 (3)
Y2 (4)

74244NT

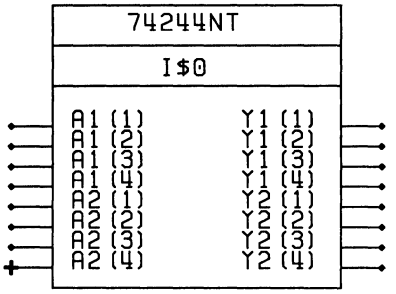
Octal Buffers

Description

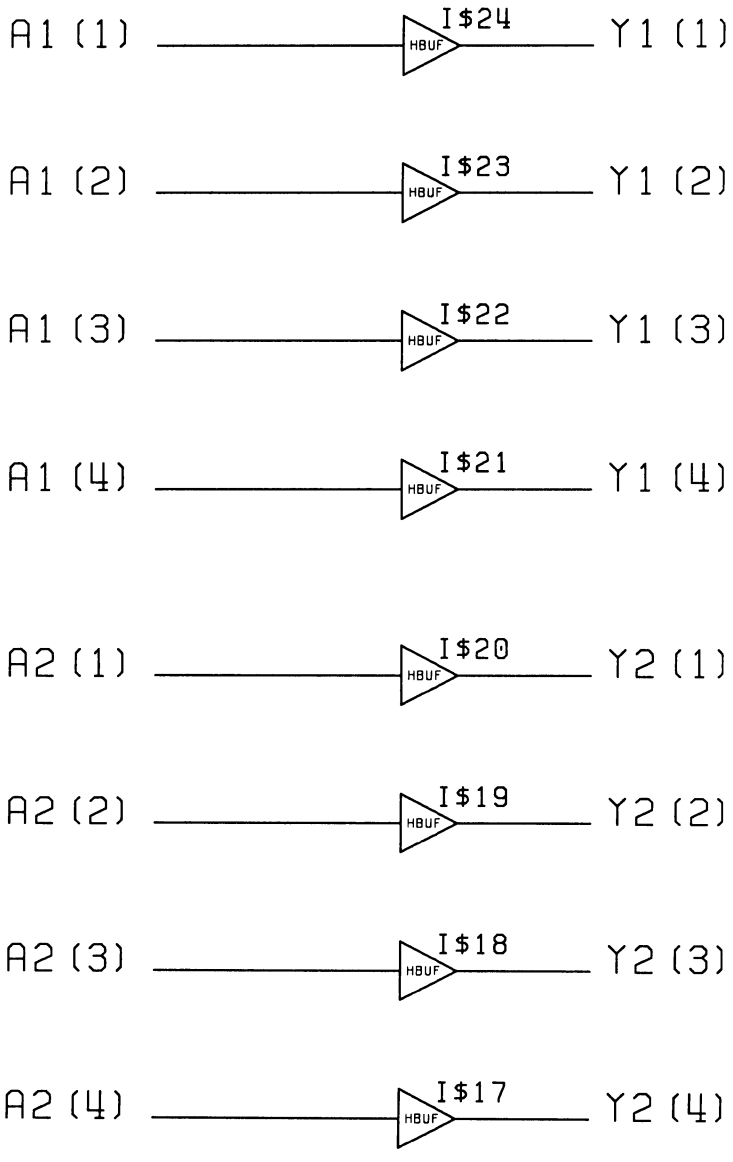
This component contains eight noninverting high-drive buffers. It is similar to the 74244 but has no enable control.

Name: 74244NT
Gates: 12.0

Symbol



Schematic


A1 (1)
I$24
HBUF
Y1 (1)
A1 (2)
I$23
HBUF
Y1 (2)
A1 (3)
I$22
HBUF
Y1 (3)
A1 (4)
I$21
HBUF
Y1 (4)
A2 (1)
I$20
HBUF
Y2 (1)
A2 (2)
I$19
HBUF
Y2 (2)
A2 (3)
I$18
HBUF
Y2 (3)
A2 (4)
I$17
HBUF
Y2 (4)

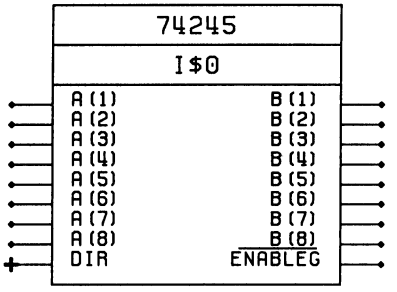
74245

Octal Bus Transceivers

Description

This component allows bi-directional data communication from the A bus to the B bus or from the B bus to the A bus depending on the logic level of the direction control input, DIR. When $\overline{\text{ENABLEG}}$ and DIR are low, data transfers from the B bus to the A bus. When $\overline{\text{ENABLEG}}$ is low and DIR is high, data transfers from the A bus to the B bus. When the input $\overline{\text{ENABLEG}}$ is high, the A and B busses are isolated. NOTE: Because the $\overline{\text{ENABLEG}}$ and DIR control lines are slower than the bus inputs A(n) and B(n), there is a hold-time requirement on the bus inputs.

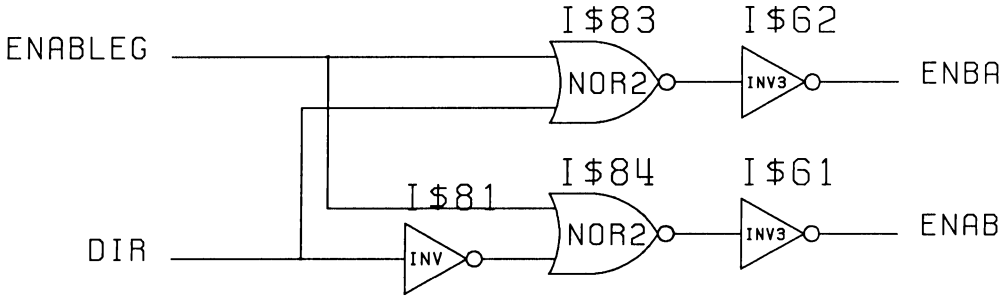
Symbol

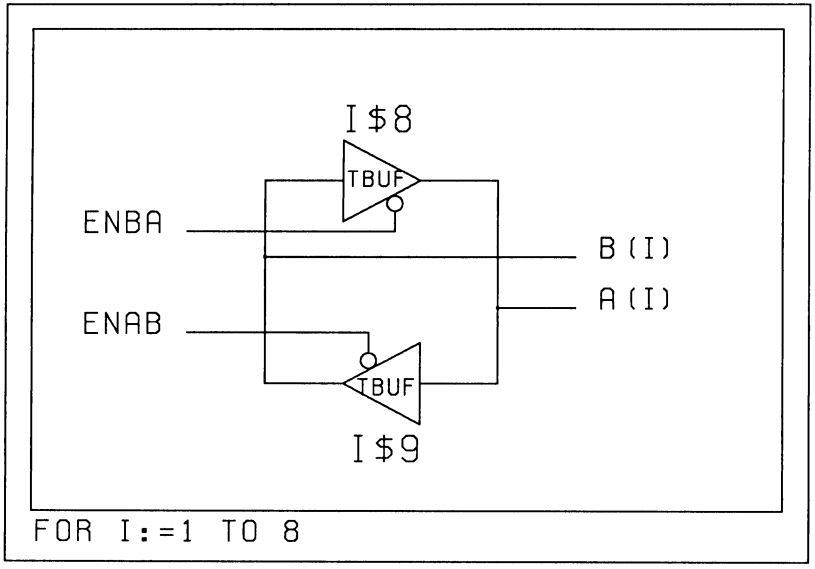


Name: 74245
Gates: 56.5

$\overline{\text{ENABLEG}}$	Direction Control	Operation
	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Schematic


ENABLEG
DIR
I$83
NOR2
I$62
INV3
ENBA
I$81
INV
I$84
NOR2
I$61
INV3
ENAB


I$8
TBUF
ENBA
B(I)
A(I)
ENAB
TBUF
I$9
FOR I:=1 TO 8

74251

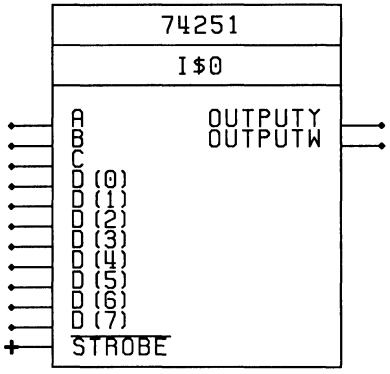
1 of 8 Data Selector/Multiplexer

Description

This component provides a 3-bit binary decoded select (A, B, and C) to multiplex one of eight data inputs. This component also has an active low strobe ($\overline{\text{STROBE}}$) for both the true and inverted values of the selected input. When $\overline{\text{STROBE}}$ is high, the outputs OUTPUTY and OUTPUTW are in the high-impedance state.

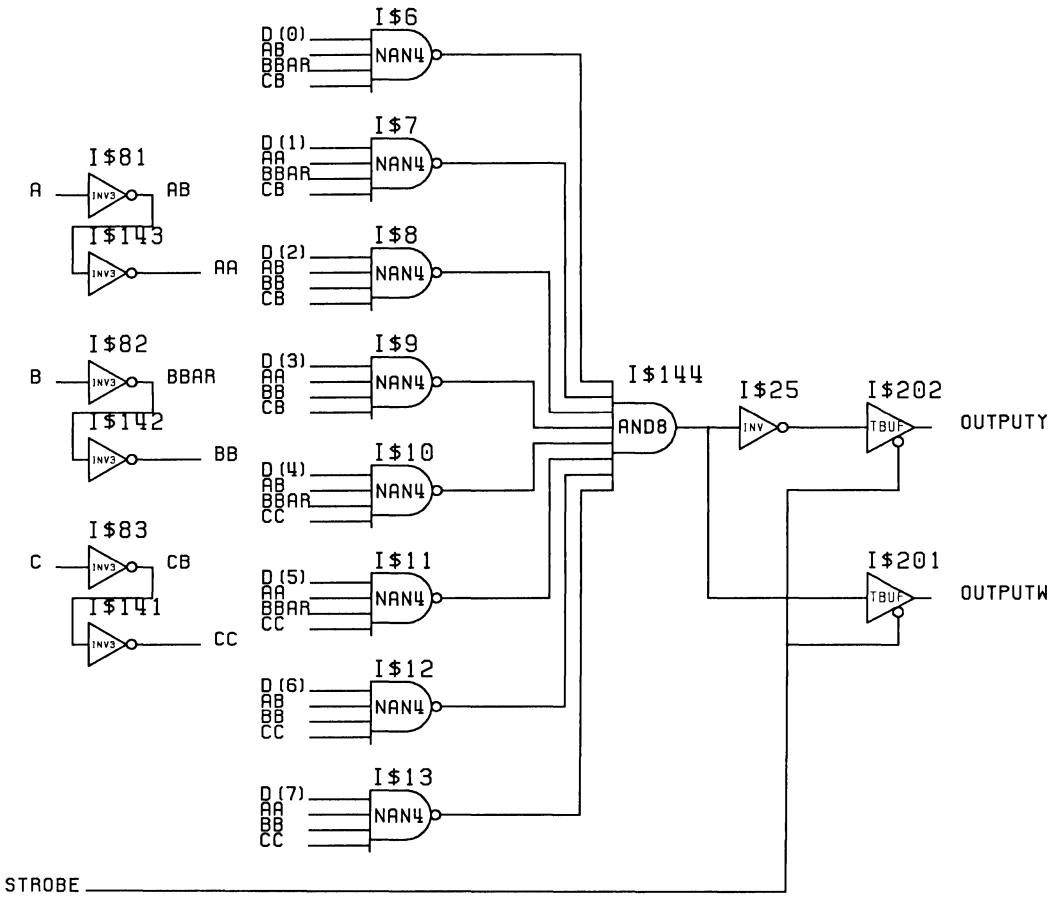
Name: 74251
Gates: 33.3

Symbol



C	B	A	$\overline{\text{WSTROBE}}$	Y	W
X	X	X	H	Z	Z
L	L	L	L	D(0)	D(0)
L	L	H	L	D(1)	D(1)
L	H	L	L	D(2)	D(2)
L	H	H	L	D(3)	D(3)
H	L	L	L	D(4)	D(4)
H	L	H	L	D(5)	D(5)
H	H	L	L	D(6)	D(6)
H	H	H	L	D(7)	D(7)

Schematic



SUPERCELLS

74257

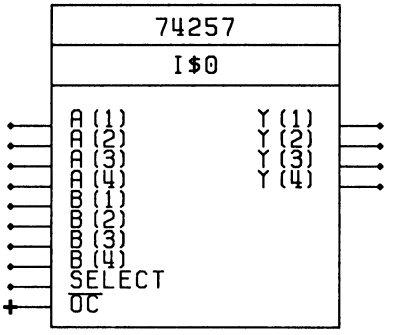
Quad Data Multiplexers

Description

This multiplexes from two 4-bit data sources to four output data lines with tristate outputs. When SELECT is low, A inputs are selected. When SELECT is high, B inputs are selected. The selected data is transferred to the Y outputs in true (noninverted) form. The output enable, $\overline{OC}$, controls the tristate output drivers. When $\overline{OC}$ is low, the outputs are enabled, and when $\overline{OC}$ is high, the outputs are in the high-impedance state.

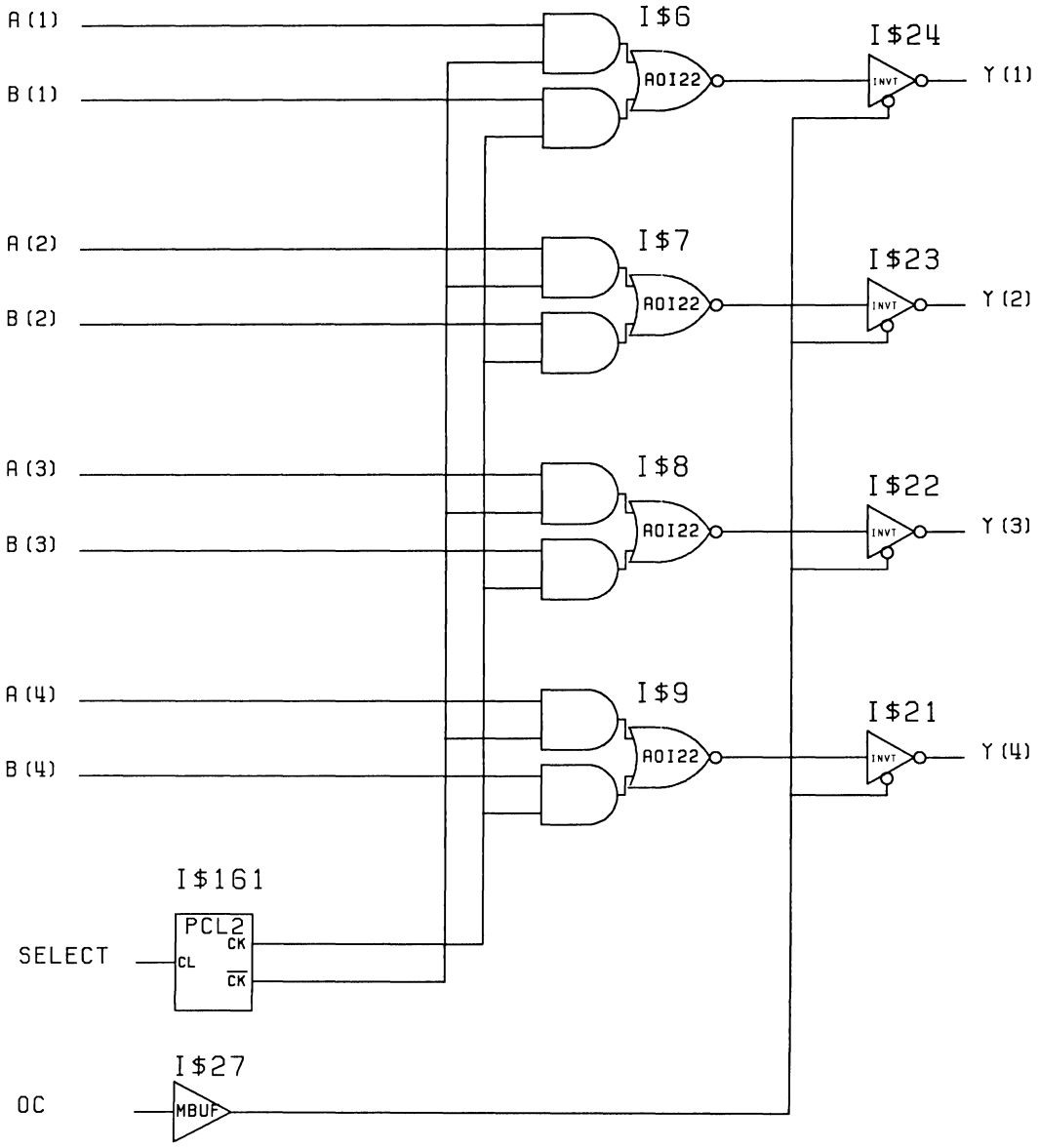
Name: 74257
Gates: 18.8

Symbol



$\overline{OC}$	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Schematic


A (1)
B (1)
A (2)
B (2)
A (3)
B (3)
A (4)
B (4)
SELECT
OC
I$6
I$7
I$8
I$9
I$161
I$27
I$24
I$23
I$22
I$21
AOI22
INVT
MBUF
PCL2
CK
CL
Y (1)
Y (2)
Y (3)
Y (4)

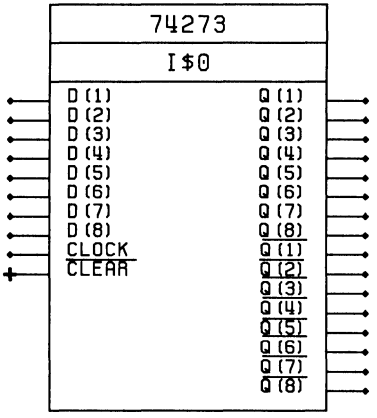
Octal D Flip–Flops

Description

This component is an 8-bit parallel register with a common clock (CLOCK) and a common master reset ($\overline{\text{CLEAR}}$). When $\overline{\text{CLEAR}}$ is low, the Q outputs are low, independent of the other inputs. On the rising edge of CLOCK, data is transferred from the D inputs to the Q outputs. The Q outputs and their complements are available.

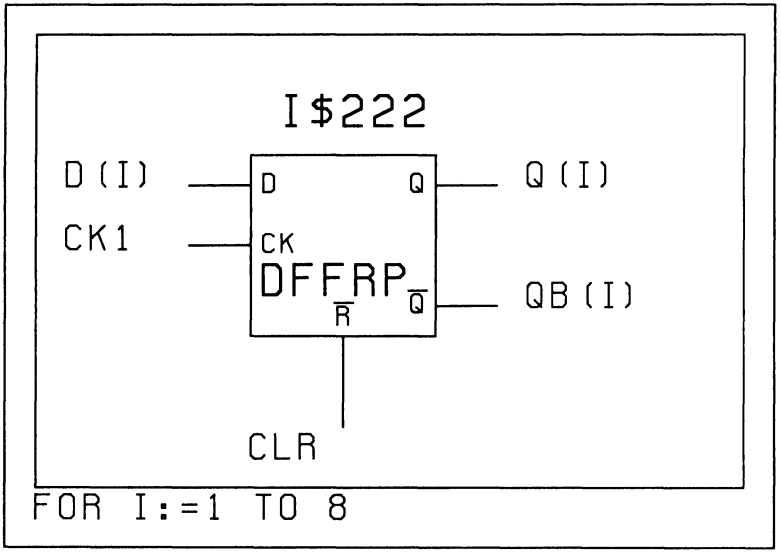
Name: 74273
Gates: 67.0

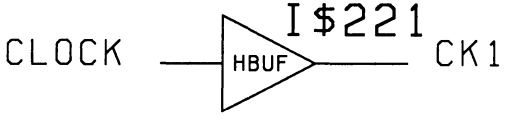
Symbol

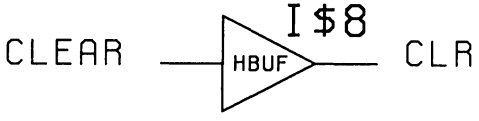


CLEARB	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Schematic


I$222
D(I)
D
Q
Q(I)
CK1
CK
DFFRP
R
Q
QB(I)
CLR
FOR I:=1 TO 8


CLOCK
I$221
HBUF
CK1


CLEAR
I$8
HBUF
CLR

74273NC4

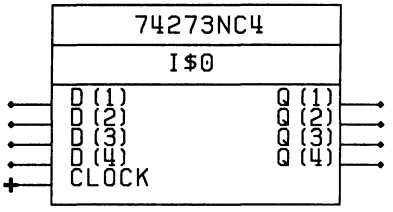
Quad D Flip–Flops

Description

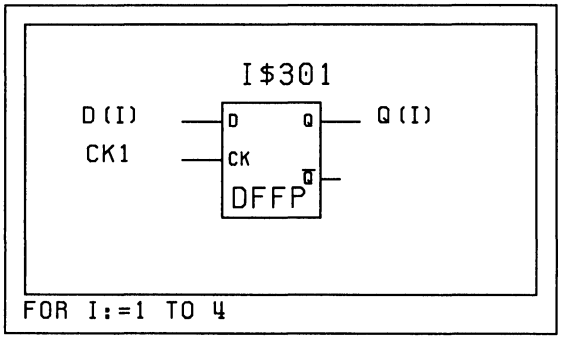
This component is a 4–bit, parallel register with a common clock (CLOCK). On the rising edge of CLOCK, data is transferred from the D inputs to the Q outputs.

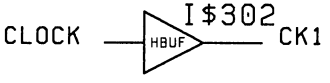
Name: 74273NC4
Gates: 26.5

Symbol



Schematic





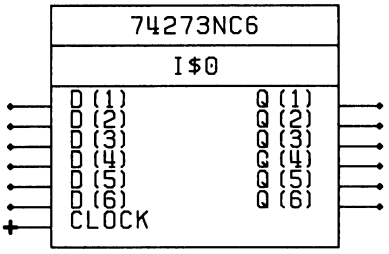
Hex D Flip–Flops

Description

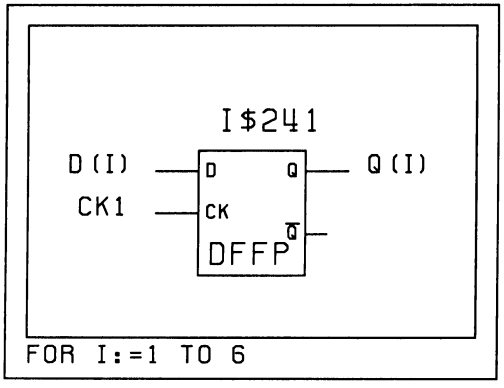
This component is a 6–bit, parallel register with a common clock (CLOCK). On the rising edge of CLOCK, data is transferred from the D inputs to the Q outputs.

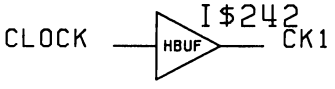
Name: 74273NC6
Gates: 39.0

Symbol



Schematic





SUPERCELLS

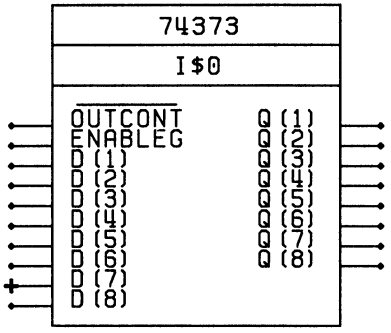
74373

Octal D–Type Latches

Description

This component contains eight D–type latches with individual D–type inputs and tristate true outputs. When the ENABLEG input is high, the latches are transparent, i.e., the latch Q outputs reflect the D inputs. On the falling edge of ENABLEG, the latches store the state of the D inputs. When the tristate output enable control line (OUTCONT) is high, the outputs are in the high–impedance state. When OUTCONT is low, the value of the latch outputs is transferred to the Q outputs. Schmitt–trigger buffering of ENABLEG input is not implemented.

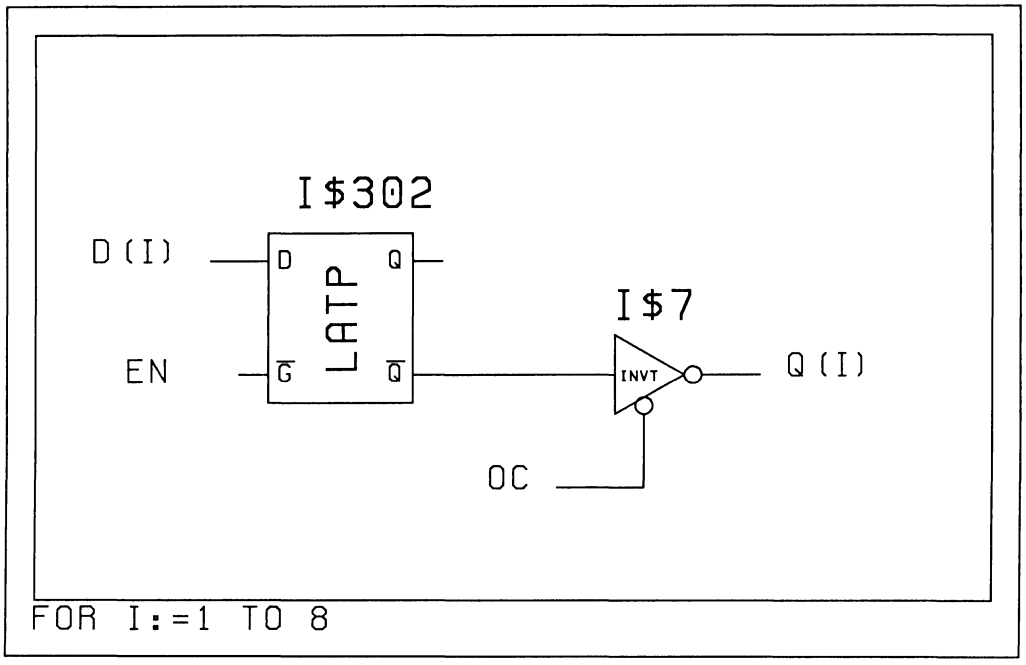
Symbol

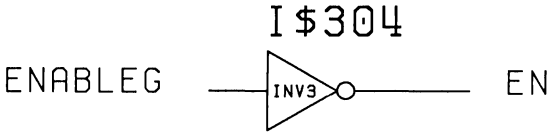


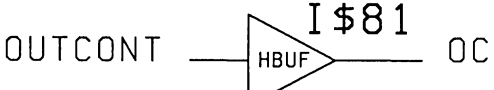
Name: 74373
Gates: 52.5

Input			Output
$\overline{\text{OUTCONT}}$	ENABLEG	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Schematic


I$302
D(I)
D
Q
LATP
EN
G
Q
I$7
INVT
Q(I)
OC
FOR I:=1 TO 8


I$304
ENABLEG
INV3
EN


I$81
OUTCONT
HBUF
OC

74374

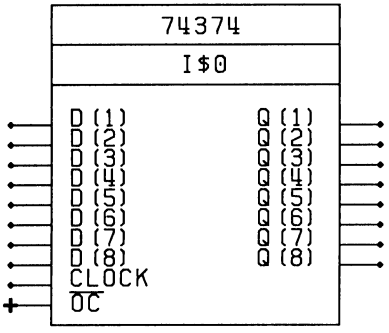
Octal D–Type Flip–Flops

Description

This component contains eight positive edge–triggered flip–flops with individual D–type inputs and tristate true outputs. Each flip–flop will store the state of the corresponding D input on the rising edge of the CLOCK input. When the asynchronous $\overline{OC}$ enable input is high, the Q outputs go to a high–impedance state. When $\overline{OC}$ is low, the contents of the flip–flops are available at the Q outputs. Schmitt–trigger buffering of CLOCK input is not implemented.

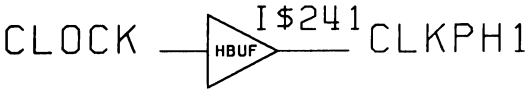
Name: 74374
Gates: 79.0

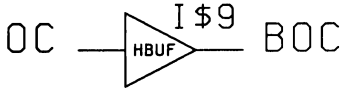
Symbol

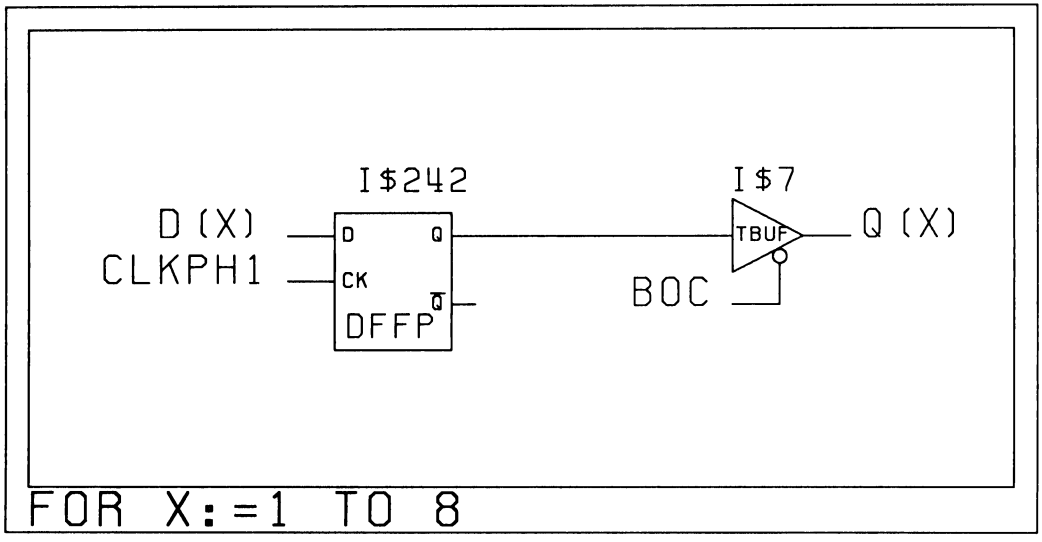


$\overline{OC}$	CLOCK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Schematic


CLOCK
I$241
HBUF
CLKPH1


OC
I$9
HBUF
BOC


I$242
I$7
D(X)
CLKPH1
D
Q
CK
DFFP
TBUF
Q(X)
BOC
FOR X:=1 TO 8

74374NT

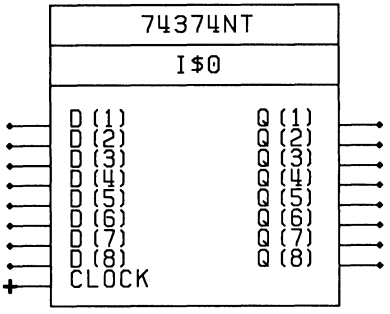
Octal D–Type Flip–Flops

Description

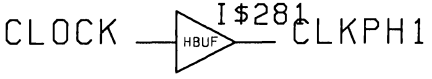
This component is the same as the 74374 except that it does not have the tristate outputs. This component contains eight positive edge–triggered flip–flops with individual D–type inputs. Each flip–flop will store the state of the corresponding D input on the rising edge of the CLOCK input. The stored data of the flip–flop is available on the Q outputs.

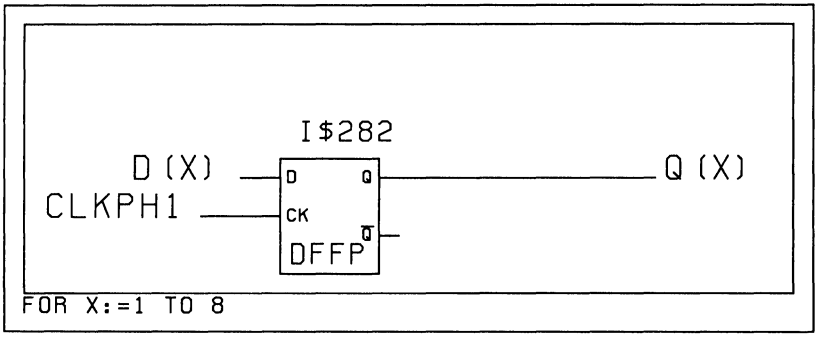
Name: 74374NT
Gates: 51.5

Symbol



Schematic





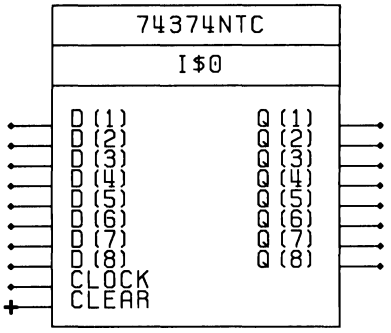
Octal D–Type Flip–Flops

Description

This component is the same as the 74374 except that it does not have the tristate outputs, and it contains a common clear input. This component contains eight positive edge–triggered flip–flops with individual D–type inputs and a common clear input (CLEAR). When CLEAR is low, each flip–flop will store the state of the corresponding D input on the rising edge of CLOCK. When CLEAR is high, all Q outputs will be low. The stored data of the flip–flop is available on the Q outputs.

Name: 74374NTC
Gates: 66.5

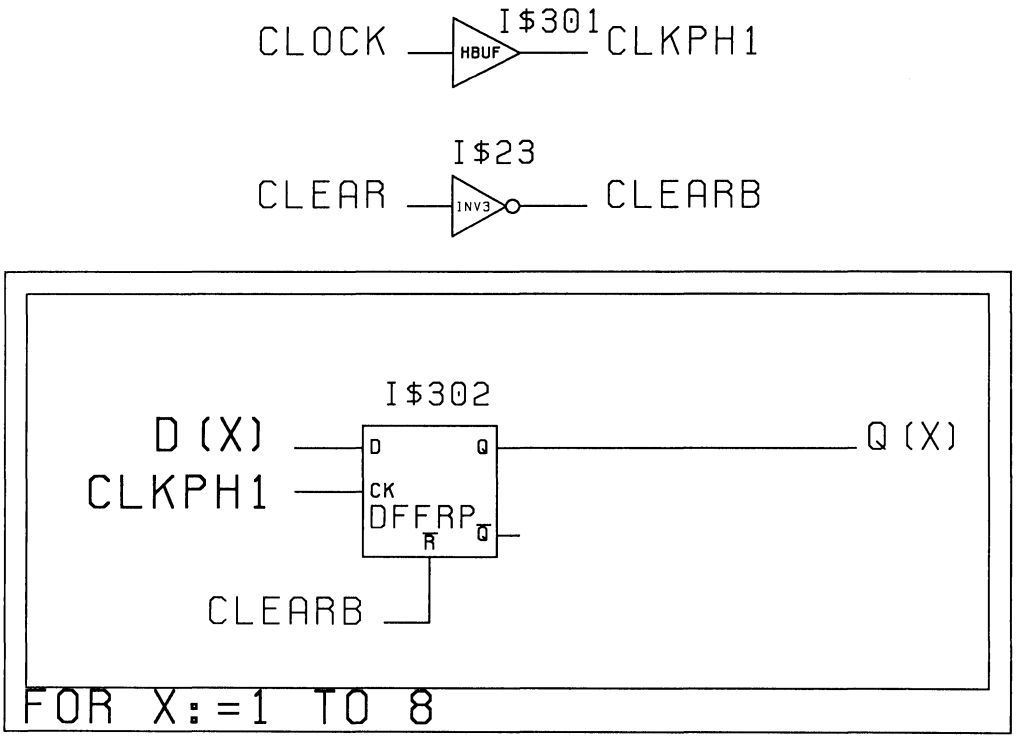
Symbol



SUPERCELLS

74374NTC

Schematic



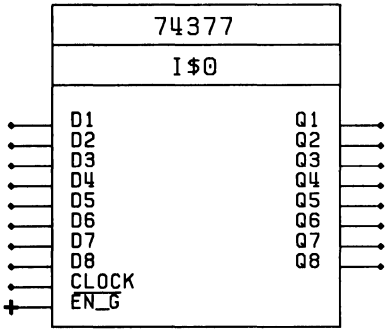
Octal D–Type Flip–Flops

Description

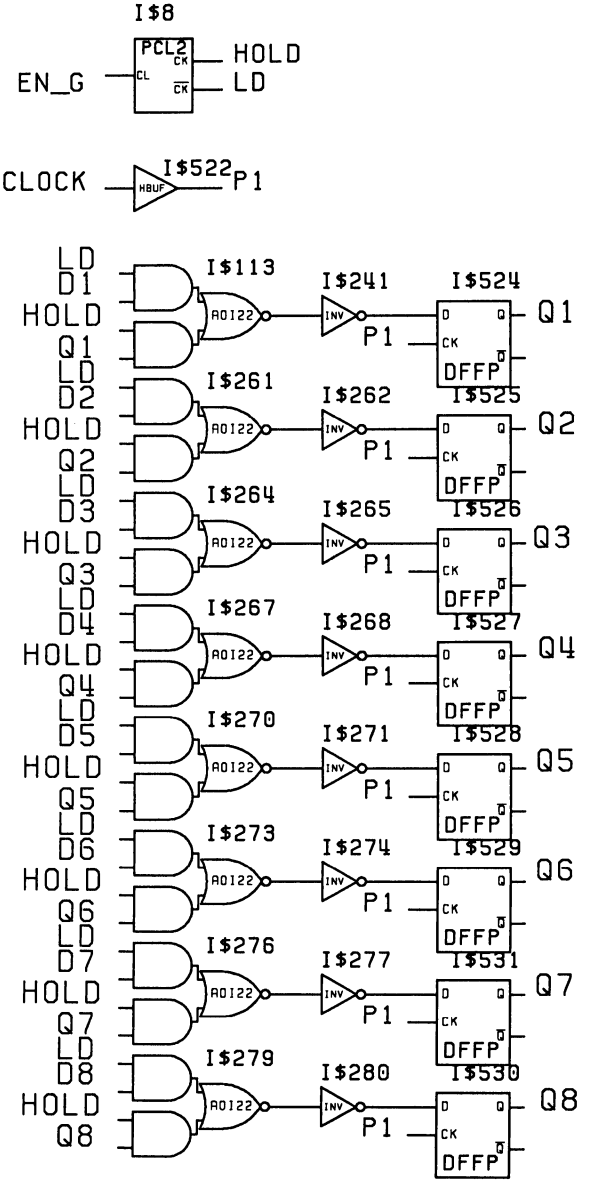
This positive edge–triggered component is similar to a 74273 and includes a common enable. When enable ($\overline{EN\_G}$) is low, the data on the D inputs is transferred to the Q outputs on the positive going edge of the CLOCK input.

Name: 74377
Gates: 73.3

Symbol



Schematic


I$8
PCL2
CK
CL
CK
EN_G
HOLD
LD
CLOCK
I$522
HBUF
P1
LD
D1
HOLD
Q1
I$113
AOI22
I$241
INV
P1
I$524
D
Q
CK
DFFP
Q1
LD
D2
HOLD
Q2
I$261
AOI22
I$262
INV
P1
I$525
Q2
LD
D3
HOLD
Q3
I$264
AOI22
I$265
INV
P1
I$526
Q3
LD
D4
HOLD
Q4
I$267
AOI22
I$268
INV
P1
I$527
Q4
LD
D5
HOLD
Q5
I$270
AOI22
I$271
INV
P1
I$528
Q5
LD
D6
HOLD
Q6
I$273
AOI22
I$274
INV
P1
I$529
Q6
LD
D7
HOLD
Q7
I$276
AOI22
I$277
INV
P1
I$531
Q7
LD
D8
HOLD
Q8
I$279
AOI22
I$280
INV
P1
I$530
Q8

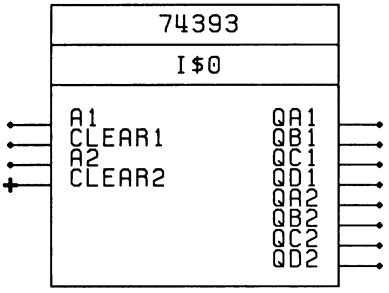
Dual 4–Bit Binary Counter

Description

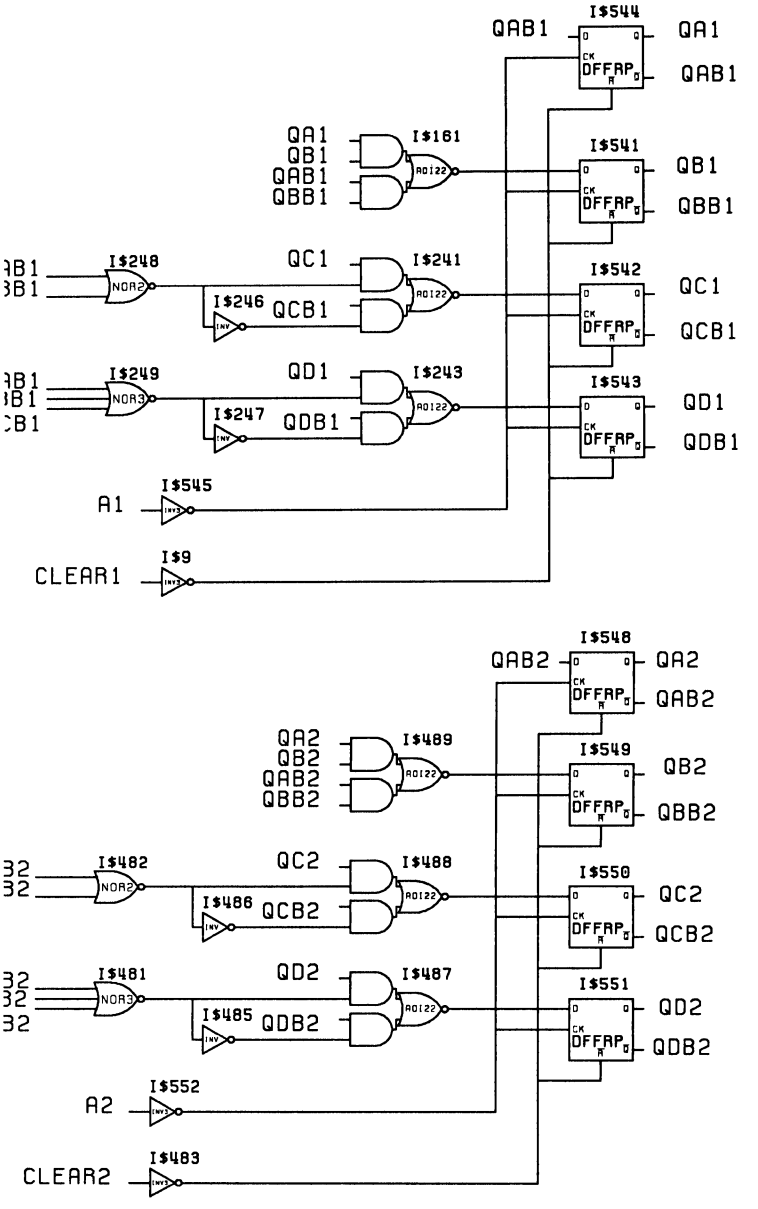
This component contains two independent, 4–bit, binary counters that each have a clear and a clock input. When CLEAR(n) is high, the Q(n) outputs are set to a low logic level. Counting occurs on the negative going edge of toggle input A(n).

Name: 74393
Gates: 85.5

Symbol



Schematic


I$544
QAB1
QA1
QAB1
I$161
QA1
QB1
QAB1
QBB1
I$541
QB1
QBB1
I$248
QC1
I$241
I$542
QC1
QCB1
I$246
QCB1
I$249
QD1
I$243
I$543
QD1
QDB1
I$247
QDB1
I$545
A1
I$9
CLEAR1
I$548
QAB2
QA2
QAB2
I$489
QA2
QB2
QAB2
QBB2
I$549
QB2
QBB2
I$482
QC2
I$488
I$550
QC2
QCB2
I$486
QCB2
I$481
QD2
I$487
I$551
QD2
QDB2
I$485
QDB2
I$552
A2
I$483
CLEAR2

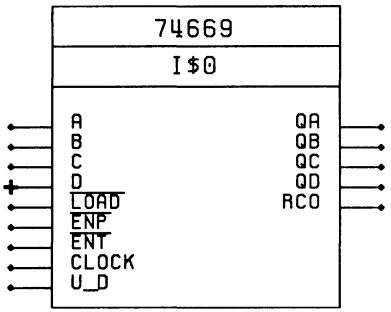
4–Bit Up/Down Binary Counter

Description

This component is a positive edge-triggered, synchronous, 4-bit, up/down binary counter with a synchronous parallel load. The active low $\overline{\text{LOAD}}$ input presets the outputs to the logic levels present on the data inputs at the rising edge of the next clock. Counting occurs synchronously on the positive clock edge when the enable inputs ($\overline{\text{ENP}}$ and $\overline{\text{ENT}}$) are both low. The direction of the count is determined by U_D; counting up when U_D is high, counting down when U_D is low. The look-ahead carry circuitry provides for cascading counters to n-bits without any additional circuitry. The active low carry (RCO) is enabled when the up count is a maximum (i.e. 15) or the down count is a minimum (i.e. 0) and may be used to enable successive stages. Transitions at the control inputs ($\overline{\text{ENP}}$, $\overline{\text{ENT}}$, $\overline{\text{LOAD}}$, U_D) that modify the operation mode have no effect until clocking occurs.

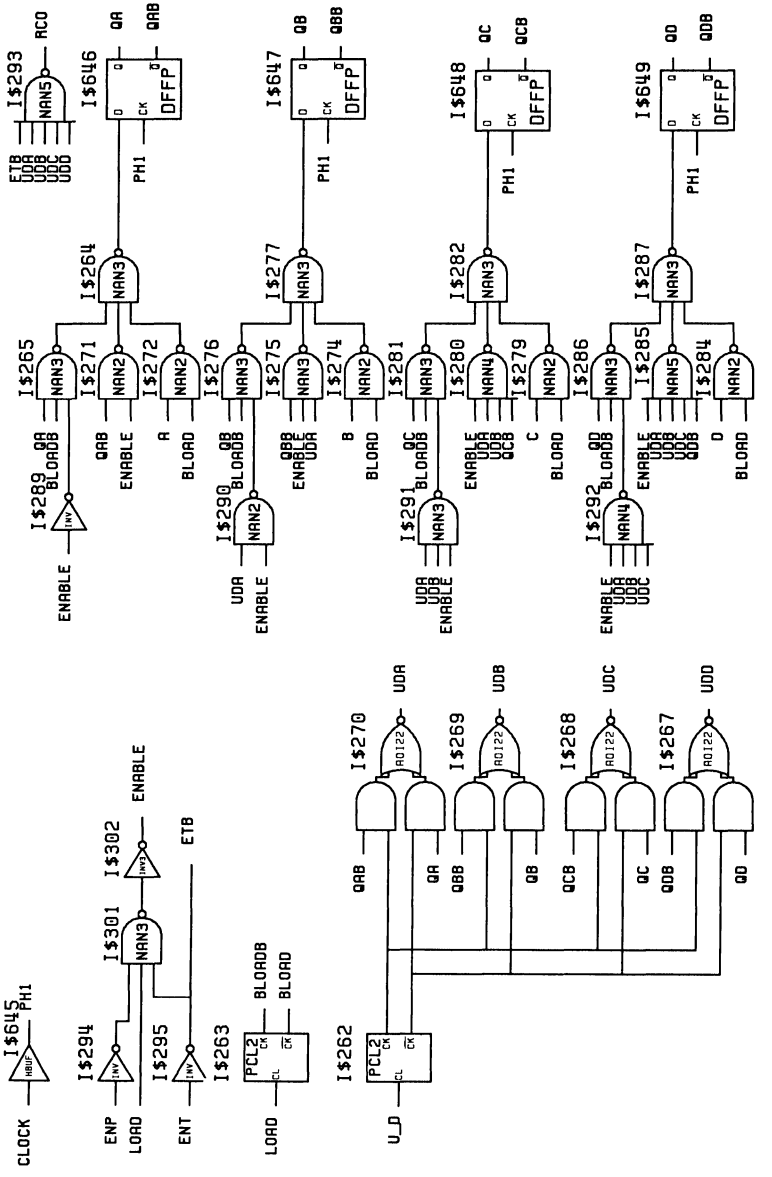
Name: 74669
Gates: 72.3

Symbol



SUPERCELLS

Schematic


I$293
NAN5
RCO
ETB
UDA
UDB
UDC
UDD
I$646
DFFP
QA
QAB
PH1
I$264
NAN3
I$265
NAN3
QA
BLOADB
ENABLE
I$271
NAN2
QAB
ENABLE
I$272
NAN2
A
BLOAD
I$289
INV
ENABLE
I$647
DFFP
QB
QBB
PH1
I$277
NAN3
I$276
NAN3
QB
BLOADB
ENABLE
I$275
NAN3
QBB
ENABLE
UDA
I$274
NAN2
B
BLOAD
I$290
NAN2
UDA
ENABLE
I$648
DFFP
QC
QCB
PH1
I$282
NAN3
I$281
NAN3
QC
BLOADB
ENABLE
I$280
NAN4
UDA
UDB
UDC
QCB
I$279
NAN2
C
BLOAD
I$291
NAN3
UDA
UDB
ENABLE
I$649
DFFP
QD
QDB
PH1
I$287
NAN3
I$286
NAN3
QD
BLOADB
ENABLE
I$285
NAN5
UDA
UDB
UDC
QDB
I$284
NAN2
D
BLOAD
I$292
NAN4
ENABLE
UDA
UDB
UDC
I$270
AOI22
UDA
QAB
QA
I$269
AOI22
UDB
QBB
QB
I$268
AOI22
UDC
QCB
QC
I$267
AOI22
UDD
QDB
QD
I$645
HBUF
PH1
CLOCK
I$294
INV
ENP
LOAD
I$301
NAN3
I$302
ENABLE
I$295
INV
ENT
ETB
I$263
PCL2
CK
CL
BLOADB
BLOAD
LOAD
I$262
PCL2
CK
CL
U_D

NCR Application Notes

Cells

Handling and Storage

Packaging

Power

Rules

Specifications

Testing

Timing

Cell Technology Matrix

Digital Cells

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
ADD4	•	•			Adder, 4-bit
ADD4CS	•	•			Adder, 4-bit
ADFUL	•	•	•	•	Adder, full adder
AND2	•	•	•	•	AND, 2-input
AND3	•	•	•	•	AND, 3-input
AND4	•	•	•	•	AND, 4-input
AND8	•	•	•	•	AND, 8-input
AOI211	•	•	•	•	AND-OR-INVERT, 2-1-1 input
AOI22	•	•	•	•	AND-OR-INVERT, 2-2 input
AOI22C	•	•	•	•	AND-OR-INVERT, 2-2 input, complementary outputs
AOI22CH	•	•	•	•	AND-OR-INVERT, 2-2 input, complementary outputs, high drive
AOI31	•	•	•	•	AND-OR-INVERT, 3-1 input
AOI333C	•	•	•	•	AND-OR-INVERT, 3-3-3 input, complementary outputs
AOI44C	•	•	•	•	AND-OR-INVERT, 4-4 input, complementary outputs
BUF8	•	•	•	•	Buffer, 8x drive
CCND	•	•	•	•	Cross coupled NAND latch
CCNDG	•	•	•	•	Cross coupled NAND latch, gated
CCNR	•	•	•	•	Cross coupled NOR latch
DEC10F4	•	•	•	•	Decoder, 1 of 4
DEC1OF8	•	•	•	•	Decoder, 1 of 8
DFFP	•	•	•	•	D FF, 1 phase clock, positive edge
DFFPF	•	•			D FF, 1 phase clock, positive edge, fast
DFFPQ	•	•			D FF, 1 phase clock, positive edge
DFFRMP	•	•			D FF, 1 phase clock, positive edge, reset, multiplexed data
DFFRP	•	•	•	•	D FF, 1 phase clock, positive edge, reset
DFFRPF	•	•			D FF, 1 phase clock, positive edge, reset, fast
DFFRPP	•	•			D FF, 1 phase clock, positive edge, reset, parallel load
DFFRPQ	•	•			D FF, 1 phase clock, positive edge, reset
DFFRPQT	•	•			D FF, 1 phase clock, positive edge, reset, tristate output
DFFRPZ	•				D FF, 1 phase clock, positive edge, reset, hi z output
DFFRSP	•	•	•	•	D FF, 1 phase clock, positive edge, reset, set

Digital cells (Sheet 1 of 6)

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
DFFRSPF	•	•	•	•	D FF, 1 phase clock, positive edge, reset, set fast
DFFRSPH	•	•	•	•	D FF, 1 phase clock, positive edge, resetb, setb, high drive
DLYCEL	•	•	•	•	Delay cell
DS1216	•	•			Schmitt trigger, 1.2/1.6
DS1218	•	•	•	•	Schmitt trigger, 1.2/1.8
DS1238	•	•			Schmitt trigger, 1.2/3.8
DS1323	•	•			Schmitt trigger, 1.3/2.3
DS1527	•	•			Schmitt trigger, 1.5/2.7
DS1728	•	•			Schmitt trigger, 1.7/2.8
DS2028	•	•			Schmitt trigger, 2.0/2/8
DS2232	•	•			Schmitt trigger, 2.2/3.2
EXNOR	•	•	•	•	Exclusive NOR
EXNORS		•			Exclusive NOR
EXOR	•	•	•	•	Exclusive OR
EXOR3	•	•	•	•	Exclusive OR, triple drive
EXORH	•	•	•	•	Exclusive OR, high drive
EXORS		•			Exclusive OR
HBUF	•	•	•	•	Buffer, 4x drive
INBUF	•	•	•	•	Input buffer, TTL input
INPD	•	•	•	•	Input pad (used with INBUF or DSnnnn)
INV	•	•	•	•	Inverter
INV2	•				Inverter, 2x drive
INV3	•	•	•	•	Inverter, 3x drive
INV8	•	•	•	•	Inverter, 8x drive
INVH	•	•	•	•	Inverter, high drive
INVT	•	•	•	•	Inverter, tristate output
INVT3	•	•	•	•	Inverter, 3x drive, tristate output
INVTH	•	•	•	•	Inverter, high drive, tristate output
INVTS		•			Inverter, tristate output
IOBUF	•	•	•	•	Bidirectional I/O pad driver
IOBUF8	•	•	•	•	Bidirectional I/O pad driver, 8x drive
IOBUFM	•	•	•	•	Bidirectional I/O pad driver
IOBUFS	•	•			Bidirectional I/O pad driver
IONPD48	•	•	•	•	I/O pad, 48 mA drive, 7V open drain
IOPD2	•	•	•	•	I/O pad, 2 mA drive
IOPD4	•	•	•	•	I/O pad, 4 mA drive

Digital cells (Sheet 2 of 6)

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
IOPD8	•	•	•	•	I/O pad, 8 mA drive
IOPD16	•	•	•	•	I/O pad, 16 mA drive
IOPD24	•	•	•	•	I/O pad, 24 mA drive
IOPPD2	•	•	•	•	I/O pad, 2 mA drive, pullup/pulldown
IOPPD4	•	•	•	•	I/O pad, 4 mA drive, pullup/pulldown
IOPPD8	•	•	•	•	I/O pad, 8 mA drive, pullup/pulldown
IOPPD16	•	•	•	•	I/O pad, 16 mA drive, pullup/pulldown
IOPPD24	•	•	•	•	I/O pad, 24 mA drive, pullup/pulldown
IPPD	•	•	•	•	Input pad, pullup/pulldown
JKFFRP	•	•			JK FF, positive edge, reset
JKFFRSN	•	•			JK FF, negative edge, 1 phase clock
JKFFRSNF	•	•			JK FF, negative edge, 1 phase clock
JKFFRSP	•	•	•	•	JK FF, positive edge, 1 phase clock, reset, set
JKFFRSPF	•	•			JK FF, positive edge, 1 phase clock, reset, set, fast
LATP	•	•	•	•	Latch, high level active
LATPF	•	•			Latch, high level active, fast
LATPQ	•	•			Latch, positive edge
LATPQT	•	•			Latch, positive edge, tristate output
LATRP	•	•	•	•	Latch, high level active, reset
LATRPF	•	•	•	•	Latch, high level active, reset, fast
LATRPH	•	•	•	•	Latch, high level active, reset, high drive
LATRPQ	•	•			Latch, positive edge, reset
LATRPQT	•	•			Latch, positive edge, reset, tristate output
LATRTP	•	•			Latch, positive edge, reset, tristate output
MBUF	•	•	•	•	Buffer, medium drive
MUX2	•	•	•	•	Multiplexer, 2 to 1 single enable
MUX2H	•	•	•	•	Multiplexer, 2 to 1, single enable, high drive
MUX2TO1	•	•	•	•	Multiplexer, 2 to 1, dual enables
MUX4C	•	•	•	•	Multiplexer, 4 to 1, single enable
NAN2	•	•	•	•	NAND, 2-input
NAN2C	•	•	•	•	NAND, 2-input, complementary outputs
NAN2CH	•	•	•	•	NAND, 2-input, complementary outputs, high drive
NAN2H	•	•	•	•	NAND, 2-input, high drive
NAN3	•	•	•	•	NAND, 3-input
NAN3C	•	•	•	•	NAND, 3-input, complementary outputs
NAN3H	•	•	•	•	NAND, 3-input, high drive

Digital cells (Sheet 3 of 6)

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
NAN4	•	•	•	•	NAND, 4-input
NAN4H	•	•	•	•	NAND, 4-input, high drive
NAN5	•	•	•	•	NAND, 5-input
NAN5C	•	•	•	•	NAND, 5-input, complementary outputs
NAN6	•	•	•	•	NAND, 6-input
NAN8	•		•		NAND, 8-input
NOR2	•	•	•	•	NOR, 2-input
NOR2C	•	•	•	•	NOR, 2-input, complementary outputs
NOR2CH	•	•	•	•	NOR, 2-input, complementary outputs, high drive
NOR2H	•	•	•	•	NOR, 2-input, high drive
NOR3	•	•	•	•	NOR, 3-input
NOR3C	•	•	•	•	NOR, 3-input, complementary outputs
NOR3H	•	•	•	•	NOR, 3-input, high drive
NOR4	•	•	•	•	NOR, 4-input
NOR5C	•	•	•	•	NOR, 5-input, complementary outputs
OAI22	•	•	•	•	OR-AND-INVERT, 2-2 input
OAI222	•	•			OR-AND-INVERT, 2-2-2 input
OAI22C	•	•	•	•	OR-AND-INVERT, 2-2 input, complementary outputs
OAI31	•	•	•	•	OR-AND-INVERT, 3-1 input
OAI333C	•	•	•	•	OR-AND-INVERT, 3-3-3 input, complementary outputs
OAI4333	•	•			OR-AND-INVERT, 4-3-3-3 input
ODPD2	•	•	•	•	Output pad, 2 mA, 5V open drain
ODPD4	•	•	•	•	Output pad, 4 mA, 5V open drain
ODPD8	•	•	•	•	Output pad, 8 mA, 5V open drain
ODPD16	•	•	•	•	Output pad, 16 mA, 5V open drain
ODPD24	•	•	•	•	Output pad, 24 mA, 5V open drain
ODPD48	•	•	•	•	Output pad, 48 mA, 5V open drain
ONPD2	•	•	•	•	Output pad, 2 mA, 7V open drain
ONPD4	•	•	•	•	Output pad, 4 mA, 7V open drain
ONPD8	•	•	•	•	Output pad, 8 mA, 7V open drain
ONPD16	•	•	•	•	Output pad, 16 mA, 7V open drain
ONPD24	•	•	•	•	Output pad, 24 mA, 7V open drain
OPD2	•	•	•	•	Output pad, 2mA drive
OPD4	•	•	•	•	Output pad, 4 mA drive
OPD8	•	•	•	•	Output pad, 8 mA drive
OPD8SYM		•			Output pad, 8 mA drive, symmetrical output

Digital cells (Sheet 4 of 6)

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
OPD16	•	•	•	•	Output pad, 16 mA drive
OPD16SYM	•				Output pad, 16 mA drive, symmetrical output
OPD24	•	•	•	•	Output pad, 24 mA drive,
OPPD2	•	•	•	•	Output pad, 2 mA drive, pullup/pulldown
OPPD4	•	•	•	•	Output pad, 4 mA drive, pullup/pulldown
OPPD8	•	•	•	•	Output pad, 8 mA drive, pullup/pulldown
OPPD16	•	•	•	•	Output pad, 16 mA drive, pullup/pulldown
OPPD24	•	•	•	•	Output pad, 24 mA drive, pullup/pulldown
OR2	•	•	•	•	OR, 2-input
OR3	•	•	•	•	OR, 3-input
OR4	•	•	•	•	OR, 4-input
OR8	•	•	•	•	OR, 8-input
OSCP	•				Oscillator
OSC5301		•			1-10 MHZ crystal oscillator
OSCP	•				Oscillator
OSC5301		•			1-10 MHz crystal oscillator
OSC5302		•			10-25 MHz crystal oscillator
OSC5402		•			10-25 MHz crystal oscillator
OSC5502		•			10-25 MHz crystal oscillator
OSC1401	•				10-25 MHz crystal oscillator
OSC1501	•				10-25 MHz crystal oscillator
OSC1502	•				10-25 MHz crystal oscillator
OTPD2	•	•	•	•	Output pad, 2 mA drive, tristate
OTPD4	•	•	•	•	Output pad, 4 mA drive, tristate
OTPD8	•	•	•	•	Output pad, 8 mA drive, tristate
OTPD16	•	•	•	•	Output pad, 16 mA drive, tristate
OTPD24	•	•	•	•	Output pad, 24 mA drive, tristate
OUTINV	•	•	•	•	Inverter, 4x drive, for driving pad cells
PCL2	•	•	•	•	Clock driver, complementary outputs
PD30	•	•	•	•	Pulldown cell, 30 μA
POR	•	•	•	•	Power on reset
PPD25	•	•	•	•	Pad pulldown cell, 25 μA
PPD100	•	•	•	•	Pad pulldown cell, 100μA
PPD200	•	•	•	•	Pad pulldown cell, 200 μA
PPD400	•	•	•	•	Pad pulldown cell, 400 μA
PPD800	•	•	•	•	Pad pulldown cell, 800 μA

Digital cells (Sheet 5 of 6)

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
PPD1600	•	•	•	•	Pad pulldown cell, 1600 µA
PPU25	•	•	•	•	Pad pullup cell, 25 µA
PPU100	•	•	•	•	Pad pullup, 100 µA
PPU200	•	•	•	•	Pad pullup cell, 200 µA
PPU400	•	•	•	•	Pad pullup cell, 400 µA
PPU800	•	•	•	•	Pad pullup cell, 800 µA
PPU1600	•	•	•	•	Pad pullup cell, 1600 µA
PU30	•	•	•	•	Pullup cell, 30 µA
SBUF	•	•	•	•	Buffer, small
SRP	•	•			Shift register, positive edge, 1 phase clock, 1-bit, serial and parallel input
SYNCRP	•				Metastable hard latch
TBUF	•	•	•	•	Buffer, tristate
TBUF3	•	•	•	•	Buffer, tristate, 3x drive
TBUFP	•	•	•	•	Buffer, tristate, enable active high
TBUFS		•			Buffer, tristate, enable active low
TFFRP	•	•			T FF, positive edge, 1 phase clock, resetb, toggle enable
TFFRPF	•	•			T FF, positive edge, 1 phase clock, resetb, toggle enable, fast
TFFRPP	•	•			T FF, positive edge, 1 phase clock, resetb, toggle enable, parallel load

Digital cells (Sheet 6 of 6)

7400 Series Macrocells

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
7430	•	•	•	•	8-input NAND
7442	•	•	•	•	4-line to 10-line decoder
7443	•	•	•	•	4-line to 10-line decoder
7444	•	•	•	•	4-line to 10-line decoder
7451	•	•	•	•	Dual 2-wide input AND-OR-invert gates
7482	•	•	•	•	2-bit binary full adder

7400 series macrocells (Sheet 1 of 3)

Cell Name	VS700	VS15000F	VGX7000	VGX15000	Description
7483	•	•	•	•	4-bit binary full adder with fast carry
7485	•	•	•	•	4-bit magnitude comparator
7486	•	•	•	•	Quad 2-input exclusive OR gates
7487	•	•	•	•	4-bit true/complement
7490	•	•	•	•	Decade counter
7492	•	•	•	•	Divide by two, six, or twelve counter
7493	•	•	•	•	4-bit binary counter
7494	•	•	•	•	4-bit shift register with presets
7498	•	•	•	•	4-bit data selector registers
74126	•	•	•	•	Quad tristate buffers
74138	•	•	•	•	3-line to 8-line decoder/multiplexer
74139	•	•	•	•	Dual 2-line to 4-line decoders/multiplexers
74147	•	•	•	•	Decimal to BCD priority encoder
74148	•	•	•	•	8-line to 3-line priority encoder
74150	•	•	•	•	1 of 16 data multiplexer
74151	•	•	•	•	1 of 8 data multiplexer
74151NS	•	•	•	•	1 of 8 data multiplexer
74152	•	•	•	•	1 of 8 data multiplexer
74153	•	•	•	•	Dual 4-line to 1-line data multiplexer
74156	•	•	•	•	Dual 2-line to 4-line decoder
74157	•	•	•	•	Quad 2-line to 1-line data multiplexers
74157NS	•	•	•	•	Quad 2-line to 1-line data multiplexers
74158	•	•	•	•	Quad 2-line to 1-line multiplexers
74161	•	•	•	•	Synchronous 4-bit counter
74161NE	•	•	•	•	4-bit binary counter without enable
74163CP	•	•	•	•	4-bit binary counter
74163L	•	•	•	•	4-bit binary counter
74163LC	•	•	•	•	4-bit binary counter
74163LCP	•	•	•	•	4-bit binary counter
74164	•	•	•	•	8-bit serial shift register
74165	•	•	•	•	8-bit shift register
74165C	•	•	•	•	8-bit shift register
74166	•	•	•	•	8-bit shift register
74173	•	•	•	•	Quad D-type flip-flops

7400 series macrocells (Sheet 2 of 3)

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
74174	•	•	•	•	Hex D-type flip-flops
74193	•	•	•	•	4-bit up/down binary counter
74193L0	•	•	•	•	4-bit up/down binary counter
74193L0001	•	•	•	•	4-bit up/down binary counter
74194	•	•	•	•	4-bit bidirectional shift register
74195	•	•	•	•	4-bit shift register
74195J	•	•	•	•	4-bit shift register
74195S	•	•	•	•	4-bit shift register
74240	•	•	•	•	Octal tristate buffers
74244	•	•	•	•	Octal tristate buffers
74244NT	•	•	•	•	Octal buffers
74245	•	•	•	•	Octal bus transceivers
74251	•	•	•	•	1 of 8 data selector/multiplexer
74257	•	•	•	•	Quad data multiplexers
74273	•	•	•	•	Octal D flip-flops
74273NC4	•	•	•	•	Quad D flip-flops
74273NC6	•	•	•	•	Hex D flip-flops
74283	•	•	•	•	4-bit binary full adder
74293	•	•	•	•	4-bit binary counter
74373	•	•	•	•	Octal D-type latches
74374	•	•	•	•	Octal D-type flip-flops
74374NT	•	•	•	•	Octal D-type flip-flops
74374NTC	•	•	•	•	Octal D-type flip-flops
74377	•	•	•	•	Octal D-type flip-flops
74393	•	•	•	•	Dual 4-bit binary counters
74669	•	•	•	•	4-bit up/down binary counter

7400 series macrocells (Sheet 3 of 3)

Supercells

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
NCR85C30	•				Serial communication controller
NCR16C450	•	•			UART
NCR16C550	•	•			UART
82077AA compatible	•				Floppy disk controller
7990 compatible	•				Ethernet LAN controller
NCR53C90A	•				SCSI core
NCR146818A		•			Real time clock plus RAM
NCR82C37A	•	•			DMA controller
NCR82C54		•			Programmable interval timer
NCR82C59A	•	•			Programmable interrupt controller

Supercells and generated cells

Compiled Supercells

Cell Name	VS700	VS1500F	VGX700	VGX1500	Description
DPRGEN	•	•			Dual Port RAM generator
FIFOGEN	•	•			First-in first-out memory block
MACCGEN		•			Configurable multiplier-accumulator
MULTGEN		•			Configurable multiplier
RAMGEN	•	•	•		Configurable RAM; up to 1024 words, up to 32 bitwords
ROMGEN	•	•	•		Configurable ROM; up to 8192 words, up to 32 bitwords
SRAM	•	•			Configurable static RAM; up to 1024 words by 16 bits

Analog Cells

Cell Name	VS700	VS1500F	Description
ADC5121		•	10/12-bit dual-slope integrating A/D converter
ADC5121AC		•	Dual-slope integrating A/D converter analog section
ANSW10K		•	Analog switch, 10 kohm on-resistance
ANSW1K		•	Analog switch, 1 kohm on-resistance, charge injection cancellation
BANDGAP		•	Bandgap voltage reference
CAPn		•	Capacitor, Poly/Active
CAP10		•	Capacitor, 10 picofarad
CP1001	•		General-purpose comparator
CP1101	•		High-speed comparator
CP5001		•	General-purpose comparator
CP5151		•	High-speed comparator
DAC5041		•	4-bit current output Digital/Analog converter
DAC5061		•	6-bit current output Digital/Analog converter
DAC5082		•	8-bit current output Digital/Analog converter
IPDA	•		Analog input pad
I4UPD		•	Analog input pad
I4UPD1	•	•	Analog input pad
OPDA	•		Analog output pad
O4UPD		•	Analog output pad
O4UPD2		•	Analog output pad
OA5001		•	General-purpose opamp
OA5001B		•	General-purpose opamp
OA5002		•	Micropower opamp
OA5201		•	Rail-to-rail opamp
RESMN		•	Matched pair of N-plus diffusion resistors
RESMNW		•	Matched pair of N-well resistors
RESMP		•	Matched pair of P-plus diffusion resistors
RESMPO		•	Matched pair of poly resistors
RESN		•	Resistor, custom N-plus diffusion
RESNW		•	Resistor, custom N-well
RESP		•	Resistor, custom P-plus diffusion

Analog cells (Sheet 1 of 2)

Cell Name	VS700	VS1500F	Description
RESPO		•	Resistor, custom Poly
VCO5401C		•	Voltage-controlled oscillator core

Analog cells (Sheet 2 of 2)

Scan Cells

Cell Name	VS700	VS1500F	Description
BSENBR	•		Boundary for tristate enable
BSINMUX	•		Multiplexor
BSINR	•		Boundary for input pads
BSINV4	•		Multiplexor
BSINV8	•		Multiplexor
BSIOR1	•		Boundary for input/output pads
BSIOR4	•		Boundary for input/output pads
BSIOR8	•		Boundary for input/output pads
BSOTR1	•		Boundary for tristate pads
BSOTR4	•		Boundary for tristate pads
BSOTR8	•		Boundary for tristate pads
BSOUTR1	•		Boundary for output pads
BSOUTR4	•		Boundary for output pads
BSOUTR8	•		Boundary for output pads
DFFRPFX00	•		Internal D flip-flop with muxed data clock
DFFRPFX04	•		Internal D flip-flop with muxed data clock
DFFRPFX08	•		Internal D flip-flop with muxed data clock
DFFRPFX120	•		Internal D flip-flop with muxed data clock
IRCELL0	•		Instruction register
IRCELL1	•		Instruction register
TAP_CONTROLLER	•		Tap controller

Library Naming Conventions

The naming conventions for the Standard Cell and Gate Array libraries follow the same conventions. Equivalent cell functions have the same name in each of the libraries. As an example, an EXOR cell (the name of the cell that performs a 2-input exclusive OR function) is called an EXOR cell in each of the VS1500F, VS700, VGX1500, and VGX700 libraries.

The digital cell naming conventions are built around a root name and include several different types of identifying characters called "tags". These tags are mnemonic indicators that further differentiate a cell's function, behavior, or configuration. As an example, Figure 9-1 identifies the root name and tags of a high drive, Input/Output Buffer.

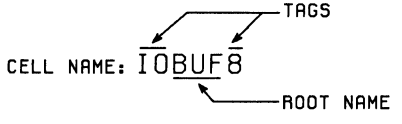


Figure 9-1 Cell name

There are two basic types of tags. The suffix tag and the prefix tag. The most commonly found are suffix tags which consist of letters and/or numbers. The prefix tags consist of letters only. There is no significance as to whether the tag precedes the root name or follows it. However, in the case of pad and pullup/pulldown cells, the numbers that indicate pad drive and pullup/pulldown currents are always suffix tags. In the case of multiple suffix tags, the number is last.

A class of cells also exist that are not pad or pullup/pulldown cells. They are the AND-OR-Invert, the OR-AND-Invert, and Schmitt Trigger gates. These cells have, as a suffix tag, a sequence of numbers with implied meaning. The meaning of these "coded" numbers is shown in Table 9-4.

The cell naming conventions are just that, "conventions". In the "early days of development" the naming rules were not as strictly adhered to as in the present. As a result, there are a number of anomalies, which for historical and migration reasons, have been carried through the various libraries. Some of the more common cell name anomalies are listed in Table 9-5. This table includes a short description of what the cell name should be.

The JTAG Scan cells are a recent addition to the VS700 library. For user identification convenience, the Scan cells have been divided into two types: Boundary Scan (root name BS) and Internal Scan. Instruction Register (IR) and Tap Controller cells are also included under the Boundary Scan cell heading. The Internal Scan cells are essentially multiplexed Flip-flops (root name DFFR). Note: The DFFRMP in the basic Standard Cell library is also considered to be an Internal Scan cell.

Table 9–1 has examples of cell names showing their root names and tags. Next to the tag in the Meaning column is a brief explanation of that particular tag.

Description	Cell Name	Root Name	Tags	Meaning
8–input AND gate	AND8	AND	8	inputs
2–input NAND gate	NAN2	NAN	2	inputs
D–type Flip–Flop with Reset & Set	DFFRS	DFF	RS	with Reset & Set
Latch with Reset	LATR	LAT	R	with Reset only
Input Pad	INPD	PD	IN	
1 of 4 Decoder	DEC1OF4	DEC	1OF4	1 of 4
AND–OR–Invert gate	AO1222	AOI	222	number coding
Tristate Inverter	INVT	INV	T	Tristate

TABLE 9–1 Cell and root names

In general, there are two kinds of identifying tags. Those that are added to the end of the root name and the "type" prefixes. The "type" prefixes identify what type of signal relationship or configuration the cell has and precede the root name. These are normally found on pad and buffer cells. In Figure 9–1, the IO tag is a type prefix indication that this Buffer cell is to be used for buffering bidirectional pads.

Only for pad cells and pullups and pulldowns does the number at the end of the cell name ("n" and "m" in the table) have additional design meaning. The "current" tags represent drive current and pullup/pulldown current, respectively. In the case of buffers, the number at the end DOES NOT indicate current capability. It is a gross approximation for the relative size of the normalized n–channel area of the output transistor. This indirectly translates into a drive current capability.

Table 9–2 lists the tags, meanings, and gives examples for each non–pad and pullup/pulldown cell name.

Tags	Meaning	Example
H	High Drive Characteristics	NAN2H
M	Medium Drive Capability Multiplexed inputs	MBUF DFFRMP
C	Complimentary Outputs	NOR3C
R	Reset	DFFR
S	Set	DFFRS (has both set & reset)
P	Positive Edge Trigger (parallel load when used with clocked devices)	DFFP DFFRPP
T	Tristate may precede root; such as.... Toggle (Flip–Flops)	INVT TBUF TFFRPP
G	Gated	CCNDG
Q	Only 1 Q output (indicates a smaller–sized cell)	
F	Fast (special high speed cells)	DFFRPF
Z	Zero set–up time (on Flip–Flops)	DFFRPZ
n	If the cell is not a pad or a number coded cell, then: n = number of inputs (an exception: MUX1OF4)	NAN6

TABLE 9–2 Tag meanings

Table 9–3 lists the "type" prefixes for the Input/Output pads. Although not a true type prefix (because they are "tacked on to the end" of the cell name), the number reference for pad and pullup/pulldown cells is included.

	Tags	Meaning	Example
Direction Indicators	I, IN	INput only	INPD
	O	Output only	OPD4
	IO	Input/Output	IOPD2
Pad Configurations	D	open Drain (with external pullup)	ODPD2
	T	Tristate	OTPD16
	P	Internal Pullup/pulldown port	IOPPD4
Current	n	number n x 1 mA for outputs	OPD2 ← 2 mA output drive current
	m	number m x µA for pullup/pulldown	PPU400 ← 400µA pullup current

TABLE 9–3 Input/Output pads

The Special Gate Naming Convention table describes the number coded cells consisting of the combinational gates (AOIxxx, OAIxxx), and the Schmitt Trigger (DSxxxx) gates.

For the combinational gates, the following terminology has been adopted:

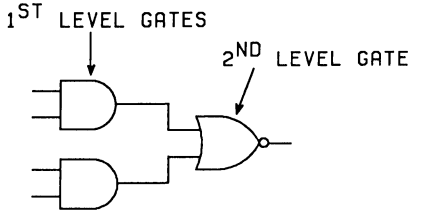


Figure 9–2

For the Schmitt Trigger, use this diagram as a reference.

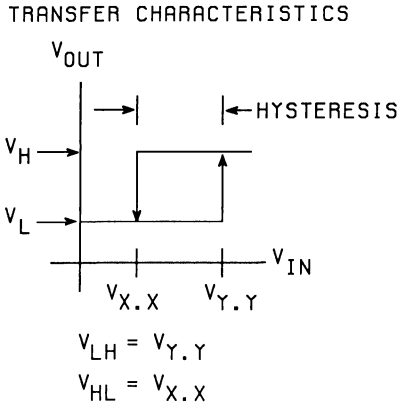


Figure 9–3

Description	Explanation	Example
Combinational Gates: AOIxxx (AND–OR–Invert) OAIxxx (OR–AND–Invert)	X identifies the number of inputs to each first level gate. If X = 1, then a single input to the next stage is implied. The total number of first stage gates equals the total number of X's.	OAI4333 An OR–AND–Invert gate having one 4–input OR gate, three 3–input OR gates and feeding a 4 input NAND gate.
Schmitt Triggers: DSXXYY (Digital Schmitt Trigger)	XX = X.X = the nominal high to low threshold switching voltage. YY = Y.Y = the nominal low to high threshold switching voltage Hysteresis = (Y.Y – X.X)volts	DS1218 A Schmitt trigger buffer having a low to high switching threshold of 1.8 Volts (nominal) and a high to low switch point of 1.2 Volts (nominal).

TABLE 9–4 Special gate naming conventions

In general, the naming convention rules hold for about 95% of all of the Standard Cell and Gate Array libraries. There are a number of anomalies, which (for historical and migration reasons) have been kept in the cell libraries. Some of the more obvious ones are listed below.

Cell Name	Reason for Anomaly
ADD4CS	CS is Carry Select; not Complementary output with Set
ADFUL	This is a single-bit FULL ADDer
BUF8	The 8 indicates 8x drive capability, not an input
CCND	Should be CCNAN
CCNR	Should be CCNOR
DEC1OF4	1 of 4 is part of the Decoder description, not part of the characteristic
DEC1OF8	1 of 8 is part of the Decoder description, not part of the characteristic
IPPD	Should be an INPPD
IOBUFM	MBUF with I/O capability
IOBUFS	SBUF with I/O capability
OPPD#	Tristate output pad

TABLE 9-5 Cell naming anomalies

CMOS Latch–up and ESD

Latch–up will not be a problem for most designs but the designer should be aware of its causes and prevention.

Figure 9–4 shows the cross–section of a typical CMOS inverter and Figure 9–5 shows the parasitic bipolar devices that are activated during latch–up. The circuit formed by the parasitic transistors and resistors is the basic configuration of a Silicon Controlled Rectifier (SCR). In the latch–up condition, transistors Q1 and Q2 are turned ON, each providing the base current necessary for the other to remain in saturation, thereby latching the devices in the ON state. Unlike a conventional SCR, where the device is turned ON by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned ON by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output; therefore, to latch–up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than V_{SS} – 0.5 Vdc and have sufficient current to trigger the SCR. The latch–up mechanism is similar for the inputs.

To help eliminate latch–up, an extra collector has been added to the CMOS devices as shown between the n– and p–channel devices in Figure 9–5. This shows up as an additional collector with a low resistance to the respective power supply. This effectively adds a parallel path to the well resistance, reducing the available bias current for the parasitic bipolar devices.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences follow.

1. Ensure that inputs and outputs are limited to the maximum rated values, as follows:

   $-0.5 < Vin < V_{DD} - 0.5$ Vdc
   (referenced to V_{SS})
   $-0.5 < Vout < V_{DD} - 0.5$ Vdc
   (referenced to V_{SS})
   $|Iin| < |20mA|$
   $|Iout| < |20mA|$
2. If voltage transients of sufficient energy to latch–up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum rating of 20 mA.
3. Sequence power supplies so that the inputs or outputs of standard cell devices are not activated before the supply pins are powered up (e.g. recessed edge connectors and/or series resistors may be used in plug–in board applications).
4. Voltage regulating or filtering should be used in board design and layout to ensure that power–supply lines are free of excessive noise.
5. Limit the available power supply current to the devices that are subject to latch–up conditions. This can be accomplished with the power supply filtering network or with a current–limiting regulator.

All NCR devices have input protection circuitry to prevent gate oxide breakdown due to electrostatic discharge (ESD). This protection consists of a diode to V_{DD} and a diode to V_{SS}. A series resistor is also placed between the pad and the gate of the input cell. This resistor shows the fast rising static pulses to the input. The ESD protection for NCR standard cell devices is typically 5 kV.

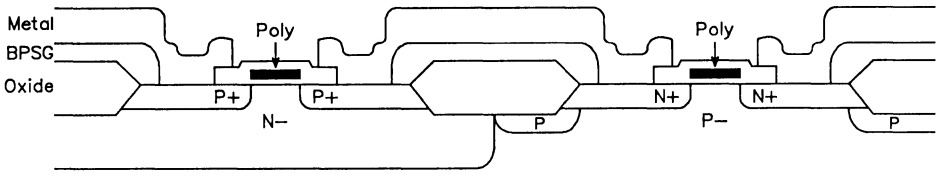


Figure 9–4 CMOS Inverter cross section

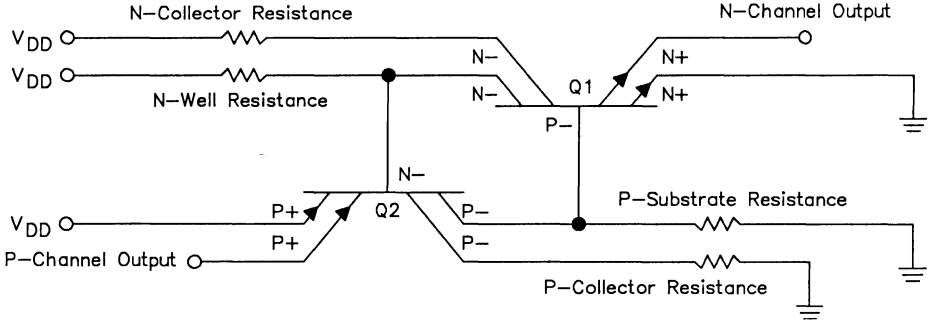


Figure 9–5 Latch–up circuit schematic

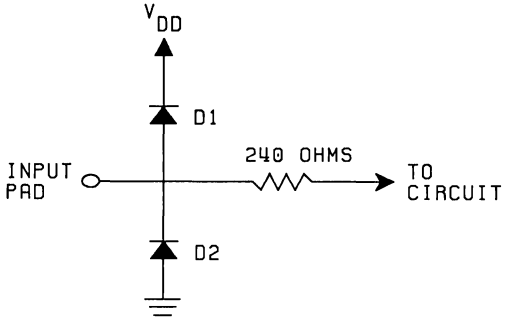


Figure 9–6 Input protection network

		ESD* #		LATCHUP**	
		Typical	**Minimum**	**Typical**	**Minimum**
NCR Library	VS700	above 3KV	2KV	above 400 mA	150 mA
	VGX700	above 3KV	2KV	above 400 mA	150 mA
	VS1500	above 5KV	3KV	above 250 mA	150 mA
	VGX1500	above 5KV	3KV	above 250 mA	150 mA

*ESD uses MIL-STD-883C Method 3015 as a guideline to testing.
**Latchup testing complies with JEDEC JC-40.2 "A Standardized Test Procedure for the Characterization of Latchup in CMOS ICs".
#Excludes OSCP.

TABLE 9-6 Environmental electrical protection (temperature = 25 C)

Handling Precautions

The NCR CMOS libraries like all MOS devices have isolated gates that are subject to voltage breakdown. The gate oxide on standard cell devices breaks down at a gate–source potential of about 35 V. To guard against such a breakdown from static discharge or other voltage transients, the protection network shown in Figure 9–7 is used on each pad cell. The input protection network (IP) is a diode to V_{DD} and a diode to V_{SS}. In addition to this protection, a series resistor is placed between the pad and the gate of the input cell to slow the fast rising static pulses to the input. The protection for standard cell inputs is typically 5 kV, greatly reducing the chance of ES–damaged devices. The electrostatic discharge rest circuit is shown in Figure 9–8.

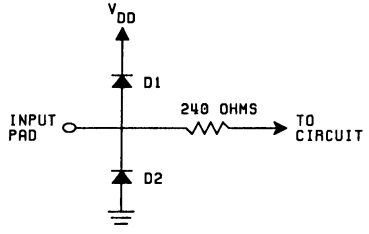


Figure 9–7 Input protection network

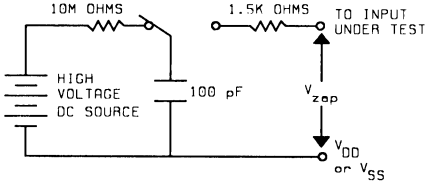


Figure 9–8 Electrostatic discharge test circuit

Static–damaged devices behave in various ways depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS} or open–circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–15 kV range (depending on humidity, surface conditions, etc.). The following precautions should be observed:

1. Do not exceed the maximum ratings specified in the electrical characteristics.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low–impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS standard cell devices is merely an extension of the device, and the same handling precautions apply. Contacting edge connectors wired directly to CMOS standard cell device input can cause damage. Plastic wrapping should be

avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. For convenience, a graph of the typical added propagation delay is given in Figure 9–9 for a switch point of 0.5 V_{DD} and an input capacitance of 10 pF. Note that the maximum input rise and fall times should not be exceeded. For an input capacitance of 10 pF, a maximum series resistance of 30k ohms can be used without violating the maximum input rise and fall times. In Figure 9–10, two possible networks are shown using a series resistor to help eliminate off board ESD (Electrostatic Discharge).

5. All CMOS standard cell devices should be stored or transported in materials that are antistatic. CMOS standard cell devices must not be inserted into conventional plastic "snow", Styrofoam or plastic trays, but should be left in their original container until ready for use.

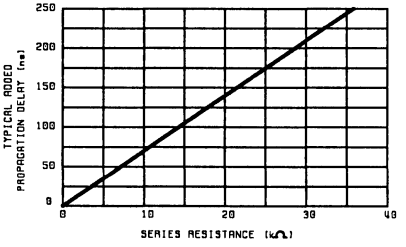


Figure 9–9 Series resistance effects

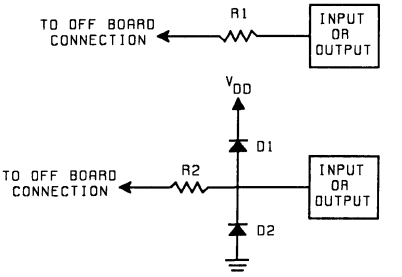


Figure 9–10 Networks for minimizing ESD and reducing CMOS latch–up susceptibility

6. All CMOS standard cell devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices since a worker can be statically charged, with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 9–11 for and example of a typical workstation.

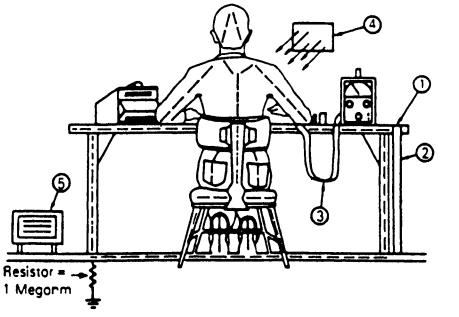


Figure 9–11 Typical manufacturing work station

7. Nylon or other static generating materials should not come in contact with CMOS standard cell devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the

device, the belts or the boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom or sides of CMOS packages must be grounded to metal or other conductive material.

9. Cold chambers using CO_2 for cooling should be equipped with baffles, and CMOS standard cell devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board-cleaning operations.
    a. Vapor degreasers and baskets must be grounded to an earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards containing CMOS standard cells are grounded and a static eliminator is directed at the board.
13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the 'presence of CMOS devices and require familiarization with this specification prior to performing any kind or maintenance or replacement or devices or modules.
15. Do not insert or remove CMOS standard cell devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of V_{DD} and V_{SS} before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Continuous use causes deterioration of their antistatic coating.

Recommended for Reading

"Total Control of the Static in Your Business"

Available by writing to:
3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769-2963

Or by calling:
1-800-328-1368

Effects of Moisture on Surface Mount Components

The effects of moisture absorbed by plastic encapsulating compounds on surface mountable components have become a matter of concern for systems manufacturers utilizing these components. To date, many studies have been performed regarding these effects including those performed by NCR Microelectronic Products Division. The following statements and recommendations have resulted from these studies.

All surface mount plastic packages are susceptible to these effects, including QFPs, SOICs and PLCCs.

The presence of moisture in the amounts studied does not represent quality or reliability issues until the components are exposed to the temperatures typical of Infrared (IR) or Vapor Phase reflow soldering. These temperatures are typically in excess of 200°C and the components are exposed to these temperatures for typically 10 to 60 seconds. If sufficient moisture is present, the internal stress induced by these conditions can be sufficient to crack the encapsulating compound. Other effects such as delamination of the encapsulating compound at the lead frame or die interface have also been observed.

Manufacturers who socket components or use lower temperature surface mount techniques will not observe this phenomenon.

Failure of components, if it occurs, is generally detected during testing of the product after the surface mount process.

The amount of moisture necessary to cause these effects has been studied by NCR. For QFP packages the maximum acceptable moisture content in 0.15% by weight as determined by NCR. This value is similar to that observed by other manufacturers of surface mount components. Studies suggest that the maximum for PLCCs is somewhat higher, near 0.2% or greater. The exact values for SOIC packages could be as low as 0.05%. The reason for this variation is primarily due to the thickness of mold compound beneath the die paddle.

The factors which affect the susceptibility of a package to cracking include not only the moisture content but also the leadframe and die paddle size and configuration, the reflow process temperature profile, the plastic thickness under the die paddle, and the strength of the encapsulating plastic. (Although studies to date at NCR have not quantified all of these effects, they have been taken into account when formulating recommendations.)

Of critical importance to the amount of moisture absorbed by a component are the storage conditions prior to surface mount and the length of time stored. Absorption curves for QFP packages have shown that harmful amounts of moisture may be absorbed by a component at 30°C in a 95% relative humidity environment in 12 to 15 days. However, experiments have also shown no measurable increase in moisture content for PLCCs for storage periods up to 90 days in a 20% relative humidity environment at room temperature. Obviously, the storage conditions are of considerable importance in minimizing these effects, especially when ambient conditions include high temperature and humidity. Components which will be surface mounted should be stored in a dry environment or sealed in moisture barrier packaging. The packaging should include a

desiccant to absorb any moisture which is sealed in the packaging. Once the package is opened the components should be surface mounted within 72 hours, or returned to dry storage (less than 20% R.H.), or resealed in moisture barrier bags. If this does not occur, the components may require baking prior to surface mounting.

The baking of surface mountable components can be performed within plastic shipping tubes; however, this must be performed at 40°C or less making typical bake times about a week. They may also be baked at 125°C for 24 hours or at 150°C for 12 hours; however, this may require transfer of the components to high temperature trays or metal tubes.

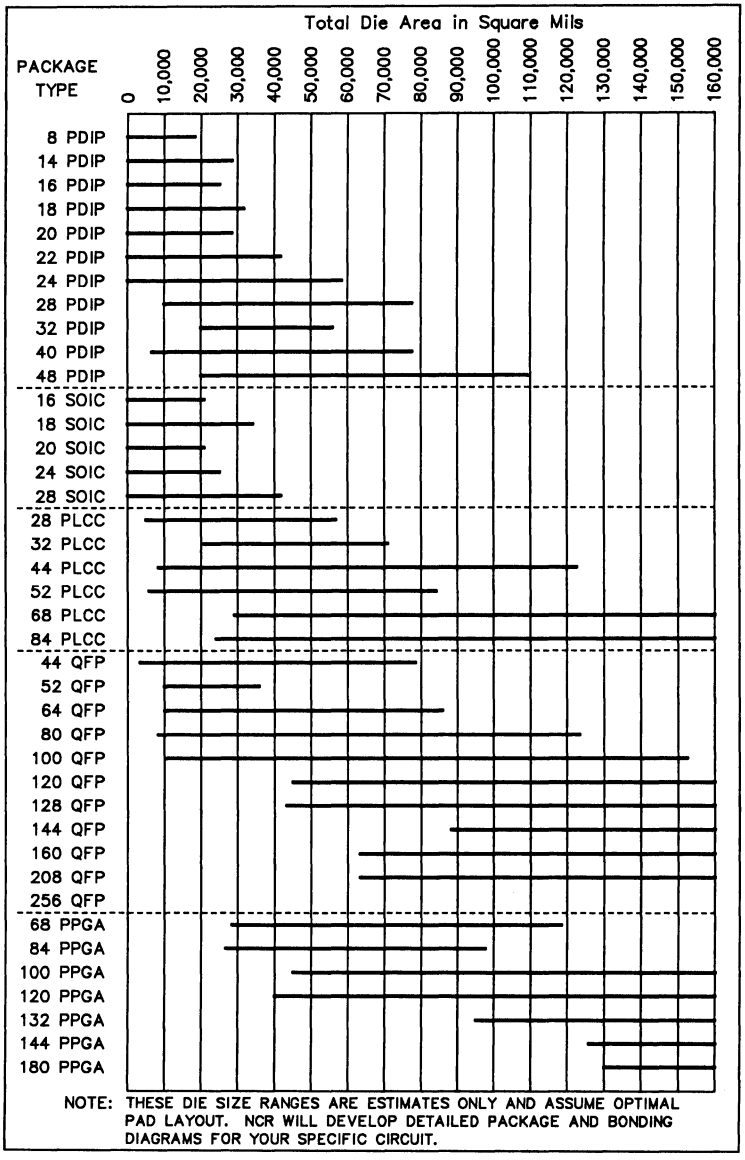
There is a JEDEC-approved standard bakable tray for QFPs which is capable of withstanding a 150°C bake. PLCC and SOIC packages may be transferred to metal tubes for baking.

Other very important precautionary measures a customer can take include minimizing the surface mount temperature and exposure time and maintaining statistical control of these variables.

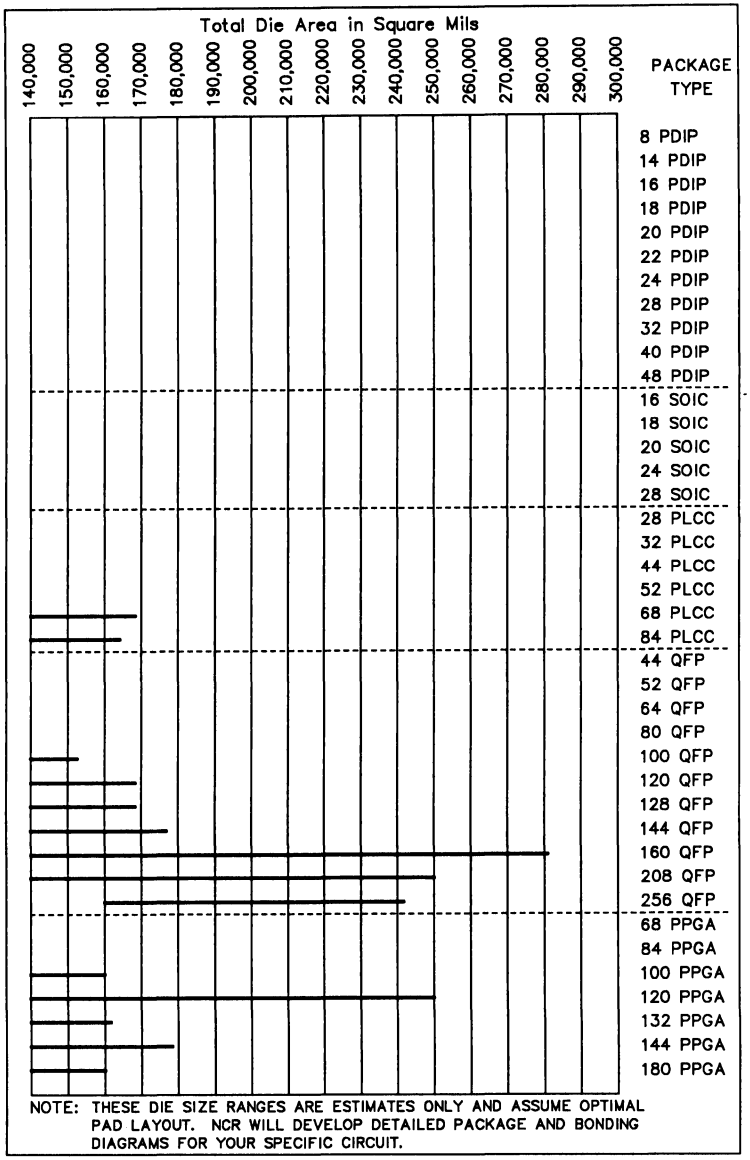
NCR began supplying all surface mount components in moisture barrier packaging in the third quarter of 1989. NCR also requires dry-pack from all assembly subcontractors for shipments back to NCR. The dry-pack which the subcontractors perform for shipment to NCR will typically provide a dry environment for up to 6 months. This is more than sufficient for the typically short shipment times from the Far East to the U.S. The dry-pack which NCR performs prior to shipment to the customer will provide a dry environment for 1 1/2 to 2 years, depending on the package type.

NCR's strategy is to require our subcontractors to provide a product with an acceptable level of moisture content, and utilize dry-pack for all shipment and storage. NCR believes that the most effective way to provide a dry product to our customers is to effectively control the exposure to moisture. Since implementing these procedures, NCR has eliminated customer-related issues with moisture-absorption failures resulting from surface-mount board assembly techniques.

Typical Plastic Package Die Size Ranges



(Sheet 1 of 2)


Total Die Area in Square Mils
140,000
150,000
160,000
170,000
180,000
190,000
200,000
210,000
220,000
230,000
240,000
250,000
260,000
270,000
280,000
290,000
300,000
PACKAGE TYPE
8 PDIP
14 PDIP
16 PDIP
18 PDIP
20 PDIP
22 PDIP
24 PDIP
28 PDIP
32 PDIP
40 PDIP
48 PDIP
16 SOIC
18 SOIC
20 SOIC
24 SOIC
28 SOIC
28 PLCC
32 PLCC
44 PLCC
52 PLCC
68 PLCC
84 PLCC
44 QFP
52 QFP
64 QFP
80 QFP
100 QFP
120 QFP
128 QFP
144 QFP
160 QFP
208 QFP
256 QFP
68 PPGA
84 PPGA
100 PPGA
120 PPGA
132 PPGA
144 PPGA
180 PPGA
NOTE: THESE DIE SIZE RANGES ARE ESTIMATES ONLY AND ASSUME OPTIMAL PAD LAYOUT. NCR WILL DEVELOP DETAILED PACKAGE AND BONDING DIAGRAMS FOR YOUR SPECIFIC CIRCUIT.

(Sheet 2 of 2)

Packaging Summary Table

LEAD COUNT	PDIP	SIDE BRAZE	WIDE SOIC	LCC	LDCC/ CFP	PLCC	CERQUAD	QFP	CPGA	PPGA
8	x	x								
14	x	x								
16	x	x	x	x						
18	x	x	x	x						
20	x	x	x	x			x			
22	x	x								
24	x	x	x	x	x					
28	x	x	x	x		x	x			
30										
32				x		x				
36				x						
40	x	x		x						
44				x	x	x	x	x		
48	x	x		x	x				x	
52				x	x	x	x	x		
56										
64				x				x	x	
68				x	x	x	x		x	x
72										x
80								x		
84				x	x	x	x		x	x
88										
96										
100				x	x		x	x	x	x
104										
108									x	x
120								x	x	x
124				x	x		x		x	
128								x		
132					x		x		x	x
139										
144					x				x	x
148							x			
160								x		
172									x	
180										x
196					x					
208								x		
224										
256								x		

ASIC package type listing

Note: New packages are added on a regular basis. Please contact your NCR Sales Representative if the package you need is not listed.

Plastic Package Outline Drawings

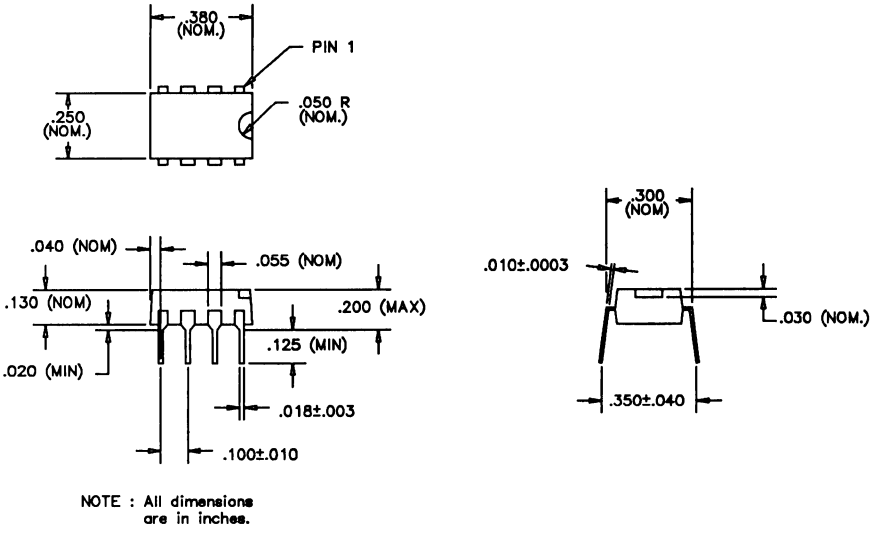


Figure 9–12 8–lead plastic DIP package

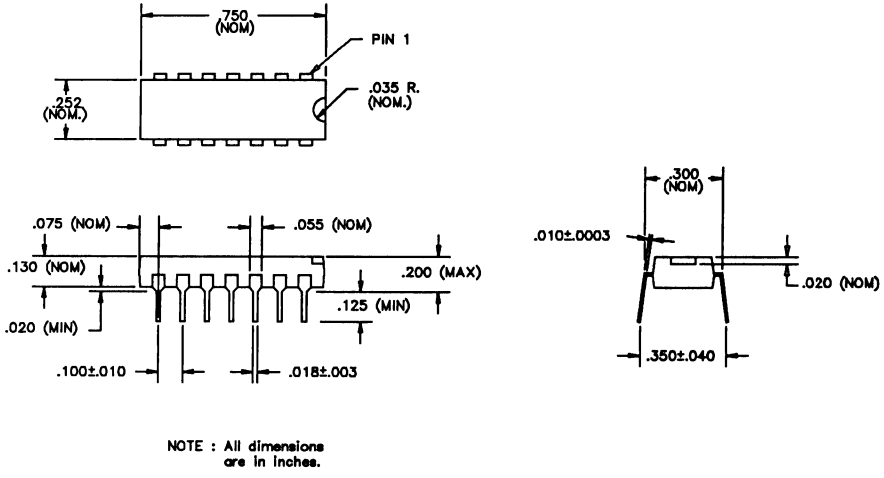


Figure 9–13 14–lead plastic DIP package

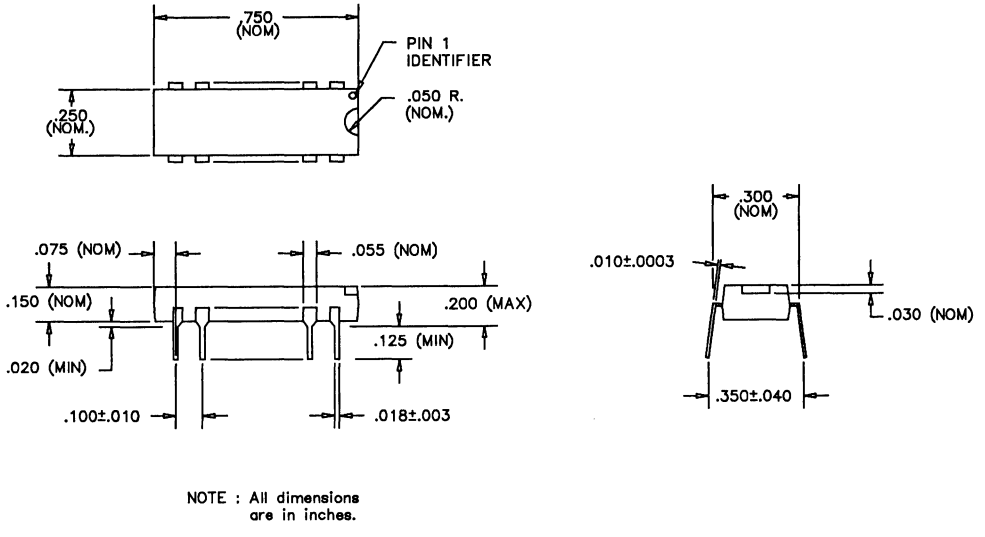


Figure 9–14 16–lead plastic DIP package

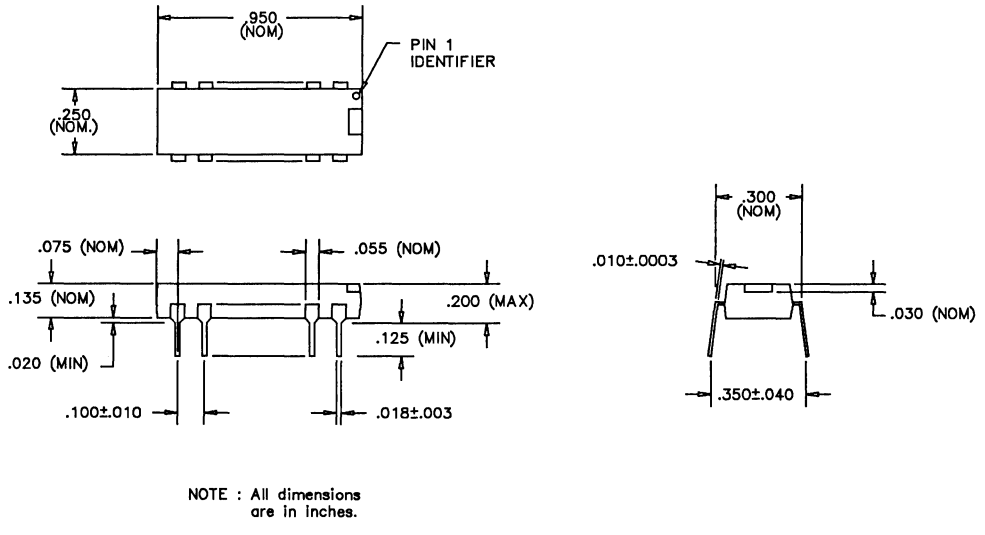


Figure 9–15 18–lead plastic DIP package

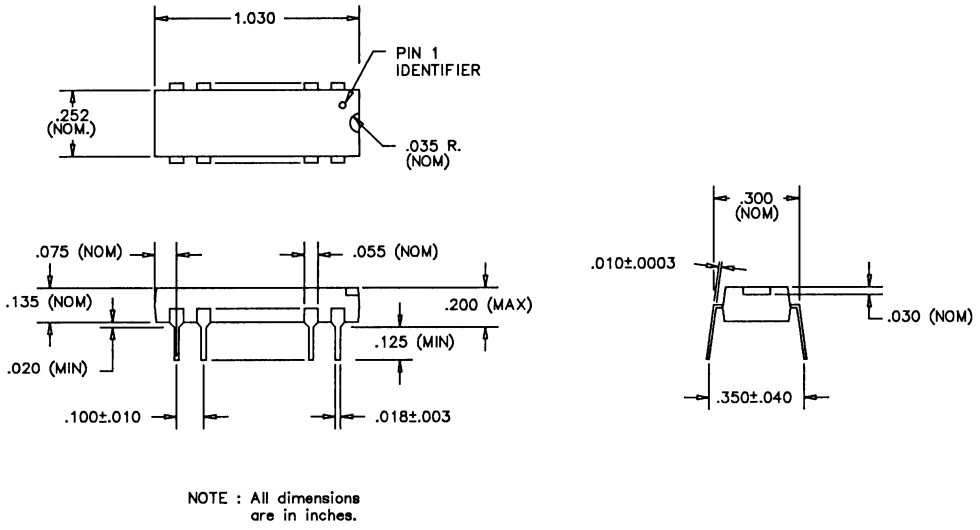


Figure 9–16 20–lead plastic DIP package

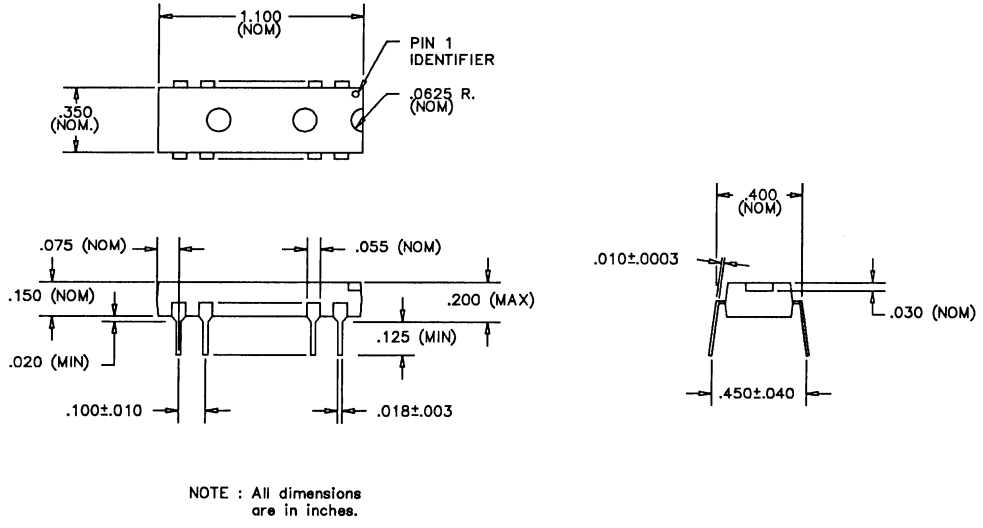


Figure 9–17 22–lead plastic DIP package

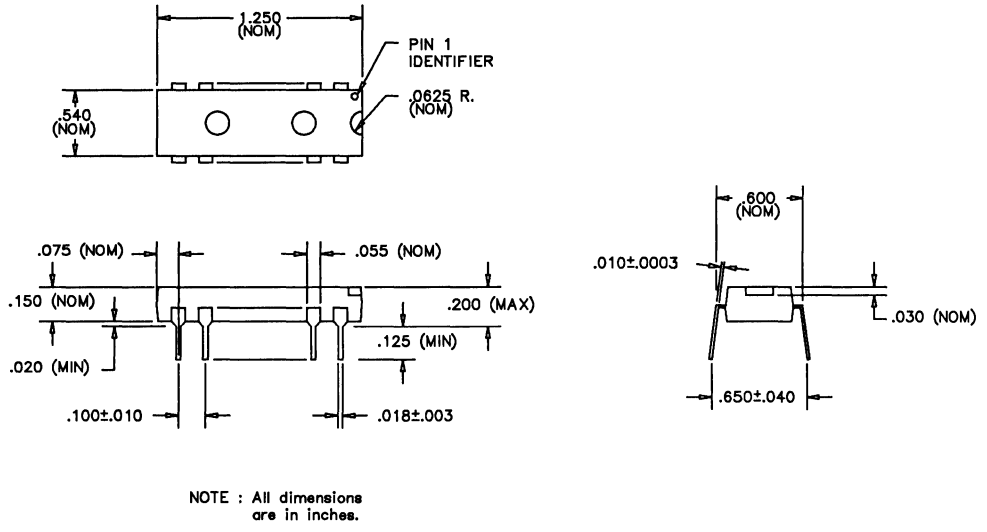


Figure 9-18 24-lead plastic DIP package

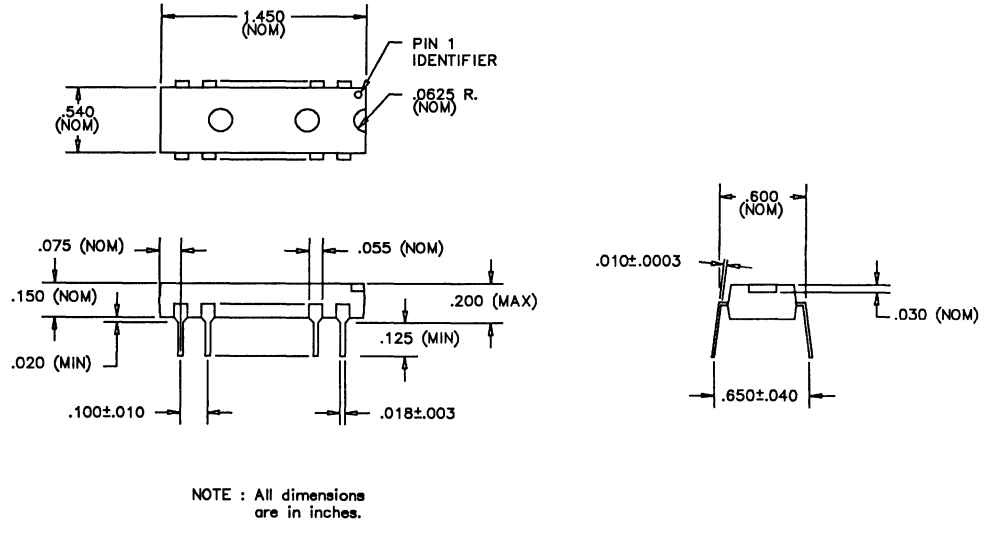
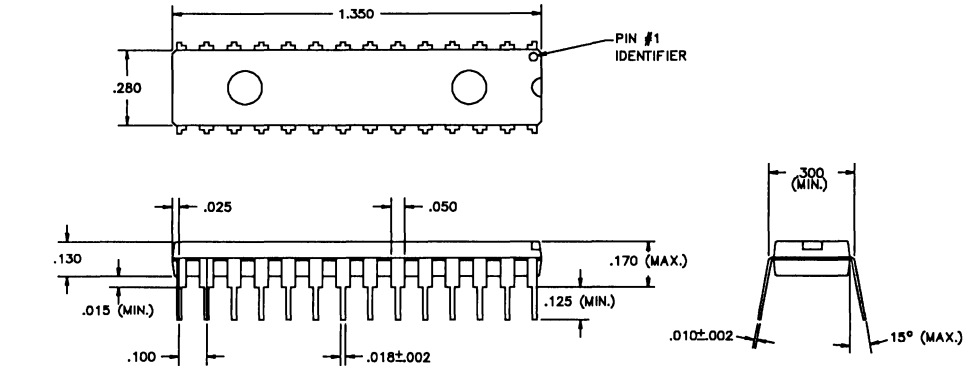
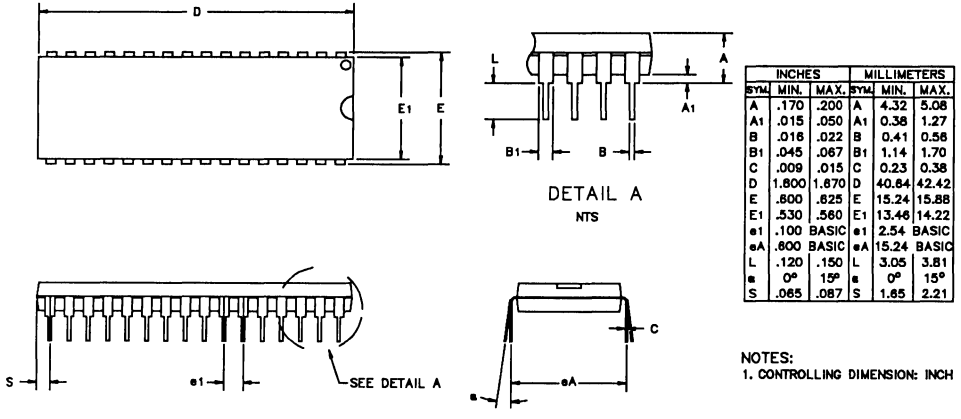


Figure 9-19 28-lead plastic DIP package



NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL.
2. ALL DIMENSIONS ARE SHOWN IN INCHES.

Figure 9-20 28-lead PDIP (skinny) customer package outline



	INCHES			MILLIMETERS	
SYM.	MIN.	MAX.	SYM.	MIN.	MAX.
A	.170	.200	A	4.32	5.08
A1	.015	.050	A1	0.38	1.27
B	.016	.022	B	0.41	0.56
B1	.045	.067	B1	1.14	1.70
C	.009	.015	C	0.23	0.38
D	1.600	1.670	D	40.64	42.42
E	.600	.625	E	15.24	15.88
E1	.530	.560	E1	13.46	14.22
e1	.100	BASIC	e1	2.54	BASIC
eA	.600	BASIC	eA	15.24	BASIC
L	.120	.150	L	3.05	3.81
e	0°	15°	e	0°	15°
S	.065	.087	S	1.65	2.21

NOTES:
1. CONTROLLING DIMENSION: INCH

Figure 9-21 32-lead plastic DIP customer package outline (.600 inch)

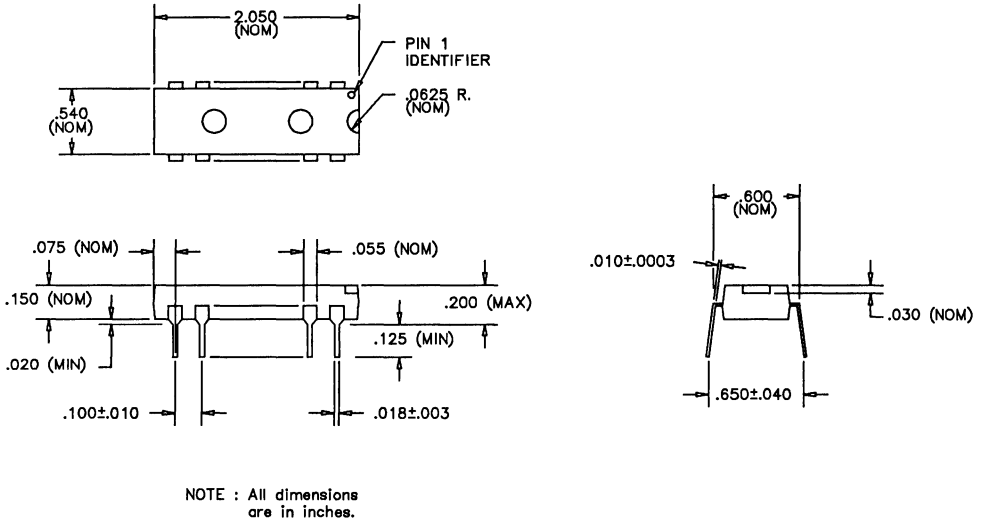


Figure 9–22 40–lead plastic DIP package

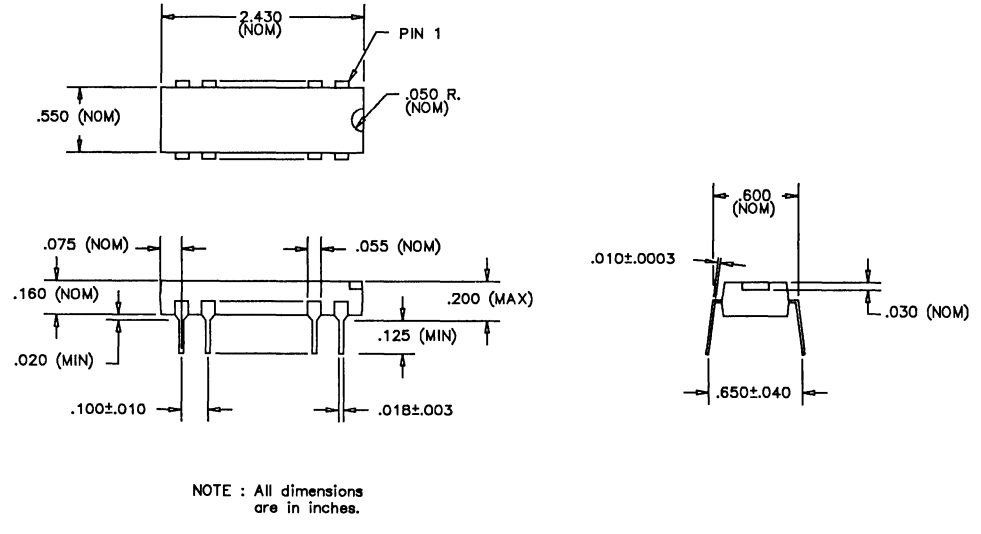


Figure 9–23 48–lead plastic DIP package

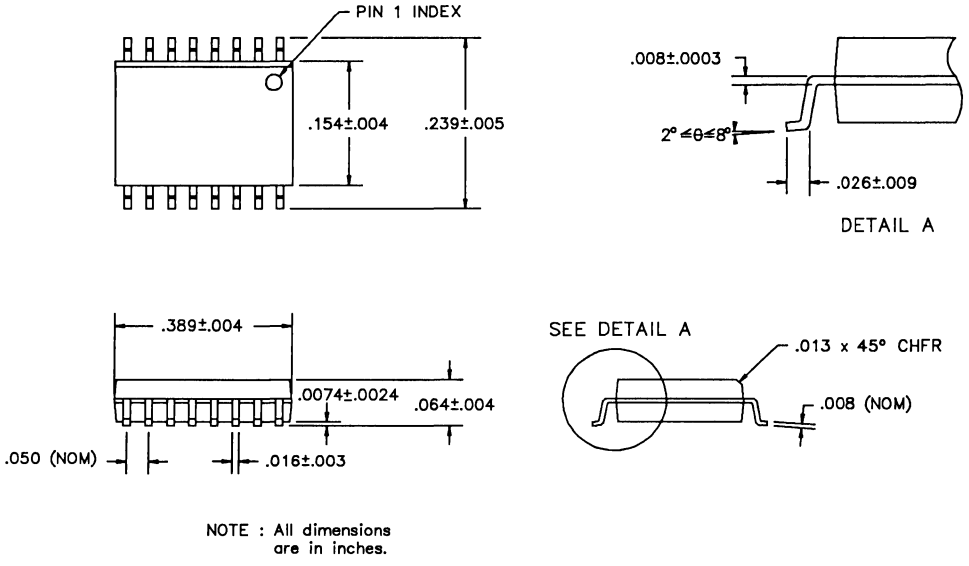


Figure 9–24 16–lead wide SOIC molded package

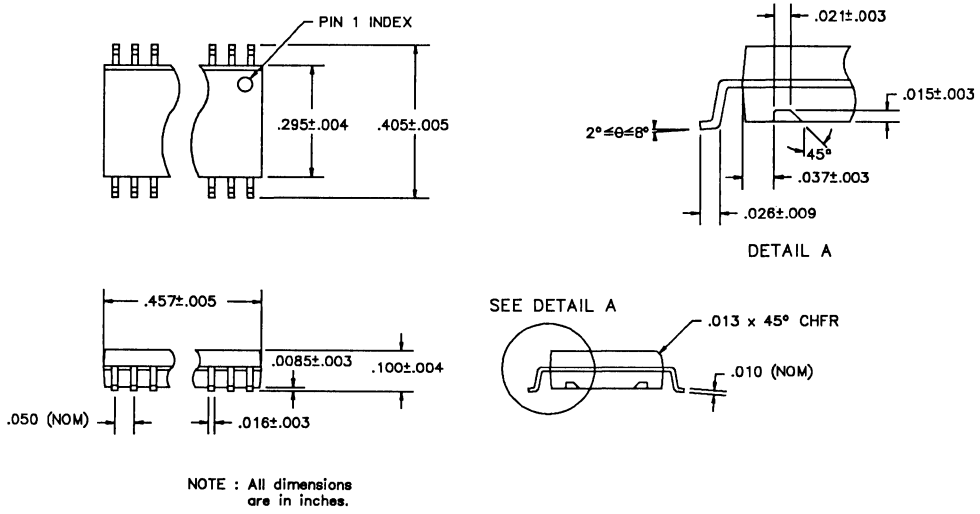


Figure 9–25 18–lead wide SOIC molded package

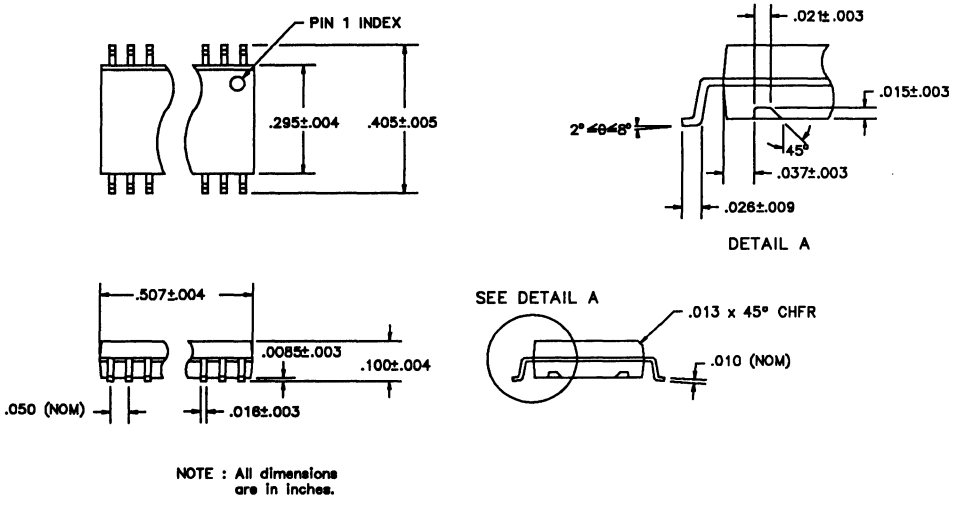


Figure 9-26 20-lead wide SOIC molded package

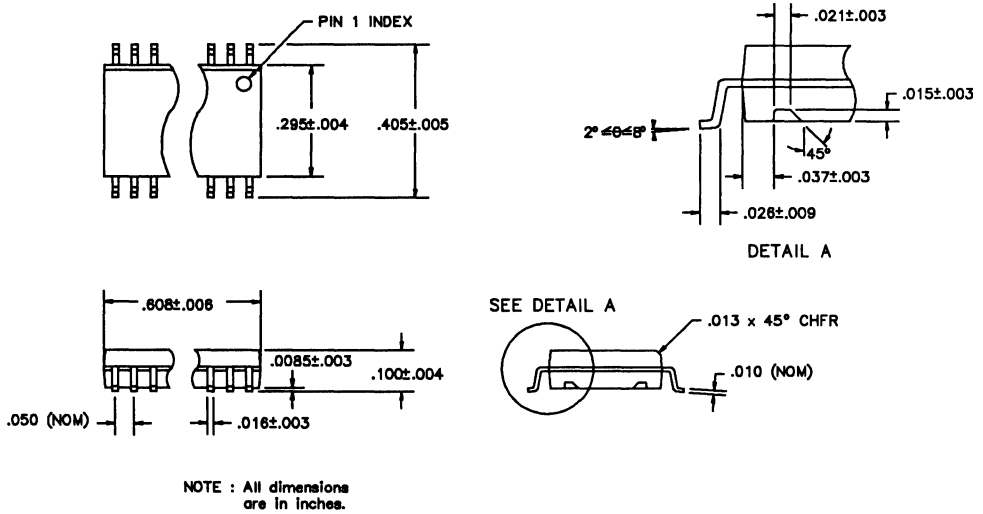


Figure 9-27 24-lead wide SOIC molded package

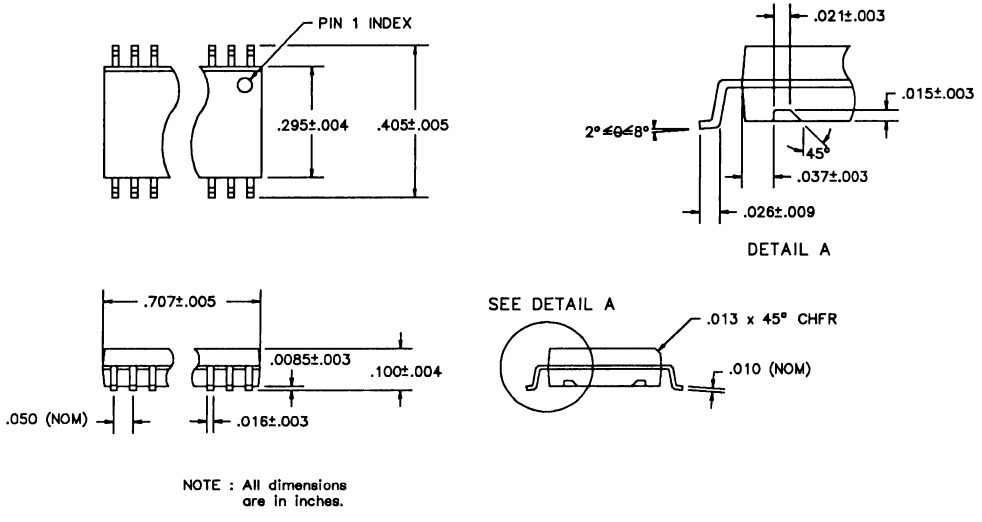
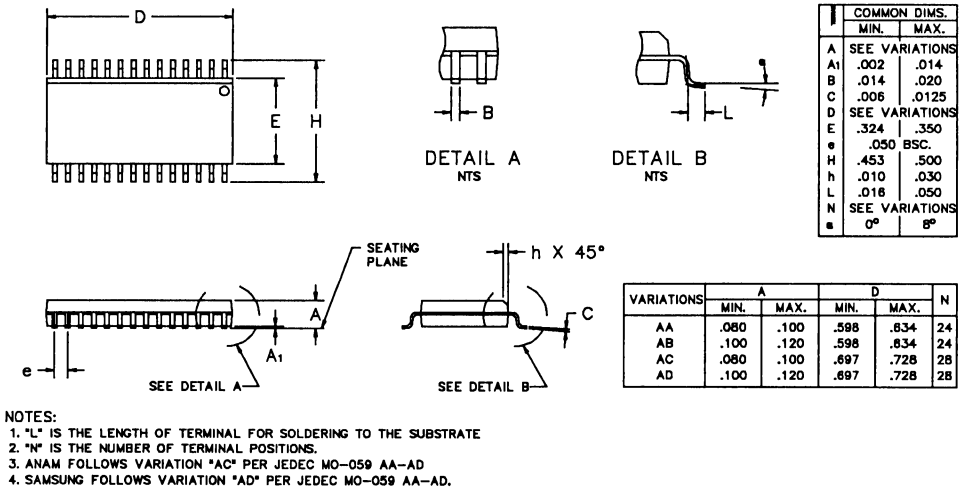


Figure 9-28 28-lead wide SOIC molded package

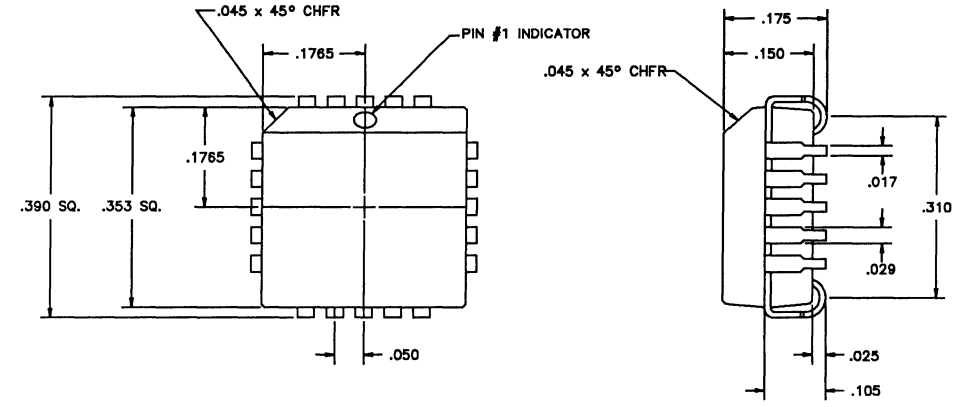


	COMMON DIMS.	
	MIN.	MAX.
A	SEE VARIATIONS	
A1	.002	.014
B	.014	.020
C	.006	.0125
D	SEE VARIATIONS	
E	.324	.350
e	.050 BSC.	
H	.453	.500
h	.010	.030
L	.016	.050
N	SEE VARIATIONS	
α	0°	8°

VARIATIONS	A		D		N
	MIN.	MAX.	MIN.	MAX.	
AA	.080	.100	.598	.634	24
AB	.100	.120	.598	.634	24
AC	.080	.100	.697	.728	28
AD	.100	.120	.697	.728	28

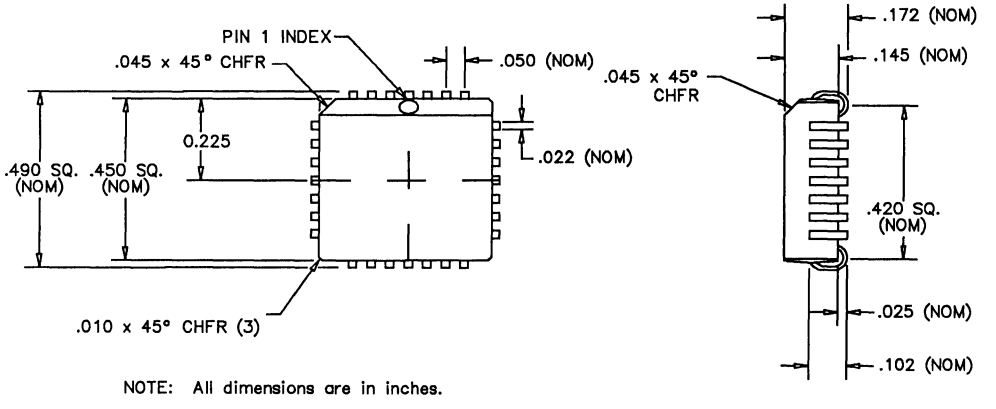
NOTES:
1. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO THE SUBSTRATE
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. ANAM FOLLOWS VARIATION "AC" PER JEDEC MO-059 AA-AD
4. SAMSUNG FOLLOWS VARIATION "AD" PER JEDEC MO-059 AA-AD.

Figure 9-29 28-lead plastic SOIC customer package outline (.330 body)



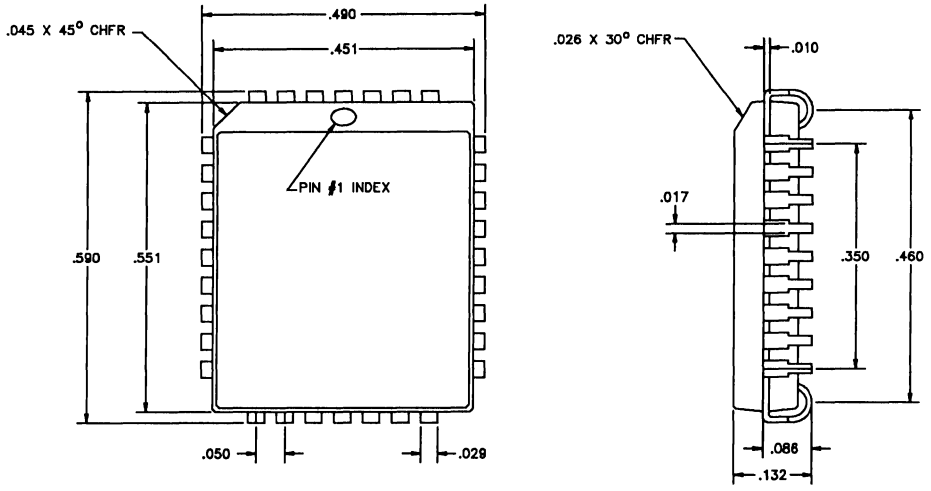
NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
2. ALL DIMENSIONS ARE SHOWN IN INCHES.

Figure 9-30 20-lead PLCC customer package outline



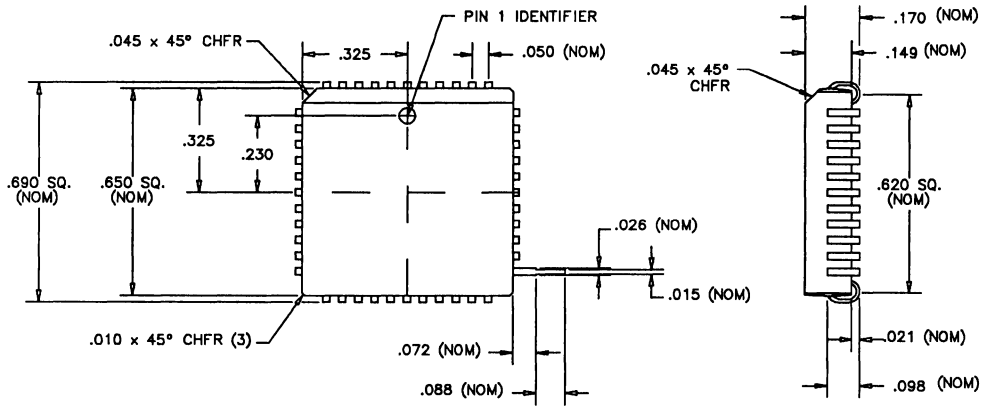
NOTE: All dimensions are in inches.

Figure 9-31 28-lead PLCC package



NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL.
2. ALL DIMENSIONS ARE SHOWN IN INCHES.

Figure 9-32 32-lead PLCC package



NOTE : All dimensions are in inches.

Figure 9-33 44-lead PLCC package

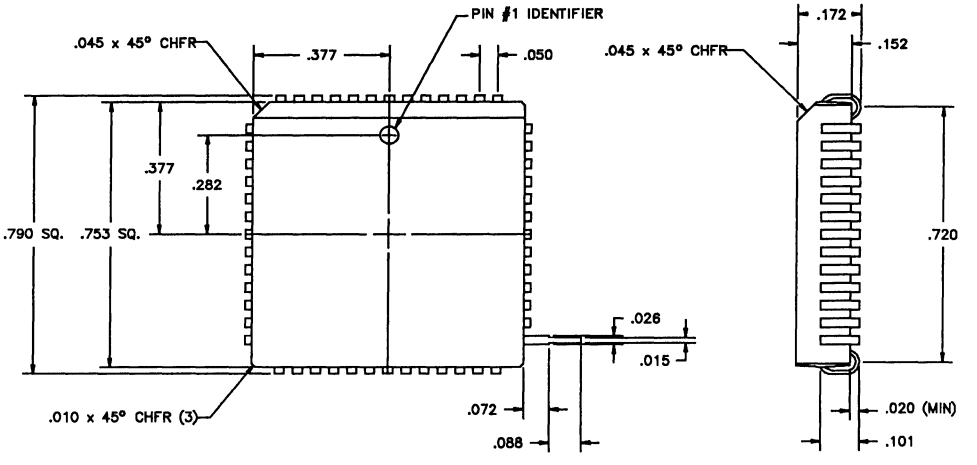


Figure 9-34 52-lead PLCC customer package outline

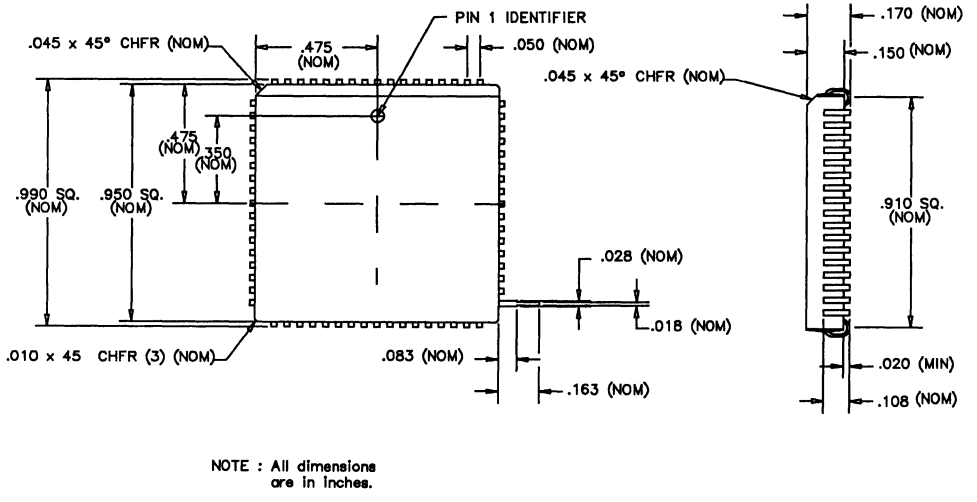


Figure 9-35 68-lead PLCC customer package outline

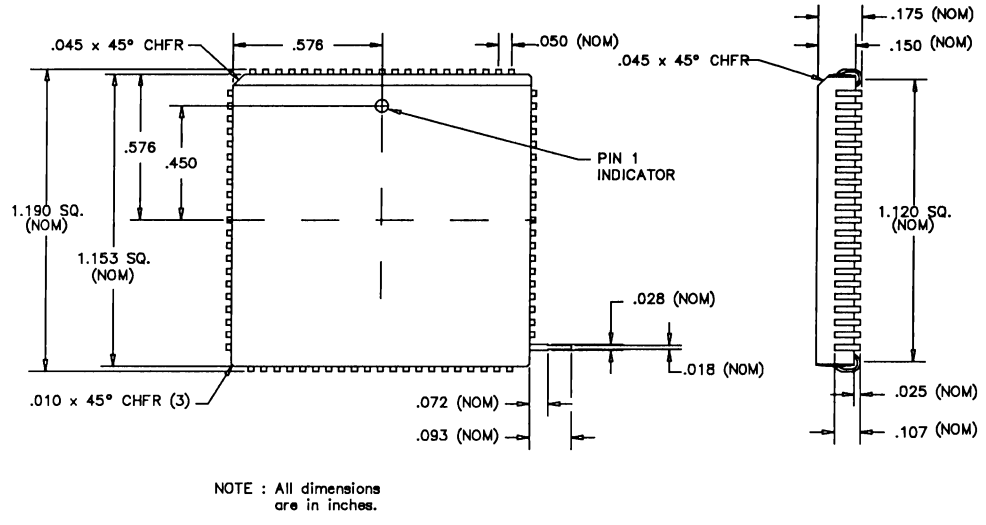
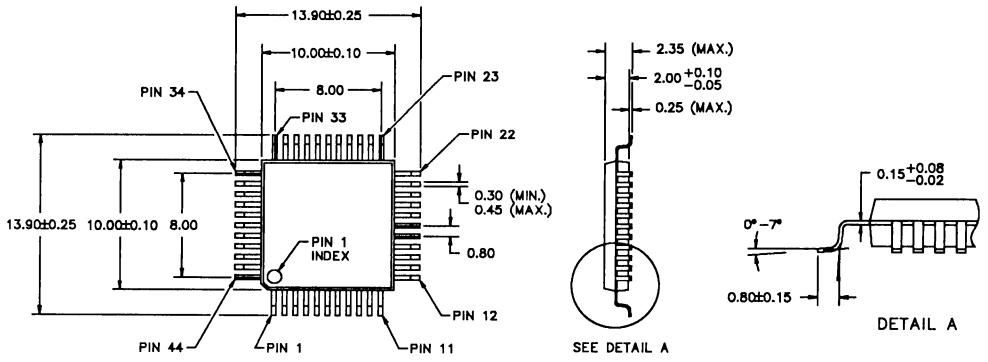
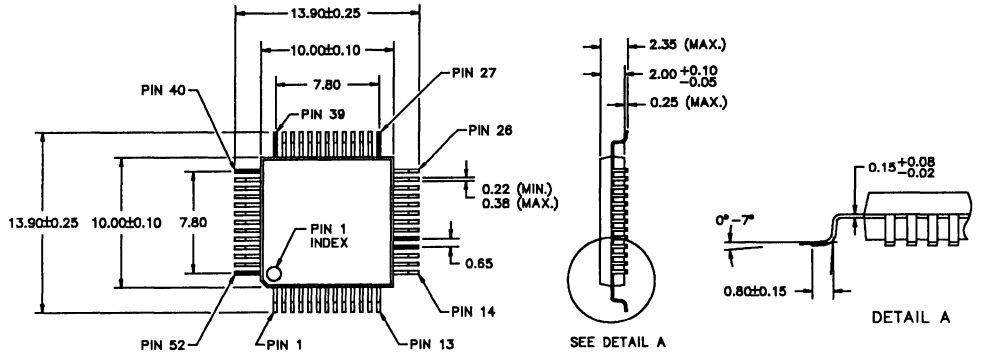


Figure 9-36 84-lead PLCC package



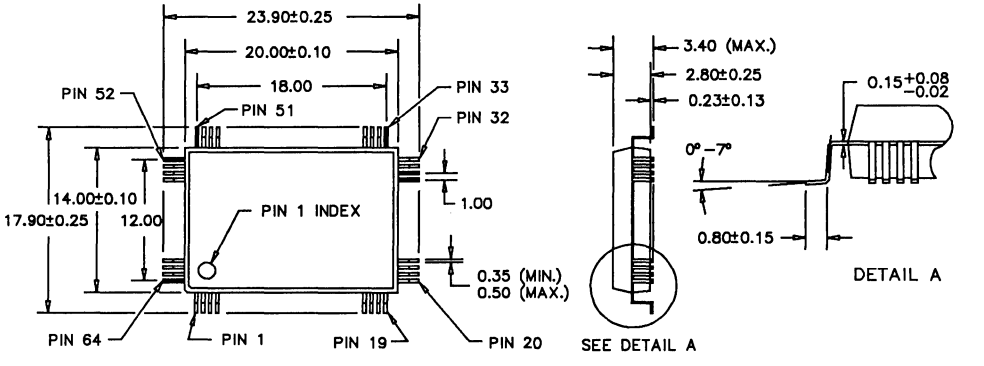
NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9-37 44-lead plastic metric flat pack customer package outline



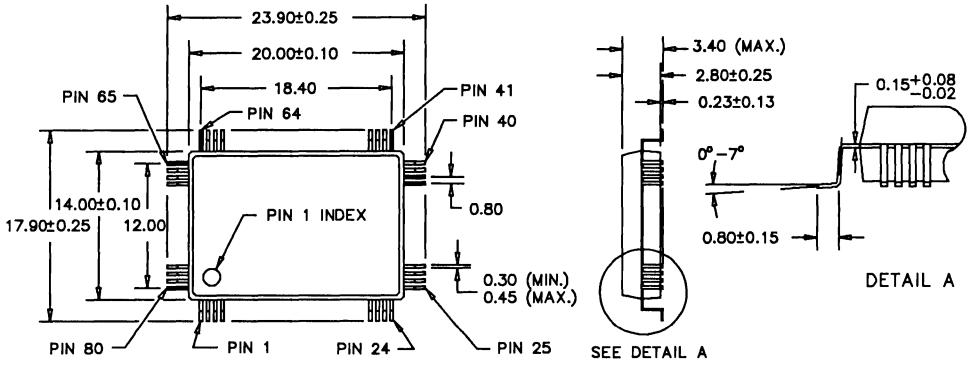
NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY

Figure 9-38 52-lead plastic metric flat pack customer package outline



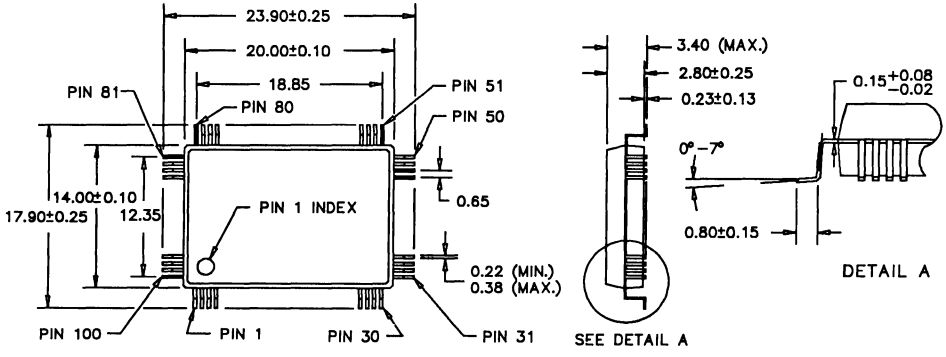
NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9-39 64-lead plastic metric flat pack customer package outline



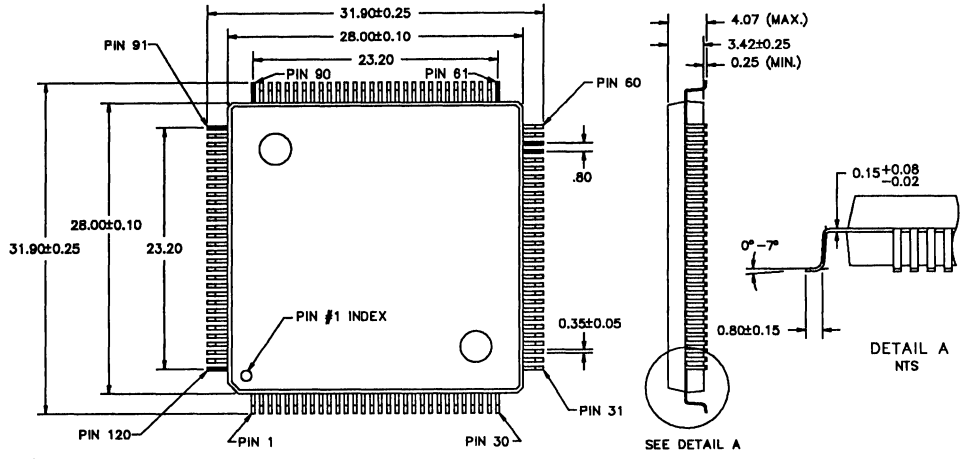
NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9-40 80-lead plastic metric flat pack customer package outline



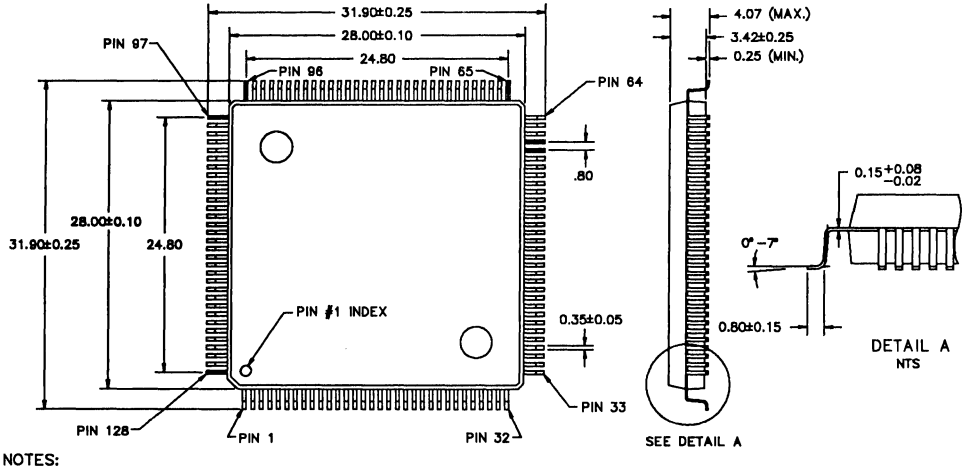
NOTES:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9-41 100-lead plastic metric flat pack customer package outline



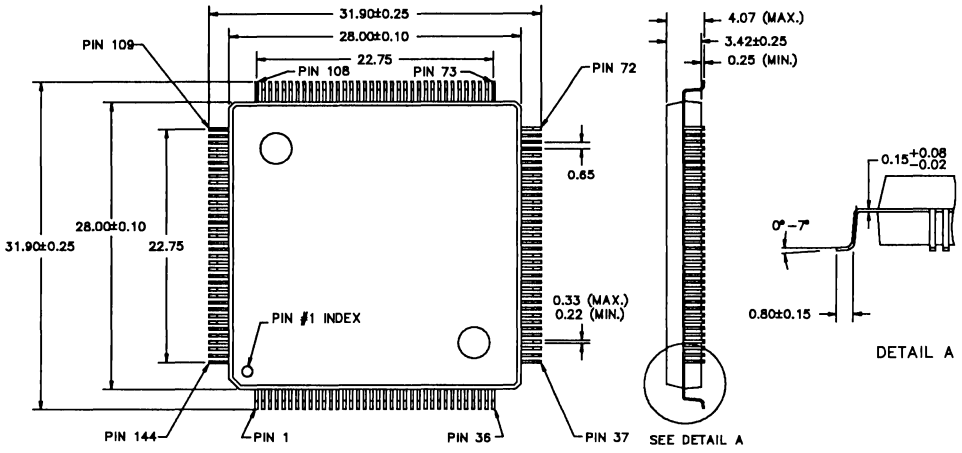
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9–42 120–lead plastic metric flat pack customer package outline



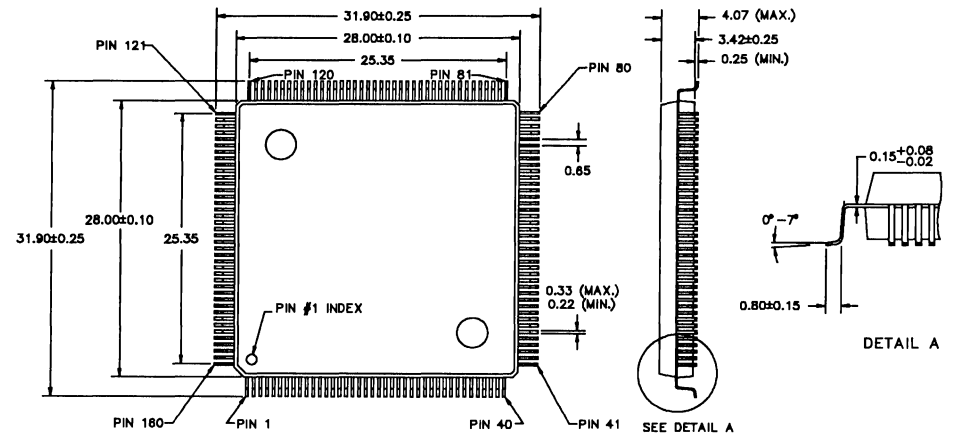
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MMILIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9–43 128–lead plastic metric flat pack customer package outline



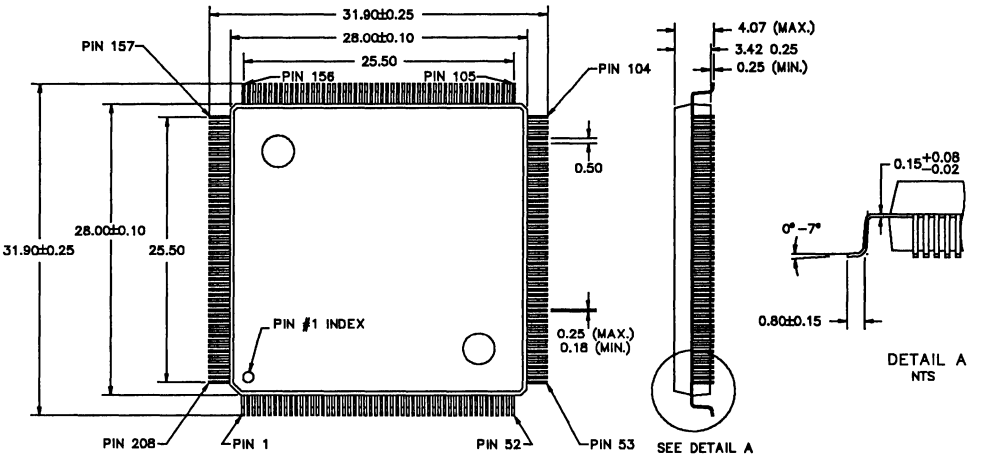
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9-44 144-lead plastic metric flat pack customer package outline



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMTERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

Figure 9-45 160-lead plastic metric flat pack customer package outline



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY

Figure 9–46 208–lead plastic metric flat pack customer package outline

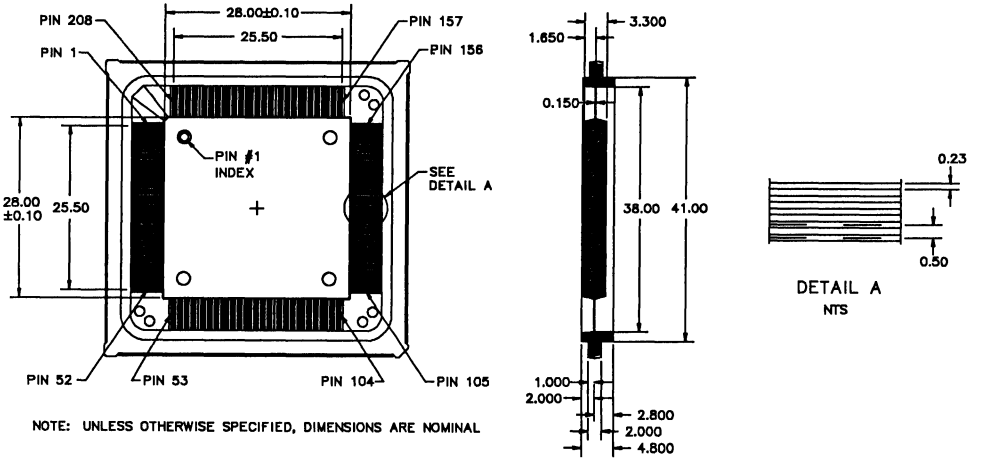


Figure 9–47 Molded carrier ring QFP, 208–lead customer package outline (1 of 4)

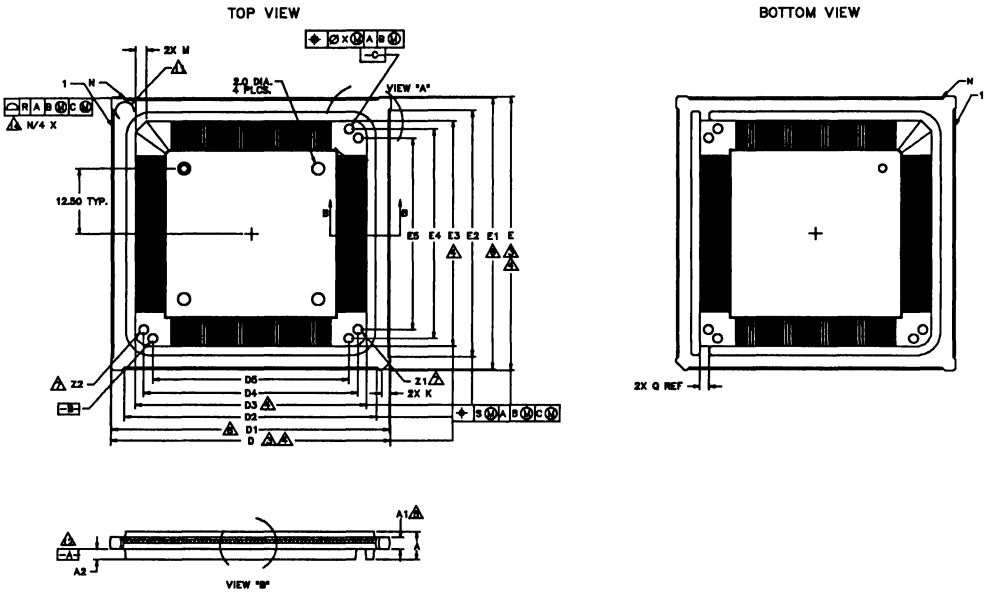


Figure 1–36 Molded carrier ring QFP, 208–lead customer package outline (2 of 4)

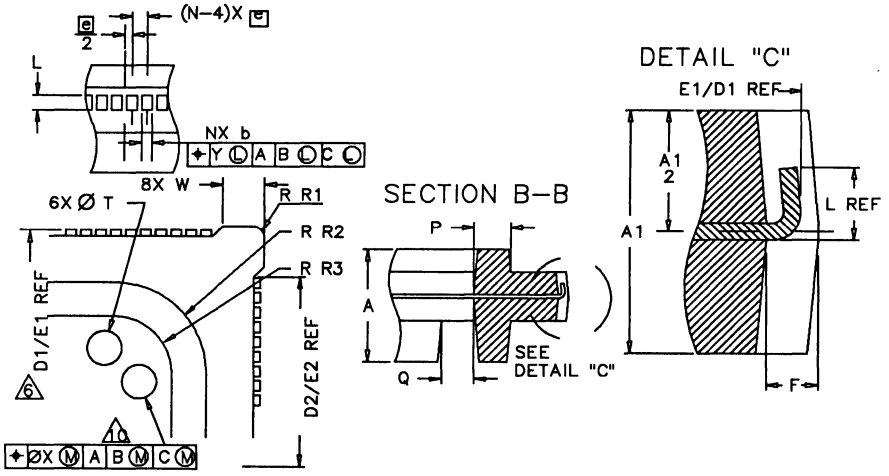


Figure 1–36 Molded carrier ring QFP, 208–lead customer package outline (3 of 4)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M– 1982.
2. CONTROLLING DIMENSION: MILLIMETER. CONVERTED INCH DIMENSIONS ARE SHOWN FOR REFERENCE ONLY AND ARE NOT NECESSARILY EXACT.
3. D AND E DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.2 mm PER SIDE.
4. D, D3, E AND E3 DIMENSIONS INCLUDE MOLD MISMATCH, AND ARE MEASURED AT THE PARTING LINE.
5. A1 DIMENSION CENTERED ABOUT CENTERLINE OF LEAD MATERIAL.
6. DIMENSIONS D1 AND E1 ARE FROM OUTSIDE EDGE TO OUTSIDE EDGE OF THE TEST POINTS.
7. THERE ARE SIX LOCATING HOLES IN THE RING. B AND C DATUM HOLES ARE TO BE USED FOR THE TRIM, FORM AND EXCISE OF THE MOLDED PACKAGE ONLY. HOLES Z1 AND Z2 ARE TO BE USED FOR ELECTRICAL TESTING ONLY.
8. LOCATION OF THE SECONDARY GATE (GATE FOR THE MOLDED PACKAGE INSIDE THE CARRIER RING) IS 180° WITH RESPECT TO THE CHAMFERED CORNER OF THE CARRIER RING. THERE ARE NO HOLES ON THIS CORNER OF THE CARRIER RING.
9. IN THE INTEREST OF MORE COMPLETE STANDARDIZATION, THE RINGS SHOULD NOT BE DEPOPULATED.
10. NON-DATUM HOLES ONLY.
11. THIS AREA RESERVED FOR VACUUM PICKUP ON EACH OF THE FOUR CORNERS OF THE RING AND MUST BE FLAT WITHIN .025 mm. NO EJECTOR PINS IN THIS AREA.
12. DATUM A SURFACE FOR SEATING IN SOCKET APPLICATIONS.
13. PIN 1 ORIENTATION WITH RESPECT TO CARRIER RING AS INDICATED
14. COPLANARITY APPLIES TO ALL FOUR TEST POINT ROWS.

	VARIATIONS						
	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	4.70	4.80	4.90	0.185	0.189	0.193	
A1	1.90	2.00	2.10	0.075	0.079	0.083	5
A2	1.70	1.80	1.90	0.067	0.071	0.075	
D	45.87	46.00	46.13	1.806	1.811	1.816	3,4
D1	—	48.7 BSC	—	—	1.799 BSC	—	6
D2	41.37	41.50	41.63	1.629	1.634	1.639	
D3	37.87	38.00	38.13	1.491	1.496	1.501	4
D4	—	35.2 BSC	—	—	1.386 BSC	—	
D5	—	32.2 BSC	—	—	1.268 BSC	—	
E	45.87	46.00	46.13	1.806	1.811	1.816	3,4
E1	—	48.7 BSC	—	—	1.799 BSC	—	6
E2	41.37	41.50	41.63	1.629	1.634	1.639	
E3	37.87	38.00	38.13	1.491	1.496	1.501	4
E4	—	35.2 BSC	—	—	1.386 BSC	—	
E5	—	32.2 BSC	—	—	1.268 BSC	—	
F	0.30	0.35	0.50	0.012	0.014	0.024	
K	1.27	1.40	1.53	0.050	0.055	0.060	
L	0.45	0.85	0.85	0.018	0.026	0.033	
M	1.30	1.80	2.30	0.051	0.071	0.091	
N		256			256		9
P	1.37	1.50	1.63	0.054	0.059	0.064	
Q	1.37	1.50	1.63	0.054	0.059	0.064	
R	—	0.25	—	—	0.010	—	
R1	0.40	0.50	0.60	0.016	0.020	0.024	
R2	3.50	4.00	4.50	0.138	0.157	0.177	
R3	2.00	2.50	3.00	0.079	0.098	0.118	
S	—	0.10	—	—	0.004	—	10
T	1.45	1.50	1.55	0.057	0.059	0.061	
W	1.77	1.90	2.03	0.070	0.075	0.080	
X	—	0.05	—	—	0.002	—	
Y	—	0.07	—	—	0.003	—	
b	0.40	0.45	0.50	0.016	0.018	0.020	
e	—	0.65 BSC	—	—	.0256 BSC	—	

Figure 1–36 Molded carrier ring QFP, 208–lead customer package outline (4 of 4)

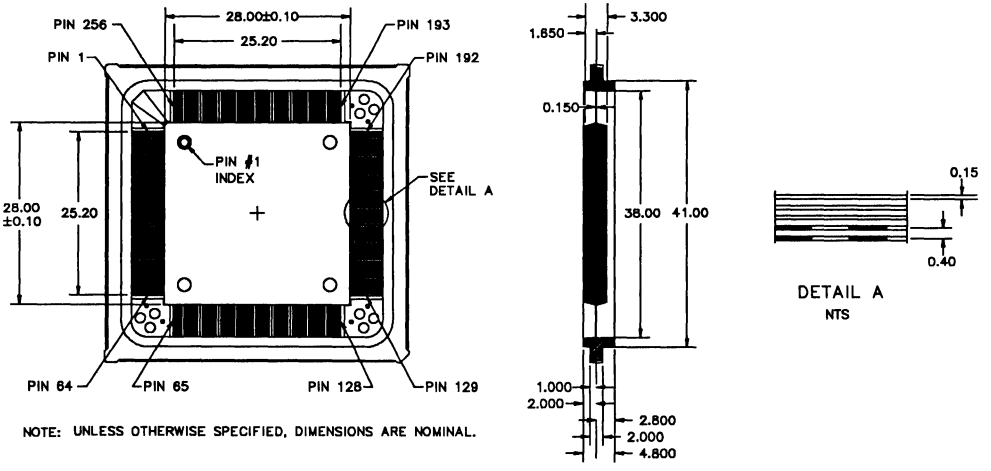


Figure 9–48 Molded carrier ring QFP, 256–lead customer package outline (1 of 4)

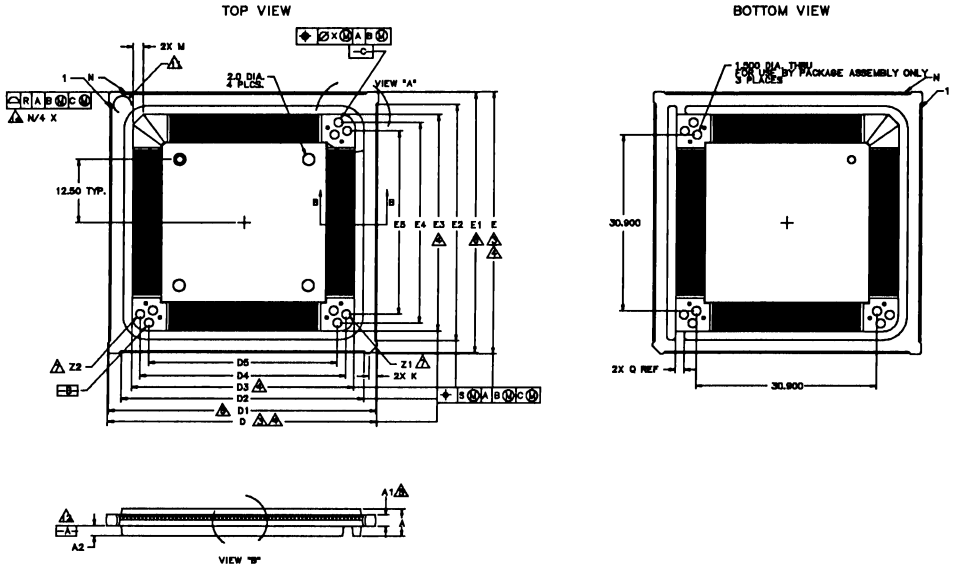


Figure 1–37 Molded carrier ring QFP, 256–lead customer package outline (2 of 4)

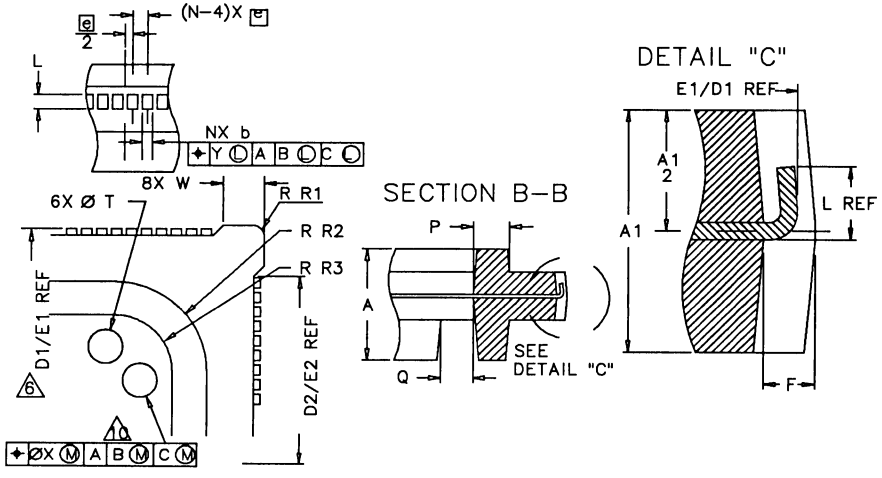


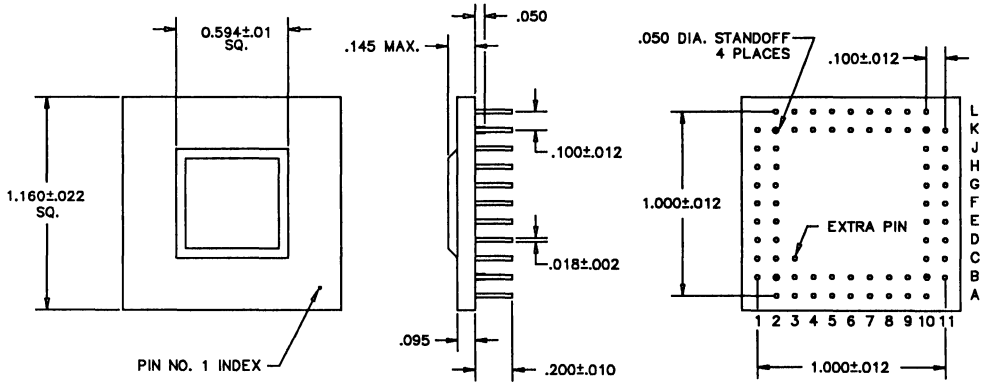
Figure 1–37 Molded carrier ring QFP, 256–lead customer package outline (3 of 4)

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M– 1982.
2. CONTROLLING DIMENSION: MILLIMETER. CONVERTED INCH DIMENSIONS ARE SHOWN FOR REFERENCE ONLY AND ARE NOT NECESSARILY EXACT.
3. D AND E DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.2 mm PER SIDE.
4. D, D3, E AND E3 DIMENSIONS INCLUDE MOLD MISMATCH, AND ARE MEASURED AT THE PARTING LINE.
5. A1 DIMENSION CENTERED ABOUT CENTERLINE OF LEAD MATERIAL.
6. DIMENSIONS D1 AND E1 ARE FROM OUTSIDE EDGE TO OUTSIDE EDGE OF THE TEST POINTS.
7. THERE ARE NINE LOCATING HOLES IN THE RING. B AND C DATUM HOLES ARE TO BE USED FOR THE TRIM, FORM AND EXCISE OF THE MOLDED PACKAGE ONLY. HOLES Z1 AND Z2 ARE TO BE USED FOR ELECTRICAL TESTING ONLY.
8. LOCATION OF THE SECONDARY GATE(GATE FOR THE MOLDED PACKAGE INSIDE THE CARRIER RING) IS 180° WITH RESPECT TO THE CHAMFERED CORNER OF THE CARRIER RING. THERE ARE NO HOLES ON THIS CORNER OF THE CARRIER RING.
9. IN THE INTEREST OF MORE COMPLETE STANDARDIZATION, THE RINGS SHOULD NOT BE DEPOPULATED.
10. NON–DATUM HOLES ONLY.
11. THIS AREA RESERVED FOR VACUUM PICKUP ON EACH OF THE FOUR CORNERS OF THE RING AND MUST BE FLAT WITHIN .025 mm. NO EJECTOR PINS IN THIS AREA.
12. DATUM A SURFACE FOR SEATING IN SOCKET APPLICATIONS.
13. PIN 1 ORIENTATION WITH RESPECT TO CARRIER RING AS INDICATED.
14. COPLANARITY APPLIES TO ALL FOUR TEST POINT ROWS.

	VARIATIONS						
	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	4.70	4.80	4.90	0.185	0.189	0.193	
A1	1.90	2.00	2.10	0.075	0.079	0.083	5
A2	1.70	1.80	1.90	0.067	0.071	0.075	
D	45.87	46.00	46.13	1.806	1.811	1.816	3,4
D1	—	45.7 BSC	—	—	1.799 BSC	—	6
D2	41.37	41.50	41.63	1.629	1.634	1.639	
D3	37.87	38.00	38.13	1.491	1.496	1.501	4
D4	—	35.2 BSC	—	—	1.386 BSC	—	
D5	—	32.2 BSC	—	—	1.268 BSC	—	
E	45.87	46.00	46.13	1.806	1.811	1.816	3,4
E1	—	45.7 BSC	—	—	1.799 BSC	—	6
E2	41.37	41.50	41.63	1.629	1.634	1.639	
E3	37.87	38.00	38.13	1.491	1.496	1.501	4
E4	—	35.2 BSC	—	—	1.386 BSC	—	
E5	—	32.2 BSC	—	—	1.268 BSC	—	
F	0.30	0.35	0.40	0.012	0.014	0.024	
K	1.27	1.40	1.53	0.050	0.055	0.060	
L	0.45	0.65	0.85	0.018	0.026	0.033	
M	1.30	1.80	2.30	0.051	0.071	0.091	
N		256			256		9
P	1.37	1.50	1.63	0.054	0.059	0.064	
Q	1.37	1.50	1.63	0.054	0.059	0.064	
R	—	0.25	—	—	0.010	—	
R1	0.40	0.50	0.60	0.016	0.020	0.024	
R2	3.80	4.00	4.50	0.138	0.157	0.177	
R3	2.00	2.50	3.00	0.079	0.098	0.118	
S	—	0.10	—	—	0.004	—	10
T	1.45	1.50	1.55	0.057	0.059	0.061	
W	1.77	1.90	2.03	0.070	0.075	0.080	
X	—	0.05	—	—	0.002	—	
Y	—	0.07	—	—	0.003	—	
b	0.40	0.45	0.50	0.016	0.018	0.020	
e	—	0.65 BSC	—	—	.0256 BSC	—	

Figure 1–37 Molded carrier ring QFP, 256–lead customer package outline (4 of 4)



NOTE : All dimensions are in inches.

Figure 9–49 68–lead plastic pin grid array package

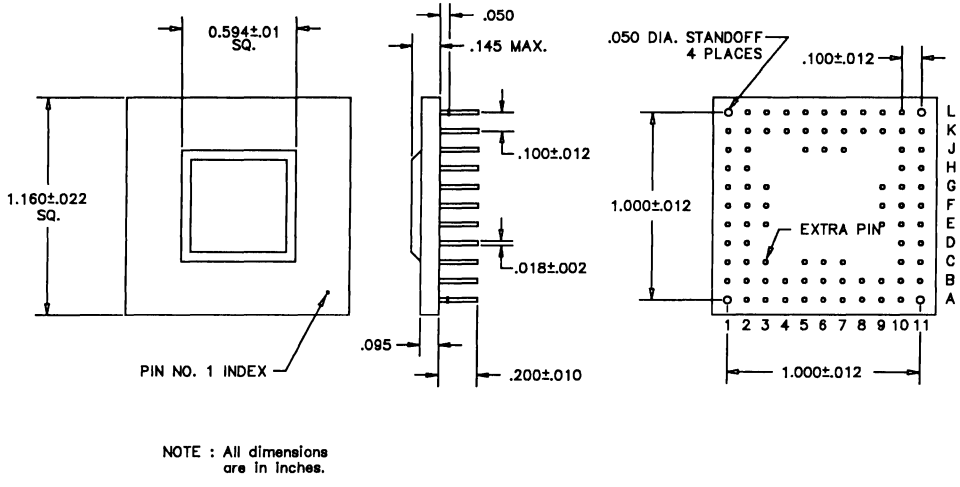


Figure 9-50 84-lead plastic pin grid array customer package outline

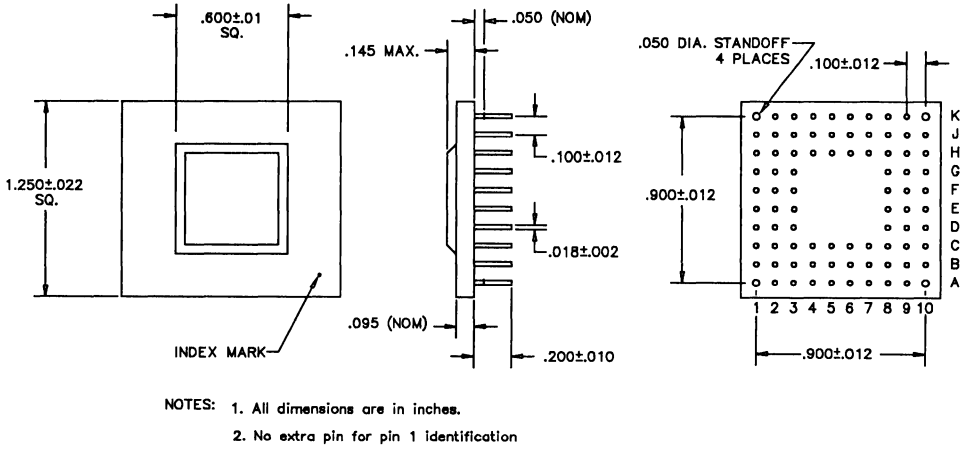


Figure 9-51 84-lead plastic pin grid array package

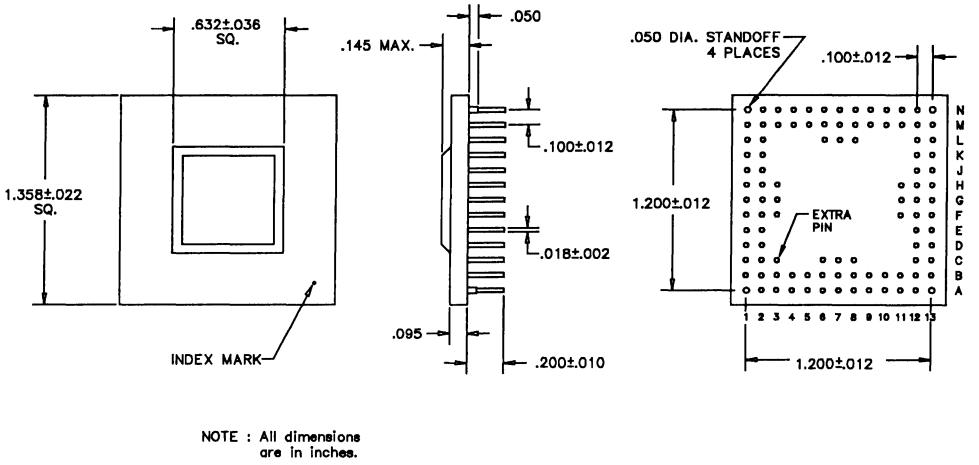


Figure 9-52 100-lead plastic pin grid array package

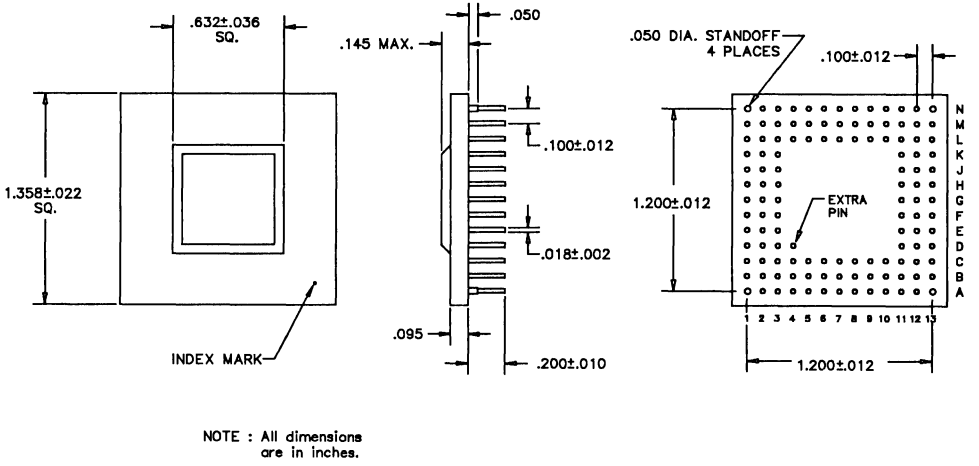


Figure 9-53 120-lead plastic pin grid array package

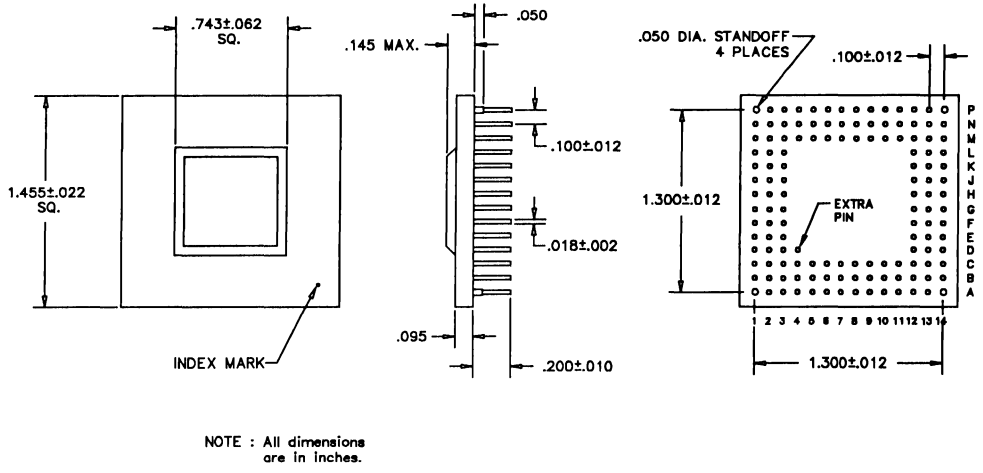


Figure 9–54 132–lead plastic pin grid array package

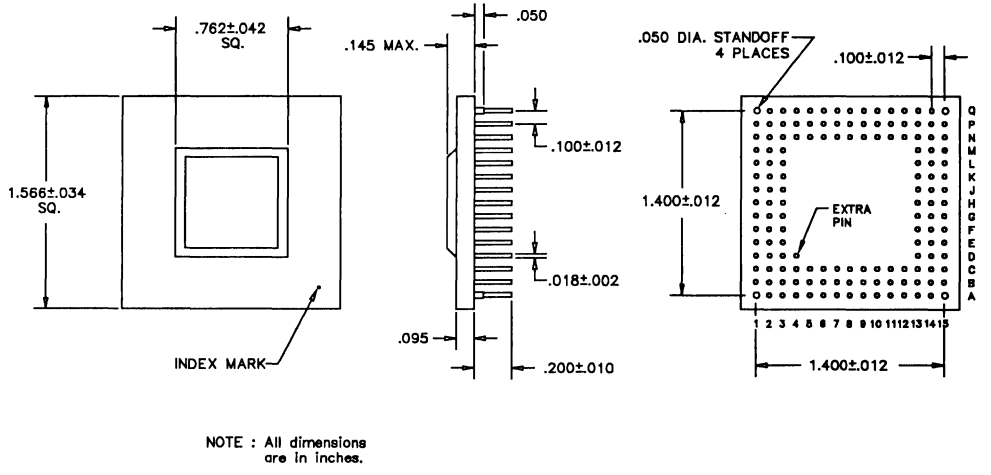


Figure 9–55 144–lead plastic pin grid array package

Thermal Considerations for Integrated Circuit Packaging

Purpose

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long term operating life of an IC. Some of the variables affecting T_J are controlled by the user and the environment in which the device is used. Management of thermal characteristics is also a concern because as IC packages get smaller, the thermal energy is concentrated more densely on the printed circuit board (PCB). For these reasons, the designer and manufacturer of the device must be more aware of all the variables affecting T_J. The purpose of this document is to define guidelines for estimating the thermal performance of standard plastic packages.

Definitions

Thermal Resistance (θ_{JA})

The ability of the package to conduct heat from the chip to the environment is expressed in terms of thermal resistance, as °C/Watt. The term normally used is Theta JA(θ_{JA}). θ_{JA} represents the total resistance to heat flow from the chip to ambient.

Junction Temperature (T_J)

When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated using the following:

$$T_J = (P_D x \theta_{JA}) + T_A$$

where:
T_J = Actual Junction Temperature (°C)
P_D = Power Dissipation (Watts)
$(V_{CC}$ Max.)x(I_{CC} Max.)
θ_{JA} = Thermal Resistance – Junction to Ambient (°C/W)
T_A = Ambient Temperature (°C)

Example:

A device is operated at +55°C with a power dissipation of 145mW and a package θ_{JA} of 100°C/W.

$T_J = (0.145x100)+55$
$T_J = (14.5)+55$
$T_J = 69.5°C$

Power Dissipation (P_D)

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_D(T_A) = (T_J(Max.) - T_A)/\theta_{JA}$$

where:
$P_D(T_A)$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and the supply currents at the worst case operating condition. P_D is measured in Watts.
T_J(Max.) = Maximum operating junction temperature.
T_A = Maximum desired operating ambient temperature.
θ_{JA} = Typical thermal resistance–junction to ambient.

Example:

The maximum allowable power dissipation for a device with a maximum junction temperature T_J = 150°C and maximum temperature T_A = 70°C. θ_{JA} = 65°C/W.

$P_D(70°C) = (150°C - 70°C)/(65°C/W)$
$P_D(70°C) = 80°C/(65°C/W)$
$P_D(70°C) = 1.23W$

Package Considerations

There are several factors which affect the thermal resistance of any IC package. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and other variables such as the die size and die attach methods. Because of these differing variables, each plastic package type has been characterized for its particular θ_{JA}. In this report are tables of θ_{JA} values for each of these plastic packages. To estimate the θ_{JA} value for your IC's specific package leadframe and die size combination, you can plot a graph of the slopes for both the die size and the pad size with the measured values given on the tables. The following example outlines how to find a θ_{JA} value from your own graph.

Example:

Find the θ_{JA} value for a 68 PLCC with a pad size of 260 sq. mils and a die size of 170 sq. mils.

Find the appropriate table of θ_{JA} values.

Package	Pad Size	Die Size	θ_{JA}
68 PLCC	320x320	150x150	39.97
	320x320	225x225	39.04
	410x410	225x225	34.35

Using graph paper, make a graph with the θ_{JA} on the X axis and scale of 0–500 mils on the Y axis.

Plot the two θ_{JA} values given for differing pad sizes and the same die size.

Pad Size	θ_{JA}
320x320	39.04
410x410	34.35

Use only the 320 mil and 410 mil pad size values for the Y axis. For a quick approximation the θ_{JA} values may be rounded off. Draw a line between these two points and label it pad size.

Plot the two θ_{JA} values given for differing die sizes and the same pad size.

Die Size	θ_{JA}
150x150	39.97
225x225	39.04

Use only the 150 mil and 225 mil die size values for the Y axis. Draw a line between these two points and label it die size . (The pad size and die size can be plotted on the same scale because the same units of measure are used. The points for the die size should always be below the points for the pad size.)

The slope of the lines plotted for the pad size and the die size should not be the same. This is due to the difference in thermal conductivity between the silicon and the leadframe material.

To find the coordinate for a 260 pad size follow the line labeled pad size until it intersects the 260 mil point on the Y axis. Mark a point here and label it "PS".

To find the coordinate for a 170 mil die size draw a parallel line to the line labeled die size and begin drawing downward from the point "PS" until the line intersects the 170 mil point on the Y axis. Mark a point here and label it "DS".

The θ_{JA} value on the X axis directly below the point labeled "DS," 43.4°C/W, is the approximate thermal resistance for a 68 pin PLCC package with a pad size of 260 sq. mils and a die size of 170 sq. mils.

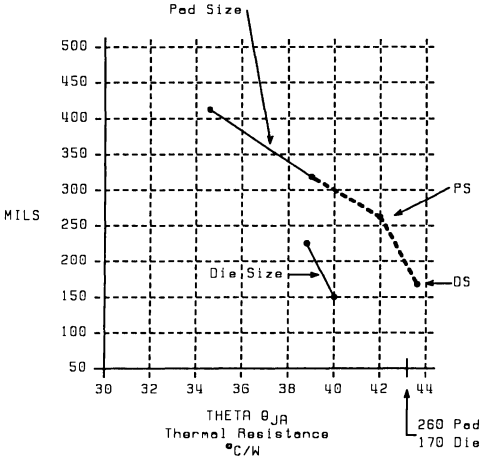


Figure 9-56 Example of graph: 68 PLCC

Thermal Impedance Measurements

The following table shows the θ_{JA} measurements for each pin count using various pad and die sizes.

Test Conditions:
Air: Ambient (25°C)
Power: 1 Watt

Package	Pad Size (mils)	Die Size (mils)	θ_{JA} (°C/W)
16 SOIC	110x110	75x75	95.24
	160x200	75x75	83.46*
	160x200	150x150	87.56*
24 SOIC	120x120	75x75	85.07
	170x220	75x75	76.29
	170x220	150x150	72.93
28 SOIC	150x150	75x75	77.87
	182x300	75x75	71.21
	182x300	150x150	67.69

(*These numbers are based upon actual measurements and not out of order.)

SOIC Package Construction:
- Alloy-42 Leadframe
- 84-1 LMI Epoxy
- Nitto MP150SG Molding Compound

Test Conditions:
Air: Ambient (25°C)
Power: 1 Watt

Package	Pad Size (mils)	Die Size (mils)	θ_{JA} (°C/W)
28 PLCC	180x180	150x150	53.86
	260x260	150x150	52.38
	260x260	225x225	51.78
44 PLCC	200x200	150x150	45.97
	370x370	150x150	41.81
	370x370	225x225	40.38
52 PLCC	250x250	150x150	40.77
	250x250	225x225	39.35
	310x310	225x225	37.30
68 PLCC	320x320	150x150	39.97
	320x320	225x225	39.04
	410x410	225x225	34.35
84 PLCC	320x320	150x150	33.34
	320x320	225x225	31.46
	400x400	225x225	31.13

PLCC Package Construction:
- Copper Leadframe
- 84-1 LMI Epoxy
- Nitto MP150SG Molding Compound

Test Conditions:
Air: Ambient (25°C)
Power: 1 Watt

Package	Pad Size (mils)	Die Size (mils)	θ_{JA} (°C/W)
64 QFP	236x236	150x150	85.04
	236x236	225x225	74.89
	315x315	225x225	67.82
80 QFP	255x255	150x150	78.31
	255x255	225x225	70.95
	370x370	225x225	62.91
100 QFP	255x255	150x150	73.41
	255x255	225x225	68.23
	360x360	225x225	63.86
120 QFP	330x330	225x225	58.98
	330x330	300x300	52.70
	405x405	300x300	50.43
128 QFP	340x340	300x300	54.29
	430x430	300x300	52.26
	430x430	375x375	49.22
144 QFP	355x355	300x300	51.91
	420x420	300x300	50.42
	420x420	375x375	49.38
160 QFP	400x400	300x300	49.89
	400x400	375x375	46.55
	430x430	300x300	50.22
208 QFP	400x400	300x300	49.78
	433x433	300x300	48.98
	433x433	375x375	47.60

QFP Package Construction:
- Alloy-42 Leadframe
- 84-1 LMI Epoxy
- Sumitomo 6300H Molding Compound

Test Conditions:
Air: Ambient (25°C)
Power: 1 Watt

Pin Count	Die Size (mils)	Pad Size (mils)	θ_{JA} (°C/W)
68 PPGA	300x300	325x325	51
	300x300	450x450	45*
	375x375	450x450	46*
84 PPGA	225x225	300x300	60*
	225x225	360x360	64*
	300x300	360x360	59
100 PPGA	300x300	350x350	47
	300x300	450x450	43
	375x375	450x450	42
120 PPGA	300x300	325x325	51
	300x300	450x450	47
	375x375	450x450	41
132 PPGA	300x300	394x394	43*
	300x300	450x450	45*
	375x375	450x450	42
144 PPGA	225x225	400x400	
	225x225	472x472	41
	300x300	472x472	37
180 PPGA	300x300	450x450	48.02
(Multilayer)	375x375	450x450	44.31

PPGA Package Construction:
- High Tg Glass Epoxy Board
- Metallized Cavity
- 84-1 LMI Epoxy Die Attach
- Silicone Gel Die Coat
- Hysol FP4323 Epoxy Lid Seal
- Anodized Aluminum Lid

* The test measurements have a tolerance of ±2°C. Because of this tolerance and the close proximity of the readings, some of the test measurements may appear in reverse order.

Determining Power Pad Requirements

The number of power pads required for your design will be affected by the following variables: the power consumption of the core logic, the total DC load (this includes the DC current of internal cells and the DC load that the pads must drive), and the number of simultaneous switching outputs.

This application note is intended to provide guidelines for V_{DD}/V_{SS} pin selection and placement as well as provide insight into those factors which are most likely to influence the noise immunity of an ASIC design. Many factors on- and off-chip influence the noise immunity of ASIC input buffers. Understanding NCR's V_{DD}/V_{SS} pin requirements requires the ASIC designer to look at his circuit and at the environment in which it operates.

General Guidelines

NCR standard cell and gate array I/O buffers are designed for high output drive capabilities. These higher drive buffers can generate voltage spikes on the power busses when driving large capacitive loads. When a number of outputs switch simultaneously, (within 5 ns) the peak current on a V_{SS} or V_{DD} pad may be sufficient to cause a voltage spike on an internal V_{SS} or V_{DD} power bus. This may in turn affect the noise immunity of the input buffers. The primary factor contributing to the internal power bus spikes is the inductance of the V_{DD}/V_{SS} pins. Higher pin count packages have larger lead inductances. Because of this, more V_{DD}/V_{SS} pins will be required to support simultaneously switching outputs in higher pin count packages.

The effect of these simultaneous switching outputs can be lessened by increasing the number of V_{DD}/V_{SS} pads, by separating the V_{DD}/V_{SS} pads that supply power for the core logic from the V_{DD}/V_{SS} pads that supply power for the input and output pad cells, and by using Schmitt trigger inputs for sensitive asynchronous signals.

Although voltage spikes can occur on both power and ground busses, TTL inputs are much more sensitive to ground bounce due to their low trip point. For this reason, NCR recommends additional ground pads for designs with TTL level inputs.

In order to minimize the effect of ground bounce on your design, NCR offers the following recommendations:

1. Use as many V_{DD}/V_{SS} pins as possible. A formula for calculating the minimum number of V_{DD}/V_{SS} pins is given later in this application note. If you have extra package pins, they should be used as additional V_{DD}/V_{SS} pins.

2. Use separate V_{DD}/V_{SS} pins for the core logic and pad cells. The impact of noise caused by output switching can be minimized by separating the V_{DD}/V_{SS} pins that are used to supply power to the noisy pad cells from the V_{DD}/V_{SS} pins that are used to supply power to the core logic cells which include the noise-sensitive input buffers. NCR will work with you to provide separation of pad V_{DD}/V_{SS} pins and internal core V_{DD}/V_{SS} power pins during layout to improve noise isolation on-chip.

3. Place pad cell V_{DD}/V_{SS} pins close to simultaneously switching outputs to minimize ground bounce and improve noise immunity. V_{DD}/V_{SS} pins should be evenly distributed throughout the simultaneously switching output pins weighted by the number of total simultaneously switching output pins times the current drive per pin. Placing pad cell V_{DD}/V_{SS} pins close to simultaneously switching outputs allows high drive busses to be completely isolated from the rest of the chip. Place core V_{DD}/V_{SS} pins near the center of the package sides.

4. Minimize the simultaneous switching output current by slew rate limiting the simultaneously switching outputs. NCR recommends that you do this by using smaller buffers to drive the output pads. For more information on this, see the Buffer Selection for Pad Cells and Slew Rate Control application notes.

5. Minimize the simultaneously switching output current by adding skew between outputs on busses that switch simultaneously. Any delay will help, but NCR recommends 5 ns separation between switching outputs.

6. Place asynchronous inputs such as clocks, presets, clears, etc., away from simultaneously switching outputs and oscillator cells and near a core V_{SS}. Use Schmitt trigger inputs for asynchronous inputs if they meet your timing requirements.

7. Use Schmitt trigger buffers on I/O cells with pullup or pulldowns cells (PPUs or PPDs) connected.

8. Place pad cell V_{DD}/V_{SS} pins near high frequency oscillator pins.

Determining the Number of VDD/VSS Pins Required

To help determine the number of power pins required for a given design, use the following guidelines. Any deviations from these guidelines should be reviewed by NCR before beginning your design.

There are three factors that are used to determine the number of V_{DD}/V_{SS} pins required by a design. These are the DC current requirements, the core switching requirements, and the simultaneously switching output requirements.

Analog power requirements are considered separately since analog typically requires separate isolated V_{DD}/V_{SS} pins.

The number of power and ground pins required for a given device is the sum of the power requirements from the following three calculations, plus the requirements for any analog circuitry.

Calculation #1 (DC Power Requirements)

Sum all the DC power requirements for the design including:

- DC loads on the output pads
- Pullup and pulldown currents
- DC power draw from cells (POR, SRAMGEN)

All CMOS simple digital cells (AND, OR DFF, etc.) consume an insignificant amount of DC current compared to other cells and do not affect this calculation. You will need one V_{DD}/V_{SS} pair for every 100 mA of DC current.

$$V_{DD}/V_{SS}(DC) = \frac{\text{Total DC current}}{100\ mA}$$

Calculation #2 (Core Switching Requirements)

Break your design into blocks of logic based upon switching frequency. Use the appropriate table based on your technology to determine the number of V_{DD}/V_{SS} pins required to support core switching of each of the blocks. Then total the number of V_{DD}/V_{SS} pins required to support the core switching of all the blocks.

VS1500 and VGX1500					
Internal Gates	**0–10 MHz**	**>10–20 MHz**	**>20–30 MHz**	**>30 –40MHz**	**>40–50 MHz**
0 – 2,500	1	1	2	2	2
2,501 – 5,000	1	2	3	3	4
5,001 – 10,000	2	3	5	6	8
10,001 – 15,000	3	5	7	9	12
15,001 – 20,000	3	6	9	12	15
20,001 – 25,000	4	8	12	15	19
25,001 – 30,000	5	9	14	18	23

VS700 and VGX700					
Internal Gates	**0–10 MHz**	**>10–20 MHz**	**>20–30 MHz**	**>30 –40MHz**	**>40–50 MHz**
0 – 2,500	1	1	1	1	1
2,501 – 5,000	1	1	1	2	2
5,001 – 10,000	1	2	2	3	3
10,001 – 15,000	1	2	3	4	5
15,001 – 20,000	2	3	4	5	6
20,001 – 25,000	2	3	5	6	8
25,001 – 30,000	2	4	6	8	9

TABLE 9–7 Number of VDD/VSS pairs required

V_{DD}/V_{SS}(core) = Total V_{DD}/V_{SS} for each block of logic at a given operating frequency.

Calculation #3 (Simultaneously Switching Output Requirements)

Total the number of simultaneous switching outputs (SSOs) of each pad type for a given drive strength for your design (i.e., 16–2mA, 8–16mA). Refer to Table 9–8 for the given technology and determine the maximum number of SSOs per ground pin for each type of output in your design. Divide this number into the number of SSOs for each pad of a given drive strength in your design to determine the number of V_{SS} pins per output cell type of your design. Now sum these V_{SS} pins per output cell type to determine the total number of V_{SS} pins required for all your SSOs.

V_{SS}(SSO) = Total V_{SS} for each SSO cell type for a given drive strength

VS1500 and VGX1500							
Package Pins							
DIPS	**PLCCs & QFPs**	**2mA**	**4mA**	**8mA**	**16mA**	**24mA**	**48mA**
0–23	0–52	18	15	9	4	3	2
24–39	53–100	12	8	6	3	3	2
40–48	101–208	8	6	4	3	2	1

VS700 and VGX700							
Package Pins							
DIPS	**PLCCs & QFPs**	**2mA**	**4mA**	**8mA**	**16mA**	**24mA**	**48mA**
0–23	0–52	12	10	6	3	3	2
24–39	53–100	8	6	5	3	2	1
40–48	101–208	6	5	3	2	2	1

TABLE 9–8 Number of simultaneously switching outputs per ground pin

If your design contains any TTL level input cells, then calculate the number of required V_{DD} pins to support the SSOs as follows: V_{DD}(SSO) = V_{SS}(SSO)/3

If your design contains only CMOS and/or Schmitt input cells, then calculate the number of required V_{DD} pins to support the SSOs as follows: V_{DD}(SSO) = V_{SS}(SSO)/2

Calculation #4 (Determine Power Pad Requirements)

Calculate the number of power and ground pins required for your design by totaling the required V_{DD}/V_{SS} pins for DC, core switching, and SSO determined in the previous three calculations.

$$V_{DD}/V_{SS}(\text{total}) = V_{DD}/V_{SS}(\text{DC}) + V_{DD}/V_{SS}(\text{core}) + V_{DD}/V_{SS}(\text{SSO})$$

Example:

Suppose your VS700 design contains 30,000 gates and has a 40 MHz input clock. It has 16–8 mA and 4–16 mA output pads that can switch simultaneously and is packaged in an 80-pin QFP. All inputs are TTL level. The design has no analog or cells that have significant DC power requirements. Ten percent of the logic runs at the maximum clock frequency (40 MHz). The input clock is divided by 2 and clocks a third of the logic. The remainder of the logic runs at 10 MHz or less.

Since there are no cells that draw DC current, you can skip Calculation #1.

Use Calculation #2 to calculate the number of V_{DD} and V_{SS} pins required to support the switching of the core cells. This design would be broken into three blocks and the number of V_{DD}/V_{SS} pins required to support each block would be summed as follows:

	Gates	Frequency	V_{DD}/V_{SS} Pins
Block #1	3,000	40 MHz	2
Block #2	10,000	20 MHz	2
Block #3	17,000	0–10 MHz	2
Total V_{DD}/V_{SS} pins for core switching requirements			6

Use Calculation #3 to calculate the number of V_{DD} and V_{SS} pins required to support the simultaneously switching output requirements using Table 9–8.

Output Pad Drive	# of SSOs	# of SSOs/V_{SS} Pin	# of V_{SS} pads required
8 mA	16	5	16/5 = 4
16 mA	4	3	4/3 = 2
Total V_{SS} pins for simultaneously switching output requirements			6

The number of V_{DD} pins required for simultaneously switching output requirements is 6/3 = 2.

The total number of V_{DD} and V_{SS} pins required for the design is the sum of calculations 1–3.

Total V_{DD} pin requirements = 0 + 6 + 2 = 8
Total V_{SS} pin requirements = 0 + 6 + 6 = 12

Estimating Power Consumption

The amount of power consumed by a CMOS device is dependent upon the frequencies and load capacitances associated with each design. Because these factors vary greatly across designs, it is difficult to derive an accurate rule of thumb for estimating power consumption in CMOS devices.

An approximation for the power consumption for any design may be calculated by using the following equation.

$$P = Pd + Ps + Po$$
$$= PF * \{\Sigma(n * fb)\} + Iq * V_{DD} + \Sigma(C_L * V_{DD}^2 * fo)$$

where

- P = total power consumption
- Pd = dynamic power consumption
- Ps = static power consumption
- Po = dynamic power consumed by output pads
- PF = power factor for a given technology (see Table 9–9)
- n = number of gates in a logic block operating at frequency f
- fb = toggle frequency (clock or data rate) for block of logic
- Iq = total quiescent current, including PPU and PPD cells
- V_{DD} = power supply voltage
- C_L = load capacitance on output pads
- fo = output pad frequency

The summation indicates that accurate power consumption approximations are made by considering as many blocks of logic and output pad groups as possible. Less accurate approximations can be derived by considering only elements that have high switching frequencies.

Please note that the above equation only gives an approximation of the actual power that a CMOS device will dissipate. The power factor (microwatts per megahertz per gate) data in Table 9–9 includes typical load (CV^2f) plus totem pole power dissipation.

Library	PF (µW per MHz per gate)
VS1500F	15
VGX1500	15
VS700	6
VGX700	6

TABLE 9–9 Power factor for various libraries

Example:

Assume a 40,000 gate design in the VS700 library with the following characteristics.

2,000 gates operate at 25 MHz
30,000 gates operate at 2 MHz
8,000 gates operate at 10 MHz
32 PPU400 cells
V_{DD} = 5V
16-bit bus driving 50 pF at 10 MHz

$$P = Pd + Ps + Po$$

$$P = 6\ \mu W * \{(2{,}000 * 25) + (30{,}000 * 2) + (8{,}000 * 10)\} + 32 * 400\ \mu A * 5V + 16 * 50\ pF * 5^2 * 10\ MHz$$

$$P = 1.14W + 0.06W + 0.20W = 1.40W$$

Power Supplies

The NCR CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive conventional power supplies instead of switching power supplies and power supplies with cooling fans. In addition, batteries may be used as either a primary power source or for emergency backup.

The absolute maximum power supply voltage for .7–micron and 1.5–micron is 7.0 V_{DC}. Figure 1 offers some insight as to how this specification was derived. In Figure 9–57, VS is the maximum power supply voltage and IS is the sustaining current of the latch–up mode. The value of VS was chosen so that the secondary breakdown effect may be avoided. The low–current junction avalanche region is between 10 and 14 V_{DC} at T_A = 25° C.

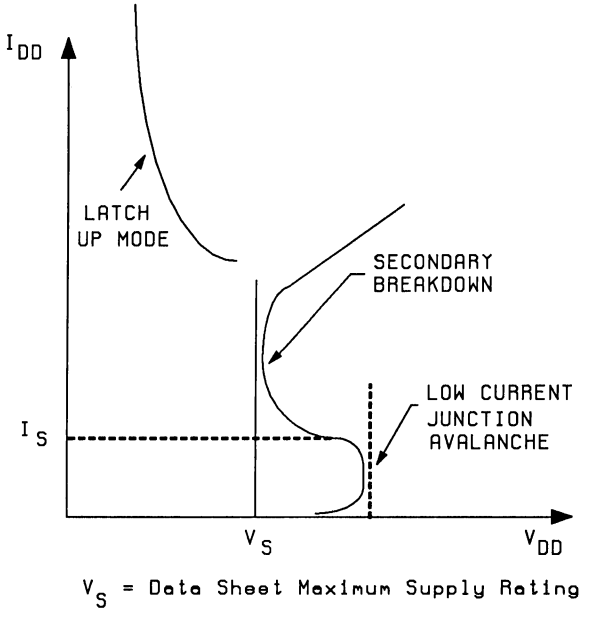


Figure 9–57 Secondary breakdown characteristics

In an ideal system design, a power supply should be designed to deliver only enough current to ensure proper operation of all devices. The obvious benefit of this type of design is cost savings; an added benefit is protection against the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

CMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing a battery operated system.

1. The recommended power supply voltage should be observed. For battery backup systems such as the one in Figure 9-58, the battery voltage must be at least 3.7 Volts (3 Volts from the minimum power voltage and 0.7 Volts to account for the voltage drop across the series diode). Please note that most simulation results are invalid at these low voltages. Chip performance will be significantly slower.
2. Inputs that might go above the battery backup voltage should either use a series resistor to limit the input current or use high-to-low voltage translators.
3. Outputs that are subject to voltage levels above V_{DD} or below V_{SS} should be protected with a series resistor to limit the current.

Inputs

Inputs to the internal cells can be made by using either input buffers or bidirectional buffers. Input buffers can only be used as inputs while bidirectional buffers can be used as an input, output or I/O buffer. All input buffers have input protection circuitry and can be configured for either TTL, CMOS or Schmitt trigger switching levels with or without a pullup resistor. The following design information pertains to all CMOS input buffers regardless of the input or bidirectional option chosen.

While in the recommended operating range ($V_{SS} < V_{IN} < V_{DD}$), all inputs can be modeled as shown in Figure 9-59. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case, I μA (at T_A = 85°C), when the inputs are at V_{DD} or V_{SS}, and V_{DD} = 6 V_{DC}. This model does not apply to inputs with a pullup resistor.

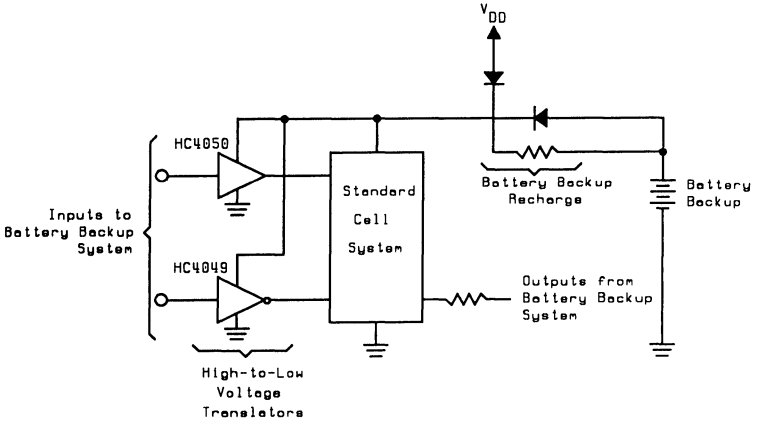


Figure 9–58 Battery backup system

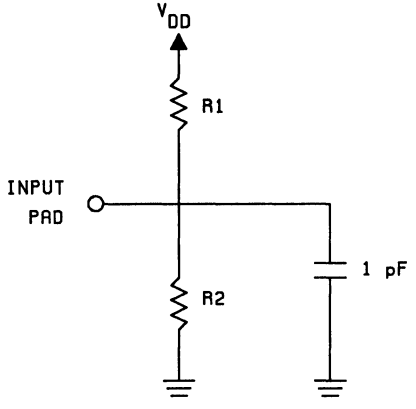


Figure 9–59 Input model for VSS < VIN < VDD

When the inputs are left open-circuited, it is possible for the inputs to be biased at or near the typical switch point where both the p-channel and n-channel transistors are conducting, causing excess current drain.

Due to the high gain of the input buffers (see Figure 9–60), the device may also go into oscillation from any noise in the system. Since CMOS devices dissipate the most power during switching, this oscillation can cause large current drain and undesired switching.

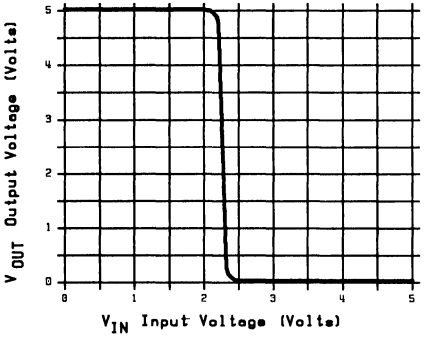


Figure 9–60 Typical transfer characteristics for input buffers

For these reasons, all unused input buffers should be connected either to V_{DD} or V_{SS}. For applications with inputs going to edge connectors, a 100K–10M ohm resistor to V_{SS} should be used as well as a series resistor for static protection and current limiting (Figure 9–61). The resistor to V_{SS} will help eliminate any static charges that might develop on the printed circuit board.

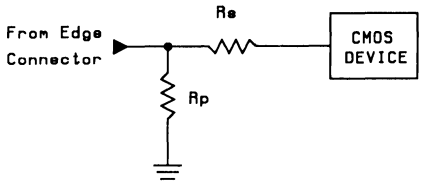


Figure 9–61 External protection

For input voltages outside of the recommended operating range, CMOS input is modeled as in Figure 9–62. The resistor–diode protection network allows the user greater freedom when designing a worst case system. At low capacitive loads, the output rise and fall times of output buffers can be as low as 3 ns, producing some amount of overshoot and undershoot. With the input protection provided, however, most designs will require no special terminations or design considerations.

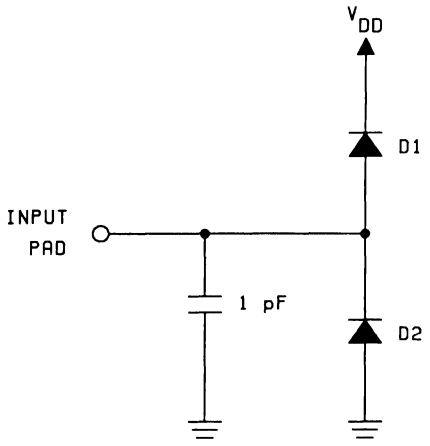


Figure 9–62 Input model for VIN > VDD or VIN < VSS

Other specifications that should be noted are the maximum input rise and fall times. Figure 9–63 shows that oscillations that may result from exceeding the 500 ns maximum rise and fall times. The output may oscillate because, as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input is amplified and passed through to the output. The oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed 500 ns, Schmitt–trigger devices such as the DS1216, DS1218, ... DS2028 or D2232 are recommended.

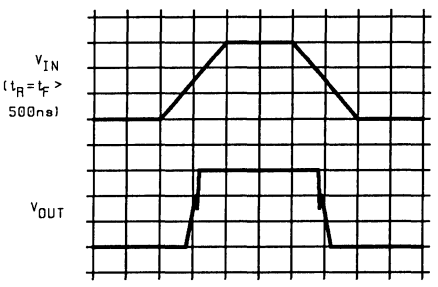


Figure 9-63 Maximum rise time violations

Outputs

Outputs from internal cells can be made through either output buffers or bidirectional buffers. All CMOS cell outputs are buffered to ensure consistent output voltage and current performance. All output and I/O pad cells have ESD protection circuitry. The output drives for all CMOS standard cell output and bidirectional options are user selectable from 2 mA to 48 mA.

CMOS cell outputs are limited to externally forced output voltages of V_{SS} −0.5 V < V_{OUT} < V_{DD} + 0.5 V_{DC}. When voltages are forced outside of this range, a parasitic Silicon Controlled Rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch up. For more information on this, see the explanation of CMOS latch-up in this section.

The maximum rated output current for any output buffer is 2, 4, 8, 16 or 48 mA depending on the pad used. The output short-circuit currents of these devices will typically exceed these limits. The outputs can, however, be shorted for brief periods of time for logic testing if the maximum package power dissipation is not violated.

Cell Selection and Usage

This section describes how and when to use particular NCR Standard Cells when designing a circuit. The standard cells described in these usage notes are the standard pad cells (input, output, and bidirectional) along with their corresponding buffer cells. For assistance with particular design situations not described elsewhere, contact your NCR applications engineer.

Standard Input Configurations

Each integrated-circuit input requires an input pad and an input buffer. The input pad functions as an input protection cell, protecting the circuit form electro-static discharge and excessive input voltages. The input buffer converts the input voltage to a voltage acceptable for the other standard cells. The input pad is separate from the input buffer to better protect against noise.

Two types of input pads are available: Input Pad (INPD) and Input Pad With Pullup or Pulldown (IPPD).

Two primary types of input buffers are available: an Input Buffer (INBUF) and several Schmitt triggers (DSxxyy). (The xxyy of DSxxyy indicates the high-to-low and low-to-high transition trigger voltages, respectively, with decimals implied.) An SBUF, MBUF, HBUF, or BUF8 can also be used for CMOS only inputs.

The input pads and input buffers can be assembled in a variety of combinations, depending upon the type of input signals expected. Typical combinations are shown in Table 9-10.

INPUT SIGNAL EXPECTED	INPUT PAD	INPUT BUFFER
Standard TTL or CMOS	INPD	INBUF
CMOS only	INPD	HBUF, BUF8, etc.
Standard TTL or CMOS	INPD	DSxxyy
Non-TTL or non-CMOS	INPD	DSxxyy
Standard TTL or CMOS with pullup or pulldown	IPPD	INBUF
CMOS only with pullup or pulldown	IPPD	HBUF, BUF8, etc.
Standard TTL or CMOS with pullup or pulldown	IPPD	DSxxyy
Non-TTL or non-CMOS with pullup or pulldown	IPPD	DSxxyy

TABLE 9-10 Typical combinations of input pad and input buffer

Standard Inputs

The configuration shown in Figure 9–64 should be used to obtain inputs that are compatible with both TTL and CMOS. This is the standard input configuration; it can be connected directly to either TTL or CMOS outputs.

The input pad cell is INPD; the input buffer cell is INBUF. The switch point is 1.4 V. Maximum voltage input low (V_{IL}) is 0.8 V and minimum voltage input high (V_{IH}) is 2.0 V.

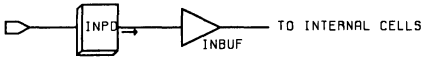


Figure 9–64 Standard input configuration

Schmitt Trigger Inputs

To obtain switch points different from TTL standards (0.8 V V_{IL} and 2.0 V V_{IH}), use an INPD cell and a Schmitt trigger cell. Several Schmitt trigger cells are available each with a different set of threshold voltages. The trigger cell acts as the input buffer for the input configuration.

For example, the configuration shown in Figure 9–65 has typical input switch points of 1.2 V V_{THL} and 1.8 V V_{TLH}. (These figures are listed in the cell's data sheet. They are also coded in the cell name; here, DS1218.) The input pad cell is INPD; the Schmitt trigger cell is DS1218.

If none of the available Schmitt trigger cells is suitable for your application, contact your NCR product marketing engineer to discuss designing a suitable new cell.

Figure 9–65 Sample input using Schmitt Trigger

Inputs With Internal Pullups or Pulldowns

An input pad cell is available which can be configured with switchable pullup or pulldown resistors. The pad cell is named IPPD. The pullup cells are named PPUnnn and the pulldown cells are named PPDnnn. The nnn of the PPUnnn and PPDnnn indicate the amount of pullup and pulldown current in units of microamps. An input buffer is also required. The configuration for an input with internal pullup, therefore, is the input pad (IPPD), the pullup cell (PPUnnn), and input buffer (INBUF or DSxxyy).

The PPUnnn and PPDnnn cells may be turned on and off by controlling its only input, or may be turned on continuously. To turn on PPUnnn cell, the input must be low. To turn on a PPDnnn cell, the input must be high.

PPUnnn and PPDnnn cells are available in standard sizes from 25 µA to 1600 µA. If your application requires pullup or pulldown current different from those available, please contact your NCR product marketing engineer to discuss designing a suitable new cell.

The configuration shown in Figure 9–66 is compatible with both TTL and CMOS inputs due to the INBUF. Because it uses cells IPPD and PPU400, it has a nominal internal pullup current of 400 µA.

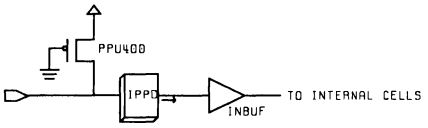


Figure 9-66 Standard Input with pullup current

Please note that PPUxxx or PPDxxx cells are normally connected to the UPDN input port of PPD (OPPD4, IOPPD2, IPPD, etc.) type pad cells. Timing numbers generated for these PPU/PPD cells assume a nominal 50 pF "off chip" load on the pad port of the pad cell. This 50 pF load is incorporated into the input capacitance value given to the UPDN input port. If pad loading in your system is expected to be substantially different from 50 pF and you are concerned about accurate pad pullup/pulldown rise/fall times (due to PPU/PPD cells) in your chip simulations, please contact your NCR applications engineer to determine how to proceed.

Standard Output Configurations

Each integrated-circuit output requires an output pad and an output buffer. The output pad can be standard, tristate or open drain. The output buffer drives the signal and can invert it. The output pad is separate from the output buffer to better protect against noise.

Three types of output buffers are available: Inverting Output Buffer (OUTINV, INV, INV2, INV3 or INV8), Noninverting High Drive Buffer (HBUF, SBUF, MBUF or BUF8), and Tristate Noninverting Input/Output Buffer (IOBUF, IOBUFS, IOBUFM or IOBUF8).

Four types of output pads are available:

- Inverting Output Pad (OPDn)
- Tristate Inverting Output Pad (OTPDn)
- Inverting Open-Drain Output Pads (ODPDn or ONPDn)
- Inverting Output Pad with Pullup or Pulldown (OPPDn)

The ONPDn is an open-drain output pad which can be used with an external resistor to pull up to 7 volts maximum. The n is the mA of sink current at V_{OL} = 0.4 V, or source current at V_{OH} = 2.4 V (see Electrical Specifications, DC Characteristics table).

The output pads and output buffers can be assembled in a variety of combinations, depending upon the type of output signals required. Typical combinations are shown in Table 9-11.

REQUIRED OUTPUT SIGNAL FROM PAD	OUTPUT BUFFER	OUTPUT PAD
Inverted	HBUF/BUF8/ SBUF/MBUF/	OPDn
Noninverted	OUTINV/INV8/ INV/INV3	OPDn
Noninverted or high-impedance, depending on IOBUF enable signal	IOBUF/IOBUF8/ IOBUFS/IOBUFM	OTPDn
Noninverted Open Drain	OUTINV/INV8/INV2 INV/INV3	ODPDn/ONPDn
Inverted Open Drain	HBUF/BUF8/ SBUF*/MBUF	ODPDn/ONPDn
Noninverted, with logical pulldown and resistive pullup	OUTINV/INV8/ INV/INV3	OPPDn and PPUnnn
Inverted, with logical pulldown and resistive pullup	HBUF/BUF8/ SBUF/MBUF	OPPDn and PPUnnn
Noninverted, with logical pullup and resistive pulldown	OUTINV/INV8/INV2 INV/INV3	OPPDn and PPDnnn
Inverted, with logical pullup and resistive pulldown	HBUF/BUF8/ SBUF/MBUF	OPPDn and PPDnnn
Noninverted, or high-impedance, with pullup and pulldown	IOBUF/IOUBUF8/ IOBUFS/IOBUFM	OPPDn, PPUnnn or PPDnnn

TABLE 9-11 Typical combinations of output buffer and output pad

Standard Outputs

Use the configuration shown in Figure 9-67 to produce a noninverted output capable of driving 4 mA of output current. The pad inverts the signal, so the output buffer must invert it as well to make the output signal noninverted. This output configuration, besides driving CMOS parts, provides these output voltage levels to provide compatibility with TTL parts: $V_{OH}(min) = V_{SS} + 2.4$ volts and $V_{OL}(max) = V_{SS} + 0.4$ volts, at the times specified in the cell data sheets.

To produce an inverted output with the same current characteristics as the preceding configuration, use a Buffer (SBUF, MBUF, HBUF, etc.) rather than an Inverting Output Buffer (INV, INV2, OUTINV, etc.). This configuration is shown in Figure 9-68. The Output Pad inverts the signal and this output buffer does not.

To produce different levels of output current, use the appropriate Output Pad (OPDn). Each pad's output current is specified in the pad's data sheet. Current drive values from 2 to 24 mA are possible for all output pad types. Some 48 mA pad types also exist.

Open Drain Pads (ODPDn or ONPDn) may be used in place of standard output pads shown in Figures 9-67 and 9-68 to create an open drain output.

Tristate Outputs

Use the configuration shown in Figure 9–69 to produce a noninverted output capable of driving 4 mA of output current and to be able to put the pad in a high–impedance state. The pad OTPDn inverts the signal, so the output buffer must invert it as well to make the output signal noninverted.

When the buffer (IOBUFS, IOBUFM, IOBUF, IOBUF8) enable signal is low, the inverted output signal is transmitted to the pad. When the buffer enable signal is high, the pad has a high–impedance state; both the p–channel and n–channel transistors on the pad are disabled.

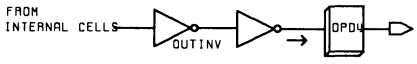


Figure 9–67 Standard output configuration for noninverted signal

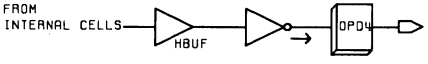


Figure 9–68 Standard output configuration for inverted signal

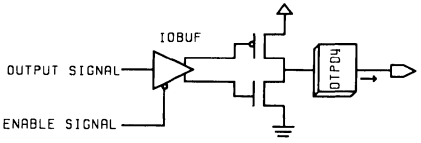


Figure 9–69 Standard tristate configuration for noninverted signal

Outputs with Internal Pullups or Pulldowns

Use the OPPDn pad with INV, INV2, INV3, OUTINV, or INV8 for logical low pulldown and resistive pullup; or for logical high pullup and resistive pulldown. The OPPDn pad may also be driven with an IOBUFS, IOBUFM, IOBUF or IOBUF8 and either PPUnnn or PPDnnn for resistive pullup or pulldown.

Figure 9–70 is an example of a tristate output to produce a noninverted signal with resistive high pullup and logical low pulldown. It uses the combination of OPPD4 and PPU400 to produce a 400 µA pullup current. Both the OUTINV output buffer and the OPPD4 output pad invert the signal, so the output signal is noninverted.

This sample configuration operates as follows:

1. When the output signal is a logical low, the logical pulldown is produced because the N–channel transistor on OPPD4 is enabled.
2. When the output signal is a logical high, the resistive pullup is produced by the PPU400.

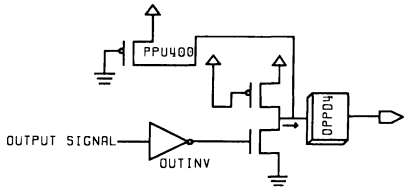


Figure 9–70 Tristate configuration for noninverted signal with pullup

Standard Bidirectional Configurations

Bidirectional configurations are those allowing either input or output by means of the same pad. Two types of bidirectional pads are available: Bidirectional Pad (IOPDn) and Bidirectional Pad with Pullup or Pulldown (IOPPDn). The n is the number of mA of output current drive. An IONPD48 is also available which has no p-channel pullup.

The cells used for the standard configuration are the bidirectional pad (IOPDn), an input buffer (INBUF or DSxxyy), and an input/output buffer (IOBUFS, IOBUFM, IOBUF or IOBUF8). The input buffer functions as an ordinary input buffer when the pad is used for input. The input/output buffer functions as the output buffer when the pad is used for output.

Bidirectional Configuration

The configuration shown in Figure 9-71 is the standard to be used for bidirectional pins. As with any bidirectional bus design, noise is a problem if large transient currents exist because of bus contention with this configuration.

This configuration functions as follows:

1. When the output enable signal is low, the configuration produces a noninverted output signal with 4 mA of current drive. (Note that the output signal is also available through the input path by means of the input buffer.)
2. When the output enable signal is high, the pad is put into a high-impedance state. This allows the pad to accept input from off the chip; the input is directed through the input buffer.

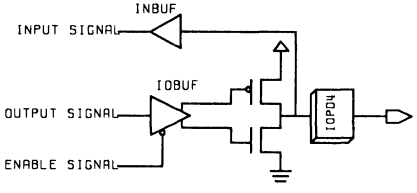


Figure 9-71 Standard bidirectional configuration

Bidirectional Pad with Internal Pullup or Pulldown

Bidirectional pad cells can be used with the PPUnnn and PPDnnn cells to achieve internal pullups or pulldowns. These cells are named IOPPDn.

An input buffer and input/output buffer are also required, like the other bidirectional pads. The configuration for a bidirectional pad with internal pullup, therefore, is the bidirectional pad (IOPPDn), pullup cell (PPUnnn), and input/output buffer (IOBUFS, IOBUFM, IOBUF or IOBUF8). The standard configuration shown in Figure 9-72 should be used for bidirectional pads with pullups. To have a pulldown configuration, use the PPDnnn cells. A Schmitt trigger (DSxxyy), or CMOS Buffer (SBUF, HBUF, etc.) could replace the INBUF if necessary.

This configuration functions as follows:

1. When the output enable signal is low, the configuration produces a noninverted output signal with a 4 mA of current drive. (Note that the output signal is also available through the input path by means of the input buffer.)
2. When the output enable signal is high and the pad is in a high-impedance state, the pad is pulled high by the pullup cell. This is the primary difference between this configuration and the standard bidirectional configuration.

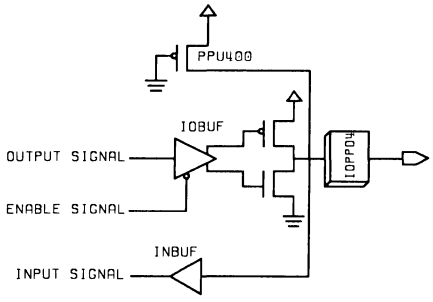


Figure 9-72 Standard bidirectional configuration with pullup

Buffer Selection for Pad Cells and Slew Rate Control

In general, there is a direct trade-off between pad cell speed performance and noise generated on V_{SS} (ground bounce) or V_{DD} bus lines. The faster the pad propagation delay, the higher the pad output slew rate (dV/dt and dI/dt), and the greater the noise for a given environment. The quality of the ground plane can vary between device tester, bench test setup, and printed circuit board environments. The device package is also a key component in establishing the quality of the ground plane because of package lead inductance (see Determining Power Pad Requirements).

NCR has investigated a number of techniques for controlling slew rate and found that proper selection of the pad buffer and pad cell will achieve slew rate control and minimize noise. NCR libraries offer a wide range of buffers and pad cells to provide low noise systems. The following are the variables which determine noise immunity.

- Pad cell sink/source current. The higher the pad drive, the more noise.
- Pad buffer drive. The higher the buffer performance, the greater the dV/dt on the buffer output (pad cell input), and the greater the dI/dt for the pad driver transistors.
- Ground plane quality. Keep resistance and inductance as low as possible. Package choice is critical.

The following are design recommendations for improving noise immunity.

- Use the smallest pad buffer and pad driver necessary to meet speed requirements. Refer to Table 9-12.
- Consider skewing transitions on wide signal busses to minimize simultaneous switching.
- Avoid the use of INBUF cells if TTL compatibility is not necessary. The lower TTL trip-point on the INBUF makes it more sensitive to ground bounce compared to CMOS buffers (SBUF, MBUF, HBUF).
- Use Schmitt triggers in high noise environments.
- Follow the recommended number of V_{SS}/V_{DD} power pins (see Determining Power Pad Requirements).

In addition, NCR will provide separation of I/O pad V_{SS} and internal core V_{SS} power pins during layout to improve noise isolation on-chip.

Table 9-12 shows recommended buffer and pad cell combinations for designing a low noise device. For example, you should use an INV or SBUF to drive an OPD4 in the VS700 library. You should use an IOBUFM to drive an IOPD8 pad.

Standard Buffer Type	Output Pad Size	VS1500	VGX1500	VS700	VGX700
Noninverting buffer	2–4 mA 8–16 mA 24–48 mA	SBUF MBUF HBUF	SBUF MBUF HBUF	SBUF MBUF HBUF	SBUF MBUF HBUF
Inverting buffer	2–4 mA 8–16 mA 24–48 mA	INV INV3 OUTINV	INV INV3 OUTINV	INV INV2 OUTINV	INV INV3 OUTINV
I/O buffer	2–4 mA 8–16 mA 24–48 mA	IOBUFS IOBUFM IOBUF	IOBUFM IOBUFM IOBUF	IOBUFS IOBUFM IOBUF	IOBUFM IOBUFM IOBUF

TABLE 9–12 Buffer selection for low noise applications

Table 9–13 shows the buffer and pad combinations for high speed devices. Use of these options may result in greater noise generated on V_{SS} or V_{DD} busses.

Standard Buffer Type	Output Pad Size	VS1500	VGX1500	VS700	VGX700
Noninverting buffer	2–4 mA 8–16 mA 24–48 mA	MBUF HBUF BUF8	MBUF HBUF BUF8	MBUF HBUF BUF8	MBUF HBUF BUF8
Inverting buffer	2–4 mA 8–16 mA 24–48 mA	INV3 OUTINV INV8	INV3 OUTINV INV8	INV3 OUTINV INV8	INV3 OUTINV INV8
I/O buffer	2–4 mA 8–16 mA 24–48 mA	IOBUFM IOBUF IOBUF8	IOBUF IOBUF IOBUF8	IOBUFM IOBUF IOBUF8	IOBUF IOBUF IOBUF8

TABLE 9–13 Buffer selection for high speed applications

Buffer Fanout Rules of Thumb

Listed below are the recommended fanouts for buffer cells. Although it is possible to make buffer selections other than those recommended, using the recommended buffer sizes ensures optimum performance.

Standard Buffer Type	VS1500	VGX1500	VS700	VGX700
Inverting				
INV	1–4	1–4	1–4	1–4
INV2	n/a	n/a	4–8	n/a
INV3	6–12	6–12	6–12	6–12
INVH	6–12	8–16	6–12	8–16
INV8	16–32	16–32	16–32	16–32
OUTINV	8–16	8–16	8–16	8–16
Noninverting				
SBUF	1–6	1–6	1–6	1–6
MBUF	6–12	6–12	6–12	6–12
HBUF	12–24	12–24	12–24	12–24
BUF8	24–48	24–48	24–48	24–48
Input				
INBUF	1–16	1–8	1–16	1–8
DSxxxx	1–16	1–4	1–16	1–4
Tristate				
INVT	1–4	1–2	1–4	1–4
INVTH	4–8	4–8	4–8	4–8
INVT3	6–12	6–12	6–12	6–12
TBUFP	1–8	1–4	1–4	1–4
TBUF	8–16	1–4	1–4	1–4
TBUF3	1–12	4–12	4–16	4–12
Clock driver				
PCL2	8–16	8–16	8–16	8–16

TABLE 9–14

Proper Techniques to Add Delay in Critical Paths

In many circumstances it may be necessary to add delay to a critical path. NCR recommends the use of single input gates (inverters or buffers) for this purpose. Do not use multiple input combinational gates (NANDs, NORs, etc.) with inputs tied together. Because of the simultaneous switching effect with the tied inputs, the actual delay through the gate is much faster than modeled by the logic simulator. Simultaneous switching gates can only be accurately modeled with a transistor-level simulator.

Figure 9-73 illustrates the incorrect use of tied input gates compared to the recommended application of single input gates.

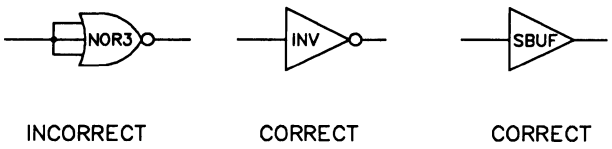


Figure 9-73 Techniques to add delay in critical paths

Pullup and Pulldown Current Range Specifications

Table 9–15 specifies multiplication factors used to compute current ranges for different operating conditions obtained by PPU (PPU25, PPU100, etc.) or PPD (PPD25, PPD100, etc.) type cells.

Type	Conditions	Current Multiplying Factor	
		VS1500, VS700	VGX1500, VGX700
Commercial – Low	Worst Case Process, V_{DD} = 4.5V, 70C	.50	.50
– High	Best Case Process, V_{DD} = 5.5V, 0C	1.65	2.00
Industrial – Low	Worst Case Process, V_{DD} = 4.5V, 85C	.45	.45
– High	Best Case Process, V_{DD} = 5.5V, –40C	2.00	2.40
Extended – Low	Worst Case Process, V_{DD} = 4.5V, 125C	.40	.40
– High	Best Case Process, V_{DD} = 5.5V, –55C	2.20	2.60

TABLE 9–15 Pullup/pulldown current range factors

To compute the current range for a specific PPU/PPD cell, obtain the typical (Nominal Conditions) current value specified in the cell's data sheet and multiply by the given factor in Table 9–15. The current range obtained is valid under test conditions specified in the data sheets (For PPUxxx cells: $V_{ENB} = V_{SS}$, $V_{OUT} = V_{SS}$. For PPDxxx cells: $V_{EN} = V_{DD}$, $V_{OUT} = V_{DD}$).

As an example, to compute the full current range expected over Commercial Conditions for a VS700 PPU400 cell, the following calculations would be necessary:

Low range limit = (Typical Value) * (Low Mult. Factor)
= (400 µA) * (.50) = 200 µA

High range limit = (Typical Value) * (High Mult. Factor)
= (400 µA) * (1.65) = 660 µA

The current range for the PPU400 would therefore be 200 µA to 660 µA over the entire range of Commercial Operation Conditions.

Pullup/Pulldown Cell Delays

PPUxxx or PPDxxx cells are normally connected to the UPDN input port of PPD (OPPD4, IOPPD2, IPPD, etc.) type pad cells. Timing numbers generated for these PPU/PPD cells assume a nominal 50 pF "off chip" load on the pad port of the pad cell. This 50 pF load is incorporated into the input capacitance value given to the UPDN input port. If pad loading in your system is expected to be substantially different from 50 pF and you are concerned about accurate pad pullup/pulldown rise/fall times (due to PPU/PPD cells) in your chip simulations, please contact your NCR applications engineer to determine how to proceed.

Oscillator Application Note

NCR offers a variety of oscillators covering the frequency range of 32 KHz to 50 MHz. See Table 9–16. The oscillators provided are parallel resonant circuits. Each oscillator has unique specifications and requirements. For detailed information on a particular oscillator, consult the data sheet. This application note is intended to provide oscillator design information. The application note discusses crystal mechanics and Pierce oscillator circuits.

Standard Cell		VGX Gate Array	
Frequency	**Cell**	**Frequency**	**Cell**
10 KHz to 100 KHz	OSC5001	1 MHz to 50 MHz	OSCFP
1 MHz to 10 MHz	OSC5301		
10 MHz to 25 MHz	OSC5302		
25 MHz to 50 MHz	OSC5401		

TABLE 9–16

Quartz Crystals

A quartz crystal is a thin, circular slice of quartz placed between two electrodes. When a potential difference is applied to the electrodes, the quartz undergoes a mechanical stress and deformation. Likewise a stress applied to the quartz will produce a potential difference at the electrodes. This property of quartz is known as the piezoelectric effect. At most frequencies the quartz crystal resembles a capacitor. Over a certain range of frequencies, the piezoelectric property of quartz will cause the crystal to resonate. At these frequencies the crystal displays an inductive reactance. Various modes of mechanical resonance are possible. These modes are commonly referred to as the fundamental, 3rd, 5th, and 7th overtone responses. The overtone responses are not exact harmonics of the fundamental; but rather different mechanical modes of vibration. Usually several hundred KHz above a main response, the crystal will display spurious responses. These responses could cause the oscillator to capture at a frequency above the main response. This usually does not happen because of the large series resistance associated with the spurious modes. An example of the magnitude and phase response of a 14.3 MIHz crystal is given in Figure 9–74.

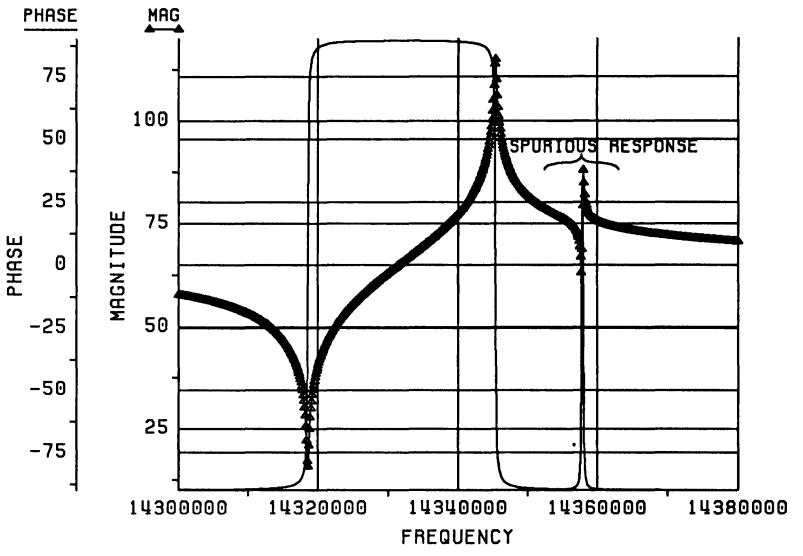


Figure 9-74 Magnitude and phase response of a 14.3 MHz crystal

An equivalent circuit for the crystal at a particular response is represented in Figure 9-75. C_0 in the circuit represents the holder capacitance. For frequencies above and below resonance, the impedance of the crystal is capacitive, with a value of C_0. The second branch of the equivalent circuit, comprised of C, R, and L, is called the motional branch. The frequency at which C and L resonate is called the series resonant frequency. At this frequency,

$$F_S = 1/(2\pi\ (LC)^{1/2}),$$

the impedance of the crystal, is approximately R_1. For frequencies greater than series resonance, L_1 in the motional branch dominates resulting in the inductive behavior of the crystal. The antiresonant frequency of the crystal occurs after the series resonant frequency. At this frequency,

$$F_A = 1/(2\pi\ (LCC_0/(C+C_0))^{1/2}),$$

the motional branch, resonates with the holder capacitance C_0. The difference between the antiresonant frequency and the series resonant frequency defines the region in which the reactance is positive. This difference marks the total amount of frequency adjustment. The output oscillator frequency will always be bounded by the series and antiresonant frequencies. The bandwidth of a crystal is given by

$$F_A - F_S = F_S C/2C_0.$$

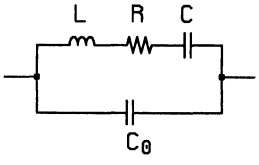


Figure 9-75 Crystal equivalent circuit

Pierce oscillator circuits for VGX1500 gate arrays

A Pierce oscillator circuit (Figure 9–76) operates at the frequency where the crystal is in parallel resonance with the load capacitance. The load capacitance is the total capacitance in parallel with the crystal. For Figure 9–76 this capacitance includes C_1, C_2, and the parasitics at the input and output pins. The load capacitance is defined as

$C_L = C_{XTLO}C_{XTLI}/(C_{XTLO} + C_{XTLI})$,
where $C_{XTLI} = C_1 + C_{1PAR}$
$C_{XTLO} = C_2 + C_{2PAR}$.

If C_L is decreased the operating frequency is increased. Likewise, if C_L is increased, the operating frequency is decreased. Given a certain load capacitance, the operating frequency can be calculated from

$$F_{OP} = 1 / (2\pi(LC(C_L+C_0)/(C+C_L+C_0))^{1/2}).$$

When purchasing crystals for a Pierce oscillator, the crystal manufacturer will ask for a load capacitance specification. Given the load capacitance, the crystal manufacturer can trim the crystal to obtain the desired resonance frequency. Sometimes a crystal is specified as series. In this case the crystal manufacture has specified the series resonate frequency. When a series specified crystal is placed in a Pierce circuit, the operating frequency is greater than the specified frequency. In most computer and peripheral applications the frequency shift is not detrimental to the application. The Equation for F_{OP} can be used to calculate an approximate operating frequency.

Figures 9–76 and 9–77 are two examples of Pierce oscillators configured from the VGX1500 free-place gate array oscillator. Figure 9–76 is a fundamental application and Figure 9–77 is an overtone application. Shown in the figures are the external components required to bias the inverter and those components necessary for the crystal pi network. R_B causes the inverter to self bias at approximately $V_{DD}/2$. At this point the inverting amplifier has high gain which is necessary for the circuit to oscillate. The value of R_B should be chosen in the range of 1 MΩ to 5 MΩ; such that it will not affect the AC performance of the circuit.

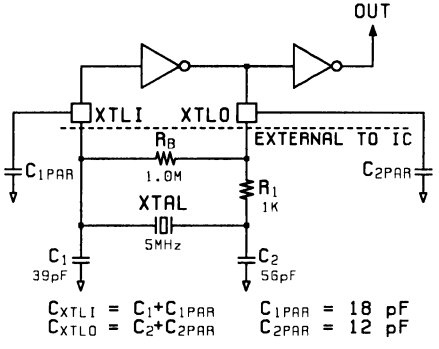


Figure 9–76 Typical fundamental mode circuit for VGX1500 gate array

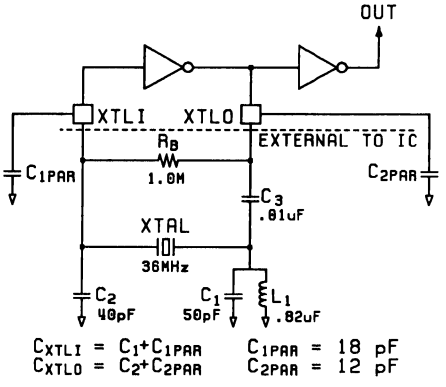


Figure 9–77 Typical third overtone circuit for VGX1500 gate array

C_{XTLI} and C_{XTLO}, in Figure 9–76, along with the crystal form a pi network which resonates at the specified crystal frequency. The ratio C_{XTLO}/C_{XTLI} should be somewhat greater than unity since it is a term in the loop gain equation. Increasing the ratio too much will cause the voltage swing on XTLI to exceed the supply rails which is undesirable. Typically the ratio is between 1.1 and 1.5. The series combination of C_{XTLO} and C_{XTLI} should be approximately equal to the load capacitance specified for the quartz crystal.

Example calculation:

$C_{XTLI} = C_1 + C_{1PAR}$
$= 39 + 18\ pF = 57\ pF$
$C_{XTLO} = C_2 + C_{2PAR}$
$= 56 + 12\ pF = 70\ pF$
$C_{XTLO} / C_{XTLI} = 1.22$
$C_L = (57 \times 70) / (57 + 70)$
$= 31.4\ pF$

An exact analysis would need to include the effect of R_1 between the oscillator output and the crystal. The method shown is a reasonable approximation. The crystal load capacitance can be specified as 32 pF which is the closest standard value.

The output resistance of the oscillator core, along with C_{XTLO}, form an RC low pass circuit. This pole contributes additional phase shift around the loop. Phase shift in excess of 360 degrees is necessary to insure oscillator start up and stability. At lower oscillator frequencies, it may be necessary to add R_1 in series with the output to add additional phase shift. This is most important in the 1–20 MHz region. Typical values for R_1 are shown in Table 9–17. At frequencies above 25 MHz, R_1 can usually be omitted. R_1 also reduces the drive to the crystal and thus reduces crystal power dissipation.

Frequency	R1
1 MHz	2 K – 5 KΩ
2 MHz	2 KΩ
5 MHz	1 KΩ
10 MHz	500 Ω
20 MHz	200 Ω

TABLE 9–17 Typical values for R1

To achieve overtone oscillation, the fundamental frequency must be suppressed. The fundamental can be suppressed by making the loop gain at the fundamental less than one. In this situation, if the loop gain is greater than one at the overtone frequency, the overtone mode will be selected. The additional components necessary for overtone operation are a capacitor and an inductor. The capacitor (C_3) is simply a DC block so the inductor does not short the inverter output to ground. C_{XTLO} and L_1, shown in Figure 9–77, are collectively called a tank circuit. This circuit resonates at the frequency of

$$F_{TANK} = 1/(2\pi\ (L_1 C_{XTLO})^{1/2}),$$

At frequencies below F_{TANK}, the tank impedance is inductive. Conversely for frequencies above F_{TANK}, the tank circuit is capacitive. If the tank impedance is inductive, the gain and phase conditions for the circuit do not meet the requirements for oscillation. For this reason, L_1 and C_{XTLO} are typically chosen to place the tank resonant frequency midway between the fundamental frequency and the third overtone frequency of the crystal. In this way the tank circuit is capacitive at the overtone frequency, and the conditions for start up are achieved. The effective capacitance of the tank circuit at the overtone frequency can be calculated from

$$C_{EFF} = C_{XTLO}(\omega^2 - 1/C_{XTLO}L_1)/\omega^2$$

By properly choosing the tank circuit component values, the overtone can be selected.

Three equations can be used to calculate approximate values for L_1, C_1, and C_2. The first equation,

$$C_L = C_{EFF} C_{XTLI} / (C_{EFF} + C_{XTLI})$$

is used to insure that the crystal is presented with the proper load capacitance. C_L is the load capacitance specified by the crystal manufacture. The second equation is given by

$$C_{EFF} / C_{XTLI} = 1.1.$$

If C_{EFF} is greater than C_{XTLI}, the feedback pi network will have gain, which improves startup. The third equation is used to place the tank resonating frequency midway between the fundamental and the third overtone frequency. This equation is given by

$$1/(2\pi (L_1 C_{XTLO})^{1/2}) = (F_{FUND} + F_{3rd})/2.$$

When the three equations are solved, approximate values for L_1, C_1, and C_2 are found. Due to additional PC board parasitics and crystal variances, these values should be verified in the lab for oscillator start up. Slight adjustments might be necessary to insure that the fundamental is stopped and the third overtone is selected. The circuit values shown in Figure 2 are typical for a 36 MHz third overtone crystal.

Example Calculation

Given C_l =25pF C_{1PAR}=18pF C_{2PAR}=12pF

C_{EFF} = 48 pF
F_{TANK} = 20.7 MHz
C_{XTLI} = 27 pF + 18 pF C_1 = 27 pF
C_{XTLO} = 60 pF + 12 pF C_2 = 60 pF
L_1 = .82 µH
C_{XTLO}/C_{XTLI} = 1.06

Pierce oscillator circuits for VS1500F

The previous fundamental and overtone examples focused on the VGX1500 free-place gate array oscillator. The design methodology outlined within the examples is also applicable to NCR's standard cell oscillators. The circuit topology is similar for both the gate array oscillator and the standard cell oscillators. In most cases the standard cell oscillators offer features not available with the gate array oscillator. For fundamental applications, NCR has included on-chip capacitors and a feedback resistor. Placing the capacitors and the feedback resistor on chip greatly reduces the board space necessary for the oscillator. With the capacitors on chip, the load capacitance and the capacitor tolerance is fixed. The fixed load capacitance will affect the nominal output frequency. Likewise, the capacitor tolerance will impact the output frequency tolerance. In most computer and peripheral applications, the board space savings is more critical then the slight frequency difference. The feedback resistor provided on chip is approximately 1 MΩ. The value of the feedback resistor will not affect the AC performance of the Pierce circuit. The OSC5401, overtone standard cell oscillator, is identical to the gate array oscillator with the exception of the inclusion of an on-chip feedback resistor and a power-down mode. The design methodology presented for the gate array is identical for the overtone standard cell oscillator.

The preferred package location of an oscillator is at the center of any side. Placing the oscillator at the center, minimizes bondwire and leadframe parasitics. This is especially important in DIP packages. It is also desirable to place power (V_{DD}) and ground (V_{SS}) near the oscillator, especially at frequencies above 25 MHz. The crystal and the pi network should be mounted close to the chip, with short connections to X_{TLI}, X_{TLO}, and V_{SS}.

The oscillator output, X_{TLO}, should not normally be used to drive external circuits except the oscillator pi network. To drive off chip, the on-chip generated clock should be buffered through an output pad (Figure 9-78).

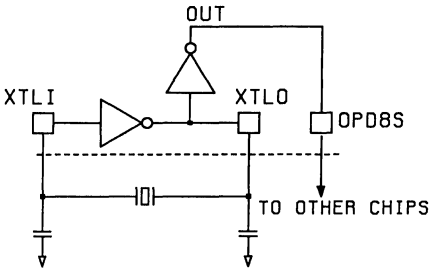


Figure 9-78 Using the on-chip oscillator to drive external chips

Crystal Frequency	L	C	C_0	R
1 MHz	3082 µH	8.223 fF	4.230 pF	575 Ω
1 MHz	2960 µH	8.560 fF	4.615 pF	255 Ω
2 MHz	732.5 µH	8.648 fF	3.918 pF	28 Ω
2 MHz	987.4 µH	6.416 fF	3.105 pF	122 Ω
5 MHz	56.36 µH	17.99 fF	4.451 pF	12 Ω
10 MHz	10.64 µH	23.83 fF	5.998 pF	14 Ω
20 MHz	3.042 µH	20.81 fF	5.310 pF	6.7 Ω
31 MHz	18.35 µH	1.4 fF	4.45 pF	27.6 Ω
40 MHz	9.34 µH	1.69 fF	4.35 pF	19 Ω

TABLE 9-18 Typical measured crystal parameters (Represents several manufacturers' AT cut crystals)

Suggested References:

Crystal Oscillator Design And Temperature Compensation by Marvin Frerking

Design Of Crystal And Other Harmonic Oscillators by Benjamin Parzen

JTAG Boundary Scan Cells Application Note

A boundary scan system employs the use of a shift-register with a bit corresponding to each component pin, such that signals at component boundaries are controllable and observable using scan testing techniques. Building a boundary scan system with the NCR standard cell library that is in conformance with the IEEE 1149.1 standard involves using the BSxxxx cells in conjunction with input, output, and bidirectional pads and buffers to form a shift register around the system logic. The shift register path is provided with a serial input (TDI) and a serial output (TDO) as well as an appropriate clock (TCK) and control signals. The connection from the TAP_CONTROLLER to the various control signals will be discussed below. For an N-bit shift register bit[N-1]'s 'prev' pin is connected to TDI, bit[j]'s 'next' pin is connected to bit[j-1]'s 'prev' pin, and bit[0]'s 'next' pin is connected to TDO. That is to say the most significant bit is connected to TDI and the least significant bit is connected to TDO.

For all input pads and associated buffers, the output of the pad is connected to the 'PAD_DI' pin of the BSINR as shown in Figure 9-82. The input of the buffer (INBUF, DS1218, etc.) is connected to the 'DI' pin of the BSINR.

For output pads with only one input pin (OPDx, ODPDx, ONPDx, IONPD48), the 'PAD_DO' pin of the BSOUTR1, BSOUTR4, or BSOUTR8 is connected to the input of the pad cell, as is seen in Figure 9-83.

For other output pads, the 'PAD_PCII' and 'PAD_NCH' pins of the BSOTR1, BSOTR4, or BSOTR8 are connected to their respective inputs on each pad cell, as shown in Figure 9-84. The BSENBR cell is also needed for the tristate enable signal used for these pad cells. The 'BSENB' pin of the BSENBR is connected to the 'ENB' pin of the BSOTR1, BSOTR4, or BSTR8 cell for tristate enable. Note that with a tristate bus that is enabled by a common signal, only one BSENBR is needed for the entire bus.

For Input/Output pads, the same connections as the BSOTR plus BSINR cells are used, as shown in Figure 9-85. The 'DI' output of the IO pad is connected to the 'PAD_DI' pin of the BSIOR1, BSIOR4, or BSIOR8. The input buffer is connected to the 'DI' pin of the BSIOR cell. The 'PAD_PCH' and 'PAD_NCH' pins are connected to the respective inputs of the IO pad. Again, only one BSENBR cell is needed if the IO bus is controlled by a common tristate enable.

Boundary scan output and I/O cells are available in several drive capabilities. A general rule of thumb for selection of a cell is to use the lowest numbered cell which will still meet your speed requirements. A set of general guidelines is given in Table 9-19.

	General Usage			High Speed Designs		
Output Pad Size	Output Cell	Tristate Cell	IO Cell	Output Cell	Tristate Cell	IO Cell
2–4 mA	BSOUTR1	BSOTR1	BSIOR1	BSOUTR4	BSOTR4	BSIOR4
8–16 mA	BSOUTR1	BSOTR1	BSIOR1	BSOUTR4	BSOTR4	BSIOR4
24–48 mA	BSOUTR4	BSOTR4	BSIOR4	BSOUTR8	BSOTR8	BSIOR8

TABLE 9–19 Boundary scan cell selection

The instruction register for the TAP allows instructions to be shifted into a design. The instructions are used to select test modes and/or which test data register to access. The minimum instruction register configuration is two bits and is shown in Figure 9–80. The two least significant instruction register cells must load a binary '01' pattern in the CAPTURE_IR state. There are three required instructions: BYPASS -- 11, EXTEST -- 00, SAMPLE -- 01. An optional command, INTEST is implemented by 10. BYPASS is required to be all 1's, and EXTEST is required to be all 0's. The routing of data through each boundary scan cell is derived from the instruction register mode control outputs. The following table shows the input mode control and output mode control for each instruction.

INSTRUCTION	b1	b0	IMC	OMC
BYPASS	1	1	0	0
EXTEST	0	0	0	1
SAMPLE	0	1	0	0
INTEST	1	0	1	1

The instruction decode for this is very simple and is seen in Figure 9–80.

There are three inputs to the TAP_CONTROLLER and they should be connected as shown on Figure 9–79; TMS and TRSTB should have pull–ups on them to cause the TAP_CONTROLLER to go to the test logic reset state if they are not driven to specific values. If a TRSTB chip pad is not desired, the TRSTB pin of the TAP_CONTROLLER may alternately be driven by a circuit using a POR (Power–on–Reset) cell. The outputs of the TAP_CONTROLLER will need to be connected to every boundary scan cell and instruction register cell; therefore, it is advised that these connections be made with page connectors as seen on Figure 9–79. Note that the drive capability for the outputs of the TAP is that of a BUF8 and the user may need to add additional buffering in some cases. Finally, Figure 9–81 shows a proper configuration of the test data serial output (TDO). The BYPASS register is clocked by CLOCKDR. Bypass_select from the instruction register decode selects either the test data register or the BYPASS register. The SELECT signal from the TAP_CONTROLLER selects either the instruction register or the data register selected by bypass_select. The ENABLE signal from the TAP_CONTROLLER either puts TDO into high impedance or outputs the appropriate register.

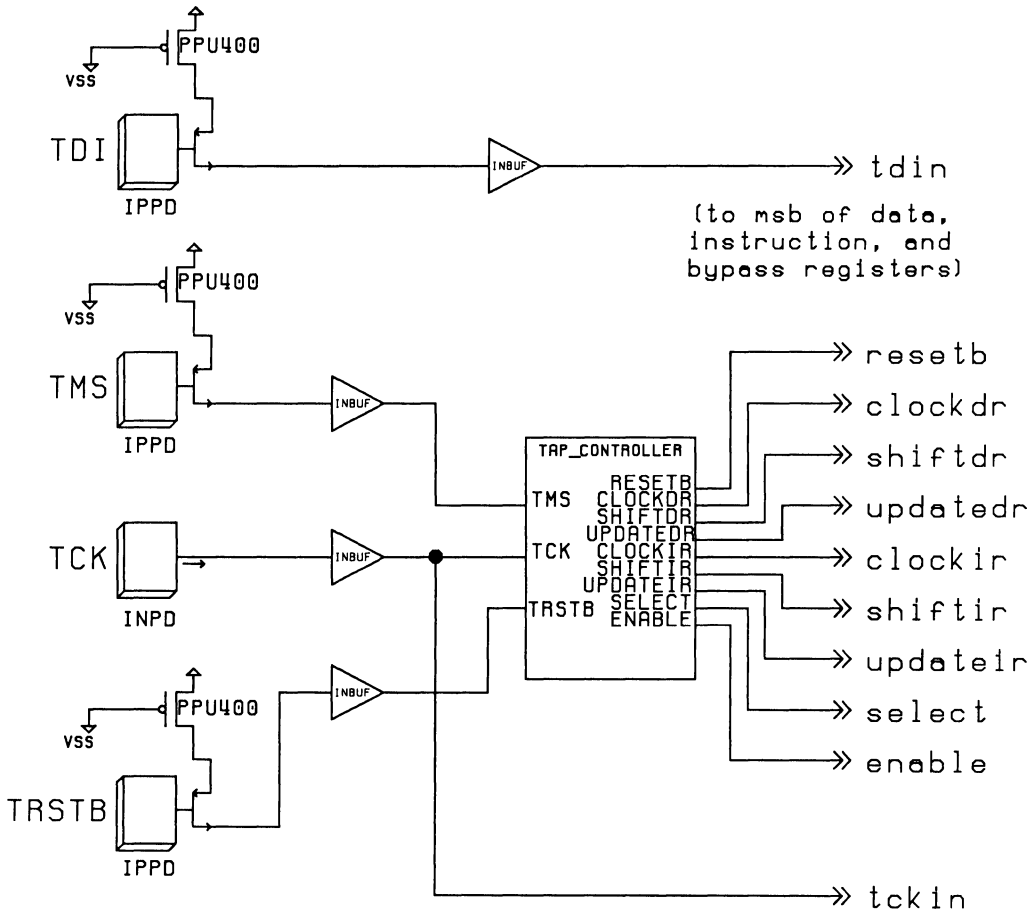


Figure 9–79 Boundary scan TAP_CONTROLLER connections

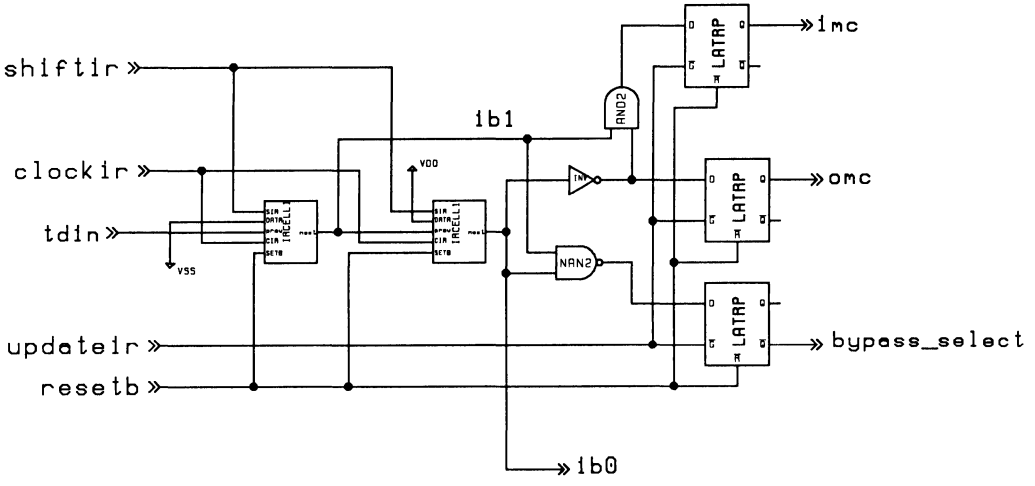


Figure 9-80 2-bit instruction register connections for boundary scan

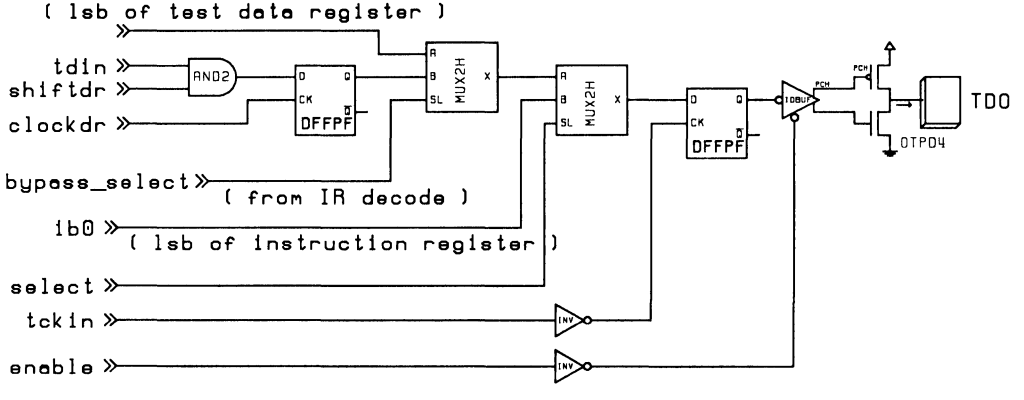


Figure 9-81 Boundary scan configuration for TDO output

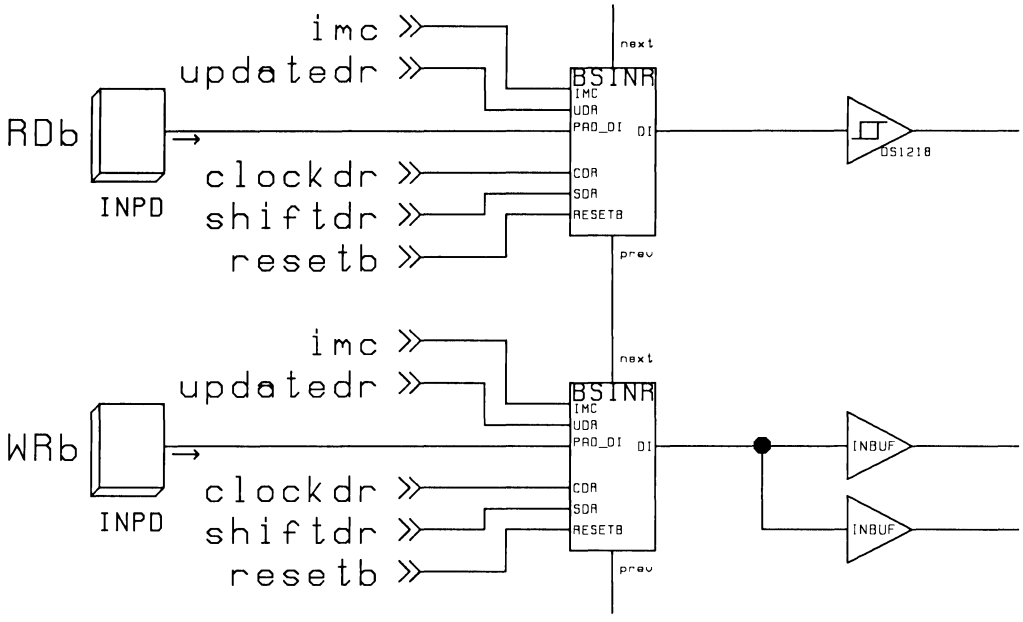


Figure 9–82 Boundary scan connections on input cells

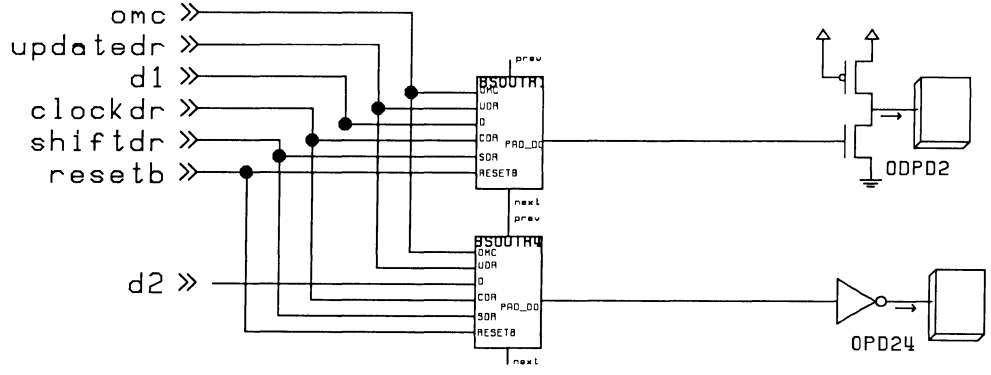


Figure 9–83 Boundary scan connections on output cells

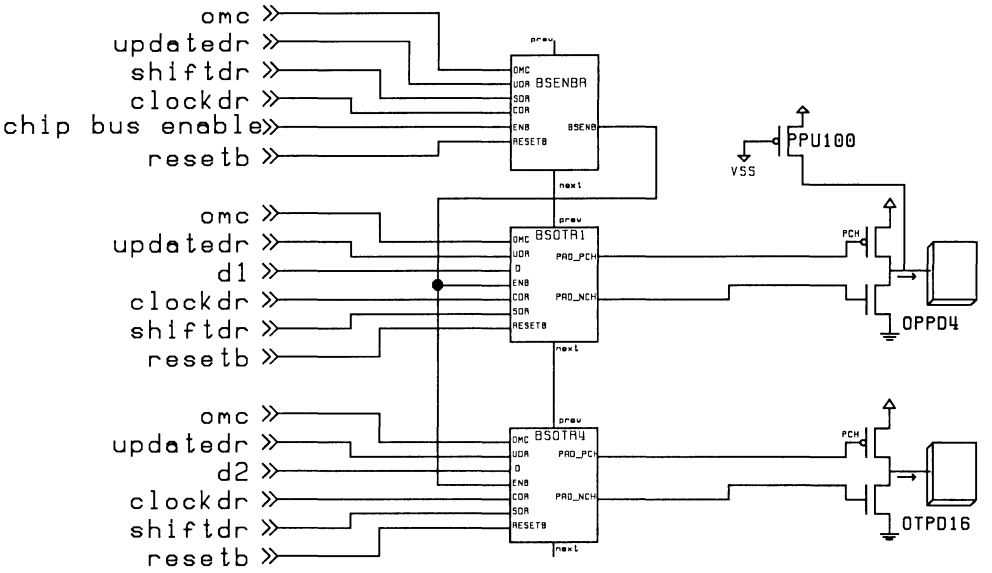


Figure 9–84 Boundary scan connections on tristate output cells

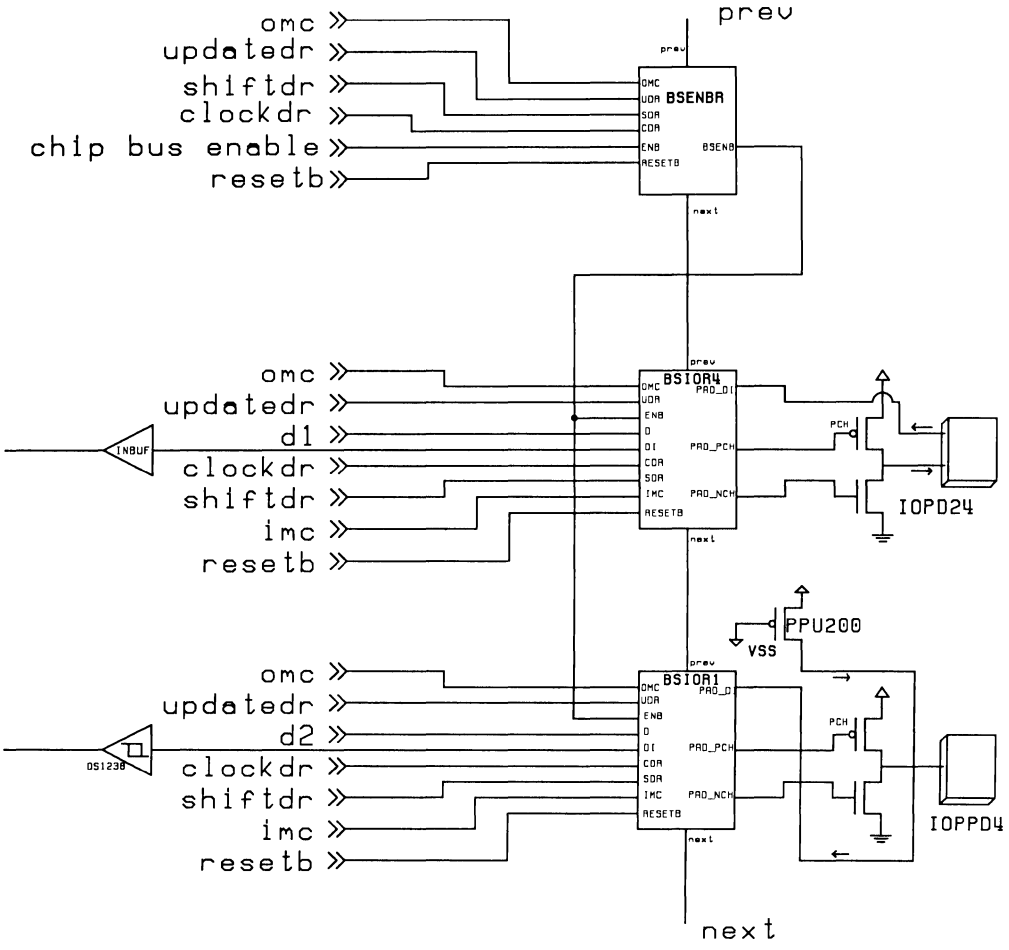


Figure 9–85 Boundary scan connections on bidirectional I/O cells

7400 Series Soft Macrocells Application Note

About this Application Note

This application note is intended for the circuit designers who are developing CMOS semicustom devices using NCR's ASIC products. Readers should be familiar with the process of developing and verifying ASIC designs using NCR's design system.

What are Soft Macrocells?

Soft macrocells are software tools which increase the efficiency of the design cycle by eliminating the need to design high level functions at the gate or cell level. This allows a designer to design his circuit using previously designed high level functions. Soft macrocells are a collection of standard cells configured to perform a given function and are represented hierarchically by a single component symbol. Upon expansion, the device's hierarchy is flattened. Thus, the soft macrocell's hierarchy is also flattened, and the macrocell is represented by its underlying cells which are indistinguishable from the circuit's other standard cell logic.

The 7400 Series Soft Macrocells are a set of 64 logic functions each of which is functionally equivalent to the standard TTL part of the same name. Each macrocell consists of a single, unique workstation symbol for use in schematic capture and the underlying collection of standard cell circuitry which implements the function.

Capturing Soft Macrocells

Single symbol capture of the 7400 Series Soft Macrocells eliminates the time and resources required to design and capture TTL functions (some of which may incorporate over 90 gates) at the gate or cell level. The 7400 Series Soft Macrocells also provide an efficient method for converting the functionality of a TTL–based printed circuit board design into a semicustom device. When converting TTL PC board designs to CMOS semicustom circuits, attention must be given to timing performance considerations.

The 7400 Series Soft Macrocells are available for use with all NCR ASIC libraries. The method used to capture the 7400 Series Soft Macrocells is identical to the method used to capture other NCR standard cells. The 7400 Series Soft Macrocells are part of NCR's Design Kits and are available on various platforms.

An example of a 7400 Series Soft Macrocell data sheet is shown on the next page. Each macrocell's data sheet includes the macrocell symbol, general description, equivalent gate count, a schematic drawing of the macrocell's underlying circuitry and other details pertaining to the specific macrocell. The macrocell's schematic drawing depicts the NCR standard cells and associated interconnections used to implement the macrocell's function.

The data sheet schematics show example standard cell instance numbers (I$#). In an actual design, each macrocell symbol is assigned a unique instance name and each standard cell used to implement each occurrence of a particular macrocell is assigned a unique instance name. As an example, on the Mentor Graphics™ workstation, each standard cell in a macrocell is assigned the instance name that appears in the data sheet schematics preceded by an occurrence letter that differentiates one macrocell from another.

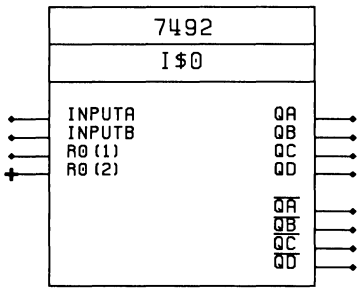
Divide by Two, Six, or Twelve Counter

Description

This counter contains a gated zero reset. When R0(1) and R0(2) are high, all of the counter outputs are low. To achieve a divide by twelve counter, connect output QA to INPUTB and apply count pulses to INPUTA. The output will be at QD. No modifications are necessary for the divide by two or six counters. The divide by two counter is clocked at INPUTA and the output will be at QA. The divide by six counter is clocked at INPUTB and the output will be at QD. The Q outputs and their complements are available.

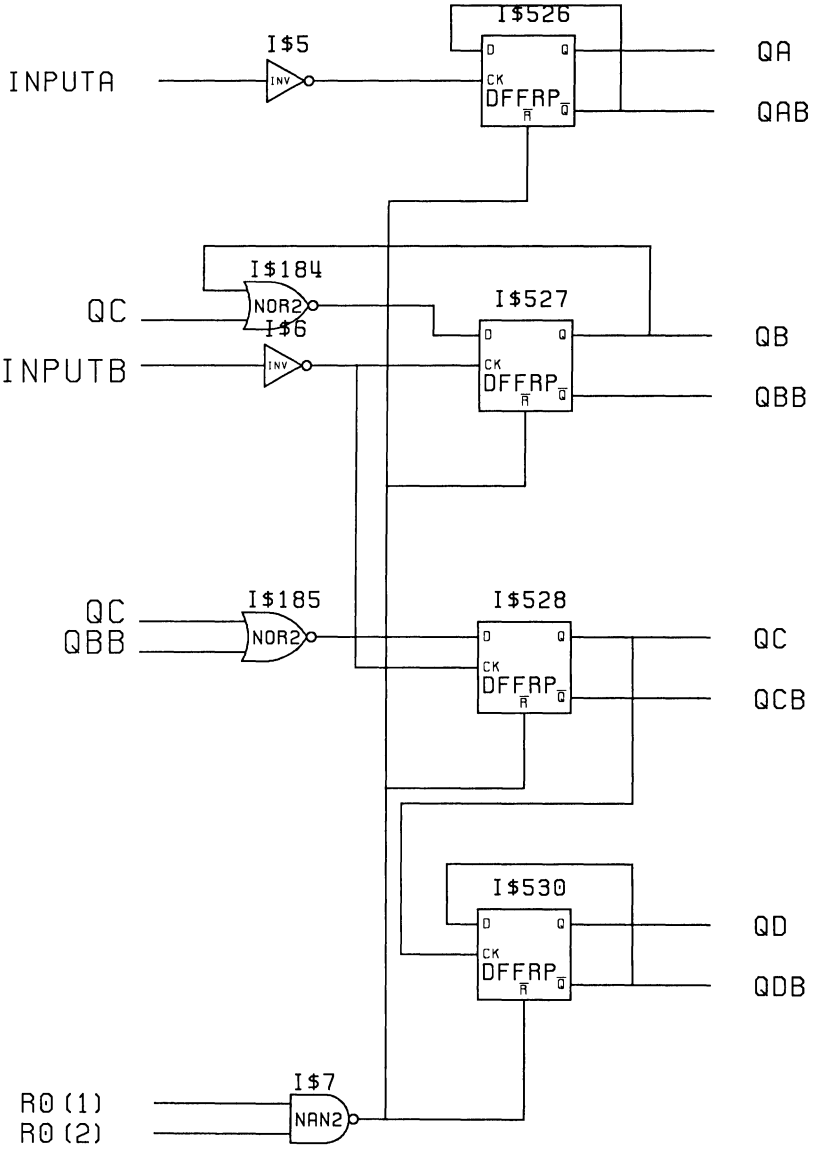
Name: 7492
Gates: 36.0

Symbol



Sample data sheet (1 of 2)

Schematic



Sample data sheet (2 of 2)

Design Considerations

Input and Output Pin Loading

Though not obvious when viewing a macrocell's top level symbol, some macrocell input and output pins are connected to more than one underlying standard cell component. Please refer to the sample data sheet shown on the previous page for examples of a macrocell output pin QAB which is connected to two macrocell internal cells.

A single macrocell input pin affects a connected output's fanout count by the number of fanouts associated with the underlying circuitry. A macrocell's input capacitance for any particular pin is determined by summing the input capacitance of each standard cell component connected to that pin. Likewise, a tristateable macrocell output loads a particular net according to the number and type of underlying cells connected to a given output. Macrocell output pins may be connected to one or more macrocell internal cells. Since the same rules pertaining to standard cell output pin loading apply to macrocells, and since the total fanout of a macrocell output is the sum of all connections to internal standard cells and external connections, the number of external fanouts available to the designer may be reduced. In the data sheet example, QAB is a macrocell output that is also connected to the D input of a macrocell internal flip-flop.

A review of specific macrocell data sheets will highlight inputs and outputs with internal connections. For more detail regarding input and output loading rules and other design considerations, please consult an NCR data book, an NCR workstation specific users' manual and the *NCR Semicustom Design Course* manual.

Function Exceptions

While NCR's 74xx Soft Macrocells are, in general, functionally equivalent to corresponding TTL functions, some exceptions do exist and are noted below. A macrocell's functional behavior may be verified using the workstation simulator. For further details, please refer to a specific macrocell data sheet or contact your local NCR sales office.

1. 74126, 74240, 74244, 74245. Because the delays on the enable lines are greater than the delays on the data lines, the enable signal to the TBUF standard cell components of these macrocells is delayed from the data line. Therefore, for the correct data to appear on the outputs, the input data must be present for some time after the enable signal transitions to an active state.

2. 74245. Because of the nature of certain workstation simulators, driving the data input of a 74245 from an input port connector may create an unknown condition if the simulator is not given a known data value at the instant that the enable lines are activated low, or if the input data is not defined for a period which completely includes the time that the enable input is activated.

3. 74151NS, 74157NS, 74161NE, 74163CP, -L, -LC, -LCP, 74193L0, L0001, 74195J, -S. 74244NT, 74374NT and 74374NTC. These macrocells are permutations of the standard parts and macrocells of the same number with additional or reduced features and functionality. Thus, while functional equivalence may be obtained by using the corresponding macrocells without the suffixes, these macrocells allow the designer to take advantage of other features not available on the standard part or to eliminate unused functions which would otherwise take up die space. Please refer to the respective data sheets for additional information.

4. 74373 and 74374. Schmitt trigger clock buffers, available on the standard parts, are not included in these macrocells but may be added external to the macrocells if so desired. Because of the limited noise exposure that a signal internal to a CMOS device realizes, the Schmitt triggers are generally not required.

Modifying Soft Macrocells

You may modify the macrocells to obtain additional functionality or to eliminate unused circuitry. You can verify the modified macrocell's functional behavior and timing performance by using the workstation simulator.

To modify the macrocell, the underlying schematic must be adjusted. If the modifications include adding, subtracting or changing an input or output, then the macrocell's symbol must also be modified. NCR recommends that the original, unaltered macrocell not be modified. Instead, copy the macrocell, rename it and change the copy accordingly. The procedure to modify a macrocell's symbol and schematic varies according to the workstation in use. Therefore, you should refer to the applicable workstation user's manual for details. As an example, the Mentor Graphics™ workstation procedure is as follows:

1. Make a copy of the pertinent macrocell into your working directory.
2. Change the name of the macrocell to more accurately reflect its intended functionality. If the macrocell's original name is maintained, you may inadvertently reference the original. Therefore, a name change is strongly recommended.
3. Enter the symbol editor and edit the symbol as required. Edit only the version of the macrocell located in your working directory.
4. Exit the symbol editor and enter the schematic editor.
5. Modify the macrocell circuitry as required. Remember, the symbol I/O lines (pin properties) must correlate to the schematic I/O lines (net names).
6. Instantiate the macrocell symbol into the schematic. Be sure to reference the modified version located in your working directory.

Simulation and Testability

As with other hierarchical design components, the designer may desire to implement a test mode that allows test vectors to have direct access to an isolated macrocell. A designer may create simulation patterns which exercise the macrocell separately from the remainder of the logic and may create other patterns to verify the macrocell's interaction with other design components. As with other standard cells, testability is greatly enhanced if the macrocell's internal states (e.g. flip-flops) can be controlled and forced into known states upon power up. Therefore, the designer has the ability to fully verify the performance of the macrocell either separately or in conjunction with the other design logic, and to optimize the design's and macrocell's testability.

Discussion of Testability

The ever increasing complexity of ASIC designs continues to reiterate the need to design testable circuits. If circuits are to be testable, test requirements must influence the design procedure from the start of the development process. Test issues must be discussed and resolved beginning with the conceptual design phase and continuing through final, post-layout simulations.

Two major concepts pervade all design for testability (DFT) schemes: controllability and observability. Controllability is the ability to establish the circuit into a controlled initial state by applying stimuli at the device's input pins. This initial state is such that from it all future states can be predicted. Observability is the ability to observe, through the primary outputs of the device, the internal states and internal signals of a circuit.

Similarly, a node internal to a device is controllable if it can be forced to all logic levels (0, 1, and high impedance) by applying stimuli at the input pins of the device. An internal node is observable if the value of a node at all levels (0, 1, and high impedance) can be observed at the device outputs.

Design for Testability Approaches

Design for testability (DFT) techniques involve increasing the controllability and observability of the constituents of a design. All DFT techniques can be categorized to contain one or more of the following methods:

Test Points

Test points are defined as poorly controllable and/or poorly observable nodes. Identification of these test points can be achieved either by checklist and/or by using a software program that computes testability measures. The testability analysis programs attempt to quantify a testability measure of a design.

Once test points are identified, the next step is to modify the basic design by providing a logical access to these test points through the device's primary inputs and/or outputs. With the limitations in the number of primary inputs or outputs, additional control logic such as decoders, multiplexors and shift registers can be used to provide additional test points. Control signals such as clocks, presets, clears and tristate enables, and observation signals such as data inputs to storage devices, global feedback signals, internal control signals and outputs from combinational devices such as encoders, multiplexors and parity generators are good candidates for test points.

An example is shown in Figures 9-86 and 9-87. In Figure 9-86 the inputs of the embedded block B are difficult to control and the outputs of block B are difficult to observe. By incorporating multiplexors at block B's inputs and de-multiplexors at block B's outputs (as shown in Figure 9-87) the controllability and observability of block B has increased.

Partitioning

An increase in the circuit complexity of VLSI chips and higher levels of integration results in an increase of testing difficulty. The testing time of a circuit is related to the cube of its complexity. Therefore testing complexity is reduced by dividing the circuit into parts which may be tested individually, in modules. For example, testing one half of a circuit takes approximately one-eighth of the time required to test the whole circuit Partitioning increases the observability and/or controllability of the constituents of a design by decomposing the overall design into more manageable elements for test purposes. Some of the partitioning techniques available are:

- Natural Partitioning. Natural partitioning is found by the analysis of system blocks in VLSI design and the availability of design methodologies that include supercells such as RAM, ROM, microprocessors and microcontrollers

An advantage of system block partitioning is the ability to reuse test program modules developed for common block types. Use of multiplexors and de-multiplexors to access block B of the above example creates direct access to block B. As a result, the test program that was developed for block B can be applied directly and repeated for any other occurrences of block B.

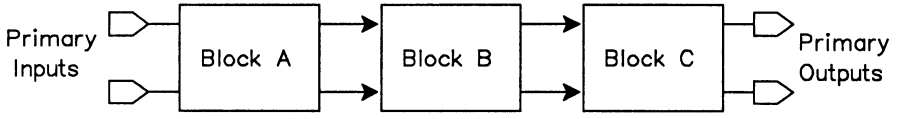


Figure 9-86 Network partitioned into three subnetworks

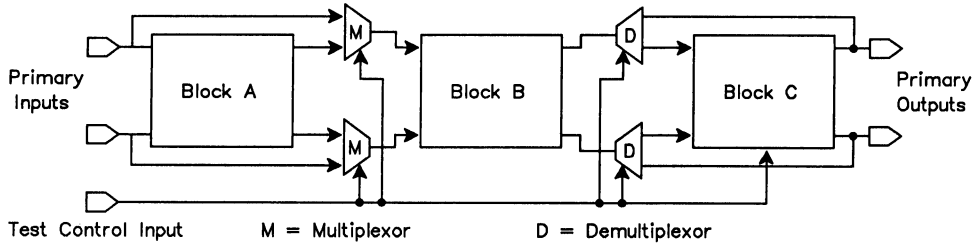


Figure 9-87 Direct access for testability improvement

- Partitioning created by adding DFT structures. DFT techniques such as scan path and LSSD structures partition the circuit into one or more shift registers and a collection of purely combinational logic thus creating a more testable device than standard synchronous design structures.
- Partitioning by bus architecture. Bus architecture provides visibility to and from circuit elements that are tied to the bus. To take advantage of this approach, the bus must be accessible to the device's primary inputs and outputs. Via the bus, circuit blocks may be accessed individually and tested as modules. For example, an internal ROM connected to a bus that is directly accessible to the device's pins may be verified by reading its contents onto the bus and comparing the value of the bus via the device pins to a correct copy of the ROM.

Scan Design

Scan design techniques connect the state storing elements of a design (not including RAM, ROM EEPROM, etc.) into one or more shift registers that provide the ability to scan data into and out of the circuit. Scan design alleviates the reliance on internal logic to generate latch input since the latch data can be input and controlled externally. This capability provides completely observable and controllable access to the state of the circuit.

Access to the data can be accomplished in two ways. The first access method connects a design's state elements into a serial shift register that, via input multiplexors provides the ability to serially shift test data in and out of the device. The second method, random access scan, uses an addressing technique that allows each storage element to be individually and randomly selected.

While scan methods improve the testability of a device they do increase a device's design and manufacturing cost by increasing die size (generally from 5 to 25%) and affecting performance.

Automated tools are commercially available that minimize die size and performance penaltics while attempting to maximize testability.

There are several different versions of scan design techniques that are being used in the industry. Some of these techniques are:

Level Sensitive Scan Design (LSSD)

LSSD is a serial scan DFT approach that uses latches for memory elements. To ensure race-free system operation and testing, the LSSD technique is based on the following concepts:

- Logic design is implemented in accordance to a set of rules that are outlined in LSSD reference manuals. As a result of these rules, operation of the circuit is insensitive to AC characteristics such as rise time, fall time, and the minimum delays associated with an individual gate.
- The basic memory element must be a level-sensitive, two input port latch that is hazard-free and race-free. This latch is connected to additional gates including another single port latch. This additional logic is used to chain the system memory elements into a shift register. An example of a shift register latch (SRL) is shown in Figure 9-88. An SRL is composed of two latches L1 and L2. L1 is generally used to store normal data, while L2 is used for shift register linkage as shown in the next figure. Non-overlapping clocks are used for shifting clock signals A and B. The L2 latch can be used by the designer for other circuit functions thus minimizing increases in silicon area associated with the test logic.

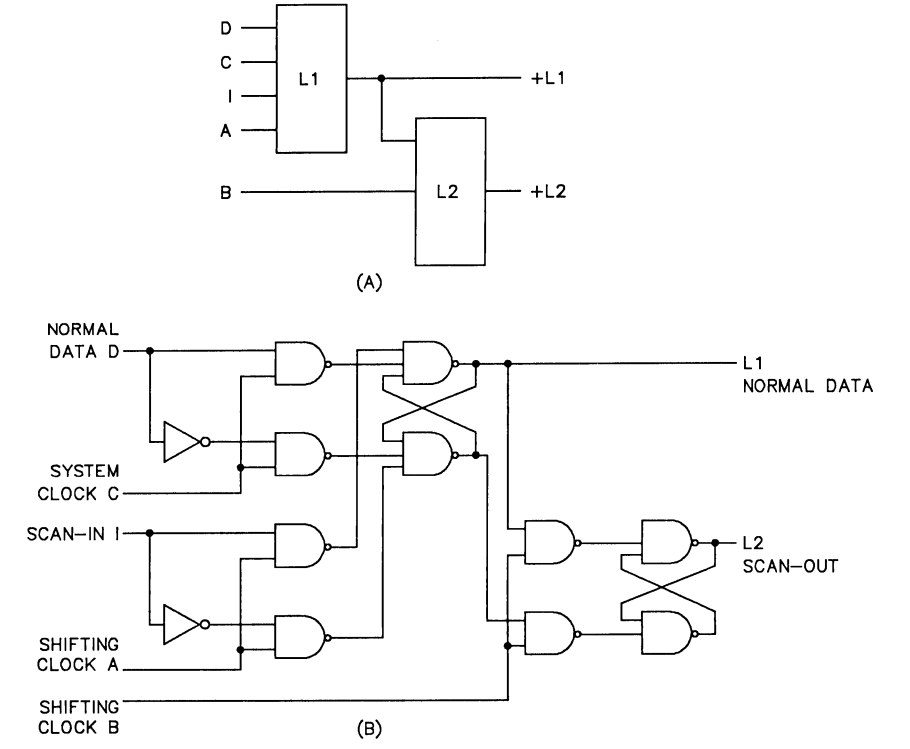


Figure 9–88 Shift register latch, (A) symbolic representation, (B) NAND gate implementation

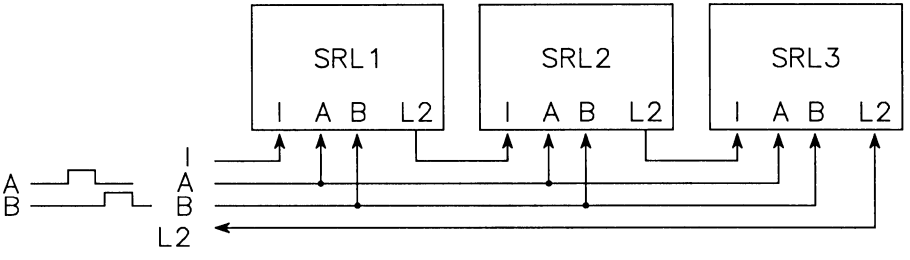


Figure 9–89 Linking several SRLs

Scan Path

The scan path design technique uses the same design methodology as LSSD but does not use level-sensitive memory elements. Scan path uses only one system clock and scan path designs can be exposed to race conditions. This exposure can be easily minimized by using careful design rules regarding synchronous operations.

As shown in Figure 9-90 a two-to-one multiplexor can be added at each data input of a memory element (e.g. edge-triggered D flip-flop). The result is an equivalent of an SRL with one clock. Similar techniques can be applied to other types of memory elements, such as J-K flip-flops.

To implement the scan path technique, each memory element in a circuit is modified by replacing each regular memory element with a data-multiplexed storage element. The output of each memory element, in addition to the system logic, is connected to the next memory elements test data input. A test mode signal selects whether the normal system data or test data are latched into each memory element. Thus, the circuit's memory elements are daisy chained together to form a shift register. Scan path design rule checking should be applied to the modified circuit to ensure correct scan design techniques and race-free operation. An example is shown in the following figures.

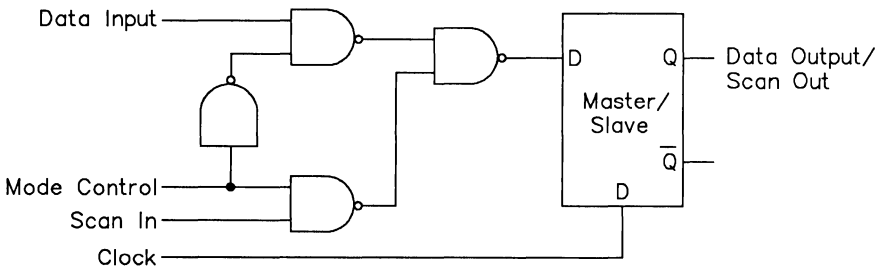


Figure 9-90 D-type master-slave flip-flop with scan capability

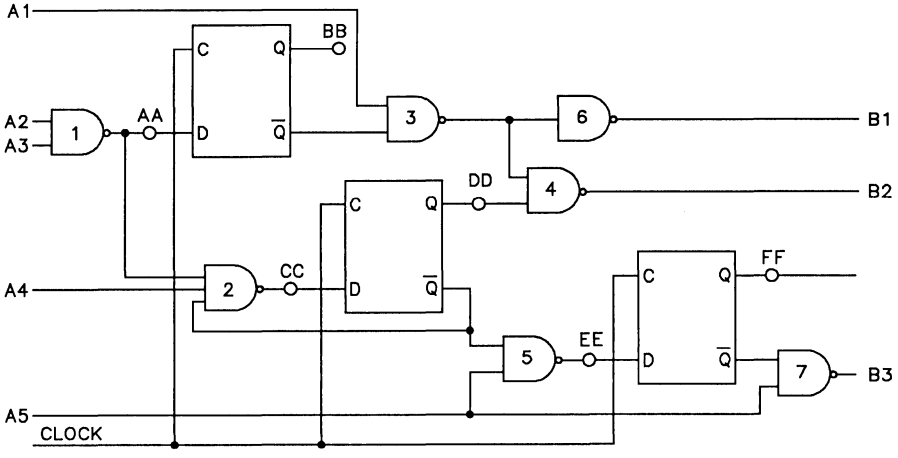


Figure 9–91 Sequential network with a sequential depth

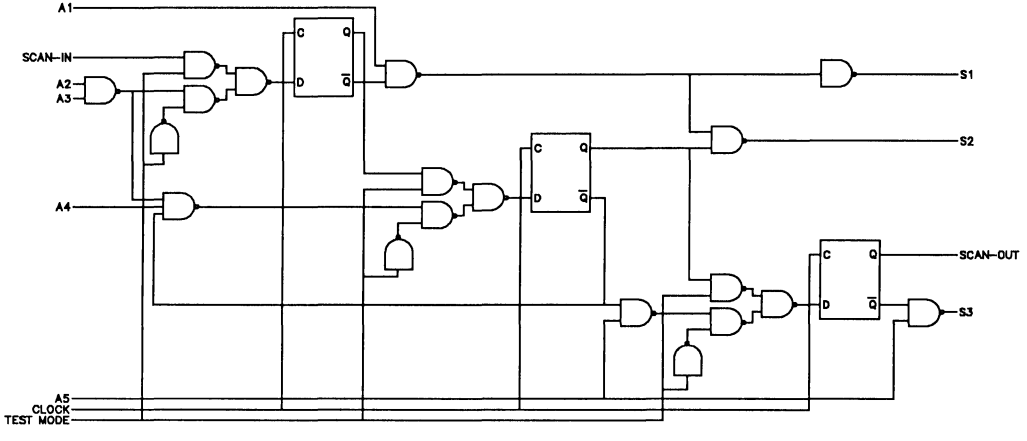


Figure 9–92 Sequential network with complete scan path

Self Test

Built in self-test (BIST) uses tools and techniques in the design and the implementation process to give a chip the ability to test itself by generating its own test patterns and compressing the results to indicate whether the chip is good or bad.

Like scan techniques the designer faces a trade-off between testability and die size increases/performance decreases associated with the test logic. Figure 9-93 depicts a general self-test approach.

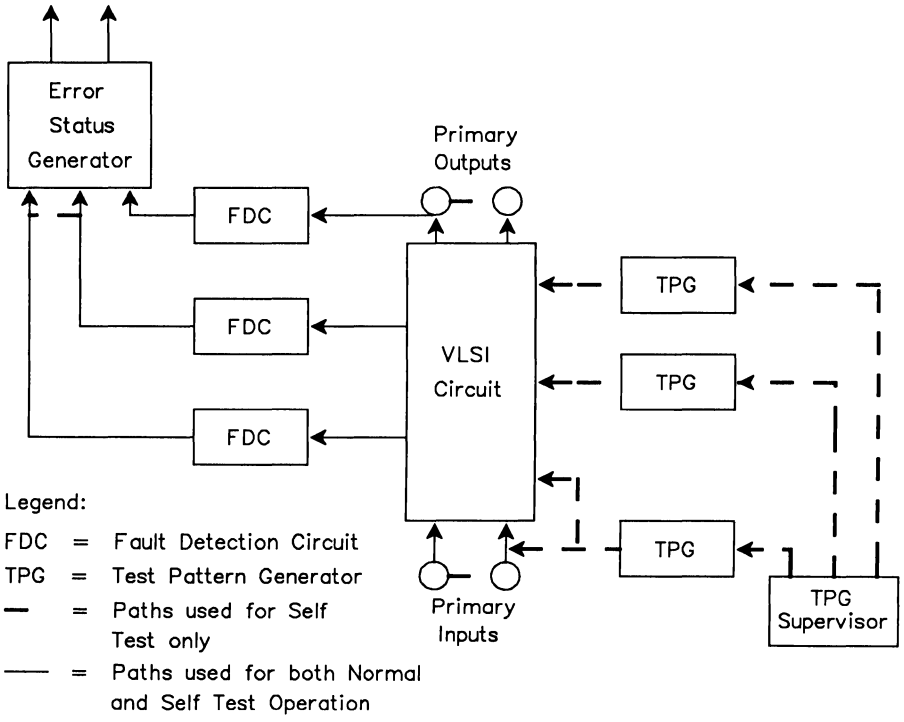


Figure 9-93 General self test approach

Most BIST approaches utilize scan type design techniques. The following figure shows a general approach to BIST. There are four general resources that can be included on the chip. The two basic resources are:

Test Pattern Generators (TPG)

TPGs are used to provide stimuli to the circuit under the control of the TPG Supervisor. For a large circuit, partitioning will provide smaller silicon overhead for TPG implementation. The following are examples of TPGs:

- Counters/state machines: Provide somewhat deterministic stimuli.
- ROM: Can store a limited number of deterministic stimuli.
- Linear Feedback Shift Register (LFSR): Generates a random sequence of stimulus vectors. It allows a large number of stimuli to be generated and applied to a circuit without requiring a large silicon area to store them. A large number of randomly generated patterns are required to achieve a given fault coverage. BIST approaches can require long test times, but minimal test equipment.
- Fault Detection Circuit (FDC): FDC detects faults in the circuit and feeds them into the error status generator for analysis. Some uses of Fault Detection Circuitry are:
  - ROM can be used to store test results; with a comparator, fault detection can be accomplished
  - LFSR is used as a data compressor that develops a compressed syndrome of test results. This syndrome (or signature) can then be compared by the error status generator to a stored value. A multiple input implementation of LFSR, called multiple input signature register (MISR), is shown below.

By adding a few gates to an LFSR a multifunctional register is obtained. The new structure is called a Built In Logic Observer (BILBO) register. One implementation is shown below.

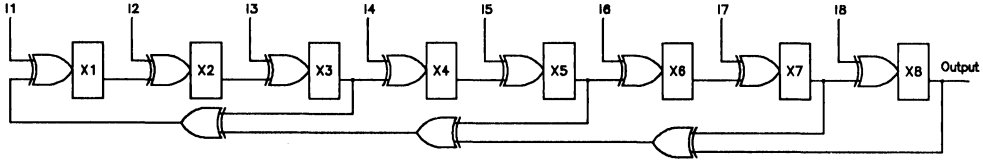


Figure 9-94 Multiple input signature register

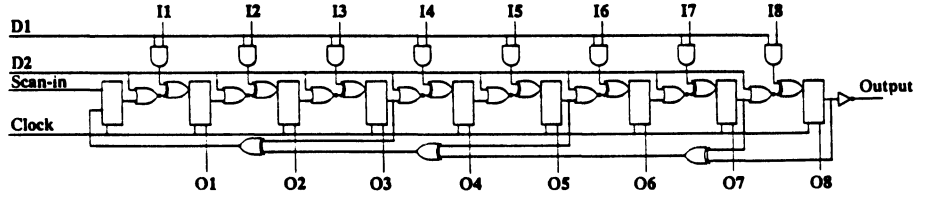


Figure 9-95 A multifunctional register

Guidelines for Improving Testability

The following are general guidelines for improving the testability of semicustom devices:

- Design using dedicated test pins to monitor critical nodes of the circuit. If no dedicated test pins can be made available, it may be possible to replace some output buffers with bidirectional buffers and use the newly created inputs as test inputs. The same method may be used with input buffers to create test outputs. Also, output pins may be multiplexed between normal circuit functions and test-circuit functions.

- As a last resort, when the above methods cannot be used, it may be possible to use the normal circuit inputs for testing. This is done by using input logic combinations that will not occur under normal circuit operations and internally decoding them as test modes.

- Use test pins to exercise the I/O buffers independently of the internal logic.

- Design using dedicated test logic to provide and control such functions as reset, tristate output enable, preset, data-bus enable, or other means of initializing and controlling the states of the logic. Do not design flip-flops, registers, latches, and counters to which there is no access for initialization.

- Partition large circuits into smaller, more manageable circuits that will allow the use of control and test logic.

- Design using synchronous logic. Asynchronous designs can exhibit race conditions that vary as IC processing varies and may not appear on CAD simulations. Do not allow any unclocked feedback paths, such as those found in ring oscillators.

- Design so that the circuit does not depend upon internal propagation delays for timing. Such delays will be unreliable, and race-condition problems may arise:

  - Avoid race conditions to cells (such as between data and clock, reset and clock, preset and clock, or preset data and preset enable).
  - Avoid using internal gate delays to create pulses. Specified minimum pulse widths are in the 20 to 30 nanosecond range, but typical minimum pulse widths vary widely as a function of processing.
  - When using more than one clock, design for the worst-case skewing between clocks.

- Avoid having large fanouts on edge-sensitive cell inputs. A large fanout causes slow rise and fall times, which may result in oscillations, circuit timing problems, or excessive current draw. The maximum rise and fall times that should be seen by the inputs of any cell is 500 nanoseconds.

- Design so that tristate cells do not remain in the high-impedance state for an indefinite period of time. This will prevent the cell, and subsequent cells that are driven by the tristate cells, from drawing current unnecessarily and possible losing data. Use several pairs of power-supply (V_{DD} and V_{SS}) pins, especially in designs with high I/O counts.

- During functional and AC simulation, observe several internal nodes, to ensure that the circuit is function as desired.

- To avoid long counting sequences during simulation and testing, design counters so that they are broken up, with each section separately presettable. This allows simulation and test steps (vectors) to be used for simulation and testing; not for counting.

- Insert test logic into state machines. Large state machines should be designed so that they may be broken up into smaller blocks similar to counters.

- One important simulation function is to ensure that the device can be tested by wafer-probe and final-test equipment. Race conditions may exist not only because of design flaws, but also because of IC tester limitations. Ideally, a test system would simultaneously apply all input test vectors and later compare circuit outputs with simulation results. Actually, IC testers can have more than 20 nanoseconds of skew between needle points (bonding pads) at wafer probe. For this reason, a circuit that simulates properly and is designed for proper flip-flop setup and hold times can fail at wafer probe or final test. Designers should be aware of the possibility of test race conditions and should define test vectors accordingly. When specifying timing relations, try to allow enough margin to take into account the possible skew of the tester. When using more than one clock, design for worst-case clock skew. To avoid skewing problems, do not change any input signal to a clocked cell on the active clock edge.

A designer needs to maintain awareness of the tester limitations and design his device with the applicable constraints in mind.

- Simulation (and test) vectors may be different from the input sequence of the actual system application. Initialize all storage elements at the beginning of the simulation (and test) sequences. Do not clock a cell and change the data on the same vector. Do not clock cells or change data on the vector after a reset or enable signal has been removed. There may not have been sufficient recovery time, and the new data may not get clocked in. Unpredictable simulation results may occur.

- Within workstation simulators it is possible to initialize any or all circuit storage elements using some form of a set or reset command. IC tester does not have this automatic initialization capability. In actual operation, when powered up, the storage elements can be in either a set or reset state, and this power-up state can change from circuit to circuit. A simulation test pattern that depends upon initialized storage elements will almost certainly fail actual test at wafer probe or final test. Initialization should be accomplished by input stimuli.

- Do not design using flip-flops that self-initialize; or otherwise have the circuit provide the logic necessary to put the output into a desired state. Problems arise because the tester is not able to do the same initialization procedure. Therefore, use controllable flip-flops such as resettable D flip-flops.

- Try to always drive device inputs and bidirectional pins when in input mode. Extended periods of high impedance during testing could cause generation of excessive currents.

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Timing Calculations for VS700 Standard Cell and VGX700 Gate Array Libraries

Introduction

Accurate Precision Model Technology is implemented by NCR's ViTa5 (VLSI Timing Analysis, fifth generation) software which uses a timing algorithm that is much more accurate than previous tools. The increased accuracy is achieved by accounting for the input rise and fall time effect on cell delay times. Inherent in the increased accuracy is an increase in the complexity of the algorithm itself. This application note explains how the Accurate Precision Model Technology is implemented. Please keep in mind that you will not have to perform these calculations yourself, the NCR software does this for you.

For use in comparing cell timings, each data sheet contains a Timing characteristics table (see item 1 in the sample data sheet), which gives the cell delay for a typical input waveform and output load capacitance. For internal cells, load capacitance conditions which represent an inverter driving two 2-input NAND gates are specified. The cell timings are provided at nominal, worst case commercial, worst case industrial, and worst case extended operating conditions.

The Cell Equation

The delay time for any signal through a cell consists of two components. The first component is the base delay, which assumes a square wave input signal. Base delay is a function of the delay coefficients for a particular cell (see sample data sheet item 2) and the total output load capacitance the cell is driving. Output load capacitance is the sum of all cell input capacitance due to fanout, the capacitance of any tristate output pins, and either the estimated prelayout capacitance or the actual post-layout capacitance provided by NCR.

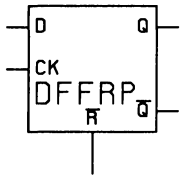
The second component of delay time is the added delay due to the actual rise and fall time of the input signal. A rise/fall time correction must be added to the base delay to determine an accurate propagation delay for each cell. See Figure 9-96 for the relation between base delay and corrected delay. The applied correction is determined from the output rise/fall time of the driving cell and the sensitivity of the cell under analysis to the rise/fall time. The input rise/fall time is calculated from the Rise/Fall time coefficients table of the driving cell (see item 3 of the sample data sheet), whereas the rise/fall sensitivity for the cell under analysis is given by the correction multiplier parameters MCLH and MCHL (see sample data sheet item 4).

D Flip–Flop with Reset, Positive Edge Triggered

DFFRP is a fully static D-type edge triggered flip-flop. It is positive edge triggered with respect to CK. RB is asynchronous and active low.

Inputs: RB, D, CK
Outputs: Q, QB
Input Cap.: RB: 0.162
D, CK: 0.081 pF
Timing Constants: K = 0.08ns
M_{CLH} = 0.074 M_{CHL} = 0.066
Process Derating: B = 0.66 N = 1.00 W = 1.40
Cell Size: 8.00 gates, 22 array sites

4



FUNCTION TABLE

D	CK	RB	Q	QB
L	↑	H	L	H
H	↑	H	H	L
X	X	L	L	H

(Input t_r,t_f= 0.5ns nominal, C_L= 0.16pF)

SYMBOL	PARAMETER	NOMINAL V_{DD}=5V	WORST CASE PROCESS V_{DD}=4.5V		
		T_A=25C	T_A=70C	T_A=85C	T_A=125C
t_{PLH}	CK to Q	1.17	2.19	2.28	2.56
t_{PHL}		1.06	1.98	2.07	2.32
t_{PLH}	CK to QB	1.40	2.61	2.72	3.05
t_{PHL}		1.35	2.53	2.64	2.96
t_{PHL}	RB to Q	0.710	1.33	1.39	1.56
t_{PLH}	RB to QB	1.04	1.94	2.03	2.27

Timing characteristics 1

SYMBOL	PARAMETER	NOM. PROCESS, 5V, 25C DELAY COEFFICIENTS	
		A	B
t_{PLH}	CK to Q	0.947	1.20
t_{PHL}		0.891	0.885
t_{PLH}	CK to QB	1.18	1.16
t_{PHL}		1.22	0.651
t_{PHL}	RB to Q	0.563	0.745
t_{PLH}	RB to QB	0.821	1.16

Delay coefficients 2

Sample VS700 data sheet (1 of 2)

DFFRP

Use the rise/fall time coefficients to calculate the input rise or fall time for any cell driven by this cell. See Timing Equation application note.

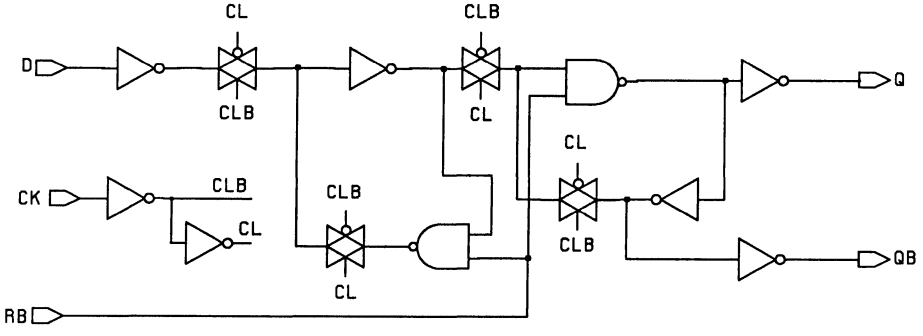
OUTPUT PIN	NOMINAL PROCESS, 5V, 25C			
	RISE TIME COEFFICIENTS		FALL TIME COEFFICIENTS	
	R1	R2	F1	F2
Q	0.339	2.49	0.434	0.935
QB	0.304	2.50	0.363	0.848

Rise/Fall time coefficients for the next cell (3)

Minimum Specifications (ns)

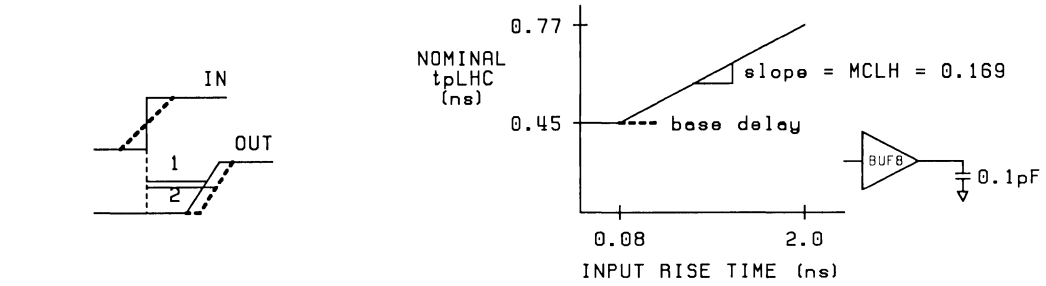
SYMBOL	PARAMETER	WORST V_{DD}=4.5V T_A=70C	NOMINAL V_{DD}=5.0V T_A=25C	BEST V_{DD}=5.5V T_A=0C
t_{su}	Setup Time D to CK	0.853	0.500	0.306
t_h	Hold Time CK to D	−0.341	−0.200	−0.122
t_{pwh}	Pulse Width (high) CK	3.34	1.96	1.19
t_{pwl}	Pulse Width (low) RB	3.14	1.84	1.12
t_{pwl}	Pulse Width (low) CK	3.73	2.19	1.34
rt	Recovery Time RB	1.54	0.900	0.550

Timing requirements (5)



Functional diagram: DFFRP

Sample VS700 data sheet (2 of 2)



a) Input rise/fall effect
1: base delay with square wave input
2: delay corrected with rise/fall time

b) Relation between input rise time and delay for a VS700 cell

Figure 9-96 Input rise/fall effect on delay time

The simplified form of the timing equation is:

Propagation Delay = Base Delay + Rise/Fall Correction

The actual equation used by ViTa is:

Delay = (A + B * CL) * DFn + MC * max[0, (RFT * DFn-1 - K)]

--- Base Delay --- ----- Rise/Fall Correction -----

The parameters of this equation and how they are used by ViTa will be explained in subsequent sections of this application note. Please see the Glossary of Timing Model Parameters at the end of this application note for a handy reference on the complete timing equation.

Base delay

Base delay is the delay through a cell assuming an ideal square wave input signal. The base delay is calculated using the delay coefficients A, B (see sample data sheet item 2) and the total load capacitance (CL) on the relevant output. This portion of the delay is calculated using a linear equation of the form Y = mX +b or Delay = A + B*CL.

The base delay equations are:

tpLH = A1 + B1 * CL

tpHL = A2 + B2 * CL

where

tpLH is the base delay from when a changing input reaches the threshold of the cell to when the rising output reaches the threshold of the cell that it is driving.

tpHL is the base delay when the output is falling

A1, B1 are the cell specific delay coefficients used in the tpLH equation

A2, B2 are the cell specific delay coefficients used in the tpHL equation

CL is the total capacitance at the output of the cell under analysis. CL is the sum of all cell input capacitance due to fanout, any tristate output capacitance, and either the estimated prelayout capacitance or the actual post-layout capacitance provided by NCR.

The logic threshold voltage of a cell is defined as the voltage level at the input required to make the output transition. Unless otherwise stated in the data sheets, the threshold voltage for all cells is at 50% of the V_{DD} supply. Therefore, in most cases, tpLH and tpHL are measured from when the input reaches 50% of V_{DD} to when the output reaches 50% of V_{DD}. Output pad cells, while still having a threshold voltage of 50% of V_{DD}, are designed to be TTL compatible and are assumed to drive external circuitry with a 1.4 volt threshold voltage. Therefore, delays for output pads are measured from when the input reaches 50% of V_{DD} to when the output reaches 1.4 volts. Input pads drive either an INBUF, which have a 1.4 volt threshold, or a Schmitt trigger (DSxxyy), which have hysteresis and thresholds that are transition dependent. For these special cells, timings are measured from when the input reaches the logic threshold to when the output reaches 50% of V_{DD}.

Rise and fall correction of the base delay

The corrected cell delay is equal to the base cell delay plus a rise/fall time correction factor. The rise and fall time correction is added to the base delay to account for the fact that rise and fall times in actual circuits are not ideal. The rise/fall time corrections are calculated uniquely for each node of a circuit. The correction term in the delay equation considers the sensitivity of each cell to changing input rise and fall time, the calculated rise/fall time of the output of the driving cell, and the rise/fall time used during the characterization of the cell's base delay.

The complete equations used by ViTa are:

For non-inverting cells:

$$tpLHC = tpLH + MCLH * \max[\ 0, (\ RT - K\ )\ ]$$
$$tpHLC = tpHL + MCHL * \max[\ 0, (\ FT - K\ )\ ]$$

For inverting cells:

$$tpLHC = tpLH + MCLH * \max[\ 0, (\ FT - K\ )\ ]$$
$$tpHLC = tpHL + MCHL * \max[\ 0, (\ RT - K\ )\ ]$$

where

tpLHC and tpHLC are the corrected delay times

tpLH and tpHL are the base delay times

MCLH and MCHL are the Timing Constant factors (see sample data sheet item 4) for rise/fall sensitivity of the cell under analysis

RT and FT are the rise and fall times on the input of the cell under analysis (see the next section to calculate RT and FT)

K is the standard rise and fall time used during cell characterization (a constant).

max is a function which returns the maximum of two arguments. The base delay is not corrected if the rise or fall time is less than K.

In order to take full advantage of process capability, the VS700 and VGX700 libraries were characterized using two different input rise/fall times. A rise/fall time (K), which approximates an ideal square wave, was used to extract values in the Delay coefficients tables. A second input with a longer rise/fall time was used to characterize the MCLH and MCHL parameters. This dual characterization allows NCR to offer the maximum possible library performance with a high degree of simulation accuracy.

Cell input rise and fall time calculations

The rise/fall time on the input of a cell is equal to the rise/fall time on the output of the (previous) driving cell. Therefore, the input rise and fall times (RT and FT) are calculated from the Rise/Fall time coefficients table of the driving cell. Rise and fall coefficients model the 10 to 90% of V_{DD} transition times with a linear equation:

RT = R1 + R2 * CIN

FT = F1 + F2 * CIN

where

RT and FT are the calculated rise/fall times on the input of the cell under analysis. RT and FT are equal to the rise/fall time on the output of the driving cell.

R1 and R2 are the Rise Time coefficients (see sample data sheet item 3) from the data sheet of the cell driving the cell under analysis

F1 and F2 are the Fall Time coefficients (see sample data sheet item 3) from the data sheet of the cell driving the cell under analysis

CIN is the total load capacitance on the output of the driving cell, which is the same as the total capacitance on the input of the cell under analysis.

The important point to remember about rise and fall time calculations is to use the Rise/Fall time coefficients from the previous (driving) cell, not the cell for which you are calculating the delay. In the case of multiple drivers on buses, ViTa calculates the rise and fall times for the worst case (slowest) driver on the bus.

Compensating delays for variations in process, temperature, and voltage

The delay coefficients in the data sheets provide equations to calculate delay at nominal operating conditions, i.e., 25 degrees centigrade, 5.0 volts, and nominal process. In order to adjust nominal delays for the extremes of your particular operating range, ViTa uses a performance derating factor to increase and decrease delay from the nominal condition. The effects of operating voltage, temperature, and process are multiplicative. Therefore, the derating factor is calculated as:

DF = PDF * TDF * VDF

where

PDF is the process derating factor

TDF is the temperature derating factor

VDF is the voltage derating factor

The temperature and voltage factors are consistent from cell to cell in both VS700 and VGX700 libraries and are listed in Table 9–20. Process derating factors are listed in the data sheet for each cell. In most cases, process derating is also consistent from cell to cell. These values are also listed in Table 9–20. However, a few cells are less sensitive to process variation than are others. The overall derating factor (DF) is automatically calculated by ViTa when you select an operating point during simulation.

Timing requirements for clocked cells (see item 5 in the sample data sheet) are guardbanded differently than are cell delays. Therefore, timing requirements have different derating factors, as listed in Table 9–20. These requirements are given over commercial operating ranges in the data book. To calculate the worst case extended specifications, simply multiply the values in the worst case column by the 125 to 70 degree conversion factor of 1.17 (1.38/1.18 = 1.17). Likewise, best case extended values can be calculated by using the −55 to 0 degree conversion factor of 0.77 (0.71/0.92).

PARAMETER	CONDITIONS	DERATING FACTOR
Process Variation		
* Cell Propagation Delay:		
Worst Case	+ Process Deviation	1.40
Typical Case	Nominal Process	1.00
Best Case	− Process Deviation	0.66
** Timing Requirements:		
Worst Case	+ Process Deviation	1.28
Typical Case	Nominal Process	1.00
Best Case	− Process Deviation	0.73

TABLE 9–20 Derating factors for the VS700 and VGX700 Libraries

PARAMETER	CONDITIONS	DERATING FACTOR
Voltage		
Worst Case	4.5 volts	1.13
Typical Case	5.0 volts	1.00
Best Case	5.5 volts	0.91
Temperature		
Worst Case Extended	125° C	1.38
Worst Case Industrial	85° C	1.23
Worst Case Commercial	70° C	1.18
Typical Case	25° C	1.00
Best Case Commercial	0° C	0.92
Best Case Industrial	−40° C	0.76
Best Case Extended	−55° C	0.71

TABLE 9–20 Derating factors for the VS700 and VGX700 Libraries [continued]

NOTES:

* The process derating factors listed above apply to all VS700 standard cells except the POR, DLYCEL, all Schmitt triggers (DSxxyy), and all pullup and pulldown cells. These cells have tighter process derating factors. The data sheet lists the process derating factors for every cell.

** Timing requirement process factors apply only to the clocked cell parameters of setup, hold, pulse width, and recovery times. The same temperature and voltage derating factors apply to both timing requirement and cell propagation delay deratings.

The complete delay equation, including derating and rise/fall correction, takes the following form:

Delay = (Base Delay) * DFn + MC * max[0, (RFT * DFn−1 − K)]

where

Base Delay is the calculated base delay (tpLH or tpHL)

DFn is the derating factor for the cell under analysis

DFn−1 is the derating factor for the previous (driving) cell

RFT is either RT or FT, depending if the cell in inverting or not

MC is either MCLH or MCHL
K is the standard rise and fall time used during cell characterization

Note that DFn is the derating factor for the cell under analysis, and DFn−1 is for the driving cell. DFn does not necessarily equal DFn−1, but in most cases the two derating factors are equal.

Cells with dependent or complementary outputs

In order to minimize propagation delays, many cells were designed with a dependent output architecture. In these cells, the delay through one output depends on the load capacitance and delay through another path. For example, the VS700 DFFRP cell has two dependent output paths. The propagation delay from CK to QB depends on the CK to Q propagation delay and the rise/fall time of the Q output. The delay from RB to Q depends on the delay from RB to QB and the rise/fall time of the QB output. See Figure 9–97 for the DFFRP functional diagram.

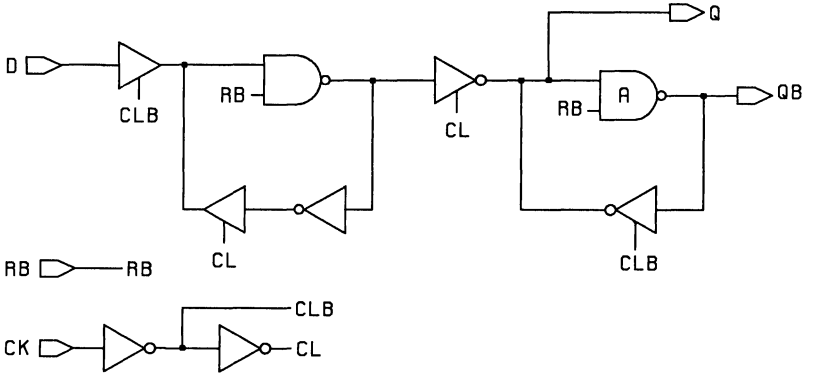


Figure 9–97 VS700 DFFRP functional diagram

The total delay CK to QB is equal to the CK to Q delay plus the Q to QB delay through the 2–input NAND gate A. Note the Q to QB delay is corrected with the rise/fall time on Q.

In order to calculate timings for delays through dependent outputs, ViTa first calculates the delay for the independent path and then calculates an incremental delay for the dependent path and adds this to the independent delay. For the DFFRP example, the CK to QB dependent delay is:

CK to QB = CK to Q + Q to QB (CK)

where

CK to Q is the independent delay calculated from a standard equation

Q to QB (CK) is the incremental delay dependent on the CK to Q delay

Likewise,

RB to Q = RB to QB + QB to Q (RB)

For dependent output delays, the rise/fall time on the independent output (Q for the CK to QB path and QB for the RB to Q path) is used to correct the base delay on the incremental path. See Example 3 for a detailed example of a dependent output delay calculation.

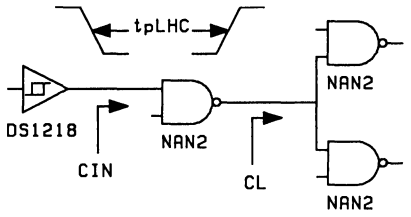
Please note that the delay coefficients provided for dependent delays are for calculation of the incremental delay, not the total delay through the path.

Example timing calculations

All examples shown below use timing numbers for the VS700 cell library.

Example 1: Calculation for NAN2 Nominal Delay Time Low to High

Consider the tpLH delay with rise/fall correction for a VS700 NAN2 cell. The NAN2 is being driven by a DS1218 and is driving 2 NAN2 cells as load.



Step 1: Calculate the NAN2 Base Delay

The NAN2 delay coefficients for the base delay are needed. From the data sheet, the base delay at nominal conditions is:

tpLH = 0.148 + 2.07 * CL

where the output load capacitance is due to cell capacitance and interconnect capacitance:

CL = sum(Cell Input Capacitance) + Fanout *(Prelayout Estimated Capacitance)

For this case, the load capacitance on the output of the first NAN2 is:

CL = (0.042 + 0.046) + 2 * 0.05 = 0.188 picofarads

Therefore, the NAN2 base delay is:

tpLH = 0.148 + 2.07 * 0.188 = 0.537 nanoseconds

Step 2: Calculate the rise/fall time of the driving cell

Since the NAN2 low to high output transition is driven by a DS1218 fall time, the fall time can be calculated using the fall coefficients from the DS1218 data sheet.

FT = 1.04 + 1.32 * CIN

For this case, assume the DS1218 is driving input pin 'A' of the NAN2 plus the estimated interconnect capacitance.

CIN = 0.046 + 0.05 = 0.096 picofarads

Therefore, the DS1218 fall time is:

FT = 1.04 + 1.32 * 0.096 = 1.167 nanoseconds

Step 3: Calculate the base delay rise/fall correction

The correction multiplier for the output low-to-high transition (MCLH) is required from the NAN2 data sheet in order to correct the tpLH base delay. (Note: Regardless of whether the cell is inverting or non-inverting, always use the MCLH parameter in the tpLH correction; likewise use MCHL in the tpHL correction).

MCLH = 0.244

The corrected delay for the NAN2 in this example is:

tpLHC = Base Delay + Rise/Fall Correction

= tpLH + MCLH * max[0, (FT - K)]

= 0.537 + 0.244 * max[0, (1.167 - 0.08)]

= 0.537 + 0.244 * 1.087

= 0.537 + 0.265

tpLHC = 0.802 nanoseconds

In this case, the correction is 26% (0.211/0.802 * 100%) of the total delay.

Example 2: Calculation at Worst Case Commercial Operating Conditions

To calculate Example 1 at worst case commercial operating conditions (worst case process, 4.5 volts, and 70 degrees centigrade), the combined derating factor for each cell must be calculated.

DFn = PDF * TDF * VDF
= 1.40 * 1.18 * 1.13 = 1.87 (for the NAN2 delay)

DFn−1 = PDF * TDF * VDF
= 1.31 * 1.18 * 1.13 = 1.75 (for the DS1218 driving cell)

The NAN2 tpLHC with the proper derating factors for each cell is:

tpLHC = (Base Delay) * DFn + MCLH * max[0, (FT * DFn−1 − 0.08)]

= 0.537 * 1.87 + 0.244 * max[0, (1.167 * 1.75 − 0.08)]

= 1.004 + 0.244 * 1.962

tpLHC = 1.483 nanoseconds

Example 3 : Cell Delay with Dependent or Complementary Outputs

Many standard cells were designed with dependent output architecture in order to minimize propagation delay through the cell. As an example, the DFFRP cell has two dependent output paths. The propagation delay from CK to QB depends on the CK to Q delay and output rise/fall time. Also, the delay from RB to Q depends on the RB to QB delay and rise/fall time. For the DFFRP, the delays in the Timing characteristics (tc) table are calculated from the Delay coefficients (DC) table in the following manner:

CK to QB (tc) = CK to Q (DC) + Q to QB (CK) (DC)
RB to Q (tc) = RB to QB (DC) + QB to Q (RB) (DC)

The last term in each of the above equations represent the incremental delay for each path, as evident in the functional diagram of Figure 9–97.

For simplicity, assume that a DFFRP cell is being driven with a 0.5 nanosecond rise/fall time (10–90% of VDD) at nominal conditions, and both the Q and QB outputs are loaded with a 0.1 picofarad load capacitance. These conditions match the convention used in the Timing characteristics tables for all internal cells in the VS700 library. The CK to QB delay with QB going low to high is:

tpLHC (CK–QB) = tpHLC (CK–Q) + tpLHC (Q–QB)

The CK to Q term is calculated using the standard delay equation.

tpHLC = A + B * CL + MCHL * (TR – K)

tpHLC (CK–Q) = 0.892 + 1.65*0.1 + 0.167 * (0.5 – 0.08) = 1.13 nanoseconds

Notice this value matches the entry in the DFFRP Timing characteristics table.

In order to correct the Q to QB tpLH delay, the fall time on Q must be calculated.

TF (Q) = 0.440 + 2.69 * 0.1 = 0.709 nanoseconds

Therefore, the corrected tpLH of the Q to QB path is:

tpLHC = A + B * CL + MCLH * (TF – K)

tpLHC (Q–QB) = 0.293 + 2.13 * 0.1 + 0.170 * (0.709 – 0.08) = 0.613 nanoseconds

The total CK to QB delay is sum of the CK to Q and Q to QB delays.

tpLHC (CK–QB) = 1.13 + 0.613 = 1.743 nanoseconds

This value also matches the entry in the DFFRP Timing characteristics table.

Glossary of timing model parameters

PARAMETER (units)	DEFINITION
A (ns)	Intrinsic base delay coefficient (Delay with RFT = K and CL = 0 pF)
B (ns/pF)	Load dependent base delay coefficient
CL (pF)	Total load capacitance at the output of cell under analysis
tpLH (ns)	Base propagation delay time with output rising (low to high)
tpHL (ns)	Base propagation delay time with output falling (high to low)
CIN (pF)	Total capacitance at the input of the cell under analysis, same as the total load capacitance at the output of the driving cell
R1 (ns)	Intrinsic rise time coefficient (with RFT = K and CL = 0)
R2 (ns/pF)	Load dependent rise time coefficient
RT (ns)	Rise time equation (RT = R1 + R2 * CIN)
F1 (ns)	Intrinsic fall time coefficient (with RFT = K and CL = 0)
F2 (ns/pF)	Load dependent fall time coefficient
FT (ns)	Fall time equation (FT = F1 + F2 *CIN)
RFT (ns)	Representation of either rise time or fall time (RFT = RT or FT)
K (ns)	Standard input rise and fall time for cell characterization
max	a function which returns the maximum of two arguments
MCLH	Correction multiplier in tpLH for input rise/fall sensitivity
MCHL	Correction multiplier in tpHL for input rise/fall sensitivity
MC	Representation of either MCLH or MCHL (MC = MCLH or MCHL)
PDF	Derating factor for process variation
TDF	Derating factor for temperature conditions
VDF	Derating factor for voltage conditions
DF	Combined derating factor (DF = PDF * TDF * VDF)
DFn	Combined derating factor for cell under analysis
DFn−1	Combined derating factor for driving cell

General format of the delay equation:

$$\text{Delay} = (A + B * CL) * DFn + MC * \max [0, (RFT * DFn-1 - K)]$$

Timing Calculations for VS1500F Standard Cell and VGX1500 Gate Array Libraries

The Cell Equation

The cell equations describe the node delay from inputs to outputs and the rise and fall times of the outputs. For each output of a library cell there are four response times to a standard pulse on an input to the cell: High-to-low node delay (t_{PHL}), low-to-high node delay (t_{PLH}), rise time (t_r), and fall time (t_f). These four response times can be approximated by linear functions of the capacitive load (C_L) on the output of the cell, giving rise to the following equations:

$$t_{PHL} = t_{PHL0}(@C_L = 0pF) + K_{LH} * C_L$$
$$t_{PLH} = t_{PLH0}(@C_L = 0pF) + K_{HL} * C_L$$
$$t_r = t_{r0}(@C_L = 0pF) + K_r * C_L$$
$$t_f = t_{f0}(@C_L = 0pF) + K_f * C_L$$

The response times are in nanoseconds and C_L is in picofarads. The four times are defined as follows:

t_{PHL}: The time from when a changing input reaches the threshold voltage of the cell to when the falling output reaches the threshold voltage of the cell that it is driving.

t_{PLH}: The time from when a changing input reaches the threshold voltage of the cell to when the rising output reaches the threshold voltage of the cell that it is driving.

t_r: The time from when a rising output reaches its 10% voltage level to when it reaches its 90% voltage level.

t_f: The time from when a falling output reaches its 90% voltage level to when it reaches its 10% voltage level.

The threshold voltage, or trip-point, of a cell is defined as the voltage level at the input required to make the output transition. Unless otherwise stated in the data sheets, the threshold voltage for all cells is at 50% of the V_{DD} supply. Therefore, in most cases, t_{PHL} and t_{PLH} are measured from when the input reaches 50% of V_{DD}. Output pad cells, while still having a threshold voltage of 0.5 V_{DD}, are designed to be TTL compatible and are assumed to drive external circuitry with a 1.4 V threshold voltage. Therefore, t_{PHL} and t_{PLH} for an output cell is measured from when the input reaches 50% of V_{DD} to when the output reaches 1.4 V. Input pads usually drive a cell with a 1.4 V threshold voltage called INBUF which then drives cells with the standard 50% of V_{DD} threshold voltage. Schmitt triggers have two different threshold voltages depending on whether the output is rising or falling. These threshold values are listed in the data sheets. Schmitt triggers are used in place of INBUF with input pads.

Calculating Delays and Transition Times

The cell equations given in the data sheets reflect nominal response times. The nominal environment consists of a 5 volt V_{DD} and 25° C operating temperature. Parameter variation testing was done on a large number of cells to obtain multiplication factors for approximating response time for other than the nominal case. Testing was done on voltage, temperature, and process variation. The multiplication factors for each type of variation in the operating environment are given in Table 9–21. The time response for a cell can be approximated for any combination of voltage, temperature, and process variations given in the table by multiplying the appropriate multiplication factors by the nominal response time derived from the cell equations given in the data sheets.

Parameter	Conditions	Multiplying Factor
Process:		
Worst Case	+ Process Deviation	1.40
Typical Case:		1.00
Best Case	– Process Deviation	0.62
Voltage:		
Worst Case	4.5 V	1.13
Typical Case	5.0 V	1.00
Best Case	5.5 V	0.91
Temperature:		
Worst Case Extended	125°C	1.38
Worst Case Industrial	85°C	1.23
Worst Case Commercial	70°C	1.18
Typical Case	25°C	1.00
Best Case Commercial	0°C	0.92
Best Case Industrial	– 40°C	0.76
Best Case Extended	– 55°C	0.71

TABLE 9–21 Multiplication factors

Simple Outputs

The VLSI Timing Analysis (ViTa) software uses the cell equations in performing a best–, typical–, and worst–case timing analysis on a chip design. For most commercial designers, worst case is defined as 4.5 volts V_{DD}, 70°C, and + process deviation.

ViTa computes the delay on the cells by first computing the total capacitive load on each output. This involves summing the input and tristate capacitances of all connections to each output of each cell. ViTa also adds in an additional capacitance from the interconnects between the cells. Before the chip layout is done, ViTa estimates the interconnect capacitance by adding a 0.05 pF capacitance per connection to the total capacitance. The total estimated capacitive load can be expressed as:

$$C_L = \{\Sigma CAP[cell]\} + Fanout * 0.05\ pF$$

After the chip layout is done, ViTa calculates the real interconnect capacitance from the layout. The calculated capacitive load values are then used in the cell equations to compute the node delays.

Very often the node delays have to be "corrected" to compensate for the shape of the input signal. The cell equations for VS1500F and VGX1500 were derived assuming a library standard rise time of 1.4 ns on the inputs. Inputs rising or falling slower than 1.4 ns will cause additional node delay not accounted for in the t_{PLH} and t_{PHL} equations alone. Therefore, ViTa compensates for this additional node delay by adding a delay proportional to the additional input rise or fall time of the driving gate, if the time is greater than 1.4 ns. This proportionality constant is 0.2. The "corrected" t_{PLH} and t_{PHL} values are given by the following formulas, where t_r and t_f are the rise and fall times calculated using the t_r and t_f equations given in the data sheets.

$t_{PLHC} = t_{PLH} + \max [0, 0.2(t_r - 1.4\ ns)]$
$t_{PHLC} = t_{PHL} + \max [0, 0.2(t_f - 1.4\ ns)]$

t_{PLHC} is the corrected low-to-high node delay and t_{PHLC} is the corrected high-to-low node delay.

*NOTE: The max function states the value chosen is the larger of the two values separated by a comma.

ViTa references cell inputs and outputs by pin number rather than name. So that users can easily cross reference between the ViTa delay file output listing and the data sheets, the inputs and outputs of each cell have been listed on each data sheet in numerical order according to pin number.

Example:

For a 2-input NAND gate (VS1500F), NAN2, the propagation delay and output rise time are calculated using worst-case processing conditions, 4.5V, and 70° C. To calculate this, several bits of information must be gathered.

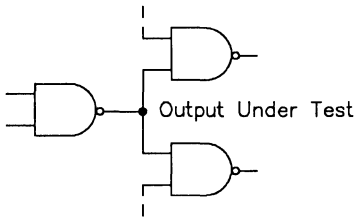


Figure 9-98 NAN2 example

1. The node delay equation given in the data sheet is needed. For the NAN2, the equation for propagation delay low-to-high is:

$t_{PLH} = 0.508 + (1.64 * C_L)$

Note that the delay equations given in the data sheets are at typical conditions.

2. The output rise time equations from the data sheet is needed.

$t_r = 0.565 + (3.63 * C_L)$

As with the node delay equation, the rise time equation is a typical condition.

3. The multiplication factors for the desired conditions are needed. The worst case factor, K_{WC}, combines worst case processing, worst case voltage (4.5 V),and T_A + 70°C. See Table 9-21 for values.

$K_{WC} = 1.40 * 1.13 * 1.18$
$= 1.87$

4. The load capacitance is calculated using the formula:

$C_L = \{\Sigma CAP[cell]\} + Fanout * 0.05\ pF$

The input capacitance of each NAN2 is 0.077 pF (value found on data sheet). The fanout is 2. Therefore, the load capacitance is:

$C_L = (0.072 + 0.072)\ pF + 2 * 0.05\ pF$
$C_L = 0.244\ pF$

t_{PLH} and t_r can now be calculated for the NAN2.

$t_{PLH} = [0.508 + (1.64 * 0.244)] * 1.87$
$t_{PLH} = 1.70\ ns$

$t_r = [0.565 + (3.63 * 0.244)] * 1.87$
$t_r = 2.71\ ns$

The propagation delay value calculated does not take into account the effect of input rise time. To adjust this value, the equation for the compensated value must be used and will give the propagation delay as calculated by the ViTa tools.

$t_{PLHC} = t_{PLH} + \max [0,0.2*(t_r - 1.4\ ns)]$
$t_{PLHC} = 1.70ns + \max [0,0.2*(2.71ns-1.4ns)]$
$t_{PLHC} = 1.96\ ns$

Dependent Outputs

It is sometimes necessary to use a device that has a dependent output, such as the NAN2CII shown in Figure 9-99.

On the data sheet, you can see that three paths are specified: A,B to X, A,B to Y, and X to Y.

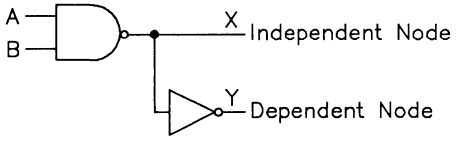


Figure 9-99 Dependent node

To calculate the propagation delay for this device, simply treat it as two separate components, a NAND gate and inverter. The effect of the inverter load is already included in the NAND gate propagation delay equation. Therefore, the propagation delay for A,B to Y is calculated as follows:

t_{PLHC} (A,B to Y) = t_{PHLC} (A,B to X) + t_{PLHC} (X to Y)

t_{PHLC} (A,B to Y) = t_{PLHC} (A,B to X) + t_{PHLC} (X to Y)

Note that alternating senses must be used in these calculations. For example, to calculate the low-to-high delay for A,B to Y use t_{PHL} (A,B to X) and t_{PLH} (X to Y).

Clocked Cell Timing Requirement Definitions

The following sections define the timing requirement parameters specified in each of the clocked cell data sheets. Timing numbers are always specified in each of the clocked cell data sheets. Timing numbers are always given from one edge at its 50% (of V_{DD}) voltage point to another edge at its 50% point. An active edge of a clock pin signifies the edge of a clock input signal that will cause data to propagate to the output pins.

Data Setup Time

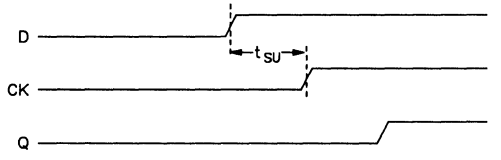


Figure 9–100 Data setup time for DFFP cell

t_{SU} = Minimum time (positive value) before the clocks active edge that data need be stable to propagate that data from data input to output.

The setup time value given for a cell is for propagating worst case data ("1" or "0"). In this diagram for a DFFP cell, a "1" is shown propagating from D to Q.

For latch type cells (LATP, LATRTP, etc.), the setup time is defined as the minimum time before the clock goes from transparent state to latched state that data need be stable such that the desired data is latched and propagated to the output.

Data Hold Time

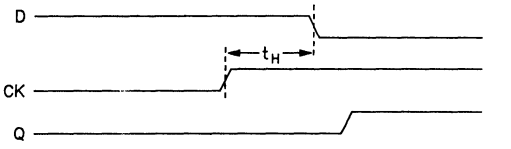


Figure 9–101 Positive hold time for DFFP cell

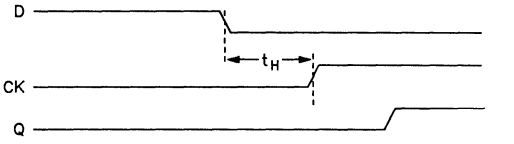


Figure 9–102 Negative hold time for DFFP cell

t_H = Minimum time (positive value) after clocks active edge that data need be stable to propagate data from data input to output.

The hold time value given for a cell is for propagating worst case data ("1" or "0"). In Figure 9–101, a "1" is shown propagating from D to Q. It is important to note that hold time can be a negative value which means that data can switch before the clock active edge and still produce a valid output (Figure 9–102).

For latch type cells (LATP, LATRTP, etc.), hold time is defined as the minimum time after the clock goes from transparent state to latched state that data is stable such that the desired data is latched and propagated to the output.

Minimum Pulse Width

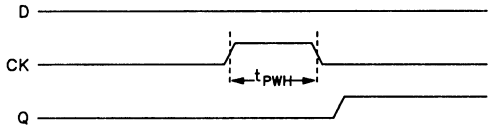


Figure 9–103 Minimum high clock pulse width for DFFP cell

t_{PWH}, t_{PWL} = Minimum pulse width (high or low, respectively) on an input pin that produces the correctly corresponding action on an output pin. An applied pulse smaller than the specified value will cause the output pin to go unknown.

A clock pulse wider than the minimum pulse width specification on a positive edge triggered flip-flop will propagate data from data input to output (Figure 9–103). A high clock pulse wider than the minimum pulse width specification on a latch cell (transparent = high) will latch data from the data input and propagate data to the output. A low reset pulse wider than the minimum pulse width specification on a reset input (active low) will reset the Q output pin.

For a latch cell that is transparent when clock is high, a t_{PWL} for that clock pin is meaningless and is not specified. The same holds true for t_{PWH} on a latch cell that is transparent when clock is low.

All minimum pulse widths are specified given a rise and fall time of 1.75 ns for VS1500F, VGX1500 libraries and 0.5 ns for VS700, VGX700 libraries. Therefore, pulse widths of less than 1.75 ns or 0.5 ns respectively are not specified.

Recovery Time

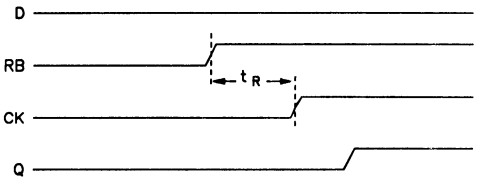


Figure 9–104 Positive reset recovery time for DFFRP cell

t_R = The minimum time (positive value) after an asynchronous pin (Reset, Set, RB, SB, etc.) is disabled that an active clock edge will propagate data from input to output. If the active edge of clock occurs before the specified recovery time, the input data will not propagate.

The example shown in Figure 9–104 is of a DFFRP cell with a positive value recovery time. Figure 9–105 shows a cell with a negative value recovery time. In this case, the clock active edge can occur before the RB pin is disabled and the input data will still propagate to the output. Good design practice would suggest keeping the active clock edge at least the "t_R" time away from any asynchronous pin edge.

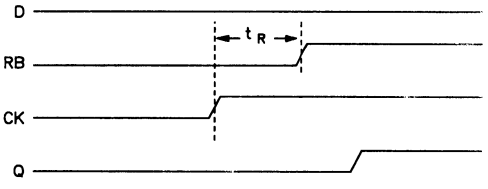


Figure 9–105 Negative reset recovery time for DFFRP cell

D02911MPD